Switched-Tank VCO Designs and Single Crystal Silicon Contour-Mode Disk Resonators for use in Multiband Radio Frequency Sources

Christopher A. Maxey

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Sanjay Raman, Chair
Randy Heflin
G.Q. Lu

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(ABSTRACT)

To support the large growth in wireless devices, such as personal data assistants (PDAs), wireless local area network (WLAN) enabled laptop computers, and intelligent transportation systems (ITS), the FCC allocated three high-frequency bands for unlicensed operation. Of particular interest is the 5-6 GHz Unlicensed National Information Infrastructure (UNII) band intended to support high-speed WLAN applications. The UNII band is further split into three smaller 100 MHz sub-bands: 5.15 - 5.25 GHz; 5.25-5.35 GHz; and 5.725-5.825 GHz.

VCOs that can be switched between each of the three UNII sub-bands offer flexibility and optimum phase-locked loop (PLL) design versus non-switchable VCOs. This work presents switched-tank voltage controlled oscillators (VCOs) designed in Motorola's 0.18 μm HIP6WRF BiCMOS process that could be used in multiband receivers covering the three UNII sub-bands. The first VCO was optimized for low power consumption. The VCO draws a total of 6.75 mA from a 1.8 V supply including buffer amplifiers. The VCO is designed with a switched-capacitor LC tank circuit that can switch to two center frequencies, 5.25 GHz and 5.775 GHz, with 200 MHz of varactor-supplied tuning range. The simulated output voltage swing is 2.0 V peak-to-peak and is kept constant between sub-bands by an active PMOS load integrated into the biasing circuitry. The second VCO was optimized for a high output voltage swing by replacing the current biasing circuit with a degenerating inductor. This design targeted three center frequencies, 5.2 GHz, 5.3 GHz, and 5.775 GHz, with 100 MHz of tuning range. This design has an output peak-to-peak voltage swing of 5.2 V but consumes an average of 16.5 mA from a 1.8 V supply. The two fabricated circuits exhibit tuning ranges similar to the simulated results; however, the center frequencies of each decrease due to interconnect parasitics there were unaccounted for in the designs. The measured center frequencies are 4.4 GHz and 5.37 GHz for

the first design, and 4.4 GHz and 4.7 GHz for the second design (with one state inoperative due to a faulty switch).

The phase noise of the fabricated VCO designs was limited primarily by the low quality factor (Q-factor) of the on-chip LC tank circuits. Oscillators referenced with high-Q off-chip components such as quartz crystal references and surface acoustic wave (SAW) resonators in a PLL can exhibit much improved performance; however, these off-chip components add packaging/assembly cost and higher bill of materials, impedance matching issues, and parasitics that can significantly affect performance for RF applications. Thus, there is tremendous incentive for integrating high-Q components on-chip with the eventual goal of consolidating all of the RF/analog/digital components onto a single wireless-enabled chip, commonly called RF system-on-a-chip (SoC).

Microelectromechanical (MEM) resonators have received significant attention based on their ability to provide high on-chip Q-factors at RF frequencies using fabrication techniques that are compatible with modern IC processes. MEM resonators transduce electrical signals into extremely low-loss mechanical vibration and vice versa. Consequently, this thesis also describes the modeling, simulation, and fabrication of contour-mode disk-shaped MEM resonators. This resonator geometry is capable of providing high-Q oscillation at frequencies exceeding 1 GHz at sizes easily within the limits of modern photolithography techniques. Finite element analysis is used to predict the frequency response of disk resonators under various operating conditions and to determine variables that are most critical to the resonator design. A silicon-on-insulator (SOI) fabrication process for constructing the disk is also discussed. Finally, the possible future integration of MEM resonators with multiband VCOs in a common IC process is proposed.

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Chapter 1

Introduction

One of the primary focuses for research and development in the area of radio frequency (RF) wireless communications electronics has been device miniaturization. Miniaturization offers many advantages, such as enhanced mobility, reduced cost and improved form factors. Cellular phones, for example, have been transformed over the past half decade from bulky and inconvenient handset units requiring large batteries into small, multifunctional personal communicators that weigh only a few ounces and can operate for days on a relatively small battery before recharging.

The principal technological advancement that has enabled such miniaturization is *integration*. Traditionally, RF communications transceivers have been realized with discrete components and large-scale integrated (LSI) circuit chips interconnected at the board level. However, these components are now being integrated together into single integrated circuit (IC) chips that dramatically decrease the size of the transceiver section. The corresponding reduction in off-chip component count also leads to lower packaging and handling costs, and the elimination of board-level interconnect parasitics that can significantly affect performance for high-frequency applications. Integrating multiple functional components into a single chip also eliminates the need to match the terminations of each component to a specific impedance, such as the traditional 50 Ω. Thus, there is tremendous incentive for developing complex mixed RF/analog/digital ICs for wireless applications, now referred to as RF system-on-a-chip (SoC) [1].

Although there have been significant strides made in the area of RF SoC, there

Band Name		Frequency Range	Application	
ISM		2.4 - 2.5 GHz	802.11b & g (11 & 54 Mbps WLAN), Bluetooth	
UNII	A	5.15 - 5.25 GHz	50 mW Max	802.11a (54 Mbps WLAN)
	B	5.25 - 5.35 GHz	250 mW max	
	C	5.725 - 5.825 GHz	1 W max (outdoor)	
UWB		3.1 - 10.6 GHz	802.15.3a (Proposed 480 Mbps WLAN)	

Table 1.1: Summary of unlicensed frequency band allocations for high speed data networks.

still remain a number of barriers to true single-chip wireless transceivers. Most notable is the lack of high quality-factor (Q-factor) passive components in even the most advanced integrated circuit processes. Off-chip high-Q components can exhibit Q-factors on the order of 10,000, while state-of-the-art on-chip passive components typically only offer Q-factors of 100 or less. RF wireless transceivers require high-Q elements for resonator and filtering functions. This chapter presents the challenges associated with the integration of such high-Q components, and introduces various solutions including the integration of microelectromechanical (MEM) resonators, a topic that will be detailed in subsequent chapters.

The reduction in the size of wireless transceivers has enabled their incorporation into watches, personal digital assistants (PDAs), and laptop wireless local area network (WLAN) cards. A consequence of this rapid growth of wireless-enabled electronics is a severe crowding of the frequency spectrum below $\sim$2.5 GHz. In response to this crowding, the Federal Communications Commission (FCC) allocated three frequency bands for unlicensed operation: the Industrial, Scientific, and Medical (ISM) band; the Unlicensed National Information Infrastructure (UNII) band; and the ultra-wideband (UWB) frequency range[1]. Table 1.1 summarizes the three bands and their respective applications.

To access the various available networks, a transceiver must now be able to switch quickly and reliably between different frequency bands. The first part of this thesis describes the design and fabrication of a prototype Voltage Controlled Oscillator (VCO) for a multi-band transceiver that can tune over the three sections of the UNII band. The second part of this thesis deals with the development of RF micro-

[1]Any number of handsets or base stations can operate in unlicensed bands without prior FCC approval. However, the devices must adhere to certain regulations governing maximum transmitted power, mutual interference, etc.

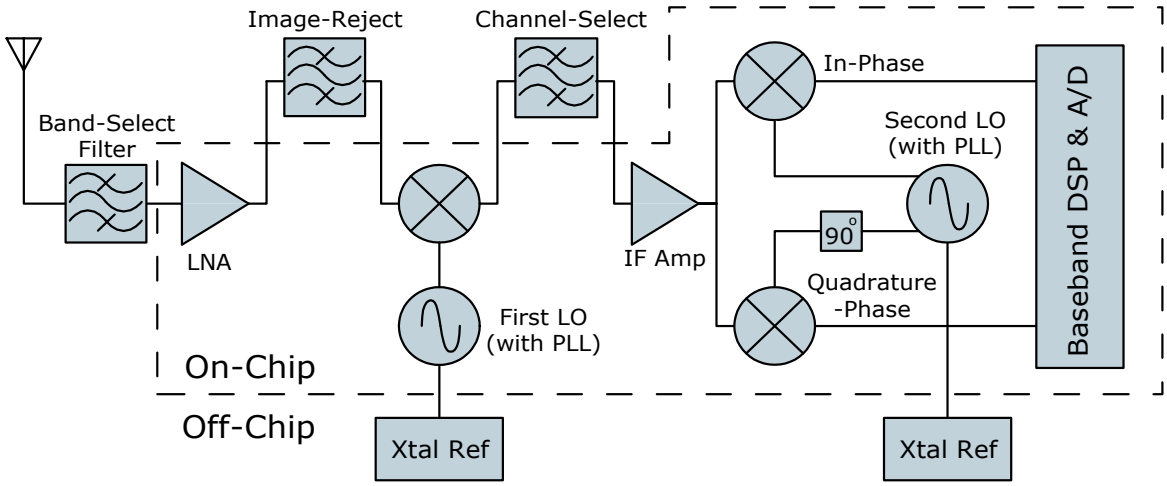


Figure 1.1: Simplified superheterodyne receiver architecture (after [2]).

electromechanical (MEM) resonators suitable for use in multi-band RF receivers.

1.1 Modern RF Receiver Architectures: Off-Chip Component Requirements

The traditional approach for RF wireless receivers has been the superheterodyne architecture shown in Figure 1.1 [2]. Most of the subcircuits, including the amplifiers, mixers, and oscillators, are now generally amenable to integration. On the other hand, the band-select, image-reject, and channel-select filters, as well as the stable crystal oscillator references, typically require substantially higher Q-factors than what is achievable on-chip in standard IC processes[2]. High-Q components, which are currently realized using off-chip surface acoustic (SAW), ceramic, or quartz piezoelectric devices, can offer Q-factors of 10,000 or greater [3]. On the other hand, on-chip realizations using monolithic inductors and capacitors would typically have Q-factors three orders of magnitude lower.

SAW filters and quartz crystal frequency references are piezoelectric devices. The

[2] Actual receivers may incorporate more than two mixing stages, and some approaches may not require I and Q downconversion as shown in Figure 1.1; however, the challenges to on-chip integration are the same nonetheless.

piezoelectric effect is an inherent physical property found in quartz (SiO_2) and various other materials. Applying tensile or compressive stress on the crystal lattices of these materials causes positive and negative electric charges to accumulate on opposing surface of the crystal. Likewise, an externally applied voltage will generate stress that consequently mechanically deforms the crystal lattice. If the applied voltage is periodic, the crystal will vibrate slightly at the frequency of excitation. At very specific resonant frequencies defined by the shape and cut of the quartz crystal, these vibrations can be significant enough to cause acoustic waves to propagate through the crystal lattice.

Figure 1.2(a) shows the cross section of a thickness-shear bulk mode quartz crystal resonator. Typically, two electrodes are deposited onto opposing surfaces of the crystal. One electrode is driven with the excitation signal which causes the crystal to vibrate. The resulting acoustic waves travel across the crystal and are transduced into an electric signal at the opposite output electrode. Since the crystal is inherently very low-loss for the acoustic wave, signals traversing the device will suffer little degradation or added noise. These properties make quartz piezoelectric devices very attractive for use as resonators and filters in RF subsystems.

Quartz crystals operating in the bulk thickness mode have physically-defined limits on their potential resonant frequencies. At resonance, an odd-number of acoustic wave half-wavelengths must fit inside the thickness plane of the crystal. At the fundamental frequency, a single half wavelength can be confined between the bottom and top electrode. Thus, the crystal thickness is the primary resonant frequency-determining parameter, i.e. the thinner the crystal, the higher the frequency. At frequencies above 30 MHz the required crystal dimensions for fundamental operation are too thin to be practical and odd harmonics, or overtones, of the fundamental resonant frequency are typically excited in the crystal to achieve higher frequencies. Even at the 9^{th} overtone, the normal limit for such harmonic excitation, the maximum resonant frequency is approximately only 250 MHz.

To circumvent the frequency limits of the thickness-mode devices, piezoelectric quartz is often incorporated into surface acoustic wave (SAW) devices [Figure 1.2(b)]. In the SAW device, the electrodes are patterned on one side of the quartz crystal and the acoustic wave travels along the surface of the quartz, between the electrodes. The frequency is now determined by the distance between the electrodes, not by

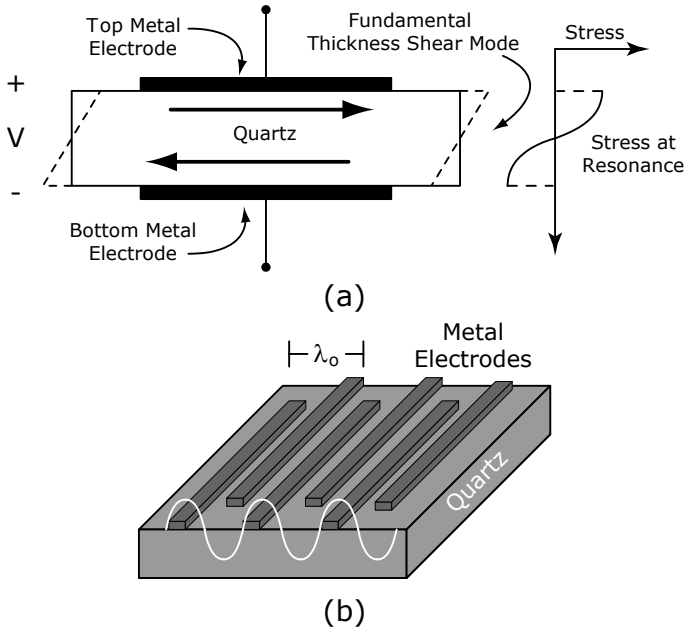


Figure 1.2: Piezoelectric devices: (a) Cross section of a bulk thickness-shear mode quartz crystal resonator; (b) surface acoustic wave (SAW) resonator.

the thickness of the quartz. Modern electrode deposition technology is capable of fabricating SAW devices that operate close to 2.5 GHz. However, the temperature stability and long-term frequency stability are worse in the SAW device compared to the bulk-mode resonator, and high precision applications such as RF local oscillators still require the use of the bulk-mode device [4].

Unfortunately, crystalline quartz cannot be easily integrated on-chip along with other RF circuitry due to the processing steps needed to properly grow the crystal. Piezoelectricity for the types of quartz used in RF resonators only occurs for specific crystal orientations that must be cut from a large starter crystal. Attempts at integrating SAW devices on chip typically involve bonding precut quartz blanks onto a processed Si wafer and patterning interconnects [5]. The bonding process adds cost and potential damage to devices fabricated on the Si wafer. Thus, there has been recent focus on piezoelectric films such as ZnO or AlN that can be deposited on silicon substrates using reactive magnetron sputtering, a deposition technique compatible with CMOS and BiCMOS processing. SAW-type resonators fabricated using ZnO [6] and bulk

acoustic wave (BAW)[3] resonators fabricated in AlN [7] have exhibited GHz-range vibrational frequencies and Q-factors above 1,000. However, these materials are also not standard IC materials and typically many additional lithography steps are required to fabricate the resonator devices. Additionally, the deposition quality and thicknesses of these materials must be very accurately controlled in order to guarantee low-loss piezoelectric operation. The added steps and required control can significantly increase the cost to fabricate the chip. In order to achieve the goal of a low-cost, truly single-chip integrated radio, either the need for high-Q resonator components must be eliminated, or an on-chip resonator solution more compatible with standard IC processing must be found. The remainder of this section focuses on the various off-chip components in RF transceivers and approaches to integrating them on-chip.

1.1.1 Band-Select, Channel-Select, and Image-Reject Filters

Q-Factor and the Band-Select Filter

The Q-factor of a resonating element can be most generally defined as:

$$Q = 2\pi \cdot \frac{E_S}{E_D}, \tag{1.1}$$

where E_S is the energy stored by the device and E_D is energy dissipated by the device in the same cycle. Filters are often constructed by cascading resonating elements in a ladder configuration as shown in Figure 1.3. In simple terms, the number of cascaded elements, or poles, determines the sharpness or selectivity of the filter, i.e. the ratio of passband transmission to out-of-band rejection will increase as the number of poles are increased. In reality, each resonant element will have some non-zero loss associated with it resulting in a finite Q-factor. Therefore, increasing the number of finite-Q poles has the undesired effect of increasing insertion loss, i.e. decreasing the filtered signal transmission in the passband.

Figure 1.4 shows how low Q-factors can adversely affect the passband transmission

[3] On-chip BAW resonators operate similarly to that of bulk-mode quartz resonators in that an acoustic wave is excited across the thickness of a piezoelectric material.

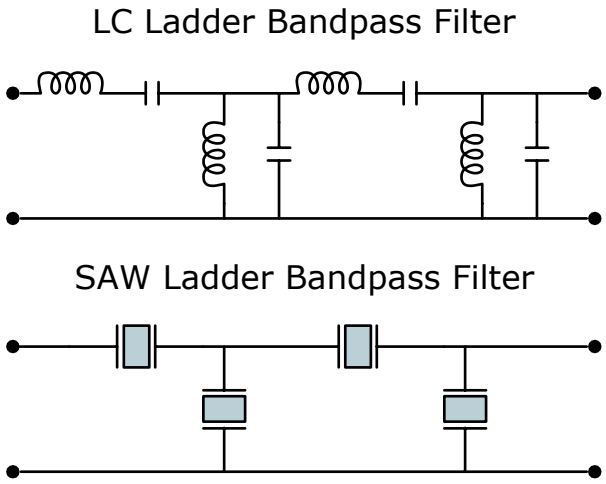


Figure 1.3: Configurations for LC and SAW-based bandpass ladder filters.

for a 4^{th} order Chebyshev filter designed as a band-select filter for the lowest division of the UNII band (5.15 - 5.25 GHz). Q-factors as high as 10,000 are required if the loss in the passband is to be kept to a reasonable level ($\leq$ 1 dB). (The insertion loss of the filter simulated in Figure 1.4 is approximately 11 dB for Q=100 and 0.12 dB for Q=10000.)

The band-select filter is the first component of the transceiver seen by the incoming signal after the antenna, and since it is a passive component, its noise figure (NF) is approximately equal to the insertion loss of the filter in the band of interest. It is well-known that the first element in the receive chain is the most critical in determining the overall NF of the system. Therefore, in order to reduce the overall system NF the band-select filter loss must be reduced as much as possible. Modern IC inductors tend to have Q-factors in the range of 10-50 depending on their size, frequency of operation, etc., meaning that any band-select filter designed using such low-Q on-chip passive components would be prohibitively lossy (e.g. total NF close to 65 dB as shown in Figure 1.4). Currently, only off-chip components can provide the Q-factor necessary for sufficiently low-loss filters.

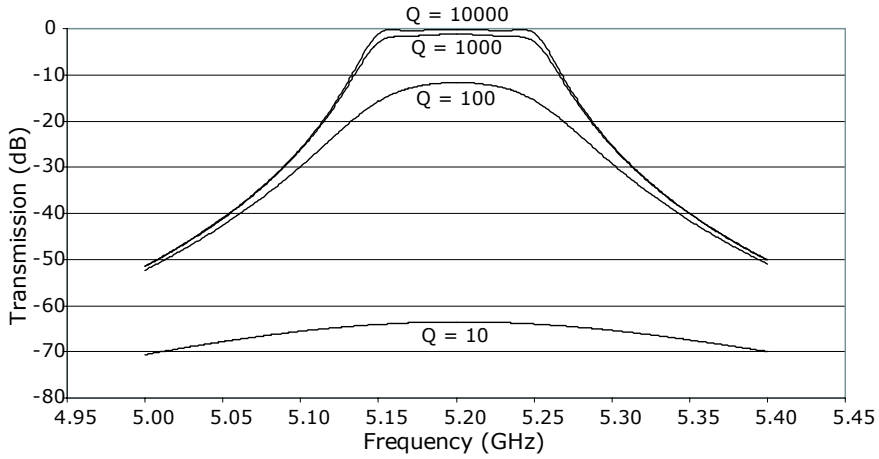


Figure 1.4: Transmission (dB) versus frequency for a 4^{th} order LC Chebyshev filter with various values for inductor Q.

Channel-Select Filter

The channel select filter is designed to distinguish desired signals from any other in-band signals that may have been received by the antenna. Since these channels could be closely spaced in frequency, the fractional bandwidth of this filter must be very small and the filter rolloff must be very sharp. Small fractional bandwidths with high selectivity require more filter poles and therefore the individual resonator Q-factors must be very high to avoid significant signal degradation.

The superheterodyne architecture attempts to relax the Q-requirements of the channel-select filter by first lowering the center frequency, f_o, of the desired spectrum using a mixing stage. It is well-known that the selectivity of a filter with a given Q-factor will increase as the center-frequency of the filter is decreased. Therefore, fewer poles can be used at a lower center frequency reducing the filter insertion loss. The resulting downconverted signal, called the intermediate frequency (IF), is then filtered by the channel-select filter before being mixed down again to low frequency baseband where demodulation occurs. While the resonator Q-factors needed are still typically too high for current on-chip solutions, the cost and complexity of the channel-select filter is significantly reduced in this architecture. On the other hand, this mixing process inherently makes the superheterodyne vulnerable to information corruption from interference at the *image frequency*.

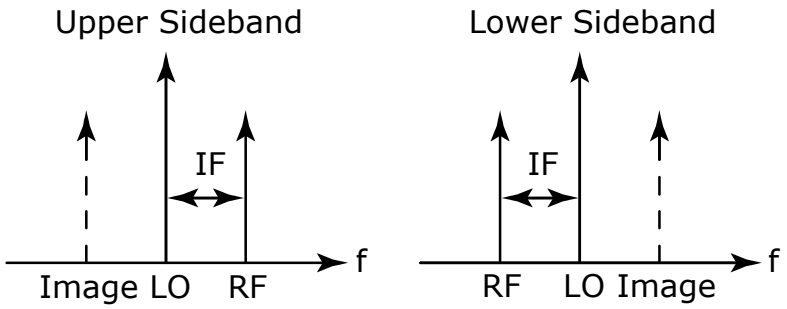


Figure 1.5: Comparison of USB and LSB spectra.

Image-Reject Filter

The image frequency is defined as the frequency of an in-band interferer which mixes to the same intermediate frequency as the desired signal for a given local oscillator (LO) frequency. Mathematically, the image frequency can be found from the following equations:

$$f_{image_LSB} = f_{signal} + 2f_{IF}, \tag{1.2}$$

$$f_{image_USB} = f_{signal} - 2f_{IF,} \tag{1.3}$$

where f_{image_LSB} is the image frequency for a lower sideband (LSB) RF signal, f_{image_USB} is the image frequency for an upper sideband (USB) RF signal, and f_{IF} is defined by:

$$f_{IF} = |f_{LO} - f_{signal}|\,. \tag{1.4}$$

Figure 1.5 compares the USB and LSB spectra.

Since the power or information content of an interferer at the image frequency cannot be predicted, it is critical that the image be sufficiently attenuated before it reaches the first mixing stage to prevent signals at the image frequency from swamping out the desired information after downconversion. This is typically accomplished using an image-reject filter located after the LNA (Figure 1.1). The Q required for the image-reject filter depends largely on the value of the IF. Figure 1.6 shows the relationship between the IF frequency selection and image attenuation for a given image-reject filter selectivity.

By choosing a high value for the IF, the resonator Q-factor requirements for the image-

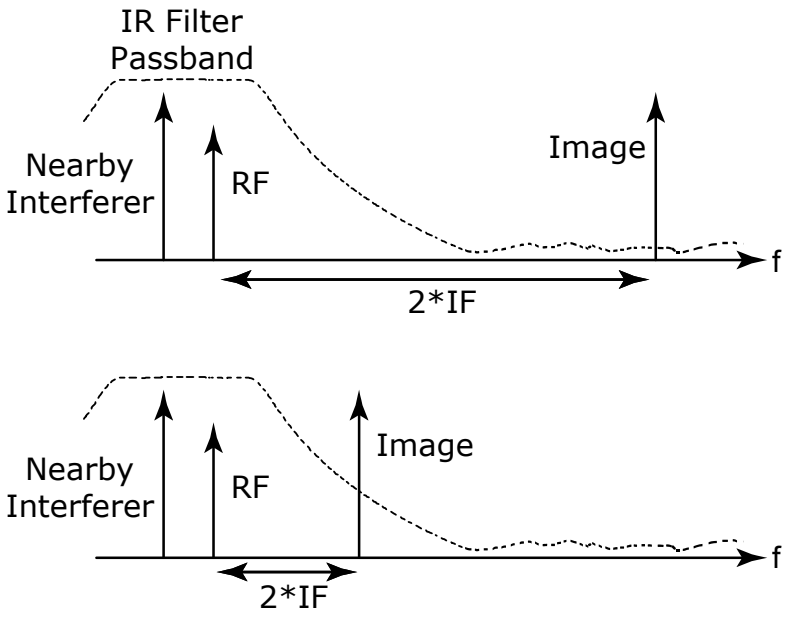


Figure 1.6: Relationship between IF frequency selection and image attenuation for a given image-reject filter selectivity (after [2]).

reject filter can be relaxed since fewer poles are needed to sufficiently attenuate the image frequency. Lower values of IF require steeper filter rolloffs to obtain the same rejection as the high IF case and thus require more poles and higher Q resonators. Meanwhile, the purpose of the superheterodyne architecture is to lower the center frequency and thus the required Q-factor of the channel-select filter. Therefore, there is a fundamental design trade-off with superheterodyne receivers between sensitivity (high IF, high image-rejection but decreased channel selectivity) and selectivity (low IF, low image-rejection but increased channel selectivity). In either case, however, the resonator Q-factors required for low filter insertion loss exceed those currently available on chip and are realized using off-chip solutions. For this reason, the heterodyne architecture cannot be fully integrated as indicated in Figure 1.1. Therefore, two alternative architectures have recently become popular since they can obviate requirements for an image-reject filter and allow the possibility of low-frequency channel selection using integrated active filters or digital signal processing (DSP).

Direct Conversion Receivers In principle, a straightforward solution to the image frequency problem is to collapse the multiple mixing stages of the superheterodyne

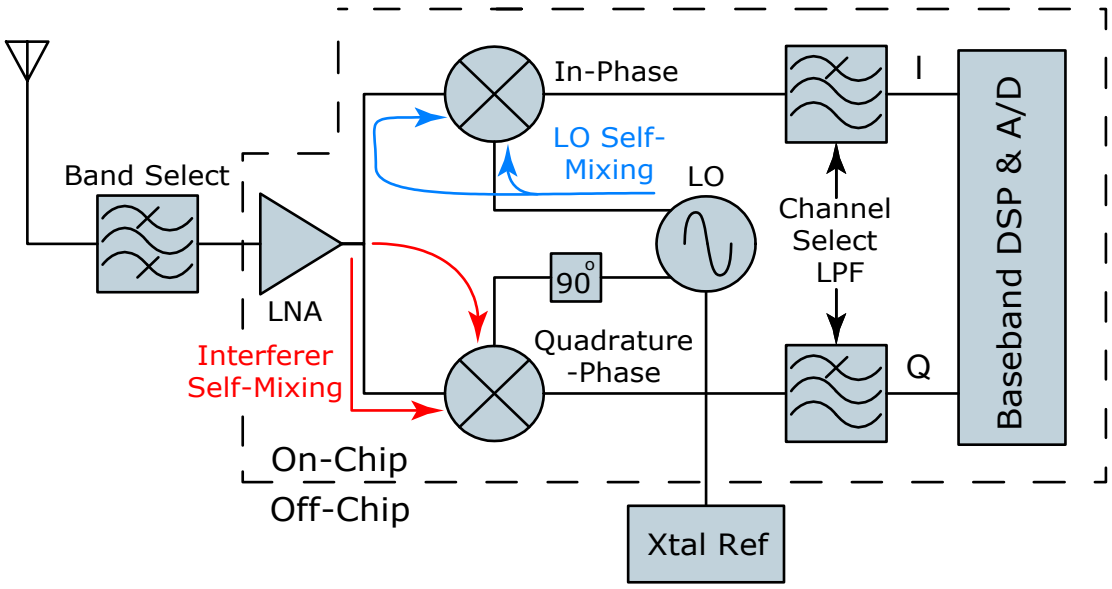


Figure 1.7: Simplified direct conversion receiver architecture showing leakage paths that can lead to DC offset generation.

architecture into a single stage of mixing. If the LO for this mixing stage is set to be exactly the RF frequency of interest, the desired information spectrum is directly mixed down to baseband for subsequent demodulation. The *direct-conversion,* or *zero-IF*, receiver is the realization of this idea; a simplified schematic is shown in Figure 1.7. I and Q channels are required to provide discrimination between positive and negative spectra around the zero IF. As is evident in Figure 1.7, the direct conversion receiver (DCR) achieves a significant reduction in off-chip component count, resulting in a substantial cost advantage over the superheterodyne approach. Since the LO and the signal frequency are identical in the direct-conversion case, Equations 1.2 and 1.3 combine with Equation 1.4 to yield an image frequency identical to the signal frequency; therefore an image-reject filter becomes unnecessary. The channel-select filters are then implemented as low-pass filters that can be fabricated on-chip using an active, operational amplifier-based design; alternatively, the filtering can be performed in the digital domain after analog-to-digital conversion. There are, of course, non-trivial issues with the DCR, the most damaging of which is the possibility of LO and interferer self-mixing (Figure 1.7) [2].

In the case of LO self-mixing, finite, albeit highly attenuated, leakage from the local

oscillator to the high-frequency input of the mixer can be reflected off of components that precede the mixer, such as the LNA or the antenna input port. This reflected signal is at the same center frequency as the desired spectrum and thus will also be downconverted to zero frequency. Information at or very close to zero frequency can be consequently corrupted by the self-mixing component. Strong interferers may also leak through substrate coupling or other mechanisms to the LO port of the mixer and can then themselves self-mix down to zero frequency in a process called interferer self-mixing. Despite the possibility of information corruption at DC, a great deal of research and development has been devoted to the DCR and it has found practical application in wireless products such as pagers, local area network (LAN) systems, and cellular telephones [8–11].

Low-IF Receivers In the Low-IF receiver (Figure 1.8), the incoming signal is downconverted to an intermediate frequency very close to, but not exactly at zero. This frequency is chosen to be low enough that the information can be processed by available low-power analog-to-digital converters, so a second downconversion stage is not explicitly required (i.e. this processing can be performed in the digital domain). The problem of self-mixing is eliminated because the desired spectrum is no longer converted to exactly DC by the mixing process and any self-mixing products fall outside of the IF band. Of course, the image problem reappears in this scenario, so the Low-IF receiver must incorporate some sort of on-chip image cancellation without the use of an RF image-reject filter if it is to be a viable candidate for integration. Most Low-IF receivers utilize either a Hartley or a Weaver architecture as described in [12–14]. Fundamentally, the Hartley and Weaver receivers process the image and the signal frequency in the I and Q channels differently; Figure 1.8 outlines this process for the Weaver architecture. When the two independently processed channels are subtracted from one another, the image is eliminated and the desired frequency is amplified.

Although the problem of self-mixing is mitigated, the Low-IF architecture is extremely sensitive to I and Q channel mismatches. If the I and Q channels of the Low-IF differ in phase by as little one degree, the ability to reject the image frequency is severely compromised. Several avenues of research are being conducted to address the I/Q mismatch problem in such receivers [15–17].

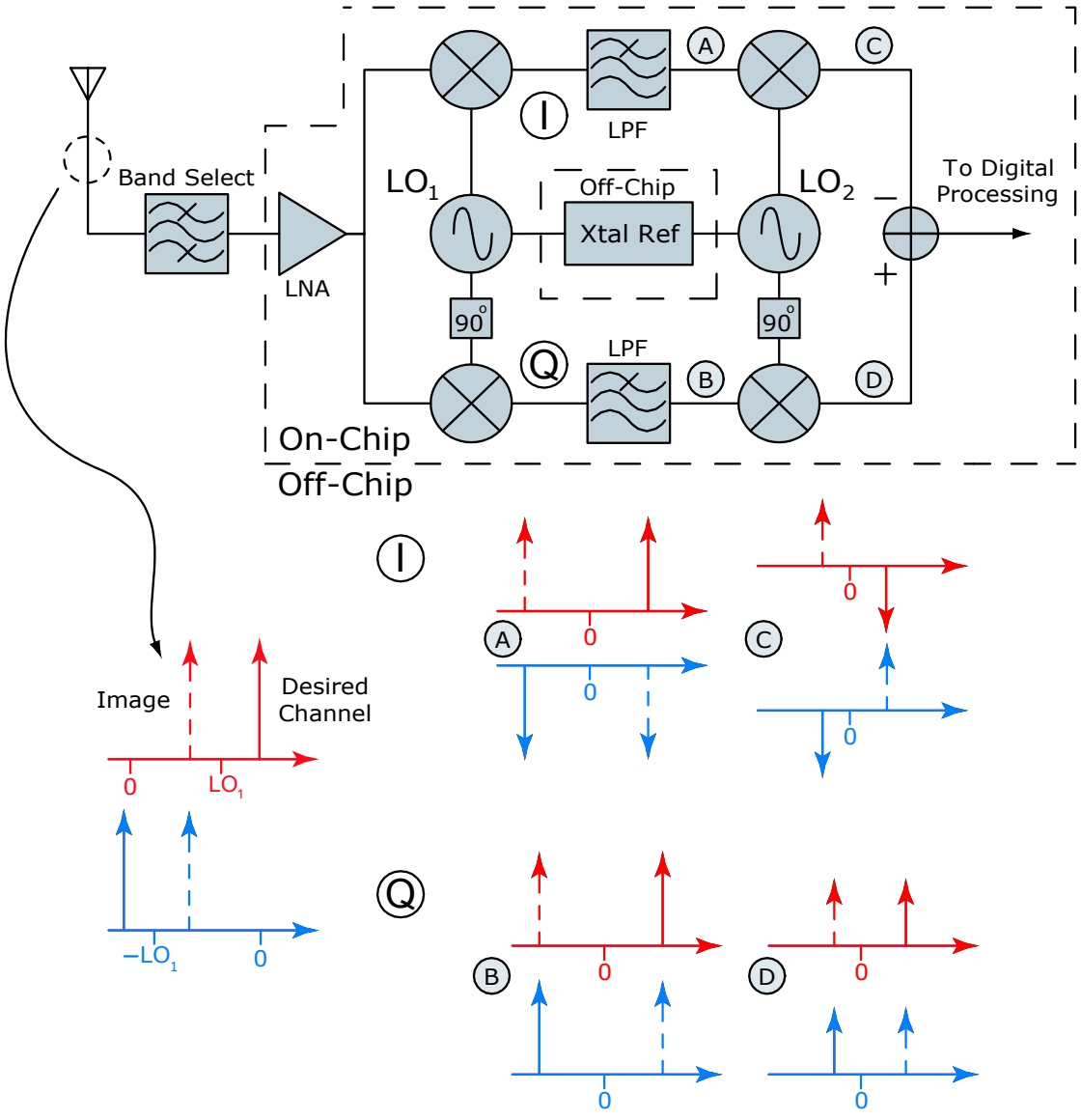


Figure 1.8: Simplified Low-IF receiver based on the Weaver configuration.

The work of this thesis focuses on the development of highly integrated "single-chip" multi-band RF transceivers. As discussed above, the image-reject and channel-select filters can be replaced either through on-chip implementations or through architectural changes such that the remaining off-chip components are the band-select filter and the crystal frequency reference. The band-select filter has been briefly introduced above while the crystal frequency reference is the focus of the next section.

1.1.2 Crystal Frequency References

Modern narrowband transceivers require ultra-stable frequency references, e.g. quartz crystal resonators, to operate properly. Crystal referenced oscillators are critical components in phase-locked loop (PLL) circuits used to generate precise frequency signals used for RF-range local oscillators.

Crystal Referenced Oscillators

The simple feedback oscillator shown in Figure 1.9 consists of a source of signal amplification and a resonator provided by either an off-chip crystal or an on-chip inductor/capacitor (L/C) tank circuit. The transfer function of the loop in Figure 1.9 is:

$$H(j\omega) = \frac{Output}{Input} = \frac{A(j\omega)}{1 - A(j\omega)B(j\omega)}, \tag{1.5}$$

where A is the gain of the forward amplifier and B is the gain (or loss) of the resonant circuit in the feedback loop. Two conditions, called the Barkhausen criterion, can be inferred from this transfer equation which will result in the feedback loop becoming unstable or oscillatory. First, the total phase shift around the loop must be an integer multiple of 360 degrees at the oscillation frequency, i.e. the product of A and B must be positive. This can be accomplished through a 0 degree phase shift from the amplifier and the fact that the resonating element appears purely resistive (0 degree phase shift) at its natural frequency; combined, these two phase shifts are equivalent to a total shift of 360 degrees. Second, the magnitude of total gain around the loop must be equal to or greater than one ($|AB| \geq 1$) at the oscillation frequency. This simply means that the amplifier must at least compensate for the loss contributed by

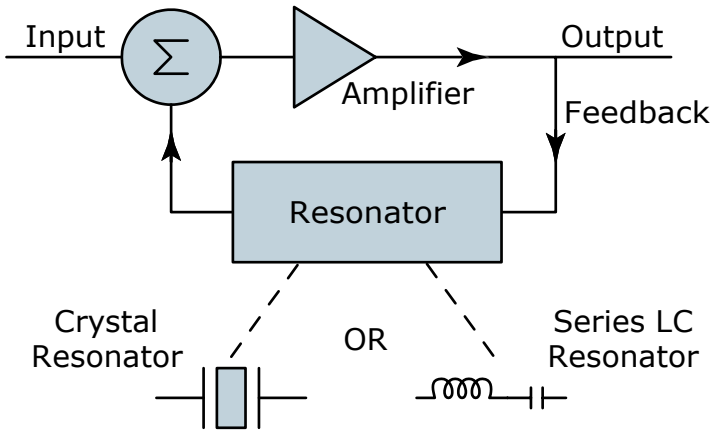


Figure 1.9: High-level diagram of a feedback oscillator.

the resonant element. If these conditions are met, the result is continuously growing output. Since an infinitely-growing output is obviously impossible, the circuit output will be limited by some other mechanism, typically the DC supply rail voltages.

Just as the insertion loss of the filters discussed in Section 1.1.1 is determined by the resonator Q-factors, the loss of an oscillator resonator is also quantified by its Q-factor. The greater the loss in the resonator, the more amplification is required to achieve self-sustaining oscillation. The Q-factor for a resonator can be shown to be:

$$Q = \frac{f_o}{BW}, \tag{1.6}$$

where f_o is the center frequency of the resonator and where BW is the half-power (-3dB) bandwidth of the one-port reflection coefficient of the resonator [18]. As shown by Equation 1.6, for a given resonant frequency, a lower Q oscillator will result in a larger fractional BW meaning that the oscillator frequency can more easily drift from the desired f_o. This manifests itself as *phase noise*, which will be discussed further in Chapter 2.

A simple electrical model of a quartz crystal resonator is shown in Figure 1.10. The series resistor represents the resonator loss and is typically less than 100 Ω in value. The package capacitance is a physical capacitance derived from the external leads and electrodes and does not factor into the primary series resonant frequency of the crystal. The energy storage is represented by the equivalent inductor and capacitor which

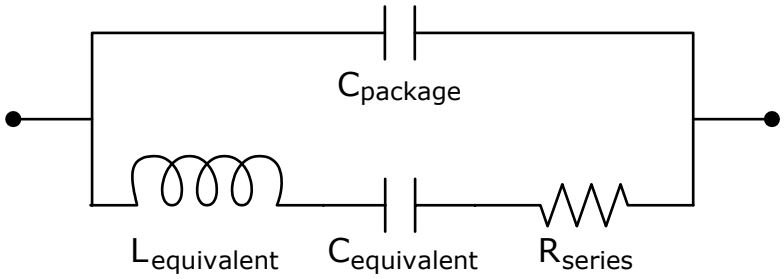


Figure 1.10: Crystal resonator equivalent circuit.

typically range in value between 1-10 Henries and 1-10 femto-Farads respectively [3]. Resonator Q can also be defined as:

$$Q = \frac{X}{R}, \tag{1.7}$$

where X is the reactance of the element and R is the loss of the element. Therefore, it is evident that a high reactance to loss ratio of the crystal leads to its high Q values, typically ranging between ten thousand and several hundred thousand[4]. These high Q-factors make crystals ideal for use in low phase noise ultra-stable oscillators.

As discussed previously, high-quality bulk-mode quartz resonators have a frequency limit of around 250 MHz. However, multi-band RF transceivers must operate in the GHz regime if they are to take advantage of bands such as those summarized in Table 1.1. On-chip LC resonant circuits can produce these high frequency oscillations, but they have significantly lower Q-factors. A control circuit known as a PLL is typically used to merge the high frequency capability of on-chip oscillators with the exceptionally high Q-factor of off-chip, crystal-based oscillators.

1.1.3 Phase-Locked Loops

A typical PLL is shown in Figure 1.11. The operation of the PLL depends on a crystal-referenced oscillator as described in detail in the previous section. This oscillator produces an ultra-stable sinusoidal waveform that is used as the reference

[4]The inherent Q-factor of quartz at 1 MHz can be as high as 10 million, however, the crystal cuts used and the electrode geometries used to excite the acoustic waves typically limit the useable Q-factor to a few hundred thousand.

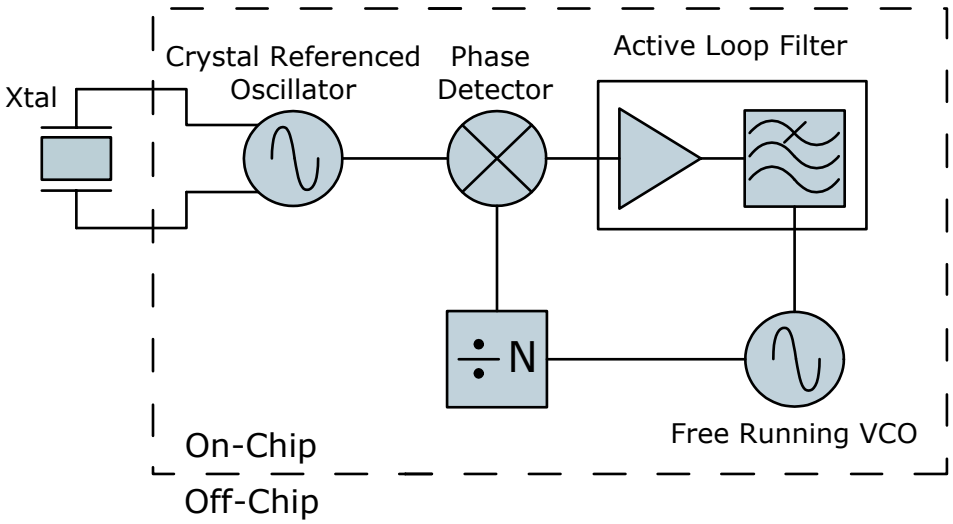


Figure 1.11: High level diagram of a phase-locked loop.

frequency for the PLL. (The reference oscillators are often temperature compensated so as to provide an accurate and stable reference over a wide range of operating conditions [19].) There is also a higher frequency oscillator in the PLL that is normally fabricated on-chip with an LC tank resonator in place of the crystal. This second oscillator is almost always a voltage-controlled oscillator (VCO).

Voltage Controlled Oscillators and the -G_m Topology

While Figure 1.9 gives a good overview of oscillator operation from a control systems point-of-view, it does not provide details on the specific oscillator topology chosen for this work. The VCOs designed for this thesis can be categorized as negative transconductance (-G_m) oscillators. Figure 1.12 is a high-level diagram of the -G_m oscillator that highlights the two main components: the resonant tank circuit and the active -G_m circuit.

On-Chip LC Tank Circuit Recall that the first Barkhausen criteria states that the phase shift around the feedback path must approximately equal an integer multiple of 360 degrees. At resonance, the impedance of the parallel tank circuit in Figure 1.12 is equal to the value of the equivalent resistance, R_{eq}. Since purely resistive circuits present no phase shift (and assuming no phase shift through the amplifier),

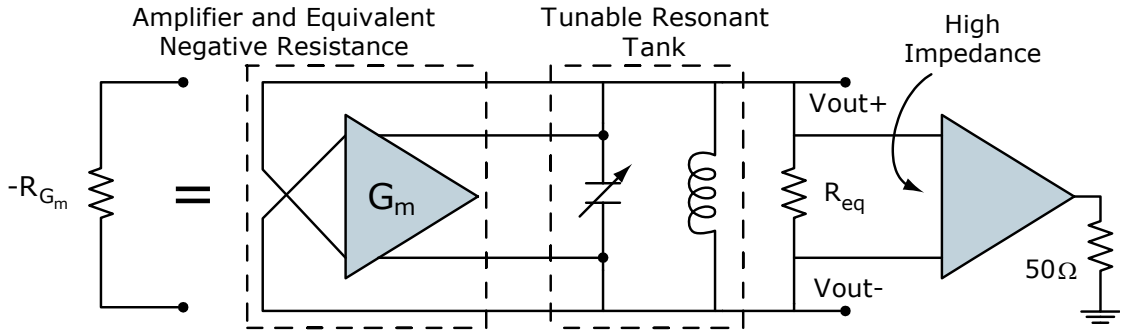


Figure 1.12: High-level diagram of the -Gm oscillator core, tank circuit, and buffer amplifier.

the Barkhausen criterion for loop oscillation is satisfied for the resonant frequency of the tank, given by:

$$f_o = \frac{1}{2\pi\sqrt{LC}}. \tag{1.8}$$

Typically, on-chip VCO tank circuits are fabricated with a monolithic planar inductor and a varactor. The inductor is normally the greatest source of loss for the tank circuit and is responsible for a significant fraction of the total phase noise of the oscillator. Chapter 2 describes the impact of the inductor loss on the phase noise and methods to mitigate its effects. Varactors supply the capacitive reactance of the tank and the majority of its tuning capability. Varactors are devices that exhibit a voltage dependant capacitance. By controlling this capacitance via an external voltage control line, the center frequency, f_o, of the oscillator can be shifted according to Equation 1.8. Therefore, the PLL can stabilize and lock the VCO to the frequency of the crystal referenced oscillator.

-Gm Amplifier The second Barkhausen criteria states that the magnitude of the gain-loss product around the feedback loop of the oscillator must exceed one. To calculate this product, the amplifier is normally considered to be a transconducting amplifier with a gain factor defined by:

$$G_m = \frac{i_o}{v_i}, \tag{1.9}$$

where G_m is the transconductance in Siemens, i_o is the amplifier output current, and v_i is the input voltage for the amplifier. G_m depends largely on the bias point of the active devices and on the input signal level, but, for the purposes of this general

discussion, Equation 1.9 is sufficient. The impedance seen by the tank circuit looking back into the amplifier block can be approximated by:

$$R_{G_m} = -\frac{1}{G_m}. \tag{1.10}$$

This negative resistance must offset the loss of the LC resonant tank to satisfy the second Barkhausen criterion, i.e. the magnitude of the negative resistance of the amplifier must be *less than* or equal to the positive parallel equivalent resistance presented by the tank[5]. This condition will result in oscillation in the feedback loop at the resonant frequency of the LC tank. Ideally, the loss resistance and amplifier gain would exactly cancel so as to produce oscillation with a minimum of excess power consumption. In reality, there must be some additional safety factor to ensure that the gain does not drop below some critical value for the circuit to continue to oscillate. This safety or *startup factor*, α, can be defined as:

$$\alpha = \frac{R_{G_m}}{R_{eq}}, \tag{1.11}$$

where α is typically chosen to be around 2 [20].

When connected to the VCO, the low (typically 50 Ω) input impedance of most measurement equipment and other on-chip circuits can significantly lower the equivalent resistance, R_{eq}, of the tank circuit, thus requiring more gain from the -G_m amplifier to sustain oscillations. For this reason, an impedance buffer amplifier is normally placed between the output of the VCO and the 50 Ω load as shown in Figure 1.12. This buffer is designed to transform the 50 Ω into a high impedance so as to reduce the loading effect on R_{eq}.

Phase-Frequency Detector

The phase detector closes the feedback loop of the PLL and is responsible for comparing the phases and frequencies of the VCO and the stable reference oscillator.

[5] This might be confusing since, intuitively, the magnitude of the gain should be *greater than* the loss. This would be true if the loss was represented as a resistor in series with the tank circuit. However, since a parallel representation is used here, higher resistance values indicate less loss and thus the gain should be less than R_{eq}.

The phase detector produces a waveform whose average DC value is directly proportional to the phase difference between the two oscillator outputs. The output of the phase detector is then passed through a low-pass filter to remove any spurious high-frequency components. This low-pass filter may be an operational amplifier-based active filter or a passive RC filter depending on the application of the PLL. The resulting signal from the filter is considered to be an *error voltage* representing the phase error between the two oscillator waveforms. The error voltage is then passed to the VCO varactor control line and the capacitance of the varactor is changed which consequently tunes the output frequency of the oscillator. The nature of the PLL is such that the error voltage settles to the steady-state output of the phase detector. Once the phase detector output is in steady state, the phase difference between the reference and the VCO is constant. Phase difference is related to frequency difference in the following equation:

$$\frac{d}{dt}(\theta_1 - \theta_2) = f_1 - f_2, \tag{1.12}$$

where θ_1 and f_1 are the phase and frequency of the reference respectively and θ_2 and f_2 are the phase and frequency of the VCO. By driving the phase difference to a constant steady-state value, the PLL locks the frequencies of the reference and the VCO together.

Divide-by-N Block

The final subcircuit of the PLL is the divide-by-N frequency prescaler block. This circuit divides the frequency of the VCO to a frequency close to that of the crystal reference. For instance, if the crystal reference is running at 200 MHz and the VCO center frequency is 5 GHz, the division factor, N, would need to be 25. The divider is typically programmable so that it can track changes in the VCO center frequency as it is switched in a multi-band system.

Today, all of the subcircuits of the PLL can currently be integrated except for the crystal reference. If a high-Q frequency reference component could be integrated on-chip, the PLL could be modified by replacing the off-chip crystal with an on-chip implementation. This would eliminate the chip-to-module interface between the crystal and the rest of the crystal-referenced oscillator.

1.1.4 Summary

The classical superheterodyne radio structure is not well suited for high levels of integration due to the need for off-chip components such as the band-select filter, image-reject filters, channel-select filters, and the crystal frequency references for local oscillator PLLs. Through the use of alternative architectures such as the DCR and Low-IF receiver, the image-reject filter can be eliminated and channel-select filters replaced by analog or digital low pass filters that can be realized on-chip. The PLL crystal references and the band-select filter, however, continue to remain off-chip in such designs. Since on-chip inductors and capacitors cannot meet the high Q-requirements of these components, *microelectromechanical (MEM) resonators*, that demonstrate similar advantages as piezoelectric-based devices but are amenable to IC fabrication, have been proposed as on-chip replacements. The remainder of this chapter discusses such MEM resonators, which offer the potential for ultimate single-chip transceiver integration.

1.2 Micro/Nano-Electromechanical Systems

The field of Micro-/Nano-Electromechanical systems (MEMS/NEMS) encompasses a wide range of devices fabricated at or below the micron scale that involve the transduction of energy from the electrical, thermal, or optical domains into the mechanical domain and vice versa. These devices are fabricated using IC processing techniques and offer the potential for direct integration with transistor devices such as metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar-junction transistors (BJTs). MEMS and NEMS can generally be subdivided into three major categories: sensors, actuators, and transducers (although the lines between these categories are often blurred).

MEMS sensors are used to detect physical, chemical, or biological phenomenon and translate them into electrical signals such as resistance or capacitance. Examples of MEMS sensors include: micro-miniature accelerometers used for deploying automobile airbags [21], detectors of volatile airborne gases [22], and DNA sensors capable of zepto-mole resolution [23].

MEMS actuators perform active functions such as: pumping of fluids at the micron scale [24], optical switching [25], and electronic switching [26]. A defining trait of micro-actuators is the ability to precisely control the mechanical motion or position of micron-scale devices, fluids, or other media on-chip.

Devices that are both sensors and actuators fall into the category of MEMS transducers. MEMS resonators are examples of such transducers, and operate on a principle similar to the piezoelectric quartz crystal, i.e. electrical signals at a particular resonant frequency generate inherently high-Q mechanical vibration in a stiff material, usually silicon or polysilicon. However, the specifics of resonator physics are different than those of piezoelectric devices and will be introduced in the next section.

1.2.1 MEMS Resonators

A simple schematic of a MEMS resonator and a micrograph of a corresponding fabricated resonator in Si technology are shown in Figure 1.13. The MEMS resonator shown is comprised of three main elements: the excitation electrode, the vibrating mechanical structure, and the DC bias supply and current readout. The vibrating structure in this case is a doubly anchored (also known as "clamped-clamped") polysilicon beam suspended a distance d above a metallized polysilicon excitation electrode. Basically, a parallel-plate capacitor is formed between the electrode and the area of the suspended beam directly above the electrode. When a voltage is applied across the plates of the capacitor, an electrostatic force arises that can be determined from the derivative of the potential energy of the capacitor as follows [27]:

$$F_d = \frac{\partial U}{\partial x} = \frac{1}{2}\left(v_e - v_b\right)^2 \frac{\partial C}{\partial x}, \tag{1.13}$$

where U is the potential energy, x is the displacement as defined in Figure 1.13, v_e is the small-signal voltage on the electrode, v_b is the voltage on the beam, and $\frac{\partial C}{\partial x}$ is the change in resonator-to-electrode capacitance per unit displacement[6].

Since the beam is anchored at both ends but is free to move in the x-direction at the center, the force described in Equation 1.13 will deflect the center of the beam

[6]There exist other methods for inducing mechanical motion in MEMS resonators that involve optical [28] or air flow [29] excitation that have, at best, limited application for RF devices.

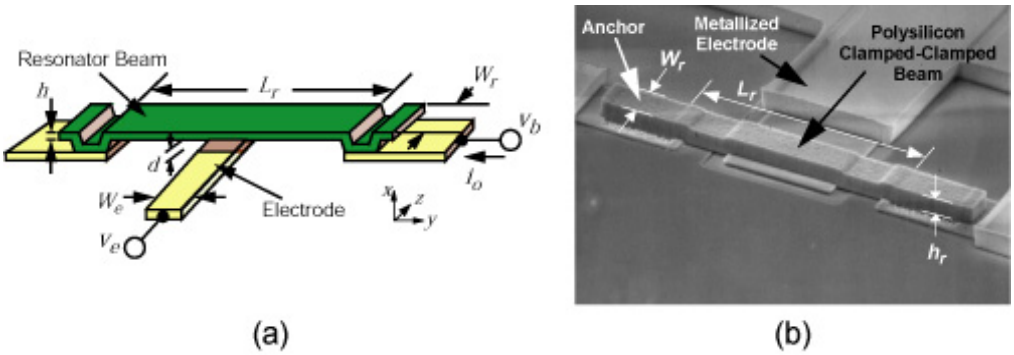


Figure 1.13: A simple MEMS resonator: (a) Perspective-view schematic of a clamped-clamped beam μmechanical resonator showing excitation voltages; (b) SEM micrograph of an 8.5 MHz polysilicon clamped-clamped beam ("CC-beam") μmechanical resonator [27].

towards (or away depending on the polarity of the applied voltages) the electrode by a distance proportional to the potential difference. By applying a periodic excitation voltage, v_e, of the form $V_i \cos(\omega_i t)$, and by applying a constant DC voltage, V_{DC}, for the beam voltage, v_b, Equation 1.13 simplifies to [27]:

$$F_d(t) = \frac{\partial C}{\partial x}\left[\left(\frac{V_{DC}^2}{2} + \frac{V_i^2}{4}\right) - V_{DC}V_i\cos(\omega_i t) + \frac{V_i^2}{4}\cos\left(2\omega_i t\right)\right]. \tag{1.14}$$

The first term of Equation 1.14 is a DC term that results in static deflection of the beam but has little effect on high frequency oscillations. The second term is the most important for filter and tank circuit applications because it results in oscillations at the frequency of excitation; electrical excitations at frequency ω_i will result in a mechanical force multiplied by the DC bias voltage at frequency ω_i. At most frequencies away from ω_i, the beam will not respond appreciably to the force and there will be little detectable vibrational amplitude. However, at the natural, or resonant, frequency of the beam, the vibrational amplitude will be markedly higher. In this case, the resonator will source a current given by:

$$i_o = V_{DC}\frac{\partial C}{\partial x}\frac{\partial x}{\partial t}, \tag{1.15}$$

A two-port measurement of the beam using the excitation electrode as the input port and the beam's DC connection (the DC bias and small-signal output are isolated by

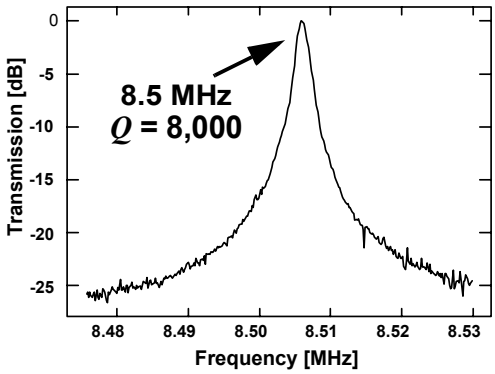


Figure 1.14: Typical measured frequency transmission spectrum for an 8.5 MHz polysilicon clamped-clamped beam ("CC-beam") μmechanical resonator [27].

a bias tee) as the output port (50 Ω load) will result in a transmission characteristic similar to that shown in Figure 1.14 [27].

The natural frequencies of a clamped-clamped beam can be found using [30]:

$$f_o = \frac{k_i^2}{L_r^2 2\pi}\sqrt{\frac{EI}{\rho A}}, \tag{1.16}$$

where k_i is a constant that depends on the harmonic of interest (4.730 for the fundamental mode of the geometry shown in Figure 1.13), L_r is the length of the beam, E is the Young's modulus for the beam material, I is the cross-sectional moment of inertia, ρ is the density of the beam material, and A is the cross-sectional area. Substituting the moment of inertia for a simple beam:

$$I = \frac{w_r h_r^3}{12}, \tag{1.17}$$

where w_r is the beam width and h_r is the beam thickness, Equation 1.16 simplifies to:

$$f_o = 1.03\sqrt{\frac{E}{\rho}}\frac{h_r}{L_r^2}. \tag{1.18}$$

There are an infinite number of resonant frequencies for a beam of a certain shape and material; however, the fundamental mode is typically the frequency of primary interest for this resonator. Both the resonator material and its dimensions have an effect on

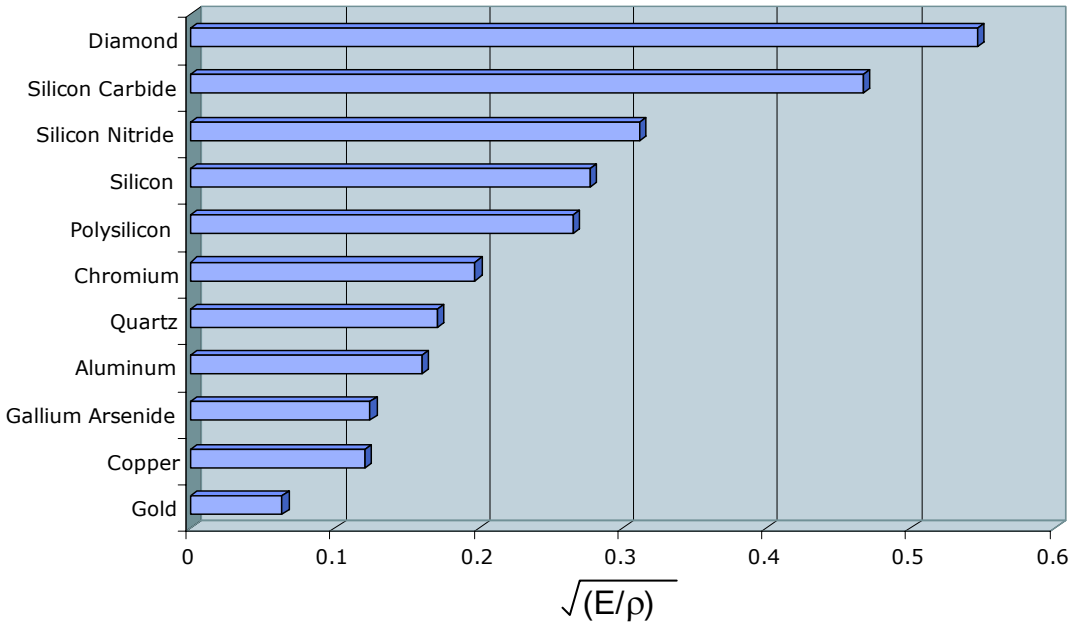


Figure 1.15: Ratio of Young's modulus to density for common IC materials and exotic high-ratio materials.

the natural frequency. From the point of view of geometry, long, thin beams have lower natural frequencies than short, thick ones. From the point of view of material composition, the ratio between Young's modulus and density (E/ρ) is most important. Figure 1.15 compares the E/ρ ratio for several materials common to IC processing and for some more exotic, high-ratio materials. Metals have fairly low ratios and are not as well-suited for use in high-Q electromechanical resonators. Polysilicon and single-crystal silicon, on the other hand, offer the highest ratio amongst the common IC materials and are good choices for high-frequency on-chip resonator designs.

The third term of Equation 1.14 represents a harmonic force that has a twofold effect on the resonator frequency response. First, input frequencies, ω_i, at half the resonant frequency ($f_o/2$), will result in resonant vibration at frequency f_o due to this term. Since this term is not multiplied by the DC bias it is typical that this harmonic is of sufficiently small amplitude to avoid significant degradation in the resonator performance. However, if large interferers are present at this half frequency it may be necessary to filter excitation components at this frequency. Second, for input excitation at the resonant frequency, this term results in a time-varying force at twice the resonant frequency. Since the beam is unlikely to have a natural resonant

response at this double frequency, the vibration and current at this frequency should be negligible in comparison to that at the fundamental natural frequency.

MEMS Resonator Applications in the RF Multi-Band Receiver

One of the main advantages of MEMS resonators is their size. The dimensions of the resonator in Figure 1.13 are 40.8 μm by 8 μm by 2 μm, easily small enough to fabricate on-chip alongside RF, analog and digital circuitry. Another advantage is that they do not require non-standard materials since they do not depend on piezoelectricity for electromechanical transduction. Silicon, the most common IC substrate material, turns out to be ideal for MEMS resonator fabrication due to its high Young's modulus to density ratio.

Like piezoelectric quartz, single-crystal silicon (SCSi) also has the property of being a mechanically low-loss material, i.e. there is virtually no elastic hysteresis in the material[7]. Therefore, silicon is generally regarded as a high-Q mechanical material when it is incorporated into resonators such as those described in the previous section. The Q-factors of the resonator described in Section 1.2.1 are on the order of 10,000. Indeed, factors such as silicon's low mechanical loss, its relatively high natural frequencies, and the compatibility of MEM resonator fabrication techniques with IC fabrication processes make on-chip silicon-based MEM resonators strong potential candidates for replacing the current high-Q off-chip components.

Figure 1.16 shows how a multiple-pole filter (such as the one described in Figure 1.3) can be constructed with two mechanically coupled clamped-clamped beam resonators [27] (the electrical equivalent circuit shown in the figure will be discussed in detail in Chapter 3). Since the Q-factors of the individual resonating elements are extremely high, the insertion loss of a MEM-based on-chip multiple-pole filter would be acceptably low. MEMS filters could then potentially be used to replace the band-select filter in a DCR or a Low-IF receiver.

Meanwhile, individual resonators could be used to replace crystal frequency references

[7]The elastic hysteresis is the ratio between the energy required to deform a material and the elastic energy stored in the material by the deformation. Since the elastic energy can be completely restored, any difference between the deformation energy and the elastic energy is considered loss. This loss is normally introduced by friction between interstitial lattice defects, of which, SCSi has very few.

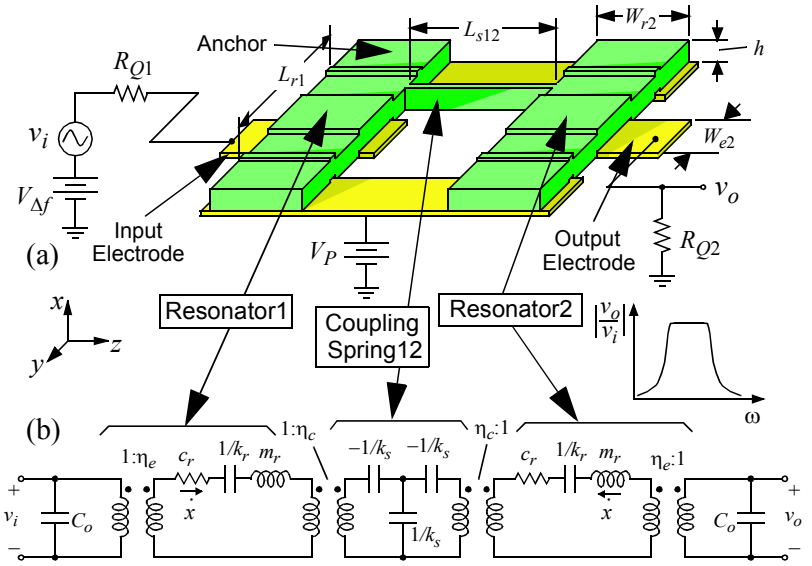


Figure 1.16: Example of a multiple-pole MEM resonator filter (a) schematic; (b) equivalent circuit [27].

in a PLL circuit. Additionally, the dependence of the resonator output current on the DC bias (Equation 1.15) provides the opportunity for integrated MEMS-based ultra-stable VCOs. By selectively activating resonators of different sizes, the total tank resonant frequency could be discretely tuned. Therefore, MEMS resonators offer the promise of a fully-integrated, minimum component count receiver. However, there are a number of non-trivial drawbacks to using beam-shaped MEMS for filter and frequency reference realizations. The main problem with beam-shaped resonators is the exceedingly small size required to achieve RF-range operation.

To achieve a resonant frequency of 150 MHz using the beam resonator shown in Figure 1.13, the length of the beam would have to be scaled below 10 μm (for a uniform thickness of 2 μm). There are several consequences to reduced device size. First, the contributions of most noise sources in MEM resonators are increased with decreasing resonator size [31]. Noise in resonators is highly dependent on the volume to surface area ratio which decreases as the resonator geometry is scaled [27]. Second, the ability to actuate and detect the motion of the resonator is decreased with decreasing geometry. Recall from Equation 1.14 that the forcing function is directly dependent on the amount of differential capacitance between the drive electrode and the beam.

Since the capacitance of a parallel-plate capacitor is:

$$C = \frac{\varepsilon_o A}{d}, \tag{1.19}$$

where ε_o is the dielectric constant of the material between the plates, A is the cross sectional area of the plates, and d is the spacing between the plates, it is evident that reducing the size of the beam will significantly reduce the amount of available capacitance, and thus force, supplied by the drive electrode. If the force is significantly reduced, the resulting displacement will be very difficult to detect since the output current is directly dependant on the displacement (Equation 1.15).

The effects of anchor losses, a primary factor when determining resonator Q-factor, are also exacerbated in small structures. Since the anchors shown in Figure 1.13 (b) are generally of the same size regardless of the length of the beam, a larger percentage of the available vibrational energy will be lost into the substrate for smaller beams. Comb-drive based resonators similar to that shown in Figure 1.17 offer increased capacitance due to the increased surface-area; however, the added mass of the comb-drive structure reduces the frequency capabilities to below 1 MHz [32, 33]. Alternatively, the contour-mode disk-shaped resonator, originally adapted to MEMS implementation by Nguyen, *et al.,* has shown promise for exhibiting high resonant frequencies at relatively large dimensions.

1.2.2 Contour-Mode Disk-Shaped MEMS Resonators

In the standard contour-mode resonator depicted in Figure 1.18, the resonating shape is a disk supported at the center by a stationary post. The electrodes are positioned around the circumference of the disk with a specific gap spacing, d, just as the beam resonator described above is separated a certain distance above the excitation electrode. The force applied by the electrodes is the same as in Equation 1.14 except in this case the force is applied laterally around the resonating element. At certain frequencies, this force will result in contour-mode vibration of the disk, a mode characterized by radial expansion and contraction of the disk edge in the plane of the electrode. An advantage to this type of vibration is the mitigation of thermoelastic damping, a major contributor of loss in flexure or torsional-modes found in

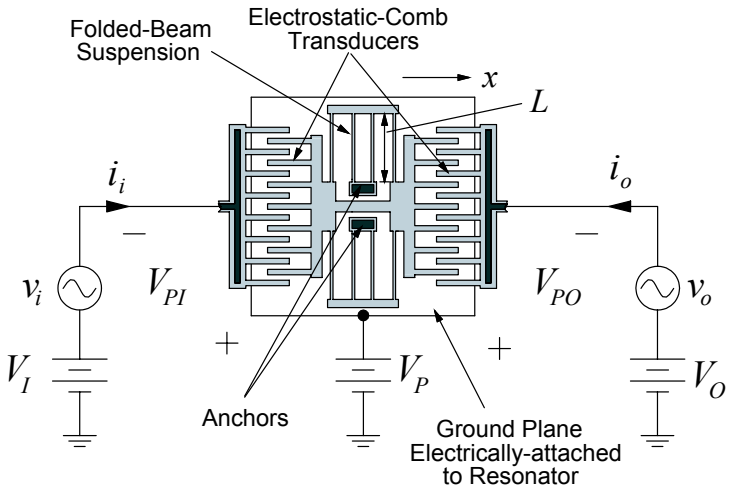


Figure 1.17: Overhead view of a two-port, folded-beam, lateral comb-driven resonator with typical applied bias and excitation voltages. All areas of the resonator and electrodes are suspended 2 μm above the substrate, except for the darkly shaded areas, which are the anchor points [33].

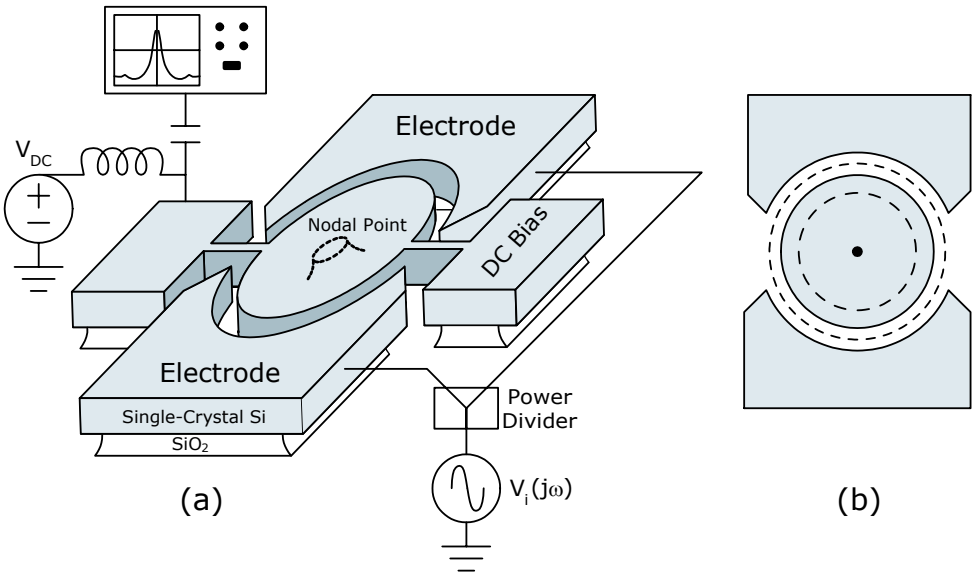


Figure 1.18: Contour-mode disk resonator fabricated in a silicon-on-insulator (SOI) process: (a) resonator and accompanying measurement and excitation electrodes shown in a one-port testing setup; (b) top view of resonator indicating mode shape of contour vibration (dashed lines indicate extremes of edge displacement).

beam-shaped resonators [34]. Thermoelastic damping occurs when certain regions of the resonator structure are experiencing compression while others are in expansion. Compressed materials tend to heat while materials in expansion tend to cool. The thermal gradient between these two regions induces irreversible energy loss due to heat flow. This loss is significant in beam structures; however, all areas of the contour-mode disk-resonator are theoretically entirely in expansion or contraction and thus this heat flow is reduced.

Neglecting second order effects such as the disk thickness and anchor effects, determination of the expected contour-mode frequency can be accomplished through a two-step process [35]. First, the frequency parameter, ζ, is solved using:

$$\frac{\gamma}{\xi}\frac{J_0\left(\frac{\gamma}{\xi}\right)}{J_1\left(\frac{\gamma}{\xi}\right)} = 1-\sigma, \text{where } \xi = \sqrt{\frac{2}{1-\sigma}}, \tag{1.20}$$

and where σ is the Poisson's ratio and J_n is the Bessel function of the first kind of order n. The resulting γ is then substituted into:

$$f = \frac{\gamma}{2\pi R}\sqrt{\frac{E}{\rho\,(2+2\sigma)}}, \tag{1.21}$$

where R is the disk radius, E is the Young's modulus, and ρ is the density of the disk material. Assuming a Young's modulus of 165 GPa, a density of 2330 $\mathrm{kg/m^3}$, and a Poisson's ratio of 0.22 for silicon, Figure 1.19 compares the predicted contour-mode frequency versus disk radius and the clamped-clamped beam resonant frequency versus length. Resonators constructed in the contour-mode shape have exhibited Q-factors of 9,400 for vibrational frequencies around 150 MHz [36], and 7,330 and 1,595 for harmonically excited frequencies around 732 MHz and 1.14 GHz, respectively [37].

Resonator Fabrication

The contour-mode resonator work done by Nguyen, *et al.*, uses a sequence of lithography steps that are described in detail in [36] and [38] and briefly summarized here in Figure 1.20. First, a thin layer of polysilicon that will serve as the electrical connection to the center post is deposited on the surface and etched to the desired pattern.

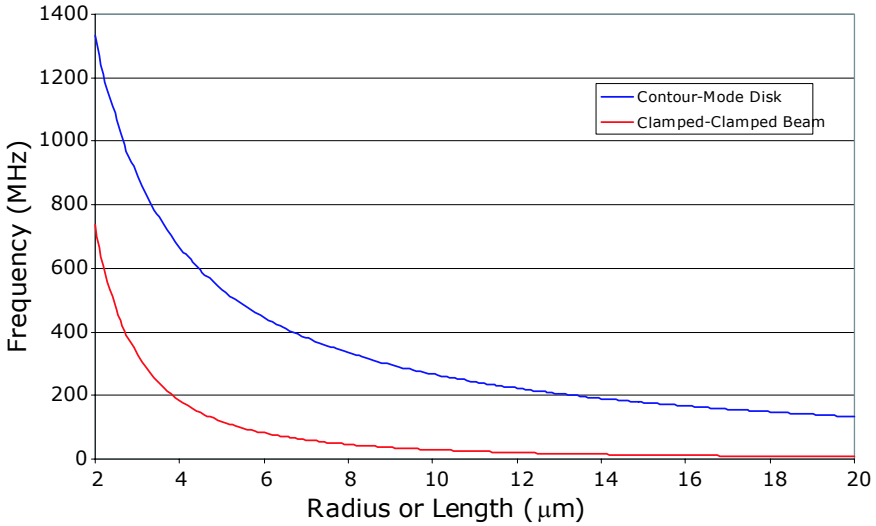


Figure 1.19: Comparison between the predicted contour-mode frequency versus disk radius and the clamped-clamped beam resonant frequency versus beam length.

Second, a 500 nm-thick layer of oxide is deposited over the surface of the sample which is then etched in the location of the electrode and the center post. Third, a 2 μm-thick layer of polysilicon is deposited over the entire surface and etched in the shape of the disk. Next, a conformal 100 nm-thick oxide layer is grown over the disk and a thick PR electroplating mold is deposited. Metal is electrodeposited in the space between the conformal oxide and the PR mold and, finally, an HF step etches away the oxide, leaving the 100 nm gap spacing between the electrode and disk.

Due to some limitations in available processing capabilities, the resonators for this work were rather designed for fabrication in a Silicon-on-Insulator (SOI) surface micromachining process developed by Barnhart, *et al.* [39] and shown in Figure 1.21. The process steps (corresponding to the numbered steps in Figure 1.21) are outlined as follows:

1. The starting material consists of an approximately 1 cm $\times$ 1 cm diced sample from an SOI wafer. The SOI wafer consists of three layers: a highly doped top layer in which the resonator disk and electrodes are fabricated, a buried silicon dioxide layer, and an underlying thick bulk substrate layer.

2. Two layers of PMMA, an electron-sensitive resist, are spun on the surface of

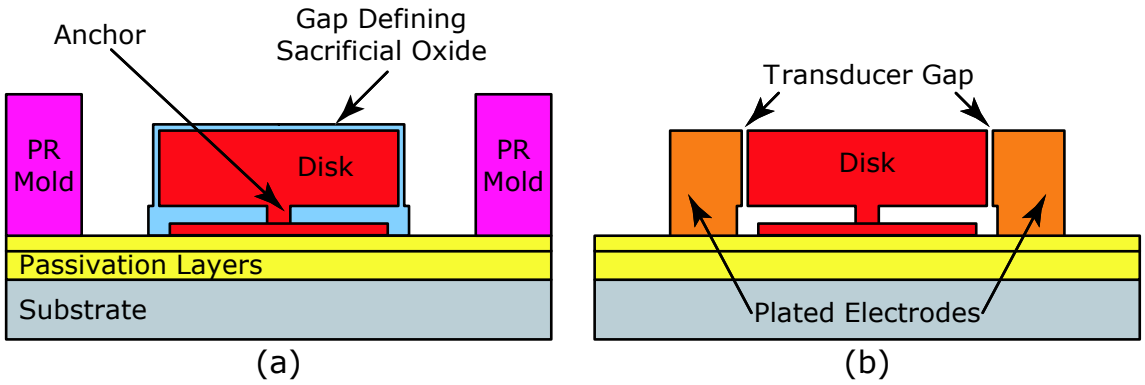


Figure 1.20: Polysilicon disk resonator process cross section: (a) A conformal oxide and photoresist (PR) electroplating mold are fabricated using a surface micromachining process; (b) Electrodes are plated between the PR mold and sidewalls, then the structure is released. (After [36])

the substrate for a total thickness of ∼500 nm.

3. A scanning electron microscope (SEM) is used in conjunction with the Nabity Pattern Generation System (NPGS) [40] to raster scan a beam of high energy electrons in the shape of the resonator across the surface of the resist. Polymer chains in the resist are broken, and thus made more soluble in a developer, by the electron beam.

4. A solution of MIBK and IPA removes broken polymer chains, exposing the top layer of silicon in the patterned areas.

5. A thin (25 nm - 150 nm) layer of metal is evaporated on the surface of the sample using electron-beam evaporation.

6. Liftoff of remaining resist is performed in an acetone solution, leaving a metal mask in the shape of the disk on the sample surface.

7. A fluorine-based reactive ion etch is used to remove the silicon in the top layer that is not protected by the metal mask.

8. Finally, a timed HF wet-etch is used to remove the oxide layer from underneath the resonator, leaving only a small post in the center of the disk for support.

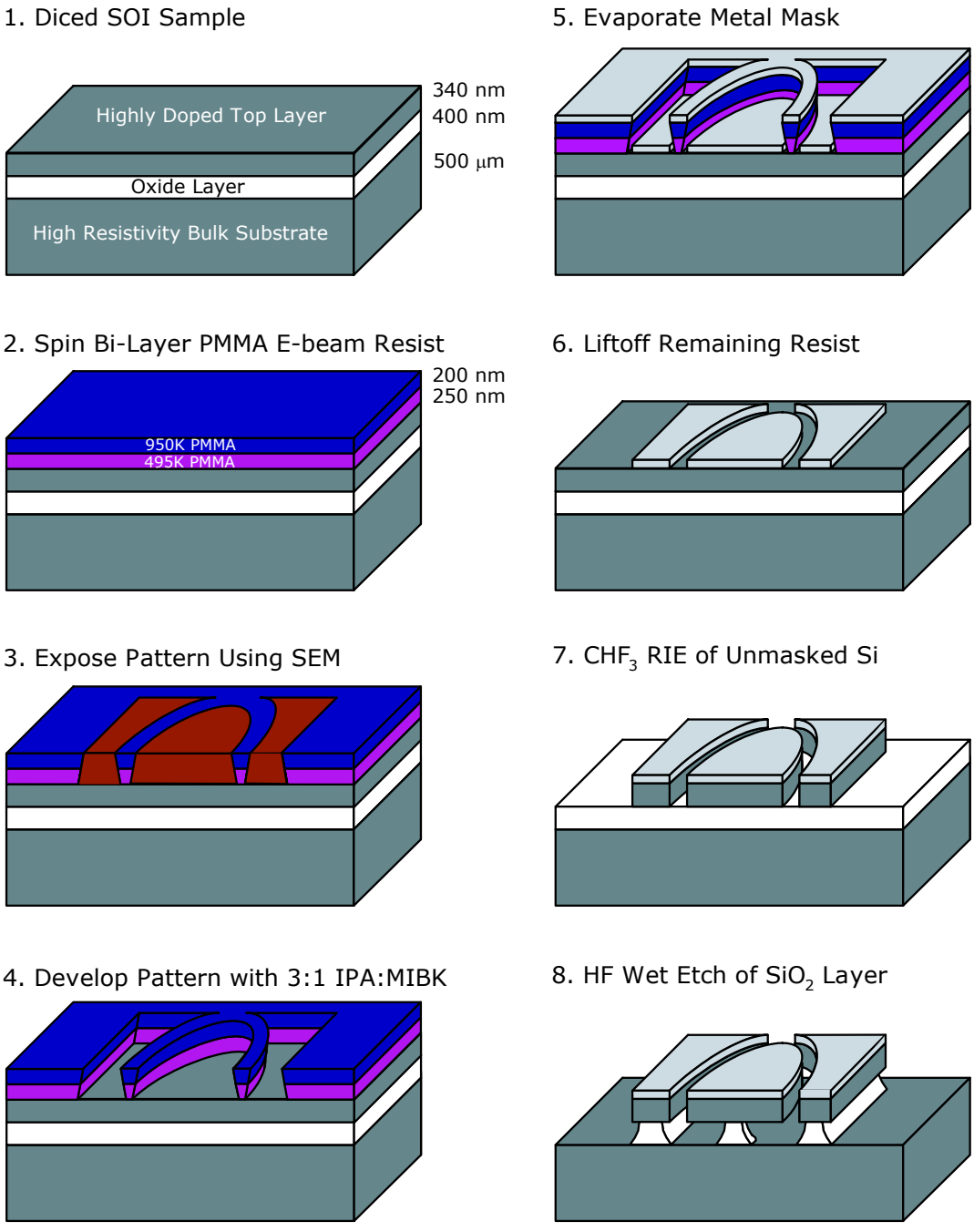


Figure 1.21: Steps of SOI disk-resonator fabrication process.

SOI provides certain advantages over conventional Si technology for IC designs in the analog and digital domain, and is thus used in state-of-the-art low-power CMOS applications [41, 42]. SOI has also been used for fabrication of some MEMS devices [43,44]; however, it is relatively expensive. For this reason, migration of this resonator to another, more commercially viable, process will be proposed in the conclusions of this thesis.

1.3 Thesis Objective

The goals of this thesis are twofold. The first is to present the design of a multi-band VCO for use in a 5-6 GHz range receiver. An overview of the various challenges in low-power and low phase-noise VCO design is provided. Measured results for the multi-band VCO design are presented, and possible improvements for future design iterations are suggested. The second goal of this thesis is to present the design and fabrication of contour-mode disk resonators and suggest new methods by which these resonators be integrated with RF transceiver subcircuits, including the aforementioned VCO.

1.4 Overview of Thesis

This chapter has introduced the motivations and challenges associated with single-chip integration of RF wireless functions. The topics of VCO design and high-Q MEMS resonators have thus far only been introduced. The remaining chapters of this thesis will examine the realization of multi-band VCOs and MEMS disk resonators in more detail.

Chapter 2 focuses on the design of a switched-tank multi-band VCO. Two different VCOs are presented; one is designed for minimum phase noise while the other is designed for minimum power consumption. Layout, testing procedures, and measured results are documented. Possible improvements to these designs are also suggested.

Chapter 3 presents the electromechanical modeling of the contour-mode disk resonator, including lumped element electrical modeling and finite-element mechanical

modeling. Design variables and trade-offs are discussed along with expected RF performance for various transduction configurations.

Chapter 4 documents the enhanced SOI fabrication process used in this work to create micron-scale contour-mode resonators. Design choices made at each fabrication step are discussed in detail. Problems encountered with the fabrication process are discussed, along with methods to mitigate their impact on the resonator structure.

Chapter 5 provides conclusions on the work presented, and proposes future work building on the accomplishments of this thesis are also proposed. Also included is a discussion of the outlook for MEMS resonator integration into silicon RFICs, specifically multi-band VCOs.

Chapter 2

Design and Characterization of SiGe BiCMOS Switched-Tank VCOs

As discussed in Chapter 1, the VCOs designed in this thesis are intended for use in multi-band receivers operating over the 5-6 GHz unlicensed UNII band. This chapter elaborates on the introductory material from Chapter 1 and discusses in detail the topologies for two VCOs: the first optimized for low power consumption and the second optimized for high output power. A discussion of the fabrication and testing of the VCO designs follows. Possible design improvements, including the future integration of MEMS devices, are included in Chapter 5.

2.1 Differential VCO Architecture

The schematic for a single-ended output oscillator is shown in Figure 2.1(a). This schematic is similar to that in Figure 1.12, except that the generic -G_m amplifier block has been replaced with a BJT (Q_1) biased near the active region by a base voltage source and an emitter current source. The tank circuit consists of an inductor, a capacitor, and a parallel equivalent resistance that represents the loss (Q-factor) of the tank circuit. In this configuration, the impedance looking into the feedback loop

from the tank circuit is approximately equal to $1/G_m$ (assuming that the current source presents a very large output impedance). This resistance value is typically relatively low compared to the parallel equivalent resistance of the tank circuit and will load the tank circuit, reducing its effective or *loaded Q-factor*. Since the Q-factor should be as high as is possible, the tank can be buffered from the low input resistance using a buffer amplifier as shown in Figure 2.1(b). The buffer can be realized by a second BJT (Q_2) biased in a common-collector (emitter follower) configuration as in Figure 2.1(c). The common-collector configuration is characterized by a high input impedance, thus maximizing the loaded Q-factor of the tank circuit. Adding a second, identical tank circuit to the collector of Q_2 and connecting Q_1 so that it too acts as a buffer for the second tank circuit leads to the *differential* implementation shown in Figure 2.1(d). In the differential implementation, the oscillations are driven 180° out of phase with respect to each other, providing $V_{out}+$ and V_{out}-, respectively, at the collector nodes of each transistor.

Differential oscillators have two distinct advantages over their single-ended counterparts. First, the downconversion mixers for which the VCO acts as the LO source are inherently differential. Second, differential circuits provide common-mode rejection (quantified by the common-mode rejection ratio, CMRR) that single-ended circuits cannot. Since the two outputs of the VCO are differential, they can be subtracted to double their peak voltage output. By subtracting them, noise signals that are common to both outputs are cancelled leading to a high CMRR. For these reasons, differential implementations are preferred in RF applications despite the added power consumption of the second active device.

A differential oscillator schematic more specific to the work done in this thesis is shown in Figure 2.2. Here, the symmetry of the circuit allows the two tank circuits to be connected to a center virtual ground. The inductance is supplied by a differential inductor with a center tap connected to the DC supply. The capacitance of the tank is supplied by two separate sets of capacitors: switched capacitors and varactors. The switched capacitors provide discrete tuning between each of the three sub-bands of the UNII band. With the switches open, no additional capacitance is added to the tank and the oscillation frequency is at its maximum, defined only by the inductor and varactors. When the switch is closed, a certain amount of capacitance is added to the tank and the frequency drops a discrete amount, e.g. from 5.725 to 5.25 GHz.

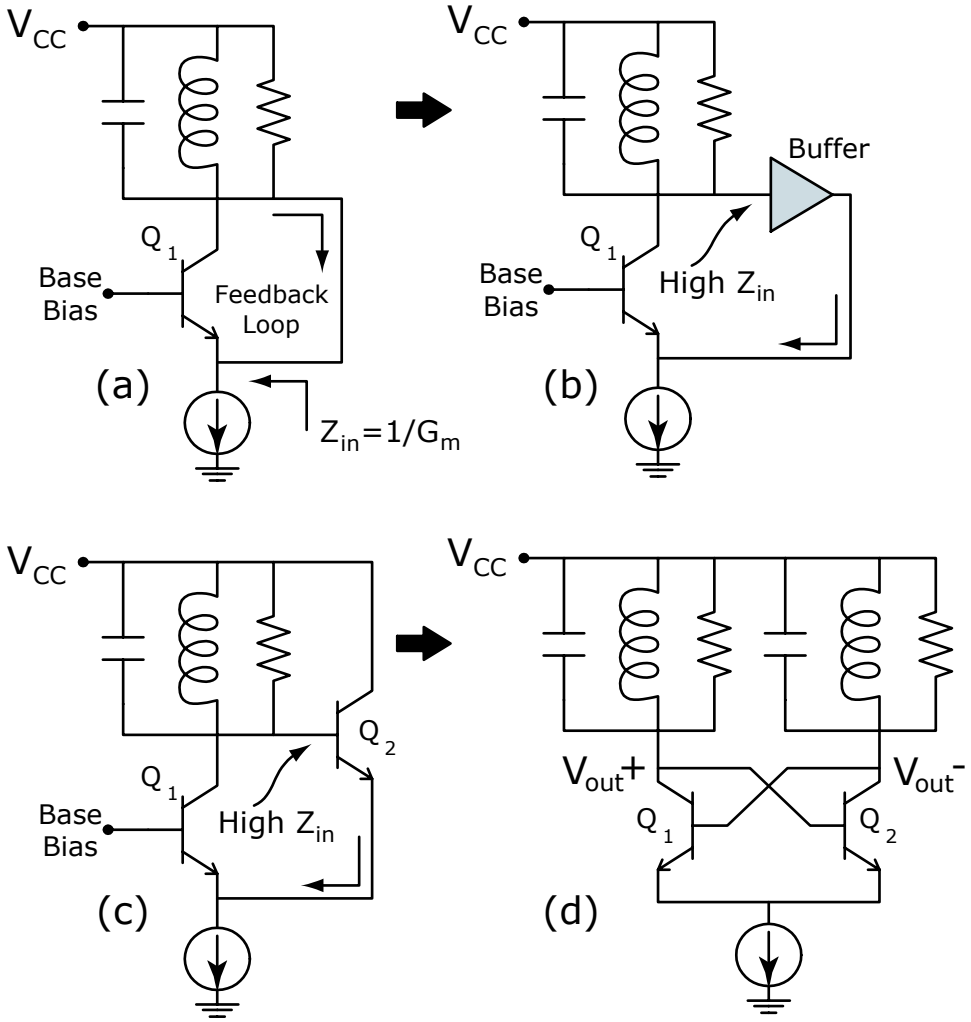


Figure 2.1: Development of cross-coupled differential VCO model: (a) single-ended VCO with direct feedback; (b) addition of high-impedance buffer to feedback path; (c) common-collector (emitter follower) buffer implementation; (d) differential implementation of (c).

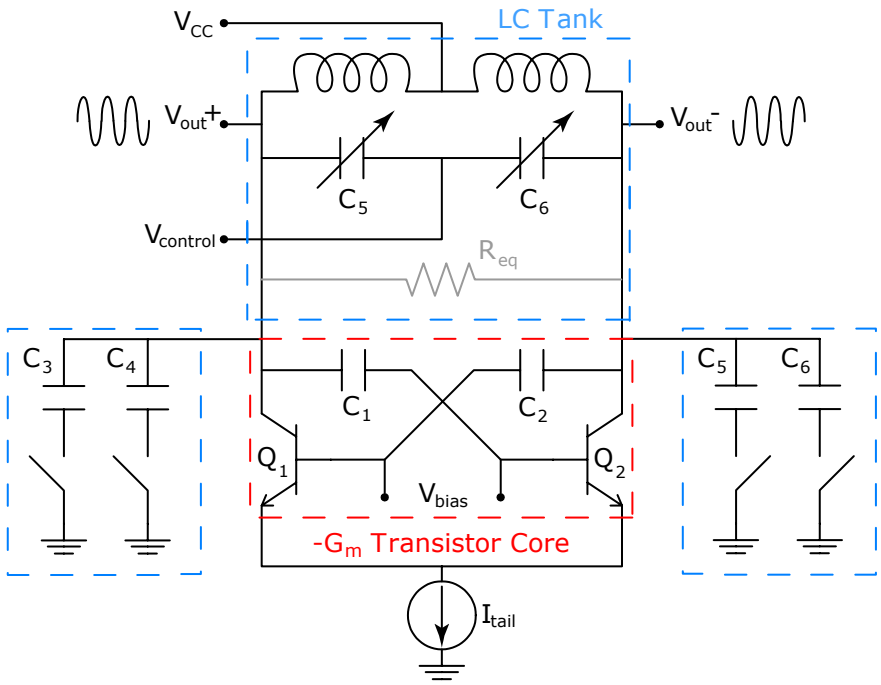


Figure 2.2: Simplified schematic for the two VCOs designed for this thesis.

The varactors, on the other hand, provide continuous fine tuning within each of the sub-bands. The capacitance provided by the varactors is controlled via an external voltage, $V_{control}$. The switched capacitors are tuned to switch between the three sub-bands of the UNII band: 5.15-5.25 GHz, 5.25 GHz-5.35 GHz, and 5.725-5.825 GHz and the varactors are tuned to provide the 100 MHz of tuning necessary to completely cover each band.

As stated previously, the -G_m amplifier is realized by two BJTs that are biased by a base voltage and an emitter current. The capacitors in the cross-coupled feedback path (C_1 and C_2) are large enough to pass the high-frequency signal at the output nodes but will isolate the DC base voltage from the DC collector voltage, allowing a larger output voltage swing without driving the transistors into saturation. The current source, I_{tail}, is implemented differently in each design; the two designs will covered individually later in this chapter. The focus of this chapter now shifts to cover the specifics of the tank circuit and amplifier transistor pair used in this work, and design choices made with respect to each.

2.2 Switched LC Tank Circuit

The elements of the integrated LC tank circuit, along with any parasitic capacitances and inductances due to circuit interconnects, determine the frequency of oscillation for the VCO. As stated earlier, the LC tank consists of a fixed-value component, the differential spiral planar inductor, and two variable components, the varactors and the switched-capacitors. The following subsections describe the impact of each of the components on the performance of a VCO.

2.2.1 Monolithic Planar Inductors

Due to its loss, the monolithic planar inductor is typically the passive component most responsible for degradation of the phase noise of the oscillator (to be explained further in Section 2.2.2). Since phase noise is a critical specification of the VCO, it is important to understand the sources of loss in such inductors so that their effects may be minimized.

Any alternating current-carrying wire will exhibit inductance. In hybrid circuits, lengths of wire are typically wound into a coil shape to increase the total magnetic flux, and thus the net inductance. In integrated circuit applications, metal traces cannot be formed into a three-dimensional coil without significant derivation from standard processing techniques; therefore the windings of the inductor are formed parallel to the plane of the substrate. Figure 2.3 shows three standard coil winding geometries available on-chip; the orange color represents the top metal of the inductor while the red color represents lower metal layer underpasses at the inductor ports. A parameterized model of a planar inductor is shown in Figure 2.4. Other than L_s, every component in Figure 2.4 models some loss or energy coupling mechanism of the inductor. Since the Q-factor of the inductor is dependent on the ratio of stored energy to lost energy (Equation 1.1), it is important to understand the sources of the loss mechanisms and how best to mitigate their effects. The equivalent circuit elements can be grouped into three general categories: conductor losses, substrate losses, and interwinding capacitances.

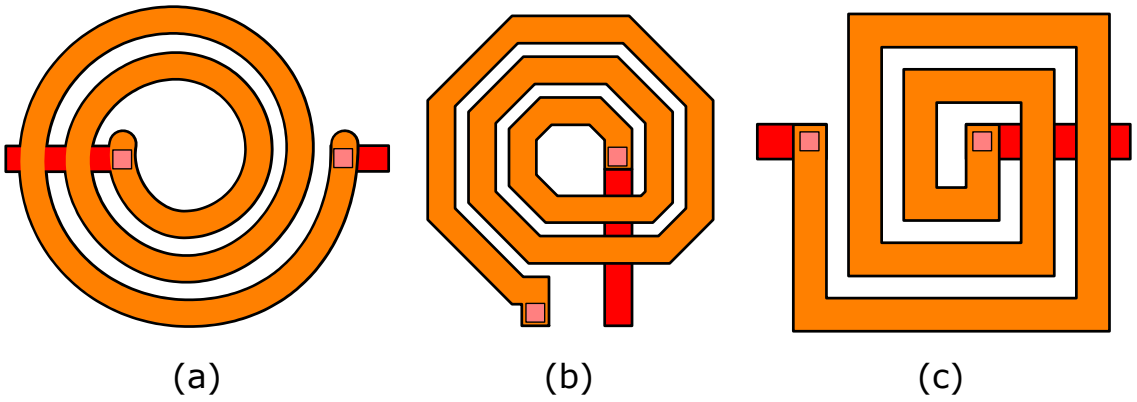


Figure 2.3: Three standard planar inductor geometries: (a) circular spiral; (b) octagonal spiral; (c) rectangular spiral.

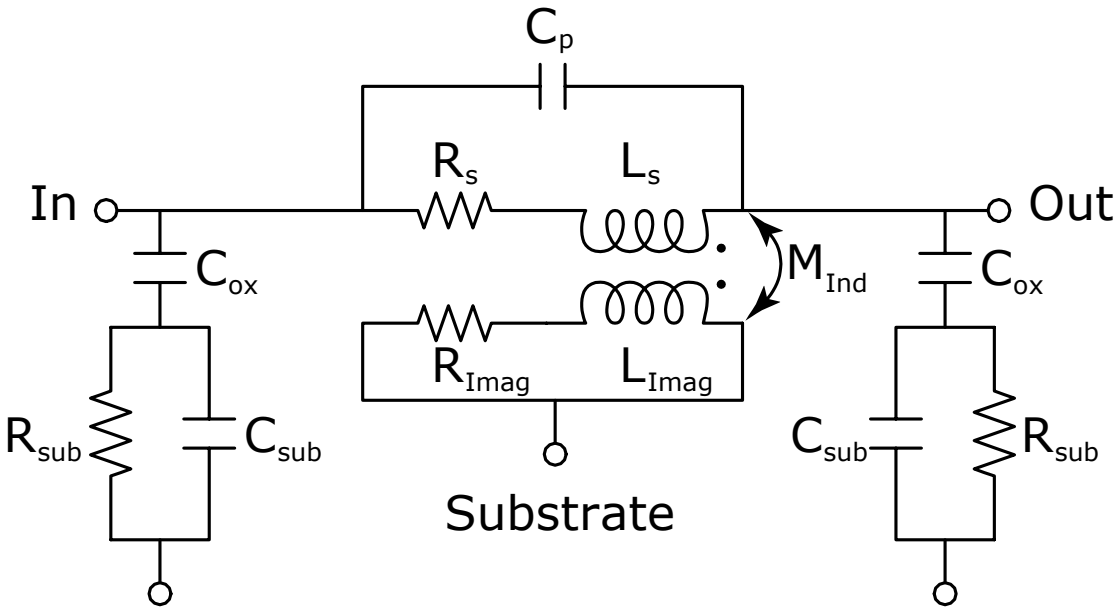


Figure 2.4: Model of an on-chip spiral inductor (After [45]).

Conductor Losses

The series resistor, R_s, in Figure 2.4 represents the loss of the windings of the inductor and is generally split into three contributors: resistive loss, skin effect losses, and current crowding from eddy currents.

- *Resistive Loss*

The resistance of any uniform conductor trace can be expressed as:

$$R = \left(\frac{\rho}{t}\right)\left(\frac{l}{w}\right), \tag{2.1}$$

where ρ is the resistivity of the metal, t is the thickness, l is the length, and w is the width. In order to reduce the trace resistive loss, three actions can be taken: utilize a metal with minimum resistivity; increase the cross-sectional area of the trace ($t \cdot w$); or shorten the length of the trace. Historically, IC interconnects and inductor windings have been fabricated with aluminum. Al offers low-cost deposition, does not contaminate Si crystal lattices, and forms a protective oxide. However, since the thin film resistivity of evaporated Al (4.8 $\mu\Omega \cdot$ cm) is fairly high when compared to that of electroplated copper (1.9 $\mu\Omega \cdot$ cm), IC processes have gradually migrated towards copper as the primary interconnect metal despite its attendant processing challenges.

Inductors are typically fabricated a thick "analog" or "bump" electroplated copper layer (such as in the Motorola process used in this work) that is deposited above the other layers of metal interconnects. To prevent the copper from doping the dielectric layer, a barrier layer such as Ti or TiN is deposited before the copper is electroplated [46]. Since the copper layer is the last metal layer and there are no circuit components above it on the chip, it is not subject to the same planarization and thickness rules as the other metal layers and can be made much thicker and wider. The copper layer in the Motorola HIP6WRF process used for the VCO designs in this thesis is $\sim$10 μm thick and can be up to 20 μm wide.

The final design variable impacting resistive losses is the conductor length. Inductor geometries that can reduce the overall trace length necessary to generate a certain inductance value will have a minimum series resistance. Since magnetic flux is

generated by a loop of current carrying wire, the inductance of a planar inductor is determined largely by the number of turns in the trace. Flux is most efficiently generated in the circular spiral inductor shown in Figure 2.3(a) because the entire length of each trace contributes to the magnetic flux of the inductor. The 90 ° bends of the square inductor shown in Figure 2.3(c), on the other hand, are the least efficient in terms of generating magnetic flux. Therefore, circular spiral inductors offer the lowest resistance for a given inductance. However, most lithographic processes require that metal traces be laid out in discrete angles, often only 45 or 90 degrees. For this reason, the octagonal approximation of the circular inductor shown in Figure 2.3(b) is often used to minimize the series resistance. Unfortunately, at the time these designs were completed, the HIP6WRF process did not offer octagonal inductor parameterized cells (p-cells) in the design library so available rectangular inductor p-cells were used in the LC tank.

- *Skin Effect and Eddy Currents*

At low frequencies, the current density is uniform throughout a conductor and Equation 2.1 is an accurate estimate of the total resistance of the conductor. However, at high frequencies, induced magnetic fields force the flow of current into a reduced cross-sectional area of the conductor, effectively increasing the resistance.

The skin effect can be understood as the restriction of current flow to the outside edges of a conductor as a result of magnetic fields arising in a high-frequency current-carrying conductor. The majority of the current flow in such a conductor will be constricted to a *skin depth*, δ, (measured from the outside edge) expressed as:

$$\delta = \sqrt{\frac{2\rho}{\mu\omega}}, \tag{2.2}$$

where μ is the magnetic permeability of the conductor and ω is the frequency in $\mathrm{rad/s}$. The skin depth becomes a more significant contributor to loss at frequencies approaching 10 GHz [47].

Another source of conductor loss in planar inductors is current crowding introduced by field-induced *eddy currents*. The magnetic field lines emanating from the center of the planar inductor penetrate the winding traces in the inductor causing currents

to swirl in circular patterns as depicted in Figure 2.5. At the outside edge of the inductor trace, the primary current through the trace and the induced eddy current are flowing in opposite directions. The eddy current acts to diminish the primary current magnitude at the outside edge of the trace, thus increasing the overall effective resistance of the trace. The magnitude of the added resistance due to the eddy currents can be approximated by [48]:

$$R_{EQ} = R_{DC} + \frac{1}{2}\left(\frac{\omega}{\omega_{crit}}\right)^2 \sum_{n=1}^{N} R_n \left(\frac{n-M}{N-M}\right)^2, \tag{2.3}$$

where R_{DC} is the resistance of the coils at DC, ω is the frequency of interest, R_n is the DC resistance of one of the coils, N is the number of coils counted from the outermost coil to the innermost, M is a factor that depends on the number of coils near the center of the inductor ($N/4$ is a good estimate for most geometries), and ω_{crit} is the frequency at which the eddy crowding becomes significant. ω_{crit} can be found through the following relation:

$$\omega_{crit} = \frac{3.1}{\mu_o}\frac{P}{W^2}R_{sheet}, \tag{2.4}$$

where μ_o is the permeability of free space, P is the total of the winding width and the interwinding spacing, W is the winding width, and R_{sheet} is the sheet resistance of the material [48]. Equation 2.3 shows that R_{EQ} is at a maximum for the innermost traces, i.e. the eddy currents are stronger in these traces. Therefore, one method of combating the effect of the eddy currents is to lay out inductors with "hollow" centers, i.e. with no windings in the center of the structure. Since these windings contribute little to the overall inductance, removing them serves to increase the Q-factor without a significant impact on inductor value.

Substrate Losses

Coupling, or loss of energy, to the substrate can be categorized as either electrical coupling or magnetic coupling. Electrical coupling is simply described as energy loss through the leakage of current into the substrate through the equivalent circuit components C_{ox}, R_{sub}, and C_{sub}. R_{sub} represents the real part of the substrate impedance and is usually high for most substrates. C_{sub} represents the capacitance between the

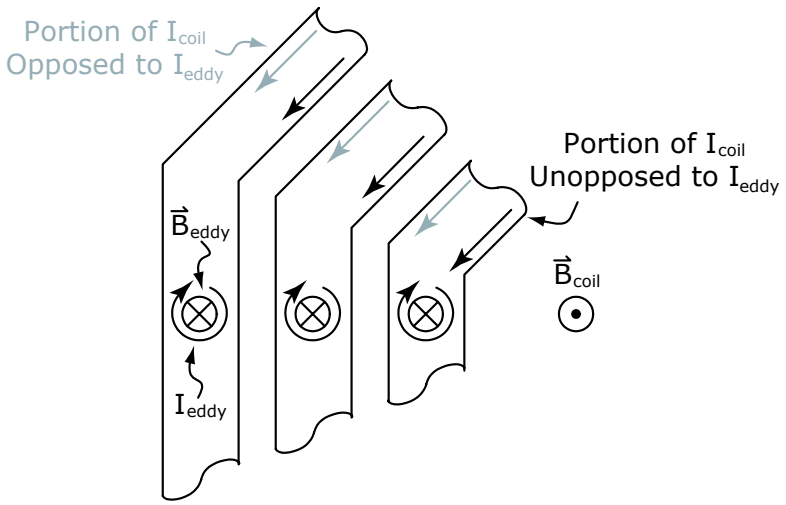


Figure 2.5: Eddy currents generated by the magnetic field of the coil windings. The $\otimes$ and $\odot$ symbols show magnetic flux into and out of the page respectively (after [47]).

top and bottom of the substrate and, at high frequencies, represents a significant source of lost energy through the substrate. This capacitance, in conjunction with R_{sub} and C_{ox}, is one of the major factors responsible for the decrease in inductor Q-factor at high frequency. C_{ox} accounts for any capacitance between the inductor coils and the substrate which can be approximated as a parallel-plate capacitance. Recall that parallel-plate capacitance is a function of the cross-sectional area of the plates (Equation 1.19). Therefore, wider windings lead to larger values for this parasitic capacitance. Since the resistance of the coils at high frequencies can become independent of their width due to the skin effect, it is sometimes beneficial to reduce the width of the windings to decrease this parasitic capacitance.

Magnetic coupling often has a far greater impact on the loss of the inductor than either electrical coupling or conductor losses, and typically accounts for $\sim$60% of the total loss [49]. Magnetic flux generated by the inductor coils penetrates the substrate giving rise to an image current in the substrate that flows in the opposite direction to the current in the physical inductor windings. Since there is finite loss in the substrate and since the image currents themselves give rise to a magnetic field, the loss due to the image current can be expressed as a parasitic resistor, R_{imag}, and a parasitic inductance, L_{imag}, that are coupled back to the primary inductor coils via mutual inductance, M_{ind}. Figure 2.6 shows the image current in a cross-section of a

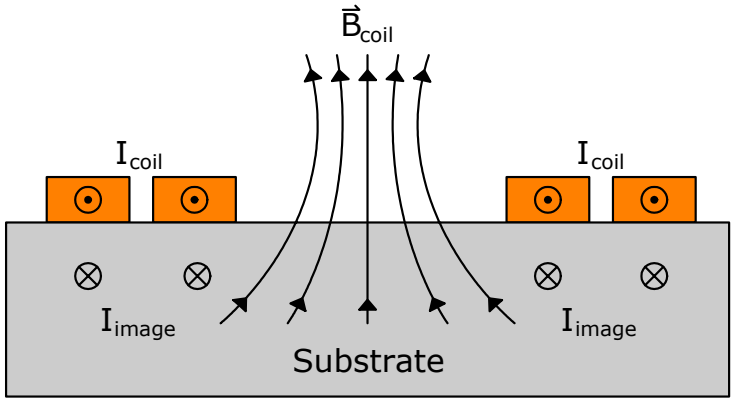


Figure 2.6: Image currents in the substrate induced by the magnetic field of the coil. The $\otimes$ and $\odot$ symbols show current into and out of the page respectively (after [47]).

planar inductor.

High substrate resistivities can reduce the magnitude of the image current and the associated energy loss. For this reason, inductors fabricated on high-resistivity substrates such as Gallium Arsenide or silicon-on-sapphire (SOS) will have higher Q-factors. However, VLSI silicon substrates are typically heavily doped to reduce their resistance and increase the immunity of CMOS circuits to latch-up, so further steps must be taken to improve the Q-factors of standard silicon-based inductors. The simplest method by which to reduce substrate loss is to design for high-value inductors. Higher-valued inductors store more energy per cycle than lower-value inductors with only a slight increase in substrate loss. However, at a certain point, the loss from the series resistance of the coils will dominate over the image current loss, thus placing a practical limit on the size of low-loss inductors. Therefore, other methods have been developed to increase local resistivity of the substrate region directly underneath the inductor. These methods include: diffusing n+ regions perpendicular to the image current into p-doped substrates [50], fabricating specially patterned ground shields beneath the inductor [51], or separating the substrate from the inductor either by lifting the inductor out of the plane of the substrate [52] or by micromachining the substrate under the inductor [53]. Q-factor improvements of 13% and 21% were reported for the perpendicular n+ diffusions and for the patterned ground shields respectively. Q-factors greater than 30 were achieved with the suspended inductor while Q-factors in excess of 80 were reported with the out-of-plane inductor. Figure

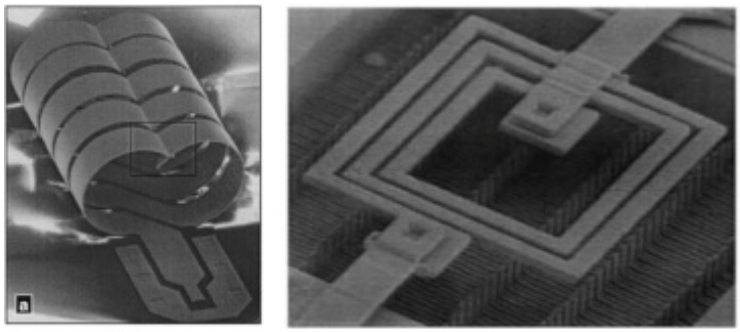


Figure 2.7: SEM micrographs of two high-Q inductors: (a) out-of-plane inductor lifted by residual sputtered thin-film stress [52]; (b) suspended micromachined inductor [53].

2.7 shows two such inductor structures designed for low substrate loss.

Interwinding Capacitance

The final element of Figure 2.4 is the capacitance between the individual windings of the inductor coil and the capacitance between the coils and the underpass traces, represented together by C_p. Since the interwinding capacitance does not couple energy outside of the inductor itself, C_p is not considered a loss mechanism. However, it does contribute to the absolute operational frequency limit known as the *self-resonant frequency* (f_{sr}). C_p, C_{sub}, and L_s will resonate together at the frequency determined by:

$$f_{sr} = \frac{1}{2\pi\sqrt{C_{total}L_s}}, \tag{2.5}$$

where C_{total} represents the contribution of the C_p and C_{sub} to the f_{sr}. Above this frequency the capacitive reactance dominates over the inductive reactance and the inductor appears capacitive. The value of this capacitance usually limits on-chip inductors to no more than a few nano-Henries. For larger inductors, the f_{sr} is too low for the inductor to be of practical use in RF circuits. Empirical formulas have been developed to model the various fringing fields associated with interwinding capacitance, however, the standard parallel plate capacitance equation (1.19) is sufficient for a first order approximation [54]. When choosing an RF spiral inductor, there is a trade-off between inductance value and f_{sr}. Reducing the winding spacing or

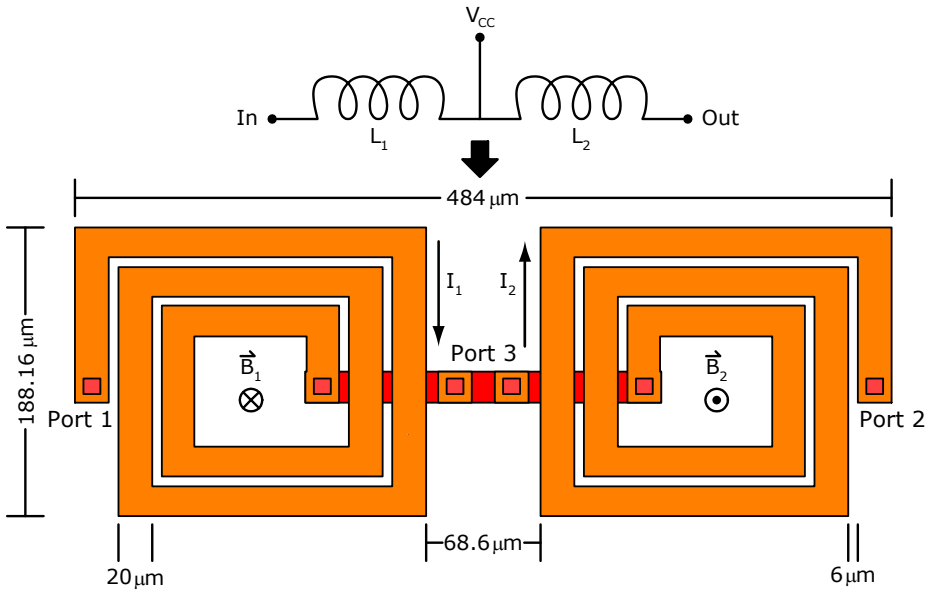


Figure 2.8: Dimensions and geometry of the differential inductor chosen for this work. The $\otimes$ and $\odot$ symbols show flux into and out of the page respectively.

increasing the number of turns in the inductor will increase the inductance at the cost of increased capacitive coupling and thus decreased f_{sr}.

EM Modeling of Spiral Inductors

The dimensions and geometry of the inductor designed for this thesis are shown in Figure 2.8. The inductor is differential in that it consists of two coils of same inductance value that share a center tap that is connected to V_{CC}. The basic rectangular inductor was included in the Motorola design kit used in this work as a parameterized cell (p-cell); unfortunately the models provided for these inductors do not accurately account for effects above ~7 GHz, which is borderline for 5-6 GHz UNII-band applications. Also, by placing the inductors close together, complex magnetic field interactions will arise that are not accounted for in the design kit model. For these reasons, the inductor layout was simulated in Agilent's Advanced Design System (ADS) 2.5-dimensional Momentum (Method of Moments) Electromagnetic Field Solver [55].

The S-parameters from the Momentum simulation are converted to Y-parameters for

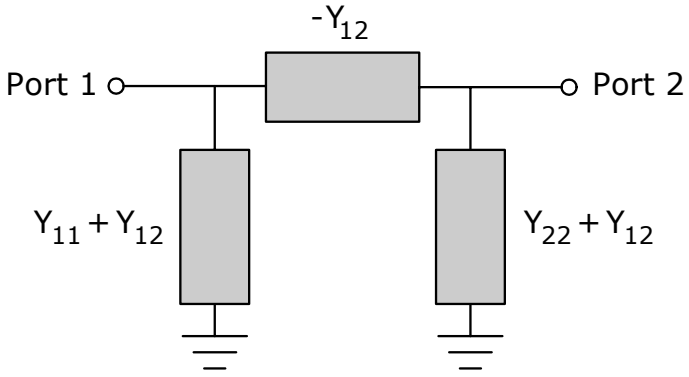


Figure 2.9: Equivalent Y-parameter π-network for monolithic planar inductor [56].

the purposes of calculating effective inductance and Q-factor. The lumped element model of Figure 2.4 can be converted to the equivalent Y-parameter π-network shown in Figure 2.9 [56]. The differential impedance between the input and output ports of the inductor (ports 1 and 2) can be calculated as follows:

$$Z_{in} = R + jX = \frac{Y_{11} + Y_{22} + 2Y_{12}}{Y_{11}Y_{22} - Y_{12}^2}. \tag{2.6}$$

Equation 2.6 can then be used to calculate the inductance and the Q-factor from the Y-parameters as follows [56]:

$$L = \frac{\mathrm{Im}(Z_{in})}{2\pi f}, and \tag{2.7}$$

$$Q = \frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})}. \tag{2.8}$$

Figure 2.8 shows the Q-factor and effective inductance calculated from the Momentum simulations of the differential inductors used in this work. Two important conclusions can be drawn from Figure 2.10. First, the Q-factor of the square spiral inductor is relatively poor. Fortunately, the peak Q-factor is centered close to the operational frequency range; however, the simulated Q at 5 GHz is only 11.2. The expected phase-noise and frequency stability of the VCOs fabricated with this inductor are expected to be correspondingly degraded. Second, the value of the inductance suffers significantly from the dual-inductor layout. Since the currents in the two coils are flowing in opposite directions, the magnetic flux for each are in opposite directions

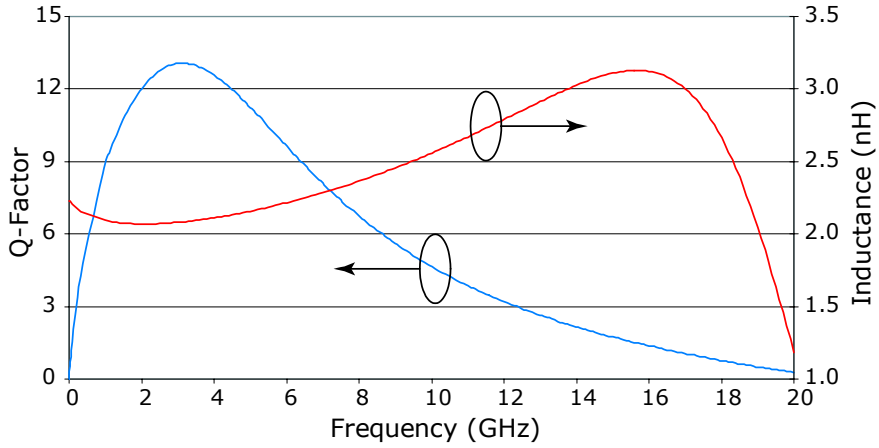


Figure 2.10: Simulated Q-factor and inductance for differential inductor used in this work.

(Figure 2.8). This leads to a cancellation of some of the field, a corresponding loss of energy storage capability, and a decrease in effective inductance. The inductors were sized to provide a differential inductance of 2.8 nH according to the design kit; however, simulation results show only 2.16 nH of total inductance for the two coils at 5 GHz, a reduction of 23%. This value of inductance will resonate at 5 GHz with a total tank capacitance of approximately 938 fF. This capacitance is supplied through the varactors, the switched capacitors, and the transistor and interconnect parasitics to be discussed in Section 2.2.3.

In order to counter this effect, differential inductors are often fabricated by combining L_2 and L_1 into a single coil, creating an *electrically* symmetric inductor layout such that the currents are flowing in the same directions. (This type of structure is described in more detail in Appendix A.) Since adjacent currents are oriented in the same direction in this type of inductor, their magnetic fields add constructively and the total inductance is increased such that a given inductance can be realized with approximately 50% less die area than the dual-inductor layout [57]. Since the loss of the inductor is related to the conductor area (Equation 2.1), reducing the area has the effect of increasing the Q-factor. Theoretically, this Q-factor improvement can be as much as a factor of two; however, typical results are closer to a 50% increase due to added via resistances and substrate coupling [58, 59]. Since there were no electrically symmetric differential inductor p-cells available at the time these designs were completed, and since time-constraints made it impossible to lay out and optimize

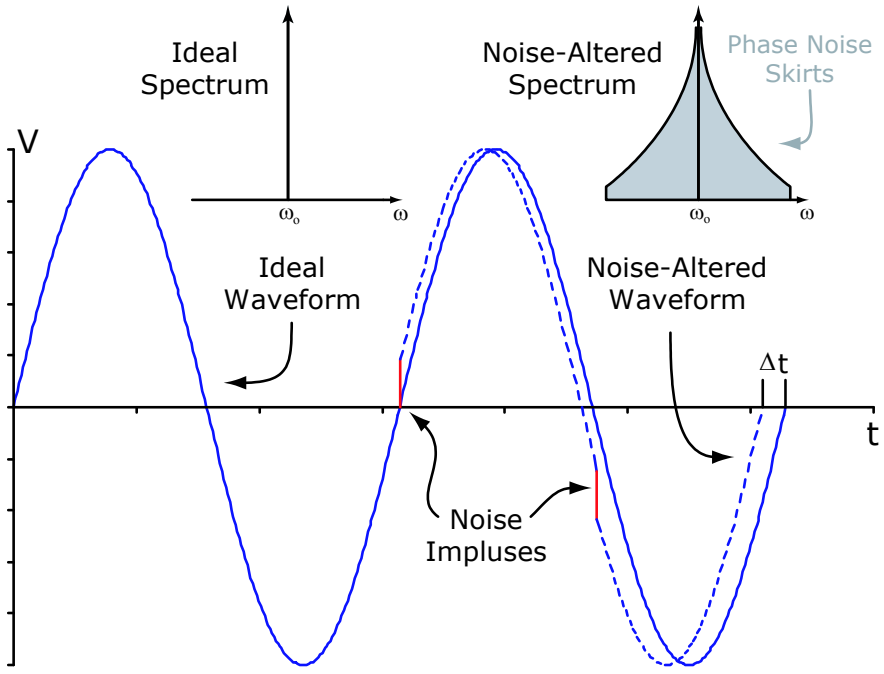


Figure 2.11: Noise-induced deviations in the ideal zero-crossings of the oscillator output waveform and the corresponding noise-skirts in the frequency-domain spectrum (after [60]).

a custom differential inductor, the differential pair of square inductors in Figure 2.8 were used. Appendix A describes the subsequent simulation results for a number of symmetric inductors designed for a second generation, higher-Q tank-circuit VCO design.

2.2.2 Oscillator Phase Noise and Reciprocal Mixing

Oscillator phase noise can be described as noise-induced deviations from the ideal zero crossings in the oscillator output waveform. The effect of injected noise on the shape of an ideal sine wave can be seen in Figure 2.11. The noise can be generated from numerous sources such as resistive thermal noise and transistor shot noise and can be assumed to occur randomly in time across the waveform. Without the addition of noise, the output spectrum in the frequency domain appears as an ideal, singular peak at the center frequency of the LC tank circuit. However, in the presence of noise sources, the deviations in the zero-crossings lead to variations in the apparent

center frequency of the oscillator and give rise to spectral "skirts" around the center frequency.

A major impact of phase noise on receiver performance is the introduction of reciprocal mixing of nearby channels with the non-ideal oscillator spectrum. Figure 2.12 shows the effect of phase noise on two received nearby in-band channels. Since the actual spectrum of the VCO can spread across multiple channels due to non-zero phase noise, the downconverted spectra of incoming channels can overlap. Large strength interferers in nearby channels can therefore potentially swamp out information in the desired channel. This is particularly critical in systems that rely on close channel spacing to maximize the number of users in a given bandwidth. To measure the potential for reciprocal mixing, phase-noise is often quantified as:

$$PN = 20\log\left(\frac{\text{Total Noise Power in a 1 Hz Bandwidth}}{\text{Peak Carrier Power}}\right), \tag{2.9}$$

with units in dBc/Hz (decibels with respect to the carrier per Hertz). Communications standards typically state the required phase noise at a given offset frequency that will provide an acceptably low level of interference due to reciprocal mixing. For example, the IEEE 802.11a standard requires a phase noise level of -107 dBc/Hz at a 1 MHz offset from the carrier frequency of the LO [61]. In order to meet these specifications, it is critical to understand the sources of phase noise in oscillators so that their effects may be mitigated.

The above discussion of Figure 2.11 is a time-domain explanation of the origins of phase noise first introduced by Hajimiri, *et al.* [60]. The time-domain description of phase noise assumes time-variance of the phase noise spectrum, i.e. the phase noise depends on the time of the injected noise. If the noise is injected close to the zero-crossing of the waveform, the phase and frequency will be significantly affected. On the other hand, if the noise is injected close to the peak of the waveform, the phase is minimally affected. An alternative view of phase noise described by Leeson assumes time-invariance of the phase noise spectrum and describes the sources of phase noise in the frequency domain. This view is the focus of the next section.

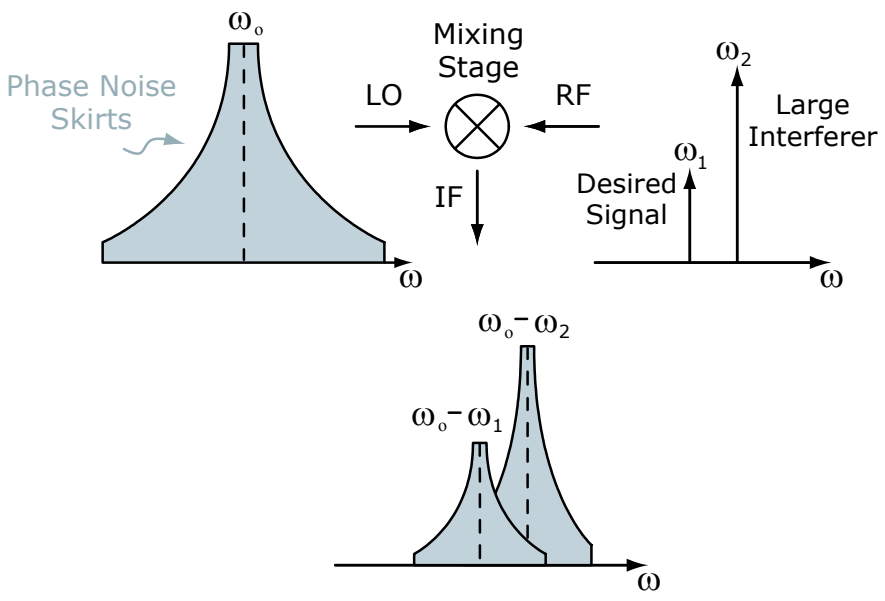


Figure 2.12: Effect of mixing an oscillator output with non-zero phase noise skirts with two closely separated incoming channels (after [2]).

Frequency-Domain Sources of Phase Noise and Leeson's Equation

Figure 2.13 shows two principal sources of phase noise in an oscillator: broadband noise that is filtered by the oscillator loop transfer function [2.13(a)] and low-frequency noise upconverted near the oscillator center frequency [2.13(b)].

Broadband noise is comprised of thermal noise from resistors, shot noise from transistors, etc. and has no dependence on frequency. For the purposes of investigating phase noise, broadband noise can be assumed to be injected into the signal path at the input of the feedback loop in Figure 1.9. This noise is then filtered by the open loop transfer function of the feedback loop. Plotting this transfer function versus frequency reveals a peak at the center frequency of the oscillator and a half-power bandwidth inversely proportional to the Q-factor of the resonator (Equation 1.6). By assuming that the only broadband noise contribution is resistor thermal noise, the noise power relative to the carrier power in a given offset frequency, $\Delta\omega$, can be determined by [3]:

$$L(\Delta\omega) = 10\log\left[\frac{2k_BT}{P_{sig}}\cdot\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right], \tag{2.10}$$

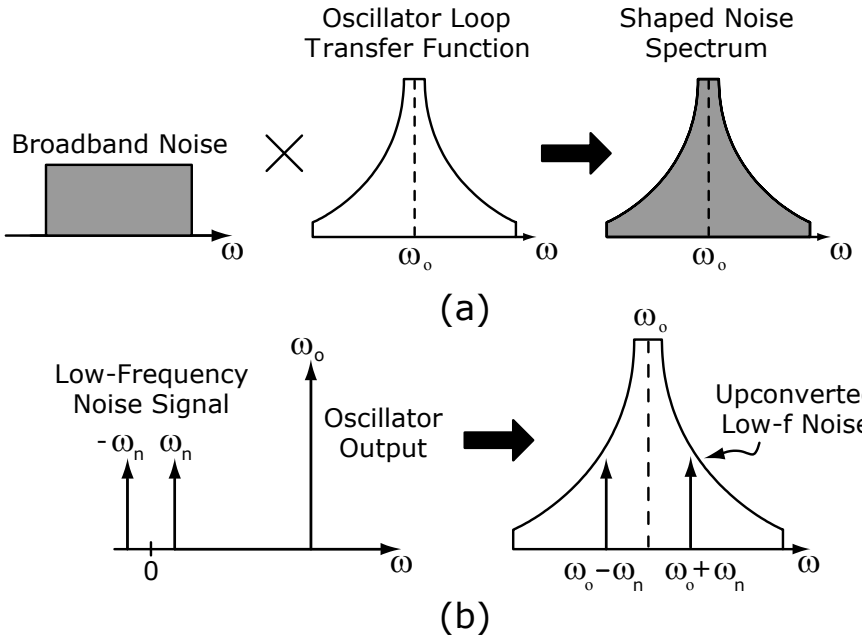


Figure 2.13: Sources of oscillator phase noise: (a) filtered broadband noise; (b) low frequency upconverted close to the oscillator spectrum (after [62]).

where k_B is Boltzmann's constant, T is the temperature in Kelvin, and P_{sig} is the output power of the oscillator at the center frequency, ω_o. This equation is also known as Leeson's original equation for phase noise. As expected, the relative noise power is inversely proportional to both the offset frequency and Q-factor of the resonator. By maximizing the Q-factor (parallel equivalent resistance) of the tank circuit, the total phase noise can be reduced.

The second source of noise can best be understood as upconverted noise due to the modulation of the center frequency of the VCO. The simplest example of this is noise on the varactor control line. Since the voltage on the control line controls the center frequency of the VCO, any noise on this line will frequency modulate the VCO. This modulation translates low-frequency noise components present in the control line into the region near the carrier frequency [Figure 2.13(b)]. Another possible source of modulation noise is the low-frequency $1/f$ noise of the current source ($\mathrm{I_{tail}}$). Noise present in the current source will modulate the bias current of the active devices in the VCO, thus modulating the center frequency [62]. Since the effect of upconverted noise is more pronounced for noise sources at low frequency, transistor $1/f$ noise is

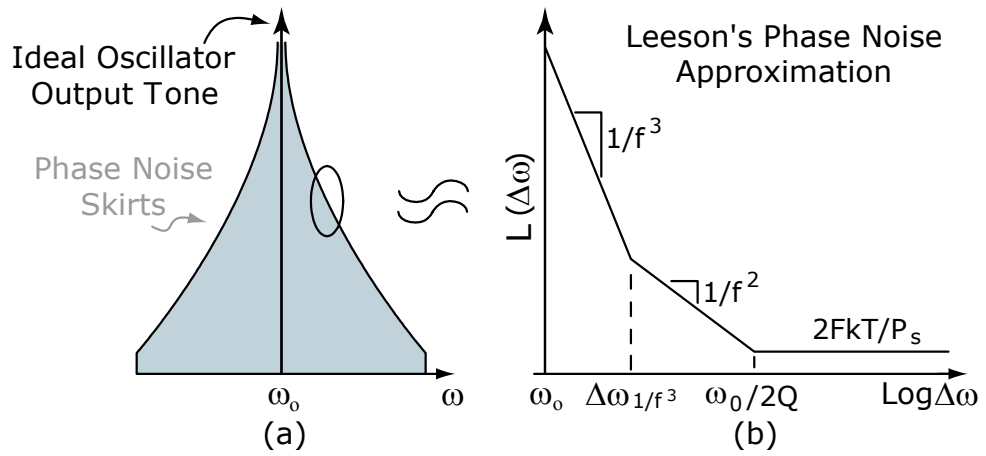


Figure 2.14: Representation of phase noise: (a) skirts around center frequency; (b) Leeson's phase noise approximation (after [3]).

particularly detrimental to phase noise.

To account for the effect of $1/f$ noise, Leeson adapted his original equation (2.10) into the following time-invariant description of phase noise [63]:

$$L(\Delta\omega) = 10\log\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\omega_{1/f^3}}{\Delta\omega}\right)\right\}, \tag{2.11}$$

where F is an empirically derived constant included to take into account broadband noise sources other than resistor thermal noise (such as transistor shot noise), and ω_{1/f^3} is an empirically determined constant related to the $1/f$ corner frequency, i.e. the frequency at which the current source noise transitions from being dominated by $1/f$ noise to being dominated by shot noise. Equation 2.11 is plotted for arbitrary values in Figure 2.14. Leeson's modified equation for phase noise can be split into three regions: the $1/f^3$ region dominated by upconverted $1/f$ noise, the $1/f^2$ region created by filtered broadband noise, and a zero slope region included to account for the absolute noise floor of the oscillator. Although it requires several assumptions and empirically derived variables, Equation 2.11 yields some insight into techniques that could reduce the total phase noise. The phase noise in all regions can be decreased by increasing the output power of the oscillator, P_{sig}. Architecture modifications to the biasing current source can reduce the contribution of $1/f$ noise; a circuit demonstrating such modifications is presented later in this chapter. The $1/f^2$ noise region

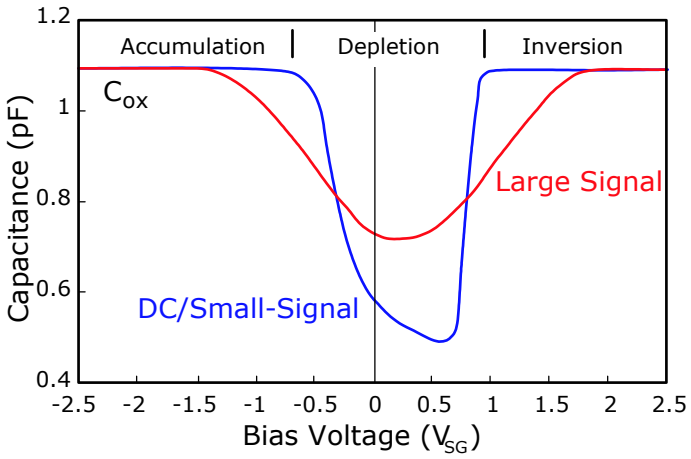


Figure 2.15: Typical small-signal and large-signal capacitance versus gate-source voltage curves for a D=S=B varactor (after [64]).

can be reduced by increasing the Q-factor of the tank circuit. In most applications and frequency regimes of interest, the inductor Q dominates the total tank loss thus the inductor Q should be maximized to minimize phase noise.

2.2.3 Frequency Tuning with MOS Varactors

As stated earlier, varactors provide the fine tuning capability of the VCO. Varactors in MOS technology can be implemented as PMOS devices that have their drain, source, and bulk connections tied to a single node (D=S=B) [64]. The capacitance between the drain-source node and the gate node can then vary with the voltage applied across the nodes as shown in Figure 2.15. In the inversion region of operation, the applied source-gate voltage (V_{SG}) is higher than the absolute value of the threshold voltage (V_{th}) and a channel of majority carriers arises between the drain and source. For the case $V_{SG} \gg |V_{th}|$, the device is considered in the strong inversion regime. In the accumulation regime, V_{SG} is negative and minority carriers build up in the channel. In these two voltage ranges, the capacitance between the bulk node and the gate node is constant and equal to the gate capacitance, C_{ox} [65].

For values of V_{SG} between the accumulation and inversion regimes, however, the population of all carriers in the channel is depleted and the capacitance drops below the static value of C_{ox}. When considering small-signal operation, i.e. where V_{SG}

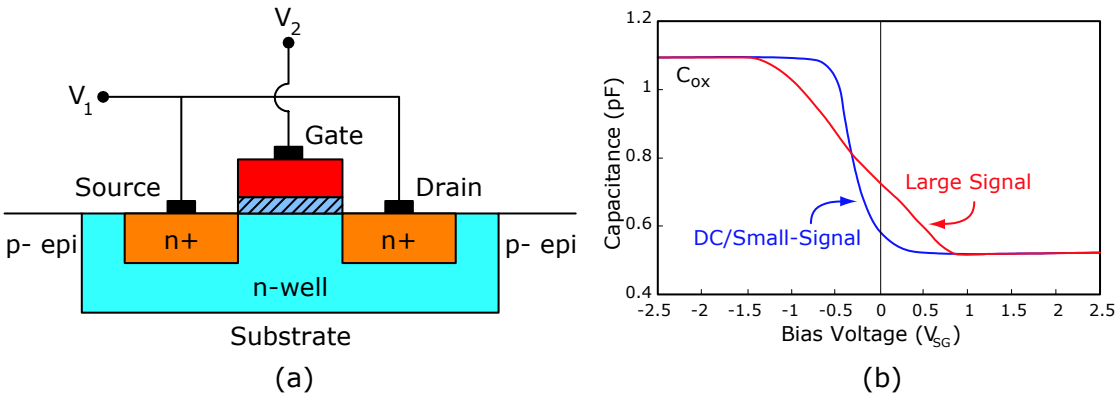


Figure 2.16: Accumulation-mode varactor: (a) cross-section of device in an n-well; (b) typical small and large-signal capacitance versus voltage curves (after [64]).

is constant with time or varies very little with time, the drop in capacitance with respect to C_{ox} in this so-called depletion regime can be significant. However, when considering large-signal operation, i.e. where the amplitude of a time-varying V_{SG} is larger than ~0.5 V, the capacitance versus average value of V_{SG} is smoothed out (Figure 2.15). This results in a decrease of the available tuning range of the varactor [64]. Since most oscillators exhibit large-signal behavior, many varactors are designed to either operate in the depletion and inversion regimes only (inversion-mode) or in the depletion and accumulation regimes only (accumulation-mode) where the voltage versus capacitance curve is monotonic and the tuning range does not suffer as significantly from the large-signal effect.

The varactors used for the VCOs in this thesis are accumulation-mode varactors; a device cross-section and large-signal capacitance versus voltage curve are shown in Figure 2.16. The accumulation-mode varactor is different from the D=S=B varactor in that the drain and source are doped n-type instead of p-type in an n-type well. In this scenario, there are very few majority carriers available to invert the channel and the inversion mode is avoided. By avoiding the inversion regime, the averaging effect due to large-signal operation does not decrease the tuning range from that of the small-signal tuning range.

Inversion-mode varactors, on the other hand, differ from D=S=B varactors in that the bulk is tied to V_{CC} instead of the drain and source. Since holes are the majority carrier for this device, inversion-mode varactors typically exhibit lower Q-factors than

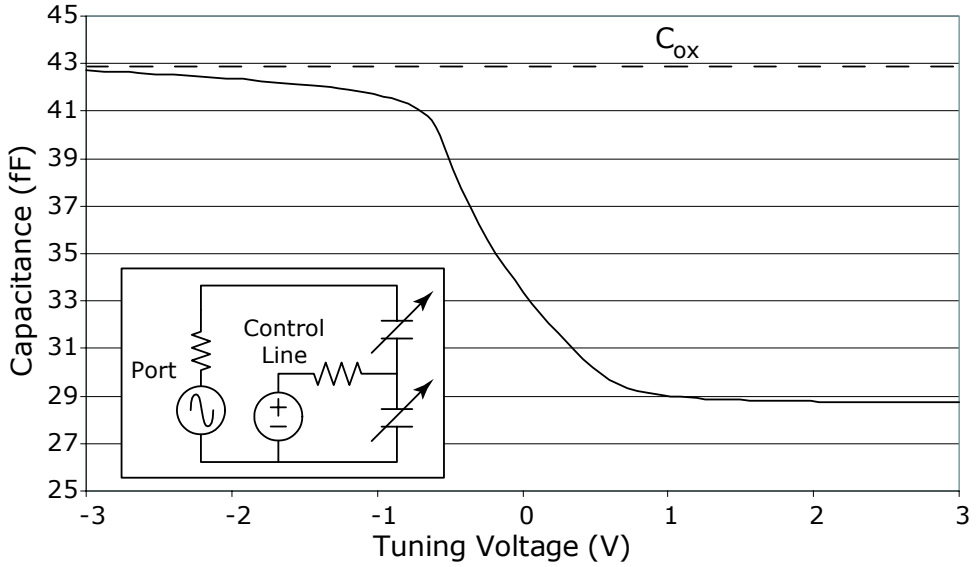


Figure 2.17: Small-signal capacitance versus voltage for accumulation-mode varactor used in this work. Inset: one-port S-parameter simulation schematic used to obtain the C-V curve.

accumulation-mode varactors due to the lower mobility of holes versus electrons. Also, the extra bulk contact increases the die area requirements for the inversion-mode varactor over the accumulation-mode varactor for the same tuning range [65].

The small-signal capacitance versus voltage tuning curve for the pair of differentially connected varactors as used in one of the VCO designs in this thesis is presented in Figure 2.17. The center of the tuning range occurs at a voltage around -0.25 V and the capacitance maximum is approximately equal to that of the gate-to-channel capacitance, C_{ox}. In the case of these varactors, the frequency tuning range is directly related to the applied varactor control voltage, i.e. the higher the voltage, the lower the capacitance and thus the higher the frequency. For this work, varactors were chosen to provide 100 MHz of fine frequency tuning across each of the three sections of the UNII band (5.15-5.25 GHz, 5.25-5.35 GHz, and 5.725-5.825 GHz) – an approximate tuning range of only 2%. The small tuning range requires a low ratio of varactor-supplied capacitance to the remaining fixed circuit capacitance, thus the choice of minimum sized varactors with a length of 1.75 μm and a width of 9 μm that, together, have an average capacitance of 36 fF.

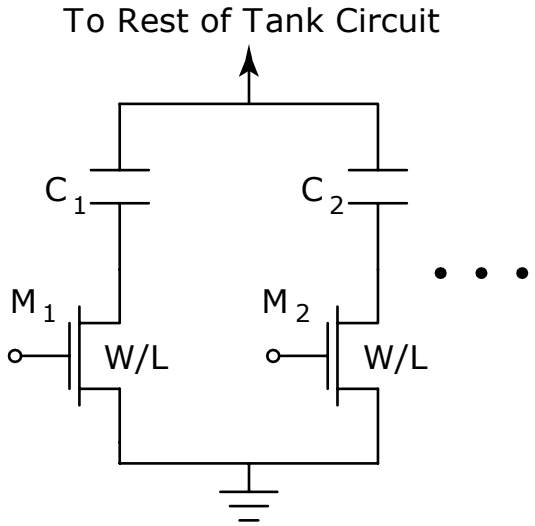


Figure 2.18: Schematic of NMOS switched capacitors.

2.2.4 Frequency Switching with MOS Switched Capacitors

The capacitor/switch combination used in this work to complete the LC tank circuit is shown in Figure 2.18. To create the switched capacitor, a static capacitor (e.g. C_1) is placed in series with an NMOS transistor (e.g. M_1) that acts as a switch. If the gate voltage of the NMOS switch exceeds the threshold voltage (V_{th}), a channel is formed between the drain and source and the switch is effectively closed. When the switch is closed, the fixed capacitor will be connected in parallel with the tank circuit and the added capacitance dictated by the size of the static capacitor will lower the center frequency of the VCO by a discrete amount. For this design, the standard supply voltage of 1.8 V is used to turn close the switch. Any applied voltage less than V_{th} will result in an open switch condition and the capacitor will be effectively removed from the tank. For this design, a gate voltage of 0 V is used to close the switch.

The VCO shown in Figure 2.2 could be simplified by removing the coarse tuning capability of the switched capacitors and simply increase the varactor size relative to the inductance so that they could tune across the entire UNII band (5.15 GHz-5.825 GHz). However, this will result in an excessive VCO tuning gain. The VCO tuning

gain, K_{VCO}, is given by:

$$K_{VCO} = \frac{\Delta f_o}{\Delta V_{control},} \tag{2.12}$$

where Δf_o is the change in VCO center frequency for a given ΔV on the varactor control line. Assuming an effective tuning range, ΔV, of -1.8 V to +1.8V, the K_{VCO} for a VCO that tuned over the entire UNII band without the help of switched-capacitors would be 187.5 MHz/ V. With such a high value for K_{VCO}, noise present on the VCO control line can result in undesirable fluctuations of the output frequency. Also, in PLL applications, the gain of the VCO (along with the gain of the phase detector and loop filter) is directly related to the bandwidth of the PLL. The consequence of large PLL bandwidths is the possibility of false locking to high-frequency harmonics of the reference frequency that would normally be filtered out by a lower gain, lower bandwidth PLL [66]. By using the switched capacitors to switch between the three UNII sub-bands and by reducing the tuning range to tune only within the 100 MHz of these bands, the K_{VCO} can be reduced to ∼28 MHz/ V. Therefore, the switched-tank approach increases the immunity of the VCO to noise on the control line and decreases the likelihood of false locking in a PLL.

There are two important considerations when designing the RF switch: the on-state resistance of the switch and the off-state junction capacitance of the transistor [67]. In CMOS technologies, the on-state resistance is dominated by the resistance of the polysilicon gate and can be minimized by using minimum length and large width devices (large W/L ratios). Unfortunately, increasing gate width leads to larger gate capacitance which can be significant in the off-state of the transistor. This large capacitance is in series with the static capacitor and will add parasitic capacitance to the tank when the switch is open[1]. For this work, the designed tuning range in each sub-band was small and the added capacitance was not a significant issue. Therefore, large gate widths of 160 μm split into 8 fingers of 20 μm each were used to reduce the on-state resistance. However, the large junction capacitance made it difficult to design the center frequencies of the different switched states of the VCO since any design modification to one of static switched capacitors would also shift the center frequencies of all of the other states.

[1]Ring-shaped transistors, such as those described in [68], can reduce the junction capacitance for a given size but were unavailable in the available HIP6WRF process.

2.3 -G_m Transistor Amplifier

As shown in Figure 2.2, the amplification necessary to cancel the loss through the tank circuit is supplied by two npn heterojunction bipolar transistors (HBTs). This section discusses the specific device technology used for the transistors and the advantages for using HBTs over MOS devices as the -G_m amplifiers in a low-noise VCO.

2.3.1 Device Technology

The specific nature of the -G_m amplifier is dictated by the IC process chosen for the VCO design. As discussed previously, the VCOs in this work were designed in Motorola's 0.18 μm BiCMOS HIP6WRF process. HIP6 has five standard Cu metal interconnect layers in addition to the topmost copper "bump" layer discussed in Section 2.2.1. In addition to the inductor and accumulation mode varactor discussed in Section 2.2.3, there are two other HIP6 passive elements used in this work: a thin film Tantalum resistor with a sheet resistance of 50 Ω/sq and a metal-insulator-metal (MIM) static capacitor with a capacitance per unit area of 1.6 fF/ μm^2.

BiCMOS processes such as HIP6 offer the potential for mixed RF and digital circuit design by offering both bipolar and CMOS active devices in the same technology. Characteristics of the two specific active devices used in this work, low threshold voltage (V_{th}) MOSFETs and heterojunction bipolar transistors (HBTs), are shown in Table 2.1 [69]. (High-voltage MOSFETs and traditional BJTs are also available in this process but were not utilized in this work.)

The short (0.18 μm) channel for the NMOS devices allows for high speed operation, which is evident in the high values of f_T and f_{MAX}. f_T represent the maximum frequency at which the current gain of the transistor is greater than unity, and f_{MAX} denotes the maximum frequency of oscillation. The low threshold voltage for the NMOS devices facilitates low-power operation with a standard supply voltage of 1.8 V. In this work, the NMOS devices are used in the aforementioned switched capacitor tank and as the active devices in the biasing current mirrors (to be described later). Likewise, a PMOS device is used as an active load in one of the oscillator biasing circuits.

Active Device	Critical Parameters			Application in VCO
Low Threshold Voltage NMOS	Oxide Thickness	Å	35	Switch transistors and biasing current source transistors
	Min Gate Length	µm	0.18	
	Threshold V	mV	350	
	Peak f_T	GHz	60	
	Peak f_{MAX}	GHz	50	
Low V_{th} PMOS	Oxide Thickness	Å	35	Active current mirror load
	Min Gate Length	µm	0.18	
	Threshold V	mV	350	
	Inherently low f_T and f_{MAX}			
SiGe HBT	Min Emitter W	µm	0.25	-Gm oscillator core transistors
	Peak Current Gain		120	
	Early Voltage	V	90	
	Peak f_T	GHz	50	
	Peak f_{MAX}	GHz	110	

Table 2.1: Characteristics of HIP6WRF active devices used in this work (after [69]).

The -G_m transistor core, on the other hand, is designed using a pair of *npn* SiGe:C HBTs. Like the *npn* BJT, the *npn* HBT is a bipolar junction device with an *n*-doped collector region, a *p*-doped base region, and an *n*-doped emitter region. The significant difference in the HBT versus the BJT is that a very finely controlled amount of Ge is alloyed with the Si in the base via a chemical vapor deposition (CVD) technique [70, 71]. Since the intrinsic band gap of Ge is less than that of Si, bandgap of the base can be engineered such that there is a gradient in the conduction energy band across the base from the emitter to the collector regions. This gradient establishes a constant acceleration field for carriers injected from the emitter across the base into the collector. This acceleration field vastly improves the speed (f_T and f_{MAX}) of the HBT over the BJT. The f_{MAX} of HBTs also often outperforms that of FET transistors and, in the HIP6 process, the HBTs are more than twice as fast as the FET devices. It should be noted here that f_T and f_{MAX} are figures of merit and many other factors determine the practical operating frequency limit; however, the 5-6 GHz range of the UNII band is well within the high f_T and f_{MAX} ranges of the transistors.

In addition to the frequency performance there are three other important advantages of HBTs over FET devices in RF oscillator circuits. First, HBTs offer superior $1/f$ noise performance over both BJTs and FETs [72]. $1/f$ noise is attributed to carrier surface trapping in defects in the semiconductor used to fabricate the transistor [73, 74]. These defects are most common at the interfaces between surfaces such as the oxide to semiconductor interface in a MOSFET. Since the primary transport path for carriers in FETs is laterally along the oxide/Si surface interface while typical HBT transport paths are vertically through the thin base/emitter and base/collector surface interfaces, the probability of carrier trapping is higher in the FET than in the HBT [75, 76]. Therefore, the $1/f$ noise, and thus the magnitude of the close-in $1/f^3$ region of phase noise, is expected to be higher in oscillators using FET devices versus those using HBTs. Second, broadband shot noise and thermal noise are reduced in the HBT compared to that of the FET [77]; thus the magnitude of the $1/f^2$ region of phase-noise is also reduced in HBT oscillators. Finally, HBTs have a higher transconductance for a given bias current (G_m/mA) than FET devices. HBT oscillators will consume less current to sustain oscillations for a given amount of tank circuit loss.

Combined, these properties justify the SiGe:C HBT as an ideal choice for a -G_m oscillator amplifier. The next sections describe the design, layout, and testing of two such oscillators: the first is designed for low power consumption and the second is designed for a high output power.

2.4 Design 1: Low Power Consumption

Low power consumption is a critical design consideration for battery-operated mobile applications such as cellular telephones and laptop computers. Reducing power consumption maximizes the time between battery charges for these devices. The VCO presented in this section is designed for such low power applications.

2.4.1 Schematic

The schematic for the switched-tank, low power consumption VCO is shown in Figure 2.19. The differential inductor (L_1 and L_2), the accumulation mode varactors (C_5 and C_6), and the MOS switches are identical to those in Figure 2.2 and are described in the previous sections. However, the base bias node and I_{tail} from Figure 2.2 are replaced by the base bias and emitter current mirror circuits seen in Figure 2.19. These bias circuits, including the PMOS active load used for automatic gain control, are described in the Section 2.4.4 along with design choices made with respect to the power consumption of the transistors. The next section covers the simulation methods used to determine the performance of the VCO shown in Figure 2.19.

2.4.2 Simulation Method

All simulation results presented for the VCO designs in this thesis were obtained using SpectreRF, a component of the Cadence Design Suite [78]. All of the circuit components are simulated as p-cells models from the HIP6 process design kit with the exception of the inductors. As was discussed in Section 2.2.1, the inductor p-cells were simulated using a separate EM solver. The S-parameter data from these simulations was included as a generic three-port S-parameter component (n3port). This component allows simulation of the S-parameter data in both the time and frequency domains.

SpectreRF periodic steady-state (PSS) analysis was used to determine the frequency and time domain operation of the oscillator. PSS has three components: a DC solver that computes the steady-state solution at time zero; a transient simulation that roughly establishes the period and shape of the oscillator output waveform; and a shooting method that more accurately determines the oscillator period and waveform shape. Since the oscillator is an autonomous circuit, i.e. there is no input source to drive oscillations in the circuit, an extra step must be taken to ensure that the circuit oscillation starts up. In the fabricated oscillator, thermal noise or power supply transients are sufficient to "jump-start" the circuit into oscillation. However, these signals are not present in the simulated circuit, so an ideal 1 aF capacitor is placed between the $V_{out}+$ node and ground and given an initial condition of 1.8001 V. The

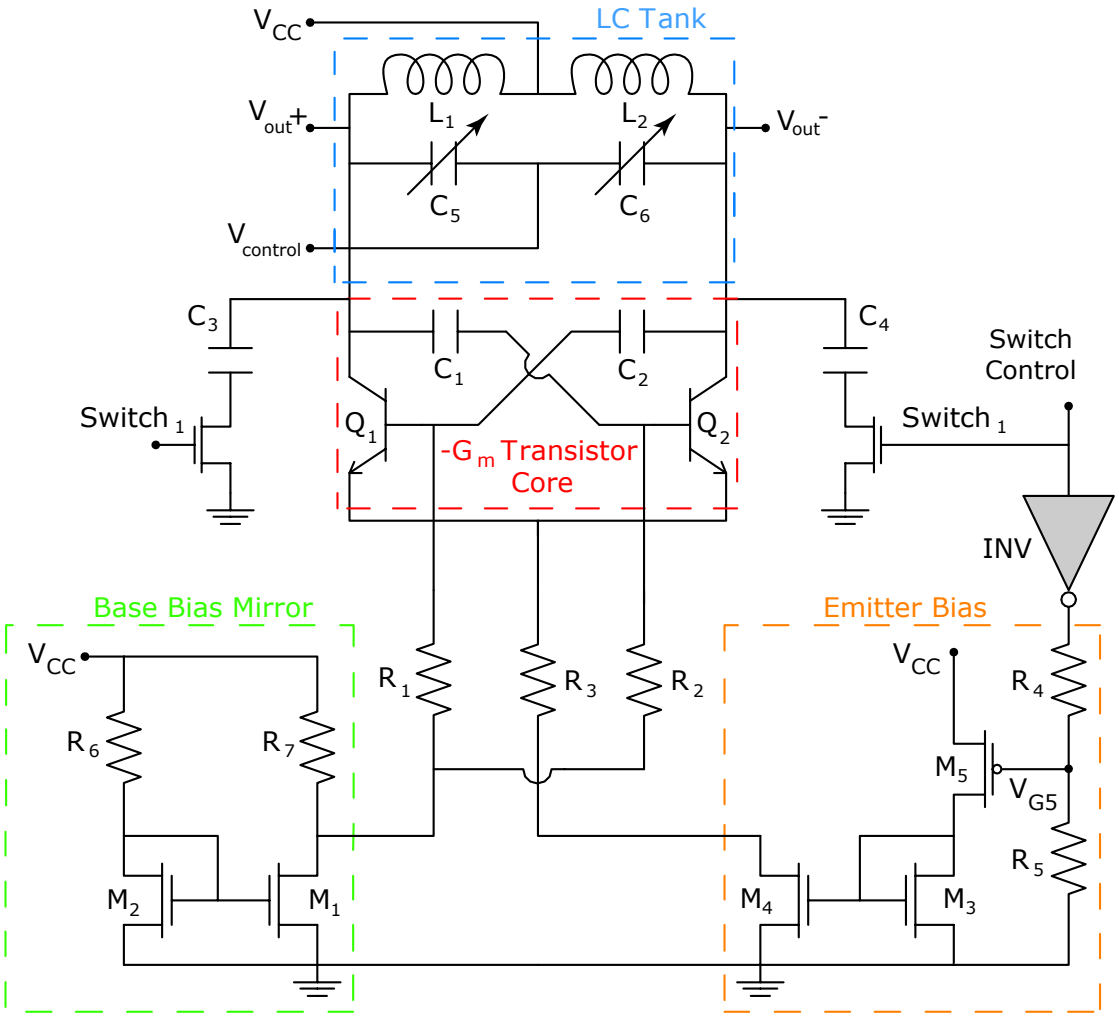


Figure 2.19: Schematic of switched-tank VCO with variable current mirror bias for reduced power consumption.

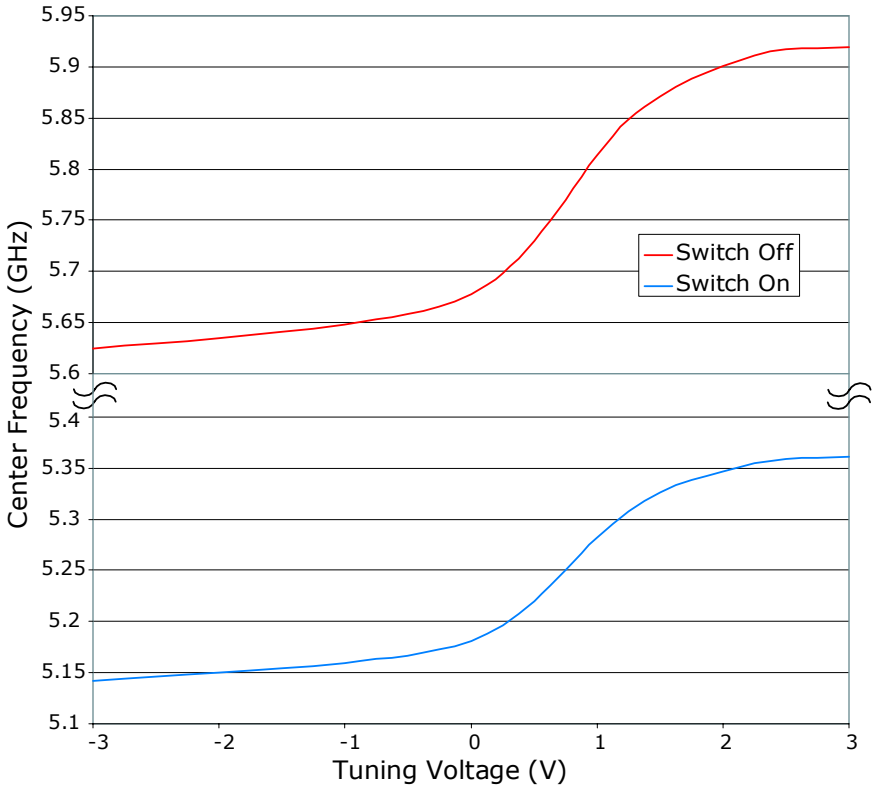


Figure 2.20: Capacitance versus tuning voltage for mirror-biased VCO.

capacitor will not affect the output frequency or amplitude due to its small size but the non-physical initial condition (the DC voltage at this node must be less than 1.8 V due to the inductor voltage drop) causes the DC solver to generate an incorrect, non-equilibrium, steady-state solution. This perturbation from steady-state is sufficient to start the oscillator in the subsequent transient solution.

Once the transient solution has run for a user-determined amount of time ($\sim$25 ns for the simulations presented here), PSS makes an estimate of the period and shape of the waveform. The period estimate and the condition of the circuit at the end of the transient simulation are fed to the shooting method which iteratively simulates the circuit over one estimated period attempting to establish a more precise value for the circuit period and wave shape. The results of this simulation that are of primary interest include the center frequency and the output oscillation amplitude.

2.4.3 Frequency Tuning

A simplified tuning scheme with only one switch was used in this design since the primary focus was the demonstration of the variable active load in the collector current bias. (The alternate high-output power design presented in the next section has two switches.) The tuning ranges corresponding to the two switched states were designed to be: 5.15 GHz - 5.35 GHz (the two lower UNII sub-bands) for the switch-on state and 5.625-5.925 GHz (a liberal coverage of the highest UNII sub-band) for the switch-off state. To account for the 200 MHz of tuning range, the varactors used in this design have a length of 1.75 μm and a width of 18 μm and together provide an average capacitance of 72 fF. The capacitance value for the two identical switched capacitors, C_3 and C_4, is 417 fF and the frequency versus tuning voltage for the two switched states is shown in Figure 2.20. The center of the tuning ranges is approximately 750 mV which is shifted from the small-signal tuning range center of -250 mV (Figure 2.17).

2.4.4 MOS Current Mirrors and Transistor Biasing

- **Base Bias Current Mirror**

The base-bias current mirror supplies the base current and the base voltage to the transistors. The base voltage must be set so that the transistors operate in the forward active region, i.e. the base-emitter junction must be forward biased ($V_{BE} \gtrsim$ 0.7 V) and the base-collector junction must be reversed biased ($V_{BC} \lesssim 0.5$ V). A MOS current mirror similar to that used in the VCO is shown in Figure 2.21. Low-voltage MOSFET transistors are used in the place of HBTs for the current mirror since they require less voltage headroom across the transistor to be operating in their active region. The reference current for the mirror is set by the voltage drop across the resistor, R_1. This voltage drop also sets the gate voltage of both transistors, and, if the transistors are identical, a current of equal magnitude to the reference current flows through the second transistor. By increasing the size of the second, or mirror, transistor by the mirror ratio, x, the current through the second transistor can be increased by a factor of x. The mirror current determines the voltage drop across resistor R_2 and thus the voltage at the drain node of the mirror transistor (Figure

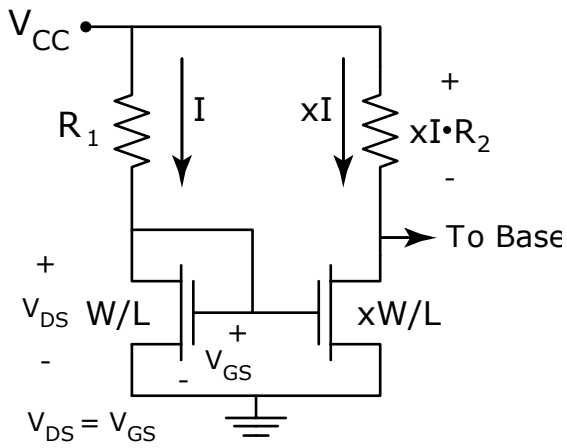


Figure 2.21: Typical MOS current mirror with mirror ratio x.

2.19). This voltage is then used to set the base voltage for each of the HBTs.

For each VCO design, the reference resistor was 10 kΩ and the mirror ratio was set to 1. The mirror current for these values is approximately 160 μA and the second resistor was set to 3.5 kΩ to supply a base bias voltage of 1.2 V. This voltage is sufficient to maintain a forward bias across the B-E junction. In addition, a small amount of current is drawn from the mirror transistor into the bases of each of the HBTs. The base currents are typically only a few tens of μA, therefore the mirror current requirement is very small. The base currents flow from the mirror into the transistor bases through a large RF blocking resistor. These 2 kΩ resistors serve to block RF power from being shorted to ground through the low impedance mirror transistor and do not drop significant voltage due to the relatively low base currents. The value of the base current is determined by the relation of the base current to the collector current through the DC current gain, β:

$$I_B = \frac{I_C}{\beta}, \tag{2.13}$$

where I_C is the collector current set by the emitter bias current mirror described in the next subsection

- **Emitter Bias Current Mirror with Active Load**

The emitter bias current mirror is primarily intended to provide a biasing current as opposed to a biasing voltage. Therefore, the resistor in series with the mirror transistor is removed and the mirror current is directly coupled to the emitters of the HBTs. The collector current, I_C, of the HBT is related to the current at the emitter, I_E, by the following equation:

$$I_C = \frac{\beta}{\beta + 1} I_E. \tag{2.14}$$

In addition, the reference resistor is replaced by an active PMOS load that provides a reference current that depends on the switched state of the VCO, as will be explained later in this section.

The bias current mirror sets the transconductance of the BJT according to:

$$G_m = \frac{I_C}{V_T}, \tag{2.15}$$

where V_T is the thermal voltage which is approximately 26 mV at room temperature. By increasing the emitter current, the transconductance can be increased and the negative resistance available to cancel the equivalent tank resistance can be increased. Since the output voltage amplitude is related to the excess gain above what is required to exactly cancel the tank resistance, increasing the collector current will increase the output voltage swing according to:

$$V_{out} = 2 I_C R_{eq}, \tag{2.16}$$

where R_{eq} is the equivalent parallel resistance of the tank. The output swing will increase with collector current until the peak voltage at the collector reaches $2 \cdot V_{CC}$ or until the transistor is limited by an inherent nonlinearity. If the output is limited by the tank circuit impedance, the oscillator is said to be *current-limited*. If the gain is sufficient to push the output voltage to the limits of the active range of the transistor, the oscillator is said to be *voltage-limited*.

To reduce the current consumption of this design, the oscillator is operated in the current-limited regime. Another advantage of operating in the current-limited regime is that the waveform is not clipped by the saturation points of the transistor and the waveform is closer to an ideal sine wave and thus more spectrally pure. However, power consumption and output voltage swing are not the only factors to consider when

choosing the collector current of the HBTs; transistor noise must also be considered.

Recall that I_C is related to I_B through the DC current gain, β. Since transistor $1/f$ noise spectral density is proportional to $I_B^{1.9}$ [79], it is critical to reduce I_B as much as possible for a given I_C. This is done by biasing the transistor at a collector current that offers the maximum β. Increasing the size of the transistor also has the effect of lowering the $1/f$ noise. Therefore large transistors biased at maximum β will offer the maximum noise performance for a given collector current. The transistors chosen for this design have a relatively large area ($W_{emitter} \times L_{emitter}$) of 0.5 μm $\times$ 40 μm to minimize noise. There are two detriments to the large transistor size. First, the bias current required to operate the transistor at peak f_T increases with device size. However, the f_T of this transistor at the selected bias current is $\sim$33 GHz. This value of f_T exceeds the generally accepted thumbrule of 5 times the maximum oscillation frequency (5.825 GHz). Second, the parasitic junction capacitance of the HBTs adds to the total tank capacitance and can effect the output frequency. As long as the other tank components are tuned accordingly, the junction capacitance effect on the tank can be mitigated.

Figure 2.22 shows the simulated β versus collector current for the HBT used in the low power consumption VCO. As is evident in the figure, the peak β occurs at a collector current of approximately 1 μA. Since this current is far too small to supply the transconductance needed to cancel the loss of the tank circuit, a higher collector current of 2.1 mA was chosen to bias the HBTs[2]. The β at this current is a reasonably high value of 102 and is located on a relatively flat section of the curve so that small collector current fluctuations will not significantly impact the β value.

One of the consequences of operating the VCO in the current-limited regime is that changes in the parallel equivalent tank circuit resistance will have an effect on the output voltage swing of the oscillator. This is not a problem for non-switched-tank VCOs since their Q-factors are relatively constant (ignoring slight Q-factor changes versus tuning voltage in the varactors). However, the Q-factor of the switched-tank VCO tank changes with each switched capacitive state. By switching capacitance into the tank circuit, the finite Q-factor of the capacitor and switch will lower the overall Q-factor of the tank and the oscillation output will decrease if the collector

[2]This current was chosen for the VCO operating state in which the switch is closed and the varactor is tuned to the center of its capacitance range.

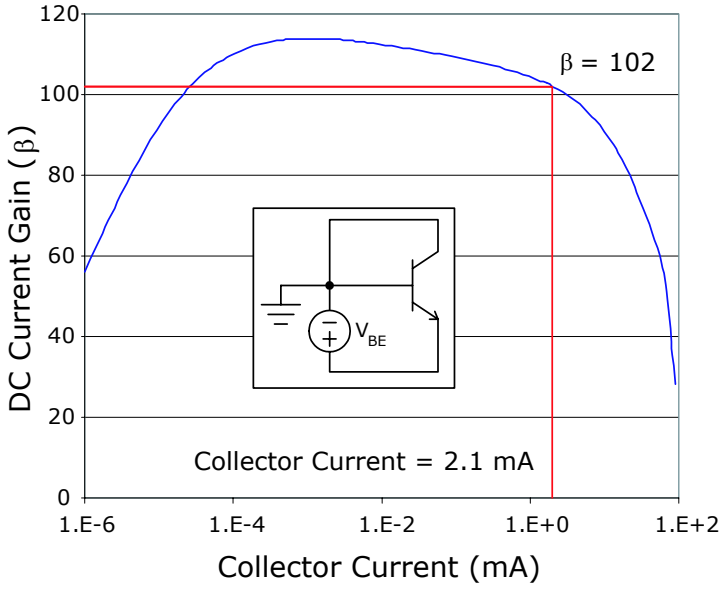


Figure 2.22: DC current gain versus collector current for low-power consumption VCO HBT Inset: schematic of β simulation circuit.

current is held constant. Figure 2.23 shows how the peak output voltage (measured differentially from node $V_{out}+$ to $V_{out}-$) varies with the varactor tuning voltage for a switched-tank VCO design similar to that shown in Figure 2.19 with the active PMOS current source load, M_5, replaced by a fixed resistor. Since the fixed resistor will set the emitter bias current to a certain value regardless of the switch state, the output swing will change depending on the switch control voltage. With this bias scheme, the output voltage swing changes by more than 225 mV between switched states ($Switch_1$ on and off).

By incorporating an active load into the emitter current source, however, the emitter current can be changed to maintain a constant output voltage between switched states. Figure 2.24 shows the simulated I_D versus V_{SG} ($V_{CC}-V_{G5}$) curve for the PMOS transistor used as the active load in the emitter current source. By changing the voltage on the gate of the PMOS device (V_{G5}), the drain current can be changed, i.e. the higher V_{G5}, the lower the current. For instance, in the switch-on condition, the Q-factor of the tank is the lowest and the gate voltage should be low to produce a high tail current. By inverting the switch control voltage of 1.8 V to 0 V, V_{G5} is set to 0 V (there is no drop in the resistive divider for a 0 V input). V_{SG} is thus set

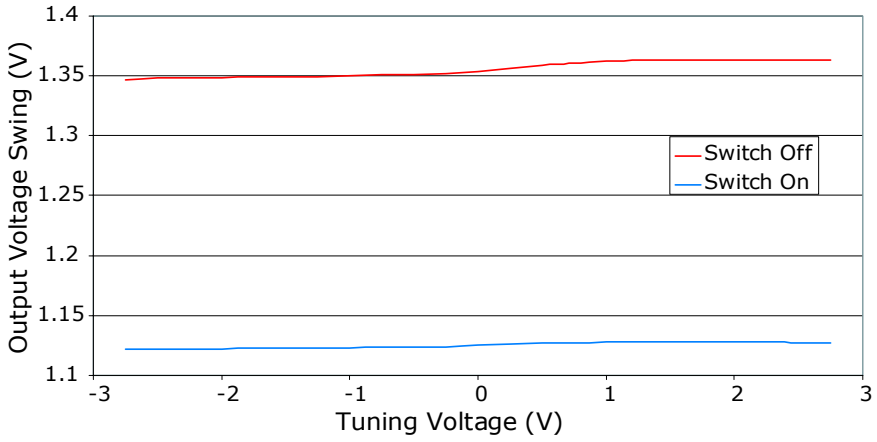


Figure 2.23: Peak differential output voltage swing versus tuning voltage for switched-tank VCO without active load bias compensation.

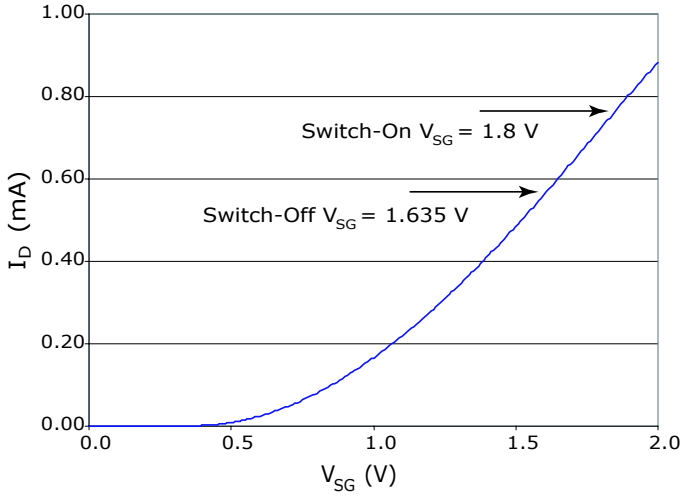


Figure 2.24: I_D versus V_{SG} for the PMOS transistor used as the active load in the emitter bias circuit.

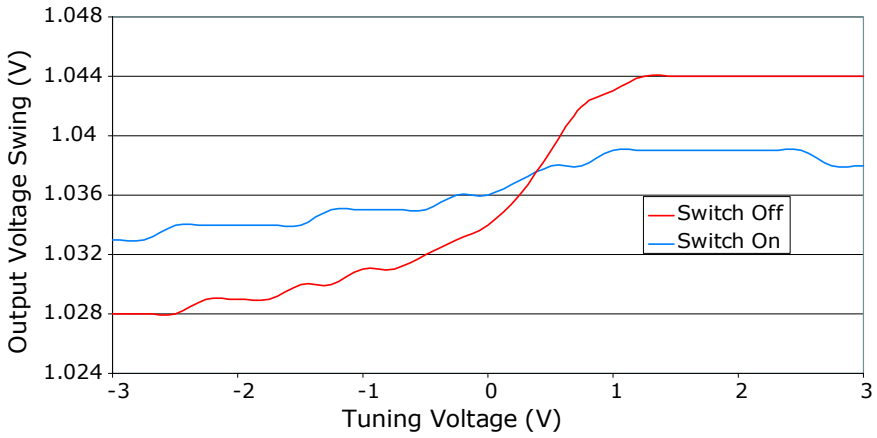


Figure 2.25: Output voltage swing versus tuning voltage for low power consumption switched-tank VCO.

to 1.8 V and the drain current is set to 720 μA. The mirror ratio in this circuit is six, therefore the current through the mirror transistor is 4.2 mA. When this current is split between the two HBTs, the final emitter current is 2.1 mA.

On the other hand, for the switch-off condition, the tank Q-factor is the highest and the gate voltage should be lower to maintain the same output voltage swing. In this case, the switch control voltage of 0 V is inverted to 1.8 V. The resistive divider circuit (R_4 and R_5 in Figure 2.19) converts the 1.8 V from the inverter into 165 mV at the gate of the PMOS load. V_{SG} drops from 1.8 V to 1.635 V and the current drops to 588 μA. The mirror transistor converts this current to 3.5 mA, which splits to 1.75 mA per HBT. Figure 2.25 shows the output differential peak voltages versus tuning voltage with the PMOS active load. The maximum voltage change is only ~6 mV, and the voltage swings are identical at the center of the voltage tuning range.

2.4.5 Transient Simulation Results

The time-domain differential voltage output calculated by PSS for the low power-consumption VCO is shown in Figure 2.26. Both of the switch-off and switch-off states are shown with the varactor tuning voltage set to 750 mV. As is evident in the figure, both waveforms are close to pure sine waves, thus containing little harmonic content. The amplitudes, as discussed earlier, are nearly identical and the peak

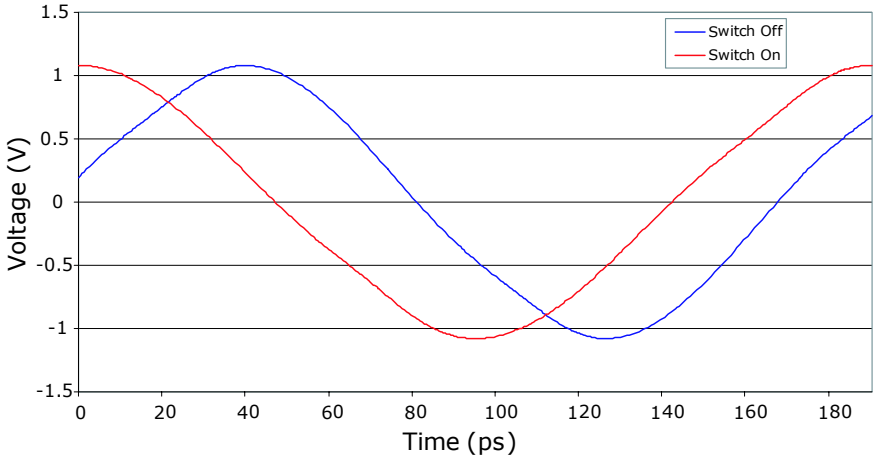


Figure 2.26: Comparison of the differential output as calculated by PSS for the switch-off and switch-on states for the low-power VCO.

voltage for both is close to 1 V. As expected, the period for the switch-on state is slightly longer than the period for the switch-off state due to the lower frequency.

2.4.6 Phase Noise Results

The phase noise was simulated using the periodic noise (pnoise) analysis available in Spectre as an additional feature of the PSS analysis. Once PSS has determined the periodic steady state, the initial conditions are perturbed with noise signals corresponding to the noise sources in the system. The resulting noise power in a 1 Hz bandwidth is then calculated for a range of offset frequencies from the carrier.

The phase noise results for the low-power VCO in the switch-off and switch-on states is shown in Figure 2.27. The simulated phase noise of the switch-on state at 100 MHz is -107 dBc/Hz, at the edge of the specification for 802.11a. However, close inspection of Figure 2.27 reveals a phase noise of 60 dB *above* the carrier at an offset of 1 Hz. This is obviously a non-physical result that may be a result of the device models used in the SpectreRF simulator. Also, the switch-on state exhibits superior phase noise performance over the switch-off state. Since the switch-on state should present a lower Q-factor and a higher biasing current, it was expected that the phase-noise performance would be worse. Motorola has indicated that some problems exist with the noise models for their components in HIP6 and it is believed that these flaws

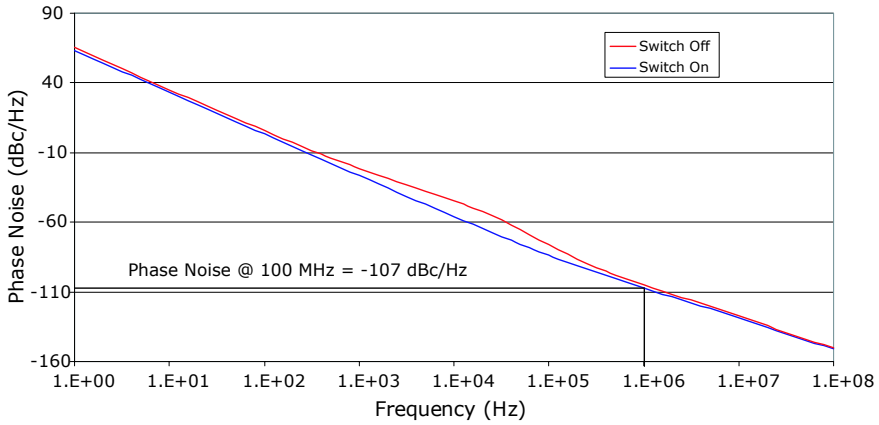


Figure 2.27: Phase noise of low-power VCO for switch-off and switch-on states.

are responsible for the high close-in phase noise.

2.4.7 Buffer Amplifier

For characterization purposes, the output power and tuning range of the oscillator are measured using a spectrum analyzer that has a standard termination impedance of 50 Ω. To prevent the measurement equipment from degrading the loaded Q-factor of the tank, a differential buffer must be placed between the output of the VCO and the 50 Ω load of the measurement equipment. The buffer used in this work is a pair of simple common-collector amplifiers shown in Figure 2.28. The buffer circuit is biased to draw approximately 1.5 mA per HBT. While this configuration offers no appreciable power gain (∼1.0 dB), the input and output impedances are the more critical specifications of the circuit. The single-ended input impedance was simulated at 5.5 GHz to be approximately 1.25 kΩ looking into the bases of each of the buffer transistors, and the output impedance is approximately 90 Ω looking back into each of the transistor emitters. The high input impedance should not significantly load the Q-factor of the tank circuit and the low-output impedance should match well to the low input impedance of the test equipment. Another important factor for the buffer amplifier is the 1-dB compression point, i.e. the power handling capability of the amplifier. Since the output power from the VCO is relatively high, it is critical that the buffer amplifier not compress and distort the signal. The 1-dB compression point of this amplifier was measured to be around 0 dBm, high enough to handle the

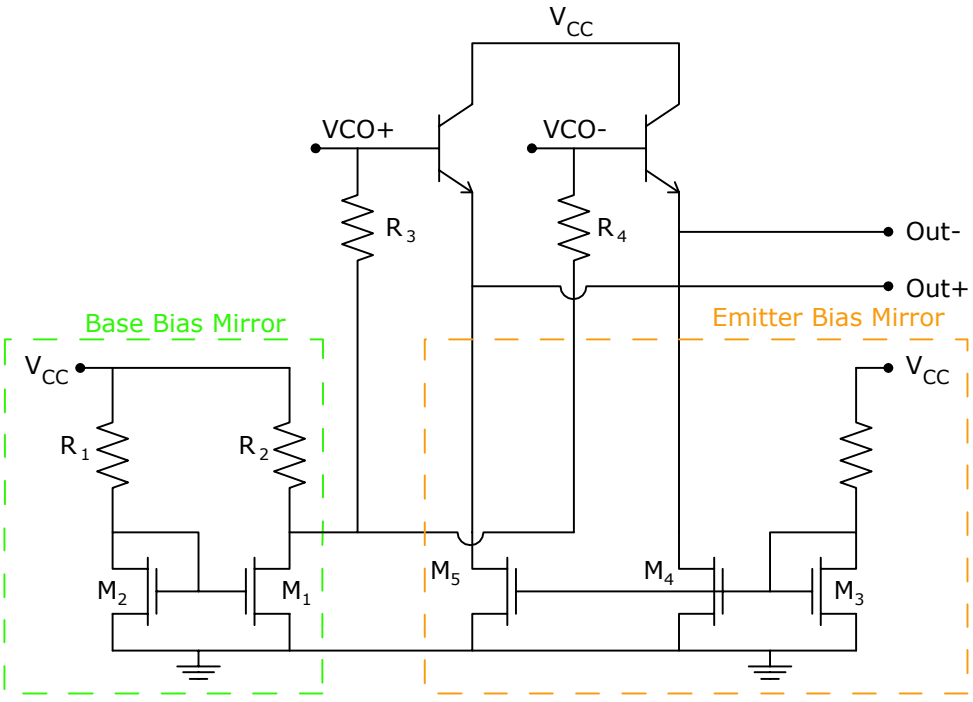


Figure 2.28: Common-collector buffer amplifier schematic used in this work.

output power of the VCO without compression.

2.4.8 Layout

The layout of the low power switched-tank VCO and buffer amplifier is shown in Figure 2.29. The die area of the circuit is 0.756 mm × 1.04 mm. The majority of the metal traces are defined in metal layers 3-5 due to their lower resistance compared to metal layers 1 and 2. A major concern during the layout process was maintaining symmetry between the two halves of the differential circuit. Efforts must be made to keep the traces for each half the same length and width so as to equalize the parasitic capacitance and resistances on each half of the circuit. Any difference in layout between the differential paths will result in a degradation of the CMRR of the circuit.

The bondpads were laid out to facilitate on-wafer probe testing as opposed to board-level testing of a packaged die. This resulted in some constraints on the placement

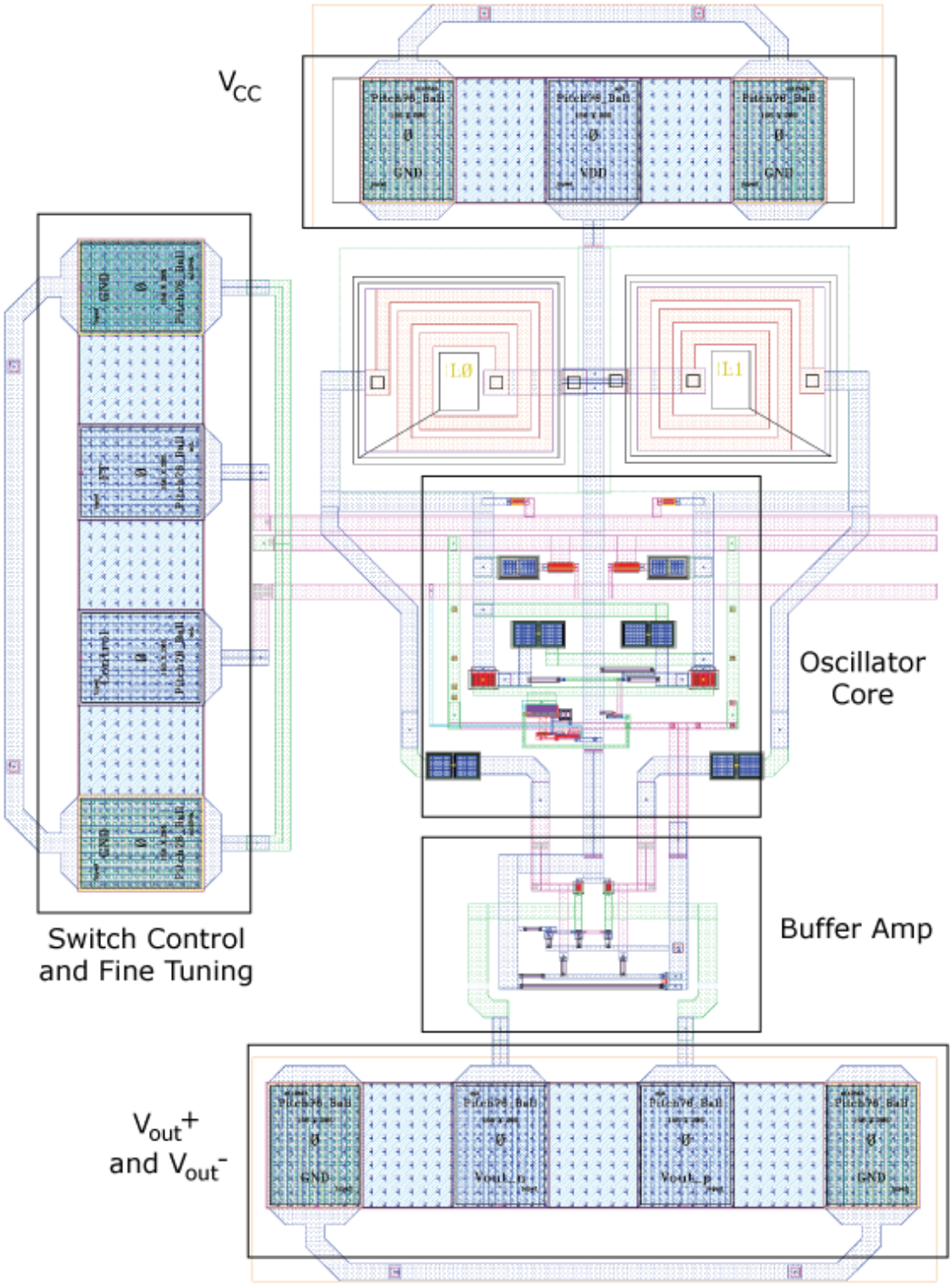


Figure 2.29: Layout of low-power VCO and buffer amplifier for fabrication in the HIP6 process. Die area = 0.756 mm × 1.04 mm.

and number of the bondpads that could be used. The $V_{out}+$ and $V_{out}-$ outputs from the buffer amplifier were connected to pads laid out for probing via a ground-signal-signal-ground (GSSG) wafer probe. The switch control and varactor control traces are connected to pads laid out for probing via a four-point DC probe. The outside pair of DC pads were connected to ground to help ensure a uniform ground throughout the substrate and the two innermost DC pads were connected to the varactor control line and to the switch control line. Since there was only four-point DC probe available at the time of testing, the V_{CC} bias for both the buffer amplifier and the VCO was applied using the signal probe tip of a ground-signal-ground (GSG) probe.

2.5 Design 2: High Output Power

As shown in the receiver architectures of Figures 1.1, 1.7, and 1.8, the oscillators on the receive side of the circuit are most often used as the LO source for the downconversion mixers. Since most mixers fundamentally act as switches, the ideal LO input is a high amplitude square wave [2]. Since high-frequency square waves cannot typically be synthesized with low phase noise, a sinusoidal LO is typically used instead. Sinusoids can approximate a square wave input if the amplitude of the wave is sufficiently high compared to the turn-on voltage of the switches in the mixer. Therefore, oscillators that provide a maximum output voltage swing are optimum for use as LO sources for mixers. Also, recall that the phase noise is inversely proportional to the output signal level of the VCO (Equation 2.11). By increasing the output power, the phase noise of the circuit should decrease. The following sections discuss the design changes made to the previously described VCO and the motivations behind the modifications.

2.5.1 Schematic

The schematic for the high-output power VCO is shown in Figure 2.30. There are two significant differences between this design and the low-power design. First, an additional pair of switches was added.. This allows for 4 different switched-capacitor states, of which, three correspond to the three sub-bands of the UNII spectrum. Second, the emitter bias circuit has been replaced with a single on-chip planar inductor.

This eliminates the $1/f$ noise contribution and DC voltage drop associated with the NMOS tail current source in the previous design. This should serve to reduce the phase noise and increase the voltage swing of the modified VCO design.

2.5.2 Frequency Tuning

As mentioned above, this design incorporates two pairs of switches so that the three sub-bands of the UNII band can be tuned independently. Figure 2.31 shows the simulated tuning ranges for each of the three switched states of interest in the UNII band (the state in which Switch_1 is off and Switch_2 is on was not used). The value of the capacitor that corresponds to Switch_1 is 372.5 fF and the value of the capacitor that corresponds to Switch_2 is 158.1 fF. As is evident in Figure 2.31 , the majority of each sub-band of the UNII band is covered by the linear portion of the tuning curve for each switched state. The available tuning range decreases as the frequency decreases due to the added fixed capacitance switched into the tank. By increasing the amount of fixed capacitance, the varactor represents a smaller fraction of the total tank capacitance and its ability to tune the tank circuit is therefore reduced. The addition of the second switch also required the use of a smaller size transistor in this design versus the low-power design (0.5 μm $\times$ 10 μm versus 0.5 μm $\times$ 40 μm). The high capacitance of the large transistor would have required prohibitively small switched capacitors to set the center frequencies of each switched state. Lowering the transistor size has the unfortunate side effect of increasing the $1/f$ noise; however, the change in size was required if the inductor size was to be kept consistent between the two designs.

2.5.3 Inductive-Degeneration and Transient Simulation

As previously mentioned, the inductive degeneration of the -G_m transistor emitters serves to lower the phase noise and increase the available headroom to the HBT thus increasing the output voltage amplitude. Since there is no collector current control, the VCO operates in the voltage-limited regime, i.e. the output amplitude is limited by transistor nonlinearity rather than the current available to compensate for the loss of the tank circuit. The collector current biases at steady-state to a

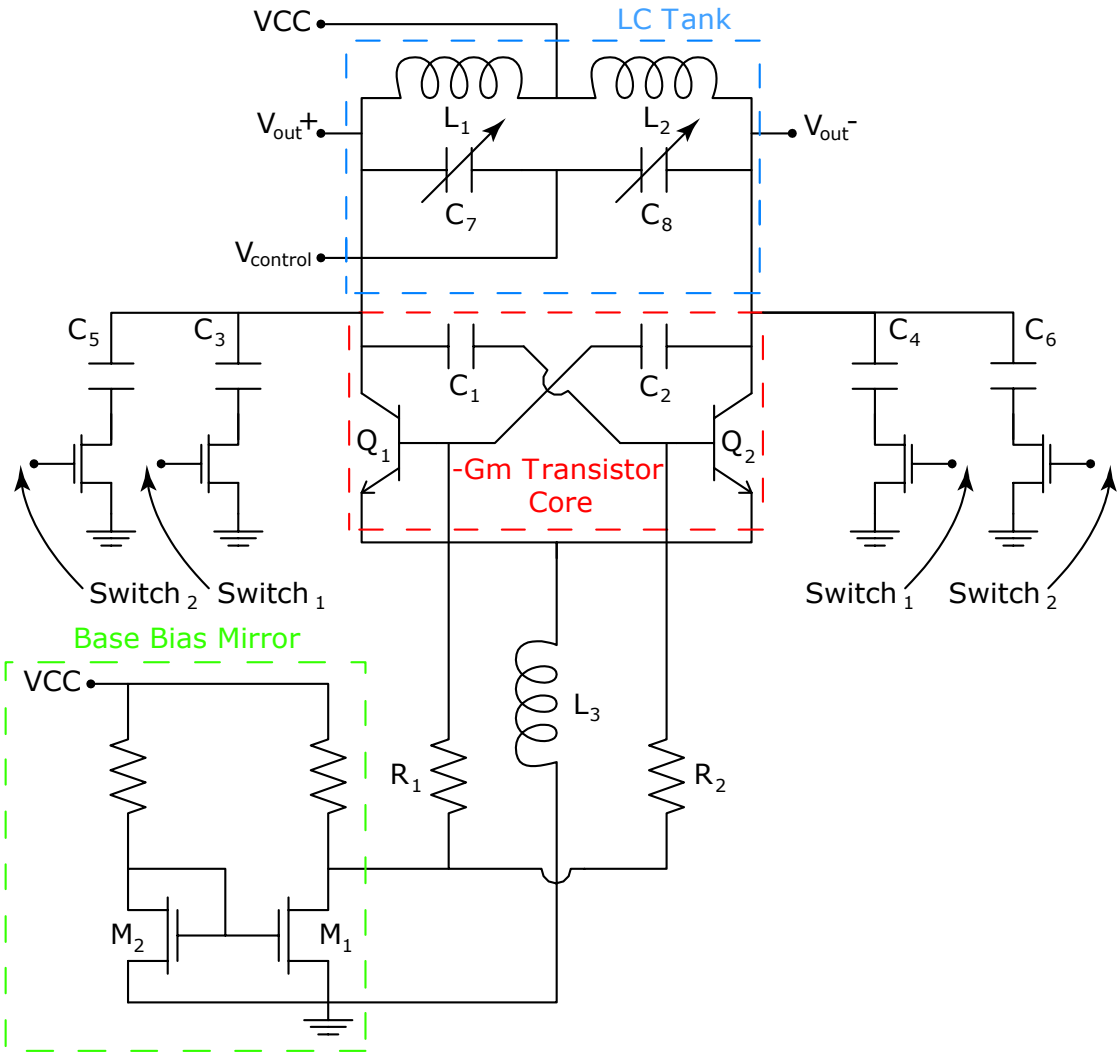


Figure 2.30: Schematic of the inductively-degenerated, high output power VCO.

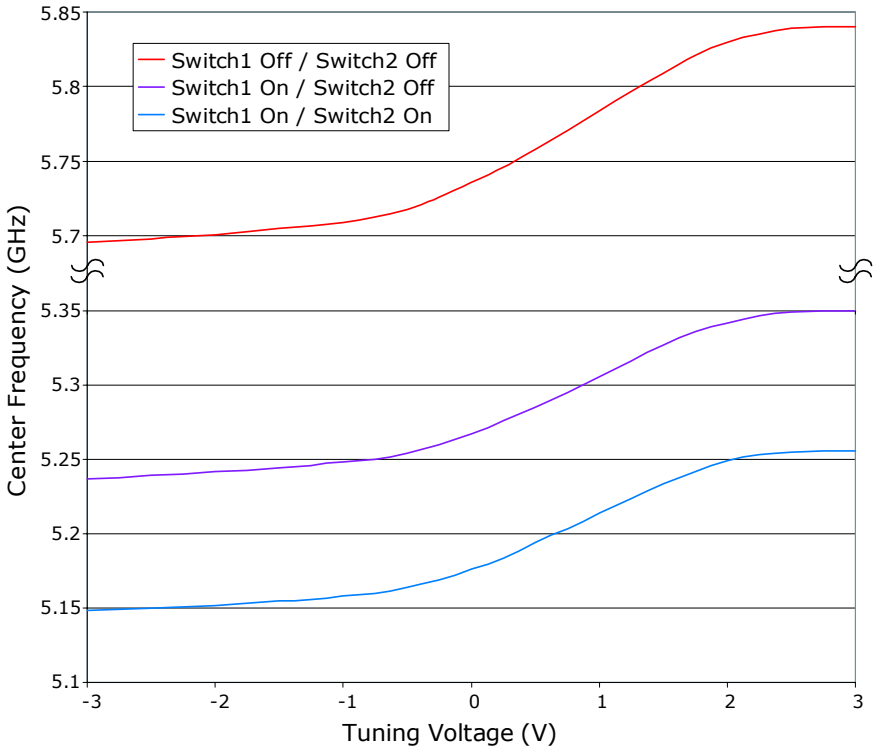


Figure 2.31: Simulated tuning ranges for the three switched states of interest in the high-output power VCO.

value determined by Equation 2.16, where V_{out} is the nonlinearity voltage limit of the oscillator. For this circuit, the nonlinear dependence of the transconductance on the output voltage limits the output power of the oscillator. In other words, as the voltage swing increases, the transconductance of the HBT becomes limited and does not increase linearly with I_C as stated by Equation 2.15. The amount of available transconductance is not sufficient to completely cancel the high loss of the tank circuit in this case, therefore the voltage swing cannot reach the theoretical limit of $2 \cdot V_{CC}$.

In order to ensure that the low impedance of the emitter inductor does not load the HBT differential pair, it should be sized to parallel resonate with the parasitic emitter capacitance of the HBT at the second harmonic of the center frequency [80]. Since the parasitic capacitance is expected to be small, a large inductor value is required to resonate at the second harmonic of the approximate center of the UNII band. (Assuming that the center of the UNII band is 5.5 GHz, this harmonic is at 11 GHz.) In simulation, this circuit would not oscillate for inductor values below 1.5 nH; however, very little change in the output amplitude was noticed for inductor values greater than 4 nH. For this reason a 4.5 nH inductor was chosen to degenerate the emitters of the HBTs.

The differential output swing over one period of oscillation at a tuning voltage of 750 mV with both of the switches in the off state is shown in Figure 2.32. The 5.2 V peak-to-peak swing produced by this oscillator configuration far exceeds that of the low-power VCO. However, the steady-state collector current is 6.35 mA for each transistor, resulting in a total current consumption of 12.7 mA. Another down side of this circuit is the increased die area of the large degenerating inductor relative to the current mirror circuit used in the previous design.

2.5.4 Phase Noise

By increasing the output voltage swing and eliminating the $1/f$ noise from the tail current source, it can be expected that this design would have superior phase noise performance when compared to the low-power VCO. However, the simulated phase-noise of this VCO shown in Figure 2.33 indicates that this is not the case. There are several possible explanations for this result First may be the aforementioned problems with Motorola noise models. Second is the increased current consumption of

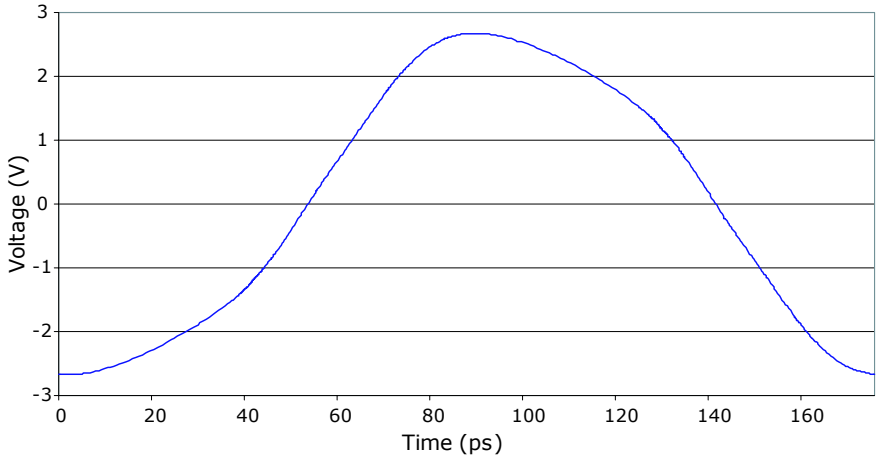


Figure 2.32: Differential output swing over one period for the high-output power VCO.

the oscillator. Recall that the $1/f$ noise spectral density of the HBTs is proportional to $I_B^{1.9}$. By increasing the biasing current, the phase noise in the $1/f$ region due to the HBT pair will increase. Also, the transistor sizes are decreased which will lead to additional noise from the HBT pair. Finally, the use of the four switches compared to the two switch tank of the low-power VCO will lead to a lower Q-factor of the tank for each of the switched-states.

2.5.5 Layout

The layout of the high output power VCO is shown in Figure 2.34. The die area of the circuit is 0.739 mm $\times$ 1.35 mm. The only difference in the pad arrangements for this design versus the previous layout is the GSSG pad layout used for the V_{CC} biasing. The two signal pads of this layout allow the buffer amplifier and VCO core to be biased from separate pads. This could help diagnose problems with the circuit if the bias levels during testing do not match the expected values from simulation. This modification was possible in this design due to the placement of the buffer amplifier. Symmetry concerns made it difficult to run two separate V_{CC} lines in the previous design so it was decided, in that case, to simplify the layout and share the V_{CC} between the buffer and the VCO.

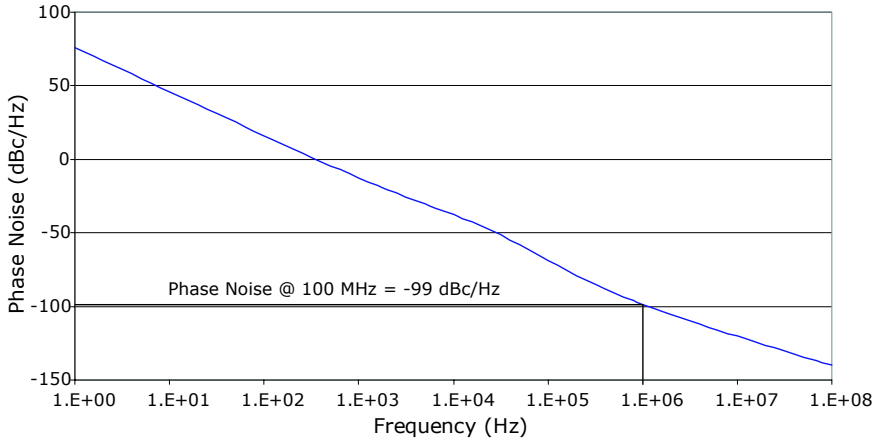


Figure 2.33: Phase noise of the high-output power VCO.

2.6 Comparison of Simulated Results

Table 2.2 compares the critical performance values of the two VCO designs. At a cost of about 10 mA of additional current consumption, the high output power VCO more than doubles the output voltage swing of the low power VCO. Despite the change in Q-factors between the switch states, the output voltage swings for both designs are nearly identical for each frequency range. In the low power design, the voltage is kept constant by an active load incorporated into the current mirror that facilitates automatic control of the HBT biasing current. In the high output power design, the voltage swing is limited by the nonlinearity of the transistor. Therefore, the HBTs "self bias" to a DC current that will result in the output swing of 5.2 V depending on the Q-factor of the tank circuit. Simulated phase noise barely meets 802.11a specifications in the low-voltage case and does not meet the specification in the high-power case. However, there may be a significant amount of error in the phase noise simulations due to noise model problems, and measured results are required to draw conclusions as to the actual phase noise performance of the two designs.

2.7 Measured Results

The circuit layouts of Figures 2.29 and 2.34 were submitted to Motorola (now Freescale) for fabrication on a HIP6 engineering run. Die photos of the fabricated chips with

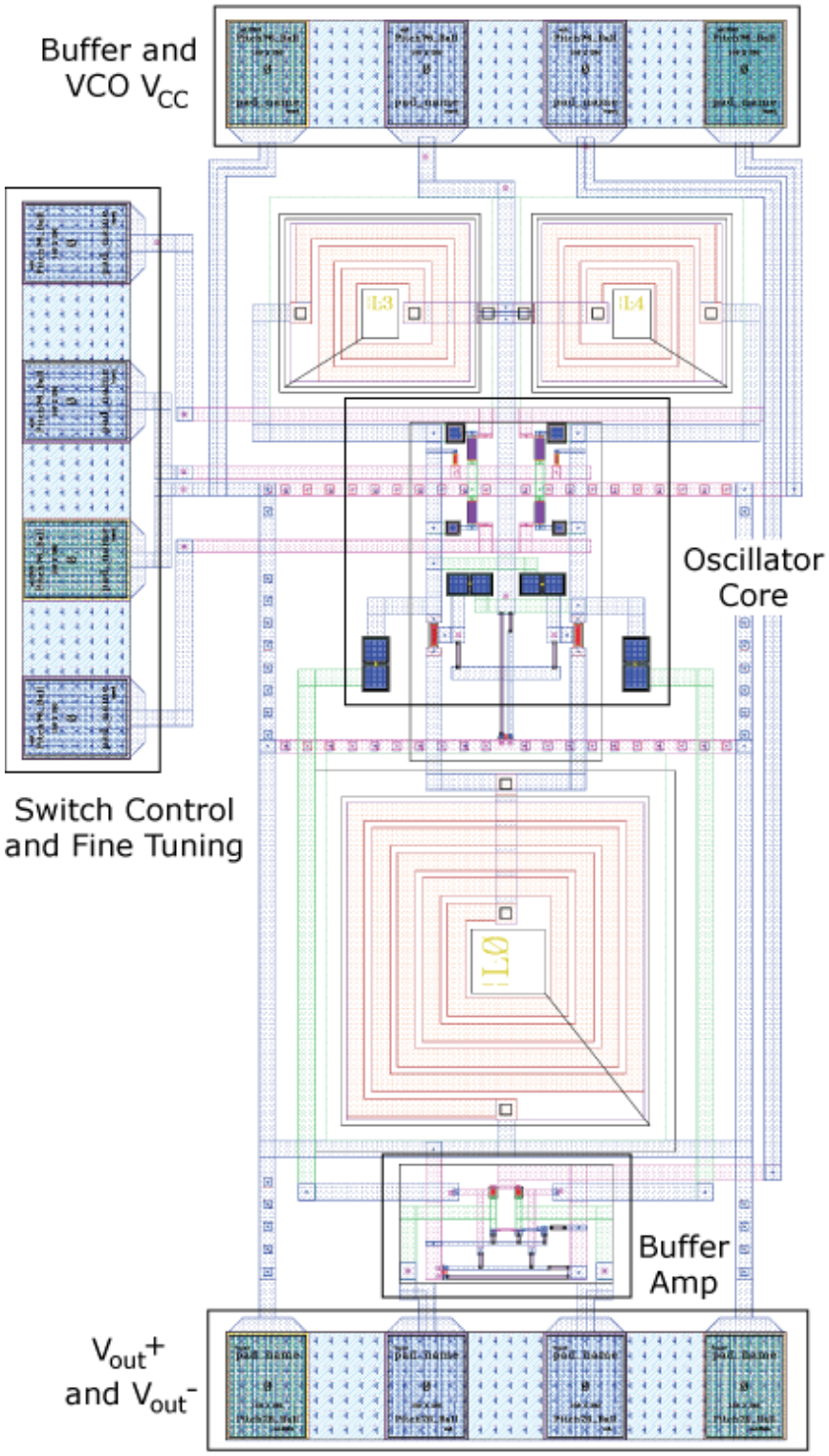


Figure 2.34: Layout of high output power VCO and buffer amplifier for fabrication in the HIP6 process. Die area = 0.739 mm × 1.35 mm.

Design Title	Frequency Ranges	Current Consumption	With Buffer	Output Swing	Phase Noise @ 100 MHz
Low-Power	5.14 - 5.36 GHz	4.2 mA	7.2 mA	2.06 V	-107
	5.625 - 5.925 GHz	3.5 mA	6.5 mA	2.06 V	-105
High-Output Power	5.15 - 5.25 GHz	14 mA	17 mA	5.2 V	-100
	5.25 - 5.35 GHz	13.5 mA	16.5 mA	5.2 V	-99
	5.7 - 5.84 GHz	12.7 mA	15.7 mA	5.2 V	-99

Table 2.2: Comparison of selected simulated results for the two VCO designs.

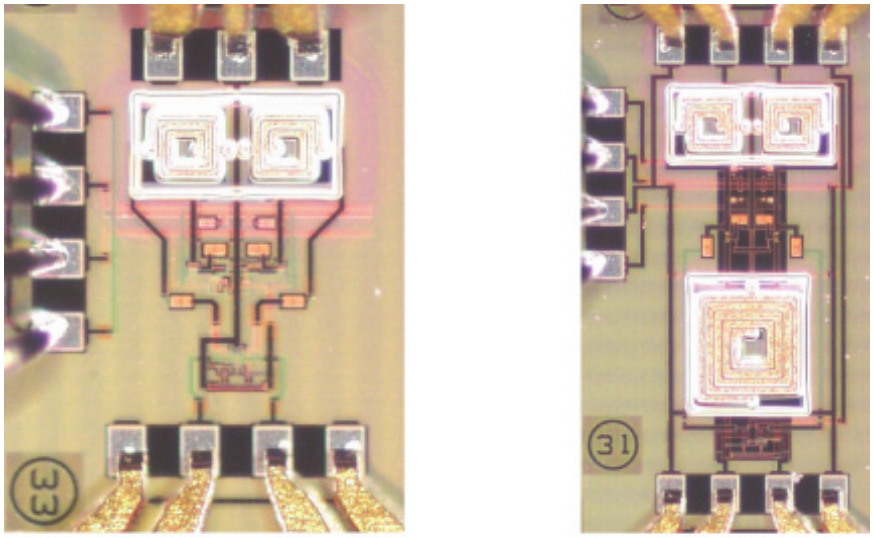


Figure 2.35: Die photos of fabricated circuits: (a) lower power VCO; (b) high output power VCO

the RF probes in contact for testing are shown in Figure 2.35. This section describes the testing procedure and measured results of the two fabricated VCOs.

2.7.1 Measurement Setup

Figure 2.36 shows a schematic of the test setup used to measure the tuning and output power performance of the two VCOs. This schematic is specific to the high output power design; however, the only difference in the testing setup for the two designs is in the probe configuration used to supply the DC bias voltages to the VCO core and buffer amplifiers. Recall that the high output power VCO layout allows for the VCO

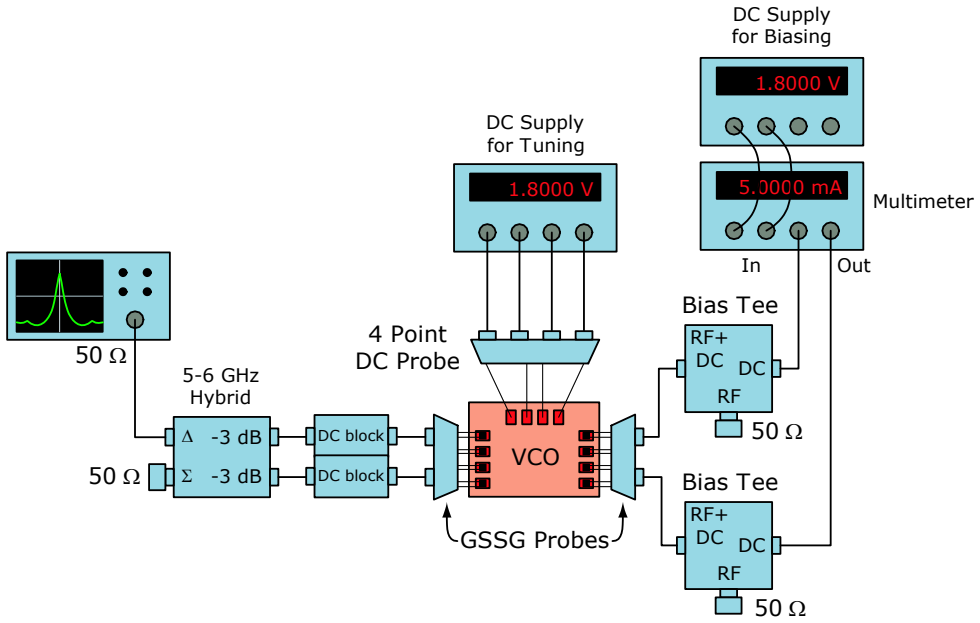


Figure 2.36: VCO test setup schematic for the high output power VCO.

and buffer amplifier to be biased separately using a GSSG probe pad setup. The low power VCO design, on the other hand, was laid out with a common bias pin and a GSG probe was used. Therefore, the testing setup for the low-power design replaces the GSSG probe (shown on the right hand side of the schematic) with a GSG probe, and the additional bias tee is not needed.

DC blocking capacitors were used in between the high frequency output and the spectrum analyzer to prevent the DC biasing of the common collector buffer from sourcing to ground through the analyzer. A hybrid coupler designed for use in the 5-6 frequency range was used to convert the differential signal from the VCO into a single-ended signal at the analyzer. It should be noted here that this probe-based test setup uses a spectrum analyzer instead of a network analyzer, so no vector calibration of the cable losses or equipment losses was performed. It is estimated that there is approximately 1.5 dB of loss from the output of the VCO to the input of the spectrum analyzer.

As for the DC signals, the switch control and fine tuning signals are applied via the four point DC probe which is connected to a dual-output DC supply. Since the V_{CC} pins are connected to a GSSG (or GSG) probe that requires a coaxial cable input,

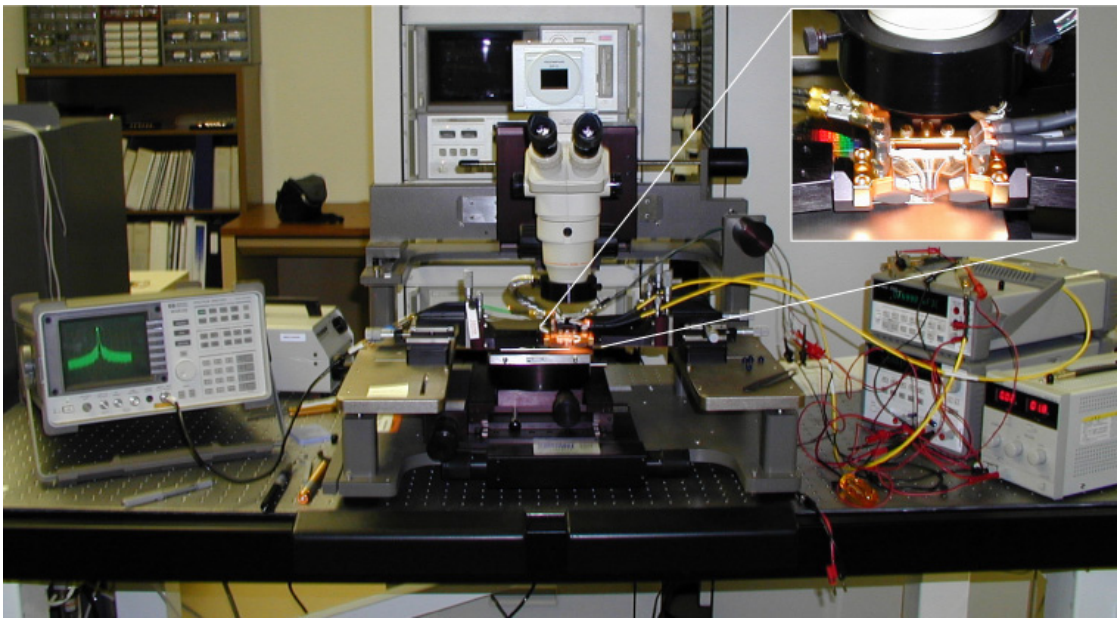


Figure 2.37: Photograph of testing setup Inset: close-up of probes in contact with the die.

a bias tee was used to apply V_{CC} to the center conductor of the coax cable. Since there is no RF to supply to these pins, the RF input port of the bias tee is terminated in 50 Ω. A multimeter is placed in series with the DC supply and the bias pads to measure the current drawn by the circuit.

A photograph of the testing setup is shown in Figure 2.37. The probe station is set up on a vibration-isolation table so as to minimize the possibility of damage to the probes and die due to ambient vibrations. The two DC power supplies and the multimeter are to the right of the probe station while the spectrum analyzer is to the left. (The network analyzer in the background of the photo was not used in this test setup.)

2.7.2 Tuning Range Results

The center frequencies corresponding to the applied varactor tuning voltage for each switched state were obtained by setting the appropriate control and supply voltages on the DC power supplies, waiting ∼30 sec for the circuit to stabilize, and recording the peak frequency from the spectrum analyzer. The frequency would also drift

considerably immediately after the power supply was turned on, so an additional waiting time of ∼5 min was used before the first measurements were made.

Low Power VCO Design

The measured tuning ranges of the low-power VCO design for the two switched states are presented in Figure 2.38. The physical limits of the tuning voltage are -750 mV to +2.0 V. Above and below these voltages, the varactors begin to draw DC current, indicating device breakdown. For voltages significantly beyond these limits, the varactors catastrophically fails and the VCO is rendered inoperable. For the available tuning range, the frequencies for the lower frequency sub-band are shifted down from 5.14 GHz - 5.36 GHz to 4.34 GHz - 4.47 GHz. Likewise, the frequency range of the higher frequency sub-band is shifted down from 5.625 GHz - 5.925 GHz to 5.25 GHz - 5.488 GHz. The primary reason for this is interconnect parasitics. Each of the critical traces in Figure 2.29 were laid out with relatively large widths in order to reduce the series resistance in the signal path. Maximum width traces, however, also present the maximum parasitic capacitance to the substrate. Each of the traces, therefore, adds capacitance to the tank circuit and lowers the resonant frequency. The effect is less pronounced in the switch-off state compared to that of the switch-on state. This indicates that there is more parasitic capacitance associated with the on-state of the switch than what was accounted for in simulation. The parasitics also reduce the frequency tuning range of the varactors since the fraction of the total capacitance represented by the varactors is reduced. The shape of the tuning curve, however, is not significantly altered by the parasitics and the center tuning voltage is still approximately 750 mV.

Typically, parasitics can be extracted from the layout and simulated with the rest of the circuit to determine their effect before fabrication. Due to time constraints, this step was not performed. Also, the author and Motorola have low confidence, at best, in the available Assura parasitic extraction deck for RF applications. Consequently, it was decided that it would be best to fabricate the circuit without compensation for parasitics so that their effect could be extracted empirically from the fabricated die and used in the design of future VCOs.

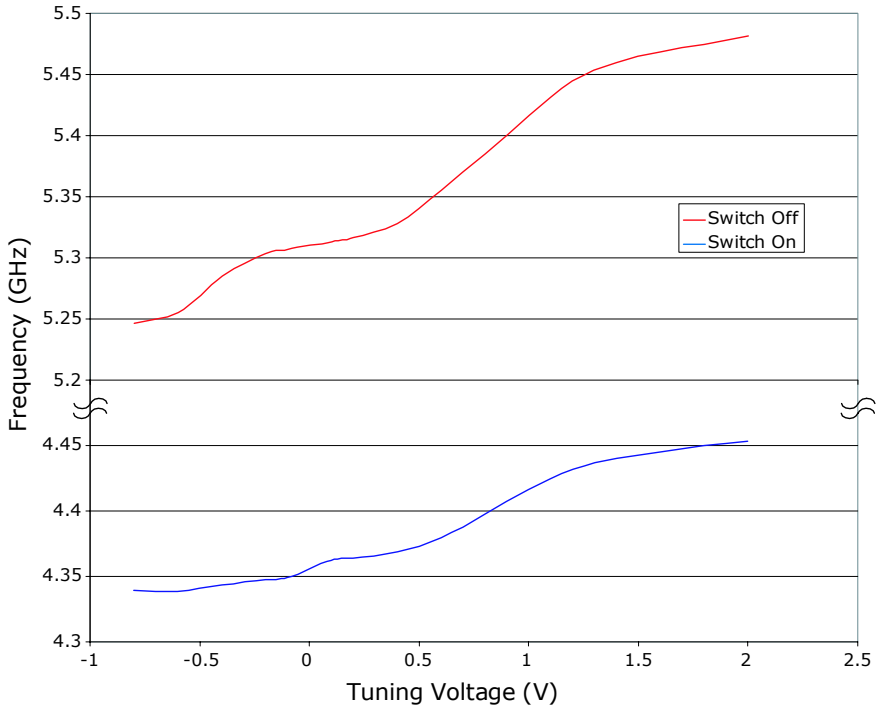


Figure 2.38: Measured tuning ranges of the low power VCO design.

High Output Power VCO Design

The measured tuning ranges of the high output power VCO design are shown in Figure 2.39. There are only two curves shown due to a problem associated with Switch_1. For all of the fabricated samples, there was no difference in measured frequencies between the Switch_1-on state and the Switch_1-off state. For this reason, only the two operational switch states associated with the Switch_1-on condition are plotted in Figure 2.39. Despite the faulty switch, the tuning ranges for the two cases in which Switch_1 is on were close to the expected values (accounting for the interconnect parasitics). Switch_2 appears to work as expected since the frequency range of the middle sub-band starts at the frequency at which the first sub-band stops, exactly as it should.

The lower two frequency ranges show the same average decrease as the low frequency range in the low power design, suggesting that the total parasitics for the two designs are similar. The lowest frequency range drops from 5.15 GHz - 5.25 GHz to 4.36 GHz - 4.43 GHz and the middle frequency range drops from 5.25 GHz - 5.35 GHz to

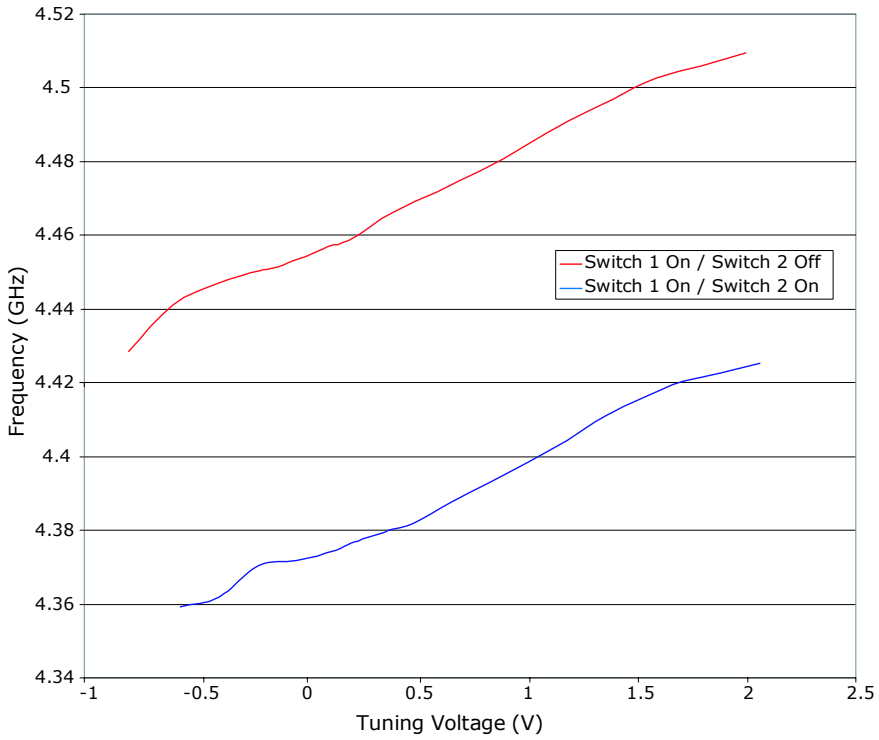


Figure 2.39: Measured tuning ranges of the high output power VCO.

4.43 GHz - 4.51 GHz. Again, the parasitics affect both the absolute frequency values and the available tuning range.

2.7.3 Amplitude and Power Consumption Results

At each of the tuning voltage steps, the peak power, as measured by the spectrum analyzer, was also recorded for each design.

Low Power VCO Design

Figure 2.40 shows the plots of the frequency spectrum for the highest varactor tuning voltage (2 V) for the switch-off state [Figure 2.40(a)] and the switch-on state [Figure 2.40(b)]. The average current consumption values through the shared bias supply pin are 4.2 mA and 4.55 mA for the switch-off state and switch-on state, respectively. As expected, the peak output powers are near equal despite the higher Q-factor of

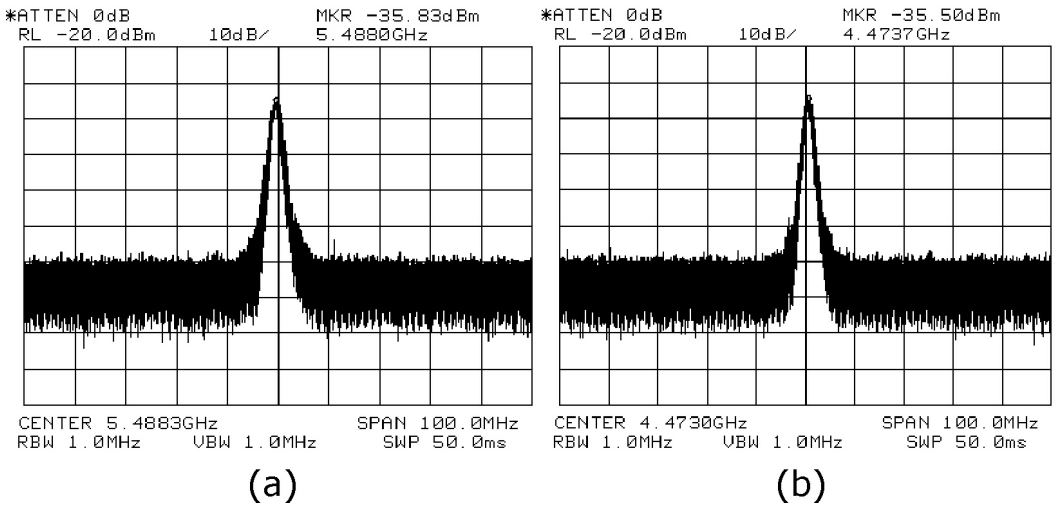


Figure 2.40: Measured output spectra for the low power VCO at a varactor tuning voltage of 2 V: (a) switch off state; (b) switch on state.

the switch-off state. However, the power is a very low -35.5 dBm for both states. Even with the assumed cable and test-setup loss, this measured power is extremely low. Since the buffer and VCO share the same bias pin, the measured total current of 4.2 mA is too low to adequately account for both the buffer consumption and the VCO consumption (the total should be closer to 7.2 mA). Unfortunately, the problem could not be isolated due to the single bias pin; however, it is believed that the buffer amplifier is not biasing correctly and thus significantly attenuating the VCO output signal.

High Output Power Design

Figure 2.41 shows the plots of the frequency spectrum for the middle varactor tuning voltages (750 mV) for the lower and middle frequency tuning ranges of the high-output power VCO design. The average current consumptions for the operational switched states were 16 mA and 17 mA – close to the expected values of 16.5 mA and 17 mA. The amplitude was relatively constant for the two switch states and was significantly higher than in the low-power design (-8 dBm versus -35 dBm), as expected. However, the buffer amplifier only biased to 2 mA (versus 3 mA as simulated), suggesting a serious problem with the fabricated buffer amplifier and supporting the conclusions

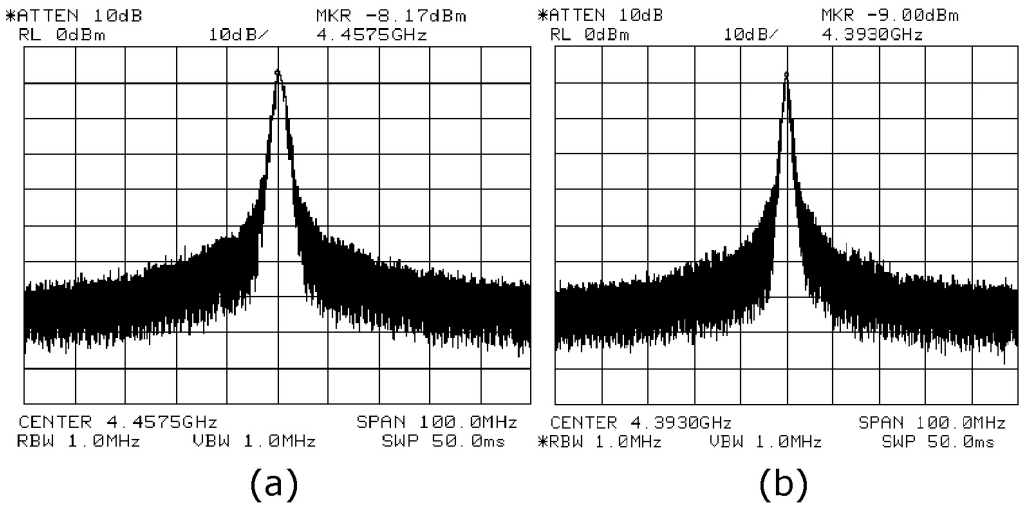


Figure 2.41: Measured output spectra for the high output power VCO at a varactor tuning voltage of 750 mV: (a) middle frequency range; (b) low frequency range

from the low-voltage design.

2.8 Summary

Two VCOs with different power consumption and output power goals were designed, fabricated, and tested. Both circuits performed well in simulation and the results of the simulations are presented in Table 2.2. In summary, the low-power VCO draws a relatively small amount of current, tunes over the lower and higher sub-bands of the UNII band, and has a spectrally pure sinusoid with low phase noise, albeit with a low output voltage swing. For LO applications in RF transceivers, such a low output power may not sufficiently drive mixing stages, so a second, high output power design was simulated. This design tunes over all three UNII sub-bands individually with an output voltage swing more than twice that of the low power design at the cost of significantly higher current consumption. However, the fabricated circuits did not perform as simulated, which was expected given the prototype nature of the two designs. Due to interconnect parasitics, the center frequencies and tuning ranges of each switched state are decreased from expected values. For the high output power design, a faulty NMOS device led to an inoperative switch state. However, the second

switch worked within expectations. The output powers are decreased from simulation values due to a problem with the buffer amplifier biasing; however, the relative values between the two designs are within expectations. Several improvements for future designs are described in Chapter 5.

Chapter 3

Modeling and Design of Electromechanical Disk Resonators

The remainder of this thesis focuses on the development of MEMS contour-mode disk resonators in silicon-on-insulator (SOI) technology. This chapter focuses on the design and modeling of the resonator structure while Chapter 4 focuses on the SOI fabrication process.

Complex physical systems such as MEMS resonators encompass variables and degrees-of-freedom that are too numerous to completely describe using closed form expressions. Reduced order or "lumped-element" models are often employed in order to reduce the number of variables to a reasonable set containing only those factors that are most critical for determining the response of the system in the domain of interest. For the models considered in this chapter, the total energy of the system is reduced into an equivalent reduced-order representation. Table 3.1 summarizes the relationships between the three components of energy and their corresponding reduced order elements in the mechanical and electrical domains.

All oscillating systems, whether they are mechanical or electrical in nature, can be expressed as the periodic transfer of energy from a potential state (storage) to a kinetic state (release). The nonconservative loss is the difference between the energy stored as potential energy and the energy released in the form of kinetic energy. Nonconservative energy can take the form of air-damping, friction, or any other mechanism that transfers energy away from the vibrating system. By reducing the total energy

Component of Energy	Mechanical Model Equivalency	Electrical Model Equivalency
Potential Energy (U)	Mass (m)	Inductor (L)
Kinetic Energy (K)	Spring (k)	Capacitor (C)
Nonconservative Loss	Dashpot (c)	Resistor (R)

Table 3.1: Relationships between components of energy and reduced-order model elements.

description of the system to a reduced-order model, system designers can more efficiently simulate or calculate the operation of the system in conjunction with other reduced-order models of the same type in the presence of various stimuli. Modeling is of particular importance in the field of MEMS where systems are comprised of coupled mechanical and electrical elements. Reducing a MEMS resonator to a purely mechanical description or a purely electrical description can aid in the simulation of integrated systems such as an oscillator or a filter in an RF transceiver.

This chapter presents methods for deriving both the electrical and mechanical reduced-order models and also presents methods for modeling the resonator using Finite-Element Analysis (FEA). FEA is a computational method that can more accurately simulate the physical and electrical response of the resonator; however, this comes at the expense of greatly increased simulation times.

3.1 Reduced-Order Mechanical Model: Mass-Spring-Dashpot System

To model the resonator as a mechanical lumped element model, consider the response of a single degree-of-freedom (DOF) system (i.e. a system that is free to move in a single direction such as the x-direction in a Cartesian coordinate system or the radial direction in a polar coordinate system) to a harmonic excitation:

$$m\left(\frac{d^2x(t)}{dt^2}\right) + c\left(\frac{dx(t)}{dt}\right) + kx(t) = F_d(t), \tag{3.1}$$

where $x(t)$ is the displacement of the system with respect to time, $F_d(t)$ is the forcing function, m is the mass of the system, c is the damping coefficient, and k is the

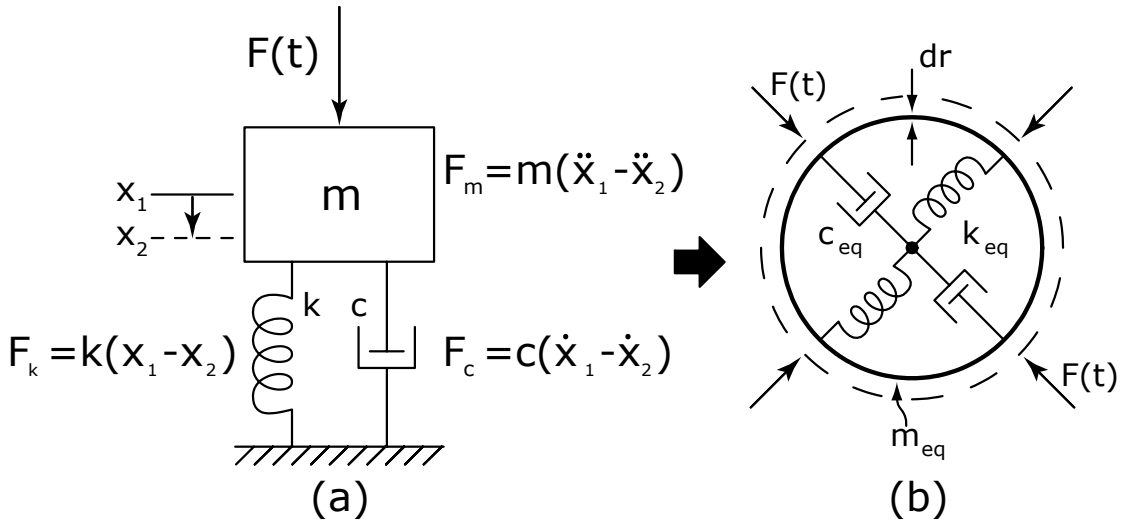


Figure 3.1: Reduced-order models: (a) generic single degree-of-freedom forced mechanical system; (b) equivalent model for contour-mode resonator.

effective spring constant. The forces defined by m, k, and c are represented by the mass, spring, and dashpot elements, respectively, in Figure 3.1(a). k represents the storage and release of potential energy in the system as described by Hooke's Law:

$$U = \frac{1}{2}k\delta^2, \tag{3.2}$$

where δ is the total displacement. Potential energy is stored by the elastic elements in the system; for contour-mode resonators, this element is a Si disk anchored at its central nodal point[1]. The restrictive force described by c is nonconservative and it represents the loss of the system. The force from the mass, m, represents the storage and release of kinetic energy from the system according to:

$$K = \frac{1}{2}mv^2, \tag{3.3}$$

where v is the velocity of the mass. Together, the mass, spring, and dashpot completely describe the total energy of the system at any given time, t.

[1]The deformation of even highly stiff materials, such as silicon or polysilicon, is considered elastic for small displacements.

Equation 3.1 can be rewritten as:

$$\frac{d^2x(t)}{dt^2} + 2\zeta\omega_n\left(\frac{dx(t)}{dt}\right) + \omega_n^2 x(t) = \frac{\omega_n^2}{k}F_d(t), \tag{3.4}$$

where ω_n is the natural frequency defined by $\sqrt{k/m}$, and ζ is the *damping ratio* defined by $c/2\omega_n m$. In the specific case of the disk resonator, the natural frequency can be found through Equations 1.20 and 1.21, which are repeated here for completeness:

$$\frac{\gamma}{\xi}\frac{J_0\left(\frac{\gamma}{\xi}\right)}{J_1\left(\frac{\gamma}{\xi}\right)} = 1-\sigma, \text{where } \xi = \sqrt{\frac{2}{1-\sigma}}, \tag{3.5}$$

$$\omega_n = \frac{\gamma}{R}\sqrt{\frac{E}{\rho\,(2+2\sigma)}}, \tag{3.6}$$

ζ is a measure of the loss of the system and can be related to the mechanical Q-factor of the resonator through [81]:

$$\zeta = \frac{1}{2Q}. \tag{3.7}$$

Since there are many factors that influence the actual mechanical Q-Factor of the device, it is typically extracted from experimental results rather than predicted mathematically. However, there are methods by which the Q can be approximated reasonably well which will be discussed in Section 3.4.

The dashpot damping coefficient, c, can be solved through the relation $c = \zeta 2\omega_n m_{eq}$, where m_{eq} is the equivalent mass. The equivalent mass represents the fraction of the total physical mass that participates in the storage of potential energy. In the disk resonator, the majority of the potential energy is stored in the outer edge of the disk while the inner portion of the disk stores very little. To find the equivalent mass of the system, the ideal kinetic energy of the entire disk is equated with the kinetic energy of an infinitesimally small annular ring of width dr and mass m_{eq} located at the radial position R (the edge of the disk) [Figure 3.1(b)] as follows [82]:

$$\frac{1}{2}m_{eq}v^2(R) = \frac{1}{2}\int_0^R 2\pi t\rho r \cdot v^2(r)dr, \tag{3.8}$$

where $v(r)$ is the velocity of the portion of the disk at radius r, t is the thickness

of the disk, and ρ is the density of the disk material ($\pi\rho tR^2$ is equal to the physical mass of the disk). The velocity of the portion of the disk at radius r can be replaced by the derivative of the displacement [35]:

$$v(r) = x'(r) = -Ah\omega J_1(hr)\sin(\omega t), \tag{3.9}$$

where A is an arbitrary displacement amplitude and h is defined as:

$$h = \sqrt{\frac{\rho\omega^2}{\frac{\sigma E}{1-\sigma^2} + \frac{2E}{2+2\sigma}}}, \tag{3.10}$$

where E is the Young's modulus and σ is the Poisson's ratio. Combining Equations 3.8 and 3.9 yields:

$$m_{eq} = [J_1^2(hR)]^{-1} \cdot 2\pi t\rho \int_0^R rJ_1^2(hr)dr, \quad \longrightarrow \tag{3.11a}$$

$$m_{eq} = \frac{\pi t\rho R^2 \left[J_1^2(hR) - J_0(hR)J_2(hR)\right]}{J_1^2(hR)}. \tag{3.11b}$$

The relation $k_{eq} = \omega_n^2 m_{eq}$ can then be used to calculate the effective spring constant of the resonator.

The reduced-order mechanical model provides a good foundation for modeling the physics of the contour-mode resonator; however, electrical-based lumped element models, such as the one derived in the next section, are often more useful from a electronic circuit simulation point of view.

3.2 Electrical Lumped-Element Model: Series RLC Circuit

The electrical lumped element model replaces the mass, spring, and dashpot elements of the mechanical model with their electrical analogs, specifically the inductor, capacitor, and resistor. The motivation for this is to provide simple electrical models that can be simulated with other circuit components (e.g. in an electric circuit simulation software package such as Spice). The electrical element values are directly related to

the values for the equivalent mass, spring constant, and damping factor as described below.

The derivation of the electrical lumped-element model consists of three steps. First, a mechanical transfer function is derived that relates the motion of the system to the applied force. Second, the mechanical transfer function is converted to an electrical transfer function that relates the applied voltage to the output current. Finally, the electrical transfer function is compared to that of the expected equivalent circuit, in this case a series RLC circuit, and equations for equivalent circuit parameters are derived.

3.2.1 Mechanical Transfer Function

Recall that the vibration of a single DOF system is described by Equation 3.4 and that $F_d(t)$ is the forcing function for the vibration. The forcing function of interest for the contour-mode disk resonator is the second term of Equation 1.14, $F_d(t) \approx -\frac{\partial C}{\partial x}\left[V_{DC}V_i\cos(\omega_i t)\right]$. Assuming that $\frac{\partial C}{\partial x}$, V_{DC}, and V_i can be grouped into a single phasor term, $F_d(j\omega)$, and using Euler's formula to rewrite the trigonometric function as an exponential, the forcing function simplifies to:

$$-\frac{\partial C}{\partial x}\left[V_{DC}V_i\cos(\omega_i t)\right] = F_d(t) = F_d(j\omega)e^{j\omega t}. \tag{3.12}$$

Substituting the forcing function of Equation 3.12 into Equation 3.4 and solving the differential equation gives the following form for $x(t)$:

$$x(t) = X(j\omega)e^{jwt}, \tag{3.13}$$

where $X(j\omega)$ is the displacement of the system in phasor notation. Substituting Equation 3.13 back into Equation 3.4 yields:

$$\left(\omega_n^2 - \omega^2 + j2\zeta\omega\omega_n\right)X(j\omega)e^{jwt} = \frac{\omega_n^2}{k}F_d(j\omega)e^{j\omega t}. \tag{3.14}$$

The mechanical transfer function, $G(j\omega)$, can be then defined as the ratio of the

displacement response of the system, $X(j\omega)$, to the force applied, $F_d(j\omega)$, as follows:

$$G(j\omega) = \frac{X(j\omega)}{F_d(j\omega)} = \frac{k^{-1}}{1 - (\omega/\omega_n)^2 + j2\zeta(\omega/\omega_n)}. \tag{3.15}$$

To convert from a purely mechanical formulation to an *electromechanical* formulation, reconsider the forcing function in Equation 3.12 in the form:

$$F_d(j\omega) = -V_i(j\omega) \left(\frac{\partial C}{\partial x}\right)\Big|_{in} V_{DC}, \tag{3.16}$$

where $\left(\frac{\partial C}{\partial x}\right)\Big|_{in}$ and V_{DC} are separated out as constants[2] from the phasor input voltage (the subscript *in* distinguishes these values as input-referenced values; the difference between input and output-referenced values will be discussed in Section 3.2.3). Substituting Equation 3.16 into 3.15 and using Equation 3.7 for ζ yields the following transfer function:

$$\frac{X(j\omega)}{V_i(j\omega)} = -\left(\frac{\partial C}{\partial x}\right)\Big|_{in} \frac{V_{DC}}{k} \left[1 - \left(\frac{\omega}{\omega_n}\right)^2 + \left(\frac{j\omega}{Q\omega_n}\right)\right]^{-1}. \tag{3.17}$$

From this equation, the mechanical displacement is now related to electrical quantities, the input voltage and gap capacitance. To derive a fully electrical formulation of the transfer function, the mechanical displacement is equated to an output motional current across the transducer gap as discussed in the next section.

3.2.2 Electrical Transfer Function

As mentioned above, the eventual goal of this analysis is to derive a transfer function for the resonator similar to that of a series RLC circuit so that the mechanical quantities m, k, and c can be related to the electrical quantities L, C, and R. (A parallel RLC circuit would also serve the same purpose; however an equation relating force to velocity instead of voltage would be required to develop the equivalent model [32].)

[2] The extent to which $\partial C/\partial x$ can be considered a constant will be discussed in Section 3.2.4.

The admittance looking into a series RLC circuit can be written as:

$$Y_i(j\omega) = \frac{I_i(j\omega)}{V_i(j\omega)} = \frac{j\omega}{L\omega_n^2}\left[1 - \left(\frac{\omega}{\omega_n}\right)^2 + \left(\frac{j\omega}{\omega_n^2 Q^2 RC}\right)\right]^{-1}, \tag{3.18}$$

where ω_n is the resonant frequency defined by $1/\sqrt{LC}$, and Q is the electrical Q-factor of the series resonant circuit. In order to equate Equation 3.17 to Equation 3.18, an expression relating the current phasor, $I_i(j\omega)$, to the displacement phasor, $X(j\omega)$ must be found. This can be accomplished by deriving an expression relating the capacitance across the transducer gap to the AC current across the gap. Since the capacitance is a function of the mechanical displacement of the edge of the resonator, this expression will also relate the current to the mechanical displacement.

First, the capacitance across the gap is assumed to be a time dependent quantity given by the piecewise function [32]:

$$C(x,t) = \begin{cases} \approx C_o & \text{for nonresonant conditions} \\ C_o + C_m(x(t)) & \text{for resonant conditions} \end{cases}, \tag{3.19}$$

where C_o is the static capacitance between the disk edge and the electrode when the disk is not vibrating, and C_m is the variation in capacitance as a function of the distance of the disk edge to the electrode (referenced from the edge of the non-vibrating disk). $x(t)$ can be written as $X\sin(\omega_n t)$ where X is the mechanical displacement amplitude and ω_n is the resonant frequency. The current across a capacitor is equal to $\frac{\partial(CV)}{\partial t}$ where V is the voltage across the capacitor. Therefore, the current across the capacitance found in Equation 3.19 can be written as:

$$i(t) = C(x,t)\frac{\partial v_g(t)}{\partial t} + v_g(t)\frac{\partial C(x,t)}{\partial t}, \tag{3.20}$$

where $v_g(t)$ is equal to the voltage across the gap, $v(t) - V_{DC}$. Substituting Equation 3.19 for the resonant condition into Equation 3.20 gives the following expression for the current across the gap for at resonance:

$$i(t) = C_o\frac{dv(t)}{dt} + x\frac{\partial C_m(x(t))}{\partial x}\frac{dv(t)}{dt} - V_{DC}\frac{\partial C_m(x(t))}{\partial x}\frac{\partial x}{\partial t} + v(t)\frac{\partial C_m(x(t))}{\partial x}\frac{\partial x}{\partial t}. \tag{3.21}$$

Assuming time-harmonic excitation and converting to phasor notation yields the fol-

lowing expression for current in the frequency domain:

$$I(j\omega) = C_o j\omega V(j\omega) + 2\left(\frac{\partial C}{\partial x}\right) j\omega V(j\omega)X(j\omega) - V_{DC}\left(\frac{\partial C}{\partial x}\right) j\omega X(j\omega). \quad (3.22)$$

The first term represents a static current flowing across the gap through the static capacitor C_o. This is analogous to the static capacitance arising from the electrodes and packaging of the quartz crystal as shown in Figure 1.10. The second term represents a current at twice the frequency of oscillation and a current at DC as a result of the mixing between the nonlinear relation of capacitance to disk displacement and the excitation voltage [32]. The third term represents the current at the resonant frequency of oscillation. Typically, only the first and third terms of Equation 3.22 are used to model the current across the gap as shown in Figure 3.2. The second (2ω) term is not multiplied by the DC bias and is therefore typically much smaller in magnitude than the third (ω) term and can be ignored. On the other hand, the contribution due to C_o cannot be ignored due to the typically small values for the static spacing between the electrode and the disk. The third term is referred to as the *motional current* and can be used to derive the R, L, and C parameters of the equivalent series RLC circuit. To derive these parameters, assume that the current can be approximated by only the third term as follows:

$$Y_i(j\omega)V_i(j\omega) = I_i(j\omega) \approx -V_{DC}\left(\frac{\partial C}{\partial x}\right)\Bigg|_{in} j\omega X(j\omega), \text{ or alternatively,} \quad (3.23a)$$

$$\frac{I_i(j\omega)}{X(j\omega)} \approx -j\omega V_{DC}\left(\frac{\partial C}{\partial x}\right)\Bigg|_{in}, \quad (3.23b)$$

where $Y_i(j\omega)$ is the admittance of the gap through the motional element (Figure 3.2).

A purely electrical transfer function can be formulated by multiplying Equation 3.23b and Equation 3.17:

$$Y_i(j\omega) = \frac{I_i(j\omega)}{X(j\omega)} \cdot \frac{X(j\omega)}{V_i(j\omega)} = \frac{I_i(j\omega)}{V_i(j\omega)} = \left(\frac{\partial C}{\partial x}\right)\Bigg|_{in}^2 \frac{j\omega V_{DC}^2}{k}\left[1 - \left(\frac{\omega}{\omega_n}\right)^2 + \left(\frac{j\omega}{Q\omega_n}\right)\right]^{-1}. \quad (3.24)$$

Comparing Equation 3.24 and Equation 3.18 yields three simultaneous equations that

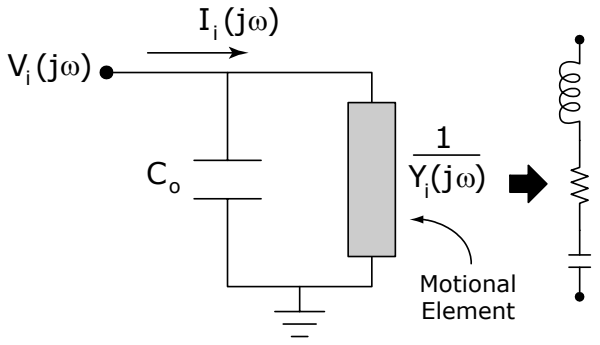


Figure 3.2: Model of the transducer gap including the static capacitance, C_o, and the motional admittance, $Y(j\omega)$ (after [32]).

can be solved for the equivalent resonator R, L, and C:

$$\frac{j\omega}{L\omega_n^2} = \left(\frac{\partial C}{\partial x}\right)\Big|_{in}^2 \frac{j\omega V_{DC}^2}{k}, \tag{3.25a}$$

$$\omega_n = \sqrt{\frac{1}{LC}}, \tag{3.25b}$$

$$RC = \frac{1}{Q\omega_n}. \tag{3.25c}$$

Solving each equation yields the following values for the lumped-element parameters:

$$L_{eq} = \frac{k}{\omega_n^2 \left[\left(\frac{\partial C}{\partial x}\right)_{in} V_{DC}\right]^2} = \frac{m_{eq}}{\eta_i^2}, \tag{3.26a}$$

$$C_{eq} = \frac{\left[\left(\frac{\partial C}{\partial x}\right)_{in} V_{DC}\right]^2}{k} = \frac{\eta_i^2}{k_{eq}}, \tag{3.26b}$$

$$R_{eq} = \frac{k}{\omega_n Q \left[\left(\frac{\partial C}{\partial x}\right)_{in} V_{DC}\right]^2} = \frac{\sqrt{k_{eq} m_{eq}}}{Q\eta_i^2}, \tag{3.26c}$$

where η_i is the electromechanical coupling coefficient and is equal to $\left(\frac{\partial C}{\partial x}\right)\Big|_{in} V_{DC}$. $\left(\frac{\partial C}{\partial x}\right)\Big|_{in}$ is assumed to be a constant and can be calculated using the following expression:

$$\left(\frac{\partial C}{\partial x}\right)\Big|_{in} \approx \frac{C_o}{d_i} = \left(\frac{N}{180}\right)\frac{\varepsilon_o 2\pi R t}{d_i^2}, \tag{3.27}$$

where N represents the portion of the disk circumference that is faced by the input

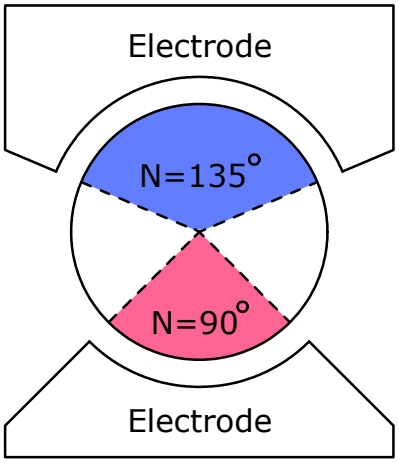


Figure 3.3: Electrode coverage of disk circumference $N = 135\,^\circ$ (top) and $N = 90\,^\circ$ (bottom).

electrode (Figure 3.3 shows electrode coverage for $N = 135\,^\circ$ and $N = 90\,^\circ$) and d_i is the gap spacing between the input electrode and the disk.

3.2.3 One and Two-Port Testing Setups

The electrical model also depends on the manner in which the resonator is excited and the resulting response is measured. Figure 3.4(a) shows the resonator in a "one-port" testing environment in which the excitation signal is applied in-phase to both electrodes. The measured quantity in this case can either be of the reflected signal at the input port (i.e. S_{11}) or the current sourced by the resonant disk as depicted in Figure 3.4(a). The one-port testing setup has the advantage of maximum electromechanical coupling between the disk and the electrode. Since both electrodes are excited in-phase, the force described by Equation 1.14 is effectively doubled. However, the feedthrough current due to the static capacitance, C_o, is also maximized by this test setup. If this current is large enough in magnitude, it becomes difficult to detect the current component that is due to resonant vibration. Furthermore, measuring the current through the thin DC bias lines attached to the edges of the disk becomes more difficult due to the high resistance of these lines.

The nature of the DC bias lines is dictated by the SOI process used to fabricate the disk resonators in this work. Ideally, the DC bias would be applied through the

central nodal point so as to have a minimum impact on the displacement characteristics of the contour-mode. The bottom-up fabrication approach shown in Figure 1.20 is capable of connecting the DC bias at the polysilicon central nodal point [36, 37]. However, in the SOI process used here, the DC bias cannot be fed through the central node since it is fabricated from nonconducting SiO_2. For this reason, the DC bias lines are fabricated in-plane with the disk and connected at its edges. Since the disk edge experiences the maximum displacement in contour-mode vibration, the DC bias lines must have as small a width as possible to avoid significant degradation of the mode-shape. Since electrical resistance is inversely related to trace width, the bias lines will have a high resistance.

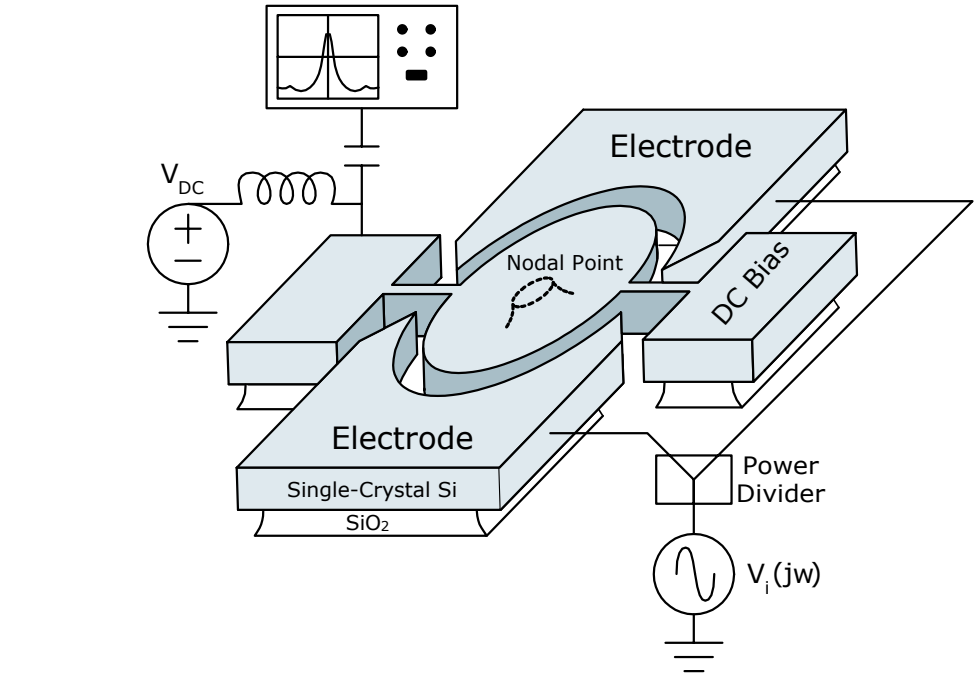
Alternatively, in the "two-port" setup, the excitation can be applied to one of the electrodes and the output current measured from the opposite electrode as shown in Figure 3.4(b)[3]. Since the excitation is supplied only through one electrode, the current due to the static capacitance is reduced by a factor of two. In addition, current readout is less of a problem due to the larger width and lower resistance of the electrodes, as compared to that of the DC bias line. On the other hand, the force on the disk is also reduced by a factor of 2 in the two-port setup, leading to an overall lower motional current value.

Two-Port Model

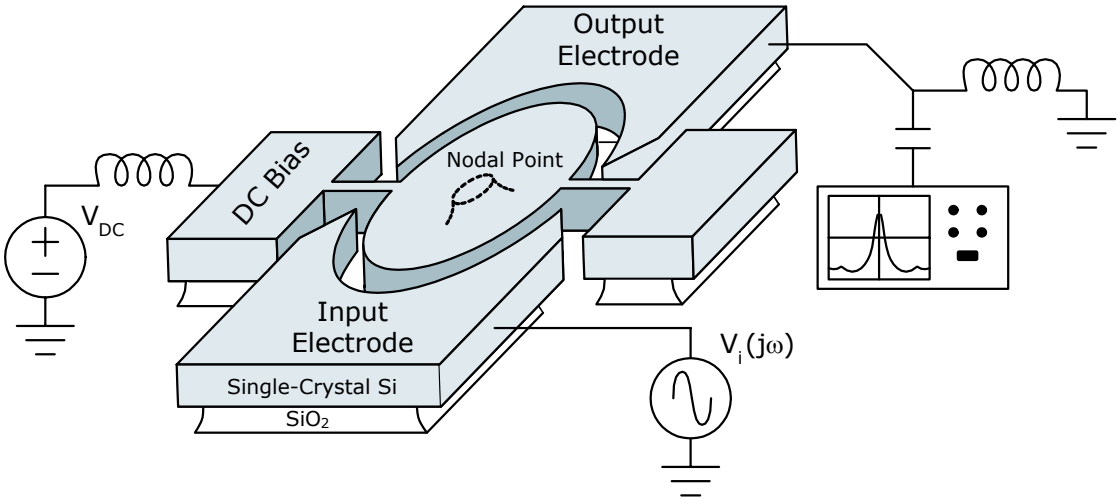
The analysis of Section 3.2.2 resulted in a model for the transducer gap in the presence of an external AC excitation voltage. The specific resonator excitation/measurement setup will determine how each of the transducer gaps on either side of the disk are modeled. For instance, in the two-port setup of Figure 3.4(b), the input electrode can be modeled as described in Section 3.2.2 due to the presence of the AC excitation. However, there is no excitation voltage present on the output electrode, thus the current through the output gap is dependent only on the current at the input gap. Assuming that excitation from only the input electrode will force contour-mode vibration[4], the motion of the disk with respect to the output electrode will induce

[3]It should be noted that the two-port and one-port designations used here are switched from those used by [32]. It is the opinion of the author that the input/output orientation of the two AC electrodes is more accurately described by the microwave definition of a two-port device; thus the nomenclature here was chosen to reflect this definition.

[4]The extent to which this assumption is true is covered in Section 3.3.6.



(a)



(b)

Figure 3.4: Disk resonator testing setups: (a) one-port; (b) two-port.

a motional current across the output gap represented by to the third term of Equation 3.22. Therefore, the current to displacement ratio at the output gap can be approximated as follows:

$$\frac{I_o(j\omega)}{X(j\omega)} \approx -j\omega V_{DC} \left(\frac{\partial C}{\partial x}\right)\Big|_{out}, \tag{3.28}$$

where the subscript *out* distinguishes these values as output-referenced quantities. Due to symmetry, the displacement at the input electrode can be assumed to be the same as it is at the output electrode, and Equations 3.28 and 3.17 can be multiplied together as before to yield the following admittance expression:

$$Y_o(j\omega) = \frac{I_o(j\omega)}{V_i(j\omega)} = \left(\frac{\partial C}{\partial x}\right)\Big|_{in} \left(\frac{\partial C}{\partial x}\right)\Big|_{out} \frac{j\omega V_{DC}^2}{k} \left[1 - \left(\frac{\omega}{\omega_n}\right)^2 + \left(\frac{j\omega}{Q\omega_n}\right)\right]^{-1}. \tag{3.29}$$

Rather than derive new circuit parameters for the motional current at the output gap, Equation 3.29 can be divided by Equation 3.24 to give the following ratio of the currents:

$$\phi_{oi} = \frac{I_o(j\omega)}{I_i(j\omega)} = \frac{\left(\frac{\partial C}{\partial x}\right)\big|_{out}}{\left(\frac{\partial C}{\partial x}\right)\big|_{in}}. \tag{3.30}$$

The current ratio, ϕ_{oi}, can then be incorporated into the lumped-electrical model of the entire two-port resonator as a controlled current source. Typically, the two gaps of the resonator are fabricated to be identical and ϕ_{oi} can almost always be assumed to be 1, meaning that the output motional current is equal to the motional current across the input gap.

Due to the absence of excitation at the output gap, the static current across C_o is only dependent on the input current. The static current across the input gap will flow through the disk and across the static capacitance of the output gap. The two static capacitors can, therefore, be said to be in series and the effective impedance to the static current from these two capacitors is doubled. This will result in the aforementioned reduction of static current in the two-port setup.

The general electrical lumped-element model for the two-port setup is shown in Figure 3.5. The input gap is modeled by the RLC series network parallel with C_{oi} and the output gap is modeled by the current controlled current source parallel with C_{oo}. The disk itself is connected to DC (AC ground) through the RF choke inductor of

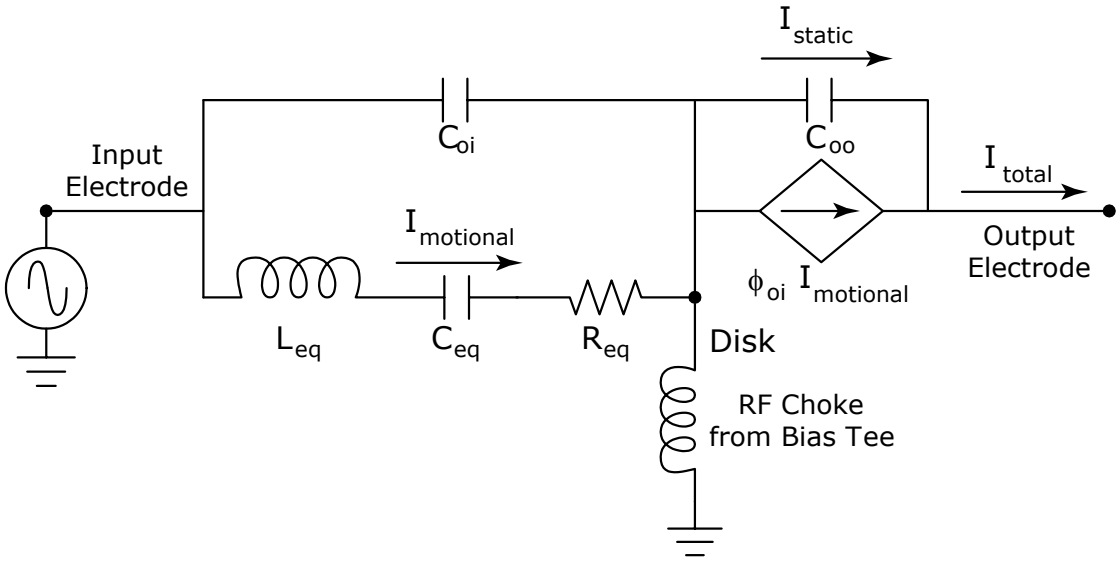


Figure 3.5: Equivalent circuit model for the two-port testing setup.

the bias-tee shown in Figure 3.4(b).

Table 3.2 summarizes the calculated mechanical and electrical lumped-element values an example disk resonator fabricated in the SOI process described in Section 1.2.2. The capacitance and inductor values resemble those of a quartz crystal model; however, the series resistance value is much higher. The series resistance is the most critical of the equivalent circuit parameters since it determines the value of the disk impedance at resonance. In a typical RF system, 185 kΩ is an extremely high resistance value, and matching other components to the resonator would be difficult. In addition, this impedance must be kept at a minimum to maximize the motional current of the device.

According to Equation 3.26c, the series resistance is proportional to η^{-2}. Assuming that the available DC voltage is limited by other devices in the IC process being used, $\frac{\partial C}{\partial x}$, which is proportional to t/d^2, is the only design parameter that can affect the series resistance. Furthermore, assuming that mechanical Q is constant and that t is limited by the chosen process (in the SOI process chosen for this work, the thickness of the disk is limited by the thickness of the top Si layer), the initial gap spacing, d, remains as the only design variable that affects the series resistance. As seen from Equation 3.26c, R_{eq} is proportional to d^4 so any decrease in the gap

Parameter	Value	Units	Parameter	Value	Units
Physical Constants			Calculated Parameters		
Material	SCSi		Frequency, f_o	274.2	MHz
Radius	10	μm	Physical Mass	249	pg
Thickness	340	nm	Eq Mass, m_{eq}	189	pg
DC Voltage	50	V	Eq Spring, k_{eq}	5.63E+05	
Gap Spacing	100	nm	Electrical Lumped Elements		
Q-Factor	9400		Coupling, η	420	nC/m
Young's Modulus	165	GPa	Capacitance, C_{eq}	0.31	aF
Poisson's Ratio	0.22		Inductance, L_{eq}	1.07	H
Density	2330	kg/m^3	Resistance, R_{eq}	185	kΩ

Table 3.2: Summary of physical constants and calculated parameters for prototype disk resonator.

spacing will dramatically decrease the series resistance. Figure 3.6 shows the effect of the gap spacing on the simulated transmission coefficient of the equivalent model shown in Figure 3.5 with component values listed in Table 3.2, referenced to a 50 Ω termination[5]. At a gap spacing of 100 nm, the resonance condition is barely noticeable at 275 MHz and the impedance mismatch limits the transmission to -75 dB. On the other hand, the transmission at resonance is quite evident for a gap spacing of 10 nm, emphasizing the need for small gap spacings.

The 10 nm case also shows the two modes of resonance for the equivalent circuit. The first is the series resonant frequency through the equivalent RLC series network representative of the fundamental contour-mode frequency. The impedance in this mode is slightly capacitive due to the shunt capacitance, C_o. At frequencies above the series resonant frequency, the series RLC circuit appears inductive. The shunt capacitance will resonate with the inductive RLC network at the parallel resonance frequency indicated in Figure 3.6. Quartz crystal references exhibit a similar transmission versus frequency curve.

[5]The choice of 9400 for Q-factor for this simulation was based on an empirical result from [36] for a similar disk. The effect of Q-factor on frequency response will be discussed later in this chapter.

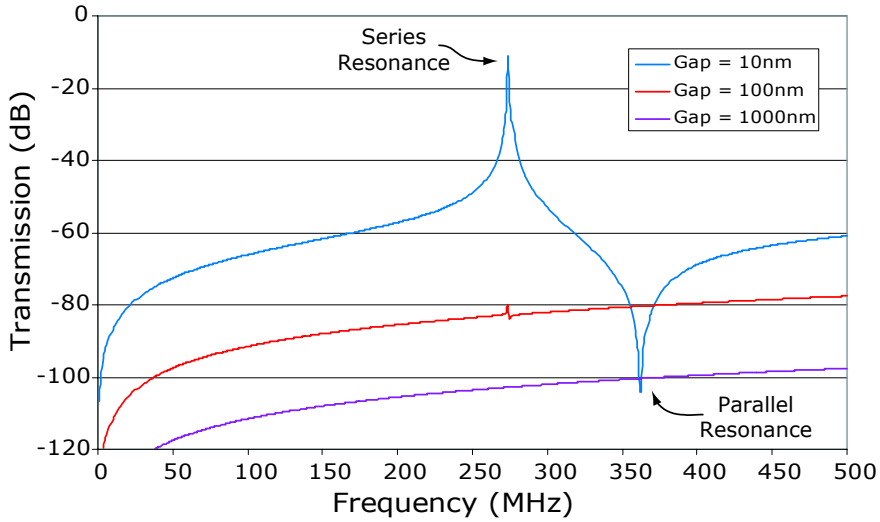


Figure 3.6: Simulated transmission coefficient versus gap spacing for the two-port equivalent model.

One-Port Model

In the one-port model, the AC excitation is applied in-phase to both electrodes and the current at both gaps is dependent on the AC excitation. The output gap is modeled as a separate series RLC circuit with a parallel static capacitor as shown in Figure 3.7(a) [32]. Again, since the input and output gaps are often fabricated to be identical, the network of Figure 3.7(a) can be simplified to the form shown in 3.7(b). Since the currents flow into the disk, the total current can be measured through the DC bias lines as described above. Alternatively, the reflection coefficient seen by the source could be measured as it would be in a normal one-port network analyzer measurement.

3.2.4 Resonator Nonlinearity

In Equation 3.16, $\frac{\partial C}{\partial x}$ was assumed to be a constant, i.e. the change in capacitance versus the displacement of the disk was assumed to be strictly linear. While this is true for comb-driven resonators as shown in Figure 1.17, it is not true in the case of disk and beam-shaped resonators. Ignoring small fringing fields, the capacitance

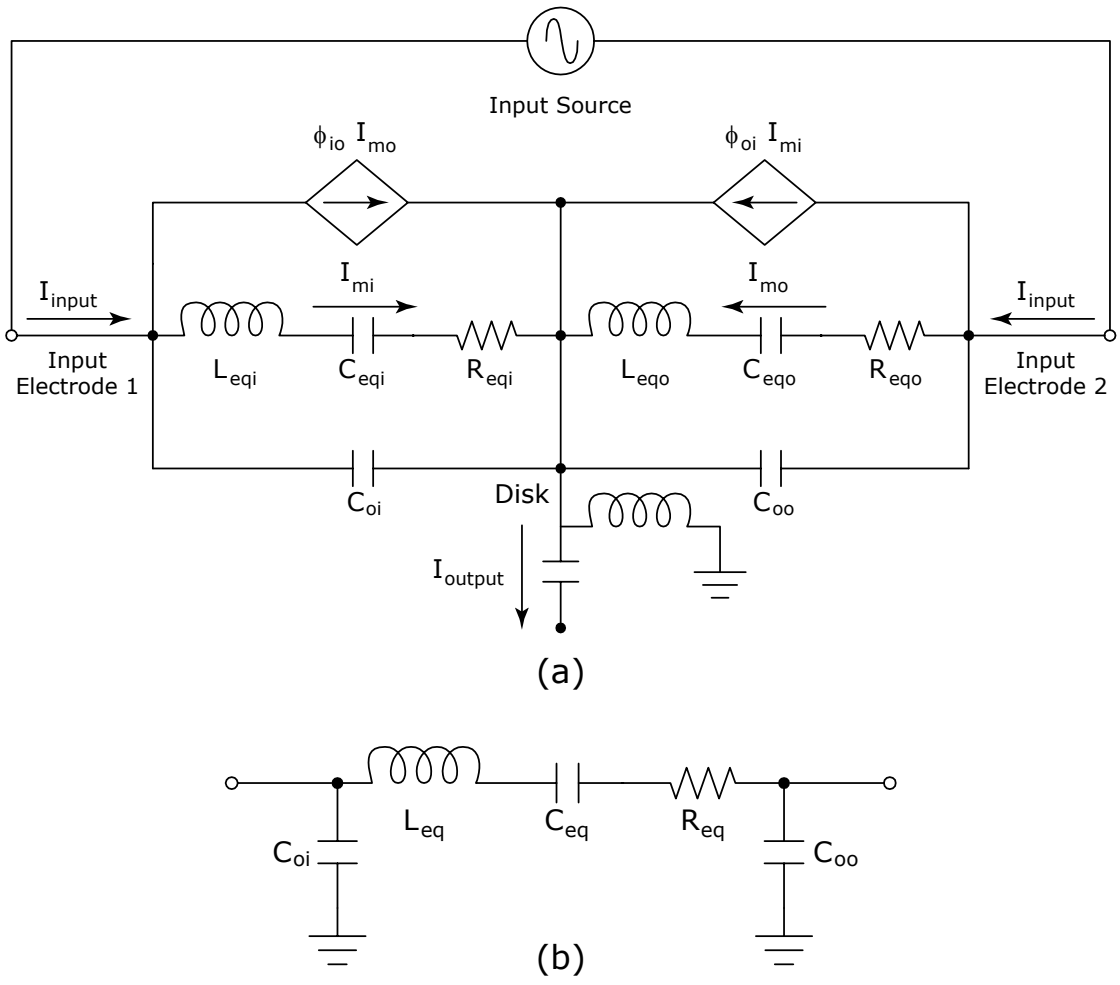


Figure 3.7: Equivalent circuit model for the one-port testing setup: (a) general model; (b) model for the case of identical gaps [32].

between the electrode and disk versus displacement can be expressed as [32]:

$$C(x) = \frac{\varepsilon_o A}{(d \pm x)} = C_o \left(1 \pm \frac{x}{d}\right)^{-1}, \tag{3.31}$$

where A is the area of the electrode directly parallel with the disk, d is the initial gap spacing between the electrode and the disk under no bias or excitation, C_o is the static capacitance between the nonresonant disk and the electrode, and x is the displacement of the disk away from or towards the electrode (with respect to the edge of the disk in a non-vibrating condition). Taking the derivative of Equation 3.31 yields the following:

$$\frac{\partial C\,(x)}{\partial x} = \frac{C_o}{\pm d}\left(1 \pm \frac{x}{d}\right)^{-2}. \tag{3.32}$$

For very small displacements, $x/d \approx 0$, $\frac{\partial C}{\partial x}$ can be assumed to be equal to $\frac{C_o}{d}$, a constant value. However, if the displacement of the disk edge is considered nontrivial, then $\frac{\partial C}{\partial x}$ will be a nonlinear quantity with respect to displacement.

The nonlinearity of the resonator can impact the frequency response and the power handling capability of the resonator. In terms of frequency response, the nonlinearity leads to a DC dependence on the center resonance frequency of the disk [32]. Perhaps the most important impact of nonlinearity, however, is the generation of harmonic distortion in the output of the resonator. If the resonator is operated in a two-port mode, harmonics present at the input of the resonator are filtered by the high Q-factor of the resonator and are generally not an issue; however, harmonics generated by the nonlinearity in the output gap distort the output signal. These distortions grow in magnitude with input power and set an upper limit on the power handling capability of the resonator. Harmonic generation can lead to higher phase noise in a oscillator application by increasing the total power in the spectral skirts of the output spectrum.

The effect of harmonic generation can be mitigated by decreasing the DC bias or increasing the initial, nonresonant gap spacing. By increasing the gap spacing, the ratio of the displacement, x, to the gap spacing, d, increases and $\frac{\partial C}{\partial x}$ can be assumed to be closer to the constant quantity $\frac{C_o}{d}$. Unfortunately, increasing the gap spacing and decreasing the DC bias have the effect of decreasing the electromechanical coupling coefficient η, and thus increasing the equivalent series resistance of the resonator. As discussed earlier, this resistance should be minimized in order to facilitate matching

between the resonator and other on-chip components. Thus, there exists a trade-off in resonator design between linearity and matching capability in resonator design. The resonators in this work are were initial proof-of-concept designs and therefore the V_{IIP3} was not specifically considered during the design. However, future filters and oscillators based on the disk resonator will have to be designed with nonlinear effects in mind.

3.2.5 Equivalent Electrical Model Summary

At first-order, the contour-mode disk resonator can be modeled as a series resonant RLC circuit with a parallel capacitance derived from the static capacitance between the electrode and the disk edge. Figures 3.5 and 3.7 show the equivalent models for the two-port and one-port testing setups, respectively. From these analytically derived models, it was shown that the electrode to disk resonator gap spacing was the most critical design variable due to its significant impact on the motional resistance and the linearity of the resonator. On the other hand, second-order effects such as processing variables, higher-order harmonic excitation, and damping effects must be modeled using a computational method. Finite-element analysis is one method capable of modeling these second order effects, and the results of such an analysis on various disk resonator structures are presented in the next section.

3.3 Finite Element Analysis

Finite Element Analysis (FEA) involves the discretization, or meshing, of a complex structure into numerous sub-structures, or elements. These elements are commonly simple shapes such as 3-D bricks or 2-D surface tiles for which the describing mechanical and electromagnetic equations can be easily formulated. By calculating interactions between elements and appropriately combining the results, FEA-based software packages can simulate the response of the entire meshed structure. The advantage of this method is the ability to accurately simulate the response of complex 3-D structures to multiple mechanical and electromagnetic stimuli in a fraction of the time it would take to create a comparable model through other analytic methods. For this reason, FEA has become a popular method for simulating complex problems

in thermodynamics, electromagnetics, and fluidics.

FEA models can include various second-order effects that may be impossible to account for using other methods. For instance, in this work, FEA was used to calculate the electromechanical frequency response of finite thickness Si disks, including effects of finite-sized center supports and edge-connected DC bias lines, and disks with non-ideal metal coatings. All of these effects are neglected in the lumped-element model presented in the previous section. Additionally, the effects of gap-spacing, DC bias and small-signal excitation levels, and higher-order harmonic vibration were studied with the FEA model and compared to the results of the analytical lumped-element model.

3.3.1 Frequency Response of the FEA Model

Figure 3.8 shows a finite element model of a simple disk resonator structure created in the FEA software package ANSYS [83]. The lines shown across the surface of the disk represent the boundaries of the elements used to describe the physical structure. These elements are ANSYS 'SOLID45' 3-D bricks with eight nodal points (one at each corner) and three degrees of freedom at each node (translation in the x, y, and z directions). SOLID45 elements support a wide range of simulations including the mechanical harmonic and modal analyses used to determine the vibration response of the disk.

To model the electromechanical transduction across the input and output gaps, an array of ANSYS 'TRANS126' elements are created around the circumference as shown in Figure 3.8 (The size of the TRANS126 elements is exaggerated in the figure; in reality, the size of the element is equal to the gap spacing.) The TRANS126 element has two nodes, one is attached to the disk edge and is free to move in the three polar DOFs (radial displacement, rotation, and z-direction displacement), while the other is located in space at a radial distance from the disk edge determined by the gap spacing. This node is then constrained in all three polar DOFs to model the static, non-moving electrode. A single node on the bottom center of the disk is also constrained in all three polar directions to simulate the nodal point of contour-mode vibration.

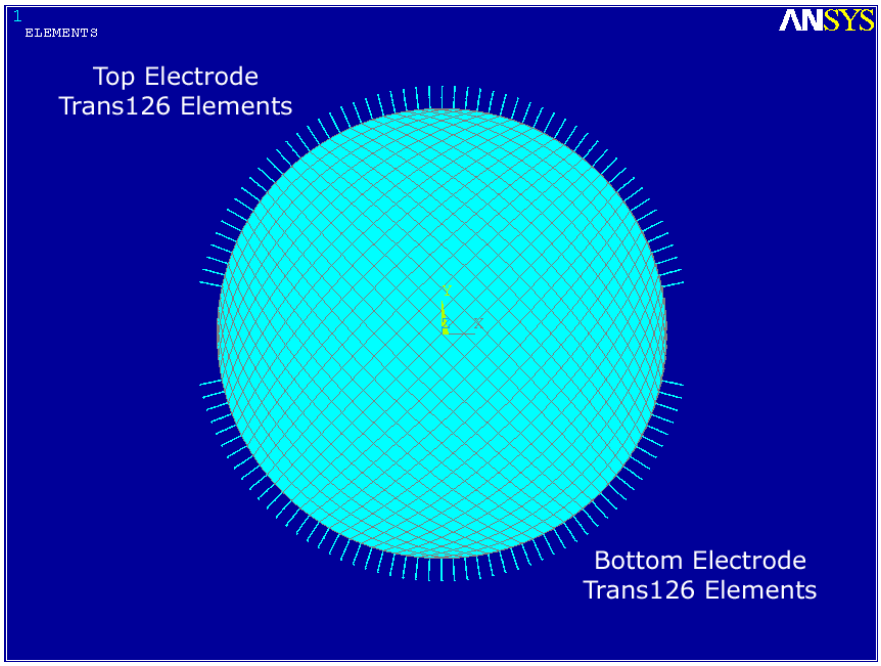


Figure 3.8: FEA model of a simple disk resonator structure with TRANS126 transducer elements.

Figure 3.9 shows the transduction curve for the TRANS126 element. A DC or AC voltage applied to the electrode side of the element is transduced into a static or time-varying force respectively at the disk side. As expected, this force varies nonlinearly with the displacement of the disk relative to the electrode (see discussion in Section 3.2.4). At a certain displacement, the TRANS126 element assumes the disk has come into contact with the electrode and the force due to the capacitance levels off at the maximum value before contact.

To model the frequency response of the disk, three separate FEA simulations must be performed. Initially, a one-port testing configuration was simulated [see Figure 3.4(a)]. The radius, thickness, and Q-factor listed in Table 3.2 were used for these simulations; however, the gap spacing was narrowed to 30 nm, the smallest achievable gap to-date using the in-house SOI fabrication process shown in Figure 1.21. First, a DC bias of 5 V was applied to the disk side of the TRANS126 element and the electrode side was grounded. A DC simulation was then performed to determine the stress in the disk due only to the DC bias. The results of this prestress analysis were then included in a modal analysis that calculates all possible resonant modes

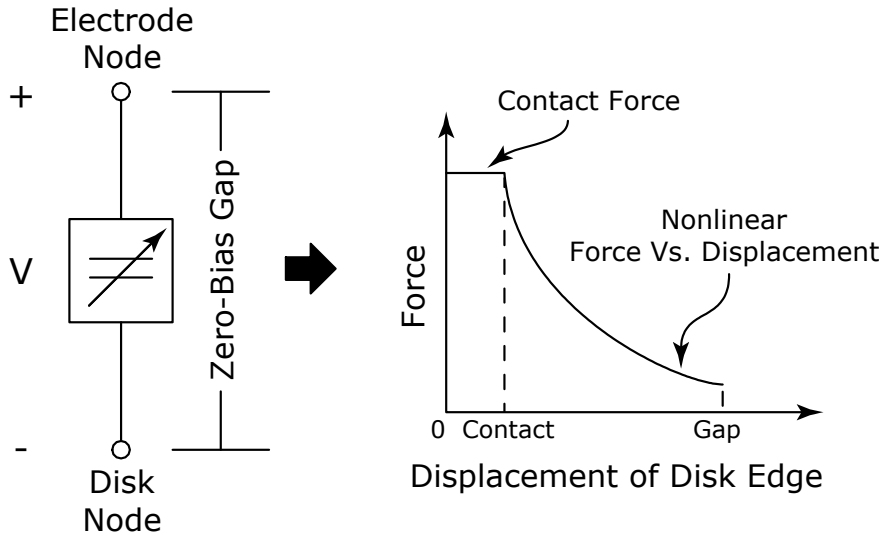


Figure 3.9: Schematic and transduction curve for the TRANS126 element.

in a given frequency range. The contour-mode frequency was identified from the predicted modes by plotting the radial displacement of each mode and comparing the results to the expected radial displacement in the contour mode. Finally, an AC voltage was applied to both electrodes in phase and a non-linear harmonic simulation was performed for a range of frequencies centered at the contour-mode frequency to determine the displacement of the disk and the total current through the transducer element versus frequency. The maximum radial displacement for a disk resonator with the parameters described is shown in Figure 3.10. The concentric circles indicate areas of equal displacement, with red representing the largest displacements from steady-state. The contour-mode frequency solved by ANSYS was 275.00 MHz, very close to the 274.2 MHz predicted by the electromechanical model derived in the previous section.

One advantage of the ANSYS FEA model is that both current and displacement data can be taken from the simulation results. Figure 3.11 shows the average peak displacement of the nodes located on the edge of the disk and the magnitude of the current across the TRANS126 elements that define the gap. Both curves show the resonant condition at 275 MHz and the lack of significant displacement and current away from this resonance.

The total gap current can be decomposed into real and imaginary components as

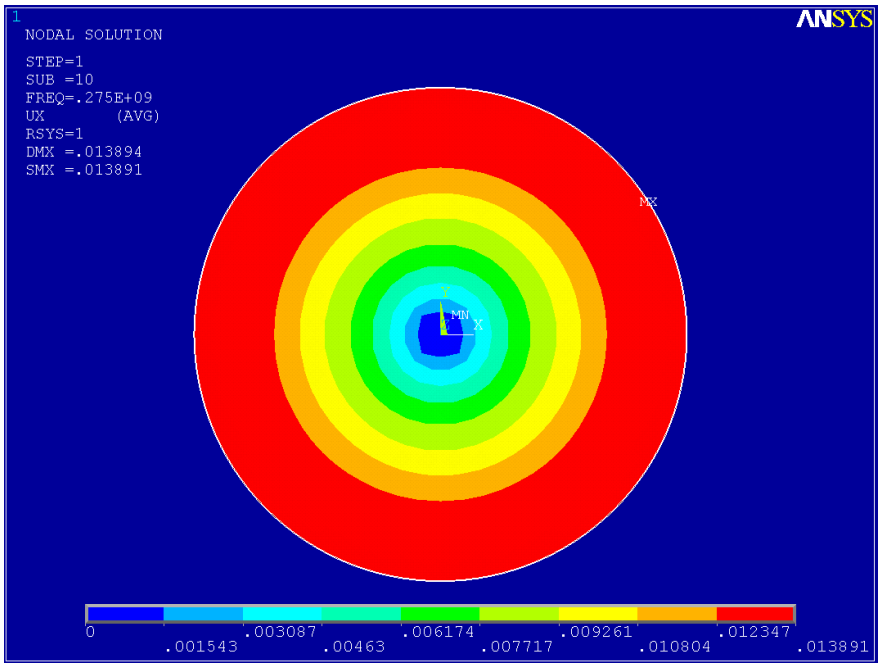


Figure 3.10: Maximum radial displacement of the disk resonator at the contour-mode frequency (displacement legend is in microns).

shown in Figure 3.12. The peak real current, i.e. the current that is in-phase with the excitation signal, occurs at the series resonant frequency of the motional RLC equivalent circuit in Figure 3.7(b). At this frequency, the motional inductance and capacitance resonate and the impedance of the series RLC circuit is purely resistive. This resonance is equivalent to the contour-mode resonance. At frequencies other than resonance, the current is essentially zero. The imaginary current, i.e. the current out of-phase with the excitation signal, generally increases linearly with frequency as one would expect for the current through the shunt capacitance C_o. As the frequency approaches the contour-mode resonance frequency of 275 MHz, two peaks appear. The first occurs at 274 MHz and can be explained by the decrease in the imaginary impedance of the series RLC circuit as the frequency approaches resonance. The second occurs at 276 MHz and can be explained by a parallel resonance of the series RLC circuit with the static capacitance C_o. At the contour-mode frequency, the imaginary current through the RLC series circuit is zero; thus the imaginary current is equal to the current through C_o.

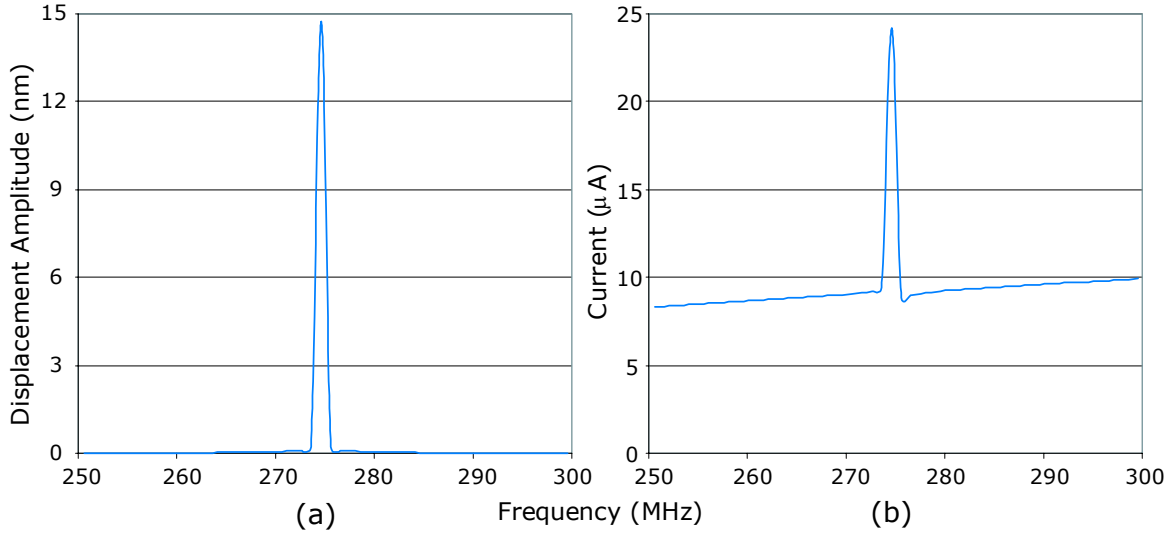


Figure 3.11: Simulation results for the disk resonator of Figure 3.8: (a) average peak displacement of the disk edge nodes; (b) total current across the gaps between the disk and the two excitation electrodes.

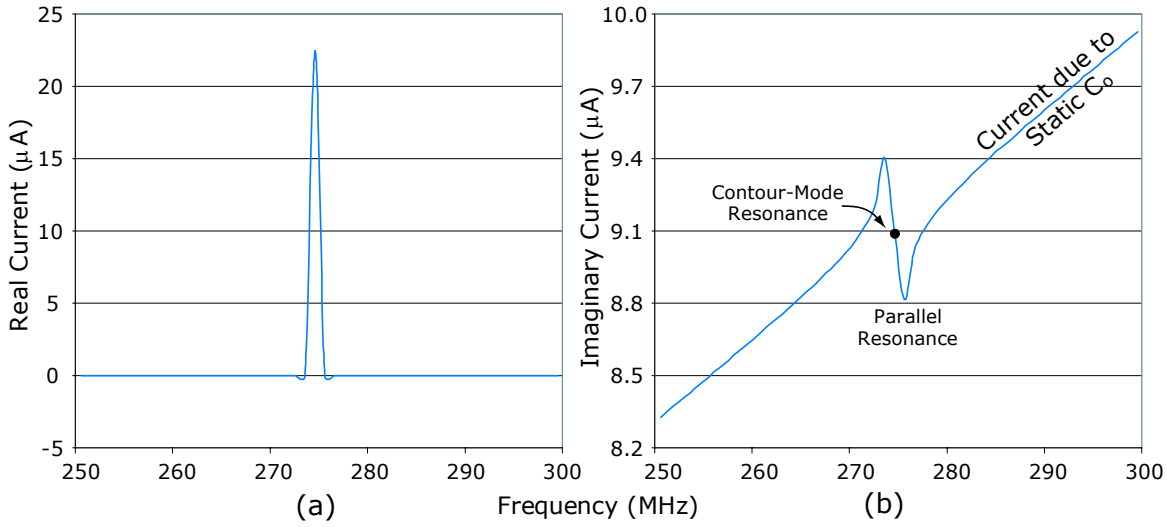


Figure 3.12: Components of total current shown in Figure 3.11(b): (a) real component; (b) imaginary component.

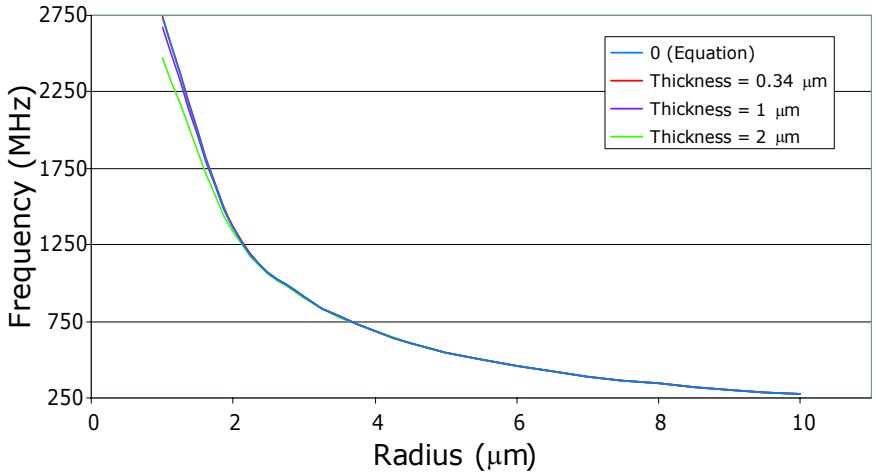


Figure 3.13: Predicted contour-mode resonant frequency versus disk radius for Equations 1.20 and 1.21 versus those predicted by ANSYS for 3 non-zero thicknesses.

Resonant Frequency Versus Radius and Thickness

The contour-mode resonance frequencies predicted by Equations 1.20 and 1.21 assume an ideal disk of zero thickness. Obviously, disks of zero thickness are not realistic in practice and FEA simulations accounting for disks of finite thicknesses are used for making more accurate predictions of the actual frequency response of a disk. Figure 3.13 shows the comparison between the center frequencies predicted by Equations 1.20 and 1.21 versus those predicted by ANSYS for disks of various thicknesses. As can be seen in the figure, there is actually strong agreement between the frequency equations and the ANSYS simulations even for non-zero thicknesses. The only significant deviations from the ideal results occur when the disk thickness is equal to or greater than the disk radius, and even then, the maximum deviation is only $\sim$10% for the 2 μm thick disk. The decrease in frequency with increasing thickness agrees with empirical results from Clark, *et al.* [36]. Nonetheless, FEA simulations are still needed to account for other second-order variables such as the effect of disk anchors and non-ideal coatings. These second-order effects are discussed in the following sections.

3.3.2 Anchor Effects

As shown in Figure 3.4, DC bias lines are connected to the edge of the disk resulting in nodal points that are not accounted for in the simple disk model. While the disk resonators described in [36] use a multiple-step lithography process that enables connecting of the DC bias to the center post (Figure 1.20), the SOI process used for this work dictated that the DC bias lines be in the plane of the electrode and the disk. Additionally, the central nodal point is assumed to be singular in the simple model, whereas actual fabricated disks have center posts of finite size. To simulate the effects of these non-ideal anchor conditions on the disk frequency response, simulations were performed for posts of varying radii and for disks with and without the DC bias lines. Figure 3.14 shows the contour mode response for a disk with DC bias anchors attached and a 1 μm radius central post. The changes in mode shape due to these factors are negligible and the resonant frequency only increases to 275.2 MHz, which can be explained as the result of the increased stiffness of the disk with the added constraints. As seen in the top view in Figure 3.14, the DC bias lines oscillate as clamped-clamped beams in the second harmonic mode. The loss attributed to these added anchors is discussed in Section 3.4.

Figure 3.15 shows the FEA simulated center contour-mode frequency versus central post radius for disks with and without the DC bias lines. Both cases show a quadratic relation between the size of the post and the frequency of vibration. The frequencies for the disk with the DC bias lines are only slightly higher than those without the DC lines. This is an important result since it was not known if the disks would support the contour-mode vibration with the additional anchor points.

Figure 3.16 compares the displacement amplitude and total motional and static current across the gap for the disks with and without the DC anchors. As expected, the current values show the same trends as the displacement values. The results for the DC-bias connected disks also closely follow the results for the non-biased disks expect for post radii of around 3, and 6 μm (the discrepancy at 0 μm is most likely a simulation anomaly due to the non-physical nature of the singular central nodal point). At these radii, the vibration mode shape deviates significantly from the contour-mode shape, and this deviation is more significant for the disks with DC bias connections. Figure 3.17 shows an isometric view of a DC-bias connected disk

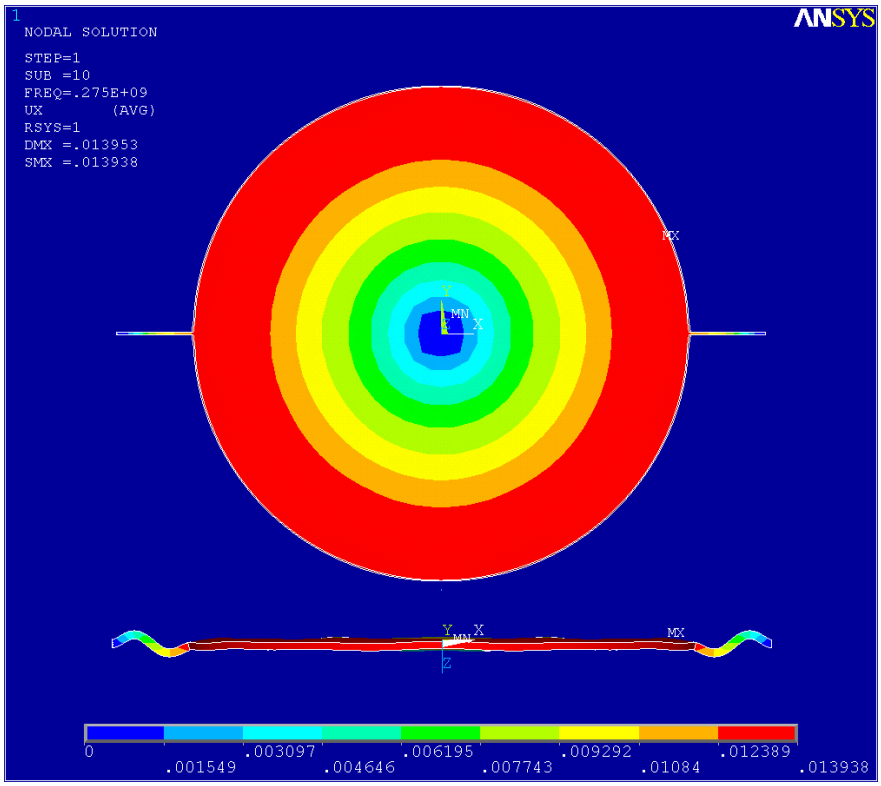


Figure 3.14: Front and top views of contour-mode vibration with DC bias-line effect.

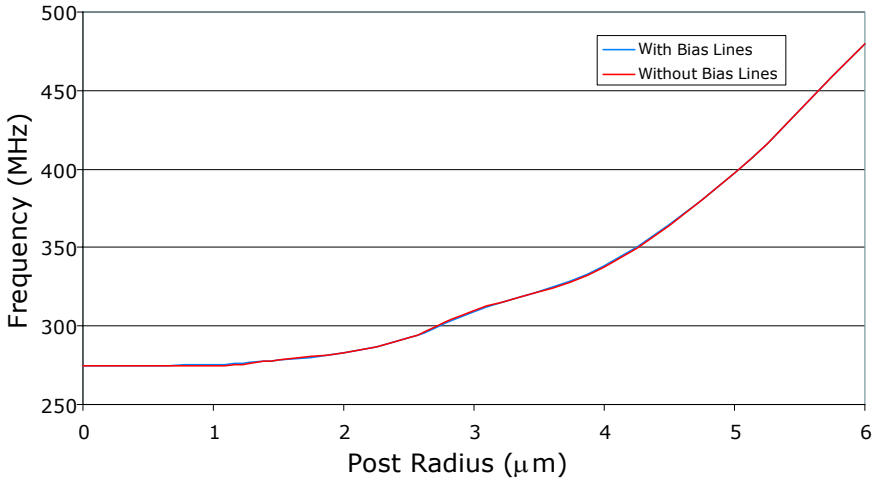


Figure 3.15: Center frequency versus post radius for disks with and without DC bias lines.

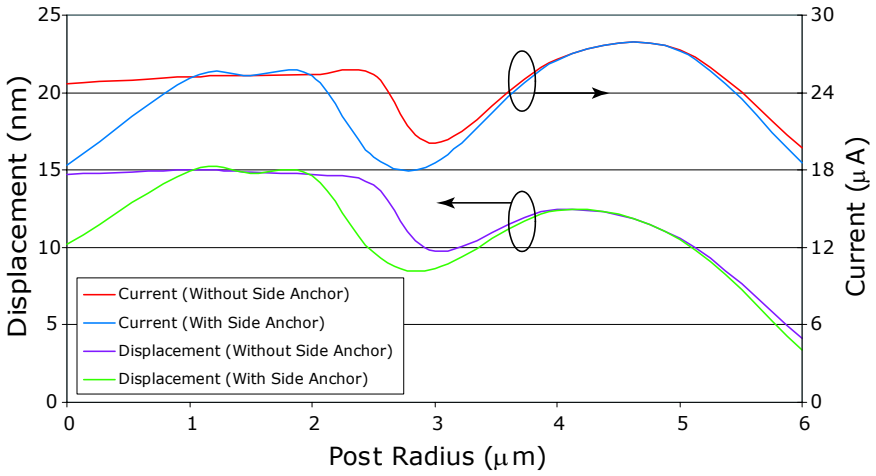


Figure 3.16: Displacement and current versus post radius for disks with and without DC bias connections.

with a 3 μm radius post size. The energy lost due to the out-of-plane (z-direction) displacement in this mode is responsible for the decreased radial displacement and current. It is not known if this is a numerical anomaly of the FEA model or if it is a representation of how an actual disk would react under these conditions. However, the same simulations were run with various mesh densities and convergence criteria with the same results. This leads to the conclusion that the data is a representation of a physical phenomenon that may arise due to the combination of two modes that occur at the same frequency for this particular geometry.

The center post size is determined by a post-lithography timed wet-etch release step (Figure 1.21, Step 8). This process step will be further discussed in Chapter 4; however, in simple terms, the longer the etch time, the smaller the diameter of the post size. Since the current does not suffer from the increased post size (with exceptions for radii $\sim$ 3 μm and $\gtrsim$ 6 μm), and since the frequency is dependent on the size of the post, contour-mode resonators could be tuned for a specific center frequency during fabrication by timing the disk release etch.

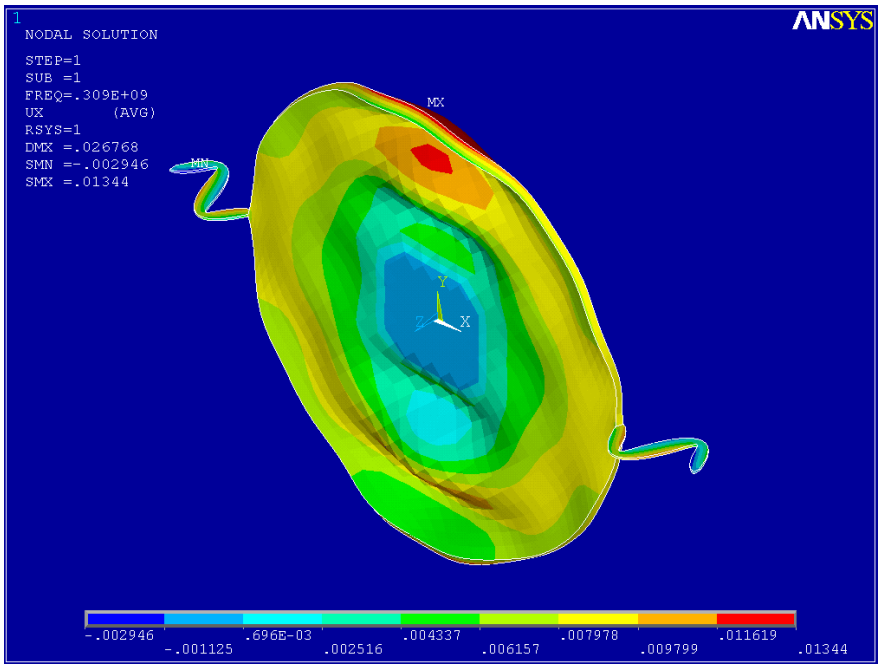


Figure 3.17: Isometric view (exaggerated in the z-direction) of a DC-biased disk with a 3 μm radius post size.

3.3.3 Metal Layer Effects

All simulations presented to this point assumed that the disks were fabricated from a single homogeneous material, single-crystal Si. While this would be ideal from a Q-factor standpoint, the processing method chosen for this work requires that a metal layer be deposited on the surface of the disk to act as an etch mask. The metal mask is used to protect the areas of the disk resonator and electrodes during the reactive ion etch of the top layer of Si (Figure 1.21, Step 4). The metal mask could be removed after the RIE step, however the metal also provides a more electrically conductive path along the resonator structure and to the electrodes. Even though the Si substrate is doped to approximately 18 $\Omega \cdot$ cm, the resistivity is still 7 orders of magnitude larger than metals such as Au or Al. Unfortunately, the metal layer potential introduces second-order effects such as Q-degradation and frequency-lowering due to the lower stiffness of the metal layers compared to single-crystal Si.

To determine the effect of such metal layers, SOLID45 elements representing the metal are meshed on top of the silicon disk. The simulations for the metal-covered disk

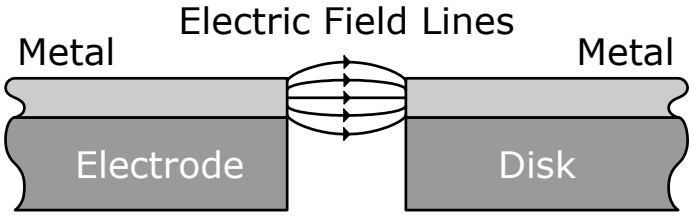


Figure 3.18: Electric field lines between the disk and electrode under AC excitation.

proceed as those for the regular disks except that the electric field lines are assumed to be concentrated between the metal layer on the electrode and the metal layer on the disk as shown in Figure 3.18 with only small fringing fields terminating on the Si layer. Therefore, the TRANS126 transducer elements are only connected to the top metal layer and not to the underlying Si. This reduces the overall force driving the disk; however, this configuration is a more accurate representation of the actual disk operation.

Figure 3.19 shows the frequency response versus total film thickness for disks coated with Au on a Cr adhesion layer and disks coated with just Cr for comparison (the total thickness was kept the same in each case). Gold was chosen for its high relative conductivity and ease of deposition; however, its propensity to diffuse into the Si lattice and poor adherence to Si requires the use of an intermediate barrier layer. Chromium was chosen for the intermediate layer due to its excellent adhesion to Si and immunity to the HF wet etch release step. Since the E/ρ ratios for both Cr and Au are less than that of Si (Figure 1.15), the center frequencies of the coated disks are lower than that of the uncoated disk. The Au coating results in a much lower center frequency and a more drastic change in frequency as the thickness is varied due to the large difference in E/ρ ratios of Cr and Au. The inverse relation between thickness and frequency leads to a design trade-off between conductivity and frequency. Thick layers of Au offer higher conductivity, but with a significant impact on resonant frequency; whereas thin Cr layers offer a lower deviation in frequency but higher electrical losses.

Figure 3.20 shows the relationship between the vibration displacement amplitude and total current across the gap versus the total thickness of the metal layers[6]. Since

[6]The current values only represent the motional current across the gap due to the vibration and

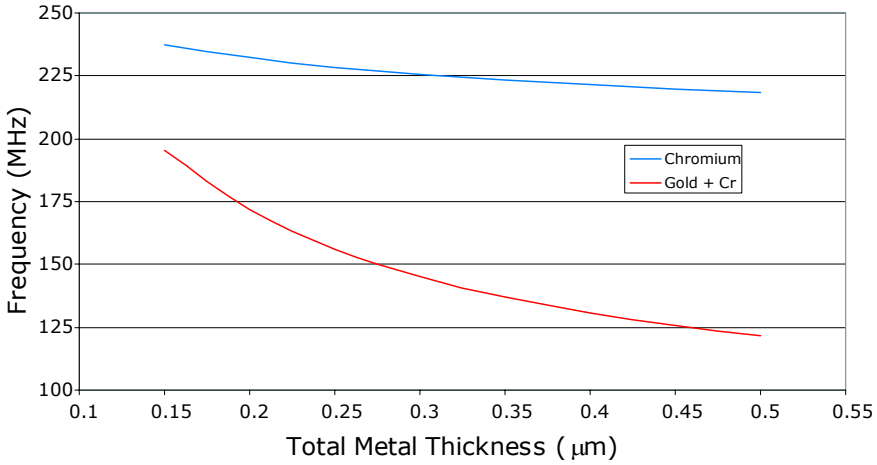


Figure 3.19: Frequency versus thickness for evaporated films of Cr only and Au with a Cr adhesion layer.

the capacitance was only assumed to be between the metal layers on the disk and electrodes, the currents and displacements in Figure 3.20 are slightly lower than shown in Figures 3.11, 3.12, and 3.16. However, it is believed that these values are a more accurate depiction of the expected displacements and currents of a fabricated disk due to the inclusion of the metal layers and the modeling of the capacitance. It may be surprising that the Cr/Au disk has a smaller through current despite the higher value for the displacement amplitude. Since the magnitude of the current through the static capacitance, C_o, increases with frequency, it can be expected that the current across C_o will be the largest for the disk that vibrates at the highest frequency. The frequency of vibration of the Cr-coated disk is significantly higher that that of the Cr/Au disk, therefore the total current (motional + C_o current) is higher for the Cr disk.

3.3.4 Transducer-Related Variables

The electrical models derived in Section 3.2.3 can relate the current across the gap of the ideal disk to transducer-related variables such as the gap spacing, the DC bias, and the AC excitation magnitude. The ANSYS simulations described in this subsection determine the displacement and current across the gap for a non-ideal disk

do not account for the conductivities of either metal layer.

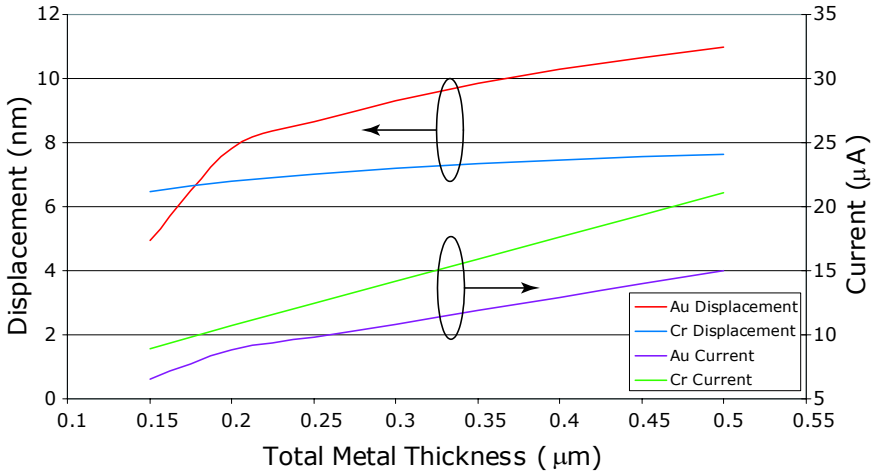


Figure 3.20: Displacement amplitude and through current for evaporated Cr and Au films.

with finite thickness and edge-connected DC-bias lines.

Figure 3.6 shows the relationship between the transmission of the two-port model and the gap spacing between the electrode and the disk. From this plot, it is evident that a decrease in gap spacing results in a significant increase in the signal transmission at resonance. However, there is a limit to how much the gap can be reduced before the electrostatic forces acting on the disk pull the disk edge into contact with the electrodes. This effect is known as "pull-in" and the resulting short-circuit would likely destroy the resonator. Unfortunately, the simple lumped-element model yields no insight into the value of the pull-in voltage of the resonator, so a series of ANSYS simulations were run to ascertain these voltages for a number of different gap-spacings.

The pull-in voltage is determined by three factors: the gap spacing; the DC voltage; and the amplitude of the AC excitation voltage at the electrodes. Assuming a peak AC excitation voltage amplitude of 1.0 V, the relationship between the vibrational displacement amplitude and the DC bias voltage is shown in Figure 3.21 for 4 different gap spacings. The displacement amplitude shows a linear relation to the DC voltage, which is expected since the electromechanical coupling coefficient is directly related to the bias voltage. (It should be noted here that ANSYS does not accurately model the displacement of the disk close to the pull-in voltage, and it is expected that, in reality, the relation between the DC bias and displacement will deviate somewhat from the linear prediction close to the pull-in voltage.) The pull-in voltage increases

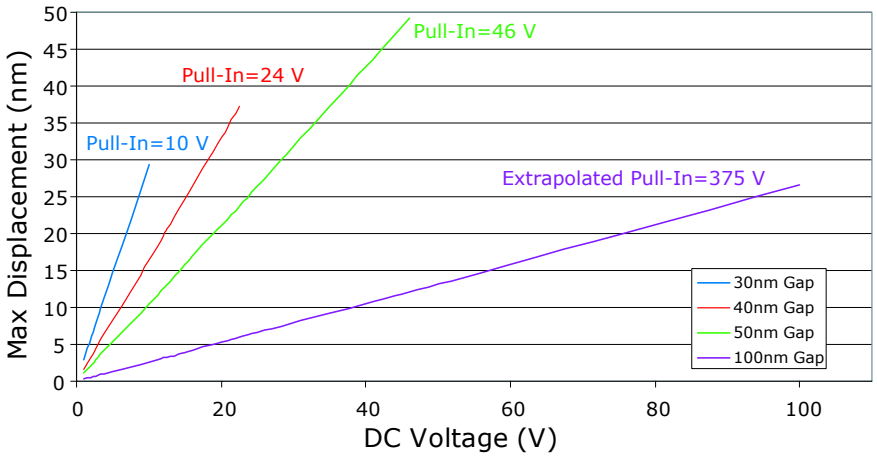


Figure 3.21: Displacement amplitude versus DC bias voltage for 4 values of zero-bias gap spacing. (In reality, the displacement will show a nonlinear relation with the DC-bias at values close to the pull-in voltage.)

quadratically with gap spacing, with spacings of 100 nm exhibiting a very high pull-in voltage of 375 V. However, it is likely that the disk would fail due to the high current densities well before pull-in at this high a voltage and operating voltages of this magnitude are not practical in modern IC technology. On the other hand, the pull-in voltage for the 30 nm gap case is only 10 V.

Since the current across the gap is a more meaningful quantity to electronics designers than the displacement of the disk, this quantity is plotted for the same DC voltages and gap spacings in Figure 3.22. The quadratic relation between bias voltage and current is expected since the current is related directly to both the displacement and bias voltage as given in Equation 1.15. From this plot, it is evident that higher values of current can be supported by larger gap devices due to the higher values for device pull-in. However, the voltages required to achieve these currents are exceedingly high for realistic IC implementations. The goal, then, becomes engineering the gap to be as small as possible to maximize the current from relatively lower on-chip voltage supplies.

Figure 3.23 compares the displacement and current of the 50 nm gap case versus DC bias voltage with peak AC excitation voltages of 1.0 V and 2.0 V. The rate of change of both the displacement and the current versus the DC bias are doubled by the increase in AC excitation voltage, implying a linear relation between the displacement,

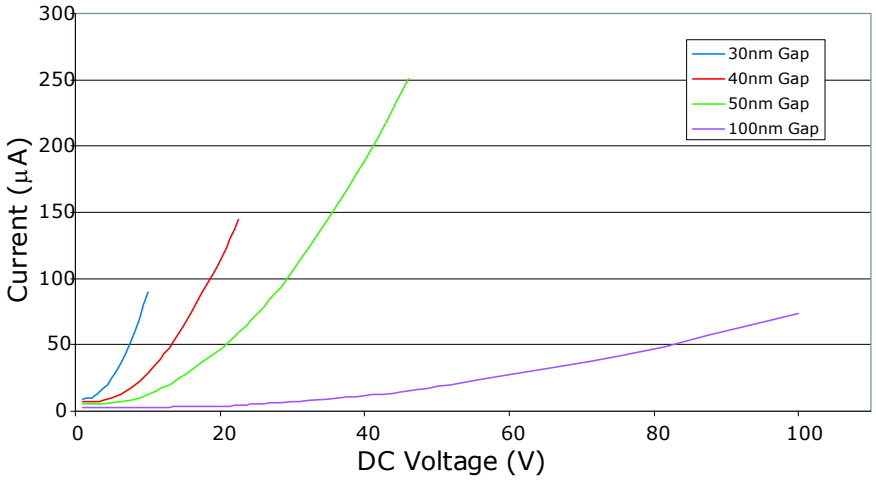


Figure 3.22: Current across the gap versus DC bias voltage for four values of zero-bias gap spacing.

current, and AC excitation voltage. The pull-in voltage is reduced by one-half to 23 V for the 2.0 V case, meaning that the maximum achievable current before pull-in is also halved. On the other hand, higher currents are possible at lower bias voltages with the higher AC excitation voltage.

Another effect not accounted for in the electrical lumped element model is the relationship between the DC bias and the contour-mode resonant frequency. Figure 3.24 shows this relation for the four gap spacings simulated previously. The plot does show an inverse relation between the disk resonant frequency and the applied voltage; however, the maximum change in frequency is only 0.2 %. Therefore, it is impractical for a single disk resonator to be used as the tunable element in a VCO application due to the small tuning range. It is more likely that tuning would be accomplished through an array of resonators with different diameters that would each individually vibrate at one of the center frequencies required by the application. The resonators could be then switched on and off through the applied DC bias voltage and tuning would be analogous to the switched capacitor discrete tuning of the VCOs in Chapter 2. Due to the very high Q resonances, the need for PLL frequency control could potentially be obviated.

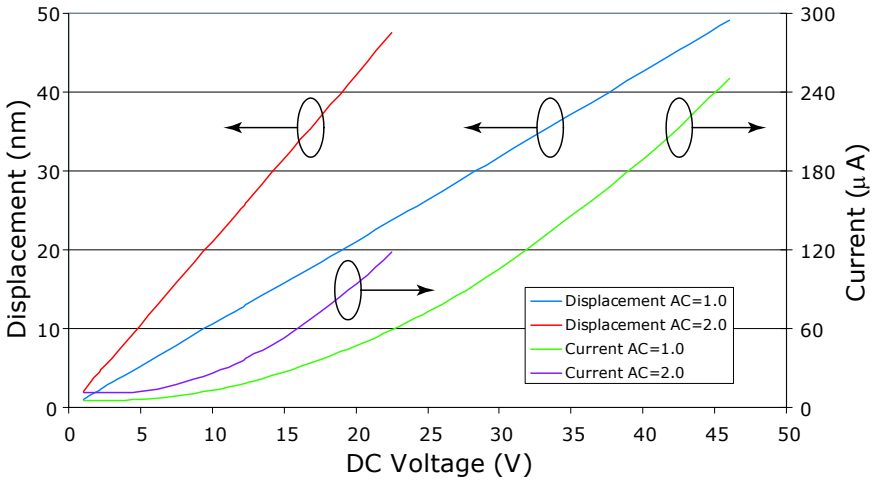


Figure 3.23: Displacement and current versus DC bias voltage for two values of AC excitation voltage with a 50 nm zero-bias gap spacing.

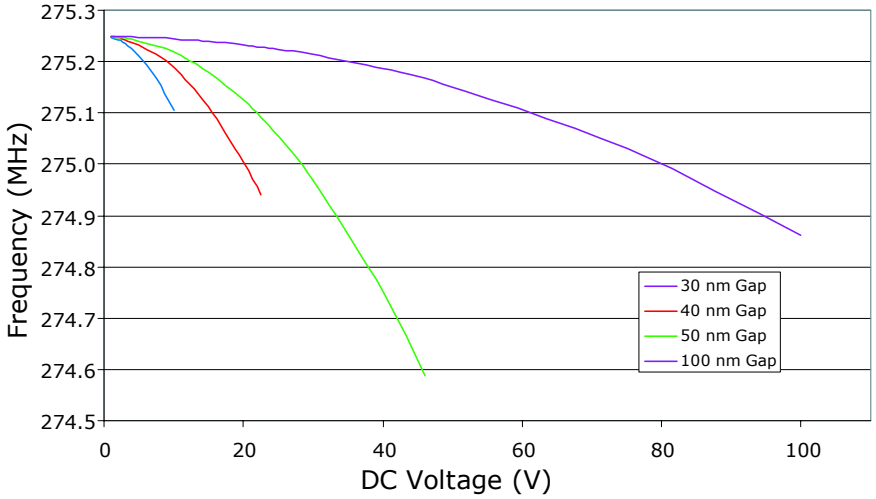


Figure 3.24: Frequency versus DC bias voltage for 4 values of initial gap spacing.

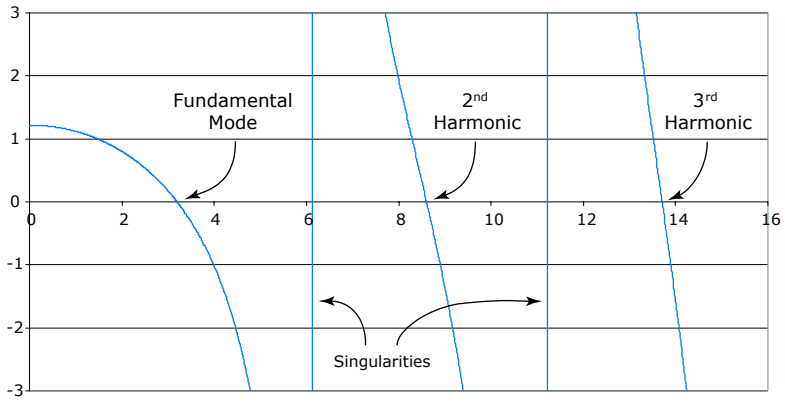


Figure 3.25: Plot of Equation 1.20 versus the frequency parameter γ.

3.3.5 Contour-Mode Harmonics

For on-chip MEMS resonators to be viable as tank circuits for high-frequency local oscillators, their center frequencies must be increased into the GHz regime. Previous examples have shown fundamental contour-mode resonators with center frequencies in the 200-300 MHz range. However, vibrational frequencies exceeding 1 GHz have been obtained in disk resonators by exciting higher-order harmonics of the contour-mode [37]. The frequency of these modes can be found through the higher-order roots of Equation 1.20. Figure 3.25 shows a plot of Equation 1.20 versus the frequency parameter γ and identifies the harmonics at the zero-crossings.

ANSYS simulations were performed to study the mode shapes at these harmonics and to investigate the displacement and current of these modes. Table 3.3 compares the ANSYS frequency results with that of the frequency equation and lists the response values at each mode. ANSYS closely agrees with the predictions of the equation for the center frequency. As expected, the displacement decreases for the higher order harmonics; however, the current values actually increase due to the increasing frequency. As stated earlier in Section 3.3.3, higher frequencies will result in higher current values through the static capacitor, C_o, and thus increase the total current across the gap. Excitation at the third harmonic allows high-frequency vibration with no change in disk geometry.

Figure 3.26 shows a plot of the simulated radial displacement of the 2^{nd} harmonic. The higher harmonics are characterized by the addition of nodal circles (the green ring

Harmonic	Equation Freq (MHz)	ANSYS Freq (MHz)	Disp (nm)	Current (μA)
1st	274.3	274.6	14.8	24.2
2nd	737.8	740.4	1.66	26.2
3rd	1176	1186	0.65	40.6

Table 3.3: ANSYS results for excitation of higher-order modes.

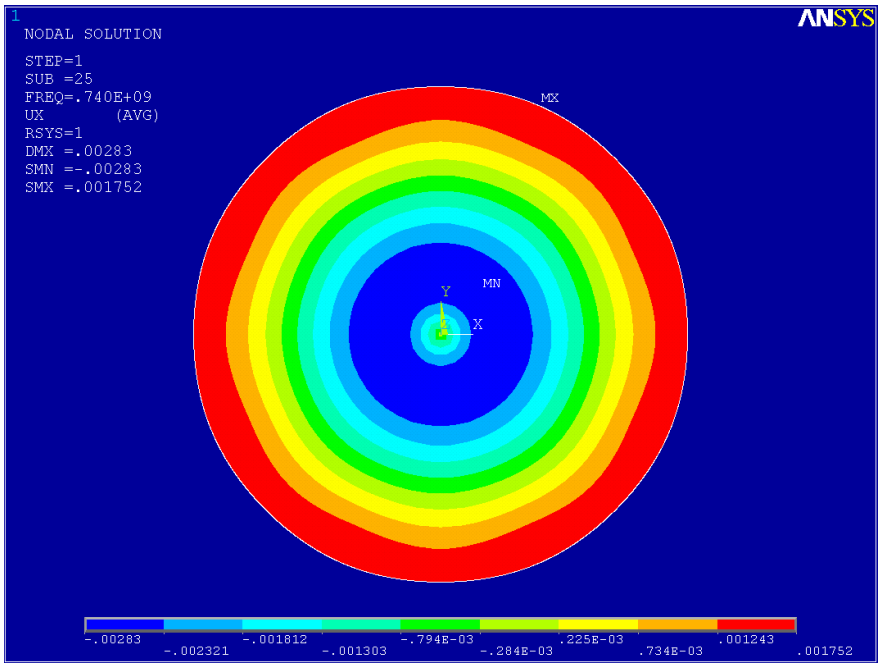


Figure 3.26: Radial displacement of the 2^{nd} harmonic contour-mode.

centered at exactly one-half radius from the center of the disk) to the fundamental contour-shape. These nodal circles are areas of zero vibration and result in the lower displacement for these modes. The 3^{rd} harmonic has two such circles centered at exactly one-third and two-thirds of the radius of the disk.

3.3.6 Two-Port Versus One-Port Actuation

All of the simulations discussed to this point have assumed a one-port excitation/ measurement setup, i.e. the excitation signal is applied symmetrically to both electrodes. Since a two-port excitation/measurement setup may be more advantageous for the reasons discussed above, simulations were performed to ascertain the effect

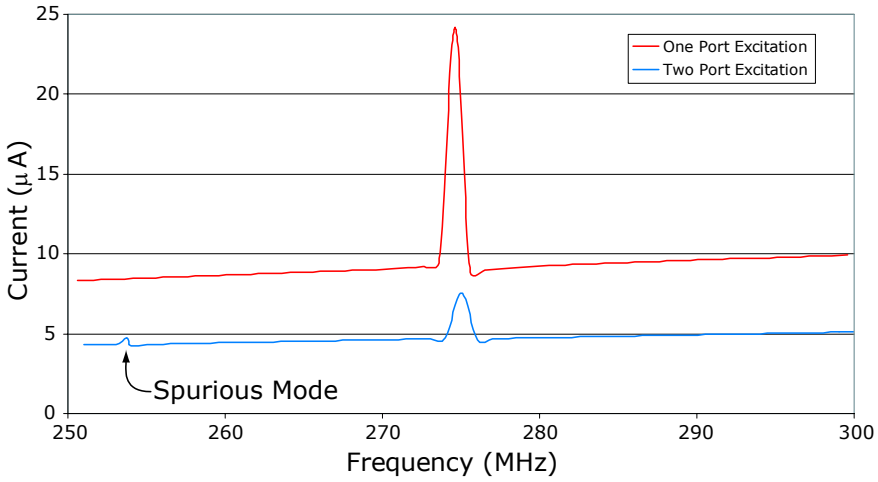


Figure 3.27: Comparison of the current across the gap for the two-port and one-port excitation/measurement setups.

of the asymmetric actuation with this case. In Figure 3.27, the current across the electrode/disk gap of a two-port setup is compared to that of the one-port current results of Section 3.3.1. As expected from the discussion in Section 3.2.3, the current due to the static capacitor is reduced by a factor of two in the two-port setup; however the overall peak current is diminished by a factor of more than 3. The two-port setup also introduces a spurious mode at approximately 254 MHz. This "push-pull" mode is characterized by lateral motion of the entire disk towards and away from the excitation electrode and is a result of the asymmetric force on the disk. The displacement for this mode is shown in Figure 3.28. The excitation is applied to the top electrode and most of the radial displacement is in the direction of this electrode. For large input powers or large bias values, this spurious mode could lower the selectivity of filters based on two-port resonators.

3.4 Estimating Q-Factor

The Q-factor for the above simulations was assumed to be 9400, an empirical value from contour-mode resonator measurements performed by Clark, *et al.* [36]. This assumption was made due to the difficulty in predicting the Q-factors of these resonators structures prior to their fabrication and measurement. Unfortunately, ANSYS has

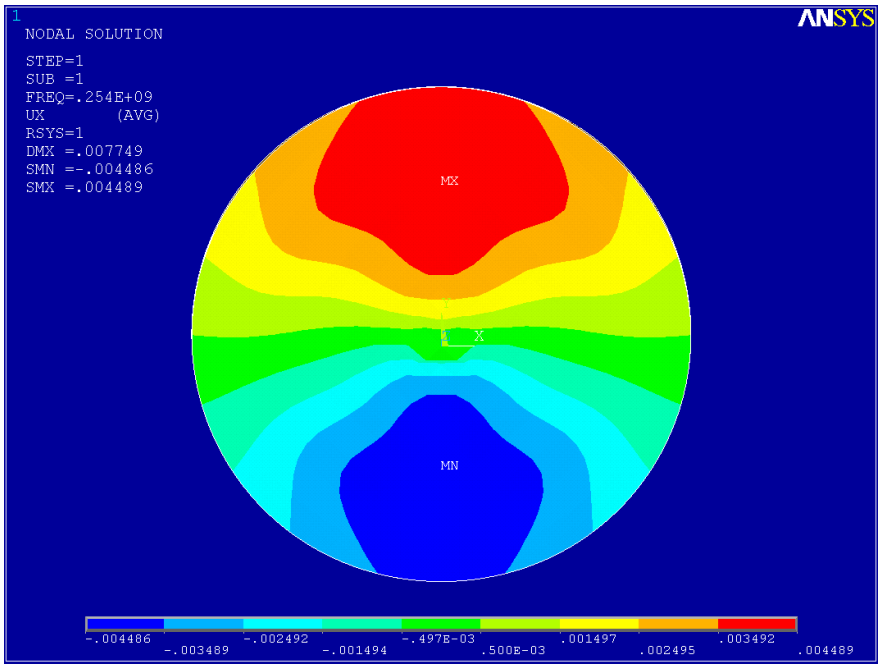


Figure 3.28: Radial displacement of disk in the spurious mode arising from two-port excitation/measurement.

no mechanism to calculate Q-factor – it must be supplied by the user as a constant damping ratio (ζ). Performing a simple simulation of the edge displacement of the Si disk in Section 3.3.1 with a zero-bias gap spacing of 50 nm versus the entered Q-factor yields the plot in Figure 3.29. As expected, the displacement increases with decreasing internal loss, approaching infinity for infinite Q-factor. (In reality, the displacement is limited by the pull-in voltage of the device and by nonlinear material behavior at high strains.) Using this plot, the results from previously discussed simulations could, in principle, be scaled to account for the actual Q of the disk in the contour-mode.

The loss of any resonating element is dependent on a number of factors which can be generally divided into three main categories: fundamental losses common to even perfect materials (i.e. materials with perfect crystal lattices with no other inherent loss mechanisms); intrinsic losses related to material imperfections; and losses due to coupling to the external environment [84]. The contributions of all of these loss mechanisms can be related to the total Q-factor through the following equation

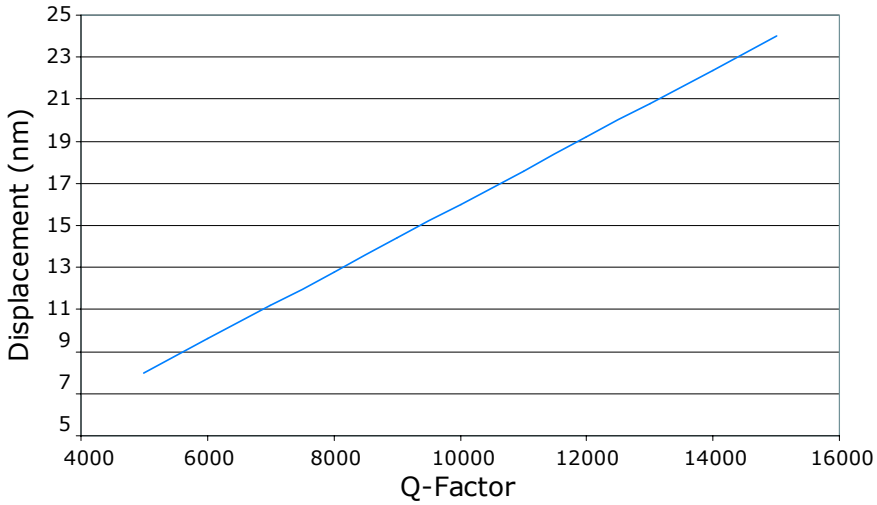


Figure 3.29: Displacement of simple Si disk versus assumed Q-factor.

(after [85]):

$$\frac{1}{Q_{total}} = \sum_i \frac{1}{Q_i} = \frac{1}{Q_{fundamental}} + \frac{1}{Q_{internal}} + \frac{1}{Q_{external}}. \tag{3.33}$$

According to Equation 3.33, the overall Q-factor of the resonator is limited by the lowest Q component. Isolating the most significant component can aid in designing an optimum high-Q resonator. The following subsections focus on each of the loss mechanisms included in Equation 3.33.

3.4.1 Fundamental Losses

Fundamental dissipation mechanisms exist that are common to all vibrating materials, even physically 'perfect' materials. For non-metals, these mechanisms are generally limited to thermoelastic damping and phonon-phonon interaction [84].

Thermoelastic Damping

For certain modes of vibration, e.g. flexural and longitudinal modes, there are sections in the resonating structure that are undergoing compression while there are others undergoing extension at the same instant in time. The simplest example of this is the

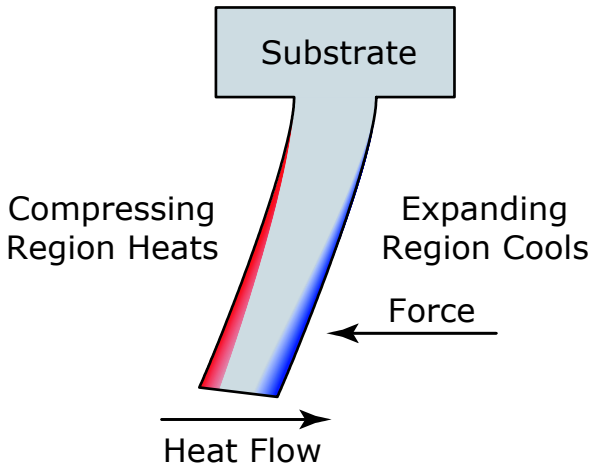


Figure 3.30: Thermoelastic heat flow in a cantilever beam for the fundamental in-plane bending mode.

cantilever beam in a flexural bending mode as shown in Figure 3.30. In this mode, one edge of the beam will compress while the opposite edge will expand while the beam is bending. Volumes that are in expansion will cool down at a rate proportional to their volumetric thermal expansion coefficient. Likewise, volumes in compression will heat up. The adjacent regions of higher and lower temperature in the flexural beam will form a thermal gradient across which heat flow will occur. This heat flow is an irreversible process and represents loss in the resonator system.

The disk resonator fundamental contour-mode vibration, on the other hand, is an example of a transverse mode, i.e. there are no localized volume changes in the solid that will result in the formation of a thermal gradient since the entire disk is either in expansion or contraction at a given moment in time. Transverse modes do not suffer appreciable loss due to thermoelastic damping and this effect can generally be ignored in the disk resonators [86].

Phonon-Phonon Interaction

Periodic oscillation of the crystal lattice of the resonator establishes a time-dependent modulation of the local lattice constant. This modulation perturbs thermally distributed phonons out of the equilibrium state. Local phonon-phonon scattering events restore the system equilibrium with the cost of heat dissipation [87]. This mechanism

is known as the Akhiezer effect, and the Q-factor due to this effect can be calculated from [84]:

$$\frac{1}{Q_{fundamental}} \approx \frac{1}{Q_{ph\cdot ph}} = \frac{CT\gamma^2}{\rho v_s^2}\frac{\omega\tau_{ph}}{1+(\omega\tau_{ph})^2}, \tag{3.34}$$

where C is the heat capacity of the material, T is the temperature, γ is an empirically derived constant, ρ is the material density, v_s is the speed of sound in the material, and τ_{ph} is the relaxation time constant of the phonons which is related to the thermal coefficient of expansion, κ, by:

$$\kappa = \frac{1}{3}Cv_D^2\tau_{ph}, \tag{3.35}$$

where v_D is the Debye sound velocity given by:

$$\frac{3}{v_D^3} = \frac{1}{v_l^3} + \frac{2}{v_t^3}, \tag{3.36}$$

where v_l and v_t are the longitudinal and transverse sound wave velocities respectively. Assuming <100> Si and taking γ to be 2 [88], the Q-factor for single-crystal due to phonon-phonon interaction at the contour-mode frequency is approximately 2×10^6. Given such a high value Q-factor value, it can be safely assumed that this particular mechanism does not set the lower limit on the Q-factor of the contour-mode resonator. The negligible contributions of both phonon-phonon scattering and thermoelastic damping are another reason that single-crystal Si resonators operating in the contour-mode are attractive candidates for very high-Q on-chip resonators.

3.4.2 Internal Losses

The majority of internal friction mechanisms can generally be considered to be relaxation processes associated with transitions of lattice atoms in and out of the equilibrium state. Several relaxation mechanisms exist for crystalline materials such as: relaxation of interstitial defects back to equilibrium; atom dislocation relaxation; and stress relaxation along interfaces of crystal grains [84]. Of these, the most important potential sources of loss in SCSi is defect relaxation of implanted doping ions and stress relaxation at the exposed resonator/gap interface.

As discussed earlier, Si substrates for VLSI applications are typically highly doped (to increase immunity to latch-up) which introduces a high density of point-defects in

the Si lattice. It might be expected that high doping levels would have a detrimental effect on resonator Q, however, empirical results show that Q-factor is unaffected by doping levels sufficient to lower the substrate resistivity to 0.02 $\Omega \cdot$ cm [89] (recall that the doping level in the top Si layer used in the resonators for this work is sufficient to lower the resistivity to approximately 18 $\Omega \cdot$ cm). On the other hand, resonator Q-factors have shown a stronger dependence on the relaxation of the interface atoms. This is due to the fact that RIE step that defines the vertical edges of the disk damages the Si lattice through the introduction of dislocations and point defects (Figure 1.21, Step 7). Yasumura, *et al.* describe the loss due to the damaged surface area as [85]:

$$\Delta W_s = \pi \int_V E_u^S \varepsilon_m^2(r) dV, \tag{3.37}$$

where ΔW_s is the energy lost per cycle due to surface effects, E_u^S is the unrelaxed Young's modulus related to the surface effects, $\varepsilon_m(r)$ is the strain on the surface. By growing a thermal oxide on these surfaces such that the damaged lattice is filled-in by the oxide layer, Q-factors can be doubled compared to those of unprotected resonator structures [89]. Obviously, this effect is depends on the amount of resonator area that is damaged in the RIE process; however, since the edges of the disk are the surfaces that experience the highest stress, it is postulated that this particular loss mechanism will have a significant impact on the overall Q-factor of disk resonators.

3.4.3 External Vibrational Energy Coupling

External energy loss can be described as the coupling of vibrational energy into the surrounding environment. The surrounding environment is considered to include the medium in which the resonator vibrates, the substrate, and any materials deposited on the resonator. Three common mechanisms for this coupling in the disk resonator are viscous gas damping, loss attributed to surface metal layers (such as those discussed in Section 3.3.3), and coupling of vibrational energy to the substrate through anchor supports.

Viscous Damping

Viscous gas damping involves the interaction between the resonator and the medium in which it resonates. Since this medium is most commonly air, it can be expected that the air pressure surrounding the resonator is the dominating factor in determining the amount of viscous energy loss. Indeed, viscous damping can be split into three pressure-related regimes as shown in Figure 3.31: intrinsic, molecular, and viscous regimes [90]. It should be noted here that the data plotted in Figure 3.31 is the normalized Q-factor given by $Q_{intrinisc} \cdot (length/thickness)^2$, where length and thickness are dimensions of a cantilever beam. For a first approximation of the effect on disk resonators, the length variable could be replaced by the disk diameter. At pressures above approximately 100 Pa (750 mTorr), the resonator operates in the viscous regime and the Q-factor is proportional to $1/\sqrt{P}$ where P is the pressure of the system. In this region, sources of damping include Stokes-type damping on the surfaces of the disk parallel to the substrate and squeeze-film damping between the edge of the disk and the electrode [91]. Q-factors of typical resonators in this regime can be three orders of magnitude lower than the intrinsic Q-factor of the device. For this reason, resonators are typically operated in a vacuum environment in which the pressure is far less than 100 Pa. Between 1-100 Pa, the resonator operates in the molecular damping regime, a regime characterized by an inverse dependence of Q-factor on P. Below 1 Pa (7.5 mTorr), the pressure of the surrounding environment is considered to be in the intrinsic regime and the loss due to damping can be typically neglected relative to other losses.

In order to maximize the Q-factor related to the viscous gas damping, resonators are frequently sealed in hermetic packaging structures that can provide a constant vacuum on the order of a few mTorr [92] such that the disk will operate exclusively in the intrinsic region. The requirement of on-chip vacuum packaging is one of the major obstacles to MEMS device integration. However, Abdelmoneum, *et al.* argue that the high energy of the radial contour vibrational mode significantly lowers the impact of viscous damping for the disk resonator and that the Q-factor should remain nearly constant regardless of the pressure of the surrounding environment [93]. Therefore, contour-mode disk resonators are prime candidates for low-cost integration of high-Q resonating components on-chip.

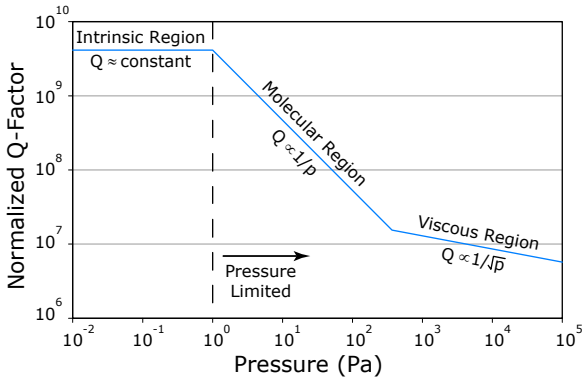


Figure 3.31: Normalized Q-factor for cantilever beams ($= Q \cdot (length/thickness)^2$) versus pressure (after [90]).

Metal Layer Damping

Since metals have more internal friction than Si, any addition of metal to the surfaces of a Si resonator is will tend to degrade the Q-factor. Experimental results for a paddle-shaped resonator have shown a linear dependence of the resonator loss on the thickness of an aluminum layer evaporated on the surface of the device [94]. The Q-factor of such a structure was halved by surface layers as thin as 30 nm. The following expression relates the Q-factor due to the metal losses to the change in Q-factors between an uncoated resonator and a coated resonator [95]:

$$\frac{1}{Q_{metal}} = \frac{G_{\mathrm{Si}} t_{\mathrm{Si}}}{3 G_{metal} t_{metal}} \frac{1}{\Delta Q_{measured}}, \tag{3.38}$$

where G_x and t_x are the shear modulus and thickness, respectively, of the different material layers. The main source of damping in polycrystalline evaporated metal films is the relaxation of macroscopic line imperfections in the crystal lattice [88].

Since metal layers significantly degrade the Q-factor and lower the frequency of vibration, fabrication of high-frequency low-loss resonators should be avoid the deposition of such layers. One alternative is to use doped polysilicon instead of single-crystal silicon for the resonator material as shown in Figure 1.20. Since doped polysilicon is more conductive than intrinsic silicon and can be deposited using standard processing techniques, the need for conducting metal layers is circumvented in this design. However, polysilicon has a somewhat lower Q-factor compared to SCSi. A second

option for the SOI process would be to construct the electrodes and disk in separate lithography steps so that the disk and electrode could be coated with two different metals. The electrode metal (e.g. Au) should be immune to the HF wet etch, while the disk metal (e.g. Al) should be susceptible to etching by HF. In this scenario, only the electrodes are coated in metal after the HF step. This should increase the Q-factor of the resonator while maintaining a high conductivity path from the electrode to the gap edge.

Anchor Losses

Vibrational energy is coupled to the substrate (which can be considered to be an energy sink) through the resonator support structures (anchors). The amount of loss through the anchors is proportional to how efficiently the energy in the device is transferred to the substrate. For the contour-mode disks being considered in this work, there are three anchors: the two lateral DC bias lines and the central post. Losses can be considered minimal for anchors located at points in the resonator that exhibit low vibrational energies [89]. Therefore, the loss through the center post is minimized due to the zero displacement at the central nodal point for contour-mode vibration. The DC bias anchors, on the other hand, are located at the disk edge, the area of highest vibrational energy.

To examine the possible effects of these anchors on the Q-factor of the resonator, assume that the DC bias lines can be generalized as cantilever beams with their nodal point connected to the substrate and their free end connected to the disk. Also assume that the beams are considered part of the resonating structure and energy coupled to the beam itself is not considered loss. The Q-factor of loss coupled to the substrate can be calculated from [96]:

$$Q_n^{-1} = \frac{T_n}{n\pi}, \tag{3.39}$$

where T_n is the energy transmission coefficient from the mode n of the cantilever at the mode resonance frequency in the vibrational modes of the substrate. Out of the four possible modes of vibration for the cantilever – compressional, torsional, in-plane bending, and flexural bending – the mode with the least transmission of energy into the substrate is the in-plane bending mode [96]. The Q-factor for this

type of vibration is proportional to $(L/b)^3$, where L is the length of the beam and b is the beam width in the plane of motion. As expected, the Q-factor is inversely proportional to the cross-sectional area at the interface of the beam and substrate. The ANSYS results shown in Figure 3.14 for the disk supported on the edges by the DC bias lines reveal that the vibration of the DC bias line is indeed experiencing in-plane bending and that the Q-factor degradation due to these DC bias lines should be minimized with this design. Obviously, the loss will still be higher than if the DC bias could be applied at the central-nodal point; however, the design presented here should provide a maximum Q-factor given the planar SOI process used in this work.

3.5 Summary

By reducing the resonating disk into an infinitesimally small ring of mass, m_{eq}, and spring constant, k_{eq}, a reduced-order model for the resonator consisting of a mass element, an equivalent spring, and a dashpot damper can be formulated. Equating the mechanical impedance of this model with the electrical impedance of a series RLC circuit leads to an equivalent RLC model for the disk. This model is dependent upon the actuating/testing method used to measure the device (one-port versus two-port). The two models differ in how the gaps between the electrode and disk are modeled.

Since certain second-order effects can not be modeled with the aforementioned electrical lumped element models, FEA was performed using ANSYS to provide a more representative disk model. This model showed excellent correlation with Equations 1.20 and 1.21 for expected center frequency versus disk radius, and that the disk thickness did not have a significant effect on the center frequency. ANSYS results also showed that varying the diameter of the center post has a quadratic effect on the center frequency of a 20 μm diameter disk without dramatic effects on displacement or current for post radii less than 6 μm. DC bias lines added to the disk edge did not significantly affect the frequency response of the disk but did have some effect on the displacement and output current of the disk. Metal layers added to the disk surface dramatically lower the resonant frequency and displacement of the disk. Unfortunately, these layers are necessary to provide a conductive path along the electrodes to the disk edge; however, a two-step lithography process could be implemented to metallize only the electrodes and leave the disk uncoated. Au layers caused a more

significant decrease in frequency when compared to Cr; however, the displacement was higher for the Au-coated disk.

Effects on disk performance through variation of the transducer parameters were also studied in ANSYS. Disk edge displacement has a linear relationship with the DC bias while the current has a quadratic relation with DC bias up until a critical voltage at which the vibrating edge comes into contact with the electrode. This "pull-in" voltage has a quadratic relation with the gap spacing meaning that much higher currents can be achieved at high bias voltages for wide gap spacings. However, such bias voltages are impractical for on-chip designs, thus a primary design motivation should be to lower the gap-spacing so as to achieve the highest amount of current for the available bias supply. The contour-mode center frequency shows an inverse relation to increasing DC bias; however, the available tuning range is only $\sim$0.2%. Finally, the displacement and current have linear relations with the AC voltage applied to the excitation electrode according to the ANSYS simulations.

A comparison of the one-port and two-port testing methods was also performed in ANSYS. As expected, the current due to the static capacitance, C_o, is reduced with the two-port setup at the expense of lowering the peak resonant current. The two-port setup also introduces a spurious, "push-pull" mode that is close to the fundamental contour-mode in frequency and could affect the selectivity of filters based on the two-port device configuration.

An examination of the possible origins of the loss in the contour-mode disk resonator yielded two mechanisms in particular that will most likely have the largest effect on device Q-factor. The first is the surface loss attributed to RIE damage of the vertical sidewalls of the disk as well as the deposited metal layers on the surface of the disk. The second is the anchor loss through the DC bias lines to the DC bias supply bondpad. The DC bias lines can be designed to mitigate the effects of the anchor loss; however, the surface losses are an inherent result of the process chosen to fabricate the disks and will likely dominate the final Q-factor of the measured devices.

Chapter 4

Single-Crystal Silicon Disk Resonator Fabrication

This chapter focuses on the fabrication process used to construct the single-crystal silicon contour-mode disk resonator designs presented in this work. The fabrication process was initially developed at Virginia Tech in [39] and adopted here for the fabrication of the disk resonator geometry. Each of the processing steps outlined briefly in Chapter 1 are discussed in further detail in this chapter. In addition, an electroless copper deposition process is introduced as an alternative method to metal evaporation for increasing the capacitance of the transducer gaps and the conductivity of the electrodes.

4.1 SOI Wafer

The SOI wafer used as the substrate for this work (Figure 4.1) consists of a 340 nm thick top "device" layer of highly p-doped Si, a 400 nm thick intermediate layer of SiO_2, and a 500 μm thick bottom "handle" layer of intrinsic Si. The SOI wafer is created through a process known as bond-and-etchback SOI (BESOI). In this process, two separate Si wafers are coated with a thin thermal oxide layer. The two wafers are then aligned so that the oxide layers are in contact with one another. A high-temperature bonding step fuses the two wafers at the oxide/oxide interface. The top silicon layer is then etched back using a wet etch step until the final desired

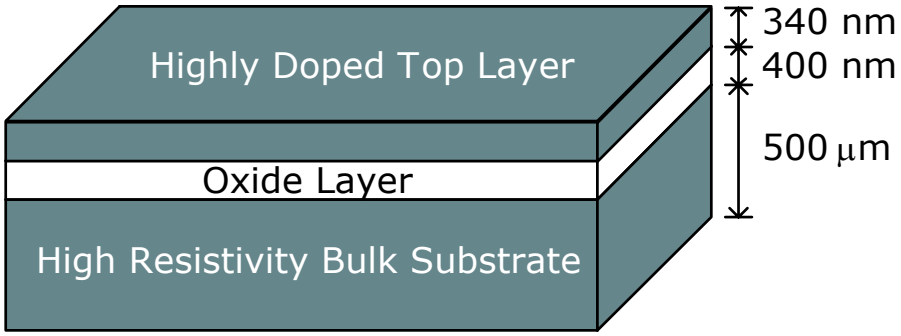


Figure 4.1: SOI wafer with layer dimensions.

device layer thickness is reached. To prepare the 4" SOI wafers for subsequent resonator fabrication steps, they are cleaved into quarter sections using a diamond-tipped scribe. This avoids sacrificing entire wafers during the process development stages of this work.

4.2 PMMA Resist Deposition

The pattern-transfer resist used in this work is the polymer polymethylmethacrylate (PMMA). PMMA is a positive electron-beam sensitive polymer, i.e. incident beams of electrons will result in the breaking of polymer chains in the resist. Once these polymer chains are broken, particular solvents will remove the broken chains while leaving the intact chains on the substrate. Therefore, areas of resist subjected to e-beam radiation will be removed, exposing the underlying Si. This process is the foundation of the electron-beam lithography technique used in this work.

As with most resists, PMMA is spin coated onto the wafer. The thickness of the deposited resist is a function of the viscosity of the resist, the speed at which the wafer is spun, and the amount of resist initially transferred to the surface of the wafer. As will be discussed later, the thickness of the resist has a significant impact on the subsequent processing steps. With thick resists, thicker layers of metal can be deposited and lifted off reliably. On the other hand, thinner resists offer greater lithographic resolution. Since the thin gap spacings required to maximize the motional current of the resonator, thin layers of resist were used to maximize resolution.

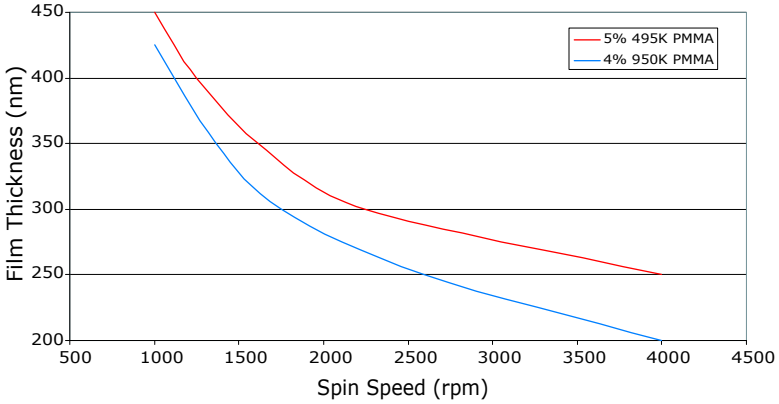


Figure 4.2: Film thickness versus spin-speed for 4% 950K PMMA and for 5% 495K PMMA (after [97]).

PMMA is specified according to the solvent in which it is dissolved, the polymer-to-solvent concentration, and the polymer molecular weight (MW). The solvent chosen for this work is anisole, which is safer to users than the alternative chlorobenzene. The concentration of the resist determines the viscosity and thus the film thickness versus spin speed curve for the resist. Weaker concentrations are less viscous and will result in thinner layers for a given spin speed. The MW determines the rate at which exposed resist will be removed by the developer. Generally, the lower the MW, the more quickly the developer reacts with the broken chains.

Figure 4.2 shows the relationship between spin speed and PMMA film thickness for the two types of resist used in this work: 5% 495K MW PMMA dissolved in anisole and 4% 950K MW PMMA dissolved in anisole. These resists are used to achieve a bilayer resist profile with a layer of 950K PMMA spun on top of a 495K layer. The bilayer profile is conducive to improved metal liftoff, which will be described shortly. The different concentrations of the two resists allows a thicker layer of the more sensitive 495K layer to be spun for the same speed as the 950K layer.

To prepare the sample surface for PMMA deposition, a simple cleaning of the surface with alternating rinses of acetone and isopropyl alcohol (IPA)[1] followed by a spin-dry at high speed is required. After the surface is cleaned, approximately 0.75 ml of 5%

[1] An IPA rinse should always follow an acetone rinse since acetone is a strong solvent for PMMA and any acetone residue will inhibit adhesion of the PMMA to the Si surface. In any case, the wafer should be spun dry for at least 30 seconds after the final rinse step.

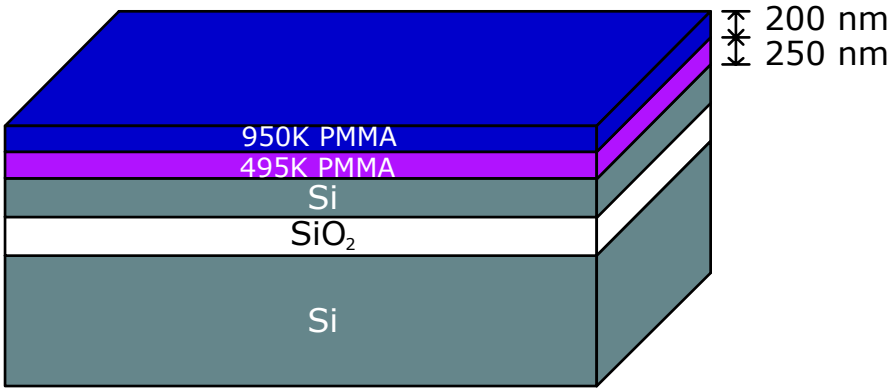


Figure 4.3: Bi-layer PMMA resist profile.

495K PMMA is dropped onto the center of the quarter wafer and the spin program is initiated. The program consists of two steps: (1) a 10 s ramp-up to an intermediate speed of 100 rpm that spreads the resist over the entire surface of the wafer; and (2) a fast acceleration step to the final spin speed of 4000 rpm, which is then maintained for 1 min, that thins the resist to the desired thickness. After 1 min, this program should result in a 250 nm layer of resist. The wafer is then hard baked at 180 °C for 90 s and then allowed to cool for 2 min. A second layer of 950K PMMA is then spun over the top of the first layer with the same program, resulting in a 200 nm layer of resist, for a total of 450 nm for the two layers. The final resist structure on the sample is shown in Figure 4.3. To prepare for lithography, the quarter wafer is then further diced into 1 cm× 1 cm squares. As many as 8 individual disk resonator structures can be defined on each square, enabling numerous processing trials from a single quarter wafer.

4.3 Electron Beam Lithography

It has been stated previously that the contour-mode disk resonator does not require a submicron radius to attain high-frequency oscillation. However, the modeling efforts described in Chapter 3 indicate that the gap spacing between the electrode and the disk *must* be of submicron dimension in order to maximize the current flow and to minimize the series motional resistance. In fact, this dimension must be as small as possible (while avoiding pull-in) to provide a measurable current at the bias

voltage levels that are available on chip. State-of-the-art photolithography systems employing deep- and sub-UV or x-ray wavelengths can provide 90 nm resolution, but the added cost of mask manufacturing renders this method prohibitively costly for the prototype designs discussed in this work. An alternative method to conventional photolithography that can provide sub-10 nm resolution [98] without the need for photolithography masks is electron-beam lithography (EBL).

Non-commercial EBL systems such as the one used to create the disk resonators in this work typically include a personal computer-based computer-aided design (CAD) system and a digital-to-analog converter (DAC) that are connected to a standard scanning electron microscope (SEM). A simplified schematic of an SEM-based EBL system is shown in Figure 4.4. An SEM, such as the LEO 1550 used in this work, consists of an electrode emission source, an accelerating anode, various lenses to focus the beam, stigmators to shape the beam, an aperture to control the beam width, and scan coils to control the position of the electron beam after it leaves the aperture. Most SEMs are operated as imaging systems, in that the beam of electrons is raster-scanned over a portion of the substrate (in much the same way that the electron beam of a CRT television is swept across the screen) and the reflected electrons are collected to form an image of the scanned sample. EBL systems simply take control of the SEM scan coils via an external DAC and steer the electron beam in the pattern of the desired structure. Therefore, no mask set is needed in EBL which can significantly reduce the cost of the fabrication of prototype samples. However, since the direct-write exposure of an entire wafer would take far longer (days) than the flash exposure of photolithography (seconds), EBL systems have not taken hold as production lithography systems.

The CAD and SEM control system used in this work is the Nabity Pattern Generation System (NPGS) [40]. The DAC used in this system can control the position of the beam spot at the rate of 5 MHz. Patterns in NPGS are transferred to the resist as a matrix of closely separated dots. To create each dot, the DAC applies a voltage between +10 V and -10 V to the scan coils to move the beam to the first location of the pattern to be exposed. The beam sits at the spot for a period of time proportional to the desired energy dosage at that location. After exposing the first dot, the beam is moved to the second, and so on, until the pattern is fully exposed. If the exposure times are long enough, i.e. the dosages are high enough, the dots will blend together to

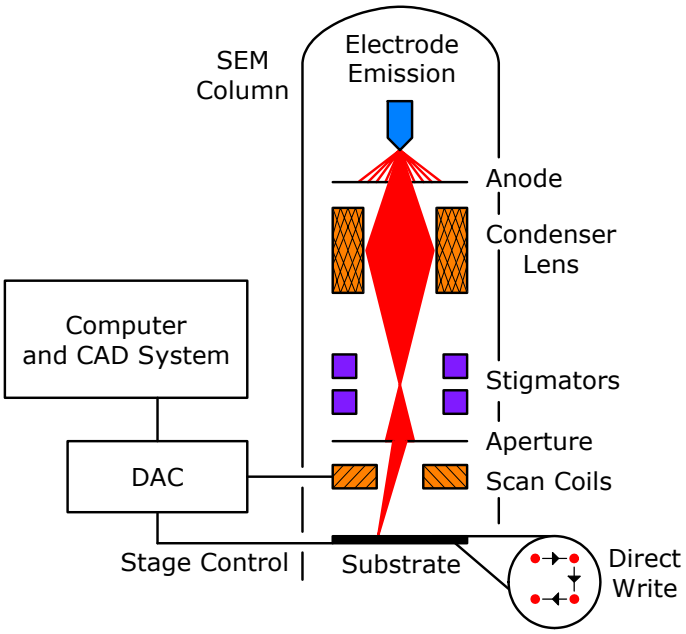


Figure 4.4: Simplified schematic of an SEM-based EBL system.

create a contiguous region in the resist corresponding to patterns in the CAD drawing. Ideally, the electrons will affect the chemical structure of the PMMA only where the beam spot is incident and a perfect image is transferred from the computer to the resist. In reality many factors control the resolution and quality of EBL-generated patterns such as accelerating voltage at the anode, focus, stigmation, resist thickness, and proximity effect.

4.3.1 EBL Resolution

The major advantage to using EBL systems for submicron pattern generation is the exceptionally short wavelength of the electron at high accelerating voltages. The wavelength of the electron can be approximated as:

$$\lambda_e \approx \frac{1.23\,\mathrm{nm}}{\sqrt{V}}, \tag{4.1}$$

where V is the accelerating voltage. Using the maximum voltage for the LEO 1550 SEM of 30 kV, the wavelength of the electron is approximately 7 pm, several orders

of magnitude smaller than the shortest UV wavelength currently used in optical lithography. The diffraction-limited resolution of the system is related to the wavelength through Abbe's equation:

$$r \propto \frac{\lambda_e}{n \sin \alpha}, \tag{4.2}$$

where r is the smallest resolvable dimension, n is the index of refraction of the medium (1.00 for a vacuum), and α is the half angle of the condenser lens or aperture, whichever is smaller. For EBL systems the lenses typically have a very small α of about $1\,^{\circ}$; however, the smallest resolvable dimension is still an exceptionally low value of about 0.4 nm. This theoretical limit of resolution is sufficient for creating the submicron gap spacings required for resonator operation. However, the practical resolution limit is set by operator-influenced parameters such as the beam focus, astigmatism, and pattern design.

4.3.2 Focus and Astigmatism

The focus of the SEM, along with the aperture size, determines the size of the beam spot incident with the sample surface. The better the focus, the smaller the beam spot and the finer the resolution of the EBL. The focus can be optimized by controlling the current through the electromagnetic lenses in the SEM column. Prior to the exposure of the PMMA-coated samples, the focus is refined by imaging a sputtered-gold ultra-high resolution standard at high magnification. Located on the standard are gold particles ranging in size from 1 nm to 50 nm which can be used to focus the beam at magnifications as high as 500,000 X. Since most patterns for this work were written at about 2000 X, focus of this quality is more than sufficient to guarantee high resolution.

Unfortunately, practical electromagnetic lenses used to focus the electron beam inherently contain some defects and aberrations that result in a distortion of the beam shape from a perfect circle to an oval shape. Optical systems normally do not suffer such astigmatism issues since glass can be made into near perfect lenses. However, e-beam systems are especially sensitive to astigmatism and this can be one of the most difficult problems to correct for successful EBL. Oval shaped electron beams can lead to an uneven distribution of the electron energy on the resist. Astigmatism can be seen in the high-resolution standard as elongation of the normally spherical Au

particles into oval shapes. By adjusting the stigmators (Figure 4.4) the aberrations of the lenses can be compensated for and the astigmatism corrected. Only when the focus and astigmatism are correctly set will the resolution of the system be optimized.

4.3.3 Proximity Effect

As incident electrons strike the surface of the resist, some of their energy is spent in breaking the bonds of the resist that facilitate subsequent development. As the electrons break the bonds of the resist, secondary electrons can be generated that can travel through the resist, breaking additional nearby bonds. Also, electrons will scatter and "fan-out" as they encounter molecules in the resist widening the area that is affected by the electrons beyond the spot directly defined by the beam. Furthermore, electrons can backscatter off of the Si substrate and assume a trajectory that takes them back through the resist layer. These secondary exposure events contribute to what is known as the *proximity effect* which can widen and blur the developed pattern in the resist. Figure 4.5 shows the mechanisms responsible for proximity effect and the consequences of this effect on closely-spaced exposure locations.

Proximity effect can be minimized by increasing the accelerating voltage, decreasing the resist thickness [100], and decreasing the beam-spot diameter [101]. Figure 4.6 shows effects of accelerating voltage and resist thickness on the energy density in the resist surrounding the beam. Increasing the accelerating voltage has the effect of greatly reducing the contribution of backscattered electrons. This is due to the fact that the electrons will reflect off of the substrate at higher angles, thus reducing the energy density in areas close to the beam spot. Reducing the resist thickness, on the other hand, has the effect of reducing the forward scattering of the incident beam. To maximize disk resolution, a thin resist layer should be used in conjunction with the highest available accelerating voltage.

4.3.4 CAD Design

Figure 4.7 shows the CAD drawings for the resonating disk, the bias lines, the excitation electrodes, and the bondpads along with typical exposure dosages used for each structure. The critical dosage for complete PMMA exposure using the development

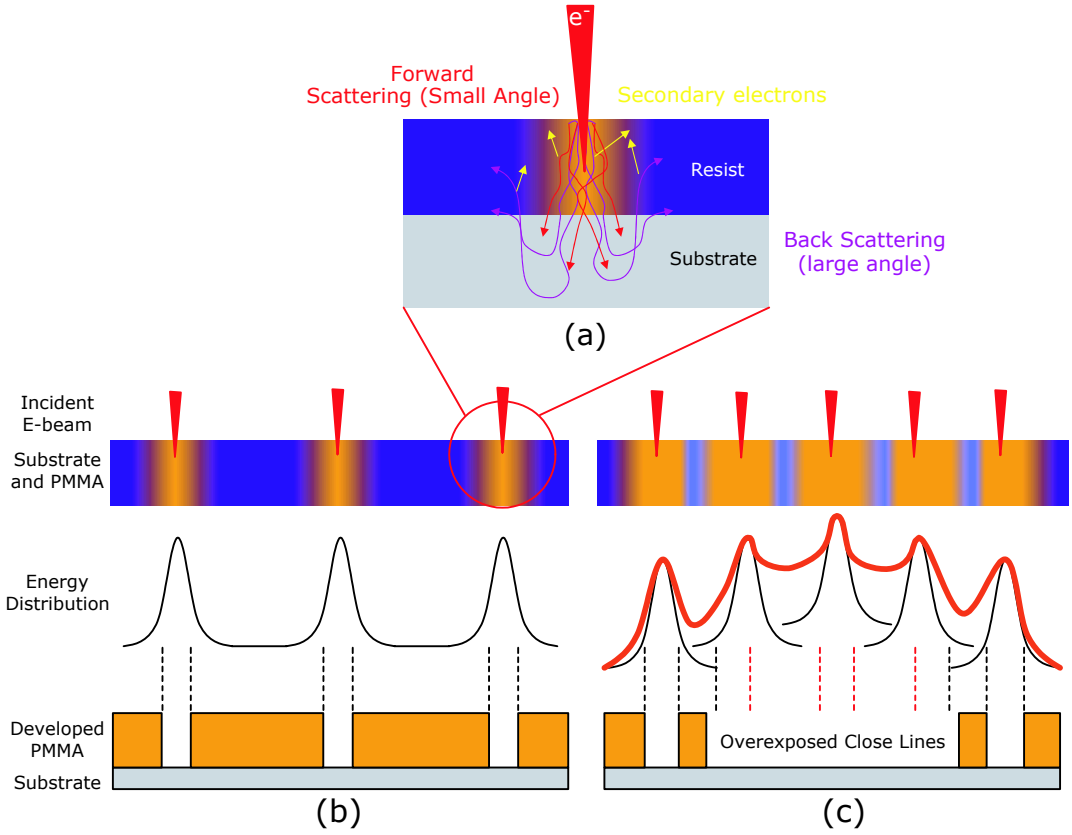


Figure 4.5: Proximity effect in EBL: (a) sources of proximity effect; (b) relatively benign effect for widely-spaced lines; (c) overexposure in closely-spaced lines (after [99]).

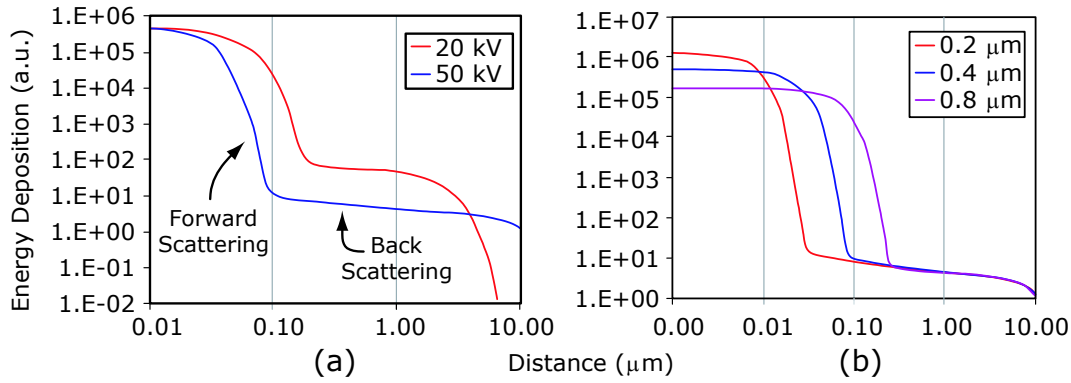


Figure 4.6: Energy density versus distance from beam axis for: (a) varying accelerating voltages for 0.4 μm thick PMMA; and (b) varying PMMA resist thicknesses for 50 kV accelerating voltage (after [100]).

process described in the next section is approximately 300 $\mu C/cm^2$ [102]. Most of the pattern areas were given less than the critical dose to compensate for the proximity effect exposure. Doses higher than those listed in Figure 4.7 results in a gap spacing that would be overexposed near the top center and the bottom center of the disk. By lowering the doses, the gap spacing will be closer to the dimensions defined in the CAD program. However, at the left and right edges of the disk, where there is no electrode coverage, there is less of a proximity effect. To compensate for the lower electron energy in this area, the extra higher-dosage arcs were added (indicated in yellow).

The pattern elements are exposed in the following order: (1) large bondpads; (2) top electrode; (3) DC bias connections and disk from left to right; and finally (4) the bottom electrode. Ordering of the elements is critical during the exposure step since the SEM used for this work did not have a beam blanker that could turn off the beam between pattern elements. Extra care must be taken to ensure that the beam does not inadvertently cross over the gap spacing creating a short between the electrode and the disk. Dump points (the white asterisks located in the top electrode and the left-hand DC bias anchor) are used to position the beam before exposure of those elements and ensure that the beam does not cross over the gap.

After pattern exposure, there is little visible change in the appearance of the resist. However, a very slight color change from light pink to a darker shade can be seen under the correct lighting conditions. Figure 4.8 exaggerates this color difference and outlines the cross section of the disk and electrodes as it would appear in the resist. To complete the pattern transfer into the resist film, a development step is required.

4.3.5 Pattern Development

To develop the exposed pattern for subsequent metallization, the sample is immersed in a 1:3 methyl isobutyl ketone (MIBK) and IPA solution for 70 s with slight agitation. This particular solution has offers exceptional resolution over those with higher concentrations of MIBK; however, the sensitivity is low, i.e. it requires more e-beam dosage to fully develop the pattern. Since resolution is of paramount concern during the fabrication of the resonator, the 1:3 solution was chosen for development. Figure 4.9 shows the result of development on the conceptual cross-section wafer.

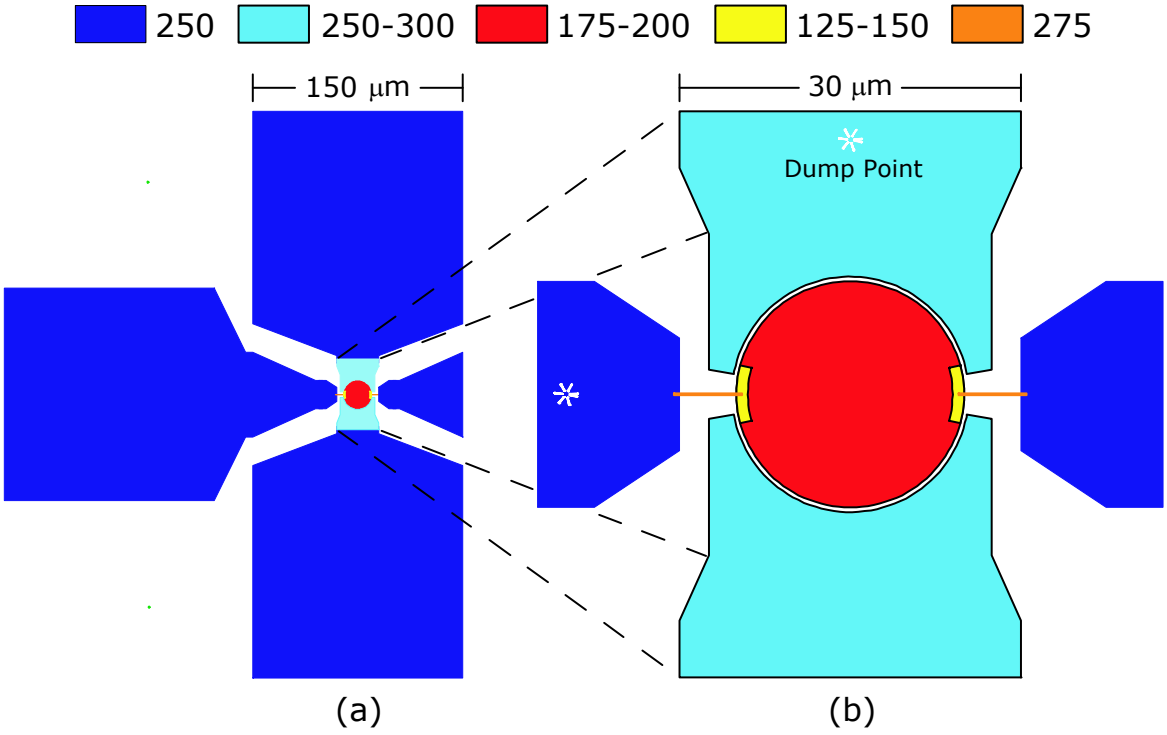


Figure 4.7: CAD drawings of disk resonator: (a) complete structure including bonding pads; (b) blow-up of disk resonator and electrodes (dosages given in legend are in $\mu C/cm^2$).

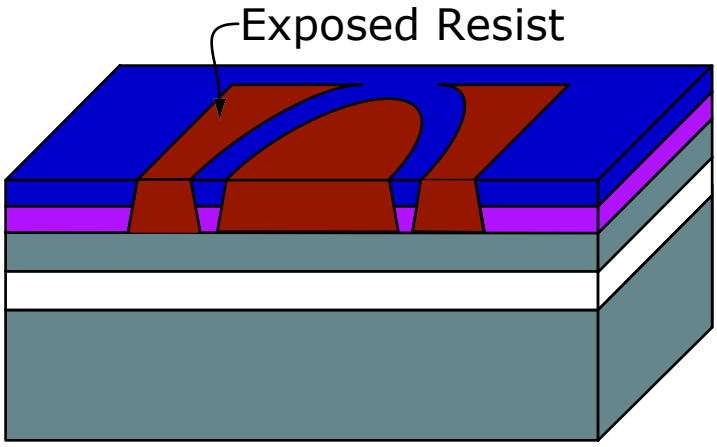


Figure 4.8: Resist film after exposure.

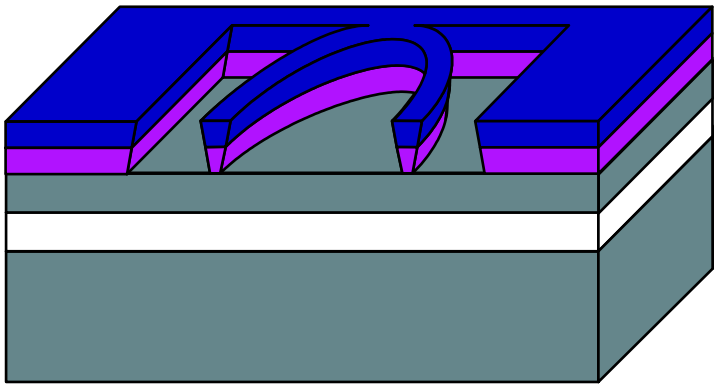


Figure 4.9: Resist film after exposure and development.

Since the lower 495K MW resist is removed more quickly than the 950K resist, the resist sidewalls are sloped slightly. This reentrant profile facilitates liftoff after metal evaporation.

Figure 4.10 shows an SEM micrograph of the disk and electrodes after development. A slight resist residue is left at the intersection of the DC bias lines and the disk edge. As described earlier, this is due to the smaller proximity effect in these areas and the extra higher dose arcs in the CAD design were subsequently added to eliminate this residual resist. Additionally, a short oxygen plasma descum of the sample can be used to clean the surface of residual resist.

4.4 Metallization

Metallization of the resonator (shown in Figure 4.11) is required to provide: (1) a metal mask for subsequent reactive ion etching of the Si device layer and (2) a more conductive path for signals applied to the electrodes. Transfer of the metallized pattern to the Si surface involves two steps: (1) evaporation of a metal layer and (2) liftoff of the remaining, unexposed resist.

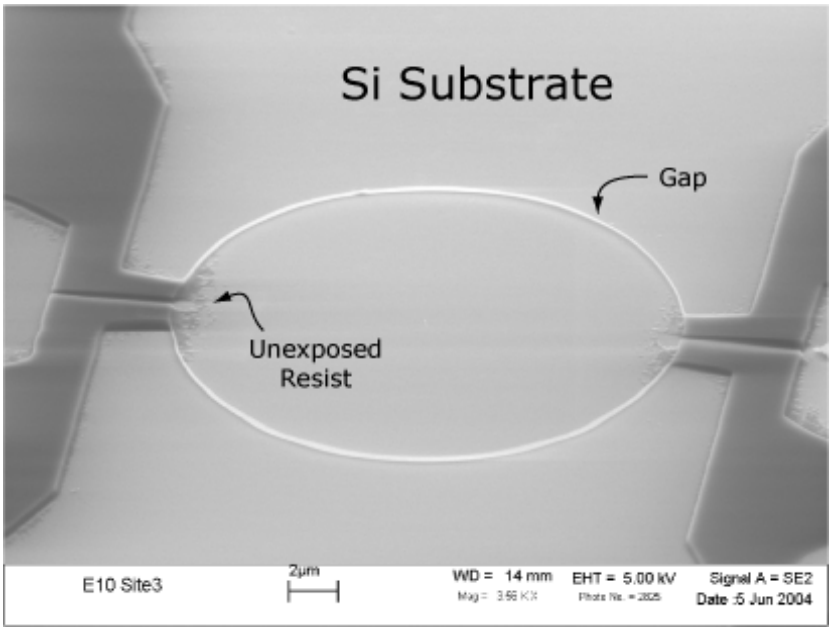


Figure 4.10: SEM micrograph of developed electrodes and disk.

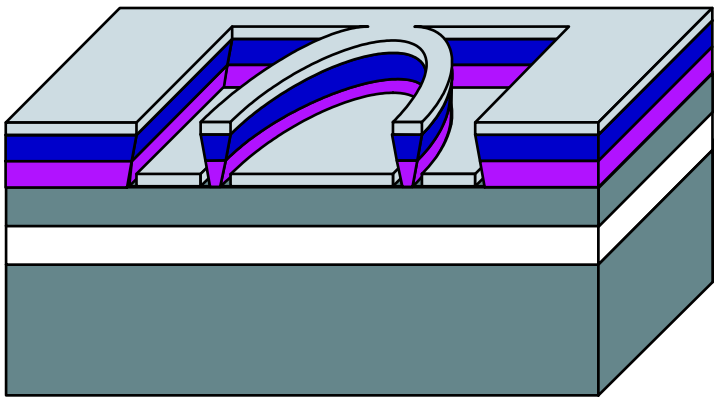


Figure 4.11: Substrate and resist film after metallization.

4.4.1 Evaporation

Evaporation of the metal films used in this work was performed using electron-beam physical vapor deposition (EBPVD). Electron beam excitation is an efficient method for creating localized temperatures in excess of 3500 °C in a metal source, hot enough to boil most metals at low vacuum. To generate the electron beam, 3 kW of DC power is fed to a tungsten filament. The current will cause the filament to glow and emit a steady stream of electrons by thermionic emission[2]. The emitted electrons are steered via a large permanent magnet into a water-cooled carbon crucible containing the target metal evaporant. The beam spot is approximately 3 mm in diameter and provides an energy density of 25 kW/cm^2. The incident electrons super-heat the metal within the beam spot, causing the metal to evaporate. The evaporated metal travels upward in the evaporation chamber in a spherical wavefront, condensing on any cool surfaces such as the chamber walls and the sample to be metallized. The sample is placed approximately 25 cm away from the crucible to ensure a uniform metal coating and to minimize heat damage from the filament. A thickness-monitoring crystal is positioned close to the sample to measure the rate of condensing material and total thickness.

Like all PVD systems, the e-beam evaporator must be operated at low chamber vacuum for numerous reasons. First, the low vacuum minimizes the ambient particles that can interfere with the line-of-sight transport of the evaporant to the substrate. As shown in Figure 4.11, PVD is a directional deposition technique, i.e. only those surfaces perpendicular to the evaporant wavefront are coated. Evaporant particles in a poor vacuum environment can collide with ambient particles, changing their trajectory so that some metal is deposited on the side walls of the resist. Any coating of the sidewalls will have a detrimental effect on subsequent liftoff processing. Second, any amount of oxygen present in the system can rapidly oxidize metals at these temperatures, significantly reducing the film quality. Third, the low vacuum decreases the boiling points of the metals, thus requiring lower temperatures for evaporation. Finally, the high voltages required for EBPVD could result in ionization of the atmosphere in the chamber if not under vacuum, shorting the power to the chamber walls. The Thermionics 3kW multi-pocket e-beam gun used in this work

[2]Tungsten is used as the filament material since it has the highest melting point of all elemental metals and can thus withstand the extreme temperatures.

Metal	Boiling Point @ 1e-6 Torr	DC Current Required	Evaporation Rate	Notes
Al	1100 K	< 100 mA	5 nm/s	Evaporates quickly at low power
Au	1250 K	225 mA	8 nm/s	Sweep coils used to accelerate evaporation
Cr	1300 K	125 mA	3.5 nm/s	Sublimates, high stress film
Ti	1650 K	250 mA	5 nm/s	Low thermal conductivity, use sweep coils

Table 4.1: Evaporation characteristics for various metals.

has 5 possible crucible locations so that as many as five metals can be evaporated onto the substrate without breaking the chamber vacuum. This setup is advantageous when depositing metals such as Au that require an intermediate layer of either Cr or Ti for deposition onto a Si surface.

Table 4.1 shows evaporation characteristics for four common processing metals: Al, Au, Cr, and Ti. As mentioned earlier, Cr and Au were chosen for the resonator metal layers due to their relative immunity to the HF wet-etch step compared to Al and Ti. Cr thin films exhibit high internal stresses that increase with thickness [103]. For this reason, the maximum thickness for Cr films is about 10-15 nm to prevent cracks and fissures from arising in the film.

For most sample runs, a Cr film was used as an intermediate layer between the Si and a subsequent Au deposition. Since Au deposits at a relatively high e-beam current value, steps must be taken to ensure that the excessive heat generated does not melt the resist on the substrate. The best method to reduce the heat load on the resist is to lower the total deposition time. This is done by sweeping the beam spot over the surface of the metal in a raster-scan pattern. By increasing the area of the metal source heated by the beam, the deposition rate can be approximately tripled thus lowering the amount of time that the substrate is subjected to excessive temperatures.

For other sample runs, the evaporation was stopped with the Cr film to facilitate a subsequent copper deposition through an electroless plating process to be described in Section 4.6. In either case, the remaining undeveloped resist must be removed before further processing. Since this resist is covered by a metal layer, the removal process is called "metal liftoff" and is described in the next subsection.

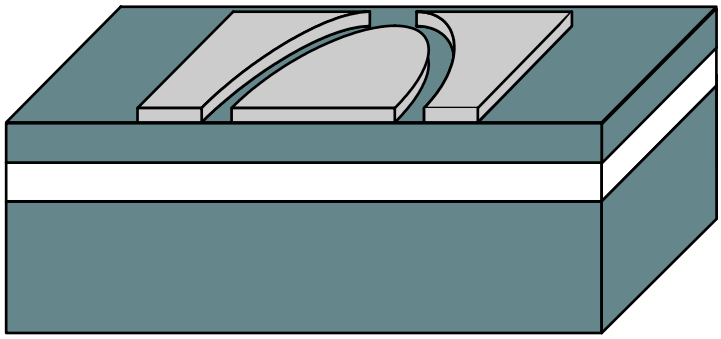


Figure 4.12: Substrate and metal pattern after liftoff.

4.4.2 Liftoff

To remove the remaining unexposed resist, the sample is immersed in a 1:1 solution of acetone and dichloromethane, both strong solvents for PMMA. The liftoff solution is then agitated in an ultrasonic bath (i.e. sonicated) to aid in the removal of the resist in tight areas such as the gap spacing. The reentrant profile of the resist allows the solvent solution to better remove the resist layer from around the desired metal patterns. The liftoff process typically takes between 1 and 2 min, and visual inspection of the sample surface is normally a sufficient indicator of when the majority of the resist has been removed. After the liftoff is complete, the samples are rinsed in an IPA bath followed by a deionized (DI) water bath to remove solvent residue, and then air dried with compressed N_2. Care must be taken to avoid damaging the metal mask with excessive N_2 pressure. Figure 4.12 shows the patterned surface of the SOI sample after liftoff.

Figure 4.13 shows the unsuccessful liftoff of a sub-100 nm gap resonator structure. The small dimensions of the gap permitted the evaporated metal to completely envelop the resist in the gap, inhibiting liftoff. The result is a "tunnel" of leftover Au and Cr over the area where the resist has been dissolved by the liftoff solution. This was a common problem when using relatively thick Au depositions on sub-100 nm gaps. The metal thickness in this micrograph is approximately 125 nm total. The easiest remedy for this is to increase the gap spacing or decrease the metal thickness, both of which will decrease the disk-electrode capacitance and decrease the current.

Figure 4.14 shows successful liftoff for an gap spacing of $\sim$150 nm and a 15 nm-thick

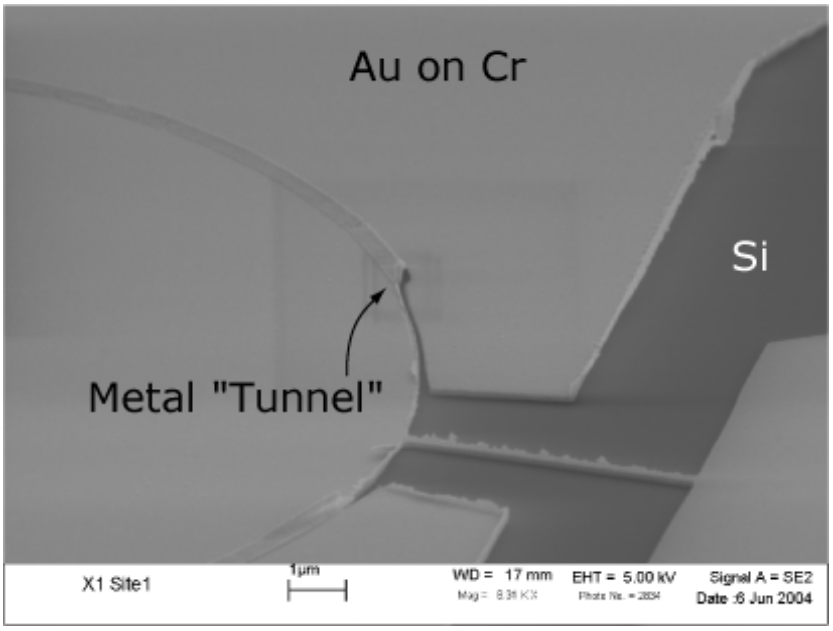


Figure 4.13: Unsuccessful liftoff showing leftover metal bridging the gap spacing.

metal mask of Cr. The SEM micrograph was taken with the sample at a slight angle to show the thickness of the Cr. Cr-only masks typically exhibit far better liftoff than Au and Cr masks; however, as was already mentioned, Cr can only be deposited in very thin films due to the high intrinsic internal stress of the evaporated metal.

4.5 Etching

The ultimate goal of the fabrication process is to transfer the pattern of the resonator into the Si device layer and to release the disk so that it is free to vibrate (Figure 4.15). The final two steps to complete the fabrication process are as follows: (1) a reactive ion etch (RIE) etches the area of the Si device layer that is unprotected by the metal mask; and a (2) timed HF wet etch which dissolves most of the underlying oxide layer.

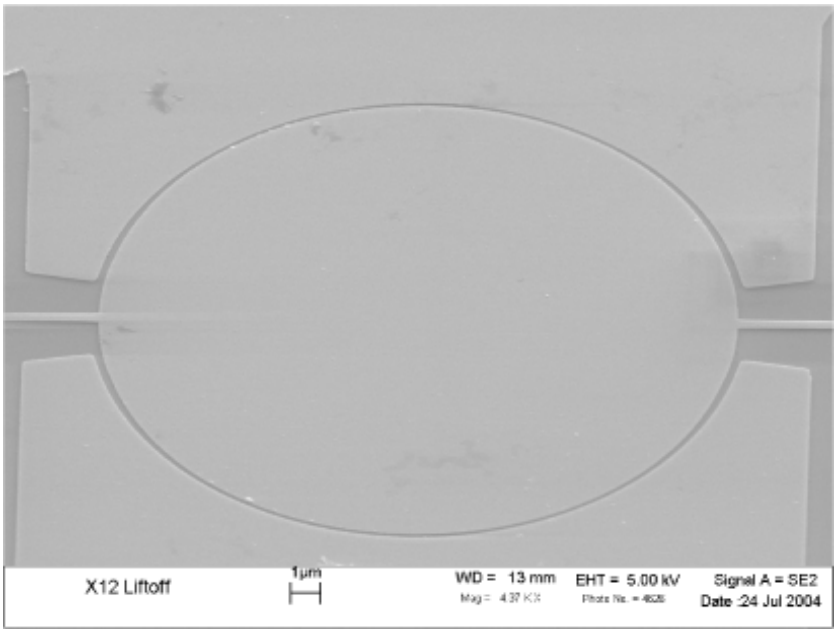


Figure 4.14: SEM micrograph of a sample with successful liftoff of a 15 nm-thick Cr metal mask.

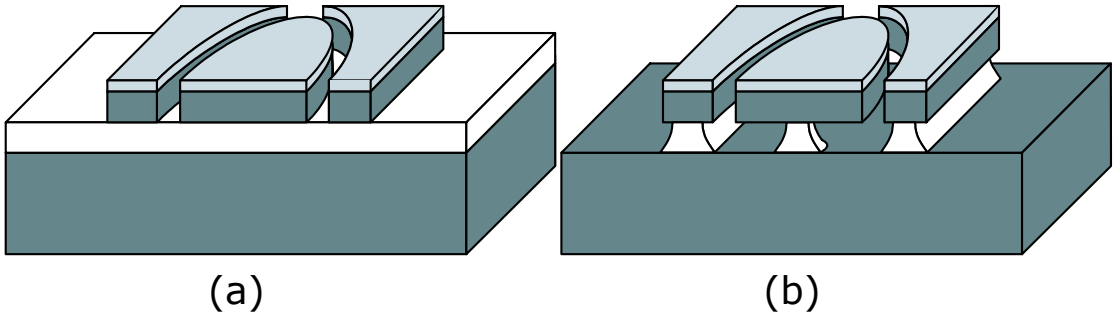


Figure 4.15: Final etching and release of a disk resonator: (a) RIE etch of device layer; (b) HF release etch of oxide layer.

4.5.1 Reactive Ion Etching

RIE is also known as a plasma-assisted dry etch, i.e. the etching process is initiated by a plasma ignited in an gas that is chemically reactive with the substrate. A standard RIE chamber consists of a vacuum pump to remove ambient particles, a negatively-charged plate on which the substrate is positioned, and an etchant gas inlet port situated opposite of and perpendicular to the substrate. An RF source tuned to 13.56 MHz and capable of suppling 150 W of RF power is also connected to the vacuum chamber. When an etchant gas is introduced into the chamber via the inlet port, and RF power is applied, a plasma is ignited around the substrate. The constituents of the plasma vary from gas to gas; however, they can generally be subdivided into three active species: electrically charged ions; reactive free radicals; and nonreactive or passivating radicals [104]. Positively charged ions will be accelerated towards the substrate due to the attraction of the negatively charged plate beneath it. Ions that strike the sample will cause atoms on the surface to be dislodged from the lattice and ejected, causing physical etching of the surface. Reactive free radicals, on the other hand, will bond with the substrate and remove atoms via a chemical process. Nonreactive radicals tend to accumulate on all surfaces of the reactor, passivating them and preventing further interaction with ions and reactive species. Figure 4.16 shows these processes for two common Si etch gases, tetrafluoromethane (CF_4) and trifluoromethane (CHF_3).

For each plasma type there is a characteristic recombination event, dependent on the fluorine to carbon atom (F/C) ratio, that determines the nature of the etch chemistry. In the case of CF_4, the F/C ratio is 4 which leads to a large population of free F atoms in the plasma gas. Any CF_x free radicals are quickly consumed by F atoms to reform CF_4. Therefore ionic bombardment and free F atoms dominate the etch characteristics of the CF_4 plasma [Figure 4.16(a)] [104]. As stated earlier, the ions will dislodge Si from the surface due to their high incident energy. If the ions encounter an ambient particle, their trajectory will be altered such that the ion will strike the vertical sidewall of the Si, resulting in a more isotropic etch profile. However, for low vacuums, ion bombardment can generally be considered an anisotropic (in the vertical direction only) etch process. Since free F atoms, on the other hand, are not affected by the electric field, they will chemically attack all exposed Si surfaces, forming silicon tetrafluoride (SiF_4). The SiF_4 then deabsorbs

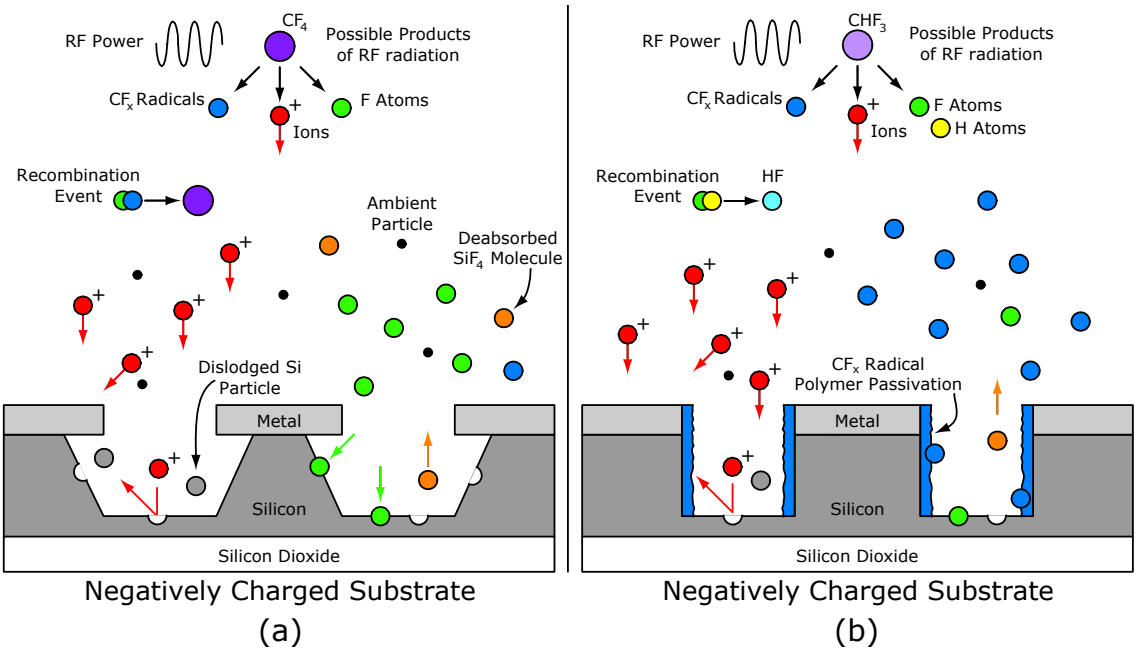


Figure 4.16: RIE reactions at Si surface for two common etch gases: (a) CF_4; (b) CHF_3

from the surface resulting in further isotropic etching. Since the isotropic etching tends to widen the gap near the metal/Si interface, this type of etch chemistry is not ideal for the resonator structures.

An alternative etch chemistry that relies more on physical ion etching than chemical etching is a CHF_3 etch. Due to the high reactivity of the H atom, the free H and F atoms products of the CHF_3 plasma recombine to form hydrofluoric acid (HF). The effective F/C ratio is then reduced to 2, allowing for more CF_x radicals in the plasma. Most of the free fluorine atoms then combine with carbon to form CF_x radicals, leaving positively-charged ions as the only active species that will cause etching of the Si. Since CF_x radicals are not reactive with Si, they simply build-up on all surfaces of the Si and the metal layer [Figure 4.16(b)]. The composition of the resulting fluorocarbon (FC) polymer depends on the RF power used to generate the plasma and, for the low powers used in this work, the dominant radicals are CF and C-CF_x radicals where x ranges from 1 to 3 [105]. The FC passivation protects the sidewalls from further ion damage and chemical etching from stray F atoms. The FC passivation that builds up on the flat surfaces of the Si, on the other hand, is removed by the incident ions, allowing for vertical etching of the Si. The polymer

on the sidewalls can be removed by a subsequent O_2 plasma etch since oxygen atoms are reactive with the FC film, but not with the Si surface.

Since the etch process relies almost completely on ion bombardment, the etch rate is relatively slow. This is compounded by the fact that passivation only occurs for lower power levels. At low power levels, there is a decreased amount of ion generation due to the high activation energy of ion species [104]. For this reason, CHF_3 is more often used as an etchant for SiO_2 since the HF by-product is highly chemically active towards the oxide. In fact the selectivity of CHF_3 for SiO_2 over Si is approximately 10:1, therefore CHF_3 etches performed on the SOI samples invariably penetrate into the oxide layer after the Si device layer has been removed. This is normally not a concern for the resonators designed in this work since the oxide layer is later removed. It should be noted here that the Cr etch mask is quite stable under the CHF_3 etch and even thin (15 nm) Cr layers remain intact after etching of the entire 340 nm-thick Si device layer [106].

Figure 4.17 shows the result of a 14 min CHF_3 etch of the SOI sample at an RF power of 50 W. The dump point shown to the right of the bottom electrode is a location where the SEM beam paused during the lithography while refocusing between exposure of the bonding pads and the disk. Figure 4.18 is a close-up of the same resonator structure near a DC bias line connection that shows two side effects of the CHF_3 etch. The first effect is the aforementioned penetration into the underlying SiO_2 layer due to the plasma-generated HF chemical etch. The boundary between the two layers of the SOI wafer can be seen as the light-to-dark transition underneath the electrode and DC bias line. The second effect is the creation of what is known as "RIE grass" on the exposed oxide surfaces. It is postulated that this is formed by the sputtering of Cr due to ion bombardment and subsequent redeposition onto the surface. The redeposited Cr particles then block further chemical etching of the SiO_2 layer resulting in unetched pillars or "grass". This is supported by the fact that there is very little grass in areas of the oxide far from the resonator, i.e. areas are not adjacent to metal mask layers. The sputtering theory is also supported by the existence of a relatively "grass-free" area next to the DC anchor pad. The slightly peeled-back edge of Cr on the surface of the anchor may block Cr particles that are sputtered off of the surface in that area.

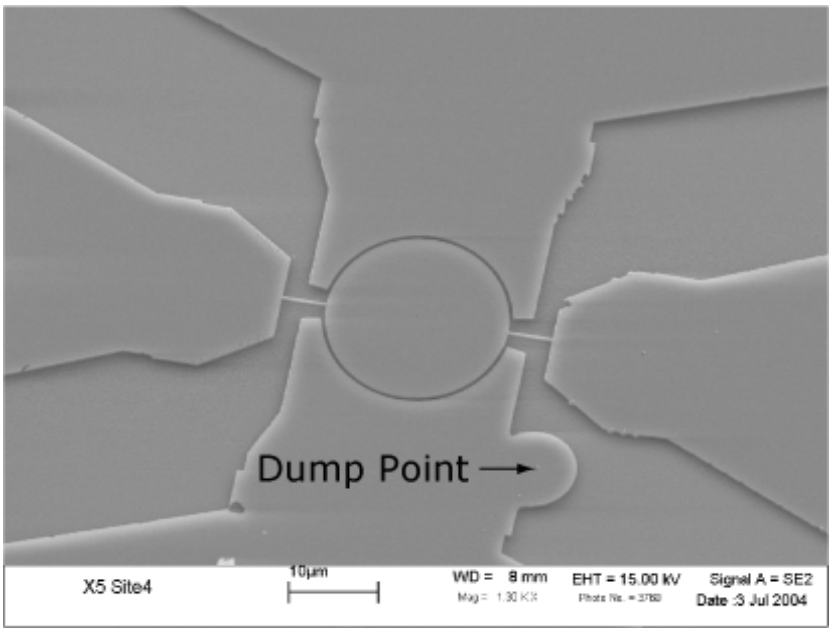


Figure 4.17: Overhead SEM micrograph of disk and electrodes taken after a 14 min CHF_3 etch.

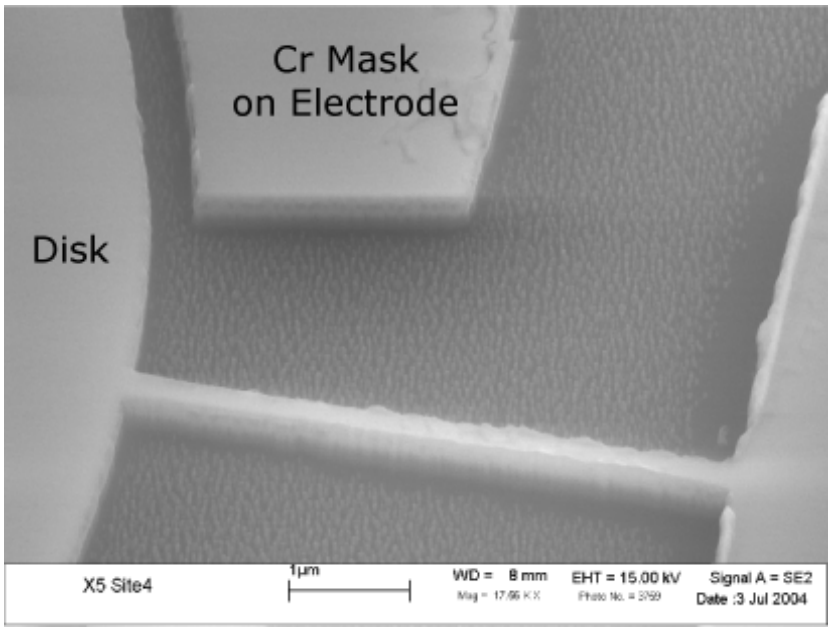


Figure 4.18: Closeup of the post-RIE resonator structure near DC bias line.

4.5.2 HF Release

After dry etching, the sample is immersed in an oxide-selective wet etch that releases the majority of the disk with the exception of the central post. The wet etch solution chosen to release the disk is a buffered oxide etch (BOE) consisting of a 10:1 solution of 40% ammonium fluoride (NH_4F) and 49% HF acid. HF consumes SiO_2 according to the following reaction:

$$6HF + Si\,O_2 \rightarrow H_2 + Si\,F_6 + 2H_2O \tag{4.3}$$

The ammonium fluoride is present to replenish spent fluoride ions and to increase the pH. Using BOE also significantly reduces the health hazards associated with unbuffered HF acid. The SiO_2 etch rate of 10:1 BOE is approximately 60 nm/ min. At this rate, it takes $\sim$2.5 h to etch inward under the disk edge towards the center and leave a 1 μm central post. Sonication or agitation is used to free hydrogen bubbles from the surface of the SiO_2. Without agitation the bubbles coalesce in the gap spacing and prevent circulation of fresh reactive fluoride ions to the oxide surface preventing the etch from continuing in the gap area. It was originally thought that the small gap spacing would inhibit release of the disk due to the close proximity of the electrode and disk. However, with sufficient agitation this did not seem to be an issue. Figure 4.19 shows a partially released disk and electrode (the DC bias lines were not included in this design to aid in SEM characterization). Figure 4.20 shows a partially released disk focusing on the released DC bias lines.

4.6 Electroless Copper Plating

The steps described above provide a platform for fabricating released surface micromachined disk resonators. However, there are several shortcomings with respect to the gap spacing that could be addressed through the addition of a second metallization step after the disk etch step. Figure 4.21 provides a cross-section comparison of the disk fabrication process employed by Clark, *et al.*, the SOI process described to this point, and an SOI process that includes the addition of an electroless copper deposition step. The bottom-up approach used by Clark, *et al.* allows the thickness of the disk, and thus the gap capacitance, to be arbitrarily large (within the limits of

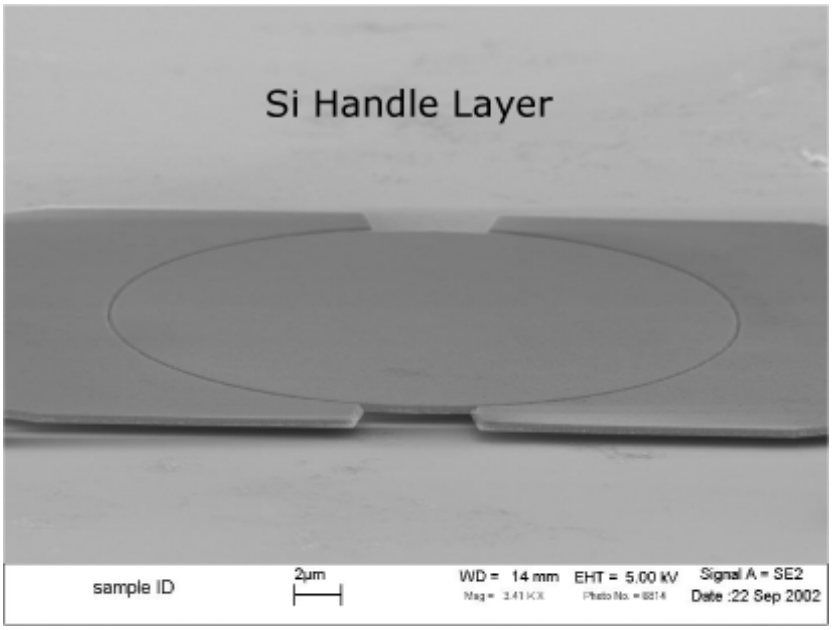


Figure 4.19: SEM micrograph of partially released disk (without DC bias lines or pads).

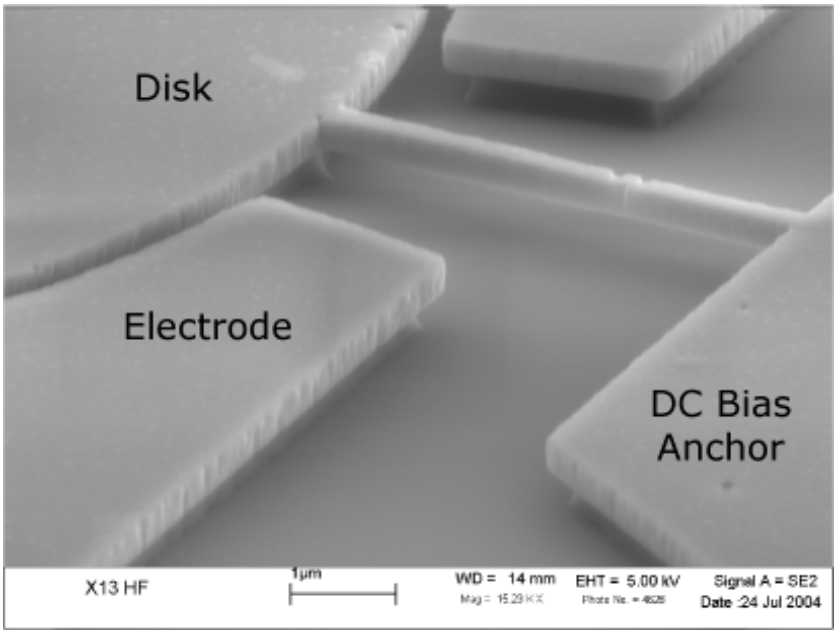


Figure 4.20: SEM micrograph of partially released disk focusing on the released DC bias lines.

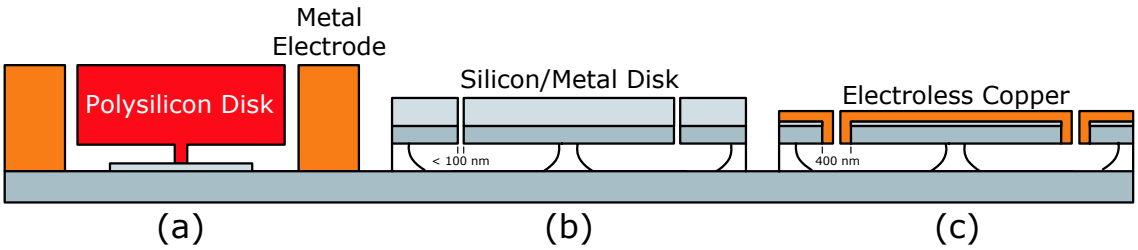


Figure 4.21: Cross-section comparison of three disk fabrication methods: (a) Nguyen bottom-up fabrication method [36]; (b) SOI process derived from [39]; (c) SOI process with addition of electroless copper deposition.

the polysilicon deposition process). In the SOI process, on the other hand, the thickness of the disk is defined by the SOI device layer thickness, the gap spacing and top metal thickness are the only variables that can be modified to increase the gap capacitance. Unfortunately, small gap spacings can suffer from have lithography-related issues such as proximity effect overexposure and poor liftoff. Also, the majority of the capacitive force will occur between the metal layers deposited on the disk and the electrode. This will restrict the current flow and disk displacement in comparison to the disk structure of Clark, *et al.*

A possible solution to these issues is the addition of an electroless copper plating step. Electroless deposition is a chemical process that selectively deposits Cu metal onto catalyzed Si surfaces while leaving SiO_2 surfaces uncoated. If this step is performed after the disk etch RIE, when the sidewalls of the disk and electrode are exposed, copper will also be plated in the gap spacing. There are three distinct advantages to metal deposited in the gap spacing. First, the lithographic dimensions of the gap spacing can be initially wider since the final distance between the disk and electrode will be defined by the thickness of the deposited copper. Second, only a thin Cr metal mask is required, thus eliminating the liftoff problems associated with thick Cr/Au films. Third, the electric field will now couple between the entire surface areas of the electrode and disk sidewalls, increasing disk displacement and current flow. This section will describe the electroless copper deposition process and contrast it with standard electroplating processes.

4.6.1 Analytical

Electroplating is a common IC process technique for depositing thick interconnect layers. For example, the high-Q monolithic on-chip inductors in Section 2.2.1 are fabricated in an electroplated copper layer. The process requires a high voltage source, an anode, a cathode (the target substrate), and a bath containing a salt of the metal to be deposited. By immersing the cathode and the anode in the metal salt bath and applying a large potential between the cathode and anode, metal ions will dissociate from the salt and be attracted to the negatively charged substrate. Excess electrons present at the cathode reduce the metal ions to metal atoms and a metal film begins to form on the substrate. Electroplating is used to deposit layers of metals such as copper and nickel at much greater thicknesses than can be achieved through evaporation or sputtering; however, the process requires that the target area for deposition be electrically connected to the cathode. Since the disk and electrodes in the SOI micromachining process are isolated from the substrate by the SiO_2 layer, standard electroplating is not straightforward. For this reason, an electroless method that does not require a conductive path was considered.

Electroless deposition is an electrochemical process, i.e. the excess electrons needed to reduce the metal ions at the substrate surface are provided by the solution, not by an external current source. Fundamentally, the overall chemical reaction of electroless deposition can be summarized as [107]:

$$\mathrm{M}^{z+}_{\mathrm{solution}} + \mathrm{Red}_{\mathrm{solution}} \overset{\text{catalytic surface}}{\rightarrow} \mathrm{M}_{\mathrm{lattice}} + \mathrm{Ox}_{\mathrm{solution}}. \tag{4.4}$$

In this model, the excess electrons required to reduce the metal ion, $\mathrm{M}^{z+}_{\mathrm{solution}}$, to the metal state, $\mathrm{M}_{\mathrm{lattice}}$, are supplied by a reducing agent, $\mathrm{Red}_{\mathrm{solution}}$, present in the same chemical bath. $\mathrm{Ox}_{\mathrm{solution}}$ is a by-product of the reduction reaction. Equation 4.4 must take place at a catalytic site. Therefore the electrochemical process can be split into three separate reactions: catalytic activation of the Si surface [Figure 4.22 (b)-(c)]; and simultaneous cathodic (reduction of metal ions) and anodic (oxidation of the glyoxylic acid reducing agent) reactions at the catalytic site [Figure 4.22 (d)]. Each of these reactions are discussed briefly in the following subsections.

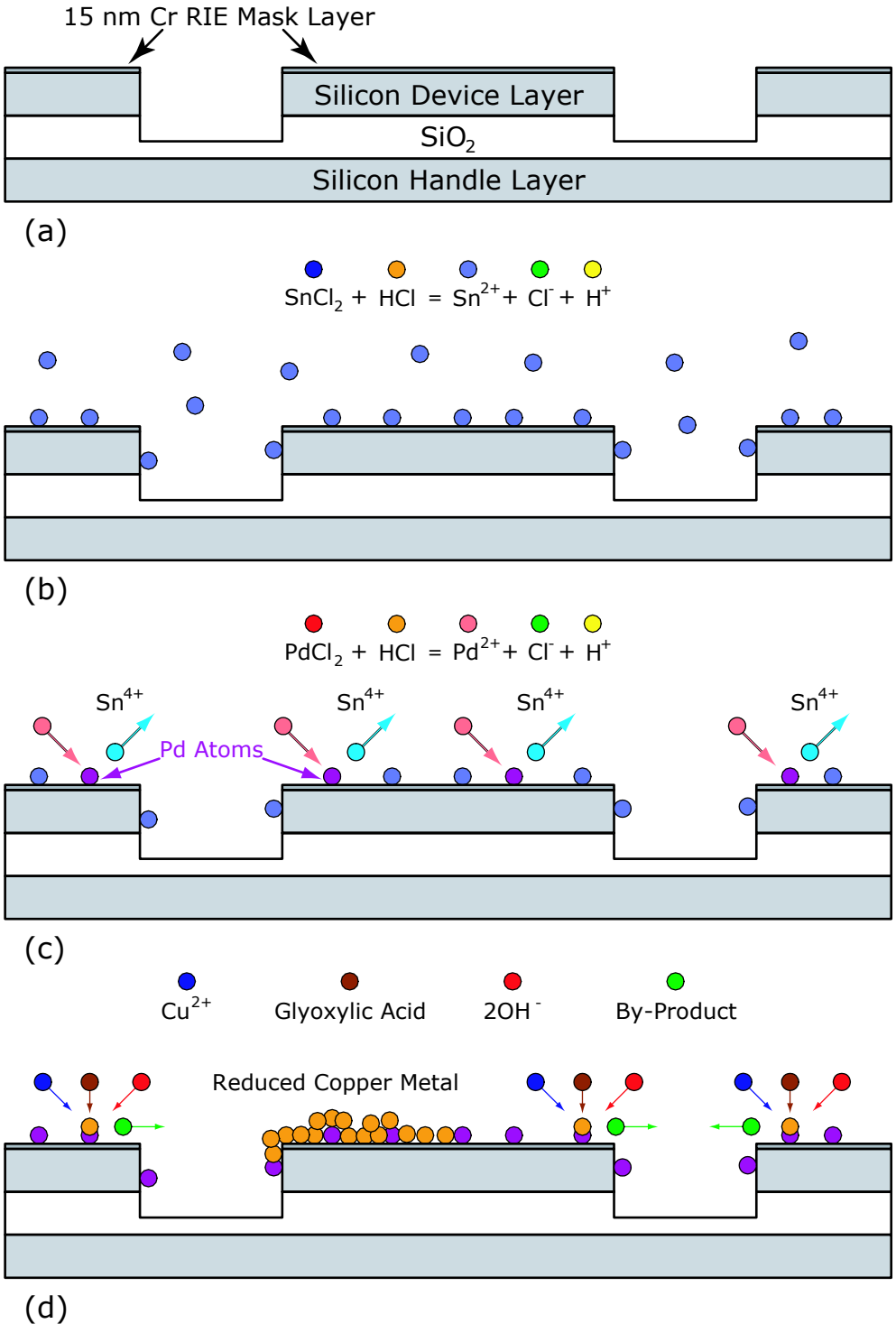


Figure 4.22: Electroless copper deposition process: (a) substrate after RIE; (b) Sn^{2+} sensitization; (c) Pd activation of catalytic sites; (d) simultaneous oxidation of reducing agent and reduction of metal ion.

Catalytic Activation

Electroless copper deposition cannot occur if the metal to be deposited is more noble than the target substrate. Since copper is a fairly noble metal (i.e. nonreactive towards less noble metals), copper will not deposit on most substrates without prior catalytic activation. The most commonly used catalytic metal is palladium due to its rapid initiation of the copper deposition process. To deposit catalytic Pd metal onto the device layer, the surface must first be sensitized by adsorbed ionic tin according to the equation [107]:

$$\text{Surface} + \text{Sn}^{2+}_{\text{solution}} \rightarrow \text{Surface} \cdot \text{Sn}^{2+}_{\text{ads}}. \tag{4.5}$$

The Sn^{2+} are introduced to the surface via a HCl and $SnCl_2$ solution where the HCl is used to disassociate the $SnCl_2$ into its ionic species. After sensitization, the sample is rinsed with DI water and moved to an activation solution.

The activation reaction of the surface with adsorbed Pd metal proceeds according to:

$$\text{Surface} \cdot \text{Sn}^{2+}_{\text{ads}} + \text{Pd}^{2+}_{\text{solution}} \rightarrow \text{Surface} \cdot \text{Pd}_{\text{ads}} + \text{Sn}^{4+}_{\text{solution}}. \tag{4.6}$$

Pd ions are not catalytic to electroless deposition and will rapidly oxidize in the plating solution. Therefore, the Sn ions deposited in the sensitization reaction serve to reduce the free Pd ions to their metallic state on the surface. Pd ions are provided through ionic disassociation of $PdCl_2$ by HCl. The overall catalytic reaction, then, is:

$$\text{Pd}^{2+} + \text{Sn}^{2+} \rightarrow \text{Pd}_{\text{catalytic}} + \text{Sn}^{4+}. \tag{4.7}$$

This process selectively activates Si and metal surfaces over SiO_2 surfaces [108]. Since the SiO_2 must be subsequently removed by the HF wet-etch release step, it is critical that the SiO_2 surfaces remain free of these catalysts so that copper deposition cannot initiate on the oxide surface. The Pd atoms are randomly located on the Si gap sidewalls and on the thin Cr RIE mask layer. After activation, the sample is again rinsed in DI water and immediately moved to the copper plating solution where the simultaneous cathodic and anodic reactions occur at the Pd catalytic locations.

Cathodic Partial Reaction

The cathodic reaction portion of Equation 4.4 can be expressed in two steps [107]: (1) the dissociation of the metal ion from a complexing ligand, L_z,

$$[ML_x]^{z+xp} \rightarrow M^{z+} + xL^p; \tag{4.8}$$

and (2) a reduction of the metal ion to the metal atom,

$$M^{z+} + ze^- \rightarrow M_{\text{lattice}}. \tag{4.9}$$

The complexing ligand introduced in Equation 4.8 serves to prevent the highly reactive metal ions from prematurely reacting with the reducing agent or hydroxide ions away from the Pd catalytic sites. In most electroless copper solutions, the copper ion is provided by copper (II) sulfate pentahydrate salt ($CuSO_4{\cdot}5H_2O$) and the complexing agent is ethylenediaminetetraacetic acid (EDTA). The complexing reaction is then:

$$CuSO_4 \cdot 5H_2O + EDTA^{2-} \rightarrow CuEDTA^{2-}_{\text{ads}} + SO_4^{2-} + 5H_2O. \tag{4.10}$$

Combining Equations 4.8, 4.9, and 4.10 yields the following cathodic partial reaction for copper deposition [109]:

$$CuEDTA^{2-}_{\text{ads}} + 2e^- \rightarrow Cu_{\text{lattice}} + EDTA^{4-}_{\text{ads}}, \tag{4.11}$$

where the electrons, $2e^-$, are supplied by the anodic partial reaction to be described in the next section.

Anodic Partial Reaction

The anodic reaction portion of Equation 4.4 can be expressed as the oxidation of the reducing agent:

$$Red_{\text{solution}} \overset{\text{catalytic surface}}{\rightarrow} Ox_{\text{solution}} + ze^-. \tag{4.12}$$

This reaction requires a catalyst (such as Pd) to initiate dehydrogenation of the reducing agent, thus the need for the Pd activation step. Historically, the most common reducing agent for electroless copper deposition has been formaldehyde

(HCOH) [109, 110]. However, due to the carcinogenic properties of formaldehyde, a safer solution using glyoxylic acid (CHOCOOH) as a reducing agent was used for this work [111, 112]. The anodic partial reaction for glyoxylic acid in the presence of an alkaline solution is as follows [111]:

$$\mathrm{CHOCOOH} + 2\mathrm{OH}^- \rightarrow \mathrm{HC_2O_4^-} + \mathrm{H_2O} + \frac{1}{2}\mathrm{H_2} + e^-, \tag{4.13}$$

where $\mathrm{HC_2O_4^-}$ is a by-product of the oxidation reaction and $\frac{1}{2}\mathrm{H_2}$ is the dehydrogenation product of the Pd catalyst. The creation of $\mathrm{H_2}$ gas bubbles at the substrate surface serves as an *in situ* visual indicator of the success of the electroless deposition process.

Complete Reaction

Combining Equations 4.11 and 4.13 yields the final electroless reaction equation at the catalytic surface:

$$\mathrm{CuEDTA^{2-}_{ads}} + 2\mathrm{CHOCOOH} + 4\mathrm{OH}^- \rightarrow \mathrm{Cu_{lattice}} + 2\mathrm{HC_2O_4^-} + 2\mathrm{H_2O} + \mathrm{H_2} + \mathrm{EDTA^{4-}}. \tag{4.14}$$

The electrons supplied by Equation 4.13 facilitate the reduction of Cu in Equation 4.11, therefore the two reactions must occur simultaneously at the Pd catalytic site. The activation energy of this reaction is fairly high ($\sim$60 kJ/mol) and must be conducted at an elevated temperature. High deposition rates have been reported for temperatures near 50 °C [113]. The solution must also be highly alkaline (pH > 12) to supply the needed hydroxide ions. This is normally done by the addition of potassium hydroxide (KOH) or sodium hydroxide (NaOH).

Thin film copper growth proceeds in three stages: (1) nucleation of seed copper grains at the Pd sites; (2) growth of the copper seeds in favorably oriented crystal grains; and (3) coalescence of growing crystals from different Pd sites. The coalescence of sites forms an encapsulating layer of copper over the surface of the disk and in the gap spacing [Figure 4.22 (d)].

There are two reactions that compete with the principal reaction and contribute to the consumption of the reactants. First is the Cannizzaro reduction of glyoxylic

acid into glycolate and oxalate, two products that do not contribute to electroless deposition, as follows [111]:

$$2\mathrm{CHOCOOH} + 2\mathrm{OH}^- \rightarrow \mathrm{C_2O_4^{2-}} + \mathrm{HOCH_2COOH} + \mathrm{H_2O} \tag{4.15}$$

The Cannizzaro reaction rate for glyoxylic acid is faster than that of formaldehyde; however, the effect can be significantly reduced by using KOH over NaOH as the source of the hydroxide ions. The consumption of glyoxylic acid in this manner has a time scale on the order of a few hours, meaning that electroless copper solutions have short shelf lives.

An additional competing reaction is the formation of cuprous oxide (Cu_2O) from the copper ions. This reaction is accelerated for bath temperatures above 70 °C and electroless depositions above this temperature result in the deposition solution changing from a bright blue color to a dark gray color and the deposition of a red-colored residue on the substrate and solution beaker. Decomposition of the Cu in this manner can render the solution useless for deposition in less than 10 min [113]. This can be avoided by maintaining a bath temperature closer to the optimum 50 °C and by the addition of stabilizing additives such as 2,2'-dipyridyl ($C_{10}H_8N_2$).

4.6.2 Experimental

Table 4.2 shows the solution concentrations of the sensitization, activation, and copper plating solutions. The activation and sensitization solution chemistries are adapted from [114], while the copper plating solution was adopted from [112]. The observed deposition of the electroless copper is approximately 30 nm/min in the first minute and increases to 60 nm/min as the copper sites coalesce on the surface. RE-610 is a proprietary surfactant which consists of a nonionic surfactant (ethoxylated nonyl phenol) associated with an anionic surfactant (phosphate ester). The surfactant serves to reduce the surface tension at the sample/solution interface, resulting in a more uniform copper coating [110].

Figure 4.23 shows the results of 1 min of electroless copper deposition on the sample shown in Figure 4.20. The gap spacing was initially ~600 nm and the copper has grown ~30 nm inward on each side of the gap. Since the copper deposition was

Step	Solution Composition		Immersion Time	Notes
	Chemical	Amount		
Sensitization	$SnCl_2$ HCl (37%)	10 g/L 40 mL/L	30 s - 1 min	Slight agitation, 25°C
Rinse	DI Water		10 -15 s	
Activation	$PdCl_2$ HCl (37%)	0.25 g/L 2.5 mL/L	1 - 2 min	Slight agitation, 25°C
Rinse	DI Water		10 -15 s	
Electroless Copper Deposition	$CuSO_4 \cdot 5H_2O$ EDTA 50% Glyoxylic Acid KOH RE-610 2,2'-dipyridyl	7.5 g/L 10.25 g/L 12.5 mL/L pH 12-13 Trace Trace	Deposition rate is 30-60 nm/min	Slight stirring at 75 rpm, Temperature ranges from 50°C to 70°C
Rinse	DI Water		10 -15 s	Leave to air dry

Table 4.2: Electroless copper deposition solution formulations.

performed after the HF release for this sample, the copper deposits everywhere except on the sidewalls of the SiO_2 layer supporting the electrodes. Since this will result in significant capacitive coupling between the excitation electrodes and the substrate, the copper deposition should be performed after the RIE but before the HF step. It is critical, therefore, to time the RIE so that the etching stops just after the device layer has been completely etched. Since the CHF_3 plasma is more selective for etching oxide over Si, this is sometimes difficult to accomplish with the RIE equipment available at the time this work was completed. Figure 4.24 shows an electroless layer deposited on a disk where the SiO_2 layer remains on the surface of the sample. There is some copper on the SiO_2 surface; however, the coverage is not significant enough to keep the HF step from etching away the oxide. Since no copper will remain on the surface in this sample, increased parasitic capacitance from the electrode to the grounded substrate is avoided.

4.6.3 ANSYS Simulations

As is evident in the atomic force microscope (AFM) micrograph of an electroless copper deposition shown in Figure 4.25(a) [108], electrolessly deposited copper layers

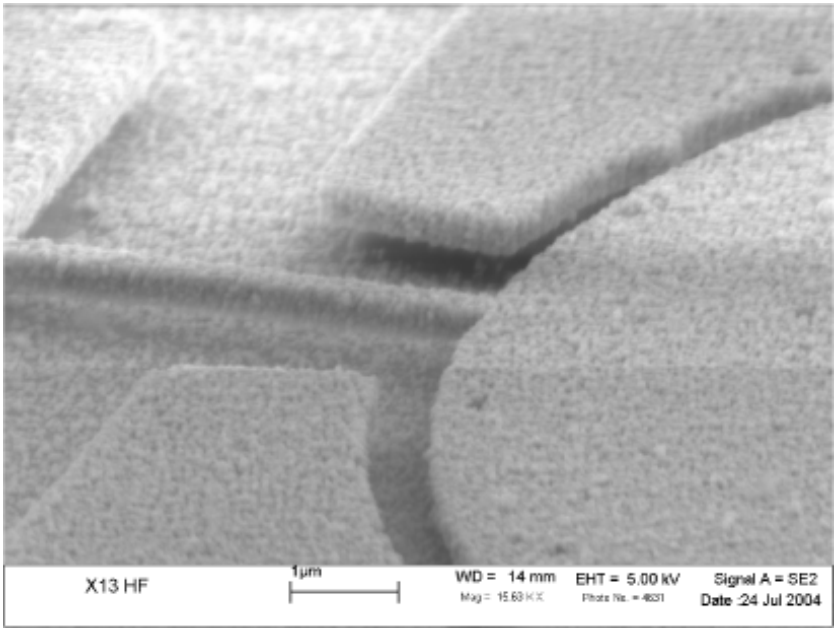


Figure 4.23: SEM micrograph of an electroless copper coated disk and electrode.

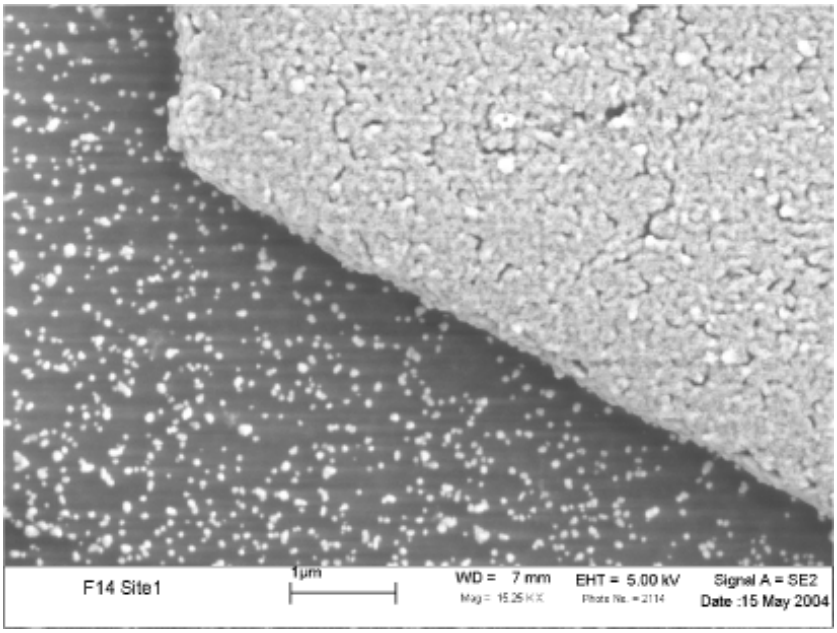


Figure 4.24: SEM micrograph of selective copper deposition on the Cr/Si disk and electrode versus the SiO_2 substrate.

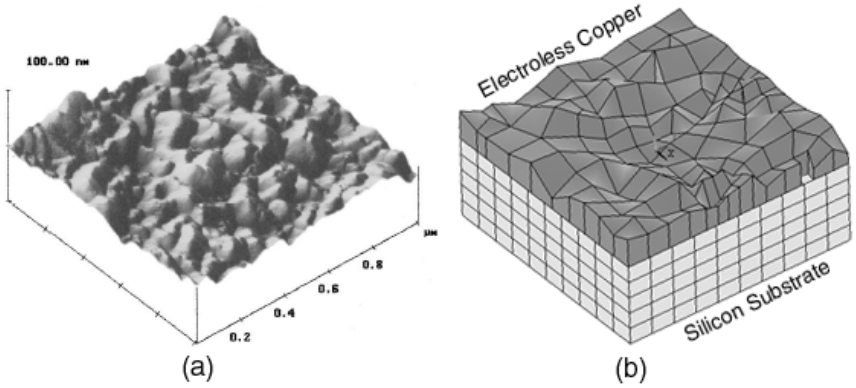


Figure 4.25: Comparison of electroless copper topographies: (a) atomic force microscope (AFM) micrograph of copper surface [108]; (b) ANSYS mesh of simulated copper surface.

exhibit a higher surface roughness than evaporated or sputtered metal films. In order to ascertain any potential effects that these rough copper layers would have on the frequency response and displacement response of the disk, structures using randomized SOLID45 meshes representing the electroless copper layer [Figure 4.25(b)] were simulated using the ANSYS FEA tool described in Chapter 3.

To generate the randomized copper mesh, seed nodes were created in random positions on the surface of the disk (much as the Pd catalytic sites are randomly arranged on the disk surface). These nodes are then extruded outwards to random heights perpendicular to the disk surface and connected together to form the copper mesh elements. The extrusion heights are determined from a Gaussian distribution. Therefore, the average thickness of the copper layer is determined by the mean of the distribution, and the average surface roughness is determined by the standard deviation of the distribution. The standard deviation was given as a percentage of the mean thickness. A standard deviation of 50% of the mean thickness represents an extremely rough surface while a standard deviation of 1% of the thickness represents a fairly smooth surface. The mesh shown in Figure 4.25(b) has a roughness value of 25% of the mean thickness of 200 nm. The same process is repeated for the nodes on the sidewall of the disk and the TRANS126 elements are attached to the copper surface covering the sidewall of the disk. (For a more detailed description of the meshing process and simulation, see Appendix B for a listing of the ANSYS code used.)

Once the mesh is constructed, simulations similar to those described in Chapter 3 are performed to determine the frequency of oscillation and current across the gap for the copper-coated disk. Table 4.3 shows the results of the copper-coated disk simulations. Five simulations were run in a Monte-Carlo type format for each combination of mean thickness (values in μm) and mean roughness shown n the table. The frequency and current values recorded in Table 4.3 are the average results of these five simulations.

As expected, the frequency decreases for increasing mean copper thickness due to the low E/ρ ratio for Cu. There is also a slight downward trend in frequency and upward trend in the standard deviation of the frequency as the surface roughness increases. The current increases monotonically with both thickness and roughness. This is expected since both the roughness and the thickness will increase the effective surface area and thus the capacitance in the gap spacing. It is estimated that the mean roughness for the copper layers deposited in this work is approximately 25%, meaning that current values in excess of 51 μA can be achieved with a 5 V bias and a 50 nm final gap spacing between the copper-coated electrode and disk.

4.7 Summary

The process steps used to fabricate the disk resonator and its accompanying electrodes are described in detail in this chapter. The process presented is relatively simple in that it only requires a single lithography step; however, the difficulty in lifting off thick Cr/Au metal layers makes it difficult to achieve the narrow gap spacings required to achieve detectable current flow across the gap. Gap spacing issues can be resolved by the incorporation of an electroless deposition step into the standard process that selectively coats the disk and electrode with a conductive Cu metal layer. The final gap dimensions in this process are ultimately determined by the duration of the Cu deposition step. The effects of this metal layer on the frequency response and the current across the transducer gap were simulated in the ANSYS FEA software. As expected, the added Cu layer decreases the center frequency of the disk but the addition of the metal in the gap region significantly increased the capacitance and current of the disk at resonance. Possible future applications of this process for IC implementations of disk resonators are described in the next chapter.

Mean Thickness	Mean Roughness	**Freq (MHz)** Mean Std. Dev.	**Current (uA)** Mean Std. Dev.
0.1	1%	207.98	26.66
		0.09	0.10
	10%	207.83	28.30
		0.17	0.49
	25%	207.74	33.36
		0.12	1.44
	50%	207.25	48.14
		0.31	3.26
0.2	1%	182.14	29.50
		0.05	0.07
	10%	182.13	34.03
		0.05	0.65
	25%	181.68	51.20
		0.16	2.91
	50%	180.10	103.45
		0.31	7.89
0.3	1%	167.98	32.10
		0.14	0.54
	10%	167.89	39.90
		0.19	1.85
	25%	167.12	72.75
		0.14	6.06
	50%	165.88	129.07
		0.41	19.92

Table 4.3: Results of ANSYS simulations of copper-coated disks.

Chapter 5

Conclusions and Future Work

The first goal of this thesis was the development of two switched-tank voltage-controlled oscillator designs for use in multiband receivers operating in the 5-6 GHz UNII band. The primary focus of this effort was the switched-tank functionality; phase noise optimization was not pursued. Traditionally, sub-par oscillator phase noise can be compensated for with a PLL circuit that locks the oscillator output to an extremely low phase noise off-chip quartz crystal resonator or SAW resonator. However, connections between on-chip circuitry and off-chip resonators introduce added cost, parasitics, and matching issues that could be mitigated by an exclusively on-chip solution. The second goal of this thesis, then, was to develop potential on-chip replacements for these off-chip resonators that could provide the same performance as the off-chip components. MEMS contour-mode disk resonators have been identified as a particularly attractive candidate due to their ability to achieve high (> 1 GHz) oscillation frequencies with reasonable dimensions, and compatibility with common IC processing techniques. The following sections highlight the accomplishments of this work and propose future research directions indicated by the knowledge gained in this work.

5.1 Conclusions

5.1.1 VCO Designs

As discussed in Chapter 2, two switched-tank VCOs with different power consumption and output power goals were designed in Motorola's HIP6WRF 0.18 μm BiCMOS process. The first VCO was designed with low power consumption as the primary goal; simulated results showed a total average current consumption of 6.75 mA (including the buffer) from a 1.8 V supply and a peak-to-peak output voltage swing of $\sim$2.0 V. The second VCO was designed with high output power as the primary focus; simulated results showed a peak-to-peak output voltage swing of $\sim$5.2 V but with a much higher average current consumption of 16.5 mA from a 1.8 V supply. The intended application of these VCOs was integration as LO sources for multi-band direct-conversion or low-IF receivers operating in the 5-6 GHz UNII band; thus the VCOs were designed with switchable-tank circuits that could discretely change the center oscillation frequency of the LO to cover the three sub-bands of the UNII spectrum. Specifically, the first design was intended to switch between two center frequencies, 5.25 GHz and 5.775 GHz, with 200 MHz of tuning range around each frequency using varactors. The second design was intended to switch between three center frequencies, 5.2 GHz, 5.3 GHz, and 5.775 GHz, with 100 MHz of tuning range around each frequency.

Measurements of the fabricated circuits showed significant, albeit expected, deviations from the designed tuning ranges. First, the center frequencies of each switched-state were shifted down from their design values. The first design exhibited center frequencies of 4.4 GHz and 5.37 GHz and the second exhibited center frequencies of 4.4 GHz and 4.7 GHz (the highest frequency range was not operational due to a faulty switch). The primary reason for the shift in frequencies is the unavoidable parasitic capacitances and inductances from the interconnect traces. It was anticipated that these parasitics would impact the frequency; however, there was a lack of confidence in the available parasitic extraction tools, so it was decided to attempt to extract the parasitics empirically from a subsequent comparison of the measured results to the simulated results. The measured tuning ranges and the frequency differences between the switched states were not significantly different from the simulated VCO

results. It can be concluded, therefore, that the switches and varactors perform as expected and can be used in future VCO designs.

The measured VCOs also exhibited lower output power values than predicted by the simulations. While the measured output power of the high output power VCO was significantly higher than that of the low-power VCO (-8 dBm versus -35 dBm), both values were lower than expected given the simulated output voltage swings. Some of this loss can be attributed to test setup losses ($\sim$1.5 dB) which were not calibrated out of these measurements. However, it is believed that the buffer amplifier design is responsible for the majority of the loss since the buffer amplifier did not bias to the expected current in the high output power VCO. In the low power VCO, the buffer amplifier and the VCO share the same bias line so it could not be specifically identified as the cause in this case. Therefore, before this buffer amplifier design is used in future iterations, the reason behind the faulty biasing must be determined.

Unfortunately, due to equipment and time constraints, the phase noise of the fabricated VCOs could not be measured. However, simulation results show the phase noise at a 1 MHz offset from the carrier was -107 dBc/Hz for the low power VCO, and only -99 dBc/Hz for the second VCO design (despite the high output power). The degraded phase noise of the high output power design is most likely due to the lower Q-factor of the tank circuit due to the added switch state as well as the increased current and shot noise in the -G_m transistors. A phase noise of -107 dBc/Hz is borderline for UNII band applications, meaning that currently only the low-power VCO would provide a sufficiently low phase noise performance. Therefore, the focus of the thesis turned to the development and characterization of on-chip MEMS contour-mode disk resonators that could potentially lower the phase noise of future VCOs.

5.1.2 MEMS Resonators

Contour-mode disk resonators have been deemed superior to beam-shaped resonators in that they offer higher resonant frequencies for a given size and are less susceptible to the effects of thermoelastic damping that can limit the Q-factor of beam-shaped resonators. Larger resonator size at a give resonant frequency offers higher capacitive coupling between the resonating element and the excitation electrodes, which leads to higher motional currents for the device. Chapter 3 discussed in detail the modeling

of such MEMS resonators through reduced-order mechanical and electrical lumped-element models, and through the use of finite element analysis. Since the mechanical model has limited application to electric circuit designers, the mass, spring, and dashpot mechanical elements were converted to their electrical analogs in the form of an equivalent series RLC circuit. From this viewpoint, it can be seen that the most critical design parameter with respect to the motional current through the device is the gap spacing, d, between the electrode and the disk. The current is proportional to d^{-4}, therefore the gap should be reduced as much as possible to maximize transduced current.

The lumped-element series resonant RLC circuit model is derived for ideal disk resonators, i.e. zero thickness disks with a singular centrally located nodal point; non-idealities such as finite-sized central posts, edge-connected DC bias lines, and multiple metal layers deposited on the disk surface cannot easily be modeled analytically. Therefore finite element analysis (FEA) was performed to characterize various second-order effects on the resonator frequency response. From this analysis, it was found that the center frequency of for disks of finite thicknesses did not differ appreciably from the zero-thickness predictions. It was also determined that increasing the size of the center nodal post caused a quadratic increase in center frequency. The displacement and motional current of disks with finite post sizes did not decrease significantly from the ideal case except for anomalies at post radii around 3 μm and greater than 6 μm.

The edge-connected DC bias lines did not significantly effect the displacement, motional current, or the frequency of the disks in the FEA simulations as long as their widths were kept thin in relation to the radius of the disk. Meanwhile, with multiple metal layers deposited on the disk it was found, as expected, that the resonant frequency was inversely proportional to the thickness of the metal layer, and the effect was more pronounced for disks coated in Cr/Au compared to those coated in just Cr due to the lower E/ρ ratio of Au. Simulations of the disk also showed that the motional current has a quadratic relationship with the DC bias, as expected. Neglecting possible inaccuracies of the ANSYS results near pull-in, the maximum allowable DC bias for the disks was found to have a quadratic relation with gap spacing, meaning that higher current values could be obtained with high voltages and large gap spacings. However, the voltages required to obtain high currents in wide gap devices are

unrealistically high for use on an IC. Therefore, the primary design consideration remains reduction of the gap spacings to be as small as possible to maximize the current from the relatively small available on-chip voltage supplies. Finally, it was determined that the center frequency does not vary appreciably with the DC bias ($\sim$0.2%), meaning that a single resonator could not be used as the voltage-controlled tuning device in a VCO.

Based on the knowledge gained from the FEA and lumped-element modeling, a fabrication process focusing on minimizing the gap spacing was developed for the contour-mode disk resonator in an available SOI technology. However, realizing gap spacings less than $\sim$100 nm was difficult using Cr/Au metal masks despite the high resolution capability of electron beam lithography. Therefore, a new metallization process utilizing electroless copper deposition was introduced that could define small gaps and increase the conductivity of the electrodes coupling to the disk. ANSYS Monte Carlo simulations of randomly arranged copper coatings on the disk surface revealed that the increased surface area from the uneven copper surface would significantly increase the motional current across the gap. However, it is also expected that the Q-factor of these devices would suffer from the additional copper layer. Nonetheless, this process may have potential for realizing reasonably high-Q on-chip resonators.

Unfortunately, time constraints did not allow testing of the fabricated resonators. However, the fabrication process is sufficiently optimized other researchers will be able to demonstrate operational RF-range resonators. This, along with other possibilities for future work, are listed in the next section.

5.2 Future Work

Several items remain for future work for both the VCOs and MEMS resonator topics. This section then concludes with a brief discussion of the possibility of integration of MEMS disk resonators into switched-tank VCOs.

5.2.1 VCO Designs

- As mentioned in Section 2.2.1, octagonal symmetric differential inductors offer superior Q-factor compared to the dual square-shaped inductors used in this design. Since there were no p-cells available in the HIP6 design kit for symmetric differential inductors at the time this work was completed, and since time constraints prohibited the design of a custom octagonal inductor prior to submission of designs for fabrication, the square-inductors were used in the prototype VCO. Subsequent to the design tape-out, custom-designed octagonal differential inductors were laid out and simulated. The design and performance of these inductors is presented in Appendix A. The higher Q-factor of these inductors would help both the phase noise and the current consumption for a given output voltage swing of future VCO designs.

- Since the parasitics of the interconnect traces have a significant effect on the oscillation frequencies of the fabricated designs, more attention must be paid to these interconnects in the future. First, the width of the traces can be reduced to find an optimum compromise between the effects of the lowered capacitance and the added series resistance. Second, parasitic extraction can be performed to determine the final simulated design frequencies (assuming availability of a more robust extraction tool). By comparing these results to the empirical results taken from this work, future designs can be modified to properly cover the frequency ranges of the UNII band. Layout modifications should also be performed to reduce the overall die area, which, in turn, will help with decreasing the trace lengths.

- Adequate equipment for testing the phase noise of the VCOs was not available at the time that these results were reported. To accurately determine the phase noise performance of the two designs, the circuit should be tested using an Agilent E5500, or equivalent, phase noise measurement system.

- Issues with the buffer amplifier were discovered with the fabricated circuits and efforts must be made to isolate the problem and eliminate it. In addition, a gain stage should be added after the buffer to boost the output signal. However, this will come at the expense of added power consumption.

5.2.2 MEMS Resonators

- The most immediate item is testing of a fabricated SOI MEMS disk resonator structure. The fabrication process has been fully developed; however, time constraints did not allow for resonator testing before this work was completed. Improvements to the available fabrication equipment will certainly increase the yield of the fabricated devices. Testing should be performed at ambient pressure and in vacuum to evaluate the hypothesis that a hermetic package is not necessarily required for contour-mode disk resonators due to their high energy of vibration. Testing should also vary such parameters as the radius, central post size, and copper layer thickness to determine the validity of the ANSYS and lumped-element model results.

- Multiple pole filters, such as those based on beam resonators described in [27], should be designed using contour-mode resonators. Theoretically, connecting disks of different radii together through the DC bias lines could result in a wide bandwidth, high-Q filter. This filter could be first designed and simulated in ANSYS to determine the frequency response and then fabricated using the SOI process described here, or other commercially available MEMS process. This type of filter could be used to replace the currently off-chip SAW-based bandpass filter in multiband receivers such as those described in Chapter 1.

5.2.3 MEMS/VCO Integration

Finally, the possibility of integration of the MEMS devices into switched tank VCOs should be explored. Figure 5.1 shows a conceptual schematic of how such a VCO could be designed. The low-Q LC tank could be replaced with an array of disks of different radii that could be turned on and off by simple control circuitry. This would discretely change the center frequency of the VCO just as the switched capacitors shift the center frequency in the LC VCO. Alternatively, a PLL could be designed with the disk resonator taking the place of the normally off-chip crystal frequency reference. Both scenarios would serve to significantly reduce the RF frequency source phase noise compared to existing single-chip designs. The switched-tank circuit shown is conceptual in nature, and several modifications would be required to design an actual differential VCO based on the MEMS disk resonator. For instance, two

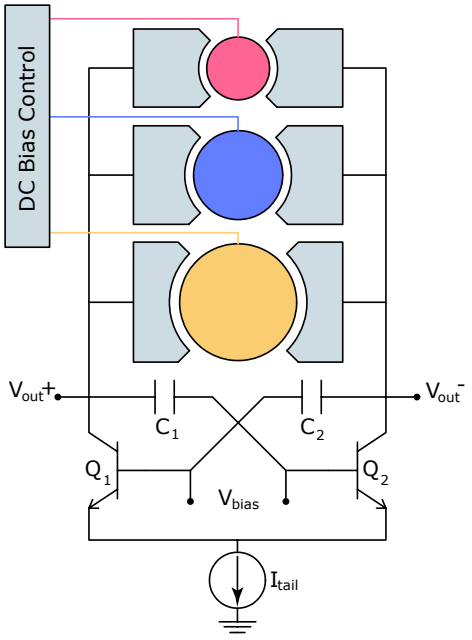


Figure 5.1: Conceptual schematic of contour-mode disk resonators integrated into a switched-tank VCO.

disk resonators would be required for each frequency to guarantee symmetry of the differential VCO. The exact topology of the circuit is left as an item of future work.

Before topologies such as the one shown in Figure 5.1 could become common in multi-band receivers, it is critical that the fabrication process be migrated to a commercially available multiple layer CMOS or BiCMOS process similar to the HIP6 process. The SOI process used in this work is an example of how the MEMS resonators can be fabricated with techniques compatible with IC processing; however, the surface micromachining of the Si substrate ultimately reduces the commercial viability of this process.

Figure 5.2 shows, conceptually, how the contour-mode resonator could be fabricated in a three metal layer CMOS process. The MEMS resonators could be fabricated in the top "bump" layer after all of the processing the lower metals has been completed. By patterning vias in the topmost passivation layer (blue color), and growing a thick copper layer via a standard electroplating process, the MEMS resonators could be fabricated in the much the same way that the inductors used in the VCOs of this

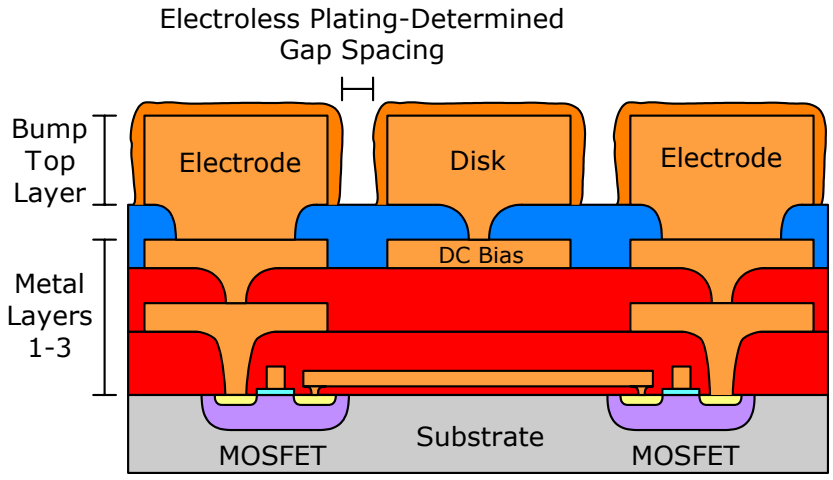


Figure 5.2: Conceptual diagram showing the cross section of a potential CMOS/MEMS integrated process layer stack.

work are fabricated. By etching the last passivation layer, the MEMS resonator could be released from the substrate and left free to vibrate. Since the deposition rate of electroless plating is typically far slower than that of electroplating, the gap spacing between the electrode and the disk can be very finely controlled using an electroless deposition step after the bulk of the copper has been electrodeposited (Figure 5.2) Unfortunately, the high Q-factors and resonant frequencies achievable using single-crystal Si are obviated in this design. Nonetheless, it is critical that MEMS resonators be integrated into a commercial process if they are to compete with off-chip crystals or SAW resonators.

Appendix A

Symmetrically Wound Octagonal Differential Inductor Simulations

As discussed in Section 2.2.1, the square spiral inductors used in the VCO designs presented in this work have lower Q-factors for a given inductance value compared to circular spiral or octagonal spiral-shaped inductors. In addition, the layout of a differential inductor consisting of a pair of individual inductor p-cells reflected about the line of symmetry leads to the cancellation of some of the magnetic field generated by each inductor, thus reducing the total inductance value of the pair by more than 20% from the value provided by the p-cells. In a symmetrically wound differential inductor, on the other hand, the currents in each coil flow in the same direction. There is no field cancellation and the mutual inductance between the coils will increase the total inductance for a given number of turns. This increases the ratio of energy storage to loss in the inductor and thus the Q-factor. This appendix discusses the layout and simulation results for octagonal-shaped symmetrically wound differential inductors for potential use in a second-generation, higher performance VCO.

A.1 Layout

A generic layout for the symmetrically wound differential octagonal spiral planar inductor is shown in Figure A.1. Due to the topology of the inductor, the current in each adjacent coil flows in the same direction, meaning that there is no cancellation of

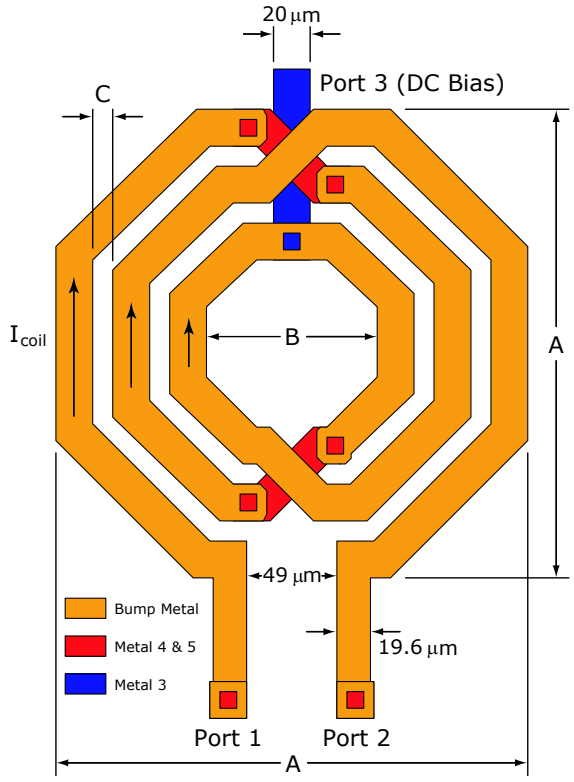


Figure A.1: Dimensions and layout of differential octagonal inductor.

magnetic field as was the case with the dual spiral inductor. The layout was ported from a p-cell inductor available in the Motorola CDR1 process, a more mature SiGe BiCMOS process similar to the HIP6 process used for the VCOs in this work. To port the inductor geometry, the inductor was laid out in the CDR1 process, exported to a GDSII stream, and imported into a HIP6 layout. The layer designations were then changed to correctly match those in HIP6 and the geometry was modified to meet the design rule specifications of HIP6.

Since the symmetric octagonal differential inductor structure was available as a p-cell in the CDR1 design kit, the inductance values were known to a good approximation before transferring the design to HIP6. Five different symmetric octagonal inductor designs were laid out and simulated with the Momentum EM solver. For each geometry, the overall width and height (dimension A), the inner diameter of the innermost trace (dimension B), and the trace spacing (dimension C) were changed to obtain the needed inductance value. The first inductor was sized for a value of 2

nH to closely match the design inductance of the square inductors used in the VCO designs. The remaining four inductors were designed for smaller inductance values in order to compensate for the added parasitics of the interconnects. The values of these inductors were chosen to be 1.7 nH, 1.6 nH, 1.5 nH, and 1.2 nH.

A.2 Simulation Results

The symmetric octagonal inductor geometries were simulated using the Momentum 2.5D EM solver and the resulting Y-parameters were converted to the effective inductance and Q-factor through the following equations:

$$Z_{in} = R + jX = \frac{Y_{11} + Y_{22} + 2Y_{12}}{Y_{11}Y_{22} - Y_{12}^2}, \tag{A.1a}$$

$$L = \frac{\mathrm{Im}(Z_{in})}{2\pi f}, \text{and} \tag{A.1b}$$

$$Q = \frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})}. \tag{A.1c}$$

The resulting simulated Q-factors for each of the octagonal spiral inductors (and the dual square inductor for comparison purposes) are shown in Figure A.2. As expected, the Q-factors for the symmetric octagonal inductors exceeds that of the square inductor by ∼50% in the frequency range of interest (5-6 GHz). Therefore, VCOs based on these symmetric octagonal inductors should have lower phase noise performance due to the higher Q of the inductor in the frequency range of interest.

The simulated effective inductances from 1-20 GHz are shown in Figure A.3. As expected, the self resonant frequency, f_{sr}, for the symmetric octagonal inductors decreases for increasing inductor size. By extrapolating the simulated data beyond 20 GHz, it can be seen that only the 1.2 nH octagonal inductor has a f_{sr} that exceeds that of the dual inductor. Therefore, the most significant detriment to using the octagonal inductor versus the square inductor is the lowering of f_{sr}. However, the f_{sr} of the 2 nH is inductor ∼16 GHz, which is sufficiently far from the frequency range of interest for f_{sr} not to be an issue.

Figure A.4 shows, in more detail, the simulated inductance values over the frequency

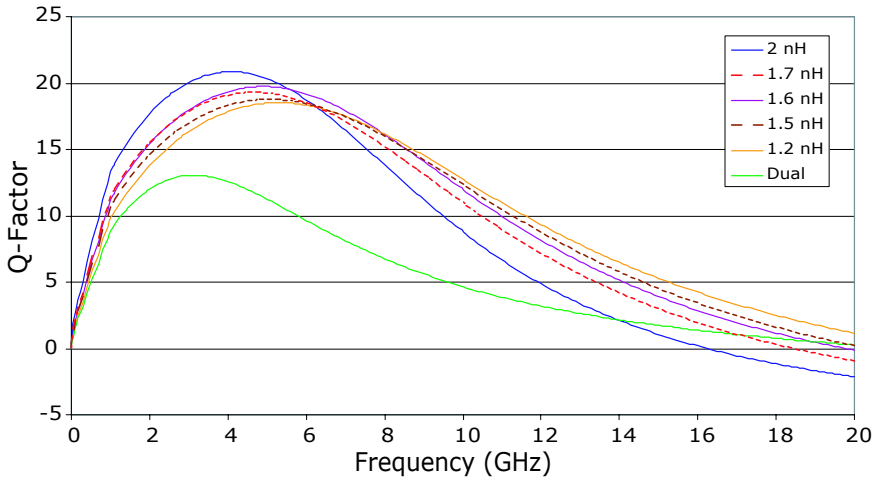


Figure A.2: Comparison of Q-factors for 5 symmetric octagonal inductor sizes versus the differential square inductor used in the VCO designs described in Chapter 2.

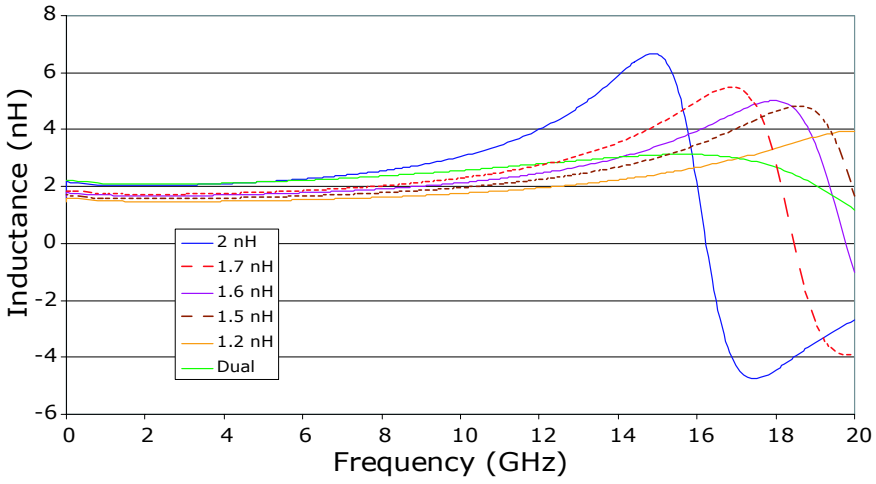


Figure A.3: Comparison of inductance values for 5 symmetric octagonal inductor sizes versus the differential square inductor used in the VCO designs described in Chapter 2.

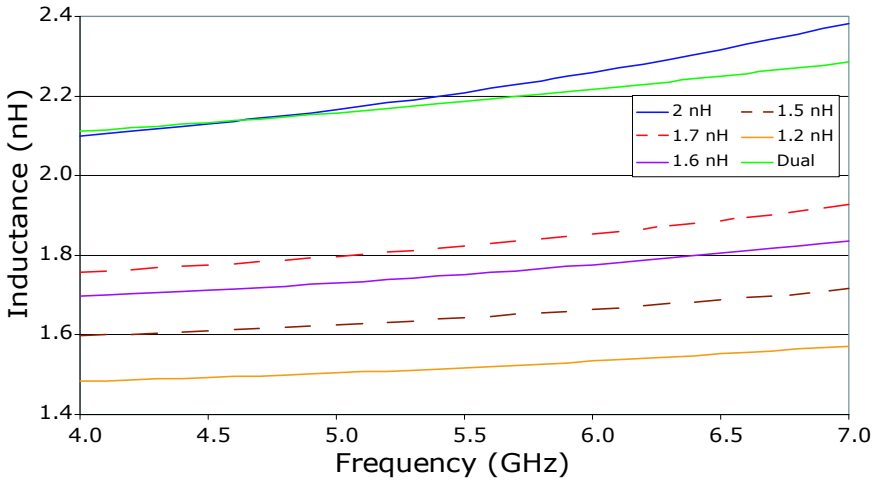


Figure A.4: Comparison of inductance values for 5 octagonal inductor sizes versus the differential square inductor used in this work focusing on the 4-7 GHz range.

Inductance (P-Cell Value)	Dimensions (See Figure A.1)			Simulated Ind at 5.5 GHz	Simulated Q at 5.5 GHz	Self Resonant Frequency
	A	B	C			
1.2 nH	274.4	78.4	19.6	1.52 nH	18.5	> 20 GHz
1.5 nH	258.7	94.1	11.76	1.64 nH	18.7	> 20 GHz
1.6 nH	265.6	100.9	11.76	1.75 nH	19.6	19.78 GHz
1.7 nH	258.7	105.8	8.82	1.82 nH	19.0	18.45 GHz
2.0 nH	278.3	125.4	8.82	2.21 nH	19.6	16.25 GHz
2.8 nH (Square)	See Figure 2.8			2.19 nH	10.4	> 20 GHz

Table A.1: Comparison of 5 octagonal differential inductors to the square differential inductor introduced in Section 2.21 (dimensions are in microns).

range 4-7 GHz. As is evident, the inductance for the 2.0 nH octagonal inductor and the square inductor are similar over the frequency range of interest. Therefore, the dual square inductors could be replaced by the 2.0 nH octagonal inductor with minimal tuning changes. The other inductance values, on the other hand, are significantly lower than the square inductor and could be used to compensate for the capacitances added to the tank from the interconnect parasitics. Indeed, the 1.2 nH symmetric octagonal inductor was used in a second generation VCO designed for use in an ultra wide band transmitter [115]. Table A.1 summarizes the dimensions and the simulated performance for the six inductors discussed in this appendix.

Appendix B

ANSYS Code for Simulating Electroless Copper Layers

The following code listing can be used to model, mesh, and simulate the electroless copper layers deposited on the contour-mode disk resonator. Exclamation points indicate comments.

```
/prep7
/title, Electromechanical Simulation of 20 Micron Disk
/uis,msgpop,3

!!!!!!!!!!!!!!!!!!!!!Seed Random Generator!!!!!!!!!!!!!!!!!!!!!!!!!!!!
!The random number generator must be seeded with a pseudorandom number!
!(i.e.  the current CPU time) so that the random number sequence      !
!differs from simulation to simulation                                !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

*get,time,active,0,time,cpu        !Retrieve the current CPU time
bigtime=time*1e7                   !These four lines isolate the
smalltime=nint(time*1e4)*1e3       !four last digits of the time
*if,smalltime,gt,bigtime,then      !which are assumed to be random
smalltime=smalltime-1e3
*endif
```

```
randindex=nint(bigtime-smalltime)  !Call the rand function a number
*do,randcounter,1,randindex        !of iterations determined by the
temprand=rand(0,1)                 !last four digits of the CPU time
*enddo

!!!!!!!!!!!!!!!!!!!!!!!!!Define Constants!!!!!!!!!!!!!!!!!!!!!!!!!!!!
!Define constants such as the radius of the disk and Q-factor         !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

Q=9400                 !Q-factor from Nguyen, et al
dr=1/(2*Q)             !Constant damping ratio is related to Q-factor
mean = 0.1             !Mean height of copper mesh on disk surface (um)
stdDev = 0.00001       !Standard Deviation (mean thickness) (um)
maxHeight = 0.2        !Maximum height of copper mesh (um)
minHeight = 0.02       !Minimum height of copper mesh (um)
radius = 10            !Radius of Disk (um)
refinementLevel=25     !Number of iterations for mesh randomization
.                      !routine (determines randomness of seed mesh)
blankSpaceRatio=0.99   !Percentage of voids in copper surface
postSize = 1.5         !Size of center post (um)
diskVoltage = 5.0      !DC bias voltage
ACVoltage=1.0          !AC excitation voltage

!!!!!!!!!!!!!!!!!!!!!!!!!Define Elements!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
!Define element types for the Si disk and Cu surface                   !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

csys,1       !Rotate into Cylindrical Coordinates
et,1,42      !Plane element for copper seed mesh layer
et,2,45      !Solid element for Si disk and Cu surface
et,3,200,10  !Placeholder solid element for use in sidewall meshing

!!!!!!!!!!!!!!!!!!!!!!!!!Define Materials!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
```

```
!Define Cu and Si material properties - material data files are       !
!available from the ANSYS website www.ansys.com                       !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

mat,1                    !Define material 1 as Cu
mpread,Cu_Blk_ln,SI_MPL
mat,2                    !Define material 2 as Si
mpread,Si_Blk_ln,SI_MPL

!!!!!!!!!!!!!!!!!!!Create Copper Seed and Mesh!!!!!!!!!!!!!!!!!!!!!!!!
!Define a seed mesh of nodes from a random mesh of a circle with a    !
!radius equal to the disk radius.   These nodes will be extracted into!
!the z-direction to define the copper elements                        !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

mat,1
type,1
cyl4,0,0,radius,0,0,360   !Create circle that will be the seed for
!the copper mesh layer

asel,all                  !Select this circle
esize,,50                 !50 divisions per line for meshing
expansionRatio=rand(2,3)  !Randomly determine the outer element size
.                         !to inner element size ratio
mopt,expnd,expansionRatio !Allow inner mesh areas to increase 3 times
.                         !the size of the exterior elements
.                         !This creates a more varied and random mesh
.                         !at the disk exterior
mshape,0                  !Quad shaped elements
mshkey,0                  !Free meshing
amesh,all                 !Mesh area

!!!!!!!!!!!!!!!!!!!!!!Randomly Refine Mesh!!!!!!!!!!!!!!!!!!!!!!!!!!!
!Refine the largest of the plane elements in order to increase the    !
```

```
!mesh density (the higher expansionRatio, the less dense the mesh)    !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

*do,outsideCounter,1,refinementLevel,1
.            !RefinementLevel determines number of refinement iterations
*get,elemCount,elem,0,count   !Find number of elements
maxarea=0                     !Initialize maximum area
*do,counter,1,elemCount,1     !Calculate the largest element by size
*get,elemarea,elem,counter,area
*if,elemarea,gt,maxarea,then
maxarea=elemarea              !Reassign the maximum area and element
.                             !if a larger is found
maxelem=counter
*endif
*enddo
erefine,maxelem,maxelem,1,1   !Refine the largest existing element
*enddo

!!!!!!!!!!Extrude planar elements into random 3-D elements!!!!!!!!!!!!!
!This is where the 3-D copper elements are formed.  Each of the nodes !
!defined by the random planar mesh are copied and extruded a random   !
!in the z-direction from the surface.  These nodes are then connected !
!into the block shape and assigned an element number                  !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

immed,0                       !Turn off immediate display
shpp,warn                     !suppress warning messages

type,2                        !Switch to the volume elements

*get,elemCount,elem,0,count   !Get new number of elements
*get,nodeCount,node,0,count   !Get number of nodes
*dim,nodes,array,nodeCount    !nodes will store the zcoord nodes
.                            !paired with the planar nodes
```

```
*dim,blockNodes,array,8       !blockNodes will store the 8 nodes
.                             !needed for the creation of the block node

*do,currentElem,1,elemCount,1 !Cycle through every element

*do,nodeLoc,1,4,1             !Cycle through all 4 nodes connected
.                             !to current element

currentNode = nelem(currentElem,nodeLoc)
blockNodes(nodeLoc)=currentNode   !Start the block node with this node
*if,nodes(currentNode),EQ,0,then  !If there exists no z-coord node
.                                 !for this location create one
xloc = nx(currentNode)
yloc = ny(currentNode)
zloc = gdis(mean,stdDev)         !Use Gaussian distribution to
.                                !determine height of node
*if,zloc,lt,minHeight,then       !Reset height if too tall or short
zloc=minHeight
*elseif,zloc,gt,maxHeight
zloc=maxHeight
*endif
nodeCount=nodeCount+1            !Increment global node count to make
.                                !room for new node
n,nodeCount,xloc,yloc,zloc       !Create new node at some z-offset
.                                !from planar node
nodes(currentNode)=nodeCount     !Store the new node into the
.                                !array of pairs
*endif
blockNodes(nodeLoc+4)=nodes(currentNode)
!This pair is offset 4 nodes from the original in the element creation

*enddo
blank=rand(0,1)
*if,blank,lt,blankSpaceRatio,then !Create the element if blank check passes
```

```
e,blockNodes(1),blockNodes(2),blockNodes(3),blockNodes(4),
blockNodes(5),blockNodes(6),blockNodes(7),blockNodes(8)

*endif
*enddo

nsel,s,loc,z,0
cm,bottomCopper,node            !Save z=0 nodes in component bottomCopper
nsel,all

!!!!!!!!!!!!!!!!!!!!!!Create Sidewall Nodes!!!!!!!!!!!!!!!!!!!!!!!!!!
!To create the nodes of the sidewall, the seed copper layer used to   !
!create the top copper is extruded in the negative z-direction five   !
!times.  The resulting nodes are extruded in the radial direction just!
!the top copper nodes are extruded in the positive z-direction        !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

!To create nodes on side of disk, the top copper meshed surface is
!extruded random distances and with random rotation

type,3                       !Change to placeholder MESH200 elements
extopt,esize,1               !Advance one division at a time
extopt,attr,0,0,0            !No attributes are kept

finalZdir=0.34               !Final depth of extrusion
currentZdir=0
*do,currentArea,1,20,1       !Maximum of 20 steps (should never reach this)
*if,currentZdir,eq,finalZdir,exit     !Exit if 0.34 um has been reached
rotation=rand(-1,1)          !Find random rotation angle between 1 and
.                           !-1 degrees

zdisp=rand(0.05,0.086)      !Find random height of slice from
.                          !-0.16 to +0.16 of 0.34/5
```

```
*if,(currentZdir+zdisp),gt,finalZdir,then !Reset depth if the resulting
.                                          !depth is greater than 0.34 um
zdisp=finalZdir-currentZdir
*endif
currentZdir=currentZdir+zdisp
vext,all,,,0,rotation,-zdisp,1,1,1   !Extrude by random offset and angle

asel,s,loc,z,-currentZdir   !Select the lower area to be extruded next
*enddo

!!!!!!!!!!!!!!!!!!!!!!Create Sidewall Copper!!!!!!!!!!!!!!!!!!!!!!!!!

nsel,s,loc,x,radius         !Select nodes around outermost edge of disk
cm,edge,node                !Define all edge nodes as component

esel,u,type,,1              !Unselect unneeded plane nodes
*get,maxElem,elem,0,num,max !Find maximum element number
*get,minElem,elem,0,num,min !Find minimum element number
*get,elemCount,elem,0,count !Find total element count

*get,minNode,node,0,num,min !Find minimum element number
*get,maxNode,node,0,num,max !Find maximum element number
*get,maxNodeDefined,node,0,num,maxd

*dim,newNodes,array,maxNode,2 !Stores location and number for all new nodes
created
*dim,faces,array,elemCount,9  !Stores existing nodes in groups of faces

facesIndex=1

immed,0

*do,currentNode,1,maxNode,1
*if,nsel(currentNode),eq,1,then
```

```
yloc=ny(currentNode)
zloc=nz(currentNode)
xloc = gdis(mean,stdDev)      !Use Gaussian distribution to determine
.                              !extension of node from center (x coord)
*if,xloc,lt,minHeight,then    !Reset node if it oversteps bounds
xloc=minHeight
*elseif,xloc,gt,maxHeight
xloc=maxHeight
*endif
xloc=xloc+nx(currentNode)
maxNodeDefined = maxNodeDefined+1
n,maxNodeDefined,xloc,yloc,zloc
newNodes(currentNode)=maxNodeDefined
.                      !Store new node and its new location in newNodes
newNodes(currentNode,2)=xloc
*do,currentElem,1,10,1
element=enextn(currentNode,currentElem)
.                      !Find all elements connected to the current node
*if,element,eq,0,exit
.                      !If element equals 0 then all elements connected
.                      !to this node have been processed
*if,esel(element),eq,1,then      !If the node is selected
faces(facesIndex,1)=element      !Store the element's nodes in faces
.                                !in the order of their positions
*do,elemPosition,1,8,1
tempNode=nelem(element,elemPosition)
*if,nsel(tempNode),eq,1,then
faces(facesIndex,(elemPosition+1))=tempNode
*endif
*enddo
facesIndex=facesIndex+1
esel,u,elem,,element     !Unselect element so that it is not reprocessed
*endif
*enddo
```

```
*endif
*enddo

type,2
mat,1
*dim,newElement,array,8  !Array will store 8 nodes that make up new element


*do,currentFace,1,elemCount,1
doneSoFar=1
*if,faces(currentFace,1),eq,0,exit   !End of array has 0
*do,elemPosition,2,5,1               !Go through the first half
.                                    !of the nodes in faces

*if,faces(currentFace,elemPosition),ne,0,then
.                                    !If the node is in a position

newElement(doneSoFar)=faces(currentFace,elemPosition)
.            !Place it and its companion in newFaces in the newElement array

newElement(doneSoFar+4)=newNodes(faces(currentFace,elemPosition))
doneSoFar=doneSoFar+1
*endif
*enddo
*if,doneSoFar,ne,5,then
!If doneSoFar does not equal 5 then not all 4 nodes have been stored and the
!remainder must be in the last half of the faces array
doneSoFar=4
*do,elemPosition,6,9,1
!Place second half nodes in to elemPosition backwards to
!ensure that they are in order

*if,faces(currentFace,elemPosition),ne,0,then
newElement(doneSoFar)=faces(currentFace,elemPosition)
```

```
newElement(doneSoFar+4)=newNodes(faces(currentFace,elemPosition))
doneSoFar=doneSoFar-1
*endif
*enddo
*endif
e,newElement(1),newElement(2),newElement(3),newElement(4),
newElement(5),newElement(6),newElement(7),newElement(8)
.                   !Create the new element
*enddo

!!!!!!!!!!!!!!!!Clear Volumes, Areas and Elements!!!!!!!!!!!!!!!!!!!

alls           !select everything
aclear,all     !delete everything
vclear,all
vdele,all
adele,all

numcmp,node    !Compress node and element numbers
numcmp,elem

!!!!!!!!!!!!!!!!!!!!Create Si Disk and Mesh!!!!!!!!!!!!!!!!!!!!!!!!!
!Now that the copper shell is created, need to create a disk that     !
!will represent the Si.                                               !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

type,1
mat,2
esel,none
nsel,none
cyl4,0,0,radius,0,0,360 !Create circle that is top face of silicon disk

esize,,20               !20 divisions per line for meshing
mshape,0                !Quad shaped elements
```

```
mshkey,1                !Mapped meshing
amesh,all               !Mesh area

!!!!!!!!!!!!!!!!!!!!!!!!Extrude with vext!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

type,2                      !Change to anisotropic solid
extopt,esize,5              !Five divisions of disk in z-direction
vext,all,,,0,0,-0.34,1,1,1 !Extrude circle -0.34 um in z-direction

esel,r,type,,2
!Make sure that the less dense elements and the dense nodes are selected
cm,topSilicon,elem

asel,all
aclear,all                  !Remove all planar elements from database
numcmp,elem

!!!!!!!!!!!!!!!!!!Constrain nodes at interface!!!!!!!!!!!!!!!!!!!!!!!
!Need to glue together the nodes on the outside edges of the Si and   !
!the nodes on the inside edge of the copper                           !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

nsel,all
nrotat,all   !Ensure that all nodes are rotated into cylindrical system

nsel,none
esel,none
cmsel,s,bottomCopper   !Select the Cu nodes at the Si/Cu interface
cmsel,a,edge
nsel,r,loc,z,0,-0.34
cmsel,a,topSilicon     !Select the Si elements at the Si/Cu interface
ceintf,,all
!Constrain all of the nodes from the Cu coating to the
!elements of the Si disk
```

```
!!!!!!!!!!!!!!!!!!!!!Define Transducer Nodes!!!!!!!!!!!!!!!!!!!!!!!!!!
!The TRANS126 transducer nodes model the gap spacing between the      !
!electrode and the disk.   The TRANS126 nodes span from the edge of   !
!the copper plated to a location in space determined by the gap       !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

nsel,all
nsel,u,loc,x,0,10
cmsel,u,edge               !Select the sidewall nodes of the copper
nsel,u,loc,y,-10,10        !excluding a 20 degree area on each side
nsel,u,loc,y,170,190

cm,edge,node
emtgen,'edge','trans_elem','elec_nodes','UX',0.001
!Use the emtgen macro to automatically generate the TRANS126 elements
keyopt,4,4,1
!Constrain TRANS126 voltage drop so that the matrix is symmetric

nsel,none
cmsel,s,elec_nodes         !Rotate new nodes into csys 1
nrotat,all
cmsel,s,trans_elem
nsle
cmsel,u,elec_nodes         !Redefine edge nodes
cm,edge_nodes,node

!!!!!!!!!!!!!!!!!!Define Loads and Constraints!!!!!!!!!!!!!!!!!!!!!!!!
!Constrain center post as nonmoving in all radial directions          !
!Constrain electrode edge as nonmoving in all radial directions       !
!Apply 0 V DC bias to electrode                                       !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
```

```
nsel,all

nsel,s,loc,x,0,postSize   !Constrain (all DOFs) center post 1 um radius
nsel,r,loc,z,-0.34        !from center and on bottom side of disk
d,all,all,0

cmsel,s,elec_nodes        !Constrain edge of electrodes as nonmoving
d,all,ux,0,,,,uy,uz
d,all,volt,0              !Constrain edge of electrodes as DC ground

nsel,all
esel,all
finish                    !Finished with modeling

!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!Solve!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
!Three solve steps:                                                  !
!DC solution of bias prestress                                       !
!Modal solution to find all mode shapes in a given range             !
!Harmonic solution at contour-mode frequency to find disp and current !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

/solu
antyp,static                  !Perform static simulation with prestress
pstres,on                     !effects turned on
kbc,1
nsubs,1
d,edge_nodes,volt,diskVoltage !Constrain edge of disk as +5 DC volts
outres,all,all
cnvtol,f,1,1e-3               !Set convergence tolerance
solve
finish

/solu
antyp,modal                   !Modal analysis
```

```
modopt,lanb,5,200e6           !Block Lanczos (default);
.                              !extract 10 modes; start at 200MHz
mxpand                        !Expand all found modes
pstres,on                     !Include prestress effects
solve
finish

/solu
antyp,harm                    !Change to harmonic solution
pstres,on
harfrq,freq-10e6,freq+10e6    !Set sweep around center frequency found
.                              !from modal simulation
kbc,1                         !Loads are stepped, not ramped
nsubs,20                      !Number of substeps (1MHz per step)
outres,all,all                !Output all data
d,edge_nodes,volt,ACvoltage   !Apply AC voltage to electrode
dmprat,dr                                    !Set damping ratio
solve
finish

!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!Results!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
!Two solve steps:                                                      !
!Find current through TRANS126 elements                                !
!Find displacement of edge nodes attached to TRANS126 elements         !
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

/post26                       !Enter time-hist postprocessor
!Find current total current
esel,s,ename,,126             !Select TRANS126 elements
*get,minelem,elem,0,num,min   !Find lowest numbered TRANS126 element
*get,maxelem,elem,0,num,max   !Find highest numbered TRANS126 element
currElem=minelem
*do,elemIndex,minelem,maxelem !Loop over all TRANS126 elements
esol,2,currElem,,nmisc,24,IR  !Get real current component from TRANS126
```

```
esol,3,currElem,,nmisc,25,IR  !Get imaginary current component
realvar,2,2                   !Re(real value of current)
imagin,3,3                    !Im(imaginary value of current)
prod,2,2,2                    !Re^2
prod,3,3,3                    !Im^2
add,4,2,3                     !Re^2+Im^2
sqrt,4,4                      !sqrt(Re^2+Im^2)
add,5,5,4                     !Running total of all TRANS126 elements
currElem=elnext(currElem)     !Skip to next element
*if,currElem,eq,0,exit
*enddo

!Find average maximum displacement
esel,s,ename,,126             !Select TRANS126 elements
esln                          !Select all nodes connected to TRANS126
cmsel,u,elec_nodes            !Unselect electrode nodes
*get,minnode,node,0,num,min   !Find lowest numbered node
currNode=minnode
*get,maxnode,node,0,num,max   !Find highest numbered node
*get,nodecount,node,0,count   !Get total node count
*do,nodeIndex,minnode,maxnode !Loop over all nodes
nsol,6,currNode,u,x           !Get radial displacement of node
abs,6,6                       !Take absolute value
add,7,7,6                     !Running total of all displacements
currNode=ndnext(currNode)     !Go to next node
*if,currNode,eq,0,exit
*enddo
prod,7,7,,,,,,1/nodecount     !Take average of all nodes
nsel,all                      !Reselect everything
esel,all
```

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Vita

Christopher Allen Maxey was born on June 20^{th}, 1980 to Jim and Donna Maxey in Fayetteville, AR. After moving to several locales, he and his family settled in Simpsonville, SC in the spring of 1987. Ten years later, he graduated from Southside High School in the nearby city of Greenville, SC with an International Baccalaureate degree. During his tenure at Southside, he successfully completed the requirements for the Eagle Scout award, which he received in 1995. His interest in math and science led him to pursue a Computer Engineering degree at Virginia Polytechnic Institute and State University (Virginia Tech) starting in the summer of 1997. In 1999, he joined Nortel Networks in Durham, NC as a co-op student where he specialized in Oracle databases, PERL scripting, and web-interface programming. By the spring of 2002, his undergraduate studies were complete and he received his Bachelor's of Science degree *summa cum laude*.

Based on his experiences at Nortel, he decided to pursue an Electrical Engineering Master's of Science degree. He chose Virginia Tech from among three other prestigious universities due, primarily, to a strong relationship with the Wireless Microsystems Laboratory and its primary investigator, Dr. Sanjay Raman, forged during an undergraduate research project. He was awarded a National Science Foundation Fellowship in 2002 to help fund his graduate studies. On August 6^{th}, 2004, Christopher's seven year tenure in Blacksburg, VA will come to an end. He has accepted a job with the Institute for Scientific Research (ISR) in Fairmont, WV as a research engineer.