Design, Implementation, and Analysis for an Improved Multiple Inverter Microgrid System

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ABSTRACT

Distributed generation (DG) is getting more and more popular due to the environmentally-friendly feature, the new generation unit developments, and the ability to operate in a remote area. By clustering the paralleled DGs, storage system and loads, a microgrid (MG) can offer a power system with increased reliability, flexibility, cost effectiveness, and energy efficient feature. Popular energy sources like photovoltaic modules (PV), wind turbines, and fuel cells require the power-electronic interface as the bridge to connect to the utility grid for usable transmission.

The inverter-based microgrid system, however, suffers more challenges than traditional rotational power system. Those challenges, including much less over current capability, the nature of the intermittent renewable energy sources, a wide-band dynamic of generation units, and a large grid impedance variation, call for more careful system hardware and control designs to ensure a reliable system operation. Major design interests are found in (i) precision power flow control, (ii) proper current sharing, (iii) smooth transition between grid-tie and islanding modes, and (iv) stability analysis.

This dissertation will cover a complete design and implementation of an experimental microgrid with paralleled power conditioning systems operating in the grid-tie mode, islanding mode, and mode transfers. A universal inverter is proposed with the LCL filter to operate in both grid-tie and standalone mode without any hardware modification.

Next, controllers of individual inverters running in basic microgrid modes will be discussed to ensure high quality output characteristics. The admittance compensation will also be proposed to avoid reverse power flow during the grid-tie connection transient. Combining previous designed single inverters, a CAN-bus multi-inverter microgrid system will be established. The current sharing with the proposed frequency-decoupled transmission will be implemented to extend the transmission distance. Next, smooth mode transfer procedures between grid-tie mode and islanding mode will be suggested based on the circuit principles to minimize the excessive electrical stresses. Finally, the state-space analysis of the proposed multi-inverter microgrid system will be conducted to investigate the stability under system variations and optimize the system performance.

Experimental and simulation results show that the designed universal inverter can provide stable outputs in different basic microgrid operation modes. With the proposed current sharing scheme, the output current is equally shared among paralleled inverters without a noticeable circulating current. Both the simulation and experimental results of mode transfer show that the multi-inverter based microgrid system is able to switch between grid-tie and islanding modes smoothly to guarantee an uninterrupted power supply to the critical loads. Based on eigenvalue analysis, the study of stability analysis also shows the agreement of the design, simulation and test results which further verifies the reliability of the designed multi-inverter microgrid system.

To my parents

Yu-Tang Chen and Po-Quai Huang

To my grandparents

Zhang- Cheng Chen and Chan Xie

To my wife

Shu-Hui Liu

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Chapter 1

Introduction

1.1 Research background

In the past few decades, distributed generation (DG) [1]-[4] has gained lots of attention due to the environmentally-friendly feature of alternative energy, the development of new generation units, and its ability to offer more options of price-quality combination to meet the changing electricity market. DG units provide power in the vicinity of loads, which reduces the losses during power transmission and improves the power quality to the loads. Furthermore, the DG units can also be utilized in a remote area where the grid is not reachable, or it can be used as a backup source when the grid is not available.

Photovoltaic modules (PV) [5], and wind turbines [6], fuel cells [7], Microturbines [8] are commonly used as the sources for the DG units. Because the first two energy sources do not require purchasing fuel and their installation cost falls in the order of $1/W, the installation of PV and wind turbines increased at a rate of 20-40% per year in the last few years [9]-[10]. Even though fuel cells and microturbines have a higher fuel cost compared to the first two energy sources, they are preferable for the system stability because they do not rely on the weather for power production.

In order to utilize the energy resources efficiently, the DG units can also be powered by a hybrid generation systems [11]-[12]. Two types of hybrid system are available: (1) combining a high temperature fuel cell and other thermal-related energy sources to increase the system efficiency, (2) incorporating intermittent DG sources and rechargeable DG sources to extract the most available energy. A high-temperature solid-oxide-fuel-cell-gas-turbine system and a PV-wind-fuel-cell system belong to the first type and the second type, respectively.

If DG units are powered by intermittent energy sources only, such as PV or wind, and supply a local load without connecting to the utility grid, it is necessary for DG units to have the storage devices to handle the transient energy demands. These storage devices include batteries, flywheels, super-capacitors, hydrogen, compressed air, pumped-hydroelectric storage and super-conducting magnetic energy storage devices (SMES) [12]-[13].

A typical microgrid system (MG) consists of paralleled distributed generation units, storage systems, and a cluster of loads within a local area [14]-[17]. Microgrids not only have the inherited advantages of DG but also can offer several substantial benefits including: increased reliability from the redundant configuration of paralleled DG units; flexible, cost effective, and energy efficient features by power management and control.

As shown in Fig. 1.1, a microgrid can be operated in both grid-tie and islanding modes. If the grid is present, the microgrid can not only supply power to the local loads but also exchange power with the grid through a solid-state switch. If the grid is abnormal, the microgrid system needs to disconnect from the grid and to keep supporting the critical loads through load sharing schemes. The ability to switch between grid-tie and islanding modes is the key to guarantee uninterrupted power to critical loads within the microgrid.

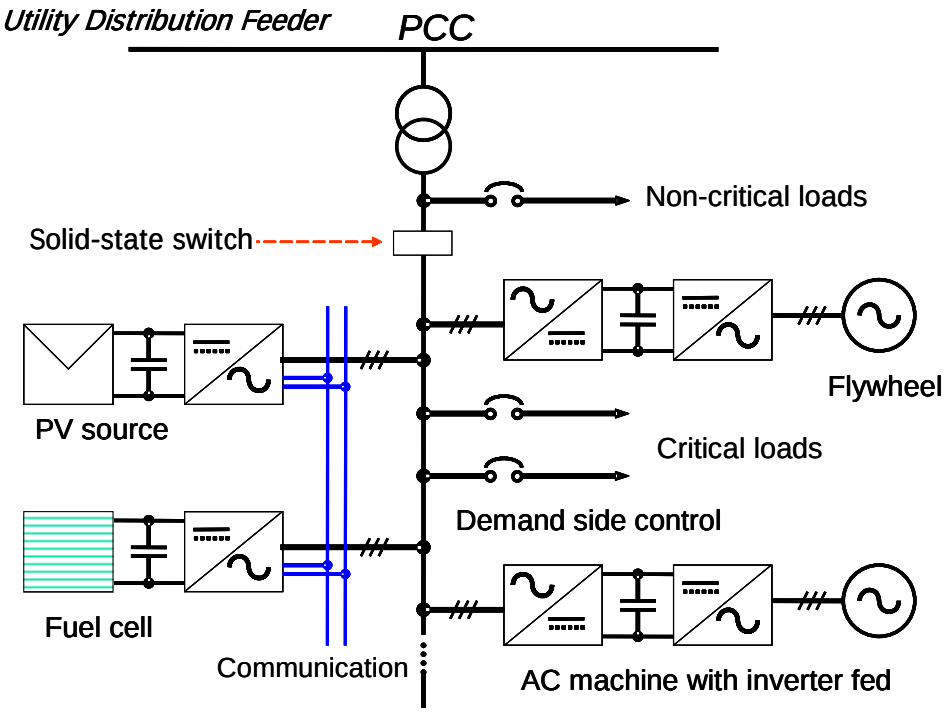


Fig. 1.1. Typical microgrid architecture.

Even though DG units can also be powered by conventional gas-fired engines coupled to rotating generators at 50Hz/60Hz, the major energy sources mentioned above need the power-electronic interface [1] ,[12], [18]-[19] as the bridge connecting to the utility grid due to the different forms of energy sources. DG sources could be dc power (photovoltaic), variable-frequency ac power (wind) or high-frequency ac power (microturbines) while the utility grid is ac 50/60Hz.

Compared to rotational-machine-based DG units, the inverter-based DG units tend to have a faster dynamic; therefore, it can quickly switch between grid-tie and islanding modes. However, it is susceptible to a large switching transient during transition. Unlike the rotational machine based DG units, which normally rely on the droop-control method to balance the voltage and to adjust the current sharing, the inverter allows operating modes to switch between voltage and current modes. On the other hand, the mode changes with a fast dynamic and a low output impedance which tends to produce very large current transients and can easily upset or damage the electronics.

The approaches to paralleling multiple inverters can be found in the design of high power uninterruptible power systems (UPS's). Different current sharing control techniques have been derived from conventional UPS inverter paralleling methods. Although some of these techniques can be employed for paralleling DG units, it should be noticed that the conventional UPS does not need to tie to the grid; and thus the low source impedance and mode transition induced transients do not exist. Another unique problem found in microgrid systems is how to transmit the command signals among inverters separated far apart. Therefore, paralleling microgrid inverters is much more challenging than paralleling UPS inverters.

Major design interests are found in (i) precision power flow control, (ii) proper current sharing, (iii) smooth transition between grid-tie and islanding modes, and (iv) stability analysis.

1.2 Precision power flow control

Once the microgrid system is in grid-tie mode, the injected power quality to the grid is required to comply with the interconnect standards [20]-[22], which leads to the issues of interface (filter) design and controller design.

When connecting a voltage source inverter (VSI) to utility grid, the most common type of filter could be a pure inductor (L) or an inductor-capacitor-inductor (LCL) filter as the inverter output stage to filter the high-frequency harmonic generated by pulse-width switching (PWM). Compared with the L filter, the LCL filter is more attractive because it can not only provides higher harmonics attenuation, but also allow the inverter to operate in both standalone and grid-tie modes, which makes it a universal inverter for the distributed generation applications [23]. Traditional UPS only need to operate in standalone mode in which the filter design is typically an inductor-capacitor (LC) filter [24]-[26]. The grid presents an unknown grid impedance which may cause instability by the dramatic changes of the resonant frequency in grid-tie mode with an LC filter [27], [83]-[84]. Major factors to select LCL value include inductor current ripple, reactive-power consumption in capacitor [28], the range of LCL resonant frequency, and the total inductance value of LCL filter [29]. In [30], the sensor position selection and the universal application for inverter are also included to design the LCL filter.

For single inverter system, many control strategies [31]-[46] have been proposed to achieve the goal of high quality output with precision power controls. Proportional-integral (PI) control is probably the most well-known control scheme in dc-dc converters

[31]-[32]. The controller places a pole at the origin to achieve an infinite gain at zero hertz, which eliminates the steady-state error of dc components. This method, however, does not have a very good tracking performance at 50/60Hz fundamental frequency due to the finite gain at desired frequencies. A proportional resonant (PR) controller [23], [33]-[36], having extremely high gain at the desired frequencies to reduce the steady-state error, is proposed. The infinite gain that is possible in theory for a PR controller is not possible in practice. Another way to solve this steady-state error problem is to use the single-phase d-q frame transformation method [37]-[38]. With the frame transformation, the error signal is regulated in dc quantity by an integrator to achieve infinite gain. This infinite dc gain can then be transformed back to fundamental frequency to eliminate steady-state error. However, all the frame transformations in feedback and control signals must be done within every sampling cycle which needs intensive computational effort.

Deadbeat control is one kind of predictive control which calculates the derivative of control variables to predict the system action [39]-[40]. This controller has very fast theoretical response which makes it suitable for high-band-width applications, such as active filter or motor drive. This method, however, is prone to have stability issue due to model and parameter mismatching. For the nonlinear control schemes, hysteresis control should be the simplest one which changes the switching state whenever the feedback signals exceed the preset bands [40]. This control has the advantage of fast response, inherent current-limit capability and no need of the plant parameters. This control scheme, however, has the variable switching frequency characteristic which makes it hard to design filter, difficult to perform frame transformation, not easy to perform interleaving technique, and could introduce over-heat and electromagnetic interference (EMI) issues. A

hysteresis control with fixed switching frequency by varying the hysteresis band is proposed to overcome this variable frequency issue [41]. The sliding mode control is one kind of variable structure control which modifies the dynamic of a system by applying a high-frequency switching control [42]. This control scheme has many advantages such as fast response, good disturbance rejection and insensitivity to parameter variations. Because the switching of sliding mode control is to force the system trajectory moving along the sliding surface based on the sign of error signal, this control also has the variable frequency issue mentioned in the hysteresis control. In [43], a quasi-sliding mode control is utilized to have a fixed switching frequency on a parallel inverter system so as to apply the interleaving technique to improve the system efficiency.

In grid-tie applications, the load is normally modeled as a constant voltage source in series with the source impedance. Because the grid voltage is known, the way to control the power sending to the grid is to control the inverter output current with current-mode control. On the other hand, most of the standalone loads require the output voltage to be regulated to supply the loads with a desired voltage. Unlike the current control in grid-tie mode which is normally a single current loop control, the voltage control generally be designed in multiple feedback loops to improve the output voltage performance and to damp the poles of LC filter [30], [44]-[45]. With the inner current loop in a multiple control loop, the system can also have inherent peak current protection or overload rejection to protect the system from hardware failure [30], [40].

Beside the feedback controller, the feedforward controller or admittance compensation also shows advantages to the power converter systems [23], [30], [46]. By analyzing the transfer function of the power-factor correction (PFC) converter, the reason

of the steady-state current error was found to be an unwanted current introduced by grid voltage through an undesired admittance path [46]. The admittance path has major impact on the waveform distortion due to its leading phase with respect to the line current. For the grid-tie inverter case, the situation is similar [23], except that the leading phase becomes lagging phase. It is found in [23], [46] that the current distortion can be compensated with a properly designed feed-forward controller which cancels the induced current by the undesirable admittance term. In [30], the admittance compensation concept is also utilized to design the inner current loop in a standalone inverter. The usage of the admittance compensation makes the standalone inverter plant into a first-order system which greatly simplifies the controller design.

1.3 Current sharing in islanding mode

When the grid is not available, a microgrid should form an island to continuously supply the critical load using a proper current-sharing scheme. The current-sharing schemes could be designed with communication line to offer the possibilities of flexible power management to increase the system profits [47]-[49], or without communication line to have higher reliability [24], [50]-[53]. Large inverter-based microgrid systems with ratings higher than 100 kW utilize the traditional frequency and voltage droop control to share loads without communication lines [50]-[51]. However, the load sharing capability of the droop method may be degraded if the load changes, or the line impedance changes. In order to reduce the sensitivity of line impedance unbalance to current-sharing capability and to provide harmonic-current-sharing capability, the virtual impedance concept is utilized to improve the performance of the droop control [24], [52]-[53]. In traditional frequency droop control, the frequency will be changed due to the load change; which, however, is limited by the frequency constraint of utility standard [20]. This limitation confines the allowable frequency droop controller gain and may lead to frequency chattering. An angle droop method is proposed to conduct the load sharing with a very small frequency variation [54].

The use of communication was found in some low-power paralleled inverter systems for instantaneous load balancing control schemes including central-limit [55], master-slave [56], and circular-chain controls [25] to achieve better current sharing capability. In [26], a current-weight-distribution control was proposed to allow inverters in

parallel with different output current capabilities. However, the transmission distance for load current sharing commands is quite limited with the ac signal transmission. In order to extend the transmission distance, a load sharing scheme was proposed to transmit the frequency-decoupled signal through a controller area network (CAN) bus among paralleled inverters [30] or through a low-bandwidth communication [49], [57] in microgrid systems. This transmission scheme substantially helps to extend the transmitting distance without an extremely high bandwidth communication channel.

1.4 Mode transfers between grid-tie and islanding modes

In order to guarantee uninterrupted power to critical loads, the microgrid system needs to have the ability to switch smoothly between grid-tie and islanding mode. For mode transfer between two basic modes, the first step is to determine when the microgrid should operate in grid-tie or islanding mode by islanding detection techniques [58]-[64]. Islanding detection can be classified into passive, active, and communication-based detection schemes [58]. Different active methods including current injection [59], PLL based detection [60], and frequency-drift method [61] are proposed to reduce the non-detection zone. Compared to passive islanding-detection method, active islanding-detection methods has smaller non-detection zone but tend to degrade the power quality by the injected signals. Hybrid islanding-detection methods which incorporate active and passive methods are examined in [62]-[63] to have smaller non-detection zone and less effect on power quality. In [64], the passive islanding detection is investigated under the effect of different load types, including RLC load, constant-power load and constant-current load.

When the grid is in an abnormal condition, the microgrid needs to switch from grid-tie to islanding mode within the required clearing time [20]. In [65], a method is proposed to have inverters generate a voltage difference on the output inductors to facilitate the turn-off process of a static switch, which reduces the disconnect time from grid-tie mode to islanding mode. Once the grid recovers, the microgrid should re-connect back to the utility without harming the system. In order to minimize the transients, the phase-lock

loop (PLL) design and the mode transfer procedure were proposed in [66]-[67]. In [68], a PLL is designed with an orthogonal filter to increase the robustness when grid voltage is distorted or unbalanced. In [23], an admittance compensation is proposed to reduce the transients during the startup of grid connection. By controlling the peak value of the output current with an inner voltage loop, the indirect current control can achieve smooth mode transfers between the two modes [69]. Past studies on microgrid operation typically focused on a single inverter with a single power conditioning system for islanding operation or mode transfers between islanding and grid-tie modes. In [70], the mode transfers are performed in a multiple inverter-based microgrid system that emulates real microgrid system operation.

1.5 Modeling and stability analysis

Due to the larger system uncertainties and the interface design, the inverter-based MG suffers more challenges which call for the needs of stability analysis [27], [71]-[73], [83]-[84]. First of all, the inverter-based DG units have much less over current capability compared to rotation machine based DG units [71] (normally up to 2 times of rated current for less than half a cycle). Second, the intermittent nature of some renewable energy sources such as PV and wind could cause the stability issue in case of a high-penetration system [71]-[72]. Third, the MG has a wide-band dynamic due to the presence of fast response of electronically-interfaced DG units and multiple small DG units with different power capability [73]. Fourth, a large grid impedance variation within the MG system may induce oscillations or instability [27], [83]-[84]. Due to the presence of these challenges, there is a strong need for stability analysis to guarantee proper and stable system operations.

The stability of a single inverter can be determined by Bode plots using the phase margin and gain margin as the stability criteria. In single LCL grid-tie inverter systems, Bode plots were used to study the effects of changing feedback scheme [74], controller gain [34], [75], plant parameter [27], [52], [74]-[75], and discretization method [76]. This method, however, cannot determine the stability of whole parallel-inverter system due to the possible interactions among different control loops and the current-sharing controller. The stability of cascaded systems like input filter design of a converter [77] and the dc-bus capacitor of a constant-power motor drive system are analyzed by the impedance criteria

[78]. This method determines the stability by analyzing the impedance characteristic of input ports and output ports. The impedance criteria also can be extended to analyze stability of dc paralleled power converters [79]-[80] and paralleled ac inverter systems [81]-[82]. This method, however, may not be appropriate for large systems because many subsystems may interact with each other, making the impedance criteria complicated due to too many input and output ports.

The system stability can also be determined by analyzing the system pole and zero locations using the eigenvalue analysis. With the state-space analysis, the single inverter systems studied the stability of changing the controller gain [34], [74]-[75], [87], [94], the plant parameter [27], [83]-[85], the sampling frequency [29], [86], and different feedback signal [76], [86]-[87]. Also, the state-space analysis is usually adopted to investigate the LCL filter resonance issue of grid-tie inverter systems with the passive damping methods [29], [74], [87] and active damping techniques [27], [74], [76], [86]-[87].

The stability of large-scale distributed generation systems with droop control is also usually being analyzed by the state-space model. The system stability was studied by changing the load type [88], the droop controller gain [54], [57], [73], [85], [89], and the output power [51], [73], [90]. This model is relatively easy to expand by combining single inverter state-space equations to build state-space equations for parallel inverters. In [91], the study of a 69-bus distribution system shows the flexibility and simplicity of the state-space analysis to change the system dimension.

Some studies have been conducted to analyze the stability of droop control methods and instantaneous active current-sharing control methods for a paralleled inverter system. However, the stability of a parallel system using the average-current sharing control with

low bandwidth communication is rarely addressed. In [92], the state-space model is adopted to investigate the stability of the paralleled inverter system with a low-bandwidth-communication current-sharing scheme. Even though the state-space tool is already widely used in other applications, it is worth to investigate stability of a newly built system using an existing tool. The control variables described in previous stability analysis papers such as controller gain, feedback signal, sampling frequency, output power and load type can be used as system variations to investigate the stability of the newly built microgrid system. Once the state-space model is constructed, many modern controller design techniques, such as pole assignment [75], [93]-[94], eigenvalue sensitivity [89]-[90], model-predictive control [95], and sliding-mode control [42]-[43] can be utilized to further optimize the system.

1.6 Research motivations and objectives

Previous studies have given solutions to inverters in either grid-tie mode or standalone mode, but rarely mentioned the inverter design in both operation modes. However, it is necessary for a microgrid application that both basic operation modes need to be considered which calls for a universal inverter design.

Prior arts of grid-tie inverter utilize PR controllers or d-q frame controllers to minimize the steady-state error, but not many studies focus on the connecting transient of a single inverter unit. In a microgird system which every single unit is closer to each other than traditional utility generators which may lead to larger interactions among every single unit. If only using the PR controller in the grid-tie mode, the inverter unit will still encounter the reverse power flow in the first-cycle grid-tie connection and may cause system failure. This negative power flow issue during the grid-tie connection transient requests the admittance compensation.

Traditional UPS systems transmit the control signals in ac format which may not transmit to a long distance due to the bandwidth limitation. Droop control is widely applied in large-scale power systems but may have the line-impedance-dependent sharing issue and may not optimize the system's fuel efficiency if communication is not existed. The transmission distance issue in UPS system and need of communication in droop method calls for a frequency-decoupled transmission scheme among DG units in a small-scale microgrid system.

Most early studies of mode transfers between grid-tie mode and islanding mode only focus on the transfers of a single-inverter system. This may not be enough in the real world case which a microgrid system is consisted of several small parallel DGs. It will be

meaningful to investigate the study behavior of the mode transfers in a parallel-inverter microgrid system.

Given that many challenges are presented in the inverter-based microgrid systems, it is imperative to study the stability of the designed parallel-inverter microgrid system under different plant variations and system disturbances. Even though the tool used in this study is well known, it is also worth to study the newly developed multi-inverter system with a popular means. Because of the simplicity of the state-space analysis to change the system dimension, it is a suitable measure to study the stability of a large-scale system like the proposed parallel-inverter microgrid system.

With the above research motivations, the research objectives can be summarized:

1. To design and build a single universal inverter that can operate in both grid-tie and standalone mode.
2. To solve the reverse power flow issue by admittance compensation.
3. To fulfill a parallel-inverter microgrid system using frequency-decoupled signal to extend the transmission distance of communication channel.
4. To implement a parallel-inverter microgrid with smooth mode transfer capability.
5. To study the stability of the newly built parallel-inverter microgrid system.

1.7 Dissertation outline

This dissertation aims to develop a reliable microgrid system. The study will cover from a single unit in different modes to multiple units operation with the ability to perform mode transfers. Finally, the stability of whole system will be studied to help the controller design and ensure system reliability under different variations. The following chapters are organized as below.

In chapter 2, the inductor-capacitor-inductor (LCL) filter design considerations and the controller designs of a single inverter in both grid-tie and standalone modes are discussed. For grid-tie mode controller design, a single-loop current controller is designed with proportional-resonant controller to reduce the steady-state error and the admittance compensation to reduce the start-up transients. For standalone operation, a dual-loop control system with PR-controller for outer voltage loop and a P-controlled for inner current loop is proposed to limit peak current magnitude under transient, enhance voltage loop stability, and reduce voltage steady-state error.

In chapter 3, accurate current sharing and smooth mode transfers are performed in a multi-inverter based microgrid system by the designed system-level controls with controller-area network (CAN) communication. Controller designs of individual inverters in chapter 2 are adopted to perform the basic microgrid operations. The mode transfer tests are conducted with an inverter-simulated grid to define the proper transfer procedures to guarantee an uninterrupted power supply to the critical loads within the microgrid.

In chapter 4, the state-space model and implementation results of a power conditioning system are presented. Eigenvalues with different controller gains and load conditions for gird-tie mode and standalone mode are found to analyze the system stability.

The state-space model is extended to a parallel-inverter system to investigate the effect of current-sharing controller design to the stability.

Chapter 5 provides the conclusions of this dissertation and some suggestions for future works.

Chapter 2

Single Universal Inverter with Both Grid-tie and Standalone Operations

2.1 Introduction

Inverter is the basic power interface between DG and utility grid which is the key element for a reliable microgrid system. In this chapter, we will cover the analysis and design of a single-phase universal inverter system including admittance compensation, inductor-capacitor-inductor (LCL) filter, single-loop proportional-resonant (PR) current controller, dual-loop voltage controller and the phase-lock loop design.

First of all, the current loop transfer function of a single-phase grid-tie inverter will be systematically derived with representations of conventional transfer function format using admittance terms for controller design and loop compensation. With the analysis, the issue of the undesirable admittance term will be addressed. The LCL filter is normally used in a grid-tie system to allow a higher current ripple attenuation. Here, the LCL filter is designed so that it also enables the universal outputs in which an inverter can operate in both grid-tie and standalone modes. The LCL filter design considerations including sensor

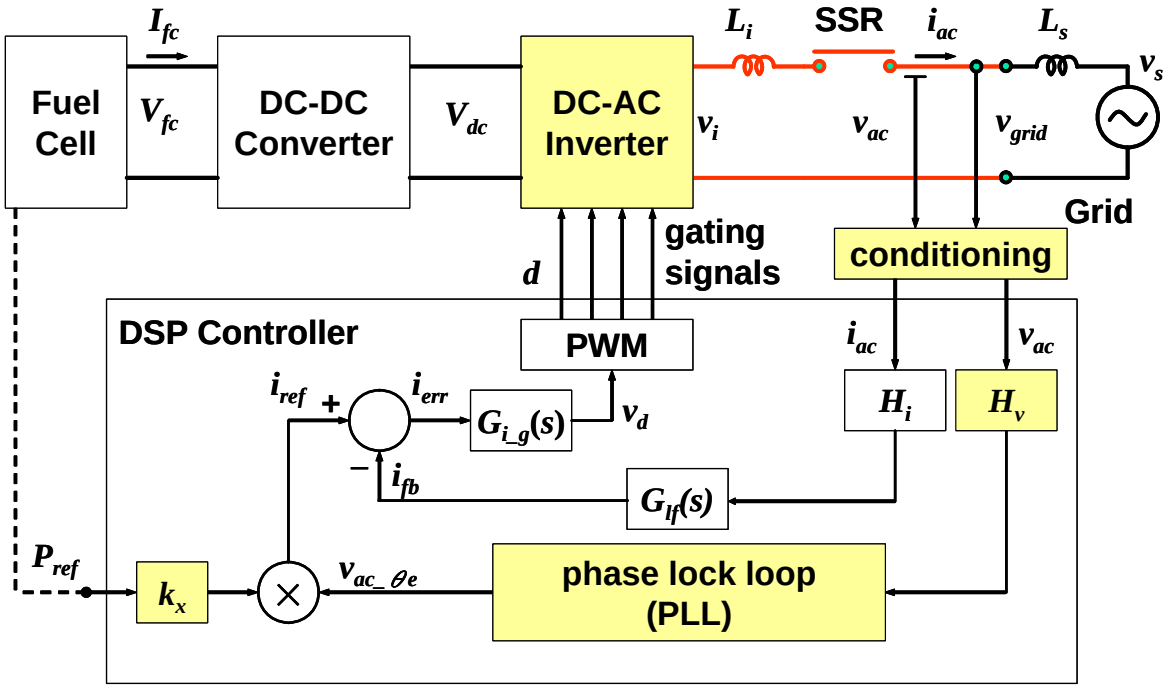
position selection and component selections are discussed.

With the LCL hardware design and admittance compensation, the grid-tie current controller and the standalone voltage loop controller are designed to allow the accurate power flow control for the microgrid system. For grid-tie mode operation, inverter is operating under a single current loop with proportional-resonant controller and admittance path compensation to reduce the steady-state error by providing a high gain at the fundamental frequency. For standalone mode operation, the inverter is implemented with a dual-loop controller to regulate the output voltage and allow the current sharing capability. Finally, in order to connect to the utility grid, a stable phase synchronization mechanism is imperative. The phase-lock loop (PLL) using d-q transformation will also be addressed in this chapter to perform the phase synchronization. Because the band-pass filter feature of the PLL, the output of PLL also serves as the input of the admittance compensation loop to avoid the dc offset and high-frequency noise induced in the feedback network.

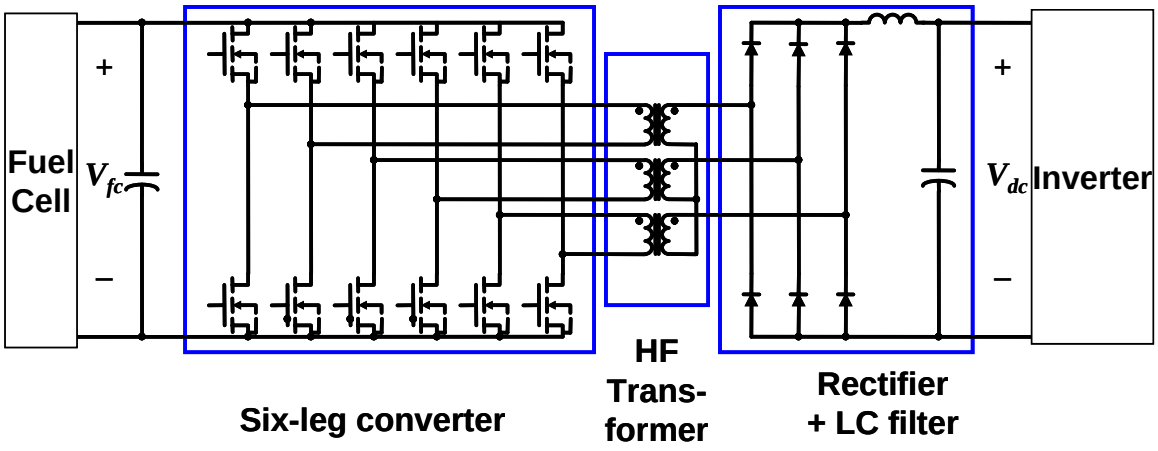
2.2 Grid-tie inverter control system modeling

Fig. 2.1(a) shows the control system of the L-based-filter fuel-cell inverter system. Because the fuel cell input voltage V_{fc} is normally low and unregulated, a dc-dc converter is required before the inverter stage. Utility grid is normally modeled as a constant voltage source v_s in series with a source impedance L_s. The inverter is connected to the grid through an inverter-side inductor L_i and a solid-state relay (SSR). In grid-tie applications, the way to control the power transfer to the grid is to control the inverter output current with current-mode control because the grid voltage is known. The inductor current i_{ac} is sensed because it needs to be controlled though a current controller. The voltage v_{ac} is sensed and feed into the PLL to be utilized as the phase information of the current reference i_{ref}. The magnitude of i_{ref} is generated proportional to the P_{ref} which is the command from the fuel cell balance-of plant (BOP) controller.

Fig. 2.1(b) shows the 6-leg (V6) dc-dc converter circuit topology used in this system [96]. The dc-dc converter consists of a six-leg converter, high-freq transformer, rectifier and a LC filter. 2.1(c) shows the inverter circuit topology which includes a full-bridge inverter and a LCL filter. A large dc-bus electrolytic capacitor bank is used to decouple the dynamic between the V6 converter and full-bridge inverter.

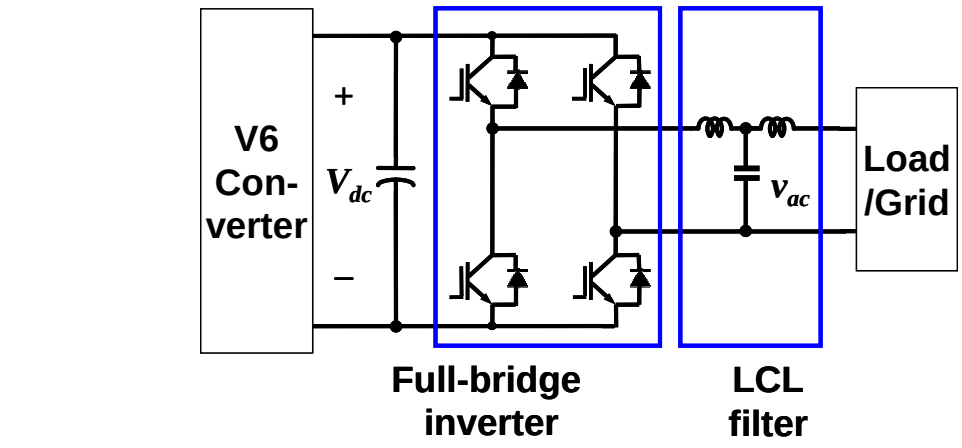


(a)

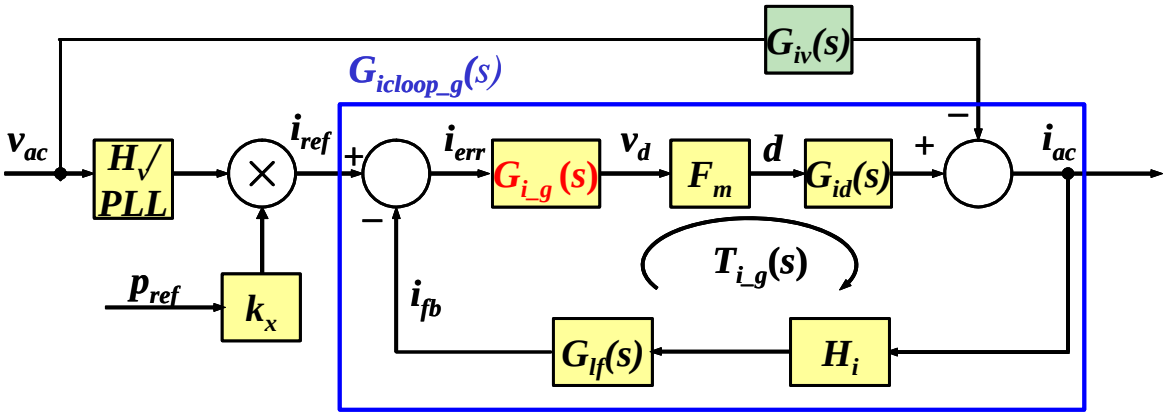


(b)

Fig. 2.1. (a) Inverter control system of a L-filter-based fuel cell PCS, and (b) V6 dc-dc converter circuit topology.



(c)



(d)

Fig. 2.1. (c) full-bridge inverter circuit topology, and (d) inverter control diagram using transfer functions.

Fig. 2.1(d) represents the inverter control diagram using transfer function blocks: G_{iv} and $G_{id}(s)$ – power stage transfer functions, $G_{i\_g}(s)$ – current loop compensator in grid-tie mode, F_m – PWM gain, H_i – current sensor gain, $G_{lf}(s)$ – hardware low-pass filters and k_x – current reference gain. Using the average inverter output voltage v_i which equals dV_{dc}, the current-loop transfer function blocks can be derived in (2.1).

$$i_{ac} = G_{id}(s)d - G_{iv}(s)v_{ac} \tag{2.1}$$

where $G_{id}(s) = \dfrac{V_{dc}}{r_{Li} + sL_i}$, $G_{iv}(s) = \dfrac{1}{r_{Li} + sL_i}$

The overall equivalent admittance can be represented in (2.2).

$$\begin{aligned} Y(s) &= \frac{i_{ac}(s)}{v_{ac}(s)} \\ &= \frac{G_{id}(s)F_m G_{i\_g}(s)}{1 + T_{i\_g}(s)} k_x P_{ref} H_v - \frac{G_{iv}(s)}{1 + T_{i\_g}(s)} \\ &= G_{icloop}(s) \cdot k_x P_{ref} H_v - G_{ivcloop}(s) \end{aligned} \tag{2.2}$$

where $T_{i\_g}(s) = H_i G_{lf}(s) G_{i\_g}(s) F_m G_{id}(s)$, $G_{icloop}(s) = \dfrac{G_{i\_g}(s)F_m G_{id}(s)}{1 + T_{i\_g}(s)}$

Defining $Y(s) = Y_1(s) + Y_2(s)$ yields $Y_1(s) = G_{icloop}(s) k_x P_{ref} H_v$, and $Y_2(s) = -G_{ivcloop}(s)$. The first admittance term, Y_1, is the power command P_{ref} generated term, which provides the desired output generated by the inverter. The second admittance term, Y_2, is the closed-loop transfer function from v_{ac} to i_{ac}, calculated by assuming that the inverter output voltage v_i equals zero and the SSR is connected.

Note that the current induced in the Y_2 path needs to be multiplied with v_{ac}, thus the resulting current will be rather large, which is noticeable even at the maximum power command condition. At the low power command, the current induced in Y_2 will eventually exceed that in Y_1, which means the impact is very significant. Because the current in Y_2 path reduces the desired current, the resulting steady state output will be less than the command input, and the situation worsens at the lighter load conditions.

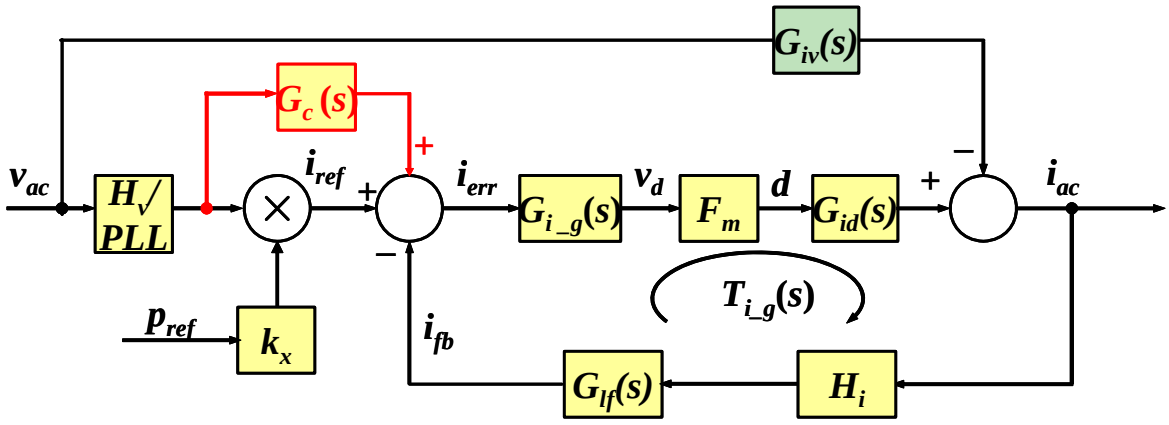
2.3 Admittance compensation

By observing the expression of *Y(s)*, the undesired admittance effect can be eliminated by adding one component, which is totally opposed to the first term in (2.2). As shown in Fig. 2.2(a) and Fig. 2.2(b), two possibilities to cancel the undesired admittance term can be observed. In Fig. 2.2(a), the admittance compensator is added at the summing junction before the current loop compensator. The compensator transfer function can be derived in (2.3).

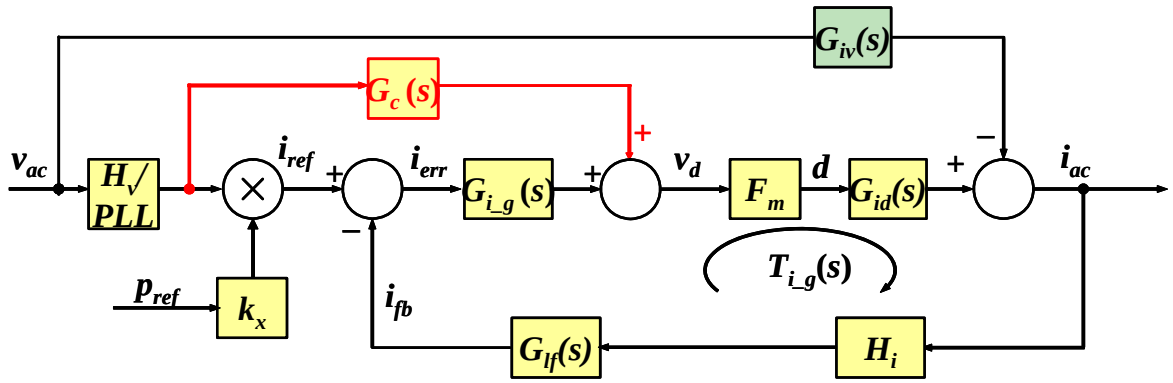
$$G_c(s) = -Y_2(s)\frac{1}{H_v G_{icloop}(s)} = \frac{1}{H_v V_{dc} F_m G_{i\_g}(s)} \tag{2.3}$$

The above derivation assumes the overall loop gain has sufficient gain at low frequencies (50 or 60 Hz), which is needed to lower the steady-state error. In Fig. 2.2(b), the admittance compensator is added after the current loop compensator, which can be expressed in (2.4).

$$G_c(s) = -Y_2(s)\frac{1}{H_v G_{icloop}(s) G_{i\_g}(s)} = \frac{1}{H_v V_{dc} F_m} \tag{2.4}$$



(a)



(b)

Fig. 2.2. (a) Current reference correction method, and (b) admittance compensation method.

The proposed admittance compensation technique can be considered as a voltage feedforward control. By rearranging the voltage sources from the plant, the equivalent control block diagram can be shown in Fig. 2.3 (a) and (b). Here v_{ac} is the voltage source from the grid. The voltage-source inverter can be considered to have two parts of the output voltages: feedback output voltage v_{FB} and the lagging-phase-admittance-compensation (LPAC) output voltage $v_{LPAC.}$ Applying the super-position theory, the effective voltage v_{eff} generating the current i_{ac} is the combination of these two voltages. Different from the conventional feedforward control, the gain of this admittance compensation is well defined and can effectively cancel the source voltage effect. The block diagram in Fig. 2.3(a) clearly indicates the voltage cancellation effect between v_{ac} and v_{LPAC} terms. The resulting equivalent circuit can be shown in Fig. 2.3(c). With this control method, the grid-tie connection can be controlled as a pure inductive load with the conventional feedback or PR control technique.

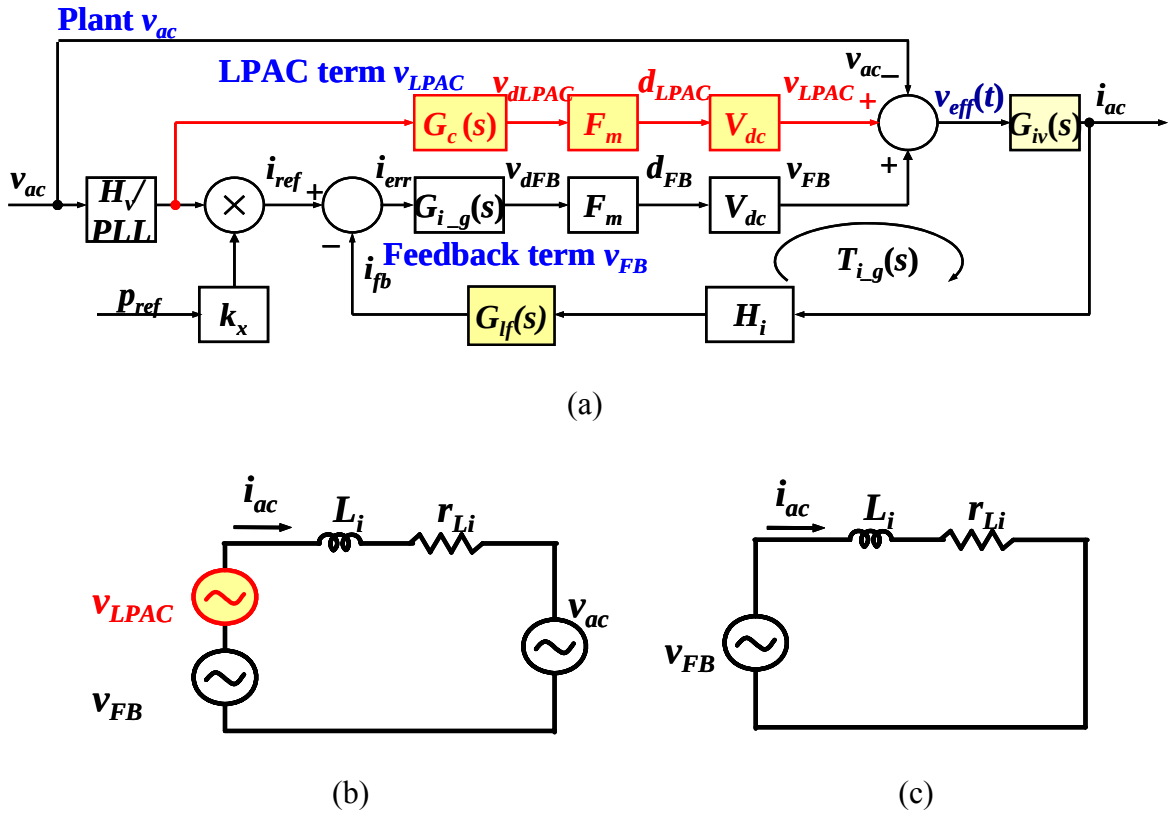
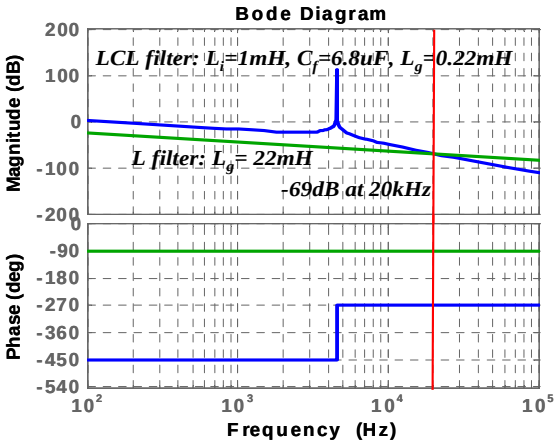


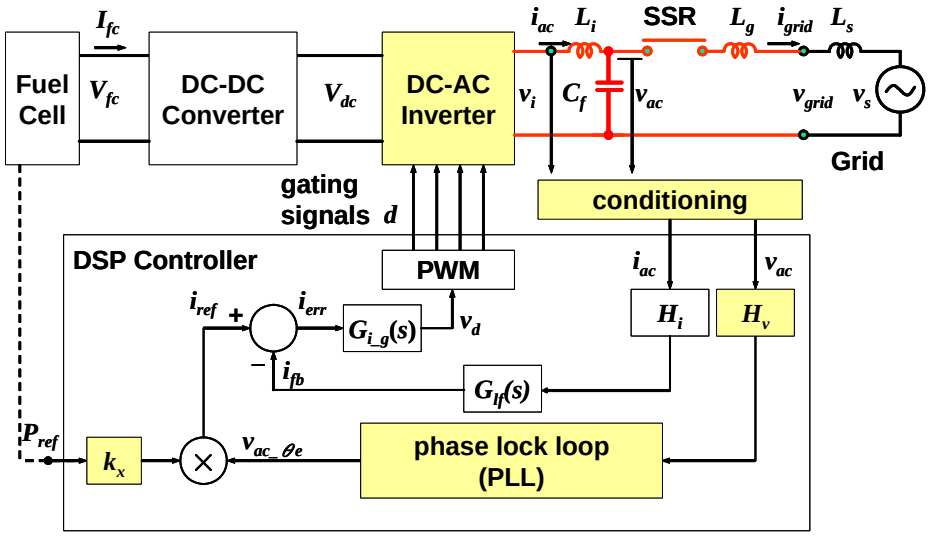
Fig. 2.3. (a) Equivalent control block diagram for a grid-tie inverter, (b) power circuit diagram for a grid-tie inverter, and (c) power circuit diagram for a grid-tie inverter with admittance compensation.

2.4 LCL filter design for universal inverter

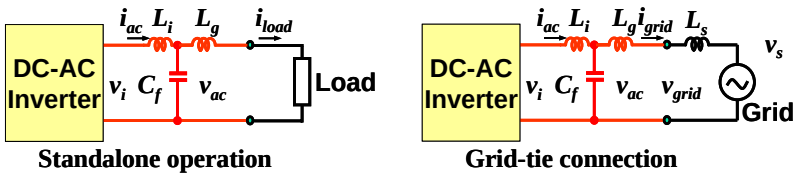
In the grid-tie inverter applications, the interconnect standard IEEE 1547 [20] suggests the injected current quality standard from distributed generation (DG) to utility grid. Small-capacity grid-tie inverter usually utilizes L-type filter for its simplicity. In a large system, however, such simple L-type filter is bulky and costly due to the large current capability. Compared to L type filter, the same amount of switching ripple reduction can be achieved with smaller bulky inductors by the LCL filter, shown in Fig. 2.4(a). As shown in Fig. 2.4 (b), the LCL filter configuration also allows the inverter to operate as a universal inverter. With the configuration shown in Fig. 2.4(c), the inverter output is a standalone load. With the configuration shown in Fig. 2.4(d), the output can be sent to the utility grid by engaging the SSR. In summary, compared to the L-filter-based inverter, the LCL filter configuration allows more flexible inverter usage and also provides more attenuation of switching ripple. However, it is more complicated when using the LCL filter; many design considerations, like sensor-location selections and component selections need to be taken into account.



(a)



(b)



(c) (d)

Fig. 2.4. (a) L and LCL filter to achieve same ripple attenuation, (b) system block diagram of a universal inverter using LCL filter, (c) standalone mode, and (d) utility grid-tie mode.

For the sensor-location selections, the grid-side voltage v_g, the capacitor voltage v_{ac} and the inverter-side-inductor current i_{ac} are selected as feedback signals in our LCL grid-tie inverter system. First of all, v_g needs to be sensed for voltage synchronization in grid-tie operations. Next, v_{ac} needs to be sensed to regulate output voltage in standalone mode operations. In addition, by selecting the v_{ac} and inverter-side-inductor current i_{ac} as feedback signals instead of v_g or grid-side inductor current i_g, the duty-cycle-to-output-current transfer function in grid-tie mode will be a first-order system which will greatly simplify the controller design [23]. Furthermore, compared to the current sensor signal i_g, feedback of current i_{ac} not only allows the sensor to be easily integrated into the inverter but also reduces the noise in the sensor conditioning circuit because the physical sensor location is closer to the controller board.

The LCL component value selection issues are described as following. First, the selection of the inverter-side inductor L_i should compromise the output current performance, system cost, size, and efficiency. For example, with a higher L_i value, lower current ripple can be obtained and a higher controller gain can be designed to obtain better current performance. However, a higher inductance value requires higher cost and occupies larger volume. For the efficiency concern, higher inductance allows lower current ripple in the inductor L_i, which decreases core losses of the inductor. On the other hand, higher inductance value increases the winding loss for longer wire required.

The selection of capacitor value depends on the application of inverters. If the inverters are implemented for only grid-tie applications, the selection of C_f can be determined by limiting the reactive power consumed in C_f [28]. On the other hand, in the design of universal inverters, the selection of the filter capacitor will be determined by the

required voltage ripple damping because the inverter-side inductor L_i and the filter capacitor C_f will form a second-order filter that provides a -40dB/dec attenuation after the resonant frequency of this L_i-C_f filter.

Finally, the criteria to select grid-side inductance L_g is described as following. For the grid-tie inverter shown in Fig. 2.4(c), the transfer function from duty cycle d to i_{ac} without admittance compensation can be derived in (2.5).

$$G_{id}(s) = \frac{\left[1 + s^2(L_g + L_s)C_f\right]V_{dc}}{s\left[L_i + (L_g + L_s)\right]\left\{1 + s^2\left[\frac{L_i\left(L_g + L_s\right)}{L_i + \left(L_g + L_s\right)}\right]C_f\right\}} \tag{2.5}$$

Comparing the $G_{id}(s)$ in (2.5) to that in (2.1), the denominator of (2.5) has two more resonant poles that may cause the stability issues. In [29], this resonant frequency needs to be limited neither close to the current cross-over frequency nor close to the switching frequency to avoid LCL resonance. After L_i and C_f are determined, L_g needs to be selected so that the resonant frequency is in a proper frequency range to ensure the stability.

Fig. 2.5 shows the block diagram of the complete LCL-filter based inverter control system, which resembles Fig. 2.2(b) except that a third admittance loop is added through the filter capacitor, i.e., sC_f. In a typical power circuit design, capacitor C_f is in the order of μF range, and the added 60-Hz current is in mA range. Thus, a small added leading phase current of this capacitor loop is negligible and will not affect the first-order control system.

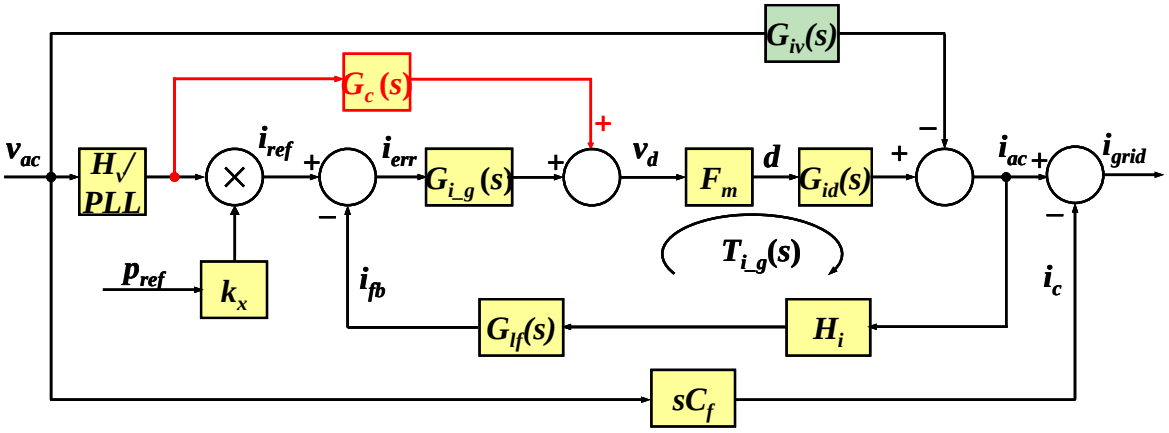


Fig. 2.5. Block diagram of the complete admittance compensated LCL-filter based grid-tie inverter.

2.5 Current proportional-resonant controller design in grid-tie inverter

The control object in grid-tie operation is its output current because the output voltage is already determined by the grid. The control system shown in Fig. 2.4 (b) employs the voltage across the filtering capacitor, v_{ac} and the current of the inverter-side inductor, i_{ac} as the feedback signals. Such an arrangement allows a simple first-order plant model $G_{id}(s)$ shown in (2.1) be utilized in the controller design. The open current loop gain $G_{ioloop}(s)$ is defined in (2.6).

$$G_{ioloop}(s) = F_m * G_{id}(s) * H_i * G_{lf}(s) \tag{2.6}$$

where $G_{lf}(s) = \dfrac{\omega_{HWF}^{\ 2}}{(s+\omega_{HWF})^2} * \dfrac{\omega_{ANF}}{(s+\omega_{ANF})}$

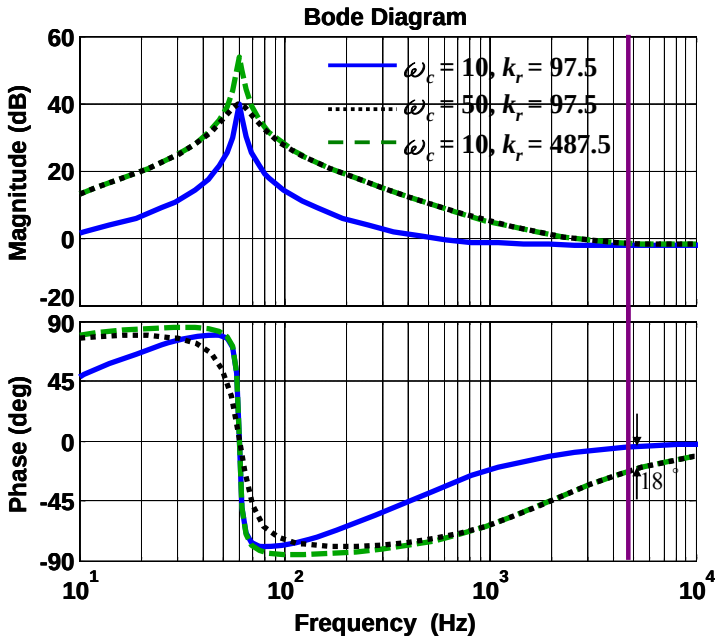
Here $G_{lf}(s)$ is the transfer function of hardware low-pass filters which includes a second-order low-pass filter at 48 kHz and a first-order anti-aliasing filter at 9.6 kHz. By choosing a proportional-resonant (PR) controller to reduce the steady-state error [23], [33]-[36] the compensated loop gain in grid-tie mode $T_{i\_g}(s)$ can be represented in (2.7). The PR controller uses proportional gain to adjust the gain for all-frequency signals and resonant gain provides the desirable gain at specific frequency by two complex poles.

$$T_{i\_g}(s) = G_{i\_g}(s) * G_{ioloop}(s) \tag{2.7}$$

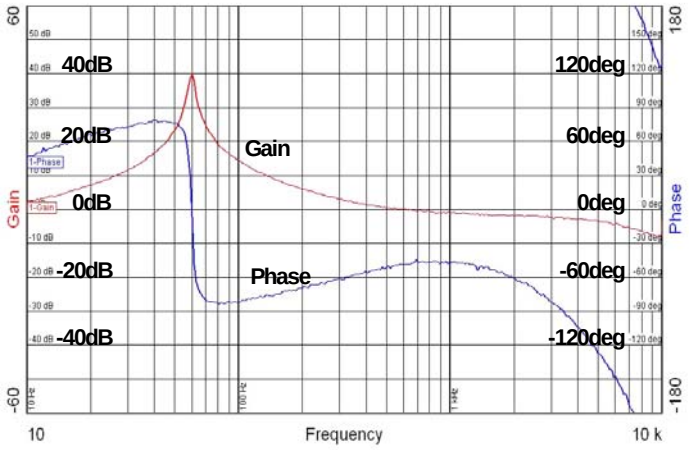
where $G_{i\_g}(s) = k_p + \dfrac{2\omega_c k_r s}{s^2 + 2\omega_c s + \omega_1^{\ 2}}$

Here k_p, k_r, ω_c, and ω_1 are the proportional gain, resonant gain, equivalent bandwidth, and fundamental angular frequency, respectively. In principle, the bandwidth ω_c needs to be as small as possible, but for digital implementation, it is quite difficult to realize a very small ω_c. A large ω_c, however, will introduce a phase lag and thus decrease the phase margin. As shown in the Fig. 2.6(a), comparing $\omega_c = 50$ with $\omega_c = 10$ lines, the phase delay is increased by 18° at where the magnitudes converge. Equation (2.7) indicates that the controller gain at fundamental frequency can be increased by increasing either k_p or k_r values. However, the k_p gain can not too high because it boosts the gain at all frequencies and will drop system gain margin. As shown in the Fig. 2.6(a), the k_r gain also cannot be too high because it will reduce the phase margin at the desired cross-over frequency.

Another critical issue regarding PR controller implementation is its high sensitivity to the controller parameter accuracy due to the sharp resonant peak at fundamental frequency. A small parameter offset will make large different in the real implementation which is even more severe in a fixed-point DSP because it has limited accuracy to display a number. This requires the designed PR controller to be measured before real implementation into a grid-tie inverter system. With TMS320F2808 DSP, the designed PR controller has been measured with a frequency response analyzer as shown in Fig. 2.6(b). The measured gain and phase results agree with the trend of the simulated frequency response below the current-loop crossover frequency. For the system under test, ω_{HWF} = 301.59k rad/s, ω_{ANF} = 60.32k rad/s, V_{dc} = 420 V, r_{Li} = 80 mΩ, and L_i = 1 mH. By choosing $k_p = 0.78$, $k_r = 97.5$, $\omega_c = 10$ rad/s, and $\omega_1 = 377$ rad/s in $G_{i\_g}(s)$; the Bode plots of $G_{ioloop}(s)$ and $T_{i\_g}(s)$ can be shown in Fig. 2.7.



(a)



(b)

Fig. 2.6. Designed controller: (a) simulation results with different ω_c and k_r values, and (b) frequency response measurement with k_p = 0.78, ω_c = 10, k_r = 97.5.

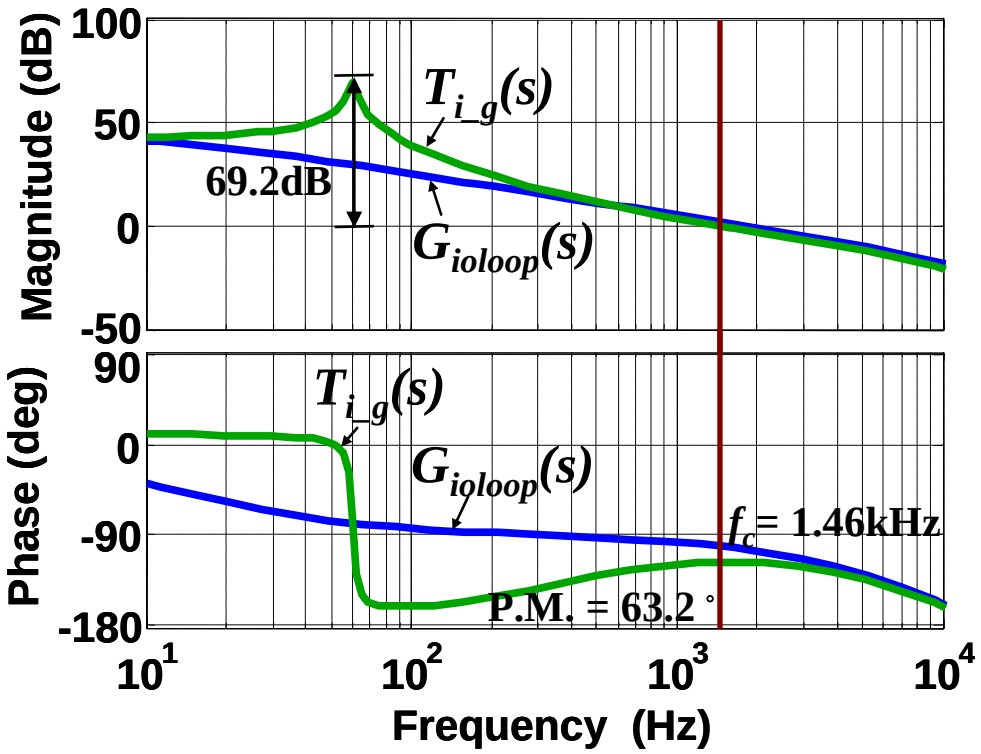


Fig. 2.7. Current loop gain plot showing crossover frequency of 1.46kHz and phase margin of 63.2°.

2.6 Voltage dual-loop controller design in standalone inverter

In standalone mode, most loads require the output voltage to be regulated within a desired voltage range. As shown in Fig. 2.8, this voltage regulation of inverter is controlled in a dual-loop voltage control to ensure system safety and allow the possibility for future current sharing [30], [44]-[45]. In this dual-loop controller, a current inner loop damps the LC resonance pole while a voltage outer loop regulates the output voltage.

Because of the same inverter hardware setup, the current open loop transfer function $G_{ioloop}(s)$ is the same as that shown in (2.6). However, the design goal of the current loop in a dual-loop control is to have a high loop bandwidth with enough stability margin rather than to reduce the current steady-state error by providing a high gain at fundamental frequency. With the first-order loop transfer function $G_{ioloop}(s)$, this current controller is only a simple proportional gain with a software low-pass filter shown in (2.8).

$$G_{i\_s}(s) = 0.5\frac{\omega_{SWF}}{(s+\omega_{SWF})} \tag{2.8}$$

Even though the control system does not contain any resonant poles by carefully selecting the sensor positions, the LCL filter hardware does contain resonant poles that could cause resonance on output voltage and current, as indicated in (2.5). The LCL parameters are L_i = 1 mH, C_f = 6.8 μF, L_g = 0.22 mH which results in a resonant frequency at 4.54 kHz. Thus a 1.5 kHz software first-order low-pass filter is designed to damp possible oscillations at outputs. With the designed current controller, the compensated

current loop gain in standalone mode $T_{i\_s}(s)$ is shown in (2.9). The Bode plots of $T_{i\_s}(s)$ and $G_{ioloop}(s)$ can be shown in Fig. 2.9(a).

$$T_{i\_s}(s) = G_{i\_s}(s) * G_{ioloop}(s) \tag{2.9}$$

After closing the inner current loop, the outer open voltage loop gain can be expressed in (2.10).

$$G_{voloop}(s) = G_{icloop\_s}(s) G_{vi}(s) H_v G_{lf}(s) \tag{2.10}$$

where $G_{icloop\_s}(s) = \dfrac{G_{i\_s}(s) \cdot F_m \cdot G_{id}(s)}{1 + T_{i\_s}(s)}$

Here H_v is the voltage sensor feedback gain, which is 5.12 in the test case. $G_{icloop\_s}(s)$ and $G_{vi}(s)$ are the current closed loop gain and output current to output voltage transfer function, respectively. Assume that the load is a pure resistive load with a R_o value in Fig. 2.4(c), the output current to output voltage transfer function $G_{vi}(s)$ can be represented in (2.11).

$$\begin{aligned} G_{vi}(s) &= \frac{L_g\left(s + \omega_{z1}\right)}{L_g * C_f * \left(s + \omega_{p_1}\right)\left(s + \omega_{p_2}\right)} \\ \omega_{z1} &= \frac{R_o}{L_g}, \quad \omega_{p1}, \omega_{p_2} = -\left[\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}\right], \\ a &= 1, \quad b = \frac{R_o}{L_g}, \quad c = \frac{1}{L_g C_f} \end{aligned} \tag{2.11}$$

The design goal of a dual-loop voltage controller is to obtain a high gain at the fundamental frequency while providing enough bandwidth and stability margin. As shown in (2.12), a PR controller is adopted here to eliminate the steady-state error by providing a high gain at the fundamental frequency.

$$G_v(s) = k_p + \frac{2\omega_c k_r s}{s^2 + 2\omega_c s + \omega_1^2} \tag{2.12}$$

With 20% load as the design plant, a PR controller is designed to have k_p = 0.02, k_r = 12, ω_c = 10 rad/s, and ω_1 = 377 rad/s. The resulting Bode plots of the compensated voltage loop gain $T_v(s) = G_v(s) \cdot G_{voloop}(s)$ along with the uncompensated voltage loop gain $G_{voloop}(s)$ are shown in Fig. 2.9(b).

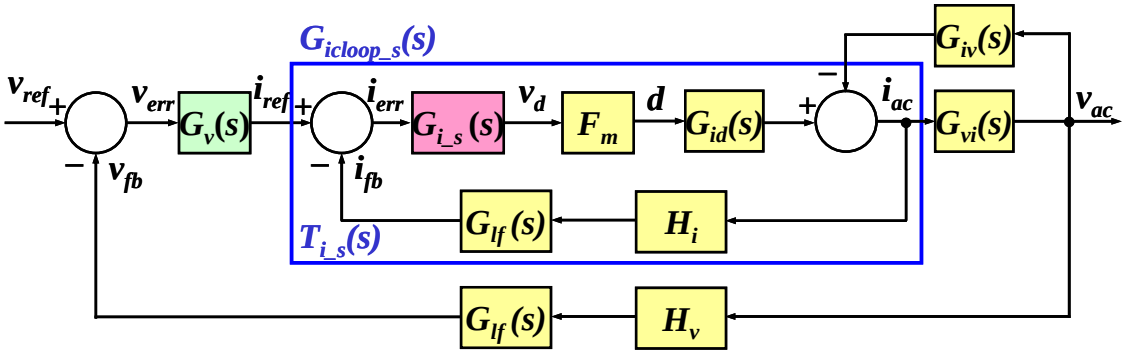
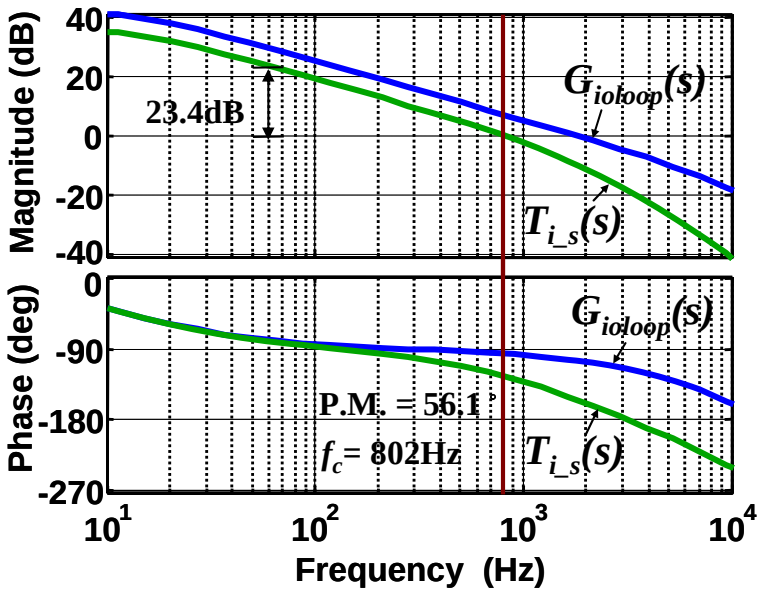
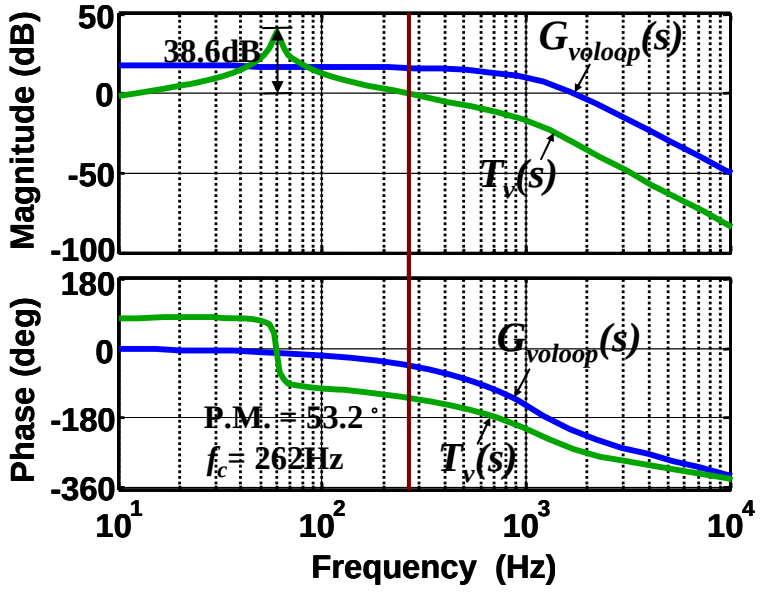


Fig. 2.8. Control block diagram of a voltage dual-loop controlled inverter.



(a)



(b)

Fig. 2.9. The Bode plots of voltage controller designs (a) current loop results, and (b) voltage loop results.

2.7 Phase-lock loop for synchronization

As shown in Fig. 2.10, a PLL block with the peak-value calculation (PC) is designed using an all-pass filter and D-Q transformation. The d-axis and q-axis components are calculated by the estimated angle, θ_e, and filter capacitor voltage, v_{ac}, and output of all-pass filter, v_{acap} as shown in (2.13).

$$\begin{bmatrix} v_{dpll} \\ v_{qpll} \end{bmatrix} = \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} v_{ac} \\ v_{acap} \end{bmatrix} = \begin{bmatrix} 0 \\ -V_m \end{bmatrix} \text{if } \theta_e = \theta \tag{2.13}$$

where $v_{ac} = V_m \sin\theta,\ v_{acap} = \dfrac{\omega_1 - s}{\omega_1 + s} v_{ac} = -V_m \cos\theta,\ v_{dpll} = -V_m \sin(\theta_e - \theta) \cong V_m(\theta - \theta_e)$

The output of the PLL/PC block is the synchronized term v_{ac_syn} which is obtained by multiplying the calculated magnitude v_{qf} term and synchronized unity sine term $v_{ac\_\theta e}$. Since the synchronized term v_{ac_syn} will be used for the admittance compensation, a ripple-free magnitude v_{af} is desirable to ensure smooth operations. A low-pass filter shown in (2.14) can be designed to damp the double-fundamental-frequency ripple caused by (2.13).

$$v_{qf} = -\frac{\omega_{pc}}{s + \omega_{pc}} v_{qpll} \tag{2.14}$$

Here ω_{pc} is the cut-off frequency of the peak-value-calculation filter. Notice that equation (2.14) is a low-pass filter with a negative sign which makes the state variable v_{qf} in steady state equal to the positive voltage magnitude, V_m. In order to design a universal PLL with wide input voltage range, the normalized signal v_{dnom} is utilized as the feedback

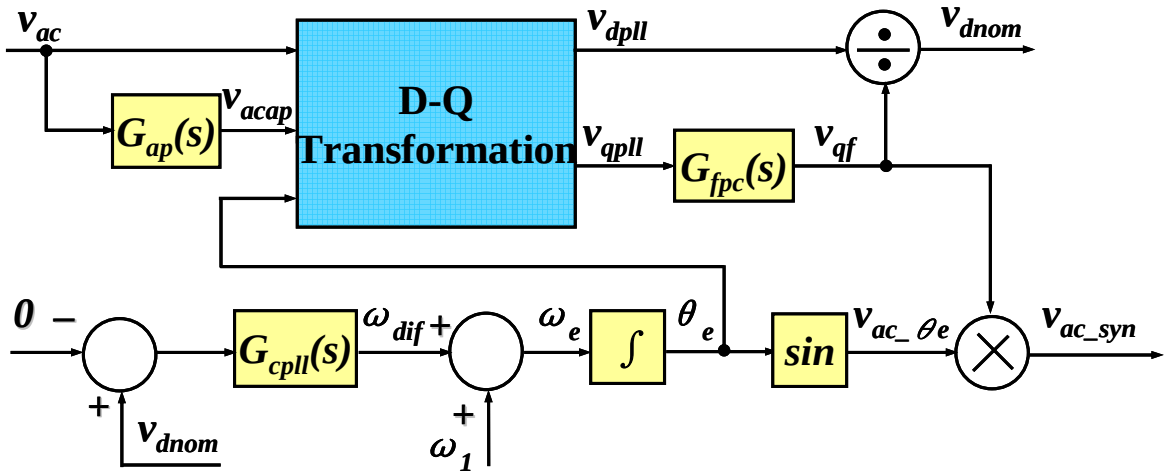
signal for the PLL. With an integrator as the PLL plant $G_{pll}(s)$, a controller $G_{cpll}(s)$ is designed to have a compensated loop gain $T_{pll}(s)$ with a 28-Hz cross-over frequency and a 36^o phase margin as shown in (2.15) and Fig. 2.10(b).

$$T_{pll} = G_{cpll}(s)G_{PLL}(s) \tag{2.15}$$

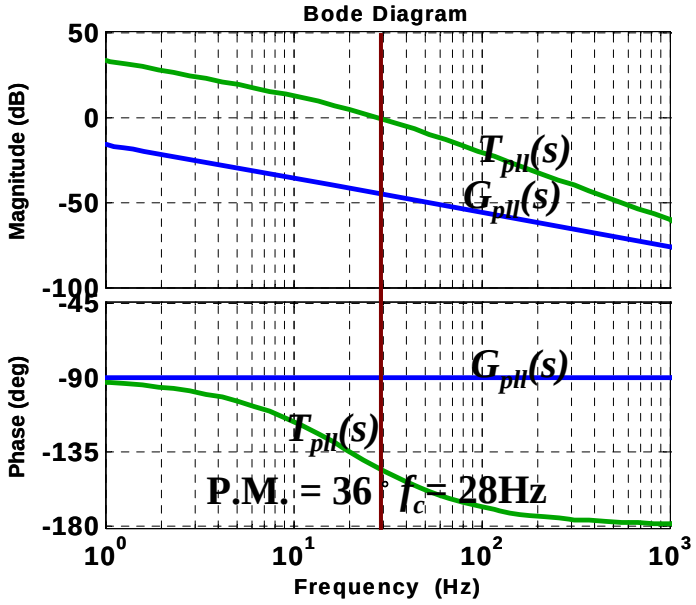
where $G_{pll}(s) = \frac{1}{s},\ G_{cpll}(s) = k_{pll}\frac{\omega_{pll}}{s + \omega_{pll}}$

Here $\omega_{pll,}\ k_{pll}$ are the cut-off frequency and gain of the PLL controller. As can be seen from the Fig. 2.10(b), the compensated PLL loop gain $T_{pll}(s)$ has a very high gain at zero Hz. This high loop gain means that the input signal v_{dnom} will eventually converge to zero and make the output estimated angle θ_e follow the input angle θ as shown in (2.16).

$$v_{dnom} = \frac{v_d}{v_{qf}} = \frac{V_m \sin(\theta - \theta_e)}{V_m} = \theta - \theta_e \ = 0 \text{ if } \theta \cong \theta_e \tag{2.16}$$



(a)



(b)

Fig. 2.10. Phase-lock loop with the peak-value calculation (a) control block diagram, and (b) PLL loop plot showing crossover frequency of 28Hz and phase margin of 36°.

2.8 Simulation and experimental verification

Fig. 2.11 shows the simulation results of the phase-lock loop and peak-value calculation. As can be seen from the top figure, the output signal v_{ac_syn} can track the input signal v_{ac} in both the phase and magnitude after a few fundamental cycles. The middle and bottom figures show the output of all-pass filter v_{acap} and the peak-value calculation output v_{qf}. The simulation results show that the designed PLL controller and peak-value calculation works properly.

A PCS prototype that contains a dc-dc converter to boost the fuel cell voltage from about 25V to 400V and a dc-ac inverter that produces 208V ac output for the grid connection is tested with a solid oxide fuel cell (SOFC) simulator, which mimics an actual low-voltage SOFC that has a stack of 36 cells operating at 1000°C. Fig. 2.12 shows test setup with the PCS prototype and associated instrumentation. A precision current shunt is used to calibrate the current measurement. The front panel of the case is open to show the DSP board.

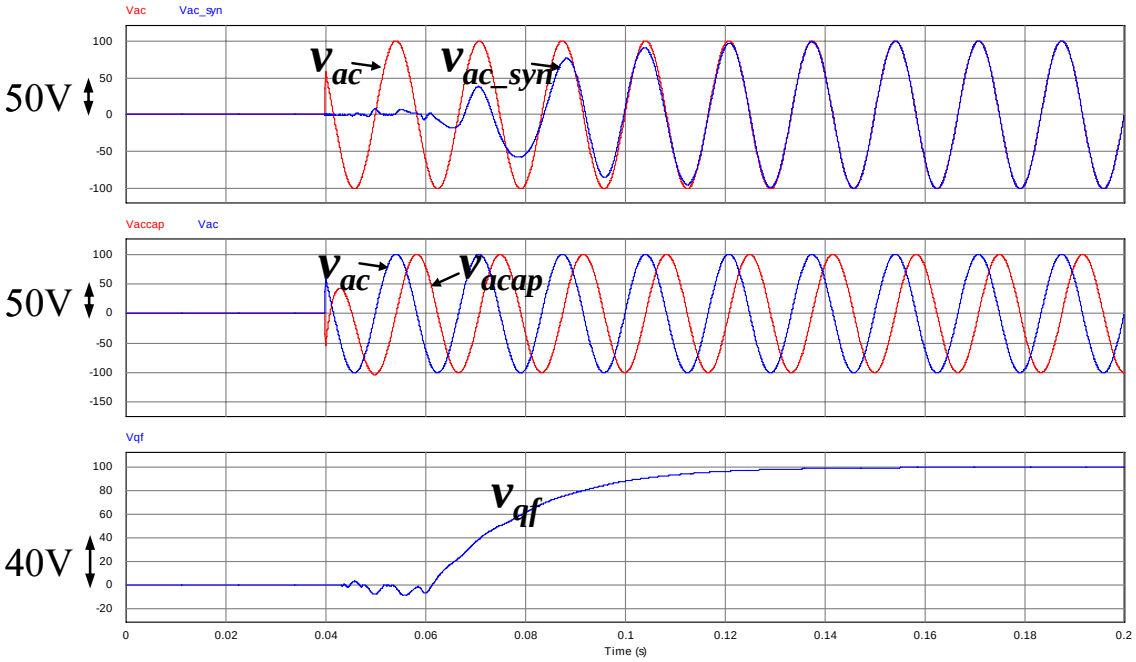


Fig. 2.11. Simulation results of phase-lock loop and peak value calculation.

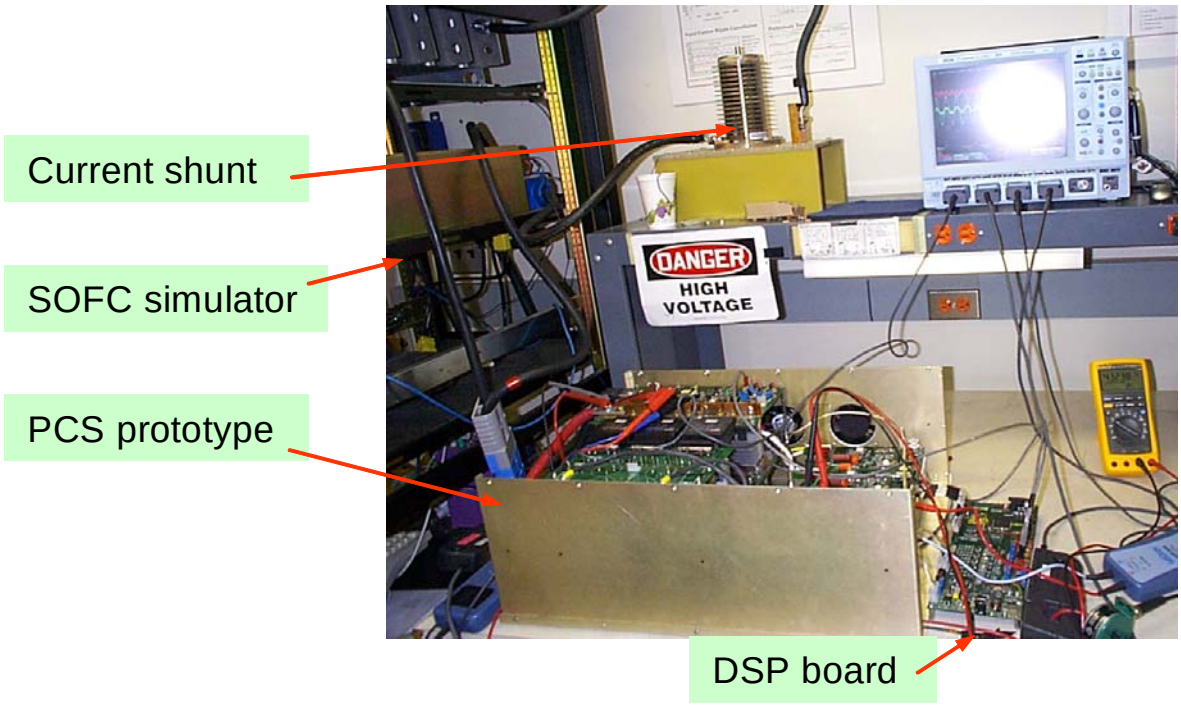
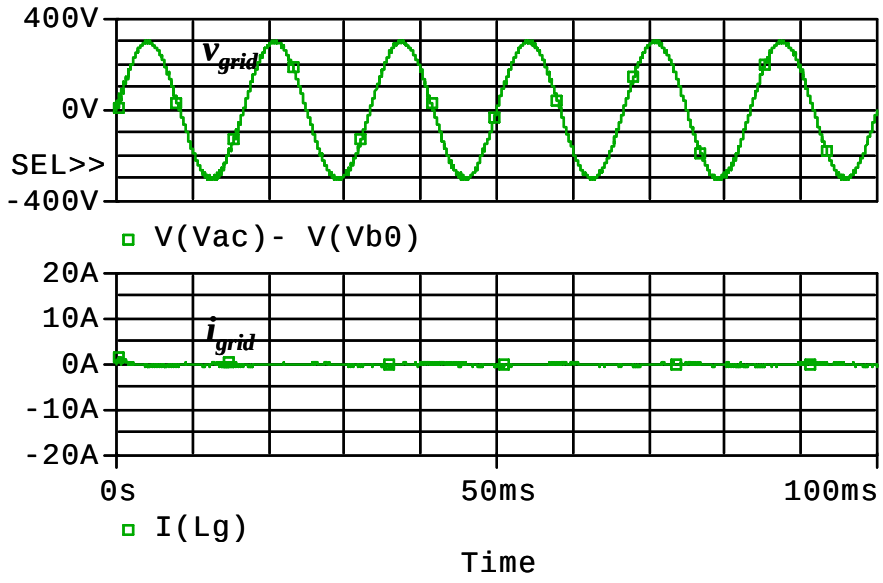


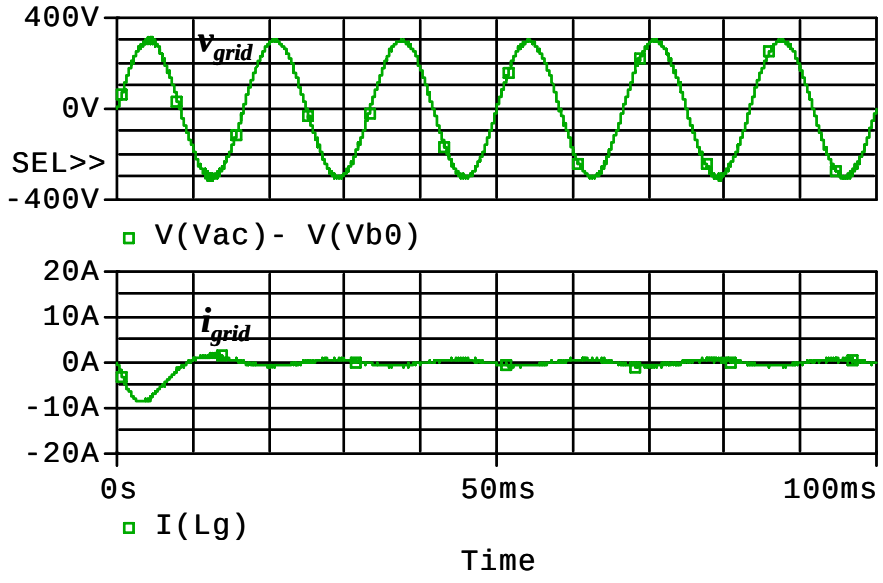
Fig. 2.12. Photograph of a fuel cell PCS prototype under test.

Fig. 2.13 shows the comparison of the simulation results with and without admittance compensation at zero power command start-up in time domain. Without the admittance path compensation, power flows back to the inverter during first simulation cycle, which will cause the dc bus capacitor to be charged and may result in catastrophe failure. Furthermore, fuel cell does not want to draw any current at zero power command due to its slow response. The simulation result shows that the addition of the admittance compensation achieves seamless current transient during system start-up and also obtains near zero current at zero power command.

Fig. 2.14 compares the experimental results without and with admittance compensation at zero power command start up. Without admittance compensation, shown in Fig. 2.14(a), the PR controller experiences a large startup transient current and 100-W output power P_o. With admittance compensation, as shown in Fig. 2.14(b), the startup transient is eliminated, and zero power output is controlled as demanded. Although a 4-W output is observed, it can be considered as measurement error and will not cause any impact to fuel cell operation. This smooth start-up characteristic is very important especially in a microgrid consisting of a large-amount of DG in parallel. With this technique, the start-up of a specific unit will not cause large transients to the whole system which is the key for a reliable microgrid system.

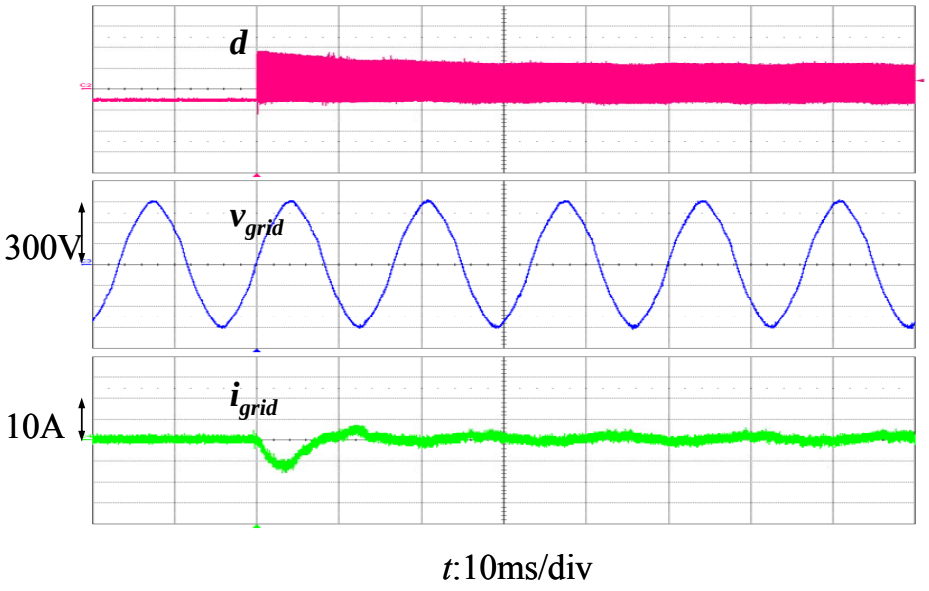


(a)

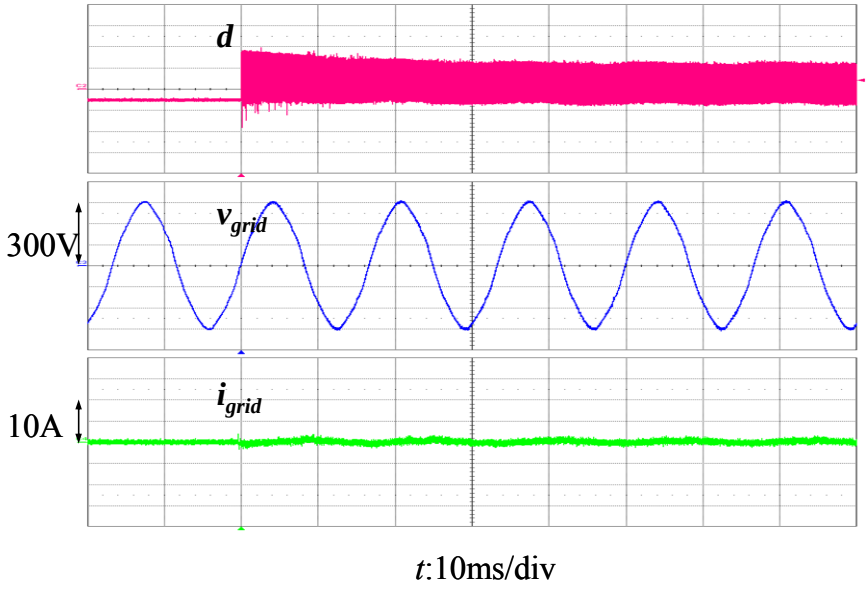


(b)

Fig. 2.13. Pspice simulation results at zero power command start-up (a) with $G_c(s)$ compensation, and (b) without $G_c(s)$ compensation.



(a)



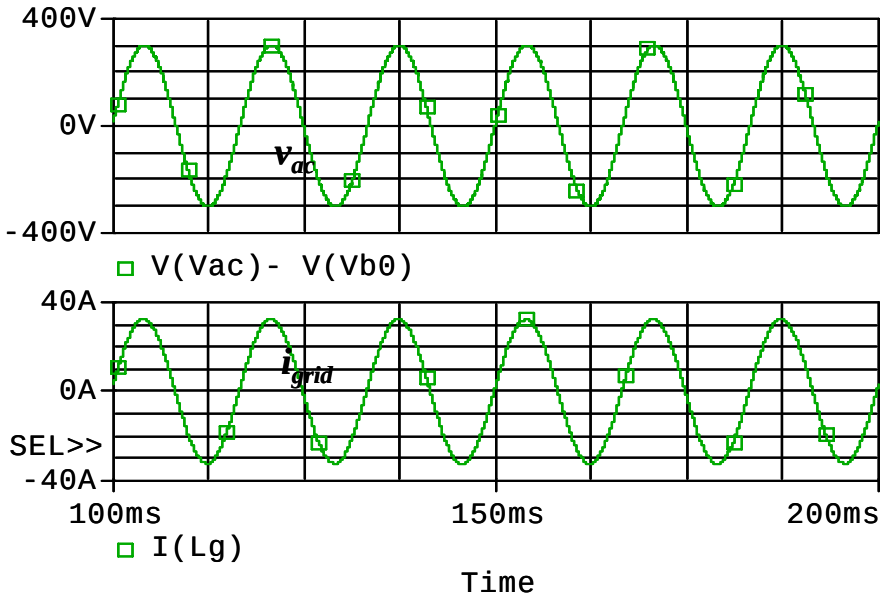
(b)

Fig. 2.14. Experimental results at zero power command start-up (a) without $G_c(s)$ compensation, and (b) with $G_c(s)$ compensation.

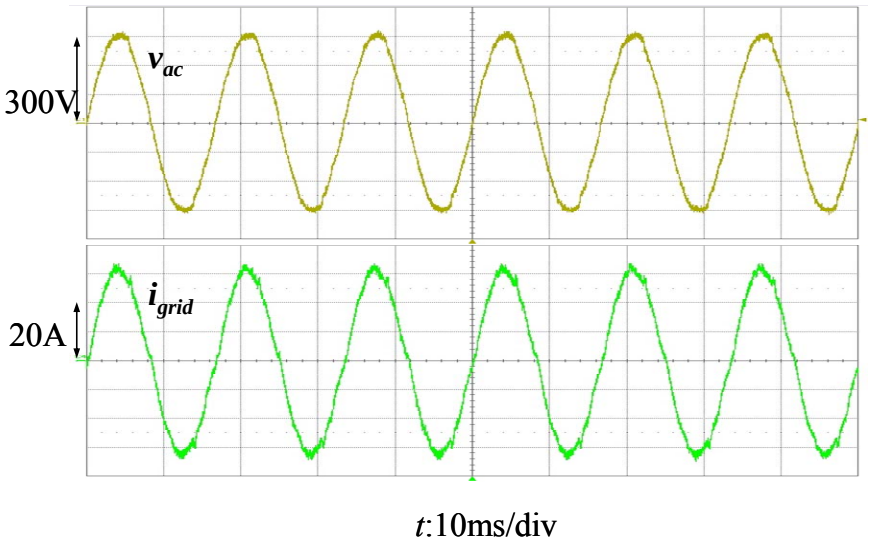
Fig. 2.15(a) shows the simulation results of the LCL-filter inverter running in current-mode control with PR controller and admittance compensation. The results show that the output current follows a 32-A peak command current very well because of a high loop gain at the fundamental frequency.

Fig. 2.15(b) shows the experimental results under 32-A peak current command in the grid-tie condition. Waveforms indicate that the output current follows the command well. Both the simulation and experimental results validate the effectiveness of the designed controller.

Fig. 2.16(a) and Fig. 2.16(b) show the simulation and experimental results of the dual-loop controlled LCL-filter inverter with a PR-controller based outer voltage-loop and a P-controller based inner current-loop operation. The output voltage v_{ac} is 215 V rms, and the output current i_{load} is 24.2 A rms. The power output of 5.2-kW goes into a pure resistive load in both simulated and tested cases. The simulation includes all the dynamics of system transfer function and controller blocks shown in Fig. 2.8. Again, the simulation result and experimental results shows that designed controller is capable to obtain stable outputs with precise power control.

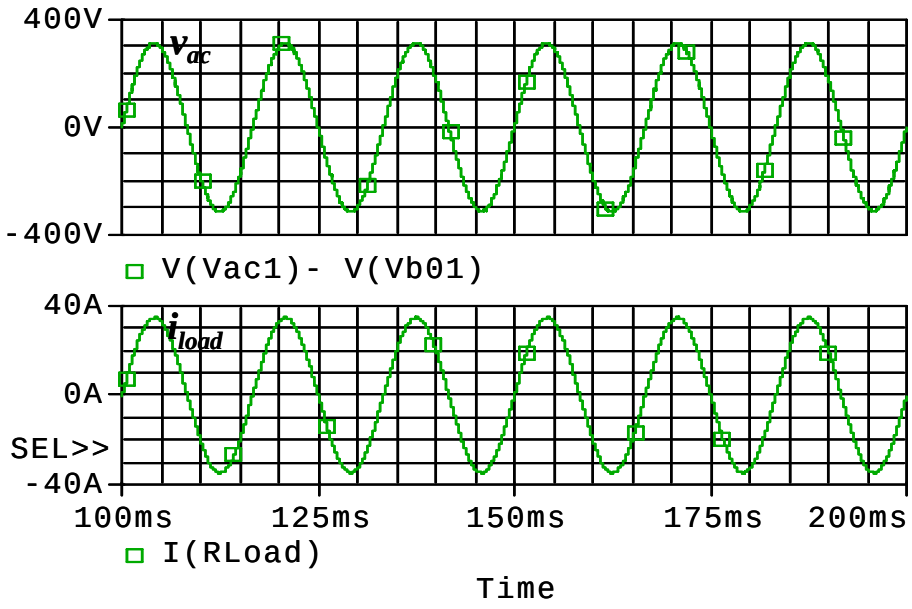


(a)

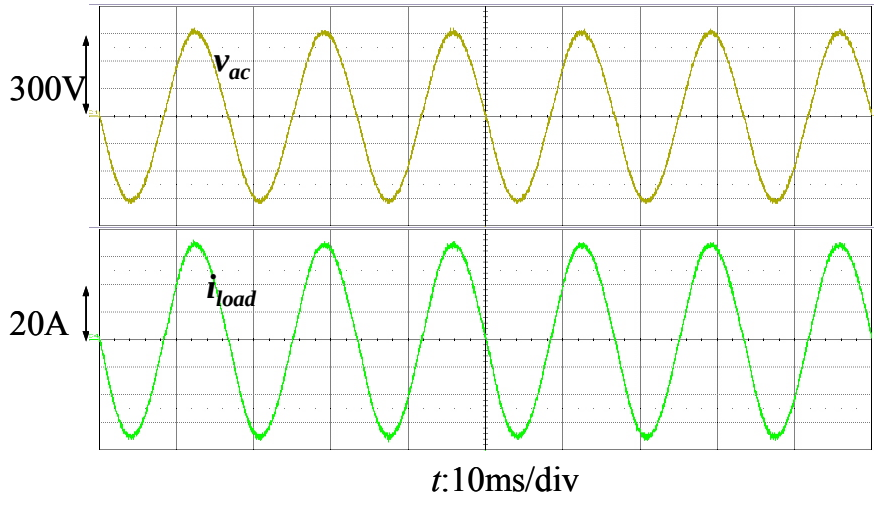


(b)

Fig. 2.15. Current loop implementation results at 4.85kW (a) Pspice simulation result at 32A $i_{ref,\,pk}$, , and (b) experimental result at 32A $i_{ref,\,pk}$.



(a)



(b)

Fig. 2.16. Voltage dual-loop results at 215V $v_{ac,\,rms}$, 5.2kW (a) Pspice simulation result, and (b) experimental result.

2.9 Summary

Complete design and implementation results of a single-phase universal power conditioning system operating in both grid-tie and standalone modes were presented in this chapter. Key design features of the proposed inverter system are summarized as follows.

1. Admittance compensation

   The proposed admittance compensation not only also allows the grid-tie system to be controlled like a first-order system but also helps reduce the start-up transient during the grid-tie connection to improve system reliability by preventing the reverse power flow.

2. Design of LCL filter

   This chapter suggests several design considerations based on the current ripple, stability, output performance, sensor location, noise concern, and the ease of controller design.

3. Design of dual- and single-loop controllers

   For the grid-tie operation, a single current loop controller design with PR controller and admittance compensation is proposed to reduce the steady-state error while maintaining system stability. For the standalone operation, a dual-loop control system with PR-controller for outer voltage loop and a P-controlled for inner current loop is proposed to limit peak current magnitude under transient, enhance voltage loop stability, and reduce voltage steady-state error.

4. Design of phase-lock loop

The PLL provides the synchronized phase of the current command which is the key for precision power flow control. The band-pass-filter feature of PLL also allows the input of the admittance compensation to avoid the dc offset and high-frequency noise in the feedback network.

The proposed admittance compensation and current loop controller has been simulated and implemented in a DSP-based 5-kW PCS. Without admittance compensation, both simulation and experiment results show that a significant startup transient and non-zero current output at zero power command. The power flow in the first cycle is reversed, and the energy is erratically fed back to the inverter, which may cause over voltage in the dc link and result in catastrophic failure. With admittance compensation, a smooth startup was observed in both simulation and experiment. The zero current command can be precisely achieved.

Simulation and experimental results show that the designed inverters are capable of operating in both grid-tie and standalone modes by adapting to different controller sets with the same hardware setup. The LCL filter based inverter controlled with the proposed single- and dual-loop controllers for different operating modes shows stable output waveforms. These results validate that the proposed universal-inverter with LCL filter, the dual-loop voltage and single-loop current controllers can be as the key elements for microgrid applications where both the grid-tie and standalone operations are required.

Chapter 3

Current Sharing and Smooth Mode Transfer of Parallel Inverters in Microgrid Applications

3.1 Introduction

In this chapter, the inverter control in previous chapter is utilized as the building block for a small-scale microgrid system with multiple inverter-based DGs. Two main issues will be discussed: (1) current-sharing in the islanding mode of a microgrid, and (2) smooth mode transfers between the islanding mode and grid-tie mode.

In order to minimize the system thermal stress or perform the power management to achieve system cost effectively, the microgrid system should perform the current sharing among the paralleled inverters through the communication channels. In this chapter, a frequency-decoupled command transmission method was proposed so that it can transmit in a longer distance with a low bandwidth communication channel.

For the microgrid system, the designed system should be able to smoothly transfer between two basic operation modes and continuously supply the critical loads. In order to minimize the excessive electrical stresses, the considerations for a seamless transfer are provided and proper mode transfer procedures are suggested.

3.2 Basic microgrid operations with LCL parallel inverters

In a microgrid system, there are two basic operation modes: grid-tie mode and islanding mode. Fig. 3.1 shows the hardware configuration of the parallel-inverter microgrid system running in the islanding mode. If the grid is not available, the SSR is disconnected and the system supplies its own power to the critical load. In chapter 2, standalone mode stands for a single inverter running in the dual voltage loop. The islanding mode here refers to a cluster of parallel inverters operating together to supply the critical load. One of the inverters has to operate in the voltage dual-loop control and serve as a voltage source, while the rest of the inverters operate in the single current-loop control to share the current as required. When the grid recovers, the SSR is reconnected and all the inverters in the system run in the single current mode to supply energy to the critical load and to exchange energy with the grid.

Fig. 3.2 shows the control block diagram of the parallel-inverter microgrid system running in the islanding mode. Every individual inverter has its own DSP controller and there is an upper-level controller which provides the mode attribute and the mode-transfer command generation for the inverters in the system. When the microgrid system in Fig. 3.1 switches from the islanding mode to grid-tie mode, only the control of the first inverter changes from the voltage-control mode to current-control mode as shown in Fig. 3.3; while the control of the other inverters stays the same. At least one inverter is operating in the voltage dual-loop control in the islanding mode. Conversely, all inverters are running in the current single-loop control in the grid-tie mode. The selection of the inverter

running in the voltage-mode or current-mode control is also determined by the upper-level controller through the CAN bus.

With the hot-swap CAN bus, the communication channel will still survive even when one single node is disconnected. In addition, when the original dual-loop unit fails, the microgrid system still can function because the upper-level controller will assign another inverter as the dual-loop control and keep the whole system running. However, the CAN bus or upper-level controller may fail. In this case, it is necessary to adopt other backup control methods such as droop control [24], [50]-[53] or circular-chain control [25] to improve system reliability. These added backup control methods may increase the hardware cost due to increased communication ports or the software burden due to additional computation requirement.

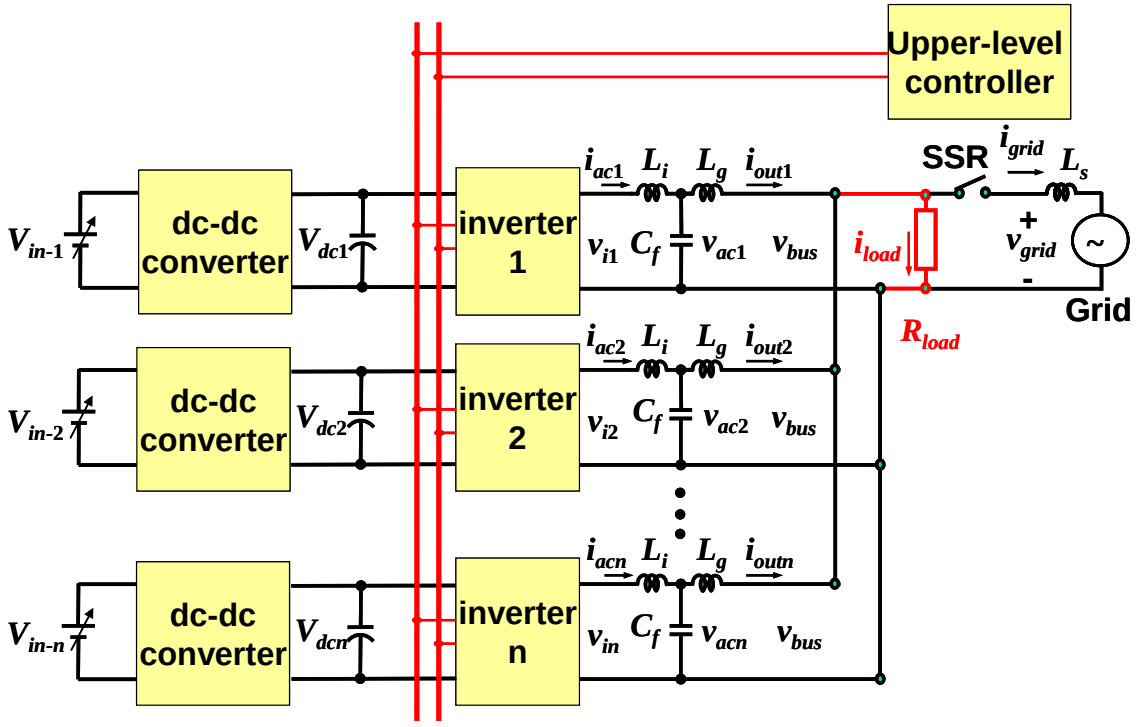


Fig. 3.1. The hardware configuration of parallel-inverter microgird system.

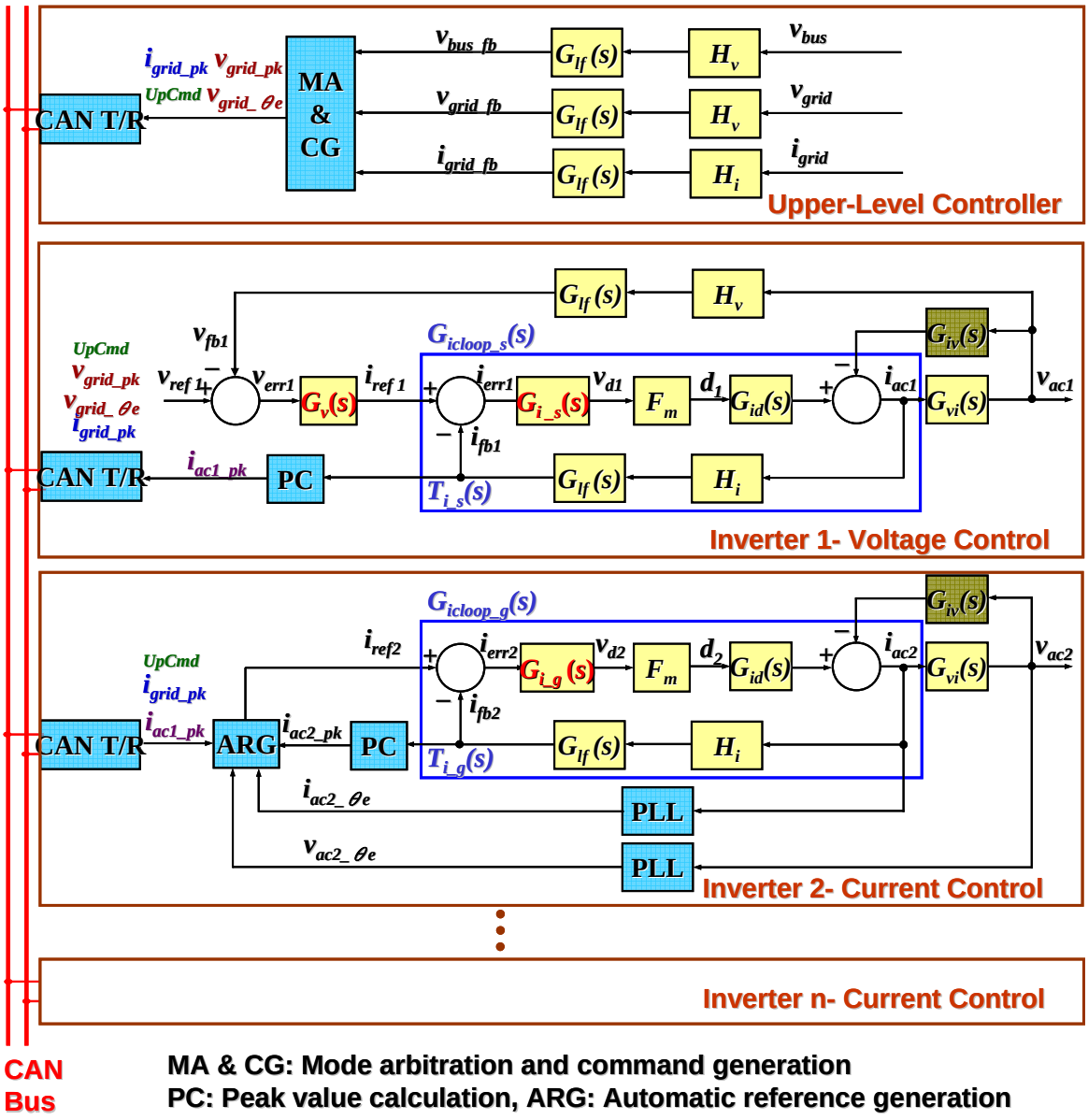


Fig. 3.2. Control block diagrams of the parallel-inverter microgrid system in islanding mode.

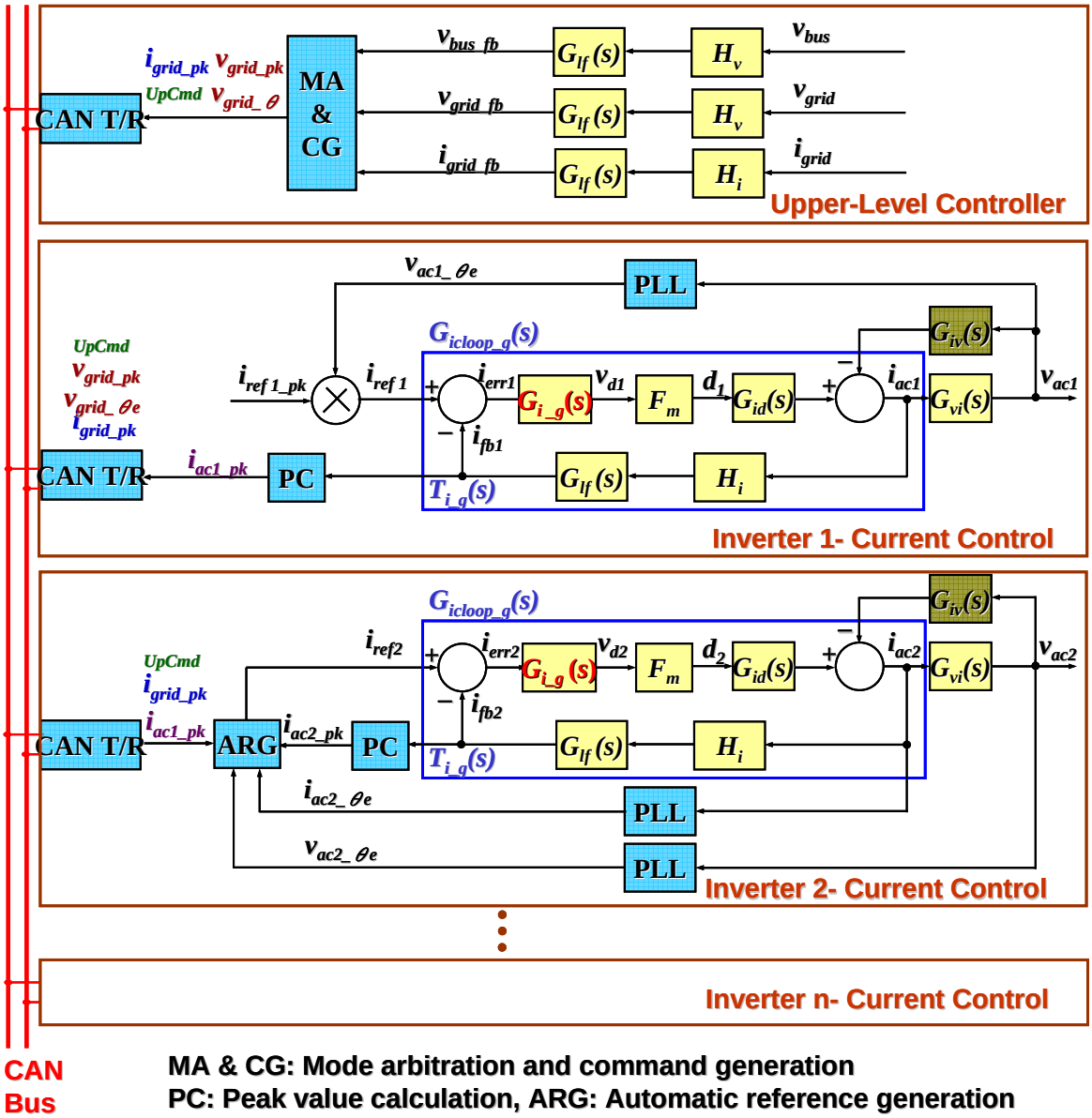


Fig. 3.3. Control block diagrams of the parallel-inverter microgrid system in grid-tie mode.

3.3 Current sharing and synchronization through CAN bus

The current sharing capability is important for a reliability and/or cost effectively system. As shown in Fig. 3.2, the microgrid can share the currents among parallel inverters by the peak value calculation (PC), the automatic reference generation (ARG), and the phase-lock loop (PLL) blocks through the CAN bus. As shown in (3.1), once the PC and the PLL detect the magnitude and phase information, the ARG adjusts the current reference i_{ref2} so that the current peak difference and phase difference are minimized.

$$i_{ref2} = i_{ref2\_pk} * i_{ref2\_\theta} \tag{3.1}$$

$$\text{where } i_{ref2\_pk} = i_{ac1\_pk} + i_{pk\_offset},\ \begin{cases} i_{pk\_offset} = i_{pk\_offset} \text{ if } \left|i_{ac1\_pk} - i_{ac2\_pk}\right| < i_{pk\_band} \\ i_{pk\_offset} = i_{pk\_offset} \pm i_{pk\_step} \text{ if } \left|i_{ac1\_pk} - i_{ac2\_pk}\right| > i_{pk\_band} \end{cases}$$

$$i_{ref2\_\theta} = v_{ac2\_\theta e} + i_{\theta\_offset},\ \begin{cases} i_{\theta\_offset} = i_{\theta\_offset} \text{ if } \left|v_{ac2\_\theta e} - i_{ac2\_\theta e}\right| < i_{\theta\_band} \\ i_{\theta\_offset} = i_{\theta\_offset} \pm i_{\theta\_step} \text{ if } \left|v_{ac2\_\theta e} - i_{ac2\_\theta e}\right| > i_{\theta\_band} \end{cases}$$

Here the i_{pk_band} and i_{θ_band} are the magnitude and phase bands for the inequality condition. The i_{pk_step} and i_{θ_step} are the magnitude and phase step sizes respectively to modify the magnitude offset i_{pk_offset} and the phase offset i_{θ_offset}. In this system, only the digitally formatted ac signal magnitude and phase information need to be transmitted. The frequency information does not need to be transmitted because it will be automatically tracked by the PLL.

Without transmitting the actual 50 or 60Hz ac signal, the transmitting bandwidth can be lowered and the transmission distance can be largely extended. For frequency-decoupled signal transmission, the signal transmitted is the current reference signal which requires a maximum 1kHz bandwidth due to the inner current loop with a 1.45kHz cross-over frequency. However, if the 60Hz signal is transmitted in ac form which frequency and magnitude are both transmitted, then a 1kHz bandwidth communication channel will cause a 21.6 degree phase delay. This means that the output currents of two parallel inverters will have at least 21.6 degree difference even if the current loop bandwidth is infinite. In order to reduce this current reference phase delay to less than one degree for 60Hz ac signal transmission, the communication channel needs to have a bandwidth at 22kHz or more. Table 3.1 shows the relationship between maximum signaling rate and cable length of CAN bus [97]. Assume the data length per transmission of both ac and frequency-decoupled signal transmission are the same, this table indicates that the bus length of the frequency decoupled method can be 30 times longer of if the signaling rate is 20 times less.

Thanks to the differential transmission and the CAN bus error checking protocol, the signal transmission can be very reliable even in a noisy environment [98]. The CAN protocol incorporates five methods of error checking: monitoring checks, cyclic redundancy check, bit stuffing, and message frame check. A very tiny message error rate of undetected error at $4.7 * 10^{-11}$ can be achieved by these well designed error-detection mechanism. For a message error rate of 100/sec, there will be 1 undetected error per 2,462 days operation.

Table 3.1 Maximum signal rates for various cable lengths of CAN bus

Bus length (m)	Signaling rate (kbps)
30	1000
100	500
250	250
500	125
1000	62.5

3.4 Mode transfer considerations Performance evaluation of generalized control structure

As shown in Fig. 3.1, the parallel-inverter microgrid system should either supply the critical load R_{load} and exchange the power with the grid when the grid is available, or keep supplying the R_{load} when the grid is not available. In order to keep supplying power to R_{load}, the microgrid system is required to switch between grid-tie and islanding modes without drastic electrical stresses. If the system does not have the proper mode transfer procedure, severe transient voltages or currents will occur which may damage the entire system. Since the whole microgrid is controlled like a current source in the grid-tie mode and a voltage-controlled output in islanding mode, the key of a smooth transfer is to comply with the basic circuit laws: (i) do not interrupt a large magnitude of current on the switch, (ii) do not connect two voltage sources directly without well matched and synchronized magnitude, frequency and phase.

With the control block diagram shown in Fig. 3.3, the proposed procedure to change from the grid-tie to islanding mode is summarized as:

(a) The upper-level controller detects the fault on the grid v_{grid} and extracts the grid current information i_{grid}.

(b) Through the CAN bus, the upper-level controller provides i_{grid} information and commands all the current-controlled inverters to change their outputs, so that the current on the SSR i_{grid} can be minimized to avoid mode transfer transient.

(c) The upper-level controller provides the turn-off signal for the SSR after a certain waiting time, for example, 5 cycles.

(d) Through the CAN bus, the upper-level controller commands a selected inverter (inverter 1) to change from the current-controlled mode to voltage-controlled mode at the next zero crossing.

(e) Inverter 1 regulates the bus voltage to a desired level and provides the output current information to inverter 2, so that they can share the total current in the islanding mode.

Since the inverter-based microgrid tends to have small over-current capability, the 5-cycle waiting is chosen to ensure smooth current transfer while considering the 10-cycle clearing time under the worse case abnormal grid voltage and frequency conditions [20]. However, this waiting time can be set to another value to accommodate equipment electrical ratings and a desirable clearing time in different fault conditions. On the other hand, the procedure to change from the islanding to grid-tie mode is summarized as:

(a) The upper-level controller detects if the grid voltage v_{grid} recovers and keeps detecting the grid voltage magnitude v_{grid_pk} and phase $v_{grid\_\theta e}$ information.

(b) Through the CAN bus, the upper-level controller provides the grid voltage information and commands the inverter 1 to adjust v_{bus} to track v_{grid} in both magnitude and phase.

(c) The upper-level controller keeps monitoring v_{bus} and v_{grid}. It turns on the SSR once the two voltages are synchronized in phase and magnitude.

(d) Through the CAN bus, the upper-level controller commands the inverter 1 to change its controller from the voltage-controlled mode to current-controlled mode at the next zero-crossing. It assigns the current references so that zero current goes through the SSR during the transfer transient.

(e) The current controlled inverters change the current reference to a desired level.

3.5 Simulation and experimental verification

Fig. 3.4 shows the hardware setup of the tested microgrid system, which consists of two identical power conditioning systems, an upper-level controller, an SSR, and the CAN bus connection. Each power conditioning system consists of a dc-dc converter to boost the low-voltage input 48 V to 420 V and a dc-ac inverter that produces 208 V ac output for the grid connection. The source of the dc-dc converter can be a fuel cell or a photovoltaic, but for this testing, a 60-V, 20-kW fuel cell simulator was used to serve as the source. Each power conditioning system is packaged in a standard 19" rack-mount case with a power connection on the back panel, and the DSP controller on the front panel. The upper-level controller communicates with power conditioning systems by the CAN bus to provide a stable communication. A solid-state relay SSR is used to connect the grid at the point of common coupling (PCC) to perform the mode transfers.

Fig. 3.5 shows the simulation and experimental results of the parallel-inverter microgrid system in the islanding mode to supply a 7.6 kW critical load. Load voltage v_{load} and the total current i_{load} are the waveforms observed at the load terminal. Current i_{out1} and i_{out2} are monitored at the individual inverters. Both simulation and experimental results indicate that the output currents of two inverters are in phase, and both parallel inverters share current evenly to supply the load together.

With the observation of the total current i_{load} being equal to the sum of i_{out1} and i_{out2}, one can easily conclude that there is no observable circulating current between the dual-loop controlled and single-loop controlled inverters. The even current distribution suggests that the microgrid system along with CAN communication, phase-locked loop and automatic phase adjustment control works effectively.

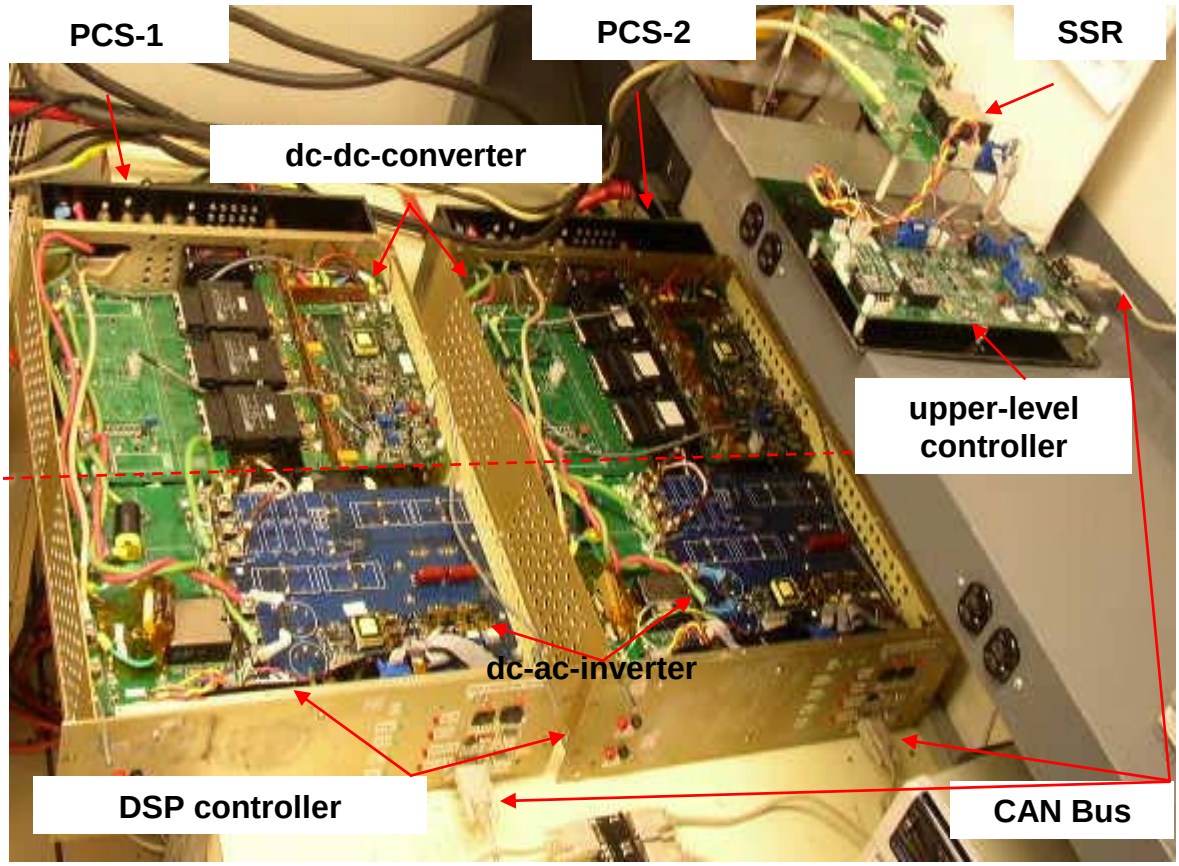
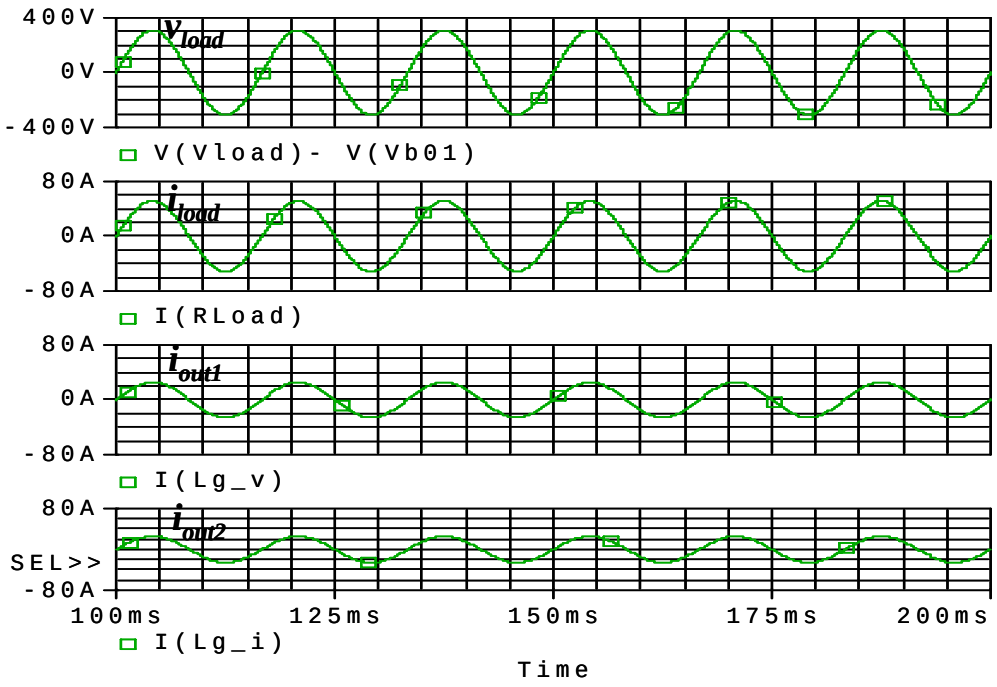
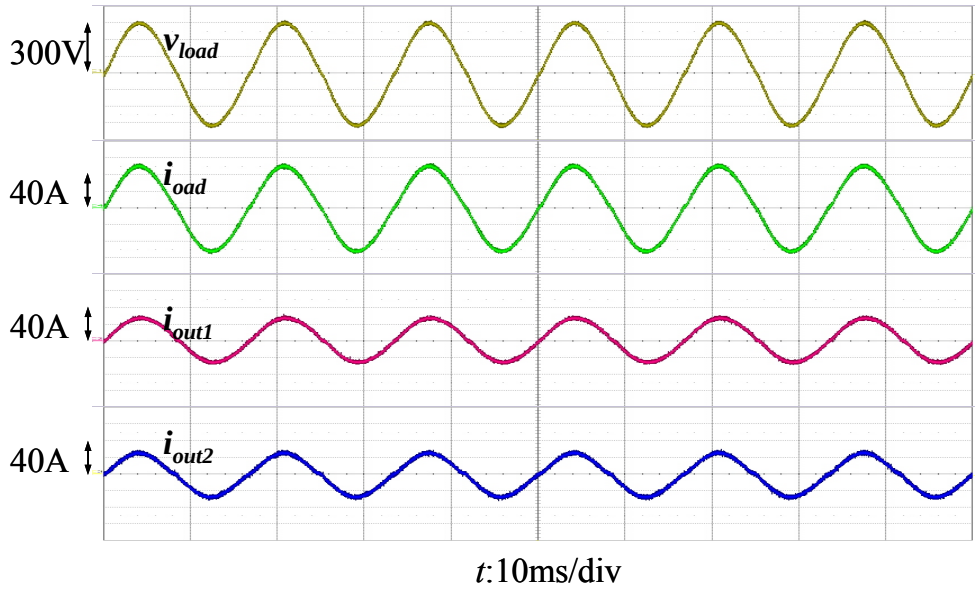


Fig. 3.4. Photograph of the proposed microgrid system.



(a)



(b)

Fig. 3.5. Islanding mode operation by designed parallel-inverter system at 215V $v_{load,\ rms}$, 7.6kW (a) Pspice simulation result, and (b) experimental result.

Fig. 3.6 and Fig. 3.7 show the simulation and experimental results of the mode transfer from the grid-tie mode to islanding mode for the parallel-inverter microgrid system. For the mode transfer tests, the grid voltage is simulated by an additional voltage-controlled inverter so that the simulated grid voltage can be regulated to trigger the mode transfer. For the safety considerations, the mode transfers are conducted with the following resistors to limit the transient currents: a 2.5-Ω resistor in series with the simulated grid, a 1.6-Ω resistor in series with the inverter 1 output, and a 1-Ω resistor in series with the output of inverter 2. Before the mode transfer, all the inverters in the microgrid system operate in the grid-tie mode so that the bus voltage v_{bus} is the same as the grid voltage v_{grid}. Notice that the i_{grid} and v_{grid} are 180 degrees out of phase which means that the grid also supplies power to the critical load R_{load} before the mode transfer. Once the grid voltage v_{grid} is higher than a preset limit (135V rms), the upper-level controller starts to command all the current controllers to change their output currents i_{out1} and i_{out2} to minimize the current in i_{grid}.

As can be seen from the waveforms, the i_{grid} starts to decay to near zero about 5 cycles ahead of changing the state of the SSR control signal V_{ssr_ctl}. Five cycles later, the upper-level controller changes the level of the SSR control signal V_{ssr_ctl} which turns off the SSR at the next zero crossing. Notice that the time V_{ssr_ctl} changes state in the simulation is the real time that the SSR starts to act, which happens at the zero crossing. The PWM signal switches from current controller to voltage controller at the same zero crossing.

The voltage controller in inverter 1 regulates the bus voltage v_{bus} and keeps supplying the load in islanding mode. At the same time, the current sharing mechanism by the CAN bus and the auto-tuning reference start to work to minimize the thermal stress of the system. Both the simulation and test results show no severe transients in the bus voltage v_{bus} and load current i_{load}, which suggests that the parallel-inverter microgrid system can transfer from the grid-tie to islanding mode smoothly. In order to clearly show the voltage level difference before and after the mode transfer during an abnormal voltage condition, the bus voltage is intentionally set at a higher level before and at a lower level after the mode transfer. The test waveform shows that when the bus voltage is 15% higher than the nominal voltage, it is transferred to the islanding mode. After the mode transfer, the bus voltage is intentionally 10% lower than the nominal voltage. In actual systems, these abnormal voltage levels can be different levels as specified in [20].

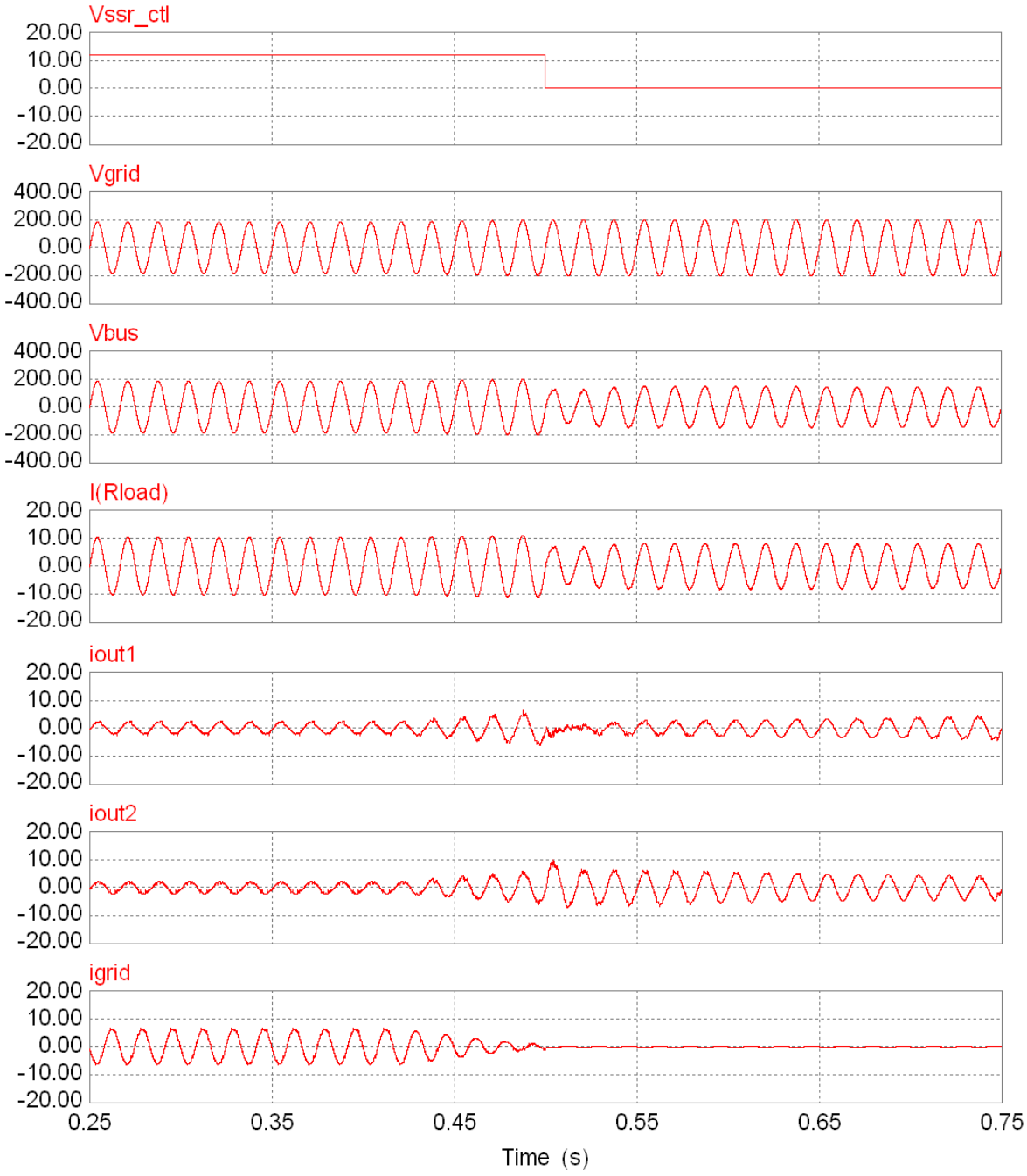


Fig. 3.6. Grid-tie mode to islanding mode transfer simulation results.

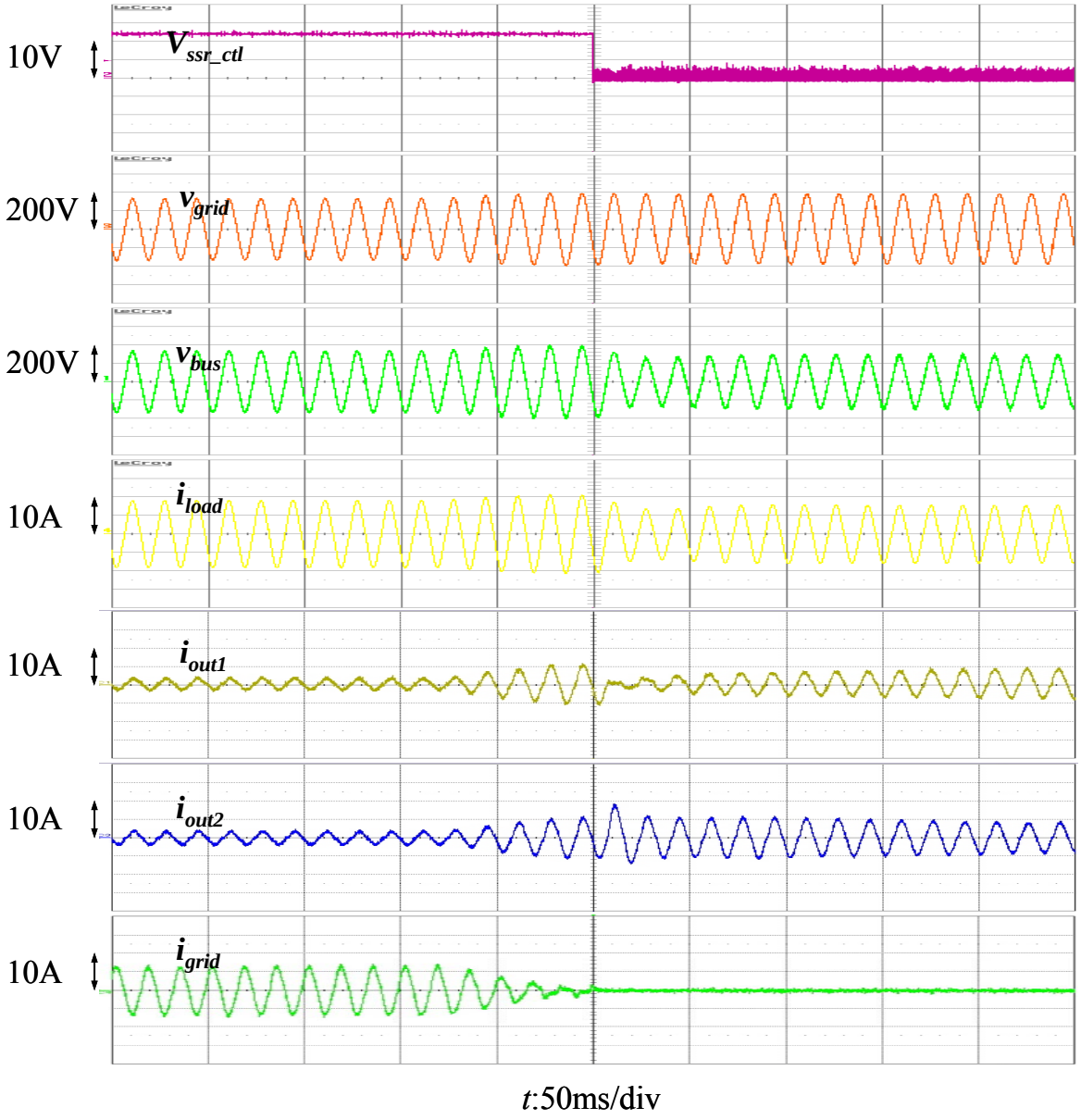


Fig. 3.7. Grid-tie mode to islanding mode transfer experimental results.

Fig. 3.8 shows the experimental result of bus voltage synchronization transition before the microgrid system reconnecting to the grid. Once the grid voltage recovers to a preset value, commanded by the upper-level controller through CAN bus, the inverter 1 starts to synchronize the magnitude and phase of bus voltage v_{bus} to v_{grid}. Fig. 3.9 and Fig. 3.10 show the simulation and experimental results of the paralleled-inverter microgrid system transferring from the islanding to grid-tie mode. If the phase and magnitude are synchronized, the upper-level controller turns on the switch SSR by changing V_{ssr_ctl} at the next zero crossing. By commanding through the CAN bus from the upper-level controller, the inverter 1 switches from voltage to current controller at the same zero crossing. The current reference in inverter 1 after the mode transfer is intentionally set so that only a small current is shown in i_{grid} to minimize the switching transient. No noticeable transients are observed in v_{bus} and i_{load} which indicates the parallel-inverter microgrid system is capable of transferring from the islanding mode to grid-tie mode smoothly.

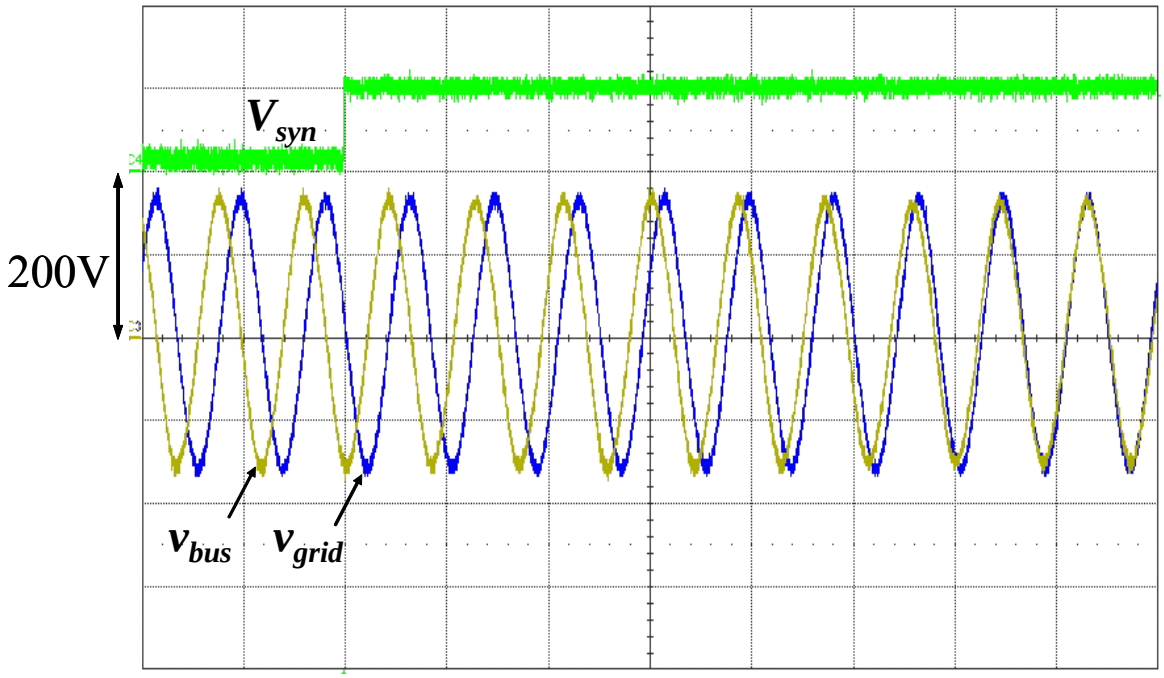


Fig. 3.8. Bus voltage synchronization transition before the micorgrid reconnecting to the grid.

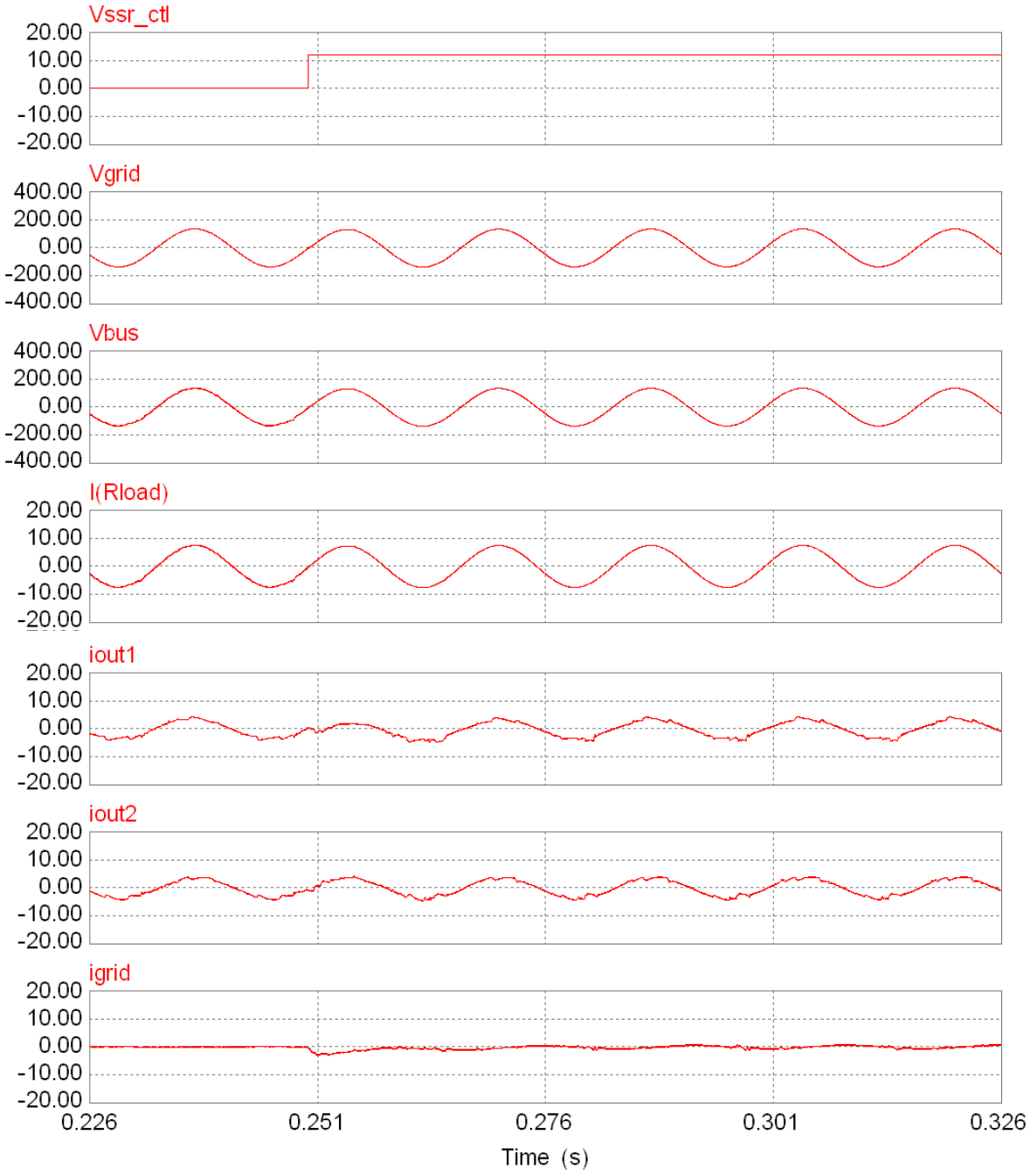


Fig. 3.9. Islanding mode to grid-tie mode transfer simulation results.

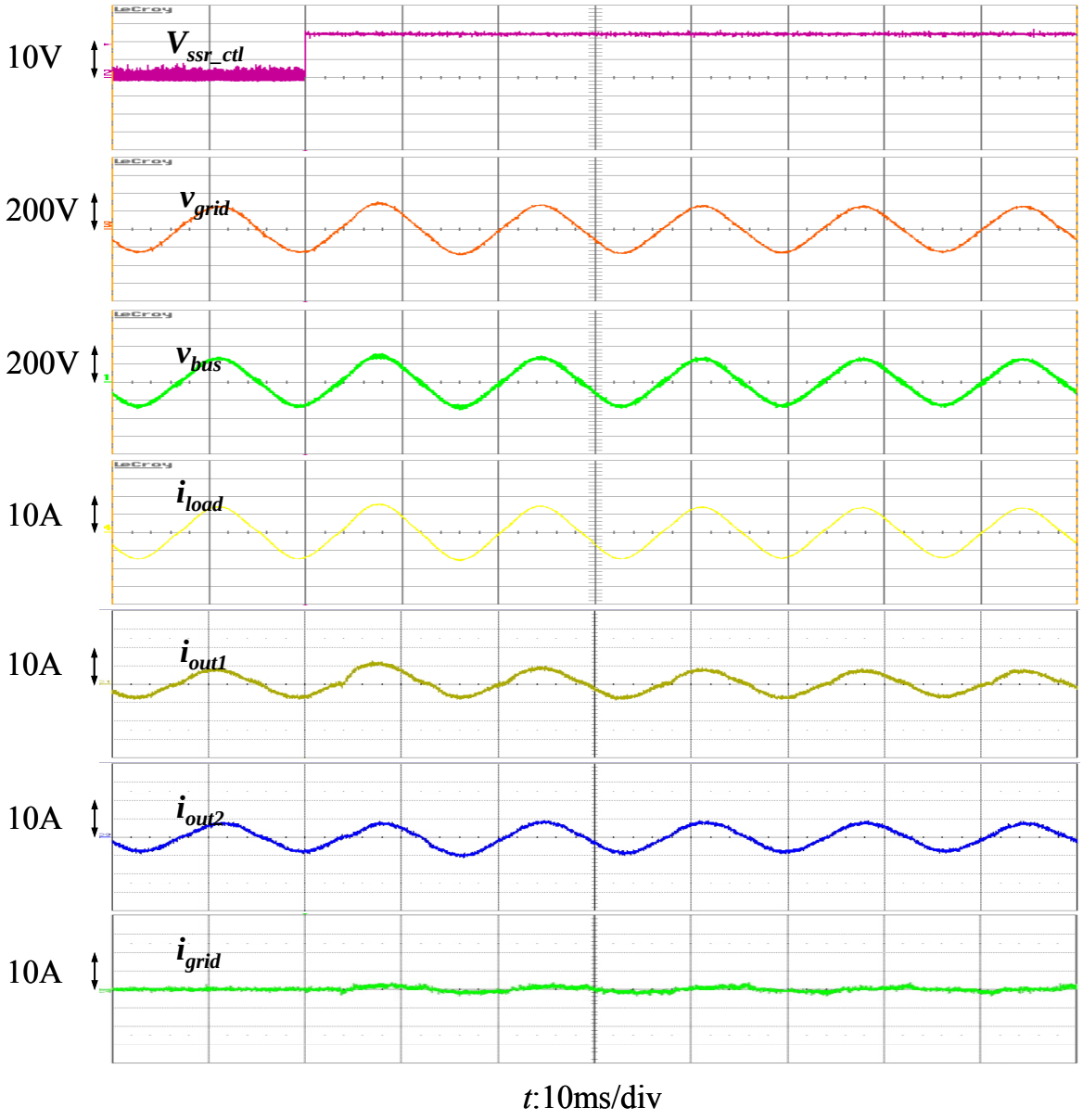


Fig. 3.10. Islanding mode to grid-tie mode transfer experimental results.

3.6 Summary

This chapter presents a complete design and implementation of an experimental microgrid with paralleled power conditioning systems operating in the grid-tie mode, islanding mode, and mode transfer. Key features of the proposed microgrid system are summarized as follows:

1. Equal current sharing and synchronization

   With the use of the CAN bus, the transmitted current magnitude is served as a reference to adjust the current reference to the rest of inverters so that every inverter shares the current equally. The phase synchronization is implemented with PLL and an automatic phase adjustment to synchronize the output currents among the inverters.

2. Smooth mode transfer between the grid-tie and islanding modes

   Key considerations for a seamless transfer are provided by applying basic circuit laws. Proper mode transfer procedures with smooth current transition are suggested to minimize the excessive electrical stresses.

Simulation and experimental results show that the output currents are equally shared among different inverters without a noticeable circulating current by the use of the proposed synchronization and upper-level control methods. Both the mode transfer simulation and experimental results show that the multi-inverter based microgrid system can switch between the grid-tie and islanding modes smoothly to ensure an uninterrupted power supply to the critical loads.

The successful system operations suggest that the proposed parallel-inverter system design with the LCL filter based inverters, mix of the dual- and single-loop voltage and current controllers, PLL synchronization and CAN bus communication architecture can be extended to microgrid or smartgrid applications.

Chapter 4

State-Space Modeling, Analysis, and Implementation of Paralleled Inverters for Microgrid Applications

4.1 Introduction

In this chapter, a state-space model of the previous proposed power conditioning system will be performed so as to study the system stability under various conditions. Eigenvalues with different controller gains and load conditions for both grid-tie mode and standalone mode will be analyzed. The state-space model will also be extended to a parallel-inverter system for the investigation of the load variation effects to the system stability. A time-domain current ripple criterion is also suggested for the light-load operation of the parallel-inverter microgrid system.

4.2 Modeling and analysis of single inverter in grid-tie mode

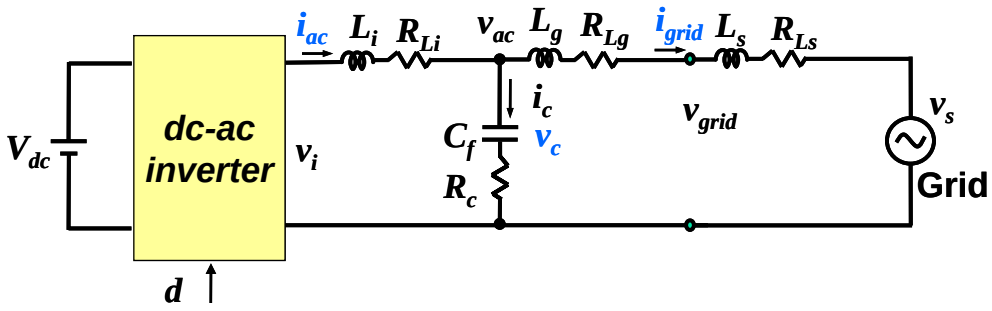
Fig. 4.1(a) and Fig. 4.1(b) show a single inverter running in the grid-tie mode and standalone mode, respectively. As shown in Fig. 4.1(a), a LCL filter is commonly used for filtering the output current ripple in the grid-tie mode. The resistances of the LCL filters and the grid-impedance are also modeled here for a general case. As expressed in (4.1), this LCL filter makes the first 3rd order dynamic equations in the grid-tie inverter system.

$$\begin{bmatrix} L_i & 0 & R_c C_f \\ 0 & L_g + L_s & -R_c C_f \\ 0 & 0 & C_f \end{bmatrix} \begin{bmatrix} \frac{di_{ac}}{dt} \\ \frac{di_{grid}}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} R_{Li} & 0 & -1 \\ 0 & -R_{Lg} - R_{Ls} & 1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} i_{ac} \\ i_{grid} \\ v_c \end{bmatrix} + \begin{bmatrix} V_{dc} & 0 \\ 0 & -1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} d \\ \\ v_s \end{bmatrix} \tag{4.1}$$

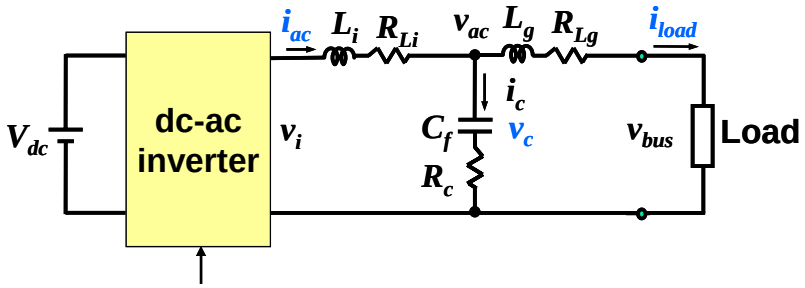
Three state variables i_{ac}, i_{grid} and v_c are the inverter-side-inductor current, grid-side inductor current and capacitor voltage, respectively. The d and the v_s are the control gating signal and the grid voltage. Fig. 4.2 shows the control block diagram of the grid-tie inverter. With admittance compensation, the duty cycle v_d consists of the feedback duty cycle v_{dFB} and admittance compensation term v_{dLPAC} to obtain two corresponding gate signals d_{FB} and d_{LPAC} which is expressed in (4.2).

$$d = F_m * v_d = F_m * (v_{dFB} + v_{dLPAC}) = d_{FB} + d_{LPAC} \tag{4.2}$$

where $v_{dFB} = i_{err} * G_{i\_g}(s)$, $v_{dLPAC} = v_{ac} * H_v * G_c = (v_c + R_c * (i_{ac} - i_{grid})) * H_v * \frac{1}{H_v V_{dc} F_m}$



(a)



(b)

Fig. 4.1. Single inverter hardware configuration: (a) grid-tie mode, and (b) standalone mode.

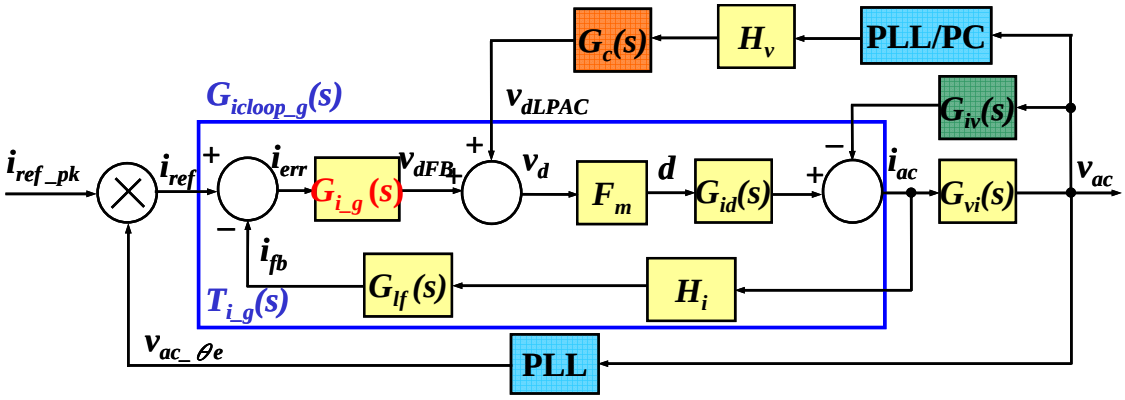


Fig. 4.2. Control block diagrams of a single inverter in grid-tie mode with admittance compensation.

In Fig. 4.2, H_i and $G_{lf}(s)$ are the current feedback gain, and the hardware low-pass filters' transfer function. This feedback network contributes to another third-order differential equation shown in (4.3).

$$\begin{bmatrix} \frac{di_{fb}}{dt} \\ \frac{di_{HA1}}{dt} \\ \frac{di_{HA2}}{dt} \end{bmatrix} = \begin{bmatrix} -\omega_{HWF} & \omega_{HWF} & 0 \\ 0 & -\omega_{HWF} & \omega_{HWF} \\ 0 & 0 & -\omega_{ANF} \end{bmatrix} \begin{bmatrix} i_{fb} \\ i_{HA1} \\ i_{HA2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \omega_{ANF} H_i i_{ac} \end{bmatrix} \tag{4.3}$$

Here H_i is a pure gain while the $G_{lf}(s)$ contains a second-order hardware filter and a first-order anti-aliasing filter. Variables ω_{HWF} and ω_{ANF} are the cut-off angular frequencies for the hardware filter and the anti-aliasing filter, respectively. Currents i_{HA1} and i_{HA2} are the two intermediate states of the hardware filters. The $G_{i\_g}(s)$ and F_m are the current controller in grid-tie mode and the DSP PWM modulation gain, respectively. $G_{i\_g}(s)$ is designed to be a proportional-resonant (PR) controller to achieve a low steady-state-error output. As shown in (4.4), the PR controller can be represented as a second-order equation.

$$\begin{bmatrix} \frac{di_{pr1}}{dt} \\ \frac{di_{pr2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\omega_1^2 & -2\omega_c \end{bmatrix} \begin{bmatrix} i_{pr1} \\ i_{pr2} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} i_{ref} \\ i_{fb} \end{bmatrix} \tag{4.4}$$

$$v_{dFB} = k_{pg} * (i_{ref} - i_{fb}) + 2\omega_c k_{rg} * i_{pr2}, i_{ref} = i_{ref\_pk} * v_{ac\_\theta e} = i_{ref\_pk} * \sin\theta_e$$

Here k_{pg} and k_{rg} are the proportional and resonant gains for the grid-tie mode controller. ω_c and ω_1 are the equivalent bandwidth and fundamental angular frequency, respectively. State variables i_{pr1} and i_{pr2} are two intermediate variables that represent the

state-space equation in canonical form. i_{ref}, i_{fb}, i_{ref_pk}, and $v_{ac\_\theta e}$ are the current reference, current feedback, peak current reference and synchronized unity sine term obtained from the phase-lock loop (PLL) [66]-[68], [93].

As shown in Fig. 4.3, a PLL block with the peak-value calculation (PC) is designed using an all-pass filter and D-Q transformation. The d-axis and q-axis components are calculated by the estimated angle (θ_e), filter capacitor voltage (v_{ac}), and output of all-pass filter (v_{acap}) as shown in (4.5).

$$\begin{bmatrix} v_{dpll} \\ v_{qpll} \end{bmatrix} = \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} v_{ac} \\ v_{acap} \end{bmatrix} = \begin{bmatrix} 0 \\ -V_m \end{bmatrix} \text{if } \theta_e = \theta \tag{4.5}$$

where $v_{ac} = V_m \sin\theta,\ v_{acap} = \dfrac{\omega_1 - s}{\omega_1 + s} v_{ac} = -V_m \cos\theta,\ v_{dpll} = -V_m \sin(\theta_e - \theta) \cong V_m(\theta - \theta_e)$

The output of the PLL/PC block is the synchronized term v_{ac_syn} which is obtained by multiplying the calculated magnitude v_{qf} term and synchronized unity sine term $v_{ac\_\theta e}$. Since the synchronized term v_{ac_syn} will be used for the admittance compensation, a ripple-free magnitude v_{af} is desirable to ensure smooth operations. A low-pass filter shown in (4.6) can be designed to damp the double-fundamental-frequency ripple caused by (4.5).

$$\frac{dv_{qf}}{dt} = -\omega_{pc} v_{qf} - \omega_{pc} v_{qpll} \tag{4.6}$$

Here ω_{pc} is the cut-off frequency of the peak-value-calculation filter.

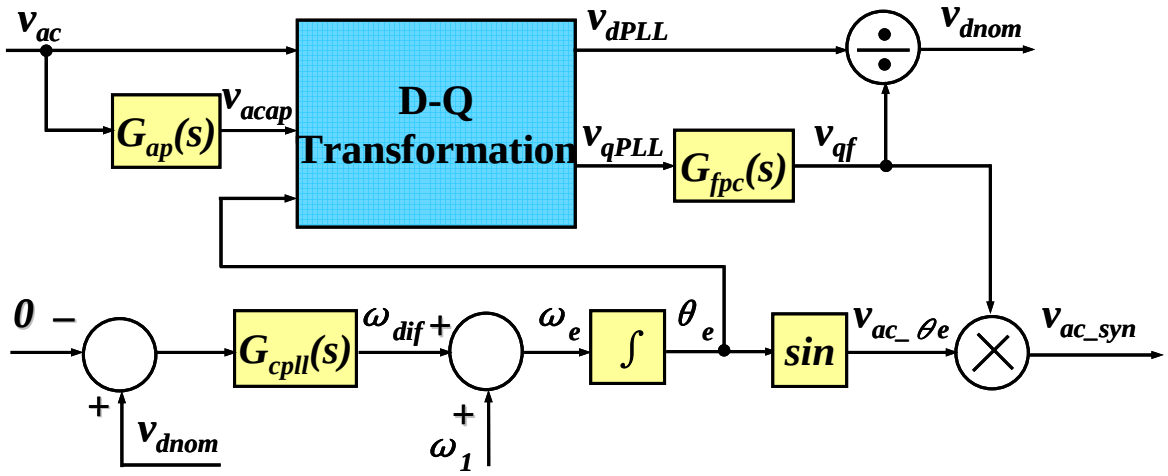


Fig. 4.3. Control block diagrams of the phase-lock loop with the peak-value calculation.

Notice that equation (4.6) is a low-pass filter with a negative sign which makes the state variable v_{qf} in steady state equal to the positive voltage magnitude, V_m. In order to design a universal PLL with a wide input voltage range, the normalized signal v_{dnom} is utilized as the feedback signal for the PLL. With an integrator as the PLL plant, a controller $G_{cpll(s)}$ is designed to have a 28-Hz cross-over frequency with a 36° phase margin. A second-order equation for the PLL controller and plant is shown in (4.7).

$$\begin{bmatrix} \frac{d\omega_{dif}}{dt} \\ \frac{d\theta_e}{dt} \end{bmatrix} = \begin{bmatrix} -\omega_{pll} & k_{pll}\omega_{pll} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \omega_{dif} \\ v_{dnom} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \omega_1 \\ \theta \end{bmatrix} = \begin{bmatrix} -\omega_{pll} & -k_{pll}\omega_{pll} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \omega_{dif} \\ \theta_e \end{bmatrix} + \begin{bmatrix} 0 & k_{pll}\omega_{pll} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \omega_1 \\ \theta \end{bmatrix} \quad (4.7)$$

where $v_{dnom} = \frac{v_{dpll}}{v_{qf}} = \frac{V_m \sin(\theta - \theta_e)}{V_m} = \theta - \theta_e = 0 \text{ if } \theta \cong \theta_e$

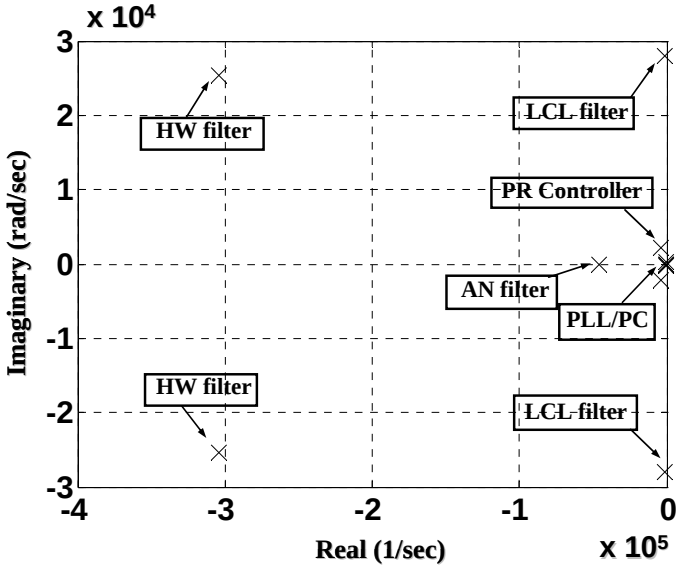
Here $\omega_{pll,}$ k_{pll} are the cut-off frequency and gain of the PLL controller. Equations (4.1) to (4.7) describe the dynamic behavior of a single-phase inverter in the grid-tie mode. The above functions can be linearized and the small-signal perturbation can be applied to derive the small signal model of the grid-tie inverter shown in (4.8).

$$\Delta \dot{X}_g = A_g \Delta X_g + B_g \Delta U_g \quad (4.8)$$

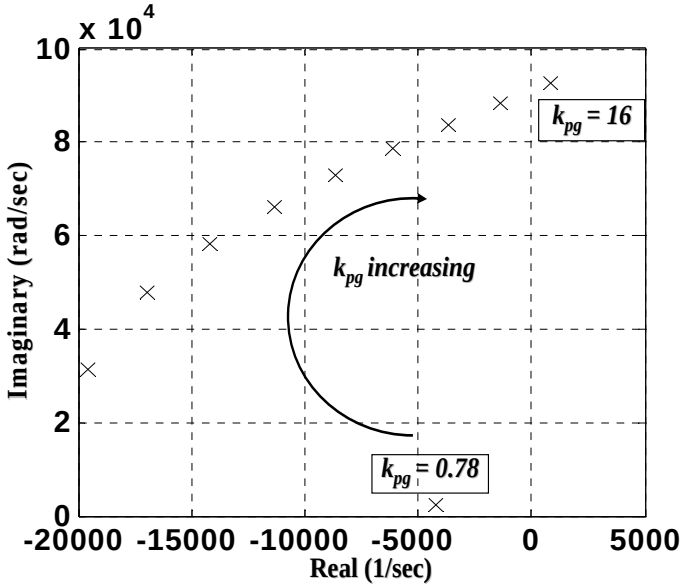
where $\Delta X_g = \left[\Delta i_{ac} \Delta i_{grid} \Delta v_c \Delta i_{fb} \Delta i_{HA1} \Delta i_{HA2} \Delta i_{pr1} \Delta i_{pr2} \Delta \omega_{dif} \Delta \theta_e \Delta v_{qf}\right]^T$, $\Delta U_g = \left[\Delta i_{ref\_pk} \Delta v_S\right]^T$

Here X_g, A_g, B_g and U_g are the state variable, state matrix, input matrix and system input to the grid-tie inverter system. In order to find the potential instability causes of the constructed model, the complete system eigenvalues are plotted in Fig. 4.4. With the

designed proportional gain k_{pg} = 0.78, Fig. 4.4(a) shows that none of the eigenvalue is located in the right-hand plane, and the system is stable. Notice that the system eigenvalues keep at almost the same positions when the current reference magnitude i_{ref_pk} changes from 20% to full load, which suggests that the stability of grid-tie mode is not related much to a load change. By varying k_{pg}, however, the system becomes unstable when k_{pg} exceeds 16 as shown in Fig. 4.4(b).



(a)



(b)

Fig. 4.4. Eigenvalue of grid-tie inverter (a) complete eigenvalue for k_{pg} = 0.78, and (b) the critical eigenvalue changes with varying k_{pg} from 0.78 to 16.

4.3 Modeling and analysis of single inverter in standalone mode

Fig. 4.1(b) shows the hardware configuration of a single inverter in the standalone mode. If the load is only a pure resistor with resistance R_{load}, then the plant equation can be expressed by a third-order system, as shown in (4.9).

$$\begin{bmatrix} L_i & 0 & R_cC_f \\ 0 & L_g & -R_cC_f \\ 0 & 0 & C_f \end{bmatrix} \begin{bmatrix} \frac{di_{ac}}{dt} \\ \frac{di_{load}}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} R_{Li} & 0 & -1 \\ 0 & -R_{Lg}-R_{load} & 1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} i_{ac} \\ i_{load} \\ v_c \end{bmatrix} + \begin{bmatrix} V_{dc} \\ 0 \\ 0 \end{bmatrix} [d] \tag{4.9}$$

Fig. 4.5 shows that an outer voltage loop is used to regulate the output voltage while an inner current loop is adopted to damp the LCL resonance poles. As shown in (4.10), the current controller in the standalone mode $G_{i\_s}(s)$ is designed as a first-order low-pass filter to damp the LCL resonance.

$$\frac{dv_{dFB}}{dt} = -\omega_{SWF} * v_{d1} + 0.5\omega_{SWF} * i_{err} \tag{4.10}$$

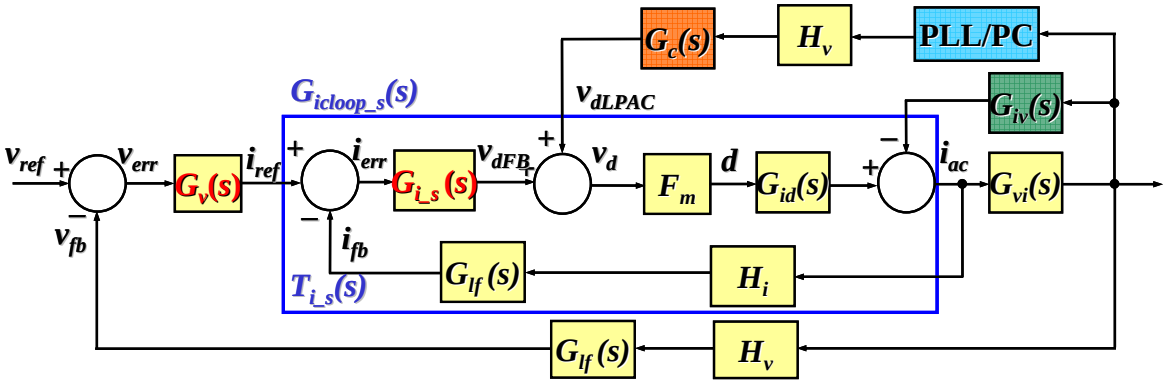


Fig. 4.5. Control block diagrams of a single inverter in standalone mode with admittance compensation.

The voltage loop also contains a third-order filter $G_{lf}(s)$ with a similar equation as expressed in (4.3) except that the currents variables change to the voltage variables. In order to achieve a high loop gain at the fundamental frequency to minimize the steady-state error, the voltage controller $G_v(s)$ is also designed to be a PR controller which leads to a second-order equation that has a similar form in (4.4) except that the current variables change to the voltage ones. The current reference generation can be represented in (4.11).

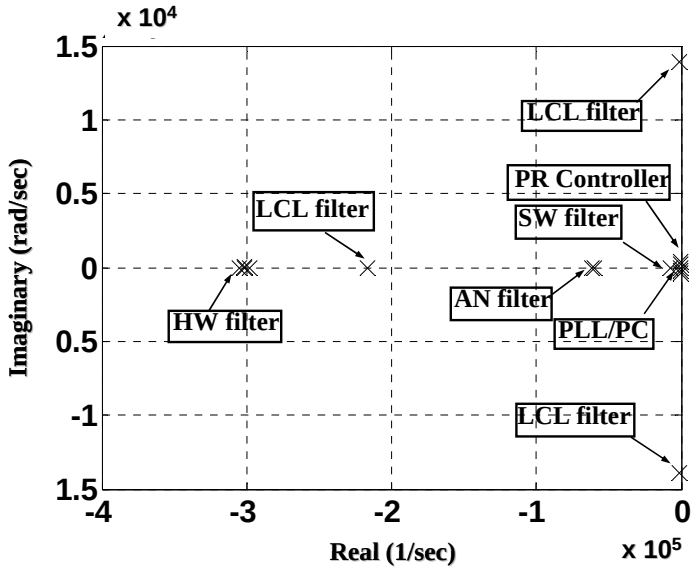
$$i_{ref} = k_{ps} * (v_{ref} - v_{fb}) + 2\omega_c k_{rs} * v_{pr2} \tag{4.11}$$

Here v_{ref} is the voltage reference. The above transfer functions from (4.9) to (4.11) can be linearized and the small-signal perturbations can be applied to derive the small-signal model of the standalone-mode inverter shown in (4.12).

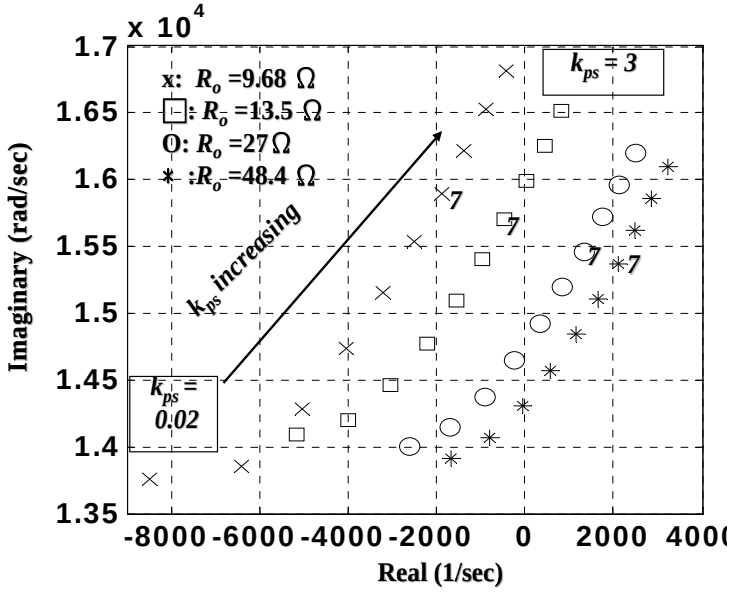
$$\Delta\dot{X}_s = A_s \Delta X_s + B_s \Delta U_s \tag{4.12}$$

$$\text{where } \Delta X_S = \left[\Delta i_{ac} \Delta i_{load} \Delta v_c \Delta i_{fb} \Delta i_{HA1} \Delta i_{HA2} \Delta v_{dFB} \Delta v_{fb} \ \Delta v_{HA1} \Delta v_{HA2} \Delta v_{pr1} \Delta v_{pr2} \Delta\omega_{dif} \Delta\theta_e \Delta v_{qf} \right]^T, \Delta U_S = \left[\Delta v_{ref} \right]^T$$

Here X_s, A_s, B_s and U_s are the state variable, state matrix, input matrix and system input corresponding to the inverter in the standalone mode. The complete system eigenvalues are shown in Fig. 4.6 to validate the state-space model. Fig. 4.6(a) shows that the system is stable with the designed proportional gain k_{ps} = 0.02. With varying k_{ps} and R_{load}, Fig. 4.6(b) suggests that the system become more unstable when R_{load} increases or when k_{ps} increases. With k_{ps} = 2, the seventh points on Fig. 4.6(b) indicates that the system is stable for R_{load} = 13.5 Ω, but not for R_{load} = 27 Ω.



(a)



(b)

Fig. 4.6. Eigenvalue of standalone inverter (a) complete eigenvalue for k_{pg} = 0.02, and (b) the critical eigenvalue changes with the varying k_{pg} and load R_{load}.

4.4 Modeling and analysis of parallel inverters with the current sharing controller

Fig. 4.7 shows the hardware of the mircogrid system in the islanding mode. As shown in Fig. 4.8, the state-space model of the mircogrid system in the islanding mode can be obtained by combining the derived equations in above sections and the current sharing controller. In order to extend the transmission distance, the transmitted signal is a frequency-decoupled current magnitude. The frequency information does not need to be transmitted because it will be automatically tracked by the PLL. As shown in Fig. 4.8, a PC block is used to calculate the frequency-decoupled current magnitude information for the current sharing.

Assume that the load is only a pure resistor, then estimated phases in voltage PLL can be used to calculate the current magnitude similar to the approach shown in (4.5) except the input becomes currents, i_{ac1} and i_{ac2}. After the D-Q transformations, two low-pass filters with the similar expression in (4.6) are utilized to filter the double-fundamental-frequency ripples. Once the transmitted current magnitude of the voltage-controlled inverter (i_{out1_pk}) and the calculated magnitude of the current-controlled inverter (i_{out2_pk}) are obtained, the automatic reference generation (ARG) adjusts the current reference magnitude of the current-controlled inverter i_{ref2_pk} to share the inverter currents. The ARG control algorithm can be implemented digitally as described in chapter 3 or a simple proportional-integral (PI) controller in (4.13).

$$i_{ref2\_pk} = i_{ac1\_pk} + i_{ref2\_offset} \tag{4.13}$$

where $i_{ref2\_offset} = (i_{ac1\_pk} - i_{ac2\_pk}) * \left[\frac{sT_w}{1+sT_w} (k_{pcs} + \frac{1}{s} k_{ics}) \right]$

Here i_{ref2_offset} is the offset of the current reference. T_w, k_{pcs}, k_{pis} are the washout-term time constant, proportional gain and integral gain of the PI controller. By combining state-state equations from (4.1) to (4.13) and applying the perturbations to these equations, the complete small-signal model of the parallel-inverter system can be derived in (4.14).

$$\Delta \dot{X}_i = A_i \Delta X_i + B_i \Delta U_i \tag{4.14}$$

where

$$\Delta X_i = \left[\Delta i_{ac1} \Delta i_{load1} \Delta v_{c1} \Delta i_{fb1} \Delta i_{HA11} \Delta i_{HA21} \Delta v_{dFB1} \Delta v_{fb1} \Delta v_{HA11} \Delta v_{HA21} \right.$$
$$\Delta v_{pr11} \Delta v_{pr21} \Delta \omega_{dif1} \Delta \theta_{e1} \Delta v_{qf1} \Delta i_{ac2} \Delta i_{grid2} \Delta v_{c2} \Delta i_{fb2} \Delta i_{HA12}$$
$$\left. \Delta i_{HA22} \Delta i_{pr12} \Delta i_{pr22} \Delta \omega_{dif2} \Delta \theta_{e2} \Delta v_{qf2} \Delta i_{ac1\_pk} \Delta i_{ac2\_pk} \Delta i_{ref2\_pk} \right]^T$$
$$\Delta U_i = \left[\Delta v_{ref} \right]^T$$

Here X_i, A_i, B_i and U_i are the state variable, state matrix, input matrix, and system input correspondingly of the microgrid system in the islanding mode.

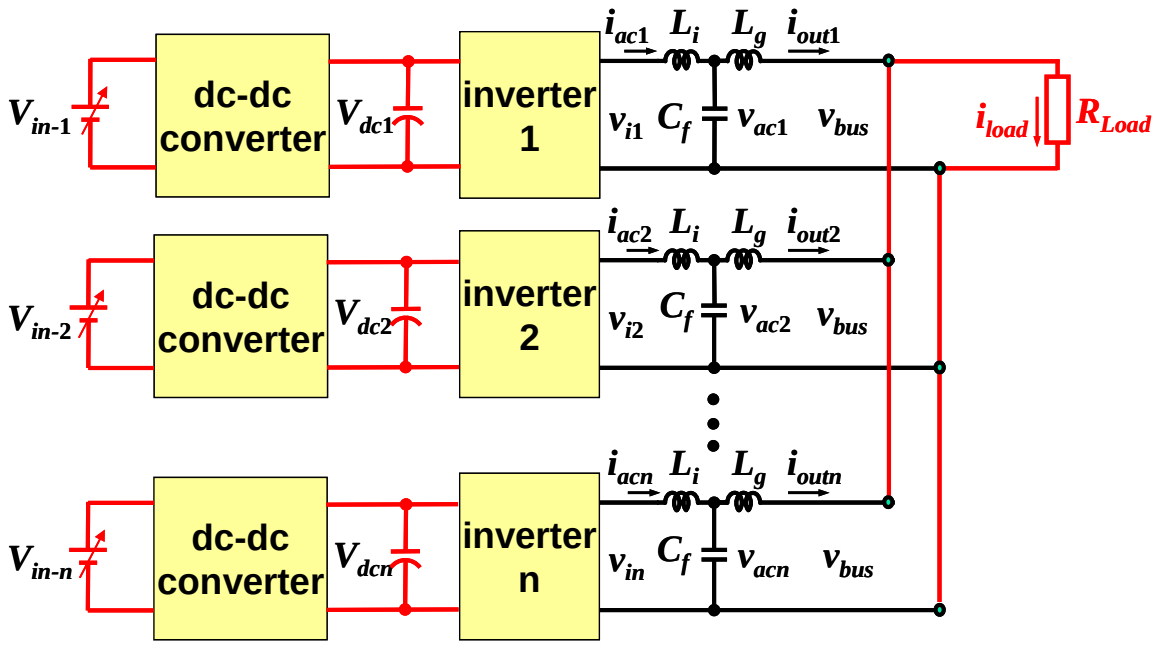


Fig. 4.7. The hardware of parallel-inverter microgrid system in islanding mode.

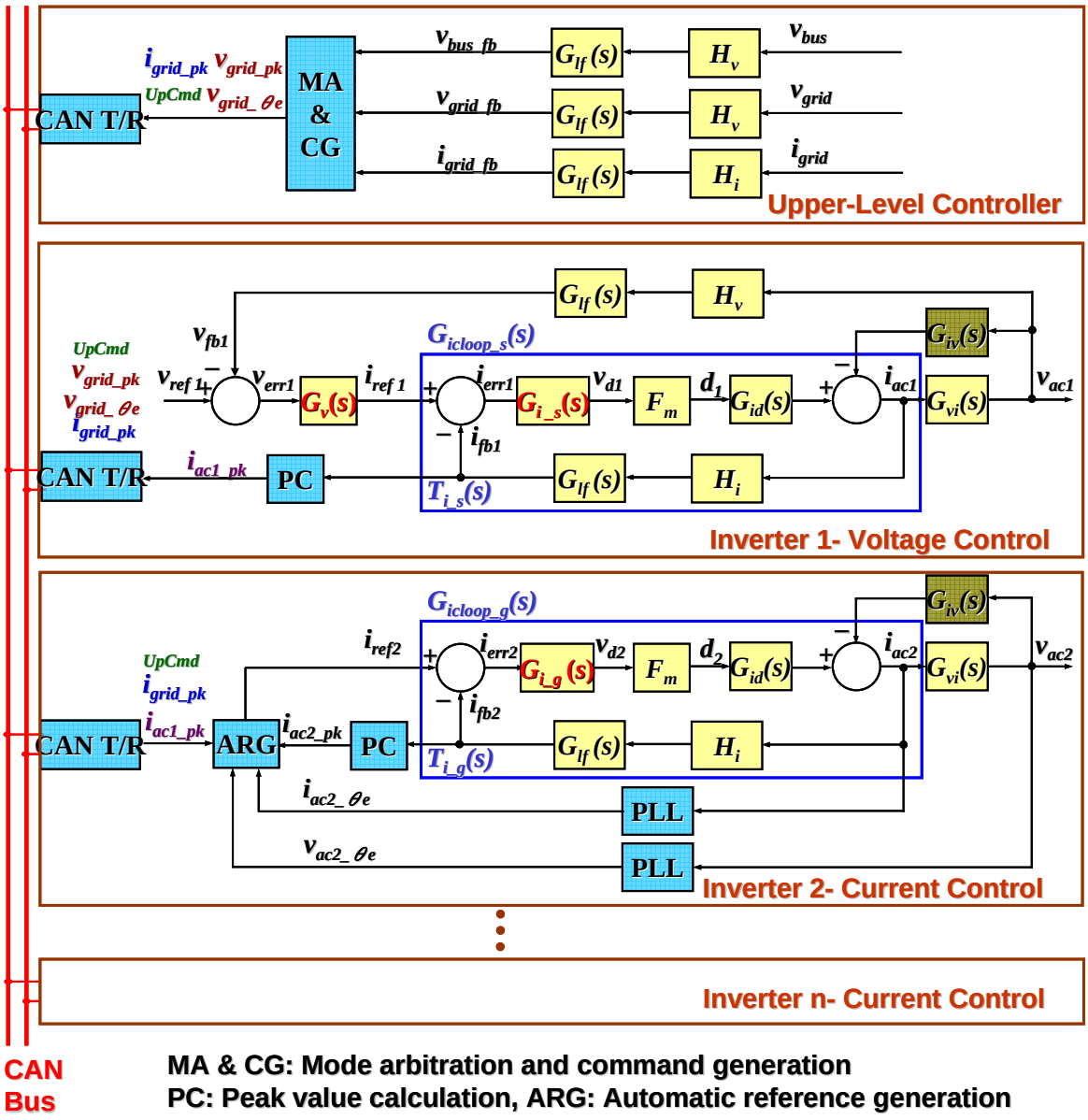
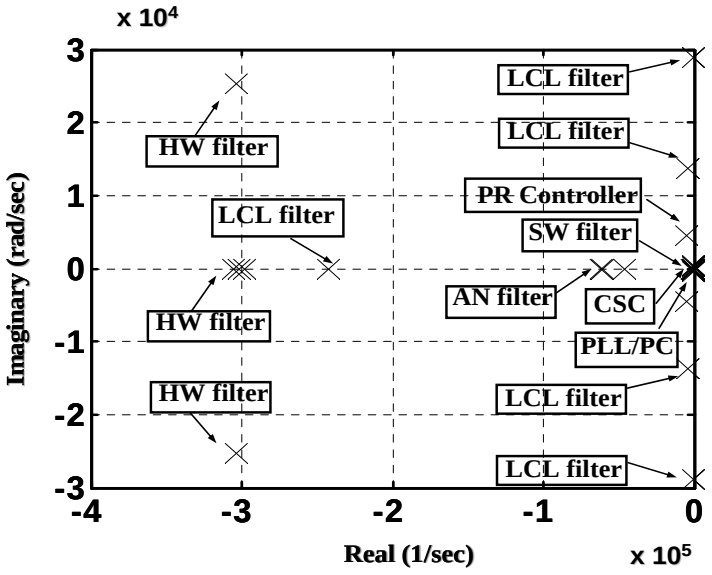
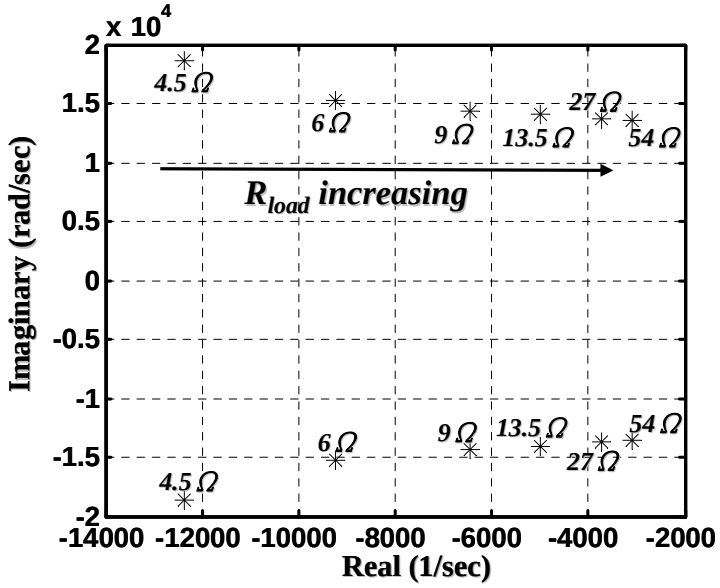


Fig. 4.8. The control block diagram of parallel-inverter microgrid system in islanding mode.

Fig. 4.9(a) shows that the system is stable with the designed controller gains at about 16% load or R_{load} = 27 Ω. Fig. 4.9(b) suggests that the system stays stable from 8% load (R_{load} = 54 Ω) to 100% load (R_{load} = 4.5 Ω). Another observation is that the eigenvalues in Fig. 4.9 stay almost unchanged regardless of the variations of current-sharing controller parameters k_{pcs} and k_{pis}. As shown in (4.13), i_{ref_offset} is close to zero because i_{ac1_pk} almost equals i_{ac2_pk} during the steady state. However, the current-sharing controller parameters, k_{pcs} and k_{pis}, will change the dynamic response when the output current magnitudes, i_{ac1_pk} and i_{ac2_pk}, are not equal.



(a)

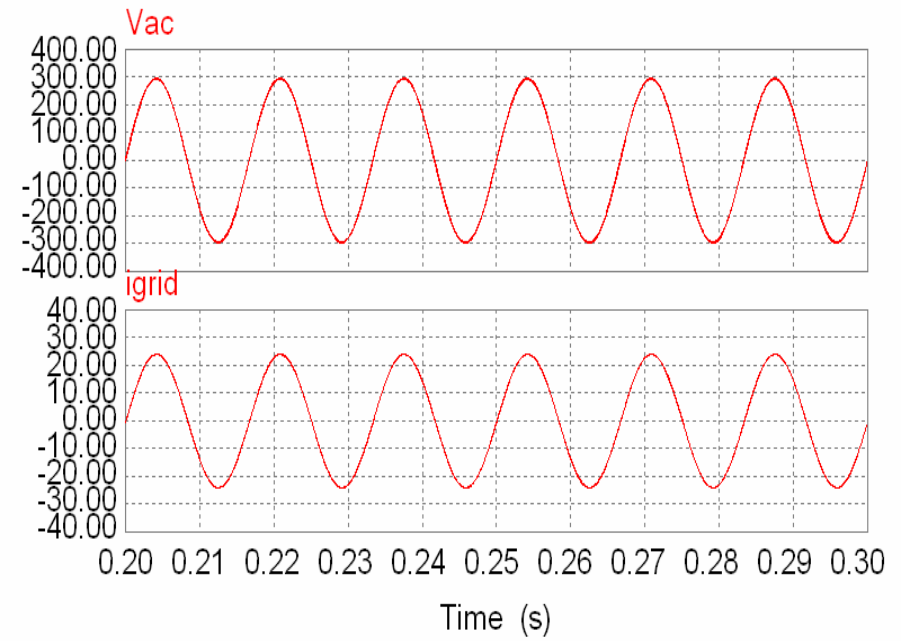


(b)

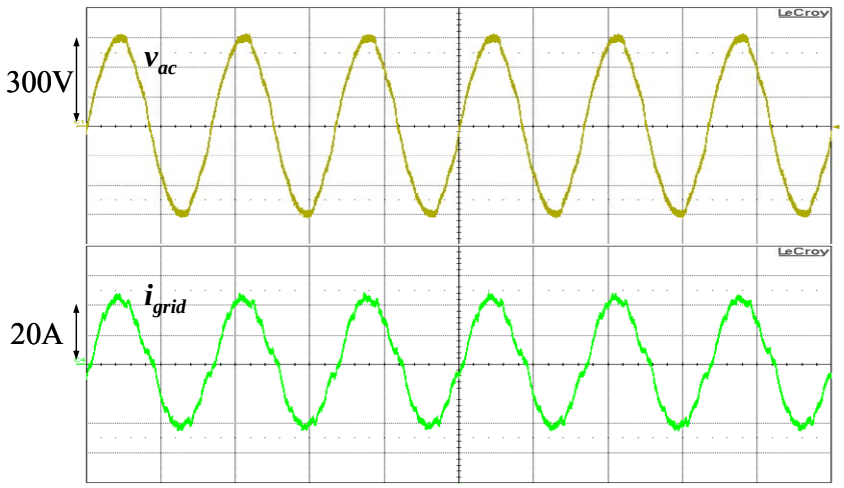
Fig. 4.9. Eigenvalues of the microgrid system in islanding mode (a) complete eigenvalues for R_{load} = 27 Ω, and (b) the critical mode eigenvalue changes with varying R_{load}.

4.5 Simulation and experimental verification

Fig. 4.10 shows the simulation and experimental results of a single-phase inverter running in the steady-state grid-tie mode at 3.2kW condition. Waveforms indicate that the system is stable with the designed controllers (k_{pg} = 0.78). Fig. 4.11 shows the transient simulation and experimental results of a single inverter running in the grid-tie mode. With the designed controller parameters, the system is stable even the output power changes from 1.8kW to 3.6kW which agrees with stability trend of the eigenvalue analysis shown in Fig. 4.4. Notice the response in the grid-tie application is intentionally set in the second range because the slow dynamic of the utility grid. With the increased controller gain (k_{pg} = 16) in the grid-tie mode, Fig. 4.12 shows the unstable results of the current loop which the current loop output current i_{Li} has a resonance around 14.5k Hz. Fig. 4.12(b) is the room-in result of i_{Li} waveform in Fig. 4.12(a). Fig. 4.12(c) and 4.12(d) shows the frequency spectrum and the Bode plot result of this set of controller gain. The eigenvalue results in Fig 4.4(b) can be verified by Fig. 4.12 which the resonance frequencies are almost the same. Notice that the switching frequency of simulation in Fig. 4.12 is intend to set to a relative high switching frequency, 200k Hz, in order to see this 14.5k Hz resonance. However, for the real implementation, a 20k Hz switching frequency is chosen for the IGBT power device.



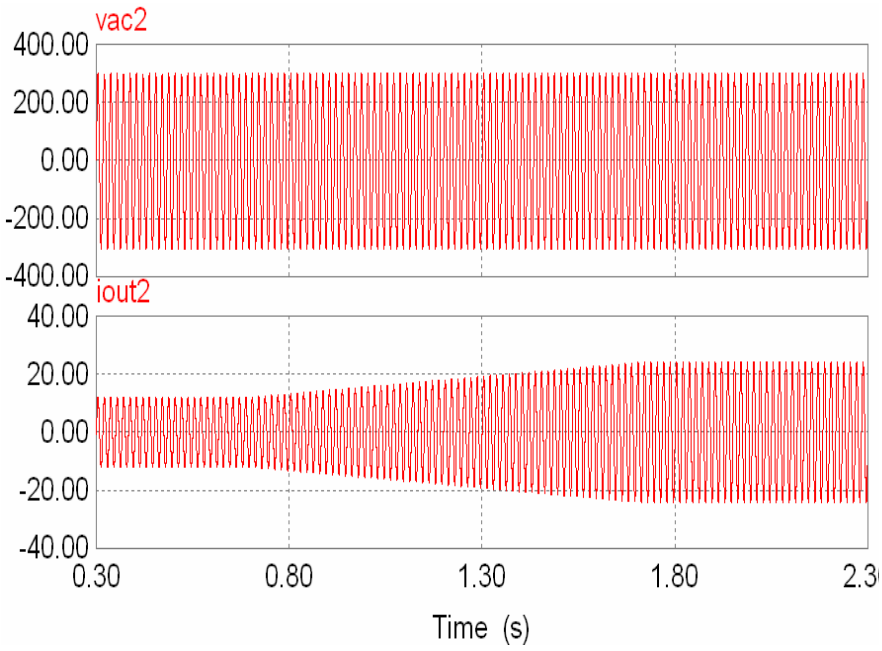
(a)



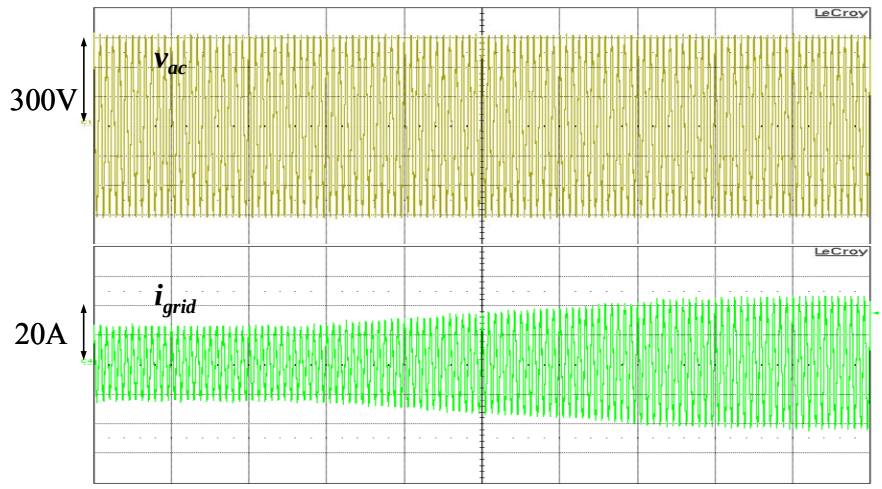
t:10ms/div

(b)

Fig. 4.10. Grid-tie mode results at 3.2 kW with k_{pg} = 0.78 and k_{rg} = 97.5 (a) simulation results, and (b) experimental results.



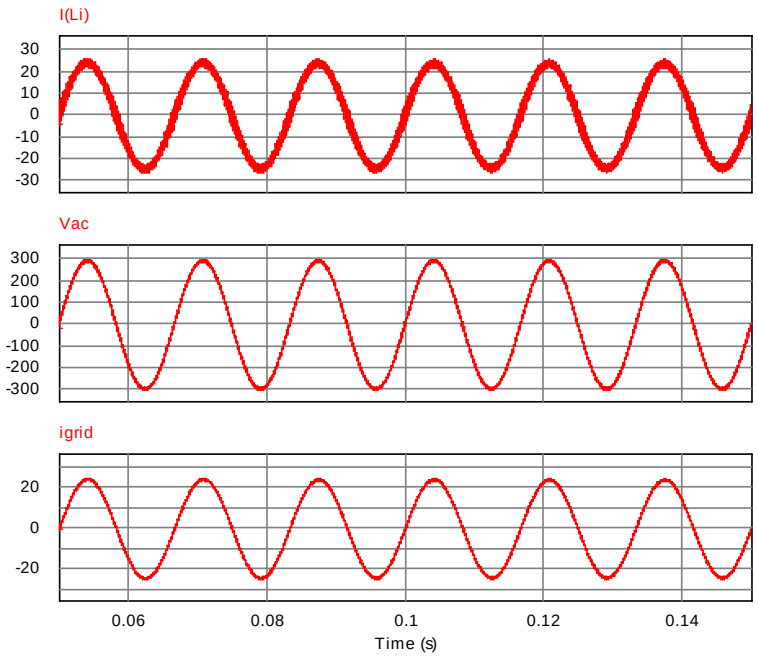
(a)



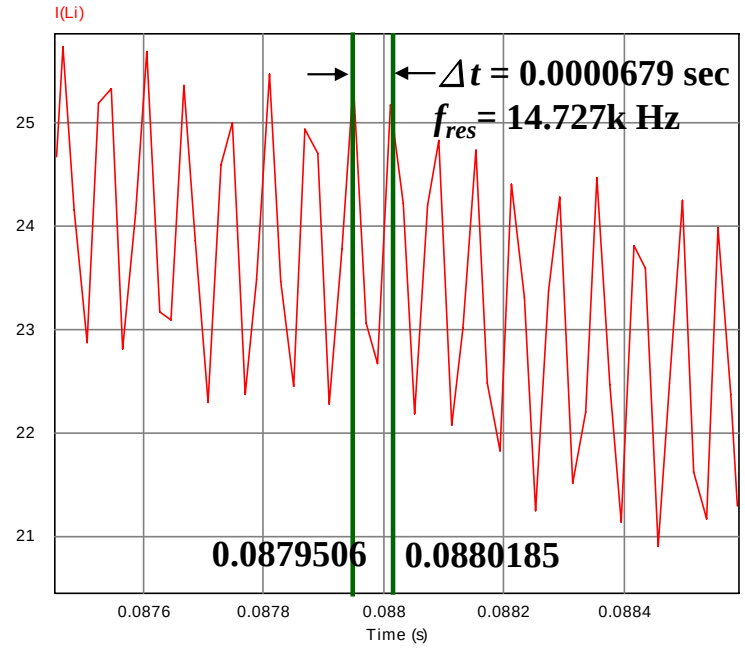
(b)

Fig. 4.11. Transient grid-tie mode results from 1.8 kW to 3.6kW

with k_{pg} = 0.78 and k_{rg} = 97.5 (a) simulation results, and (b) experimental results.

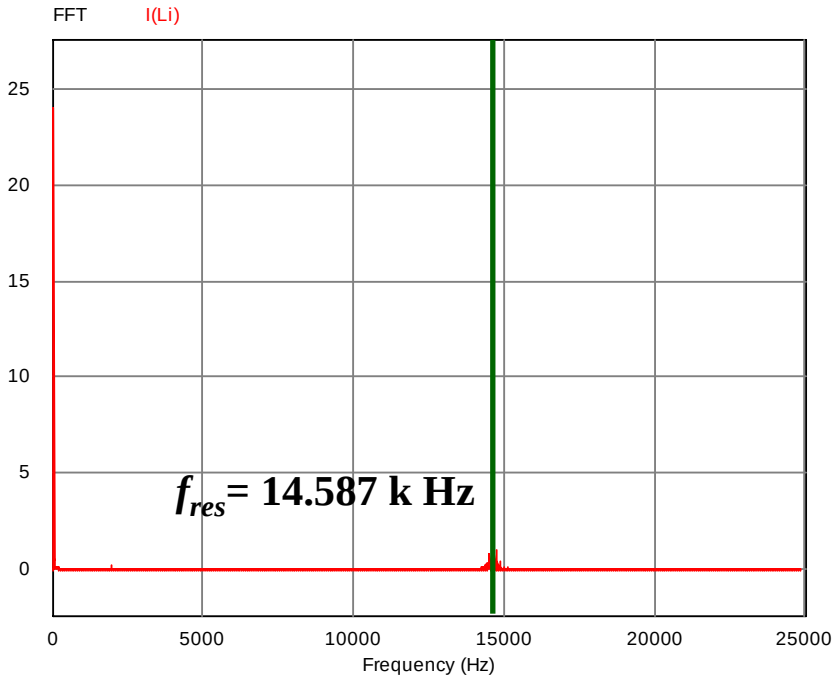


(a)

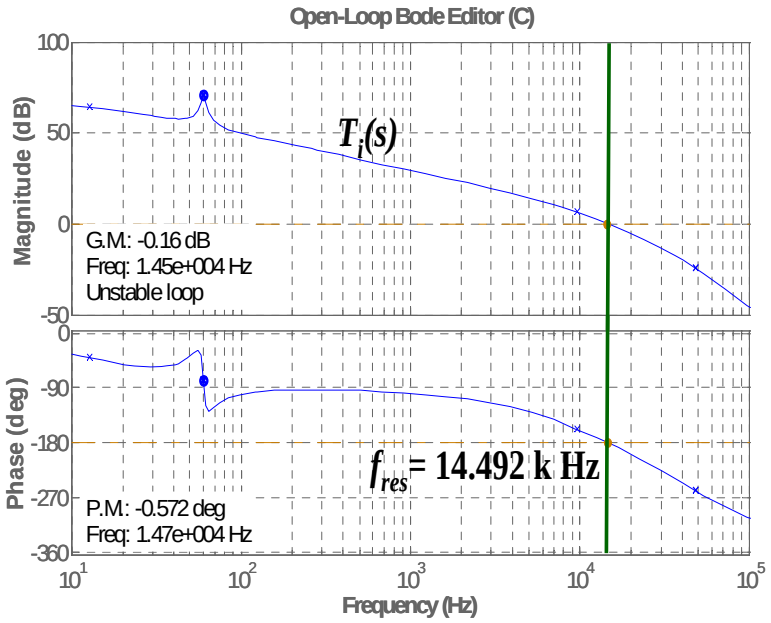


(b)

Fig. 4.12. Grid-tie mode results at 3.2 kW with k_{pg} = 16 and k_{rg} = 97.5 (a) time-domain simulation result, (b) zoom in time-domain result.



(c)

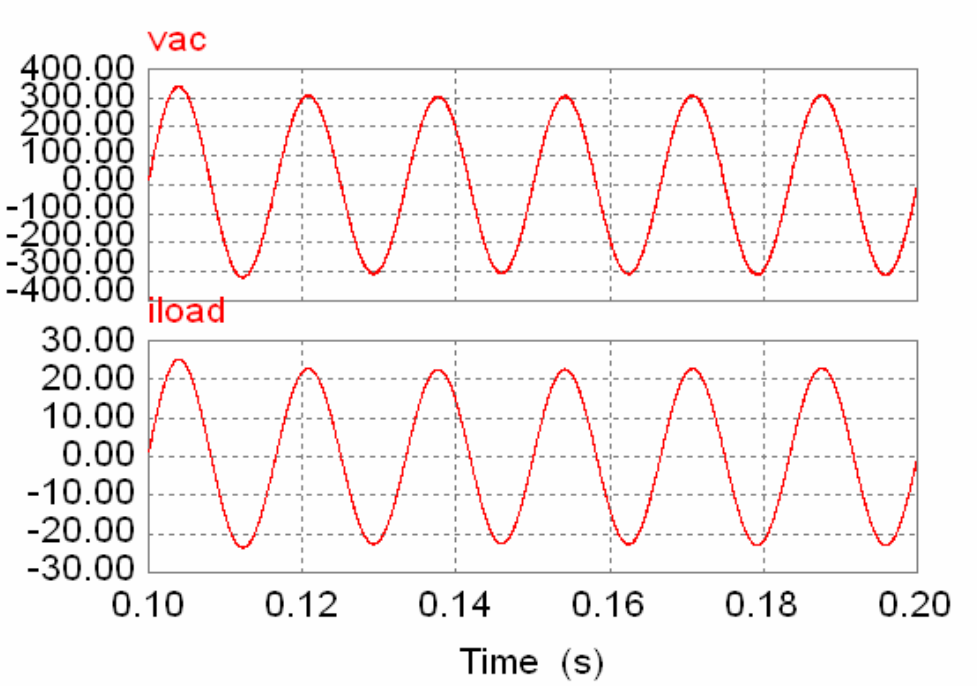


(d)

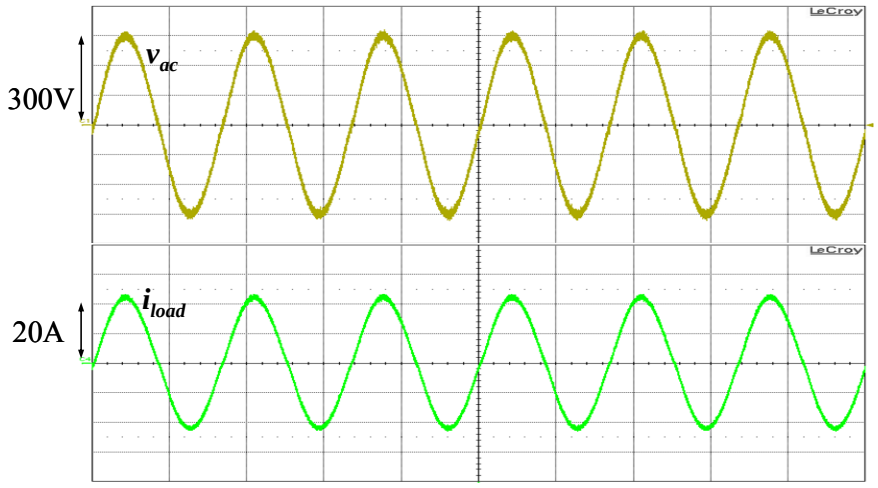
Fig. 4.12. Grid-tie mode results at 3.2 kW with k_{pg} = 16 and k_{rg} = 97.5 (c) frequency spectrum of time-domain waveform, and (d) the bode plot of current loop.

Fig. 4.13 shows the simulation and experimental results of a single-phase inverter running in the steady-state standalone mode at 3.2kW condition. Waveforms indicate that the system is stable with the designed controllers (k_{ps} = 0.02 and k_{rs} = 12) and this load condition (R_{load} = 13.5 Ω). Fig. 4.14 shows the simulation and experimental results of single-phase inverter running under the standalone-mode dynamic load step with the load changing from R_{load} = 27 Ω to R_{load} = 13.5 Ω using k_{ps} = 0.02 and k_{rs} = 12. The waveforms show that the system is stable with these controller parameters. Both simulation and experimental results agree with the stability trend predicted by the eigenvalue analysis shown in Fig. 4.6(b).

To further verify that the system can run unstable with an increased proportional gain, as predicted in Fig. 4.6, the system was simulated using k_{ps} = 2 and k_{rs} = 12. Simulation results shown in Fig. 4.15 indicate that initially when the load is 27 Ω, the system is unstable. With the same controller, when the load is increased to R_{load} = 13.5 Ω, the system becomes stable. This simulation result again validates the eigenvalue analysis results shown in Fig. 4.6(b).



(a)

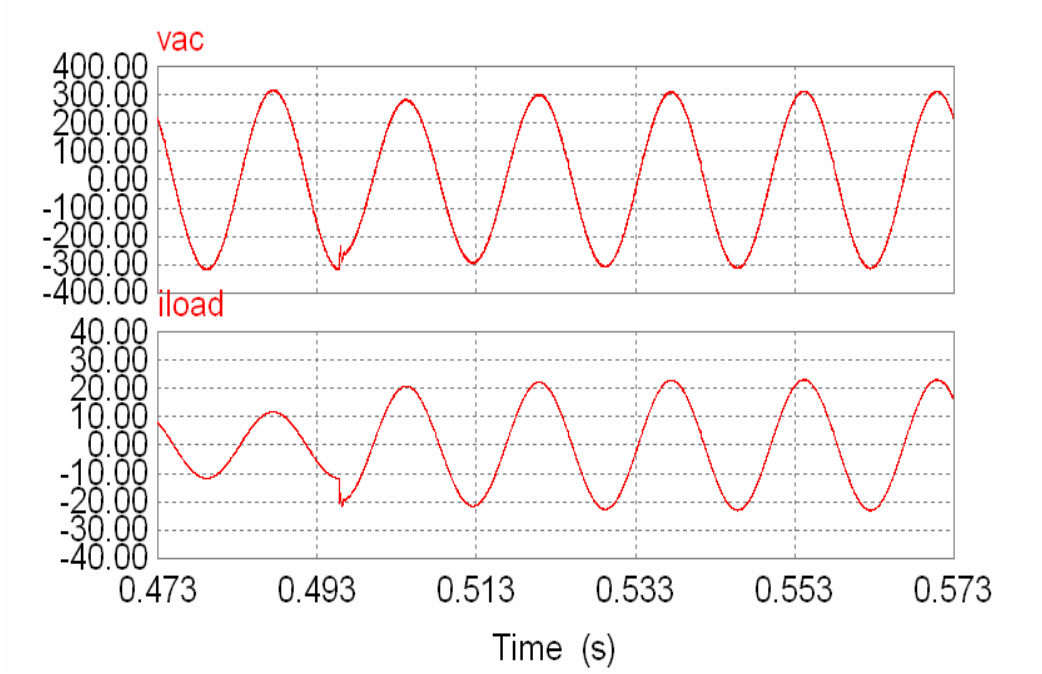


t:10ms/div

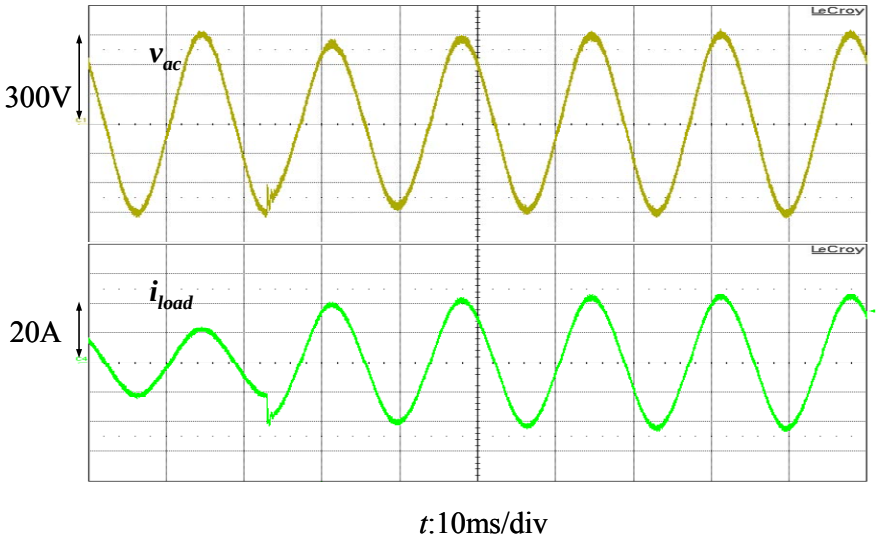
(b)

Fig. 4.13. Standalone mode results at 3.2 kW with k_{ps} = 0.02 and k_{rs} = 12

(a) simulation results, and (b) experimental results.



(a)



(b)

Fig. 4.14. Transient standalone mode results from R_{load} = 27 Ω to R_{load} = 13.5 Ω with k_{ps} = 0.02 and k_{rs} = 12 (a) simulation results, and (b) experimental results.

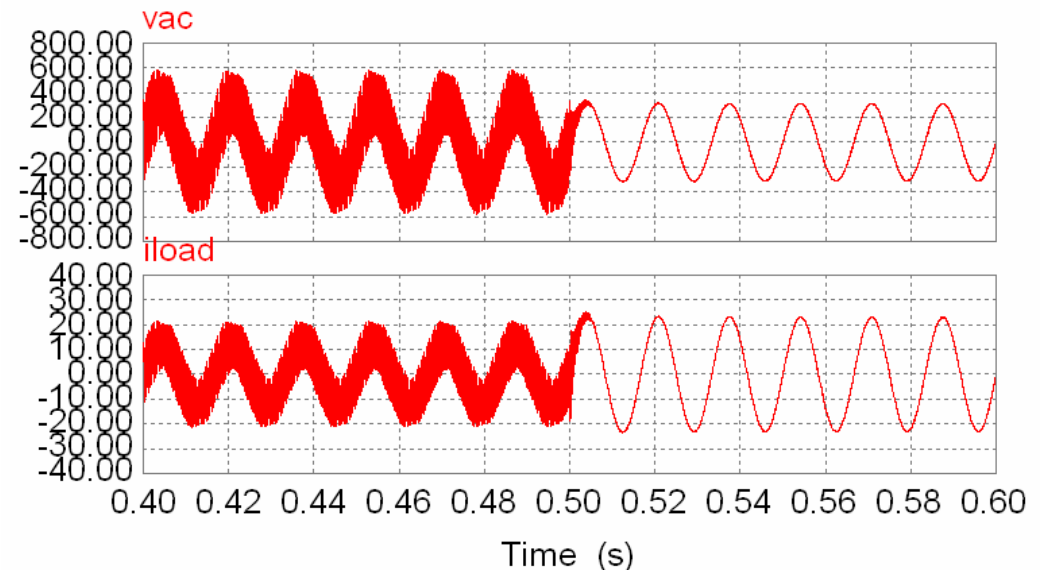
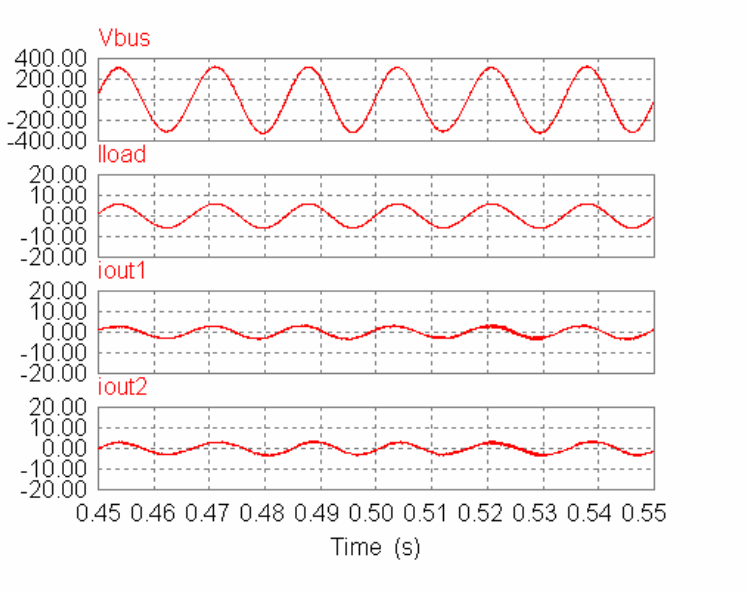
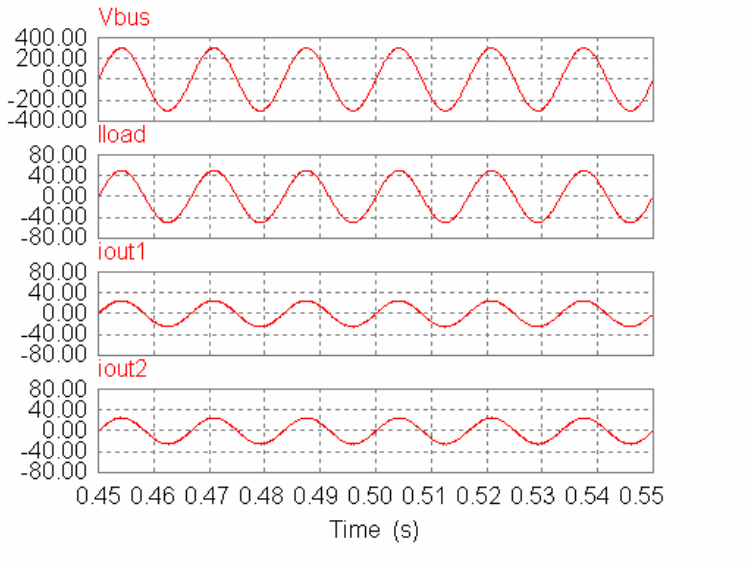


Fig. 4.15. Transient standalone simulation results from R_{load} = 27 Ω to R_{load} = 13.5 Ω with k_{ps} = 2 and k_{rs} = 12.

Fig. 4.16 and Fig. 4.17 show the simulation and experimental results of the mircogrid system in the islanding mode at light load (R_{load} = 54 Ω) and heavy load (R_{load} = 6 Ω), respectively. Waveforms suggest that the system is stable within this load range which agrees with the stability trend of eigenvalue analysis in Fig. 4.9. Fig. 4.18 shows the simulation and experimental results of the parallel-inverter system running under the islanding-mode dynamic load step with the load changing from R_{load} = 27 Ω to R_{load} = 13.5 Ω. The waveforms show that the system is stable with the designed controller which validates the eigenvalue analysis predictions shown in Fig. 4.9.



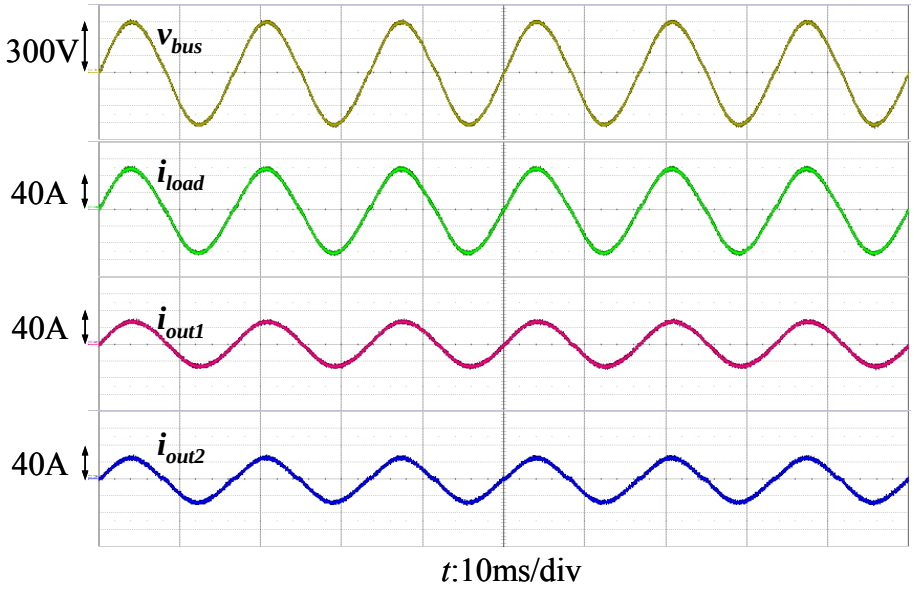
(a)



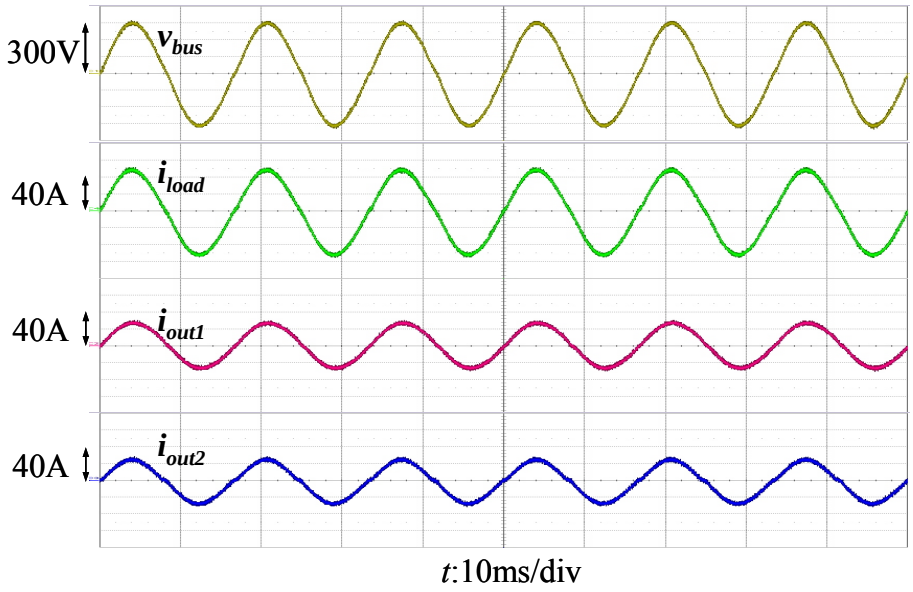
(b)

Fig. 4.16. Simulation results of the microgrid system in islanding mode

(a) P_{out} = 800 W (R_{load} = 54 Ω) and, (b) P_{out} = 7.4 kW (R_{load} = 6 Ω).



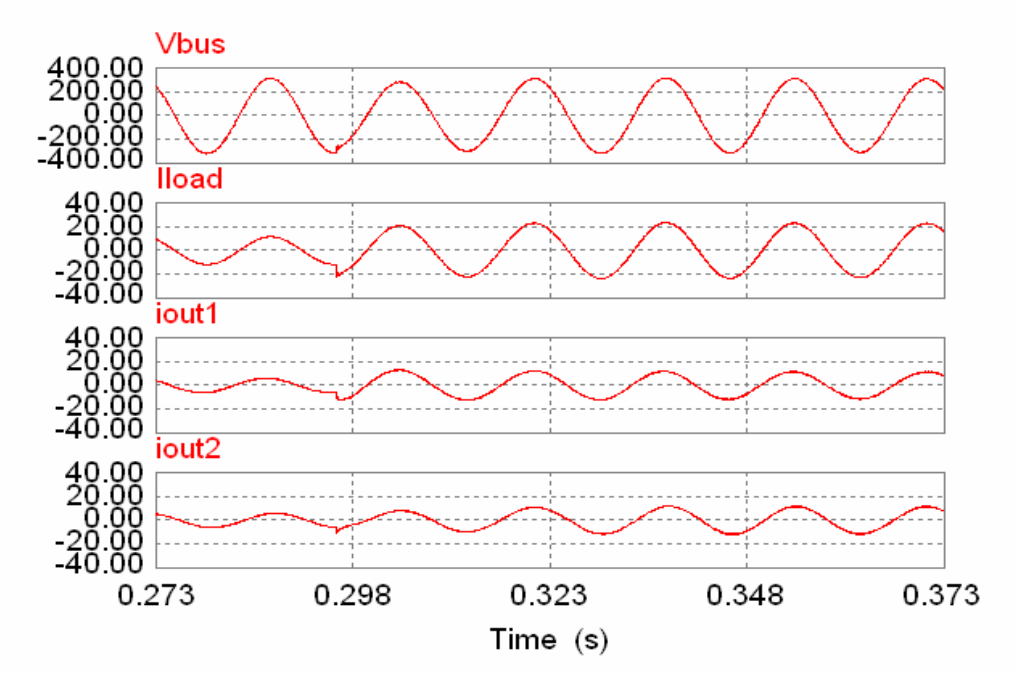
(a)



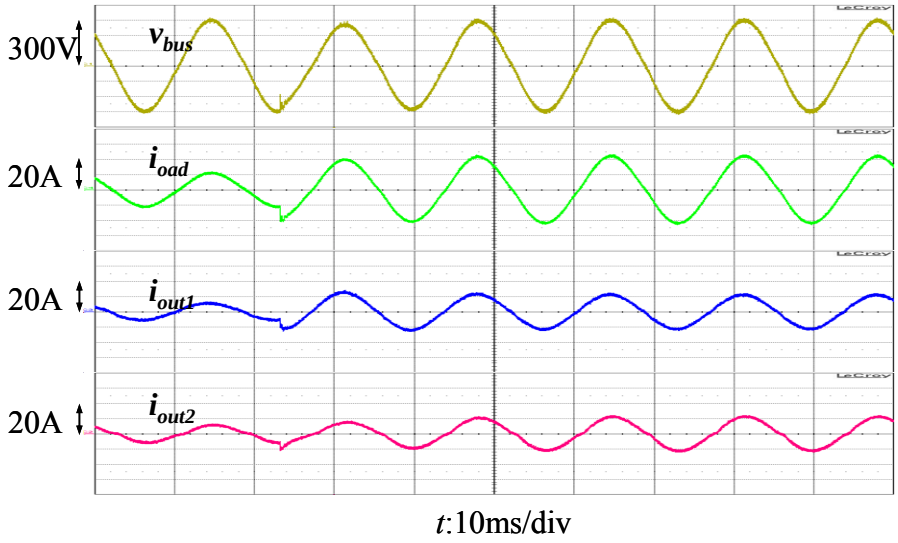
(b)

Fig. 4.17. Experimental results of the microgrid system in islanding mode

(a) P_{out} = 800 W (R_{load} = 54 Ω) and, (b) P_{out} = 7.4 kW (R_{load} = 6 Ω).



(a)



(b)

Fig. 4.18. Transient results of the microgrid system in islanding mode from R_{load} = 27 Ω to R_{load} = 13.5 Ω (a) simulation results, and (b) experimental results.

4.6 Summary

The state-space model and implementation results of a microgrid system operating in the grid-tie mode, standalone mode and the parallel-inverter mode (islanding mode) were presented in this chapter. Through the state-space analysis of the model, the following conclusions can be drawn:

1. Eigenvalue analysis for grid-tie mode

   The grid-tie system tends to be more unstable with increased proportional gain k_{pg} since the critical eigenvalue moves toward the right-half plane. The system eigenvalues do not change much with the increased current reference magnitude which implies the stability of grid-tie mode is not much related to the load change.

2. Eigenvalue analysis for the standalone mode

   With the increased proportional gain k_{ps} and load resistance R_{load}, the standalone system becomes more unstable; the critical eigenvalue moves closer to the right-half plane.

3. Eigenvalue analysis for islanding mode

   With the increased load resistance, R_{load}, the microgrid system in islanding mode stays stable but the critical eigenvalue moves closer to the right-half plane. Changes in current-sharing controller gains have very little effects on the steady-state eigenvalue results.

With the designed controller parameters, experimental and simulation results show the stable output waveforms in single-phase grid-tie mode, single-phase standalone mode and the parallel-inverter microgrid system in islanding mode. With a higher controller gain in the standalone mode, the simulation results show that the system is stable for the heavier load condition but will become unstable in the lighter load condition. This agrees with the stability trend in the eigenvalue analysis. For the grid-tie mode, the simulation results also verify the model effectiveness by changing the controller gain. The eigenvalue analysis of the parallel inverter system in islanding mode shows that the designed controllers make the system stable from light load to heavy load. This analysis result of the stable operation is confirmed by both the simulation and experimental results in the proposed multi-inverter microgrid system.

Chapter 5

Conclusion and Future Works

5.1 Summary and major contributions

This dissertation presents a complete design and implementation of an experimental microgrid with paralleled power conditioning systems operating in the grid-tie mode, islanding mode, and mode transfers. Major contributions of the dissertation can be summarized as follows:

1. The universal inverter is designed and implemented with the LCL filter which successfully operates in both grid-tie and standalone mode without any hardware modification.

2. In grid-tie mode, the reverse power flow issue during the grid-tie connection transient is eliminated by the proposed admittance compensation. Precision steady-state current control is achieved by adapting the high-gain PR controller.

3. In standalone mode, a dual-loop voltage controller with inner current loop is designed to have the inherent current limitation to improve system reliability. Outer

voltage loop controller is designed with a PR controller to minimize the steady-state error.

4. Equal current sharing among parallel inverters within the microgrid is fulfilled through a frequency-coupled-signal transmission scheme without an extreme high bandwidth communication channel. The phase synchronization is implemented with PLL and an automatic phase adjustment.

5. Smooth mode transfers of a multiple-inverter microgrid system are achieved by the proposed mode transfer algorithms based on the circuit principles to minimize the excessive electrical stresses.

6. The state-space model and eigenvalue analysis are initially conducted in the single inverter and extended to the parallel-inverter microgird system to investigate the stability under system variations and optimize the trade-off between the performance and stability.

5.2 Future works

1. Extending the developed control strategies in fuel-cell DGs to intermittent energy sourced DGs by modifying the command generation section.
2. Incorporating a storage system into the proposed microgrid system to supply the transient load requirement and allow the existence of the intermittent energy sources in the islanding mode.
3. Applying the advanced control strategies such as sliding mode control to improve the system dynamics and enhance the system immunity to the system disturbance and parameter change.
4. Implementing an energy-management system in the existing microgrid system to minimize the operation cost and enhance the system reliability.

5.3 Publications

- **C. L. Chen**, Y. B. Wang, J. S. Lai, Y. S. Lee, and D. Martin, "Design of parallel inverters for smooth mode transfer microgrid applications ," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 6-15, Jan. 2010.
- S. Y. Park, **C. L. Chen**, and J. S. Lai, "A wide-range active and reactive power flow controller for a solid oxide fuel cell power conditioning system," *IEEE Trans. Power Electron.*, vol. 23, pp. 2703-2707, Nov. 2008.
- S. Y. Park, **C. L. Chen**, J. S. Lai, and S. R. Moon, "Admittance compensation in current Loop control for a grid-tie LCL fuel cell inverter," *IEEE Trans. Power Electron.*, vol. 23, pp. 1716-1723, July 2008.
- **C. L. Chen**, Y. S. Lee, J. S. Lai and D. Martin, "State-space modeling, analysis, and implementation of paralleled inverters for microgrid applications," in *Proc. of IEEE APEC*, Feb. 2010, pp. 619-626.
- **C. L. Chen**, Y. B. Wang, and J. S. Lai, "Design of parallel inverters for smooth mode transfer micogrid applications," in *Proc. of IEEE APEC*, Feb. 2009, pp. 15-19.
- **C. L. Chen**, J. S. Lai, Y. B. Wang, S. Y. Park, and H. Miwa, "Design and control for LCL-based inverters with both grid-tie and standalone parallel operations," in *Proc. of IEEE IAS*, Oct. 2008, pp. 1-7.
- S. Y. Park, **C. L. Chen**, and J. S. Lai, "A wide-range active and reactive power flow controller for a solid oxide fuel cell power conditioning system," in *Proc. of IEEE APEC*, Feb. 2008, pp. 952 - 958.

- **C. L. Chen**, S. Y. Park, J. S. Lai, S. Moon, “Admittance compensation in current loop control for a grid-tie LCL fuel cell inverter,” in *Proc. of IEEE PESC*, Jun. 2007, pp. 520-526.
- S. Y. Park, J. S. Lai, **C. L. Chen**, S.R. Moon and T-W. Chun, "Current loop control with admittance compensation for a single-phase grid-tie fuel cell power conditioning system," in *Proc. of IEEE APEC*, Feb. 2007, pp. 1010 - 1016.
- J. S. Lai, S. Y. Park, S. R. Moon, and **C. L. Chen**, "A High-Efficiency 5-kW Soft-switched power conditioning system for low-voltage solid oxide fuel cells", in *Proc. of IEEE PCC*, April 2007, pp. 463 - 470.

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