Electrical Characterization of Gallium Nitride Drift Layers and Schottky Diodes

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Abstract

Interest in wide bandgap semiconductors such as silicon carbide (SiC), gallium nitride (GaN), gallium oxide (Ga_2O_3) and diamond has increased due to their ability to deliver high power, high switching frequency and low loss electronic devices for power conversion applications. To meet these requirements, semiconductor material defects, introduced during growth and fabrication, must be minimized. Otherwise, theoretical limits of operation cannot be achieved. In this dissertation, the non-ideal current-voltage (IV) behavior of GaN-based Schottky diodes is discussed first. Here, a new model is developed to explain better the temperature dependent performance typically associated with a multi-Gaussian distribution of barrier heights at the metal-semiconductor interface [Section 3.1]. Application of this model gives researches a means of understanding not only the effective barrier distribution at the MS interface but also its voltage dependence. With this information, the consequence that material growth and device fabrication methods have on the electrical characteristics can be better understood. To show its applicability, the new model is applied to Ru/GaN Schottky diodes annealed at increasing temperature under normal laboratory air, revealing that the origin of excess reverse leakage current is attributed to the low-side inhomogeneous barrier distribution tail [Section 3.2]. Secondly, challenges encountered during MOCVD growth of low-doped GaN drift layers for high-voltage operation are discussed with focus given to ongoing research characterizing deep-level defect incorporation by deep level transient spectroscopy (DLTS) and deep level optical spectroscopy (DLOS) [Section 3.3 and 3.4]. It is shown that simply increasing TMGa so that high growth rates (>4 µm/hr) can be achieved will cause the free carrier concentration and the electron mobilities in grown drift layers to decrease. Upon examination of the deep-level defect concentrations, it is found that this is likely caused by an increase in 4 deep level defects states located at E_C - 2.30, 2.70, 2.90 and 3.20 eV. Finally, samples where the ammonia molar flow rate is increased while ensuring growth rate is kept at 2 µm/hr, the concentrations of the deep levels located at 0.62, 2.60, and 2.82 eV below the conduction band can be effectively lowered. This accomplishment marks an exciting new means by which the intrinsic impurity concentration in MOCVD-grown GaN films can be reduced so that >20 kV capable devices could be achieved.

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General Audience Abstract

We constantly rely on electronics to help assist us in our everyday lives. However, to ensure functionality we require that they minimize the amount of energy lost through heat during operation. One contribution to this inefficiency is incurred during electrical power conversion. Examples of power conversion include converting from the 120 V wall outlet to the 5 V charging voltage used by cellphones or converting the fluctuating voltage from a solar panel (due to varying sun exposure) to the 120 V AC power found in a typical household. Electrical circuits can be simply designed to accomplish these conversions; however, consideration to every component must be given to ensure high efficiency.

A popular example of an electrical power conversion circuit is one that switches the input voltage on and off at high rates and smooths the output with an inductor/capacitor network. A good analogy of this process is trying to create a small stream of water from a fire hydrant which can either be off or on at full power. Here we can use a small cup but turning the fire hydrant on and trying to fill the cup will destroy it. However, if the fire hydrant is pulsed on and off at very short intervals (1 µs), its possible to fill the cup without damaging it or having it overflow. Now, under ideal circumstances if a small hole is poked in the bottom of the cup and the interval of the fire hydrant is timed correctly, a small low power stream of water is created without overflowing the cup and wasting water. In this analogy, a devices capable of switching the stream of water on and off very fast would need to be implemented. In electrical power conversion circuits this device is typically a transistor and diode network created from a semiconducting material. Here, similar to the fire hydrant analogy, a switch would need to be capable of holding off the immense power when in the off position and not impeding the powerful flow when in the on position. The theoretical limit of these two characteristics is dependent on the material properties of the switch where typically used semiconductors include silicon (Si), silicon carbide (SiC), or gallium nitride (GaN).

Currently, GaN is considered to be a superior option over Si or SiC to make the power semiconductor switching device, however research is still required to remove non-ideal behavior that ultimately effects power conversion efficiency. In this work, we first examine the spurious behavior in GaN-based Schottky diodes and effectively create a new model to describe the observed behavior. Next, we fabricated Ru/GaN Schottky diodes annealed at different temperatures and applied the model to explain the room-temperature electrical characteristics. Finally, we grew GaN under different conditions (varying TMGa and ammonia) so that quantum characteristics, which have been shown to affect the overall ability of the device, could be measured.

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1 Introduction

The topic of power electronics covers the conversion of electrical energy through the control of switching electronic circuits. Its application plays a key role in almost every aspect of our lives such as consumer electronics, renewable energy, lighting systems, and in transportation systems such as electric vehicles. A primary component of any power conversion circuit is a semiconductor-implemented switching device, used to regulate the power flow from input to output. This component is expected to block all current when in the OFF position and drop no voltage when switched ON, all while being able to switch at high frequencies. However, due to the material limits of semiconductor switches, this is not possible thus research is required to increase the breakdown voltage (V_{BD}) and lower the on-resistance (R_{ON}) all while ensuring the switching frequency is not hindered.

Today, most semiconductor power devices are fabricated from silicon, however the material's critical electric field (E_C) and carrier mobility ($\mu_{n/p}$) make it a poor choice for future applications that require high-power energy conversion with minimal losses. Additionally, a push toward smaller power conversion modules has led interest in wide-bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) for the creation of high power semiconductor devices. Currently, GaN offers a more promising path toward high power, high frequency, and high efficiency semiconductor power electronic devices where lateral commercial devices capable of 650 V operation currently exist. However, the currently available commercial devices are far from reaching the material limits of gallium nitride and thus work is required to further improve the devices capability.

Two important areas of research designed to help bring more capable GaN-based devices to market include device reliability and the realization of vertical device topologies. Some of the current research in both areas are summarized below in Sections 2.1.2.1 and 2.1.2.2. One of the main takeaways is that the notion of creating design-limited power semiconductor devices is only possible if defects are not introduced during device fabrication or material growth. Therefore, the work presented in Section 3 aims to complement these efforts by presenting a method for understanding non-ideal electrical characteristics in Schottky diodes in addition to revealing reliability limiting deep level states in GaN films introduced during growth by MOCVD under different conditions. Figure 1 summarizes the portion of a Schottky device where work is presented. The structure shown was fabricated only for work in Section 3.4.

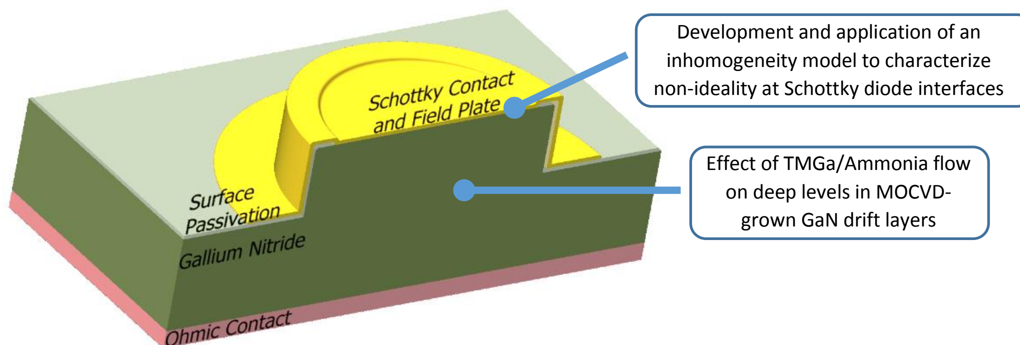

Figure 1. Schottky diode structure used in Section 3.4 with a research summary of work detailed in this dissertation and the portion of the device which is affected

2 Background and Literature Review

2.1 Power Electronic Devices

Power electronics, once referred to as industrial electronics, has come a long way since its original gas tube based power conversion techniques used mainly in industrial applications. It was the 1948 discovery of the transistor by Bardeen, Brittain and Schockley that began the transformation of the field into what we know today with silicon-based power electronics. It wasn't until 1958 when General Electric Company introduced a commercially available thyristor which began replacing mercury-arc, power magnetic amplifiers and the unreliable stacked copper-oxide and stacked selenium-based diodes [1]. Over the next 20 years semiconductor processing and fabrication efforts matured and the application of low power IC's brought the application of control theory to control power electronics [2].

Today, power electronic circuits are realized in almost every application with electric power requirements ranging from consumption of less than one watt in portable battery-operated equipment up to hundreds of megawatts for interfacial rectifiers and inverters in dc transmission lines to utility power systems [3]. The function of these circuits can include DC to AC (inverters), AC to DC (rectifiers), DC to DC (converters), and AC to AC (cycloconverters) power conversion [2]. Each conversion type can be accomplished with multiple circuit topologies depending on requirements such as power handling, phase integrity, output inversion and efficiency.

Modern power conversion is typically achieved by switching the incoming power through a capacitor and inductor network arranged to efficiently deliver required output power. At the heart of most of these converters lies a voltage controlled switch capable of holding off the incoming voltage when in the open circuit configuration and sinking large currents when in the short-circuit configuration. In addition to meeting these two requirements, the voltage-controlled switch is required to quickly switch from one state to another with very little delay and while in the short-circuit configuration, very little power loss due to internal series resistance is required. In the next few sections, these requirements for high-efficiency power conversion are discussed further.

2.1.1 Semiconductor-Realized Device Requirements

From the analysis in Appendix A.1 of an ideal and non-ideal boost converter, a few requirements of the semiconductor-realized switch could be gleaned. In this section, we will discuss the first-principle requirements of the semiconductor components so that a compact and high-efficiency converter can be obtained. These concepts will become the basis for research into developing materials and devices capable of performing a close as possible to the ideal switch shown in Figure 51 (Top).

2.1.1.1 Transistor and Diode Switching Frequency

The switching waveform through the transistor impacts both the efficiency and size of the circuit. First, an ideal switch can operate infinitely fast so that switching from Position 1 to Position 2 there is negligible delay; however, in a practical switch there is a switching delay when switching states. Below, in Figure 2, a practical switching waveform is shown for a non-ideal single pole single throw switch or a transistor.

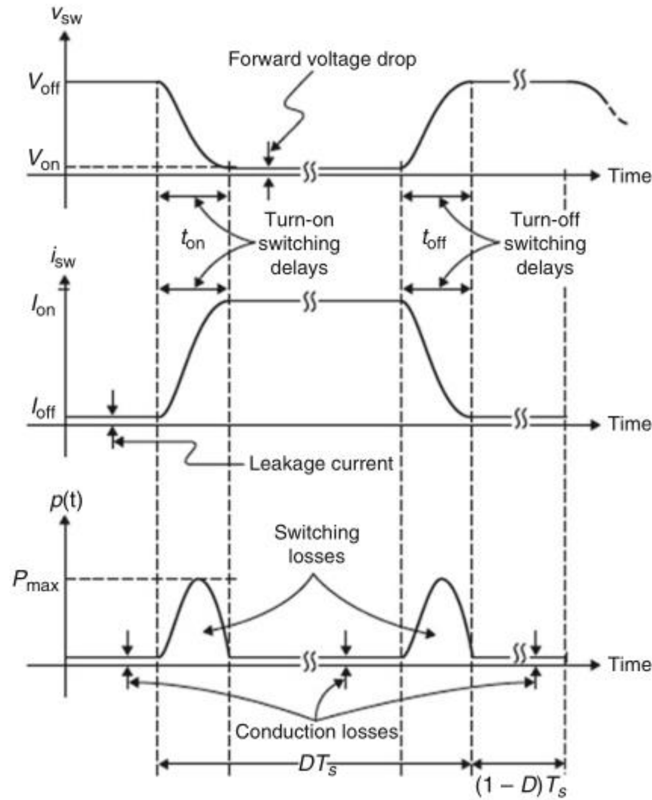

Figure 2. Switching waveform for a practical switch showing the switching losses and conduction losses [2]

In the switching waveform shown above the non-ideal switch suffers from a turn-on switching delay (t_{on}) and turn off switching delay (t_{off}). This delay causes a non-instantaneous change between V_{off} and V_{on} along with I_{on} and I_{off} causing a period of time where power is lost in the switch. This power loss is referred to as switching losses and will cause the efficiency of the circuit to drop when increasing the switching frequency. This is because the switching delays are constant with the components chosen to implement the switch while the time in which the circuit is functioning properly decreases as the frequency drops. This then causes the amount of power loss in each cycle to approach the amount of power delivered.

Although it may seem favorable to lower the switching frequency, thus easing the stringent requirements of low switching delays, an examination of Equations (96) and (99) offers a trade-off. From these equations, it can be seen that by increasing the frequency ($f_s = 1/T_s$) both the inductor ripple current and the capacitor ripple voltage decreases thereby producing a DC output with a smaller AC component. Additionally, if the required output ripple voltage has been set, increasing the switching frequency lowers both the required capacitance and inductance requirements. This can have a significant effect on the physical size of the circuit because these two components tend to be the largest.

2.1.1.2 Material and Structure Requirements for Low Loss and High Breakdown Devices

Focusing on the diode in Figure 53, while the circuit is in Position 1, the diode is approximated with an open circuit. Through KVL, assuming the on-resistance of the MOSFET is very low ($R_{on} \approx 0\Omega$), it can be seen that the voltage across the diode is approximately equal to v_{out}. In this configuration, the diode is expected to hold off the entirety of the output voltage and depending on the output requirements, it could be large. In reality, it is nearly impossible to achieve zero conduction when operated in the off-

mode. So in order for the converter to be viable in situations where overvoltage spikes and long term reliability are required, the power device isn't operated up to its breakdown voltage. Conversely, in Position 2, when the switch is in the non-conduction mode, the diode is approximated with a voltage drop and a series resistance. It was previously shown in Figure 54 (Middle) and (Left) what the forward on-voltage drop and series resistance has a large effect on the efficiency of an ideal boost converter. Additionally, for devices with large conduction losses, the removal of excess generated heat becomes a problem and consideration needs to be given to heatsink size and complexity. To minimize this conduction loss, both voltage drop and series resistance during operation needs to be minimized. Finally, it was shown in the previous section that diode and switches capable of higher frequency operation would reduce the power loss during switch transition in addition to reducing the converter volume since smaller magnitude passive components would be required. By tailoring the structure of a semiconductor switch or diode, improvements could be made on the basis of breakdown capability, conduction loss or switching loss but achieving all is ultimately limited by the material properties of the semiconductor. The radar plot in Figure 3 presents the material characteristics of the most widely implemented semiconductors for power electronic device applications.

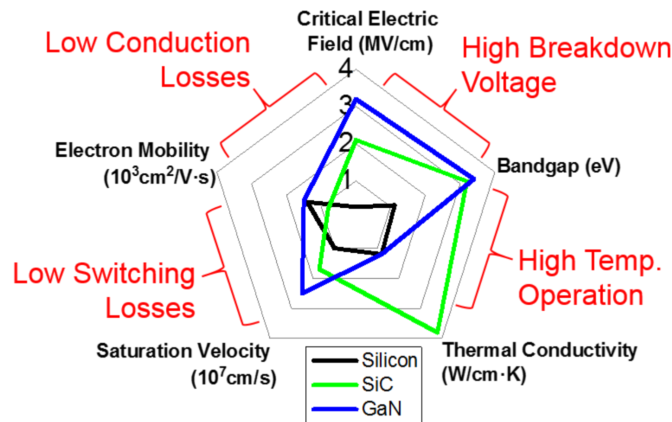

Figure 3. Radar plot comparing Si, SiC and GaN material properties on the basis of thier suitability for switching power converstion. [Adapted from: [4]]

From the plot, the material requirements to achieve specific power device characteristics are shown. The interest in gallium nitride is due largely to the ability to create drift layers capable of higher breakdown voltage and lower series resistance compared to the traditional silicon and silicon carbide based layers. Focusing on the requirements for higher breakdown voltage, a semiconductor with a large critical electric field and large bandgap is necessary. The critical electric field is a measurement of the theoretical point where conducting electrons in a material have enough energy to free bound electrons. In a semiconductor device this point is sometimes referred to as avalanche breakdown and is a set limit of the material. The 1-dimensional avalanche breakdown voltage for a drift layer can be expressed as:

$$V_{BD} = \frac{\varepsilon_S E_C^2}{2qN_D} \tag{1}$$

Here, the breakdown voltage, V_{BD}, is shown as a function of the critical electric field (E_C), the fully ionized doping concentration (N_D), and the dielectric permittivity of the material (ε_S). Accordingly, to ensure that the highest breakdown voltage is achieved for a specific material, doping concentration needs to be as low as possible and the length scale between the electrodes needs to be increased. However, an important trade-off exists with the conductivity of the layer. In the ON position, the resistance is limited by the amount of free carriers available for conduction and the distance in which conduction occurs over.

$$R_{SP,ON} \approx N_D q \mu_n \sqrt{\frac{2\varepsilon_s V_{BD}}{q N_D}} \quad (2)$$

where μ_n is the electron mobility, V_{BD} is the film breakdown voltage, and ε_s is the dielectric permittivity. Thus, to lower the on-resistance of a device, the free carrier concentration should be increased while the conduction length should be lowered, a trend which is counter to the requirements for a high breakdown layer. This innate trade-off is summarized in Figure 4 below.

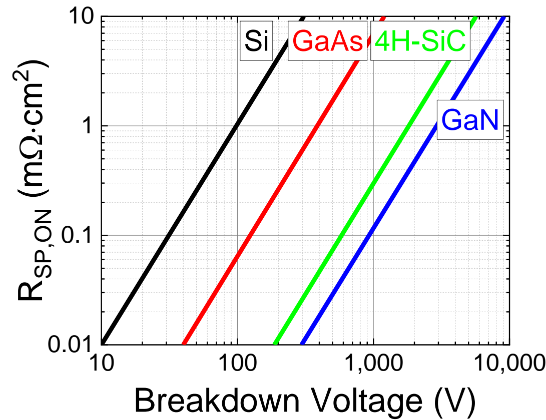

Figure 4. 1-Dimensional calculation of the drift layer on-resistance as a function of breakdown voltage for Si, GaAs, 4H-SiC and GaN.

Considering only GaN, it can be seen that in order to form a drift layer which is capable of higher breakdown voltage, the theoretically lowest achievable on-resistance will increase. Now, considering differences between each of the materials, the benefits of fabricating a drift layer from GaN over other widely used materials can be observed. In the instance where a breakdown voltage of 300 V is required, from the plot, GaN is theoretically capable of achieving a 2x lower specific on-resistance compared to 4H-SiC and a 1000x improvement compared to Si. In the instance where the on-resistance of SiC is good enough, GaN is capable of achieving the same breakdown voltage but in half of the required die area, thereby improving production efficiency and lowering the module size.

Up until now, it is assumed that breakdown is limited only by the critical electric field; however consideration needs to be given to the structure. In the case where the material dimensions allow the reverse bias depletion width to span the anode to cathode width, the maximum electric field is enhanced and breakdown occurs at lower voltages. This phenomenon is known as punch-through. The breakdown voltage equation needs to be altered to consider not only the material properties of the semiconductor but also the structure. For drift layer thicknesses smaller than this limit, the breakdown voltage becomes,

$$V_{BD} = \begin{cases} E_C W - \dfrac{q N_D W^2}{2\varepsilon_s} & W < W_{PT} \\ \dfrac{E_C W_{PT}}{2} & W \geq W_{PT} \end{cases} \quad (3)$$

where W represents the drift layer width and W_{PT} is limit where punch-through is active. Breakdown voltage versus drift layer width is calculated for different values of doping concentration according to Equation (3) and plotted in Figure 5. When considering the requirements to achieve high breakdown voltage capable devices, this plot highlights some important points. Each of the curves shown saturate at

some width, dependent on the total doping concentration. This saturation of breakdown voltage with increasing drift layer thickness is set by the limit of avalanche breakdown. As the drift layer thickness is lowered, the breakdown voltage begins to decrease due to the onset of tunneling and only worsens as the thickness is lowered further. The grey dashed line represents the point at which each of the trends saturates and thus the point where increasing thickness no longer effects the breakdown voltage.

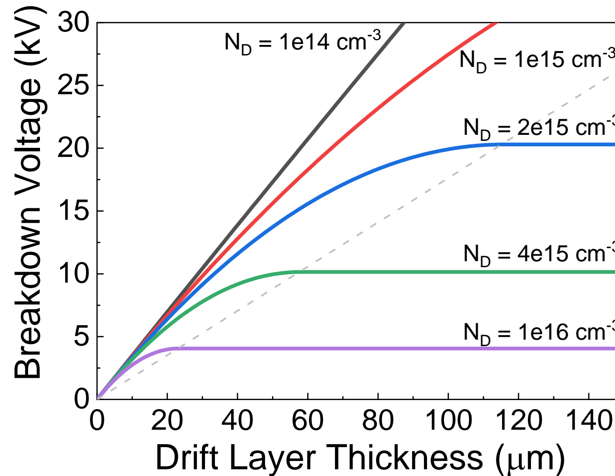

Figure 5. Theoretical calculation according to Equation (3) of breakdown voltage as a function of drift layer thickness for an abrupt one-sided junction fabricated on GaN. The light grey dashed line is the point of saturation calculated at each doping concentration.

Because drift layers take time and therefore resources to produce thicker layers, it is beneficial to know at what point extending growth time will have no effect on the breakdown voltage of a drift layer. Additionally, achieving uniformly low-doped drift layers is not always trivial. Thus, for a material grower, this plot is critical in determining the required drift layer thickness and/or carrier concentration needed to achieve a specific breakdown voltage with the least amount of time and effort.

2.1.2 Current Research

Gallium nitride is heavily researched for its use as a power electronic device. In this section, two research thrusts will be summarized, including work on vertical power devices and work improving device reliability. These two topics were selected due to their direct connection to the work presented in Section 3.

2.1.2.1 Recent Work on Vertical Gallium Nitride Devices

Vertical power devices are favorable over lateral devices for many reasons. First, in a lateral device, if a larger breakdown voltage is required the structure must be altered to increase the distance between the anode and cathode (source and drain in a transistor) so that higher breakdown devices require a larger chip area. In a vertical device, the drift layer can simply be made thicker thereby reducing the amount of area needed for an equivalent breakdown and voltage device. For a three-terminal device, this has a secondary effect in that the gate capacitance is reduced. Reducing the gate capacitance reduces the amount of charge needed to turn the channel ON and OFF thereby increasing the switching speed of a device. Secondly, lateral devices suffer from a variation of the electric field at the surface which can cause well-known side effects such as RF output power degradation, drain-lag, current collapse, increased

leakage current, and premature breakdown. By burying the channel within the bulk of the semiconductor, these non-idealities can be minimized.

Although the choice to implement a device in the vertical structure seems ideal, it has only recently become possible to accomplish with GaN. Fabricating vertical GaN devices requires access to low defect GaN substrates on which additional active layers can be grown. Traditionally, layers are grown on foreign substrates such as Sapphire, Silicon, or SiC, resulting in active layers with high dislocation densities on an insulating substrate [5]. If ohmic contact to the backside of the substrate isn't possible, a truly vertical device cannot be fabricated unless the film is lifted off. Through the development of growth techniques such as hydride vapor phase epitaxy (HVPE) and ammonothermal along with processing techniques such as void assisted separation (VAS), low dislocation free-standing GaN substrates have become feasible [5]. Currently, companies such as SCIOCS, Mitsubishi Chemical, and Six Point Materials offer commercially available GaN wafers for LED and power electronic device fabrication.

From access to these substrates, exciting capability advancements in vertical Schottky diodes, P-N diodes, and transistors fabricated from GaN drift layers have been achieved. The first P-N diode capable of blocking >1 kV was established by Nomoto et al. [6]. Here they showed that the breakdown voltage could be increased from 0.4 to >1 kV by utilizing a spin-on-glass surface passivation and field-plating technique. Improvements in breakdown voltage and specific-on resistance have been reported in years since [7-11] with the recently reported work by Ohta et al. [12] demonstrating the addition of polyimide resistive element in a guard ring to improve the breakdown from 4.7 to 5 kV.

Next, GaN-based vertical Schottky diode research has been enhanced through the possibility of vertical implementation. Similar to the P-N diode, the first report of a >1 kV operation occurred in 2010 by Saitoh et al. and they showed the effect of input V/III ratio on the YL peak and reverse leakage current [13]. Since, however, only minor improvements to breakdown voltage have been reported [14, 15] with the current maximum at 1600 V [15]. However, exciting reports of advanced junction termination techniques have been released. The focus lies on implementing junction barrier Schottky (JBS) diodes and trench MIS barrier Schottky (TMBS) diode structures so that the breakdown voltage can be improved without suffering from the higher turn-on voltage as seen in P-N diodes. JBS diodes have been implemented using ion implantation [16, 17] or utilizing a p-layer growth and etch trench-style diode [18, 19] with a maximum breakdown of 1.6 kV [19] achieved. TMBS diodes which rely on the MIS junction to pinch the diode 'channel' are easier to fabricate due to their lack of a p-GaN layer or need to tightly control etching and implantation depths. Thus far two reports show promising results for GaN TMBS structures [20, 21] on GaN substrates.

2.1.2.2 Trap-Caused Reliability Issues in GaN HEMTs

In addition to the capabilities of a power electronic device such as breakdown voltage and low conduction loss, a semiconductor device must have high reliability. Currently, GaN power electronic devices can be plagued with trapped charge or fabrication induced failure mechanisms if operated at high voltage or temperatures. In Figure 6, a schematic of a traditional AlGaN/GaN HEMT is shown along with the understood locations of deep levels or trapped charge groups that cause the degradation in the electrical behavior or these devices. First, in a typical AlGaN/GaN HEMT the channel is formed by the piezoelectric and spontaneous polarization at the heterojunction interface which causes the fermi-level to rise above the GaN conduction band and induce a 2D electron gas. Because the channel is formed without needing dopant sources, the mobility is unaffected by ionized impurities. The channel concentration is modulated

with a Schottky gate structure, whereby applying a negative voltage to the gate w.r.t. the source contact will deplete the channel. A majority of the non-ideal behavior reported on this devices such as current collapse, RF degradation [22, 23] and premature breakdown [24, 25], has recently been found to be caused by the depletion of the channel by unintentionally trapped charges in key locations. In this section, the causes and effects of trapped charge near the gate and in the bulk are reviewed.

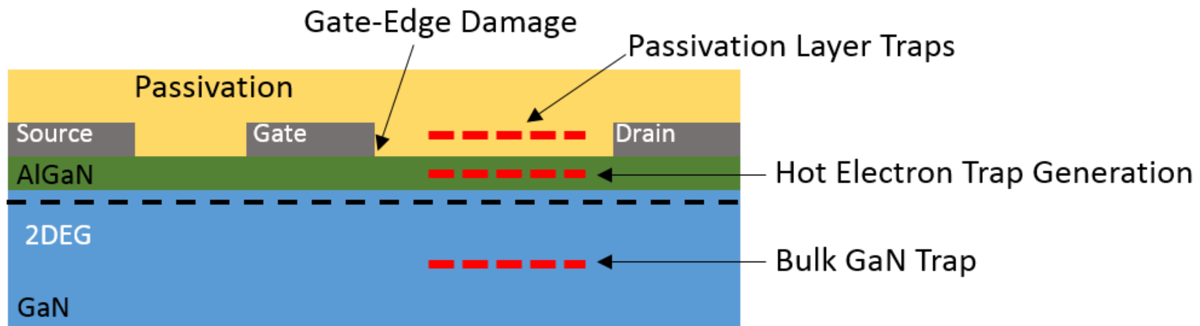

Figure 6. Schematic of a traditional AlGaN/GaN high electron mobility transistor (HEMT). The location of commonly observed trapped charge groups are indicated with an arrow.

As mentioned previously, the gate stack in a traditional AlGaN/GaN HEMT is a Schottky diode and thus prone to higher leakage current than a MOS or PN diode structure. It has been found that reverse biasing the gate terminal past a 'critical level' will create deep level defect states within the AlGaN layer [26-28]. It is hypothesized that the high electric field in this region causes strain in the AlGaN layer, and once a critical strain is reached, the material is altered and trap states will be created. These states assist current conduction from the gate into the channel in addition to creating a location for charges to be trapped [29]. The gate leakage current becomes time-dependent and noisy 'hops' in the magnitude can be observed [30], but longer stressing times will induce irreversible breakdown. Even with the addition of a p-GaN layer between the gate metal and AlGaN layer to create a normally-off device, gate degradation continues to be a problem [31, 32]. The charge trapped in these generated states as a result of stressing has widely been considered the cause of the infamous 'current collapse' problem in AlGaN/GaN HEMTs. Here, the negative charge buildup of trapped electrons near the gate causes partial depletion of the channel for a given gate voltage. In measured devices, this presents itself as dynamic behavior of the channel on-resistance and can be further exacerbated by increases to drain voltage so that electrons can hop along traps toward the drain [33-36]. In an attempt to reduce virtual gating by trapped charges at the surface of as-grown AlGaN layers, different surface passivation chemistries such as SiO2, SiN_x, AlN Al_2O_3, and others have been reported. The best results have been shown for SiN_x-based passivation layers, which are assumed to create a low interface-state density with AlGaN [37-39].

A second theory for the cause of 'current collapse' in AlGaN/GaN HEMTs relies on the idea trapped charge located in the GaN bulk layer can effectively lower the channel conductivity [40, 41]. It was noticed that after electrical stressing, certain trap signatures would become stronger, a clear indication that they could be the primary cause. However, their locations could not be accurately determined, leading some to speculate that presence in the drain access region was to blame [23]. Improvements to trap detection methods were developed where HEMTs could be biased in the saturation and triode region to reveal effects from deep level traps under the gate and in the drain-access region respectively [22, 42]. Through these measurements, it was revealed that not only trapping centers located within the GaN bulk near the heterointerface are likely causing depletion of the channel but also the signature was consistent with the

omnipresent GaN E2 trap [43]. Even more sophisticated methods of spatial deep level trap detection have been developed [44], and reports have identified impurity incorporation along pure edge dislocations as the prime suspect [45]. As a workaround to understanding methods for minimizing this defect, reports have shown that by injecting holes during operation, trapped charges can be removed through impact ionization effectively minimizing the spurious effects [46].

From studying these two sources of dispersion, it can be seen that in order for a power electronic device to operate theoretically care must be taken to ensure trapped charges are not introduced. As was discussed, trapped charges both within the interface of the HEMT and in the bulk can cause a reduction in the channel conductivity under certain circumstances; however, trapped charge states can affect behavior in other types of GaN-based devices such as FinFETs [25], Schottky diodes [47, 48], and PN diodes [49, 50]. Thus, efforts to minimize or reduce these states either through considerate fabrication techniques or improved growth methods should be pursued.

2.2 MOCVD Growth of GaN Introduction

Metal-organic chemical vapor deposition (MOCVD), also known as organometallic vapor phase epitaxy (OMVPE), is the most commonly used method for growing gallium-V layers for electrical device applications. First reported as a method capable of GaAs, GaP, GaAsP, and GaAsSb epitaxial growth on GaAs substrates by Manasevit and Simpson [51], the MOCVD-grown layers have been more popular than those grown by hydride vapor phase epitaxy (HVPE) because of early reports showing high purity GaAs films capable of minority carrier devices such as LEDs [52], photovoltaic cells [53], photocathodes [54] and lasers [55]. More recently, MOCVD has been used as the dominant method for producing gallium nitride (GaN) films for optoelectronic and power electronic applications. In this section, the basics of GaN growth by MOCVD is reviewed, and the possible sources of contamination in the Guido Group horizontal reactor are summarized.

2.2.1 MOCVD Growth of GaN Basics

As the name suggests, MOCVD is the process of using a metalorganic-containing chemical vapor to grow or deposit a solid on a substrate, whereas HVPE which uses the same process, implies that this growth is epitaxial. The growth of gallium nitride at Virginia Tech is accomplished by using a pure hydrogen carrier gas bubbled through a liquid trimethylgallium (TMGa: $Ga(CH_3)_3$) source to transport vapor which acts as the metal-organic source ($25 - 500$ µmol/min). On the hydride side, ammonia (NH_3) is used as the column V source (1300 – 10000 sccm), and is also buffered with a pure hydrogen supply (1100 – 2600 sccm) and together make the hydride source. As shown below in Figure 7, the two sources are kept separate until they reach in the quartz reaction chamber due to the possible formation of adducts such as TMGa:NH_3 or H_3N:TMGa:NH_3 which then polymerize [56]. The gas mixes in the reaction chamber and upon reaching the heated sapphire (Al_2O_3) or bulk-GaN substrate, will break down allowing elemental gallium and nitrogen to react on the surface of the substrate. Ideally, the methyl groups previously part of the TMGa molecule will pyrolize and leave elemental gallium at the surface of the substrate while the ammonia molecule decomposes leaving nitrogen. The byproducts of this reaction would then be CH_3 and H_2. It should be noted that this is a simplistic view of GaN growth and models have been developed to explain growth by adduct formation [56] or to understand impurity incorporation [57].

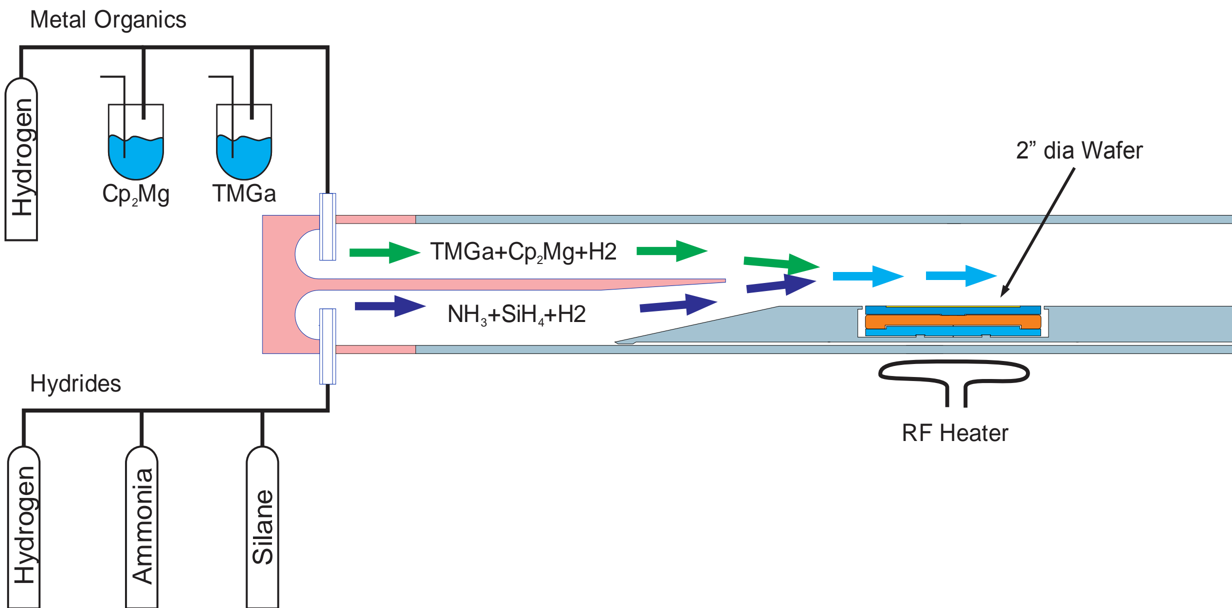

Figure 7. Schematic of the Guido Group horizontal MOCVD reactor used to grow GaN. The metalorganic and hydride sources gases are separated by a quartz plate after which they combine and transfer to the RF heated susceptor where the substrate is located.

To intentionally grow layers with a net free electron concentration, silane vapor ($10^{-11} - 10^{-8}$ µmol/min) can be added to the mixture, thereby causing silicon to incorporate. Silicon in GaN is considered to act as a shallow donor. Films with a net hole concentration are typically doped with Mg by adding bis(cyclopentadienyl)magnesium (Cp_2Mg) gas; however, due to unintentional Mg-H complex formation, as-grown layers are fully compensated. Once annealed at high temperatures within a non-hydrogen containing ambient, hydrogen will diffuse out of the film resulting in p-type GaN films [58].

2.3 Schottky Diode Characterization

2.3.1 Room Temperature IV Characterization

The current-voltage characteristics of a Schottky device are arguably the most important means of analyzing the feasibility of a device to perform in a power conversion circuit. Although simple, it has proven difficult to fabricate Schottky diodes capable of theoretical operation resulting in devices with high leakage currents, non-ideal barrier heights, or parallel current paths. This section will review some of the techniques for measuring and analyzing the IV characteristics of Schottky diodes.

2.3.1.1 Schottky Diode Characteristics

The equilibrium process of the surface band diagram for a metal-semiconductor (M-S) is visualized in Figure 8. In Figure 8(a) the surface of a metal with a work function (ϕ_m) larger than the semiconductor electron affinity (χ) far enough away from the surface of an n-type semiconductor to be considered non-interacting. As the surfaces are brought closer together the carrier wave functions are considered to interact and, because electrons in the semiconductor conduction band have a larger thermal energy than those in the metal (evident by fermi level in the semiconductor being higher than that in the metal), electrons at the surface of the semiconductor begin to migrate across the gap (δ) and into the metal. This process causes doping atoms at the surface of the semiconductor to become ionized and thus induce an electric field causing the valence and conduction bands to bend. Once the M-S junction has come into intimate contact, the process can reach full equilibrium in regards to electron migration and the balancing ionized impurity induced electric field resulting in a barrier for free charges to move from both the metal

to semiconductor (ϕ_B) and semiconductor to metal (V_{bi}). An M-S interface at equilibrium is shown in Figure 8(d).

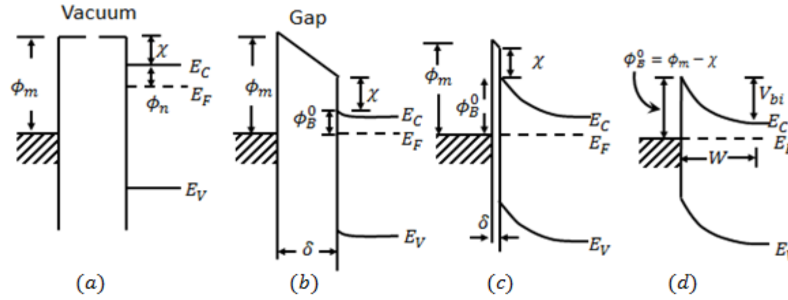

Figure 8. Energy band diagram of a metal and semiconductor surface from (a) non-interacting to (d) equilibrium [59].

The final state of the system, and thus the current-voltage dependence, is a function of two parameters including the work function of the metal, and work function of the semiconductor ($\phi_s = \phi_n + \chi$). First, a Schottky contact is formed if the metal work function falls within the forbidden gap of the semiconductor, otherwise an ohmic contact is created. For an n-type semiconductor, the ideal barrier height is considered to be the difference between the metal work function and the electron affinity in the semiconductor according to Equation (4). Thus, for a set semiconductor the barrier height should vary linearly with the metal work function as shown in Equation (5). Secondly, without considering the variation in the intrinsic material properties of the semiconductor, the equilibrium picture of the M-S interface varies with the density of dopants at the surface. As the magnitude of the dopant density increases, the depth of depletion (W) will decrease and the severity of the band bending will increase. The semiconductor in the figure is considered to be n-type doped but this model holds for p-type material except that the band bending is opposite of which is shown (the semiconductor side is inverted around the fermi level dashed line) [59].

$$\phi_B = \phi_m - \chi_S \quad (4)$$

$$S \equiv \frac{\partial \phi_B}{\partial \phi_m} = 1 \quad (5)$$

As mentioned previously, ideally the barrier height is determined only by the magnitude of the metal work function and follows the Schottky-Mott limit in Equation (5). However, experimentally this is rarely the case where I-V results follow a non-ideal work function dependence of $S < 1$. The cause of this phenomenon has been explained with various models including metal-induced gap states (MIGS) [60], defect-induced gap states (DIGS) [61], unified defect model (UDM) [62], and bond polarization models [63].

In addition to Schottky diodes not following the Schottky-Mott limit, it is common for values of the barrier height extracted from various methods (IV, CV, and Optical) to not match the theoretical values calculated from the difference of the metal work function and semiconductor electron affinity. It can be partially explained when considering the effects of image-force barrier lowering, depicted below in Figure 8. The cause of this perturbation can be understood by examining the effect of an electron approaching the surface of a metal in vacuum. The electric field of the charge causes the rearrangement of the free electrons in the metal and can be modeled as a positive charge equidistant from the surface but within the metal. As the electron continues it's approach so does the 'positive' charge and thus an increase in

electric field magnitude at the interface. According to Poissons equation, the electric field along this 1-D path can be integrated to find the induced potential energy. Modifying the initially sharp peak of the barrier height with this potential energy line results in a rounded peak whose magnitude depends on the externally applied voltage.

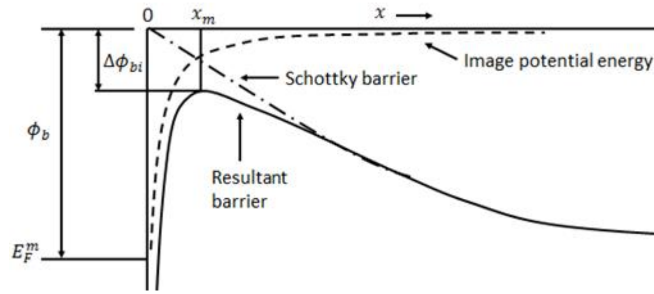

Figure 9. The diagram shows the ideal Schottky barrier profile (dash-dot), image potential (dash) and the resulting barrier profile (line) when the effects of image force lowering are considered [59].

2.3.1.2 Ideal IV Characteristics

First correctly proposed by Bethe, the rectifying behavior of a MS junction is ideally limited by the thermionic emission over a barrier that varies with voltage for carrier moving from the semiconductor to metal but is constant for carriers traveling from the metal to semiconductor. The quantitative expression of current density is shown below in Equation (6).

$$I(V_d) = AA^*T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV_d}{\eta k_B T}\right) - 1\right] \quad (6)$$

Where,

$$A^* = \frac{4\pi m^* q k^2}{h^3} \quad (7)$$

The parameter A^* is known as the Richardson constant and depends on the effect mass of carriers in the semiconductor, A is the area, T is the temperature of the device, ϕ_b is the barrier height, η is the ideality factor, and V_d is the voltage applied to the Schottky diode. From this equation, for positively applied voltages (also referred to as forward bias) the current density is expected to increase and for voltages much larger than a few k_bT, the current density is expected to increase with an exponential dependence. When negative bias is applied to the device (also known as reverse bias), the sign of the current density magnitude becomes negative and for applied bias values larger than a few k_bT the current density will remain constant. As stated previously, for a given semiconductor, metals with work functions can be selected to either create a Schottky or ohmic contact. If a Schottky contact is selected, it can be seen from Equation (6) that larger induced barrier heights will exponentially decrease current at a given voltage. Larger barrier heights are ideal for applications where low reverse bias leakage current is required. Finally, Equation (6) can be expanded to describe Schottky diodes with non-zero series resistances by defining the diode voltage as a function of the applied voltage and series resistance, $V_d = V_A - I \cdot R_s$.

2.3.1.3 Plotting Methods for Schottky IV Parameter Extraction

Because complex computer-based mathematical fitting routines were not widely available earlier, parameter extraction methods relied heavily on linearizing the exponentially dependent current data. The simplest method, used by Missous [64], relies first linearizing the I-V plot by logarithmically scaling the y-axis and then removing the low-current regime by dividing out the term responsible for it $(1 - e^{-qV/k_BT})$. This process helps linearize the data across a larger range of voltage, which can be especially helpful in

samples with higher series resistance. Next, parameter extraction is accomplished by taking the natural log of the data and fitting the linear portion of the data to extract the slope and y-axis intercept. Equations (8) and (9) can be evaluated to find the ideality factor and barrier height respectively.

$$\frac{d\left(\ln\left[\frac{I}{1-e^{\frac{-qV}{k_bT}}}\right]\right)}{d(V)}=\frac{q}{nk_bT} \tag{8}$$

$$\ln\left[\frac{I(0)}{1-e^{\frac{-qV_0}{k_bT}}}\right]=\ln[AA^*T^2]-\frac{q\phi_b}{kT} \tag{9}$$

Although simple, linearizing the low current regime requires first knowing the ideality factor or it will overestimate the transformation, leading to an upturn at low currents as shown in curve 'E' of FIG. 1 in [64]. Additionally, this method is incapable of removing or extracting the series resistance which can lead to inaccuracies in fitting if the resistance dominated region is used.

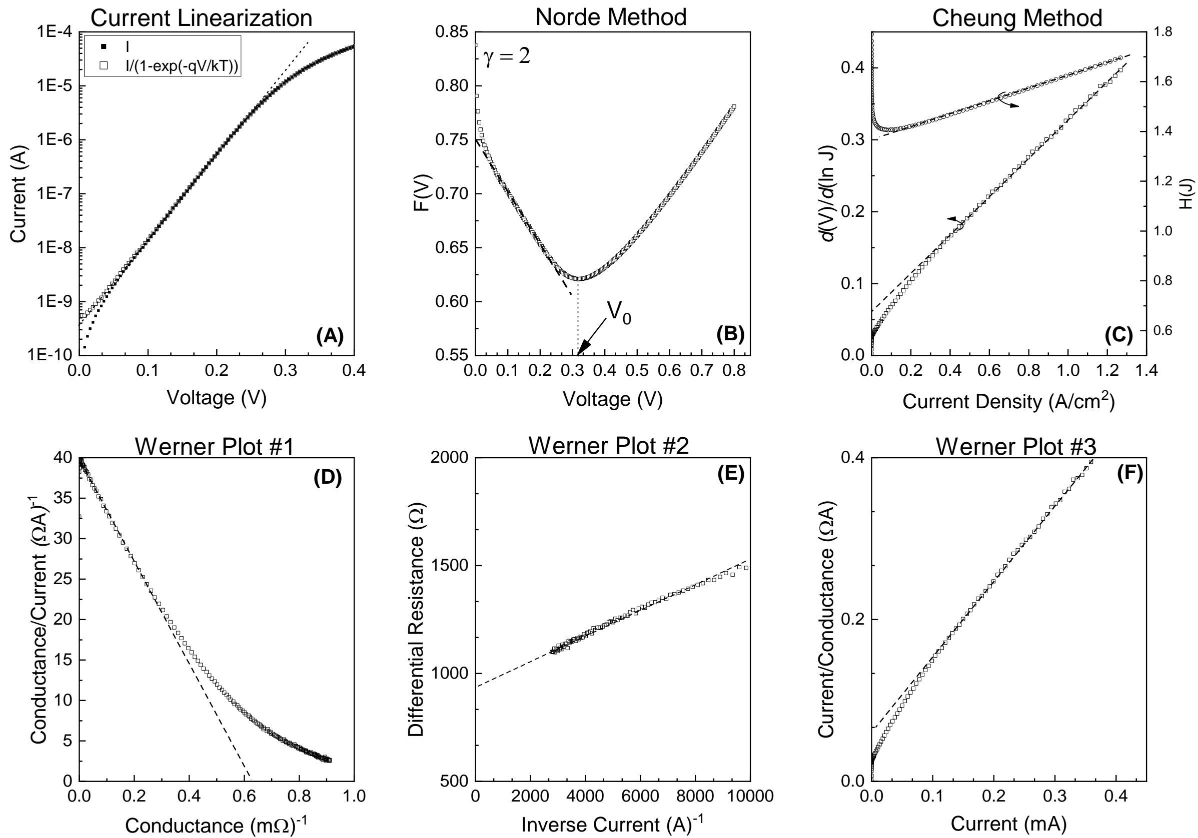

Figure 10. Examples of plotting methods to simplify the extraction of ideality factor, barrier height, and series resistance from experimental IV data.

Norde's extraction plot, shown in Figure 10(B), relies on the differential resistance along the curve to extract barrier height and series resistance parameters; however, the original method [65] did not address ideality factor extraction. This was later expanded by Bohlin [66] to describe Schottky diodes with non-unity ideality factors. The extraction process first transforms the experimental data with Equation (10),

identifying the voltage at which the minima occurs and finding the slope and y-intercept of the linear region at lower voltages.

$$F(V) = \frac{V}{\gamma} - \frac{k_b T}{q} ln\left[\frac{I}{AA^* T^2}\right] \quad (10)$$

$$R = \frac{k_b T}{q I_0} \quad (11)$$

$$\phi_b = F(V_0) + \frac{V_0}{\gamma} - \frac{k_b T}{q} \quad (12)$$

where γ is a constant larger than the ideality factor and I_0 is the current at the voltage which produces the minimum (V_0) on the $F(V)$ graph. Extraction of the ideality factor requires setting a system of equations by setting different values for γ larger than the ideality factor, extracting values of R and I_0, and finally extracting the vales of η [66]. As it has been pointed out [67], this procedure suffers from the identification of the minimum of $F(V)$ since the I-V data is quantized and only a few data points exists around the minima whereas the rest remain unused except for extracting the ideality factor.

Next, Cheung's extraction plot [68] which is show in Figure 10(C), utilizes a linearization method but first relies on extraction through the examination of the current density slope on a semi-logarithmic axis according to Equation (13). From this first graph, the series resistance and ideality factor can be gleaned from the slope and y-intercept respectively. Secondly, with these extracted values, a new graph can be plotted according to Equation (14) where the ideality factor is determined by the y-intercept.

$$\frac{d(V)}{d(ln J)} = R_s A J + \frac{k_b T \eta}{q} \quad (13)$$

$$H(V) \equiv V - \frac{k_b T \eta}{q} ln\left(\frac{J}{A^* T^2}\right) = R_s A J + \eta \phi_B \quad (14)$$

In comparison to parameter extraction from Norde plots, the Cheung method uses a large subset of the data to fit a characteristic line related to the extracted parameters. However, this method assumes that the linear region of an I-V plotted on a semi-log plot is linear along the full range of voltage. If not, error can arise from the method with which the derivative is made especially if noise in the data can be considered a problem.

The fourth method, shown in Figure 10(D-F), again relies on various slopes extracted from the original I-V data. Werner showed that even with the addition of large external resistances, the series resistance, ideality factor and barrier height could be extracted with minimal error [67]. The method required generating the small-signal conductance (dI_d/dV) from the I-V data and then using it to re-plot the linearized data and extract out the parameters. The equations that govern the three plots are:

$$\frac{G}{I_d} = \frac{k_b T}{q\eta}(1 - GR_s) \tag{15}$$

$$G^{-1} = \frac{k_b T\eta}{q}\frac{1}{I_d} + R_s \tag{16}$$

$$\frac{I_d}{G} = R_s I_d + \frac{k_b T\eta}{q} \tag{17}$$

Where $G = dI_d/dV$. Thus plotting $\frac{G}{I_d}$ $vs.G$, $\frac{1}{G}$ $vs.\frac{1}{I_d}$, and $\frac{I_d}{G}$ $vs.I_d$ will yield linear plots which, similar to the previous methods, require a fitting line to extract the ideality factor and series resistance. With these extracted vales of series resistance, the original I-V data can be corrected for the higher-current rollover so that a longer region of linearity can be formed. The three values of series resistance will yield three corrected plots and the 'current linearization' method can be implemented, resulting in three values for the barrier height. Again, this method suffers from the requirement to perform a derivative on quantized data resulting in deviation from derivative methods and signal noise.

Although all four plotting methods produce a simple way of extracting values from exponential I-V data, it does so while introducing some error or relying on the assumption that the data is only perturbed by non-unity ideality functions and series resistances. Additional sources of non-ideality include parallel resistance, noise floors and a non-homogenous M-S barrier. After evaluating each method detailed above, it was concluded that to minimize errors, a generalized model which could be used to iteratively fit the data would need to be created.

2.3.1.4 Schottky Parameter Extraction Through L-M Fitting

As mentioned in the previous section, to accurately and non-prejudicially fit experimental data, a generalized model and iterative fitting algorithm could be used. With this, the entirety of the original dataset could be utilized so that variations from fitting a subset or transforming the data are not included. Additionally, the model can be expanded to include other features of real data such as parallel resistance conduction, noise floors and multi-barrier current perturbations. The model used to fit experimental data is derived from the following equivalent circuit.

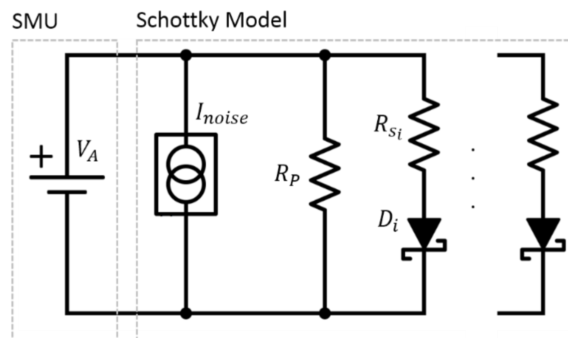

Figure 11. Circuit model used to deconvolve the individual effects of noise, parallel resistance, and parallel Schottky/resistor on the observed electrical characteristics.

Here, the voltage is applied and the resulting current is measured by the source-measurement unit (SMU) on the left. The voltage dependence of the 'Schottky Model' is determined by the behavior of each branch

in the circuit. First, the noise is modeled as a voltage-independent current source (I_{noise}) and can be a function of the SMU resolution in addition to testing apparatus leakage current. Next, the parallel resistance (R_P) is introduced in the case where conduction paths such as surface leakage or device shunting cannot be excluded. In the third branch, the M-S interface (D_i) and bulk/contact resistance (R_{s_i}) is modeled in series. Finally, the model can be extended to fit cases where overlapping diode characteristics exists by summing the current contributions of additional diode/resistor branches with varying parameters. The summation of current induced in each branch can be expressed with the following equation where I represents the current measured by the SMU:

$$I = I_{noise} + \frac{V_A}{R_p} + \sum_{i=1}^{n} I_{D_i} \quad (18)$$

$$I_{D_i} = AA^*T^2 e^{-\frac{q\phi_{b_i}}{k_bT}} \left(e^{\frac{qV_{D_i}}{\eta_i k_b T}} - 1 \right) \quad (19)$$

From here, the current through each of the diode/resistor branches needs to be determined but requires iteratively varying the voltage across the diode until the value settles. Applying the Kirchhoff's voltage law (KVL) to each of the branches yields the following equation whose root can be solved with the secant method:

$$0 = V_A - I_{D_i} R_{S_i} - V_{D_i} \quad (20)$$

Now that a method for determining the current in each branch is established, values for each diode, series resistor and parallel resistor can be plugged into Equation (18) and (19) to compare the resulting current variation with the gathered data. The Levenberg-Marquardt (L-M) procedure is a method for solving nonlinear least squares problems like this one and behaves like the gradient descent method when the parameters are far from optimized and like the Gauss-Newton method when they are close. For the Schottky diode I-V fitting done in this work, values for the saturation current, series resistance and ideality factor were used as input parameters to a LabVIEW implemented L-M fitting computer program. The values for current noise and parallel resistance remained constant for each set of measurements.

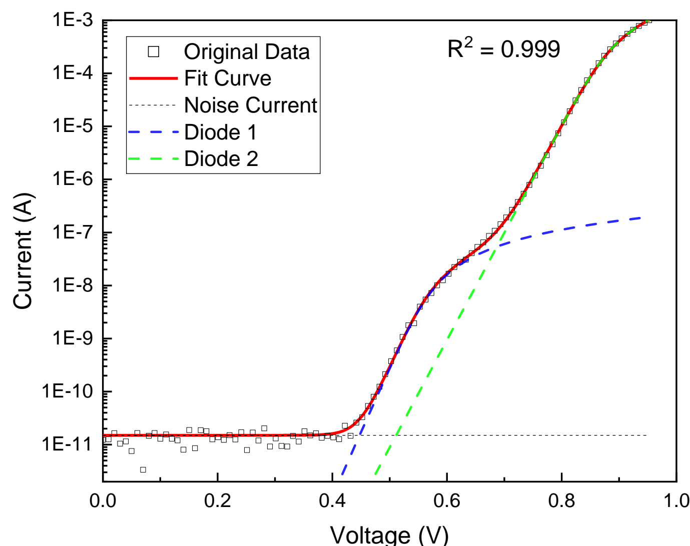

Figure 12. Example of experimental Schottky I-V data fit with two resistor/diode branches, each with different values of series resistance, barrier height, and ideality factor. A constant diode current was required to fit the data between 0 and 0.4 V while parallel resistance was found to be inconsequential

Above in Figure 12 is example data taken on a RuOx/GaN Schottky cooled to 82 K with fitting curves showing the behavior of each branch in the Schottky model. The original data is represented with a scatter plot of square points while the red line shows the final fitting curve. At low voltages the fitting curve can be seen to follow the constant noise current and then begins to quickly rise after 0.4 V to follow the trend of 'Diode 1'. Due to the higher series resistance associated with this diode, the current rolls over and exposes a new trend described by the parameters determined for 'Diode 2'. The coefficient of determination was evaluated by first taking the logarithm to base 10 of both the original and fit curves so that all errors could be properly weighted. Both, from this value and the observation of overlap, it is determined that the parameters used to model this Schottky device result in an excellent fit.

2.3.2 Barrier Inhomogeneity

Extraction of M-S interface properties from experimentally observed I-V data typically yields values considered non-ideal including lower than theoretically barrier heights and non-unity ideality factors. When comparing values of barrier height extracted by other means, such as C-V or through optical stimulation, results from I-V measurements tend to be lower and do not follow the trend predicted by Schottky in Equation (5). Secondly, review of the literature suggests that achieving near-unity ideality factors is almost impossible. Finally, when probing Schottky diodes at various temperatures, it is likely that both the extracted ideality factor and barrier height will have a temperature dependence. To explain these problems, models based on thin interface layers, tunneling current, image force lowering and G-R current have been examined but the barrier inhomogeneity model proposed by Werner and Guttler can explain experimental results by simply invoking a non-homogeneous barrier height [69].

2.3.2.1 Werner-Güttler Gaussian Barrier Distribution Model

Werner-Güttler review previous attempts at explaining the reason for η>1 but find that they all rely on the assumption that the interface is not varying and thus is atomically perfect. Instead, they assume that a continuous distribution of barriers exists at the interface and will likely be Gaussian in nature following Equation (21). The distribution is defined by a mean barrier height, $\bar{\phi}_b$, and a standard deviation, σ_s.

$$P(\phi_b) = \frac{1}{\sigma_s\sqrt{2\pi}} e^{-\frac{(\bar{\phi}_b - \phi_b)^2}{2\sigma_s^2}} \tag{21}$$

Because current will flow preferentially through the portions of the barrier which are lower, it explains why it is unlikely to create a Schottky diode whose barrier is solely dependent on the metal work function and electron affinity in the semiconductor especially if the properties vary across the interface. Secondly, the deviation of extracted barrier height between C-V and I-V can be understood assuming the variations of the barrier height is on a length scale smaller than the depletion width, then the magnitude of the depletion width will stay largely unchanged. Thus the values extracted by C-V will be indicative of the average barrier height and not that of the dominating low barrier regions. Finally, the model also sheds light on the physical significance of the ideality factor. Assuming the interface barrier is inhomogeneous, the ideality factor represents the voltage dependence of the dominating barrier for a given measurement [69].

To quantify the degree of inhomogeneity Werner assumes the barrier extracted by I-V is a superposition of thermionic emission over all interface barriers and refers to it as the effective barrier (ϕ_b^{eff}). Because the carrier flux over the barrier is exponentially dependent on temperature, forward current transport at lower temperatures will be dominated by emission over the lower portions of the barrier. At higher temperatures the free carriers have the ability to emit over larger barriers thus, the I-V characteristics will be indicative of a mixture of high and low barrier regions. Effective barrier heights extracted from a range of temperatures can then be thought of as a 'finger print' of the density function of barriers at the interface. Equation (6) can be rewritten either to include the effective barrier or to include the distribution of barriers. Each give an equivalent definition of the current's dependence on voltage so that they can be set equal to each other.

$$\exp\left(\frac{-q\phi_b^{eff}}{kT}\right) = \int_{-\infty}^{\infty} P(\phi_b) \exp\left(\frac{-q\phi_b}{kT}\right) d\phi_b \tag{22}$$

Assuming a Gaussian distribution of barrier heights, Werner and Güttler find that the effective barrier height is temperature dependent according to:

$$\phi_b^{eff} = \bar{\phi}_b - \frac{q\sigma_s^2}{2k_bT} \tag{23}$$

Finally, assuming that the emission of carriers across the interface is solely thermionic, the effective ideality factor can be attributed to the variation of barrier height with voltage. Ideality factors larger than unity imply that as the forward voltage is increased, the effective barrier height increases. Werner-Guttler explain this by noting that image forces could play a part but this effect is likely due to the pinchoff of lower barriers due to neighboring higher barriers as the electric field at the interface is lowered. Accordingly, the ideality factor can be used to extract the voltage dependence of the Gaussian mean ($\Delta\bar{\phi}_b(V)$) and standard deviation ($\Delta\sigma_s^2(V)$).

$$\frac{1}{\eta^{eff}} - 1 = -\rho_2 + \frac{q\rho_3}{2k_bT} \tag{24}$$

$$\Delta\bar{\phi}_b(V) = \rho_2 \cdot V \tag{25}$$

$$\Delta\sigma_s^2(V) = \rho_3 \cdot V \tag{26}$$

Within the literature, this process of evaluating the inhomogeneity at an M-S junction is accomplished by plotting the effective barrier height and ideality factor data against $(2k_BT)^{-1}$ to show linearity, then extrapolate the y-intercept and slope for each set of data.

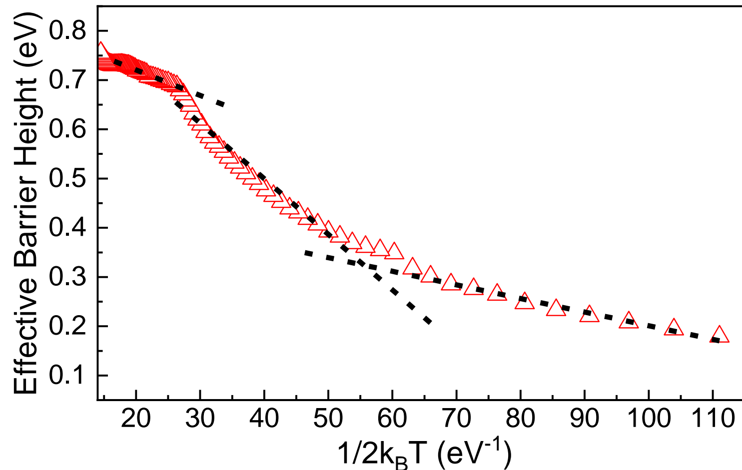

Figure 13. Effective barrier height values (scatter) plotted as a function of 1/2kBT along with the linear fitting of portions of the data (dashed).

Above, in Figure 13 is plotted an example of effective barrier height data extracted from IV measurements between 70 and 400 K. Experimentally, when a large temperature range with dense (<8 K) steps are used to measure the IV characteristics; it is rare that the full range is linear [70-72]. Accordingly, Chand and Kumar [70, 73] adapted Werner-Güttler [69] methods by accounting for the possibility of multiple, non-interacting regions at the MS interface all of which could be described by a Gaussian distribution. If this was the case, the plot of effective barrier height versus $(2k_BT)^{-1}$ would have multiple linear regions such as those shown in Figure 13. Values of y-intercept and slope for each of the linear regions could be extracted so that the mean barrier height, standard deviation and voltage dependence of each could be established for the respective parts of a multi-Gaussian distribution.

However, as Chand and Kumar point out, this method requires a few assumptions be made. First, the reason multiple linear regions would be present in the effective barrier height and ideality factor temperature dependence is because three non-interacting distributions must exists. This simply means that minimal overlap between each Gaussian distribution would have to exist in addition to a monotonic increase in the peak of the Gaussian distributions. Secondly, the extracted vales of mean barrier height need to be monotonically increasing with the temperature range they are extracted from. This implies that the values of mean barrier height extracted from effective barrier heights observable at low temperature would need to be lower than the mean barrier height extracted higher temperatures. Both of these caveats stem from the initial assumption that thermionic emission over a laterally inhomogeneous interface is the primary conduction method. At low temperatures, the density of free carriers at higher energies is lowered and during forward bias, will preferentially emit over lower regions of the barrier. Once temperature is increased, the distribution of free carriers is dispersed over a wider range of temperature so that the current will be indicative of both high and low regions of barrier height with preference given to the more prevalent of the two. When the Chand and Kumars method is applied to the data shown in Figure 13, three regions of linearity are observed but with non-monotonically increasing y-intercepts (mean barrier heights). Thus, it is inaccurate to use this method to describe inhomogeneity at the MS interface.

Jiang et al. [74] improved the technique further by re-deriving the effective barrier height temperature dependence equation assuming a multi-Gaussian distribution. The new dependence is shown below in Equation (27).

$$\phi_b^{eff}(T) = -k_B T \sum_{i=1}^{n} \left[\rho_i e^{-\frac{\bar{\phi}_{b_i}}{k_B T} + \frac{\sigma_i^2}{2k_B^2 T^2}} \right] \tag{27}$$

Here, the temperature dependence of the effective barrier height data controlled by the mean, $\bar{\phi}_{b_i}$, and standard deviation, σ_i^2, of a multi-Gaussian distribution. Additionally, the variable ρ_i represents the weight of the i-th distribution such that:

$$\rho_1 + \rho_1 + \cdots + \rho_n = 1 \tag{28}$$

One of the motivations for using both the Werner-Güttler [69] in addition to the Chand and Kumar [73] methods, was the simplistic data analysis method. As long as the data was linear, a simple linear fitting algorithm could be used to determine the mean and standard deviation of a distribution. With the method presented by Jiang et al. [74] this process could no long be used. Instead, an iterative fitting algorithm needs to be utilized, where the mean barrier heights ($\bar{\phi}_{b_i}$), standard deviations (σ_i^2), and Gaussian weights (ρ_i) could be used to generate the effective barrier height plots. Once generated, the coefficient of determination (R^2) would be calculated and new values of mean barrier height, standard deviation, and Gaussian weights would be selected with the goal of maximizing R^2.

Considering that no limit has been placed on the number of Gaussian distributions used to fit the data, it can be reasonably concluded that inhomogeneity would best be described by an arbitrary distribution. To accomplish this, information on the highest barrier height present at the interface must be known. Without this information, the barrier distribution at values larger than that observed are no longer constrained and as such the fitting algorithm could not determine a single best value. To accurately represent the regions of the interface with large barrier heights, significant temperature may be required to observe thermionic emission over these barrier heights. At a high enough temperature, the material characteristics of the interface could change. By using a continuous function (such as Gaussian), the form of the distribution at unobserved barrier height values (those measured at temperatures below or above what was actually measured) is constrained by the fitting done against those that are observed. In Section 3.1, the inadequacies of the traditional multi-Gaussian distribution is shown and work is presented on applying a modified log-normal distribution to fit experimental data.

2.3.3 Reverse Thermionic Field Emission Current

In an ideal Schottky diode biased in reverse, it's typically assumed that current caused by tunneling is minimum and thermionic emission over the barrier is the dominating conduction mechanism. For a voltage-independent barrier, the induced current will have no voltage dependence for applied biases larger than $3k_bT$ and an absolute magnitude determined by the saturation current defined below:

$$I_S = AA^*T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \tag{29}$$

However, examination of the literature reveals that experimentally measured reverse IV data on fabricated Schottky diodes rarely observes this behavior [47, 75-79], thus additional current conduction mechanisms should be considered. Introducing the phenomenon of image-force lowering, present in all

MS junctions, the induced Schottky barrier height can no longer be considered constant for applied voltages. In reverse bias, the saturation current is modified with a voltage dependent barrier height as shown below:

$$\Delta\phi_b = \sqrt{\frac{qE_{Max}}{4\pi\varepsilon_s}} \quad (30)$$

Where the maximum electric field at the MS interface is defined by:

$$E_{Max} = \sqrt{\frac{qN_D(V_{BI} - V_A)}{\varepsilon_s}} \quad (31)$$

Here, N_D is the free carrier concentration, V_{BI} is the built-in voltage, and V_A is the applied voltage. From Figure 14, comparing the simulated current density of a diode with and without assuming image-force lowering, there exists a large rise in current around zero-bias caused by the maximum electric fields square root dependence on applied voltage. Additionally, with this modest alteration to the theoretical diode equation, the induced current density at -150 V is expected to be >1 order of magnitude greater once a voltage dependent barrier height is applied.

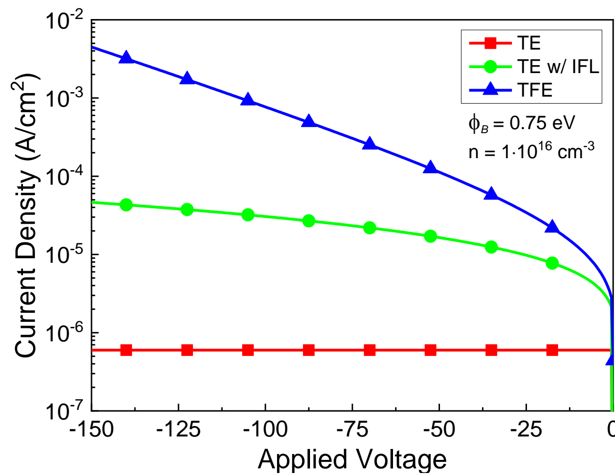

Figure 14. Simulated reverse current density for a Schottky diode on GaN with a barrier height of 0.75 eV and free carrier concentration of 10^{16} cm^{-3}. The three curves represent current calculated assuming only thermionic emission (■), thermionic emission with image force lowering (●), and thermionic field emission (▲).

Although assuming image-force lowering of the barrier is adequate to explain why experimental data may have a voltage-dependent reverse current, often the reported magnitudes are much higher. To compensate for this additional deviation, experimental data is assumed to also suffer from electron tunneling through the thinned barrier at the MS interface under reverse bias, also known as thermionic field emission (TFE). In an ideal n-type Schottky diode (assuming no IFL), as reverse bias is applied the conduction band is pulled down relative to the metal fermi-level while the barrier height remains constant. Thus, as the electric field at the interface increases, the lateral thickness of the forbidden region at the semiconductor's surface decreases with the thinnest portion existing at the top of the barrier. At reverse voltages large enough to pull the conduction band minimum below that of the metal fermi-level, the probability of electrons tunneling from the metal to the semiconductor can no longer be ignored. Current conduction caused by tunneling carriers at the metal fermi-level is called field emission (FE), while

current conduction caused by carriers with thermal energies above the metal fermi-level is called thermionic field emission (TFE).

Calculating the portion of current caused by tunneling at the MS interface into the semiconductor while under reverse biases requires knowledge of the energy distribution of carriers in both the semiconductor and the metal. Additionally, the probability of tunneling through the barrier calculated at each voltage from the conduction band minimum to the top of the barrier is required. This calculation is reflected below in Equation (32).

$$J_{TFE} = \frac{A^{*}T}{k_B} \int_{E_{C_{Bulk}}}^{E_{C_{Barrier}}} F_m(E) \cdot P(E) \cdot [1 - F_s(E)] dE \tag{32}$$

$$F(E) = \left[1 + \exp\left(\frac{E - E_f}{k_B T}\right)\right]^{-1} \tag{33}$$

$$P(E) = e^{\frac{-2\sqrt{2m^{*}}}{\hbar}} \int_{x_1}^{x_2} \sqrt{q\phi_D - E}\ dx \tag{34}$$

Here, the current is being determined by multiplying the carrier distribution on each side of the barrier (F_m and F_s) by the tunneling probability (P) and integrating across the energy from the conduction band minimum ($E_{C_{Bulk}}$) to the top of the barrier ($E_{C_{Barrier}}$). The carrier distribution can be expressed with the fermi-function shown in Equation (32) referenced to the respective fermi-level (E_f) within the metal or semiconductor. Tunneling probability is calculated using the Wentzel-Kramers-Brillouin (WKB) approximation of Schrödinger's equation for a particle arriving at an energy barrier shown in Equation (34). Thus, the tunneling probability becomes a function of the integrated energy difference between the carrier's energy level and the top of the forbidden region from the 'classical turning points' at a respective energy level.

Typically, the value of TFE current is calculated by approximating the form of the conduction band barrier with a triangle whose shape depends on the applied voltage and multiplying the probability distribution with the metal fermi-function where $[1 - F_S]$ is approximated to 1 [80]. Additionally, any perturbation of the barrier height by IFL is simply reflected in the expression for the triangles barrier's height. The appeal of this method is that an analytical solution can be found and easily applied; however, significant error can arise due to over approximation of the shape of the barrier at high voltages and elevated temperatures especially when image-force lowering is assumed. To minimize these errors, evaluation of the TFE current for a specific diode must be solved numerically.

2.3.3.1 Numerical Calculation of TFE

To understand the effect that metal and semiconductor characteristics have on the reverse current conduction properties of a Schottky diode, a program for evaluating the thermionic emission, thermionic field emission and perturbation caused by image-force lowering was created. Here, no approximations of the barrier form is assumed; however, digitization of the process requires quantizing the energy steps so that a balance can be reached between accuracy and computational efficiency. Finally, the results of each calculation can be fed into a dampened least-squares fitting algorithm so values of barrier height, free carrier concentration and conduction area can be fit with experimental data. Below, the process of approximating TFE and TE current with IFL is described.

Because the fermi-functions are easily calculated, most of the effort in calculating TFE current come in simulating the conduction band near the M-S interface and then calculating the effective tunneling probability. To accomplish, poisons equation is first used to determine the ideal band curvature of the conduction band in a uniformly doped Schottky diode. The following equation is used:

$$\frac{d^2\phi}{dx^2} = -\frac{\rho}{\varepsilon_s} = -\frac{q}{\varepsilon_s}n \tag{35}$$

$$\phi(x) = \begin{cases} 0 & x \leq 0 \\ \frac{q}{2\varepsilon_s}\left[x_d^2 - (x_d - x)^2\right] & 0 < x < x_d \end{cases} \tag{36}$$

$$x_d = \sqrt{\frac{2\varepsilon_s(V_{BI} - V_A)}{qn}} \tag{37}$$

$$V_{BI} = \phi_B - k_B T \cdot ln(N_C/n) \tag{38}$$

Here, Poisson's equation (shown in Eq (35)) is used to calculated the conduction band offset (ϕ) as a function of depth, $\phi(x)$, from the M-S junction ($x = 0$) to the depletion width edge ($x = x_d$). Note that the approximation of no free carriers (n) in the depletion region is made. The result is a piecewise equation shown in Eq (36) that can be used to graph the conduction band as shown in Figure 15 (red) out to the depletion region edge. Further calculations of the band are not necessary since tunneling probability is assumed zero for energies lower than the conduction band minimum. Next, conduction band form can be modulated by the presence of image forces lowering simply by subtracting the electric potential derived from the increasing electric field near the M-S interface.

$$qE(x) = \frac{-q^2}{4\pi\varepsilon_s(2x)^2} \tag{39}$$

$$\phi(x) = -\int_x^\infty E(x)dx = \frac{q}{16\pi\varepsilon_s x} \tag{40}$$

The electric field as a function of the distance from the M-S interface, $E(x)$, is written in Equation (39) and by again using Poisson's equation the electric potential due to image-force lowering can be found, shown in Equation (40). The perturbation of the semiconductor conduction band caused by IFL is visualized below in Figure 15 (green) at zero bias and at an applied bias of -100 V.

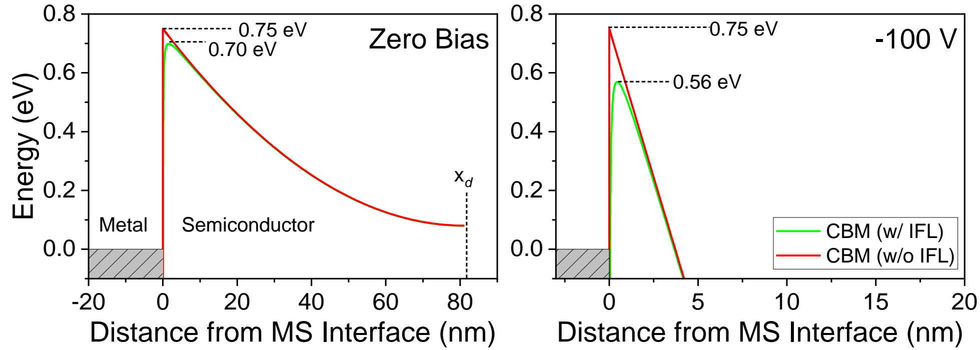

Figure 15. Energy band calculation at a metal-semiconductor interface. The colored lines represent the calculated CBM with (green) and without (red) image-force lowering. Additionally, the energy bands were calculated for an MS junction under zero-bias (left) and under a reverse bias of -100 V (right).

As the electric field at the interface is increased at a M-S interface without IFL, the barrier height remains constant but the thickness drastically decreases. In the figure above, at zero bias electrons with kinetic energy near the metal fermi-level would have to tunnel 60 to 80 nm to reach the conduction band. Once a reverse bias of -100 V is applied, this distance drastically decreases to <5 nm. Next considering a junction where IFL is present, it can be see that a majority of the perturbation is not caused by the thinning of the barrier but by the barrier height reduction. At zero bias, the barrier height is effectively reduced from 0.75 to 0.70 eV and under the reverse bias of -100 V it decreases further to 0.56 eV, a 25% reduction of the barrier. From this calculation, the importance of considering image force lowering during calculations of TFE can be observed.

Next, in order to evaluate the tunneling probability at energies from the top of the interface barrier to the bulk conduction band, the forbidden region width at a specific energy level must be found. This is accomplished simply by quantizing the energy values between the maximum and minimum conduction band values and extrapolating the two conduction band intercepts. With this information, the tunneling probability can be numerically evaluated as a function of the conduction band formula, which is in turn a function of voltage. Below, in Figure 16 (cyan), the tunneling probability is evaluated for the conduction band shown to the right (green). Additionally, the metal (red) and semiconductor (blue) fermi-functions are evaluated and multiplied with the tunneling probability to for the total probability (black). Finally, the integral in Equation (32) is evaluated using the trapezoidal rule and the current at a specific voltage is solved for.

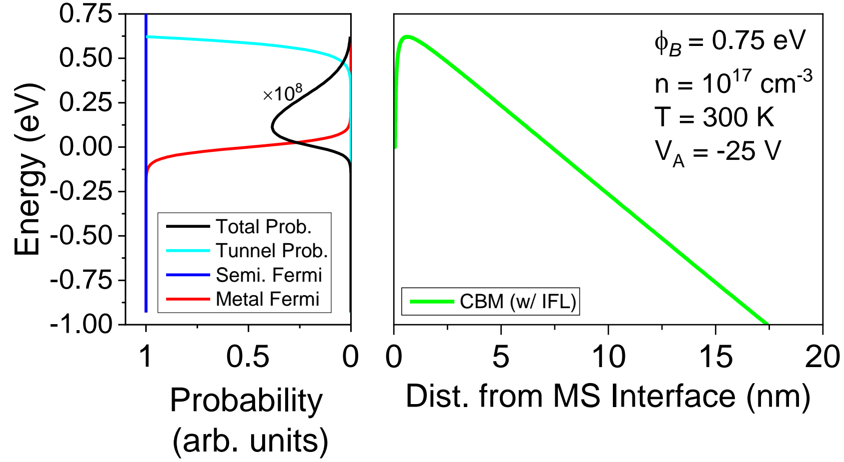

Figure 16. Probability functions (left) calculated for a GaN Schottky diode CBM (right) under reverse bias. On the left the metal fermi level (red), semiconductor fermi level (blue) and tunneling probability (cyan) distributions are plotted as a function of the energy referenced to the metal fermi-level. Multiplying each of these distributions together (black) results in an energy dependent distribution peaked at 0.12 eV above the metal fermi-level.

2.3.4 CV Characterization

Capacitance vs. voltage (C-V) measurements are commonly used to characterize semiconductor layers and devices including Schottky diodes, PN diodes, MOS capacitors, and MOSFETs to name a few. Some of the extractable parameters include barrier heights, layer thicknesses, effective carrier concentrations and interfacial impurity information. This makes C-V characterization techniques a valuable tool in understanding the role that semiconductor growth and device fabrication methods have on the final structure. In this section there is a discussion of the underlying principles including a brief overview of measurements methods used to evaluate semiconductor layers and Schottky diode device properties.

2.3.4.1 Schottky Depletion Dependence

In its simplest form, a capacitor is made of two parallel conducting plates with area, A, separated by some distance, d, across a non-conducting medium with a dielectric permittivity characterized by ε_r. The formula for the total capacitance is thus:

$$C = \varepsilon_r \frac{A}{d} \tag{41}$$

In semiconductor devices, this implies that a capacitor will exists when two conducting layers are separated by a non-conducting dielectric layer. This exists between the gate metal and channel of a MOSFET, the Schottky metal and the edge of the depletion region of a Schottky diode and between the depletion edges inside the p-type and n-type layers of a PN diode. Simply measuring the capacitance without applying a DC offset can yield information about the separation of the 'parallel-plates' or the magnitude of dielectric constant, however the real usefulness of C-V measurements comes from simultaneously varying the DC bias on the device under test. In doing this, information regarding the variation of charge densities can be gleaned from the resulting change in capacitance. The capacitance of a Schottky diode is [81]:

$$C = A\sqrt{\frac{q\varepsilon_r(N_D - N_A)}{2\left(V_{BI} - V_A - \frac{k_B T}{q}\right)}} \tag{42}$$

In Equation (42), N_A and N_D are the intentional acceptor and donor concentration (assuming full ionization), A is the profiled area, V_{BI} is the built-in voltage, and V_A is the voltage applied to the diode.

As the bais on a Schottky diode is varied, the depletion width and thereby the capacitance is expected to vary. Increasing the reverse bias on the diode will increase the depletion width and the capacitance will decrease. When the diode is forward biased, the capacitance will increase as the depletion width decreases. As the semiconductor reaches flat band conditions, the depletion width will approach zero while the capacitance approaches infinity. In the equation above, we see that the variation of capacitance with voltage depends on the free carrier concentration and built-in voltage, two quantities typically unknown prior to testing but can be extracted from experimental C-V data.

Below, in Figure 17 (Left), a typical C-V characteristic for a Schottky diode on GaN is shown alongside the A^2/C^2 vs. voltage plot. According to Equation (42), solving for A^2/C^2 yields an equation whose slope depends on the effective free carrier concentration and x-intercept depends on the built-in voltage. The dashed line is a linear fit to the data and implies that the profiled depth has a constant effective free carrier concentration. In Figure 17 (Right) the calculated effective free carrier concentration vs. depletion depth is calculated by taking the running slope of 7 points along the A^2/C^2 curve and using Equation (41) to solve for the depletion depth (d) with the measured capacitance value.

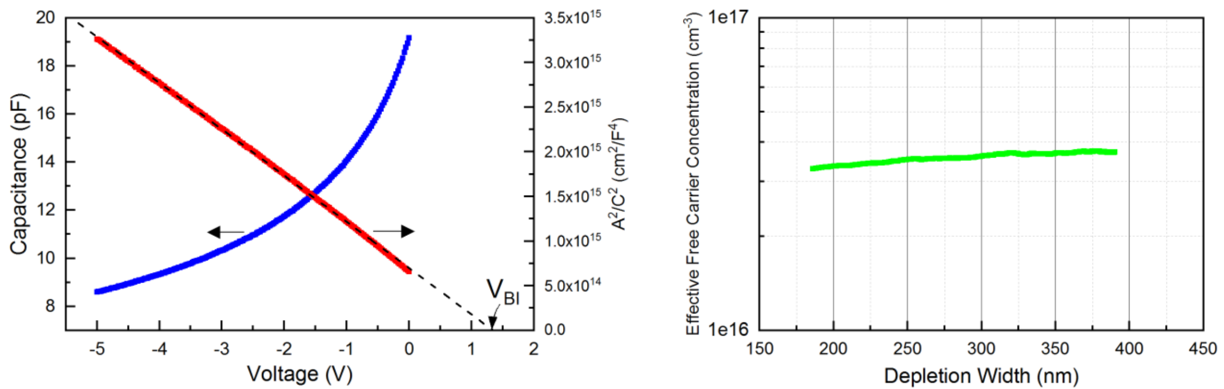

Figure 17. (Left) Typical C-V characteristics of a Schottky diode including the A^2/C^2 used to extract effective free carrier concentration and built-in voltage (Right) Effective free carrier concentration vs. depletion depth extracted from the slope of the A^2/C^2 and the measured capacitance.

In a Schottky diode, the build-in voltage can be used to calculate the M-S junction barrier height by noting that at zero-bais $V_{BI} = \phi_b - (E_c - E_f)$ (NOTE: this is for an n-type Schottky diode). This results in the following equation

$$\phi_b = V_{BI} + \frac{k_b T}{q} \ln\left(\frac{N_C}{N_D}\right) \quad (43)$$

Where, V_{BI} is the x-intercept voltage extracted from the A^2/C^2 graph, N_C is the density of states in the conduction band, and N_D is the effective free carrier concentration extracted from the slope of the A^2/C^2 graph. The barrier height extracted here rarely matches that of the IV-derived barrier height for Schottky diodes considered to have an inhomogeneous interface. This is due simply because the barrier height extracted from CV measurements is measured from a signal applied away from the interface while the free carriers contributing to the current in IV measurements will preferentially conduct across lower

barrier heights resulting in lower overall extracted barrier heights. Therefore, the barrier height extracted from CV is considered the average whenever barrier inhomogeneity is present [69].

It should be noted that complications with the extraction of effective free carrier concentration and barrier height arise for non-uniformly doped regions. In semiconductor layers where the carrier concentration at the M-S interface is different than that being profiled, a curvature in the A^2/C^2 graph will cause deviation in linearly extrapolated x-intercept values. A simple fix is to profile closer to the M-S interface; however, this required forward biasing which will induce appreciable current conduction and therefore complicate the measurement of the capacitive element in the diode.

2.3.5 Deep Trap Characterization

In first principle calculations of semiconductor device properties it is assumed that the crystal lattice is perfect, meaning there are no defects. Defects include any foreign atomic species (impurities) introduced either during growth [82, 83] or by external means (i.e. ion bombardment [84-86]) and disorder in the crystalline structure of the semiconductor [87]. When controllable, these defects can be extremely helpful in applications where they can be used as a dopant or compensation source to create high and low conductivity layers respectively. However, unintentionally introduced defects been shown to cause many problems in high power devices including static vs. dynamic characteristic variation, premature failure, and deviations from theoretical behavior. This makes understanding the cause and effect of electrically active defects in semiconductor devices of the utmost importance.

2.3.5.1 Deep Level Trap Mathematical Analysis

Electrically active defects, also known as deep-level traps, can be viewed pictorially as shown below in Figure 18 where they are characterized by a trap energy, E_T, an effective capture cross-section $\sigma_{n/p}$, and density, N_T. Deep level traps characterized with a levels closer to the conduction band are typically referred to as electron traps while those characterized with levels closer to the valence band are referred to as hole traps and act as generation-recombination (G-R) centers. This G-R can be activated thermally or optically and ultimately leads to an additional time-dependence of the electron and hole concentration in the conduction and valence band respectively.

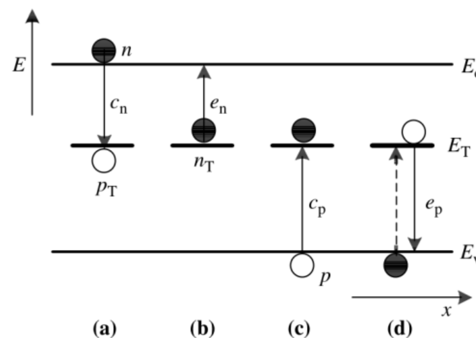

Figure 18. Band diagram showing free carrier capture and emission paths assisted by a deep level trap state located at the energy level E_T [88]

This time dependence is expressed in Equations (44) and (45) for the electron density in the conduction band and the hole density in the valence band respectively. In the case of the conduction band the emission process is characterized by e_n, the emission rate of electrons in to the conduction band and n_T, the density of trapped electrons. The capture process depends on the density of available free electrons, n, in the conduction band, the density of trapped holes, p_T, and the volumetric capture coefficient of electrons from the conduction band, $c_n = v_{th}\sigma_n$. A similar picture holds for the valence band.

$$\frac{dn}{dt} = e_n n_T - c_n n p_T \tag{44}$$

$$\frac{dp}{dt} = e_p p_T - c_p p n_T \tag{45}$$

These equations can be applied to understand the occupancy of the traps so that,

$$\frac{dn_T}{dt} = \frac{dp}{dt} - \frac{dn}{dt} = (c_n n + e_p)(N_T - n_T) - (c_p p + e_n)n_T \tag{46}$$

Noting that the concentration of trapped holes is the concentration of trap centers less the concentration of trapped electrons ($p_T = N_T - n_T$). From here, the differential equation can be solved; however, quite a few simplifications can be made depending on the material and structure of a device under test. Assuming first that trapping signatures will occur in a reverse-biased depletion region, secondly that the quasi-neutral regions have a non-time dependent carrier concentration ($n(t)$ and $p(t)$ are constant) and finally, that the trapping signature is coming only from a single layer of n-type material. These assumptions can be made in devices such as an N-type Schottky diode or one-sided PN junction (P++/N) where the reverse bias depletion width variation happens mainly in the n-type layer. Solving for the trapped electron concentration time-dependence we get the following equation (note: a similar equation exists for a p-type layer).

$$n_T(t) = n_T(0)e^{-t/\tau} + (e_p + c_n n)N_T\tau(1 - e^{-t/\tau}) \tag{47}$$

Where $\tau = 1/(e_n + c_n n + e_p)$. Finally, as with most semiconductor characterization techniques, a testing procedure needs to be implemented in order to minimize the effect different terms have in the measureable quantities so that extracted terms can be determined with minimal uncertainty. Considering Equation (47), this can be accomplished by perturbing the sample so that only the effects of carrier capture or emission are observable.

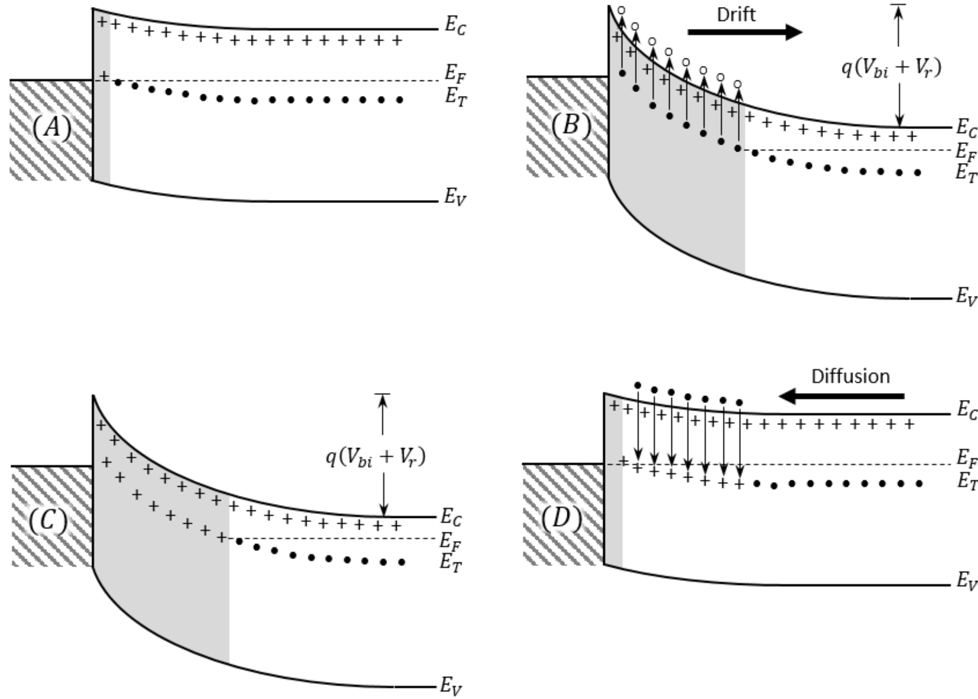

Figure 19. A schottky diode at (A) zero bias, (B) instantaneously after applying a reverse bais, (C) after charge emission has reached steady-state, and (D) instantaneously after returning to zero-bias. Figure modeled after [89]

Considering a Schottky diode under equilibrium conditions, trap levels above the fermi level are considered fully ionized thus giving rise to fixed ionized charge from the dopant species throughout both the depletion region and quasi-neutral regions and from deeper levels ionized by the bending of the bands in the depletion region as shown in Figure 19 (A). Instantaneously after reverse biasing the junction increases the depletion region width and exposes a volume of previously filled traps into a condition which exclusively favors emission, Figure 19 (A) to (B). Trapped carrier emission is favored in the depletion region because, once emitted, free carriers are swept out due to the intrinsic and extrinsic electric fields. These transit times are much shorter than typical capture times. Thus, this provides a situation for which the electron capture coefficient goes to zero so that, in addition to assuming only upper band trap contributions ($e_n \gg e_p$), Equation (47) becomes:

$$n_T(t) = n_T(0)e^{-t/\tau_e} \quad \textbf{(48)}$$

where $\tau_e = 1/e_n$. Likewise, a similar situation can be created for electron capture by first considering the case where the device is kept under reverse bias and once all of the trapped charge has been emitted and steady-state has been reached, Figure 19 (C), the magnitude of reverse bias is reduced, Figure 19 (D). Now the fermi-level resides at a position above previously unpopulated trap levels leading to a case where free carrier capture is favored over carrier emission within the swept volume. This leads to Equation (49) where $\tau_c = 1/c_n n$.

$$n_T(t) = N_T - (N_T - n_T(0))e^{-t/\tau_c} \quad \textbf{(49)}$$

Finally, a detailed understanding of the effect that material and trap characteristics have on the emission and capture rates must be established so that the detectable properties of the trap can be related to its energy level, capture cross-section and density. Considering the case for electron trapping rates as described in Equation (44) in equilibrium we find that $\frac{dn}{dt} = 0$ so that:

$$e_{n0} n_{T0} = c_{n0} n_0 (N_T - n_{T0}) \tag{50}$$

Where

$$n_0 = n_i e^{\frac{E_f - E_i}{k_b T}} \tag{51}$$

$$n_{T0} = \frac{N_T}{1 + e^{\frac{E_T - E_f}{k_B T}}} \tag{52}$$

Here, both the equilibrium electron concentration in the conduction band (n_0) and the equilibrium concentration of trapped electrons (n_{T0}) depend on fermi statistics. From here, we can combine these equations into the following.

$$e_{n0} = c_{n0} n_i e^{\frac{E_T - E_i}{k_B T}} \tag{53}$$

Next, an assumption that the emission and capture rates do not vary between equilibrium and non-equilibrium condition is made. This assumption is not necessarily true but is commonly made so that simple analysis of the material can be made. Resulting analysis will thus inevitably have uncertainty in the extracted results in addition to those added by the measurement apparatus. With $c_n = \sigma_n v_{th}$, and expansion of n_i, the emission rate becomes

$$e_n = \frac{\sigma_n v_{th} N_C}{g} e^{\frac{E_T - E_C}{k_B T}} = \frac{1}{\tau_e} \tag{54}$$

where g is the degeneracy factor. Finally, substituting the thermal velocity and density of conduction band states equations, the commonly used equation for emission rate is as follows

$$\ln\left(\frac{e_n}{T^2}\right) = \ln\left(\frac{16\pi m_e^* k_b^2 \sigma_n}{g h^3}\right) - \frac{E_c - E_T}{k_b T} \tag{55}$$

2.3.5.2 Deep Level Signature Measurement

Now that a mathematical description has been presented, a means of detecting a deep level traps signature is required. From the previous analysis, fabricating a Schottky diode and reverse biasing the junction according to Figure 19 causes free carrier to either populate the conduction band when baising the device from (A) to (B) or capture and reduce the free carriers in the conduction band when biasing from (C) to (D). These processes are not instantaneous and thus will induce a small but measurable current perturbation. Additionally, in both cases the net electric field in the depletion width will vary as the trap levels become ionized or neutral during the emission or capture process. This variation in electric field in turn perturbs the depletion width which is measureable by capacitive means according to Equation (41) where the parallel plate separation (d) can be replaced with the depletion width (W). Although charge-based and current-based measurements of the deep level traps exists, this discussion is limited to only capacitive-based measurements.

If fixed charges in the depletion region exists in addition to the already assumed dopant species, the measured capacitance will vary according to the following:

$$C(t) = \sqrt{\frac{A^2 q \varepsilon_r \big(N_D - n_T(t)\big)}{2(V_{bi} + V_r)}} = C_0 \sqrt{1 - \frac{n_T(t)}{N_D}} \tag{56}$$

Where C_0 is the capacitance of the device when the depletion region has no trapped charges (i.e. $n_T \to 0$). Making a first order approximation of Equation (56) and substituting Equation (48) for $n(t)$ we end up with,

$$C(t) \approx C_0 \left(1 - \frac{n_T(0)}{2N_D} e^{-t/\tau_e}\right) \tag{57}$$

Figure 20 shows the effect of biasing an n-type Schottky junction on the time-dependent capacitance. Initially, the device is assumed to have reached steady-state for some reverse bias at which point the magnitude of reverse bias is decreased, leading to free electrons being captured into previously ionized trap levels. This process manifests itself as a capacitance transient directly after the reduced reverse bias magnitude is applied. Given enough time, the capture process reaches steady-state. The device is then returned to the original reverse bias condition and again a capacitance transient is observed but opposite in form since its cause is from the emission process. Finally, given enough time, the emission process will saturate and the capacitance value will return to its initial value, C_0.

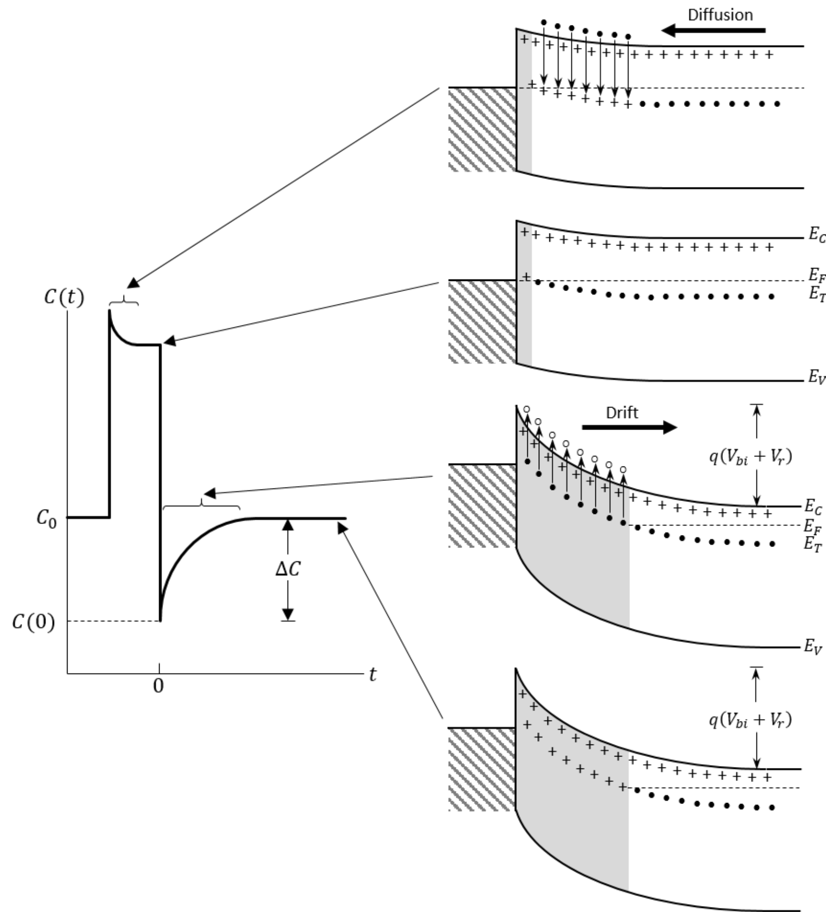

Figure 20. Schottky diode showing the cause of the time dependent capacitance in steady-state and instantaneously after reverse bias reconfiguration. Figure modeled after [89].

2.3.5.3 Deep Level Transient Spectroscopy (DLTS) Data Analysis

Now that a basis for measuring the signature of traps has been established, a means of interpreting the data for comparison is necessary. The method used in this work is a mixture of what is known as Computer-DLTS where capacitance transients at different temperatures are saved digitally and Lang's [90] original rate window analysis where only specific times during the capacitance transients are analyzed. As will be discussed later, this gives the flexibility of simple transient analysis with the ability to review and reanalyze the data without having to re-measure a sample all at the cost of large data files (>200MB).

2.3.5.4 Lang's Rate Window Analysis

In the previous sections, the capacitance transient and the temperature-dependent emission rate are shown to depend on Equations (55) and (57) respectively. The usefulness of Lang's method was the simplification of data analysis process so that traps could be visualized as peaks in what is known as a DLTS spectrum shown in the top-right of Figure 21. The rate window concept can be applied to the capacitance transients by first assuming they are monotonically decaying exponential functions of time. Next, two points in time are selected (t_1 and t_2) and the difference in capacitance magnitudes directly after emission conditions are applied are recorded. Mathematically, according to Equation (57), this results in the following relationship:

$$C(t_1) - C(t_2) = \frac{n_T(0)}{2N_D} C_0 \left(e^{-\frac{t_2}{\tau_e}} - e^{-\frac{t_1}{\tau_e}} \right) \tag{58}$$

From this it can be seen that changing the emission rate and acquiring a new transient will also change the magnitude of the capacitance difference taken at the two points in time. Accordingly, when the emission rate is low, the capacitance transient should not vary much within the window of time which is being analyzed thus leading to almost no difference in capacitance between t_1 and t_2. If the emission rate is very high, the transient will decay so quickly that steady-state is reached prior to t_1 and again there will be no different in capacitance between the two times. In between these two situations the capacitive difference will not be zero and, assuming an exponential function, will peak at some emission rate given by

$$e_{max} = \frac{\ln\left(\frac{t_2}{t_1}\right)}{t_2 - t_1} \quad (59)$$

The variation of emission rate can be accomplished by varying the temperature, where it is expected to have slower emission rates at lower temperature and increased emission rates at higher temperatures for a given trap. On the left-side of Figure 21 capacitance transients were performed for temperatures varying from 60 to 400 K. At lower temperatures (blue) the transients have almost no time dependence indicating that the emission rate is slow. Upon increasing the temperature (>200 K) the capacitance transients begin to show a time dependence and further increases in temperature lead to faster transient decay times. Plotting the capacitance magnitude difference at $t_1 = 140ms$ and $t_2 = 270ms$ results in the blue peak shown in the upper-right graph in Figure 21. As previously mentioned, notice that the result of increasing capacitance decay rate results in a peak on DLTS spectrum plot. Again, this is due to slower transient times resulting in almost no change in capacitance, faster transient times resulting in missing the time-dependence and measuring only the steady-state signal and those in between resulting in a non-zero magnitude. Repeating this procedure for other time windows results in a multiple DLTS spectrum each with their own peaks but shifted on the temperature axis. Next, the time window used to create the spectrum and the temperature at which a peak occurs can be used to generate the $\ln\left(\frac{e_n}{T^2}\right)$ vs. $1/T$ plot shown in the bottom-right of Figure 21. The Arrhenius plot shows the three points extracted form the DLTS spectrum as red, green and blue along with others derived from different time windows (not shown) as grey. Finally, the data can be fit (dashed line) according to Equation (57) and the value for the energy difference between the conduction band and trap level (ΔE_T) along with the capture cross section (σ_n) can be extracted.

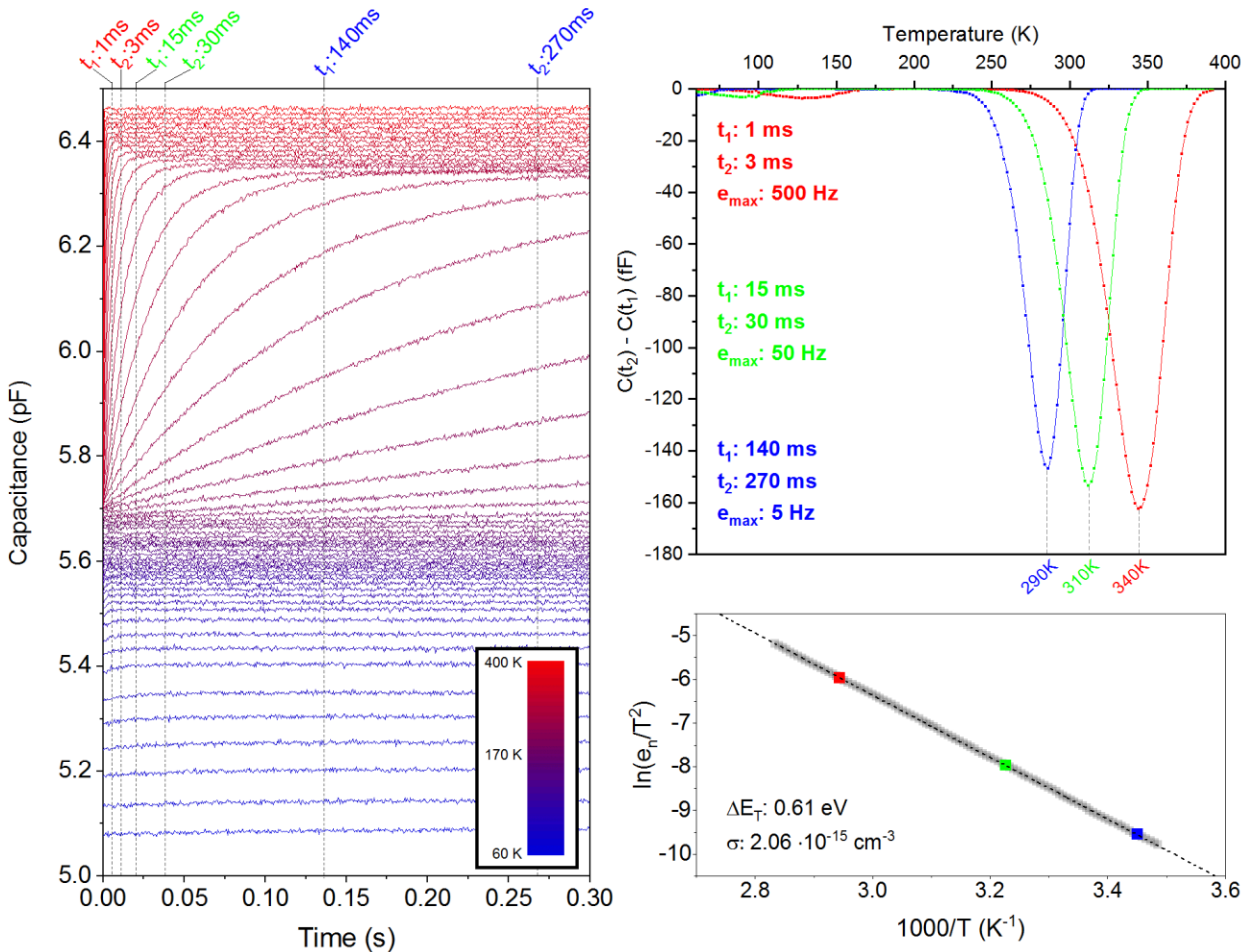

Figure 21. (Left) Experimental capacitance transient data taken between 60 K and 400 K. The dashed lines represent the t_1 and t_2 for three different emission rates colored red, green, and blue. (Top-Right) DLTS spectrum for three emission rate windows each of which is fit to extract the temperature at which the maximum occurs. (Bottom-Right) The emission rates and temperatures are plotted on an Arrhenius plot which is used to extract the characteristic trap energy and capture cross-section.

When first created, DLTS measurement systems did not have the luxury of saving the high density of data required to represent the capacitance transients and thus required a method to simplify the acquisition. Lang's [90] method requires that only two points be taken during a capacitance transient resulting in a single point on the Arrhenius plot. Thus multiple time consuming temperature sweeps were required to fill out the plot with more points and improve fitting. Additionally, analyzing only two points of a transient could lead to erroneous results from a non-exponential time dependence as a result of minority carrier capture or poor sample preparation.

2.3.5.5 Computer-DLTS Techniques

As discussed at the end of the previous section, there are draw backs to applying Lang's [90] method and only measuring the capacitance transient at two points during the transient. Because computer processing capabilities have come a long way since then, capturing and saving transients at high speed and high resolutions is possible. In this section, the additional steps required to capture, filter, fit and analyze DLTS/SSPC transients is detailed.

2.3.5.5.1 Transient Filtering

Due to noise common to electrical test equipment a filtering process is executed to help distinguish the real signal from its background. As such, the reported data is extracted from 50 to 70 transients averaged in real-time with previous measurements made in the same pulsing cycle. As a result, the time it takes to acquire a single transient increases but the signal-to-noise ratio will increase proportionally to the square root of the number of averages taken. The effectiveness of this method is visualized below in Figure 22.

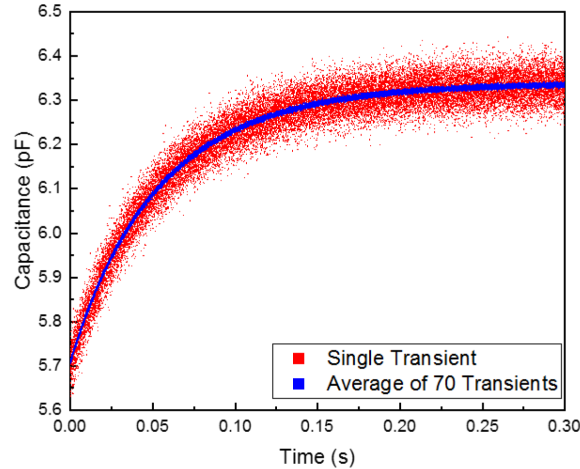

Figure 22. (Red) Experimental capacitance transient taken at room-temperature compared to (Blue) the averaged result of 70 transients.

2.3.5.5.2 Transient Fitting

Fitting the transient data with its theoretical equation can be beneficial in decreasing file size, as an indicator of closely spaced traps and as an additional means of increasing the signal-to-noise ratio in the DLTS spectrum. If observation of the transient is necessary but smaller data files are also required, capacitance transient data can be fit with Equation (60) and only the characteristic variables can be saved. This work uses the Levenberg-Marquardt least-squares minimization algorithm.

$$C(t) = \sum_{i=1}^{n} [A_i e^{-t/\tau_i}] + B \tag{60}$$

Secondly, in the case where two traps with similar characteristics exists in the same sample, it can be difficult to identify the summation of multiple transients. If the data does not fit well across the full time scale, additional amplitude (A_i) and time constant (τ_i) sets can be introduced within reason. If this introduction results in a better fit across a single transient it can then be applied to subsequent transients within a temperature range in which these traps are active. If an adequate fit exists across multiple transients this is a good indicator that more than on trap exists with similar characteristics (i.e. closely space trap energy levels).

Finally, because subsequent averaging of the transients follows the law of diminishing returns additional means of increasing the signal-to-noise ration can be helpful. Thus, utilizing the fitting parameters in the construction of a DLTS spectrum will improve subsequent extractions. The results of applying this fitting method is shown below in Figure 23. The transient derived and fit derived DLTS spectra overlap very closely in regions where the transient noise level is much smaller than the difference in capacitance

magnitudes (i.e. 250 to 360 K). At lower temperatures, in the region marked ‘x10’, an additional peak can be observed in the fit derived spectra that could not be reliably extracted in the transient derived spectra.

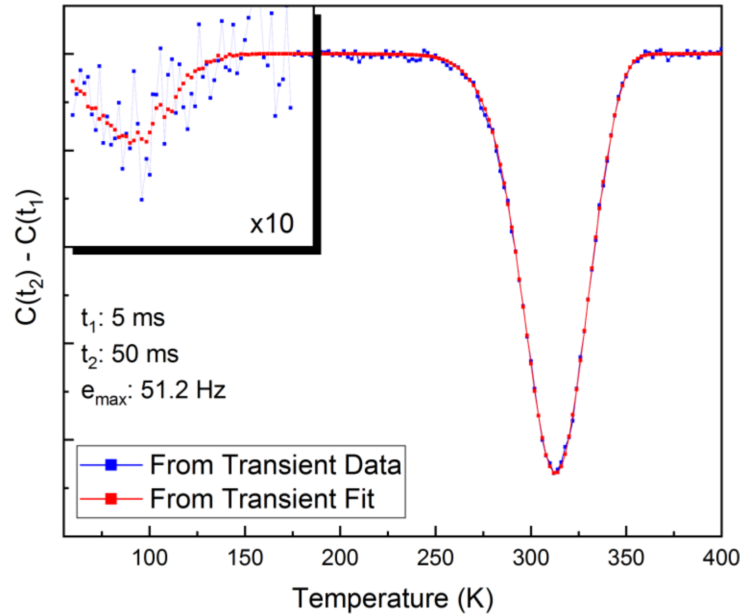

Figure 23. Example of DLTS spectrum derivation from (Blue) raw transient data and (Red) exponential fit data according to Equation (60)

2.3.5.5.3 DLTS Spectrum Peak Fitting

To successfully populate the Arrhenius plot with points, the application of many emission rate windows need to be applied to the transients and then accurate selection of the temperature for which the spectrum peaks needs to be determined. Simply selecting the local minimum or maximum can cause problems if a transient is missing or there is considerable amount of noise. Thus relying on the surrounding points improves the confidence in value extraction. This work relies on Equation (61) to fit single or multiple Gaussian peaks to a DLTS spectrum.

$$D(T) = \sum_{i=1}^{n} \left[A_i e^{-\frac{(T-\overline{\mu_i})^2}{2\sigma_i^2}} \right] + B \quad (61)$$

Here, A_i is a peaks amplitude, $\overline{\mu_i}$ is the tempertaure at which the peak is a local maximum or minimum, σ_i is the Guassian standard deviation, and B is the offset. These parameters are used as input to a levenber-marquardt fitting routine. The figure below shows the successful fitting of the larger peak shown in Figure 23 with two Gaussian peaks indicating that two traps with similar characteristics exists.

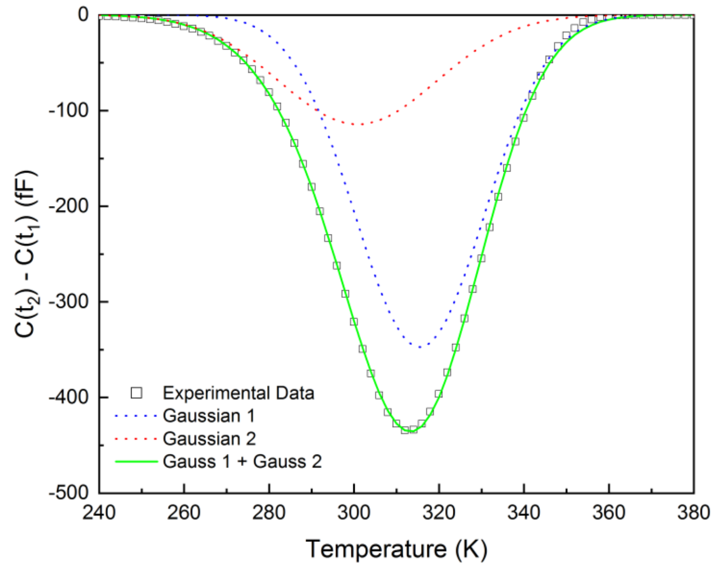

Figure 24. Experimental DLTS spectrum data fit with multiple Gaussian curves so that peak location can be recorded.

2.3.5.6 Steady-State Photocapacitance and Deep-Level Optical Spectroscopy

As stated in the previous section, the viability of DLTS is heavily dependent on the trap depth and the measurement capabilities. Practically, trap characterization with DLTS is limited to ~1 eV since profiling deeper would require temperatures capable of altering the semiconductor itself. The capabilities of the reported data span a temperature range of temperatures from 50 to 400K and emission rate detection capabilities of 0.6 to 700 Hz. In Figure 25, the theoretical calculation of emission rate for traps levels where the effect of varying trap level and capture cross-section are shown. A typical temperature-varying measurement stage is limited on the lower end by the type of cooling used such as liquid nitrogen (77K), closed-cycle He cryocooler (~20K), or liquid He (4K). At the higher temperature range, measurement is limited by the effect increased thermal energy has on the profiled material [91, 92]. The emission rate is limited on the lower end by the length of time a sample can be measured and on the upper end by the transient capture method (current, chrage or capacitance) and the data conversion rate. Traps whose characteristic line falls inside the grey boxes shown in Figure 25 are measureable by system used to take data reported in this work.

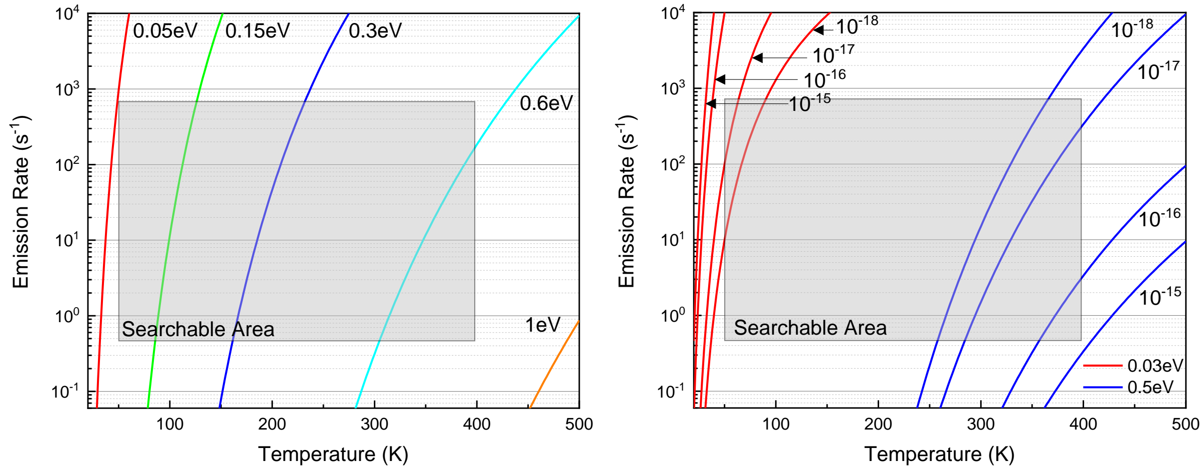

Figure 25. Emission rate vs Temperature plot showing the characteristics of electron traps close to the conduction band. This plot dictates the required measurement capabilities for traps with (Left) varying trap energy levels and (Right) varying capture cross-sections. The capabilities of the reported measurement setup is depicted as the grey box.

For wide bandgap semiconductors DLTS is incapable of profiling deeper traps and an alternative excitation source is required. Steady-state photocapacitance and deep-level optical spectroscopy are two methods for measuring deeper levels using optical excitation and much of the same equipment used for DLTS. In each of these methods a controllable monochromatic source is pulsed, resulting in the excitation of trapped charge inside the depletion region of a device with $E_c - E_T$ or $E_T - E_V$ smaller than the energy of light used. Just as with DLTS, the emission of trapped charges can be measured with fast capacitance meters and results analyzed for active trap energy levels and their respective concentration. Ideally, the sample is fabricated with a transparent but conducting contact to let uniform illumination of the depletion region [93]; however, shining light at an oblique angle to the sample surface has been shown to be effective [94]. Chantre et al. first described three methods for optically profiling deep traps in semiconductors which they referred to as electrical DLOS, thermal DLOS or optical DLOS. This work relies on a mixture of thermal and electrical DLOS methods which are described below.

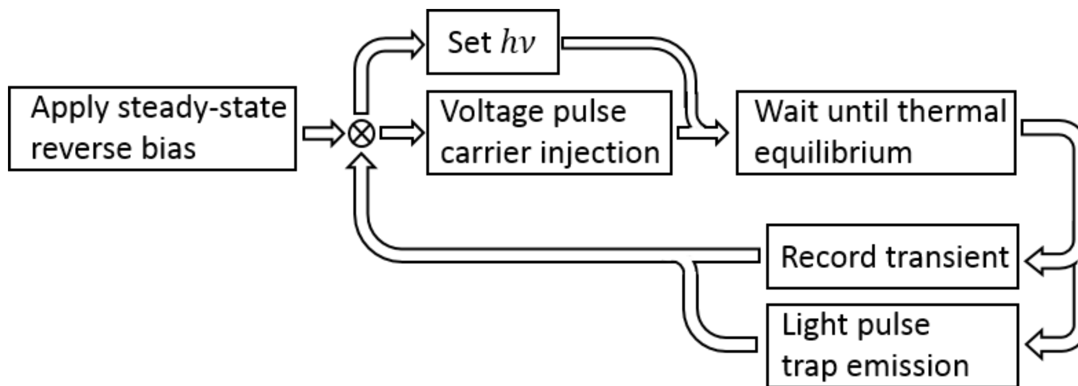

Figure 26. DLOS/SSPC process flow for measuring a single trap emission transient.

Figure 26 shows the typical process loop for measuring a single transient caused by the exposure of light ($h\nu$). First, the sample is held in reverse bias which extends the depletion region to the desired profiling depth throughout the entirety of the measurement. Next, just as with DLTS measurements, deep traps are filled with a carrier injection pulse (forward bias pulse). This brings the sample into an equilibrium so

that resulting transients can be considered as the result of all defects locating within the forbidden region. Additionally, while the shutter is closed, the monochromator is set to output the desired wavelength. If the sample is immediately exposed to light after the carrier injection pulse is completed, the collected transient data will be dominated by the response of shallow traps. Thus, the sample is left in the dark until the capture/emission process of shallow traps has equilibrated. Next, a computer controlled shutter is open while the capacitance transient is recorded for a set length of time. Finally, the shutter is closed and the process is repeated but with the monochromator set to another wavelength. Data reported in this work utilized a Xe-Hg lamp coupled into a 0.3m monochromator scanned from 1377 to 344nm.

Processing the recorded transient data is similar to what is required for DLTS measurements; however, the emission rate from deep traps is dependent on the photon flux (Φ) and optical cross-section (σ_n) (considered the probability of absorption). For and n-type semiconductor the emission rate is:

$$e_n = \Phi(hv)\sigma_n(hv) \tag{62}$$

The key to SSPC and DLOS measurements is in the plotting and fitting of the optical cross-section as it relates to the light energy impinging on the sample. In order to do this an equation relating to the capacitance transient is required. Because trapped charges are emitting from the forbidden region into either the valence or conduction band, the depletion width will vary and thus the measured capacitance, just as with DLTS measurements. The density of trapped charges as $t \to 0$ is N_T and at $t \to \infty$ it becomes [93]:

$$n_T(\infty) = N_T \frac{\sigma_p}{\sigma_n + \sigma_P} \tag{63}$$

Next we can use the ratio of initial and steady-state capacitance during a transient to find the capacitance dependence on total trap density:

$$\frac{C(0) - C(\infty)}{C(\infty)} = \frac{n_T(0) - n_T(\infty)}{2N_D} = \frac{N_T}{2N_D}\left[1 - \frac{\sigma_p}{\sigma_n + \sigma_P}\right] \tag{64}$$

If we can assume that $n_T(0) = N_T$ and $p_T(0) = 0$, then we can simplify Equation (64) with $\sigma_p \to 0$ so that:

$$N_T = 2N_D \frac{[C(0) - C(\infty)]}{C(\infty)} \tag{65}$$

Equation (65) creates a basis for measuring the density of traps in the forbidden region simply by measuring the change in capacitance initially after opening the shutter and after its reached steady-state under illumination, hence the name steady-state photocapacitance. Because some transients can last minutes or even hours, it is not practical to measure the whole transient and instead the data is analyzed with a multi-exponential fitting function and values are determined that way. In general, when observing the transient, an increase in capacitance is considered to be a signature of electrons being emitted while a decrease of capacitance indicates hole emission into the forbidden region. The energy of light which causes an onset of the increased N_T is related to the traps deep level energy with reference to the conduction or valence band for electron or hole emission respectively.

Ideally, SSPC could be used to find both the concentration and the energy depth of the trap; however, it has been shown [93, 95] that the rate of N_T change can, in addition to the trap depth, depend on the Franck-Condon relaxation energy (d_{FC}), effective phonon energy ($\hbar\overline{w}$), and temperature. Thus, to understand the actual origin of emitted charge, the dependence of the optical cross-section with applied wavelength needs to be examined and fit with the most appropriate models. The optical cross-section is related to the initial change in capacitance transient through the following.

$$\sigma_n = \frac{1}{\Phi(hv)[C(0) - C(\infty)]} \frac{dC}{dt}\bigg|_{t=0} \tag{66}$$

The optical flux ($\Phi(hv)$) is a pre-calibrated value dependent on the optical components and light source in the measurement setup. However, optical transmission into the sample can't be fully determined due to unintended absorption or reflection at the surface and as such the optical cross-section is typically shown in arbitrary units. As stated previously, with the graph of optical cross-section, the data can be fit using one of four popular fitting formulas to extract E_T and d_{FC}.

The Lucovsky equation shown below is derived assuming that $d_{FC} = 0$ so that there will be a sharp increase of the calculated optical cross-section starting when the photon energy matches that of the deep trap energy. Here, the potential well which is assumed to be a delta-function whose depth is the binding energy is also assumed to have no interactions with other wells (no long range effects) [69]. Finally, although the final derived form has a dependence on the index of refraction, effective field ratio, and electron mass, these terms are bundled and used as a single fitting value (A) so the L-M fitting algorithm requires only two input parameters. This is done because the optical cross-section, as stated previously, is not exactly determined and only the form is fit to.

$$\sigma_n(hv) = A \cdot \frac{E_i^{1/2}(hv - E_i)^{3/2}}{(hv)^3} \tag{67}$$

If the form of the experimental optical cross-section data cannot be explained by the Lucovsky model it is possible that the emitted carrier does not transition at a band minimum and may settle through phonon emission to a lower atomic configuration [96]. This would manifest itself in the experimental SSPC data as an onset at a value shifted by the Franck-Condon energy (d_{FC}). Chantre et al. created a model which assumes the optical cross-section is dependent on an average effective mass which accounts for perturbation from both conduction and valence band states, the thermal activation energy and d_{FC}. According to [93], additional assumptions can be made so that the minimized equation for σ_n becomes:

$$\sigma_n(hv) = A \cdot \frac{1}{\left(\frac{hv}{E_o}\right)\sqrt{\frac{4k_bTd_{FC}}{E_o^2}}} \int_1^\infty \frac{\sqrt{x-1}}{(x-1+m)^2}\, e^{-\frac{\left(\frac{hv}{E_o}-x\right)^2}{\left(\frac{4k_bTd_{FC}}{E_o^2}\right)}} dx \tag{68}$$

Two additional models [95, 97] exist which take the similar graphical form of Equation (68) and predict a larger d_{FC}; however, they are not used within this work. For brevity, the equations are shown below for the Passler and Mooney-Northrop-Morgan-Grimmeiss models respectively.

$$\sigma_n(h\nu) = A \cdot \frac{1}{h\nu\sqrt{2\pi d_{FC}\,\varepsilon \cdot \coth(\varepsilon/2k_bT)}} \int_0^\infty \frac{E_k^{3/2}}{(E_k + E_T)^2} e^{-\frac{(h\nu - E_T - d_{FC} - E_k)^2}{2d_{FC}\,\varepsilon \cdot \coth(\varepsilon/2k_bT)}} dE_k \quad (69)$$

$$\sigma_n(h\nu) = A \cdot \frac{\sigma_E^{3/2}}{(h\nu)^3} \int_0^\infty x^{3/2} e^{-\frac{\left(x - \frac{h\nu - E^0}{\sigma_E}\right)^2}{2}} dx \quad (70)$$

2.3.5.7 Deep Levels in GaN Associated with Carbon

Below in Figure 27, is a histogram of the observed GaN traps from 341 publications. Here, the characteristic energy levels of both (red) electron and (blue) hole traps are reported along with an arrow along the y-axis indicating trap levels reported in Section 3. These trap levels are reported on GaN layers with different structures, grown by different methods, exposed to different stresses, and measured by different means; however, the types of defects measured can be grouped into four categories including native defects, impurities, extended defects, and surface defects [98].

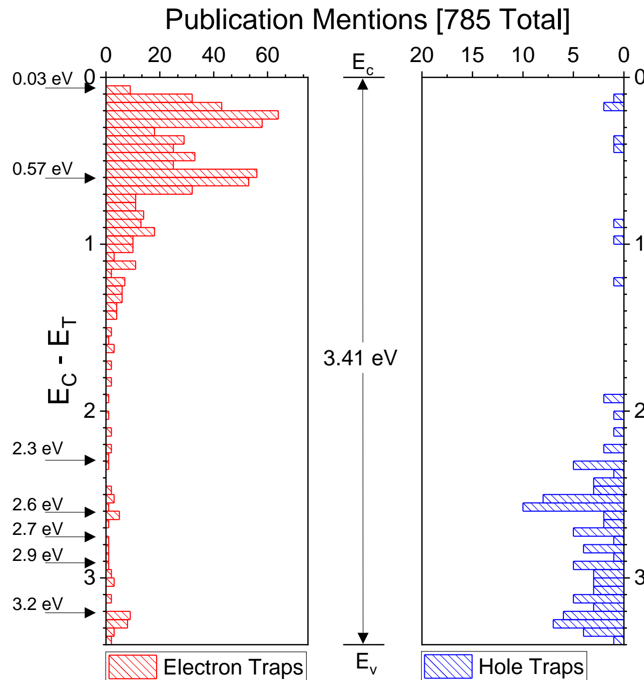

Figure 27. Histogram of reported (red) electron and (blue) hole traps in GaN. The levels observed from work presented in Section 3 are marked with an arrow and the extracted energy level

Of the deep levels associated with impurities in GaN, carbon has been the most widely investigated due to its ability to create fully compensated layers either intentionally or not. In MOCVD-grown GaN layers, the carbon concentration can be effectively controlled by tailoring the growth parameters such as pressure, temperature, III/V ratio, and growth rate. Layers where the carbon concentration is controlled can effectively be used to vary the resistivity, reduce lateral and vertical buffer leakage in GaN HEMTs, increase the breakdown voltage, and suppress short-channel transistors effects. However, these induced deep levels have been linked with spurious device behavior including current collapse and RF degradation of high frequency performance [98-100].

Carbon has been shown to induce two deep levels due to its amphoteric behavior within a GaN lattice. The deep level associated with the nitrogen substitutional (C_N) is expected to behave as shallow acceptor while the interstitial incorporation (C_i) and gallium substitutional (C_{Ga}) is expected to behave as a donor [82, 98]. It is the nitrogen interstitial incorporation that is expected to act as the compensating trap in n-type GaN layers and in high enough concentrations has been shown to generate p-type conductivity [101]. Armstrong et al., through DLTS and DLOS measurement of MBE-grown GaN layers, has observed carbon concentration affecting the trap density of levels located at E_C – 0.11, 2.05, 3.0 and 3.28 eV [96]. In MOCVD samples grown under atmospheric and low pressure they have observed levels located at E_C – 1.35 and 3.28 eV which they are considering to be associated with carbon [82]. Of the obsereved traps from these two reports, it is considered that the E_C – 3.28 eV trap is the cause of compensation in GaN films and thus related to the nitrogen substitutional, C_N, form of carbon incorporation.

3 Research

3.1 Characterization of Inhomogeneous Ni/GaN Schottky Diode with a Modified Log-Normal Distribution of Barrier Heights

3.1.1 Abstract

The current vs. voltage (I-V) characteristics of a Ni/GaN Schottky diode are measured from 50 to 400K and the temperature dependence of the extracted barrier heights and ideality factors is described as a consequence of lateral inhomogeneity at the metal-semiconductor (M-S) interface. It is shown that by invoking a modified log-normal distribution of barrier heights at the MS interface, the extracted barrier height temperature dependence can be well explained. Further, it is shown that this approach can describe the voltage dependence of the lateral barrier distribution. By calculating the distribution between zero-bias and 0.6 V, it is shown that the distribution begins to converge on a single value of 0.77 eV. This value is in good agreement with the flat-band barrier height of 0.77±0.02 eV extracted from capacitance-voltage measurements on the same device. The same procedure is used to describe the parallel conduction path apparent at low temperatures, revealing its behavior is indicative of an additional Schottky region with an increased density of low barriers which are more heavily perturbed by external bias. Finally, the model is successfully applied to previously published work on various Schottky diodes structures.

3.1.2 Introduction

Gallium nitride (GaN) has proven to be an excellent material to implement power semiconductor devices. This is largely because of its breakdown field strength, high-temperature performance, and the availability of conductive substrates so that vertical device topologies are possible. Fabricated Schottky barrier diodes (SBDs) can act as both a high frequency and low turn-on voltage rectifying device and as a means of quickly evaluating the semiconductor material quality. On GaN, however, the current-voltage (I-V) characteristics frequently deviate from ideal thermionic emission over a single barrier. These inconsistencies are typically attributed to a lateral variation in the barrier at the interface between the metal and semiconductor [102-106]. Carrier transport across this non-ideal interface has been analyzed with various models [77, 107]; however, the continuous distribution model first discussed by Song et al. [47] and formalized by Werner and Güttler [69] presents a method by which the interface inhomogeneity can be characterized by a probabilistic distribution without first having to make assumptions about the source of inhomogeneity. Ideally, if the cause of non-ideality can be accurately represented through these models, work can be done to link specific material growth and device fabrication methods to spurious electrical device behavior.

By first assuming that the fabrication of a real Schottky diode will have some lateral variation in the interfacial barrier height, and that this variation takes the form of a Gaussian distribution, Werner and Güttler present a straightforward method to determine the mean and standard deviation of said distribution. Then, assuming a bias dependence of the effective barrier height distribution, they show that voltage dependence of the mean and standard deviation induce experimentally extracted values of ideality factor larger than unity. The technique was developed further, using the same analysis method to describe interfaces with multiple non-interacting Gaussian distributions [79, 108] and then again using iterative solving techniques to describe interfaces with interacting Gaussian peaks [74]. Although these methods tend to provide agreement with experimental data, application to the sample presented in this work yielded results which did not fit the data or implied spurious behavior according to the underlying assumptions. It was found that instead of using a single or multi-Gaussian distribution model, a single

modified log-normal distribution could be used. Additionally, work was done to understand the effect that voltage has on the barrier distribution, ultimately revealing that the modified log-normal distribution can be used to describe the interface as the diode approaches flat-band conditions. This process is then applied to the typically ignored low current parallel conduction path observed at low temperatures, revealing that it can be explained as stemming from a region of the M-S interface with a lower barrier and higher voltage dependence. Finally, the model is successfully applied to previously published data on Pd_2Si/p-Si [79], Au/p-GaTe [109] and Au/n-GaAs [110] Schottky diodes where a multi-Gaussian distribution model was utilized.

3.1.3 Inhomogeneous Schottky Model

The current (I) induced across a Schottky barrier diode (SBD) according to thermionic emission theory for an applied voltage (V_A) is given by the following equation [111]:

$$I(V_A) = AA^*T^2 \exp\left(\frac{-q\phi_{b0}}{k_BT}\right)\left[\exp\left(\frac{q(V_A - IR_s)}{\eta k_BT}\right) - 1\right] \quad (71)$$

Where A is the metal-semiconductor contact area; A^* is the Richardson constant of GaN ($26.4\ A/cm^2K^2$), T is the temperature, ϕ_{b0} is the M-S interface barrier height at zero-bias, η is the ideality factor, and R_s is the series resistance. Werner and Güttler explain that the interface is likely not homogenous and perturbation due to surface roughness, metallic diffusion, and even dopant atom concentration abnormalities can create lateral variation in the barrier height [69]. The resulting I-V characteristics is thus a superposition of thermionic emission currents across an interface characterized by a distribution of barrier heights. Additionally, it is possible that the distribution itself is voltage dependent. The current-voltage relationship can be rewritten to include this distribution such that:

$$I(V_A) = AA^*T^2\left[\exp\left(\frac{q(V_A - IR_s)}{k_BT}\right) - 1\right]\int_{-\infty}^{\infty} P(\phi_b^V)\exp\left(\frac{-q\phi_b^V}{k_BT}\right)d\phi_b^V \quad (72)$$

Where $P(\phi_b^V)$ represents the voltage-dependent probability distribution of barrier heights apparent at the M-S interface and must satisfy,

$$\int_{-\infty}^{\infty} P(\phi_b^V)d\phi_b^V = 1 \quad (73)$$

A consequence of a laterally varying barrier height is both an additional temperature and voltage dependence of the I-V characteristics [69]. Werner and Güttler [69] show that if thermionic emission over these region is dominant, the resulting I-V characteristics will be indicative of a homogeneous barrier with this additional temperature and voltage dependence according to:

$$I(V_A) = AA^*T^2 \exp\left(\frac{-q\phi_b^{eff}(V,T)}{k_BT}\right)\left[\exp\left(\frac{q(V_A - IR_s)}{k_BT}\right) - 1\right] \quad (74)$$

Here, $\phi_b^{eff}(V,T)$ is the effective barrier height. For SBD's suffering from lateral inhomogeneity, values of zero-bias barrier height extracted from I-V measurements are considered equivalent to $\phi_b^{eff}(0,T)$. An expression of the effective barrier height dependence on the lateral barrier distribution can be found by setting Equation (72) equal to (74).

$$\phi_b^{eff}(V,T) = -\frac{k_B T}{q} \ln\left(\int_{-\infty}^{\infty} P(\phi_b^V) exp\left(\frac{-q\phi_b^V}{k_B T}\right) d\phi_b^V\right) \quad (75)$$

Typically, the ideality factor is used to indicate that the observed I-V characteristics deviate from pure thermionic emission. However, in the context of an M-S interface with an inhomogeneous barrier, the ideality factor quantifies the voltage dependence of the distribution. Again, assuming thermionic emission is the dominant current conduction mechanism and that the ideality factor itself is not voltage dependent, Werner and Güttler showed that the effective barrier height voltage dependence at a fixed temperature can be found by setting Equation (71) equal to Equation (74). This results in the following,

$$\phi_b^{eff}(V,T) = \left(1 - \frac{1}{\eta(T)}\right) \cdot V + \phi_{b0}(T) \quad (76)$$

Here $\phi_{b0}(T)$ and $\eta(T)$ are the values of zero-bias effective barrier height and ideality factor at the measurement temperature, T, from experimental I-V measurements, respectively. We can see that for SBD's with an ideality factor of 1, the effective barrier is voltage independent, otherwise it will increase linearly with the quantity $1 - 1/\eta(T)$. From Equations (75) and (76), work can be done to relate a proposed probability distribution and its voltage dependence to experimentally extracted values of effective barrier height and ideality factor, respectively.

Presuming the interface can be described by a single Gaussian distribution, Werner and Güttler show that the experimentally extracted values of effective barrier height and ideality factor from a range of temperatures can be plotted according to Equations (14) and (17) in [69], respectively. This results in linear trends which can be fit to determine the Gaussian mean and standard deviation along with the voltage dependence of these parameters. Using the same process, Chand and Kumar [79, 108] showed that in cases where the effective barrier height and ideality factor plots yielded multiple regions of linearity, the lateral inhomogeneity can be described by multiple Gaussian distributions. However, for this to be true only one distribution should be active at each temperature range (non-overlapping distributions) and that data analysis will yield increasingly larger Gaussian means at higher temperatures. If experimental results do not follow this, Jiang et al. [74] showed that the integral in Equation (75) could be re-evaluated with a summation of Gaussian distributions and experimental data could be fit using sets of Gaussian mean, standard deviation and weighting factors as input parameters in an iterative solver.

3.1.4 Experimental Procedure

In this work we report experimental results of Schottky diodes fabricated on an n-type GaN film grown by MOCVD on sapphire. The film thickness is estimated at 1 µm and room-temperature capacitance vs. voltage measurements indicate a free carrier concentration of $3 \times 10^{16}\ cm^{-3}$. The sample was first sonicated in acetone then isopropyl alcohol for 10 minutes and rinsed in deionized water. Then a bath of aqua regia was used to remove metal ions from the surface of the sample followed by a 49% HF bath to

remove any surface oxide layer, each sitting at room temperature for 10 minutes. Again the sample was rinsed in deionized water followed by a nitrogen drying step. Next, ohmic contact regions were defined via an optical lithography process, followed by a 1 min BOE dip to remove the native oxide layer. A Ti/Al/Ni/Ag (30/100/50/150 nm) metallization stack was deposited by E-beam and lift-off was performed in a solution of AZ400T photoresist stripper. The sample was annealed at 700 °C under a continuous flow of dry N_2 for 5 minutes to improve ohmic contact resistivity. Circular Schottky contact regions ranging in diameter from 73 to 250 µm were defined by optical lithography and a Ni/Ag (50/150 nm) stack was deposited by E-beam, yielding 128 diodes after lift-off. Barrier height and ideality factors were determined from room-temperature I-V measurements of each diode. The mean and standard deviation of extracted barrier heights across the sample was 0.74 and 0.04 eV, respectively, whereas the extracted values of ideality factor were 1.09 and 0.12 respectively. Next, the sample was mounted to a temperature controlled stage in an MMR microprobe station with a CTI Model 22 cryostat where measurements were performed between 50 and 400K in steps of 4 K on a characteristic 190 µm diameter diode. After temperature stabilized to within ±100 mK of the target temperature for >30 s, the I-V characteristics of the reported device was measured by a Keithley 2400. C-V characteristics were recorded over the same temperature range using a DC sweep from 0 to -5 V and a 1MHz probing signal from a SULA fast capacitance meter.

3.1.5 Results and Discussion

The results of the I-V measurements taken at temperatures between 50 and 400 K are shown below in Figure 28. As Equation (71) predicts, when displayed on a semi-log plot each I-V measurement has a region of linearity characteristic of thermionic emission over a barrier followed by a roll-over at higher currents (>10 µA) due to series resistance. Additionally, measurements made at low temperatures (<256 K) exhibit two regions of linearity and roll-over indicative of a parallel conduction path. It is assumed this additional region stems from a Schottky interface with characteristics that don't allow it to dominate across the full temperature and voltage range, thus it is labeled the parallel Schottky (PS) region. One possible source of this phenomenon is a region with a voltage dependent barrier height which causes pinch off resulting in higher barrier regions to dominate as bias is increased. Later analysis will show that extracted values of ideality factor support this argument. In light of this additional region, Equation (71) is modified to include the current contribution from parallel SBD's at the same M-S interface.

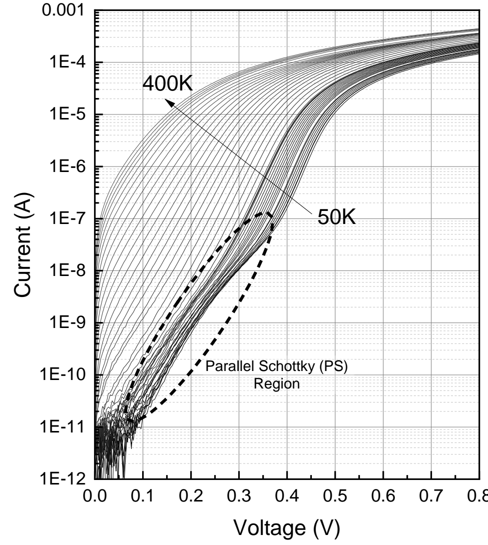

Figure 28. Measured forward bias current-voltage characteristics of the Ni/GaN Schottky diode from 50 to 400 K. The portion of the I-V characteristic measurement dominated by the low temperature parallel conduction is labeled 'Parallel Schottky (PS) Region'. (Note: I-V characteristics shown in increments of 8 K). [Single Column Fitting Image]

$$I(V_A) = AA^*T^2 \sum_{i=1}^{n} \exp\left(\frac{-q\phi_{b_i}^{eff}(0,T)}{kT}\right)\left[\exp\left(\frac{q(V_A - IR_{s_i})}{\eta_i k_B T}\right) - 1\right] \quad (77)$$

Here, the variables $\phi_{b_i}^{eff}(0,T)$, η_i, and R_{s_i} are the zero-bias effective barrier height, ideality factor and series resistance of the i-th SBD respectively. I-V data at each temperature is fit using a damped least-squares fitting procedure based on Equation (77), where zero-bias effective barrier height, ideality factor and series resistance are passed as input parameters. In the case of the reported sample, n is 2 for I-V measurements from 50 to 256 K, otherwise only one set of parameters was required and n is 1. Fitting the full current vs. voltage range produced values of $R^2 > 0.999$ for I-V measurements at each temperature. The zero-bias effective barrier height and ideality factor values which provide the best fit are plotted versus temperature in Figure 29(A) and (B), respectively.

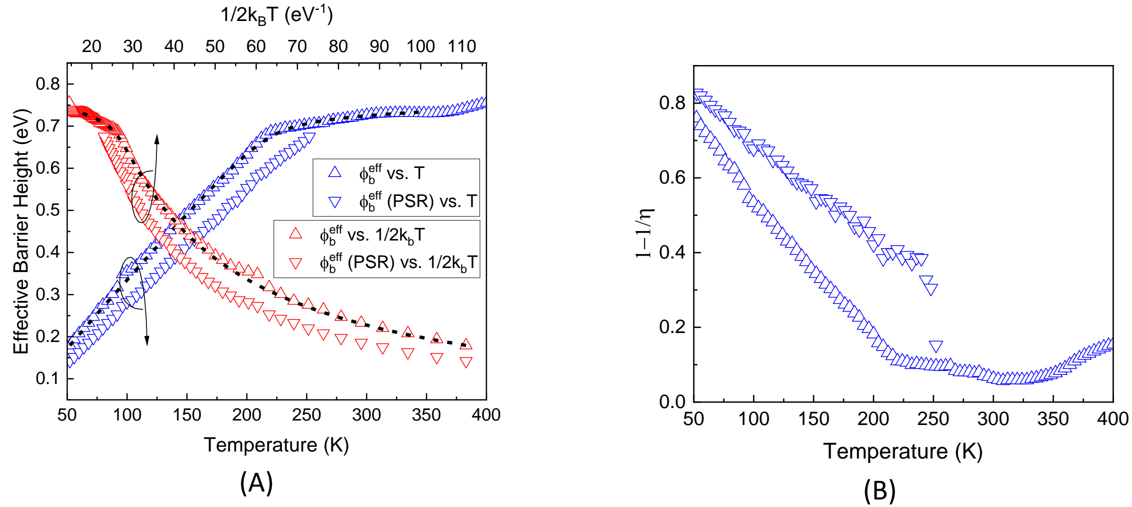

Figure 29. (A) Values for the effective barrier height extracted both from inside (▽) and outside (△) the PS region are plotted versus temperature and $1/2k_BT$. The dashed line represents the best fit curves utilizing the modified log-normal distribution. (B) The extracted values of ideality factor at each temperature are plotted as $1 - 1/\eta(T)$ according to Equation (76).

In both Figure 29 (A) and (B), parameters extracted from the PS region of the I-V curve are denoted by a downward triangle (▽) while all others are represented by an upward triangle (△). Extracted values of the effective barrier height were also plotted according to Werner and Güttler's single Gaussian distribution model, Equation (14) in [69], shown as the red data points in Figure 29(A). Reviewing the I-V curves, it is likely that at temperatures >350 K, extracted values of effective barrier height and ideality factor deviate from the actual value due to the dominance of series resistance. For this reason, values of effective barrier height and ideality factor extracted from I-V characteristics measure above 350 K were not used in subsequent fitting.

As discussed previously, if the interface is dominated by a single Gaussian distribution, plotting the effective barrier height vs. $(2k_BT)^{-1}$ would linearize the data across the full temperature range; however, this is clearly not the case. Because this deviation implies the interface cannot be represented by a single Gaussian distribution, the effective barrier height vs. $(2k_BT)^{-1}$ data was fit with multiple lines. Fitting the barriers extracted from all but the PS region indicated the existence of three Gaussian distributions according to Chand and Kumar's method [79, 108]. However, calculated values of each distribution's mean did not increase monotonically with temperature and each of the distributions implied significant overlap thus violating the underlying assumptions. Finally, an attempt was made to fit the extracted barrier temperature dependence by iteratively varying the mean, standard deviation and weight of two Gaussian distributions following work done by Jiang et al. [74]. Good agreement was found; however, the results indicated that one of the distributions was characterized by a mean of 1.4 eV, a value larger than the theoretically predicted barrier height at a Ni/GaN interface (~1.2 eV).

Broadly speaking, an arbitrary distribution of barrier heights could be used to fit the effective barrier height data according to Equation (75); however, the dominance of lower barrier regions in the I-V relationship effectively hides contributions from higher barrier regions at the M-S interface. Unless inhomogeneity is minimal or measurements are taken at high enough temperature, values of effective barrier height indicative of the higher barrier regions will not be observed. Thus, the density of the unobserved barrier heights become imperceptible and a single optimal form of the distribution cannot be found. By constraining $P(\phi_b^V)$ with a defined probability density function, the form of the distribution

outside of the observed range will be defined by the observed data and an optimal solution can be reached. In this work it was found that the range of effective barrier heights could be appropriately fit with a single modified log-normal distribution defined by Equation (78) below.

$$P(\phi_b^V) = \frac{1}{C(-\phi_b^V + A)\sqrt{2\pi}} \exp\left(-\frac{\left[ln(-\phi_b^V + A) - B\right]^2}{2C^2}\right) \quad (78)$$

Here A, B, and C are used as input parameters to an iterative fitting routine that minimizes the error between generated effective barrier heights according to Equation (75) and the experimentally determined values. In addition to these parameters, the lower limit of integration (ϕ_{LL}) was used as an input to the fitting procedure while ensuring that Equation (73) was met by scaling the resulting distribution on each iteration. This effectively estimates the form of the distribution at temperatures below what was measured; however, instead of requiring the distribution to continue infinitely, even for negative values of effective barrier height, the distribution is weighted to zero below ϕ_{LL}.

The fitting was first applied to effective barrier heights extracted from all but the PS region, represented with $\triangle$ in Figure 29(A), and the result is overlaid, shown as dashed lines. The good agreement with the experimental data indicates that a single modified log-normal distribution can be used to describe the inhomogeneous nature of the Ni/GaN SBD. The resultant fitting parameters ϕ_{LL}, A, B, and C used to fit the effective barrier heights extracted from all but the PS region are $11.5\ meV$, 0.94, -1.76 and 0.20 respectively.

With an appropriate probability density function established, the voltage dependence of the distribution can be examined. Continuing with the parameters extracted from all but the PS region, effective barrier height vs. temperature plots are generated at incremental steps in voltage using Equation (76) and extracted values of ideality factor. In Figure 30(A), values of effective barrier height are calculated in steps of 100 mV from 0 to 600 mV, shown as scatter plots. Applying the modified log-normal fitting procedure at each bias step resulted in excellent agreement with the temperature dependent effective barrier height values (solid line). The resulting distributions of best fit are shown in Figure 30(B) for each bias step.

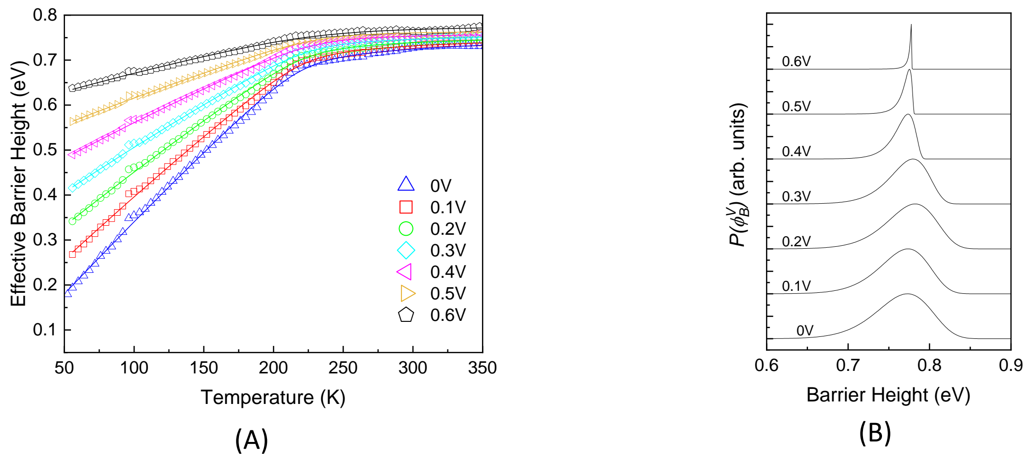

Figure 30. (A) The effective barrier height temperature dependence generated from extracted values of zero-bias effective barrier height and ideality factor according to Equation (76) in steps of 100 mV from 0 to 600 mV (scatter). Fitting each set of data with the modified log-normal distribution resulted in the solid lines of best fit. (B) Normalized best fit probability function curves from the same voltage range.

Referring to the calculated set of effective barrier heights in Figure 30(A), the data suggests that as the forward voltage is increased, regions at the M-S interface characteristic of lower effective barrier height (<0.65 eV) are strongly perturbed upward to higher values while those indicative of a higher effective barrier height are only slight perturbed as voltage is increased. Physically, this effect is consistent with the model proposed by Tung [77] where pinning at the M-S interface can induce a voltage-dependent conduction band saddle-point within the semiconductor. This saddle-point can become more strongly affected by voltage when the associated 'patch' is small and/or when strong pinning is present.

The resulting normalized best fit barrier distribution at each voltage step is shown in Figure 30(B). In the plot we can see that as the voltage is increased, the distribution tails on both sides of the peak move toward each other and the form begins to converge to a prominent barrier value. On the low side of the distribution this is expected, assuming barrier 'pinch-off' is occurring; however, this cannot explain the behavior of the distribution tail on the high side. As mentioned earlier, the temperature dependence of the effective barrier height is influenced more heavily by lower regions of barrier height according to Equation (75). As the effective barrier height is generated at higher voltages, the trend begins to flatten out and the effect that lower barrier regions typically have is minimized. Thus, as the voltage is increased and the range of effective barrier heights begins to converge, the fitting procedure can more accurately represent the high side of the distribution. Comparing the barrier distribution at 600 mV with flat-band barrier heights extracted from C-V measurements, it becomes apparent that the value at which the probability distribution converges is the flat-band barrier height.

Capacitance vs. voltage measurements were taken from 50-400 K in steps of 4 K from zero bias to -5 V. Below in Figure 31(A), the measured capacitance versus voltage characteristics have been replotted to show the linear A^2/C^2 trends which are used to extract flat-band barrier height from the extrapolated value of the x-intercept according to Equation (79).

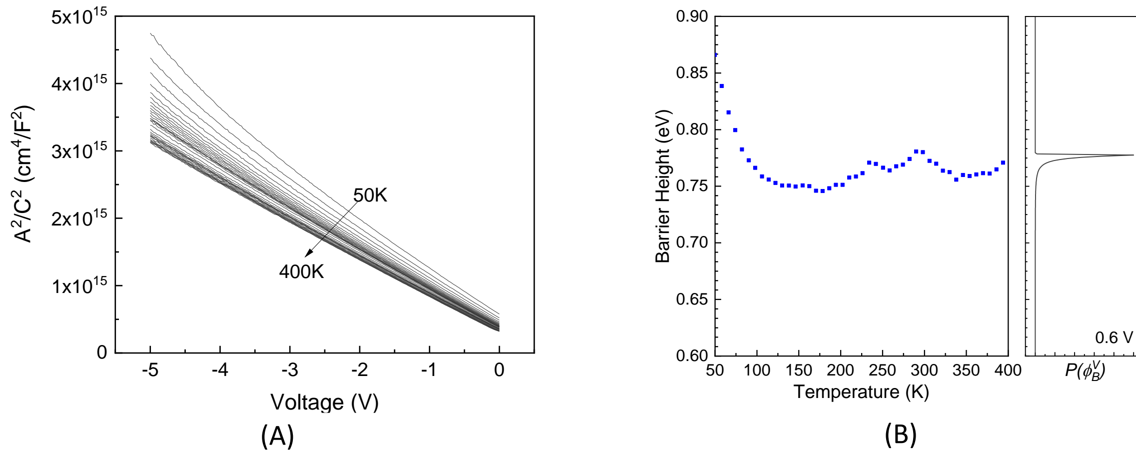

Figure 31. The (A) A^2/C^2 data calculated from C-V measurements and (B) the values of flat-band barrier height calculated at each temperature. The previously calculated barrier distribution at 0.6 V from I-V measurements is compared.

$$\phi_b^{CV} = V_{FB} + \frac{k_B\,T}{q}\ln(N_C/N_D) + k_B T/q \qquad (79)$$

$$N_D = \frac{2}{q\varepsilon_r\varepsilon_0 \frac{d(A^2/C^2)}{dV}} \qquad (80)$$

Here, V_{FB} is the voltage required to induce flatband conditions and is equal to the extrapolated value of the x-intercept on the A^2/C^2 plot. N_C is the temperature dependent conduction band density of states calculated from $4.3E14 \cdot T^{3/2}$, and the effective free carrier concentration , N_D, is calculated from the slope of the A^2/C^2 plot according to Equation (80). The value ε_r is the dielectric constant of GaN (8.9) and ε_0 is the permittivity in vacuum. Flat-band barrier heights calculated from the extrapolated values of V_{FB} are shown in Figure 31(B) versus temperature. On the right side of the graph, the barrier distribution calculated for effective barrier heights at 0.6 V is plotted for comparison. The effective barrier distribution peak occurs at 0.77 eV and the extracted values of flat-band barrier height are 0.77±0.02 eV across the full temperature range. Good agreement between these two plots shows that the value at which the barrier distribution begins to converge is in fact the flat-band barrier height.

To understand the behavior of the PS region, the effective barrier heights were analyzed using the process outlined above. However, subsequent calculations of the effective barriers at increased voltages according to Equation (76) had interesting effects. Figure 32 shows the evolution of the effective barriers extracted from the PS region (▼) as compared to those extracted from I-V characteristics outside of this region (△).

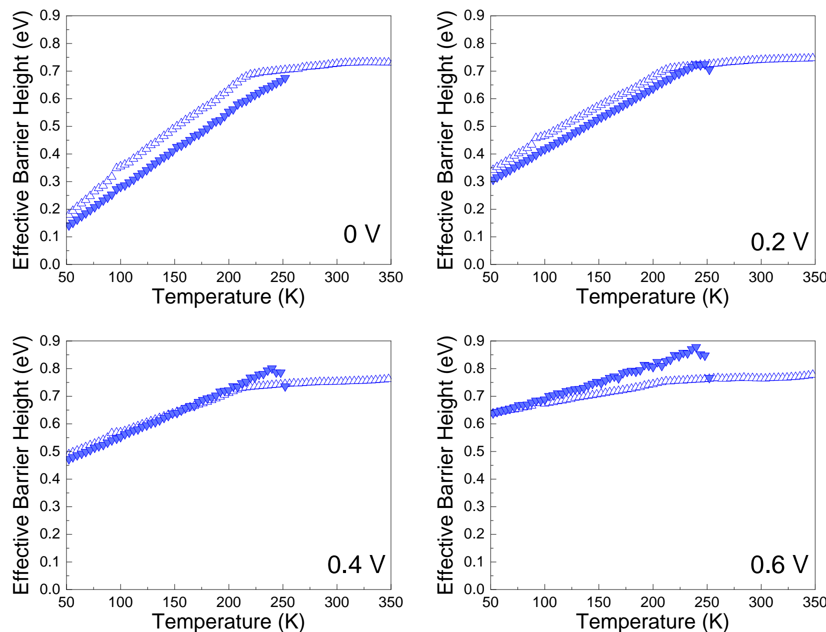

Figure 32. Effective barrier heights extracted from within (▼) and outside (△) the PS region of the I-V measurements calculated at 0, 0.2, 0.4, and 0.6 V according to Equation (76). [Double Column Fitting Images]

The zero-bias barriers extracted from the PS region (▼) increase with temperature until ~250 K at which point the parallel conduction is no longer detectable in the I-V characteristics. Because the lower barrier region will dominate the I-V characteristics, it's theorized that the PS region disappears because the associated barrier height is the same as or larger than other areas at the M-S interface. When voltage is increased, as shown in the figure above, the effective barriers extracted from the PS region (▼) increases and as the trend moves upward, the point at which it crosses those extracted from outside the PS region (△) occurs at increasingly lower temperatures. Accordingly, this implies that the PS region within each I-V measurement should transition at lower voltages as the temperature is increased. Reviewing the I-V

characteristics in Figure 28, it can be seen that this is indeed the case. Similar to Tung's model [77], physically this effect could be caused by multiple patches at the M-S interface, each with characteristics that induce different voltage and temperature dependencies including size, pinning level and neighboring barrier properties.

3.1.6 Evaluation of Previously Published Data

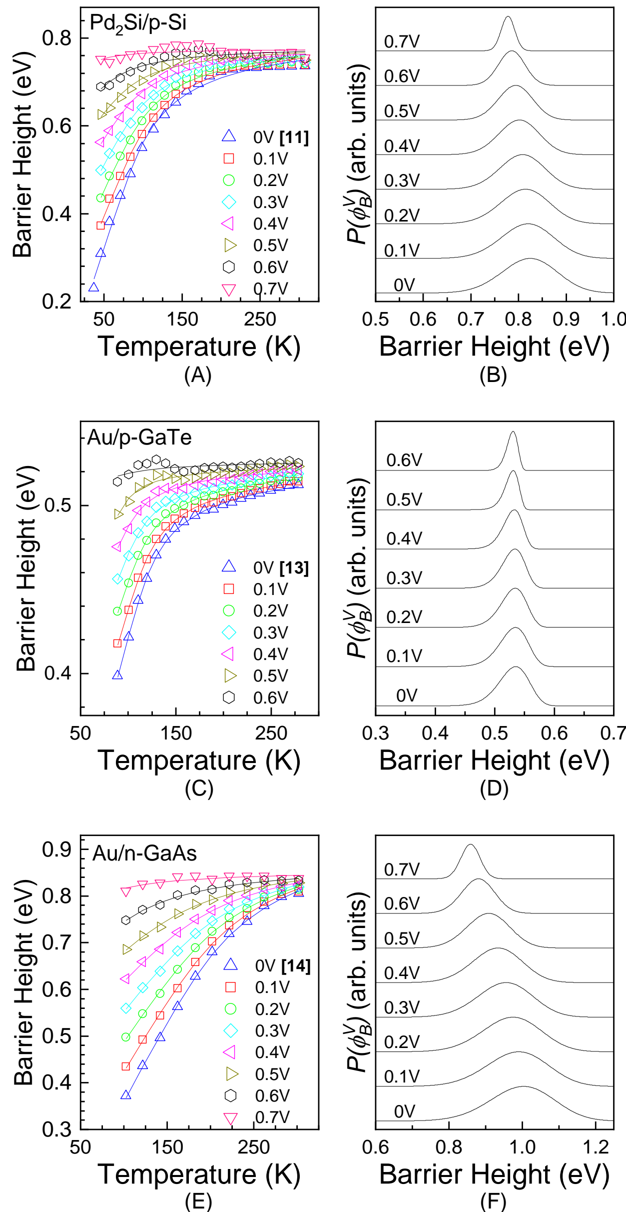

Figure 33. The modified log-normal model is applied to previously published data on (A) Pd_2Si/p-Si [79], (C) Au/p-GaTe [109], and (E) Au/n-GaAs [110] Schottky diodes (△). The scatter plot represents the temperature dependence of effective barrier heights calculated at increased forward bias. Fitting is shown as a solid line. Modified log-normal distributions calculated at each voltage are shown for the (B) Pd_2Si/p-Si, (D) Au/p-GaTe, and (F) Au/n-GaAs Schottky diodes.

To relay the applicability of the modified log-normal approach for describing inhomogeneity in various Schottky diodes, previously published zero-bias effective barrier height and ideality factor data was evaluated using the procedure outlined above. In the selected published works, it was shown that the data is well described with a multi-Gaussian model; however, reanalysis with the modified log-normal approach reveals that a single distribution can also explain the non-ideal I-V behavior. In Figure 33 (A), (C), and (E) the blue scatter (△) represents zero-bias effective barrier heights extracted from I-V measurements on Pd_2Si/p-Si [79], Au/p-GaTe [109] and Au/n-GaAs [110] Schottky diodes, respectively. Fitting these values with the modified log-normal distribution produces excellent agreement as shown by the blue line in each plot. The effective barrier height values at increased forward bias are calculated (scatter) according to Equation (76), utilizing ideality factor data taken from each published work. Again, fitting the resulting data with the modified log-normal distribution (line) results in excellent agreement at each bias step for the reported Schottky diode data. Finally, the barrier height distribution which provided the best fit at each bias step is visualized in Figure 33 (B), (D), and (F) for the Pd_2Si/p-Si, Au/p-GaTe and Au/n-GaAs Schottky diodes, respectively.

Each of the previously published works relied on a multi-Gaussian distribution to analyze extracted effective barrier height and ideality factor data implying that the inhomogeneity in each of the three devices could be caused by more than one physical mechanisms at the interface. In reality, acceptable fitting of the effective barrier height temperature dependence relies more heavily on the distribution, $P\left(\phi_b^V\right)$, at lower magnitudes according to Equation (75). Thus, it is possible that the usefulness of invoking a multi-Gaussian distributions comes from the ability to tailor the form of the distribution at lower magnitudes. With a single modified log-normal distribution, we show that the effective barrier height temperature dependence reported on Pd_2Si/p-Si [79], Au/p-GaTe [109] and Au/n-GaAs [110] Schottky diodes can accurately describe not only effective barrier height data at zero-bias but also at increasingly larger forward biases. Additionally, the model is further verified by the observation of distribution narrowing at increased bias which indicates that the Schottky diodes is approaching flat-band conditions.

3.1.7 Conclusion

In this work, we presented Ni/GaN Schottky diode I-V characteristics which could not be explained by the single Gaussian model proposed by Werner and Güttler [69] . Attempts to analyze the data with multi-Gaussian models proposed by Chand and Kumar [79, 108] or Jiang [74] yielded results which either violated underlying assumptions of the model or predicted impossibly large barrier height values for a Ni/GaN interface. To explain the temperature and voltage dependent effective barrier height behavior, a modified log-normal distribution is utilized and shows excellent agreement with experimental data. Next, it was found that subsequent calculations of the effective barrier height at increased voltages could be well explained using this distribution. Analysis of the probability distribution at these voltages revealed that the trend begins to converge on a prominent barrier height (0.77 eV) which agrees well with that extrapolated from C-V measurements under flat-band conditions (0.77±.02 eV). Next, examination of the barriers extracted from the PS region of the I-V measurements reveal its behavior is indicative of an additional Schottky region characterized by a lower zero-bias effective barrier and stronger voltage dependence compared to those extracted outside of this region. Finally, the model was successfully applied to previously published data on Pd_2Si/p-Si [79], Au/p-GaTe [109] and Au/n-GaAs [110] Schottky diodes.

3.2 Electrical Characterization of Ru Schottky Contacts on GaN Annealed in Air

3.2.1 Introduction

Gallium Nitride (GaN) has been examined with a great interest for its implementation in both optical and high power semiconductor devices. Some of the properties that make GaN such an interesting material include a large direct bandgap (3.41eV), low intrinsic carrier concentrations, high saturation-electron velocity, and high breakdown field strength. Schottky barriers have been used extensively to characterize both the material and interface properties of GaN using metals such as Ni [47, 112, 113] and Pt [114-116]. Ruthenium-based layers have been of interest for use as an ohmic contact to the p-type layer in optical devices due to its large work-function (>5.0eV), low sheet resistance and high transparency when annealed [117-120]. Additionally, its implementation as the Schottky contact to n-GaN has proven to yield high barrier, and low leakage current devices [121, 122] while further improvements to the electrical characteristics can be had by post-annealing [123, 124]. In addition to the electrical characteristic improvement, thin ruthenium layers have been shown to become more transparent after oxidation making Ru-based GaN Schottky diodes useful as ultraviolet photodetectors [123].

In this work, we report the electrical effects of annealing Ru Schottky electrodes on n-type GaN in normal laboratory air in an effort to improve Schottky diode electrical characteristics. Current versus voltage (IV) and deep-level transient spectroscopy (DLTS) measurements between 70 and 400 K in addition to capacitance versus voltage (CV) measurements at room temperature were performed, and the results are used to explain the inhomogeneous nature of as-deposited and annealed Ru Schottky contacts based on the model detailed in Section 3.1. Here we report the lowest leakage current for a Ru/GaN Schottky device, achieved by post-deposition annealing.

3.2.2 Experimental Procedure

Schottky diodes were fabricated on n-GaN grown on a sapphire substrate by metal organic chemical vapor deposition (MOCVD). The layer structure consists of a 1 μm unintentionally doped (UID) layer followed by a 1 μm active layer doped with silicon and to an effective free carrier concentration of $\sim 1.4 \cdot 10^{17}\ cm^{-3}$ from CV measurements. Prior to fabrication each sample was cleaned at room-temperature in Acetone, IPA, Aqua regia, and 49% HF, with each step performed for 10 minutes and then followed by thorough rinsing in deionized water. Next, the photolithographic processes was used to pattern top surface ohmic contact openings, and then the samples were dipped in 10:1 BOE, rinsed in deionized water, dried with nitrogen, and immediately placed in the E-beam chamber. Ohmic contacts consisting of Ti/Al (30nm/400nm) were deposited, patterned via lifted-off, and then annealed in forming gas at 600°C for 5 minutes. Next, following the same photolithography procedures, ruthenium Schottky contacts with a thickness of 10nm were deposited and patterned into circles with diameters varied between 200 and 450 μm. Samples were then annealed in normal laboratory air between 400°C and 600°C measured by a thermocouple for 5 minutes. Finally, contact pads of Ni/Ag (50nm/300nm) were deposited on both ohmic and Schottky contacts yielding 144 diodes. From room-temperature IV measurements on each sample, representative 400 μm diameter diodes were selected to perform IV and DLTS measurements between 70 and 400K with a Keithley 2400 and SULA fast capacitance meter, respectively. Temperature control and sample probing was achieved using a modified MMR cryogenic vacuum chamber. Additionally, capacitance-voltage measurements were taken using a HP4192A impedance analyzer at room temperature with a 1 MHz probing signal mixed with a DC voltage swept from zero-bias to -5 V. The extracted value of effective free carrier concentration for all four Ru/GaN samples is $1.4 \pm 0.2 \cdot 10^{17}\ cm^{-3}$.

3.2.3 Results and Discussion

IV measurements of a 400 µm diameter Schottky diode on each sample were first performed at room-temperature under both forward and reverse bias conditions. In Figure 34, the semi-logarithmic IV characteristics of the as-deposited, 400°C, 500°C, and 600°C diodes are shown. In an ideal Schottky diode, the IV relationship is governed by thermionic emission over a voltage-independent barrier and the current as a function of applied diode voltage (V_d) is [111]

$$I(V_A) = AA^*T^2 \exp\left(\frac{-q\phi_{b0}}{k_B T}\right)\left[\exp\left(\frac{q(V_A - IR_s)}{\eta k_B T}\right) - 1\right] \quad (81)$$

Here, A is the metal-semiconductor contact area, A^* is the Richardson constant of GaN (26.4 A/cm^2K^2 [125]), ϕ_{b_o} is the zero-bias barrier height, η is referred to as the ideality factor and R_S is the series resistance. For an ideal Schottky contact whose forward current is dominated only by thermionic emission, η is unity; however, values extracted from the forward bias IV characteristics of fabricated devices are typically larger.

Experimentally, values of zero-bias barrier height and ideality factor can be extracted from the forward IV characteristics according to Equation (81), but careful consideration must be given to the current or voltage range used as not to include series resistance effects. While methods for Schottky diode parameter extraction have been developed [65, 67, 68], it was found that accurate fitting to the reported experimental data could be performed by passing the zero-bias barrier height, ideality factor, and series resistance as input parameters to an iterative fitting procedure based on Equation (81) [Section 2.3.1.4]. By utilizing the Levenberg-Marquardt dampened least-squares iterative fitting algorithm, experimental data could be accurately represented with a coefficient of determination values (R^2) greater than 0.999 across the full voltage range. Values extracted from room-temperature measurements are summarized in Table 1.

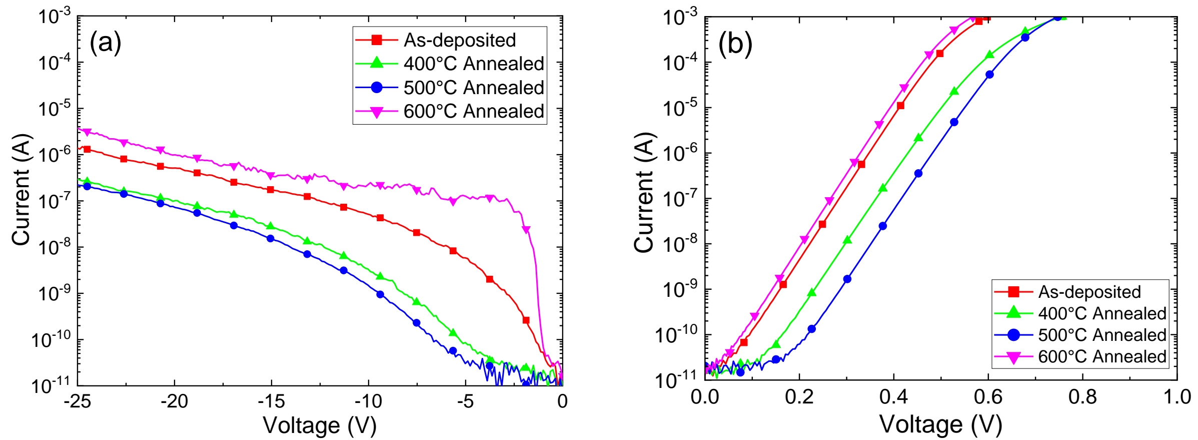

Figure 34. Room-temperature (a) reverse and (b) forward experimental IV measurements for as-deposited, 400°C, 500°C and 600°C oxidized devices.

Annealing Ru contacts in air has a considerable effect on both the forward and reverse IV characteristics, as shown in Figure 34. In the forward bias regime, the extracted values of barrier height are 0.89, 0.95, 0.99 and 0.89 eV and the ideality factors are 1.06, 1.11, 1.12, and 1.06 for the as-deposited, 400°C, 500°C, and 600°C air annealed samples respectively. In reverse bias, the leakage current magnitude of 1.38, 0.29, 0.22, and 3.77 µA at -25 V for the as-deposited, 400°C, 500°C, and 600°C air annealed samples respectively, is consistent with the variation in barrier height according to thermionic emission theory.

However, it does not account for the voltage dependence. The leakage current density for the 500°C oxidized sample is the lowest value reported to date [121-123] on GaN.

Table 1. Summary of data extracted from room-temperature IV and C-V measurements for each sample.

Sample	ϕ_{b_o} (eV)	η	R_s (Ω)	I_R at -25V (μA)
As-deposited	0.89	1.06	79.6	1.38
400°C	0.95	1.11	133.5	0.29
500°C	0.99	1.12	66.6	0.22
600°C	0.86	1.06	51.6	3.77

Extracted values of ideality factor indicate the presence of inhomogeneity ($\eta > 1$) at the M-S interface [69], thus variable temperature IV measurements were performed. Between 70 and 400 K measurements were performed in steps of 4 K on the same devices used for Figure 34. Once the temperature was stabilized to within ±100 mK for >30 s, a Keithley 2400 SMU was used to measure the IV characteristics shown in Figure 35. In addition to the linear region predicted by Equation (81) and the roll-over at increased currents caused by series resistance on a semilogarithmic plot, each of the four samples exhibits a third linear region, pronounced at temperatures below 150K and at low currents. Here, the presence of this additional region is considered to stem from isolated variation at the MS interface which presents as a small area parallel Schottky diode in the IV characteristics [108].

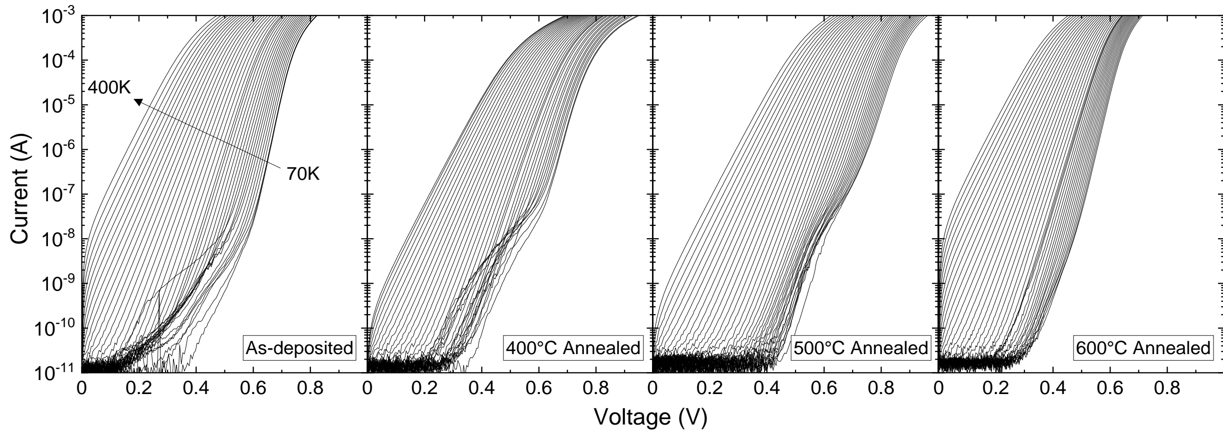

Figure 35. Forward IV characteristics of the as-deposited, 400°C annealed, 500°C annealed and 600°C annealed samples measured from 70 to 400 K.

To employ the previously mentioned iterative fitting method of parameter extraction, a multi-diode model shown in Equation (82) is used. Here, the variables $\phi_{b_i}^{eff}(0,T)$, η_i, and R_{s_i} are the temperature-dependent zero-bias effective barrier height, ideality factor and series resistance of the i-th SBD respectively. For each of the four samples, a two-diode model is used such that n is 2 for temperatures where this additional linear region is present in the IV characteristics. Fitting the IV characteristics across the full voltage and current range resulted in R^2 values greater than 0.999 for all four samples. The extracted vales of the zero-bias effective barrier height and ideality outside of the low current linear region are summarized graphically in Figure 36. Values extracted from the Schottky barrier present only at low temperatures and low currents are not reported.

$$I(V_A) = AA^*T^2 \sum_{i=1}^{n} \exp\left(\frac{-q\phi_{b_i}^{eff}(0,T)}{kT}\right)\left[\exp\left(\frac{q(V_A - IR_{s_i})}{\eta_i k_B T}\right) - 1\right] \quad (82)$$

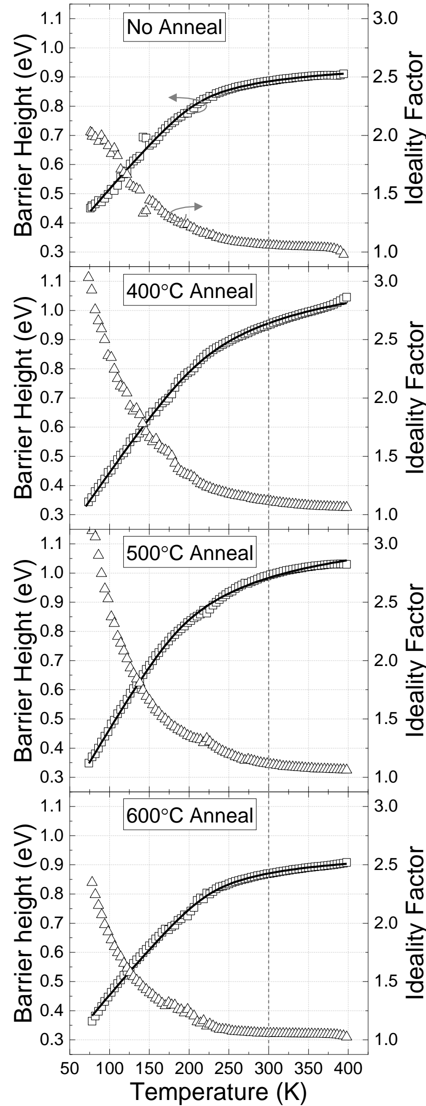

Figure 36. Extracted ideality factor (□) and effective zero-bias barrier height values (Δ)from 70 to 400 K for the (a) as-deposited, 400°C, 500°C and 600°C air annealed samples. The solid lines represents the best fit utilizing the modified log-normal distribution inhomogeneity model.

Temperature dependence of both the ideality factor and zero-bias effective barrier height confirm the likelihood of barrier height inhomogeneity at the MS interface. From Figure 36, the effective zero-bias barrier heights of each diode increase with temperature and begin to roll-off for measurements taken at >225 K. Additionally, the extracted values of ideality factor have a similar trend of roll-off with the exception that the values decrease with temperature indicating behavior indicative of a homogenous interface at higher temperatures. To understand the effect of annealing each sample, Schottky diode barrier inhomogeneity models have been developed which rely on describing the interface as a continuous distribution of barriers [69, 73, 74, 108] or regions of low barrier patches [126].

Without careful consideration to the model used, results which produce poor fitting or impossible description of the interface can occur. In a previous work [108], we showed that the interface barrier inhomogeneity both at zero bias and under simulated forward biases can be well described by a modified log-normal distribution. In this approach, the temperature dependence of the effective barrier height is defined by allowing,

$$\phi_b^{eff}(V,T) = -\frac{k_B T}{q}\ln\left(\int_{-\infty}^{\infty} P(\phi_b^V) exp\left(\frac{-q\phi_b^V}{k_B T}\right) d\phi_b^V\right) \quad (83)$$

Here, the experimentally determined zero-bias barrier height values, $\phi_b^{eff}(0,T)$, become a function of a probabilistic barrier height distribution which is itself voltage dependent, $P(\phi_b^V)$. In general an arbitrary distribution could be used; however, barrier heights observed only at temperatures which would alter the device properties, and therefore unmeasurable with IV measurement, could not be well described. Thus, the solution could not converge on a single distribution and instead a continuous distribution is used. The modified log-normal distribution used to describe the experimental data is shown below in Equation (84).

$$P(\phi_b^V) = \frac{1}{C(-\phi_b^V + A)\sqrt{2\pi}} \exp\left(-\frac{\left[ln(-\phi_b^V + A) - B\right]^2}{2C^2}\right) \quad (84)$$

Fitting the temperature-dependent effective barrier height data is accomplished by iteratively solving Equation (83) and using parameters A, B, C and the lower limit of integration to minimize the sum of squares. Using the lower limit of integration as an iteratively varied parameter effectively estimates the form of the lower barrier distribution, below that which is observed. The best fit temperature dependent effective barrier height curves are plotted as a solid line in Figure 36. Additionally, the modified log-normal distributions which produced the best fit for the zero-bias effective barrier height data, are shown below in Figure 37.

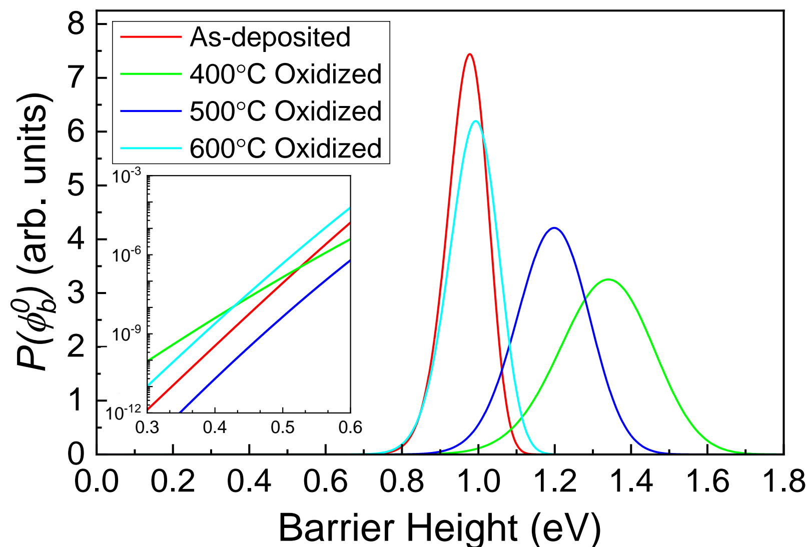

Figure 37. Modified log-normal distributions which produce the best fit the experimental zero-bias effective barrier height data extracted from IVT measurements on the as-deposited, 400°C, 500°C and 600°C air annealed samples. The inset graph shows the low barrier tails of each distribution.

The excellent agreement between the measured temperature dependence of the zero-bias effective barrier heights and the fit curve shown in Figure 36 suggests that the inhomogeneity at the metal-semiconductor interface can be characterized with the respective modified log-normal distributions in Figure 37. Typically, now that the distribution has been established, only the mean values for each samples are compared; however, according to Equation (83) it's the low barrier tail of the distribution that should have the greatest effect on the effective barrier height values and in turn the Schottky diode IV characteristics. The inset of Figure 37 shows the low barrier tail of each distribution.

Comparing the barrier distributions, we see that the greatest increase in barrier height occurs between the as-deposited and 400°C air annealed diodes. Here the peak of the distribution shifts from 0.98 to 1.34 eV while the form also widens. This implies that simply annealing the ruthenium contacts in air increases the density of higher barrier regions at the interface. However, upon examination of the inset plot, annealing the sample at 400°C also increased the density of barriers lower than 0.53 eV. This is reflected in Figure 36 where we can see the effective barrier heights extracted from higher temperature measurements (>225 K) increase with the 400°C air anneal but those extracted from lower temperatures decreases. Next, we can see that by increasing the annealing temperature to 500°C the barrier height distribution peak shifts to ~1.2 eV but the width decreases in comparison to the 400°C air annealed sample. This thinning of the distribution causes the probability of lower barrier regions at the interface of a 500°C air annealed Ru/GaN diode to drop below that of all other samples. The cause of this change can be considered to come from the change in slope of the effective barrier heights at temperatures below 150 K. Although both the 400°C and 500°C air annealed diodes can be characterized by a ~0.3 eV effective zero-bias barrier height at 70 K, the 500°C air annealed diode increases more quickly with increasing temperature to 0.70 eV at 150 K whereas the 400°C air annealed diode only increased to 0.64 eV. Finally, upon annealing the ruthenium film at 600°C in air, the distribution's form nearly returns to that of the as-deposited film. Comparing the 500°C and 600°C air annealed diodes, we see the peak again shift lower to 0.98 eV while also becoming thinner. The peak shift is related to the lower barriers extracted at higher temperatures while the higher magnitude tail is related to the lower barrier slope evident between 70 and 150 K compared to the 500°C annealed sample in Figure 36.

With the form of the inhomogeneity established at the MS interface in the as-deposited, 400°C , 500°C and 600°C air annealed samples, the variation present in the room-temperature reverse bias IV characteristics, shown in Figure 34(a), can be analyzed. Assuming the reverse current is dominated by thermionic emission over an inhomogeneous barrier, lowering the magnitude of the low barrier distribution tail will reduce the leakage current. However, in comparing the as-deposited and 400°C air annealed characteristics, we see a lowering of the leakage current for all applied voltages but, from the inset of Figure 37, the magnitude of the 400°C distribution tail is larger than that of the as-deposited one for effective barrier heights >0.53 eV. This is likely due to the screening of low barrier regions caused by the distribution of free carriers to higher energies when measurement at room temperature; however, to explain this dramatic drop in leakage current it is possible that other current conduction mechanisms are present in the as-deposited sample. Next, the leakage current decreases when comparing the 400°C and 500°C air annealed reverse IV characteristics. This is expected due to the lower magnitude of the low barrier tail between the two distributions. Finally, a large increase in the reverse leakage current can be observed after annealing a ruthenium film at 600°C in air when compared to all other samples. This rise is considered to arise from the increased magnitude of the distribution tail.

To understand how annealing the samples in air affects the GaN layers, deep-level transient spectroscopy (DLTS) was performed on the same devices used for IV characterization. DLTS measurements were made from 70 to 400 K in steps of 2 K. Deep levels were probed with a steady-state bias of -5 V and a 1 ms zero-bias filling pulse after which 300 ms of the capacitance transient was recorded. Values of activation energy and capture cross-section were extracted from Arrhenius plots of emission rate data between 6 and 400 s^{-1} according to Lang [90] and summarized in Table 2. The DLTS spectra calculated at an emission rate of 23.9Hz for each sample is shown in Figure 38.

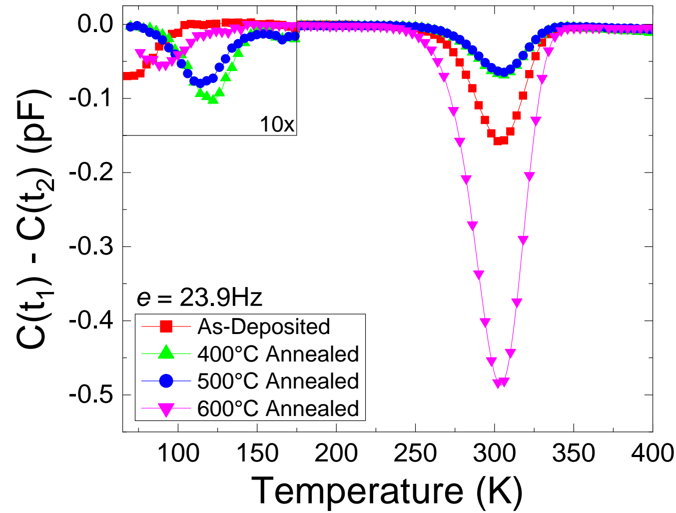

Figure 38. DLTS spectrum for the as-deposited, 400°C, 500°C, and 600°C oxidized samples.

Analysis reveals that two detectable electron traps are present in each of the samples observable by the two peaks in the DLTS spectra. In each of the samples exists the ever-present gallium nitride electron trap located at $\sim 0.58\, eV$ below the conduction band however, with varying levels of concentration. The extracted capture cross sections (σ) varied between 5.4 and $12.8 \cdot 10^{-16}\ cm^2$. Moreover, a shallow trap can be observed in each device, positioned at 82, 132, 105, and $60\ meV$ below the conduction band in the as-deposited, 400°C , 500°C and 600°C air annealed samples, respectively. The capture cross-sections are calculated at $1.47 \cdot 10^{-18}$, $3.97 \cdot 10^{-19}$, $5.40 \cdot 10^{-20}$, and $5.17 \cdot 10^{-21}\ cm^2$ for the as-deposited, 400°C , 500°C and 600°C air annealed samples, respectively. The trap concentration (N_T) can be calculated according to Equation (85) [Section 2.3.5.6]. Here, ΔC is the capacitance change from $t(0)$ to the steady-state value (C_∞) and N_D is the free carrier concentration. The trapping characteristics are summarized in Table 2.

$$N_T = 2\frac{\Delta C}{C_\infty} N_D \tag{85}$$

Table 2. Summary of observed trap characteristics in the as-deposited, 400°C, 500°C, and 600°C annealed samples.

	Trap 1			Trap 2		
	E_T (eV)	σ (cm^2)	N_T $(10^{14}\ cm^{-3})$	E_T (meV)	σ (cm^2)	N_T $(10^{14}\ cm^{-3})$
As-deposited	0.58	$5.39 \cdot 10^{-16}$	19.10	82	$1.47 \cdot 10^{-18}$	0.82
400°C Annealed	0.59	$8.68 \cdot 10^{-16}$	10.40	132	$3.97 \cdot 10^{-19}$	1.80
500°C Annealed	0.60	$12.8 \cdot 10^{-16}$	8.87	105	$5.40 \cdot 10^{-20}$	1.37
600°C Annealed	0.57	$6.53 \cdot 10^{-16}$	54.71	60	$5.17 \cdot 10^{-21}$	1.06

Previously, the concentration of the $0.59\ eV$ trap level has been linked to various impurity species [44, 85, 96, 127], growth substrate [128-130], and extrinsic perturbations [131-133]. Recent work by Galiano et al. [134] was able to spatially link the signal from this trap to pure edge dislocations and possible interactions with impurities. Accordingly, it is speculated here that by annealing the samples, impurities interacting with these edge dislocations at the surface can be modulated by the presence of ruthernium thereby contributing to the lateral variation of the barrier height at the metal-semiconductor interface. If the concentration of this trap is too high, its possible that current conduction caused by tunneling into a trap band continuum could also contribute to leakage current in reverse bias [80, 135]. Thus, it is believed here that the large change in leakage current between the as-deposited and 400°C air annealed as well as the 500°C and 600°C air annealed samples, is in part caused by a large change in concentration of the 0.57 eV trap. The change in concentration of the traps located between 60 and $132\ meV$ below the conduction band have typically been observed in GaN layers bombarded with radiation [136-138]. Presently, it is unknown what causes the energy shift of these traps.

3.2.4 Conclusion

In conclusion, the electrical behavior of ruthenium Schottky contacts as-deposited, 400°C, 500°C and 600°C air annealed on n-GaN are compared. The temperature-dependent IV characteristics were fit, and the extracted effective barrier height temperature dependence of each device was shown to be caused by inhomogeneity at the M-S interface. It was found that the barrier inhomogeneity could be well described by the modified log-normal distribution. Analysis of the apparent barrier distributions revealed the cause of variation in both the forward and reverse IV characteristics at room temperature. In reverse bias, it was shown that the low barrier distribution tail is the key factor in determining the leakage current and that favorable results occur for diodes annealed up to 500°C and further annealing the ruthenium film at 600°C drastically increases leakage current. To understand the effect that annealing the samples in air have on the GaN film, DLTS was performed revealing that each device has two observable electron traps, the ever-present 0.57 eV trap and a shallow trap. It is believed that the 0.57 eV trap may be the cause of inhomogeneity at the M-S interface and that annealing the ruthenium thin-films effectively changes the traps concentration.

3.3 Electrical Characterization of GaN-on-Sapphire Drift Layers Grown with Increasing TMGa Molar Flow Rates

3.3.1 Abstract

In an effort to understand the effects of non-ideal material growth on the electrical behavior of GaN Schottky diodes, drift layers grown with varying trimethylgallium (TMGa) and silane molar flow rates by metal-organic chemical vapor deposition are examined. In this work, results of IV, IVT, CV, DLTS and DLOS characterization of Schottky diodes prepared from drift layers grown with 1x 2x and 3x TMGa are presented. It was observed that not only the free carrier concentration but also the electron mobility suffers from the increase in compensating impurity incorporation resulting in Schottky diodes with increasing series on-resistances. DLTS and DLOS measurements revealed levels at E_C - E_T = 0.03, 0.57 and 2.30 in addition to levels at 2.70, 2.90, and 3.20 eV that show concentration dependences on TMGa and silane molar flow rate.

3.3.2 Introduction

Sustained interest in bringing high power handling electronic devices to market has led the push for thicker and lower doped GaN drift layers for use in power conversion applications. Considering the 1D calculation of electric field in a semiconductor drift layer with a rectifying contact, the breakdown voltage becomes a function of free carrier concentration and drift layer thickness. In Figure 39, it can be seen that for a given free carrier concentration, drift layers with sufficient thickness need to be grown otherwise avalanche breakdown limits cannot be met and carrier punch-through will dominate. The requirements for a 20kV breakdown-capable drift layer are indicated with a grey dashed line.

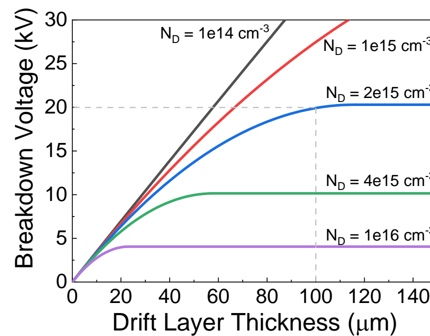

Figure 39. The 1-D calculation of breakdown voltage for drifter layers of different thickness and free carrier concentration.

To ensure avalanche breakdown of a 20kV-capable device, a 100 µm drift-layer width, uniformly doped at $2 \cdot 10^{15}\ cm^{-3}$ would need to be grown. As previously discussed in Section 2.1.2.1, lateral devices require only that the top surface separation between the high voltage contacts meet this length requirement. However, non-ideal effects from surface perturbations and larger than ideal on-resistances can be avoided with a vertical structure implementation. Thus, a 100 µm thick uniformly doped drift layer would need to be grown to reach the theoretical material limit of GaN.

The GaN grown by MOCVD in the Guido Group is performed in nitrogen-rich conditions; thus the layer growth speed is largely considered to be rate limited by the flow of TMGa during growth. In Figure 40(Left), this is confirmed for samples grown on both bulk-GaN and sapphire substrates where the growth rate is extracted from SIMS measurements on multi-layer stacks grown under different conditions. This plot shows that GaN grown with increased molar flow rates of TMGa will be able to reach the desired thickness more quickly. However, an inspection of the free carrier concentration in Figure 40(Middle),

reveals that a background carrier compensating species also increases. This presents a problem where control over the effective free carrier concentration becomes very difficult, if not impossible due to the sudden drop as the silane flow is lowered.

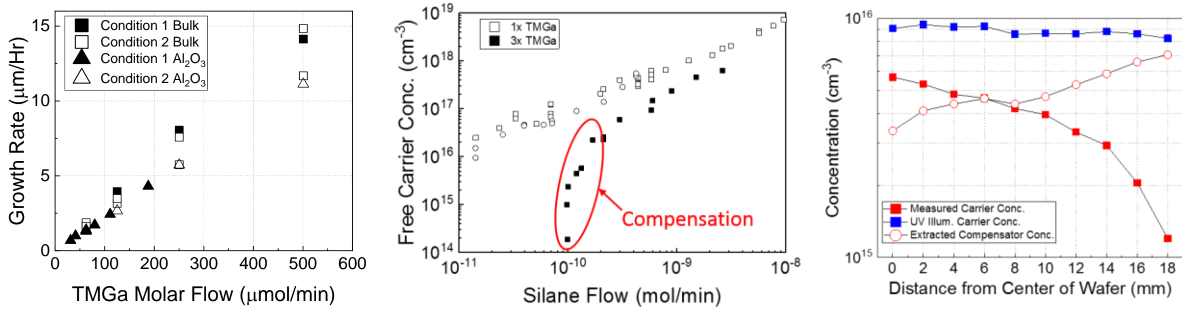

Figure 40. (Left) The growth rate extracted from SIMS measurements of GaN multi-layers with varying molar flow rates of TMGa are plotted. (Middle) The effective free carrier concentration from Hg-probe measurements is plotted versus silane flow for two TMGa molar flow rates. (Right) The effective free carrier concentration without (red) and with (blue) UV-LED backside illumination are plotted radially from the center of a low-doped GaN-on-bulk sample. The calculated compensator concentration $\left(N_D^{UVon} - N_D^{UVoff}\right)$ is also plotted versus the radial distance from the center of the low-doped GaN-on-bulk sample.

In Figure 40(Right) the effective free carrier concentration was measured by CV on an Hg probe radially from the center toward the perimeter of a 2” GaN-on-bulk wafer, first without and then with backside illumination from a UV LED. This measurement reveals that in addition to low controllability of effective free carrier concentration when the doping source approaches that of the compensating source, a lateral variation of the effective free carrier concentration is also observed. This lateral variation has also been observed within the literature for GaN grown on bulk-GaN substrates [139].

3.3.3 Experimental Procedure

To study the effects of varying TMGa on Schottky diode behavior, three MOCVD-grown drift layers on sapphire were prepared, each with varying trimethylgallium (TMGa) molar flow rates of 63, 125 and 188 µmol/min and subsequently referred to as the 1x, 2x, and 3x TMGa samples, respectively. The expected increase in compensating impurity concentrations was counteracted by proportionally increasing the silane flow from 71 to 143 to 214 pmol/min for the 1x, 2x, and 3x samples, respectively. The growth conditions are summarized in Table 3. Planar Schottky diodes were fabricated according to Section 3.1.4 except a Ni/Ag contact was deposited as the rectifying contact. In addition to the Schottky contacts, circular TLM structures were patterned on the top surface of each sample with the ohmic stack (Ti/Al/Ni/Ag) that was reported in Section 3.1.4. Next, room-temperature IV and CV characteristics of all diodes on each sample were measured. Devices with representative behavior were chosen to execute trap spectroscopy measurements. Capacitance transients were captured for each sample between 50 and 400 K in steps of 2 K to measure the DLTS spectra. Characterization of deeper traps by SSPC/DLOS was performed with optical excitation from a computer-controllable monochromatic source in photon energy steps of 10.8 meV from 0.9 to 3.6 eV.

Table 3. Summary of the MOCVD growth conditions used for the 1x, 2x, and 3x TMGa samples

Sample	TMGa Molar Flow (mol/min)	Silane Flow (mol/min)
1X	$63 \cdot 10^{-6}$	$71 \cdot 10^{-12}$
2X	$125 \cdot 10^{-6}$	$143 \cdot 10^{-12}$
3X	$188 \cdot 10^{-6}$	$214 \cdot 10^{-12}$

3.3.4 Results and Discussion

CV measurements were taken using a Sula capacitance meter with a 1 MHz 30 mV_{rms} AC probing signal superimposed on a DC sweep between 0 and -5 V. The extracted data is shown below in Figure 42(Left) and indicates that the effective free carrier concentration decreases from an average of $11.6 \cdot 10^{16}$ to $3.4 \cdot 10^{16}$ to $2.5 \cdot 10^{16}\ cm^{-3}$ in the 1x to 2x to 3x samples respectively. This trend is expected due to the predicted increase in carbon impurities and its nature to incorporate as a compensating acceptor [82, 94, 140, 141] however, the three-fold decrease from the 1x to 2x samples is not. Ideally, the extracted carrier concentration by CV will mimic that of the difference between dopant and acceptor concentration ($N_{Si} - N_C$); however, carbon incorporation can be quite complicated, resulting in more than just shallow acceptors especially under conditions where $N_{Si} \approx N_C$. Tanaka et al. has fabricated samples with carbon concentrations both higher and lower than the intentional silicon concentration and found that the effective free carrier concentration indeed cannot be considered fully compensated. It was also observed that under certain conditions a portion of the carbon concentration will participate as a donor atom, effectively increasing the overall free carrier concentration [142].

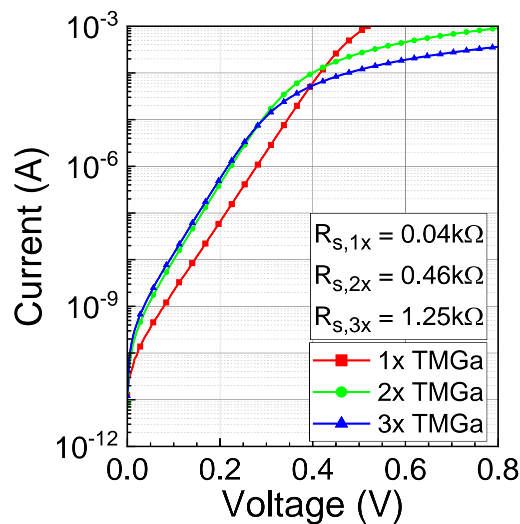

Figure 41. Typical room-temperature Schottky diode IV characteristics on the 1x, 2x, and 3x TMGa samples.

In Figure 41, the room-temperature forward IV characteristics of a typical Schottky diode are shown for each sample. The rollover at lower absolute current values indicates that the forward on-resistance is negatively affected by the increase of TMGa. Utilizing the dampened least-squares fitting algorithm according to Section 3.1.4, the extracted series on-resistance values are 0.04, 0.46 and 1.25 kΩ.

TLM patterns next to the reported Schottky diode were measured between -1 and 1 mA. Below in Figure 42(Right), the total resistance versus TLM ladder separation is plotted. The solid lines are the result of a linear least squares fit to the data so that contact resistance and sheet resistance can be extracted from the y- and x-intercept, respectively. Similar to that observed in the Schottky IV characteristics, the sheet resistance increases with increasing TMGa flow; however, the change in absolute values implies the mobility is also effected. Considering the geometry of the circular TLM patterns, the calculated values of mobility are 579.1, 347.7, and 195.3 $\frac{cm^2}{V \cdot s}$ for the 1x, 2x, and 3x samples respectively.

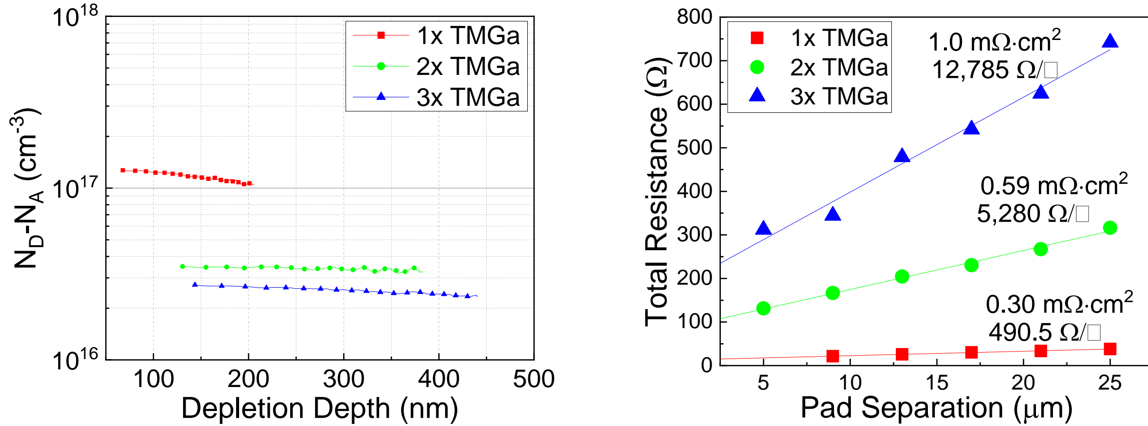

Figure 42. (Left) CV and (Right) TLM measurements of GaN samples grown with 1x, 2x, and 3x TMGa and Silane flows. The solid line on the TLM plot represents the linear least squares fit to the data.

Next, DLTS measurements were performed on the Schottky devices where each sample was held at a -5 V steady-state bias and the transient response was measured after a 1 ms injection pulses at zero-bias between 50 and 400 K. Each measurement consisted of 70 averaged transients to remove Gaussian noise and improve subsequent exponential fitting. The results of the DLTS test are summarized in Table 4 while the DLTS spectra and Arrhenius plots are shown in Figure 43.

Table 4. Summary of trap characteristics for the 1x, 2x, and 3x samples measured by DLTS

	$E1$			$E2_1$		
Sample	$E_C - E_t$ (eV)	σ_n (cm^2)	N_T (cm^{-3})	$E_C - E_t$ (eV)	σ_n (cm^2)	N_T (cm^{-3})
1x	–	–	-	$0.59\ eV$	$1.02 \cdot 10^{-15}$	$1.3 \cdot 10^{15}$
2x	–	–	-	$0.60\ eV$	$2.07 \cdot 10^{-15}$	$1.8 \cdot 10^{15}$
3x	$0.03\ eV$	$8.82 \cdot 10^{-22}$	$0.25 \cdot 10^{15}$	$0.58\ eV$	$1.04 \cdot 10^{-15}$	$1.2 \cdot 10^{15}$

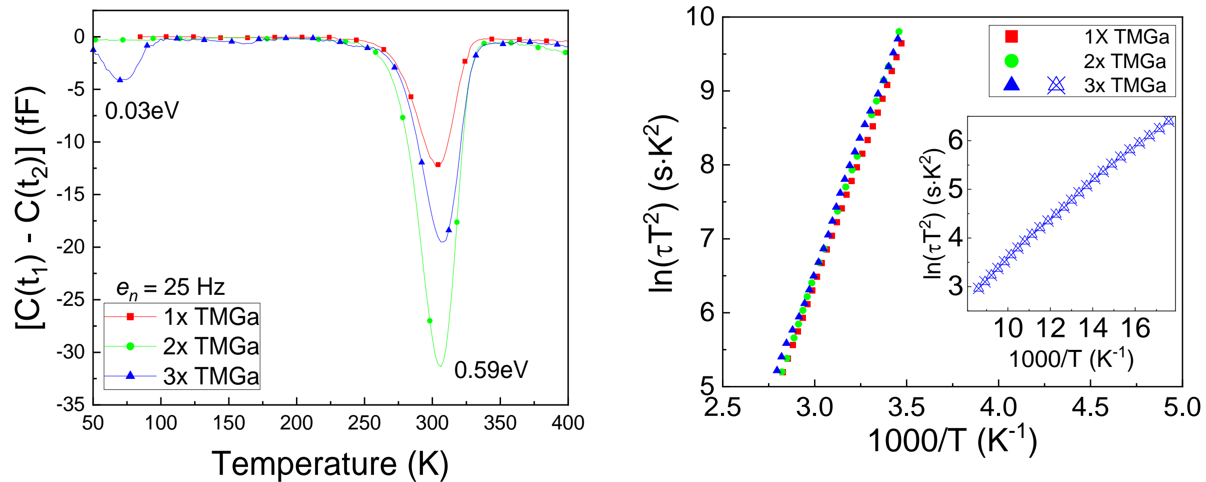

Figure 43. (Left) DLTS spectra with a rate window of 25Hz and (Right) Arrhenius plots for the 1x, 2x, and 3x samples. Each sample shows evidence of two traps centered around 300K while an additional trap level at 30meV can be observed in the 3x sample around 75K.

To probe deep level traps with binding energies larger than 1 eV from either the conduction of valence band, steady-state (SSPC) and transient (DLOS) optical response techniques were performed. The samples were illuminated with a 300W Hg-Xe lamp coupled into a 0.3 m monochromator with a computer controlled mode sorting filter on the output. The optical intensity over the wavelength range was normalized with a calibrated computer-controlled ND filter and the resulting light was coupled into the sample with an optical fiber positioned at an oblique angle. A shallow trap filling pulse of 0 V for 10 s and a subsequent 30 s at a -5 V steady-state bias was deemed sufficient in minimizing the effects of thermal emission/capture prior to the shutter opening.

In Figure 44(Left), the changes to the steady-state capacitance signal can be observed over the rage of incident wavelengths from 540 to 340nm. The onset of increased signal implies that the optical energy of the impinging monochromatic light is large enough to induce captured charge emission into either the conduction or valence band. The magnitude of this onset corresponds to the concentration of the emitted trap where positive onsets indicate that electrons are emitted from the deep level into the conduction band and vice-versa for hole emission. All of the detected traps came from carrier emission from the defect level into the conduction band. The SSPC signal has been normalized according to Equation (86) and the value of effective free carrier concentration (N_D) extracted from room temperature CV measurements.

$$N_T = 2N_D \frac{[C(0) - C(\infty)]}{C(\infty)} \quad (86)$$

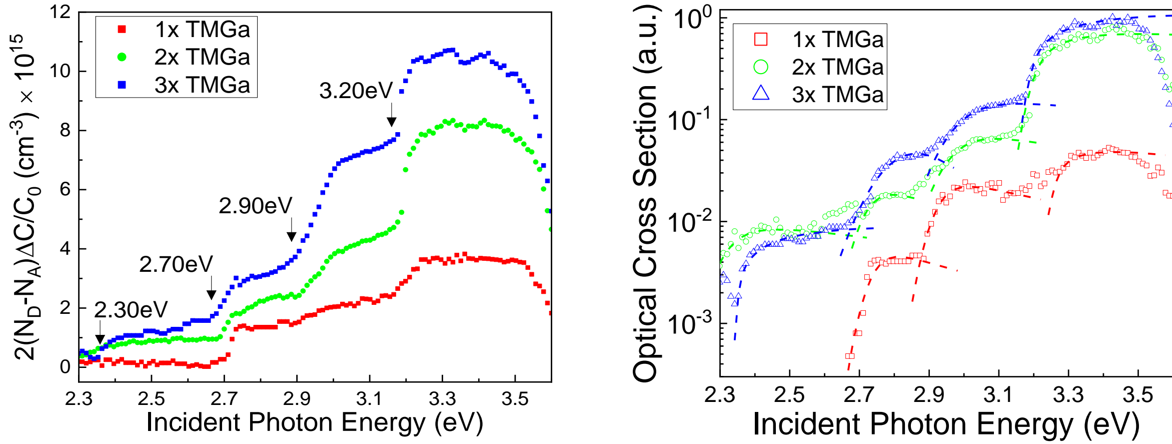

Figure 44. (Left) Steady-state photocapacitance signal and calculated optical cross-section for the 1x, 2x, and 3x samples (scatter). (Right) Sections of the ranges of optical cross section were fit with the Chantre-Vincent-Bois model yielding the energy levels plotted on the SSPC graph. Levels at 2.70, 2.90 and 3.20 eV can be observed for each of the samples; however, the level at 2.30 eV is only observed for the 2x, and 3x samples.

On the right side of Figure 44, the optical cross-section, calculated from the slope of the capacitive transients is shown for each sample. Typically, the simpler minima-to-minima transition model (Lucovsky model) is used to fit the optical cross-section data and extract the characteristic trap depth energy however fitting each region with the iterative L-M fitting procedure produced inaccurate results for all fit ranges. Therefore, the energy values for trap depth (ΔE_t) shown on the SSPC plot were calculated from fitting parts of the optical cross section with the Chantre-Vincent-Bois model shown in Equation (87). Results from the best fit are shown as dashed lines with the same color as the corresponding samples experimental data in Figure 44. The values extracted for each of the observed deep level traps from SSPC measurements are summarized below in Table 5.

$$\sigma_n(hv) = A \cdot \frac{1}{\left(\frac{hv}{E_o}\right)\sqrt{\frac{4k_bTd_{FC}}{E_o^2}}} \int_1^{\infty} \frac{\sqrt{x-1}}{(x-1+m)^2}\, e^{-\frac{\left(\frac{hv}{E_o}-x\right)^2}{\left(\frac{4k_bTd_{FC}}{E_o^2}\right)}} dx \qquad (87)$$

Table 5. Values of trap depth from the conduction band and concentration extracted from each SSPC onset shown in Figure 19 using the Chantre-Vincent-Bois equation.

	Trap 1		*Trap 2*		*Trap 3*		*Trap 4*	
Sample	E_0 (eV)	N_t $(10^{15}cm^{-3})$	E_0 (eV)	N_t $(10^{15}cm^{-3})$	E_0 (eV)	N_t $(10^{15}cm^{-3})$	E_0 (eV)	N_t $(10^{15}cm^{-3})$
1x	–	–	2.70	1.09	2.86	1	3.23	1.3
2x	2.28	0.9	2.69	1.35	2.91	2.3	3.17	3.4
3x	2.33	1.1	2.70	1.5	2.91	4.4	3.16	2.9

In order to understand what effects variable TMGa and Silane flow have on the deep level trap behavior, the currently reported physical source of each trap is discussed. Here, information is compiled and analyzed from the literature where GaN traps have been observed using various techniques and growth methods.

3.3.4.1 E1 Trap

From the DLTS spectra in Figure 43, a peak which exists in the 3x sample but not the others can be clearly observed with a characteristic trap energy of 33 meV, a capture cross-section of $8.82 \cdot 10^{-22}\ cm^2$ and an extracted concentration of $2.5 \cdot 10^{14}\ cm^{-3}$. From the Arrhenius plot, experimental data spans >3 decades along the $\ln(\tau T^2)$ axis with a clearly linear trend indicating that these results are not simply from artifacts of measurement setup or a miscalibrated temperature detector. However, this is the first known report of this trap detected by DLTS. Results reported by PL, resonance Raman scattering and variable temperature Hall measurements have identified donor trap states around this level (17-34 meV) attributing it to silicon [143-145] oxygen [144], and carbon [126, 146] but consensus has not been reached.

3.3.4.2 E2 Trap

The DLTS peak apparent around 300K could be well described by a single Gaussian peak for each of the three samples generating a single straight line on the Arrhenius plots. The extracted values of trap densities according to Equation (86) for the samples are similar and measured at $1.3 \cdot 10^{15}$, $1.8 \cdot 10^{15}$, and $1.2 \cdot 10^{15}\ cm^{-3}$ for the 1x, 2x and 3x samples respectively. Considering the closeness in both the trap characteristics and the concentrations, it is likely the reported variation in TMGa and Silane flow plays no role in perturbing this cluster of deep level traps.

In the literature there is a history of debate as to the source of the E2 trap in GaN but has been reported in different structures [104, 128], by different growth methods [105, 147, 148], and ascribed to different root causes. As part of the effort to understand where in HEMT devices large concentrations of traps are located, Galiano et al. uses a form of DLTS that has been integrated into an atomic force microscope called scanning probe DLTS to measure the surface potential with nanometer resolution. The surface potential is then modulated by the depletion region of a Schottky contact situated in plane with the AFM measured area. Applying pulses just as with conventional DLTS measurements induces the typical trap emission transients along the edge of the depletion region which includes the portion at the surface. This emission transient will therefore prompt a perturbation of the surface potential which is measured and analyzed. The results were then coupled to electron channeling contrast imaging (ECCI) made on the same area and it was concluded that pure edge dislocations were directly related to the E2 trap; however, an exact model for the trap characteristics was not found. In the report it is speculated that the pure edge dislocation may form a 'Cottrell Atmosphere' that behaves as an impurity getter thus, the signature is likely a complex mixture of native and impurity-induced defects [134]. Considering this finding holds for the reported 1x, 2x, and 3x samples, it appears neither the increase in TMGa nor silane flow under these conditions has an effect. This implies that either the defect is perturbed only by the presence of pure edge dislocations, which would not vary under these conditions, or that incorporated impurities around the pure edge dislocations does not vary under these conditions.

3.3.4.3 Trap at 2.3 eV

From the SSPC results in Figure 44 the trap corresponding to the $E_C - 2.3\ eV$ excitation threshold cannot be observed in the 1x sample but is apparent in both the 2x and 3x samples. This is likely due to either the higher background free carrier concentration reducing the transient capacitance signal below the noise floor or simply from the fact that it does not exist in the 1x sample. For this reason, the concentration of this trap in the 1x sample cannot be attributed definitively to the MOCVD growth conditions. Additionally, the concentration of Trap 1 in the 2x and 3x samples are comparable and therefore considered to be independent of the MOCVD growth conditions.

The energy of this defect determined by fitting a portion of the DLOS transient measurements is similar to the long observed yellow luminescence centered around 2.23 to 2.3 eV. This trap level has been measured by many and proposals for its origin include a complex between a lone gallium vacancy, a (V_{Ga}) complex with a carbon or oxygen atom, or nitrogen antisite (N_{Ga}) [70, 149]. However, work has shown that upon growing GaN under more Ga-rich conditions, the PL signal intensity and thus the concentration of the responsible defect decreases [73, 150]. Thus the SSPC signal in these samples is expected to decrease as the TMGa is increased unless its origin is not solely from V_{Ga} incorporation. Using a self-consistent-charge density-functional-based tight-binding approach, Lee at al. showed that the electronic structure of threading edge dislocations in GaN can induce deep-level states. From their calculations, it's possible that the observed 2.3 eV level is related to a nitrogen vacancy at the 'C site' calculated to create a level at $E_{VB} + 1.3\ eV$ [151].

3.3.4.4 Traps at 2.70 and 2.90 eV

A sharp rise in both the SSPC and optical cross-section data can be observed at the 2.70 and 2.90 eV levels for each of the samples along with an increase in concentration, extracted from the SSPC signal, in relation to the TMGa and silane molar flow rates. Levels similar to those reported here have been observed and, based on the work of Van De Walle [64], are attributed to gallium vacancies or a gallium vacancy complex [82, 152-156]. Van De Walle predicts that hydrogenated gallium vacancies in GaN will induce band gap states around 1 eV from the conduction band and shift toward the valence band as the defect becomes hydrogenated. The reported level around 2.70 and 2.90 eV are therefore assigned to a hydrogenated gallium vacancies $(V_{Ga}H)^{2-}$ and $(V_{Ga}H_2)^{-}$ respectively. Inferences have been made about traps with similar binding energies [82, 154, 155]; however, more work is needed to understand its exact origin. Upon extracting the concentration of the 2.70 eV trap, it was found that a slight increase with TMGa and silane is observable while the concentration associated with the 2.90 eV trap increases 4x. Assuming the origin is correctly attributed to a hydrogenated gallium vacancy complex, this implies that increased concentrations TMGa and silane will introduce higher levels of hydrogen into the bulk of the material either from the decomposed SiH_4, radical CH_3 molecules, or a mechanism that favors incorporation of the hydrogen carrier gas. Additionally, previous work has observed a level close to 2.90 eV assigned to C_N [94, 152] however, both modeling [157] and experimental results yield Franck-Condon energy (d_{FC}) shift of 0.4 - 0.5 eV which are much larger than the extracted values of 0.02 to 0.09 eV observed for the reported samples.

3.3.4.5 Trap at 3.20 eV

The SSPC onset around the 3.20 eV photon energy is present in all three samples and indicates that its concentration increases by 2.5x from the 1x to 2x samples but remain steady from the 2x to 3x sample. Early reports of deep levels with a characteristic energy around E_C-3.28 were attributed to Mg_{Ga} defects [158, 159] however after theoretical calculations of induced energy levels caused by carbon [160], reports almost unanimously contribute the appearance of this trap to the presence of the nitrogen substitutional defect, C_N [154, 161-163]. Therefore, the change in concentration of the E_C - 3.20 eV deep level between the 1x and the 2x samples is considered to be caused by an increase in C_N incorporation. Additionally, in keeping with the reports of carrier compensation caused by this deep level, the drop in effective free carrier concentration between the 1x and 2x samples along with the slight decrease between the 2x and 3x samples is attributed solely to the presence of C_N. However, as the TMGa molar flow rate increases from 125 to 188 μmol/min, the incorporated carbon, and compensating concentration is expected to increase. Consequently, it is presumed that the absence of additional C_N concentration implies that

carbon is incorporated instead on the gallium site (C_{Ga}) or as an interstitial (C_i). As cited previously in Section 3.3.4.1, reports on the appearance of the deep levels similar to that of the E1 trap have been associated with a shallow carbon donor. Therefore, it is reported here that as the TMGa molar flow rate is increased, substitutional carbon concentrations saturate and additional carbon incorporates as a shallow donor associated with either carbon interstitials or a complex with C_N.

3.3.5 Conclusion

A comprehensive collection of electrical characterization techniques were used to investigate the variation of the electrical behavior and deep level trapping characteristics in separate GaN layers grown with increased TMGa and silane flow. With the increase in TMGa molar flow rates, it was observed that the effective free carrier concentration from CV measurements drops even with a proportional increase in silane flow. Additionally, from TLM measurements, it was revealed that the lateral mobility is also affected, resulting in forward Schottky diode on-resistance that increased from 0.04 to 1.25 kΩ. From, DLTS and SSPC/DLOS measurements deep levels at E_C - E_T = 0.03, 0.57, 2.30, 2.70, 2.90, and 3.20 eV are revealed and compared to reports in the literature. The concentrations of the deep levels located 2.70, 2.90, and 3.20 eV from the conduction band show a dependance on TMGa flow where the first two are considered to be associated with the hydrogenated gallium vacancies $(V_{Ga}H)^{2-}$ and $(V_{Ga}H_2)^{-}$ respectively while the third is considered to be from the carbon substitutional, C_N. Finally, the appearance of the shallow donor trap around 30 meV below the conduction band is speculated to come from interstitial carbon or a complex formed with C_N.

3.4 Effect of Ammonia Variation on Device Characteristics in n-GaN/GaN

3.4.1 Abstract

Previous work reveals that control of the incorporated carbon concentrations is tightly linked to the ratio of ammonia molar flow rate to the growth rate. In this work, results of CV, DLTS and DLOS characterization of vertical Schottky diodes prepared from drift layers grown at a constant rate (2 µm/hr) on bulk GaN with 1x 2x and 4x input ammonia molar flow rates by metal-organic chemical vapor deposition (MOCVD) are presented. Capacitance versus voltage measurements revealed a noticeable decrease in compensation as the ratio was increased from 1x to 2x. Deep level transient spectroscopy (DLTS) and steady-state photo-capacitance measurements were performed, revealing four deep levels at E_C-E_T = 0.57, 2.60, 2.82, and 3.13 eV. As expected, the observed concentration of each reported deep level trap decreased, thereby validating the usefulness of these growth conditions to create low defect drift layers for GaN power devices. Finally, field-plated structures were fabricated in an attempt to observe the effect of varying growth rate and deep level defect concentration on the reverse Schottky leakage current however; it was revealed that the reverse characteristics were dominated by TFE over a homogeneous barrier and not the bulk properties.

3.4.2 Introduction

From Section 3.3, it was observed that by increasing the trimethylgallium (TMGa) molar flow rate from 1x to 3x, low-doped GaN layers grown on sapphire could be achieved. Additionally, because growth is performed in nitrogen-rich conditions, the increased TMGa flow induces a faster growth rate, a feature necessary for quickly growing thick drift layers for avalanche capable vertical devices. However, it was observed from IV, CV, DLTS and SSPC/DLOS measurements that with increasing TMGa flow during growth, the deep level defect concentration increased causing increasing donor compensation and a decrease in lateral carrier mobility. Additionally, growth of high voltage-capable drift layers becomes difficult since the compensator concentration begins to approach that of the doping concentration thereby making control difficult. Section 3.3 also revealed that the primary compensator is likely associated with carbon incorporated during growth. Thus, work was done in an attempt to understand how the carbon concentration could be controlled which is especially difficult since the main source of carbon is considered to originate from the incomplete pyrolysis of TMGa during growth [57].

First, it was observed that the increasing growth rate with input TMGa molar flow could be curtailed by the total molar flow of ammonia. In Figure 45(Left), the growth rate calculated from SIMS measurements is shown for GaN multi-layer stacks grown with variable TMGa and ammonia molar flow rates. Here, it can be observed that for a set TMGa molar flow rate, increasing the ammonia molar flow during growth will lower the overall growth rate. This effect is considered to be caused by an increase in parasitic reactions in the gas phase, which do not contribute to growth.

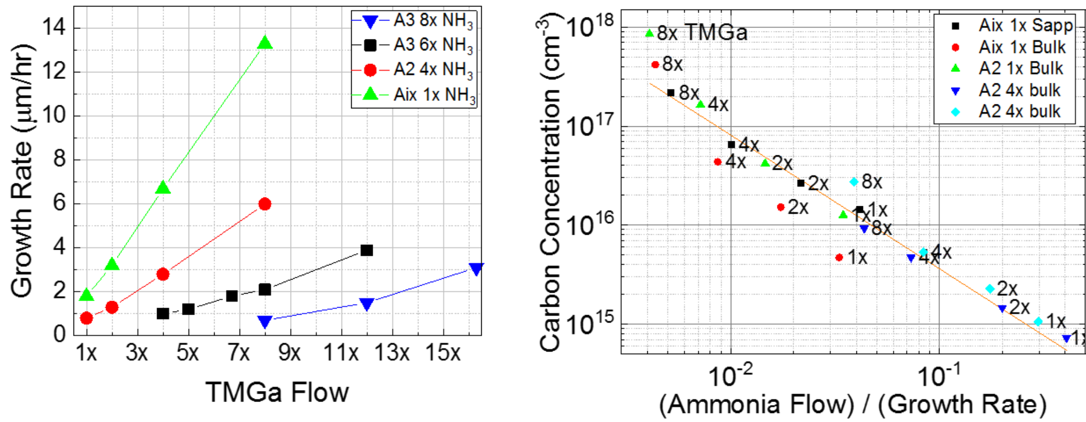

Figure 45. (Left) Growth rate extracted from SIMS measurements on GaN multi-layers growth with varying TMGa and ammonia molar flow rates. The (Right) carbon concentration was measured and plotted as a function of ammonia molar flow to growth rate ratio.

Next, the effect of varying the ammonia molar flow is plotted for different TMGa molar flow rates in Figure 45(Right). It was found that by normalizing the ammonia molar flow with the growth rate, incorporated carbon concentration could be determined regardless of the TMGa molar flow. This finding indicates that for a given TMGa flow, the compensating carbon incorporation can be decreased by increasing the total ammonia molar flow rate. This observation is considered to be, in effect, caused by increased competition from nitrogen compared to carbon for incorporation at the same lattice site.

3.4.3 Experimental Procedure

To understand the effect that varying ammonia flow has on deep level defects, three GaN drift layers were grown by MOCVD on separate Mitsubishi Chemical bulk GaN wafers. In each sample, growth was initiated with a 0.25 µm N+ layer to minimized any effect the regrown interface may have. Next, a 6 µm drift layer was grown on each sample where the ammonia molar flow rate was increased from 58 to 116 to 231 mmol/min and subsequently referred to as the 1x, 2x and 4x NH_3 samples, respectively. To ensure that the growth rate was kept constant at 2 µm/hr, the TMGa was increased according to results from previously observed trends in SIMS measurements on GaN-on-GaN multi-layer stacks. The calculated TMGa molar flows required to ensure a 2 µm/hr growth rate was maintained are 66.9, 83.0, and 213.3 µmol/min for the 1x, 2x, and 4x NH_3 samples, respectively. The silane molar flow rate was kept constant for each sample and a doping concentration of $10^{16}\ cm^{-3}$ was expected. The growth conditions are summarized below in Table 6.

Table 6. Summary of the MOCVD growth conditions used for the 1x, 2x, and 3x NH_3 samples

Sample	Ammonia Flow (mmol/min)	TMGa Flow (µmol/min)	Silane Flow (pmol/min)	V/III Ratio	Approx. Growth Rate (µm/hr)
1x	58	66.9	17.8	855	2.0
2x	116	83.0	17.8	1397	2.0
4x	231	213.3	17.8	999	2.0

Next, 1 cm^2 pieces were cleaved from each sample for the fabrication of vertical Schottky diodes. Each sample was sonicated in acetone, then isopropyl alcohol for 10 minutes and rinsed in deionized water. Samples were soaked in a bath of aqua regia followed by a 49% HF bath, each sitting at room temperature

for 10 minutes. Again the sample was rinsed in deionized water followed by a nitrogen drying step. Next, an ohmic broad-area back contact of Ti/Al/Ni/Ag (30/100/50/150 nm) was deposited by e-beam in a vacuum of <10^{-6} Torr. The sample was annealed at 700 °C under a continuous flow of dry N_2 for 5 minutes to improve ohmic contact resistivity. Circular Schottky contact regions ranging in diameter from 25 to 250 µm were defined by optical lithography, and a Ni/Au (50/150 nm) stack was deposited by E-beam, yielding 80 diodes after lift-off. The effective free carrier concentration was extracted from room-temperature CV measurements around the zero-bias depletion width at $5.8 \cdot 10^{15}$, $8.4 \cdot 10^{15}$ and $9.2 \cdot 10^{15}$ cm^{-3} for the 1x, 2x and 4x NH_3 samples, respectively. These values are close to the expected value of $1 \cdot 10^{16}$ cm^{-3}. Next, the sample was mounted to an electrically isolated temperature controlled stage in an MMR microprobe station with a CTI Model 22 cryostat where DLTS measurements were performed between 50 and 400K in steps of 2 K on a characteristic 250 µm diameter diode. Once the temperature was stabilized to within ±100 mK of the target for >30 s, a 300 ms capacitance transient was recorded after a 10 ms pulse from the steady-state voltage of -10 V to zero-bias. Finally, characterization of deeper traps by SSPC/DLOS was performed with pulses of optical excitation from a computer-controllable monochromatic source after spending 45 s in the dark to reach thermal equilibrium. The photon energy steps of 10.8 meV from 0.9 to 3.6 eV were used to profile deep levels throughout the bandgap of GaN.

3.4.4 Result and Discussion

CV measurements were taken using an HP4192 impedance analyzer with a 1 MHz 30 mV_{rms} AC probing signal superimposed on a DC sweep between 0 and -35 V. The effective free carrier concentration is shown below in Figure 46 and indicates that the extracted values remain constant throughout the measured depletion depth. This effective free carrier concentrations determined at zero-bias are $5.8 \cdot 10^{15}$, $8.4 \cdot 10^{15}$ and $9.2 \cdot 10^{15}$ cm^{-3} for the 1x, 2x and 4x NH_3 samples, respectively. Considering the effect of increasing ammonia molar flow for a set growth rate, it assumed here that the silicon concentration does not vary between samples and that this effect is caused by the variation in density of compensating species.

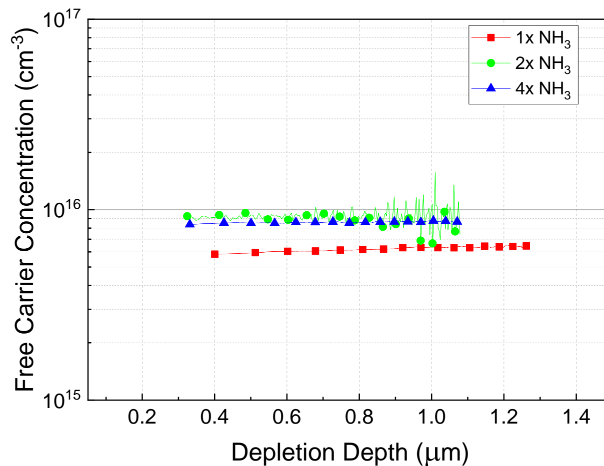

Figure 46. Effective free carrier concentration depth dependence calculated from CV measurements take from 250 um Schottky diodes on the 1x, 2x, and 4x NH_3 samples

Next, DLTS measurements were performed on the Schottky devices where each sample was held at a -10 V steady-state bias and the transient response was measured after a 10 ms injection pulses at zero-bias between 50 and 400 K. Each measurement consisted of 70 averaged transients to remove Gaussian noise and improve subsequent exponential fitting. A single trap signature is observed in the DLTS spectra

calculated with a 24.5 Hz rate window shown in Figure 47(Left). From the Arrhenius plot on the right side of Figure 47, the trap depth was found to be $0.62\ eV$ below the conduction band and has a capture cross section of $3.8 \cdot 10^{-15}\ cm^2$ for all three samples.

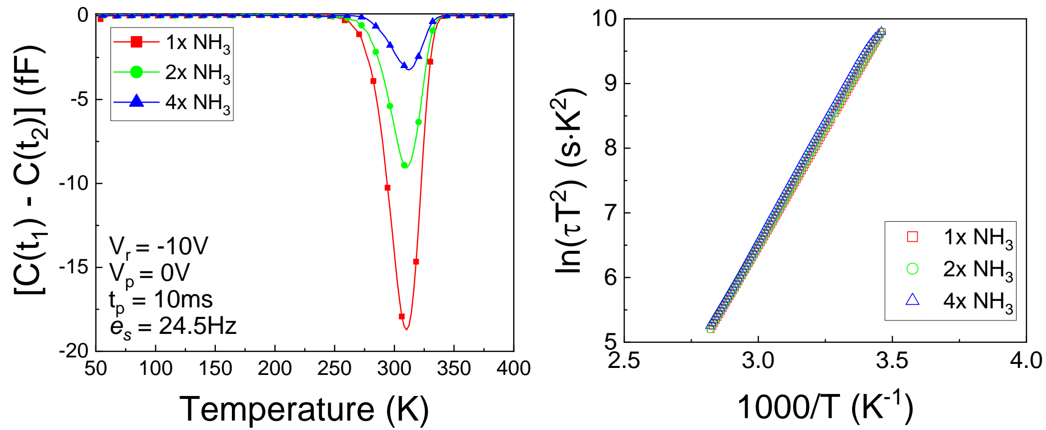

Figure 47. (Left) DLTS spectra calculated with a 24.5 Hz rate window and (Right) Arrhenius plot for the 1x, 2x, and 4x NH_3 samples.

From the total change in capacitance after a probing pulse, the density of the trap in each samples was calculated according to Equation (86). It was found that the concentration of the $E_C - 0.62\ eV$ trap decreased with the increase of ammonia so that the extracted values are $3.26 \cdot 10^{14}$, $1.75 \cdot 10^{14}$, and $0.64 \cdot 10^{14}$ for the 1x, 2x, and 4x NH_3 samples respectively.

To probe deep level traps with binding energies larger than 1 eV from either the conduction of valence band, steady-state (SSPC) and transient (DLOS) optical response techniques were performed. The samples were illuminated with a 300W Hg-Xe lamp coupled into a 0.3 m monochromator with a computer-controlled mode sorting filter on the output. The optical intensity over the wavelength range was normalized with a calibrated computer-controlled ND filter, and the resulting light was coupled into the sample with an optical fiber positioned at an oblique angle. A shallow trap filling pulse of 0 V for 10 s and a subsequent 30 s at a -10 V steady-state bias in the dark was deemed sufficient in minimizing the effects of thermal emission/capture prior to the shutter opening.

In Figure 48(Left), the changes to the steady-state capacitance signal can be observed over the rage of incident optical energies from 2.3 to 3.5 eV. The onset of increased signal implies that the optical energy of the impinging monochromatic light is large enough to induce captured charge emission into either the conduction or valence band. The magnitude of this onset corresponds to the concentration of the emitted trap where positive onsets indicate that electrons are emitted from the deep level into the conduction band and vice-versa for hole emission. All of the detected traps came from carrier emission from the defect level into the conduction band. The SSPC signal has been normalized according to Equation (86) along with the value of effective free carrier concentration (N_D) extracted from room temperature CV measurements.

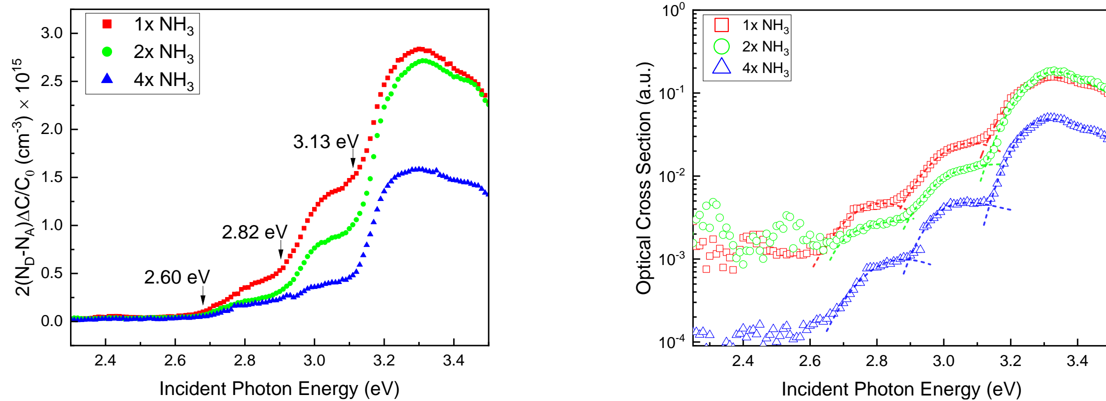

Figure 48. Room temperature (A) steady-state photocapacitance spectra and (B) DLOS optical cross section spectra for the 1x, 2x, and 4x NH_3 samples.

On the right side of Figure 48, the optical cross-section, calculated from the slope of the capacitive transients is shown for each sample. Typically, the simpler minima-to-minima transition model (Lucovsky model) is used to fit the optical cross-section data and extract the characteristic trap depth energy however fitting each region with the iterative L-M fitting procedure produced inaccurate results for all fitting ranges. Therefore, the energy values for trap depth (ΔE_t) shown on the SSPC plot were calculated from fitting parts of the optical cross section with the Chantre-Vincent-Bois model shown in Equation (68). Results from the best fit are shown as dashed lines with the same color as the corresponding samples experimental data in Figure 48(Right). The values extracted for each of the observed deep level traps from SSPC measurements are summarized below in Table 7. Additionally, the change in concentration is visualized in the plot shown in Figure 49.

Table 7. Summary of the deep level trap concentrations from DLTS and SSPC measurements on the 1x, 2x, and 4x NH_3 samples.

	Trap Concentration (10^{14} cm^{-3})			
Sample	$E_C - 0.62\ eV$	$E_C - 2.6\ eV$	$E_C - 2.82\ eV$	$E_C - 3.13\ eV$
1x NH_3	3.26	4.30	8.88	14.5
2x NH_3	1.75	2.29	6.96	17.8
4x NH_3	0.64	2.27	1.63	11.2

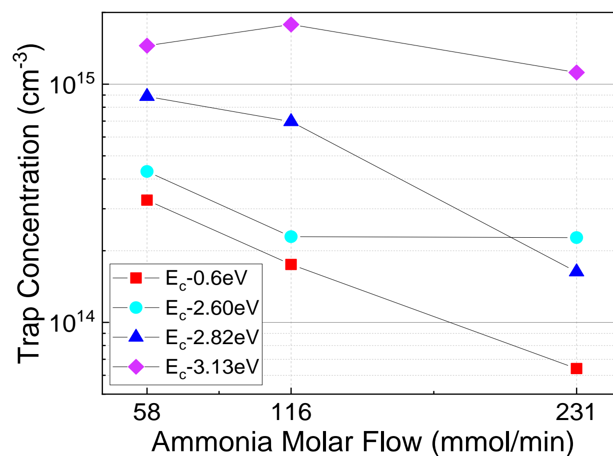

Figure 49. Trap concentration for the traps observed by DLTS and SSPC measurements on the 1x, 2x, and 4x NH_3 samples.

It is considered that the traps reported here by DLTS and DLOS are the same as those reported previously on the variable TMGa sample with the exception of the E_C-2.3 eV deep level. Therefore, the discussion of each trap can be found in Section 3.3.4. Presently, it is unknown what causes this slight energy level deviation between the two sample sets.

From the results of trapping concentration dependence on ammonia molar flow, exciting outcomes can be observed. First, the ubiquitous 0.6 eV trap reported in GaN layers, is shown to decrease proportionately to with the increase of ammonia molar flow. Because no change in the trap concentration was reported in the TMGa varied sample set (Table 4), it is presumed that carbon is indeed not the primary impurity which causes fluctuations in the observed density and that the varying ammonia flow reduces the incorporation of other defects. This trap has been attributed as one of the primary causes of current collapse in lateral AlGaN/GaN HFETs when located in the buffer [43] thereby we have revealed a method by which this trap density can be drastically lowered. Next, the E_C-2.3 eV trap is not observed in either the 1x, 2x, or 4x NH_3 samples. It is likely that this is caused by the higher quality growth on bulk GaN substrates compared to the TMGa varied sample set, which was grown on sapphire. Therefore, the argument that the presence of this defect is associated with nitrogen vacancies around threading dislocations is strengthened. Considering the E_C-2.60 and 2.82 eV defects are the same as those previously discussed at E_C-2.70 and 2.90 eV respectively, it can be inferred that by increasing the ammonia flow reduces the concentration of hydrogenated gallium vacancies. The competition for the nitrogen site which is assumed to limit incorporated carbon may also affect the unintentional incorporation of hydrogen from the TMGa molecule. However, the cause of invariance of the EC-2.6 eV trap concentration when increasing the ammonia molar flow from 116 to 231 mmol/min is unknown. Finally, the E_C-3.20 defect concentration, which was previously described as forming when C_N is present (Section 3.3.4.5), only slightly increases and then decreases when ammonia molar flow is increased while maintaining the growth rate. This result is surprising and contrary to the reported decrease in carbon concentration by SIMS in Figure 45(Right). Currently, it is unknown why this trap behaves this way, and more work needs to be done to study its characteristics.

3.4.5 Reverse Leakage Characteristics in FP Structure

To correlate the effect of varying ammonia flow with the reverse leakage current, separate 1 cm^2 samples were cleaved from the 1x, 2x, and 4x NH_3 samples and mesa-isolated Schottky diodes with a SOG surface passivation and field-plate were fabricated. The processes was designed to minimize surface conduction and distribute the electric field vertically through the sample by first etching a mesa structure with ~45° sidewalls by pattern transfer according to Section AC.3. Next, an SOG film was deposited and wet etched according to Sections AC.1 and AC.2, respectively. Finally, a Ni/Au (50/200nm) Schottky contact and field-plate was deposited by e-beam. The reverse IV characteristics were measured by sourcing high-voltage from a Stanford Research SR350 and measuring the induced current with a Keithley 2400 in series. The measurement results are shown below in Figure 50.

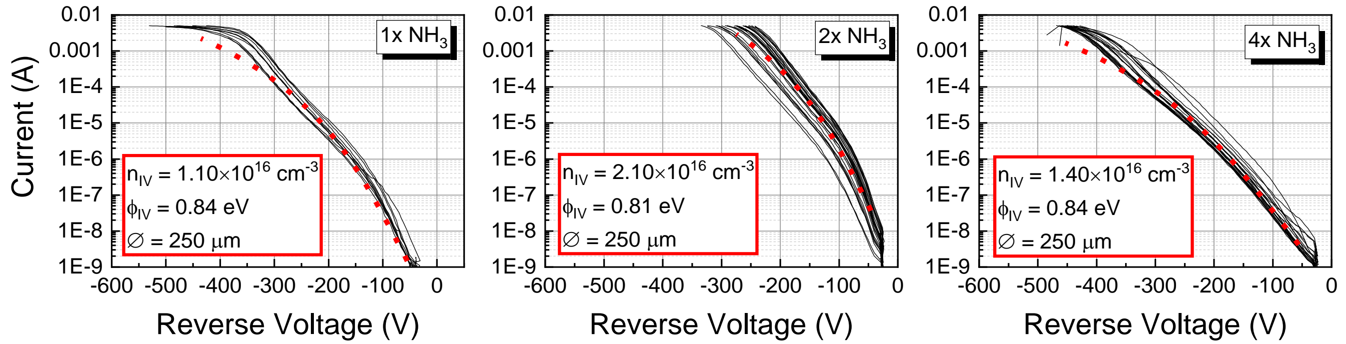

Figure 50. Results from reverse IV characterization of the field-plated Schottky diodes fabricated on the 1x, 2x, and 4x NH_3 samples.

The results are surprising in that there is no clear trend observed with respect to the increased ammonia molar flow rates. However, fitting a characteristic IV curve from each sample with the reverse thermionic field emission model reviewed in Section 2.3.3 reveals that the reverse behavior is highly dependent on the interface Schottky barrier height. In Figure 50, simulated TFE IV characteristics are displayed as a red dashed line while the parameters that produced the best fit are shown in the inset. The estimated free carrier concentration and reverse barrier heights are in very good agreement with that extracted from CV and forward IV measurements, respectively. It can be concluded that the fabricated structure was capable of removing perturbation from surface states and e-field crowding. In order to observe bulk-dependent reverse characteristics and achieve an avalanche capable device, a PN diode structure is required. Here reverse leakage current would be less coupled to the interface properties and the reverse tunneling current, which depends on the drift layer quality, could be studied.

3.4.6 Conclusion

Capacitance versus voltage, deep level transient spectroscopy and steady-state photo-capacitance techniques were used to characterize the effect that varying ammonia molar flow has on the effective free carrier concentration and observed deep level trapping behavior in a Schottky diode drift layers. With the increase in ammonia molar flow rates, it was observed that the effective free carrier concentration versus depletion depth from CV measurements was constant for each sample and only the 1x NH_3 sample showed an indication of carrier compensation. From, DLTS and SSPC/DLOS measurements deep levels at $E_C - E_T$ = 0.62, 2.60, 2.82, and 3.13 eV are revealed. It was observed that as the ammonia molar flow rate is increased while ensuring growth rate is kept at 2 μm/hr, the concentrations of the deep levels located at 0.62, 2.60, and 2.82 eV from the conduction band can be effectively lowered. However, the deep level located at 3.12 eV below the conduction band shows little dependence, contrary to the observed decrease in carbon concentration by SIMS and this level's near unanimous association with C_N. Therefore, more work is needed to understand this behavior. Finally, an optimized Schottky structure was fabricated so that reverse IV leakage characteristics could be observed. Results indicate ideal TFE behavior and thus are not related to the bulk properties. The samples will need to be regrown with a p-type layer so that PN diodes can be fabricated.

4 References

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5 Accomplishments

Gallium nitride material quality and process capability has come a long way. Progress has allowed the commercialization of lateral power devices; however, these devices suffer from reliability issues and the inability to completely take advantage of the material's capability through vertical implementation. Researching and discovering the material properties or fabrication processes which induce non-idealities in GaN-based devices will lead to higher voltage, lower loss, and smaller power semiconductor devices. First, in this work, we have explored a method to quantify the lateral barrier height variability at a metal-semiconductor interface and subsequently applied this method to Schottky diodes processed under different conditions. It was found that the normally applied Gaussian distribution used to describe inhomogeneity at the MS interface was inadequate and that by applying a modified log-normal distribution, the lateral variability along with the interface's voltage dependence could be accurately described. Applying this method to Ru/GaN Schottky diodes annealed at increasing temperatures in air revealed the variation in lateral inhomogeneity at the interface. Here it was shown that favorable results, linked to the low side of the distribution tail, could be achieved for samples annealed up to 500°C and that a deep level trap around $E_C - E_T = 0.57\ eV$ may be the cause of degradation at 600°C. Secondly, the effect of variable growth conditions on deep level state introduction and concentration were examined by DLTS, SSPC, and DLOS measurements. By increasing the TMGa molar flow rate, low carrier concentration drift layers could be grown at high rates however, the compensating deep level states also increased. Subsequent work revealed that the carbon concentration could be controlled by ensuring that the ammonia molar flow rate to growth rate ratio was minimized. Vertical GaN Schottky diodes were fabricated from drift layers grown under varying ammonia molar flow rates and subsequent analysis revealed that the deep level defect concentration decreased. This work highlights a path to achieving higher quality GaN films capable of material limited breakdown voltages and conductions losses. Finally, a simple field plating process was established and applied to vertical GaN diodes structures in an attempt to study the bulk properties of variably grown layers. The reverse diode currents were shown to be limited by ideal thermionic field emission therefore qualifying the usefulness of the process. Below, in the subsequent sections, the authors' contributions to the literature and Dr. Guido's lab is summarized.

5.1 Publications

As part of my work at Virginia Tech I have been fortunate to contribute to efforts that have been novel and worth of publishing. Below is a list of accepted, submitted, and in-progress work:

5.1.1 Journal Publications

- **Allen, Noah** et al. "Characterization of Inhomogeneous Ni/GaN Schottky Diode with a Modified Log-Normal Distribution of Barrier Heights." *Semicond. Sci. Technol. 34 (2019) 095003*

- Timothy Ciarkowski, **Noah Allen**, et al. *"Connection between carbon incorporation and growth rate for GaN epitaxial layers prepared by MOCVD" Materials 2019, 12, 2455*

- **Noah Allen**, Ming Xiao, et al. *"Vertical Ga_2O_3 Schottky Barrier Diodes with Small-Angle Beveled Field Field Plates: a Baliga's Figure-of-Merit of 0.6 GW/cm^2" IEEE Electron Device Letters 2019 doi:10.1109/LED.2019.2931697*

- Jingshan Wang, Chris Youtsey, Robert McCarthy, Rekha Reddy, **Noah Allen**, Louis Guido, Jinqiao Xie, Edward Beam, and Patrick Fay, *"Thin-film GaN Schottky diodes formed by epitaxial lift-off" APL* 110.17 (2017): 173503.

- Kevin T. Chern, **Noah P. Allen**, et al. "*GaInN/GaN solar cells made without p-type material using oxidized Ni/Au Schottky electrodes.*" *Materials Science in Semiconductor Processing* 55 (2016): 2-6.

- P. D. Nguyen, M. Clavel, P. S. Goley, J. S. Liu, **N. Allen**, L. J. Guido, and M. K. Hudait, "Heteroepitaxial Ge MOS Devices on Si Using Composite AlAs/GaAs Buffer." IEEE Journal of the Electron Devices Society 3.4 (2015): 341-348.

5.1.2 In Progress Publications

- *[In Progress]* **Allen, Noah**, et al. "*Variation of Interface Inhomogeneity in Ru/GaN Schottky Diodes Annealed at Different Temperatures*"

- *[In Progress]* **Allen, Noah**, et al. "*Impact of increasing Ammonia on deep level defects in GaN grown by metal organic chemical vapor deposition*"

5.1.3 Conference Publications

- A. Hajjiah, A. Alkhabbaz, **N. Allen**, L. Guido. "*Parameter extraction of oxidized Ni/Au and Ni-only transparent conducting oxides on n-type GaN Schottky barrier diode with bias dependent barrier height and ideality factor at different temperatures*," European PV Solar Energy Conference, Amsterdam, The Netherlands, September 25-27, 2017.

- Jingshan Wang, Chris Youtsey, Robert McCarthy, Rekha Reddy, **Noah Allen**, Louis Guido, Andy Xie, Edward Beam, Patrick Fay "*Thin-film GaN p-n Diodes and Epitaxial Lift-Off From GaN Substrates*," Compound Semiconductor Week 2017, Session B8: Surfaces and Processing, Berlin, Germany, May 14-18, 2017.

- Louis J. Guido, Timothy A. Ciarkowski, Eric P. Carlson, and **Noah P. Allen**, "*Behavior of arsenic in GaN at densities ranging from isovalent doping to dilute ternary alloys*," International Workshop on Nitride Semiconductors (IWN 2016), Session F0.3 (Paper F0.3.05), Orlando, Florida, October 2-7, 2016.

- Louis J. Guido, Eric P. Carlson, Timothy A. Ciarkowski, and **Noah P. Allen**, "*Electronic properties of n-type and p-type GaN with isovalent arsenic co-doping*," 6th International Symposium on Growth of III-Nitrides (ISGN-6), Session Tu-A (Paper A12), Hamamatsu, Japan, November, 2015.

- Kevin T. Chern, Louis J. Guido, Timothy A. Ciarkowski, **Noah P. Allen**, Oleg A. Laboutin, Roger E. Welser, and Victor C. Elarde, "*GaInN/GaN-Ni/Au transparent conducting oxide Schottky barrier solar cells*." *Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th*. IEEE, 2014.

- R. M. Umbel, T. A. Ciarkowski, K. T. Chern, **N. P. Allen**, and L. J. Guido, "*Electronic properties of n-type and p-type GaN with isovalent arsenic co-doping*," 10th International Conference on Nitride Semiconductors, Washington, DC, August, 2013.

- **Noah Allen**, Preston Pinto, Aziz Traore, Masoud Agah. "*Paper-based capacitive mass sensor*." *Sensors, 2011 IEEE*

5.2 Developed Lab Systems and Software

One of the most fun parts of my time at Virginia Tech has been developing equipment and software to more quickly and accurately measure devices and analyze the generated data. Below in Table 8 is a complete list of measurement setups and completed software packages which were built and qualified to perform the work detailed in this dissertation. Additionally, some of the software and measurement setups and LabVIEW software is detailed in Appendix D.

Table 8. Summary of semiconductor characterization/analysis techniques developed to support work within the Guido Group

Device Characterization Hardware	Device Analysis Software
IV and CV Autoprobing • Keithley 2400 and HP4192A Auto. Measuring • ElectroGlass Autoprober Setup • Bottom Contact PCB Design • PS350 Rev. Bias Setup and Teflon Well Design ***MMR Cryo Probe Station Rebuild*** • CTI CryoPump Rebuild • MMR Vacuum (re)Design • Probe Station Characterization ***IVT and CVT Measurements*** • Software Design for Automatic Measurement ***Optical Characterization Measurements*** • *Mono./Spectrometer Computer Interface* • *Linear ND Filter Computer Interface* • *Optical Shutter Design and Computer Interface*	***IV(T) and CV(T)* Automated L-M Curve Fitting Parameter Extraction (Schottky/PN)** • Specific On-Resistance • Werner-Güttler Fitting, • Inhomogeneous Barrier Reverse TFE Fitting • CV Parameter Extraction (ϕ_B^{CV}, N_D, V_{BI}) • Correlation Plotting • TLM Fitting and Analysis ***(D)DLTS*** • Data Import and Filtering • Exponential/Gaussian Fitting and Parameter Extraction • Inverse Laplace Unconstrained Fitting Routine ***DLOS*** • Lucovsky/Chantre-Vincent-Bois Model Fitting • Capacitance Transient Plotting and Fitting

Appendix

A GaN Processing Techniques

A.1 Power Electronic Energy Conversion [3]

In this section a typical switching converter is examined and the governing equations are derived assuming steady-state conditions. The purpose is to understand the first-principle limits of the circuit set by the non-ideality of its components with a special focus on the switching elements. With this, a more informed decision can be had with respect to which device structure type and material properties are favorable for implementation in switching power conversion applications.

In the figure below a typical DC to DC boost converter realized with an ideal switch in addition to the equivalent circuits for each position of the single pole double throw switch. This circuit is capable of supplying a load (R) with a voltage higher than or equal in magnitude to the incoming voltage (V_g) depending on the details of switching. Analysis of this circuit can be easily accomplished by assuming the circuit is in steady-state, and thus using the small-ripple approximation ($v \approx V$ and $i_L \approx I$), inductor volt-second balancing and capacitor charge balancing.

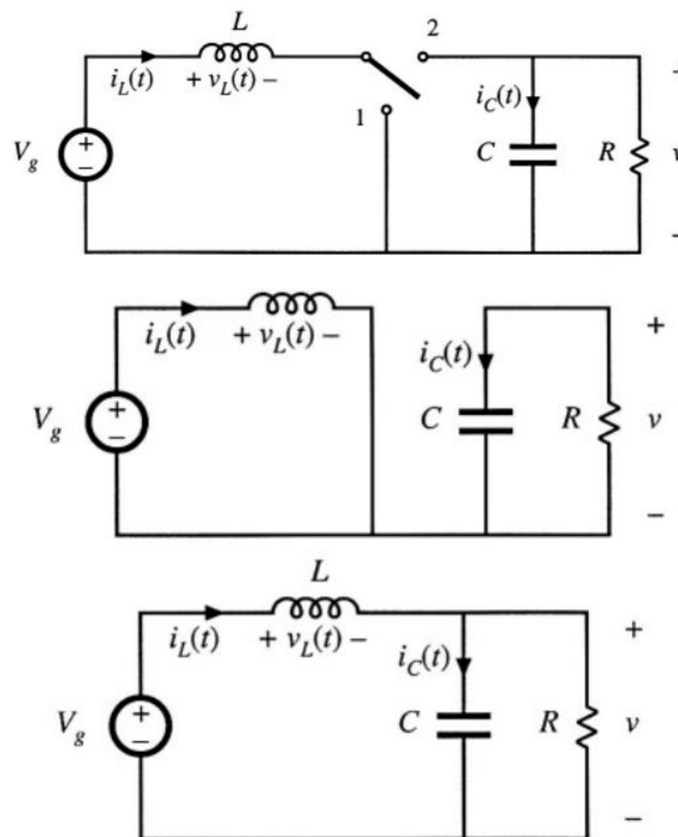


Figure 51. Basic DC/DC boost converter circuits with (Top) an ideal single pole double throw switch, (Middle) the equivalent circuit when the switch is in position 1 and (Bottom) when the switch is in position 2 [3].

In Position 1 (Figure 51 Middle), the input voltage (V_g) is applied directly across the inductor causing the current $i_L(t)$ to change linearly at a rate depending on the input voltage and inductance (L). The output voltage is equivalent to the voltage across the capacitors so that $i_c(t)$ is decreasing exponentially depending on the magnitude of the capacitance (C) and the load resistance (R). Assuming small-ripple approximation this results in the following equations:

$$v_L = V_g \tag{88}$$

$$i_C = -\frac{V}{R} \tag{89}$$

In Position 2 (Figure 51 Bottom), the voltage across the inductor is inverted, inferred from assuming volt-second balance in the inductor, causing a linear change in $i_L(t)$ but with an inverted slope when compared to its state in Position 1. This current is then split across the capacitor and resistor branches so, assuming small-ripple approximations, the resulting equations are:

$$v_L = V_g - V \tag{90}$$

$$i_C = I - \frac{V}{R} \tag{91}$$

Equating the total volt-second applied to the inductor to zero over one switching cycle the following expressions are obtained:

$$\int v_L(t)dt = (V_g)DT_s + (V_g - V)D'T_s = 0 \tag{92}$$

$$V = \frac{V_g}{D'} \tag{93}$$

Where T_s is the switching period and defined as $T_s = \frac{1}{f_s}$, D is the ratio of T_s the circuit spends in Position 1 and D' is the ratio of T_s which the circuit spends in Position 2 nothing that $(D + D') = 1$. From this analysis, we see that the output voltage increases when the circuit spends less time in Position 2. This makes sense because when the switch is in Position 1 the circuit is charging the inductors current and in Position 2 that current is dumped into both the load and capacitor effectively charging the output voltage. The DC conversion ratio is shown below in Figure 52 where $M(D) = V/V_g$.

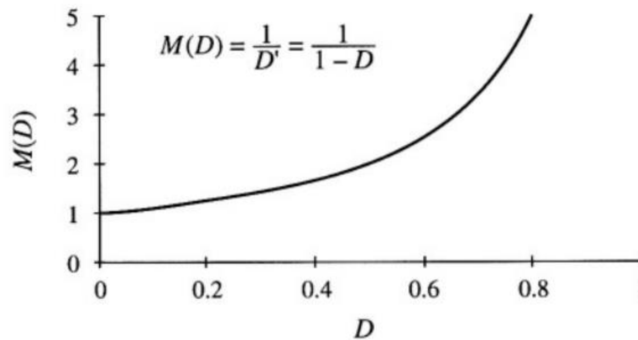


Figure 52. DC conversion ratio for an ideal boost converter [3]

Although named a DC/DC converter the DC output will be slightly modulated with an AC signal of frequency f_s. The output ripple can be calculated by first deriving the current waveform through the inductor and then relating it to the voltage across the capacitor noting that the load will be in parallel with a capacitor (C). In Position 1, the inductor current rises linearly and in Position 2 decreases linearly about the average current I as:

$$Position\ 1{:}\ \frac{di_L(t)}{dt} = \frac{V_g}{L} \quad (94)$$

$$Position\ 2{:}\ \frac{di_L(t)}{dt} = \frac{V_g - V}{L} \quad (95)$$

The change in current through the inductor can then be found from multiplying the length of time which the inductor is charging and discharging by its respective slope, thus:

$$\Delta i_L = \frac{V_g}{2L} DT_s \quad (96)$$

Applying a similar process to the capacitor but examining its voltage instead of current we get:

$$Position\ 1{:} \frac{dv_C(t)}{dt} = -\frac{V}{RC} \quad (97)$$

$$Position\ 2{:}\ \frac{dv_C(t)}{dt} = \frac{I}{C} - \frac{V}{RC} \quad (98)$$

with the change in output calculated as:

$$\Delta v = \frac{V}{2RC} DT_s \quad (99)$$

Equations (96) and (99) are significant because they can be used to dictate the required inductor magnitude, capacitor magnitude, and switching speed ($1/T_s$) to achieve a tolerable AC perturbation on the output DC voltage.

The above analysis has been completed assuming loss-less components; however, this is rarely the case considering both the capacitor and inductor elements have internal series resistances and an ideal switch does not exist. In place of the single pole double throw switch, a transistor and diode network has been shown to adequately complete the task of switching the circuit between its two states. The boost converter circuit in Figure 53 (Top) below shows the typical arrangement of transistor and diode to accomplish proper switching.

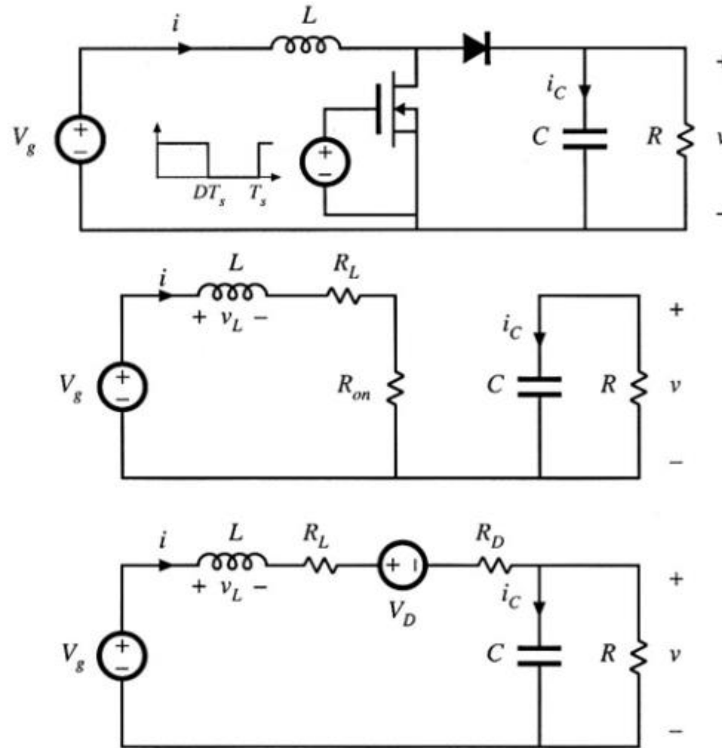


Figure 53. (Top) Boost converter circuit similar to that shown in Figure 51 but with a transistor/diode implemented switch. Additionally, the equivalent circuit for (Middle) Position 1 and (Bottom) Position 2 are shown with switch and inductor non-idealities [3].

In the equivalent circuits shown in Figure 53 representing Position 1 (Middle) and Position 2 (Bottom) of the switch, additional components have been added to model the effects of inductor copper loss (R_L), transistor on-resistance (R_{on}), diode on resistance (R_D), and diode voltage drop (V_D). Similar analysis as shown above can be applied and results in a transformation of Equation (93) to:

$$V = \left(\frac{1}{D'}\right)\left(V_g - D'V_D\right)\left(\frac{D'^2 R}{D'^2 R + R_L + DR_{on} + D'R_D}\right) \quad (100)$$

Additionally, because the circuit is no longer ideal the efficiency must be considered. The efficiency is expressed as $\eta = P_{out}/P_{in}$ so that:

$$\eta = \frac{1 - \frac{D'V_D}{V_g}}{1 + \frac{R_L + DR_{on} + D'R_D}{D'^2 R}} \quad (101)$$

Below in Figure 54 the effect on circuit efficiency due to varying the semiconductor non-idealities specifically the (Left) transistor on-resistance, (Middle) diode series resistance and the (Right) diode on voltage with an input of $V_g = 10V$ and a negligible R_L is calculated. It can be seen that even slight non-idealities in the semiconductor-realized switch network can have large consequences in a power conversion circuit efficiency. Ultimately this would reduce the usability of the circuit by limiting the range in which it is efficient and capable of operating properly or by requiring forward knowledge of output requirements so that circuit topology and components can be best chosen.

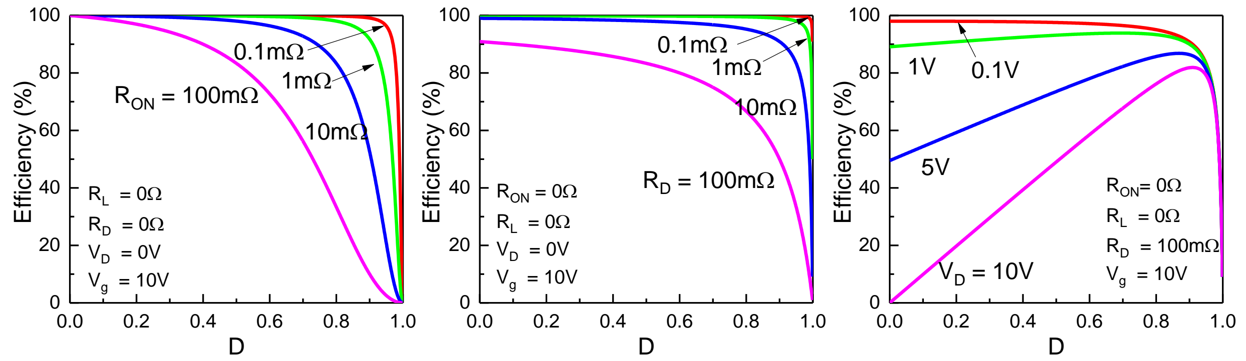


Figure 54. Calculated efficiency for a boost converter with varied (Left) transistor on-resistance (Middle) diode series resistance (Right) diode on-voltage

B GaN Processing Techniques

In this section, the processing recipes used to fabricate the electrical devices reported in this work are summarized. All devices were processed within the class 100 Mico and Nano fabrication laboratory on the 6th floor of Whittemore Hall at Virginia Tech.

B.1 Sample Cleaning

Table 9. Summary of cleaning process used for samples prior to fabrication or without any exposed metallization.

Step	Description	Notes
1	10 min Acetone Soak + Ultrasonic	Room-temperature and did not do ultrasonic if critical pattern was on sample such as metallization
2	10 min IPA Soak + Ultrasonic	Directly transferred from acetone soak, no drying. Room-temperature and did not do ultrasonic if critical pattern was on sample such as metallization
3	DI:H_2O Rinse + N_2 Dry	Samples were held directly under stream from sink and then placed on dry wipe and blown with hand drier until no liquid on front or back
4	10min Aquaregia (60mL,HCl : 20mL,HNO_3)	Mixture was performed during acetone soak and allowed to sit 20+ minutes prior to sample introduction.Tweezers also rinsed if made contact
5	DI:H_2O Rinse	Same as above but sink can be turned to higher flow if sample is patterned so that bubble are knocked off (helps when mesa exists, bubbles form in corners)
6	10min 49% HF Soak	Sample is still wet with water when introduced
7	DI:H_2O Rinse + N_2 Dry	Samples were held directly under stream from sink and then placed on dry wipe and blown with hand drier until no liquid on front or back
8	5min at 115°C Dehydrate	Hotplate is started and allowed to warm up during acetone soak. Temperature is verified with IR hand scanner.

Table 10. Summary of cleaning process used for samples with exposed metallization.

Step	Description	Notes
1	10 min Acetone Soak	Room-temperature and did not do ultrasonic if critical pattern was on sample such as metallization
2	10 min IPA Soak	Directly transferred from acetone soak, no drying. Room-temperature and did not do ultrasonic if critical pattern was on sample such as metallization
3	DI:H_2O Rinse + N_2 Dry	Samples were held directly under stream from sink and then placed on dry wipe and blown with hand drier until no liquid on front or back
4	5min at 115°C Dehydrate	Hotplate is started and allowed to warm up during acetone soak. Temperature is verified with IR hand scanner.

B.2 Photoprocess and Lift-Off

Table 11. Summary of photoresist process used to pattern reported samples.

Step	Description	Notes
1	Flood sample with HMDS	This step is only necessary if processing on a SiO2 coated sample
	>1min Bake at 100ºC	
3	Flood surface with nLof2020	Use pipet to flood the sample with enough photoresist to reach ~1mm from the edge. Too much and it will wrap around back
4	45s spin at 2800 rpm	Acceleration is set to 1000 rpm/s
5	100ºC for 2min Softbake	PR can be removed in acetone prior to this step, otherwise AZ-400T is required
6	Exposure (~80 mJ)	Exposure time varies due to Channel 1 on the MA-6 varying in intensity over time
7	110ºC for 1min Post-Exposure Bake	This step is critical, check datasheet for effects of overbaking and underbaking
8	~1min in AZ-300MIF Developer	This process is very reliable if all previous steps followed. Use the reflection from background lights to see pattern development
9	DI:H_2O Rinse + N_2 Dry	Samples were held directly under LIGHT stream from sink and then placed on dry wipe and blown with hand drier until no liquid on front or back
10	10:1 (H_2O:HF) Surface Clean	Only performed if sample will be immediately metallized

Table 12. Summary of Lift-off process used.

Step	Description	Notes
1	Heat AZ-400T to 75ºC	
2	>10 min Soak in AZ-400T at 75ºC	This step takes patience and experience. If thick metal is on the sample, the lift-off and be sped up by grabbing the sample with tweezers and tapping it on the bottom of the beaker will loosen the metal.
3	5min Acetone Soak (Possible Ultrasonic)	Sample soaked in room-temperature acetone.Ultrasonic is only used if AZ-400T soak has been performed for >30min. Ultrasonic for <5 s intervals.
4	5min IPA Soak	"
5	DI:H_2O Rinse + N_2 Dry	Samples were held directly under LIGHT stream from sink and then placed on dry wipe and blown with hand drier until no liquid on front or back

B.3 Dry Etching

Table 13. Summary of dry etching process used.

Step	Description	Notes
1	Load Blank Wafer	A silicon wafer with minimal previous etch damage was loaded into the chamber
2	10min O2 Clean process 10min Noah_GaN Process 10min O2 Clean process 10min Noah_GaN Process	This process was used to clean and season the chamber. Without it the results of etching varied wildly.
3	Load sample on Fresh Carrier	Remove the previous blank wafer and load a damage-free wafer with the sample laid in the middle.
4	Run Noah_GaN	Recipe outlined below
5	Wait 5min and Unload sample	Must wait when high chlorine flow used or else chlorine condenses on the surface and creates a liquid

Table 14. Summary of dry etching process used.

Parameter	Noah_GaN (Original)	Noah_GaN (Low Damage)
Pressure (mT)	12	12
ICP Power (W)	150	250
RIE Power (W)	50	25
BCl_3 (sccm)	20	20
Cl_2 (sccm)	20	2
Etch Rate (µm/min)	~130	~30

B.4 Metal Contacts

Table 15. Summary metallization structures typically used.

Metallization Use	Metallization Stack (Thicknesses)
GaN n-Type Ohim	Ti/Al/Ni/Au (30/100/50/150nm)
GaN p-Type Ohmic	Pd/Ni/Au (30/50/150nm)
GaN Schottky	Ru/Ni/Au (10/50/150nm)
	Ni/Au (50/150nm)

B.5 PECVD Deposition

Table 16. Summary of dry etching process used.

Step	Description	Notes
1	Load Blank Wafer	A silicon wafer with minimal previous etch damage was loaded into the chamber
2	10min O2 Clean	
3	Set Heater to 350°C and Wait	This process takes some time, so begin early
4	2min Yuhao SiO_2	This process is used to season the chamber.
5	Unload wafer from chamber	Unload the silicon wafer and place sample on it
6	Load Sample and 5min Wait	Allow the sample temperature to equalize
7	Yuhao SiO_2	
8	Unload, Cool and Remove	Unload the sample from the growth chamber, stop the unload process when in the loadlock and let sit for 5min under vacuum in the loadlock to cool. Then remove sample

Table 17. Summary of PECVD process used.

Parameter	Yuhao SiO_2
Pressure (mT)	900
ICP Power (W)	175
RIE Power (W)	50
Silane (sccm)	300
NO_2 (sccm)	71
Temperature (^{o}C)	350
Growth Rate (nm/s)	~1.13

C GaN Processing Achievements

To fabricate a PN or Schottky diode, care must be taken to ensure that a fabrication step does not introduce non-ideal behavior into the device electrical characteristics. Additionally, to ensure that the maximum capabilities of the device are achieved, complex fabrication steps may be necessary. In this section the work required to implement a smooth sloped sidewall and field-plated structure in GaN Schottky diodes is summarized. First the spin-on-glass (SOG) recipe is reviewed, then the GaN dry etching procedure is reviewed and finally the SOG pattern transfer process

C.1 SOG Deposition

The inspiration for the use of the SOG as a dielectric layer in a field-plate structure came from K. Nomoto et al. [6] where they reported the first P-N diode capable of >1 kV operation. Here they showed that by adding a thin layer of SiO_2 deposited as a liquid silica mixture, the reverse leakage and breakdown capabilities of a GaN PN diode could be drastically improved without detrimentally effecting the forward IV characteristics. The application of the SOG layer after mesa etching is ideal compared to other means of SiO2 deposition since the critical surfaces will not be exposed to a harsh plasma like those experienced during PECVD growth or high temperatures like those experienced during e-beam evaporation. Since then, the process has been modified and reports where a PECVD or sputtered SiO_2 layer has been added on top of the SOG layer observe even better results [8, 9, 164, 165].

With a PN diode, by implementing a field-plate onto a mesa structure, the e-field crowding at the P/N interface near the etched sidewall can be minimized. In a Schottky diode, there is no P/N interface thus the field plate is used to minimized the electric field bunching near the edge of the Schottky contact and minimize leakage current caused by surface states. Here, it was found that almost an order of magnitude improvement in breakdown voltage could be gained by applying the SOG field-plating process to the samples reported in Section 3.4. Subsequent fitting of the reverse leakage current revealed TFE current was the dominant conduction mechanism, thereby reaching the limit of the MS interface blocking capability and validating the processing procedure.

The SOG mixture used in this work is the NDG-3000 from Desert Silicon, Inc. Application of the mixture is very similar to that of photoresist with a few key techniques required. The process is outlined in Table 18 below.

Table 18. Summary of the SOG deposition process used on both GaN and GaOx for field-plating and etch masking.

Step	Description	Notes
1	Oxide Clean Sample	The sample needs to be freshly cleaned in BOE or HF otherwise the SOG will crack and flake once baking is complete
2	Flood NDG-3000 on Sample	If sharp edges exists on the sample (etched mesa corners) bubbles can form, depositing the first drop from a height helps minimize this
3	Spin at 3000 RPM for 45s	The spin speed curve is useful to determine the thickness for layers <500µm but slower spin speeds don't produce thicker samples.
4	Bake at 100ºC for >1min	If the samples is immediately removed from the spinner and there is a delay for High Temp bake, the films will crack the low temp bake helps
5	Bake at >470ºC for 30min in N_2	Samples should be immediately placed in the annealer from the hotplate otherwise the films seem to crack more readily
6	Remove from Anneal at <100ºC	If samples are removed at high temperature, the films instantly crack and peel

In Table 18, the deposition process is summarized along with notes to help guide future users of Desert Silicons NDG-3000. The author would also like to point a few more lessons learned while using this mixture. First, evident by the included notes in the table above, it is very easy to produce cracked films if the process is not followed directly. Secondly, although thicker films are desired it was found that the full range of thicknesses listed in the datasheet's spin speed curve could not be replicated either on GaN or GaOx, therefore multiple applications of SOG were attempted. When multiple application of SOG were attempted, only two outcomes could be achieved. Either the SOG film did not change thickness due to liquefaction of the initial layer or the film cracked and flaked off. The author came to the conclusion that in order to successfully deposit thicker films, different products must be bought that are specified to produce the correct film thicknesses.

C.2 SOG Etching

It was shown in one of the reports by K. Nomoto [8] that by utilizing the SOG as an etch mask and tailoring the mesa sidewall angle, the breakdown capability could be improved further. Thus, a lot of time was spent working on a process to control sidewall angle of a deposited SOG film to be used as an etch mask in GaN and β-GaOx. In this section the processes used to etch both SOG and PECVD/SOG bi-layers is summarized.

After the SOG layer is applied, very dilute mixtures of 49% HF and DI:H_2O can be used to vertically etch the film with some degree of controllability. The etching mixtures were created by first pouring 90mL of DI:H_2O in to a Nalgene® container. Next, 49% HF is poured into a graduated cylinder and then topped off with DI:H_2O until it reaches 100mL. Finally, only 10mL of the mixture in the graduated cylinder is poured into the Nalgene® container. The etching potential is controlled by the amount of HF initially poured into the mixture cylinder before being filled with DI:H_2O. It was found that 0.5% HF mixture by volume created by pouring only 10mL of 49% HF into the graduated cylinder etched the SOG layer very slowly and controllably. When a PECVD layer was added on top, the solution could not effectively etch the thin film. In the work reported here, all wet etching was accomplished with a 2% HF mixture by volume by pouring 40mL of 49% HF into the graduated cylinder and then filling it to 100mL with DI:H_2O. An example of the visually inspected PECVD/SOG bi-layer is shown below in Figure 55 after various etching times in a 2% HF mixture.

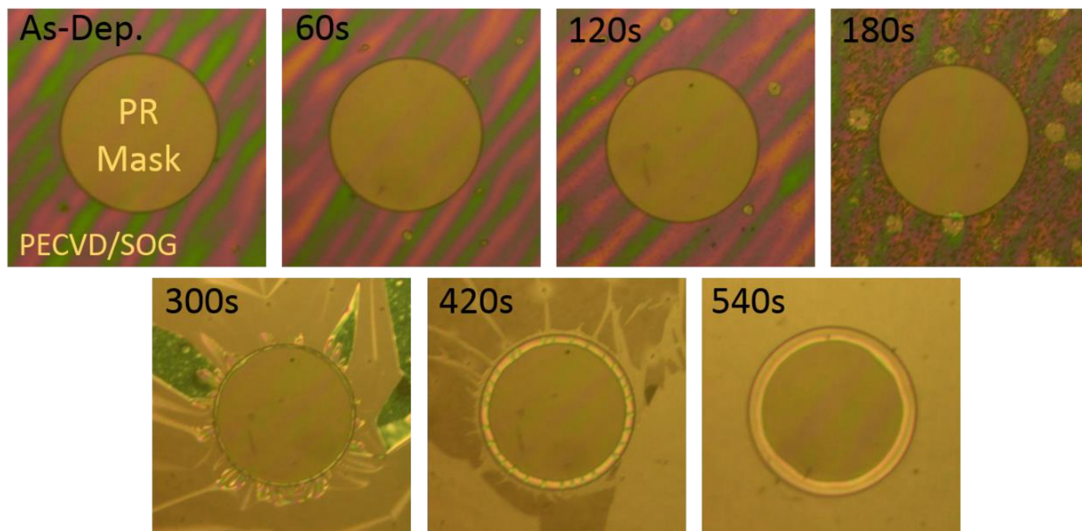


Figure 55. Optical images of a PECVD/SOG bi-layer etched in 2% HF by volume for various amounts of time.

Here optical images of the PECVD/SOG bi-layer as it is etched in 2% HF by volume with a circular PR etch mask. The green and purple streaks in the as-deposited PECVD/SOG layer are caused by the non-planar surface of annealed SOG layers. As the etching time is increased, the etching mixture makes its way through the PECVD layer at specific points and begins etching the SOG under layer more quickly. This can be observed in both the 120 and 180 second etched samples as light circles in the dielectric film. As the etching progresses, the thin layer is left (300s) and finally after 540s the film is fully removed. After 540 seconds of etching, the PR mask remains intact; however, the bi-layer around the edges has been undercut.

The SOG layer thickness under a 100nm PECVD film was varied by changing the spin speed during application. Ideally, this would create a method by which the sidewall angle could be controlled. However, from the figure below, it can be seen that no appreciable variation in the perimeter region thickness could be optically observed between the sample that were deposited at 2000 and 3000 RPM. However, it was found that by increasing the spin-speed to 4000 RPM, the film could no longer be fully etched.

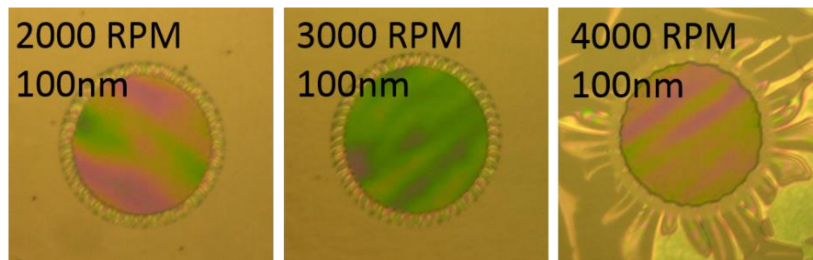


Figure 56. Optical image of PECVD/SOG bi-layer after being undercut where the SOG spin-speed has been varied.

Next, the PECVD film thickness was varied to understand its effect on the perimeter region profile of the undercut film. It was hypothesized that by varying the thickness of the PECVD deposited layer on SOG, the sidewall slope could be tailored. Below in Figure 57, the results of this test after etching are shown.

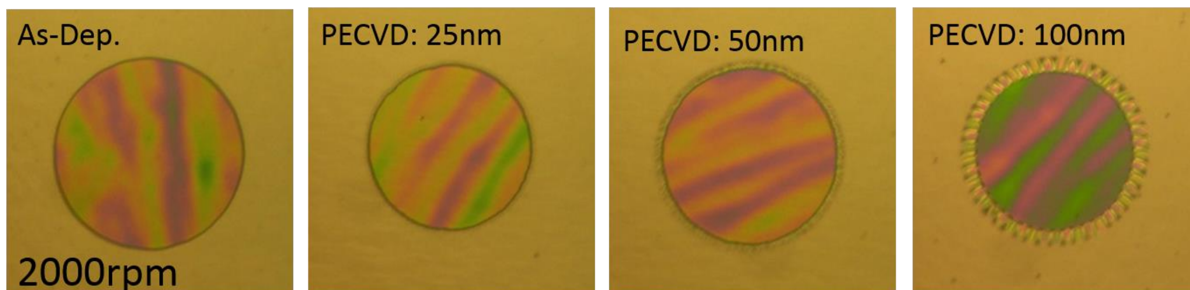


Figure 57. Etched PECVD/SOG bi-layers with varying PECVD layer thicknesses

In the SOG-only sample, only a shadow can be observed around the edges of the remaining film thought to be from a very steep sidewall. Next, in the undercut sample with a ~25nm layer of PECVD SiO_2 a very thin ring can be observed (barely) which increases in width by depositing thicker PECVD layers. This ring is easily visible in the 100nm PECVD bi-layer sample in Figure 57. To understand the physical characteristics of this thin undercut layer, a Dektak stylus profilometer was used to create a height map. The results are shown below in Figure 58.

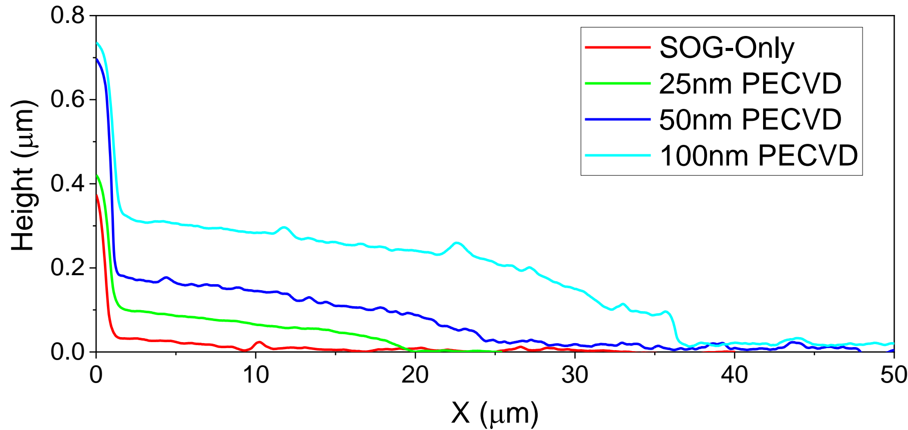


Figure 58. Surface profile of PECVD/SOG bi-layer after undercutting and PR removal. The profile shows the effect of varying PECVD SiO_2 layer thickness on the edge height.

Here we can see that as the PECVD layer thickness is increased, the height of the undercut perimeter is also increased. Although only shallow angles can be formed, this method could be used to transfer the pattern in to the underlying sample so that the mesa sidewall angle could be effectively controlled. However, due to the etch selectivity between the bi-layer and the underlying substrate, the depth at which the mesa is formed is limited by the length of the perimeter region since over-etching will cause the 90° sidewall to be patterned into the sample. Therefore much consideration needs to be given to the details of the etching chemistry and the etching time so that this does not occur.

C.3 Semiconductor Sidewall Processing

Creating sloped sidewalls in GaN is useful for both power electronic applications [8, 21] and also optical applications [166, 167]. However, care must be taken to ensure that damage to critical surfaces is not also introduced during the material removal process. In GaN, dry etching is the typical method in which surfaces are patterned. Some reports successfully observe favorable outcomes by wet etching [168] but etching times are slow unless photoenhanced [169] or performed at high temperatures [170]. Wet etching GaN has found use in damage removal after dry etching [21, 171, 172]. As far as creating a controllable sloped sidewall, reports exist but require etching chemistry not currently available here at Virginia Tech [166, 173]. Instead, it was decided that the dry etching process typically used to create 90° sidewall profiles could be tailored to improve the etch damage and use an SiO_2 mask to transfer a sidewall pattern into the GaN sample.

Prior to developing the pattern transfer recipe, it was noted that while measuring, the sample was prematurely breaking down at the mesa edge, visible through an optical microscope. Upon examination of the sample by SEM, it was found that nano-pillars formed during mesa etching was the likely cause. Below in Figure 59(left) an SEM image of a field-plated structure is shown where accidental masking during the SOG process or damage during measurement caused the underlying GaN surface to be revealed. Currently, it is hypothesized that these pillars are either caused by threading dislocations or deposition and masking of a chlorine containing molecule.

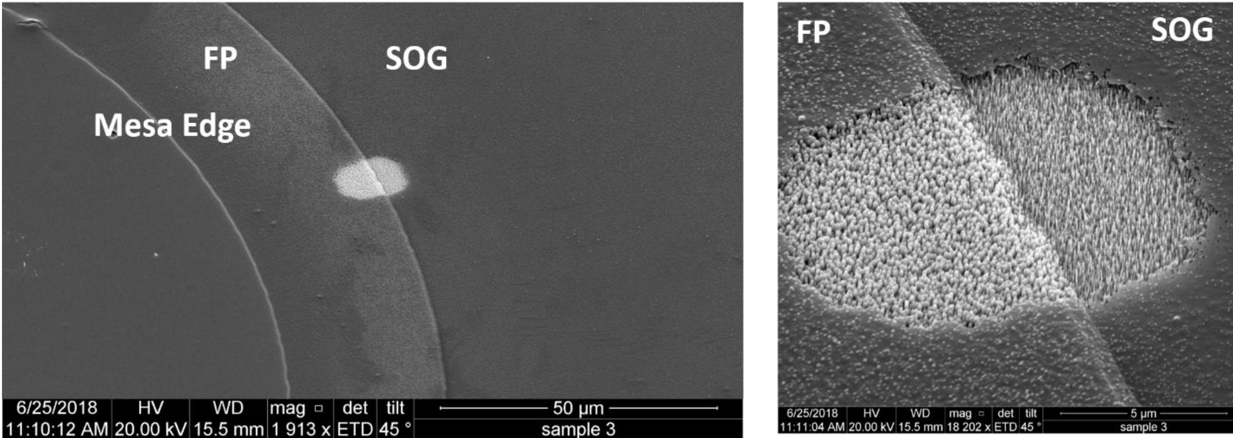


Figure 59. SEM image of a field-plated structure where the SOG has been partially removed. Here GaN nano-pillars can be observed.

Next, effort was put into optimizing the etching recipe to minimize the inclusion of these nano-pillars. To do this, GaN samples were masked with PR and the etched in Virginia Tech's TRION etcher under different conditions. Below in Table 19, the etching recipe matrix used to understand the effects of pressure, ICP/RIE power, and gas flow rates is shown. Additionally, the thick black lines between etched samples indicates that a new silicon carrier wafer was used. This was done to test whether or not contamination of the wafer could have caused the appearance of nano-pillars in the etched GaN surfaces.

Table 19. Summary of RIE etching parameters tested to achieve smooth sidewalls. Note the thick black lines indicate when a new Si carrier wafer was used.

Sample	Pressure (mTorr)	ICP Power (W)	RIE Power (W)	BCl_3 Flow (sccm)	Cl_2 Flow (sccm)	Etch Time (s)	Depth (um)	Rate (nm/min)
A	12	150	50	20	20	420	0.8929	127.5
D	12	150	50	20	20	420	0.9417	134.5
P	12	150	50	20	20	420	?	?
Q	12	150	50	20	20	420	?	?
S	12	250	25	20	20	420	?	?
T	40	250	25	20	20	420	0.22	31.4
V	12	250	25	20	2	420	0.29	41.4
X	40	350	25	20	2	420	?	?

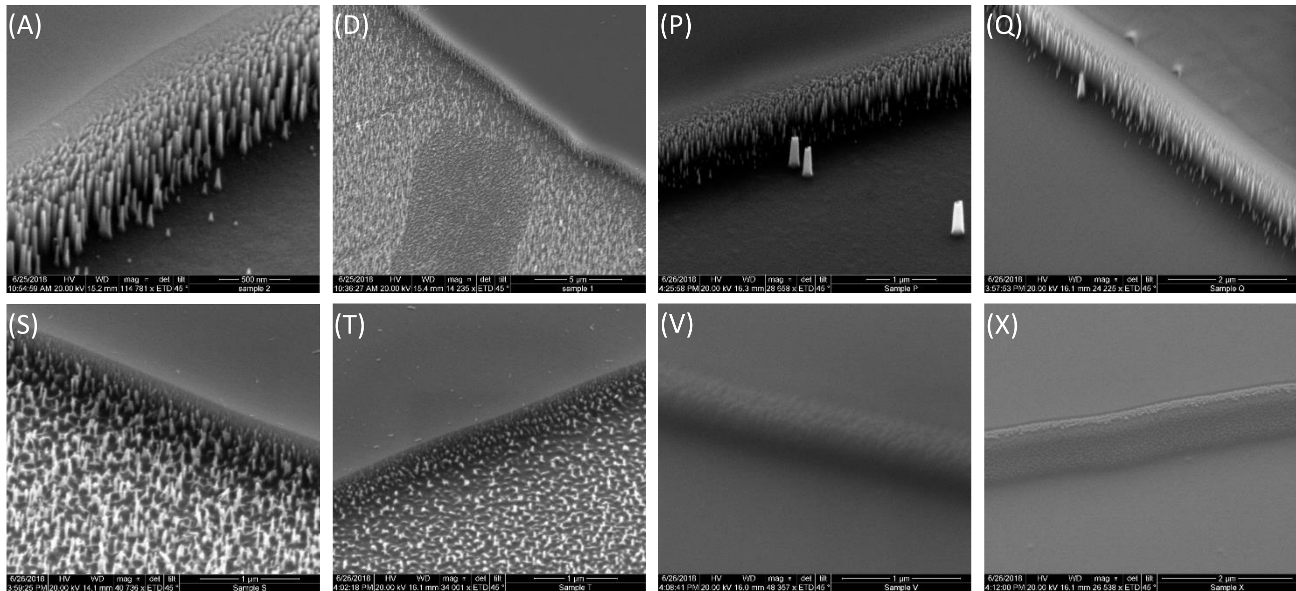


Figure 60. SEM images of mesa sidewalls formed with respective RIE process recipe according to Table 19

In Figure 60, SEM images of select samples after etching are shown. Here the nano-pillars can be clearly observed and under certain conditions, begin to lessen in density and then disappear. Below is a summary list of what was learned from these tests:

- Under the commonly used condition (A, D, P, Q), the nano-pillar density was inconsistent from run-to-run and across the sample.
- The carrier wafer seemed to have an effect on the density of the nano-pillars on the etched surface (D to P). Additionally, the damage visible by eye on the surface of the carrier wafer served as an indication of whether nano-pillars were being formed. The etched sample would have a dark hallow patterned into the carrier wafer and/or sections around the perimeter of the carrier wafer.
- Increasing the pressure and lowering the RIE power (S to T) decreases both the height and density of the nano-pillars.
- Lowering the chlorine flow rate from 20 to 2 sccm (T to V and X) had the most drastic effect and virtually removed all of the pillars. However, the etch rate dropped considerably from ~130 to ~35 µm/min.

Recipe 'V' was used for subsequent GaN etches due to its ability to remove any trace of the nano-pillars. Next, the SOG processes reviewed in the previous section was applied to both GaN and β-GaOx samples in order to pattern transfer the sloped sidewalls. However, the long sidewall was not implemented into GaN structures and only the ~45° sidewall process was used. The results of applying the pattern transfer process to a β-GaOx Schottky structure are shown below.

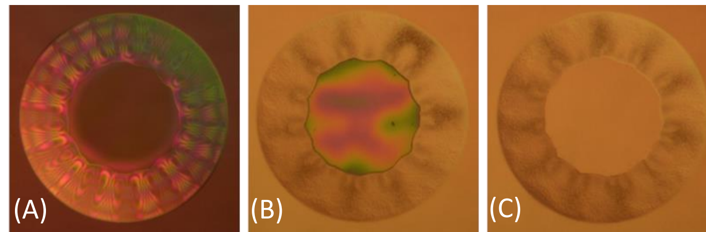


Figure 61. Optical image of SOG on β-Ga_2O_3 (A) after bi-layer undercutting, (B) after dry etching, and (C) after bi-layer wet etch removal in 49% HF.

First, the long bevel sloped sidewall process was attempted. In Figure 61, the PECVD/SOG bi-layer was first heavily undercut to ensure a long sloped sidewall could be formed. The result of dry etching the sample can be observed in Figure 61(B), where the only remaining portion of the bi-layer is the flat top of the bi-layer and a small sloped perimeter due to SiO_2 removal during dry etching. Finally, the bi-layer is removed with a 5 minute soak in 49% HF. An optical image of the final device structure with a field-plating structure fabricated with the same long bevel PECVD/SOG bi-layer undercutting process is shown in Figure 62. Additionally, the cross-section of the device is shown. Note that the initial width of the mesa was 270 µm but due to the undercutting the average width mesa top becomes ~150 µm. Thus, consideration needs to be given to the size of the mask fields.

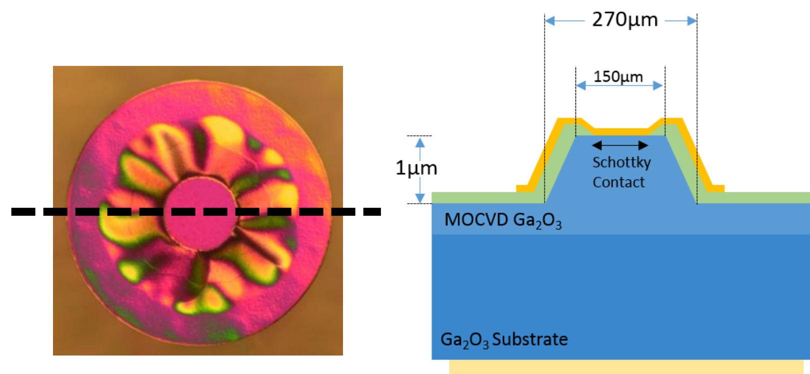


Figure 62. (Left) Optical image of a fabricated Beveled Sidewall Schottky diode on Gallium Oxide and (right) a cross-sectional schematic of the device.

Finally, a 45° process was applied to both GaN and β-GaOx Schottky samples; however, no images were taken of the fabricated GaN samples reported in Section 3.4. SEM images of the field-plated mesa cross-section are shown below in Figure 63. In this particular sample, the 45° process was applied both to pattern the mesa sidewall and crate the field-plate structure adjacent to the Schottky contact. Results from this work have been submitted in a publication through 'Electron Device Letters'.

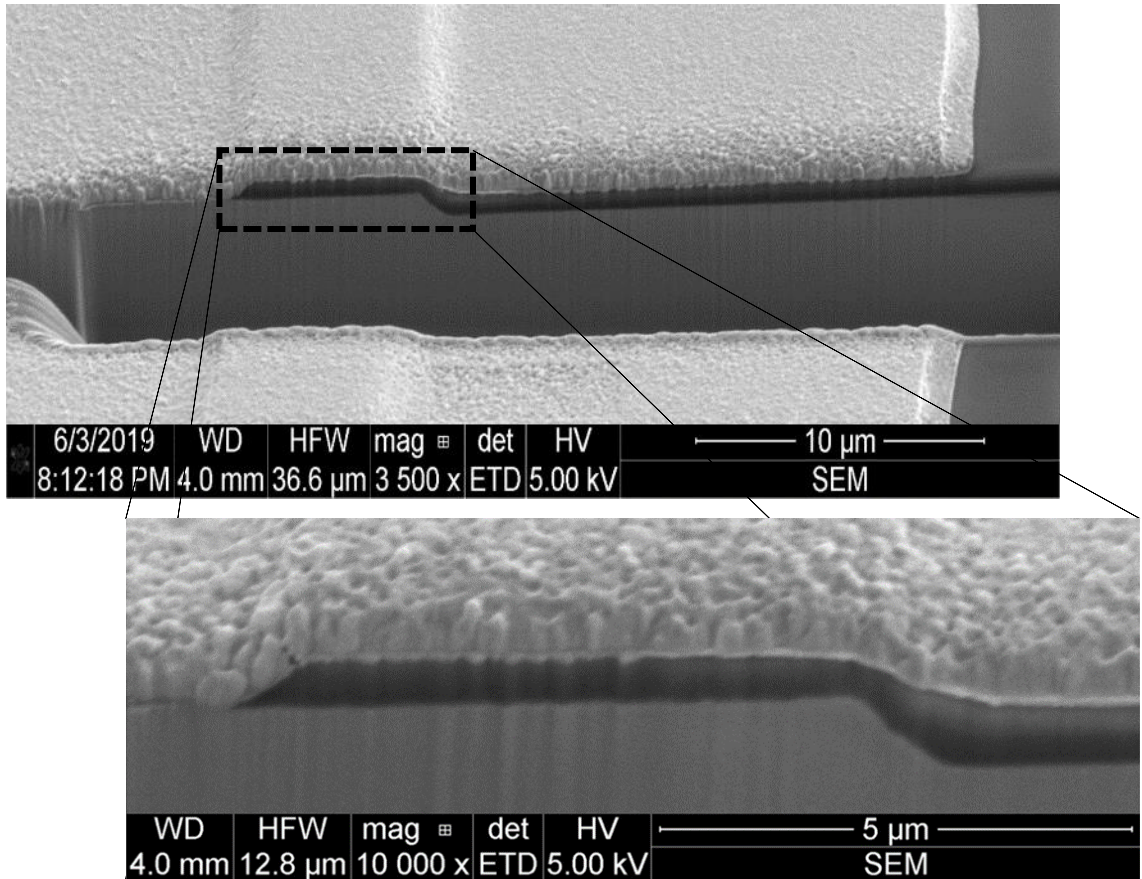


Figure 63. FIB cross-section of the pattern transfered GaOx sidewall and the fieldplate with slanted contact sidewalls.

D LabVIEW Control and Analysis Software

In order to quickly test and analyze data, a software suite was created using the LabVIEW programming language. Here, programs were built to control hardware for autonomous testing of semiconductor devices, analyze large datasets (>1 GB) quickly and save the results in a readable format for publication. This section review the programming strategy for writing the LabVIEW code and then a short summary of the capabilities of each main piece of software. If reverse engineering this software becomes necessary, much consideration should be given to Section D.1 Programming Strategy.

D.1 Programming Strategy

First it should be noted that all programming was completed in the 64-Bit LabVIEW 2014 suite, v15.3 Ni-Visa driver package, and IEEE-488.2 driver package. Executable versions of all of this software exist on the Guido Group Google Drive and the equivalent runtime versions of the three mentioned programming packages should be downloaded in order to run the '.EXE' files. **Secondly and most importantly, even erroneous data can be analyzed, it is up to the user to ensure that all conditions are met to successfully use these measurement/analysis programs.**

Each of these programs were created so that most of their processing would only be run AFTER a button push and this is why the While-Loop/Event-Structure uses on the block diagram is heavily present. The idea is that when the program starts, the variables (usually shown on the left of the block diagram) are initialized and then the While-Loop waits until the user does something such as require data be read, start a fitting procedure, or graph a type of data. Therefore if a certain feature of the measurement or analysis needs to be looked at the button or graph related to the feature needs to be traced to the corresponding event case. Inside the event case is the routine run to accomplish that specific feature. Below in Figure 64 is an example of the While-Loop/Event-Structure use.

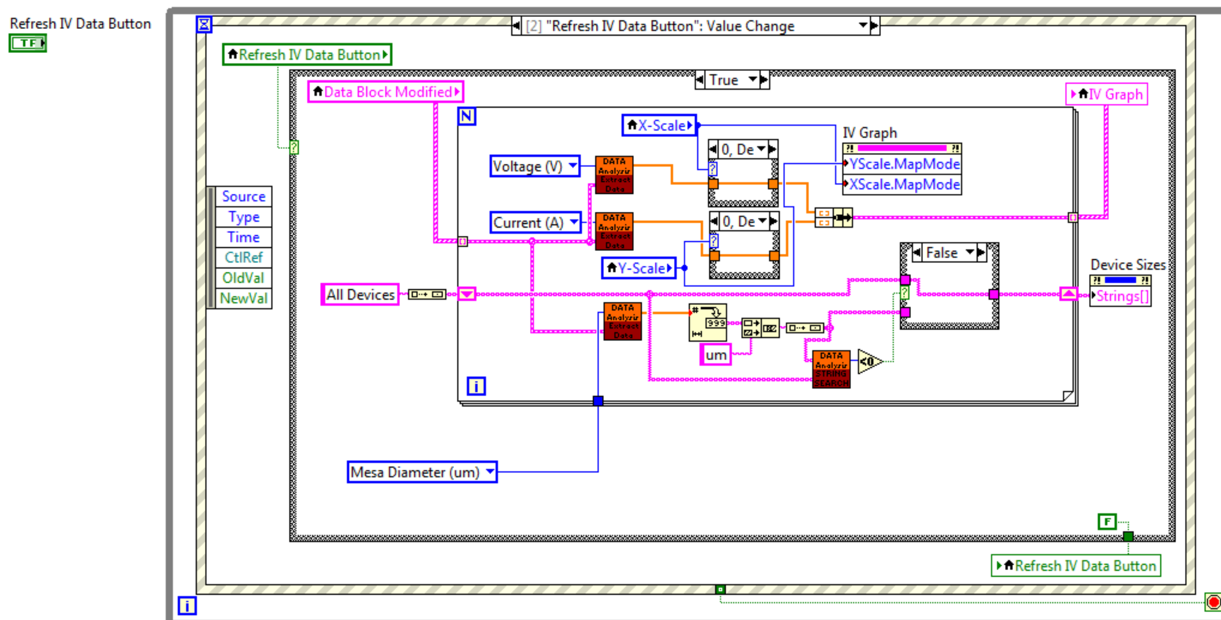


Figure 64. Example of the While-Loop/Event-Structure setup commonly used within the LabVIEW Test and Measurement suite. Here the button variable associated with refreshing the IV data is shown on the left in addition to the event case which handles the data analysis associated wih refreshing the data on the graph.

D.2 Required Data Format

In order to ensure the proper input and analysis of data to the analysis suite, it was decided that the data gathered during measurement needed to be saved in a standardized format. Thus, all data is saved into a readable Excel file with extension 'XLS' or 'XLSX' whereas DLTS and DLOS data which requires larger file sizes utilize the 'XLSB' format to save space on the hard drive. Within each of the files, the data points also need to have a specified format so that they can be easily interpreted by the LabVIEW analysis programs. The data measurement programs will only save data into one sheet of an excel file where a block of data, separated by one or more blank columns, is made up of a header, description, keyword data descriptors, and the data. The figure below is an example of IV data saved in this format.

Data Title/Summary
Details
GaN 18102611 Ni Schot 11/29/2018 4:25 PM
Voltage (V) Current (A)
Data Keywords
Data
0.003982816 1.59277E-07
0.008013709 2.88717E-07
0.012009581 4.22196E-07
0.016049204 5.50794E-07
0.020045999 6.81396E-07

Figure 65. Example of standardized data file format used to input data into LabVIEW analysis programs.

First, the 'Data Title/Summary' is used as a method to identify the material type and the device sizing for the specific sample measured. The 'Details' header is used for extra information regarding the measurement such as temperature, voltage biases during measurement, or date. The 'Data Keywords' are used as a way of identifying the type of numerical data below each keyword such as voltage, current, capacitance, or temperature. Finally, the 'Data' is the numerical data associated with a measurement.

As will be discussed in Section AD.5 Autoprober Dependent Control Software, the 'Data Title/Summary' is partially assigned during a measurement. For example, in Figure 66 below, we see a typical title summary concatenated from the user's input and the software's understanding of the current device that's being measured. The first portion of the 'Data Title/Summary' is created from the input from the user, which should be a readable text string that describes the sample being measure. Here it can be seen that the sample being measure is a Ni/GaN Schottky that has been grown with 2x Ammonia flow (NH_3) on an MCC bulk GaN wafer. Next, the device number is labeled by the auto prober program. In this example, the data being saved is from the device located in the number 2 position of the 0th row and 0th column unit in the Top Left quadrant. Additionally, the size of that device as defined by a Mask file is added and here the device has a Schottky contact diameter of 73 µm and a mesa diameter of 93 µm. Finally, if the user would like to perform multiple measurements on the same device, for example a forward bias sweep and then a reverse bias sweep IV measurement, the 'Additional Comments' section on the IV measurement

software allows the addition of a measurement designator. Here the user has used the sting 'FWD' to signify that a forward bias measurement is being taken.

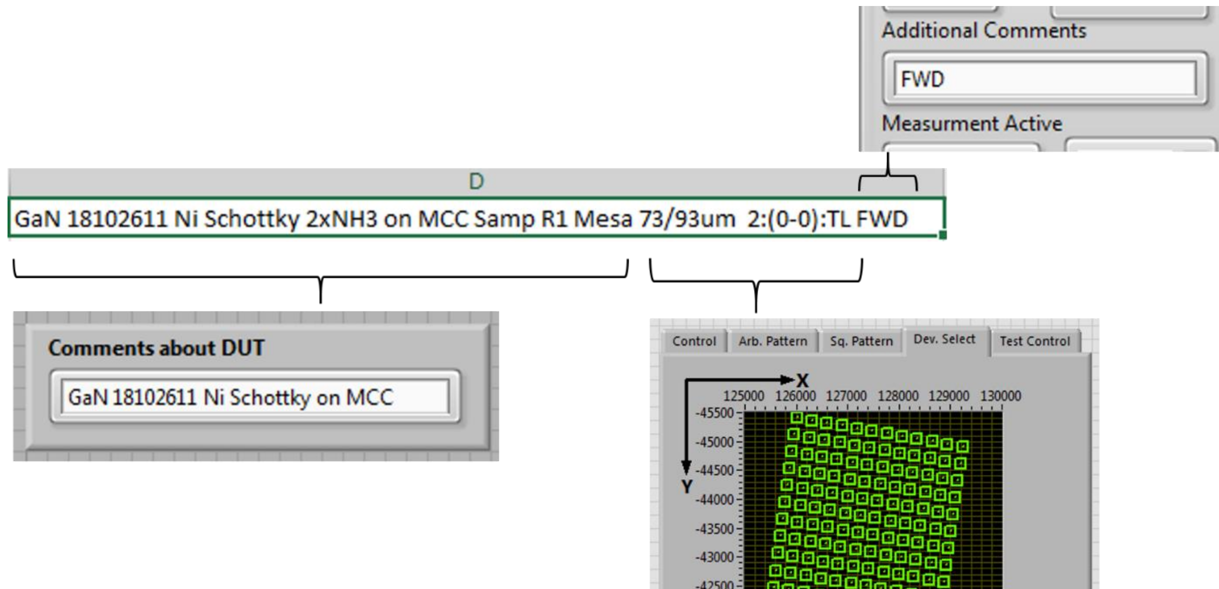


Figure 66. Example of how the 'Data Title/Summary' is created.

Within this 'Data Title/Summary' string, there are a few KEYWORDS that are required for the analysis software to recognize what is being measured. First, the use of 'GaN' signals the program that the material constants associated with gallium nitride such as effective mass and dielectric constant should be used. Secondly, the sizing is specifically written to be recognized by the analysis software as "(minorSize)/(majorSize)um" where the two different sizes can be used to specify a Schottky diode that may have a Schottky contact diameter and a mesa diameter. An example of the usefulness can be seen when analyzing a P-N diode where normalizing by the mesa area should result in the overlap of JV measurement data for a given sample unless the current is limited by the minor size (p-type ohmic contact). The user would thus have enough information to normalize by either. Finally, the location of the device is used both as a historical record of a specific device on a sample and as a means of plotting spatially varying data such as free carrier concentration or barrier height data in a contour or 3D plot.

The 'Details' portion of the data file is typically used so that a user can look at the date a device was measured; however, in other measurements where many variables can be set, this cell acts as a place to record under which conditions the data was measured. An example of this is in the large data files used to record DLTS data. Each transient is measured under a specific set of parameters at a set of temperatures; however, there are instances where its useful to keep the temperature stable and vary one of the many parameters. An example of this, data is shown below in Figure 67.

Temp:299.826/Plen:1.00E-6/Pamp:0/Pss:-5/Pper:720E-3/Pnum:50/Stim:3E-1/Srat:100000/Cinf:1.0447401003579877E-11/Date: 1/30/2018 7:11 AM

D	E	F	G	H
GaN 1607	Temp:299	Temp:299	Temp:300	Temp:300
Time (s)	Capacitan	Capacitan	Capacitan	Capacitan
0.00003	1.02E-11	1.02E-11	1.02E-11	1.02E-11
0.00004	1.02E-11	1.02E-11	1.02E-11	1.02E-11

Parameter	Value
Temperature	299.826 K
Pulse Length	1 µs
Pulse Amplitude	0 V
Pulse Steady-State	-5 V
Pulse Period	720 ms
Number of Pulses	50
Trans. Sample Time	300 ms
Sample Rate	100 ksps
C(∞)	10.4474.. pF
Date	1/30/2018 7:11am

Figure 67. Example where the 'Details' cell is used to save data other than just the measurement date and time. Here one transient of a DLTS measurement taken at a single temperature with varying pulse widths is shown.

Finally, the data column keywords are required for the analysis programs to understand what data is being interpreted. In Figure 65, the measurement produced two columns of data, voltage and current whereas in Figure 67 the varying pulse measurement produced a time and capacitance dataset. If the following keywords are not within these columns, the data cannot be accurately interpreted.

Table 20. List of 'Data Keywords' used to identify type of data being analyzed

Data Type	Keyword (not case sensitive)
Voltage	'volt' or 'bias'
Current	'curren'
Temperature	'temper'
Capacitance	'capac'
Frequency	'Freq[0-9]'
Imaginary Mag.	'|Z|'
Imaginary Admit.	'|Y|'
Imaginary Phase	'theta'
Time	'time'

D.3 IV-T, CV-T and TLM Analysis

Because IV-T, CV-T and TLM measurements are the best ways to analyze the capabilities of a device in an electrical circuit, a standardized analysis program was necessary to quickly import, filter, fit, analyze and export the data. The program reviewed here was initially written in 2010 as a way to analyze Schottky IV data by copying and pasting excel data as a string and using sliders to fit portions of the measured data. Since then, the program has grown to incorporate complex importing methods, non-linear fitting algorithms, and specialized exporting tools which allow rapid analysis of large data sets. In this section, the capabilities of the 'Data Analysis.VI' is reviewed where the Excel importing process is reviewed and then each tab from the front panel shown in Figure 68 is summarized.

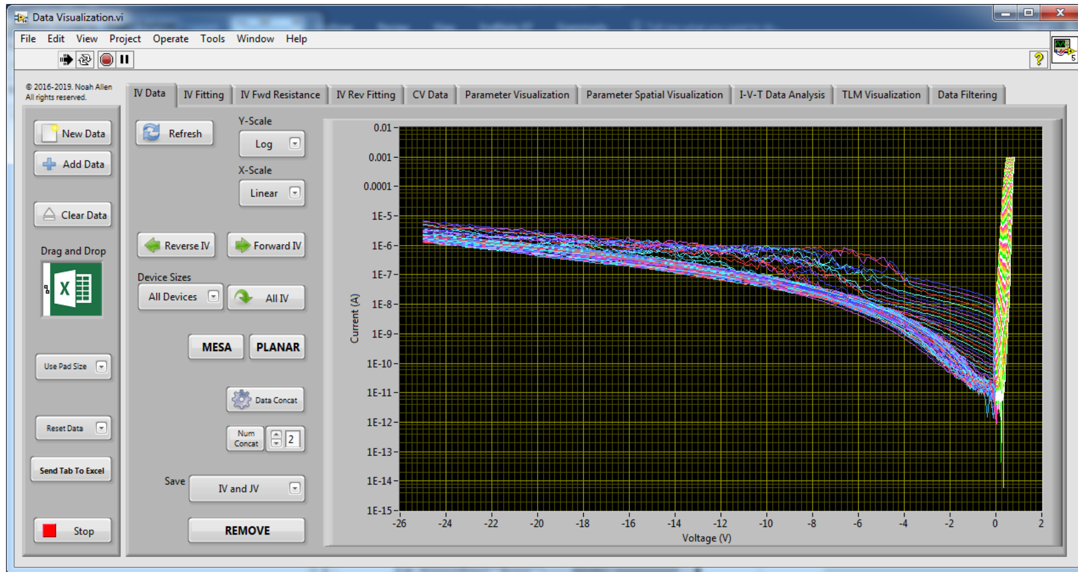


Figure 68. 'Data Analysis.VI' program used to import, analyze and export IV and CV data take from Schottky diode, PN diode and TLM structure at room temperature and variable temperatures.

D.3.1 Excel Data Importing

One of the major achievements of this software was the development of a set of programs used to quickly import all of the data in an Excel sheet. Here, LabVIEW's ActiveX toolbox was used to control Excel programmatically with only the filename needed. When a file has been specified, the software first opens the file and reads the list of sheets with available data, skipping those with only chart data. If a sheet isn't specified to import the data from, the program will pop-up a dialog asking the user to select which sheet data should be read from. Once selected, the program will find the highest column and row with data and read the sheet as a string matrix. Next, each column is indexed and all of the empty columns are identified and the matrix is segmented into smaller blocks of data. From here, block is analyzed and imported into a structure based on the keywords and cell structure detailed in Section D.2. This structure serves as the point where all other analysis tools can import and analyze data from. The program designed to parse the string matrix into the central LabVIEW structure variable named 'Data Block Array' is shown below in Figure 69 with example data.

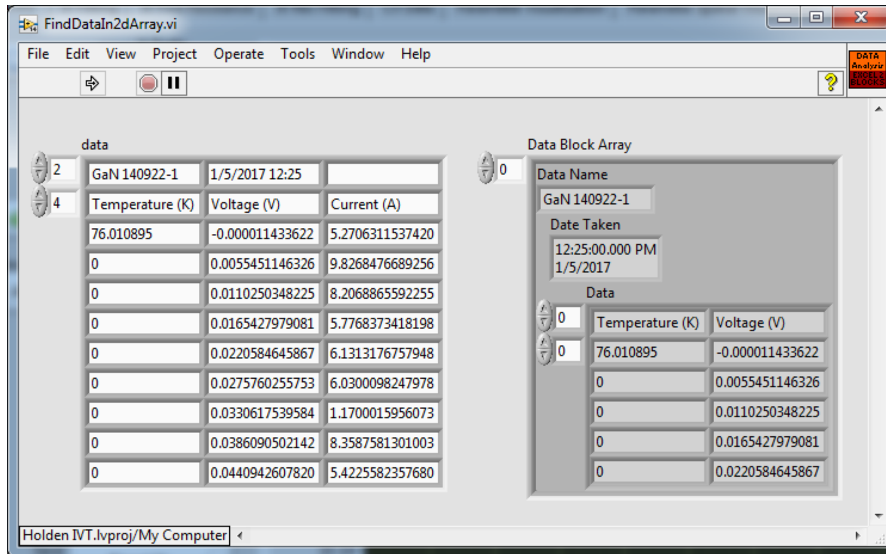


Figure 69. Example of the input string matrix imported by the Excel library which is then converted into a LabVIEW structure which is used as a jumping off point for all analysis tools to read from.

D.3.2 IV Data Tab

The usefulness of the 'IV Data' tab is the ability to read the current versus voltage characteristics from the 'Data Block Array' variable and plot the data. From here the 'Remove' button can be highlighted so that by clicking or dragging the mouse on the IV Plot certain curves can be removed from subsequent analysis methods. Additionally, the buttons on the left of the IV graph allow the user to systematically filter the data by the forward or reverse characteristics, the structure (planar or mesa) or device size by selected the appropriate size from the dropdown.

It is often necessary to concatenate the forward and reverse IV characteristics of a single device, thus the 'Data Concat' button can be used to automatically find data taken from the same device and concatenate the values. The data can also be concatenated by number, were the number next to the 'Num Concat' button is used as a grouping size. Finally, the 'Save' dropdown list is used to specify which type of data is saved once the 'Send Tab to Excel' button is pressed.

D.3.3 IV Fitting

The IV fitting tab is useful to extract barrier height, ideality factor and series resistance from experimental data on Schottky diodes. Additionally, fitting can be applied to PN diodes to extract values however this feature is currently preliminary. First, the user selects the model with which to apply to the data. The IV data which is currently present on the graph in the 'IV Data' is what is imported for further analysis. Therefore it is up to the user to ensure only good forward IV data is analyzed by filtering curves with the 'Remove' button highlighted or simply pressing the 'Forward IV' button on the 'IV Data' tab. Once the data is imported into the 'IV Fitting' tab, the user must hand fit the first diode IV characteristics. By pressing the 'Approx. Fit Param.' Button, a new window will popup depending on which model is selected. From here the user can vary input parameters into a non-linear fitting algorithm until a decent representation of the data is found. Clicking the 'Attempt Fit' button will vary the input parameters until the coefficient of determination (R^2) is minimized. The input parameters can be varied again and the fitting repeated until the model adequately represents the data. Selecting the 'Accept' button will transfer the fitting parameters back to the 'Data Analysis.VI' and the 'Auto Fit' procedure can be attempted. Once selected the program will iterate through the remaining device characteristics, using the previous best

fitting parameters as seed values for the fitting algorithm to fit the next device characteristics. It is likely that the auto fitting procedure will fail at which point the user can try to hand fit the data or remove it entirely and attempt to auto fit again. The point range scaling is a method usually used for temperature variation data where the range of the data values which are fit are linearly changed from a starting device, to a final device. This is useful for data which has a range of data not compatible with the fitting algorithm but the range varies linearly between successive IV curves.

D.3.4 IV Fwd Resistance

The 'IV Fwd Resistance' tab is simply used to import the forward IV characteristics from the 'IV Data' tab and calculate the specific-on-resistance from the running derivative and the contact area of the device. The data can be altered slightly with the array of values listing the diameter of each device. This is helpful if the values were recorded incorrectly and the user can manually alter the data accordingly. Additionally, the number of points used to calculate the first derivative of the experimental data values can be varied by changing the '# Deriv. Pts.' Variable on this tab.

D.3.5 IV Rev Fitting

The 'IV Rev Fitting' works identically to the 'IV Fitting' tab where the data from the IV characteristics from the 'IV Data' tab are imported and then fit according to specific models. The two models used either require the temperature dependence of the leakage current at specified voltage show conduction type or a thermionic field emission (TFE) model can be used to fit the IV curves at a single temperature. Currently, the first model whereby the leakage current temperature dependence is used is still preliminary but the TFE model is complete. Similar to the forward IV fitting, the user can select 'Approximate Fit Parameter' to hand fit the reverse IV characteristics accordingly. Once adequate representation of the data has been found, the user can 'Accept' the fitting and the best fit values are imported and used to fit subsequent IV characteristics.

D.3.6 CV Data

The software associated with this tab is designed to look at the first look at the 'Data Block Array' and grab only the capacitance and voltage bias data. Additionally, it will check the data blocks for magnitude and phase data and derive the capacitance values accordingly. The theory of analysis is covered in Section 2.3.4. Just as with the IV Data tap, the CV data can be imported and spurious data removed by selecting the 'Remove' button and then dragging a box around the desired curves. Once the CV data has been filtered, the A^2/C^2 plot can be shown by changing the dropdown in the 'C-V : A^2/C^2' tab. Next, the A^2/C^2 curves can be fit so that built-in voltage, barrier height, and free carrier concentration can be extracted. The slider at the top of the 'A^2/C^2 Fitting' tab allows the user to select the range of data which the linear extrapolation should be applied. Once the desired range is set, the 'Auto Fit' button can be pressed and the data can be linearly fit over the specified range. The range can be customized for various devices, but selecting the corresponding device from the dropdown list and adjusting the range accordingly. That tab labeled 'Doping Level' lets the user select the number of derivative points with which to derive the effective free carrier concentration from the A^2/C^2 data. Note that by using a small number of derivative points, the generated effective free carrier concentration will be noisier while a large number of derivative points will shorten the depletion length scale and may filter out sharp variations in the actual signal. The 'Dep. Depth Dependence' and the 'Temp. Dependence' tabs are simply used to visualize the data.

D.3.7 Parameter Visualization

It is sometimes helpful to visualize all of the analyzed data as a function of other extrapolated parameters. An example would be to plotting the IV barrier height versus the ideality factor to be used according to Tung's model [126] of Schottky barrier inhomogeneity. Additionally, two histograms are plotted for the parameters specified by the dropdown menus in the top right of this tap. Clicking the 'Get Histogram Data' button imports data from the 'Fit Data Cluster Array', thus if prior fitting was not accomplished in the same session, no data will be plotted. This analysis is typically only used for a quick view of the data and hasn't been used in this work.

D.3.8 Parameter Spatial Visualization

The software associated with this tab is used to spatially visualize the analyzed data from previous tabs once the 'Fit Paramater Cluster Array' variable is filled with data. For this to work, 'Data Name' field in the 'Data Block Array' variable needs to include the location data of the measured device (ex. 3:(0-1):TL) so that the physical location of the device referenced to the #1 Arbitrary pattern can be plotted. The parameter associated with the Z axis can be controlled by the drop down and the Z-axis spacing can be controlled with the drop downs located at the bottom left of the graph.

D.3.9 I-V-T Data Analysis

In this tab exists a mashup of IV-T analysis techniques typically used, including the Werner-Guttler [69] method and the method outlined in Section 3.1 [108]. To successfully import data into this tab, the 'Fit Parameter Cluster Array' needs to be populated with data either through the fitting procedure on the 'IV Fitting' tab or by importing fit data from an Excel sheet. The data can be imported from an excel sheet by going to the 'Defined Barrier Probability' tab and selecting the button 'Get Data Excel'.

The Werner method outlined in Section 2.3.2.1 can be applied to the data using the first three tabs, labeled 'Richarson Plot', 'Ideality and Barrie vs. Temperature', and 'Modified Richardson Plot'. Next, the method outlined in Section 3.1 [108] can be applied to the data using the 'Defined Barrier Probability' tab and followed by the 'Voltage Dep. Defined Barrier' tab. Finally, the 'Arb. Barrier Prob.' tab is an analysis method of the effective barrier height temperature dependence where the user can define an arbitrary distribution by scrolling while the mouse is hovered over the graph. Here, the Quasi-Newton, downhill simplex, and conjugate gradient methods are used to perturb the barrier distribution until the generated effective barrier height curve matches that of the data.

D.3.10 TLM Visualization

In this tab, the data imported into 'Data Block Array' is analyzed and if consistent with TLM measurement data it will plot the IV characteristics. Once plotted, under the 'IV's' tab the user can select the 'Remove' button and then click around the plot to remove specific data. Close attention should be given to IV measurements which show a shorted behavior and ones with particularly noisy behavior. Once removed, the next tab, 'IV Fitting', should be selected where the user can use the slider at the top of the screen to select the range which linear fitting of the data should occur. Typically for TLM measurements, an equal number of points around zero should be selected for further analysis. As the slider is moved, the 'IV Fit Cluster' is updated in real-time providing the user with the linear extrapolated values shown. Once the range has been finalized, the 'Auto Fit' button can be pressed at which point the remaining IV measurements will be fit with the specified range. Note that the fitting procedure does not fit all of the measurements only the remaining measurements according to the dropdown list. In the 'TLM Fitting' tab, the separation versus resistance values are plot and the user can opt to save only the data from TLM

ladders which show linearity. By selecting the specified ladder from the drop down and then clicking the button 'Save' the user will save the values of that ladder. The 'Value at Value' tab is a quick analysis to either show the current or voltage at a specific voltage or current respectively. This is only typically used to analyze non-linear IV characteristics to see if there is a correlation between the TLM separation and IV characteristics.

D.3.11 Data Filtering

The software associated with this tab is simply used to do some light filtering of the imported data. Here the user can visualize the 'Data Block Array' variable and manually remove any blocks which should not be further analyzed. Additionally the user can automate this removal by searching for a specific string in the 'Data Name' portion of the 'Data Block Array' variable and either removing if it exists or keeping if it exists. This tab is useful if the user has a set of data that was taken by mistake and needs to sort it out. Additionally, the user can save the data after filtering.

D.4 Temperature Dependent Control Software

All of the temperature variation measurement software is wrapped up into the 'D-DLTS.VI' program within the 'Holden DLTS' project. The software is capable of performing IV-T and CV-T measurements in addition to (D)DLTS measurements contrary to the naming of the program. The program was designed to run many functions in parallel each of which can be accessed by pushing one of the buttons listed within the 'Hardware Setup' panel on the left side of the front panel. Once the program has been started, each of these programs will be running in the background and take care of a specific task therefore if troubleshooting is required, the user can target effort to the specific task. In this section, the setup and device measurements with the 'D-DLTS.VI' software is summarized.

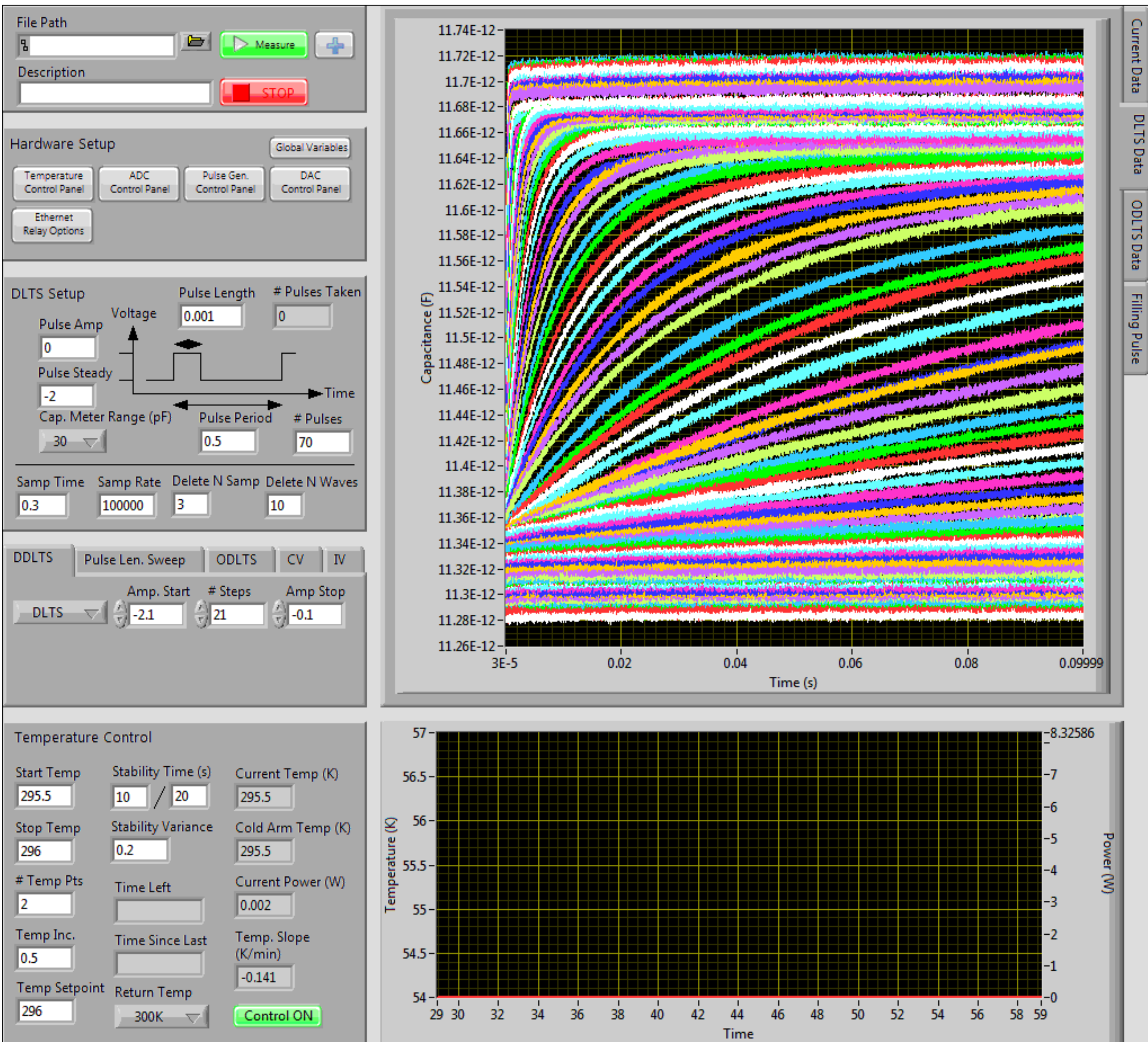


Figure 70. Front panel of the D-DLTS.vi temperature dependence measurement software. The program can be used to measure DLTS, IV-T, and CV-T characteristics on Schottky or P-N diodes.

In Figure 70 above, the 'D-DLTS.VI' software front panel is shown. From here, all of the controls needed to measure the temperature dependent characteristics of Schottky and PN diodes can be found. Prior to starting a measurement, the user is required to select a file with which the data will be saved. If it is expected that the file will be large (as with DLTS files) then selecting a blank Excel binary file (.XLSB) can help cut down the required hard drive space needed to save the data. Note that once the file has been selected, upon the first measurement the Excel file will open in the background so that the software doesn't need to re-open after ever transient is measured, thus reducing the time required to save the data. Once open, DO NOT CLOSE OR ALTER the Excel file in any way. This may cause data loss.

Once the file has been created and selected, all of the parallel tasks mentioned previously are started as can be observed in the real-time temperature plot at the bottom of the front panel. The temperature control task will constantly poll the temperature controller and update the current temperature (white line) and the output power (red line). Prior to starting a measurement it is recommended to setup the temperature points required in for the measurement located on the 'Temperature Control' panel on the

front panel. Additionally, the parameters used to fine tune the PID controller can be found in the task program by clicking the ‘Temperature Control Panel’ button while the front panel is running.

After the temperature parameters have been set, the electrical measurement settings can be set. Because the program was initially intended only to perform DLTS measurements, the panel labeled ‘DLTS Setup’ exists but is not necessarily needed to perform a measurement. This is why it is recommended to first select the type of measurement to perform from the Tab structure just below the ‘DLTS Setup’ panel as shown in Figure 71. Here, the user can select whether a (D)DLTS, pulse length DLTS, Optical DLTS, CV-T or IV-T measurement is performed.

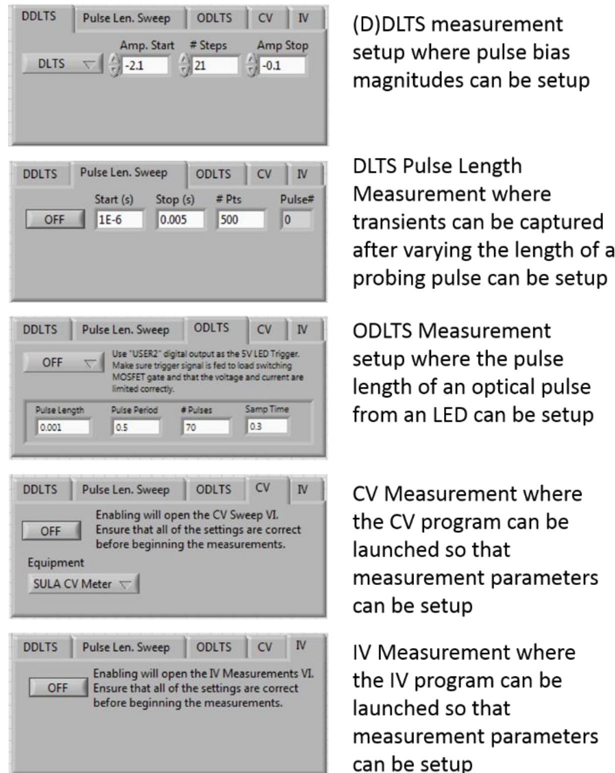


Figure 71. DLTS measurement setup tab showing the possible measurement categories including (D)DLTS, Pulse length DLTS, Optical DLTS, CV-T, and IV-T characterization.

Typically whichever tab is open when the temperature stabilizes is the characterization method performed; however, some of them can be run in sequence without intervention. This includes the (D)DLTS and the pulse length DLTS measurements. By setting the dropdown in the first tab to anything other than ‘OFF’ and then setting the button under the Pulse length tab to ‘ON’, once the temperature has been stabilized and all measurement conditions are met, the software will first measure the DLTS transient under the conditions set under the ‘DDLTS’ tab and then execute the measurement associated with the parameters under the ‘Pulse Len. Sweep’ tab. By turning any other measurements on, the program will default to turning all other measurements off.

After the file with which data will be saved to and all of the measurement settings have been finalized, the user can select the ‘+’ button at the top of the front panel to immediately run a single measurement without temperature stabilization and then save the data. This will ensure all settings have been properly set and data is being save successfully to the correct file. Once complete, the data should be manually

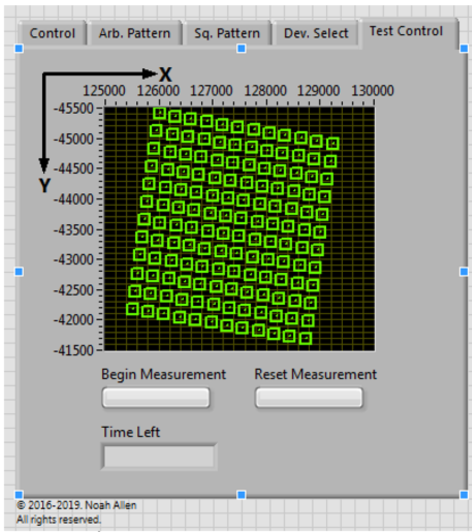
removed from the file and the user can select 'Measure' at the top of the front panel. The temperature set point will change to the first value in the temperature list dictated by the start, stop, and step of temperatures specified. Once the temperature reaches this set point and meets all of the stabilization conditions, the measurement according to the 'DLTS Setup' panel and Measurement tab structure are performed. The results of the measurement are either shown in the graph or within the respective measurement program (IV and CV measurements). Additionally, once a single data acquisition is performed, the data is sent to the 'Saving Data Parallel.VI' program for importation into the specified Excel file. Finally, the temperature set point is incremented and the process begins again.

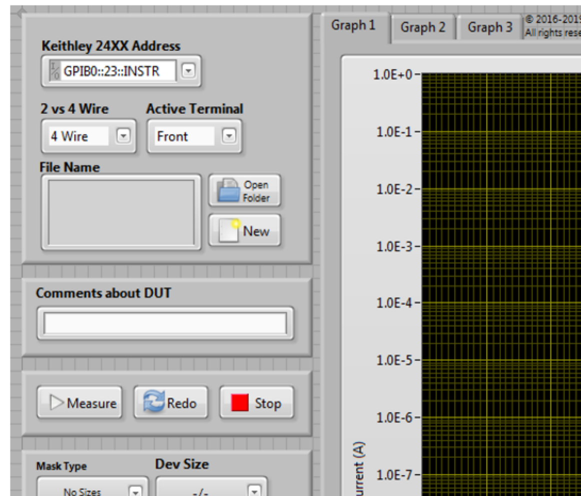
D.5 Autoprober Dependent Control Software

The Electroglas 2001 was a happy addition to the Guido lab since each full-sized sample successfully processed though the cleanroom with my mask-set could yielded >144 devices. Measuring only 20 of the devices may take around 1 hour to place the probes on the correct device, measure the IV or CV characteristics and then release the probes. Additionally, the time to measure each sample was short enough that no work could be done in parallel and if the measurement required the lights to be off, then no visual entertainment could be enjoyed. Suffice it to say, the author was quite excited to be able to automate this process.

The Electroglas autoprober is an all-in-one tool where a wafer with many die and many devices on each die could be programmed into the tool. The tool could then move the chuck to the correct position, engage stationary probes, initiate a measurement and then move to the next device. However, instead of using this interface it was decided that a pattern recognition program could be designed and the tool would simply be used to control the location of the sample chuck/platen. Therefore, this section will mainly be used to detail the pattern recognition scheme instead of understanding the instrument itself. The general idea of the Autoprober software is shown below in Figure 72.

It was realized early on that rewriting the Autoprober program to work with previously written measurement control software would have been tedious, thus the communication scheme shown in Figure 72 was implemented. In LabVIEW the easiest way for two VI's to communication is through shared access to Global Variables. Simultaneous access to these variable would have been a mess since multiple race conditions would be hard to program for therefore a walkie-talkie form of communication was used whereby the 'Ready For Measurement' Boolean was used as the PTT button. After programming the Autoprober program with the list of measurement locations, the program sets the Boolean to true which signals the measurement program to read the current location and mask data and begin measuring. Once finished, the measurement program will set the Boolean to false, signaling the autoprober to move to the next device and update its location in the global variable holder program. This back and forth communication continues until all of the devices are measured.





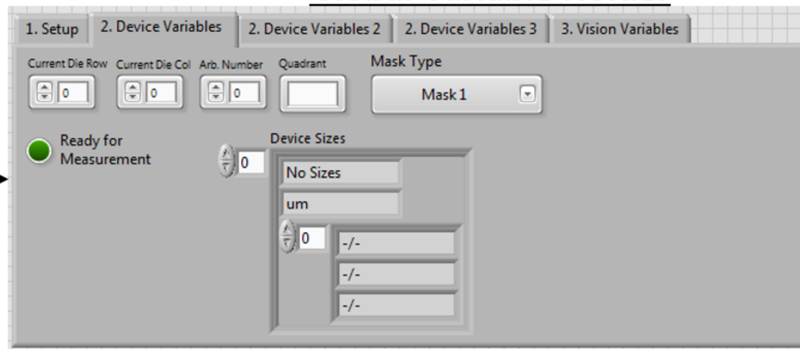


Figure 72. Layout of Autoprober communication scheme. Here the Electroglas Controller Program communicates through a Global Variable Holder with the Measurement Controller and visa versa.

In order for the Autoprober program to interpolate the location of all measurement locations, the user must input certain parameters. If a sample was fabricated with a mask that has no periodicity at all, it may be faster to manually input the locations of the devices into the 'List of Points in Arbitrary Pattern' variable located on the 'Arb. Pattern' tab. However, if a regular pattern exists then the locations of all devices can be interpolated based on the users input. In the figure below, a summary of the steps required for this interpolation are outlined.

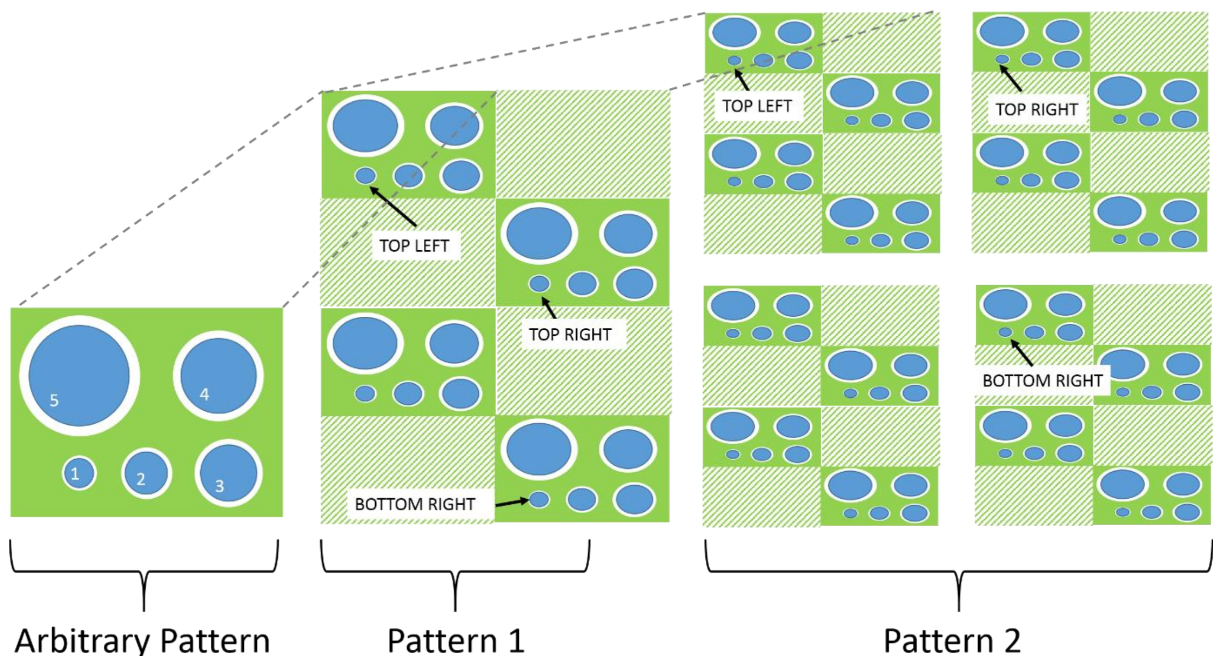


Figure 73. Pattern recognition strategy where an arbitrary pattern is input by the user and then repeated in a parallelogram configurations where the Top Left, Top Right, and Bottom Right locations are identified by the user.

In the example mask configuration shown in Figure 73 the arbitrary pattern of the blue circles within the green square are repeated throughout the full mask shown on the right of the figure. Thus, the least amount of data required to replicate the pattern includes the location of each of the circles reference to the location of the first circle, the top left (TL), top right (TR) and bottom right (BR) locations of Pattern 1 and then the TL, TR, and BR locations of Pattern 2. Then with the knowledge of how man rows and columns in the second and third patterns exists, the rest of the blue circle locations can be extrapolated assuming equal spacing. Thus the pattern recognition and alignment process is performed as follows once the sample has been secured to the platen:

- Move platen manually so that the probes are over #1 in the Arbitrary Pattern
- Manually increase platen height so that the probes are touching the device as desired and select 'Get Z' on the 'Square Pattern' tab
- Select 'Get X-Y' on the 'Arb. Pattern' tab to record the current location
- Manually move the platen to the #2, #3, #4… devices within the Arbitrary Pattern and select 'Get X-Y' for each
- Select the correct 'Mask Type' for the sample being measured (Note: Device sizes are imported from the 'AutoProbingSizes.xlsx' file)
- Ensure that all X-Y locations were recorded correctly by selecting the corresponding device from the 'List of Points in Arbitrary Patter' and selecting 'GoTo Selected'
- Go to the #1 in Arbitrary Pattern location and record it as the TL point in Pattern 1 and Pattern 2 by incrementing the array index from 0 to 1 and selecting 'Get X-Y' for the TL point on the 'Sq. Pattern' tab for each index
- Repeat for the TR and BR points by manually moving the sample under the probes to the respective points in the Pattern 1 and Pattern 2 locations on the sample

- Go to the ‘Dev. Select’ tab, use the drop-down to select ‘Die Exclusion’ and click any devices which should (white) or should not (red) be measured
- Use the drop-down and select ‘Go To Die’, click around the plot to automatically navigate to the device and check accuracy. Fix if needed.
- On the ‘Test Control’ tab, use the ‘Begin Measurement’ button to signal the measurement control VI to start taking measurements.

Once the ‘Begin Measurement’ button is pressed, the autoprober program will autonomously move the platen from device to device, while skipping those highlighted in red on the ‘Dev. Select’ tab. Once the device is in position, the ‘Begin Measurement’ Boolean is set and the measurement begins and the Boolean is unset once finished thereby autonomously measuring all of the selected devices.

D.6 Capacitance Transient Analysis Software

The capacitance transient analysis software can be used to import capacitance transients from DLTS and SSPC measurements so that data can be filtered, fit, analyzed and saved. Additionally, functionality has been added such as pulse transient analysis for DLTS measurements and Inverse Laplace fitting for LDLTS measurements. As a first step, the DLTS or SSPC data must be located within one Excel file since at this time there is no possibility of concatenating multiple files so that analysis can be done at once.

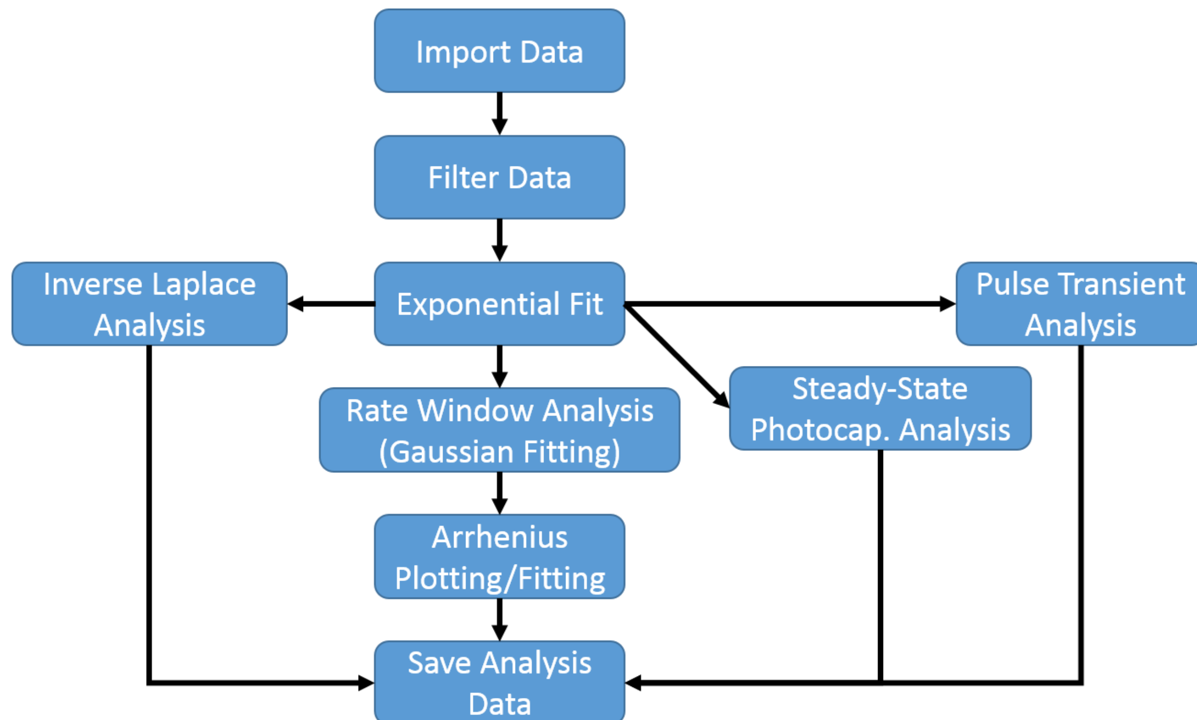


Figure 74. General process flow for analyzing DLTS and SSPC data within the 'Data Analysis.VI' program listed within the 'Holden DLTS' project.

Once all transient data has been put into one large file, the file can be dragged and dropped into the ‘Drag/Drop or Click’ box on the first tab of the front panel. Next, the excel sheet will open in the background and all of the data is read into a large LabVIEW data structure where it can be parsed and filtered. Next, a popup will be displayed where the user can choose which data from the Excel sheet is

necessary for further analysis. The usefulness of this feature is when the user only wants to analyze the transients taken from measurements with the same measurement parameter such as pulse width or pulse length. Once the dataset is selected, the program will parse and plot all of the transients associated with the measurement.

As described in Section 2.3.5.5.1, filtering the data can be crucial to ensuring that the final spectra can be accurately analyzed. First, if any of the recorded transients are obviously erroneous, such as those taken when the probes were not in contact with the sample, the user can select the 'Remove' button and then click the graph near the dataset which should be removed. This does not delete the data but simply removes it from being analyzed further. Next the transient data can be filtered with a combination of binning and averaging the data. Binning is useful to remove and 'pops' in the capacitance data usually present if the probes were jostled or a power supply was switching during a measurement. The binning is performed before the running average is taken so that artifacts can be removed. Note that over binning or averaging the data can cause deviations in the final deep level characteristics. Thus, it is OK to have some noise in the data.

As a second level of filtering, the transients can be fit with an exponential curve so that all of the noise is removed from further analysis. The equation used to fit the data is shown in Equation (60) while the effect of using the transient during rate window analysis is shown in Figure 23. As an additional feature, the transient curve can be altered again by removing sections of the curve. This is rarely done but sometimes necessary if while during data transfer from the DAQ to the program, the hardware is met with a glitch so that capacitance was erroneously reported for a large portion of the transient. The options are 'No Click', 'Remove Before', 'Remove After', and 'Keep From-To'. Most of these options are self-explanatory except for the 'Keep From-To'. This options requires the user to drag a box around the data which is desired for further analysis.

Once the fitting has been accomplished for all transients, the user has a choice of how to further analyze the data. If the user highlights the 'Use Transient Fit' button on the 'Capacitance Transient' tab, the exponential fitting parameters will be analyzed further however, if the button is not selected the raw filtered transient data will be further analyzed. By selecting 'Send to Laplace Fitting' the actual data from the current transient viewed on the plot will be sent to an inverse Laplace fitting algorithm. The seed parameters are those found during exponential fitting of the data. The transient or fit data could also be sent to the steady-state photocapacitance analysis tab where analysis according to Section 2.3.5.6 is performed. Finally, the data can be analyzed via the Lang [90] method where the transient data or transient fit will be analyzed accordingly.

The steady-stated photocapacitance and Lang's method have been adequately explained in Sections 2.3.5.6 and 2.3.5.4 adequately. The inverse Laplace method is not discussed here since no data in this work was analyzed by this method.

Finally, once the user has performed the desired fitting, the data can be saved in a separate Excel file for plotting and future analysis. In the 'Export Data' tab, the user can select one or more sections of the data to be saved and plotted. Please note that not all of the selections will plot data and thus software needs to be added to these sections to do so.