Appendix B.   Miscellaneous Information about the PEBB Leg Test

B.01   Hardware Construction

(a) Test Setup

When the PEBB leg is built, initial burns in tests are performed with low input and output power. The purpose of the initial test is to verify the correctness of the test setup, including the signals from the controller.

A controller board which has DSP and EPLD is installed with a PC emulator connected. The DSP program is designed to generate PWM switching signals for a leg with the aid of the EPLD. Duty signals are provided from the EPLD to a interface board that connects to the gate drives. The power stage of the PEBB leg and the controller board are connected through fiber optic cables for complete isolation. The interface board has transmitter and receiver sets connected with fiber optic cables. The transmitters are connected from the output of the EPLD through 100-Ω resistors to limit current. For the initial low-power test, a 600-V 4.5-A power supply is installed for the positive side of three-level input source. Figure B-1 shows the test setup. Figure B-2 shows four gate drive signals for the PEBB leg.
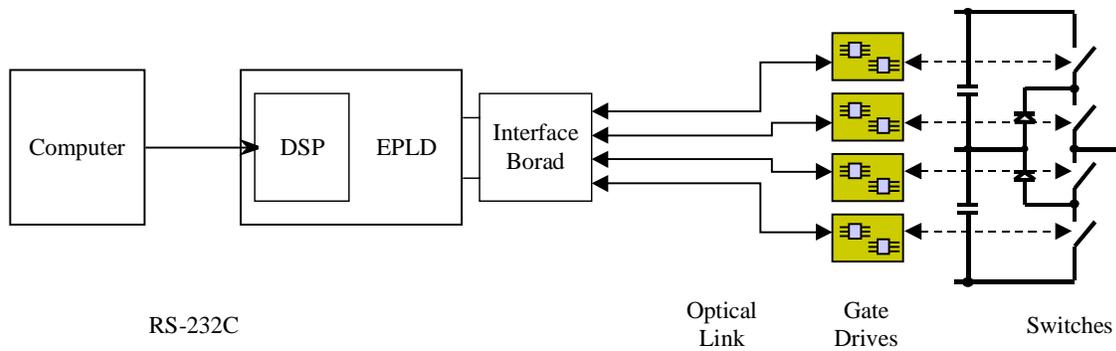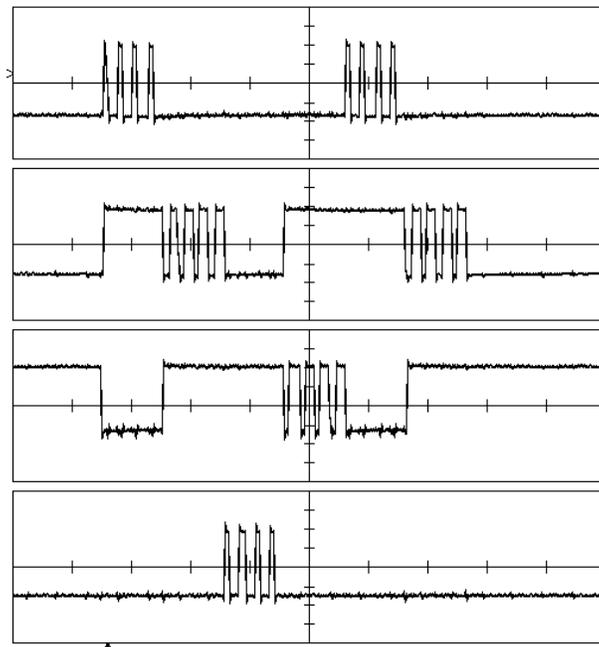
Figure B-1. Test setup of the PEBB leg

Figure B-2. Generated gate drive signals for the main switches of the three-level PEBB

leg

(b) Design of the Gate Drive

The gate drive circuit is shown in Figure B.3. A Motorola gate drive chip MC33153 is

used to generate the gate drive pulse. The chip is specially designed for an IGBT drive

for high-power applications. It has a small footprint and features under-voltage detection and desaturation protection with programmable fault blanking time.

Two on-board DC/DC converters are used to provide power. The drive chip has desaturation protection and under-voltage lockout functions. Signals from the controller are fed through fiber optic cables. The optical link is used to provide complete galvanic isolation between the power stage and control circuits.

The power supplies for the gate drive are unregulated DC/DC converters with 3000-V isolation. One of them has +15 VDC output and the other has –5 VDC output. The power capacity of the DC/DC converters is one watt, and is sufficient for driving a 400-A/1200-V IGBT module switching at a frequency lower than 20-kHz. There are eight gate drives for one PEBB leg. All of the gate drives are powered by a DC 12-V power source, and a common-mode choke is used to reduce the interference between gate drivers.

Although the output stage of the drive chip can drive a 1.0-A for a source and 2.0-A for a sink, it is still not fast enough to drive a 400-A/1200-V IGBT module. Therefore, an output current booster consisting of a PNP and NPN transistor pair is used to increase current capability. By using separated current limiting resistors, the turn-on and turn-off peak current can be adjusted independently.

The desaturation protection is realized by comparing the C-E voltage of the IGBT with a preset threshold. According to the characteristics of the IGBT module being used, this threshold voltage is about 5-V for 1000-A. The voltage rating of the series diode should be more than 1200-V, so a 2000-V diode is used. When the desaturation is detected by the chip, the IGBT is disabled and a fault signal is activated until the PWM command

from the controller is removed. The fault signal can be used by the controller for higher-level protection.
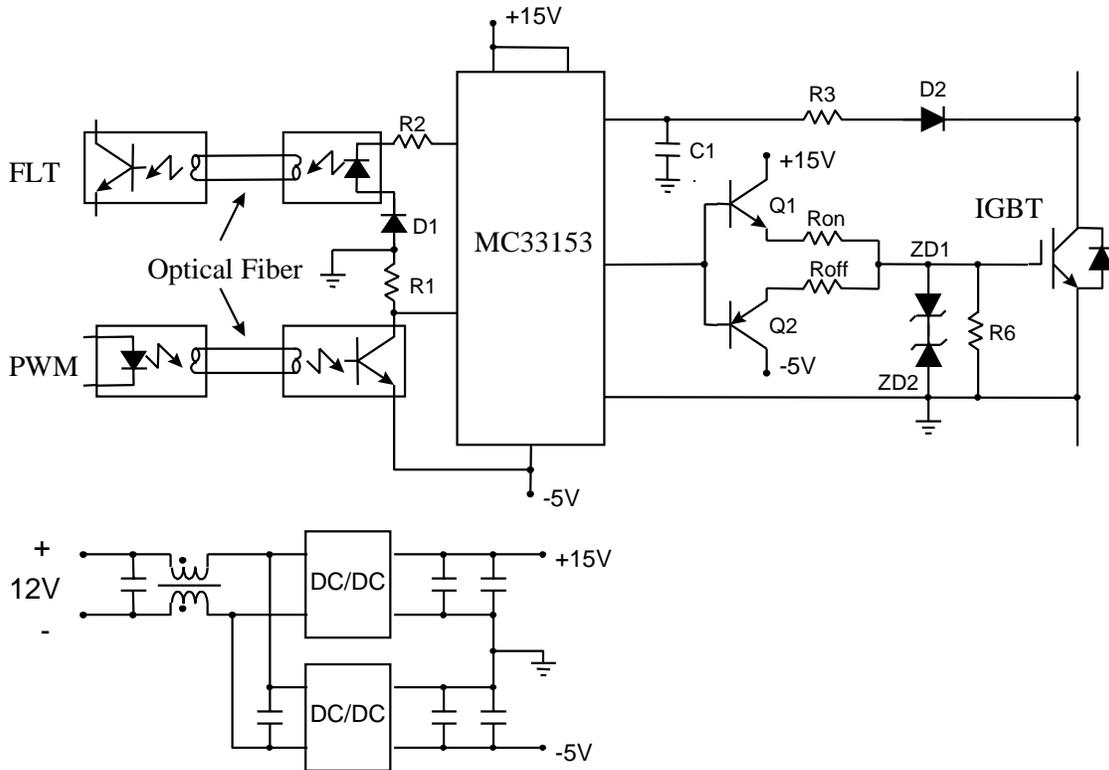

Figure B.3 Gate driver circuit for IGBT modules

(c) Design of the EPLD

To activate one switch, one pulse for the main switch and two auxiliary pulses for the soft-switching switches are needed. The length of each pulse is provided by the DSP. A PWM generator is implemented in the EPLD using a hardware description language (HDL). There are five different pieces of information for one PWM cycle. The first is the length of the main switch duty. The other four pieces of information are for the two auxiliary pulses lengths and delays. Because the length and delay time of the auxiliary pulse is much shorter than that of main pulse, four four-bits are assigned for auxiliary

data and one eight-bit is for the main pulse. Since the PWM pulses should not be changed during switching, the data must be saved in latches as they arrive. The latched data are loaded into three counters; one is an eight-bit for the PWM pulse and the other two are four-bit for the length and delay of the auxiliary pulses. The PWM generation circuit is implemented with a state machine.

Figure B-4 shows the state machine. An eight-bit latch, named *PWM,* stores the main switch duty length. This value is loaded into a counter, *cPWM*, which counts down from the value to zero to generate the gate drive signal to the main switch. The latches to generate the auxiliary switch gate drive signal are *Delay* and *Width*. These are four-bit registers. The counters for these latches are *cDelay* and *cWidth*. The auxiliary pulse generation circuit is implemented with a subcircuit to generate pulses twice during one switching cycle. This structure can simplify the combination of the auxiliary pulses. Figure B-5 shows definitions of the PWM pulse and auxiliary pulse. There is one master counter, *Timer*, which counts one switching cycle. The length of the *Timer* is the same as that of the *PWM*.

Transition conditions for each state in Figure B-4 are as follows. The state machine is restarted whenever the *Timer* becomes zero. At this time, all three counters load their values from each latch. This state is the first state, St_1. At the end of *cDelay* the state machine changes from St_1 to St_2 and the main switch gate signal is set high. During St_2 the main switch is kept high. The state transition condition for St_2 to St_3 is at the end of the counter *cPWM*. At this moment, the counters *cDelay* and *cWidth* load values from their corresponding turn-off data latches. During St_3 the main switch is kept high only when the *cDelay* is not zero. At the end of *Timer*, the state machine is reset. By definition

of the *Width*, the auxiliary switch gate signal needs to be high whenever the *cWidth* is in
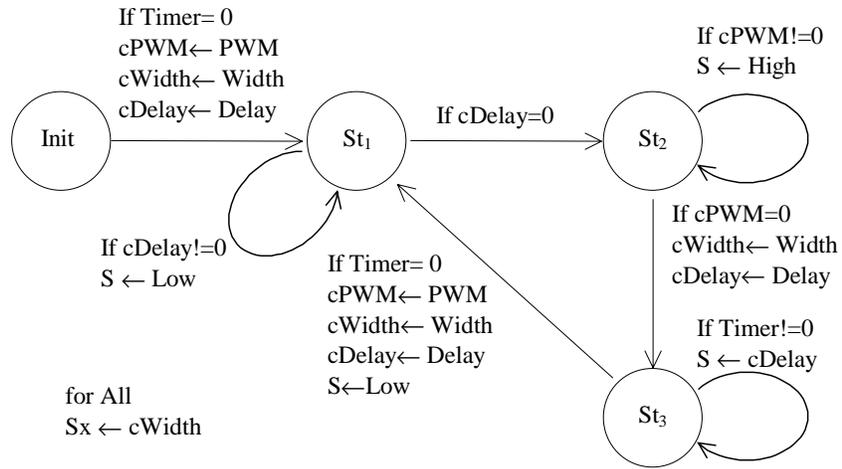
the middle of counting.

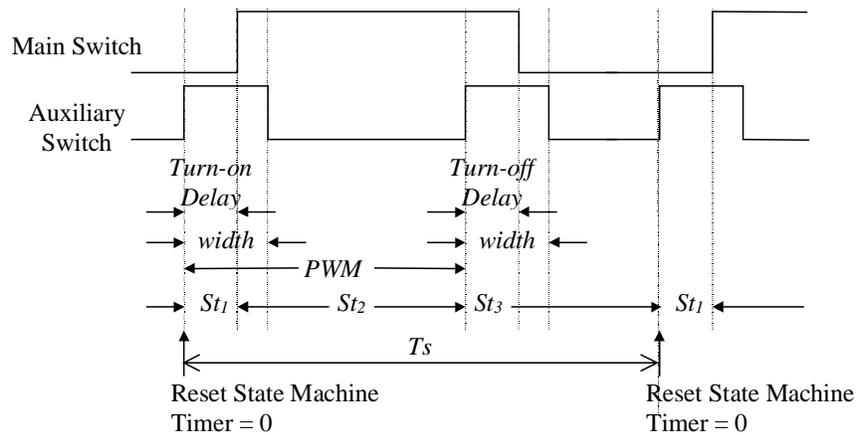Figure B-4. State machine for PWM and auxiliary pulse generation

Figure B-5. Timing definitions of the PWM and auxiliary pulse

The two switch signals generated by the state machine inside of the EPLD are provided

directly to the gate drive through the optical link.

(d) DSP Programming

The DSP used for the PEBB leg test is ADSP-2101. The DSP is activated by the interrupt from the *Timer* of the EPLD. The *Timer* activates the interrupt every 256th clock of 5-Mhz. The switching frequency generated by the interrupt is 19.531-kHz. The duty ratio information is stored in a circular table located in the program memory of the DSP. For every interrupt, the DSP reads the table sequentially and sends it to the EPLD. The shape of the PWM during testing is determined by the content of the table. For example, if the table contains sinusoidal data, the output will be sinusoid.

B.02   The PEBB Leg Test

(e) The Effect of the Parasitic Capacitor

One of the important parasitics for the switching transient is the capacitance between the collector and emitter of the main switch. The effect of the capacitance can be identified by adding an external small capacitor in parallel with the main switch. The capacitance of the external capacitor tried is 1.1-nF. Figure B-6 shows the turn-on and turn-off voltage waveform across the main switch *S1* with and without the external capacitor. As shown in Figure B-6, there is no change during turn-on. However, during turn-off, some changes are noticed. The peaks of the spike are increased by about 50-V throughout the current range. In addition, the ringing frequency is changed from 10-Mhz to 7.5-Mhz, as expected.
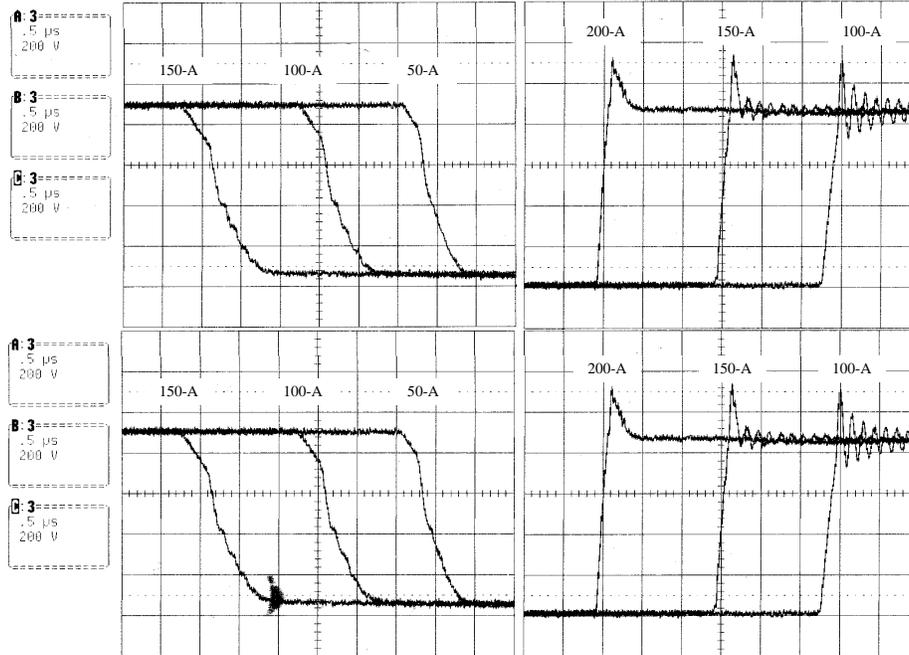
Figure B-6. Turn-on (left) and turn-off (right) voltage waveforms with (top) and without (bottom) the capacitor 1.1-nF

(f) The Effect of the DC Link Capacitor

To identify the effect of the DC link capacitor, the leg is tried with several different values and types of DC link capacitors. As mentioned before, the voltage spike during turn-on can be controlled by the gate resistor. The voltage spike at turn-off depends great deal on the parasitic of the circuit. This test could give some clues to the relationship between the DC link voltage spike and the switches. The capacitors tried are a 16.5-μF high frequency one and an additional 1200-μF low frequency one. The results show that the capacitors do not have much influence on the voltage spike across the switches. For the switches *S1* and *S4*, which have smaller areas of current, the changing paths have slightly lower spikes than those of the *S2* and *S3*, which do not have any differences at

all. Table B-1 and Table B-2 show measured voltage spikes at each current level with and without the capacitors.

Table B-1 Voltage spikes with different DC link capacitors for S1,S4

Switch Current	Voltage Spikes		
	Original C	16.5uF	16.5uF + 1200uF
100A	200	181	181
150A	200	181	181
200A	200	181	181

Table B-2 Voltage spikes with different DC link capacitors for S2,S3

Switch Current	Voltage Spikes		
	Original C	16.5uF	16.5uF + 1200uF
100A	240	240	240
150A	235	235	235
200A	230	230	230

(g) The Effect of the Snubber

A RCD snubber, as shown in Figure B-7, is tried across the S3, with a 0.16-µF ceramic capacitor, a 50-kΩ 20-W resistor, and a fast diode. The resulting spike in the 200-A case is about 200-V. At 100-A, it is about 60-V. The ringing becomes more severe then without the snubber, but the direction of the spikes is downward, as shown in Figure B-8.
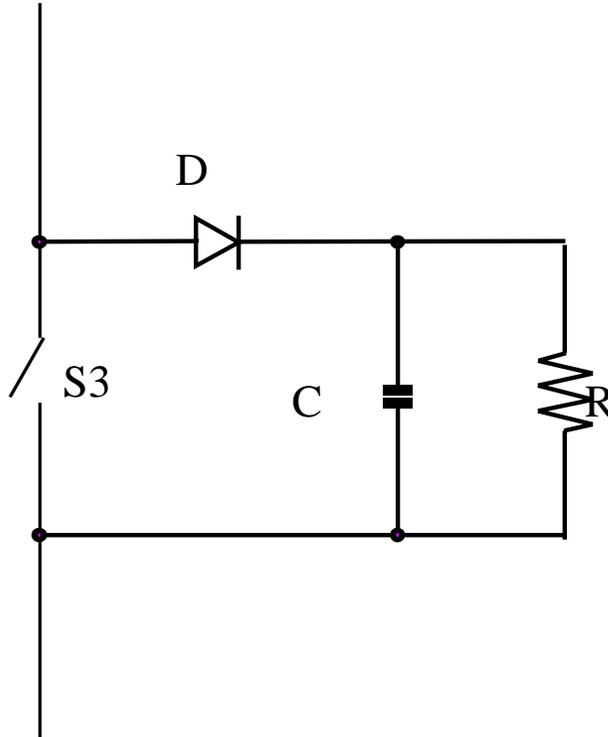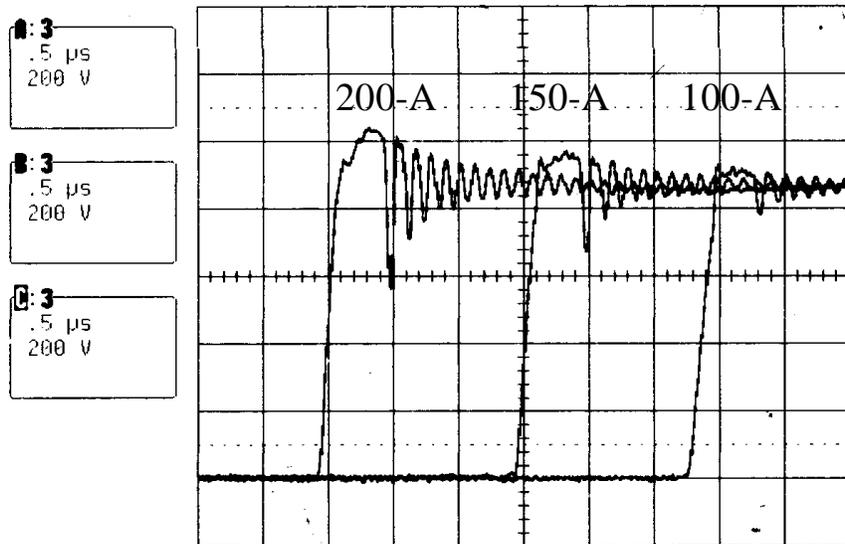
Figure B-7. The RCD snubber

Figure B-8. S3 turn-off voltage waveforms with the RCD snubber

(h) Voltage across the Diode during Transient

The value of the voltage spike at *S2* and *S3* is about 230-V at 200-A. The voltage across the opposite two diodes is about 60-V each, and about 15-V across the each of the connection conductors. The total voltage of the turn-off path is about 170-V. The remaining voltage of 60-V is across the clamping diode, which is in series with the *S2* or *S3*. This voltage is generated across the diode while the diode flows currents. Generally, a diode is forward biased while it flows current. Figure B-9 shows voltage across the *S3* and *Dn* during turn-off. It is obvious that the *S3* current is transferred into the diode *Dn* during turn-off. Therefore, the current through the diode *Dn* is forward direction current. However, the voltage across the diode in Figure B-9 shows reverse biased current. In this transition, the voltage across the diode turns out to be the voltage induced by the parasitic inductance of the diode, because the voltage across the emitter of switch *S3* and the negative input source shows same shape as shown in Figure B-10.
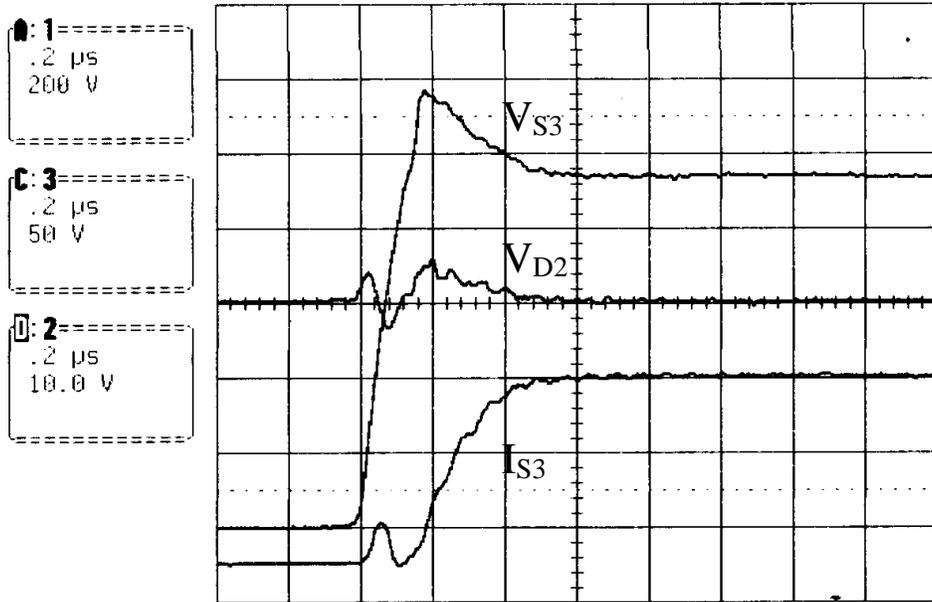
Figure B-9. Voltage waveforms of the *S3* and *D2* during turn-off transient with 200-A
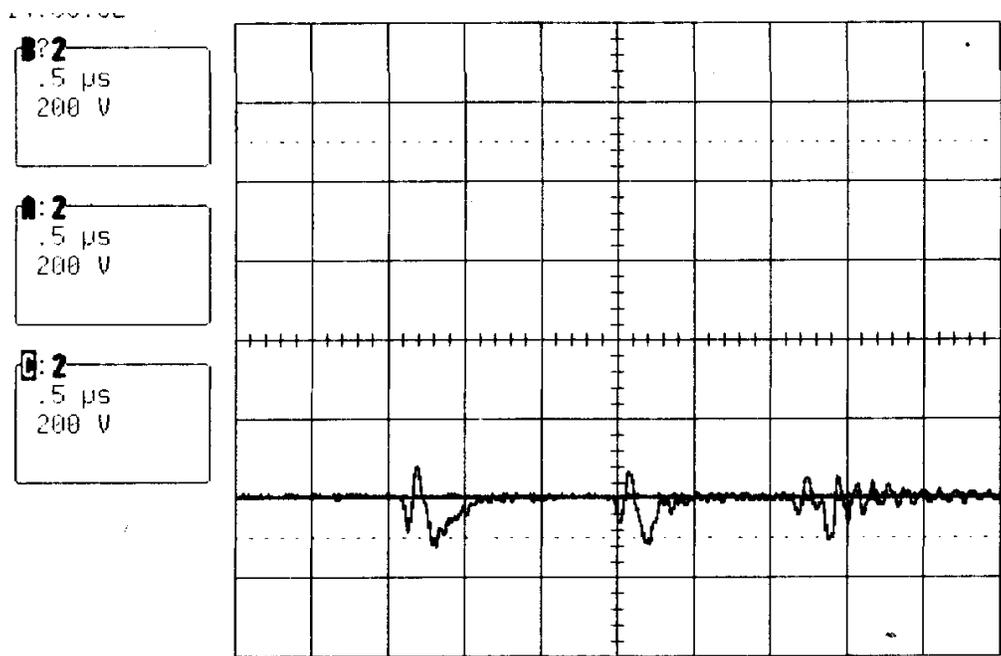
switch current

Figure B-10. Voltage waveforms between the *S3* emitter and *Vn*