A MICROPROCESSOR BASED BUS RELAY

by

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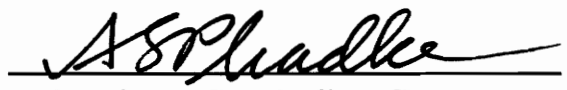

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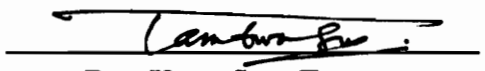

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(ABSTRACT)

A microprocessor based bus protection scheme has been proposed for a single bus system which employs a new technique to overcome the problem of current transformer saturation. The protection scheme uses a combination of the percentage differential current principle and the phase comparison principle. A sampling rate of 1440 Hz is used. Existing algorithms for a saturation detector are reviewed and a new saturation detector has been developed. This new saturation detector employs the slope difference of the secondary current to determine the CT state. It has a high sensitivity and can reveal early (one–eighth cycle) saturation. With the incorporation of this new saturation detector, the bus relay can make a correct decision for either an internal or an external fault in the presence of current transformer saturation in a half cycle in most cases.

The bus protection scheme has been coded in Fortran and tested against data produced from EMTP. The simulated results from eight sets of data are presented in this thesis. All cases show that the bus protection scheme works correctly.

The algorithm for the new saturation detector will be implemented using a 32–bit microprocessor by Mr. Paul A. Dolloff.

Acknowledgements

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CHAPTER ONE

Introduction

Bus is an important equipment in a power system where the feeders are connected. Through buses a system is formed for transferring power from sources to loads. Usually, the buses are located in substations or generation stations, and they are not greater than one or two hundred meters in length and twenty meters in width. The probability for a fault is low at a bus as compared to transmission lines; however, once a fault occurs on a bus, the consequences are more serious. This is because the bus relay will trip all feeders connected to the faulted bus, resulting in a wholesale disruption of system. Therefore, the special consideration must be given to a bus relay.

Since all the feeders are connected to the bus, in the normal state or in the case of an external fault without CT saturation, the sum of all the currents in all feeders on a bus should be zero; whereas in the case of an internal fault, the fault

current is the sum of all the source currents. These observations provide a very efficient and simple method for protecting the buses — a differential current principle. When the system is in a normal or an external fault state, some of the currents come into the bus and others go out. In the case of an internal fault, all currents come into the bus. These observations lead us to another method — the phase comparison or directional comparison method.

The primary currents in feeders are too high to be used in relay, so current transformers are introduced between the primary side and the relay to reduce the primary currents to an appropriate level. However this practice creates some problems. The current transformer is expected to faithfully transform the current, in other words, the secondary current should be a reduced scale duplication of the primary current. In fact, this is not always true. As can be seen from Fig. 1, before the knee point, the secondary voltage and the magnetizing current are in a linear relationship. After the knee point, this relationship does not hold. When the voltage increases slightly, the magnetizing current will increase dramatically and the secondary current will decrease accordingly to a very low value. This phenomenon is called CT saturation. CT saturation is likely to happen in the case of near–bus external fault such that the differential current is no longer zero. Thus the simple differential current principle will fail to discriminate between an internal and an external fault. The current waveforms will be distorted, the phase comparison scheme may also not work properly.

In order to overcome the problems caused by CT saturation efforts have been concentrated on the following aspects:

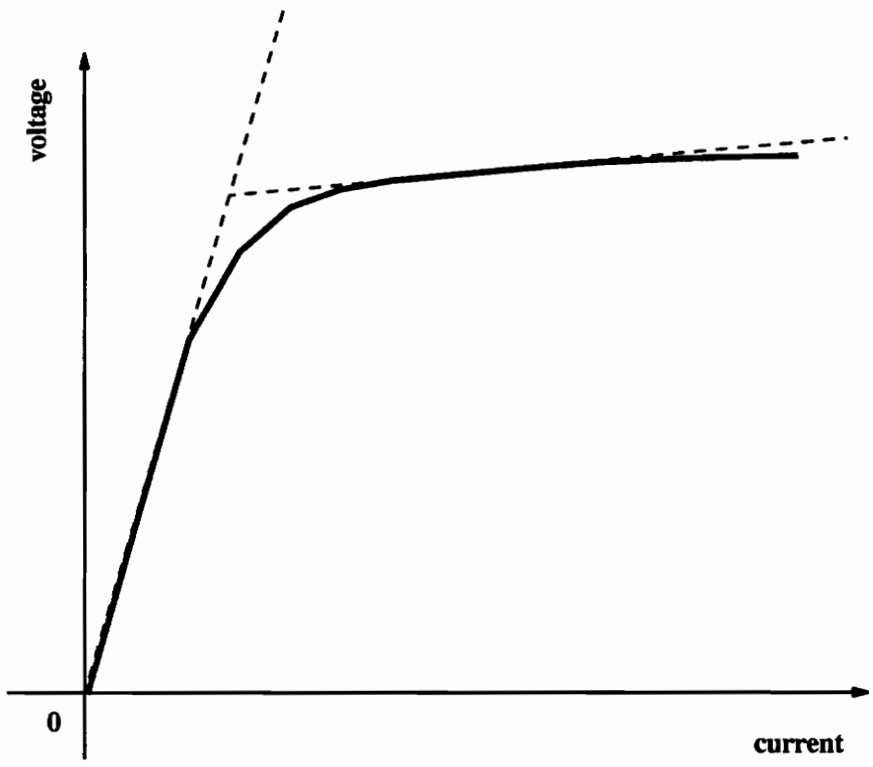

Fig. 1 CT Magnetizing Characteristic Curve

1. CT characteristic

   Air–gapped CT [1]

   Linear coupler [2]

   MOCT [3]

2. Protection Principle

   Percentage differential current scheme

   High impedance differential scheme

The air–gapped CT is similar to an ordinary electromagnetic current transformer, but there is a gap in the core. The core is made of materials with high magnetic permeability and low magnetic reluctance, whereas, in contrast, the air gap has low magnetic permeability and high magnetic reluctance. Therefore, if an air gap is inserted in the core, the magnetic reluctance of the whole core will mainly depend on the reluctance of the air gap. It will be more or less independent of external conditions and will remain almost constant. Thus the magnetic flux in the core is essentially proportional to the primary current, and in turn the secondary current is in a linear relationship with the primary current. It is free of CT saturation.

The linear coupler is a kind of current transformer without the core. It has a constant mutual reactance between the primary and the secondary, and is free of saturation problems. The secondary current is proportional to the primary current.

Both the air–gapped CT and the linear coupler have high magnetic reluctance in their main magnetic circuit. Therefore, to transfer the same amount of

energy from the primary side to the secondary side, more turns of coils are required compared to an ordinary CT. They have higher magnetizing currents such that the errors in magnitude and phase are greater than in an ordinary CT. Also the linear coupler is expensive and has not yet actually been used in a relay.

The MOCT (Magnetic–Optic Current Transformer) is a new kind of CT. Its working principle is the Faraday magnetic–optic effect. When polarized light is sent through glass in a direction parallel to the applied magnetic field the plane of polarization of light is rotated. The amount of rotation is proportional to the magnetic field intensity, which in turn is proportional to the current, so that the amount of rotation is also proportional to the current. The secondary current is digitized and well suited for computer based relays and meters. There are no coils and core at all, it is free of saturation, ferroresonance and hysteresis. It has not yet been used for relaying in practice.

It is common to adopt the percentage differential scheme against CT saturation. The tripping signal is restrained by a second signal which is proportional to the sum of the absolute values of currents. This practice enhances security in an external fault case, but lowers the sensitivity to an internal fault.

The high impedance differential scheme [4] is an excellent method for coping with CT saturation. When a CT saturates, its magnetizing inductance drops to a very low value so that it draws all secondary currents into one branch, bypassing the differential relay. High impedance in series with the differential relay generates the risk of high voltage on the secondary side so that relays and cables

may be destroyed, and CTs may be driven to saturation in some internal fault cases. Hence some steps (such as the use of MOVs) must be taken for limiting overvoltage and current transformers having high saturation point characteristics must be used in the high impedance differential scheme application. This scheme requires that the secondary sides of all CTs are physically connected together. Hence the high impedance differential scheme is not suitable for a computer based relay.

The percentage differential and the phase comparison principles are better candidates for computer based relaying. The secondaries of CTs can be individually connected to the computer. The CT ratios are not necessarily equal. In a computer all currents can be converted into a common base, combinations of various schemes can be implemented, and some new methods for bus relay and CT saturation may be developed.

In this study, a new, simple and efficient CT saturation detector has been developed. It is incorporated into the percentage differential and phase comparison schemes. This allows the percentage differential scheme to have a variable restraint signal and to adapt to CT situation. The distortion around current–zero regions of the secondary currents can be corrected so that the phase comparison principle can work properly.

The remaining chapters of this thesis are organized as follows:

Chapter two is a survey of the literature in the field of computer based bus protection. Chapter three deals with the algorithms of CT saturation detectors.

The existing methods are reviewed and a new algorithm is proposed. Chapter four describes the improved percentage differential scheme by using the new CT saturation detector. Chapter five describes the improved phase comparison principle by using the new CT saturation detector. Chapter six proposes a protection scheme for a single bus system. Chapter seven gives simulation results of the proposed bus protection scheme. Various types of internal or external faults are simulated. Chapter eight presents conclusions and future work needed.

CHAPTER TWO

Literature Review

In 1969, G. D. Rockefeller published his remarkable paper [5], in which he proposed the use of computers for power system protection and developed detailed algorithms. In this paper, he laid a foundation for the field of computer relaying. Considerable research, development, and implementation has gone forward in this area since then, and well–developed computer relays for transmission lines, transformers, generators and fault locators are available today. However, very few papers deal with bus relays. The reasons for this may be as follows:

1) Bus relays require higher security.
2) The existing bus relays are quite successful in terms of security and speed.
3) CT saturation is a key issue which has not yet been successfully solved.

In 1969, G. D. Rockefeller proposed the percentage differential principle

computer based bus relay in his milestone paper [5], and in 1970 B. J. Cory *et al* [6] used the differential principle as a stand–alone computer based bus relay. Both Rockefeller and Cory simply converted the conventional differential principle to its discretized form for computer use, not taking CT saturation into account. Since computers were quite expensive, and computation speeds were slow, the computer based relay would not be widely accepted by utilities until an inexpensive and high speed microprocessor became available. With the advent of the microprocessor, relay engineers and scientists were attracted to computer relaying. Research began to expand into several aspects of transmission line relaying. Meanwhile, little attention was paid to bus relaying. In the early 1980s, Tokyo Electric Power [17] used the percentage differential current principle, and they also incorporated a CT saturation detector into the over–all scheme as a blocking element under the assumption that saturation only occurs in external fault cases, and that only one CT may saturate. Jihuang Lu *et al* [8] used the percentage differential principle in conjunction with a scheme for making rapid distinction between an internal and an external fault. This was because CT saturation may set in in a few milliseconds after a fault inception. Lu implemented this principle using static circuits. In fact, this principle can be realized using a microprocessor. This method has a high risk of blocking relays for internal faults in which magnitudes of the differential current samples at the beginning of a fault are less than the threshold value. This method may also fail to block relays when CT severely saturates for an external fault due to high remanence.

Recently, when the integrated protection and control concept emerged [9][10][11], bus protection became a part of such a system. It is appropriate to

incorporate the bus protection into an integrated protection system, because bus protection needs all currents in feeders and their associated circuit breaker and isolator status. Udren *et al.* [10] proposed the use of variable–percentage relaying with raw current samples and the phasor–based phase comparison scheme for bus relays. They assumed that no CT saturation occurs in the first one–fourth cycle of fault current, and shortened the data window to two or three milliseconds so that the trip decision would be based only on the good current samples. There is no doubt that the variable–percentage differential principle further improves the restraint behavior so that the restraint signal adapts to a differential current. In this way, the security of the bus protection would be improved, but sensitivity to an internal fault is reduced. Other authors mentioned bus protection as a part of an integrated function, but they did not state what principles are to be used.

CIGRE 34.02 working group [12] [13] explored the feasibility of some existing schemes for computer based bus relays. The percentage differential current and phase comparison principles were recommended.

Phadke and Thorp [14] proposed that a quarter cycle phasor calculation coupled with a quarter cycle transient monitor would provide a suitable computer based bus differential relay, and sample based percentage differential characteristic could be used to provide protection within the first few milliseconds. They also proposed the phase comparison scheme in which only the start of a current half cycle would be used to determine the phase relationship, so that one of the CTs going into saturation would be of no immediate concern.

Lifeng Yang, P. A. Dolloff and A. G. Phadke [15] employed the sample based percentage differential current and phase comparison schemes using CT saturation detectors. These schemes will be described in detail in this thesis.

Since both the sample based percentage differential current and phase comparison principles are very simple, their computation burdens are relatively small, and since they use station–wide information, they can be easily made a part of the integrated protection and control system for substations.

CHAPTER THREE

CT Saturation Detector Algorithms

3.1 Introduction

As mentioned in first two chapters, CT saturation becomes a key issue whenever the differential current scheme is used. Hence if the state of the CT could be determined in real time, it would be helpful for bus protection systems, and the corresponding countermeasures against CT saturation could be taken so that the security and dependability of bus relays could be improved.

The magnetizing inductance of a CT is nonlinear, its V—I characteristic curve can roughly be divided into two segments. the slope of the first segment is very steep, while that of the second one is very flat. When a new CT is chosen and installed, it is supposed to work in the first segment. The corresponding magnetizing inductance is high, so that the ratio between the primary and the secondary current is approximately in the ratio of CT turns. Even with high currents containing DC

components, it is expected to work far beyond the knee point.

There are several factors which can lead current transformers to saturation such as CT burden, lead resistance, cable impedance, and primary current. All these factors can be minimized by careful design and arrangement. However, as the power system grows, the fault current level keeps increasing. And with new control, monitoring and measuring devices connected to the current transformers, the CT burden may increase. These may deteriorate the CT's working condition. If high remanence exists, the CT may go into the second segment — saturation state.

The problem of CT saturation has been known for a long time, some techniques have been developed for devising a CT saturation detector. Basically, these techniques fall into three categories. The first technique measures the magnetizing inductance from the CT's secondary side. This requires auxiliary devices. The second method is, instead of looking at the CT individually, to assume that only one CT saturates and identify it from the system point of view. The last method is to check the change in the secondary current.

In the following sections of this chapter, the methods mentioned above will be reviewed, and a new technique for detecting CT saturation will be described.

3.2. High Frequency Injection Principle [16][17]

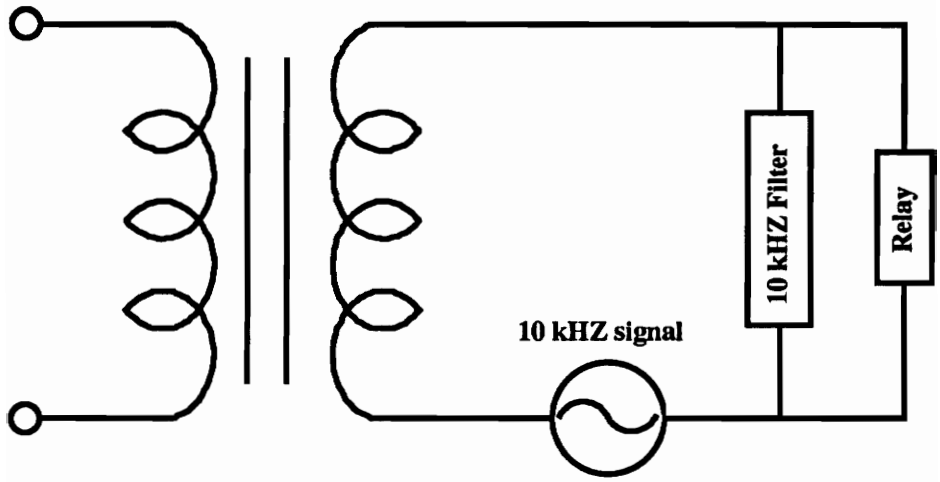

Fig. 2 High Frequency Saturation Detector Principle

As shown in Fig. 2, a stable high frequency (10kHZ) voltage source is connected to the secondary side of the CT in series with a burden (including the relay), and a series resonant circuit which resonates at the given high frequency, is paralleled with a burden such that the burden is bypassed for the high frequency signal. The high frequency signal is chosen so that the operating signal (50 or 60 HZ) has a minimum influence.

In such an arrangement, the high frequency voltage source is applied to the magnetizing inductor,

$$e_h = L_m \frac{di_h}{dt} \qquad (1)$$

Where e_h, i_h are the high frequency voltage and current, and
L_m is magnetizing inductance

From the equation above, e_h and i_h can be measured, and L_m can be determined and compared to a particular value, which is the inductance at the knee point L_k. The criterion is

$$L_m < L_p \quad ; \text{CT in saturation}$$

The magnetizing inductance is dependent on the CT structure, material, insulation used, and operating conditions. Different current transformers have different characteristics and knee points, and after long service, the characteristics may shift. Hence it is difficult to choose a reliable critical value for L_p. Besides, this method requires a high frequency generator and associated filters, thus it

complicates the relay system.

3.3 System Method --- Differential Current Method

In general, CT saturation has the worst effect on differential current schemes, and is most likely to cause trouble in case of an external fault. Usually, the CT on the faulted circuit has a high possibility of saturation. If this happens, the differential current is discontinuous in its waveform. This leads to a way to detect CT saturation from the differential current waveform.

3.3.1 Time Difference Between Fault Inception And Differential Current

This method uses a fault detector and differential current to determine the point of CT saturation. The fault detector can be either overcurrent type, or undervoltage type. For the overcurrent type detector, each phase of each feeder must be checked, while for the under voltage type detector, only six variables need to be compared to the threshold values. These variables include three phase to ground voltages and three phase to phase voltages. For bus relay applications, the voltage type fault detector is more efficient than the current type detector, but six additional voltages must be acquired, obviously increasing complexity. Because of this, in bus protection, the current type fault detector is preferred.

For an internal fault, the fault detector and differential current pick up

almost simultaneously, whereas in an external fault case, since there is always a short period of no saturation after fault inception, the differential current normally picks up after the fault detector does. This time difference between the two is used for indicating whether or not there is CT saturation.

The operating principle of this method is quite simple, it does not require much effort and is suitable for computer application. But in some cases, at the beginning of a fault inception, the fault current may not be high enough to trigger the fault detector, and if high remanence exists, the CT may saturate early, so that the differential current may unexpectedly be generated early. Consequently, this method may mistake an external fault for an internal fault and issue a wrong tripping signal.

3.3.2 The Differential Current Slope Method

The assumption made for this method is also that CT saturation only occurs in an external fault. Therefore, the differential current in an internal fault is continuous and smooth at the beginning of fault, and it is discontinuous and changes dramatically when it appears during an external fault. A CT saturation detector can be devised in response to the slope of the start of a differential current. When the differential current contains a high DC component, its slope at the beginning may be very steep even without CT saturation. On the other hand, although the slope of the differential current in case of CT saturation is high, due to the antialiasing filter, the slope could be made more gradual. Therefore, it may be difficult to choose

a proper threshold slope.

3.3.3 Non–Current State Method

This method is somewhat similar to the first one described this chapter. It checks the continuity of the differential current, if the non–current state of the differential current exceeds a specified period, then CT saturation is assumed.

3.4 The Secondary Current Method

In a normal state, the secondary current of a CT assumes a sinusoidal waveform. When a fault occurs, the secondary current may contain the decaying DC component depending on fault conditions, but its current waveform is still smooth if the CT does not saturate. If the CT saturates, especially at high currents, the secondary current will rapidly drop to almost zero. This change from pre–saturation to post saturation can be used to reveal the CT state.

3.4.1 Change In The Secondary Current

In this method, only two consecutive samples are needed. It is very easy to implement this technique into a computer relay.

Assume that a fault current is of the form

$$i_1 = I_m \sin(\omega t_1) \tag{2}$$

$$i_2 = I_m \sin(\omega t_2) \tag{3}$$

$$\Delta i = i_2 - i_1$$

$$= I_m [\sin(\omega t_2) - \sin(\omega t_1)]$$

$$= I_m \sin\left(\frac{\omega \Delta t}{2}\right) \cos\left(\frac{\omega(t_2 + t_1)}{2}\right)$$

$$= I_m' \cos\left(\frac{\omega(t_2 + t_1)}{2}\right) \tag{4}$$

Where

$$\Delta t = t_2 - t_1$$

$$I_m' = I_m \sin\left(\frac{\omega \Delta t}{2}\right) \tag{5}$$

Thus the criterion for a saturation detector is

$$\Delta i > K I_m' \ ; \text{ saturation}$$

Where ω —— angular frequency of power system

I_m —— maximum magnitude of fault current

Δt —— sample interval

K —— safety factor greater than 1

In the criterion cited above, I_m must be determined off–line, and it is taken as the maximum fault current. If the CT has a remanence and may saturate

early at a low current level, Δi may be less than the threshold value and will fail to indicate CT saturation.

3.4.2 Change In Magnitude Of Positive Sequence Current Phasor

Basically, there are two ways to compute the magnitude of a current phasor. One is to use two current samples which are one–fourth cycle apart in time. The algorithm is as follows:

$$i = I_m \sin(\omega t)$$
$$I_m^2 = [i(t)]^2 + [i(t-T/4)]^2 \qquad (6)$$

If the current is in a purely sinusoidal waveform, this method works well. When the fault current contains a decaying DC component, or in some cases, when the fault current is severely biased from time axis, the phasor computed is not stable as shown in Fig. 3, unless the DC component can be removed by either a mimic circuit or a digital filter.

Another method to compute the phasor is to use the discrete Fourier Transformation (DFT). An appropriate data window must be chosen. In a computer relay, a half or a whole cycle window is used; however, for the CT saturation application, a half cycle window is still too long. It is appropriate to devise a quarter cycle or smaller window DFT.

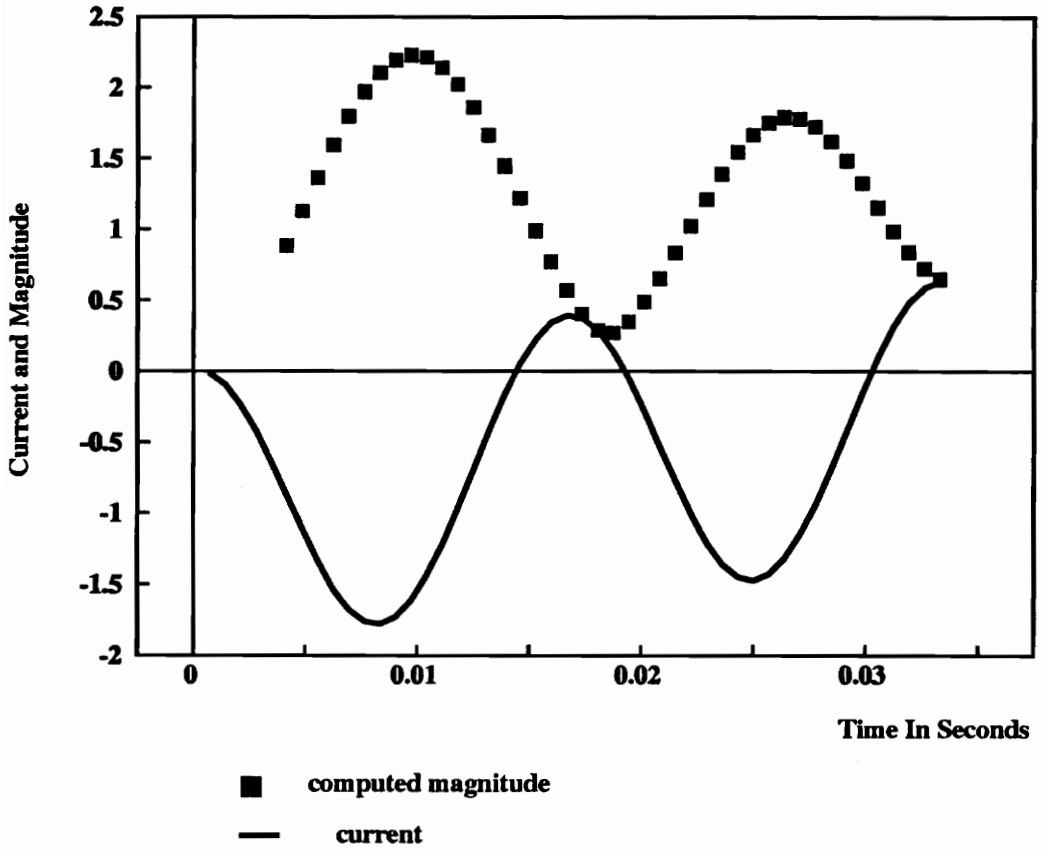

Fig. 3 Influence of DC Component on Magnitude of Current

Comparing the DFT method to the two–sample method, the DFT has the capability to filter some harmonics. A half cycle DFT is not able to filter out DC and even order harmonics. A quarter cycle DFT is severely affected by DC, and therefore has the same drawbacks as the two–sample method. And the DFT methods impose a greater computational burden.

No matter which methods are used in computing the phasor, the same criteria can be employed:

$$I_{m\,k} < K_m\, I_{max}$$

or

$$| I_{m\,k} - I_{m\,k-1} | < K_m\, I_{max}$$

Where $I_{m\,k}$ —— the current phasor at kth sample.

$I_{m\,k-1}$ —— the current phasor at (k–1)th sample.

I_{max} —— maximum magnitude of the current phasor.

K_m —— a safety factor less than 1.

I_{max} can be computed using presaturation samples under the assumption that CT saturation occurs after a quarter cycle, following a fault inception. Because of the decaying DC effect, this is not a reliable procedure. I_{max} can also be calculated off line. Usually it is so conservative as to affect the sensitivity of this criterion.

3.5 Parameter Estimation Method

Assume a fault current is of the form

$$i = I_m \cos(\omega t - \alpha + \varphi) - I_m \cos(\alpha - \varphi)\, e^{(-t/T_1)} \tag{7}$$

$$i = I_m \cos(\omega t) \cos(\alpha - \varphi) + I_m \sin(\omega t) \sin(\alpha - \varphi) - I_m \cos(\alpha - \varphi)\, e^{(-t/T_1)}$$

$$i = I_m \cos(\alpha - \varphi) [\cos(\omega t) - e^{(-t/T_1)}] + I_m \sin(\alpha - \varphi) \sin(\omega t)$$

Where α —— the voltage angle at fault inception

φ —— the impedance angle of the primary transmission line

T_1 —— the time constant of the primary transmission line

Let
$$f(t) = \cos(\omega t) - e^{(-t/T_1)} \tag{8}$$

$$X_1 = I_m \cos(\alpha - \varphi) \tag{9}$$

$$X_2 = I_m \sin(\alpha - \varphi) \tag{10}$$

In the expression of i, the time t is counted from the instant of fault inception , f(t) and sin(ωt) are known, X_1 and X_2 are unknown. Taking more than two consecutive samples and writing it in a matrix form, yields:

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix} = \begin{bmatrix} f(t_1) & \sin(\omega t_1) \\ f(t_2) & \sin(\omega t_2) \\ \vdots & \vdots \\ f(t_n) & \sin(\omega t_n) \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \tag{11}$$

This equation can be solved by using Least Squares theory. To estimate X_1 and X_2, two or more samples are needed. More samples provide greater accuracy. By assuming a fault current is free of saturation in the first quarter cycle after fault inception, and if a fault current is sampled twenty four times per cycle, then at least five or six samples of current can be used for the estimation.

After X_1 and X_2 are obtained, I_m and $(\alpha-\varphi)$ can be calculated as follows:

$$I_m = \sqrt{X_1^2 + X_2^2} \tag{12}$$

$$\alpha-\varphi = \tan^{-1} (X_1 / X_2) \tag{13}$$

Once I_m and $\alpha-\varphi$ are obtained, the next fault current sample can be predicted by the equation:

$$\hat{i}_{k+1} = X_1 [\cos (\omega t) - e^{(- t/T_1)}] + X_2 \sin (\omega t) \tag{14}$$

The criterion for CT saturation then becomes

$$| \Delta i | = | i_{k+1} | - | \hat{i}_{k+1} | \tag{15}$$

$$| \Delta i | > Ks\ I_{max}, \qquad \text{saturation}$$

Where Ks is a safety factor (less than 1), and I_{max} is as defined before.

i_{k+1} —— (k+1)th sample of secondary fault current

$\hat{i}_{k+1}$ —— the predicted secondary current at the (k+1)th sample

The fault current formula does not account for harmonics, therefore in UHV applications an additional filter may be needed, or the harmonics may be accommodated into the safety factor. The primary time constant T_1 ($X/\omega R$) must be obtained off–line, as it depends on the primary system connections. Since the primary system may change from time to time, it is difficult to give an exact value for T_1. Error in T_1 affects the decaying rate of the DC component in the predicted current. Note that in the fault current formula, time t starts from fault inception. A fault detector can determine in which interval (t_k, t_{k-1}) the fault occurs, but it can not determine the exact instant of the occurrence of the fault. The error in t may shift the predicted current from the secondary current phase. These errors may induce large errors in the estimation, hence this method is not very reliable.

It is well known that the least squares method only works well on good data. If bad data exists, the result from least square will be contaminated. Even with a single bad data, the result may be ruined. In power system state estimation, the bad data are considered to come from remote communication channels, meter calibrations, parameters, transients and so on. However, in this application of the least squares method, only local data are used, there would not be as many sources of bad data as in state estimation. In fact, bad data have not been taken into account in computer relays so far.

In the method just described above, only presaturation current samples are used in the parameter estimation. There could be an alternative: both the presaturation and the postsaturation current samples could be used. Under the assumption that the secondary current is free of saturation within a quarter cycle

after fault inception, five or six samples of a fault current can be used in estimating I_m. The I_m is stored for later use as magnitude of the periodical component of fault current. If the CT saturates, five samples of presaturated current and one postsaturated current are used in the estimation. Since postsaturated current is a very low value, so it would make the estimation collapse, and the new I_m will be a low value. Comparing the new I_m to the stored I_m against a threshold value similar to those described in 3.4 , CT saturation can be revealed. This method, in general, is sensitive to high current saturation, and errors in the fault time t and the primary time constant T_1 would not much affect this criterion, because only the two computed magnitudes of fault current are compared instead of both the magnitudes and phase angles.

3.5 Change In Slope Of Current

This is a new technique to detect CT saturation. Instead of checking the sample difference or phasor magnitude of a secondary current, a change in the slope of the secondary current is investigated.

Once again, we assume that the secondary current is sinusoidal in waveform, as shown in Fig. 4.

$$i = I_m \sin(\omega t)$$

Its first derivative then is

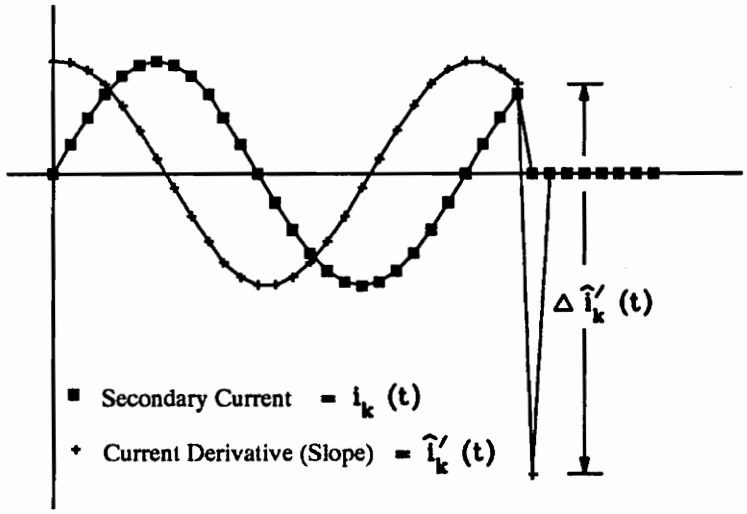

Fig. 4 Current and Current Slope Relationship

$$i' = \omega I_m \cos(\omega t) \tag{16}$$

Or

$$\hat{i}' = \frac{i'}{\omega} \tag{17}$$

$$= I_m \cos(\omega t)$$

Replacing the derivative by a differential equation yields,

$$\hat{i}'_k = \frac{1}{\omega \Delta t}(i_k - i_{k-1}) \tag{18}$$

$$= \frac{1}{\omega \Delta t}[I_m \sin(\omega t_k) - I_m \sin(\omega t_{k-1})]$$

$$= \frac{I_m}{\omega \Delta t} 2 \cos\left(\frac{\omega t_k + \omega t_{k-1}}{2}\right) \sin\left(\frac{\omega t_k - \omega t_{k-1}}{2}\right)$$

$$\hat{i}'_k = \frac{2 I_m}{\omega \Delta t} \cos\left(\frac{\omega t_k + \omega t_{k-1}}{2}\right) \sin\left(\frac{\omega \Delta t}{2}\right) \tag{19}$$

$$\hat{i}'_{k+1} = \frac{2 I_m}{\omega \Delta t} \cos\left(\frac{\omega t_k + \omega t_{k+1}}{2}\right) \sin\left(\frac{\omega \Delta t}{2}\right) \tag{20}$$

$$\Delta \hat{i}' = \hat{i}'_{k+1} - \hat{i}'_k$$

$$= \frac{2 I_m}{\omega \Delta t} \sin\left(\frac{\omega \Delta t}{2}\right) \left[\cos\left(\frac{\omega t_k + \omega t_{k+1}}{2}\right) - \cos\left(\frac{\omega t_k + \omega t_{k-1}}{2}\right)\right]$$

$$\hat{\Delta i}' = \frac{2 I_m}{\omega \Delta t} \sin \left(\frac{\omega \Delta t}{2} \right) \left[-2 \sin (\omega t_k) \sin \left(\frac{\omega \Delta t}{2} \right) \right] \tag{21}$$

$$\hat{\Delta i}' = - \left[2 I_m \frac{\sin \left(\frac{\omega \Delta t}{2} \right)}{\frac{\omega \Delta t}{2}} \sin \left(\frac{\omega \Delta t}{2} \right) \right] \sin (\omega t_k) \tag{22}$$

Since $\lim_{\Delta t \to 0} \left[\frac{\sin \left(\frac{\omega \Delta t}{2} \right)}{\frac{\omega \Delta t}{2}} \right] = 1$, then $\hat{\Delta i}'$ can be reduced to

$$\hat{\Delta i}' \approx -2 I_m \sin \left(\frac{\omega \Delta t}{2} \right) \sin (\omega t_k) \tag{23}$$

The magnitude of $\hat{\Delta i}'$ is $2 I_m \sin \left(\frac{\omega \Delta t}{2} \right)$, it is proportional to I_m. Since I_m varies with system conditions, the threshold value is determined by taking the magnitude of the maximum external fault current I_{max}, which is the periodical component of the fault current.

$$\hat{\Delta i}'_{max} = 2 I_{max} \sin \left(\frac{\omega \Delta t}{2} \right) \tag{24}$$

Then the criterion for this method is

$| \hat{\Delta i}' | > M_1 \hat{\Delta i}'_{max}$ saturation

M_1 is a safety factor, and is appropriately selected to account for DC offset and other errors.

This method needs only three consecutive samples of secondary current. Its computations are very simple and suitable for higher sampling frequency.

Examining the behavior of this method in detail, if the CT saturates between second and third sample, although the current samples are low, its derivatives are relatively high, and the presaturated and postsaturated derivatives are of different polarities. $\Delta\hat{i}'$ is then the sum of the absolute values of two derivatives. When the CT saturates around the current peak, its presaturated derivative is very low, but the postsaturated derivative is very high, and $\Delta\hat{i}'$ remains high in magnitude. From the discussions just cited, it can be seen that this method always has the same high sensitivity to CT saturation, while the other methods discussed before can only detect high current saturation.

As is the case for all other methods of saturation detection, this method easily detects a sharp drop when CT saturation occurs; however, with the antialiasing filter, the collapse of a secondary current will be softened so that the CT saturation detector may fail to reveal CT saturation, especially in the low current region. There may be a few ways to overcome this problem. One possible way is to increase the sampling rate, say to 1440 Hz, such that the cutoff frequency of a antialiasing filter increases to 600—700 Hz, the softness would be alleviated. The other way is to use raw current samples.

The high frequency sampling rate is an attractive option in a bus relay. It not only solves the problem that antialiasing filters create, but it also is able to detect early (one–eighth cycle) saturation in case of high remanence. This is the expected result, as long as there are two good samples, this detector can reveal CT saturation.

CHAPTER FOUR

Percentage Differential Current Principle

As stated in Chapter one, the differential scheme may fail in the presence of CT saturation. But the misoperation of this scheme can be prevented provided the occurrence of saturation can be correctly identified. The conventional formula for the percentage differential current principle is revised by using the new saturation detector. The operating current is the absolute sum of all currents, which is the absolute differential current. The restraint current consists of two terms, the first one is the sum of the absolute currents, the second is related to CT saturation.

$$\left| \sum_{j=1}^{n} i_j \right| - K_1 \sum_{j=1}^{n} |i_j| - K_2 \, RES \geq I_o$$

$RES = 0$; no saturation

$RES = I_{max}$; saturation

Where K_1, K_2 are constants, and

I_o is a threshold value

RES is the restraint current due to CT saturation and

n is the number of feeders

Conventionally, K_1 should be set high enough in case of CT saturation; however, it makes the criterion less sensitive to an internal fault. In this revised formula, K_1 can be set low, at say 20% . RES is set to zero if no CT saturates, otherwise RES is the maximum external fault current or differential current. K_2 is greater than 1.

In the normal case of an external or internal fault, if none of the CTs saturates, RES is equal to zero, and there is a low restraint current in the criterion. This makes the criterion more sensitive to an internal fault. When the CT saturates, RES increases to the maximum fault current such that the differential scheme is blocked.

The logic for the percentage differential scheme is shown in Fig. 5. When the kth samples of currents come in, if the criterion is satisfied, a tripping counter will be incremented by 1, otherwise it will be decreased by 1. When the tripping counter reaches six, a trip signal will be issued. For the sampling rate of 1440 Hz, six samples correspond to a quarter cycle. The differential scheme is therefore expected in most cases, to make a trip decision in a quarter cycle.

It is obvious that if a CT saturates in the case of an internal fault, the percentage differential scheme will be blocked. This is not expected. Fortunately, CT saturation is more likely in close–in external fault. Therefore, in general, the

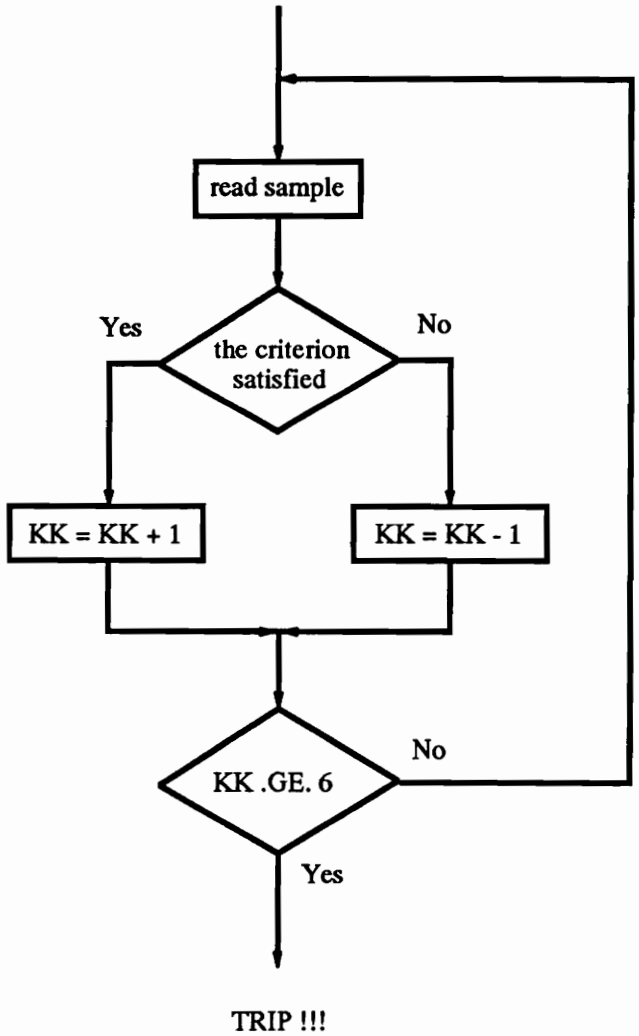

Fig. 5 Percentage Differential Scheme

trip decision for an internal fault will not be affected much by the saturation blocking scheme. Once a CT really saturates in an internal fault before the tripping decision is made, the percentage differential scheme will be disabled and the fault will be cleared through the phase comparison scheme or through a back–up protection system.

CHAPTER FIVE

Phase Comparison Scheme

Conventionally, phase comparison schemes may include positive half phase comparison, or negative half phase comparison, or both. In this study, both positive and negative half phase comparison schemes are used. These two schemes basically work independently. There is a separate trip counter for each. Whenever a trip counter increments continuously to eight, a tripping signal will be issued, otherwise the phase comparison scheme will be blocked until the next half cycle decision. Since a power system is not homogeneous, the currents of all feeders may not be exactly in phase for an internal fault. They may differ by up to 60° from each other, corresponding to 4 samples with respect to a 1440 Hz sampling rate. Therefore, the tripping threshold is set to eight.

As mentioned before, CT saturation causes the secondary current to be distorted such that the phase comparison scheme can not work properly. The distorted polarity of currents can be corrected with a CT saturation detector.

The logic of the phase comparison scheme is shown in Fig. 6. When CT saturation sets in, the CT saturation detector will reflect this change and find which CT is saturated. Then the sign of the previous unsaturated sample is determined and given to the saturated samples to follow. A back counting scheme is used to determine the number of saturated samples requiring the generated polarity. As long as the counter is less than or equal to twelve samples, the determined polarity for the incoming saturated sample is preserved. The natural signs of currents are used in phase comparison for non–saturated CTs. When a CT comes out of saturation, the corresponding counters are reset. After all the polarities of currents in the feeders are determined, the phase comparison procedure is initiated.

It should be noted that in case of an internal phase–to–phase fault, all fault currents flow into the bus, while the load currents may still flow out of the bus, hence the phase comparison scheme may fail to give a trip signal. In order to avoid this, only those current samples, whose magnitudes are greater than the maximum load current, should be used in the phase comparison scheme.

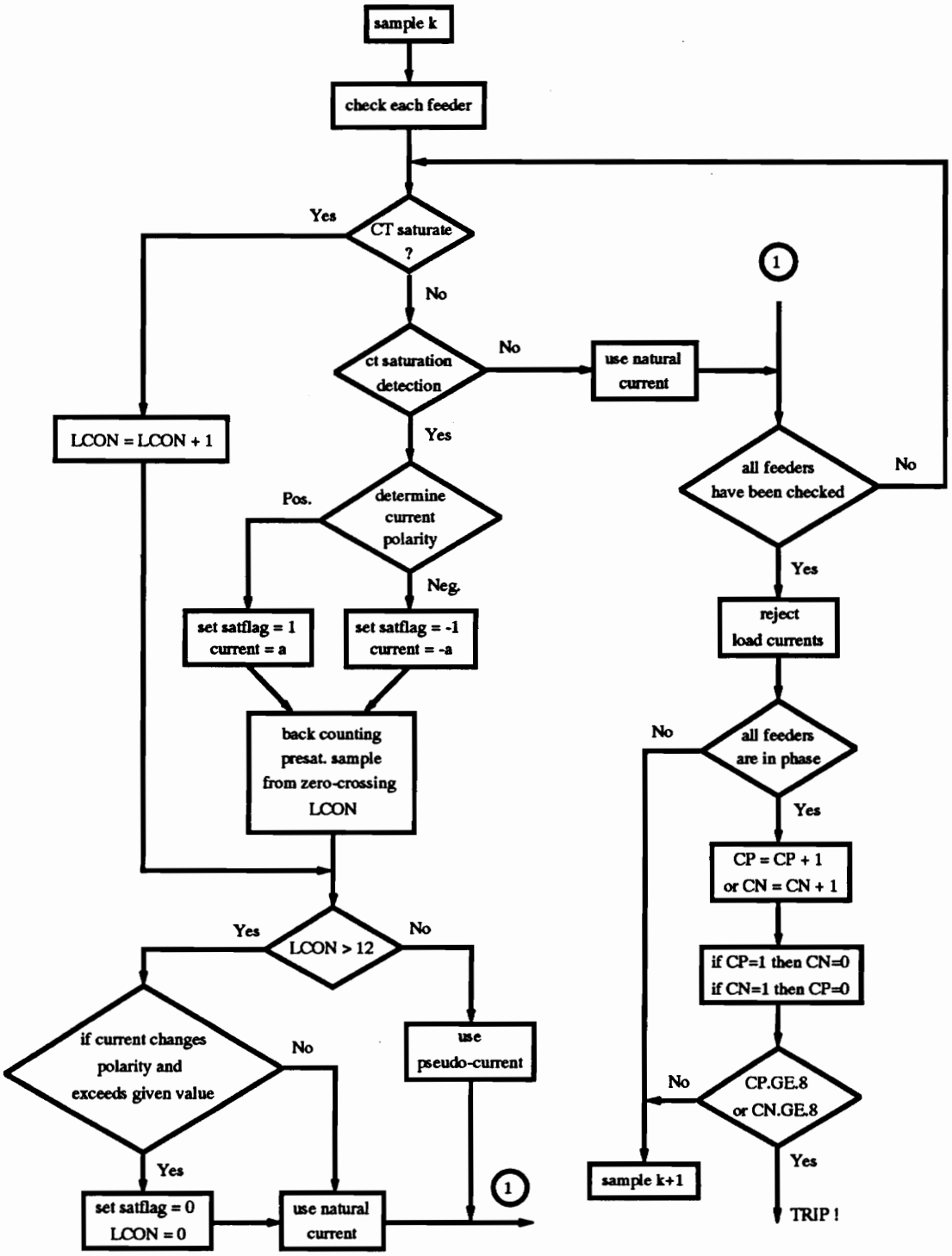

Fig. 6 Phase Comparison Scheme

CHAPTER SIX

Proposed Single Bus Protection System

The proposed relaying system for a single bus consists of a fault detector, CT saturation detectors, a percentage differential scheme, a phase comparison scheme, and tripping counters. The sampling rate of 1440 Hz is employed. The percentage differential scheme acts for primary protection and the phase comparison scheme as back up. The percentage differential scheme is designed to work at a quarter cycle, while the phase comparison scheme works at a half cycle.

The fault detector works on the overcurrent principle: as long as one or more of all the currents in the feeders exceeds a specified value, then a possible fault will be assumed, and the CT saturation detector and the percentage differential and phase comparison schemes are initiated.

Before CT saturation is detected, both the percentage differential and phase comparison schemes are run in parallel. K_1 is a trip counter for the differential

scheme, and K_{2p} and K_{2n} are counters for the phase comparison scheme. K_{2p} counts the number of coincident phases on the positive half cycle, whereas K_{2n} counts on the negative half cycle. If either of these trip counters reaches its threshold value, a trip signal will be issued.

If CT saturation is detected before K_1 reaches six, the percentage differential scheme will be disabled, while the phase comparison scheme continues. In the event that not enough samples are available for K_{2p} (K_{2n}) to reach a trip value of eight, K_{2n} (K_{2p}) is activated for the incoming half cycle. Meanwhile, K_{2p} (K_{2n}) is reset to zero. The differential scheme could be reactivated when all CTs have come out of saturation. This provides another opportunity for the differential scheme to clear an internal fault as soon as possible. If both the differential and phase comparison schemes do not issue a tripping decision, then the bus protection system will be blocked until a fault disappears. The proposed bus protection scheme could work all the time; however, due to the DC component in the fault current, the CT may saturate more severely in the second cycle as opposed to the first. There may thus exist a risk for bus relay to make a wrong decision. Moreover, in most cases, the proposed bus protection scheme is expected to give a correct decision in one cycle, and there is no need to waste time rechecking. If an internal fault really occurs and the bus relay fails to trip, then the back–up protection system must function.

The flowchart of the proposed bus protection scheme is shown in Fig. 7.

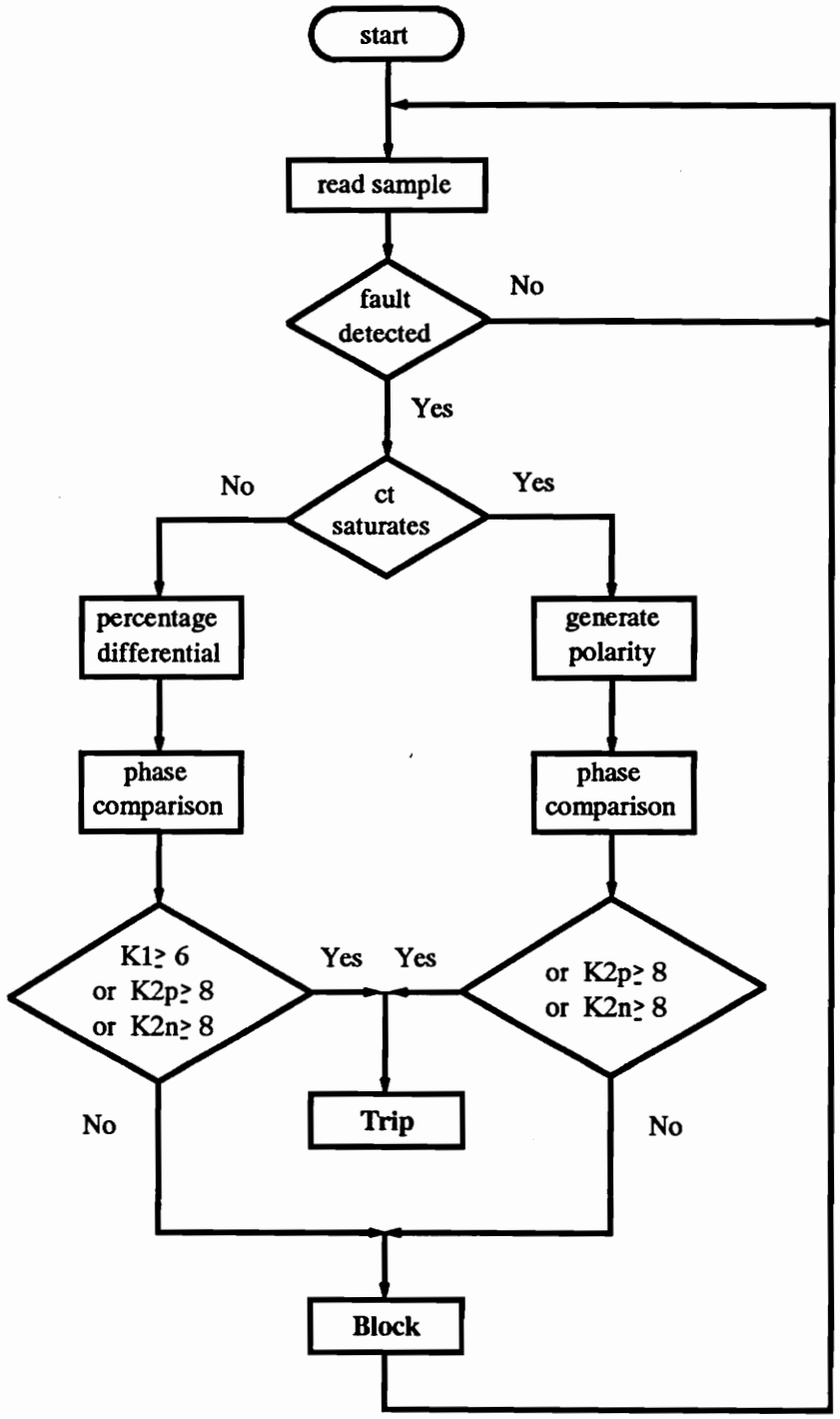

Fig. 7 Single Bus Protection System Scheme

CHAPTER SEVEN

Simulation Results

7.1 Test System Model

The proposed bus protection scheme has been coded in Fortran, and has been tested against data from the EMTP system model. The EMTP primary system model was basically constructed using TVA data in which there are five generators and one load as shown in Fig. 8. In some test cases, the primary parameters were changed so that the bus relay could see very severe conditions.

The key part of the EMTP secondary system model is the current transformer. In computer relays, it is not possible to differentially connect the secondaries of all CTs in the same phase. Each secondary is measured separately, in other words, all the secondaries are independent.

In the EMTP simulation, there is a nonlinear inductor element which can

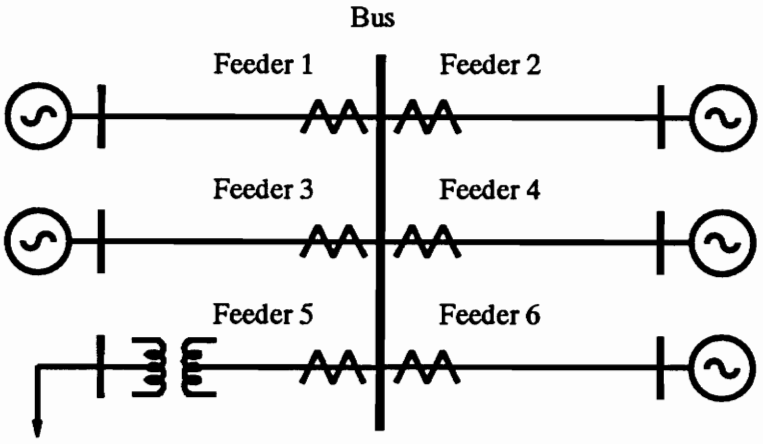

Fig. 8 Simulated Primary System

be used for simulating a hysteretic inductor. If a magnetizing characteristic or V–I curve is available, it can be converted into a Ψ–i curve by using the AUX program (in EMTP). Thus a saturable CT model can be built as in Fig. 9. The V–I curve may be obtained from either the manufacturer or by testing. In this study, in order to obtain CT saturation, the V–I curve is artificially assumed. For a fixed V–I curve, CT saturation can be obtained by setting a remanence or changing the impedance of leads and the burden.

A diagram of the CT model is shown in Fig. 9.

Actually, a CT most likely saturates in one feeder when a fault occurs. In this study saturable CT models are used in only two feeders. Although many saturable CTs can be simulated, not much benefit can be obtained from the increased complexity.

Two stage RC antialiasing filters are used in simulations with the cut–off frequency being 600 Hz.

7.2 Simulation Results

The proposed bus protection scheme has been subject to many tests, but only eight cases and their results are presented. These cases are tabulated as follows.

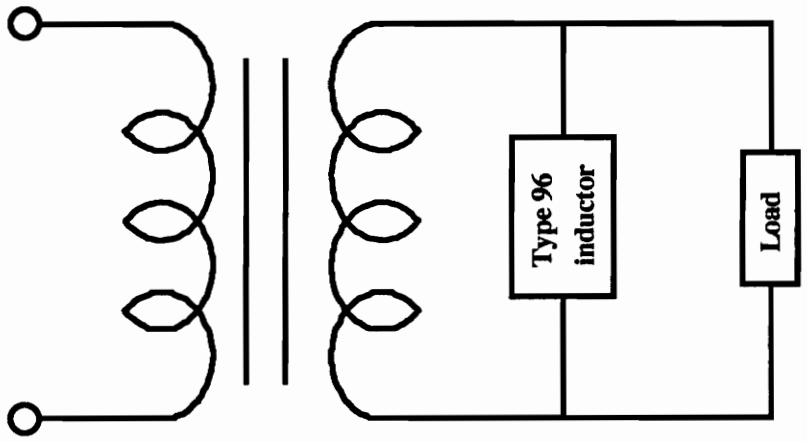

Fig. 9 Saturable CT Model in EMTP

internal fault	external fault
phase A to ground	phase A to ground
phase BC shorted	phase BC shorted
phase BC to ground	phase BC to ground
three phase fault	three phase fault

Fig. 10 shows a phase a to ground fault on the bus. Only CTs on feeder 6 are assumed to saturate. The fault occurs when the source voltage is at zero, while the current is at maximum, such that the fault current contains a high DC component, which easily leads to CT saturation. A CT on phase A of feeder 6 saturates at the sixth sample. The saturation detector correctly reveals the occurrence of the saturation and identifies the saturated current transformer. The polarity of the distorted current is corrected and, eventually, the phase comparison scheme trips at the ninth sample.

Figs. 11(a) and 11(b) show a case in which the fault occurs on the bus, and phases B and phase C are shorted. Current transformers of feeder 6 are assumed to saturate. The fault occurs at the voltage maximum of phase A. The CTs of phases B and C saturate, with phases B and C saturating at the fifth sample after the fault. Both percentage differential schemes for phases B and C are blocked. The phase comparison schemes give a trip signal at the ninth sample for phase B and at the eighth sample for phase C.

Figs. 12(a) and 12(b) show an internal phases B to C to ground fault. The fault occurs at the voltage maximum of phase A. Saturable CTs are only used in feeder 6. Phase B saturates at the sixth sample, phase C at the fourth

sample, and the saturation detectors work correctly. The percentage differential schemes for phases B and C are blocked. The phase comparison schemes trip phase B at the tenth sample, phase C at the eighth sample.

Figs. 13(a), 13(b) and 13(c) show an internal three phase fault case. Again the CTs on feeder 6 are saturable. The fault occurs when the voltage of phase A reaches zero. Phase A saturates at the fifth sample, phase B at the third sample, and phase C at the fourth sample. The saturation detectors work correctly for all three phases. Note that for phase B the saturation detector reveals saturation at one–eighth cycle. Since all three CTs saturate before the sixth sample, the percentage differential schemes for the three phases are blocked while the phase comparison schemes trip the three phases at the eighth sample.

Fig. 14 shows an external phase A to ground fault on feeder 5. The fault occurs at the zero voltage of phase A. The CTs on feeders 5 and 6 are saturable. Phase A of feeder 5 saturates at the fifth sample while the phase A of feeder 6 saturates at the third sample. The saturation detectors work correctly so that the percentage differential scheme is blocked and the phase comparison also makes a correct decision. Even with two CTs saturating, the bus protection system still works properly; no trip signal is issued.

Figs. 15(a) and 15(b) show an external phases B and C shorted on feeder 5. The fault occurs when the voltage of phase A is at maximum. The CTs of feeder 5 are assumed to be saturable. The CTs of phases B and C both saturate at the sixth sample after fault. Both percentage differential schemes for phases B and C

are blocked. The in–phase signal for phases B and C both do not reach the tripping threshold, hence the phase comparison schemes do not give a trip signal.

Figs. 16(a) and 16(b) show an external phase B to C to ground fault on feeder 5. The fault occurs at the voltage maximum of phase A. Saturable CTs are only used in feeder 5. Phase B saturates at the seventh sample, and phase C at the fifth sample. The saturation detectors work correctly so that the percentage differential and phase comparison schemes work properly and no tripping decisions are made.

Figs. 17(a), 17(b) and 17(c) show an external three phase fault on feeder 5. The CTs on feeder 5 and 6 are saturable. The fault occurs when the voltage of phase A reaches zero. For feeder 5, phase A saturates at the fifth sample, phase B at the third sample, and phase C at the fourth sample. For feeder 6, phase A saturates at the fifth sample, phase B at the fourth sample, and phase C at the fourth sample. For all three phases, saturation detectors work correctly so that the bus protection system does not misoperate.

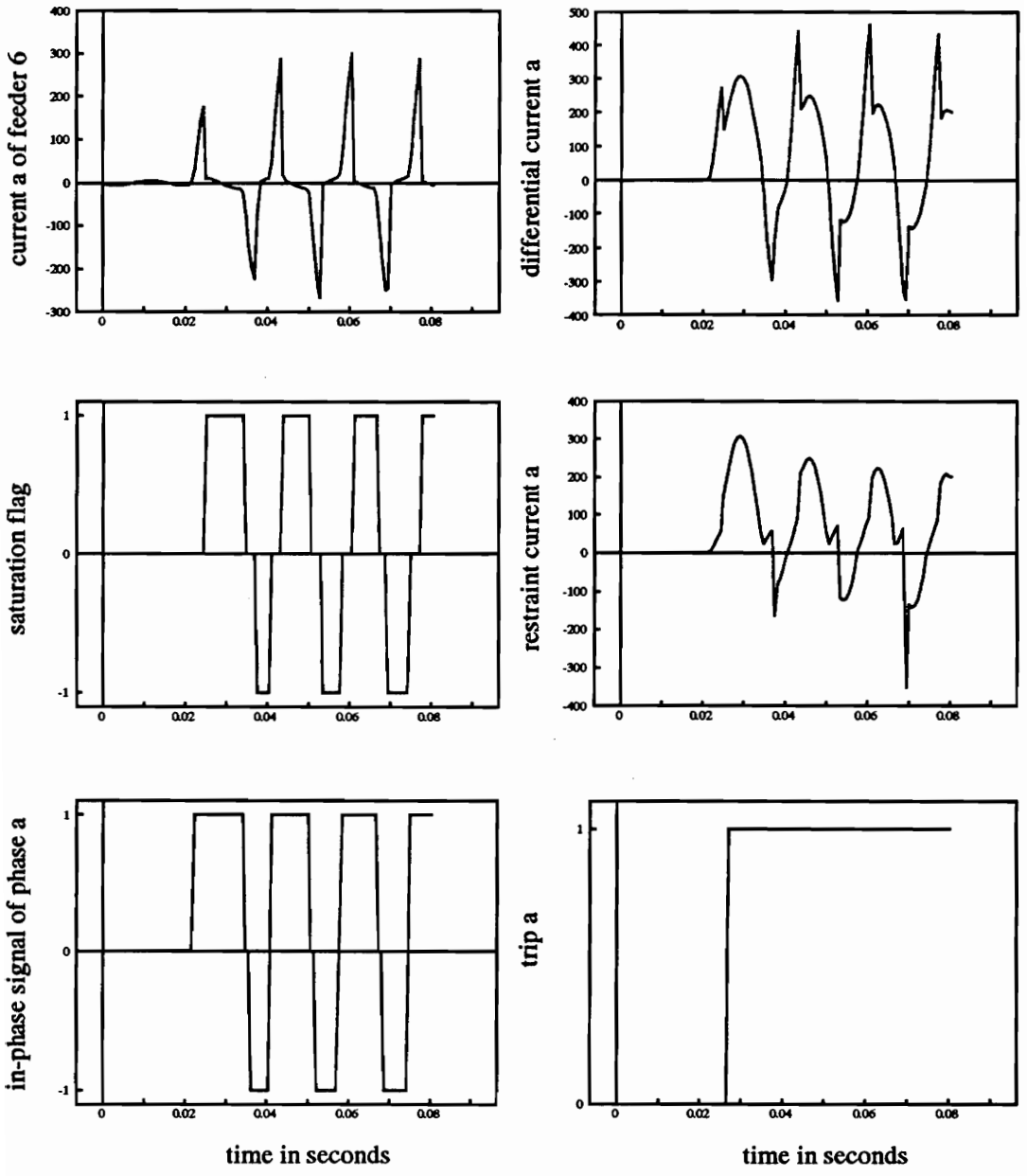

Fig. 10 An Internal Phase A to Ground Fault

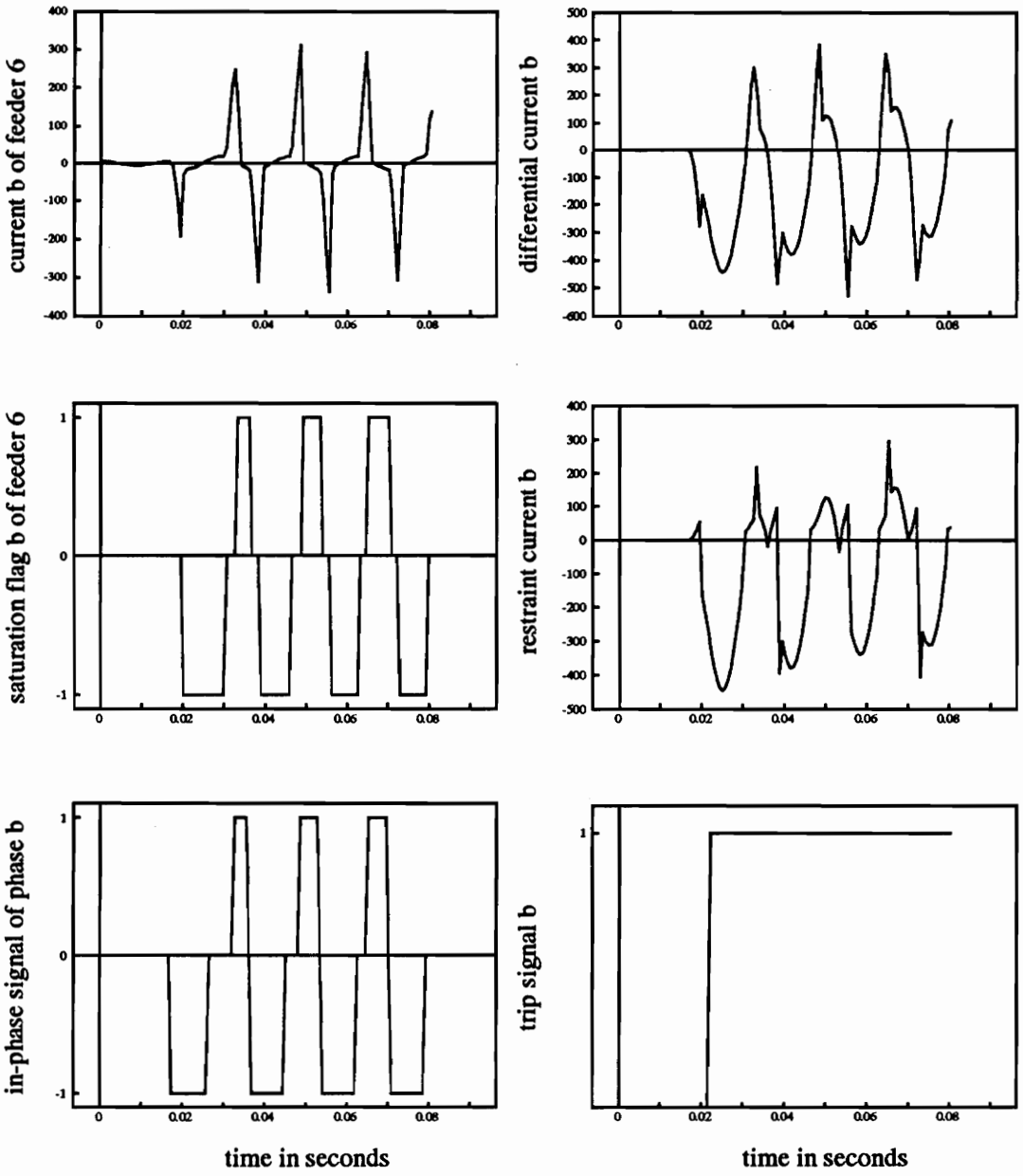

Fig. 11(a) Phase B of an Internal Phase B&C Short Circuit

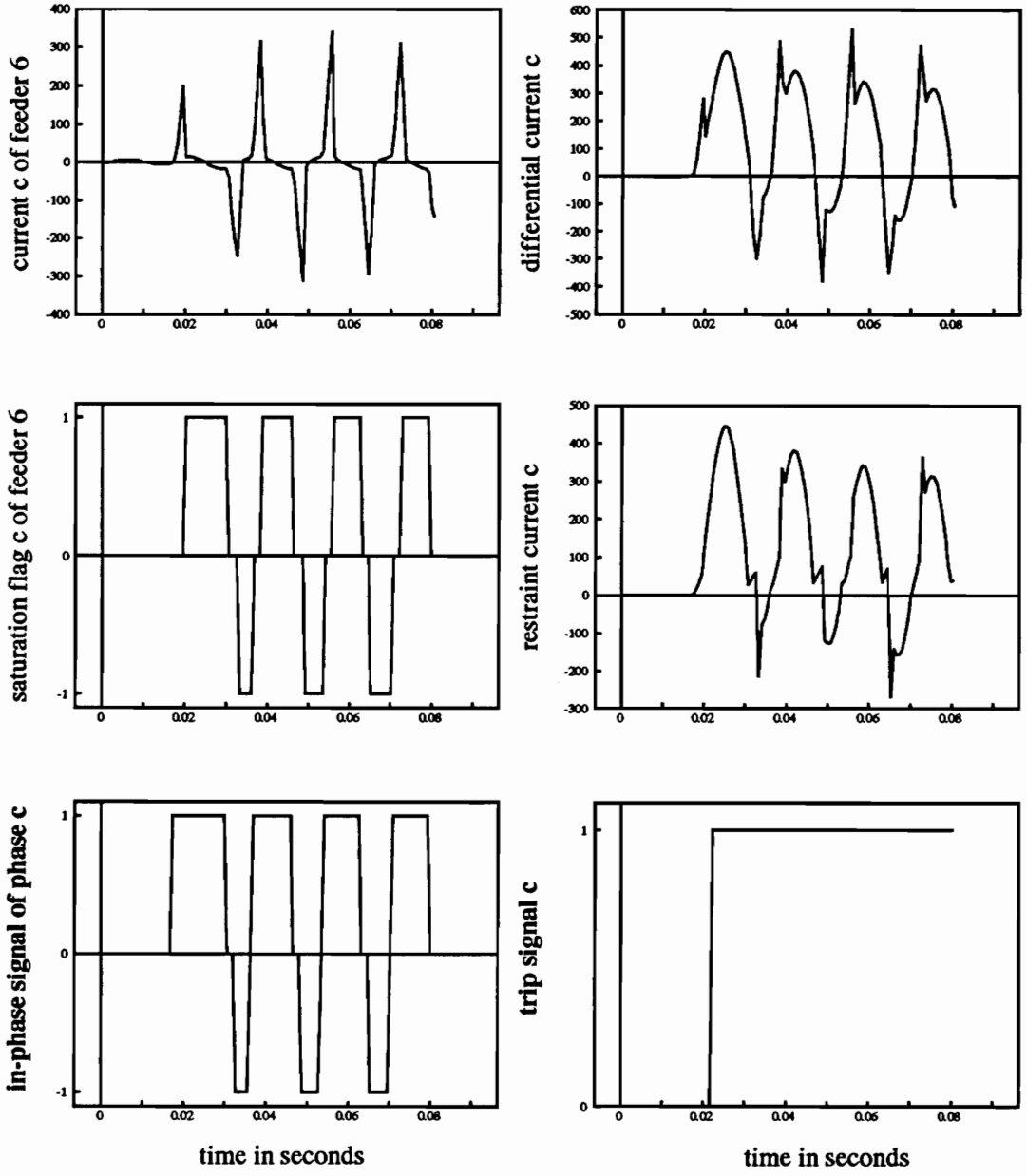

Fig. 11(b) Phase C of an Internal Phase B&C Short Circuit

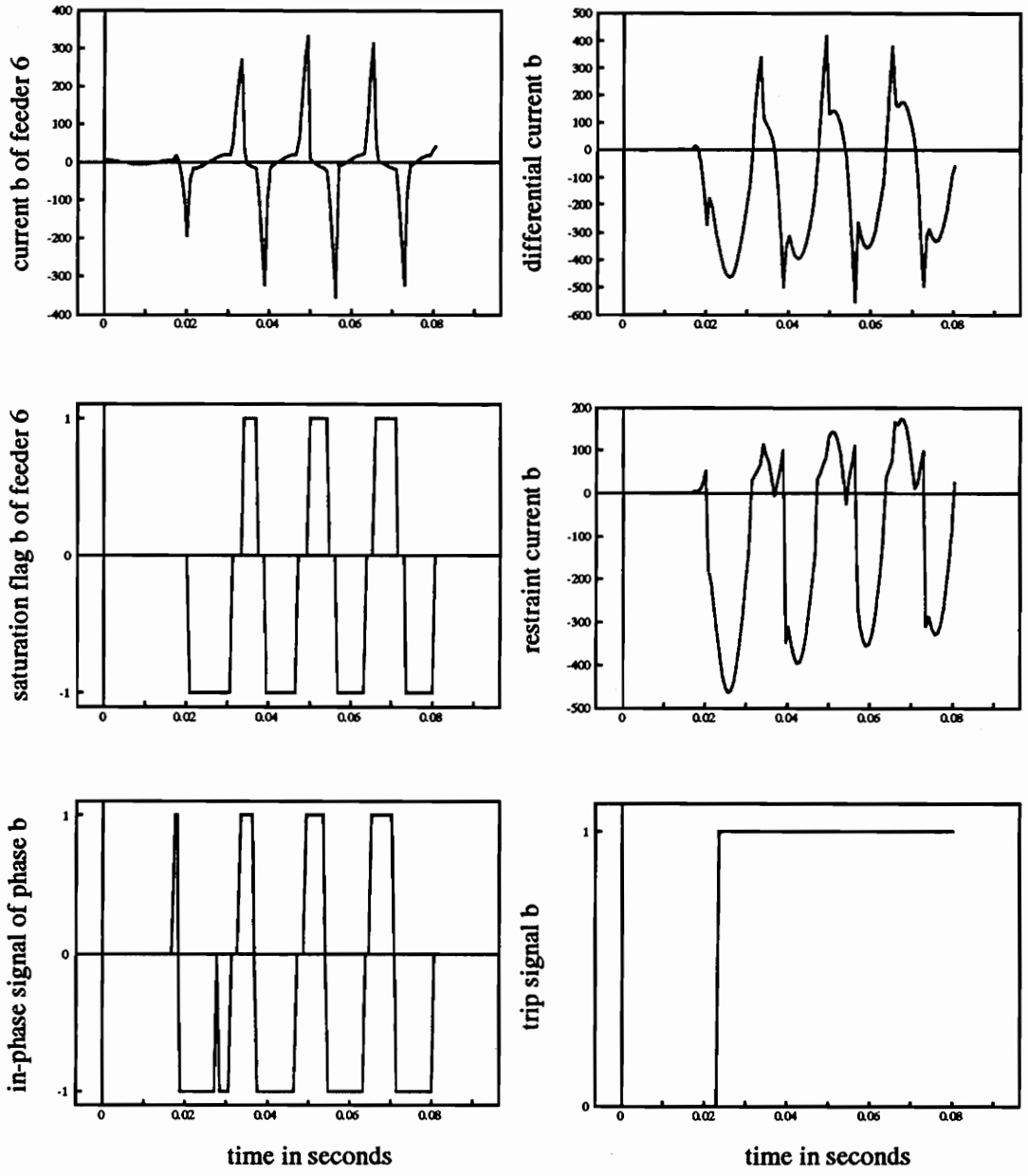

Fig. 12(a) Phase B of an Internal Phase B&C to Ground Fault

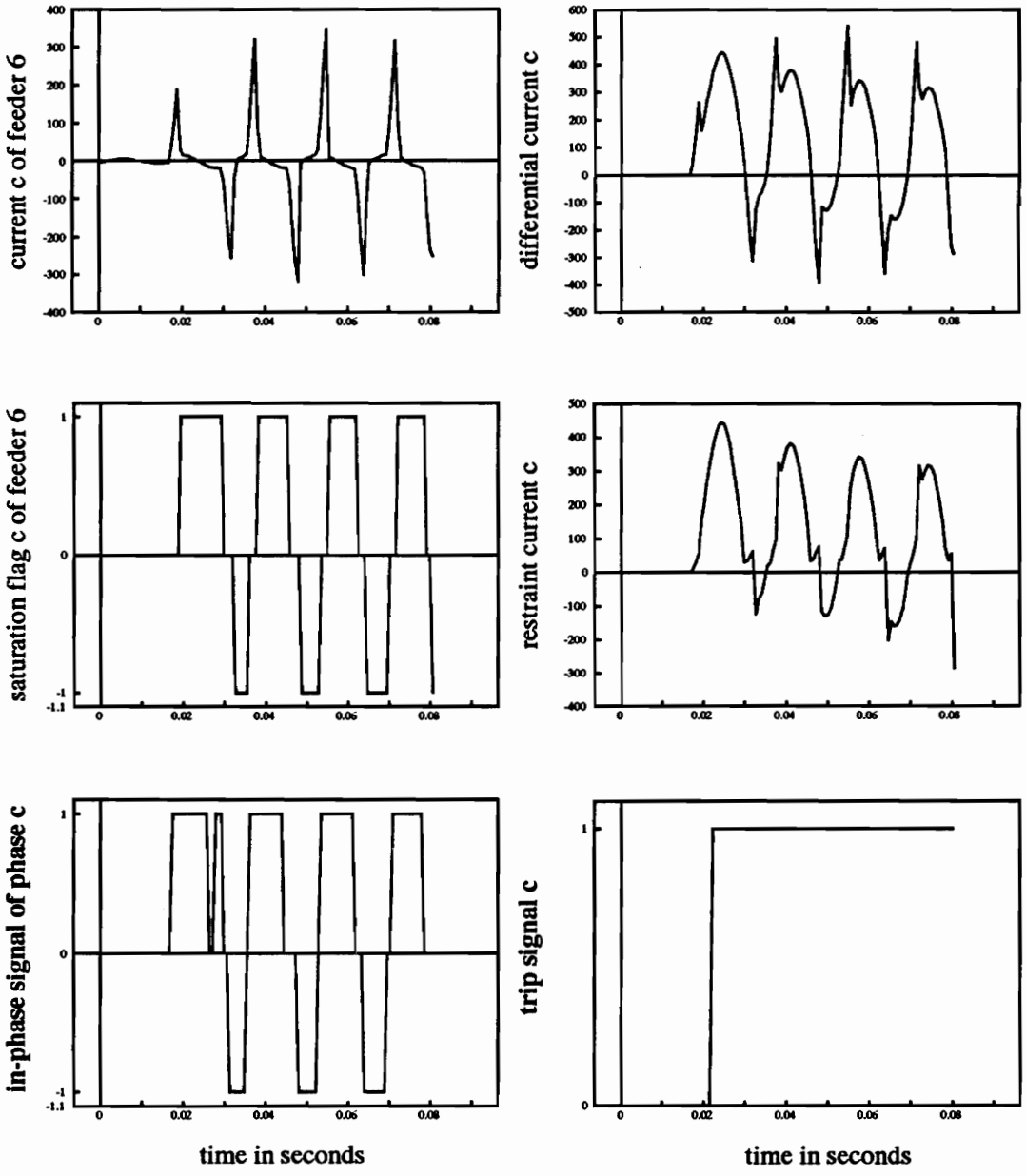

Fig. 12(b) Phase C of an Internal Phase B&C to Ground Fault

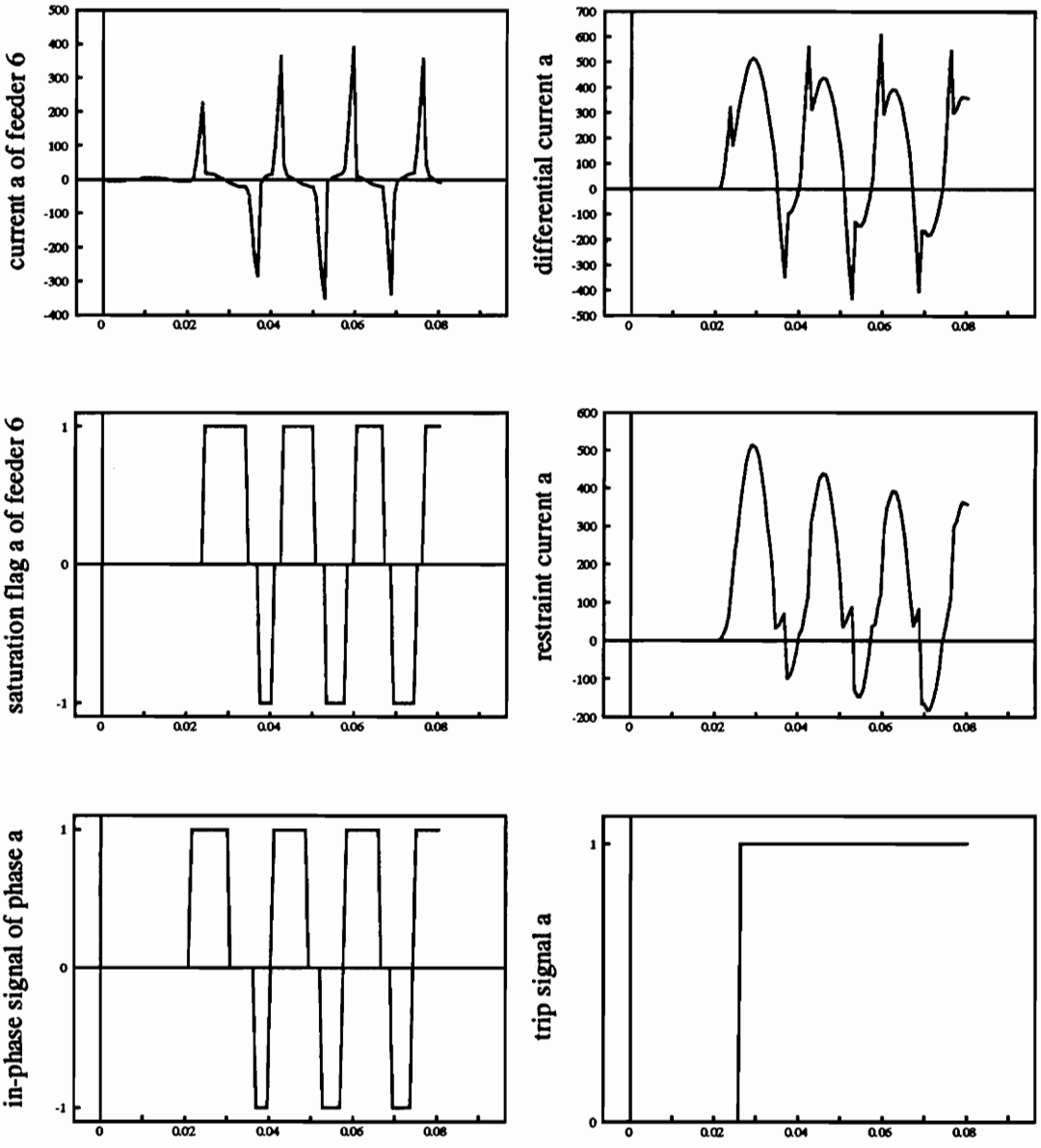

Fig. 13(a) Phase A of an Internal Three Phase Fault

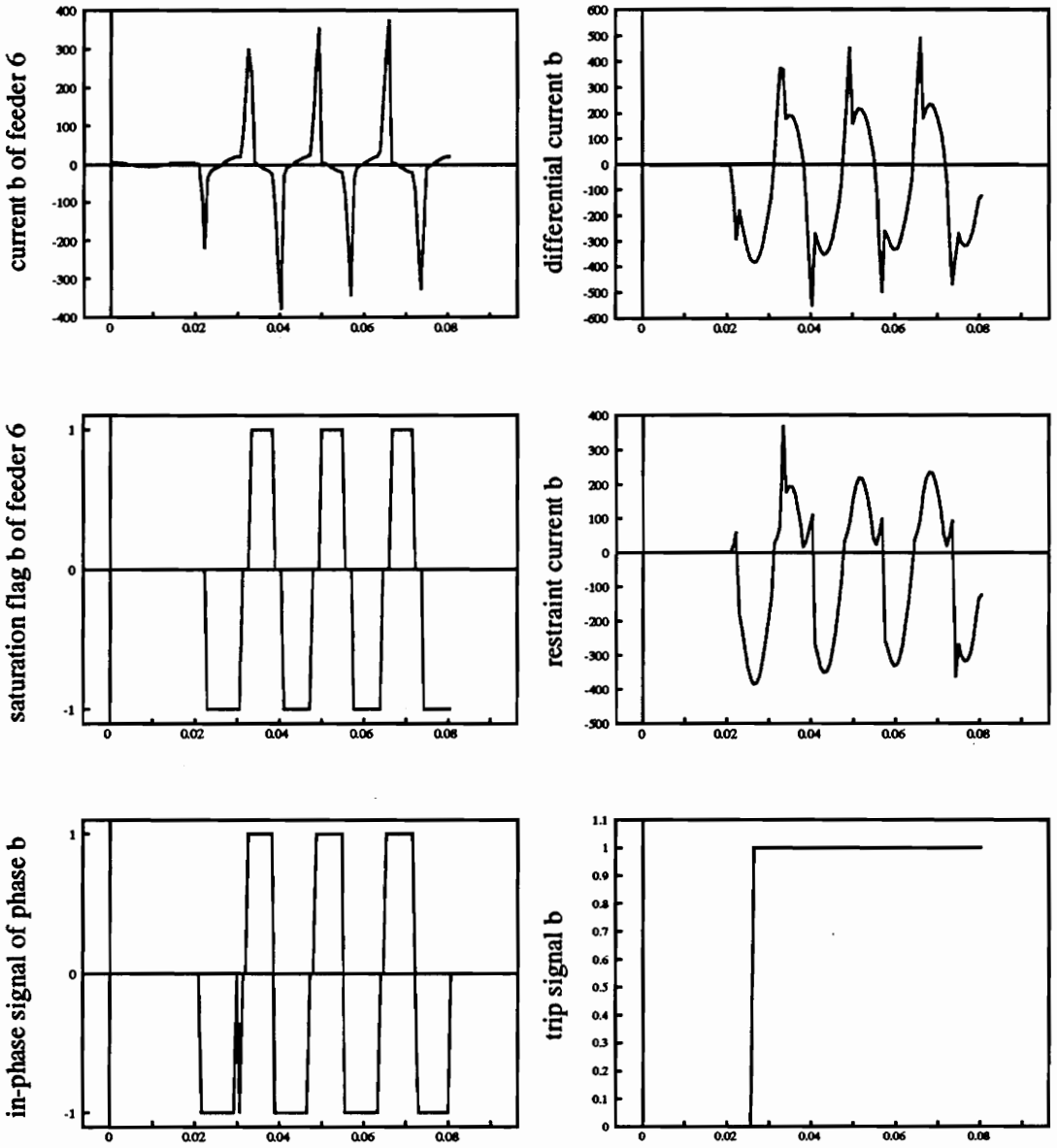

Fig. 13(b) Phase B of an Internal Three Phase Fault

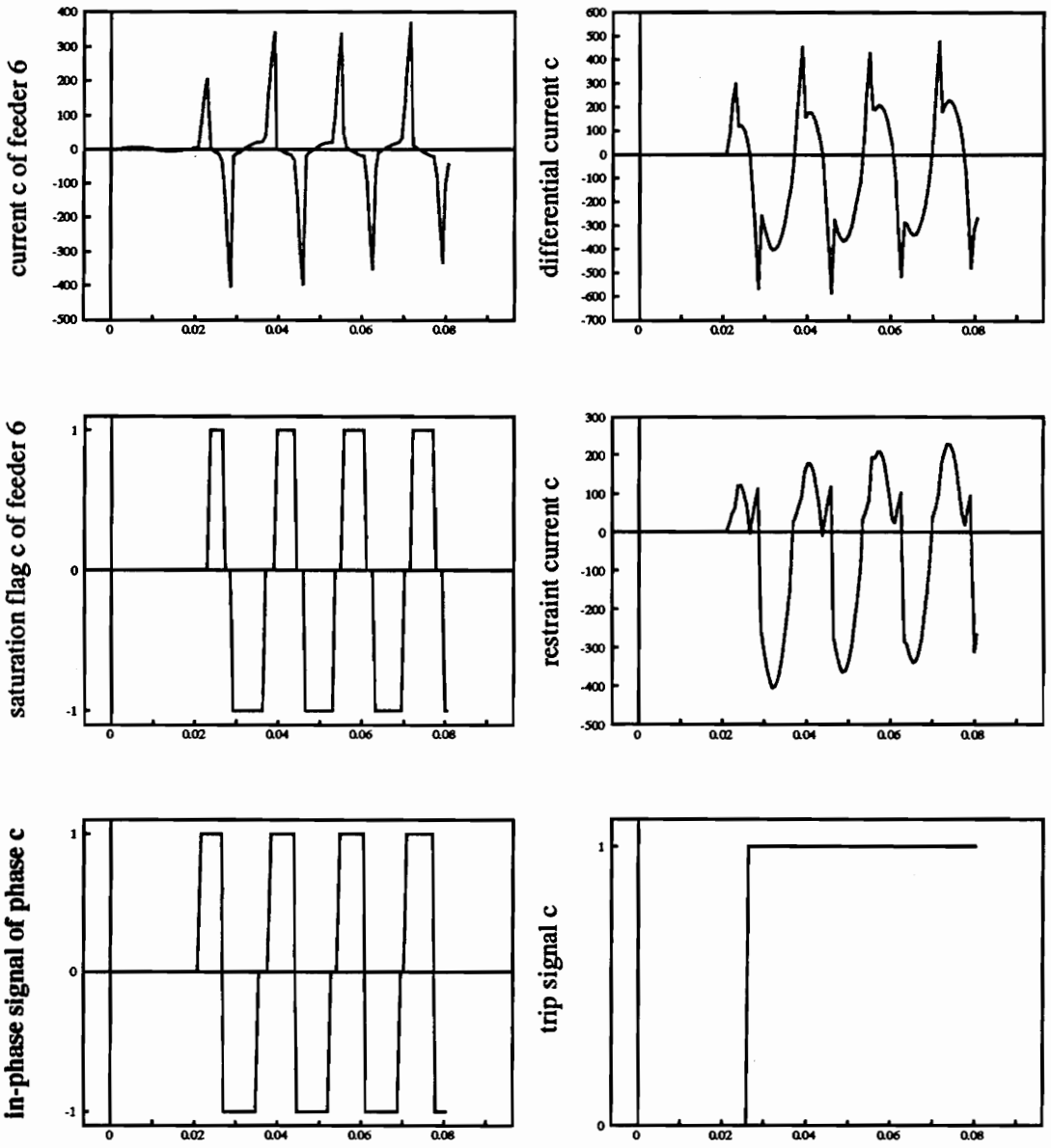

Fig. 13(c) Phase C of an Internal Three Phase Fault

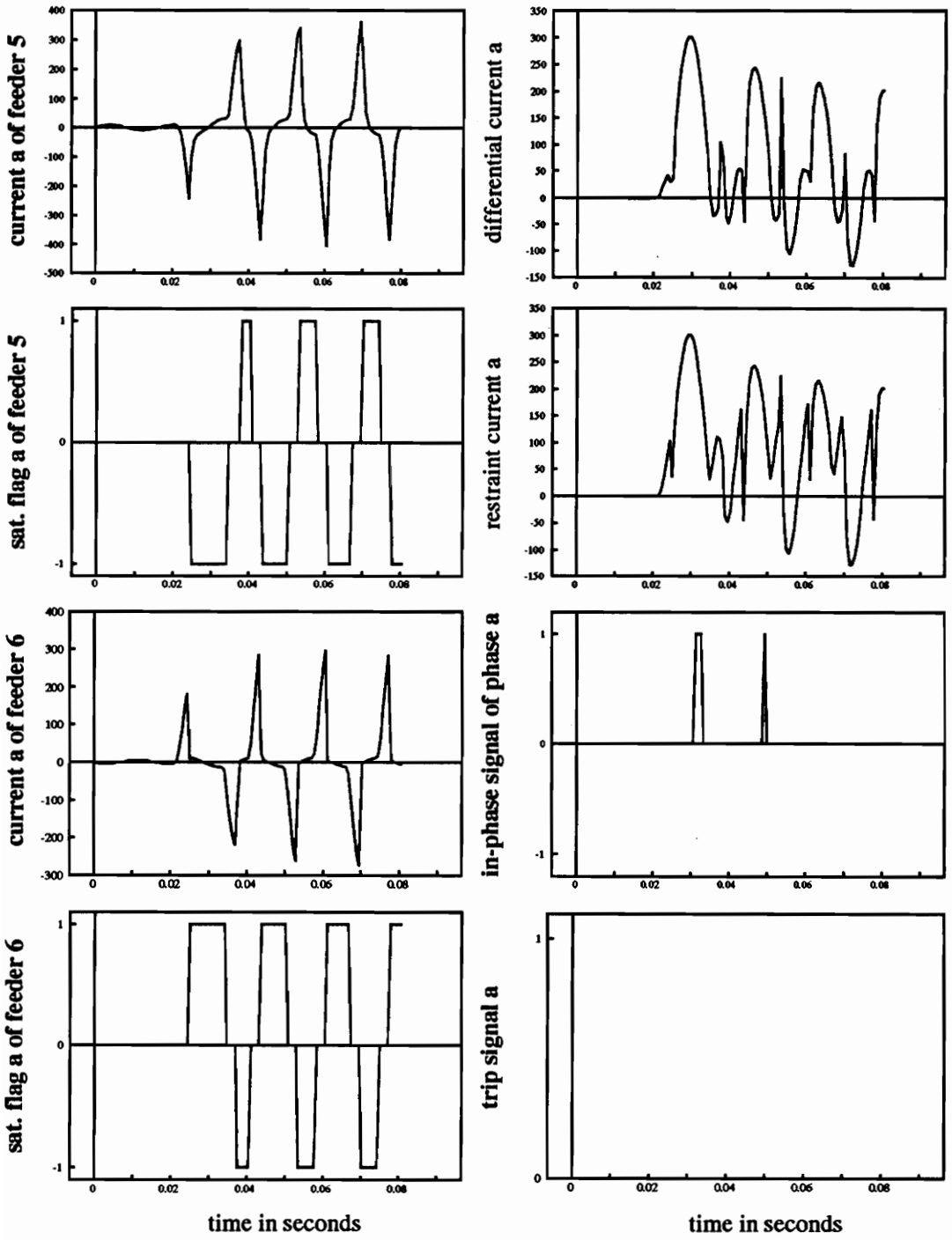

Fig. 14 An External Phase A to Ground Fault

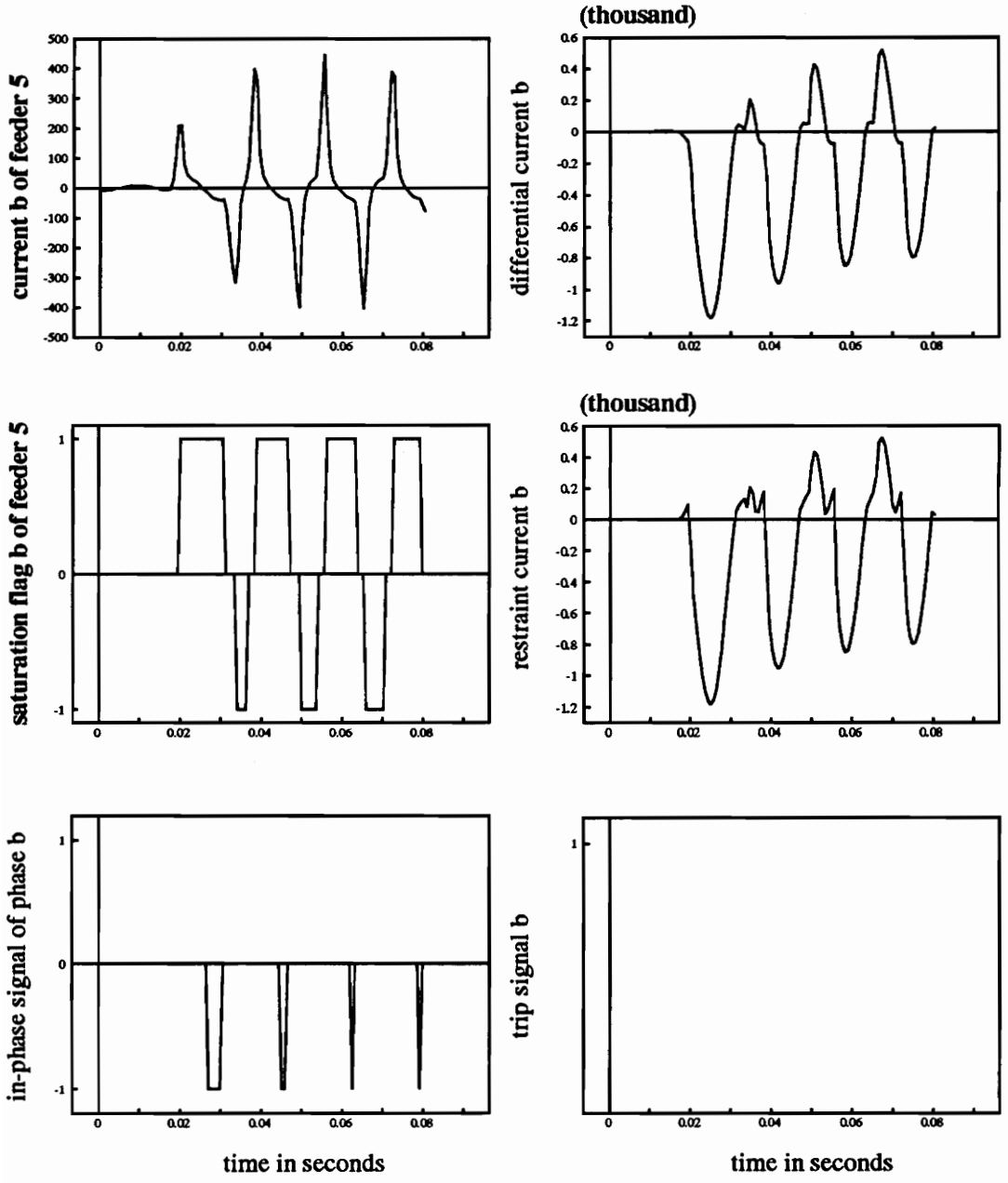

Fig. 15(a) Phase B of an External Phase B&C Short Circuit

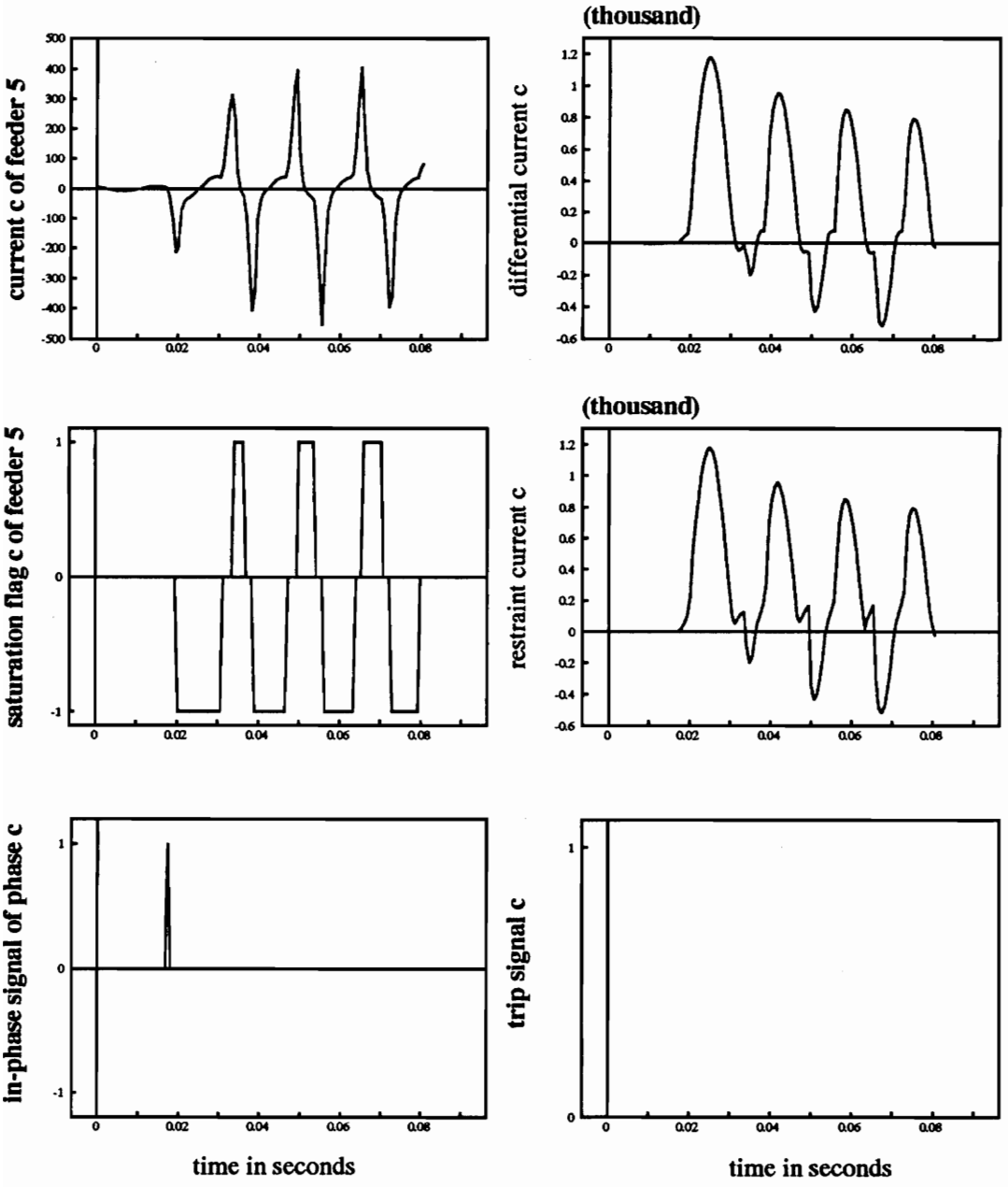

Fig. 15(b) Phase C of an External Phase B&C Short Circuit

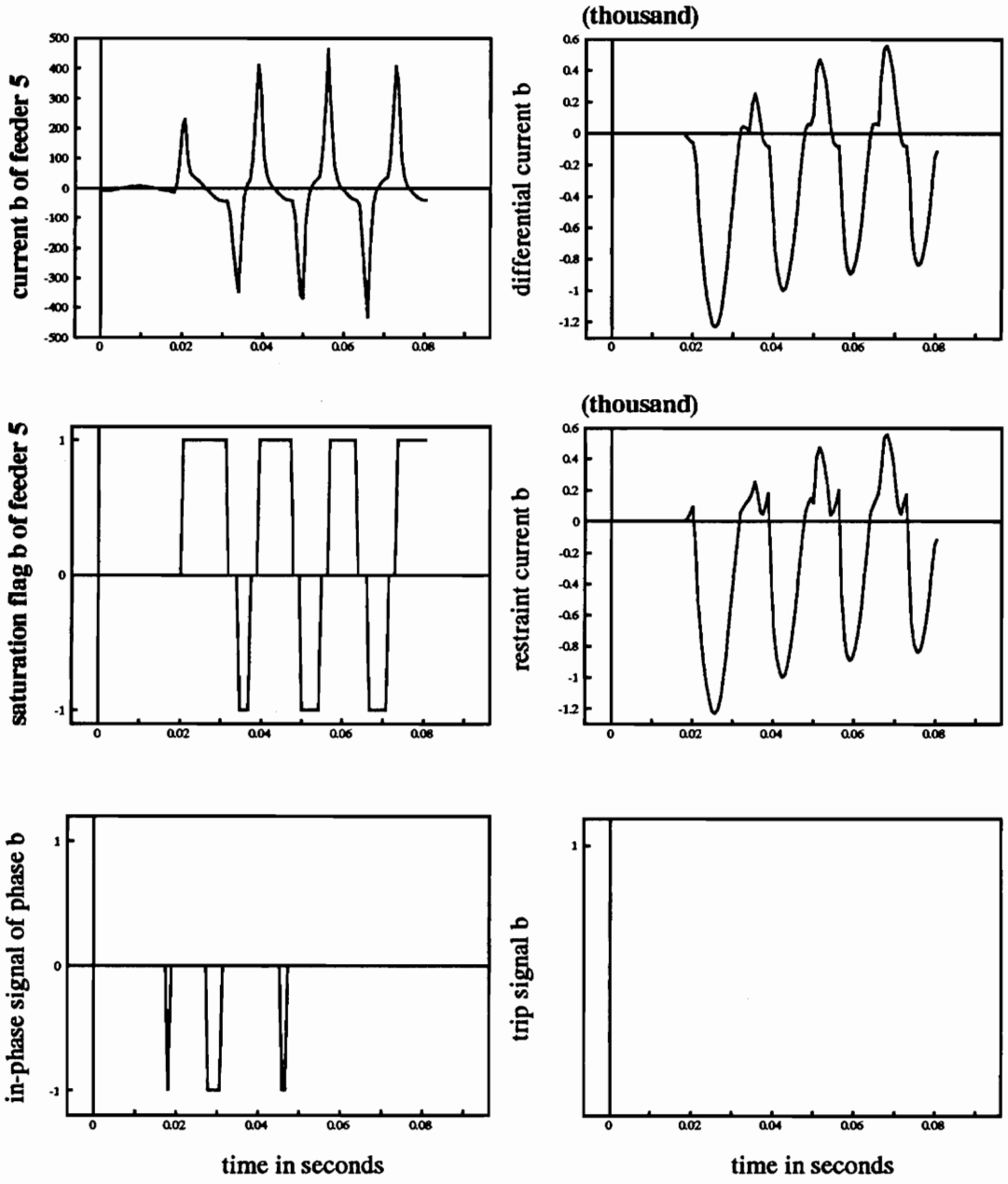

Fig. 16(a) Phase B of an External Phase B&C to Ground Fault

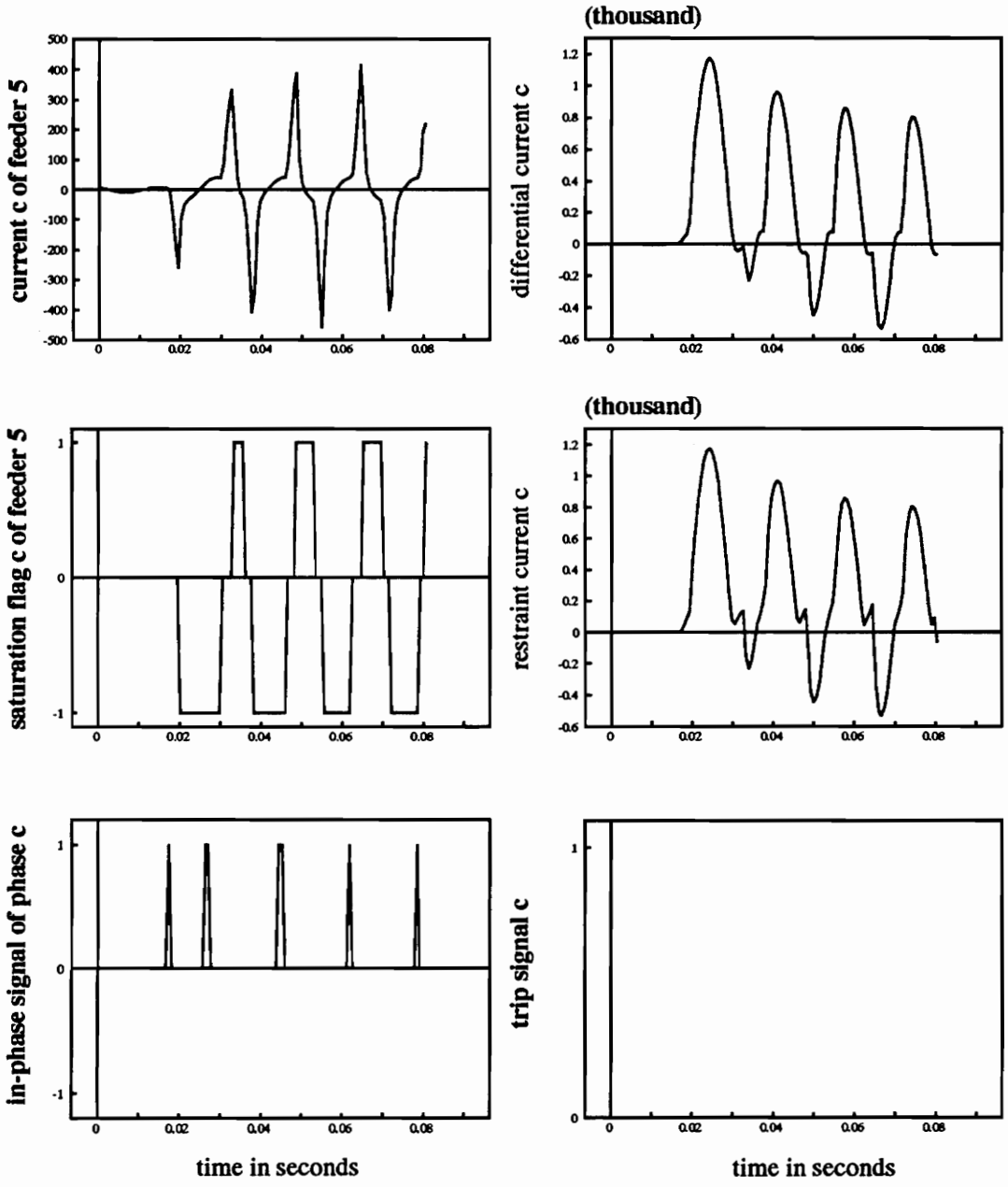

Fig. 16(b) Phase C of an External Phase B&C to Ground Fault

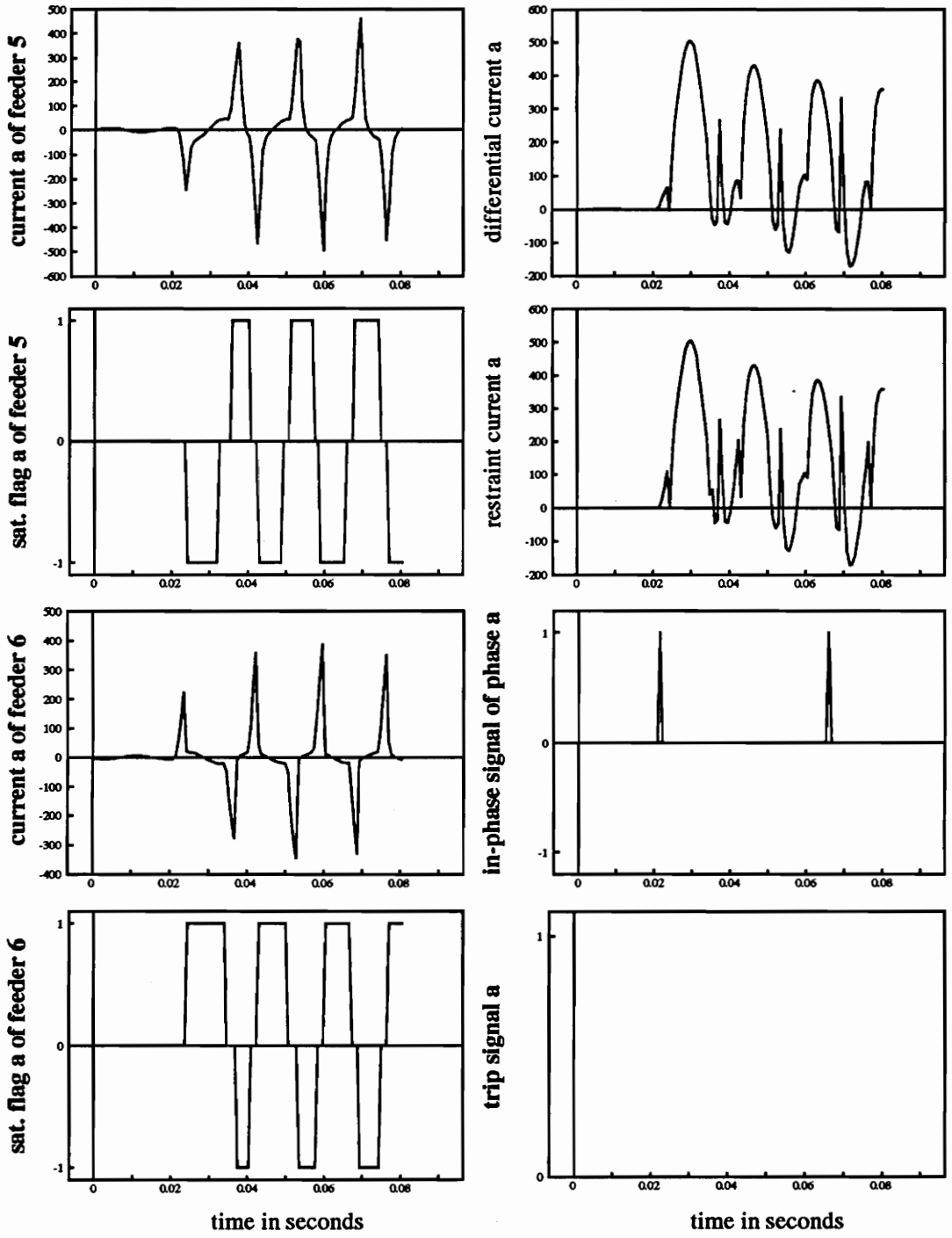

Fig. 17(a) Phase A of an External Three Phase Fault

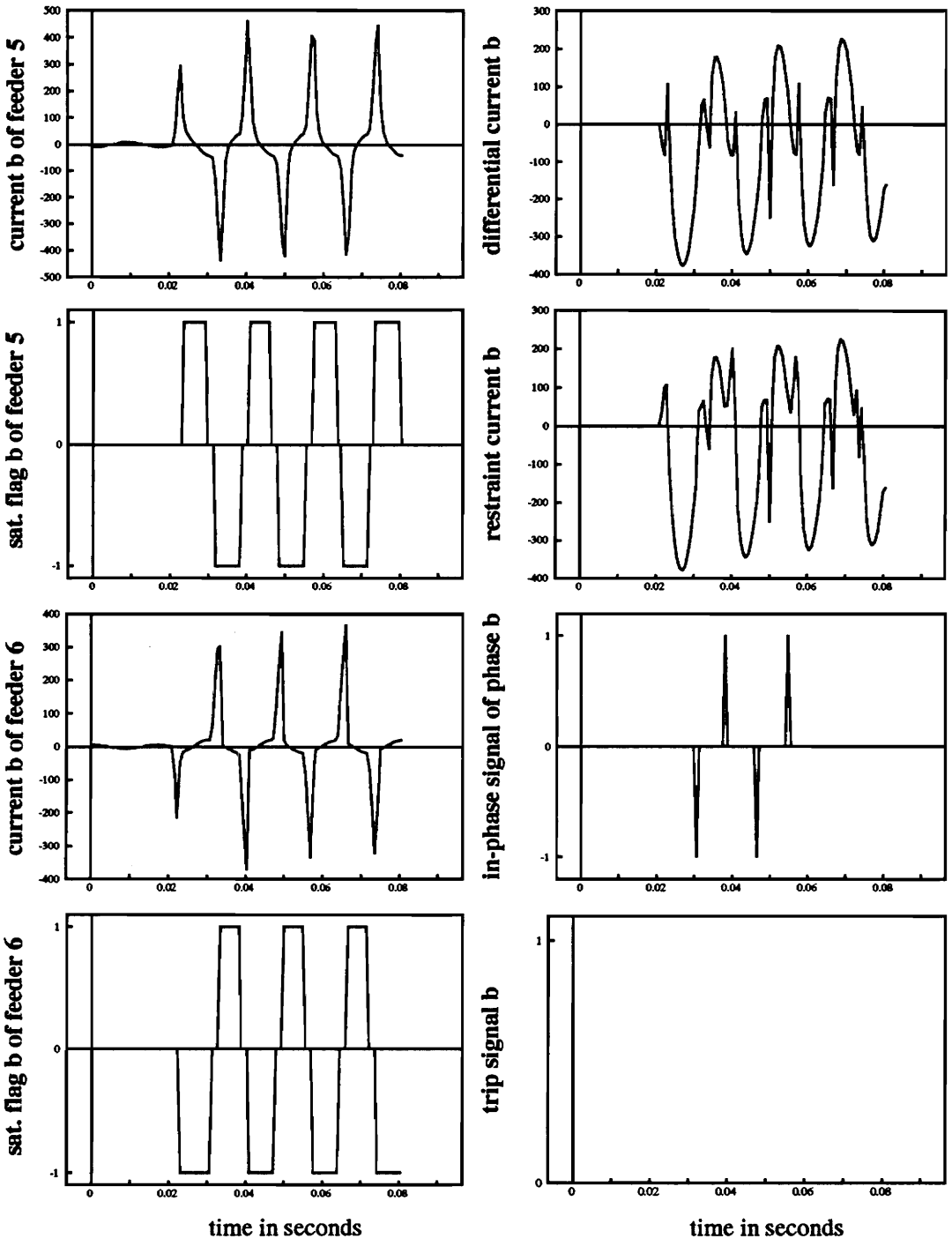

Fig. 17(b) Phase B of an External Three Phase Fault

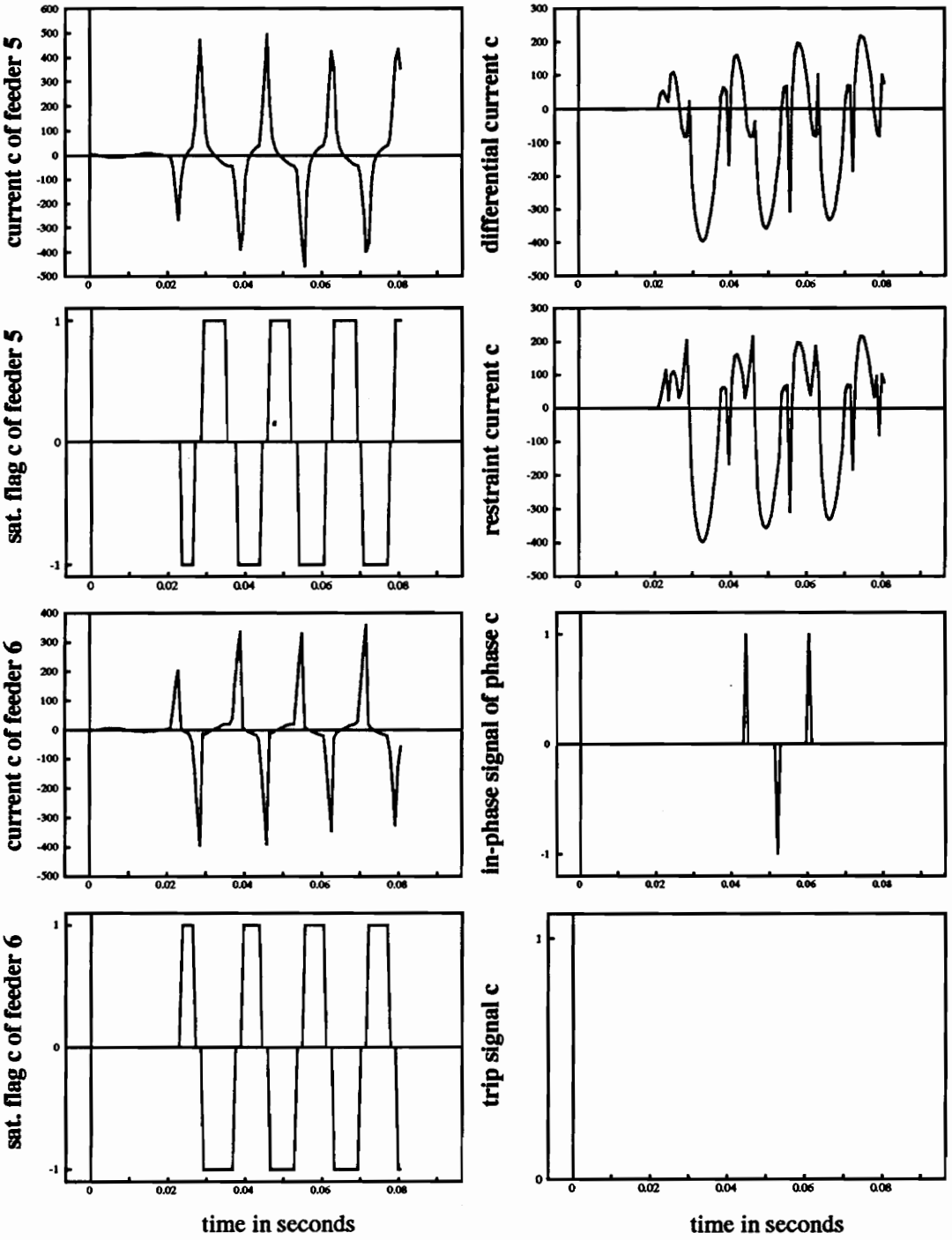

Fig. 17(c) Phase C of an External Three Phase Fault

CHAPTER EIGHT

Conclusions

The existing CT saturation detector methods have been reviewed and a new detecting method has been developed. The new saturation detector can reveal one–eighth cycle saturation. It is very simple and efficient and well suited for computer application. The new saturation detector has been incorporated into the percentage differential current scheme and the phase comparison scheme. Many simulations have shown the saturation detector and the proposed bus protection system (combination of the percentage differential scheme and the phase comparison scheme) work correctly even in case of severe saturation or multiple saturations. Because the computational burden is small for each technique involved, both the percentage differential and phase comparison schemes can be implemented in real time for bus relays dealing with multiple feeders.

With the modern high speed 32 bit microprocessor, a higher sampling frequency such as 1440 Hz can be used in the proposed bus protection system, so

that the relay can use more information from the fault condition in a short period. An early saturation can be detected and a fast trip decision can be made.

The reliability of the conventional percentage differential scheme can be greatly improved with the incorporation of the new saturation detector. The percentage restraint signal adapts to CT saturation such that the bus relay is more sensitive in normal internal fault and more reliable in external fault. The phase comparison method will also work correctly during the course of saturation with the help of this saturation detector. The polarity of the saturated currents can be determined once the saturated current transformers are identified.

From the results obtained from simulations, the new saturation detector indicates almost exactly when a saturation occurs. The bus protection system can give a correct decision in half a cycle, hence a cycle is long enough for the bus relay to open for faults. In order to enhance the reliability of the bus protection system, it is recommended that the whole bus protection system be blocked one cycle after fault inception, and that it be reactivated when the fault disappears. When an external fault transfers to an internal fault after about a cycle, the fault must be cleared by the back–up protection system.

This thesis deals only with the single bus system. However, techniques used in this study can be extended to the double bus system. For bus protection, a one and a half breaker system is similar to a single bus system, therefore, the proposed bus protection system can be directly applied in this case.

The techniques used in this study are not only suitable for bus protection, but could be also used where CT saturation affects the behavior of protection systems such as relays for short transmission lines, generators, transformers and motors. In these applications, the proposed relay system could be either a stand–alone relay unit, or a function within the integrated protection system when an appropriate microprocessor is available.

APPENDIX A

Test System Input Data File in EMTP

```
C ------------------------------------------------------------------------
C TVA SYSTEM MODEL, FILTERS ARE INCLUDED, SATURABLE CTS ARE USED IN TWO FEEDERS
C ------------------------------------------------------------------------
C
BEGIN NEW DATA CASE
C 345678901234567890123456789012345678901234567890123456789012345678901234567890
1.389e-4    0.08      60.
       5
C TACS HYBRID
C 91MBUS21          60.
C 98RKSPIG  =MBUS21/60*0.05
C 33RKSPIG
C BLANK ENDING TACS CARDS
C begin modeling the three-phase lines
$LISTOFF
C The lines in two sections
C Rock Springs
51RKSW11RKSPE1             7.8542      26.2320
52RKSW12RKSPE2             0.933       8.13947
53RKSW13RKSPE3
51RKSPF1RKSPE1                         12.6783
52RKSPF2RKSPE2                         13.5713
53RKSPF3RKSPE3
C Widow's Creek no. 3
51W3SW11WCBUS1             21.744      76.1293
52W3SW12WCBUS2             3.4736      22.6300
53W3SW13WCBUS3
51WCN3F1WCBUS1                         46.450
52WCN3F2WCBUS2                         4.8150
53WCN3F3WCBUS3
C Widow's Creek no. 2
51W2SW11WCBUS1             22.086      75.7674
52W2SW12WCBUS2             3.5755      22.81
53W2SW13WCBUS3
C East Cleveland
51ECSW11ECLVE1             4.3151      14.6377
52ECSW12ECLVE2             .9412       4.6625
53ECSW13ECLVE3
51ECLVF1ECLVE1                         91.1284
52ECLVF2ECLVE2                         35.2197
53ECLVF3ECLVE3
C Transformer Bank
51TRSW11TRNSE1             0.5443      15.3193
52TRSW12TRNSE2             0.5443      15.3193
53TRSW13TRNSE3
51TRNSF1TRNSE1                         84.4446
52TRNSF2TRNSE2                        221.5046
53TRNSF3TRNSE3
C Ridgledale
51RDSW11RGDLE1             6.0140      18.3517
52RDSW12RGDLE2             0.5705       5.5215
53RDSW13RGDLE3
51RGDLF1RGDLE1                         48.2127
52RGDLF2RGDLE2                        123.2766
53RGDLF3RGDLE3
C Concord
51CNSW11CNRDF1             4.7363      16.5130
52CNSW12CNRDF2             0.8798       5.2801
53CNSW13CNRDF3
51CNRDF1CNRDE1                         11.9246
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52CNRDF2CNRDE2                          7.4616
53CNRDF3CNRDE3
C Widow's Creek no. 1
51W1SW11WCN1E1          11.587          36.7301
52W1SW12WCN1E2          1.9700          11.7422
53W1SW13WCN1E3
51WCN1F1WCN1E1                          80.9220
52WCN1F2WCN1E2                          23.5040
53WCN1F3WCN1E3
C Nickajack
51NJSW11NKJKE1          21.826          69.3132
52NJSW12NKJKE2          3.8851          21.9547
53NJSW13NKJKE3
51NKJKF1NKJKE1                          35.7030
52NKJKF2NKJKE2                          14.7028
53NKJKF3NKJKE3
C CT MODELS
  TRANSFORMER                           CTRK11
        9999
01RKSWB1RKSW11          0.001 0.05      5.
02RKCTA1RKCTA2          0.060 3.00      300.
  TRANSFORMER CTRK11                    CTRK22
01RKSWB2RKSW12
02RKCTB1RKCTB2
  TRANSFORMER CTRK11                    CTRK33
01RKSWB3RKSW13
02RKCTC1RKCTC2
C CT BURDEN
  RKCTA1RKCTA3          0.5
  RKCTA3RKCTA2          0.05
  RKCTB1RKCTB3          0.5
  RKCTB3RKCTB2          0.05
  RKCTC1RKCTC3          0.5
  RKCTC3RKCTC2          0.05
  RKCTA2                0.1E-9
  RKCTB2                0.1E-9
  RKCTC2                0.1E-9
C FILTERING CIRCUIT
  RKCTA3FILTA1          0.01
  FILTA1FILTA2          1260.
  FILTA2FILTA3          2520.
  FILTA2                                0.1
  FILTA3                                0.1
C  FILTA1FILTA2          487.
C  FILTA2FILTA3          17400.
C  FILTA2                               1.0
C  FILTA3                               0.033
  FILTA3FILTVA          0.01
  FILTVA                1.0E+9                                          2
C
  RKCTB3FILTB1          0.01
  FILTB1FILTB2          1260.
  FILTB2FILTB3          2520.
  FILTB2                                0.1
  FILTB3                                0.1
  FILTB3FILTVB          0.01
  FILTVB                1.0E+9                                          2
C
  RKCTC3FILTC1          0.01
  FILTC1FILTC2          1260.
```

```
   FILTC2FILTC3              2520.
   FILTC2                                 0.1
   FILTC3                                 0.1
   FILTC3FILTVC              0.01
   FILTVC                    1.0E+9
 96RKCTA4RKCTA2              8888.   -.29
   -0.1512893E+02  -0.3846204E+00
   -0.1008595E+02  -0.3823034E+00
   -0.4538680E+01  -0.3741939E+00
   -0.2017191E+01  -0.3660845E+00
   -0.7564465E+00  -0.3591335E+00
    0.2521488E+00  -0.3452315E+00
    0.8825210E+00  -0.3290126E+00
    0.1462463E+01  -0.3012087E+00
    0.1765042E+01  -0.2548689E+00
    0.2017191E+01  -0.1853592E+00
    0.2521489E+01   0.1239590E+00
    0.2773637E+01   0.1714573E+00
    0.3530084E+01   0.2316990E+00
    0.4538680E+01   0.2780388E+00
    0.5496845E+01   0.3012087E+00
    0.7186242E+01   0.3243786E+00
    0.9833805E+01   0.3452315E+00
    0.1348996E+02   0.3614505E+00
    0.1765042E+02   0.3730355E+00
    0.2521489E+02   0.3846204E+00
    0.4034382E+02   0.3938884E+00
    0.5547275E+02   0.3962054E+00
            9999
96RKCTB4RKCTB2RKCTA4RKCTA28888.
96RKCTC4RKCTC2RKCTA4RKCTA28888.
C
  TRANSFORMER CTRK11                    CTW311
01W3SWB1W3SW11
02W3CTA1W3CTA2
  TRANSFORMER CTRK11                    CTW322
01W3SWB2W3SW12
02W3CTB1W3CTB2
  TRANSFORMER CTRK11                    CTW333
01W3SWB3W3SW13
02W3CTC1W3CTC2
C CT BURDEN
  W3CTA1W3CTA3              1.
  W3CTA3W3CTA2              0.05
  W3CTB1W3CTB3              1.
  W3CTB3W3CTB2              0.05
  W3CTC1W3CTC3              1.
  W3CTC3W3CTC2              0.05
  W3CTA2                    0.1E-9
  W3CTB2                    0.1E-9
  W3CTC2                    0.1E-9
  W3CTA3FIW3A1              0.01
  FIW3A1FIW3A2              1260.
  FIW3A2FIW3A3              2520.
  FIW3A2                                 0.1
  FIW3A3                                 0.1
  FIW3A3FIW3VA              0.01
  FIW3VA                    1.0E+9
C
  W3CTB3FIW3B1              0.01
```

```
  FIW3B1FIW3B2          1260.
  FIW3B2FIW3B3          2520.
  FIW3B2                            0.1
  FIW3B3                            0.1
  FIW3B3FIW3VB          0.01
  FIW3VB                1.0E+9                                          2
C
  W3CTC3FIW3C1          0.01
  FIW3C1FIW3C2          1260.
  FIW3C2FIW3C3          2520.
  FIW3C2                            0.1
  FIW3C3                            0.1
  FIW3C3FIW3VC          0.01
  FIW3VC                1.0E+9                                          2
C
  TRANSFORMER CTRK11                CTW211
01W2SWB1W2SW11
02W2CTA1W2CTA2
  TRANSFORMER CTRK11                CTW222
01W2SWB2W2SW12
02W2CTB1W2CTB2
  TRANSFORMER CTRK11                CTW233
01W2SWB3W2SW13
02W2CTC1W2CTC2
C CT BURDEN
  W2CTA1W2CTA3          1.
  W2CTA3W2CTA2          0.05
  W2CTB1W2CTB3          1.
  W2CTB3W2CTB2          0.05
  W2CTC1W2CTC3          1.
  W2CTC3W2CTC2          0.05
  W2CTA2                0.1E-9
  W2CTB2                0.1E-9
  W2CTC2                0.1E-9
  W2CTA3FIW2A1          0.01
  FIW2A1FIW2A2          1260.
  FIW2A2FIW2A3          2520.
  FIW2A2                            0.1
  FIW2A3                            0.1
  FIW2A3FIW2VA          0.01
  FIW2VA                1.0E+9                                          2
C
  W2CTB3FIW2B1          0.01
  FIW2B1FIW2B2          1260.
  FIW2B2FIW2B3          2520.
  FIW2B2                            0.1
  FIW2B3                            0.1
  FIW2B3FIW2VB          0.01
  FIW2VB                1.0E+9                                          2
C
  W2CTC3FIW2C1          0.01
  FIW2C1FIW2C2          1260.
  FIW2C2FIW2C3          2520.
  FIW2C2                            0.1
  FIW2C3                            0.1
  FIW2C3FIW2VC          0.01
  FIW2VC                1.0E+9                                          2
C
  TRANSFORMER CTRK11                CTEC11
01ECSWB1ECSW11
```

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02ECCTA1ECCTA2
  TRANSFORMER CTRK11                    CTEC22
01ECSWB2ECSW12
02ECCTB1ECCTB2
  TRANSFORMER CTRK11                    CTEC33
01ECSWB3ECSW13
02ECCTC1ECCTC2
C CT BURDEN
  ECCTA1ECCTA3          1.
  ECCTA3ECCTA2          0.05
  ECCTB1ECCTB3          1.
  ECCTB3ECCTB2          0.05
  ECCTC1ECCTC3          1.
  ECCTC3ECCTC2          0.05
  ECCTA2                0.1E-9
  ECCTB2                0.1E-9
  ECCTC2                0.1E-9
  ECCTA3FIECA1          0.01
  FIECA1FIECA2          1260.
  FIECA2FIECA3          2520.
  FIECA2                              0.1
  FIECA3                              0.1
  FIECA3FIECVA          0.01
  FIECVA                1.0E+9                                        2
C
  ECCTB3FIECB1          0.01
  FIECB1FIECB2          1260.
  FIECB2FIECB3          2520.
  FIECB2                              0.1
  FIECB3                              0.1
  FIECB3FIECVB          0.01
  FIECVB                1.0E+9                                        2
C
  ECCTC3FIECC1          0.01
  FIECC1FIECC2          1260.
  FIECC2FIECC3          2520.
  FIECC2                              0.1
  FIECC3                              0.1
  FIECC3FIECVC          0.01
  FIECVC                1.0E+9                                        2
C
  TRANSFORMER CTRK11                    CTTR11
01TRSWB1TRSW11
02TRCTA1TRCTA2
  TRANSFORMER CTRK11                    CTTR22
01TRSWB2TRSW12
02TRCTB1TRCTB2
  TRANSFORMER CTRK11                    CTTR33
01TRSWB3TRSW13
02TRCTC1TRCTC2
C CT BURDEN
  TRCTA1TRCTA3          1.
  TRCTA3TRCTA2          0.05
  TRCTB1TRCTB3          1.
  TRCTB3TRCTB2          0.05
  TRCTC1TRCTC3          1.
  TRCTC3TRCTC2          0.05
  TRCTA2                0.1E-9
  TRCTB2                0.1E-9
  TRCTC2                0.1E-9
```

```
C
  TRCTA3FITRA1              0.01
  FITRA1FITRA2              1260.
  FITRA2FITRA3              2520.
  FITRA2                                0.1
  FITRA3                                0.1
  FITRA3FITRVA              0.01
  FITRVA                    1.0E+9                                        2
C
  TRCTB3FITRB1              0.01
  FITRB1FITRB2              1260.
  FITRB2FITRB3              2520.
  FITRB2                                0.1
  FITRB3                                0.1
  FITRB3FITRVB              0.01
  FITRVB                    1.0E+9                                        2
C
  TRCTC3FITRC1              0.01
  FITRC1FITRC2              1260.
  FITRC2FITRC3              2520.
  FITRC2                                0.1
  FITRC3                                0.1
  FITRC3FITRVC              0.01
  FITRVC                    1.0E+9                                        2
C
  TRANSFORMER CTRK11                    CTTI11
01MBUS21MBUS11
02TICTA1TICTA2
  TRANSFORMER CTRK11                    CTTI22
01MBUS22MBUS12
02TICTB1TICTB2
  TRANSFORMER CTRK11                    CTTI33
01MBUS23MBUS13
02TICTC1TICTC2
96TICTA4TICTA2RKCTA4RKCTA28888.
96TICTB4TICTB2RKCTA4RKCTA28888.
96TICTC4TICTC2RKCTA4RKCTA28888.
C CT BURDEN
  TICTA1TICTA3              1.75
  TICTA3TICTA2              0.05
  TICTB1TICTB3              1.75
  TICTB3TICTB2              0.05
  TICTC1TICTC3              1.75
  TICTC3TICTC2              0.05
  TICTA2                    0.1E-9
  TICTB2                    0.1E-9
  TICTC2                    0.1E-9
  TICTA3AFILT1              0.01
  AFILT1AFILT2              1260.
  AFILT2AFILT3              2520.
  AFILT2                                0.1
  AFILT3                                0.1                           2
  AFILT3                    1.0E+9
C PHASE B
  TICTB3BFILT1              0.01
  BFILT1BFILT2              1260.
  BFILT2BFILT3              2520.
  BFILT2                                0.1
  BFILT3                                0.1                           2
  BFILT3                    1.0E+9
```

```
C PHASE C
  TICTC3CFILT1            0.01
  CFILT1CFILT2            1260.
  CFILT2CFILT3            2520.
  CFILT2                          0.1
  CFILT3                          0.1                                    2
  CFILT3                  1.0E+9
C
  TRANSFORMER CTRK11              CTRD11
01RDSWB1RDSW11
02RDCTA1RDCTA2
  TRANSFORMER CTRK11              CTRD22
01RDSWB2RDSW12
02RDCTB1RDCTB2
  TRANSFORMER CTRK11              CTRD33
01RDSWB3RDSW13
02RDCTC1RDCTC2
C CT BURDEN
  RDCTA1RDCTA3            0.05
  RDCTA3RDCTA2            1.
  RDCTB1RDCTB3            0.05
  RDCTB3RDCTB2            1.
  RDCTC1RDCTC3            0.05
  RDCTC3RDCTC2            1.
  RDCTA2                  0.1E-9
  RDCTB2                  0.1E-9
  RDCTC2                  0.1E-9
C
  TRANSFORMER CTRK11              CTCN11
01CNSWB1CNSW11
02CNCTA1CNCTA2
  TRANSFORMER CTRK11              CTCN22
01CNSWB2CNSW12
02CNCTB1CNCTB2
  TRANSFORMER CTRK11              CTCN33
01CNSWB3CNSW13
02CNCTC1CNCTC2
C CT BURDEN
  CNCTA1CNCTA3            0.05
  CNCTA3CNCTA2            1.
  CNCTB1CNCTB3            0.05
  CNCTB3CNCTB2            1.
  CNCTC1CNCTC3            0.05
  CNCTC3CNCTC2            1.
  CNCTA2                  0.1E-9
  CNCTB2                  0.1E-9
  CNCTC2                  0.1E-9
C
  TRANSFORMER CTRK11              CTW111
01W1SWB1W1SW11
02W1CTA1W1CTA2
  TRANSFORMER CTRK11              CTW122
01W1SWB2W1SW12
02W1CTB1W1CTB2
  TRANSFORMER CTRK11              CTW133
01W1SWB3W1SW13
02W1CTC1W1CTC2
C CT BURDEN
  W1CTA1W1CTA3            0.05
  W1CTA3W1CTA2            1.
```

```
   W1CTB1W1CTB3              0.05
   W1CTB3W1CTB2              1.
   W1CTC1W1CTC3              0.05
   W1CTC3W1CTC2              1.
   W1CTA2                    0.1E-9
   W1CTB2                    0.1E-9
   W1CTC2                    0.1E-9
C
   TRANSFORMER CTRK11                    CTNJ11
01NJSWB1NJSW11
02NJCTA1NJCTA2
   TRANSFORMER CTRK11                    CTNJ22
01NJSWB2NJSW12
02NJCTB1NJCTB2
   TRANSFORMER CTRK11                    CTNJ33
01NJSWB3NJSW13
02NJCTC1NJCTC2
C CT BURDEN
   NJCTA1NJCTA3              0.05
   NJCTA3NJCTA2              1.
   NJCTB1NJCTB3              0.05
   NJCTB3NJCTB2              1.
   NJCTC1NJCTC3              0.05
   NJCTC3NJCTC2              1.
   NJCTA2                    0.1E-9
   NJCTB2                    0.1E-9
   NJCTC2                    0.1E-9
C
   RKSPF1                     1.
   RKSPF2                     1.
   RKSPF3                     1.
C
   WCN3F1                     1.
   WCN3F2                     1.
   WCN3F3                     1.
C
   ECLVF1                     1.
   ECLVF2                     1.
   ECLVF3                     1.
C
   TRNSF1                     1.
   TRNSF2                     1.
   TRNSF3                     1.
C
   RGDLF1                     1.
   RGDLF2                     1.
   RGDLF3                     1.
C
   CNRDF1                     1.
   CNRDF2                     1.
   CNRDF3                     1.
C
   WCN1F1                     1.
   WCN1F2                     1.
   WCN1F3                     1.
C
   NKJKF1                     1.
   NKJKF2                     1.
   NKJKF3                     1.
C Bus tie impedances
```

```
BLANK CARD ENDING BRANCH CARDS
C measuring switches for the line currents at the bus
C Rocksprings switch
  MBUS21RKSWB1                                                  MEASURING
  MBUS22RKSWB2                                                  MEASURING
  MBUS23RKSWB3                                                  MEASURING
C Widow's Creek no. 3
  MBUS21W3SWB1                                                  MEASURING
  MBUS22W3SWB2                                                  MEASURING
  MBUS23W3SWB3                                                  MEASURING
C Widow's Creek no. 2
  MBUS21W2SWB1                                                  MEASURING
  MBUS22W2SWB2                                                  MEASURING
  MBUS23W2SWB3                                                  MEASURING
C East Cleveland
  MBUS21ECSWB1                                                  MEASURING
  MBUS22ECSWB2                                                  MEASURING
  MBUS23ECSWB3                                                  MEASURING
C Transformer Bank
  MBUS21TRSWB1                                                  MEASURING
  MBUS22TRSWB2                                                  MEASURING
  MBUS23TRSWB3                                                  MEASURING
C Ridgedale
  MBUS11RDSWB1                                                  MEASURING
  MBUS12RDSWB2                                                  MEASURING
  MBUS13RDSWB3                                                  MEASURING
C Concord
  MBUS11CNSWB1                                                  MEASURING
  MBUS12CNSWB2                                                  MEASURING
  MBUS13CNSWB3                                                  MEASURING
C Widow's Creek no. 1
  MBUS11W1SWB1                                                  MEASURING
  MBUS12W1SWB2                                                  MEASURING
  MBUS13W1SWB3                                                  MEASURING
C Nickajack
  MBUS11NJSWB1                                                  MEASURING
  MBUS12NJSWB2                                                  MEASURING
  MBUS13NJSWB3                                                  MEASURING
C The Bus Tie
C  BUSM11BUSM21                                                  MEASURING
C  BUSM12BUSM22                                                  MEASURING
C  BUSM13BUSM23                                                  MEASURING
C switches for the line to ground faults
C Rocksprings switch
C  RKSPF1          0.003      0.005      1.E10
C  RKSPF2          0.003      0.005      1.E10
C  RKSPF3          0.003      0.005      1.E10
C  RKSW11       +0.02083        2.0
C  RKSW12       +0.01667        2.0
C  RKSW13       +0.01667        2.0
C Widow's Creek no. 3
C  WCN3F1
C  WCN3F2
C  WCN3F3
C Widow's Creek no. 2
C  WCN2F1
C  WCN2F2
C  WCN2F3
C East Cleveland
C  ECLVF1
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C  ECLVF2
C  ECLVF3
C TRANSFORMERS
C  TRSW11       +0.01667          2.0
C  TRSW12       +0.01667          2.0
C  TRSW13       +0.01667          2.0
C Ridgedale
C  RGDLF1
C  RGDLF2
C  RGDLF3
C Concord
C  CNRDF1
C  CNRDF2
C  CNRDF3
C Widow's Creek no. 1
C  WCN1F1
C  WCN1F2
C  WCN1F3
C Nickajack
C  NKJKF1
C  NKJKF2
C  NKJKF3
C switches for the bus faults
C Bus number 1
C  MBUS11       20.8333E-3        2.0
C  MBUS12       16.6667E-3        2.0
C  MBUS13       16.6667E-3        2.0
C Bus number 2
C  MBUS21       16.6667e-3        2.0
   MBUS22       16.6667e-3        2.0
   MBUS23       16.6667e-3        2.0
C SATURABLE CT NONLINEAR ELEMENTS SWITCHES
C  RKCTA1RKCTA4+0.02083           2.0
C  RKCTB1RKCTB4+0.02083           2.0
C  RKCTC1RKCTC4+0.02083           2.0
C  TICTA1TICTA4+0.02083           2.0
C  TICTB1TICTB4+0.02083           2.0
C  TICTC1TICTC4+0.02083           2.0
   RKCTA1RKCTA4+5.016667          2.0
   RKCTB1RKCTB4+5.016667          2.0
   RKCTC1RKCTC4+5.016667          2.0
   TICTA1TICTA4+5.016667          2.0
   TICTB1TICTB4+5.016667          2.0
   TICTC1TICTC4+5.016667          2.0
BLANK CARD ENDING SWITCH CARDS
C Rock Springs
14RKSPF1  131455.950      60.0    000.000                    -1.0        2.0
14RKSPF2  131455.950      60.0    -120.00                    -1.0        2.0
14RKSPF3  131455.950      60.0    120.000                    -1.0        2.0
C Widow 2, 3's Creek
14WCN3F1  131455.950      60.0    000.000                    -1.0        2.0
14WCN3F2  131455.950      60.0    -120.00                    -1.0        2.0
14WCN3F3  131455.950      60.0    120.000                    -1.0        2.0
C East Cleveland
14ECLVF1  131455.950      60.0    000.000                    -1.0        2.0
14ECLVF2  131455.950      60.0    -120.00                    -1.0        2.0
14ECLVF3  131455.950      60.0    120.000                    -1.0        2.0
C Transformer Bank
14TRNSF1  131455.950      60.0    000.000                    -1.0        2.0
14TRNSF2  131455.950      60.0    -120.00                    -1.0        2.0
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14TRNSF3  131455.950       60.0   120.000                          -1.0        2.0
C Ridgedale
14RGDLF1  131455.950       60.0   000.000                          -1.0        2.0
14RGDLF2  131455.950       60.0   -120.00                          -1.0        2.0
14RGDLF3  131455.950       60.0   120.000                          -1.0        2.0
C Widow 1's Creek
14WCN1F1  131455.950       60.0   000.000                          -1.0        2.0
14WCN1F2  131455.950       60.0   -120.00                          -1.0        2.0
14WCN1F3  131455.950       60.0   120.000                          -1.0        2.0
C Concord
14CNRDF1  131455.950       60.0   000.000                          -1.0        2.0
14CNRDF2  131455.950       60.0   -120.00                          -1.0        2.0
14CNRDF3  131455.950       60.0   120.000                          -1.0        2.0
C Nickajack
14NKJKF1  131455.950       60.0   000.000                          -1.0        2.0
14NKJKF2  131455.950       60.0   -120.00                          -1.0        2.0
14NKJKF3  131455.950       60.0   120.000                          -1.0        2.0
BLANK CARD ENDING SOURCE CARDS
$LISTON
BLANK CARD ENDING SELECTIVE NODE VOLTAGE OUTPUT REQUESTS
BLANK CARD ENDING PLOT CARDS
BEGIN NEW DATA CASE
BLANK CARD
  TRANSFORMER                              UNIIDN
          9999
01CTPRI1CTPRI2              .0015015.00 5.00
02UNILED                    1.00  3.200   50.0
  -0.9975000E+00  -0.3271176E+01
  -0.6650000E+00  -0.3251471E+01
  -0.2992500E+00  -0.3182500E+01
  -0.1330000E+00  -0.3113529E+01
  -0.4987500E-01  -0.3054412E+01
   0.1662500E-01  -0.2936176E+01
   0.5818750E-01  -0.2798253E+01
   0.9642500E-01  -0.2561765E+01
   0.1163750E+00  -0.2167647E+01
   0.1330000E+00  -0.1576471E+01
   0.1662500E+00   0.1054265E+01
   0.1828750E+00   0.1458235E+01
   0.2327500E+00   0.1970588E+01
   0.2992500E+00   0.2364706E+01
   0.3624250E+00   0.2561765E+01
   0.4738125E+00   0.2758824E+01
   0.6438750E+00   0.2936176E+01
   0.8894375E+00   0.3074118E+01
   0.1163750E+01   0.3172647E+01
   0.1662500E+01   0.3271176E+01
   0.2660000E+01   0.3350000E+01
   0.7000000E+02   0.3369706E+01
          9999
```

APPENDIX B

Program for the Bus Protection System in Fortran

```
C
C      PROGRAM FOR DIGITAL BUS RELAY (no least squared saturation detector)
C      percentage differential and positive & negative half phase comparision
c      schemes are implemented.
C
       DIMENSION BA(20,48),SCMA(18),LA(3,2),MMD1(3,2),MME1(3,2),AM(6),
      $Z2(6,1),X2(6,1),AMP1(18),AN1(18),CB(18),MMC1(3,2),H1(20,20)
      $,B(20,48),AMPA(18),LCONTA(18),LDSAT(18)
       CHARACTER AAA*10
C
C      NUMBER OF FEEDERS M, SAMPLING RATE N, POWER SYSTEM FREQUENCY M1----------
C
       M=6
       N=24
       M1=60
       T=2.0*3.1416/(FLOAT(N))
       T3=1./(FLOAT(M1*N))
C
C      READ MAXIMUM LOAD CURRENTS AND MAXIMUM FAULT CURRENT
C
       OPEN (UNIT=2, FILE='LOAD.DAT',STATUS='OLD')
       READ(2,*)(AM(I),I=1,6)
       READ(2,*)CM1
       CLOSE (2)
1000   CONTINUE
C
C      CIRCUIT BREAK STATUS FROM I/O BOARD
C
       DO 1010 I=1,18
          AMPA(I)=CM1
1010   CB(I)=1.
C
C      CLEAR FAULT AND TRIPPING COUNTERS
C
       KA=0
       JA=0
       MDA=0
       MDB=0
       MDC=0
       MCA=0
       MCB=0
       MCC=0
C
C      SET RESTRAINT CURRENT FOR EACH PHASE TO ZERO
C
       EXA=0.0
       EXB=0.0
       EXC=0.0

       PRINT *, 'INPUT FILENAME.EXTENSION='
       READ (*,12)AAA
12     FORMAT(A10)
C
C      OPEN FILES FOR INPUT AND OUTPUTS
C
       OPEN(UNIT=8,FILE='bus2.out',STATUS='new')
       OPEN(UNIT=7,FILE='bus1.out',STATUS='new')
       OPEN(UNIT=6,FILE='bus.out',STATUS='new')
       OPEN(UNIT=5,FILE=AAA,STATUS='OLD')
C
```

```
C      THE PROGRAM STARTS RUN
C
       K=0

50     K=K+1
       PRINT *,'            ##################################################
      $###########'
       PRINT *,'         #
      $          #'
       PRINT *,'            #                    K=',K,'
      $  #'
       PRINT *,'         #
      $          #'
       PRINT *,'            ##################################################
      $###########'
       READ(5,60,END=310)(B(I,48),I=1,M*3)
60     FORMAT(15X,9E13.6/15X,9E13.6)

       DO IX=1,18
         B(IX,48)=B(IX,48)/0.05
       END DO

C      PHASE A
       PRINT *,'       ----PHASE  A -----       ----PHASE  B -----       ---
      $-PHASE  C -----'
       J3=1
       CALL DIFF(K,B,N,J3,M,M1,AM,CM1,LA,JA,KA,EXA,JJA,CB,MCA,MMC1,FLAGA,
      $SCMA,SUMA,MDA,MMD1,MME1,AMPA,K31,LCONTA,LDSAT)
C      PHASE B
       J3=2
       CALL DIFF(K,B,N,J3,M,M1,AM,CM1,LA,JB,KB,EXB,JJB,CB,MCB,MMC1,FLAGB,
      $SCMA,SUMB,MDB,MMD1,MME1,AMPA,K32,LCONTA,LDSAT)
       J3=3
       CALL DIFF(K,B,N,J3,M,M1,AM,CM1,LA,JC,KC,EXC,JJC,CB,MCC,MMC1,FLAGC,
      $SCMA,SUMC,MDC,MMD1,MME1,AMPA,K33,LCONTA,LDSAT)
C
       PRINT *,'        JJ=',JA,'          JJ=',JB,'          JJ=',JC
       PRINT *,'        KK=',KA,'          KK=',KB,'          KK=',KC
       PRINT *,'        PH=',MDA,'          PH=',MDB,'           PH=',MDC
       PRINT *,'        CH=',MCA,'          CH=',MCB,'           CH=',MCC

C    ********************  PHASE A **********************

C PERCENTAGE DIFFERENTIAL PRINCIPLE
       IF (JA.GE.6.AND.KA.GE.6)GO TO 230

C PHASE COMPARISION

C CHECK POSITIVE HALF WAVE
        IF (MDA.GE.8.AND.MMD1(1,2)-MMD1(1,1).EQ.MDA-1)GO TO 230
C CHECK NEGATIVE HALF WAVE
        IF (MCA.GE.8.AND.MMC1(1,2)-MMC1(1,1).EQ.MCA-1)GO TO 230
       GO TO 410
230    PRINT *,'       **TRIPPING PHASE A**'
       PRINT *,'            * !!!!!! *'
       PRINT *
C       JA=0
C       JJA=0
       flaga=1.
       KA=0
```

```
       MDA=0
       MCA=0
       DO 297 I=1,2
       IF (MMC1(1,1)-MMD1(1,2).GT.0)GO TO 232
       MMC1(1,I)=0
232    IF (MMD1(1,1)-MMC1(1,2).GT.0)GO TO 297
       MMD1(1,I)=0
297    MME1(1,I)=0

C   ***************************  PHASE B ***********************

C   PERCENTAGE DIFFERENTIAL PRINCIPLE

410    IF (JB.GE.6.AND.KB.GE.6)GO TO 430

C   PHASE COMPARISION

C CHECK POSITIVE HALF WAVE

       IF (MDB.GE.8.AND.(MMD1(2,2)-MMD1(2,1)).EQ.MDB-1)GO TO 430

C CHECK NEGATIVE HALF WAVE

       IF (MCB.GE.8.AND.(MMC1(2,2)-MMC1(2,1)).EQ.MCB-1)GO TO 430

      GO TO 610
430   PRINT *,'                                    **TRIPPING PHASE B**'
      PRINT *,'                                        * !!!!!! *'
      PRINT *
C      JB=0
C      JJB=0
      flagb=1.
      KB=0
      DO 298 I=1,2
      IF (MMC1(2,1)-MMD1(2,2).GT.0)GO TO 432
      MCB=0
      MMC1(2,I)=0
432   IF (MMD1(2,1)-MMC1(2,2).GT.0)GO TO 298
      MDB=0
      MMD1(2,I)=0
298   MME1(2,I)=0

C  *************************   PHASE C  ***********************

C   PERCENTAGE DIFFERENTIAL PRINCIPLE

610    IF (JC.GE.6.AND.KC.GE.6)GO TO 630

C  PHASE COMPARISION

C CHECK POSITIVE HALF WAVE
       IF (MDC.GE.8.AND.MMD1(3,2)-MMD1(3,1).EQ.MDC-1)GO TO 630
C CHECK NEGATIVE HALF WAVE
       IF (MCC.GE.8.AND.MMC1(3,2)-MMC1(3,1).EQ.MCC-1)GO TO 630
      GO TO 280
630    PRINT *,'
     $**TRIPPING PHASE C**'
      PRINT *,'
     $ * !!!!!! *'
      PRINT *
```

```
C       JC=0
C       JJC=0
        flagc=1.
        KC=0
        MDC=0
        MCC=0
        DO 299 I=1,2
        IF (MMC1(3,1)-MMD1(3,2).GT.0)GO TO 632
        MMC1(3,I)=0
632     IF (MMD1(3,1)-MMC1(3,2).GT.0)GO TO 299
        MMD1(3,I)=0
299     MME1(3,I)=0
C
C       UPDATE INPUT DATA
C
280     DO 290 I=1,M*3
        DO 291 J=1,47
        BA(I,J)=BA(I,J+1)
291     B(I,J)=B(I,J+1)
        BA(I,48)=0.0
290     B(I,48)=0.0
        DO 350 I=1,3
        LA(I,1)=LA(I,2)
350     LA(I,2)=0

        IF(K.GT.150)GO TO 310
C
C       OUTPUTS
C
        WRITE(6,80) T3*(K-1),EXA,SUMA,flaga,EXB,SUMB,flagb,EXC,SUMC,
      $flagc
        WRITE(7,81) T3*(K-1),SCMA(2),SCMA(3),SCMA(5),SCMA(6),SCMA(8),
      $SCMA(9),SCMA(11),SCMA(12),SCMA(17),SCMA(18)
        WRITE(8,82) T3*(K-1),KA,mda,mca,KB,mdb,mcb,KC,mdc,mcc
80      FORMAT(F7.5,1X,3(2(1X,F9.2),1X,F4.1))
81      FORMAT(F7.5,1X,10(1X,F4.1))
82      FORMAT(F7.5,1X,9(1X,I4))
        GO TO 50

310     CONTINUE
        CLOSE(5)
        CLOSE(6)
        CLOSE(7)
        CLOSE(8)
        END

C  ************************************************************************
C                                                                         *
C                              SUBROUTINE PROGRAM                         *
C                                                                         *
C  ************************************************************************

        SUBROUTINE DIFF(K1,A,N1,J1,M2,M3,AM1,CM,L,JJ,KK,EI0,J2,CB1,MC,MMC,
      $TRIPFG,SAT,SUI,MD,MMD,MME,AMPB,K3,LCONT,LDESAT)

        DIMENSION A(20,48),SAT(18),L(3,2),MMD(3,2),MME(3,2),MMC(3,2)
      $,AM1(6),D(6),CPRE(6),CB1(18)
      $,H1(20,20),REN(20,1),AMPB(18),LCONT(18),LDESAT(18)

        W=376.9911
```

```
C
C     SUI --- SUM OF CURRENTS OF KTH SAMPLE
C     SUJ --- SUM OF CURRENTS OF (K-1)TH SAMPLE
C     SUK --- SUM OF CURRENTS OF (K-2)TH SAMPLE
C
      SUI=0.0
      SUJ=0.0
      ASUK=0.0
      CCB1=0.
      D1=0.
      E=0.0
      DO 200 J=0,M2-1
C      PRINT *,'A=',AMPB(J*3+J1)
      SUI=SUI+A(J*3+J1,48)
      SUJ=SUJ+A(J*3+J1,47)
      ASUK=ASUK+ABS(A(J*3+J1,48))
C
C     FAULT DETECTORS
C
700   RB=1.2
      D(J+1)=1.
      IF (ABS(A(J*3+J1,48)-A(J*3+J1,47)).GE.RB*AM1(J+1).OR.ABS(A(J*3+J1,
     $48)).GE.1.2*AM1(J+1))GO TO 190
180   D(J+1)=0.
190   D1=D1+D(J+1)
      CCB1=CB1(J*3+J1)+CCB1
200   CONTINUE
      IF(D1.GE.1.)GO TO 262
C      PRINT *,'NO FAULT '
      L(J1,12)=K1
      J2=J2+1
      IF(J2.LT.12)GO TO 252
      IF(L(J1,12)-L(J1,1).NE.11)GO TO 252
      JJ=0
      KK=0
      MD=0
      MC=0
      J2=0
      DO 307 KIJ=1,12
307   L(J1,KIJ)=0
      TRIPFG=0.
      DO 300 J=0,M2-1
300   SAT(J*3+J1)=0.
      GO TO 252
C
C      THERE IS A POSSIBLE FAULT
C
262   JJ=JJ+1
C      PRINT *,'JJ=',JJ
C
C     DECIDE TO ISSUE BLOCKING SIGNAL IF THE BUS RELAY SCHEME IS
C     EXPECTED TO WORK IN ONE CYCLE
C
C      IF(JJ.GE.24.AND.TRIPFG.EQ.0.)GO TO 252

      IF(JJ.EQ.1)K3=K1
      DO 130 J=0,5
c
c     when ct gets out of saturation, ct saturation detector will not be used
c     until three samples later
```

```
c
      IF (K1-LDESAT(J*3+J1).LT.4.AND.LDESAT(J*3+J1).NE.0)GO TO 142
      LDESAT(J*3+J1)=0
142   CONTINUE
      IF(SAT(J*3+J1).NE.0.)GO TO 1137

c      IF(JJ.GE.3.AND.K1-LDESAT(J*3+J1).GE.3)THEN
      IF(JJ.GE.3.AND.K1-LDESAT(J*3+J1).GE.2)THEN
c
c    the algorithm for ct saturation detector, which is the incremental
c     derivative of the secondary current
c
        DERIV=(A(J*3+J1,48)-2*A(J*3+J1,47)+A(J*3+J1,46))*60.*24./377.
c
c       adaptive threshold factor
c
        if (jj.le.24)adap=0.67
        if (jj.gt.24.and.jj.le.48)adap=0.50
        if (jj.gt.72)adap=0.34
C          ADAP=0.67
C        IF(ABS(DERIV).GE.0.34*CM)THEN
        IF(ABS(DERIV).GE.adap*CM)THEN

          PRINT *,'FEEDER',J+1,'     PHASE',J1,'     CT SATURATEs'
c
c       approximation to magnitude of the current
c
          DUM1=ABS((A(J*3+J1,47)-A(J*3+J1,46))*60.*24./377.)
          DUMMY=SQRT(DUM1*DUM1+A(J*3+J1,47)*A(J*3+J1,47))
          AMPB(J*3+J1)=DUMMY
c
c      backward count how many samples have passed from the zero-crossing to
c      saturation so that the correct polarity may be established
c
          LCON=2
          DO 2111 JJJ=1,JJ-1
          print *,'A(',J*3+J1,48-JJJ,')',A(J*3+J1,48-JJJ)
          IF(ABS(A(J*3+J1,47-JJJ))+ABS(A(J*3+J1,47)).GT.
     $ABS(A(J*3+J1,47-JJJ)+A(J*3+J1,47)))GO TO 2113
          IF (ABS(A(J*3+J1,47-JJJ)).LT.0.1*CM)GO TO 2113
          LCON=LCON+1
          LCONT(J*3+J1)=LCON
2111      CONTINUE
c
c     determine the sign of saturation flag and assign the appropriate
c     polarities to the saturated currents
c
2113      CONTINUE
          IF(A(J*3+J1,47).GT.0.)THEN
          SAT(J*3+J1)=1.
          CPRE(J+1)=A(J*3+J1,47)
          ELSE
          SAT(J*3+J1)=-1.
          CPRE(J+1)=A(J*3+J1,47)
          ENDIF
        ELSE
        CPRE(J+1)=A(J*3+J1,48)
        END IF
      ELSE
      CPRE(J+1)=A(J*3+J1,48)
```

```
      END IF
      GO TO 206

1137   CONTINUE
c
c     once saturations have been detected, the polarities of the saturated
c     currents will be held about half cycle, thenafter, natural currents
c     are used in phase comparision.
c
      PRINT *,'LCONT=',LCONT(J*3+J1)
      IF (ABS(LCONT(J*3+J1)).GE.12)GO TO 1138
       LCT=LCONT(J*3+J1)
       LCONT(J*3+J1)=LCT+1
       PRINT *,'LCONT=',LCONT(J*3+J1)
       IF (SAT(J*3+J1).GT.0)THEN
       CPRE(J+1)=10.
       ELSE
       CPRE(J+1)=-10.
       ENDIF
c       GO TO 206

1138   CONTINUE
c
c    detect if ct gets out of saturation
c
       IF(ABS(SAT(J*3+J1))+ABS(A(J*3+J1,48)).GT.ABS(SAT(J*3+J1)+A(J*3+J1,
     $48)))THEN

         IF (ABS(A(J*3+J1,48)).GT.0.1*CM)THEN

           SAT(J*3+J1)=0.
           LCONT(J*3+J1)=0
           LDESAT(J*3+J1)=K1
           print *,'LDESAT(',J*3+J1,')=',LDESAT(J*3+J1)

           CPRE(J+1)=A(J*3+J1,48)

         END IF
       else
         IF (ABS(LCONT(J*3+J1)).GE.12)then
            CPRE(J+1)=A(J*3+J1,48)
         endif
       ENDIF
c           CPRE(J+1)=A(J*3+J1,48)
206    CONTINUE

130    CONTINUE
c
c     ready for checking an internal fault or an external fault
c
c     determine if the percentage differential scheme should be disabled
c
c
135       EI0=0.
          Do 209 J=0,M2-1
          if (abs(sat(j*3+j1)).eq.1)EI0=EI0+AMPB(J*3+J1)
209       CONTINUE
       IF(EI0.GT.0)GO TO 241

c 240      EI0=0.33*ASUK
```

```
240      EI0=0.2*ASUK
         GO TO 60
241      EI0=SUI

60       continue

c      fast discremination between an internal fault and external fault
c         IF (JJ.EQ.6.AND.KK.eq.0)GO TO 252

         IF (ABS(SUI)-ABS(EI0).GT.0.13*CM)GO TO 220
         KK=KK-1
         IF(KK.LT.0)KK=0
         GO TO 110
220      KK=KK+1
110    CONTINUE

C SECOND PRINCIPLE ---PHASE COMPARISION

       LPOSI=0
       LNEGA=0
       DO 150 J=0,5

c       IF (CPRE(J+1).EQ.0.)GO TO 150
c
c       reject load current for phase comparision
c
       IF (ABS(CPRE(J+1)).lt.1.2*am1(j+1))GO TO 150

       IF (CPRE(J+1).GT.0.)LPOSI=LPOSI+1
       IF (CPRE(J+1).LT.0.)LNEGA=LNEGA+1
150    CONTINUE
       IF (LPOSI.GT.0.AND.LNEGA.EQ.0)GO TO 120
       IF (LNEGA.GT.0.AND.LPOSI.EQ.0)GO TO 170

C       PRINT *,'EXTERNAL FAULT '

       GO TO 252
c
c      phases are coincidetal on negative side
c
170    MC=MC+1
       IF (MC.EQ.1)MMC(J1,1)=K1
       MMC(J1,2)=K1
       IF (MMC(J1,2)-MMC(J1,1).GT.23)GO TO 173
       GO TO 252
173    MC=0
       MMC(J1,1)=0
       MMC(J1,2)=0
       GO TO 252
c
c      phases are coincidetal on positive side
c
120    MD=MD+1
       IF (MD.EQ.1)MMD(J1,1)=K1
       MMD(J1,2)=K1
       IF (MMD(J1,2)-MMD(J1,1).GT.23)GO TO 121
       GO TO 252
121    MD=0
       MMD(J1,1)=0
       MMD(J1,2)=0
```

```
252   CONTINUE
c
c     once one counter pick up, the other is set to zero
c
      IF (MC.EQ.1)MD=0
      IF (MD.EQ.1)MC=0

      END
```

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Vita

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