Analysis and Design for a High Power Density Three-Phase AC Converter Using SiC Devices

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Abstract

The development of a high-power-density three-phase ac converter has been a hot topic in power electronics due to the increasing need in applications like electric vehicles, aircraft and aerospace, where light weight and/or a low volume is usually a must. There are many challenges due to the complicated relationships in a three-phase power converter system. In addition, with the emerging SiC device technology, the operating frequency of the converter can be potentially pushed to tens of kHz to hundreds of kHz at high-voltages and high-power conditions. The extended frequency range brings opportunities to further improve the power density of the converter. The technologies based on existing devices need to be revisited.

In this dissertation, a systematic methodology to analyze and design a high-power-density three-phase ac converter is developed. All the key factors of the converter design are investigated with the goal of high power density. The dissertation is divided into five sections. Firstly, the criteria for passive filter selection are derived, and the relationship between the switching frequency and the size of the EMI filter is investigated. A functional integration concept is proposed together with the physical design approach. Secondly, a topology evaluation method is presented, which provides insight into the

relationships between the system constraints, operating conditions and design variables. Four topologies are then compared with the proposed approach, culminating with a preferred topology under the given conditions. Thirdly, a novel average model is developed for the selected topology, and is used for devising a carrier-based control approach with simple calculations and good regulation performance. Fourthly, the converter failure mode operation and corresponding protection approaches are discussed and developed. Finally, a 10 kW three-phase ac/ac converter is built with the SiC devices. All the key concepts and ideas developed in this work are implemented in this hardware system and then verified by the experimental results.

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Chapter 1 Introduction

This chapter starts with an introduction to the background of high-power-density three-phase ac converters. The state-of-the-art research activities in the corresponding area are reviewed, which helps to identify this work and its originality. The challenges and the scope of high-density design are then presented, followed by an explanation of the structure of the dissertation.

1.1 Background

High power density is one of the key topics for the continual development of power electronics converters [1]. Power converters are designed not only to meet the input and output requirements, but also to achieve a low volume or a light weight in many specific applications. The demand for reduced converter volume is usually driven by the requirements in information technology or hybrid vehicles due to the limited space as well as the progress of the integrated circuit technology [2]-[4]. Additionally, a low converter weight is particularly important for applications in aircraft and avionics, where the weight has a dramatic impact on the cost and feasibility of the operation and maintenance [5], [6].

There has been a large increase in the power density of the power electronics converters over the last few decades, which covers a wide range of applications and converter types. This trend is shown in Figure 1-1 [7]. The increase of power density is mainly achieved by increasing the switching frequency, enabled by faster and lower loss devices. In the early stages of power electronics converters, the power density was

relatively low due to the limited speed of the available switching devices (SCR and GTO), which usually operated at less than hundreds of Hz. Since the 1990's, the power density of the converter has improved greatly with the development of high-power high-switching-frequency devices, like IGBTs and MOSFETs. Figure 1-2 indicates that further improvement is expected in the near future with the implementation of SiC devices.

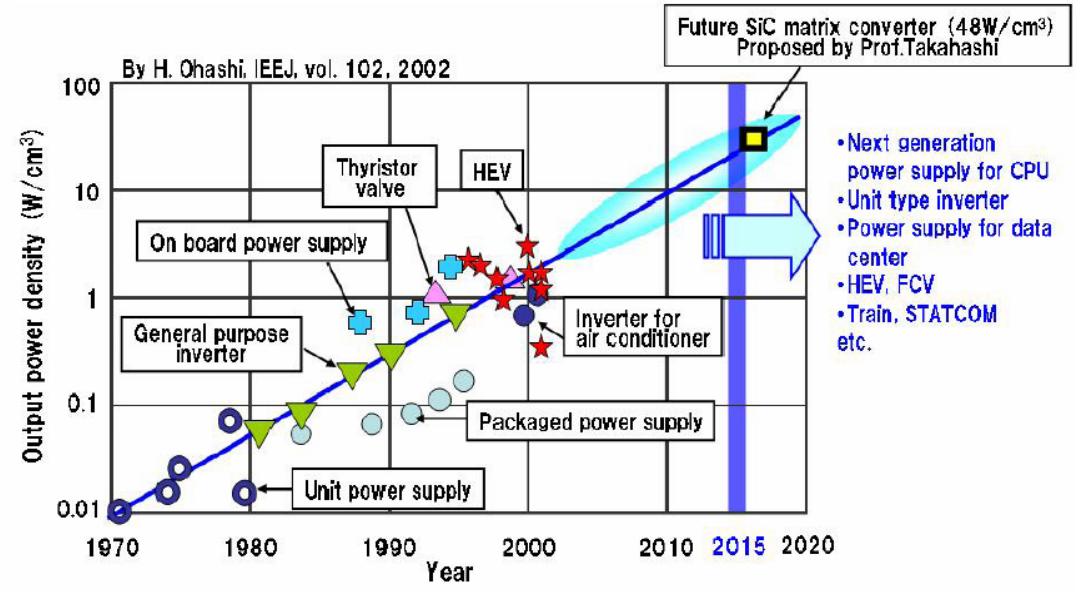


Figure 1-1 Power density roadmap for power electronics converters [7]

The SiC wide band-gap power semiconductor switches and diodes can potentially bring significant improvement to the design of the converter system. The SiC field effect transistor (FET) is expected to out-perform the Si IGBT and Si MOSFET in high voltage ranges due to their low on-resistance and very fast switching characteristics [8]. Figure 1-2 shows the static behavior of the most popular switches as well as the SiC Cascode device [9]. For comparison, the devices are chosen with a breakdown capability of 1000 V and a 1 cm^2 die size. As can be seen from Figure 1-2, the SiC switching device shows much better performance in terms of forward voltage drop. High-voltage SiC Schottky diodes also show very promising static and dynamic characteristics [10]. Figure 1-3

shows the switching loss of a SiC Schottky diode compared to a Si pin diode [9]. In addition to the electrical characteristics, these devices have a higher maximum operation junction temperature, which can potentially lead to reduced cooling effort. The features of the SiC devices provide the possibility of a high switching frequency with low loss, and therefore the flexibility to further improve the converter system design over a very wide frequency range. Technology evaluation and converter design approaches based on existing devices and materials should be revisited and modified in order to fully utilize the SiC devices and further improve the power density. For this reason, SiC devices are selected in this work while studying the high-density power converters.

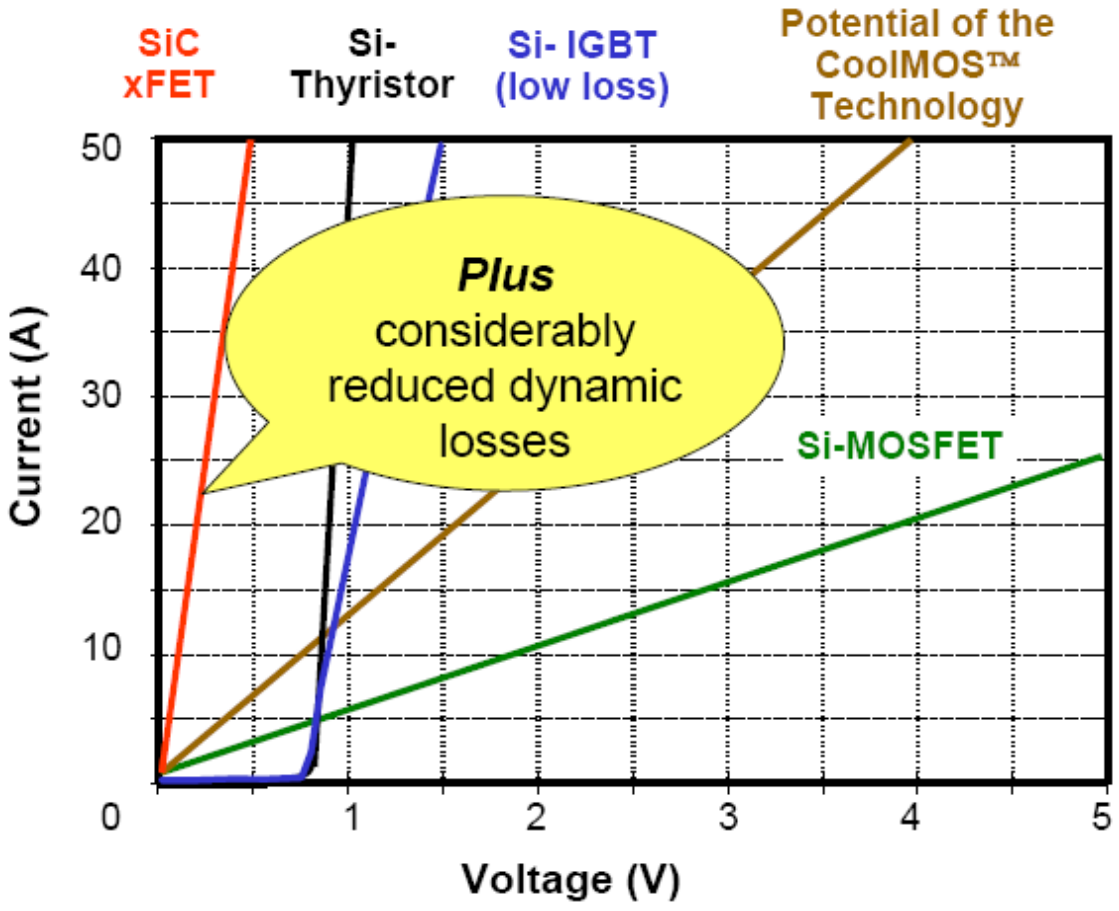


Figure 1-2 Comparison of SiC and Si based devices [9]

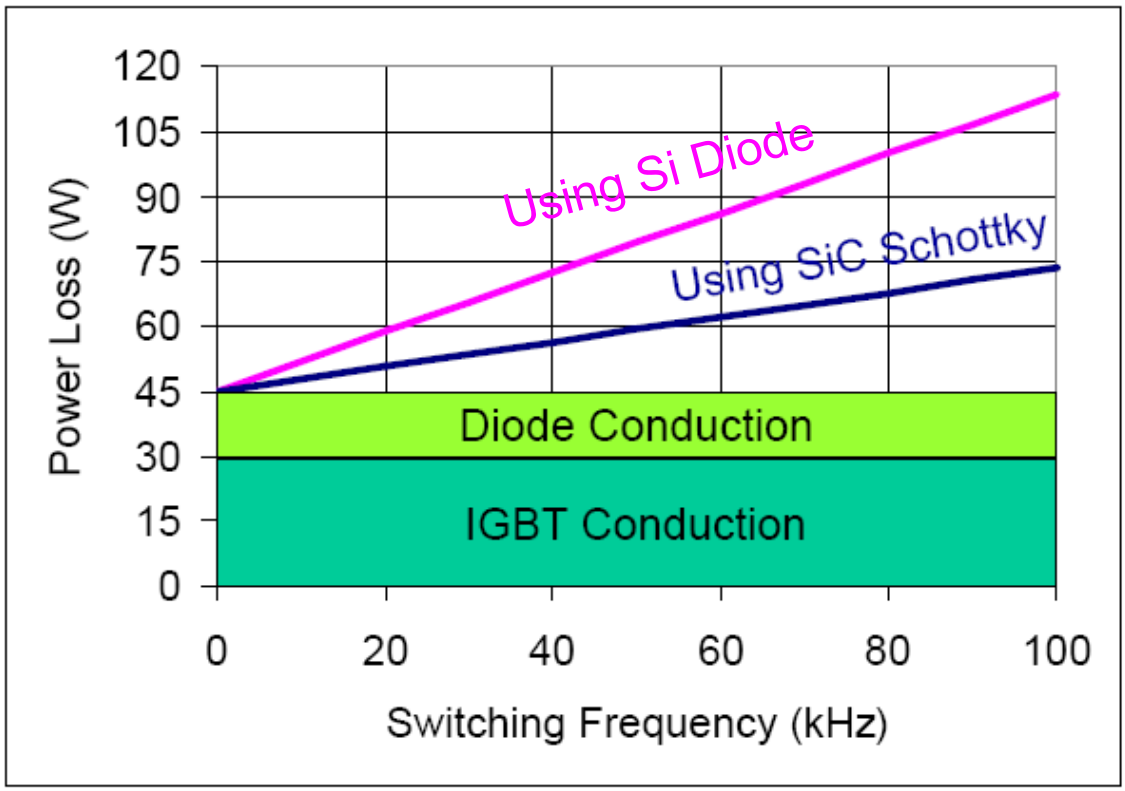


Figure 1-3 Switching loss comparison between Si-pin diode and SiC Schottky diode [9]

A power electronics converter usually consists of the following elements [1]:

- Passive filter components (input/output filter, dc-link filter)
- Cooling system
- Power semiconductors
- Control circuit and auxiliaries
- Interconnection and housing

The size and weight distribution of these elements is highly dependent on the converter structure and the system requirements. There are thousands types of topologies which vary with the application. Different types of topologies may require various approaches for high-density analysis and design. This work focuses on three-phase ac converters, since they are currently widely used in the electric transportation system

(electric vehicle/ship/aircraft) to drive variable speed motors, where high-power-density is usually necessary [2], [6], [11].

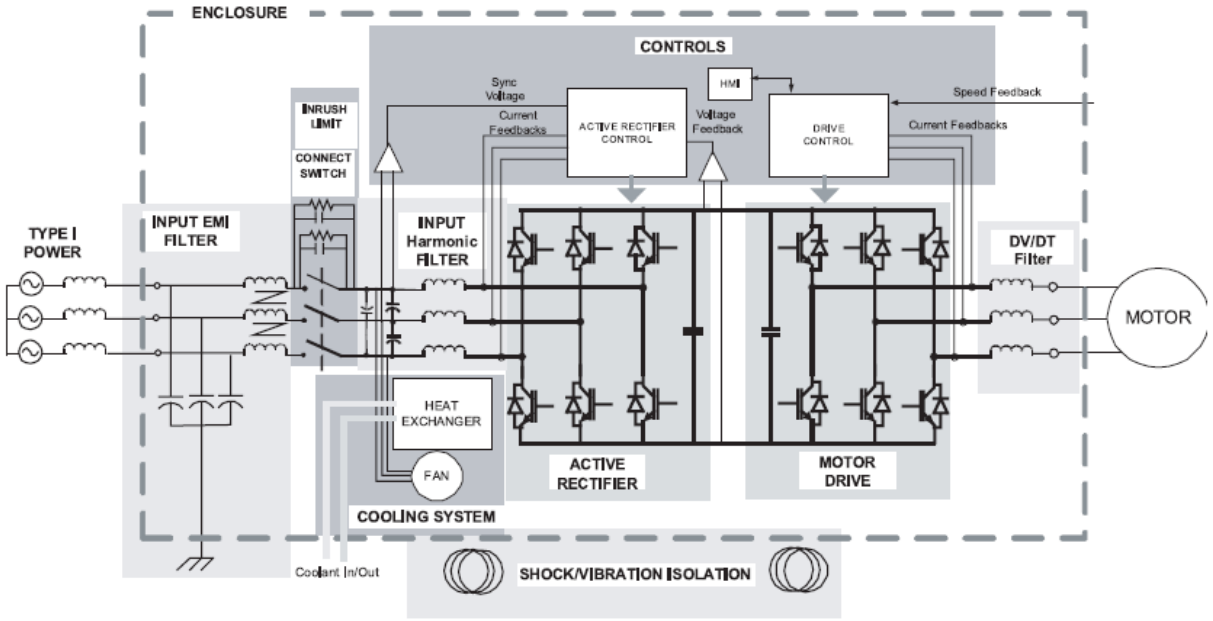


Figure 1-4 Shipboard motor drive [11]

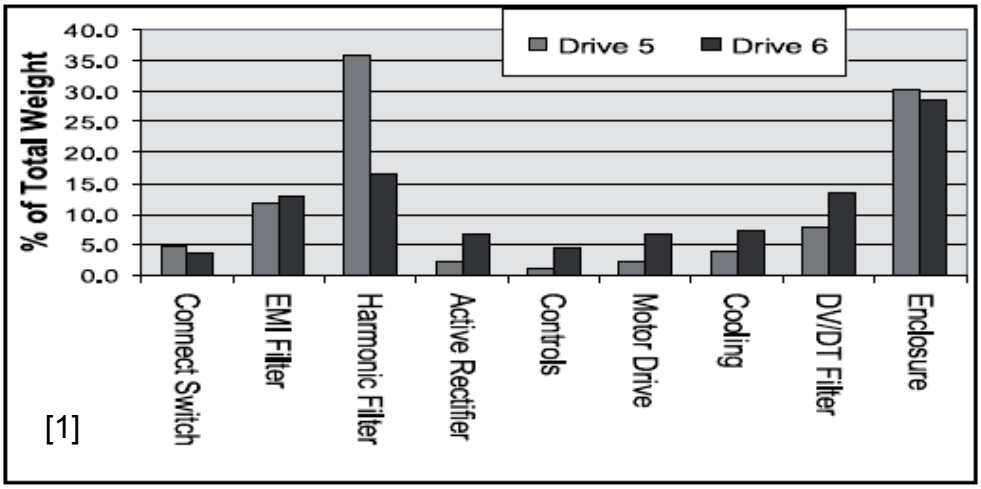


Figure 1-5 Weight distribution of shipboard converter system [11]

Figure 1-4 shows the diagram for a shipboard motor drive as an example of a three-phase ac converter [11]. The size and weight of the converter are heavily influenced by the interface requirements that are imposed on the system. Those interface requirements

include not only electric compatibility, such as power quality standard and EMI standards, but also mechanical concerns, such as shock and vibration. Reference [11] carries out example designs for two different standards, and the components weights of the whole system are shown in Figure 1-5 [11], indicating that for both passive filter designs, the cooling system and the housing are the key contributors to the weight. The housing usually is related to the system profile. Its size and weight will be reduced if the overall size is reduced. Therefore this work did not put special effort on reducing the size and weight of the housing.

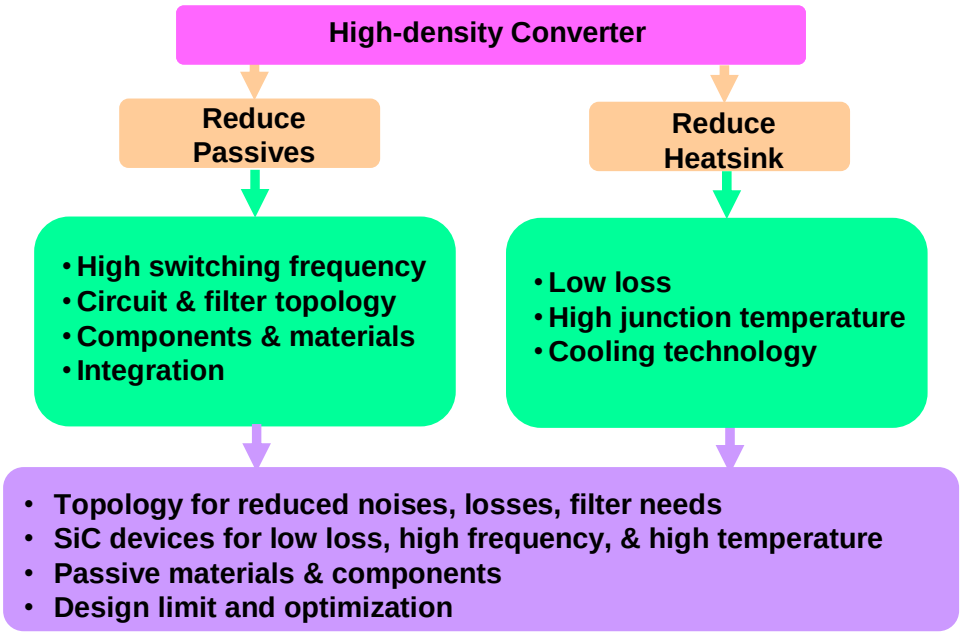


Figure 1-6 Approaches to achieve high power density

There are two ways to reduce the size of the converter by changing the electrical components. One is to reduce the passive filter; the other is to reduce the heatsink, as shown in Figure 1-6. In order to achieve the first objective, several approaches may be appropriate: raise the switching frequency, improve the circuit and filter topology, use new components and materials, and use advanced integration technology. Using a higher

switching frequency is a common practice for reducing the passive components. As mentioned above, the feasible switching frequency range has been greatly extended by the advanced SiC device technology, which will lead to new opportunities for higher-density design. Different circuit topologies will have different noise levels, loss performance, and energy storage requirements; therefore their choice will significantly impact the size of the passive components and the heatsink. Components and materials selection as well as the integration approach are clearly important aspects to reducing the component size. For the heatsink reduction, the effort is on reducing the loss and increasing the device operating junction temperature while searching for better cooling technologies.

Although the approaches discussed above seem to be common methods in the development of high-power-density power electronics converters, the relationship between the overall system performance and the variables is far from well-understood by average practitioners, especially in the extended frequency range offered by SiC devices. In addition, implementation of SiC devices in high-power three-phase converters remains a challenge due to lack of experience and the normally-on characteristics of the JFET structure. Therefore there is a clear need for a systematic analysis and design approach for high-power-density converters using SiC devices, as well as hardware implementation and verification. The literature review in the next section shows the state-of-the-art status of the research related to the high-power-density three-phase ac converter design and hardware development using SiC devices, which helps to define the challenges and research topics of this work.

1.2 State-of-the-art Research

The analysis and design for high-density power electronics converters require a wide area in research focus from the classical electrical aspects of topologies, passive filter design, modulation, and control; to other aspects such as the power semiconductors, cooling techniques, magnetic and dielectric materials, interconnection, and packaging approaches. In this work we focus on the research in the classical electrical aspects.

From the system approach standpoint, J. W. Kolar [1] indentified and quantified the technological barriers for high-power-density converters by investigating the volume of the cooling system and the main passive components as functions of the switching frequency. Analysis is carried out for 5 kW rated power while using high-performance air cooling and advanced power semiconductors. The results indicate a volume density limit of 45 kW/dm^3 for a three-phase PWM rectifier with the present technology. This paper provided a full vision for the design of high-density power converters in a general sense, but the key correlations between the system requirements and the system parameters are not clearly analyzed and reported. Y. Hayashi [7] [12] proposed a high-density power converter design platform. A power converter is classified by four factors: the power device, the converter circuit, including stray parameters, the passive filter, and control. The relationships among the factors are quantified and stored in the design database, but only the power loss estimation of the converter system was reported in this paper.

The practical approach to achieving high-density design is to investigate the key factors one by one and try to obtain minimum weight design for each of them. Obviously topology is one of the key factors, since it has a dramatic impact on the filter size and loss performance. There has been some previous work on evaluating ac converter topologies

[13]-[16]. Reference [13] compares three ac-dc converter topologies in terms of volume and weight for application in future more-electric aircraft. The loss and the input inductance with the corresponding current's harmonic performance are analyzed. Reference [14] investigated three-phase converter topologies for integrated motor drives by discussing the hardware requirements and comparing their performance. The evaluation effort focused on the size of the input inductance and the efficiency of the system. Reference [15] calculated and compared the efficiency and loss distribution of the voltage source and current source drive systems. The impact of the switching pattern is considered, and during the comparison the optimized modulation approach is implemented for the current-source converters. Reference [16] evaluates three-level topologies as a replacement for two-level topologies. The input harmonic filter size and the semiconductor loss are carefully studied. The cost and the life time are also estimated in this paper.

In summary, the previous work discussed above focuses on specific aspects of the converter design. The EMI filter, which is one of the main size contributors for active front end rectifier, is usually ignored in the evaluation. Moreover, the previous work concentrated on the evaluation and comparison of some given topologies instead of providing a systematic analysis and selection tool. In-depth understanding of the correlations between system variables and power density is still desired.

Another key aspect for the high-power-density converter is the passive filter component. In terms of function, the passive filter component includes the input harmonic filter, EMI filter, dc-link filter and output filter. The values of the passive components are related to performance requirements, such as EMI and power quality

standards, as well as to the switching frequency and control strategy. Habetler et al. [17] concluded that the voltage source configuration provides the lowest passive component size, and they also studied the effect of the modulation scheme. References [18] and [19] designed the boost inductor based on THD and the switching ripple requirement. Reference [20] proposed a step-by-step design procedure for the LCL filter to limit the switching frequency ripple injection in the range of 2-150 kHz. The boost inductor and the high-frequency stage are designed separately. For the EMI filter, reference [21] provided guidelines for the design of a multistage structure. This study points out that the capacitors and inductors have to be chosen with equal values in order to obtain maximum attenuation with minimum overall capacitance and inductance. Reference [22] designed a differential-mode input filter based on a harmonic analysis of the rectifier input current and a mathematical model of the measurement procedure, including a line impedance stabilization network (LISN) and the test receiver. However [21] and [22] did not investigate the relationship between the switching frequency and the required filter size. P. M. Barbosa [23] studied the DM filter design for a three-phase boost rectifier. The impact of the switching frequency on the EMI filter parameters was studied based on circuit simulation. However, the boost inductor was not considered to be part of the EMI filter in the design stage; therefore overall minimization may not be achieved. For the dc-link filter selection, reference [24] derived the minimum capacitance as defined in terms of power balance. The energy variations for the input rectifier and the motor load over one switching cycle were carefully studied. Reference [19] developed the criteria for dc-link capacitor selection based on the zeros and poles characteristics of the system. References [19] and [24] are highly dependent on the load condition as well as the

control approach, and complicated calculations are required. It is difficult to directly expand these approaches to general cases. For the passive filter, it can be concluded that the relationship between the switching frequency and the passive parameters, especially for the EMI filter, were not well-studied in the aforementioned work. For the input filter, the low-frequency stage and the high-frequency stage are always designed separately, which may lead to oversized selections.

In addition to electrical analysis and design, hardware implementation using SiC devices is also a challenge, due to the normally-on characteristics as well as the special gate driver requirement of JFETs, the fast switching speed, and lack of application experience. There have been increasing research efforts for SiC device hardware development in recent years [25] – [36]. Some of these efforts are focused on dc/dc applications [25] – [28], where the converter topologies are relatively simple and less fault possibility is expected. References [29] and [30] presented a 2 kW three-phase buck rectifier with a 150 kHz switching frequency. The current source topology takes the advantage of the normally-on characteristics. In 2003, reference [31] claimed to have designed the first three-phase inverter using only SiC JFETs. The inverter was tested up to 5700 W/540 Vdc with 4 kHz switching frequency. However the switching speed was limited to 1 kV/μs with a rather large gate resistance. Also in 2003, reference [32] presented a SiC voltage source inverter module, which was tested at 6500 W/250 Vdc with 4 kHz. Arkansas Power Electronics International, Inc. [33] – [35] fabricated a 4 kW high-temperature inverter module with SiC JFETs, which was tested at about 250 °C with 20 kHz switching frequency. Reference [36] presented a 100 kHz, 1.5 kW SiC sparse matrix converter. However SiC cascode devices are utilized instead of SiC JFETs. The Si

MOSFET in the cascade structure provides normally-off characteristics and allowed the use of a conventional high-speed gate driver, but the Si MOSFET also limits the maximum case temperature. Based on the reviews on the previous work for hardware implementation, we can conclude that for the three-phase voltage source inverters using SiC JFETs, only limited power and switching frequencies have been verified by hardware. There is yet to be verification of a three-phase voltage source inverter using SiC JFETs in an ac-ac converter system.

In summary, in terms of electrical design, there has been some research on various aspects for high-power-density converter design, but an in-depth systematic understanding and design tool are still desired. In addition, as the SiC devices advance, the converters operate at higher frequencies and/or have higher power ratings. The corresponding analysis and design have to cater to this need. For the hardware implementation in three-phase converters, the performance of SiC devices was verified with limited operating conditions. Higher power and/or higher switching frequency operation in a full ac/ac system needs to be explored.

We need to emphasize that control design and implementation are also key issues for high-density converters, since the higher switching frequency and smaller passive components will lead to increasing requirements for calculation speed and control performance. Since this depends on the topology, it will be included in the later chapters of this work.

1.3 Research Challenges and Objectives

According to our survey, the state-of-the-art research has investigated various aspects of high-density design for three-phase ac converters. However the system-level understanding and design approach, especially for the extended operation frequency range offered by the SiC devices, is not established. The hardware verification for SiC devices implemented in a full ac/ac system is still desired for higher switching frequencies and/or higher-power operating conditions. Many challenges still exist due to the complicated correlations in the three-phase power converter system and also the new characteristics of the SiC devices.

When developing a new converter for high-density applications, the design must take into account all aspects contributing to the converter size and weight, which requires investigation into the correlation between all major design parameters. There is thus a clear need for a systematic analysis considering the strong interdependence of all design variables and constraints. For example, increasing the switching frequency generally helps to reduce the passive size, but it also increases the converter switching loss and therefore heat sink size. As is shown later in the work, even the relationship between the filter size and switching frequency is not monotonous, due to changing spectrum characteristics and the attenuation requirements of harmonic and EMI standards. Topology is obviously another important aspect for the system design. It impacts the loss, passive filter selection and the control requirement. Determining how to make a fair comparison among different topologies under given conditions is still an issue. The controller is normally not a concern in terms of power density. However, for high-switching-frequency and high-control-bandwidth designs, the controller calculation time

and the regulation performance may become a constraint on the system. Therefore a high-performance control approach is desired to guarantee the design feasibility. Failure mode analysis and the corresponding protection are also significant, especially for applications in the aircraft and aerospace industry, where high reliability is essential [37]. The protection circuit will impact the converter size, and its requirements vary for different topologies, devices and passive parameters. It should be also taken into consideration during the design stage. For the voltage source converter built with SiC JFETs, a shoot-through failure could be a big concern for the hardware implementation due to the normally-on characteristics of the devices.

Corresponding to the challenges discussed above, the objective of this work is to develop a systematic methodology for the analysis and design of a three-phase high-power-density converter using SiC devices, and to verify the developed concepts with hardware. The dissertation accomplishes five tasks:

(1) Develops system-level criteria for minimum passive component design and selection considering all the key correlations, and investigates the optimal physical design for integration function.

(2) Provides a systematic tool for topology evaluation, based on which different topologies can be fairly compared under the given conditions and constraints.

(3) Develops a mathematical model as well as a high-performance control scheme with low calculation effort and good regulation for the selected topology.

(4) Analyzes the failure mode of the system and develops corresponding protection approaches.

(5) Builds a 10 kW three-phase ac/ac system using SiC devices. All the ideas and concepts developed in this work are included and tested.

These five items form the main content of this work. A review of the relevant literature is included within the introductory sections of each chapter.

1.4 Dissertation Organization

The dissertation presents a systematic methodology for analyzing and designing a high-power-density three-phase ac converter. The chapters are organized as follows.

Chapter 2 starts with the standard requirements on the source side. A double Fourier analysis is carried out to achieve the voltage noise spectrum, based on which the required EMI filter corner frequency can be obtained. The relationship between the switching frequency and the filter size is carefully studied. The criteria for other filter passives are developed with the system operation requirements. A filter integration concept is included in this chapter, as well as the physical design approach.

Chapter 3 presents a systematic methodology for the topology evaluation of three-phase ac converters. All the design constraints, conditions and variables of the converter system are clearly defined, and the correlations between the key factors are carefully investigated. Based on the proposed approach, four popular topologies are evaluated and compared with weight metrics under given conditions.

Chapter 4 develops a novel wide-frequency-range average model for the Vienna-type rectifier, which is chosen based on the topology comparison results in Chapter 3. An optimal zero-sequence injection is proposed for dc-link voltage balance. Using the proposed model, a carrier-based control approach is presented for the Vienna-type

rectifier, and a space vector representation is utilized to analyze the feasible operation region of this control approach.

Chapter 5 analyzes a specific over-voltage failure mode that is related to the Vienna-type rectifier topology. Two protection approaches corresponding to this failure mode are discussed, and the impact of the input inductance is investigated. Then a novel protection circuit for shoot-through failure is proposed and analyzed, which is also implemented into the converter built with SiC JFETs.

Chapter 6 presents the hardware design and development of a 10 kW three-phase ac/ac SiC converter that implements all the concepts developed in this work. The system structure, component selection, control interface, signal sensing, circuit protection and gate driver design are described in detail. The experimental results are presented and analyzed.

Finally Chapter 7 summaries the entire dissertation and discusses some ideas for future work.

Chapter 2 Passive Filter Minimization

This chapter develops design approach for finding the lower bound of the passive components for three-phase ac converter. Since the passive filter design highly relates to the topology, the two-level voltage source converter is considered as an example in this chapter. And the methodology can be extended to other three-phase ac converters. The impact of the switching frequency on the input filter is carefully studied in this chapter and some favored operating points are found. The rules for ac line inductance and dc-link capacitors are also derived from the consideration of ripple and system stability. The design approach is verified by simulation.

2.1 Introduction on Filter Design

The passive components are essential components in the converter system. They are used to maintain the dc link voltage, attenuate the input current noise and suppress the output surge voltage caused by the feeding cable. For the converter system with diode bridge front end rectifier, the filter components are usually very bulky and heavy due to its low frequency harmonics. For the converter topologies with active front end, the interaction between the grid and the converter system can be improved and the size of the harmonic filters can be highly reduced. But the front end system may also raise the issues of electromagnetic interference (EMI), which requires additional filtering [38]. At some occasions the EMI filter is also a key contributor to the size of the converter system [11]. Therefore it is still desirable to minimize the passive components value and size even in the topologies with active front end.

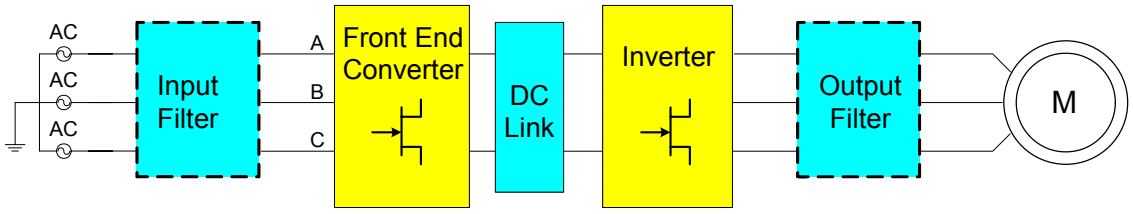


Figure 2-1 Diagram for back-to-back VSC

Section 2.2 mainly focuses on the parameters selection for a back-to-back voltage source converter (VSC) with a three-phase motor load, since it is one of the most important cases in the electric industry. Figure 2-1 shows the general configuration of an AC active VSC with required filter with a motor load. The passive components include DC link capacitor, AC input inductor, and the input EMI filter. In some cases the output filter is also required according to the concerns of over voltage and over current suppression [39] [40]. The output filter design relates to the cable length and the motor insulation, which is not in the scope of this work.

The values of the passive components under consideration are related to the performance requirements, as well as to the switching frequency and control strategy. There have been some previous studies on the passive design for the rectifier and inverter system. Habetler et al. [17] concluded that the voltage source configuration provides the lowest passive components size, and the effect of the modulation scheme was also studied. Ref [18] [19] designed the boost inductor based on THD and switching ripple requirement. Ref [20] developed the criteria for LCL filter by designing the boost inductor and the high frequency stage. Ref. [24] [41] investigated the dc link minimum capacitance from the power balance point of view, and [19] sized the capacitors based on the zeros and poles characteristics of the system. These studies were all based on the

normal operation mode with specific control techniques. In addition, the EMI filter, which can be a dominant part of the size and cost in the active front end, was not discussed in the previous work.

Generally speaking, higher switching frequency leads to smaller passives. But that is not necessarily true for EMI filter due to the noise spectrum. In section 2.2, the proposed procedure for passive minimization starts with selection of modulation scheme and switching frequencies based on EMI filter considerations. This is especially important for high-switching frequency (>tens of kHz) converters based on advanced Si or SiC devices. The impact of the switching frequency on the input filter is carefully studied, culminating with some favored operating points from the EMI standpoint.

Under a given switching frequency the minimum AC line inductance and DC link capacitance are then selected considering control, stability, power quality and dynamic performance requirements. The impact of the DC link ripple current and the failure mode performance on the parameter values are also investigated. In the end of this section, an integration design concept for the input filter is presented. It indicates that the boost inductor and the DM inductance of the EMI filter can be design as one entity for high switching frequency applications, while in the previous works the EMI filter is normally designed after the boost inductor is selected. In the end of this chapter, a Saber circuit model is built and the simulation results verify the design concepts.

The discussions below use back-to-back two-level VSC as example. The approaches can be extended to other three-phase topologies.

2.2 Passive Parameters Selection and Minimization

2.2.1 Switching Frequency Selection and EMI Filter Design

It is well know that switching frequency has a great impact on the EMI performance of the system. But the relationship was not well studied so far. Usually, the conducted EMI standard starts from the frequency of 150 kHz. If the switching frequency is lower than 150 kHz the high order harmonics of the switching frequency are required to be damped while the first order harmonic should be considered when the switching frequency is higher than 150 kHz. Therefore the relationship between the switching frequency and the EMI performance could be non-monotonous. In order to investigate the impact of the switching frequency on the required attenuation, which corresponds to the filter size, a two-level VSC as well as a commercial EMI standard for aircraft are implemented as an example in this section.

Since the phase-leg pulsating voltage is the source for the input current ripple and EMI noise, its spectrum is an important part for the analytical filter design. Double Fourier integral transform is applied to determine the harmonic spectrum of the phase-leg voltage. The harmonic components are given in complex form [42].

$$C_{mn} = \frac{1}{2\pi^2} \int_{y_r}^{y_f} \int_{x_r}^{x_f} V_{dc} e^{j(m\omega_s t + n\omega_0 t)} d(\omega_s t) d(\omega_0 t) \tag{2-1}$$

where V_{dc} is the voltage across the dc link, ω_s is the switching frequency, ω_0 is the fundamental frequency. The outer integral limit y_f and y_r, the inner integral limit x_f and x_r are determined by the modulation scheme.

Two kinds of space vector modulation schemes are discussed in this section: center-aligned continuous modulation (SVM) and center-aligned discontinuous modulation (DPWM). The modulation index is defined by

$$M = \frac{2V_{ph}}{V_{dc}} \tag{2-2}$$

where V_{ph} is the amplitude of the phase voltage. Table 2-1 [42] and table 2-2 show the outer and inner double Fourier integral limits for SVM and DPWM respectively.

Table 2-1 Double Fourier Integral Limits for SVM (Phase A)

y_r	y_f	x_r (rising edge)	x_f (falling edge)
0	$\frac{\pi}{3}$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$
$\frac{\pi}{3}$	$\frac{2}{3}\pi$	$-\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$	$\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$
$\frac{2}{3}\pi$	π	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$
$-\frac{\pi}{3}$	0	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$
$-\frac{2}{3}\pi$	$-\frac{\pi}{3}$	$-\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$	$\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$
$-\pi$	$-\frac{2}{3}\pi$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$

Table 2-2 Outer and Inner Double Fourier Integral Limits for DPWM (Phase A)

y_r	y_f	x_r (rising edge)	x_f (falling edge)
$-\frac{\pi}{6}$	$\frac{\pi}{6}$	$-\pi$	π
$\frac{\pi}{6}$	$\frac{1}{2}\pi$	$-\pi\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})$	$\pi\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})$
$\frac{1}{2}\pi$	$\frac{5}{6}\pi$	$-\pi(1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6}))$	$\pi(1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6}))$
$\frac{5}{6}\pi$	$\frac{7}{6}\pi$	0	0
$\frac{7}{6}\pi$	$\frac{3}{2}\pi$	$-\pi(1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6}))$	$\pi(1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6}))$
$\frac{3}{2}\pi$	$\frac{11}{6}\pi$	$-\pi\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})$	$\pi\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})$

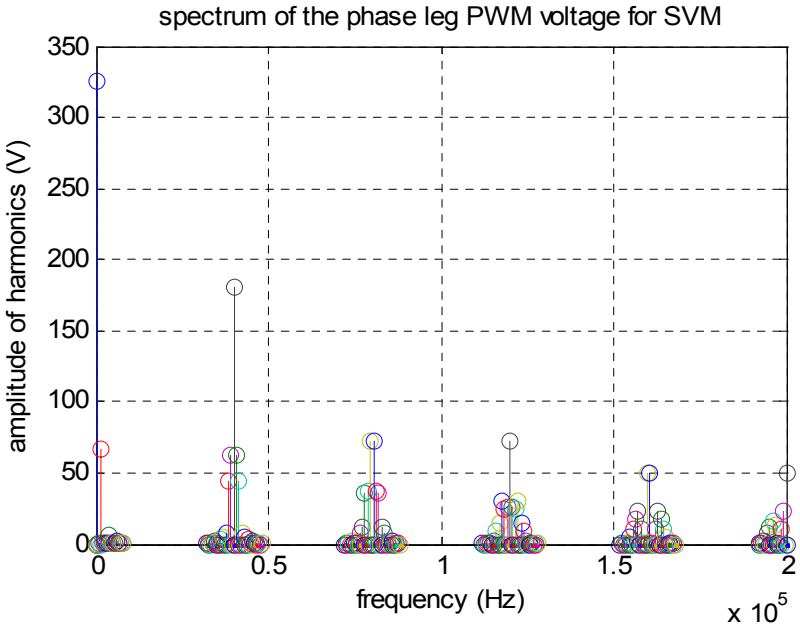


Figure 2-2 Spectrum analysis for SVM

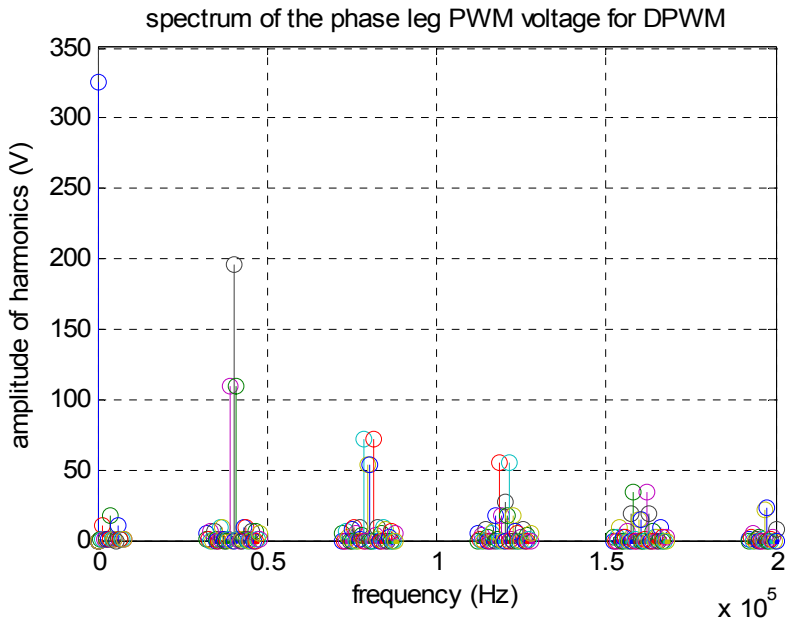


Figure 2-3 Spectrum analysis for DPWM

Assuming ideal switching behaviors, we can obtain the noise voltage spectrum for a given modulation scheme based on the data of the two tables. Figure 2-2 and Figure 2-3 show the noise spectrum results for a sample three-phase boost rectifier running at 650V DC link voltage and 40 kHz switching frequency with space vector modulation scheme (SVM) and 60° discontinuous pulse width modulation scheme (DPWM) respectively [42]. As we can see, the amplitudes of the first switching harmonic and its adjacent side band for DPWM are higher than those of SVM. But the amplitudes of the high order harmonics for DPWM decrease more quickly than SVM. It indicates that DPWM will cause higher switching current ripple. From the EMI point of view, if the switching frequency is lower than 150 kHz, which is the starting point for radio frequency conducted emission requirement, DPWM will lead to lower EMI noise level as it has lower high order harmonic component. In the applications with SiC devices, the switching frequency of tens of kilo Hertz can be achieved. The low-frequency harmonics caused by switching is not a concern, so DPWM is favored as it has better EMI noise

performance and lower semiconductor loss compared to SVM. All the following analysis in this work is based on DPWM.

With the phase-leg voltage spectrum differential mode (DM) and common mode (CM) noise can be extracted as

$$V_{CM} = \frac{V_a + V_b + V_c}{3} \tag{2-3}$$

$$V_{DM} = V_{(a,b,c)} - V_{CM} \tag{2-4}$$

where $V_{(a,b,c)}$ is the phase-leg voltage spectrum, V_{CM} and V_{DM} are the CM and DM noise respectively.

Figure 2-4 and Figure 2-5 show the DM and CM noise spectrum. Figure 2-6 shows the relationship obtained between the required filter corner frequency [43] (a two-stage filter with 80 dB attenuation is assumed, as shown in Figure 2-7) and the switching frequency based on the DO-160E standard [44], which defines the maximum power line noise current as 53 dBμA at 150 kHz. For simplicity, the terminal impedance of the LISN is assumed to be 50 Ω in this analysis. A higher filter corner frequency is desirable since it indicates a smaller filter. The non-monotonous relationship in Figure 2-6 indicates that higher switching frequencies do not necessarily lead to higher filter corner frequencies, unless the switching frequencies are beyond 300−500 kHz. Clearly, there are some preferred switching frequencies, from the standpoint of input EMI filters, as can be seen in Figure 2-6: below 40 kHz, 70 kHz, 140 kHz, or above 300-500 kHz.

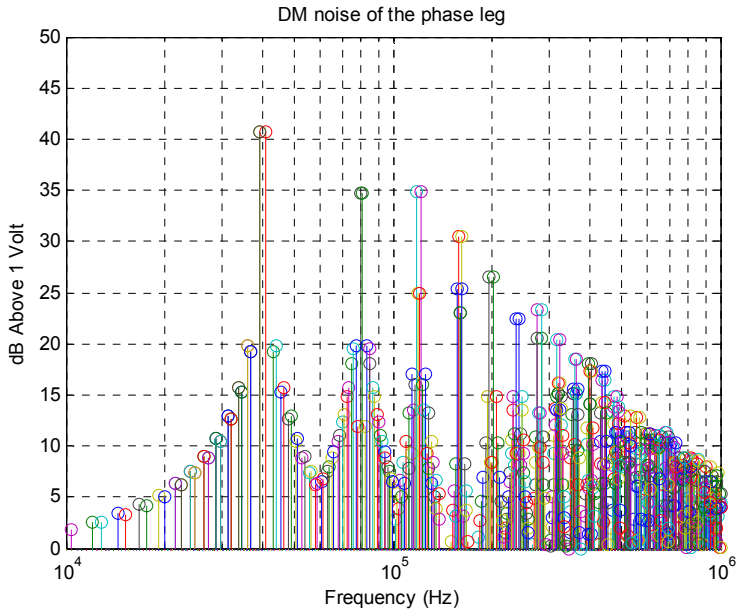


Figure 2-4 Differential mode noise

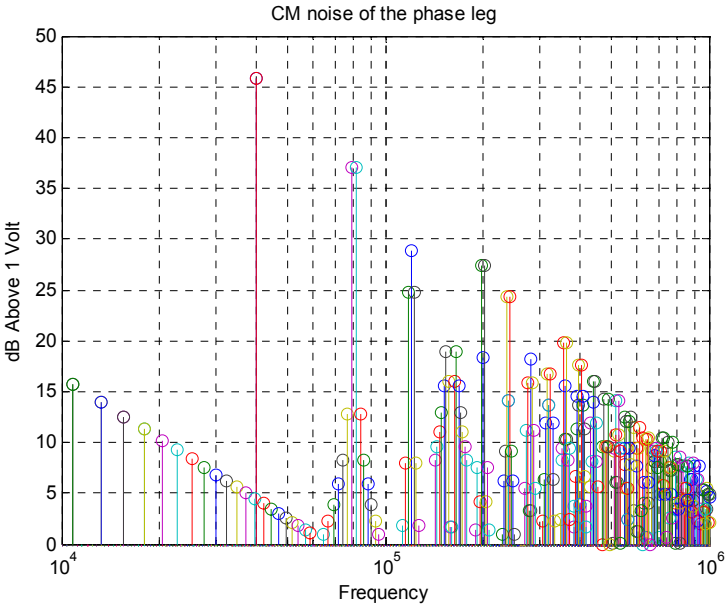


Figure 2-5 Common mode noise

Similar relationships can be established for other voltage levels, other topologies, or different filter structures. In final switching frequency determination, the impacts on the boost inductor and the loss should be also included. The result will vary with the given specs, and will also depend on which factor plays the dominant role. As can be seen in

the later sections, the impact of EMI filter is dominant compared to the harmonics filter under the conditions studied in this dissertation.

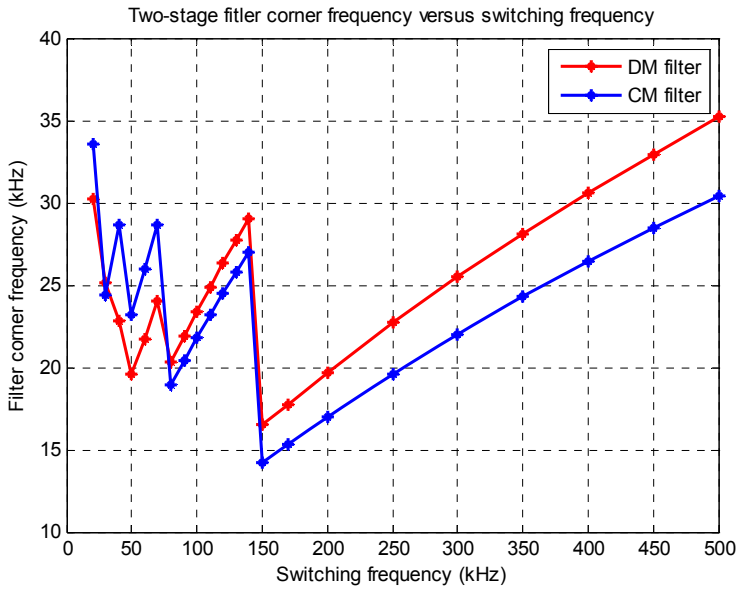


Figure 2-6 Corner frequency vs. switching frequency

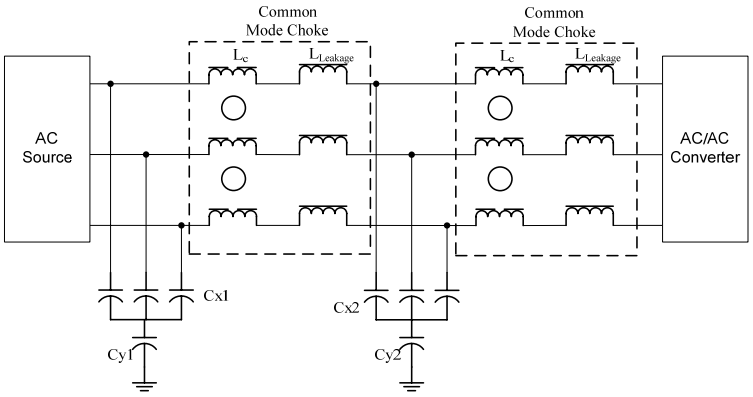


Figure 2-7 Two-stage EMI filter

Figure 2-6 indicates that if the switching frequency is lower than 40 kHz, the EMI filter size will decrease while the switching frequency decreases. But at the same time the required boost inductance will increase due to the higher switching current ripple. In

addition, the power quality standard defines the harmonic current requirement which is usually specified in the range up to 40 times of the fundamental frequency.

Table 2-3 Harmonic Current Limits

Harmonic Order	Limits
3^{rd}, 5^{th}, 7^{th}	$I_h = 0.02\ I_1$
Odd Triplen Harmonics (h = 9, 15, 21, ..., 39)	$I_h = 0.1\ I_1 / h$
11^{th}	$0.1\ I_1$
13^{th}	$0.08\ I_1$
Odd Non Triplen Harmonics 17, 19	$0.04\ I_1$
Odd Non Triplen Harmonics 23, 25	$0.03\ I_1$
Odd Non Triplen Harmonics 29, 31, 35, 37	$I_h = 0.3\ I_1 / h$
Even Harmonics 2 and 4	$I_h = 0.01\ I_1 / h$
Even Harmonics > 4 (h = 6, 8, 10, ..., 40)	$I_h = 0.0025\ I_1$

For example, Table 2-3 shows the current harmonic limits for the aircraft [44], where I_1 is the amplitude of the fundamental component. Given the 400-800 Hz fundamental frequency range, the limit is defined up to 32 kHz. If the switching frequency locates in this region the switching ripple current also needs to meet the power quality standard, which brings additional requirement for the filter design. Assuming the same filter structure, C_{x1} will not have much impact on the harmonic performance since the source impedance is usually much lower compared to the capacitor in this frequency range. Therefore the input filter is simplified to a LCL structure for the low frequency current harmonics. The relationship between the harmonic amplitude and the filter parameters is

given by (2-5), where I_k and u_k is the amplitude of the k[th] current and voltage harmonic respectively.

$$I_h = \frac{u_h}{\omega L \cdot \left|2 - \omega^2 LC\right|} \tag{2-5}$$

u_k can be achieved by the spectrum analysis. In this case, the DM noise spectrums around the first order switching frequency are dominant. Figure 2-8 shows the DM noise of the first order switching frequency for the case of 30 kHz with 800 Hz fundamental frequency. As can be seen, the second order side band is much higher than the other side band harmonics and therefore it will determine the filter size. On the other hand, as far as the switching frequency is much higher than the fundamental frequency, the amplitude of the spectrum will not change with the frequency. We can use the same amplitude value for u_k when doing the calculation for different operation point. Then with (2-5) we can obtain the required inductance for a given harmonic limit. Figure 2-9 shows the required inductance versus switching frequency while assuming the capacitance to be 1 μF. For comparison the inductance to meet EMI requirement is also shown in the same figure. As can be seen, the required inductance increases dramatically once the switching frequency enters the range defined by the power quality standard. Although the lower switching frequency can improve the efficiency and reduce the heatsink, the total system size may still increases due to the tremendous increase of the inductors.

Therefore the low switching frequency boundary is selected to be 40 kHz to avoid relatively low-order harmonics, given the 400-800 Hz fundamental frequency range. For a different design spec, a lower or higher switching frequency range may be selected.

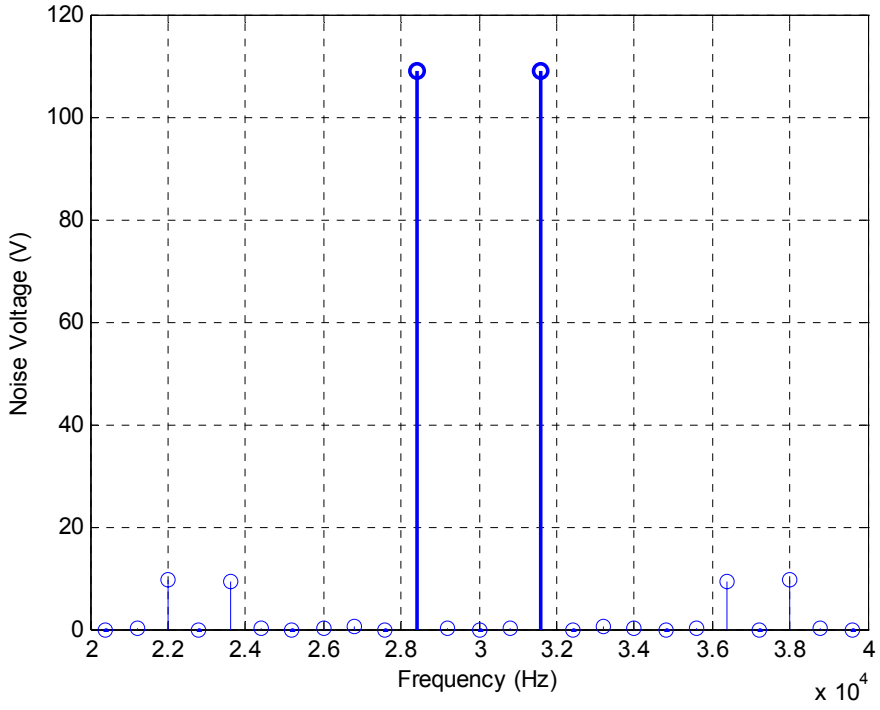


Figure 2-8 DM noise spectrum around the first order switching frequency

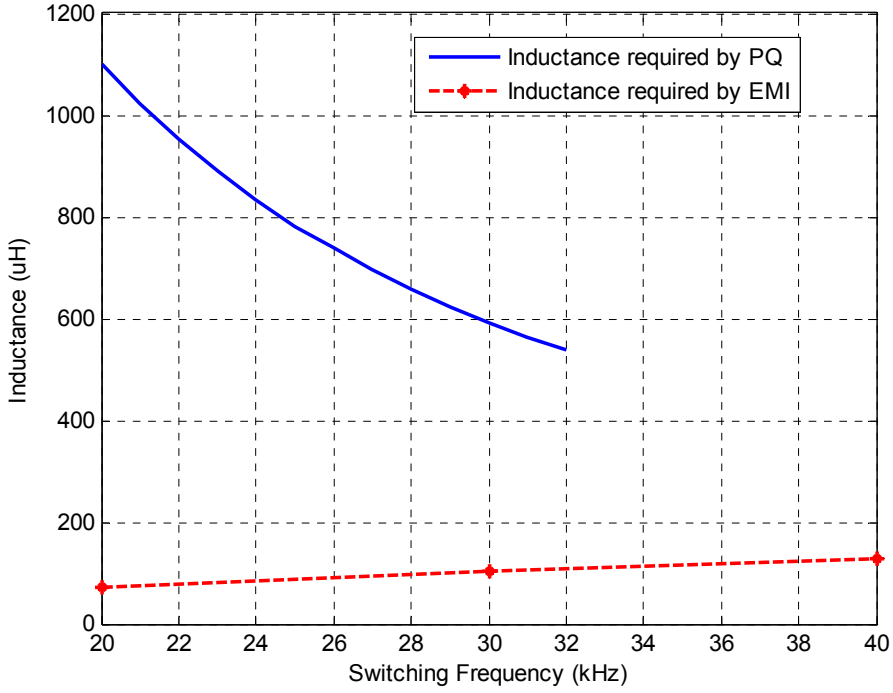


Figure 2-9 Required inductance for power quality standard and EMI standard

2.2.2 Boost Inductor and DC-Link Capacitor Design

A. Boost Inductance

When determining the boost inductance, considerations are needed for AC current harmonics, maximum ripple and inrush current. THD can be obtained with the spectrum analysis results under a given switching frequency. It is given by

$$THD = \frac{\sqrt{\sum (\frac{u_i}{\omega_i L})^2}}{I_1} \tag{2-6}$$

where u_i is the amplitude of the harmonic voltage with order i, ω_i is the harmonic frequency, L is the harmonic inductor and I_1 is the fundamental current.

Another consideration for the boost inductance design is the instantaneous switching ripple. It should be suppressed into a reasonable level to guarantee the control feasibility and the proper operation of the switching device [45]. The current ripple will vary as the mains input voltage varies over a fundamental cycle. Here we only discuss the point when the fundamental phase current reaches the peak value as it is important for the inductor physical design. The peak current can be approximated by:

$$i_{peak} = i_m + \frac{1}{2}(1 - \frac{3}{4}M)T_s V_a / L \tag{2-7}$$

where M is the modulation index, i_m is the amplitude of the fundamental phase current, T_s is the switching cycle and V_a is the voltage of phase A at that instant. Considering the worse case, the possible minimum modulation index and maximum peak phase voltage should be utilized in (2-6).

During the inrush period, the rectifier works like a diode bridge, the peak current should be constrained due to the limit of the semiconductor device. The relationship between the peak inrush current i_{peak} and the passive parameters is given by

$$Li_{peak}^{2} = \frac{1}{2}C(V_{Line} - V_{initial})^2 + \frac{3}{4}LI_m^{2} \tag{2-8}$$

where V_{line} is the line-to-line voltage, $V_{initial}$ is the initial voltage of the DC link cap when the inrush occurs, and I_m is the amplitude of the line current. With (2-6), (2-7) and (2-8), we can determine the minimum line inductance for the given current requirement.

Actually the boost inductor can also be a part of the EMI filter. So the total input inductance should be the larger one between the two values designed for the EMI filter and the line inductor respectively. Therefore the input filter can be designed as one entity to achieve both harmonic filtering and EMI suppression. For high switching frequency cases, the required harmonic attenuation is small. There is an opportunity to use only EMI filter as the whole input filter since the leakage inductance of the common mode choke is big enough to meet also the harmonic requirement.

B. DC Link Capacitance

For the DC link capacitors selection, considerations are needed for energy storage and system stability.

DC link capacitor is utilized to maintain the DC link voltage for robustness consideration and operation requirement. From the energy point of view, only extreme cases are considered for simplicity. We assume in one switching cycle the rectifier input power is zero while the inverter output power reaches maximum and vice versa. The relationship between the capacitance and the voltage dip is given by

$$C = \frac{P_{\max}}{(V_{dc}\Delta U \pm \frac{1}{2}\Delta U^2) f_{sw}} \tag{2-9}$$

where f_{SW} is the switching frequency, U_0 and ΔU denote the DC link voltage and voltage ripple.

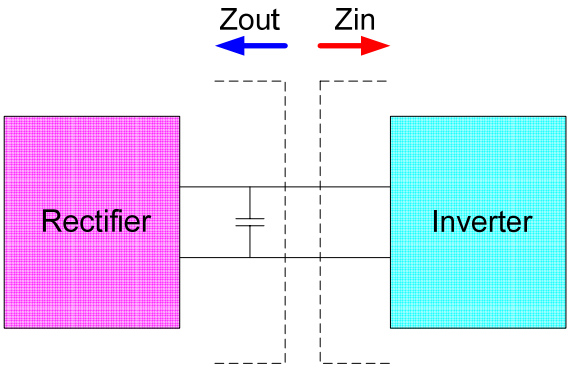


Figure 2-10 Cascaded subsystem diagram

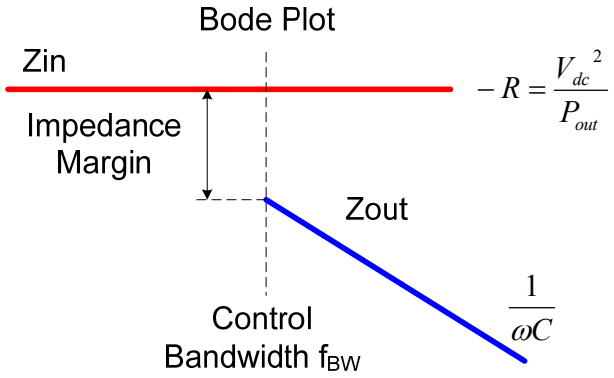


Figure 2-11 Impedance bode plot

Another concern for the DC link capacitor is the system stability. The rectifier and the inverter are two cascaded subsystems, as shown in Figure 2-10. In order to avoid the interaction between the two systems the output impedance of the rectifier should be lower than the input impedance of the inverter [46]. Figure 2-11 illustrates the impedance relationship in bode plot. The inverter can be considered as a constant power load. And we assume that the output impedance is very low in the control bandwidth while the DC link capacitor is dominant outside the bandwidth. Then the constraint for DC link capacitance is given by

$$20\lg(\frac{V_{dc}^{2}}{P_{out}}) - 20\lg(\frac{1}{2\pi f_{BW}C}) \geq Z_m \qquad (2\text{-}10)$$

where f_{BW} is the control bandwidth, Z_m is the impedance margin. Then we can decide the minimum capacitance by (2-9) and (2-10) with the specific system requirement.

In addition to the capacitance, the rms current stress is very important for the capacitor selection as it determines the actual number of capacitors required to be connected in parallel. For voltage source converter, the analytical calculation of rms current stress on the DC link is given by [47]

$$I_{link} = I_M \sqrt{M[\frac{\sqrt{3}}{4\pi} + \cos^2\theta(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M)]} \tag{2-11}$$

where M is the modulation index, I_M is the amplitude of the phase current and θ is the power factor angle. Then the rms current stress on the capacitor can be approximated by

$$I_C = \sqrt{I_{link\_rec}^2 + I_{link\_inv}^2} \tag{2-12}$$

C. Failure Mode Consideration

The parameters of the passive components will also impact the failure mode performance of the system. Figure 2-12 shows the switch short failure simulation results with the DC capacitance of 10uF and 100 μF respectively (line inductance is 100 μH for both cases). All other switches are assumed to open after the failure is detected, and the input side circuit breaker to open when the phase current crosses zero. As can be seen from the figures, the DC link voltage in 10 μF case is much higher, extra DC link protection is needed, which will increase the cost and weight of the system. Usually, lower line inductance and higher DC link capacitance can decrease the peak of the over voltage in DC link under failure modes. When designing passive components for a converter, this impact should be taken into consideration.

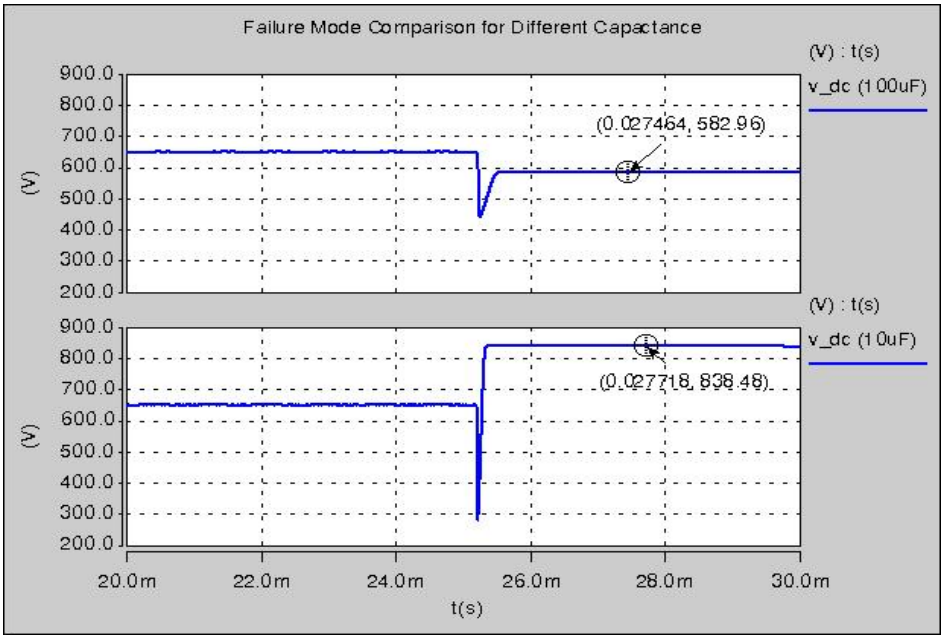


Figure 2-12 Failure mode comparison for 10uF and 100uF DC link capacitance

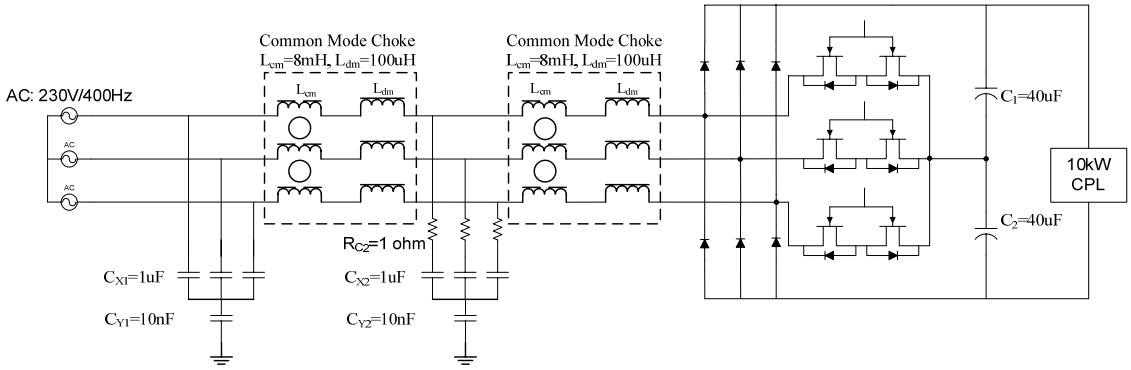


Figure 2-13 Circuit diagram for Vienna rectifier

2.2.3 Simulation Verification

In order to verify the design concept developed in this work, a three-phase Vienna type rectifier simulation model is built in Saber. The circuit diagram is shown in Figure 2-13. The parasitic capacitance from the bus to the ground is not considered in this simulation. For the EMI measurement, a 50 Ω LISN is assumed.

Table 2-4 Operation Conditions and Design Results

Source voltage	230V (line to neutral, rms)
Source frequency	400Hz
DC link voltage	650V
Switching frequency	70kHz
DC Load	10kW constant power load
CM inductor	8mH
DM inductor	100μH
DM capacitor	1μF
CM capacitor	10nF
Damping resistor	1Ω
DC link capacitor	40μF/each

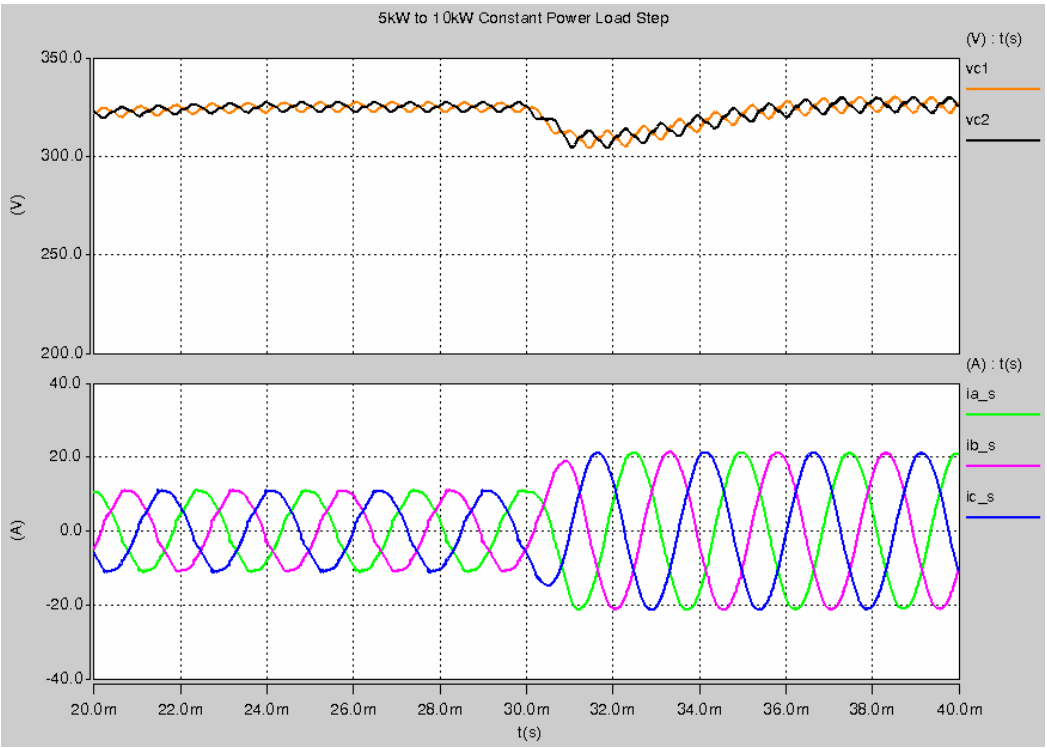


Figure 2-14 Simulation results for load step change (The top traces are the capacitor voltages, the bottom traces are the source input current.)

The operation conditions are shown in Table 2-4. The switching frequency is chosen to be 70 kHz according to the EMI considerations described in the previous section. Figure 2-14 shows the simulation results for a constant power load stepping from 5 kW to 10 kW. The results indicate that the system is stable with the designed passive parameters.

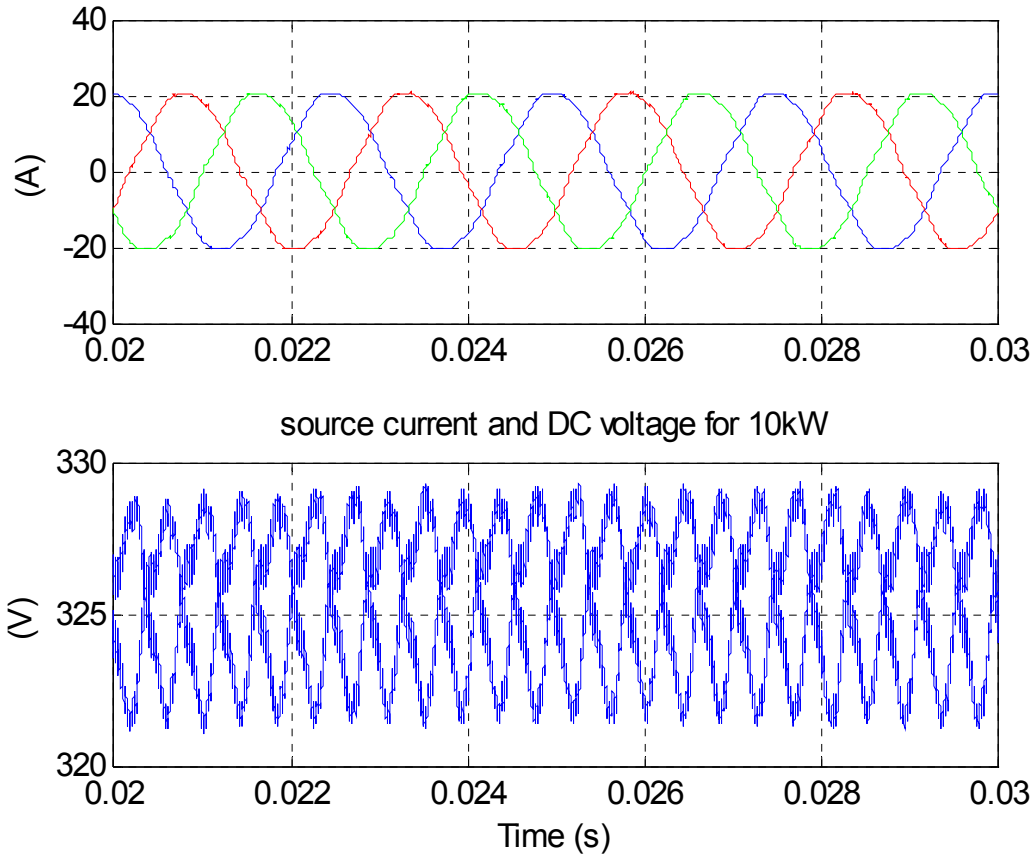


Figure 2-15 Steady state simulation waveforms (The top traces are the input currents, the bottom traces are the capacitor voltages.)

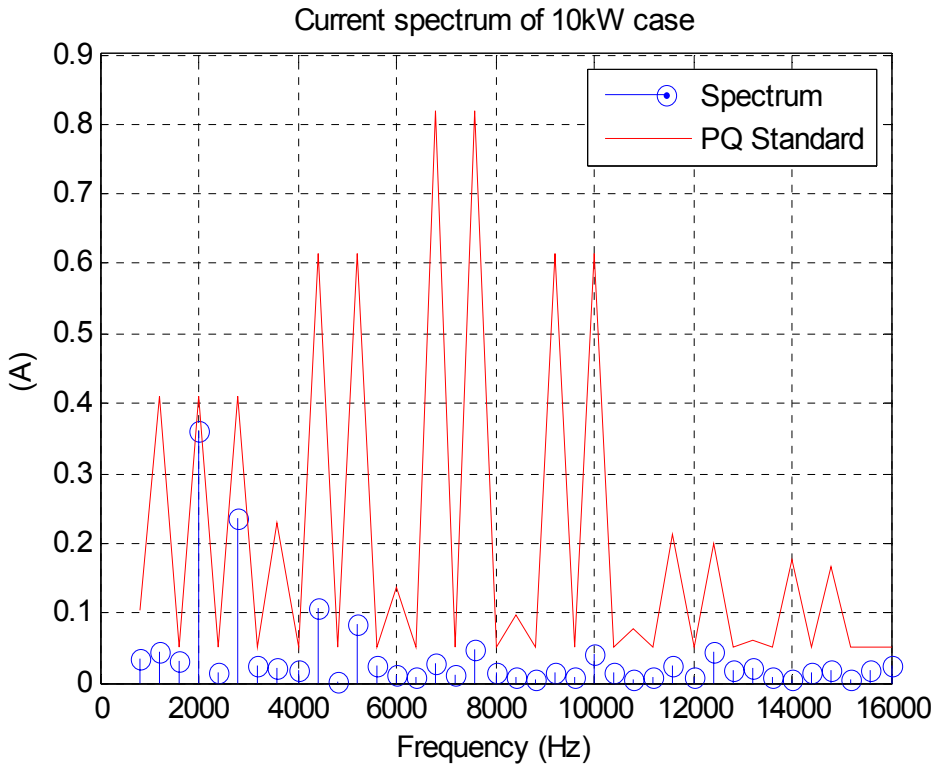


Figure 2-16 Harmonic current spectrum

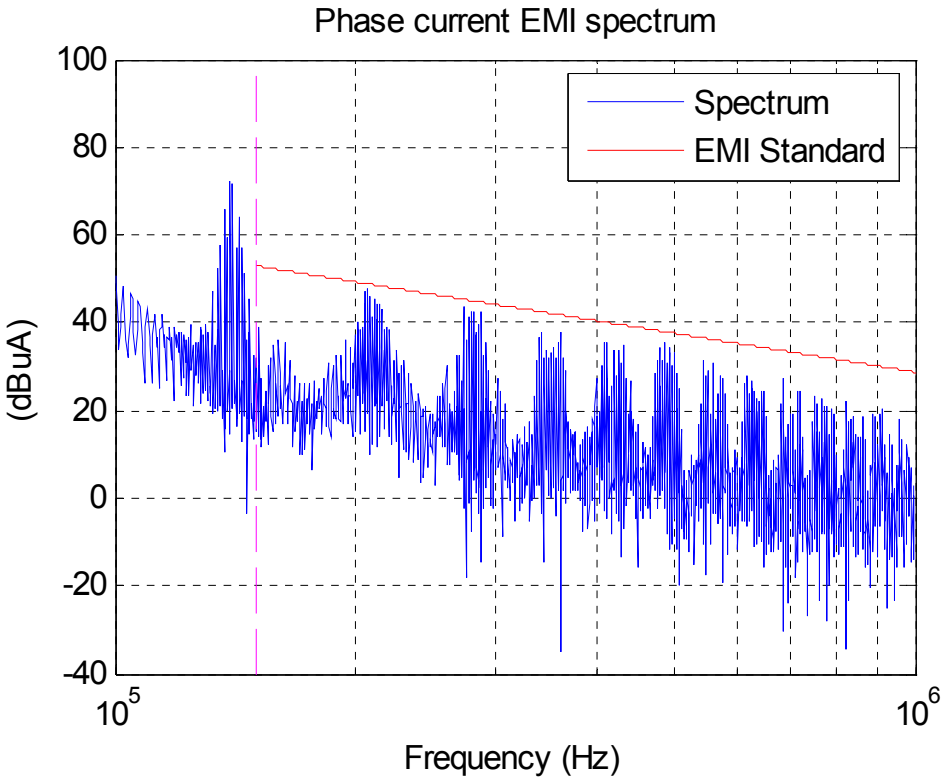


Figure 2-17 EMI spectrum

The full power steady state waveform is shown in Figure 2-15. The harmonic spectrum analysis results of the input current as well as the power quality standard are shown in Figure 2-16. The EMI spectrum analysis results and the standard requirement are shown in Figure 2-17. The simulation results show that the converter designed parameters meet the standard.

2.3 Summary

The design considerations and procedures to minimize the passive components of the back-to-back VSC converter system are discussed and developed in this chapter. The impact of the switching frequency on the filter corner frequency is studied by the spectrum analysis. It shows that the relationship is non-monotonous. Higher switching frequency will not necessarily lead to smaller EMI filter. Some preferred operating points are determined. Then the lower bound for the line inductance is derived with the current ripple requirement under a given switching frequency. The concept of using the same inductor for boost function and EMI suppression is introduced in the design. Energy storage and impedance interaction requirement are set up to determine the minimum DC link capacitor. The current stress on the DC link cap and the failure mode impact are also discussed. With the principles developed in this chapter, component parameters and switching frequency selection can be traded off in order to achieve minimum passives. The design approach is verified by simulation.

Chapter 3 Topology Evaluation

This chapter presents a methodology to evaluate the three-phase ac topologies with the metric of minimum weight [48]. The approach for passive filter selection developed in Chapter 2 is applied when comparing different topologies. All major components and subsystems in a converter are considered and the interdependence of all the constraints and design parameters is systematically studied. The key design parameters, including switching frequency, modulation scheme, and passive values, are selected considering their impacts on loss, harmonics, electromagnetic interference (EMI), control dynamics and stability, and protection. In this chapter four popular topologies are compared with the proposed methodology.

3.1 Introduction

The power stage design clearly depends on the converter circuit topology. Therefore to achieve a high-density design, it is a logical and necessary step to carry out the systematic design and evaluation for the topologies that meet the application requirements, and select among them the most suitable candidate.

For three-phase ac-ac converters, such as industrial motor drives, the two-level PWM voltage source inverters with 6-pulse diode front-end rectifier has become the topology of choice, due to its simplicity and relatively low cost. One drawback of the diode front-end topology is the low order, low frequency harmonics on the dc link and ac input line, which consequently requires bulky dc-link capacitor and inductor (ac or dc) filters. In order to improve converter performance and achieve higher power density, many

topologies for three-phase ac-ac converters or motor drives with active front-end rectifiers have been proposed and studied [49-57]. These topologies can generally operate with reduced passive components and improved input current wave form. On the other hand, they may have increased loss and electromagnetic interference (EMI) noise, requiring additional cooling and filtering [38]. Different active front-end topologies have different loss, harmonics, and EMI characteristics, which often have contradictory impact on the size and performance of the converter. To achieve a high power density design for a specific application, comprehensive analysis and evaluation are needed to obtain an optimal converter topology selection.

There has been considerable work on ac converter topologies evaluation. The previous work generally focused on specific aspects of the converter design. For instance, [58] compared the steady-state current and voltage waveforms as well as the harmonics injected to the grid for two inverter topologies; [16] discussed device losses, input filter and cost for three-level voltage source converters; [13] [14] [59] evaluated different converter systems in terms of the grid-side power quality and loss distribution; [15] compared the efficiency of the current source and the voltage source drive systems. However, when developing a new converter for high-density applications, all aspects contributing to the converter size and weight must be examined in the design, which requires the correlation between all major design parameters be clearly established. There is a clear need then for a systematic evaluation methodology considering the strong interdependence of all design variables and constraints. For example, increasing switching frequency generally helps to reduce the passive size, but it also increases the converter switching loss and therefore heatsink size. As will be shown later in the chapter,

even the relationship between the filter size and switching frequency is not monotonous, as a result of changing loss characteristics and attenuation requirements of harmonic and EMI standards. Generally speaking, operation conditions and constraints have great influence on the component and converter size and weight. The constraints can be physical ones as well as performance and system related. The examples of physical constraints are: maximum junction temperature for devices, acceptable temperature rise for magnetic and dielectric components, and voltage and current stress limits; the examples of performance and system related constraints include: power ratings, power quality and EMI requirements, etc. The auxiliary circuits, such as inrush current control, protection and sensors, can also impact converter size and vary for different topologies, and therefore should be considered in the topology evaluation as well. Finally the selection of semiconductor devices, components, materials, and packaging also affect the topology choice.

This chapter presents a systematic evaluation methodology of ac-ac converter topologies for high density applications with emphasis on topologies with active front-end rectifiers. The evaluation approach and selection criteria are first developed and described in section 3.2. The evaluation examines all aspects of the design that contribute to the size and weight of the converter, including: control, switching frequency, semiconductor device loss and cooling, harmonic and EMI filters, and component design and selection. The conclusions developed in chapter 2, including the parameters selection criteria and switching frequency impact, are utilized in the evaluation. Following the evaluation approach, a comparison study is carried out for four exemplary active front-end topologies: back-to-back voltage source converters (BTB-VSC) [49], non-

regenerative three-level boost (or Vienna-type) rectifier plus voltage source inverter (NTR-VSI) [50-52], back-to-back current source converters (BTB-CSC) [53-54], and 12-switch matrix converter [55-57]. Not only are these four well-known topologies for three-phase ac-ac converters, but they also represent a broad category of implementations (two-level, three-level, voltage-source, current-source, matrix, etc.). For each topology, a least-weight design is sought under the same design conditions. The state-of-the-art SiC devices are assumed in this study.

A main objective of this chapter is to provide a useful tool for practicing engineers for selecting a high density topology for a given application. While the methodology applies to both size and weight, the focus will be on the lowest weight design in the comparison study, owing to the complexity involving system layout in determining the volume of a converter.

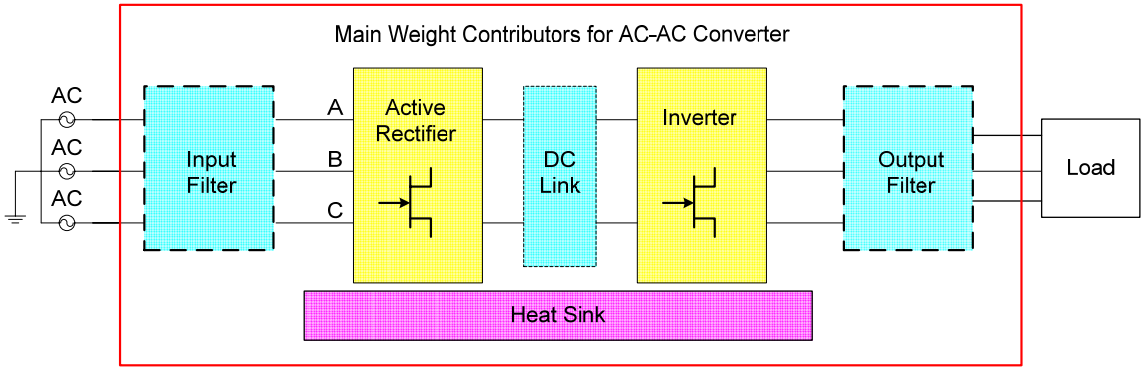


Figure 3-1 Key components for an ac-ac converter

3.2 Evaluation Approach

Figure 3-1 shows a generic three-phase ac-ac converter diagram with active front-end. All key size and weight contributors are shown, including input filter, dc link (filter and auxiliary circuits), output filter, switching devices and heatsink, and need to be

considered in the high-density design. It should be noted that not all of these elements are needed for all topologies, or for all applications. The basic evaluation and comparison approach is formulated similarly to a design optimization problem [60]. Design conditions and constraints are first identified, including: performance constraints, such as power quality and EMI standards; physical conditions and constraints, such as ambient temperature, maximum device junction temperature and passive component thermal and electrical limits. With a given design objective (in this case, size or weight), key design parameters can then be varied and determined, including: switching frequency, control/modulation strategy, minimum L and C values for both energy storage and filter passives, device losses and cooling system thermal impedances.

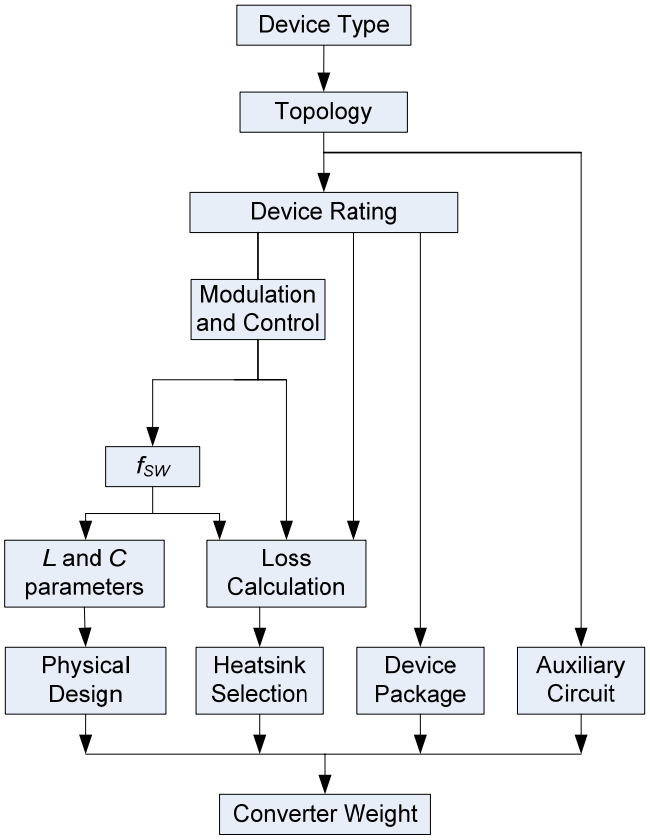


Figure 3-2 Topology evaluation procedure

The flowchart in Figure 3-2 shows the evaluation procedure for a low weight topology selection: (1) First, the type of devices are specified, whether it is IGBT, MOSFET, GTO, or SiC switches; (2) For a candidate topology, the semiconductor devices with proper datasheet rating are preliminarily selected according to the operation conditions, such as operating voltage and current; (3) Select the control and modulation scheme, which impacts passive and thermal design; (4) Choose a preferred switching frequency within a feasible range that is determined by the device characteristics. The "preferred" switching frequency concept will be explained later in this section; (5) With chosen modulation and switching frequency, the harmonic and EMI noise spectrum can be determined as functions of passive components, based on which minimum L and C parameters are designed to meet the system standards. In parallel, the device loss can be determined; (6) Carry out physical design and selection for inductors and capacitors for the least weight, and carry out thermal analysis and design for heatsink with given temperature conditions and the thermal impedances; (7) Evaluate the total weight of the converter, including the passives, heatsink, semiconductor devices, and the auxiliary circuit. Note that iterations should be expected in the design process, such as selection of a different modulator, varying the switching frequency, and adjustment of device rating selection as a result of thermal design. For clarity, the iteration processes are omitted in Figure 3-2 flowchart. All candidate topologies can be evaluated and compared with the same procedure. Some of the key steps of the evaluation approach are described in details in this section below.

A. Modulation Scheme

Ac active converters are PWM controlled. Modulation schemes affect switching loss, as well as voltage and current ripple spectrum, therefore the filter design. Modulation

schemes are topology dependent. In general, there are no clear "optimal" modulators since some are better for loss, while others may be better for ripple, or for dynamics. Selection of the modulator is a key design choice. At least, two types of modulation schemes should be evaluated in high-density design, the continuous PWM scheme, which usually generates lower ripple, and the discontinuous PWM, which results in lower loss. For some topologies, the modulator has extra functions, which have to be considered, e.g., the modulator of a multi-level converter often performs dc-link neutral-point control.

B. Preferred Switching Frequency

Switching frequency is a key design parameter. In general, increasing switching frequency is an effective way to reduce passive components and increase power density, until the increased loss in switching devices and in passive components outweighs the benefit of the increased frequency. Therefore, for a specific application, there can be an "optimal" switching frequency, which depends on the system, modulator, and components. In principle, the switching frequency selection could involve search for the optimal frequency. The conclusions from Chapter 2 can be utilized.

C. Loss Calculation and Heatsink Design

With selected modulation scheme and switching frequency, the power stage design can be carried out, particularly, design of the major weight/size contributors of heatsink and passives. The key to the heatsink design is power semiconductor device losses, which are highly dependent on the device characteristics. There are many device characterization methods. For topology evaluation study, it is appropriate to use a linear approximation device model in (3-1) to (3-4) for the loss calculation. The conduction voltage drop of the devices is given by (3-1) and (3-2), where V_{fT} and R_{on} are the

threshold forward voltage and the on-resistance of the switching device, V_{fD} and R_D are the forward voltage and the on-resistance of the diode, v_T , i_T and v_D , i_D are the voltages and currents of switch and diode respectively. The switching loss energy $e_{T\_on(off)}$ and e_{D_rev} for switch and diode at operating point *v(t)* and *i(t)* can be modeled in (3-3) and (3-4), where $e_{T\_on(off)\_r}$ and $e_{D\_rev\_r}$ are the switching energy and the reverse-recovery energy at the measured operating point v_r and i_r, which can be obtained from either the datasheet or experiments. Note that the device parameters V_{fT}, R_{on}, V_{fD}, R_D, $e_{on(off)\_r}$ and e_{rev_r} are all significant functions of junction temperature. For the evaluation, the appropriate temperature should be assumed, usually corresponding to the peak junction temperature.

On-state voltage drop of switch: $v_T = V_{fT} + R_{on} \cdot i_T$ (3-1)

On-state voltage drop of diode: $v_D = V_{fD} + R_D \cdot i_D$ (3-2)

Switching energy of switch: $e_{T\_on(off)} = e_{T\_on(off)\_r} \cdot \frac{v(t) \cdot i(t)}{v_r \cdot i_r}$ (3-3)

Switching energy of diode: $e_{D\_rev} = e_{D\_rev\_r} \cdot \frac{v(t) \cdot i(t)}{v_r \cdot i_r}$ (3-4)

Given the semiconductor devices and operating conditions, the power loss for any given topology and modulation scheme can be found with (3-1) to (3-6). Examples of loss calculations will be given for selected topologies and devices in Section III.

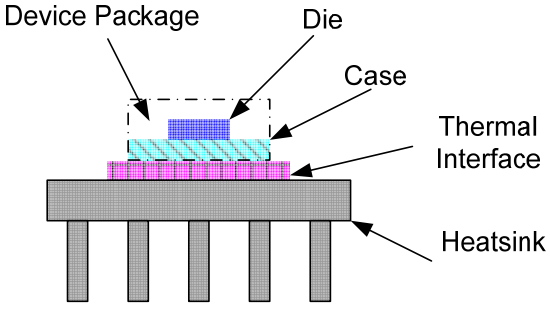


Figure 3-3 Device thermal structure illustration

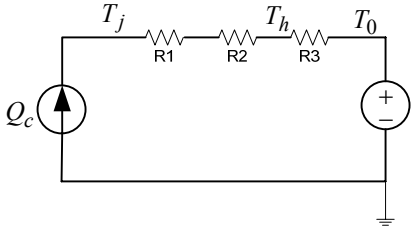


Figure 3-4 Thermal equivalent model

Knowing the loss, the thermal calculation can be performed. For topology evaluation, one dimensional equivalent thermal model, consisting of equivalent thermal impedances of device package, heatsink, and other thermal interface materials, should be sufficient. Figure 3-3 shows an example of the thermal interface structure and Figure 3-4 shows the corresponding one dimensional steady-state thermal equivalent circuit, where Q_c is the power loss generated by the device, R_1 is the thermal resistance from junction to case, R_2 represents the thermal resistance of thermal interface between the case and the heatsink, R_3 is the thermal resistance of the heatsink to the ambient. T_j, T_h, and T_0 are temperatures of the semiconductor device junction, heatsink and ambient respectively. The thermal resistances can be obtained from datasheet, measurements, or simulation. If there is transient overload, thermal capacitances should also be considered. In the case without transient overload, the junction temperature of the *k*-th device can be obtained as in (3-5), where T_{j_k} and Q_{c_k} correspond to the junction temperature and power losses for the *k*-th device, T_{limit} is the upper limit for the operating junction temperature for that device (e.g. 125°C for many commercial Si devices).

$$T_{j\_k} = Q_{c\_k} \cdot (R_1 + R_2) + T_h \le T_{\lim it} \tag{3-5}$$

With (3-5), the acceptable upper limit of the heatsink temperature corresponding to that particular device may be readily found. For an ac converter with multiple devices, this value could vary with device and the lowest one should be chosen as the upper temperature limit for the whole heatsink. Then the required thermal resistance for the heatsink is given in (3-6). With a given ambient temperature and cooling method/conditions, heatsink can be selected or designed to meet the requirement of (3-6) and the corresponding size and weight of the cooling system can be determined.

$$R_3 = (T_h - T_0)/Q_c \tag{3-6}$$

D. Passive Component Parameter Minimization and Physical Design

Depending on topologies, the passives in an ac-ac converter can include dc-link capacitor and/or dc-link inductor, ac input line inductor or capacitor, as well as input and/or output filter for suppressing harmonics, EMI, and dv/dt. The output filters are generally application dependent and will not be considered in this work. The approach used here should be applicable to output filters for specific applications.

Energy storage capacitance and inductance minimization: For energy storage passives, i.e., dc-link and ac-line capacitors and inductors, minimum parameters should first be determined according to a number of performance and system requirements. The parameter selection is topology dependent. In general, for the dc-link capacitor (for voltage source topology) or inductor (for current source topology), their selection needs to consider the following requirements:

1) Energy storage: The dc-link voltage variation (for voltage source topology) or current variation (for current source topology) caused by the instantaneous energy unbalance should be limited to an acceptable level. The energy unbalance can be caused by a sudden change in load or source conditions.
2) Stability: Impedance characteristics of the dc link determine the stability of the converter system [46].

For boost inductor (for boost topology) and capacitor (for buck topology), their selection need to consider:

1) Harmonics: often in terms of total harmonic distortion (THD).

2) Peak ripple current: The peak ripple current as results of switching will impact the inductor flux, and therefore the inductor sizes.

3) Inrush: High current peaks will occur in voltage source topologies during start up or recovery from a voltage drop, which will impact both the inductor design and the capacitor selection.

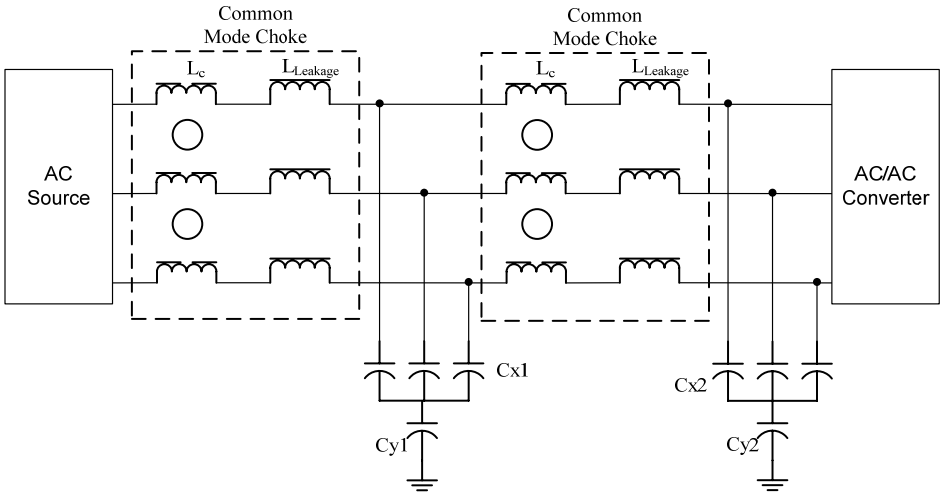


Figure 3-5 CL-CL filter for CSC

Filter Passive Minimization: The ac input filters should also be designed to meet EMI standards requirements. For comparison discussion, this section uses a two-stage LC-LC filter for voltage source topologies, as shown in Figure 2-7, and a CL-CL filter for current source topologies, as shown in Figure 3-5. The design objective is to minimize the *L* and *C* values while complying with the EMI standard. The design approach was discussed in Chapter 2. While damping design for high frequency resonance is an integral part of filter design, it is omitted here since damping components contribute little to weight and size and they can be common for all topologies. Both passive [20] and active [61] [62] damping schemes can be used. Note that the EMI filter passives and energy storage passives can be combined or integrated in the design for further reduction of size and

weight, which means that the input filter can be designed as one entity to achieve harmonic and EMI filtering functions as well as for energy storage. Examples of such design will be shown in Section 3.3.

Capacitor Design and Selection: In most practical converter designs, the capacitors are selected based on available commercial parts. For high density and light weight design, the smallest and lightest capacitors should be selected that also meet the capacitance, voltage, current, and thermal requirements. Commercial film capacitors are selected in this work for comparison purposes. The section examples are demonstrated in Section 3.3.

Inductor Design: Toroid cores are assumed for the CM choke, and EE cores for the ac-line and dc-link inductors. The design constraints are: required inductance and physical limits such as saturation, window area, insulation and maximum temperature rise [63]. The leakage inductance of the CM choke [64] is also considered as a design constraint in order to achieve the required DM attenuation. In this work ferrite (R material) from Magnetics are used for the ac-line and dc-link inductor design, and nanocrystalline (FT-3M) material for the CM choke design. The core losses under sinusoidal excitation are given by (3-7) [65] and (3-8) [66], where the core loss is in W, f is the frequency in kHz, dB is the peak flux density change in $kGauss$, and V_{core} is the core volume in cm^3. Based on (3-7) and (3-8) the improved Generalized Steinmetz Equation [67] can be used to calculate the core loss of the inductors.

Loss of ferrite (R material): $P_{core} = 7.4 \times 10^{-5} \cdot f^{1.43} \cdot dB^{2.85} \cdot V_{core}$ (3-7)

Loss of nanocrystalline (FT-3M material): $P_{core} = 8.34 \times 10^{-5} \cdot f^{1.621} \cdot dB^{1.982} \cdot V_{core}$ (3-8)

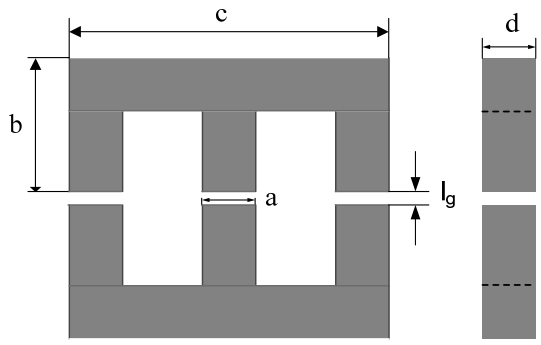


Figure 3-6 Design variables for the EE core

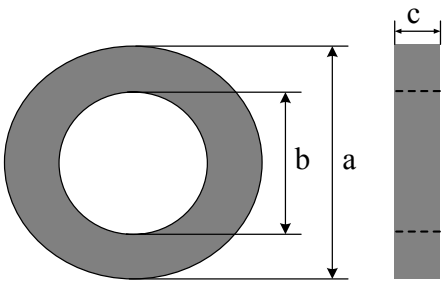


Figure 3-7 Design variables for the toroid core

An optimization function (FMINCON) in Matlab is used to determine the physical dimensions to achieve minimum weight. The design variables are the core dimensions (as shown in Figure 3-6 and Figure 3-7), air gap and the number of turns. All the designed constraints mentioned above are considered and the total weight is the objective function for both inductors. Based on this algorithm the optimal inductor design and the corresponding weight can be obtained under the given operating conditions and the designed inductance value.

E. Auxiliary Circuits, Design Variation and Iteration

In addition to cooling and passive components, the other relatively important topology-dependent weight contributors include power device packages and auxiliary circuits, such as inrush control and protection circuits. Together, the total weight of the converter can be determined and compared with the result of a different design or topology.

Clearly, for each given topology, there can be different designs with different converter weights, while all meeting the performance requirements and design constraints. In principle, every key parameter can have its design range. In practice, design variation and iteration should be performed to achieve the least weight design. For example, there

are several preferred switching frequencies observed in Figure 2-6, and the most suitable one needs to be selected through design iteration. The device rating selection should be traded off with losses, thermal impedance, and heatsink. The design variation can be systematically carried out following the flowchart process in Figure 3-2 and even automated with computer programming or optimization.

3.3 Topology Comparison

Based on the proposed approach, four three-phase ac-ac active front-end topologies as shown in Figure 3-8 are evaluated and compared. While these candidate topologies cover a range of circuits often used in high-density converter design and study, their selection is not meant to be exhaustive and is intended only to demonstrate the effectiveness of the evaluation procedure, which should also be applicable to other topologies. Table 3-1 lists the sample system specifications and requirements used in this comparison study. SiC devices are selected in the comparison since they offer the advantages of low loss, high switching frequency and high operating temperature [68]. The commercial SiC diode C2D20120 (1200V/20A) and a 1200V/5A JFET from SiCED are selected in this study. The diode parameters are available from datasheet. At 175°C, the JFET has an on-resistance of 0.8 Ω and a switching energy of 155 μJ (at 400V/10A) [69]. The number of paralleling devices required varies with the topologies according to the current and thermal requirement. For comparison purpose, all candidate topologies keep the same total number of devices (a total of 72 devices including the diodes and JFETs).

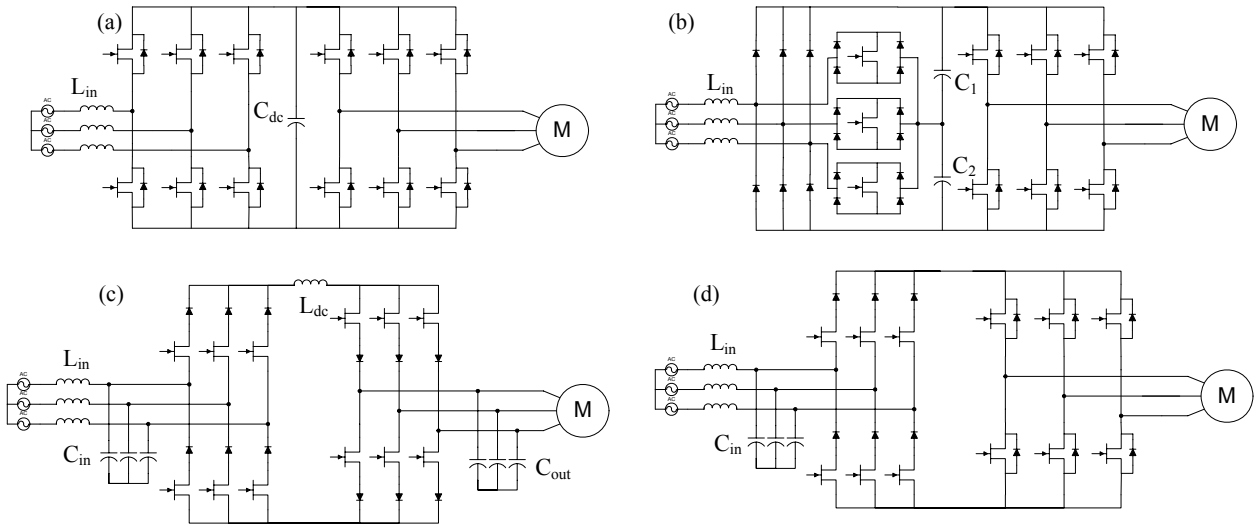


Figure 3-8 (a) Back-to-back VSC, (b) Non-generative three-level boost rectifier plus voltage source inverter, (c) Back-to-back CSC and (d) 12-switch matrix converter

As explained in Section 3.2, switching frequency is a key design parameter. There are preferred switching frequencies for the front-end rectifier based on input EMI filter requirements. In principle, for the inverter, the switching frequency can be separately selected based on output filter requirement and the load specs. Since the output filter is very application dependent and therefore omitted in this work, the inverter switching frequency is chosen to be the same as the rectifier for comparison purpose. In the comparison study, four switching frequencies are used, 40 kHz, 70 kHz, 100 kHz, and 140 kHz, and the corresponding designs are obtained and compared. From Figure 2-6, it can be seen that f_{sw}<40 kHz can result in higher corner frequency for EMI filter. The low switching frequency boundary is selected to be 40 kHz to avoid relatively low-order harmonics, given the 400-800 Hz fundamental frequency range. For a different design spec, a lower or higher switching frequency range may be selected.

Table 3-1 System Specifications

Input Voltage	230 Vrms	Dc-link Voltage (for VSC)	650 V
Power	10 kW	Dc-link Current (for CSC)	25 A
Devices	1200V SiC JFET, SiC Schottky Diode		
Line Frequency	400-800 Hz	Junction Temperature	175°C
Ambient Temp.	70°C	Air Flow	2 m/s
Standard Requirement	RTCA/DO-160E		

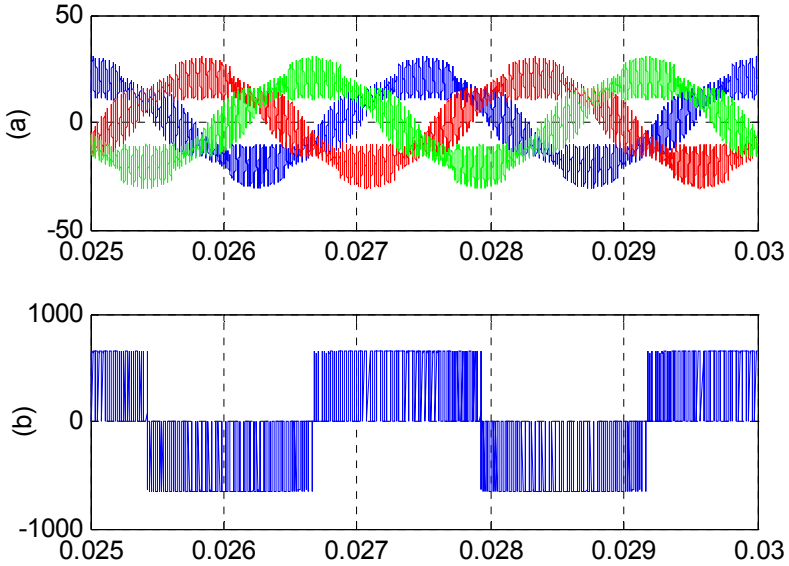


Figure 3-9 Simulation results for BTB-VSC: (a) ac-line currents; (b) PWM line-to-line voltage

A. BTB-VSC

BTB-VSC, as shown in Figure 3-8 (a), is a popular topology in many applications. 60° DPWM is implemented in this work for better EMI noise performance and lower semiconductor loss compared to continuous PWM [42]. In Figure 3-9 the simulation waveforms of ac-line currents and PWM line-to-line voltage are shown (Circuit parameters: L_{in} = 100 μH, C_{dc}=10 μF, f_{SW}=40 kHz).

Based on the conclusions in Chapter 2, we can determine the required passive filter parameters. For comparison purpose, the capacitor C_x and C_y are selected to be 1 μF and 6.8 nF respectively for all the topologies and then the inductances vary to meet the corner frequency. For the 40 kHz case, the common mode and differential mode inductances are 10 mH and 110 μH respectively. Since the ac-line inductor can also be a part of the EMI filter. So the total input inductance should be the larger one between the two values designed for the DM inductor and the line inductor respectively. In this case the EMI filter DM inductance is dominant, which can be the leakage inductance of the CM choke. Based on the designed parameters and operating conditions, the optimization algorithm shown in the previous section is used to design the actual inductor (physical unit). The dc-link capacitance is selected to be 10 μF for 40 kHz switching frequency. Four 400 V / 10 μF film capacitors are chosen in the design to form the equivalent 10 μF dc-link capacitor bank to meet the voltage and the ripple current requirement.

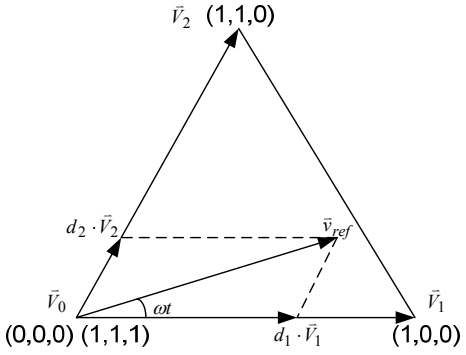


Figure 3-10 Vector synthesis in sector I of space vector diagram

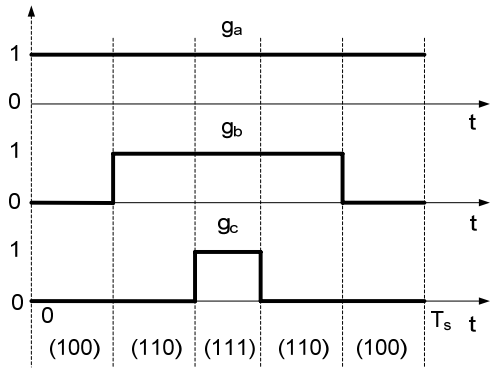


Figure 3-11 Pulse pattern for the top switches in the first 30°

Cooling System: For loss calculation in topology evaluation, the dc-link voltage ripple and ac input/output current harmonics can be neglected. Under the assumption, the current through each device is only determined by the switching pattern and the duty

cycle. With the three-phase symmetrical system, for the loss calculation, we can just consider the losses in one sixth of the line cycle. Figure 3-10 shows the voltage vector synthesis in sector I of the space vector diagram [42]. The duty cycles d_1, d_2, and d_0 for voltage vectors $\vec{V}_1$, $\vec{V}_2$ and $\vec{V}_0$ are given by (3-9). Figure 3-11 shows the pulse patterns of the top switches for the first 30° in sector I. With (3-9) the duty cycles for phase-legs are given by (3-10).

$$\begin{cases} d_1 = \dfrac{\sqrt{3}}{2} M \sin(\dfrac{\pi}{3} - \omega t) \\ d_2 = \dfrac{\sqrt{3}}{2} M \sin \omega t \\ d_0 = 1 - d_1 - d_2 \end{cases} \tag{3-9}$$

$$\begin{cases} d_a = 1 \\ d_b = d_2 + d_0 = 1 - \dfrac{\sqrt{3}}{2} M \cdot \cos(\omega t + \dfrac{\pi}{6}) \\ d_c = d_0 = 1 - \dfrac{\sqrt{3}}{2} M \cdot \cos(\omega t - \dfrac{\pi}{6}) \end{cases} \tag{3-10}$$

The switching loss of SiC diodes is ignored as they have excellent reverse recovery performance [70]. With the linear assumption the power losses of the SiC JFET and diode in the phase-leg of the rectifier at the *j*-th switching cycle are given by (3-11) and (17), where $I_r(t)$ is the instantaneous rectifier input current, $d_r(t)$ is the instantaneous duty cycle of the corresponding phase-leg of the rectifier given by (3-10), V_{dc} is the dc-link voltage, N_{r_T} and N_{r_D} are the numbers of parallel JFETs and diodes in the rectifier respectively. N_{r_T}=4 and N_{r_D}=2 for the BTB-VSC.

$$P_{r\_JFET\_j} = (1 - d_r(t)) \cdot \frac{R_{on}}{N_{r\_T}} \cdot I_r(t)^2 + e_{T\_on(off)\_r} \cdot \frac{V_{dc} \cdot I_r(t)}{v_r \cdot i_r} \cdot f_{sw} \tag{3-11}$$

$$P_{r\_Dio\_j} = d_r(t) \cdot [V_{fD} \cdot I_r(t) + \frac{R_D}{N_{r\_D}} \cdot I_r(t)^2] \tag{3-12}$$

The power losses in the inverter are given by (3-13) and (3-14), where $I_i(t)$ is the instantaneous inverter output current, $d_i(t)$ is the instantaneous duty cycle of the corresponding phase-leg of the inverter, N_{i_T} and N_{i_D} are the numbers of parallel JFETs and diodes an inverter phase-leg respectively. N_{i_T}=5 and N_{i_D}=1 in this case.

$$P_{i\_JFET\_j} = d_i(t) \cdot \frac{R_{on}}{N_{i\_T}} \cdot I_i(t)^2 + e_{T\_on(off)\_r} \cdot \frac{V_{dc} \cdot I_i(t)}{v_r \cdot i_r} \cdot f_{sw} \tag{3-13}$$

$$P_{i\_Dio\_j} = (1 - d_i(t)) \cdot [V_{fD} \cdot I_i(t) + \frac{R_D}{N_{i\_D}} \cdot I_i(t)^2] \tag{3-14}$$

Assume sinusoidal $I_r(t)$ and $I_i(t)$, equations (3-11) to (3-14) are used to calculate the average losses of the semiconductor devices on the phase-leg. The same procedure is used to obtain the losses of the other phase-legs and the sum of the phase-leg losses yields the total converter loss. And then with (3-5) and (3-6) the required thermal impedance for the heatsink can be determined. The aluminum heatsink OS080 from Aavid Thermalloy is selected in this work. The width and the height are 135 mm and 25 mm respectively. The length of the heatsink varies with the required thermal resistance. Two fans (614F series from ebm-papst Inc.) are assumed for all the topologies. The weights of the inductors are calculated by the designed core dimensions and the number of winding turns with the material density. The weights of the other components are obtained from the data sheet. The loss calculation results and the weight distribution for the BTB-VSC are shown in Table 3-2.

B. NTR-VSI

The topology is shown in Figure 3-8 (b). In comparison to the BTB-VSC, the two-level active front-end is replaced in this case by a non-regenerative three-level boost rectifier, which offers the advantages of lower voltage stress to the devices and lower

harmonic distortion. But it does not provide the regenerative capability. Three-level continuous space vector PWM is used for the rectifier [71] and DPWM is implemented for the VSI as the BTB-VSC. Figure 3-12 shows the simulation waveforms (L_{in} = 100 μH, C_1=C_2=20 μF, f_{SW}=40 kHz). The spectrum analysis for the PWM voltage is shown in Figure 3-13 for 40 kHz switching frequency. Since the non-regenerative three-level rectifier is a voltage source rectifier, the input filter design and the dc-link capacitor selection can follow the same approach as the BTB-VSC. For the 40 kHz case, the common mode and differential mode inductances are 7.8 mH and 97 μH respectively. The dc-link capacitors are 20 μF each so that the total dc-link capacitance is 10 μF.

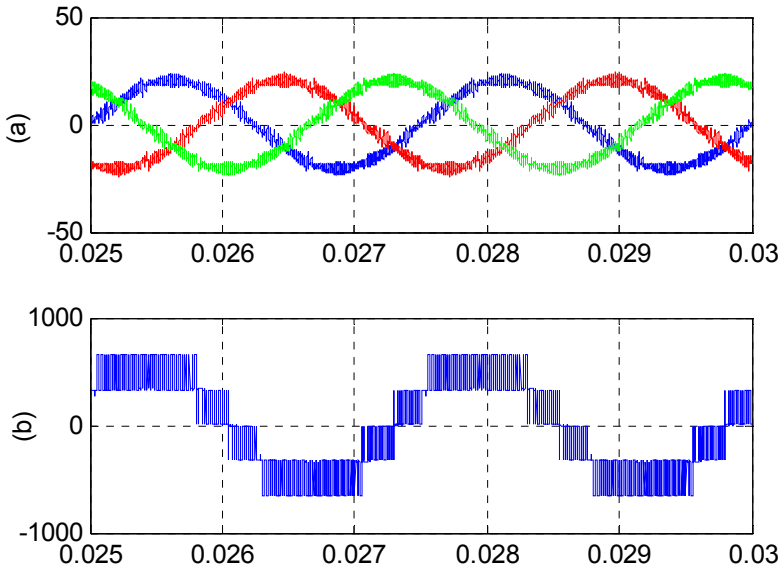


Figure 3-12 Simulation results for NTR-VSI: (a) ac-line currents; (b) PWM line-to-line voltage

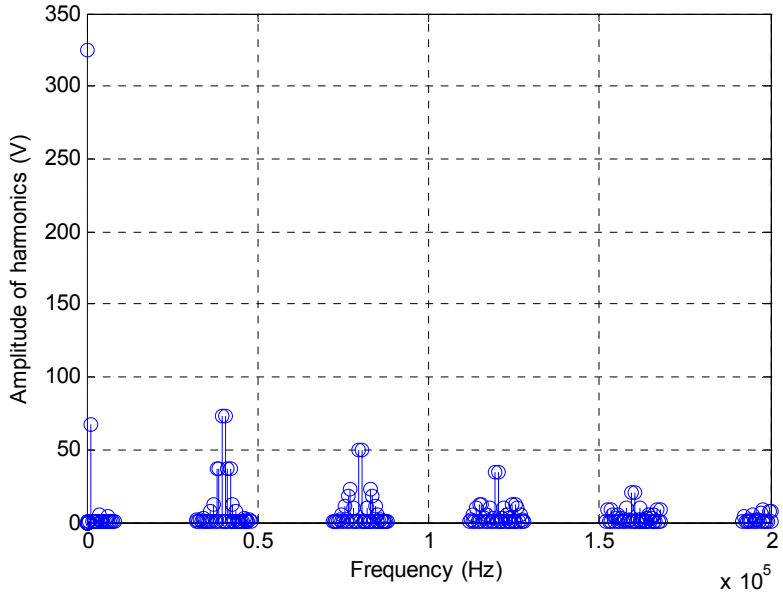


Figure 3-13 Spectrum of the PWM voltage for NTR-VSI

For the rectifier, the power losses of the JFET and the main bridge diode have the same expressions as (16) and (17) except that $0.5V_{dc}$ should be utilized instead of V_{dc} for the JFET switching energy calculation in (16). The loss of the neutral bridge diode is given by (20), where N_{r_Dn} is the number of parallel diodes in the neutral bridge. N_{r_T}, N_{r_D} and N_{r_Dn} are 4, 2 and 1 respectively in the design.

$$P_{r\_Dio\_neu\_j} = 2 \cdot (1 - d_r(t)) \cdot [V_{fD} \cdot I(t) + \frac{R_D}{N_{r\_Dn}} \cdot I_r(t)^2] \tag{3-15}$$

The VSI is modulated using DPWM and therefore its losses are determined by (3-13) and (3-14). Similar to the BTB-VSC the heatsink design is then carried out based on the loss calculation. Table 3-3 shows the design results for NTR-VSI.

C. BTB-CSC

Figure 3-8 (c) shows the topology of BTB-CSC. The energy storage component in the dc link is an inductor instead of a capacitor. Both input and output filters are required to

smooth the ripple current. The DPWM scheme is implemented in the design. Figure 3-14 and Figure 3-15 show the simulation results and pulse current spectrum for the case with 40 kHz switching frequency (Circuit Parameters: L_{in} =100 μH, C_{in}=1 μF, L_{dc} =1 mH, f_{SW}=40 kHz).

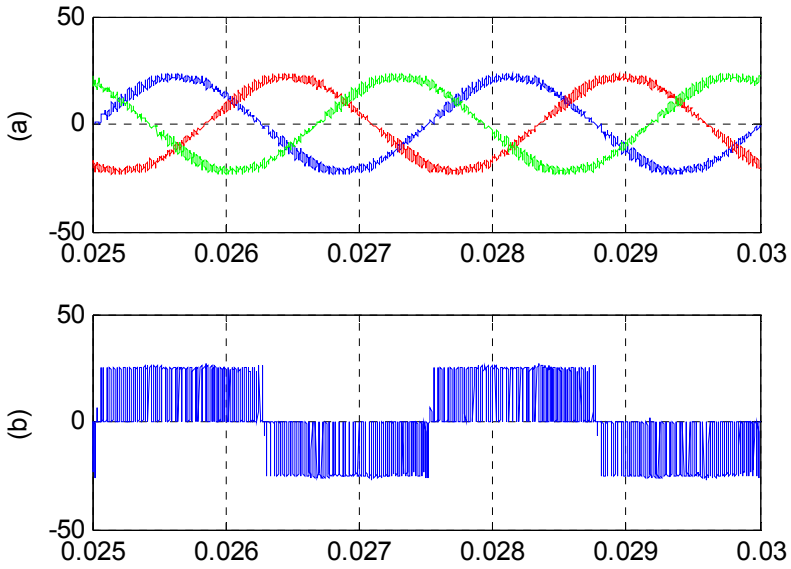


Figure 3-14 Simulation results for BTB-CSC: (a) ac-line source currents; (b) rectifier input current

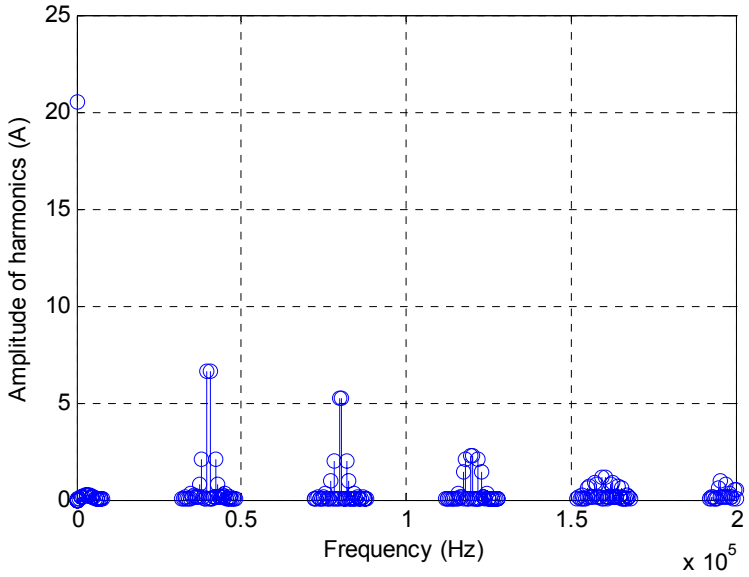


Figure 3-15 Spectrum of the PWM current for BTB-CSC

For the filter design, the same procedure as BTB-VSC is followed while the Fourier analysis is carried out for the pulsating current instead of the voltage at the rectifier input terminal. As mentioned in Section II, a CL-CL input filter is used for this topology. For the 40 kHz switching frequency case, the required inductance is 162 μH with 1 μF capacitance. This dc-link inductor should also meet the stability and energy storage requirements, expressed by (3-16) and (3-17), where I_{dc} is the dc-link current, and ΔI is the maximum ripple current (7 A in the example design).

$$L \geq \frac{P_{\max}}{f_{sw}(I_{dc}\Delta I \pm \frac{1}{2}\Delta I^2)} \tag{3-16}$$

$$20\lg(2\pi f_{BW} L) - 20\lg(\frac{P_{out}}{I_{dc}^{\ 2}}) \geq Z_m \tag{3-17}$$

With the above two equations the dc-link inductor is designed to be 1.27 mH for 40 kHz switching frequency case with 6 dB impedance margin and 4 kHz control bandwidth. In BTB-CSC the output capacitors are usually required to smooth the output waveform, especially for the motor load. In this work the voltage THD requirement is used to determine the output capacitance. Assuming all ripple components of the output current go through the output capacitors, the relationship between the output capacitance and the voltage THD can be achieved with the spectrum analysis result for the output current. For a 30% THD requirement, the capacitance is designed to be 1 μF when the switching frequency is 40 kHz.

For BTB-CSC the losses of the power devices have the same expressions for the rectifier and inverter, which are given by (3-18) and (3-19), where $d(t)$ is the instantaneous duty cycle, $V_L(t)$ is the instantaneous line-to-line voltage, N_T and N_D are the numbers of parallel JFETs and diodes respectively. N_T =5 and N_D =1 for this case. With

(3-18) and (3-19) the losses of each individual device and the total system can be achieved and then heatsink can be readily designed. The design results for the B2B-CSC are shown in Table 3-4.

$$P_{\_JFET\_j} = d(t) \cdot \frac{R_{on}}{N_T} \cdot {I_{dc}}^2 + e_{T\_on(off)\_r} \cdot \frac{V_L(t) \cdot I_{dc}}{v_r \cdot i_r} \cdot f_{sw} \tag{3-18}$$

$$P_{\_Dio\_j} = d(t) \cdot (V_{fD} \cdot I_{dc} + \frac{R_D}{N_D} \cdot {I_{dc}}^2) \tag{3-19}$$

D. 12-Switch Matrix Converter

The 12-switch matrix converter, as shown in Figure 3-8 (d), consists of a cascaded connection of two bridge converters without any dc-link energy storage components. The converter at the input terminal has the same structure as the front-end rectifier of the BTB-CSC, which is treated as the current source bridge (CSB); and the converter at the output terminal is treated as the voltage source bridge (VSB) since it has the same structure as the inverter of BTB-VSC.

A carrier based modulation scheme [72] is implemented and the corresponding noise spectrum is used for the filter parameters design. The simulation results and the spectrum analysis for the phase-leg pulsating current for 40 kHz switching frequency case are shown in Figure 3-16 and Figure 3-17 respectively (L_{in} = 100 μH, C_{in}= 4 μF, f_{SW}=40 kHz). Since the pulsating current is the noise source in the 12-switch matrix converter, the CL-CL structure is chosen for the input filter and the design follows the same way as the BTB-CSC. For the case of 40 kHz switching frequency, the inductance is 128 μH with the capacitance selected to be 1 μF.

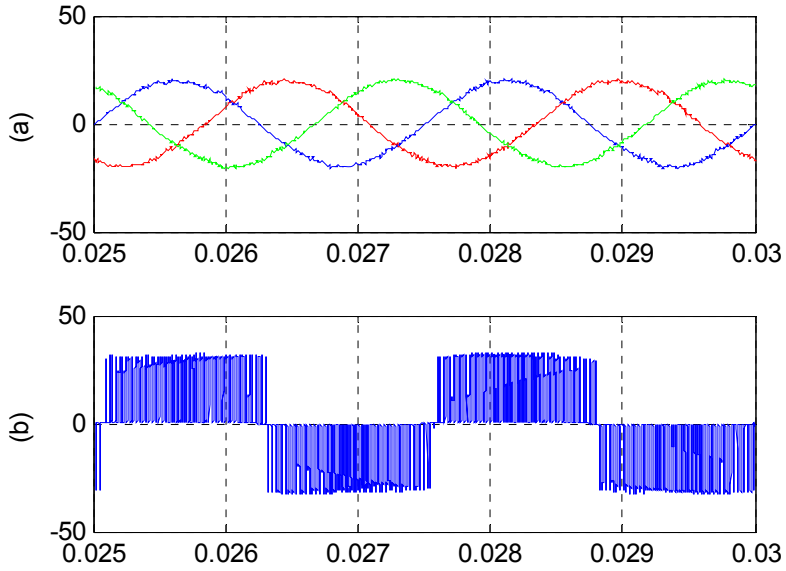


Figure 3-16 Simulation results for 12-switch matrix converter: (a) source currents; (b) PWM line current

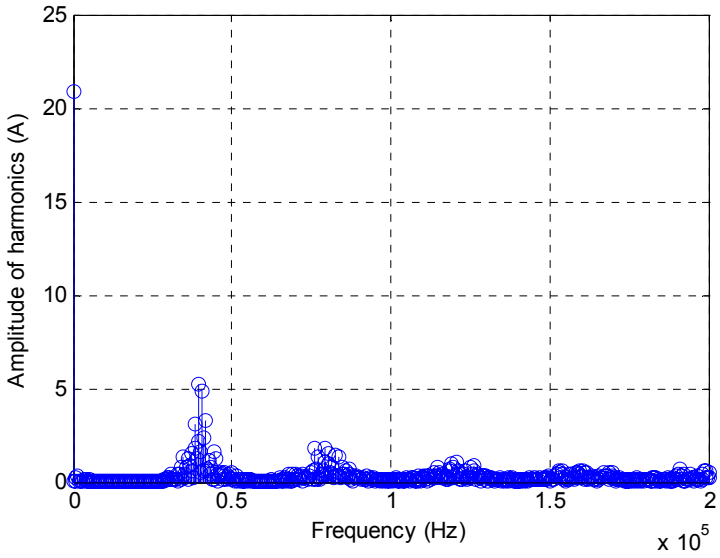


Figure 3-17 Spectrum of the PWM current for matrix converter

Losses are determined in the following way: for CSB, the switching loss is zero under the modulations scheme used, and the conduction losses are given in (3-20) [73], where I_0 is the amplitude of the output current, M_0 is the modulation index, and ϕ_0 is the output

power factor angle, which is assumed to be 0° for all the sample designs. The numbers of parallel JFETs N_{r_T} and diodes N_{r_D} in CSB are 5 and 1 respectively for the sample design.

$$P_{c\_CSB} = \frac{9}{2\pi} \cdot V_{fD} \cdot M_0 \cdot I_0 \cdot \cos(\phi_0) + \frac{3\sqrt{3}}{2\pi^2} \cdot (\frac{R_{on}}{N_{r\_T}} + \frac{R_D}{N_{r\_D}}) \cdot M_0 \cdot {I_0}^2 \cdot (1 + 4 \cdot \cos(\phi_0)^2) \tag{3-20}$$

For VSB, the conduction and switching losses are given in (3-21) and (3-22) by [73], where V_s is the amplitude of the input phase voltage and ϕ_i is the input power factor angle (0° for the sample designs). The numbers of JFETs N_{i_T} and diodes N_{i_D} in VSB are 5 and 1 respectively.

$$P_{c\_VSB} = 6\left[\begin{array}{l} \frac{V_{fD} \cdot I_0}{2\pi} + (\frac{R_{on}}{N_{i\_T}} + \frac{R_{fD}}{N_{i\_D}}) \cdot \frac{{I_0}^2}{8} - \\ \frac{3}{8\pi} \cdot V_{fD} \cdot I_0 \cdot M_0 \cdot \cos(\phi_0) + (\frac{R_{on}}{N_{i\_T}} - \frac{R_{fD}}{N_{i\_D}}) \cdot \frac{{I_0}^2}{\pi^2} \cdot M_0 \cdot \cos(\phi_0) \end{array}\right] \tag{3-21}$$

$$P_{sw\_VSB} = \frac{27}{\pi^2} \cdot f_{sw} \cdot e_{T\_on(off)\_r} \cdot \frac{V_s \cdot I_0}{v_r \cdot i_r} \cdot \cos(\phi_i) \tag{3-22}$$

With (25-27), the losses for the devices can be obtained and then the heatsink can be selected. Table 3-5 shows the design results for the 12-switch matrix converter.

E. Topology Comparison Results and Discussions

Figure 3-18 shows the total weight comparison of the four different topologies under consideration for four switching frequencies. From the results, it can be seen that the BTB-CSC has the highest losses and also the heaviest passive components. The NTR-VSI and the BTB-VSC present comparable weights, with the latter having slightly lower loss, but slightly larger filter. The 12-switch matrix converter requires the least passives but its higher loss makes it an inferior to the BTB-VSC and NTR-VSI topologies. It can also be seen that 40 kHz switching frequency is the best choice for all topologies due to the dominance of heatsink weight, except for BTB-CSC. It should be emphasized that

these conclusions are based on specific design conditions and component characteristics. For a different design, the same procedure can be applied and different conclusions on topology selections may arise.

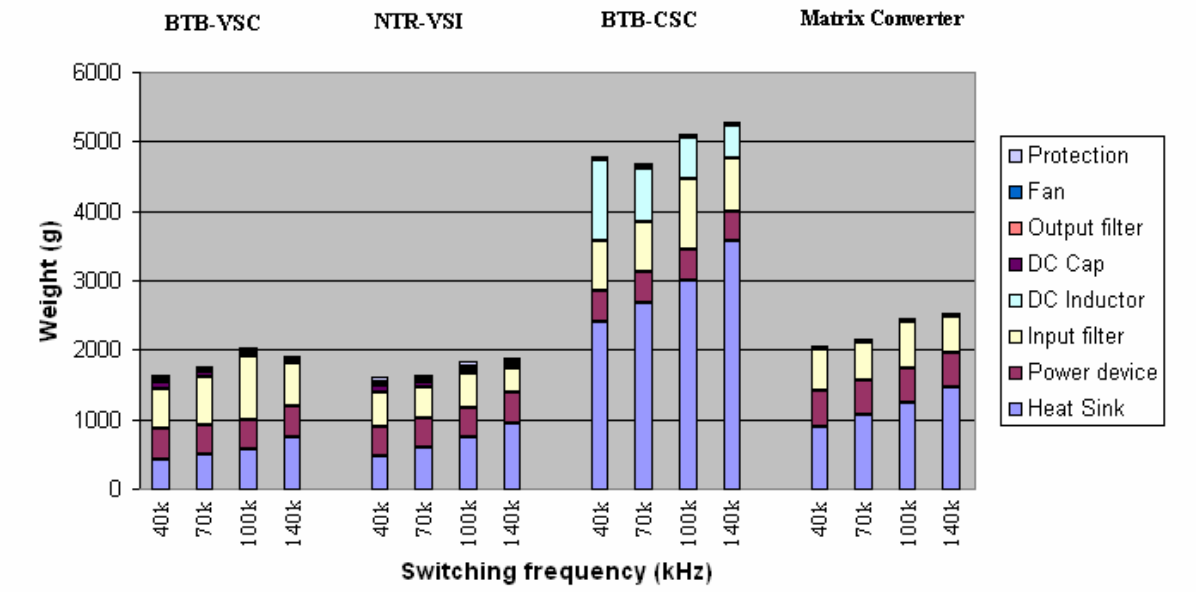


Figure 3-18 Weight comparison of four topologies under consideration

Table 3-2 Design Results for BTB-VSC

BTB-VSC	*f*=40k	*f*=70k	*f*=100k	*f*=140k
Loss (W)	206	238	268	309
Heatsink (g)	426	492	558	754
Power device (g)	432	432	432	432
Input filter (g)	576	676	912	614
DC Cap (g)	110	80	50	40
Fan (g)	50	50	50	50
Protection (g)	30	30	30	30
Total Weight (g)	**1624**	**1760**	**2032**	**1920**

Table 3-3 Design Results for NTR-VSI

NTR-VSI	*f*=40k	*f*=70k	*f*=100k	*f*=140k
Loss (W)	236	267	297	338
Heatsink (g)	459	590	738	951
Power device (g)	432	432	432	432
Input filter (g)	498	432	502	358
DC Cap (g)	110	80	50	40
Fan (g)	50	50	50	50
Protection (g)	60	60	60	60
Total Weight (g)	**1609**	**1644**	**1832**	**1891**

As mentioned above, auxiliary circuits such as inrush control and protection circuits also contribute to the converter weight and should be considered in topology evaluation. They are topology dependent. Among the four studied topologies, BTB-VSC and NTR-VSI require extra inrush control and dc-link over voltage protections [74]. Their estimated weights are included in Tables 3-2 and 3-3. Since the weights are relatively small, the detailed design descriptions are omitted here.

Note that in these Tables, the weights of the power devices are the same for all topologies with the comparison condition that all topologies use the same number of devices with the same packages. Because of the commercial package limitations for SiC devices, the device weights constitute an unusually high percentage in the converters. With better packaging, device weights should be significantly reduced. In this case, the device weight does not change the comparison results of the topologies as a common factor. The same cooling fan is also assumed in different designs due to its relatively small size.

Table 3-4 Design Results for BTB-CSC

BTB-CSC	*f*=40k	*f*=70k	*f*=100k	*f*=140k
Loss (W)	678	712	745	790
Heatsink (g)	2408	2685	3010	3565
Power device (g)	432	432	432	432
Input filter (g)	724	730	1010	756
DC Inductor (g)	1166	767	600	477
Output filter (g)	24	18	15	10
Fan (g)	50	50	50	50
Total Weight (g)	**4804**	**4682**	**5117**	**5290**

Table 3-5 Design Results for 12-Switch Matrix Converter

Matrix	*f*=40k	*f*=70k	*f*=100k	*f*=140k
Loss (W)	369	401	433	475
Heatsink (g)	902	1066	1230	1460
Power device (g)	504	504	504	504
Input filter (g)	604	548	674	510
Fan (g)	50	50	50	50
Total Weight (g)	**2060**	**2168**	**2458**	**2524**

Some interesting observations can be made based on the topology comparison results. Matrix converter, which requires no dc-link capacitors, has often been considered a natural choice for high-density design. In our case, the comparison clearly shows that the matrix converter does not result in a lower weight design due to its higher loss and corresponding larger heatsink. The BTB-CSC would be a good topology that suits well with the normally-on characteristics of SiC JFET. Unfortunately, its high loss makes it

the heaviest design among the four candidate topologies. These comparison results prove the value of a systematic topology evaluation in high-density converter design.

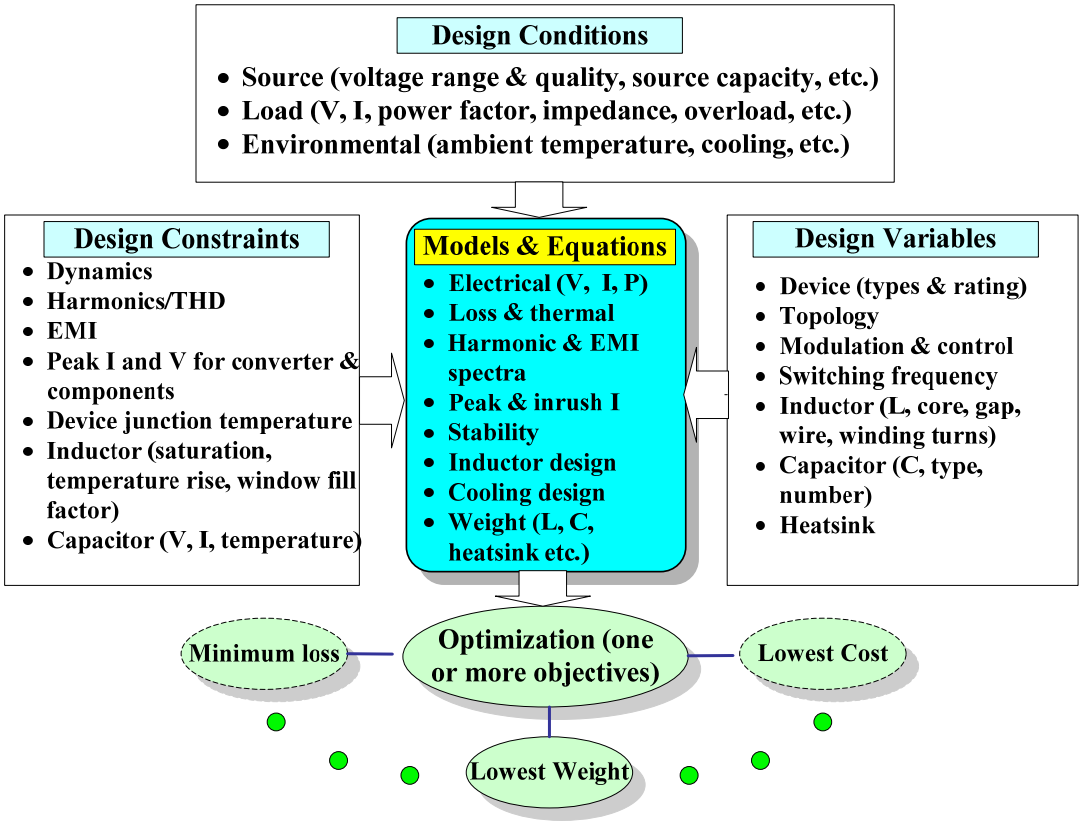


Figure 3-19 Formulation of the converter optimization

As mentioned earlier, the presented topology evaluation approach is formulated similarly to an optimization problem. The design conditions, constraints, and variables are defined for achieving a high-density design. The focus of the work has been on establishing the relationships between all these parameters and on determining the preferred topology relative to the others. Although the presented designs may only be preferred rather than optimal due to limited iterations, the approach provides insight on correlations of all key parameters, which can be applied to any ac-ac converters. The proposed approach and analysis can also form a basis for global optimization of an ac-ac converter. Figure 3-19 shows the conceptual formulation of such an optimization. The

key to the optimization is establishing the relationships, through models and equations, between design conditions, constraints, variables, and objectives, which has been the main focus of this work. The actual optimization can follow various standard algorithms including generic algorithm [75], which is not covered in this dissertation.

3.4 Summary

A systematic evaluation approach of three-phase PWM ac-ac converter topologies for high-density design has been developed in this chapter. All major components and subsystems in a converter system are considered, including the switching devices, heatsink, energy storage and filter passive components, and auxiliary circuits. A comprehensive list of design conditions, constraints, and parameters, and their interdependencies on converter density are considered. With the high frequency capability SiC devices assumed, the impact of the switching frequency is carefully studied considering loss, passive size, and EMI filter design, culminating with identifying a non-monotonous relationship. The impact of modulation schemes on loss and passives is also considered, and it is found that lower-loss modulation schemes do not necessarily lead to bigger passives. The concept of using the same inductor for harmonic suppression and EMI filtering is implemented in the design. In addition, auxiliary circuits such as protection circuits can add to the total size and weight. Based on the proposed approach four active front-end converters using SiC devices are quantitatively compared for lowest weight design. The comparison results show that the BTB-VSI and NTR-VSI topologies present lighter total weight for the given specifications than BTB-CSC or matrix

converter. The proposed methodology can be extended to other topologies with different comparison metrics and can be a useful tool for high-density topology selection.

Chapter 4 Modeling and Control for Non-Regenerative Three-Level Boost Rectifier

In the previous chapter the non-regenerative three-level boost (Vienna-type) rectifier plus voltage source inverter is found to be the preferred topology from the system weight standpoint. However the control for the Vienna-type rectifier is relatively complicated due to the three-level structure. Good control approach is desired to guarantee the high frequency operation in order to achieve the high density.

This chapter starts with the development of a new average d-q model for the Vienna-type rectifier. An optimal zero sequence injection concept is found from the perspective of dc-link voltage balance. With this average model a new control algorithm with carrier-based PWM implementation is developed, which features great simplicity and good neutral point regulation. The proposed control approach is verified by experiments.

4.1 Introduction

The non-regenerative three-level boost rectifier [76] [77] [78] is characterized by reduced number of active switching devices, high input power factor and low device voltage stress, which make it a suitable topology for medium and high power applications [13] [79]. But its controller is relatively complex because of the current forced commutation characteristics and the dc-link neutral point voltage regulation requirement.

In the past several years lots of research work has been put on the Vienna-type rectifier, including the average model manipulation [80] [81] [82] and the control scheme development [52] [71] [83] [84] [85]. The previous modeling efforts focused on the d-q

representation for the rectifier system. However, due to the intrinsic time variant nature of the dc-link neutral point current [50] it is difficult to directly achieve the equilibrium point with the conventional d-q coordinate transformation. For this reason low frequency state model [80] [81] [82] was built by averaging the dc-link neutral point operation in a complete ac line cycle.

On the control side, several approaches have been proposed for this type of rectifier. Hysteresis current control [83] is simple to implement as the switch gating signals are generated by comparison of the reference and measured currents. The drawback of this approach is that the frequency is not constant, which is not desirable for industrial applications. Constant-frequency integration control [84] and unity power factor control [52] feature both simplicity and constant switching frequency, but they do not provide closed loop regulation capability for the dc-link neutral point voltage. Consequently in order to limit the voltage unbalance of the dc link, bigger dc-link capacitors are needed. Three-level space vector based control scheme [71] [85] provides a clear insight into the system control and operation as the redundant vectors can be utilized to regulate the neutral point voltage. However large calculation effort is required for the implementation, which has limited its application in high switching frequency cases. And the control loop design for the voltage balance is absent in the existent control approaches [52] [71] [84] due to the limited frequency range of the available models.

In this chapter, a new average model for the Vienna-type rectifier with extended frequency range is proposed based on the state space analysis and the concept of optimal neutral point current injection. The state space model for the system is first built and the relationship between the controlled duty cycle and the voltage unbalance is set up with

the differential equation. Based on this correlation an optimal zero-sequence component for the duty cycle is found to achieve zero current injection to the dc-link neutral point, which implies an equilibrium point of dc-link voltage balance. By utilizing this optimal zero component into the duty cycle the average model for the neutral point operation can be greatly simplified, and a simple mathematical relationship between the voltage unbalance and the controlled zero sequence duty cycle is found. Therefore the neutral point voltage control loop can be easily designed.

Based on the proposed average model, a new control algorithm with carrier-based implementation is presented, with which the full control function of the Vienna-type rectifier is achieved by simply embedding the dc-link voltage balance control loop into the conventional multi-loop d-q controller. Compared to the previous methods, the new control approach features great simplicity and better dc-link voltage regulation. An FPGA-DSP controlled rectifier prototype is built and the proposed model and control approach are verified by the simulation and the experiment results.

The space vector representation is also utilized to analyze the voltage balance mechanism of the neutral point as well as the feasible operation region. The analysis shows that they are mathematically the same in terms of keeping the neutral point balance. However, in the proposed approach the zero sequence duty cycle is partially generated by a feed-forward method instead of the space vector modulator, which leads to a significant reduction of the calculations.

4.2 Average Model Derivation

The topology of a non-regenerative three-level boost rectifier is shown in Figure 4-1, which comprises of a main diode bridge and the neutral point switch cells. As can be seen, only one controlled switch is used for each phase leg. Since this type of rectifier is current force commutated, the rectifier pole voltage (V_{AN}, V_{BN}, V_{CN}) is determined by not only the controlled switch state but also the polarity of the phase current at the corresponding instant. For instance, if the switch Qa is off and the line current i_A is positive, the phase leg A is clamped to the positive dc link, therefore V_{AN} is equal to $V_{dc}/2$. Similarly, if Qa is off and i_A is negative, V_{BN} will be $-V_{dc}/2$. If the Qa is on, phase leg A will be clamped to the midpoint of the dc link and V_{AN} is zero, regardless of what the current polarity it is. The same operation principle applies to phase B and phase C.

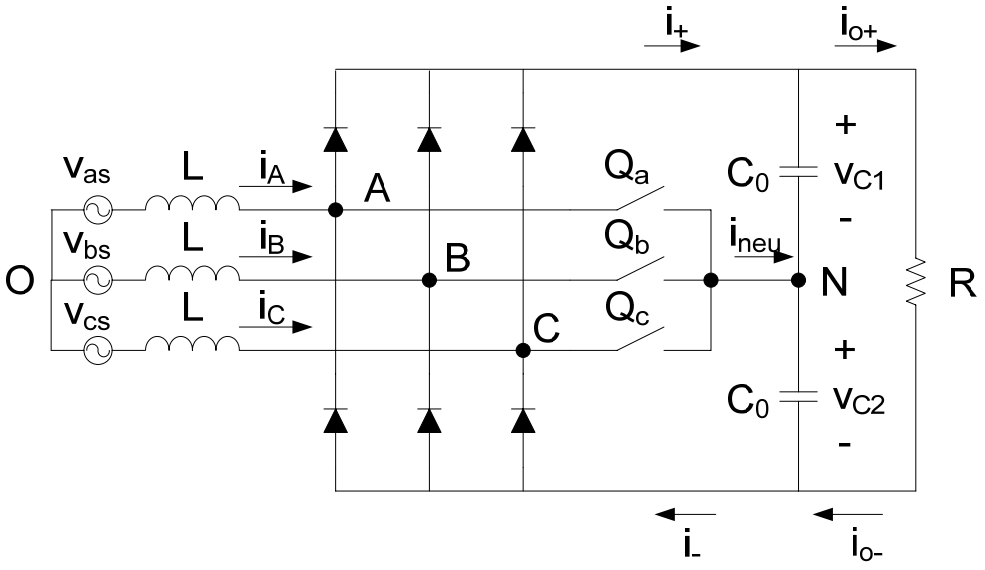


Figure 4-1 Rectifier topology

For the input stage, the state space equations are given by

$$\begin{cases} V_{as} = L\dfrac{di_A}{dt} + V_{AN} + V_{NO} \\ V_{bs} = L\dfrac{di_B}{dt} + V_{BN} + V_{NO} \\ V_{cs} = L\dfrac{di_C}{dt} + V_{CN} + V_{NO} \end{cases}. \tag{4-1}$$

Since the Vienna-tupe rectifier is current force commutated, the switch voltage V_{AN}, V_{BN} and V_{CN} are determined by both the switching pattern and the current polarity, which are given by

$$\begin{cases} V_{AN} = \dfrac{v_{dc}}{2} \cdot [\mathrm{sgn}(i_A) + \dfrac{\Delta v}{v_{dc}}] \cdot (1 - S_a) \\ V_{BN} = \dfrac{v_{dc}}{2} \cdot [\mathrm{sgn}(i_B) + \dfrac{\Delta v}{v_{dc}}] \cdot (1 - S_b) \\ V_{CN} = \dfrac{v_{dc}}{2} \cdot [\mathrm{sgn}(i_C) + \dfrac{\Delta v}{v_{dc}}] \cdot (1 - S_c) \end{cases}. \tag{4-2}$$

where $v_{dc}=v_{C1}+v_{C2}$, $\Delta v=v_{C1}-v_{C2}$, sgn is the sign function, Sa, Sb and Sc are the switching function defined as

$$S_{a,b,c} = \begin{cases} 0 & \text{if } Q_{a,b,c} \text{ is turned off} \\ 1 & \text{if } Q_{a,b,c} \text{ is turned on} \end{cases}. \tag{4-3}$$

Normally Δv is much smaller than v_{dc} and therefore the Δv components in (4-2) can be ignored, which leads to

$$\begin{cases} V_{AN} = \dfrac{v_{dc}}{2} \cdot \mathrm{sgn}(i_A) \cdot (1 - S_a) \\ V_{BN} = \dfrac{v_{dc}}{2} \cdot \mathrm{sgn}(i_B) \cdot (1 - S_b) \\ V_{CN} = \dfrac{v_{dc}}{2} \cdot \mathrm{sgn}(i_C) \cdot (1 - S_c) \end{cases}. \tag{4-4}$$

Defined the phase leg duty cycle as

$$d_{a,b,c} = (1 - \overline{S}_{a,b,c}) \cdot \mathrm{sgn}(i_{A,B,C}) = d'_{a,b,c} + d_0 . \tag{4-5}$$

where $\overline{S}_{a,b,c}$ represents the average switch on time for Q_a, Q_b and Q_c respectively, $d'_{a,b,c}$ and d_0 are the sinusoidal components and the zero sequence duty cycle.

In addition, assuming the input voltages are balanced sinusoidal and the neutral point is disconnected, it follows

$$V_{as} + V_{bs} + V_{cs} = 0 . \tag{4-6}$$

$$i_A + i_B + i_C = 0 . \tag{4-7}$$

Substituting (4-3)-(4-7) into (4-1), we can achieve the state space average model for the Vienna rectifier input stage, which is given by

$$\begin{cases} V_{as} = L\dfrac{di_A}{dt} + \dfrac{v_{dc}}{2}\cdot d_a' \\ V_{bs} = L\dfrac{di_B}{dt} + \dfrac{v_{dc}}{2}\cdot d_b' \\ V_{cs} = L\dfrac{di_C}{dt} + \dfrac{v_{dc}}{2}\cdot d_c' \end{cases} . \tag{4-8}$$

(4-8) has the same expression as the conventional two-level voltage source rectifier. With Park's transformation the equivalent d-q representation of (4-8) is given by

$$\begin{cases} V_{sd} = L\dfrac{di_d}{dt} - \omega_0 \cdot L \cdot i_q + \dfrac{v_{dc}}{2}\cdot d_d' \\ V_{sq} = L\dfrac{di_q}{dt} + \omega_0 \cdot L \cdot i_d + \dfrac{v_{dc}}{2}\cdot d_q' \end{cases} . \tag{4-9}$$

For the dc output stage, the state space model is given by

$$\begin{cases} C_0\dfrac{dv_{C1}}{dt} = i_+ - \dfrac{v_{dc}}{R} \\ C_0\dfrac{dv_{C2}}{dt} = i_- - \dfrac{v_{dc}}{R} \end{cases} . \tag{4-10}$$

According to KCL and the switching pattern, the relationship between the dc bus current and the input current is given by

$$i_+ + i_- = d_a \cdot i_A + d_b \cdot i_B + d_c \cdot i_C . \tag{4-11}$$

$$i_{neu} = i_- - i_+ = \overline{S}_a \cdot i_A + \overline{S}_b \cdot i_B + \overline{S}_c \cdot i_C . \tag{4-12}$$

After substituting (4-5), (4-11), (4-12) into (4-10) and some algebraic manipulation, the state space average model can be given by

$$C_0 \frac{dv_{dc}}{dt} = d'_a \cdot i_a + d'_b \cdot i_b + d'_c \cdot i_c - 2\frac{v_{dc}}{R} = d'_d \cdot i_d + d'_d \cdot i_d - 2\frac{v_{dc}}{R} . \tag{4-13}$$

$$C_0 \frac{d\Delta v}{dt} = |i_A| \cdot d'_a + |i_B| \cdot d'_b + |i_C| \cdot d'_c + d_0(|i_A| + |i_B| + |i_C|) . \tag{4-14}$$

Assuming

$$d_0' = -\frac{|i_a| \cdot d_a' + |i_b| \cdot d_b' + |i_c| \cdot d_c'}{|i_a| + |i_b| + |i_c|} . \tag{4-15}$$

$$d_0 = d_0' + \Delta d_0 . \tag{4-16}$$

then (4-14) can be simplified as

$$C_0 \frac{d\Delta v}{dt} = 2\Delta d_0 \cdot \frac{|i_A| + |i_B| + |i_C|}{2} . \tag{4-17}$$

Actually $\frac{|i_A| + |i_B| + |i_C|}{2}$ is equal to the absolute value of the maximum instantaneous input current. Ignoring all the harmonic components, (4-17) can be further simplified for unity power factor application as (4-18) for unity power factor case.

$$C_0 \frac{d\Delta v}{dt} \approx \frac{2\sqrt{6}}{\pi} i_d \cdot \Delta d_0 . \tag{4-18}$$

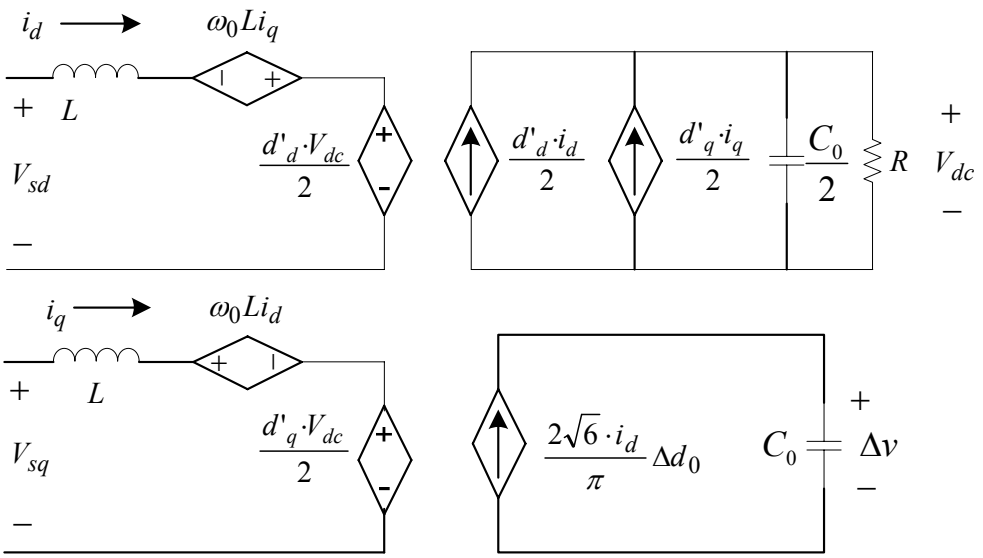


Figure 4-2 State space average model

With (4-9), (4-13) and (4-18) the equivalent circuit model is shown in Figure 4-2. In this model the impact of the voltage unbalance on the input current is neglected. As can be seen, the behavior of the dc-link unbalance is modeled as a simple first order system, based on which the neutral point voltage controller can be easily designed under a given operating point. Figure 4-3 shows the control loop for the dc-link voltage balance. A simple proportional compensator is utilized for the feed back regulation. K_p is the proportional gain, which is given by

$$K_p = \frac{\pi \cdot \omega_n \cdot C_0}{2\sqrt{6} \cdot I_d}. \tag{19}$$

where I_d is the steady state d channel current and ω_n is the control bandwidth.

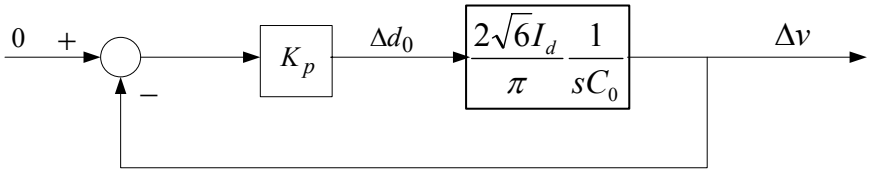


Figure 4-3 Neutral point voltage control loop

4.3 Proposed Controller

The key to making use of the proposed model is to find the zero component d'_0 defined in (4-15). In unity power factor case, ignoring the voltage drop across the inductor L, (4-15) can be represented by (4-20). M is the modulation index defined as the peak phase voltage over half of the dc-link voltage, ω_0 is the frequency of the source voltage.

$$d_0' = -M \frac{|\cos(\omega_0 t)| \cdot \cos(\omega_0 t) + |\cos(\omega_0 t - 120°)| \cdot \cos(\omega_0 t - 120°) + |\cos(\omega_0 t + 120°)| \cdot \cos(\omega_0 t + 120°)}{|\cos(\omega_0 t)| + |\cos(\omega_0 t - 120°)| + |\cos(\omega_0 t + 120°)|}. \quad (4\text{-}20)$$

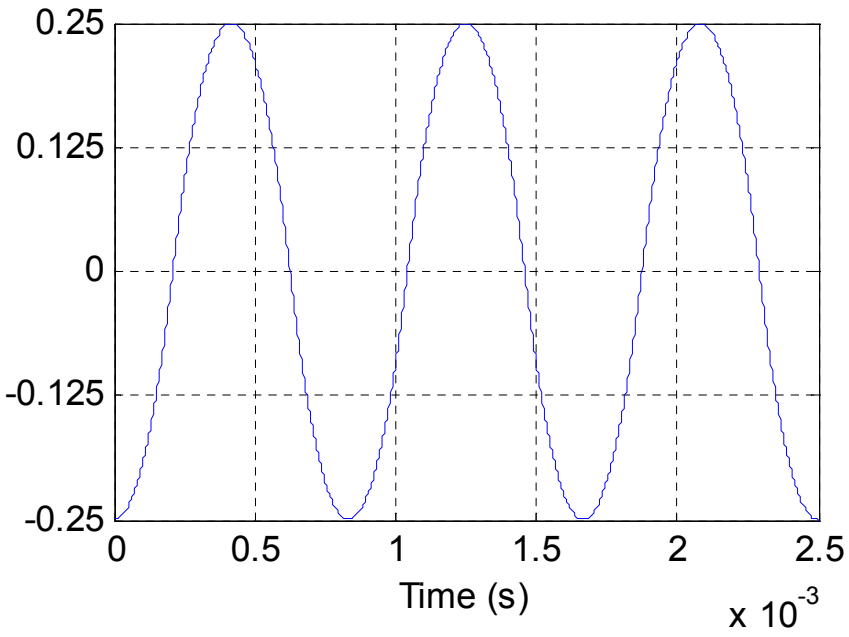


Figure 4-4 Time domain waveform of d_0' (M=1, ω_0=400 Hz)

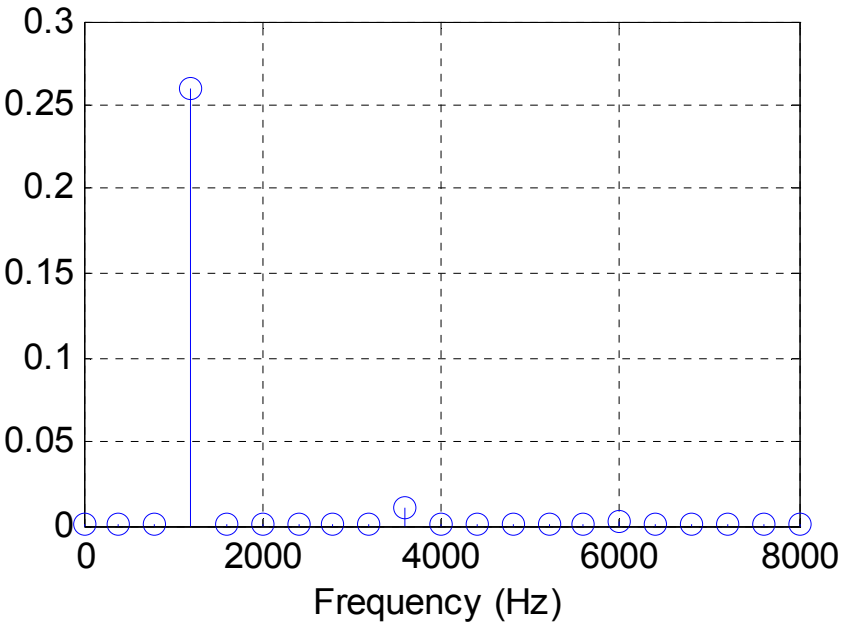


Figure 4-5 Spectrum of d_0' (M=1, ω_0=400 Hz)

The time domain waveform and the spectrum analysis of (4-20) are shown in Figure 4-4 and Figure 4-5 respectively, which indicate that

$$d'_0 \approx -\frac{M}{4}\cos(3\omega_0 t)\,. \tag{4-21}$$

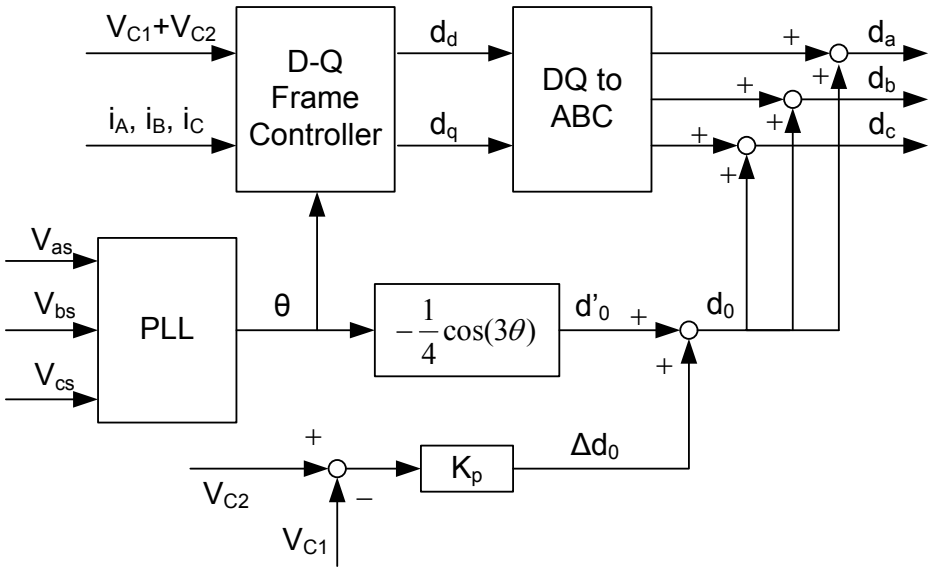


Figure 4-6 Control scheme diagram

The multi-loop controller in the synchronous reference frame (d-q frame) [86] [87] is commonly used to control the three phase boost rectifiers, either two-level or three-level topologies. Typically, the outer loop is designed for the dc link voltage regulation. For the three-level neutral point clamping topology, additional dc voltage balance loop is required. The voltage error is fed to a proportional and integral regulator (PI) and the output of the PI is fed to the inner current loop as the d channel current reference. And then the voltage reference can be achieved by regulating the current error with another PI. Since the reference voltage is in d-q frame, space vector modulation is often the choice for implementation, which is complicated, especially for the Vienna-type rectifier.

Based on the analysis in the previous section, a new controller is proposed, as shown in Figure 4-6. The basic idea of this controller is to implement the space vector modulation scheme in a carrier-based way with the optimal zero sequence developed in this work, which can guarantee zero current injection to the neutral point. In Figure 4-6, the d-q controller represents the standard multi-loop control for a two-level boost rectifier in d-q coordinates [88]. But in this case instead of using the complicated three-level space vector modulator, d_d and d_q are directly converted into abc-coordinates d_a, d_b and d_c through the inverse Park's transformation. The dc link midpoint voltage balance is regulated by the zero sequence component d_0, which consists of two parts: a feed forward component d_0' and a feedback component Δd_0. d_0' is the optimal zero sequence given by (4-21) to achieve no current injection into the neutral point. The feedback component Δd_0 is used to compensate the non-ideal factors in the real system. As can be seen, the control calculations are significantly reduced when compared to previous control schemes

developed, and the neutral point voltage is effectively regulated by the zero sequence component.

4.4 Simulation and Experiment Results

A detailed Saber model has been built to verify the model and the control scheme. Table 4-1 shows the parameters used in the small scaled simulation model. Figure 4-7 shows the steady state waveforms of dc-link voltages, source voltage and source current of phase A. As can be seen, both the input currents and the dc-link voltages are well controlled. Figure 4-8 shows the transient response for a load step up case (the load resistance steps from 50 Ω to 25 Ω). The simulation results indicate that the proposed control approach is stable under load step transient condition. Figure 4-9 shows the voltage unbalance behavior under pulsating Δd_0 with the neutral point voltage feedback loop open. For comparison the results with the mathematical model is also shown. The results show that the proposed model can predict the neutral point voltage unbalance performance under small signal perturbation.

Table 4-1 Parameters Used in Simulation

Source voltage	60 V_{rms}
Source frequency	400 Hz
DC link voltage	180 V
Switching frequency	40 kHz
Input inductance L	160 μH
DC link capacitor C_0	40 μF
Load resistance R	50 Ω

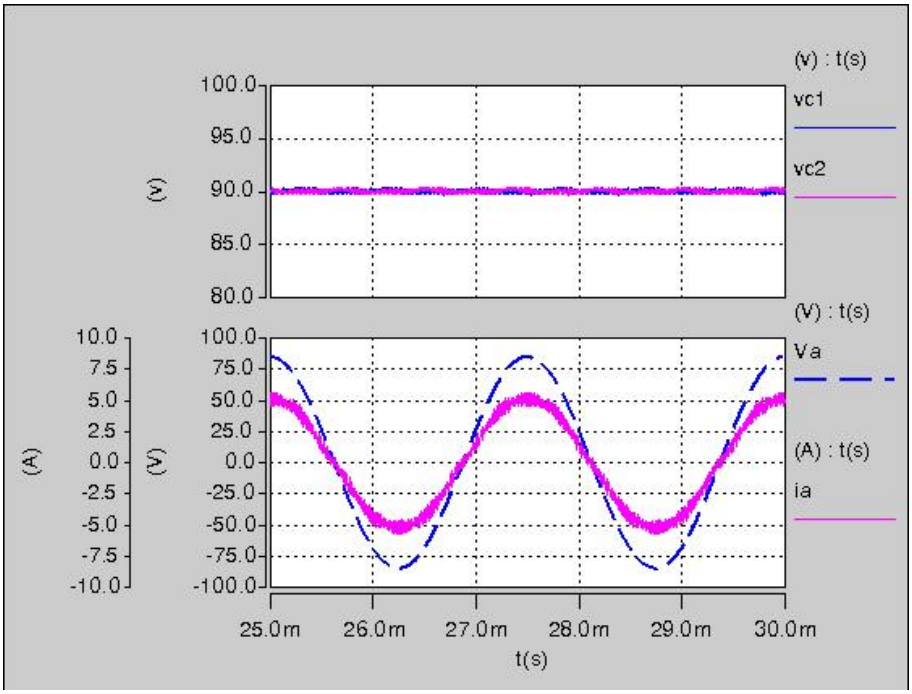


Figure 4-7 Steady state simulation results (The top traces are the voltages across the two dc-link capacitors respectively. The bottom two traces are the input voltage and the line current of phase A.)

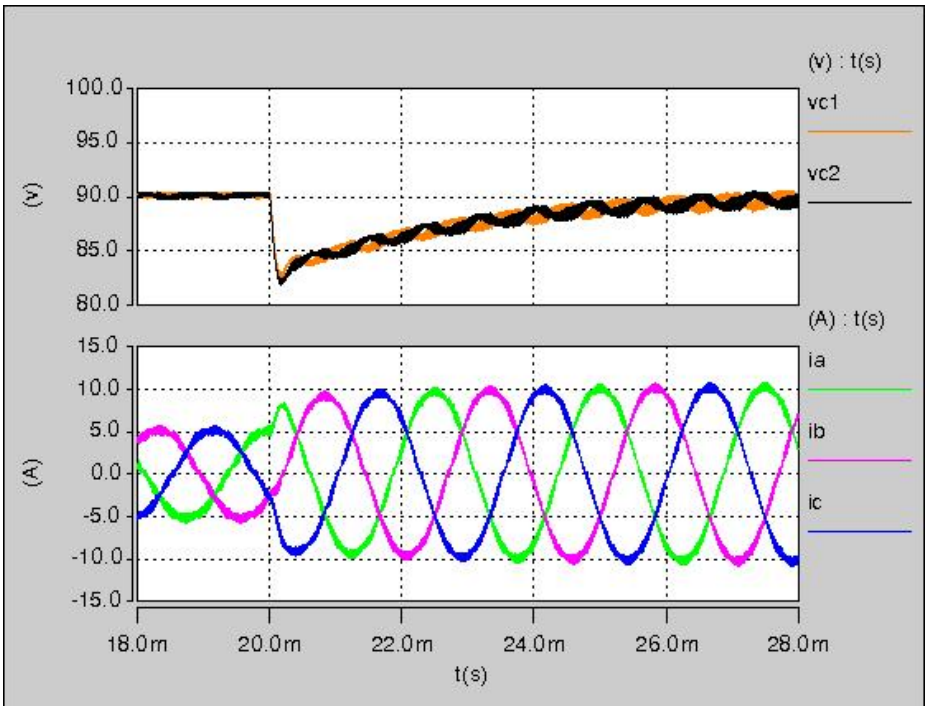


Figure 4-8 Simulation results of load step up transient (The top traces are the dc link voltages. The bottom traces are the input phase currents.)

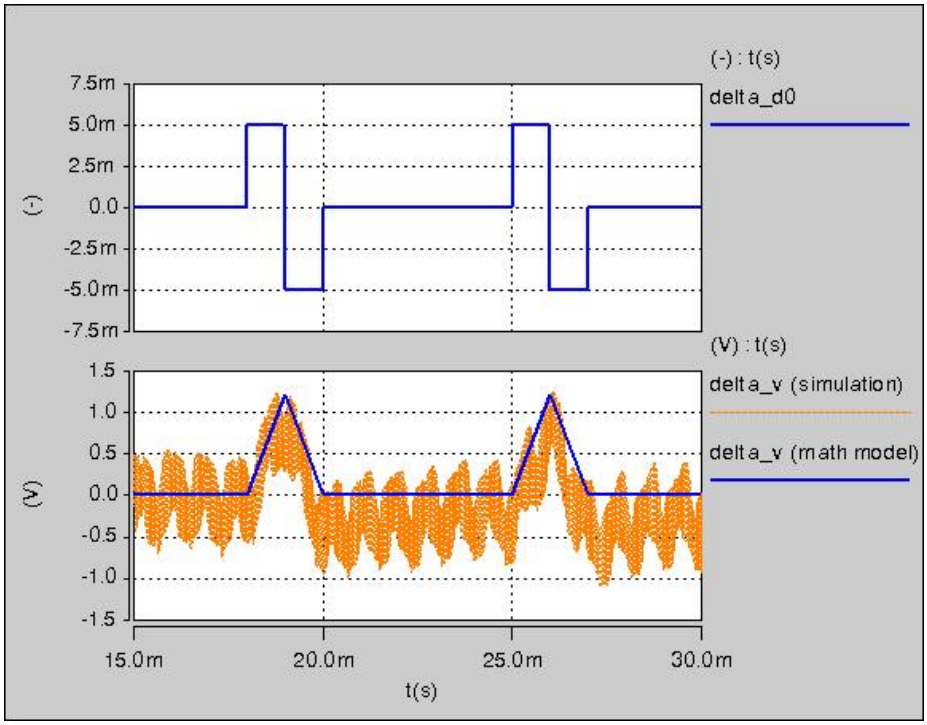


Figure 4-9 Voltage unbalance behavior under pulsating Δd_0 (The top trace is the waveform of Δd_0. The bottom traces show the dc-link voltage unbalance corresponding to the given Δd_0. The light color line is the simulation result and the dark color line is the calculation result from the proposed model.)

In order to verify the proposed controller and the simulation, an experimental system is built in laboratory scale. Figure 4-10 shows the experimental prototype, which was constructed using SiC Shottky diodes and Si MOSFET's, together with a DSP and FPGA based digital control board. The same parameters as in Table I are utilized. Figure 4-11 shows the wave forms of the transient when the converter changes from the diode rectification mode to the active control mode. As can be seen the dc-link voltage increase smoothly and the system is stable. Figure 4-12 shows the steady state experimental results of dc-link voltages, rectifier pole-to-pole voltage and source current respectively. Figure 4-13 shows the dc-link voltage unbalance (V_{C1}-V_{C2}) in steady state. The maximum unbalance is about 4 V for the proposed approach. For comparison the corresponding experimental wave forms with the space vector based controller are shown

in Figure 4-14 and Figure 4-15. The results indicate that the carrier-based control approach has similar performance compared to the space vector based control scheme. And the neutral point voltages are well regulated by both methods even though the dc-link capacitance is very small. Figure 4-16 and Figure 4-17 show the experimental duty cycle components for both control schemes. The zero sequence of the proposed method shown in Figure 4-16 indicates the characteristics of the optimal neutral point injection, which is a standard third order harmonic. The zero component of the space vector control scheme shows some different features since its voltage balance regulation is achieved by only a feedback loop, which has limited loop gain as well as bandwidth and therefore can not exactly track the optimal point.

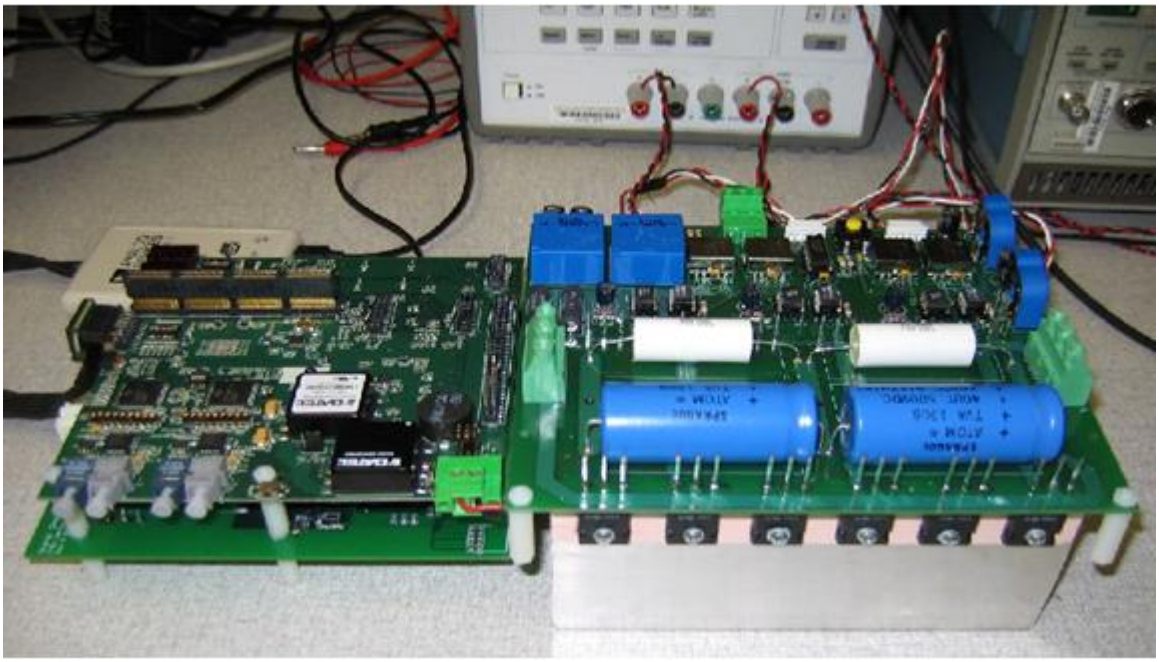


Figure 4-10 Experimental system

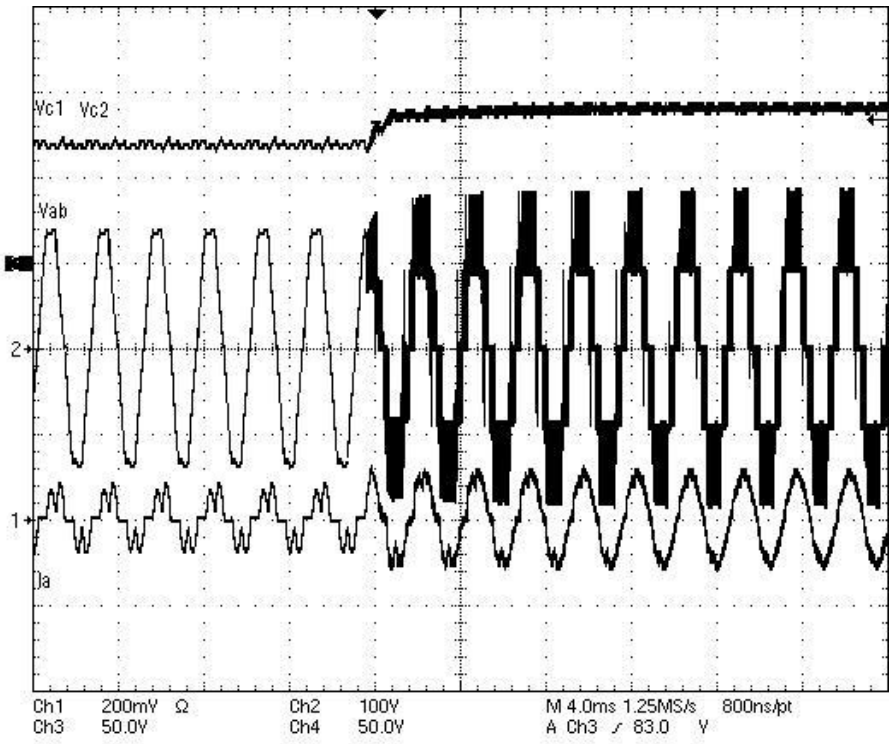


Figure 4-11 Experimental waveform of the transient for operation mode transition (Traces from top to bottom: dc-link voltages, rectifier pole to pole voltage VAB, and input current of phase A.)

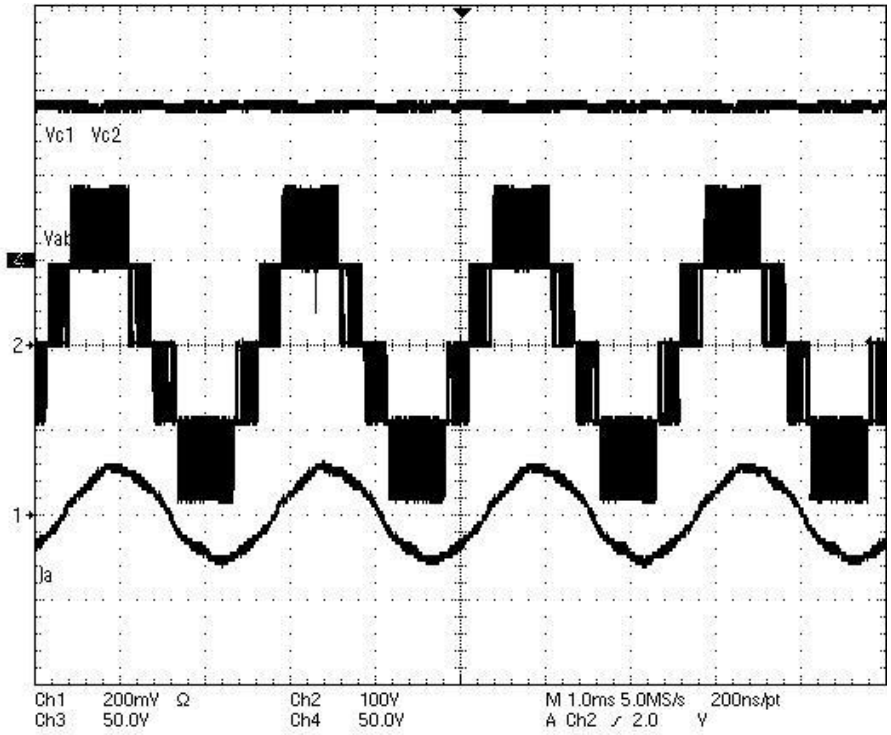


Figure 4-12 Steady state results with the carrier-based control scheme

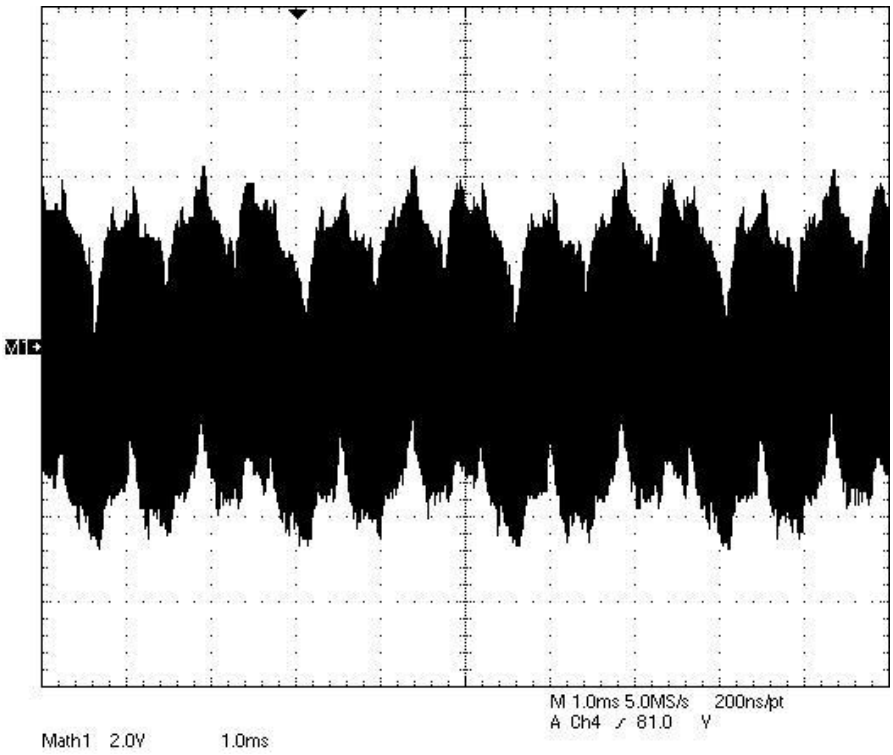


Figure 4-13 Dc-link voltage unbalance with the carrier-based control scheme

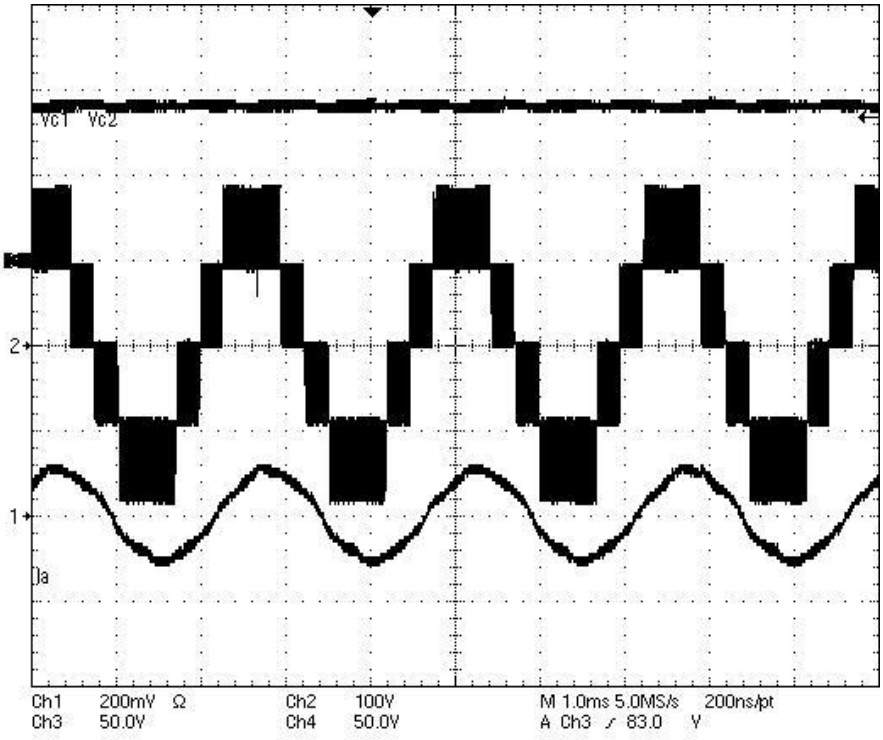


Figure 4-14 Steady state results with the space vector based control approach

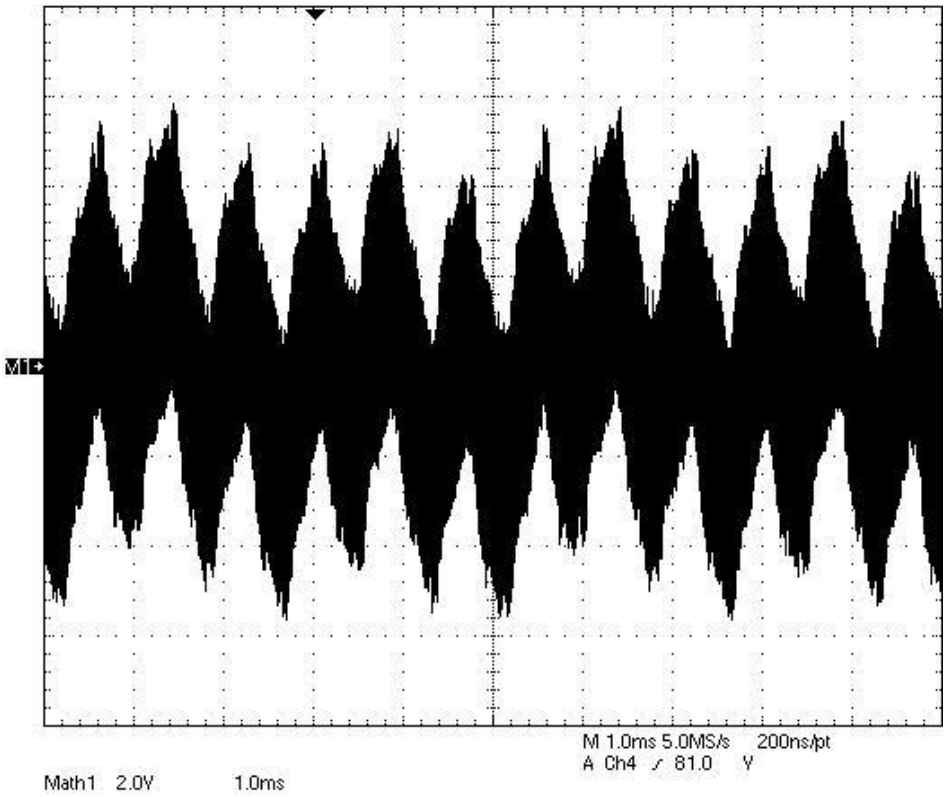


Figure 4-15 Dc-link voltage unbalance with the space vector based control approach

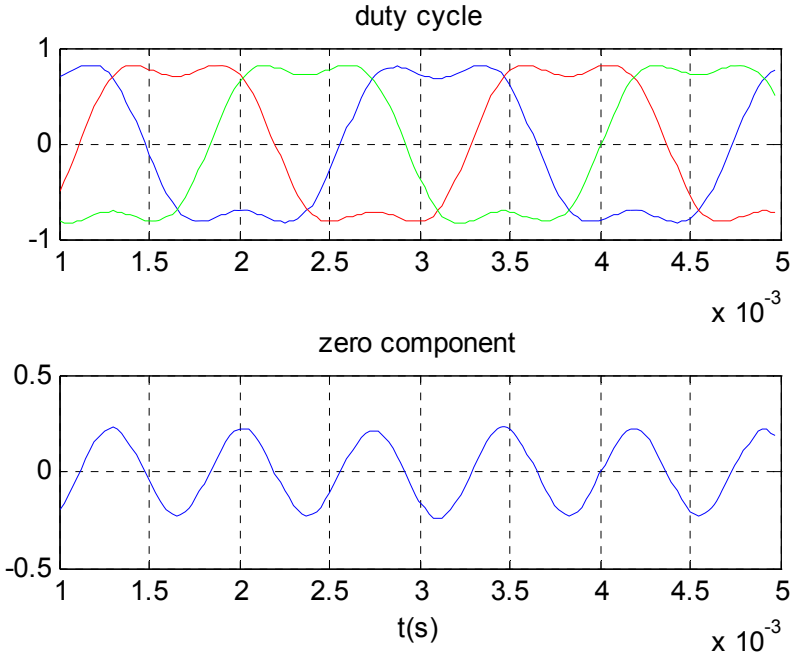


Figure 4-16 Measured duty cycle components of the proposed carrier-based control scheme (The top traces are the duty cycles for three phases. The bottom trace is the zero sequence component.)

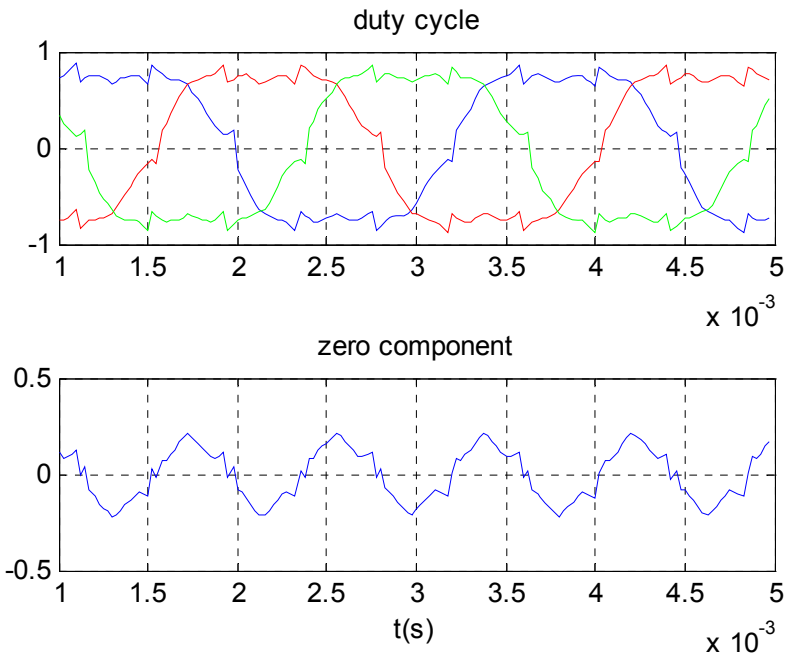


Figure 4-17 Measured duty cycle components of the space vector control scheme (The top traces are the duty cycles for three phases. The bottom trace is the zero sequence component.)

4.5 Space Vector Analysis

Space vector representation is a powerful tool for the analysis of three-phase converter since it provides the clear insight for the terminal voltage and current behavior. In this section space vector analysis is carried out to study the neutral voltage balance mechanism and the feasible operation region under the balance condition.

A. Neutral Point Voltage Balance Mechanism

According to the symmetry of space vectors, only 60° needs to be considered as shown in Figure 4-18. 1 and 0 represent the on and off states of the corresponding switch respectively. And φ is the angle between the vector (0,0,0) and the reference voltage vector. In sector I, if φ is smaller than 30°, (1,0,0) and (0,1,1) point to the same vector. If φ is larger than 30°, (1,1,0) and (0,0,1) point to the same vector. Although these

redundant vectors have the same voltage representation in the α-β plane, they lead to different current injection into the neutral point. For instance, in the first 30° region, (1,0,0) indicates the midpoint injecting current to be i_A while (0,1,1) leads to $-i_A$. In the second 30° region, (0,0,1) and (1,1,0) indicate the current injection of i_C and $-i_C$ respectively. Assuming the line current is in phase with the reference voltage, the redundant vectors are always charging or discharging the dc link midpoint with the maximum line current. Therefore the combination of these redundant vectors can be used to balance the neutral point voltage as an extra control variable in the space vector based approach [19].

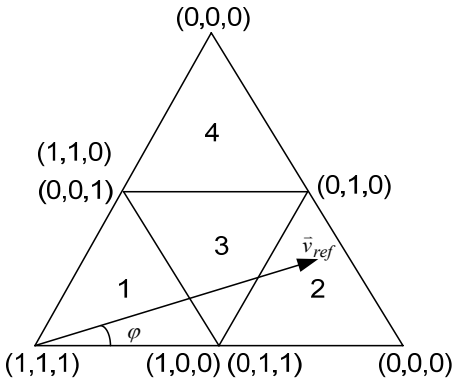


Figure 4-18 Space vector diagram in 60º

For example, if the reference voltage vector lies in sub-sector 2, the corresponding relative on-times for the vectors are given by [20].

$$\begin{cases} d_{(1,0,0)} + d_{(0,1,1)} = 2 - \sqrt{3} \cdot M \cdot \sin(\varphi + 60°) \\ d_{(0,0,0)} = \sqrt{3} \cdot M \cdot \cos(\varphi + 30°) - 1 \\ d_{(0,1,0)} = \sqrt{3} \cdot M \cdot \sin(\varphi) \end{cases} . \qquad (4\text{-}22)$$

where M is the modulation index defined as the peak phase voltage over half of the DC link voltage.

Notice that the first equation of (4-22) shows the redundant vectors (1,0,0) and (0,1,1) corresponding to sub-sector 2. And there are infinite solutions. In order to achieve zero neutral point current injection, the relative on-times in (4-22) should be also subject to

$$d_{(0,1,0)} \cdot i_B + (d_{(1,0,0)} - d_{(0,1,1)}) \cdot i_A = 0 . \tag{4-23}$$

With (4-22) and (4-23) the relative on-times of the voltage vectors can be achieved. Due to the characteristics of current force commutation, the phase leg duty cycles can be given by

$$\begin{cases} d_a = (1 - d_{(1,0,0)}) \cdot \mathrm{sgn}(i_A) \\ d_b = (1 - d_{(0,1,1)} - d_{(0,1,0)}) \cdot \mathrm{sgn}(i_B) \\ d_c = (1 - d_{(0,1,1)}) \cdot \mathrm{sgn}(i_C) \end{cases} . \tag{4-24}$$

where sgn is the signum function. Then the equivalent zero sequence for the space vector modulation scheme (SVM) can be obtained through

$$d_{0\_SVM} = \frac{d_a + d_b + d_c}{3} . \tag{4-25}$$

Assuming the line currents are in phase with the reference voltage, they are given by

$$\begin{cases} i_A = I_m \cdot \cos\varphi \\ i_B = I_m \cdot \cos(\varphi - 120°) \\ i_C = I_m \cdot \cos(\varphi + 120°) \end{cases} . \tag{4-26}$$

where I_m is the amplitude of the line current.

With (4-21)-(4-26) the optimal zero sequence duty cycle for the space vector modulation scheme in sub-sector 2 can be derived as

$$d_{0\_SVM} = \frac{M}{2\cos\varphi} \cdot (\frac{1}{2} - \cos 2\varphi) \qquad 0 \le \varphi \le 30° . \tag{4-27}$$

Following the same method, the zero sequence leading to zero neutral current injection for the other sub-sectors can be derived. The analysis results show that the optimal zero sequence is only the function of M and φ regardless of the sub-sector location. For example, When 30°≤ φ ≤60°, the zero component is given by

$$d_{0\_SVM} = \frac{M \cdot \cos\varphi \cdot (\sqrt{3}\sin\varphi - \cos\varphi)}{\sqrt{3}\sin\varphi + \cos\varphi} \quad (30° \le \varphi \le 60°) . \tag{4-28}$$

With the same assumption, substituting φ for $\omega_0 t$ in (20) leads to

$$d_0' = \frac{M}{2\cos\varphi} \cdot (\frac{1}{2} - \cos 2\varphi) . \tag{4-29}$$

(4-28) and (4-29) show that in sub-sector 2 the space vector based control scheme has the same zero sequence duty cycle as the proposed carrier based control scheme. Actually this conclusion stands for all the other sub-sectors. This analysis indicates that the proposed control approach is the same as the space vector approach from the math standpoint. But the zero sequence in the carrier-based method is generated in a partially feed-forward way instead of going through the complicated space vector modulator.

B. Operating Region Analysis

In general, the zero sequence injection technique is used in the carrier-based modulation scheme in order to increase the possible modulation index [42]. However, the zero sequence component in this work is derived from the neutral voltage balance standpoint instead. Therefore its impact on the operating region (feasible modulation index) needs to be investigated.

The analysis can be carried out based on the vector synthesis equations. For example, if the target reference voltage locates in sub-sector 2 as shown in Figure 4-15, define the distribution ratio of the redundant voltage vectors as

$$r = \frac{d_{(1,0,0)}}{d_{(1,0,0)} + d_{(0,1,1)}}. \tag{4-30}$$

After substituting (4-26), (4-30) into (4-22), (4-23) and some algebraic manipulation, the following relationship can be achieved.

$$1 - 2r = \frac{\cos(\varphi - 120°)}{\cos\varphi} \cdot \frac{\sqrt{3}M \sin\varphi}{2 - \sqrt{3}M \sin(\varphi + 60°)}. \tag{4-31}$$

Since (4-23) is included in the derivation, (4-31) guarantee zero current injection to the dc link midpoint. For a feasible solution, the distribution ratio *r* should be within the range between 0 and 1, which leads to

$$-1 \le 1 - 2r \le 1. \tag{4-31}$$

With (4-31) and (4-32) the upper boundary for the modulation index can be obtained as

$$M \le \frac{2\cos\varphi}{\sqrt{3}\sin(2\varphi + 60°)}. \tag{4-32}$$

In sub-sector 2, $0 \le \varphi \le 30°$, therefore the minimum upper boundary in (4-32) can be achieved when $\varphi = 30°$, as

$$M \le \frac{2}{\sqrt{3}}. \tag{4-33}$$

(4-33) indicates that the full modulation index can be achieved in sub-sector 2 when considering zero current injection to the dc link midpoint. The approach is applied to the other sectors and the results lead to the same conclusion. The full modulation index can be achieved when using the optimal zero sequence injection.

4.6 Summary

This chapter presented a new average model for the non-regenerative three-level boost (Vienna-type) rectifier using the concept of zero neutral point current injection. The optimal zero sequence duty cycle is found to guarantee the dc-link voltage balance, based on which an equilibrium operating point can be found and the behavior of the neutral point voltage deviation can be modeled as a simple first order system. The proposed model features extended frequency range (up to half of the switching frequency) using the conventional d-q representation and therefore can be applied for the high performance controller design. Based on the proposed model a carrier-based control approach is developed. The zero sequence duty cycle, which consists of two components, is used to control the neutral point voltage balance. The feed forward component ensures zero current injection to the neutral point with simple calculation and the feedback component compensates the non-ideal factors in the real system. The space vector analysis shows that the proposed control approach is the same as the space vector based control approach from the math standpoint while it achieves the zero sequence duty cycle in a partially feed forward way. Therefore the proposed control method can significantly reduce the calculation effort. The analysis also proves that that with the optimal zero sequence duty cycle the full modulation index can be still achieved. The proposed model and control scheme are verified by both simulation and experimental results.

Chapter 5 Failure Mode Analysis and Protection

This chapter investigates the failure modes and protection approaches related to the structure of the circuit and the characteristics of SiC devices. A fault type unique to three-level converter including Vienna-type rectifiers, the dc-link voltage-doubling fault, is first introduced. Then two types of protection methods are proposed, discussed and analyzed: the voltage-clamping and the current-breaking protection schemes. The impact of ac inductors on the voltage-doubling phenomenon is studied carefully, and a guideline for the protection scheme selection is provided. This failure mode and the current breaking protection scheme are fully analyzed and verified by simulation and experimental results. This chapter also develops a special protection approach for the shoot-through failure that is suitable for the voltage source converter system built with SiC JFETs. Design considerations are presented, and experiments demonstrate the feasibility of the proposed failure protection.

5.1 Introduction

Failure mode detection and protection is an important aspect for any converter system, especially high-power converters in critical applications where high reliability is required. Therefore, a detailed failure mode analysis and corresponding protection scheme development should be considered in the converter design stage. There are many factors that can lead to faults, such as incorrect operation, loose mechanical connections, and component malfunction. Among these, semiconductor device failure, including short or open of both switches and diodes, is one of the most common faults in a converter. For multi-level converters, the probability of device fault and the modes of failure increase

due to the complicated topology and the large number of devices. Although there has been a great effort to analyze the Vienna-type rectifier [52] [84] [85], most of this work has focused on modulation and control schemes development, with only a few limited studies on failure modes and faults of three-level neutral-point-clamped (NPC) converters, which includes the Vienna-type of converters [89]. These mainly focus on short-circuit and over-current protections [90] [91] [92], or on fault-tolerant control and operation [93]-[100]. The failure mode related to the neutral switching cell and the impacts of the system parameters remain unclear.

Addressing the above, this chapter first focuses on analysis and protection scheme development for the neutral ac switch short-circuit fault in Vienna-type converters. Specifically, it deals with the voltage doubling behavior under this fault condition—unique to three-level NPC structures, and analyzes two different types of protection schemes, namely voltage clamping and current breaking. For the voltage-clamping approach, a simplified design method for the conventional resistor clamping is first developed. Then a protection circuit with varistor clamping is proposed and discussed, which shows a better performance than the resistor clamping. The impact of the input inductance and the dc-link clamping voltage is also investigated, showing that the peak fault current and the power dissipation in the dc-link are proportional to the inverse of the ac inductance when using the voltage-clamping approach. An experimental setup has been constructed and used for verification purposes, demonstrating the validity and good results obtained by the proposed protection schemes. Although the discussions in this work are based on Vienna-type rectifiers, the results and conclusion apply to other three-level NPC converters as well.

Shoot-through failure is another concern for the converter system. The dc-link positive bus and negative bus are directly shorted during a shoot-through failure, and the shoot-through current can reach a level several times higher than the peak current limit of the semiconductor devices in just microseconds. For this reason, the key challenges for designing an effective protection approach are to detect the fault current and to block the short circuit loop within a very short time, which should be in the range of 3 to 10 μs [102]. The de-saturation characteristic of IGBT is usually utilized to detect an over current fault for a converter system built with IGBTs. The detection can be integrated into the gate driver and the protection function can be achieved with an auxiliary logic circuit [103]. This technology has been widely used in commercial gate drivers. However, the situation differs for converter systems built with SiC JFETs, because of the limited knowledge of the characteristics of these new devices. In addition, the de-saturation approach cannot protect the SiC JFETs from shoot-through failure when losing the gate drive power since they are normally-on devices. Therefore it is a necessity to design a protection circuit that can fill the need created by the SiC JFET devices.

This chapter proposes a novel shoot-through protection scheme, which is especially suitable for a converter system built with SiC JFETs. A bi-directional switch cell is embedded in the dc-link capacitor tank, with which the functions of shoot-through protection and dc-link capacitors pre-charge can be achieved. Section II explains the operation mechanism of the protection circuit. Section III describes some considerations for the parameter selection and presents the gate drive circuit. An experimental system is built and to verify the feasibility of the proposed protection approach.

5.2 Neutral Switch Shorted Failure of Vienna-Type Rectifier

5.2.1 Fault Mechanism Analysis

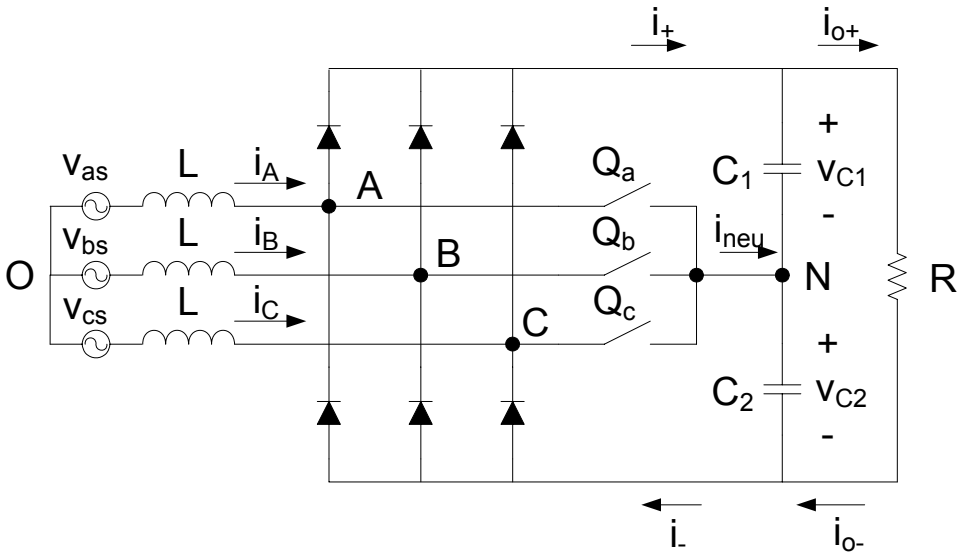


Figure 5-1 Circuit diagram of the non-regenerative three-level boost rectifier

As shown in Figure 5-1, the phase leg terminals in the Vienna-type rectifier are connected to the neutral point of the dc-link through ac switches. Any short-circuit failure of the switching device in these switches leads to a short circuit between the corresponding phase leg and the neutral point, resulting in an over-voltage failure in the dc-link. For example, if Q_a is shorted, point A is clamped to mid-point N. If all other healthy switches are assumed to open once the fault is detected, the equivalent circuit under the fault is like the one shown in Figure 5-2. In this figure, when V_A is positive and V_B and V_C are negative, capacitor C_2 charges to the peak voltage of V_{AB} and V_{AC}, as the remaining circuit acts as a diode bridge. The charging currents are indicated by the arrows shown in Figure 5-2. On the following half line-cycle, capacitor C_1 is accordingly charged to the peak voltage of V_{BA} and V_{CA}.

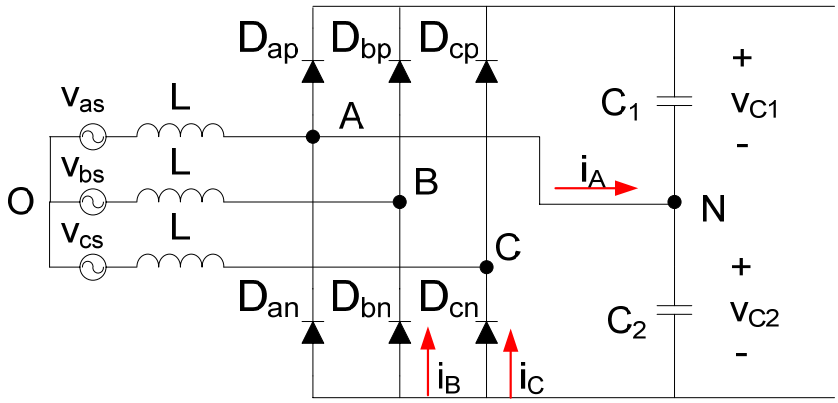


Figure 5-2 Circuit structure when Q_a is shorted

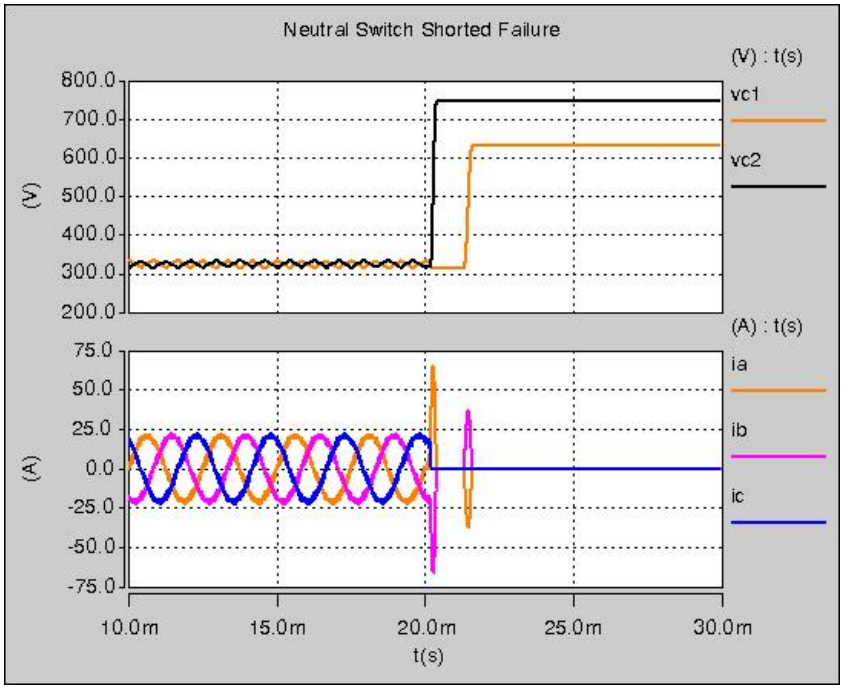


Figure 5-3 Simulation results during the Q_a short: the top traces are capacitor voltages, the bottom traces are input currents

Figure 5-3 shows the simulation results for the case when Q_a is shorted. The simulation parameters used were: input inductance of 150 μH, input phase voltage of 230 V rms and 400 Hz, dc-link load of 42 Ω, and dc-link of 650 V (V_{c1} and V_{c2} equal 325 V). The load resistor is assumed to be disconnected once the fault is detected. At time t = 20 ms, S_1 is shorted and the other two switches are open when the over-voltage condition

is detected. Assuming the source voltages remain unchanged, voltage V_{c1} rises to 620 V and V_{c2} rises to 750 V. The peak half DC voltage is higher than the peak line-to-line voltage due to the energy stored in the input inductors. Compared with the normal operation, where the peak line-to-line voltage is equally shared by C_1 and C_2, the voltages across the dc-link capacitors is basically doubled.

Although the previous analysis is based on the Vienna-type rectifier, it can be applied to any other three-level NPC converter where similar failure modes will be found. In principle, the dc-link voltage doubling can occur for inner device short circuits in both source-side and load-side converters, as long as the ac line-to-line terminal voltages are present during the fault. For instance, in a high-power drive application, the source side usually is connected to the utility grid through an electromechanical switchgear. These take several cycles (on the order of tens of ms) to open when a fault occurs: therefore they will continue feeding the fault in its occurrence. This same behavior is seen when driving synchronous motors, i.e., the terminal voltage remains during the fault, but not when driving induction motors where the voltage would drop, quickly minimizing the fault effect. In this work the focus is on the analysis and protection of the source-side converter.

5.2.2 Over Voltage Protection

As can be seen in Figure 5-3, the voltage across the dc-link capacitors will greatly exceed their voltage rating as well as that of the semiconductors when a short-circuit fault occurs. A protection scheme must then be designed to prevent this over-voltage condition. Based on the above analysis, there are two general approaches to limit the dc-link over-

voltage: 1) a voltage-clamping circuit; and 2) a current-breaking circuit in the charging loop. These two schemes are discussed below.

A. Voltage Clamping Approach

Figure 5-4 (a) shows the basic circuits for the clamping approach. In normal operation, switches S_1 and S_2 are open and the protection circuit does not affect the system. When an over-voltage is detected, the switches are closed and the resistors are connected to the capacitors. In this way the extra energy caused by the fault is dissipated, clamping the dc-link voltage. The actual voltage reached during the fault and the power dissipation is highly dependent on the system parameters, such as input voltage, input inductance, and the clamping resistance. Therefore the protection circuit must be designed according to these parameters and the worst-case system conditions.

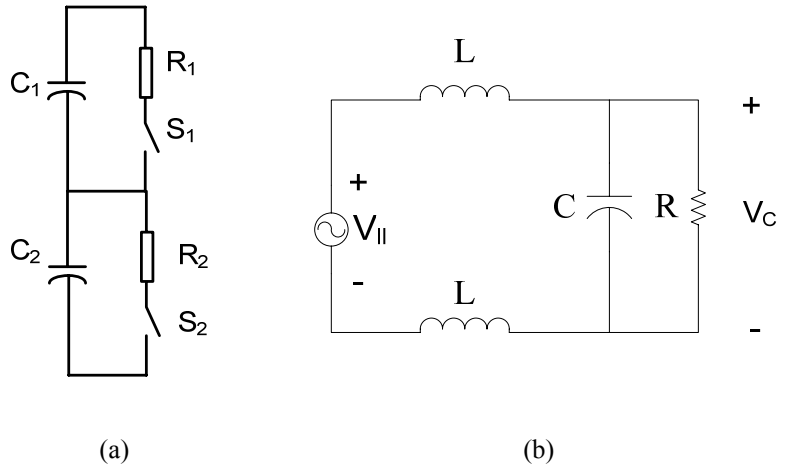


Figure 5-4 (a) Diagram for the voltage clamping protection circuit, (b) simplified circuit for peak voltage approximation

In the fault shown in Figure 5-2, C_1 is charged by the peak line-to-line voltage in a half line-cycle with the highlighted current direction, and C_2 is charged in the following half line-cycle with opposite current direction. If the capacitance value is the same for

both capacitors (as is expected per the design), the voltage across each capacitor can be roughly approximated by the circuit shown in Figure 5-4 (b). The positive half line-cycle represents the charging period for capacitor C_2, while the negative half line-cycle represent the charging of C_1 with opposite voltage polarity. The failure mode behavior of the converter can then be approximated by a second-order circuit with sinusoidal excitation. The peak voltage across the capacitor is then given by

$$\frac{V_{C\_p}}{V_{ll\_p}} \approx \frac{1}{1-2\omega^2 LC + j\frac{2\omega L}{R}} \tag{5-1}$$

where V_{ll_p} is the peak line-to-line voltage, ω is the line frequency and R is the clamping resistance. Equation (5-1) can accordingly be used to design R. For example, using the simulation parameters in the previous section, if the clamping voltage is set to 450 V, the required clamping resistance is 0.9 Ω.

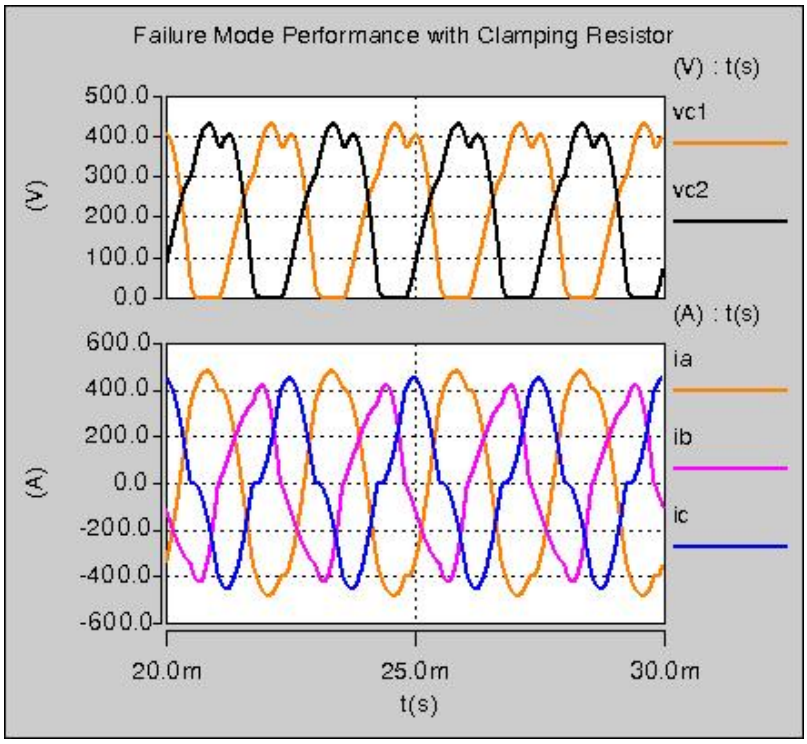


Figure 5-5 Simulation results for resistor clamping

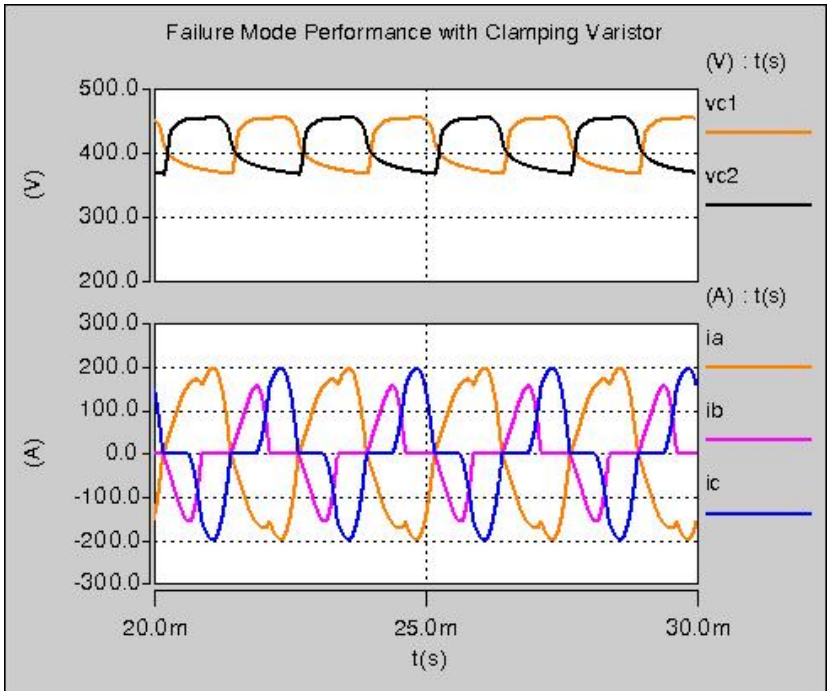


Figure 5-6 Simulation results for varistor clamping

The simulation result with resistor clamping is shown in Figure 5-5. The peak voltage across the capacitor is 430 V, which is close to the design value indicating that (5-1) can be used to design the clamping resistance The peak value of the fault input current is 450 A and the average power dissipation across the resistor is 78 kW. The rating of the resistor can be determined based on the power dissipation and the fault clear time.

Figure 5-5 shows simulation results of the proposed protection scheme where very high fault currents are observed on the input side. (With magnetic saturation, these fault currents could be even higher). There are high fault currents on the input side because the dc-link capacitors are always being discharged by the clamping resistors; therefore the average capacitor voltage is relatively low at the expense of a high fault current. In order to reduce the fault current and the power dissipation in the protection circuit, a voltage clamping circuit using a varistor is proposed instead.

The varistor is a variable resistor. When the voltage across the varistor is lower than a threshold level, the varistor shows a very high resistance; when the voltage increases above the threshold, the resistance diminishes sharply. This characteristic is usually expressed in the following way [101]:

$$I = qV^{\alpha} \tag{5-2}$$

where q and α are the coefficients dependent on the varistor material. At low voltage, even when switches S_1 or S_2 in Figure 5-4 (a) are closed, the energy stored in the capacitor will not be discharged by the varistor. At high voltages, with dramatically lower resistance, the capacitor over-voltage will be clamped to the varistor threshold voltage. Figure 5-6 shows the simulation results for the varistor clamping approach using varistor VE24P01750K from AVX (α=30, q=1.0737×10^{-79}). As can be observed from this figure, the peak voltage is clamped to 450 V and the fault current is reduced to 200 A; the power dissipation is 29.4 kW.

B. Impact of Input Inductance and Clamping Voltage

The input inductance of the converter has a significant impact on the failure mode evolution, particularly on the input current and the dc-link power dissipation during a fault. This is analyzed as follows, where, in order to simplify the study, the voltages across the dc-link capacitors are assumed to be fixed at their maximum feasible value during the fault, which is determined by both the capacitor and semiconductor device ratings. This assumption corresponds to the best scenario from the fault current standpoint, since the dc link voltage remains constant at a high level helping suppress the fault current.

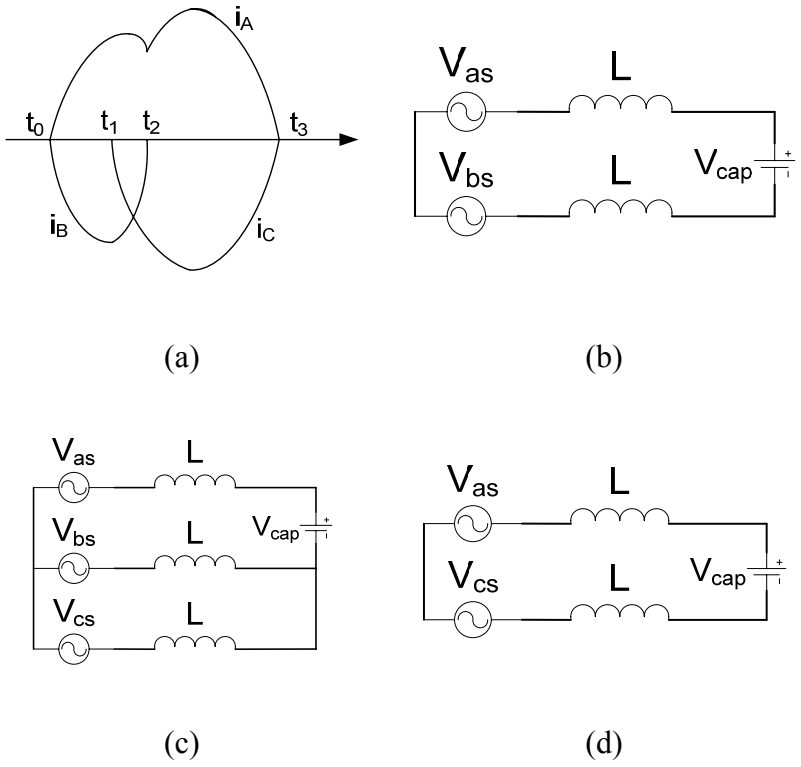


Figure 5-7 (a) Input current waveform in positive half cycle, (b) mode 1, (c) mode 2, and (d) mode 3

According to the condition states of the diodes, there are three distinct periods or operating modes during an ac switch fault. Figure 5-7 (a) shows the typical waveforms for currents i_A, i_B, and i_C observed during the three periods t_0–t_1, t_1–t_2, and t_2–t_3 within a half line-cycle. Figure 5-7 (b)–(d) show the respective equivalent circuits for the different modes. In this analysis, the ac source voltage in Figure 5-1 is assumed to remain sinusoidal during the fault, which is given by

$$\begin{cases} V_{as} = V_m \cos(\omega t) \\ V_{bs} = V_m \cos(\omega t - \frac{2}{3}\pi) \\ V_{cs} = V_m \cos(\omega t - \frac{4}{3}\pi) \end{cases} \tag{5-3}$$

where V_m is the amplitude of the phase voltage. For convenience, the clamping voltage V_{cap} is defined as in (5-4), where k is a constant ratio.

$$V_{cap} = k \cdot V_m \tag{5-4}$$

Mode 1 ($t_0 \le t < t_1$): Capacitor C_2 is charged by V_{as} and V_{bs} through the neutral short-circuit path and D_{bn} (Figure 5-2). The voltages across the inductors of Phase A and Phase B are respectively given by

$$\begin{cases} V_{La} = \dfrac{V_m}{2}[\sqrt{3}\cos(\omega t + \dfrac{\pi}{6}) - k] \\ V_{Lb} = -V_{La} \end{cases} \tag{5-5}$$

Mode 2 ($t_1 \le t < t_2$): All the three phases of the input source are feeding the capacitor C_2. Both D_{bn} and D_{cn} are conducting current. The voltages across the inductors are given by

$$\begin{cases} V_{La} = V_m[\cos(\omega t) - \dfrac{2}{3}k] \\ V_{Lb} = V_m[\cos(\omega t - \dfrac{2}{3}\pi) + \dfrac{1}{3}k] \\ V_{Lc} = V_m[\cos(\omega t - \dfrac{4}{3}\pi) + \dfrac{1}{3}k] \end{cases} \tag{5-6}$$

Mode 3 ($t_2 \le t < t_3$): Similarly to *Mode 1*, the capacitor is charged by Phase A and Phase C through D_{cn}. The inductor voltages can be obtained as

$$\begin{cases} V_{La} = \dfrac{V_m}{2}[\sqrt{3}\cos(\omega t - \dfrac{\pi}{6}) - k] \\ V_{Lc} = -V_{La} \end{cases} \tag{5-7}$$

The inductor volt-second balance condition can be applied to obtain,

$$\begin{cases} \Delta i_b = \dfrac{1}{L}\displaystyle\int_{t_0}^{t_2} V_{Lb}\,dt = 0 \\ \Delta i_c = \dfrac{1}{L}\displaystyle\int_{t_1}^{t_3} V_{Lc}\,dt = 0 \end{cases} \tag{5-8}$$

and considering the natural commutation characteristics of the diodes, the transition times for the operating modes can be found as (5-9), where T is the fundamental line cycle.

$$\begin{cases} t_1 = [\arccos(-\frac{1}{3}k) - \frac{2}{3}\pi]/\omega \\ t_0 = [\arccos(\frac{k}{\sqrt{3}}) - \frac{\pi}{6}]/\omega \quad (\text{when } I_a \text{ is discont.}) \\ t_3 - t_0 = \frac{T}{2} \quad (\text{when } I_a \text{ is discont.}) \end{cases} \tag{5-9}$$

Equations (5-8) and (5-9) indicate that the transition times are only a function of k for a given fundamental line frequency.

In equations (5-3) to (5-9), the correlation between the peak fault current and the input inductance is given by (5-10). The expression for the average power dissipation in the dc link is given by (5-11), with *f(k)* and *g(k)* representing functions of k. As seen above, both i_{peak} and P_{diss} are inversely proportional to inductance L.

$$i_{peak} = \frac{V_m}{L} f(k) \tag{5-10}$$

$$P_{diss} = \frac{{V_m}^2}{L} g(k) \tag{5-11}$$

Figure 5-8 and Figure 5-9 show the peak fault current and dc-link power dissipation under different input inductances and clamping voltages. A 400 Hz fundamental frequency is assumed in the analysis. As can be seen from these figures, higher input inductance and higher k always lead to lower peak fault currents and power dissipation. From this standpoint, the clamping voltage selection of the protection circuit should be as high as possible while meeting the component ratings. Figure 5-8 and Figure 5-9 also indicate that the fault current and power dissipation increase dramatically when the input inductance is low. In the real system the magnetic core of the inductors would normally

saturate during the fault worsening the results of the failure. In consequence, the voltage-clamping protection approach is deemed inappropriate for a converter system with low input inductance.

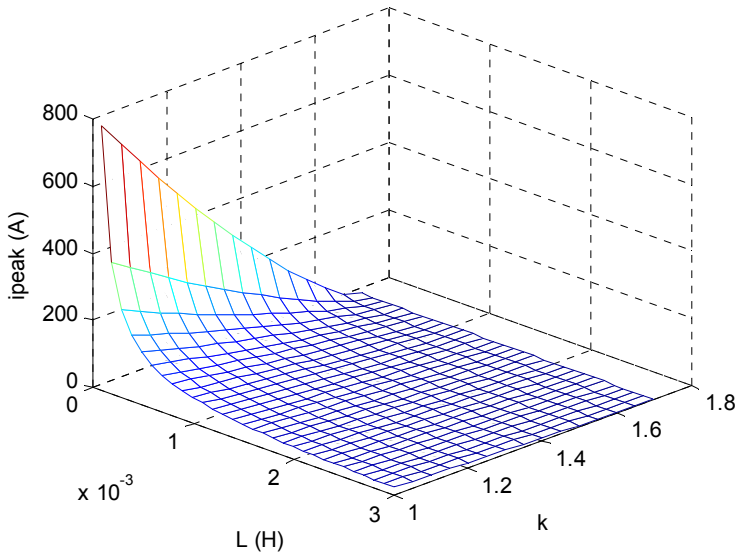


Figure 5-8 Impact of *L* and *k* on the peak fault current

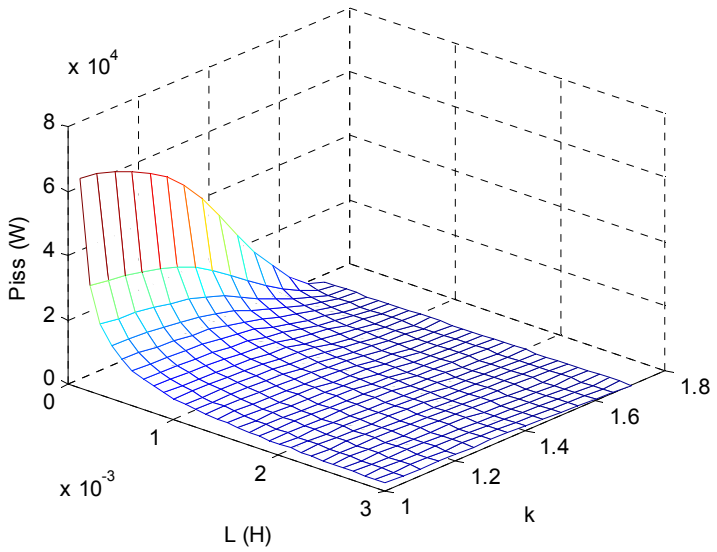


Figure 5-9 Impact of *L* and *k* on the dc-link power dissipation

C. Current Breaking Approach

The second approach to over-voltage protection is to add a current-breaking circuit in the charging loop, as shown in Figure 5-10. The additional current breaker Sw can be realized by semiconductor devices, such as a pair of IGBTs or MOSFETs. In normal operation Sw is always closed, but once the over-voltage across the capacitor is detected it opens immediately, interrupting the neutral charging loop path. Under this condition, the converter turns into a two-level diode bridge rectifier. Figure 5-11 shows simulation waveforms obtained with the current-breaking approach. These results show that the capacitors are over-charged and that the fault current is low compared to the voltage-clamping approach. Additionally, no energy absorption units are required in the dc-link during the fault. However, switch Sw is always connected in series with the neutral switches increasing the converter semiconductor losses.

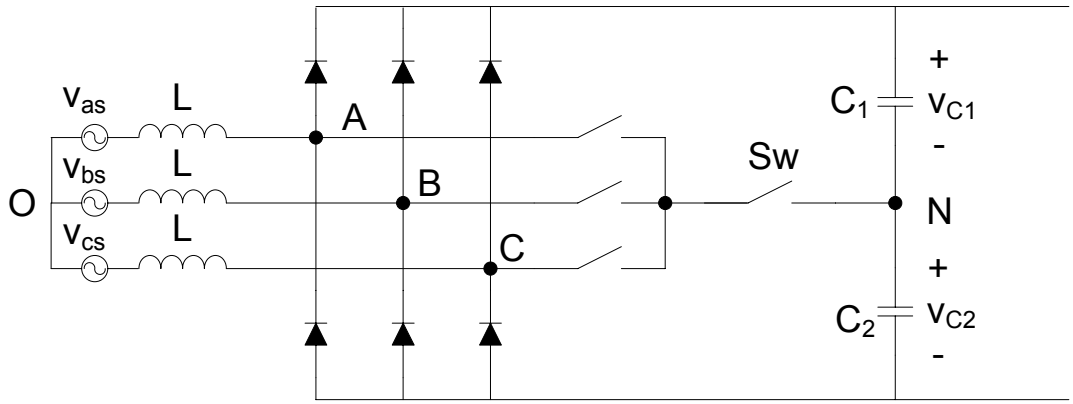


Figure 5-10 Circuit diagram for current breaking approach

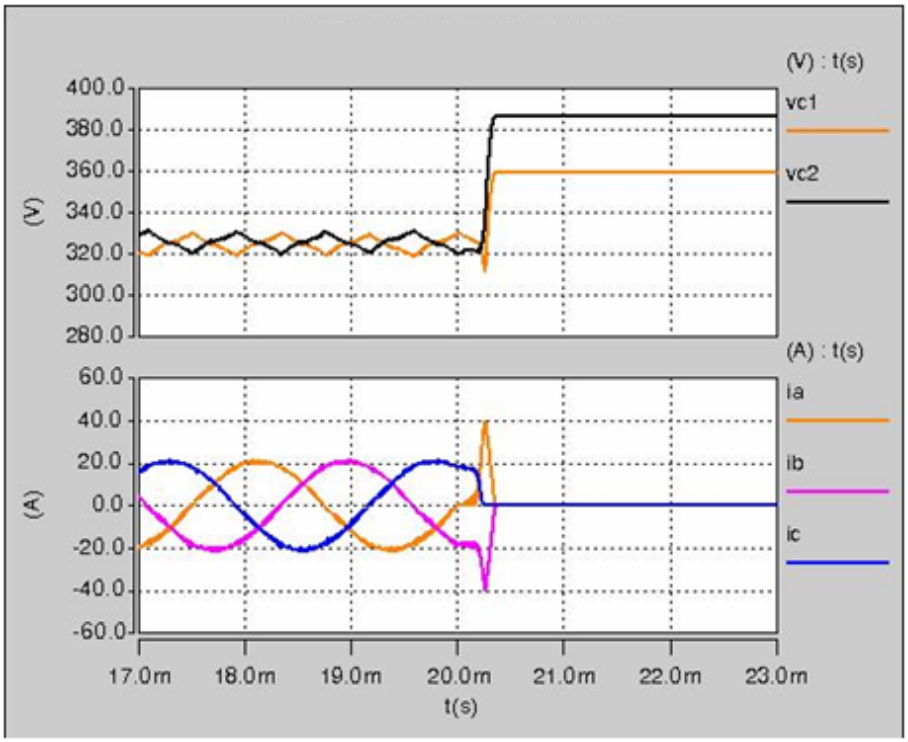


Figure 5-11 Simulation results for current breaking approach

5.2.3 Experimental Verification

In order to verify the analysis and the proposed protection approach, a scaled Vienna-type rectifier was built and tested. The circuit parameters are shown in Table 5-1. Due to the low input inductance the current-breaking protection approach is implemented. Figure 5-12 shows the results for the ac neutral switch short-circuit fault without any protection when the MOSFET in Phase A is shorted. The traces from top to bottom are: dc-link voltages V_{C1} and V_{C2}, rectifier input line-to-line voltage V_{ab}, and Phase A input current. Once a fault is detected, all the other switches in the converter are turned off while the dc-link load remains connected. The voltage across the dc-link capacitor increases from 45 V to 85 V (peak value) during the short circuit. If the load had been disconnected after the fault was detected, the peak voltage would have been even higher.

Figure 5-13 shows the experimental waveforms for the same fault under the current-breaking protection scheme. The protection signal is triggered by the over-current in this case. The results obtained show that both the peak voltage and the fault current are indeed reduced to within specified levels, verifying the effectiveness of the proposed protection scheme for non-regenerative three-level boost rectifiers.

Table 5-1 Parameters Used in Experiment

Source voltage	30 V_{rms}
Source frequency	400 Hz
DC link voltage	90 V
Switching frequency	40 kHz
Input inductance L	150 μH
DC link capacitor C	40 μF/each
Load resistance R	50 Ω

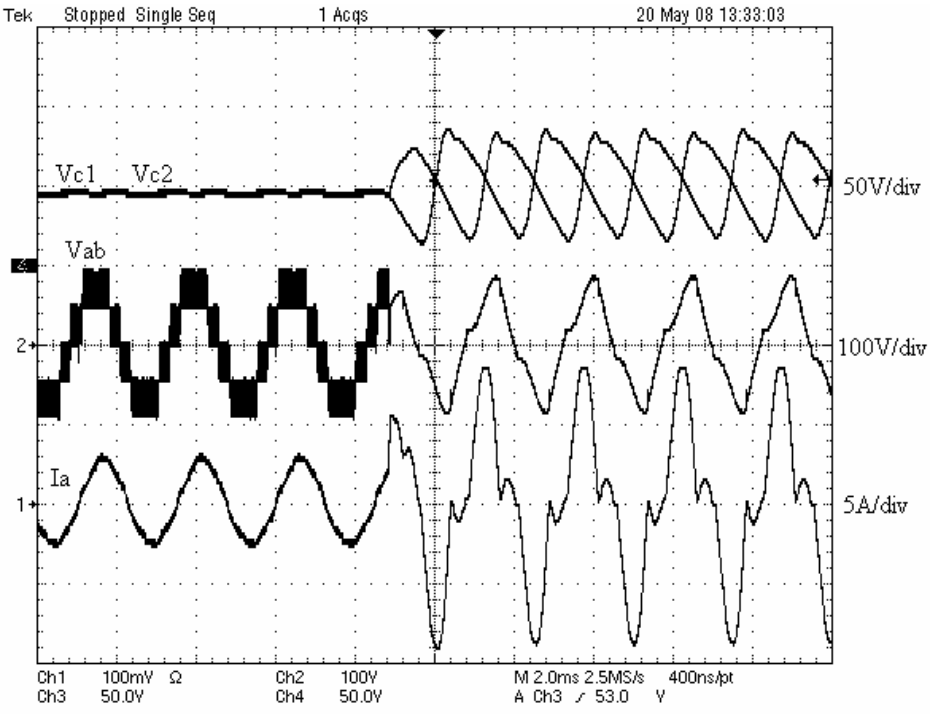


Figure 5-12 Experimental waveform neutral switch shorted failure without protection

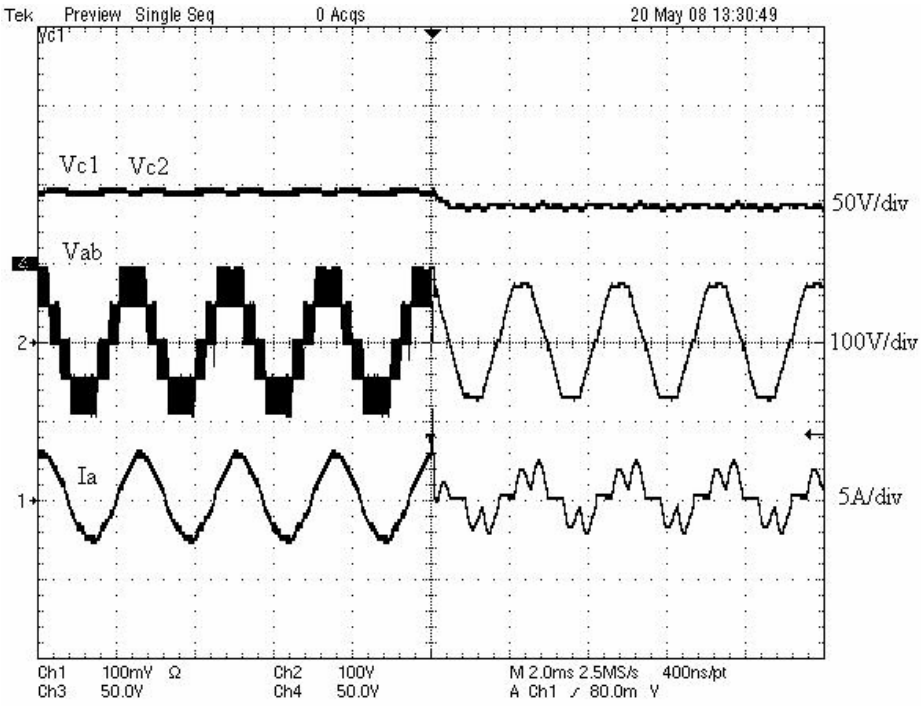


Figure 5-13 Experimental waveform neutral switch shorted failure with current breaking protection approach

5.3 Shoot-Through Failure and Protection

5.3.1 Proposed Protection Approach

The protection concept is presented in Figure 5-14. The key idea is to embed a fast response bi-directional switch into the dc-link capacitor tank. The protection circuit is highlighted by the dashed frame. The protection circuit consists of an IGBT (S_2), an anti-parallel diode (D_1), a relay (S_1) and a charging resistor (R_{cd}). The protection circuit is embedded into the neutral point between the two dc capacitors so that it will not impact the main power transmission through the positive and negative dc bus.

Usually the dc source side will have higher high frequency impedance compared to the dc capacitor tank due to the line inductance. For example, if the dc voltage is achieved

through bridge rectification as shown in Figure 5-14, the input inductor L will limit the current when the fault occurs. Therefore when the shoot-through occurs, most of the short-circuit current will have to go through the dc-link capacitor tank at the beginning instant. Then the embedded protection circuit can be used to detect and clear the fault.

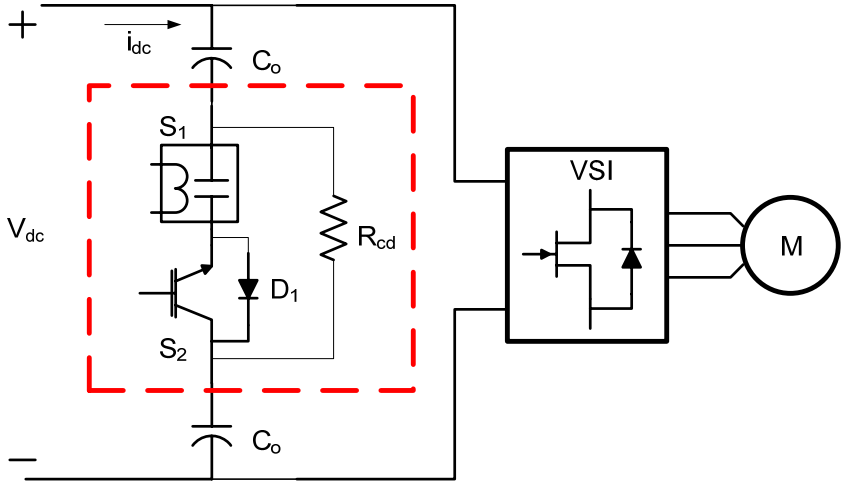
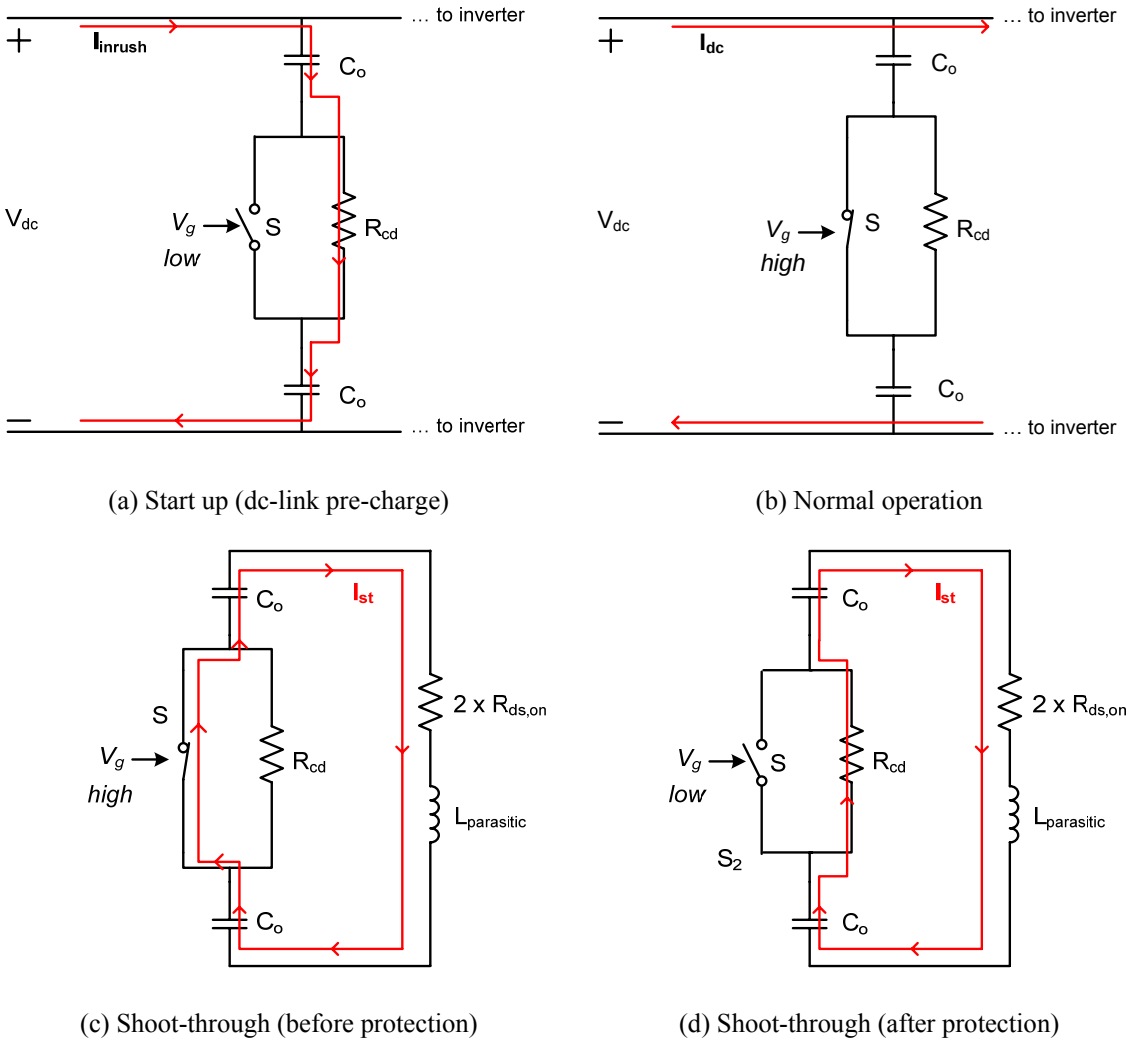


Figure 5-14 Proposed protection circuit

Figure 5-15 illustrates the circuit operation for different mode. For simplicity, switch S represents the combination of the relay and the IGBT. When the system starts up, the switch is open, and the dc-link capacitors are charged through the resistor R_{cd}. This stage is called dc-link pre-charge, as shown in Figure 5-15 (a). Once the dc link voltage is charged to the given value, the relay and the IGBT are controlled to be closed, as shown in Figure 5-15 (b). The main power will go through the positive and negative dc rails and the ripple energy will go through the capacitor-switch path. Both the IGBT and diode will conduct ripple current. Figure 5-15 (c) shows the situation for the fault case. R_{dson} represents the on resistance of the devices in the shorted phase leg, and $L_{parasitic}$ represents the short-circuit loop parasitic inductance. If a short circuit occurs in the inverter stage, the short-circuit current goes through the dc-link capacitors, the relay and the IGBT. The

IGBT exhibits a de-saturation feature above a certain collector current level, depending on the gate drive voltage. The collector-emitter voltage increases rapidly. Then the fault can be detected and cleared by the IGBT and its corresponding gate driver, regardless of what devices are implanted in the inverter bridge. Figure 5-15 (d) shows the circuit diagram after a fault is detected. The IGBT is open and therefore the short circuit current is limited by the charging resistor. In the meantime, a fault signal will be sent out to lock the active switches in the converter.



(a) Start up (dc-link pre-charge)

(b) Normal operation

(c) Shoot-through (before protection)

(d) Shoot-through (after protection)

Figure 5-15 Modes of operation

5.3.2 Gate Driver Circuit Design

In order to implement the protection concept, the gate drive voltage level for the IGBT has to be determined appropriately, and the corresponding gate driver circuit needs to be designed. Saturation current level and the conduction loss are the key factors for the gate drive voltage level selection. Usually lower gate drive voltage will lead to lower de-saturation current but it also leads to higher conduction loss. In terms of protection, the de-saturation current level can not be too high, or the devices in the shorted phase leg may be destroyed before the fault is cleared. On the other hand, under normal operation, the voltage drop across the collector and emitter of the IGBT should be as low as possible in order to minimize the conduction loss raised by the protection circuit itself. In most cases these two requirements have contradictory effects on the gate drive voltage level, so a tradeoff needs to be made in the practical design based on the system conditions and requirements.

The gate driver for the protection circuit has three functions: driving the IGBT, over-current detection and protection, and driving the coil of the relay. The first two functions are combined together in many commercial gate driver chips. However, the driving voltage for the relay coil might be different from the required IGBT gate drive voltage. On the other hand, it is desirable for the gate drive voltage of the IGBT to be adjustable, which means we can select the current protection level based on the system parameters.

In order to achieve all these functions with only one power supply, a gate driver circuit is proposed, as shown in Figure 5-16. The commercial gate driver IR21271 is utilized for the IGBT driving and protection, which is highlighted with the dashed frame. Other commercial gate drivers with the same function may be applied. Resistor R_1 and R_2 form

a voltage divider from which desired gate driving voltage can be achieved by changing the resistance ratio. The relationship between the gate-to-source voltage and the resistance is given by (5-12). V_g is the output voltage of the gate driver chip, which is determined by the supply voltage. A 12 V isolated power supply is utilized in this work.

$$V_{ge} = V_g \cdot \frac{R_2}{R_1 + R_2} \tag{5-12}$$

Since the IGBT is not switching during the normal operation, the resistance can be large and the gate driver loss can be very small. In order to increase the turn-off speed in the fault transient, Schottky diode D_2 is connected parallel to R_1. During the turn-off period, D_2 will bypass R_1, and the gate-to-source capacitor discharges only through the gate resistor R_g. D_3 is a Zener diode, which can help to constrain the voltage spike that occurs during the fault transient. D_4 is the free-wheeling diode for the relay winding. Under normal operation, both logic signals g_{neu} and error are high. Once a shoot-through is detected, the gate driver output will be locked and the error logic signal will appear low, which can be used to block all the other active switches and inform the control system.

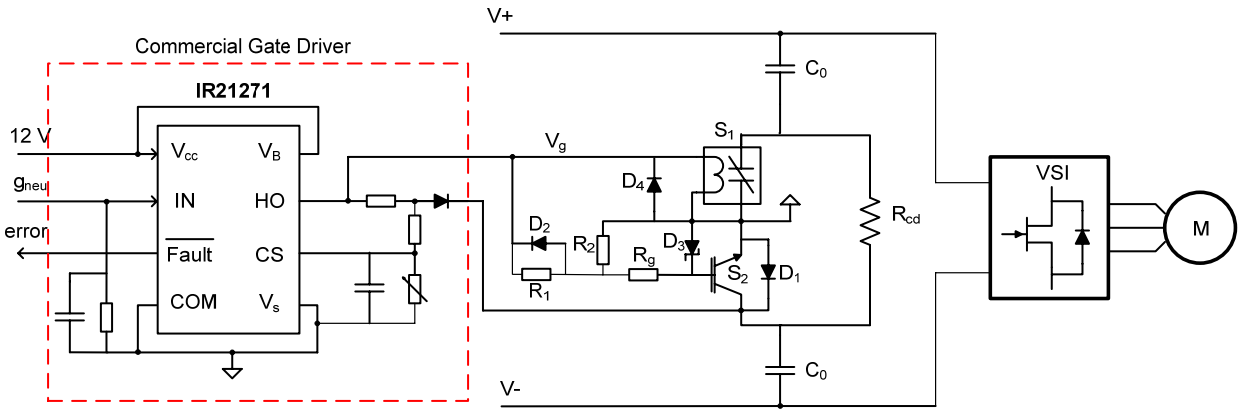


Figure 5-16 Gate driver circuit for protection

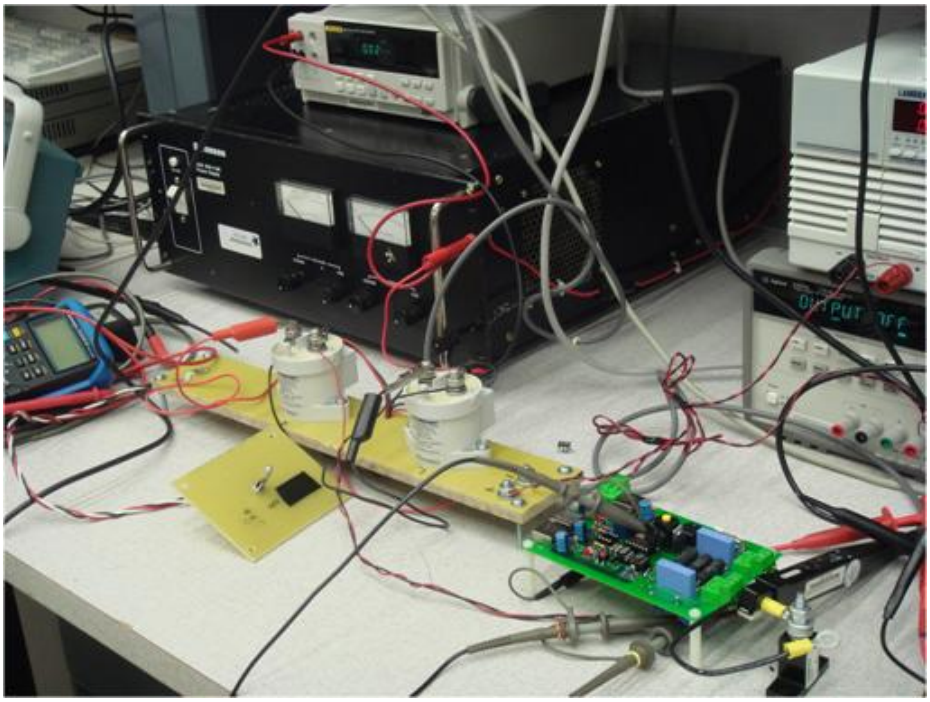


Figure 5-17 Experimental setup for shoot-through protection

5.3.3 Experiment Results

An experimental system was built to verify the protection concept and design. Figure 5-17 shows the experimental setup. The dc link capacitors are 40 μF each. The IGBT is IRG4BC20SD from International Rectifier. The gate driving voltage is selected to be 9.5 V, which leads to the de-saturation current level of 30 A. The driving voltage for the relay coil is 12 V. A MOSFET and a 0.1 μF decoupling capacitor are connected across the dc bus to emulate a shoot-through failure.

Figure 5-18 shows the experimental results for the dc link voltage of 300V. At instant t_1, the MOSFET is closed. It forms a short circuit with dc-link capacitor. The MOSFET drain current I_d starts to increase dramatically, and the drain-to-source voltage V_{ds} starts to drop. At the same time, the collector-emitter voltage of the IGBT starts to increase.

At instant t_2, the fault is detected by the gate driver chip. After about 240 ns, which is a built-in delay in the gate drive chip, the IGBT starts to turn off at t_3. At instant t_4, the MOSFET starts to turn off. The response delay of the MOSFET (t_4-t_2) is about 900 ns. This is mainly due to the propagation time of the gate driver chip and the peripheral optical couplers. As can be seen from Figure 5-18, the fault is clear in less than 1.2 µs. The semiconductor devices are protected from being destroyed by the over-current. Some oscillations are also seen in the MOSFET drain current during the transient. These are due to the resonance between the decoupling capacitor and the stray inductance in the short circuit loop.

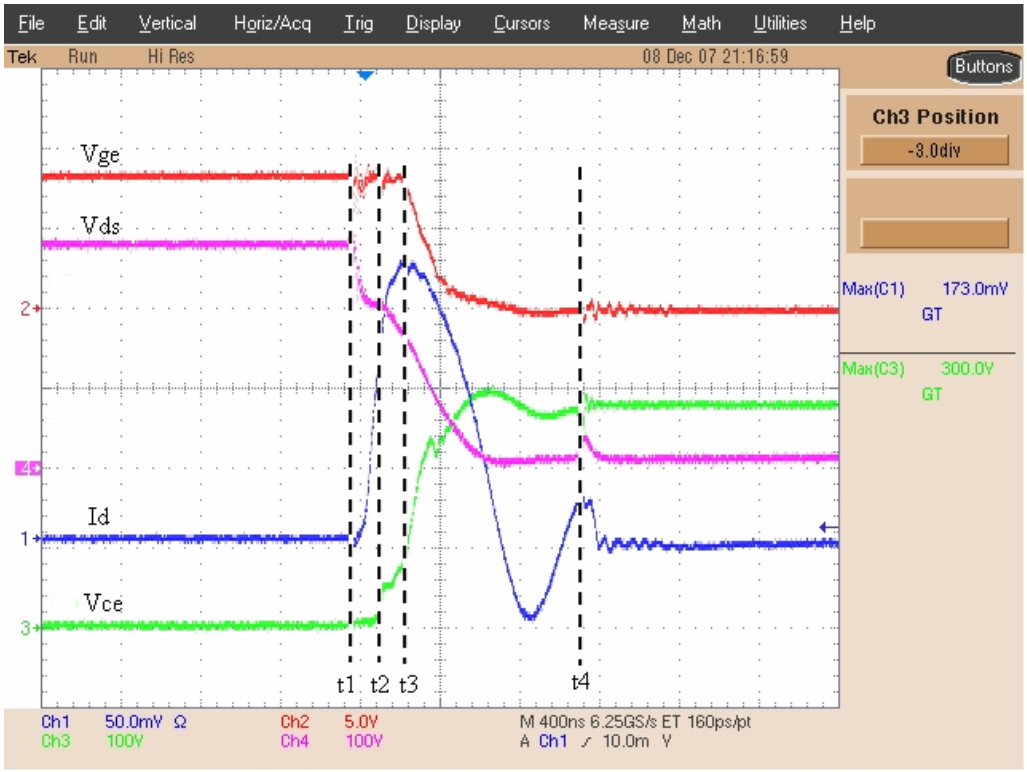


Figure 5-18 Experimental results: Traces from top to bottom: gate to source voltage of IGBT (Vge), drain to source voltage of MOSFET (Vds), drain current of MOSFET (Id) and collector to emitter voltage of IGBT (Vce)

5.4 Summary

In this chapter, an over-voltage failure mode of non-regenerative three-level boost rectifiers is identified, in which the dc-link voltage is seen to double when any of the ac neutral switches of the converter failed in short-circuit mode. Two protection approaches, voltage-clamping and current-breaking, have been thoroughly analyzed.

In voltage-clamping protection, both a resistor-based and a varistor-based clamping protection circuits were proposed, but the varistor-based circuit presented much better performance than the resistor-based circuit. The impact of the ac inductance and the clamping voltage chosen was studied carefully in this scheme. It was found that a higher clamping voltage always leads to a lower fault current and less power dissipation, indicating that the highest possible clamping voltage should be chosen within the safety margins of the converter capacitor and semiconductor devices. However, it was also found that the peak fault current and the power dissipation in the dc-link during vary inversely to the input inductance of the converter, which rules out this protection scheme for high power density applications with reduced input inductance. The current-breaking approach on the other hand, showed that it can lead to lower fault currents without any energy absorption components, at the expense of increased losses of the converter system during normal operation.

Consequently, the final choice of protection scheme needs to consider the converter operating conditions and specifications. All the above was verified through comprehensive analysis, simulations, and tests conducted with an experimental laboratory prototype. Finally, although the discussions in this work are based on Vienna-

type rectifiers, the results and conclusions apply as well to other three-level NPC converters.

A unique protection scheme for the shoot-through failure mode is also proposed in this chapter. A bidirectional switch, which is formed by an IGBT and a relay, is embedded into the dc capacitor tank to detect and clear the fault occurs in the converter bridge. The proposed protection scheme did not rely on the characteristics of the semiconductor devices in the converter. Therefore it can be used to protect against shoot-through failure in the converter system built with SiC JFETs. The circuit design for the gate driver is also presented. With the proposed circuit, different driving functions can be achieved by using only one isolated power supply, which help to minimize the size and the cost of the protection circuit. The experiments carried out verify the feasibility of the proposed approach. The shoot-through fault is clear in less than 1.2 μs, and the device in the bridge is protected from being destroyed.

Chapter 6 Hardware Development and Experiments

This chapter presents the hardware development for a 10 kW three-phase ac-ac converter with the metric of high weight density. SiC JFETs and SiC Schottky diodes are selected for the power stage in order to achieve high power and high switching frequency. Based on the topology analysis in Chapter 3, a Vienna-type rectifier plus a voltage source inverter is chosen for the hardware system. All the concept and technologies developed and described in previous chapters, including filter design, control approach and protection schemes, are implemented and verified in this hardware system. The hardware design, construction and test results are described in details. At the end of this chapter, the weight breakdown of the hardware system is analyzed and compared to the paper design.

6.1 System Configuration and Interface

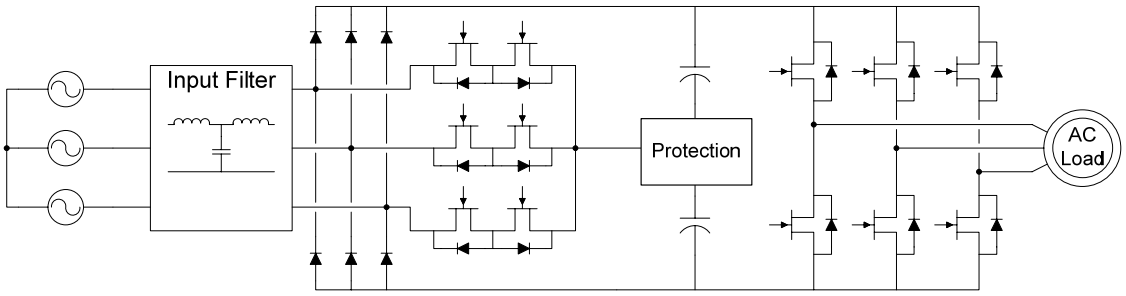


Figure 6-1 Hardware system circuit diagram

Figure 6-1 shows the circuit diagram for the hardware system. The input filter block represents the multi-stage three-phase LC filter. The protection circuit embedded in the dc-link includes the neutral blocking protection for the voltage doubling failure and the shoot-through protection for the SiC JFET inverter, which are discussed in the previous

chapter. The hardware system is classified into the following sub-systems according to the functions and layout considerations:

(1) Phase leg modules, which include all the switching devices and the corresponding gate drive, decoupling capacitors and heatsink. A compact circuit layout design is normally required for this part in order to reduce the parasitic inductance and then avoid high peak voltage stress during the switch transition. On the other hand, good noise immunity is also desired; especially for the gate drive circuit, to prevent faulty operation of the gate drive signal.

(2) DC bus board, which provides the planar dc bus structure and the connection interface for the phase modules and protection circuits. The voltage and current sensors and the corresponding processing circuits are also included on this board.

(3) Input filter, which combines the functions of boost inductor and EMI suppression.

(4) Digital controller, which consists of analog to digital conversion, DSP and FPGA for control implementation. The control system also includes the auxiliary power supplies for the control circuits.

Figure 6-2 shows the interface of the system. Converter power stage represents the combination of the phase leg modules, dc bus board and the input filter. The hardware system terminals include a three-phase main power input, a 28 V control power input, a three-phase variable frequency output, and external control buttons. The interconnections between the controller and the converter power stage include the analog sensor signals (10 channels for the full system), the error signal generated by the shoot-through detection, the 24 V power supply for the gate driver and the gate drive signals (9 channels, 3 for the rectifier and 6 for the inverter).

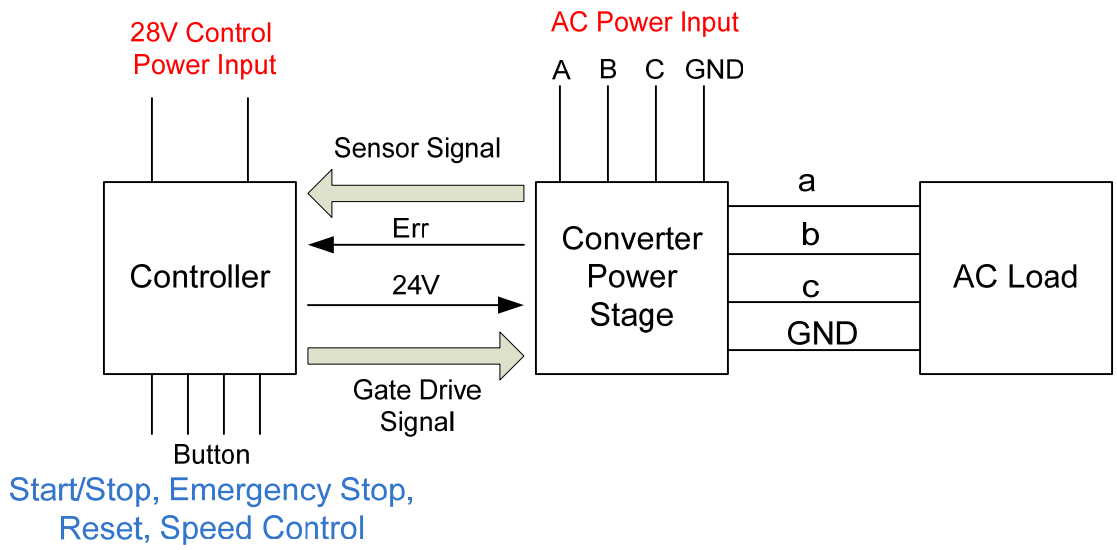


Figure 6-2 Hardware system interface

6.2 Hardware Design and Construction

6.2.1 Digital Controller

A previously developed DSP (ADSP-21160) and FPGA (XILINX-XCV400) based universal controller is chosen for the control function implementation. Two analog-to-digital converters AD7864 are included in this controller, which provides 8 channels of analog-to-digital conversion. However, a total of 10 channels analog signals are required to be processed for the full system. In addition, the calculation capability of the universal controller cannot support the high speed operation for the full system. Therefore two universal controllers are utilized at the same time to control the rectifier and inverter separately. An interface board is built to provide the necessary interconnection functions, which include the power management for the controller system, the button signal isolation, sensor signal fault detection, logic protection and signal buffering. The structure of the controller is shown in Figure 6-3.

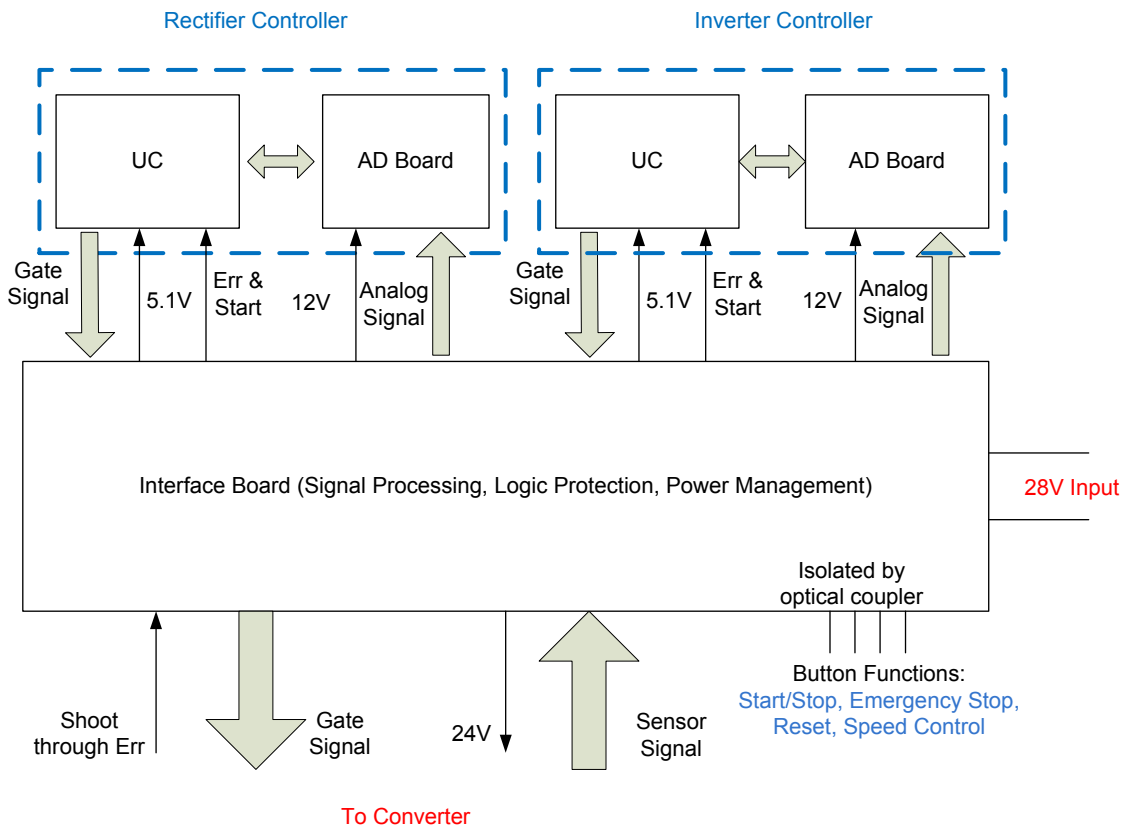


Figure 6-3 Structure of the controller

6.2.2 DC Bus Board

The dc bus board is the key interface for all the power components, which is highlighted with the solid frame in Figure 6-4. The dash frames in this figure represent the connectors for the inverter and rectifier phase leg modules. As can be seen, the dc bus board includes the over voltage protection, shoot-through protection and all the sensor circuits. The dc bus board is designed into a ring shape, which makes it suitable to be integrated with a motor.

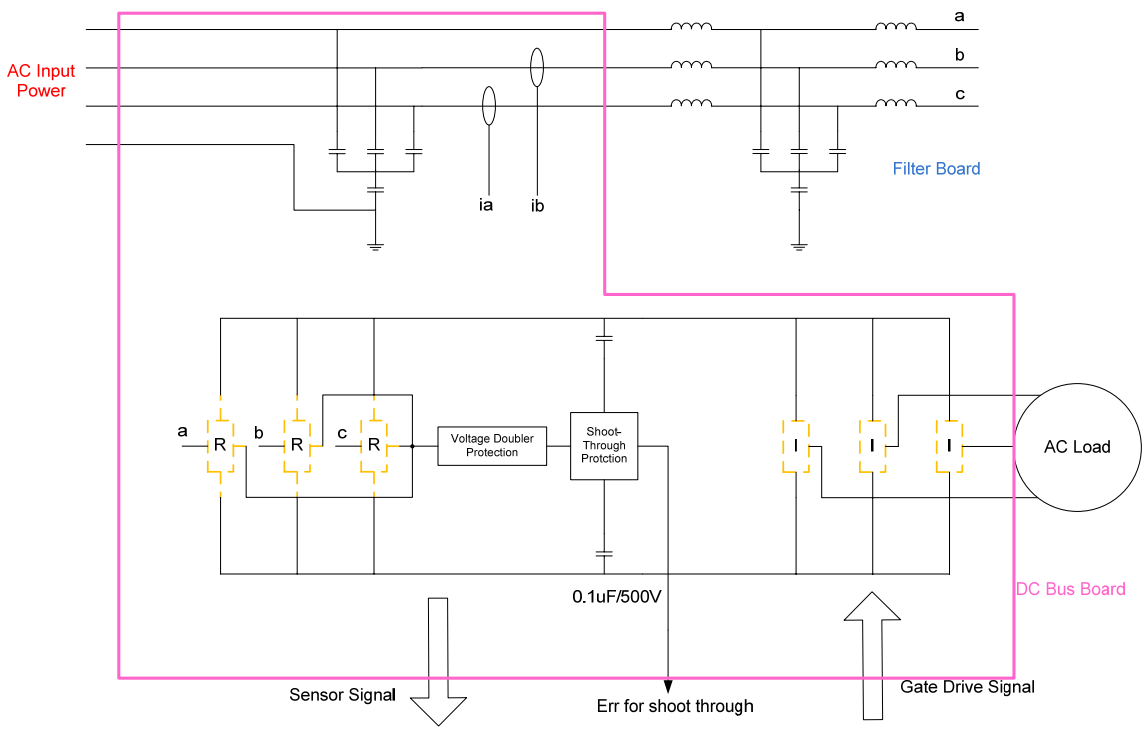


Figure 6-4 Diagram of the dc bus board

The circuit diagram for the protection is shown in Figure 6-5. The IGBT for the shoot-through detection is IRG4BC20SD from International Rectifier, which features a saturation current of 35 A at 10 V gate drive voltage. With the current level the JFET in the inverter phase leg should be safe even in a shoot-through condition if the fault only last for a short while. For the neutral blocking circuit, a CoolMOS power transistor IPW60R045CP from Infineon is selected since it has very low on resistance (0.045 Ω at 25 ºC).

In this design the dc-link capacitance is very small, therefore a film capacitor is utilized for energy storage instead of electrolytic capacitors in order to achieve better reliability and lifetime. The MKP series dc capacitors from EPCOS are selected with the rated value of 35 µF/450 V. In addition, some 10 nF/1000 V ceramic capacitors are also connected to the dc bus for decoupling purpose.

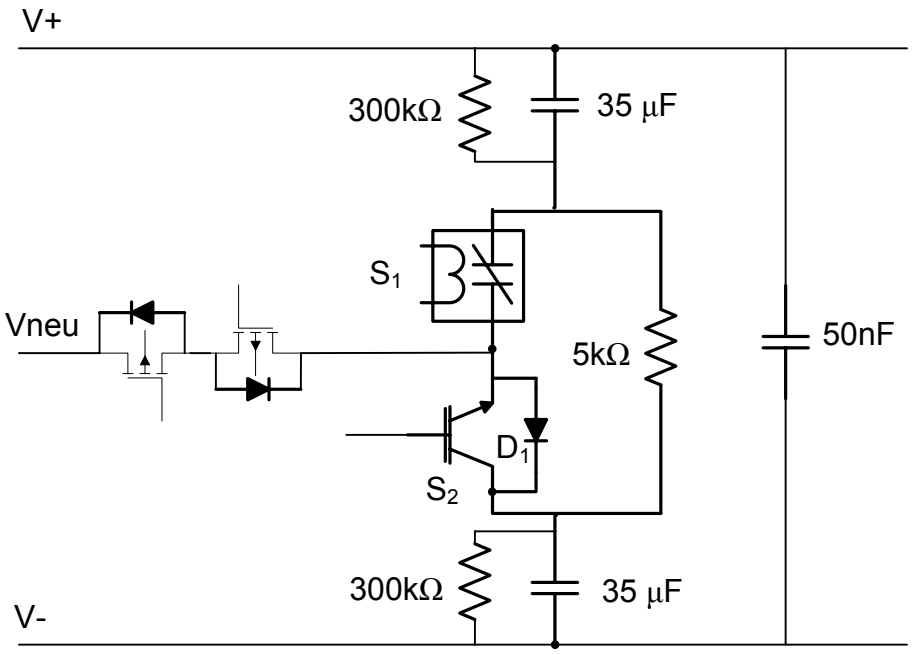


Figure 6-5 Circuit diagram of the dc bus including protection

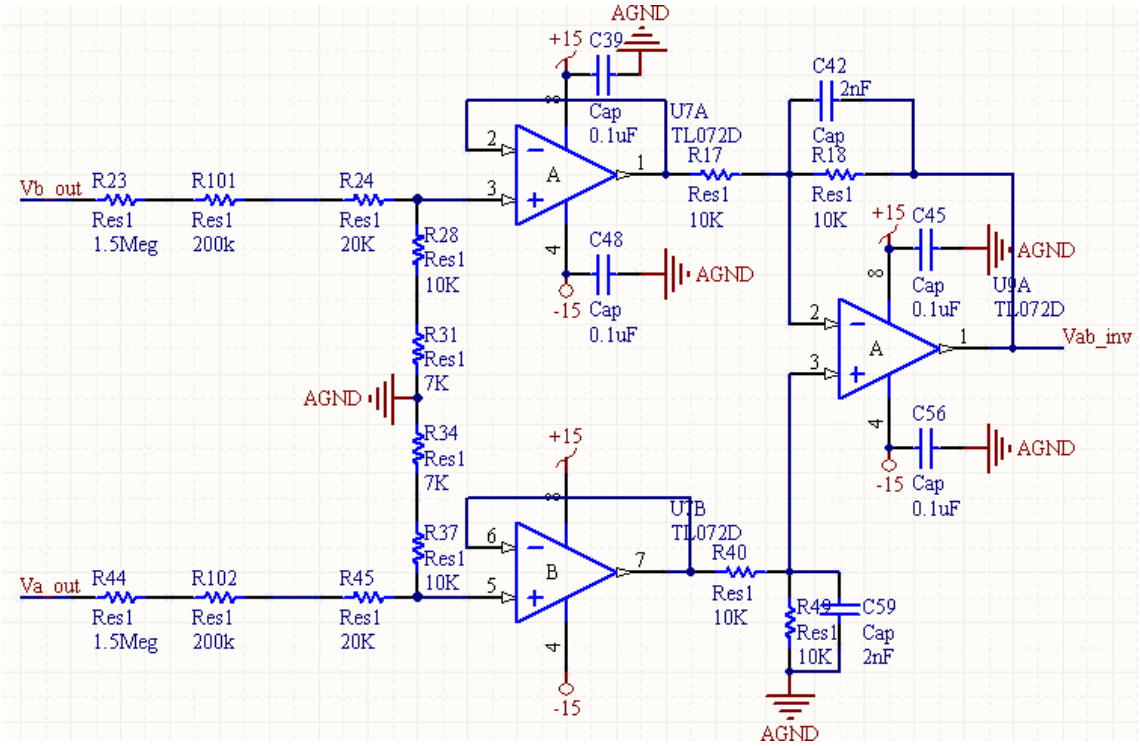


Figure 6-6 Voltage sensing circuit

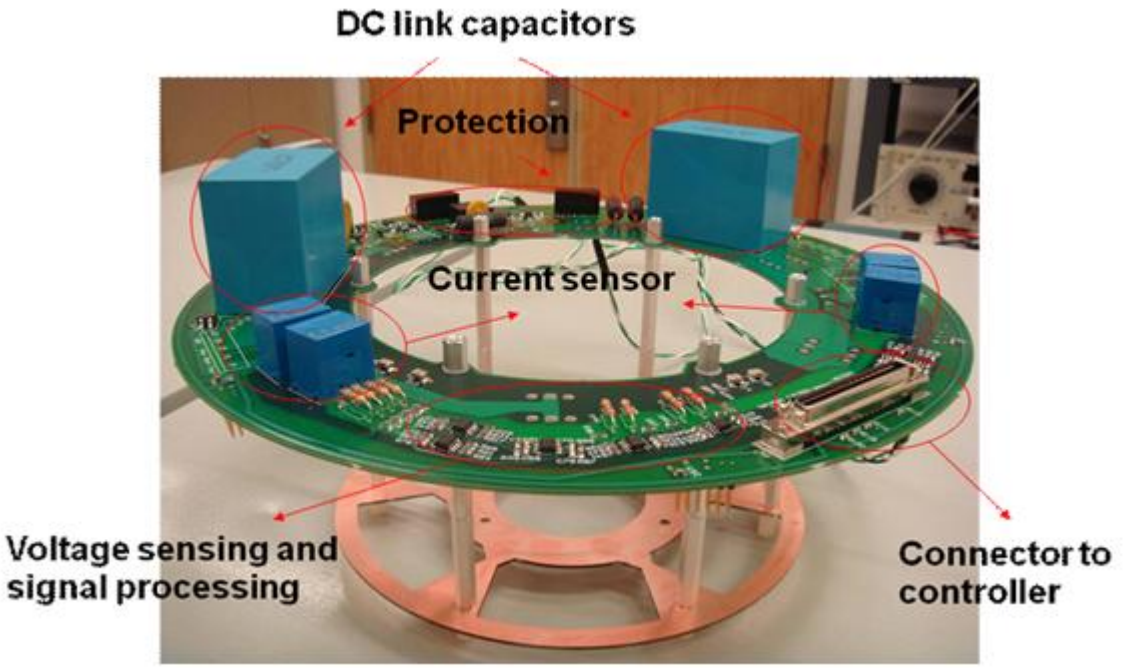


Figure 6-7 Physical structure of the dc bus board

The dc bus board includes 10 sensing signals: 2 channels for input current, 2 for output current, 2 for input voltage, 2 for output voltage and 2 for dc link voltage. Sensor HX 15-P from LEM is utilized for the input and output current sensing. For the voltage measurement, non-isolated operational amplifiers are utilized to achieve low profile and good performance. Figure 6-6 shows the measurement circuit for inverter output voltage V_{ab}. The physical layout of the dc bus board is shown in Figure 6-7.

6.2.3 Input Filter

Based on the discussion in Chapter 2, the input filter structure and the corresponding parameters are designed as shown in Figure 6-8. A customized nanocrystalline toroid core is selected for the common mode choke. In physical design the peak current is 25 A and the maximum durable flux density is 0.84 T. The design parameters are shown in

Table 6-1. C_X is the film capacitor from EPCOS and C_Y is the ceramic capacitor from Panasonic. Figure 6-9 shows the physical structure of the input filter.

Table 6-1 Physical Parameters for the CM Choke

Outer Diameter	Inner Diameter	Height	Number of Turns
6.2 cm	4.8 cm	1.1 cm	48 for the first two stages 30 for the last stage

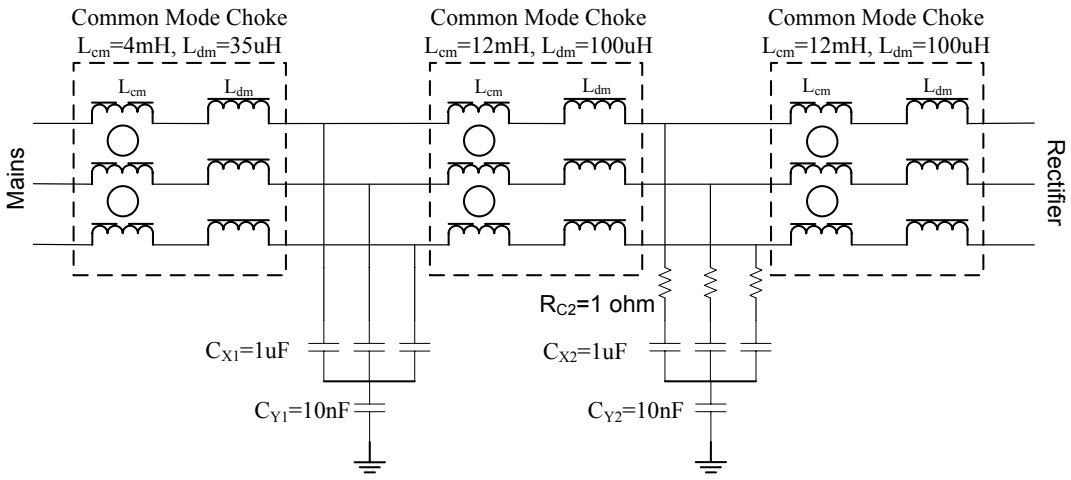


Figure 6-8 Circuit diagram of the input filter

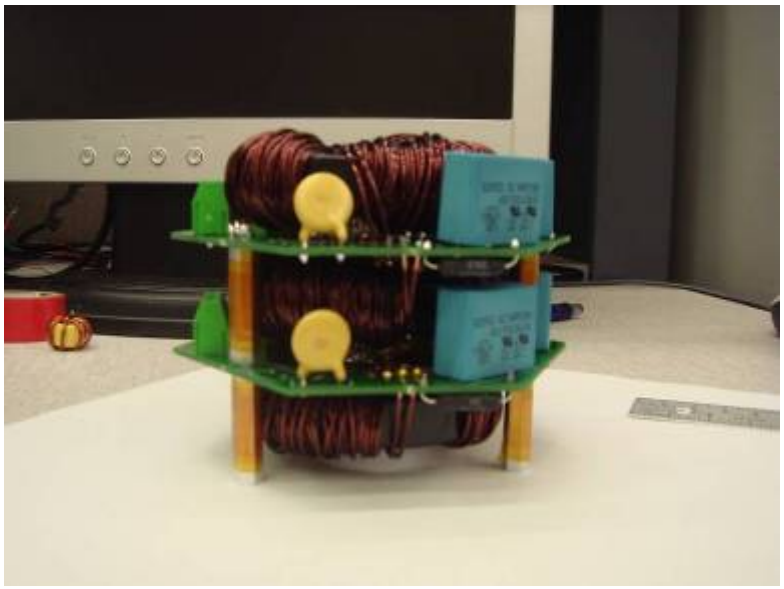


Figure 6-9 Physical structure of the input filter

6.2.4 Phase Leg Module and Gate Drive

The combination of the SiC JFET from SiCED and the SiC Schottky diode from Cree forms the power stage of the converter. Due to the limited JFET die size (2.4 mm by 2.4 mm) the parallel structure is implemented for the phase leg construction to achieve a high current capability. The number of devices in parallel is determined by the power rating. Figure 6-10 shows the circuit diagram of the rectifier phase leg. Two JFETs are connected in parallel for the neural switching cell. 1200 V/20 A SiC diodes are selected for D_1 and D_2 while 1200 V/10 A diodes are chosen for D_3 and D_4. The circuit diagram for the inverter is shown in Figure 6-11. The switching cell in inverter phase leg consists of three JFETs and one 1200 V/10 A diode.

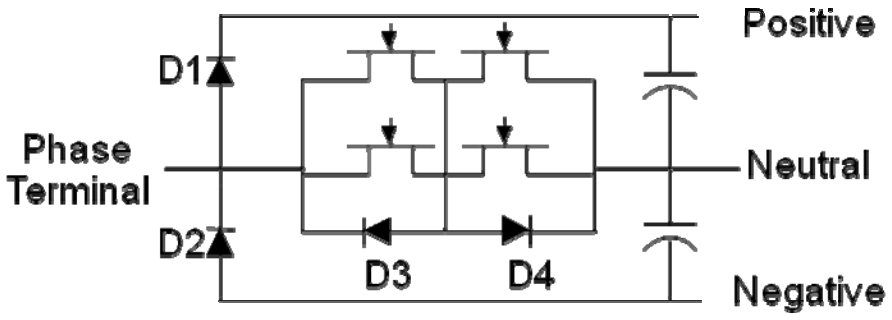


Figure 6-10 Rectifier phase leg

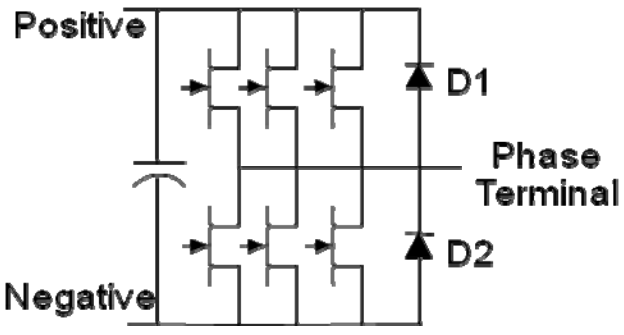


Figure 6-11 Inverter phase leg

SiC JFET is a normally-on device and a negative gate to source voltage is required to turn it off. In addition, the pinch-off voltage as well as the breakdown voltage is device and temperature dependent [104], and the tolerable voltage window between these two values is very narrow. In this hardware system a "RCD" gate driver circuit [104] is implemented to cope with the large variability in the gate characteristics. With this circuit the JFET gate can operate in avalanche without damage. Other than the special requirements of the JFET device, a short signal propagation delay-time, a good edge shape and a good common-mode transient immunity are necessary for the gate driver of a high switching frequency converter. In order to meet these demands, a digital isolator ADuM5241 and a high speed high current gate driver IXDN409 are used. ADuM5241 offers the high common-mode transient immunity of 25 kV/μs. This characteristic is particularly important for the SiC converter due to the fast turn-on and turn-off times. Figure 6-12 shows the gate driver circuit. As can be seen, the devices in parallel share the same driver chip. But each of them has their own gate resistor and RCD network, which can compensate for the gate parameters variation from device to device.

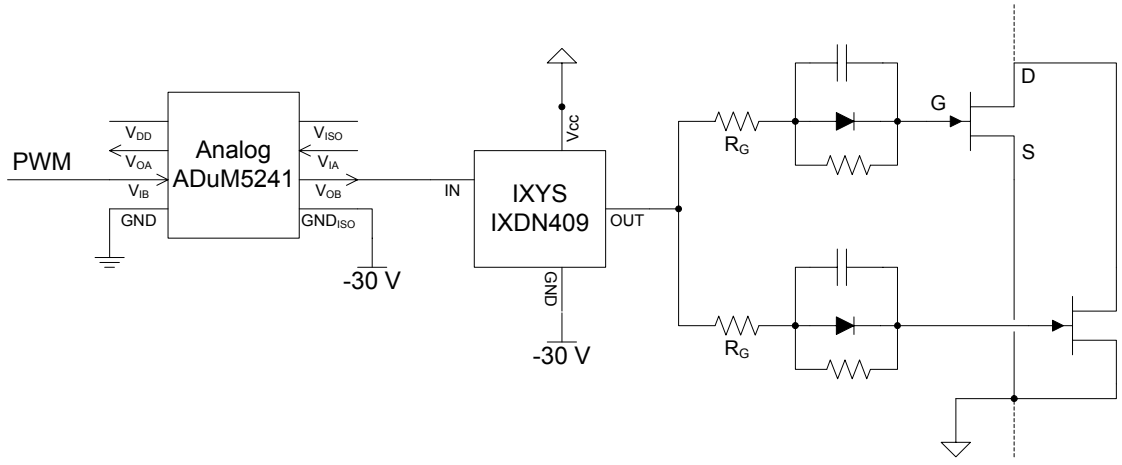


Figure 6-12 Gate driver circuit

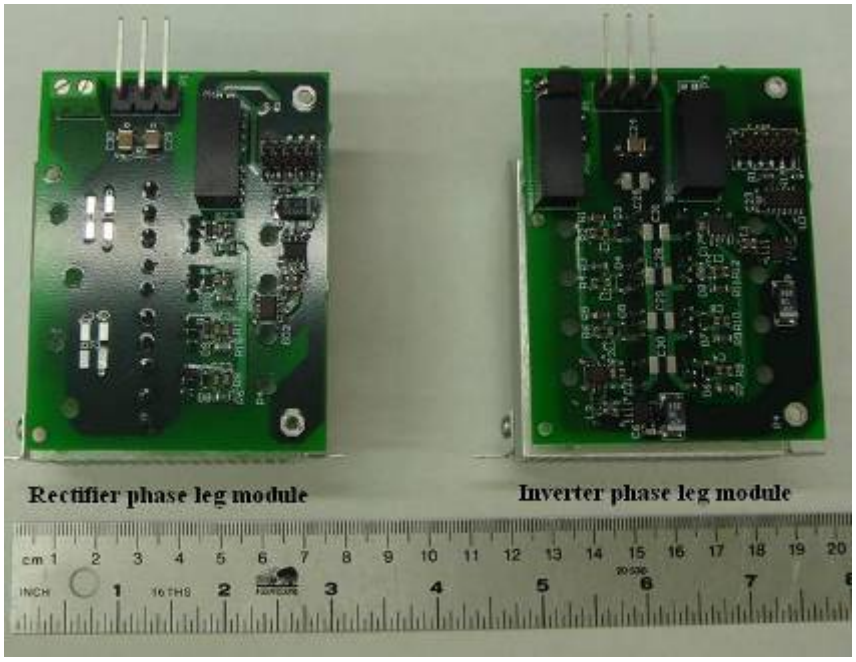


Figure 6-13 Phase leg modules

Figure 6-13 shows the physical structure of the phase leg modules. The gate driver board is directly mounted on top of the semiconductor devices. In order to verify the circuit functions, the phase leg modules are tested as a buck converter with resistor and inductor load. Figure 6-14 shows the test circuit for the inverter phase leg. The top switch is operating with a constant duty cycle while the gate of the bottom switch is always negative biased.

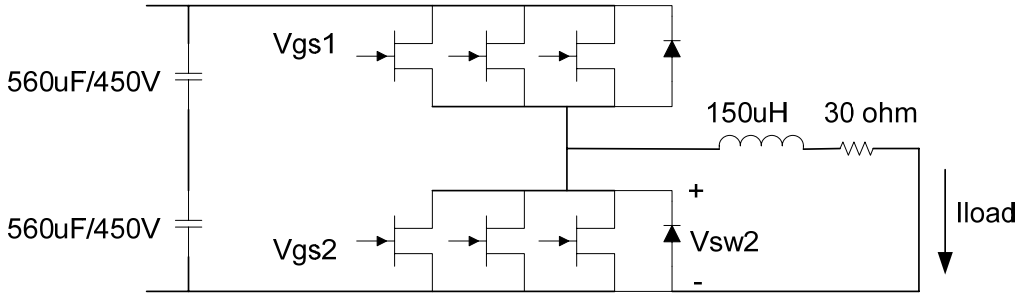


Figure 6-14 Test circuit for the inverter phase leg

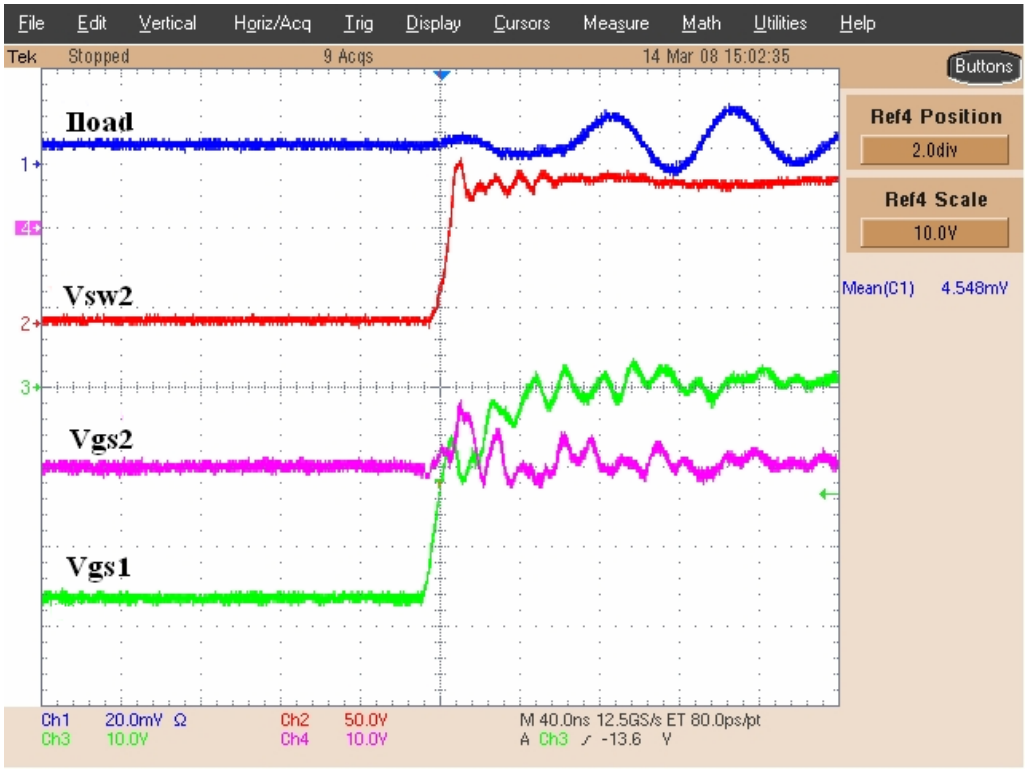


Figure 6-15 Waveforms of top switch turn on

Figure 6-15 shows the test results when the dc-link voltage is 80 V. A high voltage peak is observed in Vgs2 during the turn on transient of the top switch, which indicates a strong cross coupling between the top and bottom switch. This is due to the Miller capacitors. When the top switch turns on, the voltage across the bottom switch increases rapidly. A current will be induced via the Miller capacitor and then injected into the gate drive circuit. Since the impedance of the gate driver is not zero, a voltage peak will be generated. This voltage peak could falsely turn on the bottom switch and then lead to a shoot-through fault. A 1.5 nF capacitor is connected to the gate and source terminal in order to suppress the voltage peak.

Figure 6-16 and Figure 6-17 show the turn-on and turn-off waveforms at 600 V_{dc} with the additional gate-to-source capacitor. The turn-on time and turn-off time are about 60 ns. The voltage peak is less than 3 V, which is much less than the previous case. For the

rectifier phase leg module the cross coupling is not a concern since there is only one active switching cell in each bridge.

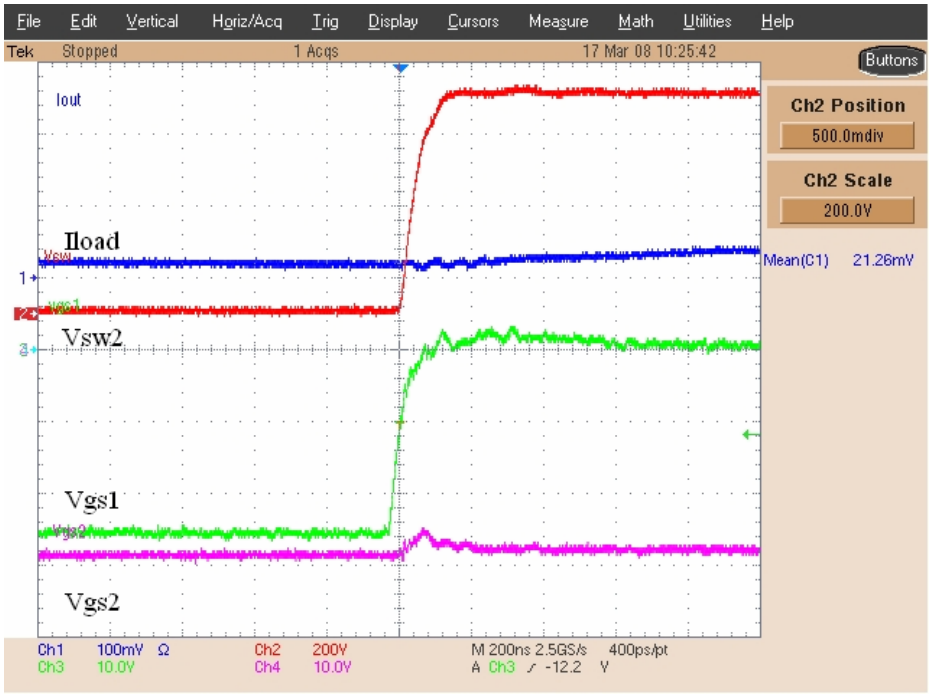


Figure 6-16 Waveforms of top switch turn on with additional 1.5 nF capacitor

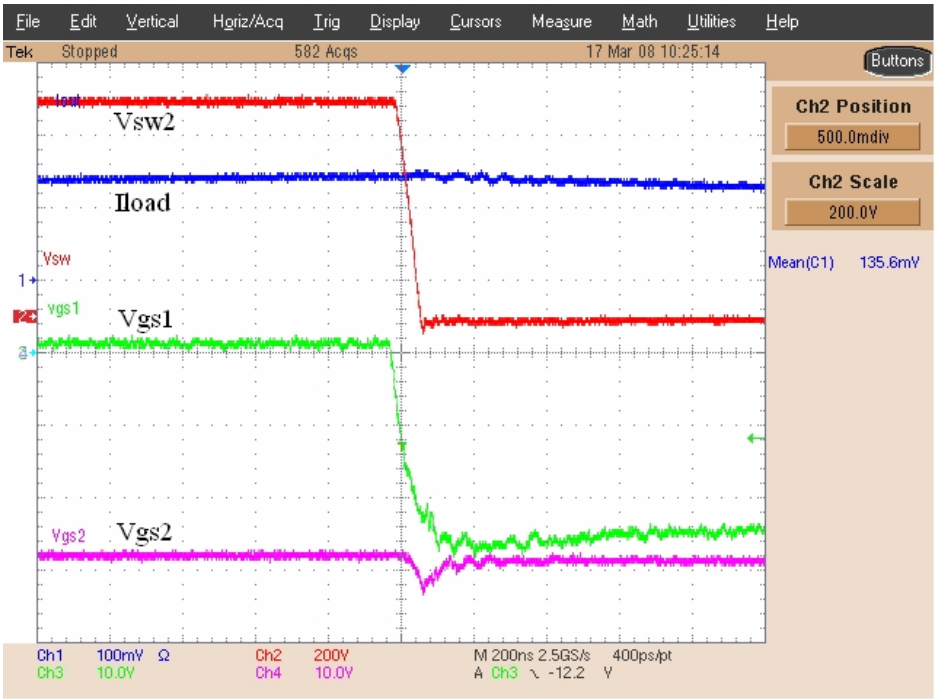


Figure 6-17 Waveforms of top switch turn off with additional 1.5 nF capacitor

6.2.5 SiC JFET Characterization

Because the SiC JFET is not fully commercialized, a full datasheet is not available. In this section the characterization results for on-resistance, switching energy and junction-to-case thermal impedance are shown since they are essential to the loss calculation and thermal design for the converter system.

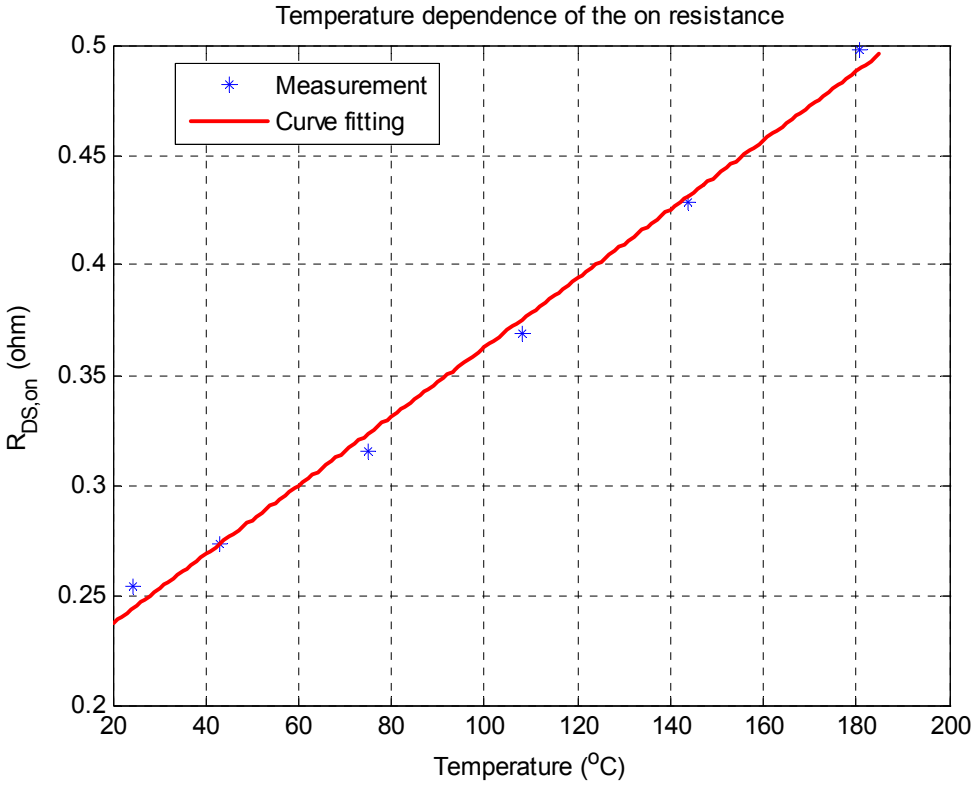


Figure 6-18 $R_{DS,on}$ versus temperature

Table 6-2 Switching energy under different conditions (@ 25°C)

Test Condition	Switch On (μJ)	Switch Off (μJ)
150 Vdc, 5 A	18.9	13.4
300 Vdc, 5A	53.9	31.0
450 Vdc, 5 A	93.3	48.3
600 Vdc, 5 A	143.9	69.2

Figure 6-18 shows the measured device on-resistance versus the temperature. As can be seen, the relationship is almost linear. The switching energy is achieved by double pulse test using the proposed gate drive circuit. Table 6-2 shows the test results under different conditions. In order to measure the junction-to-case thermal impedance, a 1.5 V dc voltage is applied to the device. At steady state the drain current (I_D) is 3.888 A with the case temperature (T_{case}) of 99 °C. The on-resistance is 0.385 Ω. Based on Figure 6-18, the junction temperature (T_j) is 114.3 °C. Then the junction-to-case thermal resistance can be obtained as (6-1), where V_{DS} is the drain to source voltage.

$$R_{th,j-c} = \frac{T_j - T_{case}}{V_{DS} \cdot I_D} = 2.6\,^{o}C/W \tag{6-1}$$

6.3 System Assembly and Test

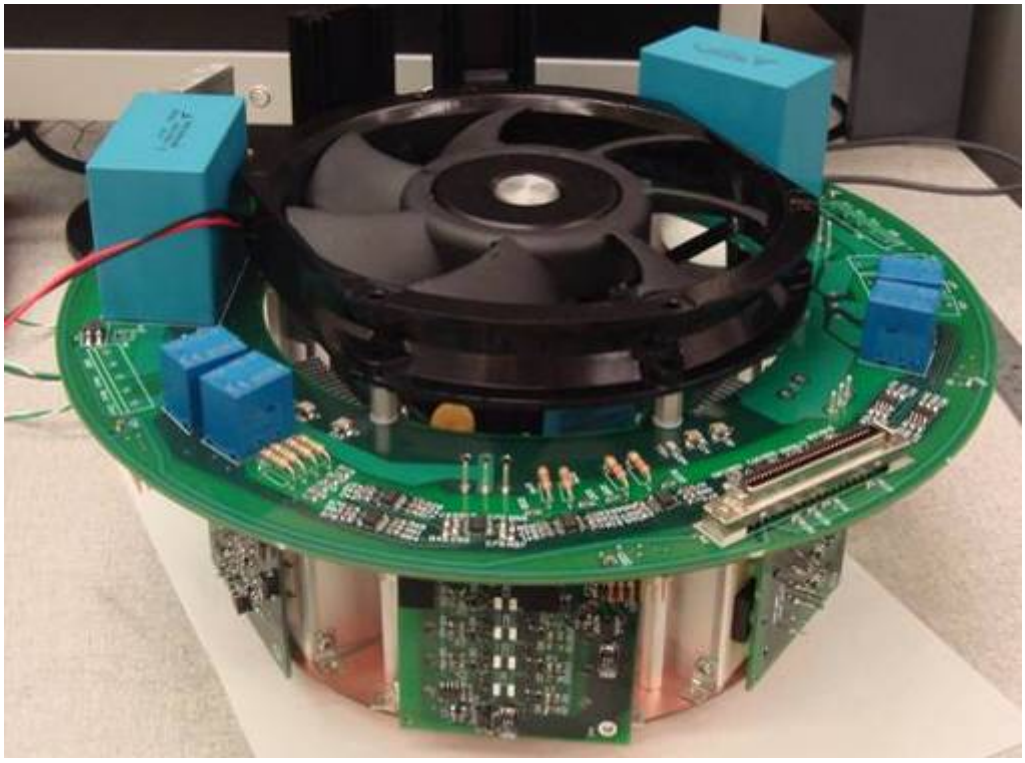


Figure 6-19 System assembling

6.3.1 System Assembly

The six phase-leg modules and the input filter are mounted on a baseplate and then the dc bus board is connected to the modules via solder, as shown in Figure 6-19. The two universal controllers and the interface board are assembled in a control box. A 68-pin mini delta ribbon (MDR) cable is used to connect the control box and the dc bus board.

6.3.2 Controller Structure and Start-up Sequence

As mentioned in the previous chapter, the DSP/FPGA based controller is used for the control approach implementation. The FPGA is the interface between the peripheral I/O and the DSP. The AD data and button status are stored in the registers of the FPGA. The FPGA also realizes the modulation function for the gate signals and generates the interruption signal which indicates the starting point of a new switching cycle. Once the DSP detects the interruption signal, it will update all the feedback signals via the corresponding registers and then carry out the control calculation. When the calculation is done, the duty cycle will be sent to the FPGA and then translated into the gate drive pulse signal. Figure 6-20 shows the structure of the controller.

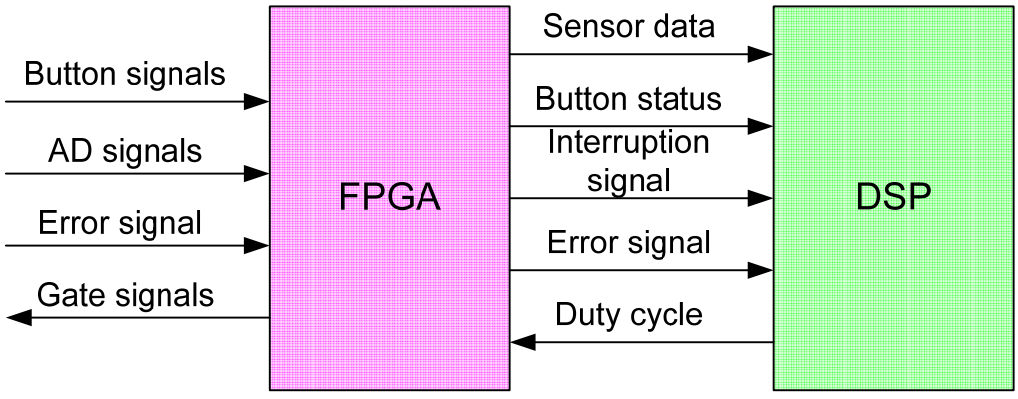


Figure 6-20 Controller structure

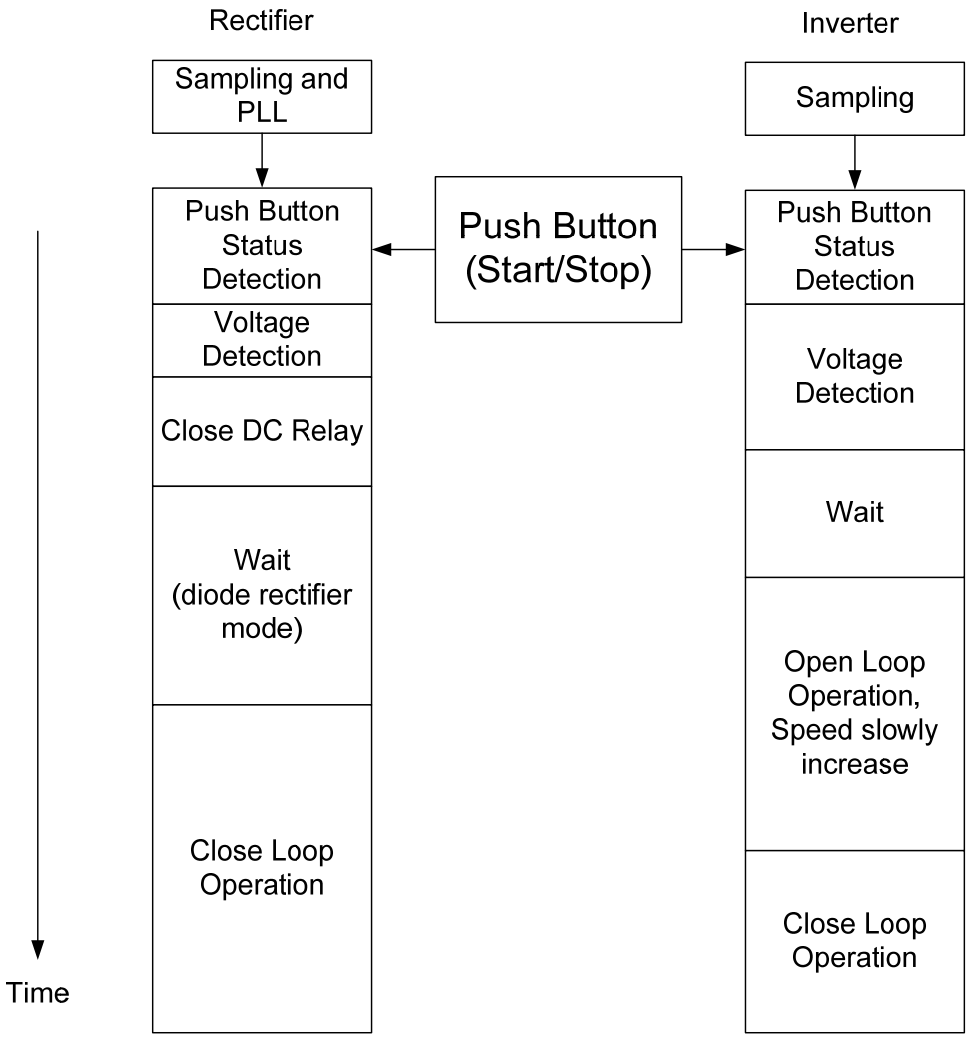


Figure 6-21 Start-up sequence

Since the Vienna-type rectifier is non-regenerative, it cannot start from a zero load condition. Therefore in the experimental system a special start-up sequence is utilized, as shown in Figure 6-21. The controllers for both rectifier and inverter are running at iteration mode for sampling and button status detection. Once the start button is pushed, the rectifier controller compares the current dc-link voltage with the given threshold value. If the dc-link voltage is higher the dc-relay will be close. At the same time the inverter will wait until the relay is totally close, which usually take tens of ms. After the waiting period the inverter runs at open loop control mode to start the motor while the

rectifier runs as a diode bridge. When the inverter runs to a certain power level, the rectifier starts running at active mode and regulates the dc bus voltage to the reference value. Then, the inverter starts the close-loop control. Figure 6-22 shows the experimental waveforms for the startup period. The traces from top to bottom are: dc-link voltages, rectifier input current and inverter output current.

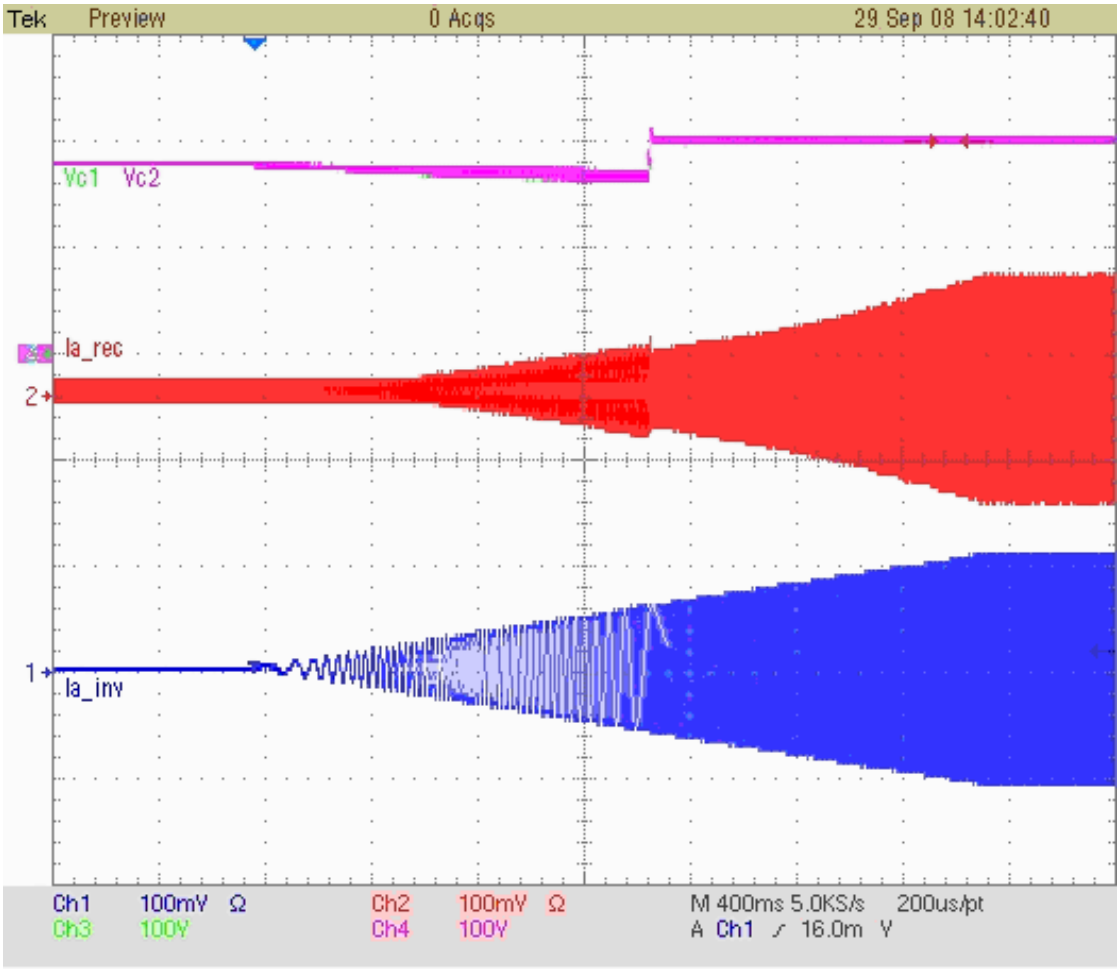


Figure 6-22 System start-up transient waveforms

6.3.3 Experimental Results

Table 6-3 shows the circuit parameters for the experiments. The steady state experimental waveforms are shown in Figure 6-23. The traces from top to bottom are: dc-

link voltages, input source current and inverter output current. As can be seen, the dc-link voltage is well balanced, and both input and output current show good waveform.

Table 6-3 Circuit Parameters for the experiment

Input Voltage	230 Vrms/ 400 Hz	Load Resistance	16 Ω
Output Voltage	230 Vrms/400 Hz	Load Inductance	1.2 mH
DC-Link Voltage	660 V	Power	10 kW

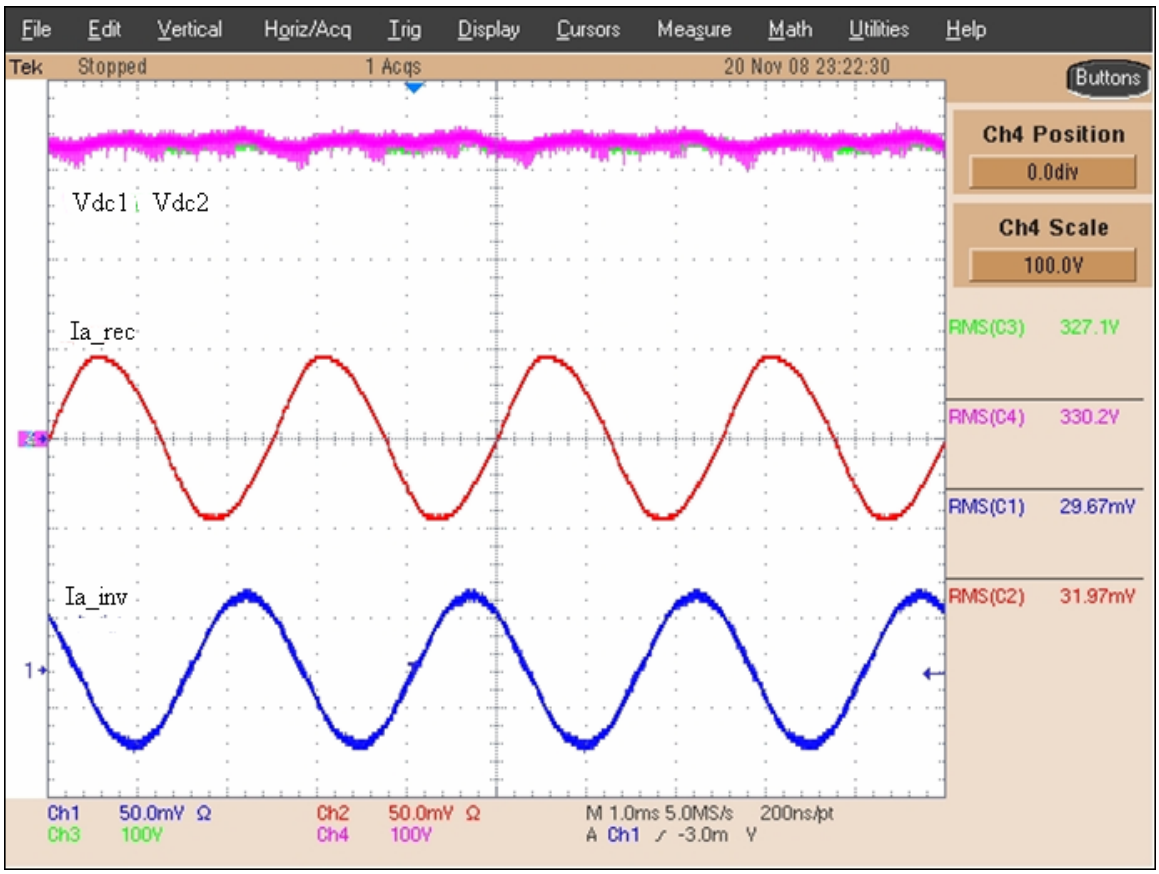


Figure 6-23 Steady state waveforms at full power

Figure 6-24 shows the Fourier analysis result for the input current. For comparison, the power quality requirement defined in DO-160E is also plotted in the same figure. As can be seen, the entire harmonics meet the standard except the fourth order, which exceeds a little bit. The non-ideality of the power source is one of the reasons for the low

frequency current harmonics. In order to improve the harmonic performance, a higher bandwidth for the current control loop is desired.

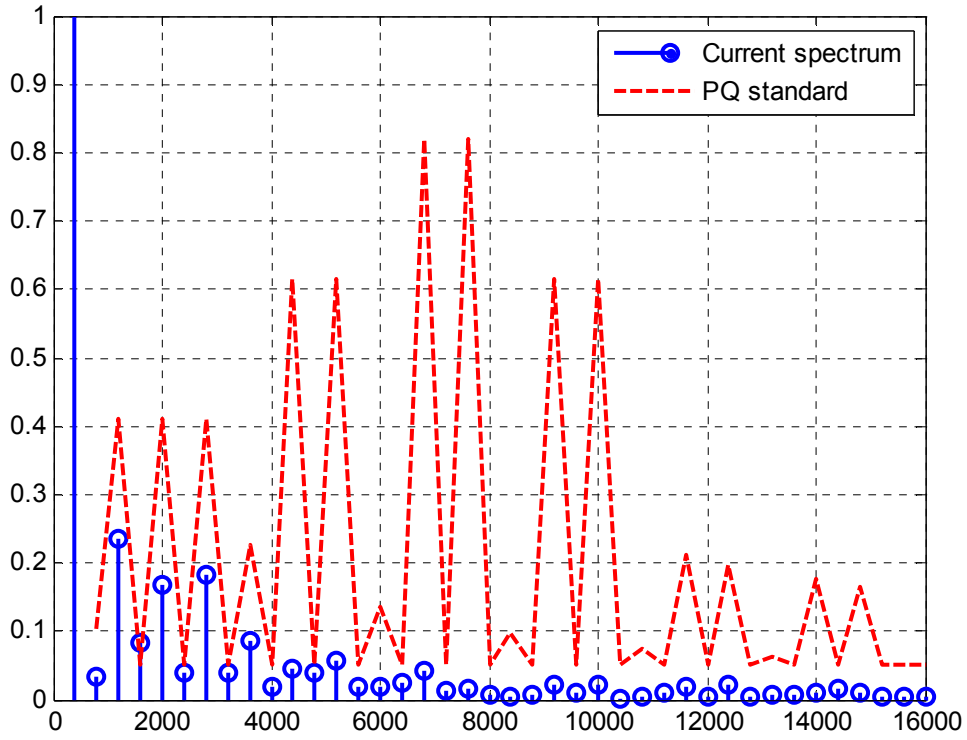


Figure 6-24 Input current spectrum analysis

In order to verify the input filter design, EMI measurement is carried out. The current probe used for the noise measurement is 91550-1 from ETS-Lindgren. Figure 6-25 shows the measurement results. The blue line is the noise current spectrum of Phase A. The pink curve is the total common mode noise current of the three phases and the red dash line represents the narrow band requirement specified by the standard DO-160E. As can be seen, the noise spectrum meets the EMI standard up to 800 kHz. This result demonstrates the EMI filter design concept proposed in Chapter 2 since the L and C parameters are determined by the relatively low frequency noise. In the frequency range higher than 800 kHz, the standard requirement is not met. The measurement results indicate that in this

frequency range the CM noise is dominant. The grounding condition of the EMI filter and the relatively high equivalent parallel capacitance (EPC) of the double-layer winding structure could be the reasons for the high CM noise. It can be improved by reducing the grounding impedance of the EMI filter.

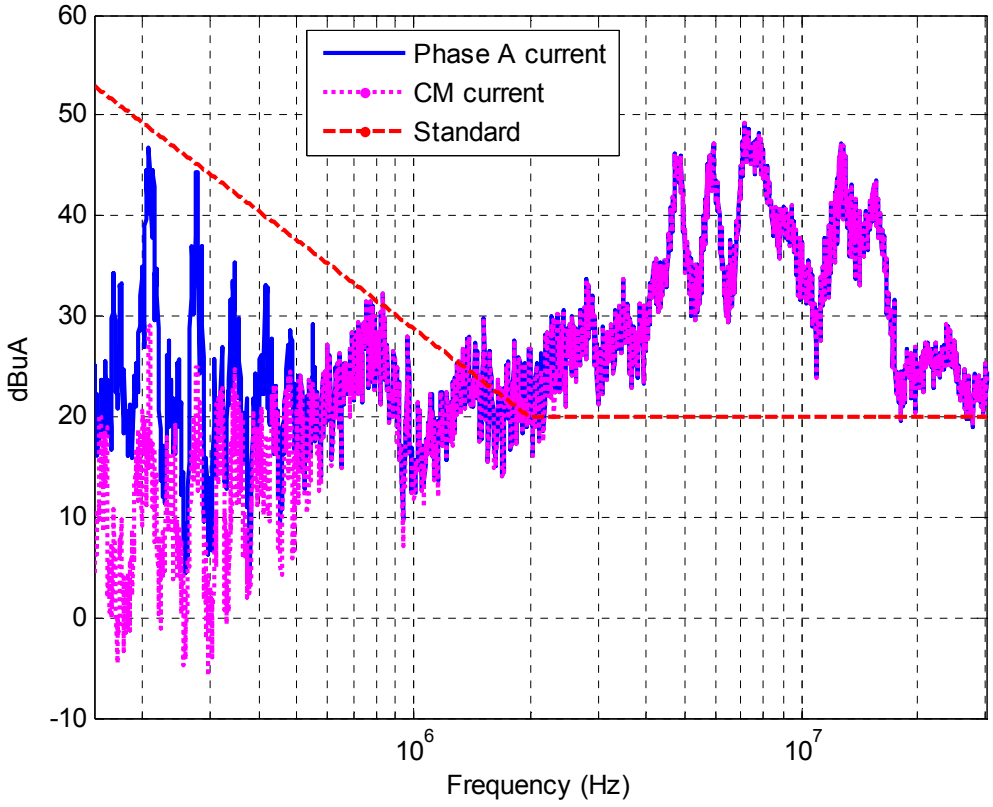


Figure 6-25 EMI measurement results

This converter is also successfully tested with a 3 kW axial flux permanent magnet motor which has 6 pole pairs. The system setup is shown in Figure 6-26. The motor is connected to the YASKAWA dynamometer via an 8 to 1 gearbox. Table 6-4 shows the test conditions. Figure 6-27 shows the measurements for the rectifier. The traces from top to bottom are: dc-link voltages, rectifier line-to-line voltage and input current. Figure 6-28 shows the measurement results for the inverter. The traces from top to bottom are: dc-

link voltage, inverter line-to-line voltage, inverter output current and rectifier input current.

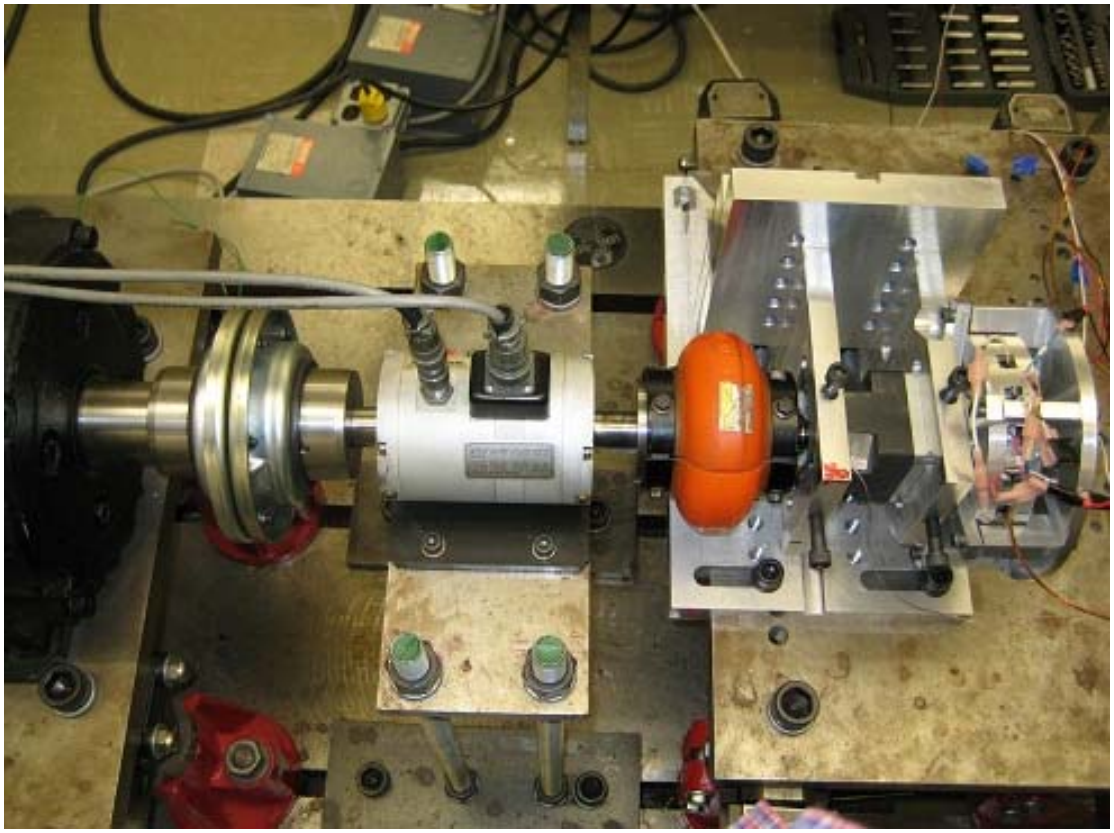


Figure 6-26 Motor test setup

Table 6-4 Conditions for the Motor Test

Input Voltage	115 Vrms/ 400 Hz	Rotor Speed	5500 rpm
DC-Link Voltage	330 V	Torque	5 Nm

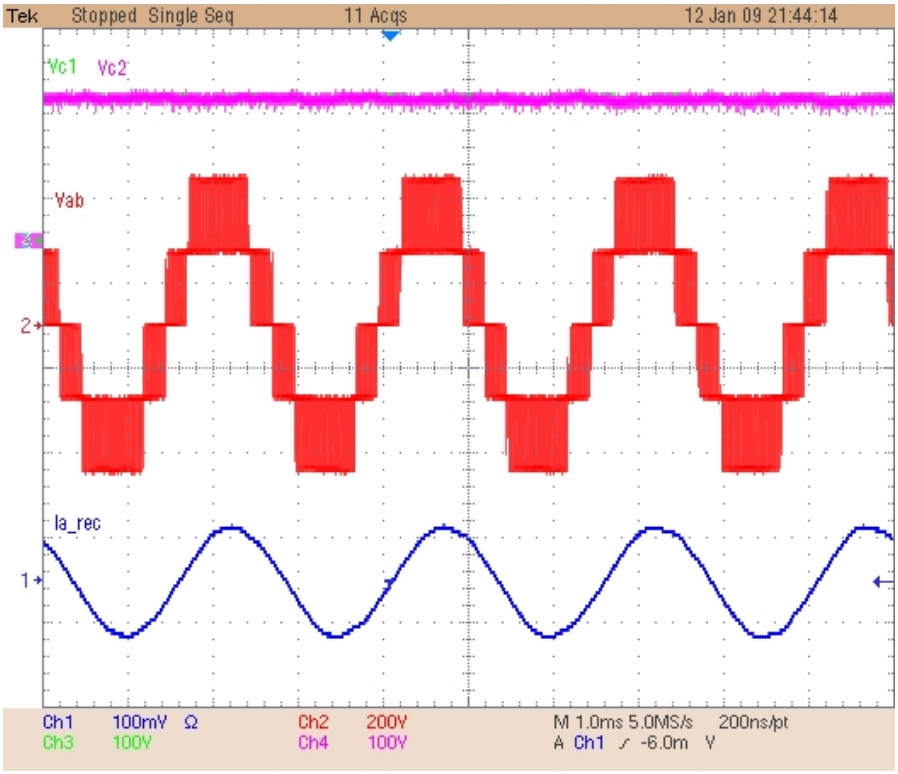


Figure 6-27 Measurement results for the rectifier

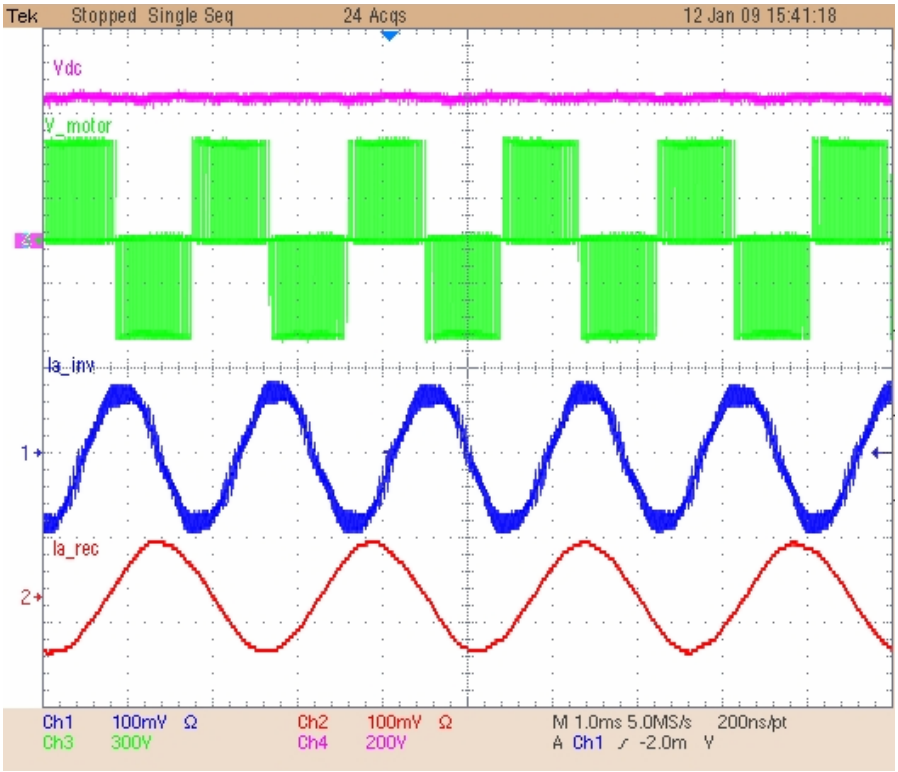


Figure 6-28 Measurement results for the inverter

6.4 System Efficiency

In order to evaluate the loss calculation and verify the overall thermal design, efficiency measurement is carried out in scale down power level with the power analyzer PZ 4000. In this test, the dc-link voltage is 450 V and the input voltage is 160 Vrms. A 1.2 mH three-phase inductor and three 16 Ω resistors are utilized as the three phase load. The ambient temperature is 25 °C. The load current amplitudes and corresponding measurement results are shown in Table 6-5.

Table 6-5 Efficiency Measurement

Load Current (A)	Input Power (W)	Output Power (W)	Loss (W)	Efficiency
9.43	2343	2238	105	95.3%
11.55	3475	3330	145	95.6%
14.33	5336	5102	234	95.4%

The temperature of the side fin for each heatsink is also monitored during the test. For the case with 14.33 A load current, the temperature rise at the measurement point are 11 °C for the rectifier and 8 °C for the inverter, which indicates that the rectifier has higher loss under this condition. Based on the finite element analysis, the thermal resistance for each heatsink is about 0.45 °C/W. Then the average temperature rise of the heatsink for this case can be roughly estimated to be 13.5 °C according to the loss measurement. Considering the non-uniform temperature distribution, the estimation is within a reasonable range compared to the measurement result. Since we measure the junction-to-case thermal resistance of the JFET device, the junction temperature can be estimated to

be 56.5 °C for this case assuming a 1 °C/W thermal resistance for the interface between the heatsink and the device case.

For comparison, the loss calculation results under the same conditions are shown in Table 6-6. The calculation results show similar trend but lower value. There is about 35% error for the loss calculation. Several factors may contribute to the discrepancy. First, the characteristics of JFET are device dependent, and the switching energy highly depends on the circuit conditions including the parasitic. Therefore the switching loss could be different from the one achieved by double pulse test. Second, the impact of the switching ripple is ignored in the calculation. Third, the power in the parallel devices may not be ideally shared and the on-resistance could be higher than the ideal value. Fourth, the loss in the interconnection and some other auxiliary components are not included. Fifth, errors exist for the power and temperature measurement.

Table 6-6 Loss Calculation @ Estimated Junction Temperature of 56.5C

Load Current (A)	Rectifier (W)	Inverter (W)	Filter & Protection (W)	Total (W)
9.43	27.3	24	18.1	69.4
11.55	44.5	33.8	30.2	108.5
14.33	79.3	48.2	50.9	178.4

Considering the 35% error, the total loss and junction temperature at full power case can be estimated. Iteration approach is applied for this calculation. A junction temperature is first assumed for the loss calculation. And then based on the calculated loss we recalculate the junction temperature. If this junction temperature is higher or lower than the previous assumption, we will pick the average value of these two to do the calculation again. This procedure is iterated until the junction temperature converges to a

constant value. With this approach, the total loss is estimated to be 490 W with a JFET junction temperature of 90 °C. The system efficiency is 95.1%. It indicates that the high junction temperature advantage of the SiC JFET is not fully taken. The heatsink and the fan are oversized.

6.5 Weight Discussion for the Hardware System

In this chapter, all the design concepts and procedures developed in the previous chapter are investigated and verified by experiments. The converter system can meet the EMI standard at low frequency range, which proves the integration design concept for the input filter. The stable operation under different conditions demonstrates the feasibility of the dc-link capacitor selection as well as the control design. For the heatsink passive, although there are some errors for the loss calculation, the design approach is still valid in terms of estimating the size of the heatsink and the junction temperature with some correction factors. Since high weight density is the key design objective for the converter system in this work, the weight distribution of the physical system also needs to be investigated and then compared to the paper design.

Figure 6-29 shows the weight breakdown of the converter system. The total weight of the system is 2785 g (6.14 lbs.). The power density of the system is 1.63 kW/lbs. As can be seen, the heatsink, the fan and the input filter dominate the weight of the system.

Before the hardware construction, the paper design is carried out based on the approaches describe in the previous sections. Table 6-7 presents the comparison between the real system and the design values.

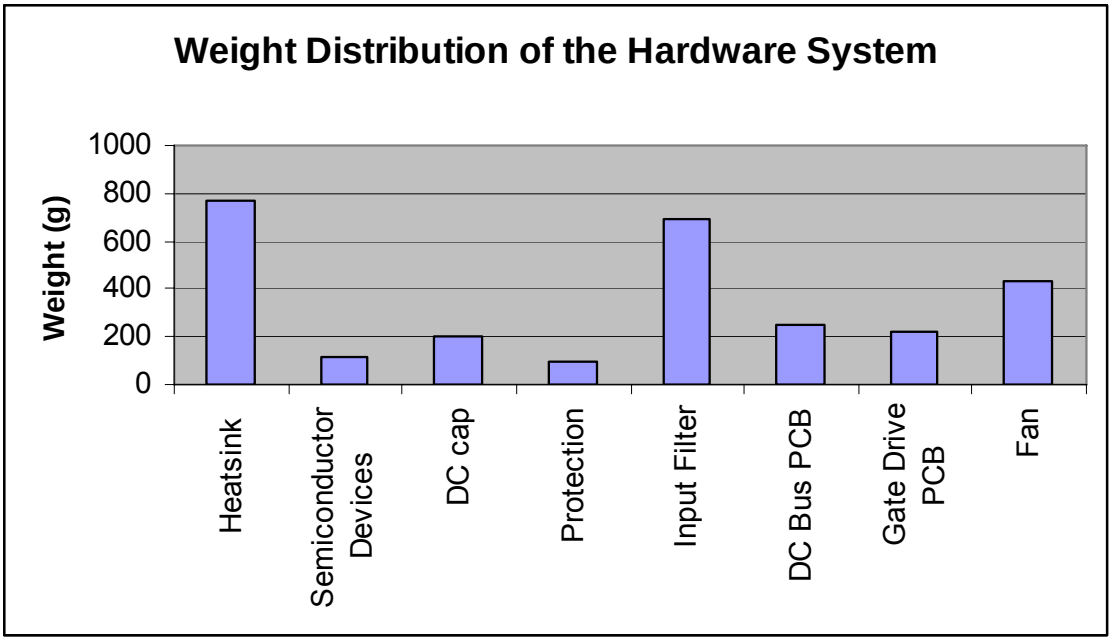


Figure 6-29 Weight distribution of the hardware system

Table 6-7 Weight Comparison

	Heatsink	Devices	DC cap	Prote-ction	Fan	LCLC Filter	Additional Inductor	DC Bus PCB	Gate Drive PCB	Total
Real Value (g)	768	120	204	100	430	513	183	248	219	2785
Design Value (g)	318	120	80	80	162	432				1192

The explanations for the weight discrepancy between the design and the real system are given as following:

- Heatsink and fan are the key contributors to the weight difference. As discussed in the previous section, these components are over-sized because of an availability issue for the commercial products.

- Dc-link capacitor: Due to the limitation of the universal controller, the actual control frequency is 35 kHz for the rectifier although the switching frequency is 70 kHz. We chose 17.5 μF instead of 10 μF for the total dc-link capacitance. On the other hand, there is also some error when scaling the size of the capacitor based on energy storage in the design stage.
- LCLC filter: The difference is caused by the winding. In the real system the weight of the winding is bigger than the designed value due to an estimation error for the multi-layer winding structure, where the mean length per turn of the outer layer is longer than the inner layer. But it is ignored in the paper design.
- As explained in the previous chapters, an additional inductor is used to compensate the impedance of the LISN at low frequency.
- The weight of the printed circuit board and some auxiliary power supplies and connectors is not considered in the paper design.

6.6 Summary

This chapter presents the hardware development of a 10 kW high power density three-phase ac-dc-ac converter using SiC JFETs and SiC Schottky diodes. The structure of parallel devices is implemented for the phase leg to achieve a high power rating and the corresponding gate driver circuit is proposed and tested. All the technologies and concepts developed in the previous chapters are applied in this hardware system and a special start-up sequence in software is developed to cope with the non-regenerative characteristics of the Vienna-type rectifier. The converter system is tested with full power and all the key functions are verified. The EMI measurement is also carried out. The low

frequency noise spectrum demonstrates the input filter design. The high frequency noise does not meet the standard, and there is still room to improve by reducing the ground impedance of the CM filter. The converter system is also successfully tested with a 3 kW permanent magnet motor. The efficiency and the heatsink temperature of the system are measured in a scaled down power level and then compared to the theoretical calculation. The results indicate that smaller heatsink and fan can be used.

The hardware system achieved 1.63 kW/lbs. The difference between the real system and the paper design is discussed and analyzed. It shows that a higher density can be obtained by customizing the heatsink and fan since the ones used in the systems are over-sized.

Chapter 7 Conclusions and Future Work

This chapter summarized the entire dissertation and discusses some ideas for the future work.

7.1 Conclusions

This work presents a systematic methodology for the analysis and design of high power density three-phase ac converter. Four key factors of the converter system, including topology, passive, control and failure mode, are carefully studied.

First, the parameters selection criteria for both input filter and dc bus energy storage are developed. The correlation between the switching frequency and the size of the input filter are investigated when considering EMI standard and power quality requirement. A non-monotonous relationship was found, accumulating with some favored operating frequency from the size standpoint. A function integration concept for input filter design is proposed, which means the input filter, including EMI filter and harmonic filter, can be designed as an entity based on the output standard requirement and the converter terminal voltage or current spectrum. The same inductors can be used for EMI suppression and for boost function. Energy storage and impedance interaction requirements are also set up to determine the minimum DC link capacitor.

Second, a systematic methodology for a three-phase converter topology evaluation, as well as the design approach, is proposed. The design objective (size/weight), constraints, conditions, and variables are clearly defined. All the key size contributors and their correlations are introduced and analyzed in a systematic way. It provides the design

guideline for both circuit parameter selection and system operation condition determination. Based on the proposed methodology, 4 candidate topologies are compared. The results show that the three-phase non-regenerative three-level boost rectifier (NTR) plus voltage source inverter has a better weight performance under the given conditions. This approach can be applied to other topologies with different metric.

Third, in order to achieve a high performance control algorithm for a high speed operation, a wide frequency range average model for the NTR is developed. An "optimal" zero sequence injection concept is proposed from the voltage balance standpoint. Based on this concept an equilibrium point for the dc-link neutral voltage balance can be found and then the average model can be built in the conventional d-q coordinate. In the proposed model the neutral point behavior is represented by a simple first order system. The control loop can be easily designed. A carrier-based control approach is developed by doing the optimal zero sequence injection in a partially feed forward way. The proposed control approach features great simplicity and good neutral regulation. Both simulations and experiments verified the validity of the model and the controller.

Fourth, an over voltage failure mode is identified for the NTR. It is a short failure associated with the switches and diodes of the neutral legs. The voltage across the capacitor will double once the failure occurs. Two protection approaches as well as the input inductance impact are investigated. For the voltage clamping approach, the fault current and the energy dissipation will increase inversely to the input inductance. It indicates that a neutral point blocking approach is preferred for the converter system with low input inductance. The shoot-through failure mode, which is particularly a serious

issue for the converter built with normally-on devices, is also discussed and analyzed. A unique protection circuit is proposed, which achieves both functions of shoot-through protection and dc-link pre-charge. The proposed approaches are verified by the experiments.

In the end, a 10 kW three-phase ac converter is design and built with SiC JFETs and SiC Schottky diodes. All the design concepts and technologies developed in this work are implemented into this hardware system. The system is successfully tested to high power and high switching frequency. The EMI measurement and current harmonics analysis are carried out and the results verify the validity of the proposed design approaches. The experimental results also indicate a clear need to further improve the high frequency EMI performance. A power density of 1.63 kW/lbs is achieved by the experimental system. It shows a larger weight than the paper design, which is mainly due to the over-sized cooling system and the printed circuit board. A customized heatsink and fan can help to further reduce the weight of the converter system.

7.2 Future Work

In order to further improve the power density of the three-phase ac converter, future work can be carried out in the following directions.

- In this work the commercial cooling technologies are chosen in the design, and there are some errors for the thermal calculation. A delicate model for the thermal system is desired. Since the heatsink and fan remain the key weight/size contributors, advanced cooling technologies and package approaches can be explored to further reduce the size of the cooling system. On the other hand, as

the advantage of SiC devices, the junction temperature of the devices can be pushed to a higher level, with which the size of cooling system can be further reduced. This requires a thermal reliability evaluation for the devices and components. The development of corresponding high temperature auxiliary circuits and packaging technology is also a necessity.

- The EMI filter design approach proposed in this work is based on the low frequency analysis. The three-phase common choke is designed to achieve a relatively high leakage inductance for the function integration purpose. That may exaggerate the coupling issues between the different filter stages and impact the noise attenuation capability. Further investigation on filter structure and shielding approach is desired. In addition, the filter behavior at high frequency, including the grounding impact, and the corresponding approach for improvements needs to be further analyzed. A full frequency range model for the input filter is desired.
- In this dissertation, the average model for the Vienna-type rectifier is built on the equilibrium point when the dc-link voltage is balanced. How to extend the model to other operating points can be further explored.
- From the system point of view, an advanced modulation scheme or circuit topology can be studied to reduce the EMI noise. For example, random PWM can spread out the noise energy in the frequency spectrum, which potentially can reduce peak noise and then lead to smaller EMI filter. The parallel topology can be also investigated since it can cancel switching ripple at some specific frequency range. This will provide new opportunities for the input filter design.

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