ANALYSIS AND DYNAMIC RANGE ENHANCEMENT OF THE ANALOG-TO-DIGITAL INTERFACE IN MULTIMODE RADIO RECEIVERS

by

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Abstract

The rapidly developing wireless market has spawned a multitude of different standards for cellular, PCS, and wireless data. To allow users the ability to access services conforming to disparate standards, multimode handsets capable of software reconfiguration are needed. These "software radios" are distinguished from their traditional counterparts by their strong reliance on digital channel filtering and demodulation which may be reprogrammed to receive different standards. In these radios, higher dynamic range is required from the analog portion, most notably, the analog-to-digital converter (ADC).

This research examines through analysis and simulation the performance requirements of analog-to-digital converters for use in radios which are conformant to the AMPS, IS-54, GSM, and IS-95 cellular standards. Simulations reveal the degradation in performance under conditions of off-channel interference, fading, and converter nonlinearities. Included in this analysis is the design of automatic gain control (AGC) for narrowband and IS-95 spread spectrum systems to optimize quantization noise and distortion due to A/D overload. Lastly, methods for improving the dynamic range of the analog-to-digital interface such as nonuniform quantization, companding, and dither are presented. The development of a novel A/D using a direct-sequence pseudo-noise (DSPN) technique in conjunction with an asymmetrical quantizer is presented and compared with standard dither techniques. Advantages of this technique compared to ordinary ADC's include an almost one bit improvement in resolution, quantization noise whitening, elimination of A/D offsets, and the ability

to simultaneously digitize multiple analog signals with a single quantizer. The technique requires no synchronization and is easily implemented.

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Chapter 1

Introduction

Since its introduction only twenty years ago, cellular radio has grown to over thirty-eight million subscribers. New digital wireless communications standards promise to deliver enhanced coverage and capacity, better quality of service at lower cost, and multimedia message formats including voice, data, and video. In the United States, three major cellular standards are being simultaneously deployed and at least six are being considered for use in the new Personal Communication Services (PCS) band.

This plethora of standards has created a need for receivers which can be reconfigured through software to allow reception of different signal formats. These "software radios" posses analog and digital hardware, but shift the burden of processing to software where configuring the radio to demodulate a new standard is as simple as writing a new program, which could in principle allow remote reconfiguration of a receiver.

Receivers for existing equipment rely heavily upon analog hardware to process the received cellular signal. However, the use of digital signal processing (DSP) has some advantages which may be exploited. Digital signal processing does not suffer some of the limitations inherent in analog processing such as component mismatch, drift, and poor reproducibility of performance from unit to unit. DSP can also implement complex signal processing algorithms either difficult or impossible to perform using analog circuitry. Additionally, analog hardware is custom designed to the standard being implemented, and a complete hardware development cycle must be completed to design a receiver for a new standard.

In recent years, improvements in semiconductor technology have led to vast advances in the processing power of DSP chips. This in turn had made practical radio receivers with an increasing amount of digital signal processing. However, to process a radio signal digitally, it must first be converted from analog form to digital form with an analog to digital converter (ADC). The analog signal must be converted with high fidelity to achieve good receiver performance, yet the analog-to-digital converter must also meet the goals of low cost and low power to be suitable for use in wireless portable equipment.

1.1 The Analog to Digital Interface in DSP-based Radio Receivers

As the amount of analog circuitry in a digital receiver is reduced in favor of DSP, the performance requirements for the analog components which remain including the analog to digital converter (ADC) become more stringent. This is especially true in a software radio, since the analog front end must be wideband enough to pass the widest signal of interest to the digital portion where channel filtering can be programmed for the standard being demodulated. This means that the analog to digital converter will be required to simultaneously digitize several other signals along with the signal of interest. In a cellular radio environment, the interfering signals present are often much larger than the signal of interest. Additionally, the cellular signal undergoes severe fading due to multipath propagation which can cause the signal power to vary in excess of 40 dB. This dynamic, cluttered signal environment requires the converter and associated circuitry to have a very high dynamic range.

To assess the required resolution and dynamic range of an ADC in a digital radio, simplifying assumptions are often made which consider the quantization error as an additional source of Gaussian noise in the system. This assumption is not valid under a variety of conditions [1] which may be present in a digital radio. To completely asses the performance impact of the analog to digital conversion, complete system simulations are necessary.

1.2 Purpose of Research

The principle purpose of this research is to study the analog-to-digital interface in digital radio receivers. Specifically, three contributions are made by this work:

1. **An improved understanding of the mechanisms by which the analog to digital conversion process degrades performance in a digital radio receiver**

   Simulations have provided insight into how A/D converters may be modeled for system simulation. In addition to harmonic and intermodulation distortion from the small-scale integral nonlinearities in an ideal converter, the effect of threshold errors and overload distortion were examined. Overload distortion has been observed to significantly degrade performance in digital receivers. Digitally modulated signals were seen to exhibit some amount of self-dither which gives improved harmonic and intermodulation performance than would be expected from testing with tones.

2. **Establishment of the analog to digital performance specifications necessary to implement type conformant receivers for various cellular standards**

   Analytical and simulated results were generated to provide insight into the resolution and dynamic range requirements demanded of AMPS, GSM, USDC, and IS-95 mobile receivers. Realistic A/D models with overload and threshold errors were simulated. A/D blocking in IS-95 receivers due to strong cochannel AMPS interference has been simulated to examine the performance of practical IS-95 receivers in an AMPS overlay deployment.

3. **Development of new methods for improving the performance of the analog to digital interface in digital radio receivers**

   Several techniques were studied for improving the dynamic range of the A/D conversion subsystem in digital radio receivers. Among these are subsampled radio architectures, dither, bandpass sigma-delta conversion, and nonuniform quantization. A novel spread-spectrum quantizer has been developed which provides quantization noise whitening with lower complexity than pseudorandom dither generation. Additional benefits of the new method include a one-bit

improvement in resolution and the ability to quantize two or more multiplexed signals with a single converter.

The results of this effort are expected to be of interest to both analog to digital converter designers and wireless hardware developers. Converter designers must assess the performance requirements demanded from each wireless standard in order to properly design and market analog to digital converters to successfully serve specific wireless applications, while wireless hardware designers must interpret analog to digital converter specifications to determine suitability for a given radio application.

1.3 Outline of Thesis

In Chapter 2 of this thesis, the theory of analog to digital conversion is reviewed with an emphasis on the distortion mechanisms present in ideal converters and practical converters. In Chapter 3, digital cellular receiver architectures and standards are described. Chapter 4 presents analysis and simulation of analog to digital resolution requirements in cellular radio receivers for AMPS, IS-54, IS-95 and GSM. In Chapter 5, several techniques including a novel spread spectrum technique are presented for improving the dynamic range performance of the analog to digital interface in digital radio receivers. Chapter 6 concludes this thesis with a summary of the findings of this work and potential areas of related future research.

Chapter 2

Analog to Digital Conversion Theory and Techniques

To convert an analog waveform into a form suitable for digital computation, the waveform must be represented by a finite number of parameters. That is to say, the continuous analog signal is represented at discrete time intervals by values from a discrete set. These processes of discretization in time and amplitude are referred to respectively as *sampling* and *quantization* as illustrated in Figure 2.1.

In this chapter, we will introduce the theory of sampling and quantization. This theory will enable us to establish the performance of ideal analog to digital converters and demonstrate the trade off possible between sample rate and signal to noise ratio (SNR). We will proceed to investigate the effect of non-ideal effects in real-world A/D converters. Lastly, we will discuss analog to digital converter implementations and technologies.

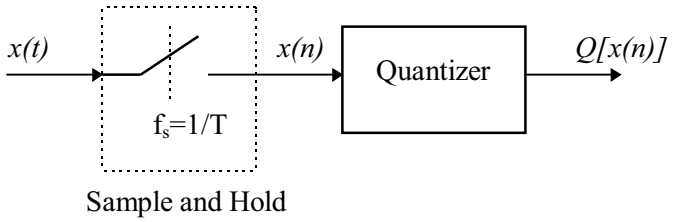


Figure 2.1: Block Diagram of the Digitizing Process

2.1 Ideal A/D Converters

2.1.1 Sampling

The process of sampling represents a continuous-time signal at discrete instants in time. For the sake of simplicity, the signal is usually sampled at uniform time intervals. Mathematically, this may be represented as multiplication of the signal by a uniform impulse train, i.e.

$$x_s(nT_s) = x(t)\delta(t - nT_s) \tag{2.1}$$

where x_s is the sampled signal, $x(t)$ is the analog signal, T_s is the sampling interval, $\delta(t)$ is the Dirac delta function defined as

$$\delta(t) = \begin{cases} 1, & t = 0 \\ 0, & t \neq 0 \end{cases} \tag{2.2}$$

and n includes all integers.

In the frequency domain, sampling has the effect of replicating the input spectrum at intervals of f_s where $f_s = 1/T_s$ is the sampling frequency. In Figure 2.2, the effect of sampling a lowpass signal of bandwidth B is illustrated for the case when $f_s > 2B$, $f_s = 2B$, and $f_s < 2B$. Clearly, when the sample rate is reduced to less than twice the bandwidth of the signal, the images overlap and aliasing distortion results. If $f_s \geq 2B$ the original signal can be reconstructed perfectly from the sampled signal by filtering with an ideal lowpass filter. This is the well known Nyquist criterion for lowpass uniformly sampled signals. To avoid aliasing distortion, analog antialiasing filters are put before the analog to digital converter to provide rejection of signal components above the Nyquist frequency. By sampling the signal of interest at a rate higher than the Nyquist rate, the transition bandwidth of the antialias filter is increased allowing reduced complexity for the filter.

2.1.2 Bandpass sampling

When the signal to be digitized occupies a narrow bandwidth centered about some frequency f_c, the required sample rate is modified from the lowpass case. Consider

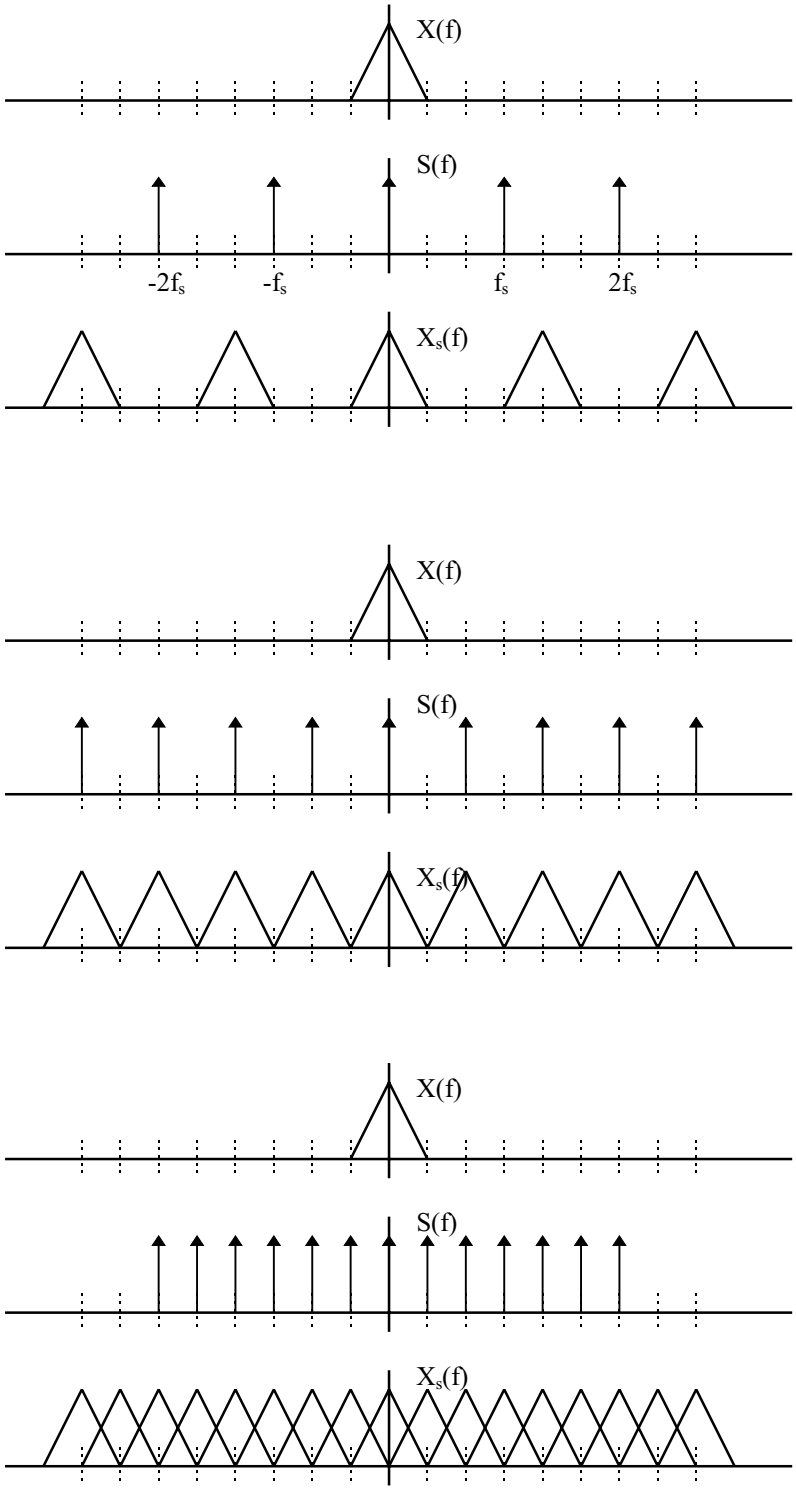


Figure 2.2: Frequency domain result of sampling for a) oversampling $f_s > 2B$ b) critically sampling ($f_s = 2B$) and c) undersampling $f_s < 2B$

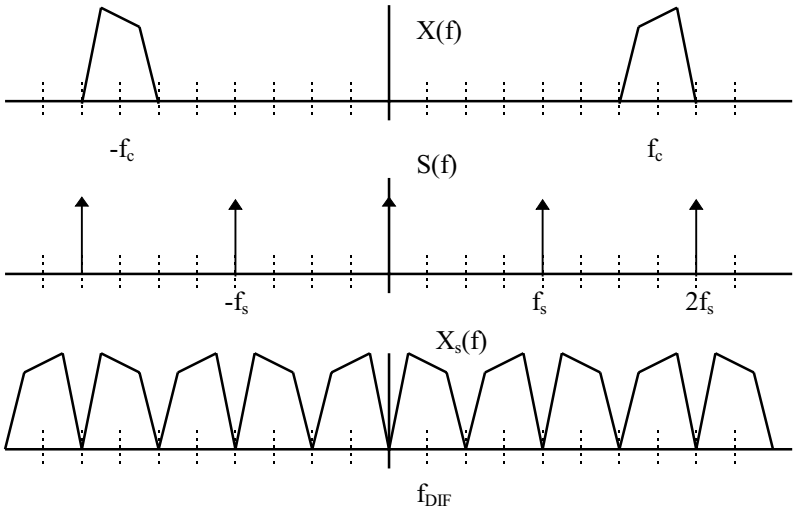


Figure 2.3: Bandpass Sampling

the situation depicted in Figure 2.3 in which a bandpass signal with bandwidth B centered at a frequency f_c is sampled at a rate f_s where $f_s < f_c$. The aliases from the sampling process fall at frequencies given by

$$f_{DIF} = f_c \pm nf_s \tag{2.3}$$

where n is any positive integer.

The notation f_{DIF} has been used to denote "digital IF"; that is, the sampling process is equivalent to a mixing process which translates the input narrowband signal to a new frequency. Notice the sample rate may be much less than the highest frequency of the input signal without aliasing distortion, provided that the following relationship is met [2].

$$nf_s + B \leq 2f_s \leq (n+1)f_s - B \tag{2.4}$$

where k is a positive integer. This is equivalent to saying that the band to be sampled must not fall on integer multiples of $f_s/2$ to avoid aliasing.

Because the signals at the Radio Frequency (RF) and Intermediate Frequency (IF) stages of a receiver are narrowband bandpass signals, this theory can be used to

simplify the radio. Architectures which exploit this phenomenon and their advantages and limitations will be explained in detail in Chapter 3 when we discuss digital radio architectures. It is also important to note that when the signal to be processed using bandpass sampling, the antialising filters must in general also be bandpass.

2.1.3 Quantization

The process of quantization maps an analog signal with infinitely many possible amplitudes to a finite precision representation which can be encoded with a relatively small number of bits. Because some information is lost in the process, this operation necessarily introduces an error. The quantization process can be considered as passing the signal through a memoryless stairstep nonlinearity [3]. Most commonly, uniform quantization is used where the input thresholds and output values are evenly spaced, and the number of levels is chosen to be a power of two to provide efficient coding with binary logic.

Figure 2.4 shows the transfer function of a "mid-riser" quantizer and the error as a function of input level. The quantization stepsize Δ ultimately determines the resolution of the quantization process.

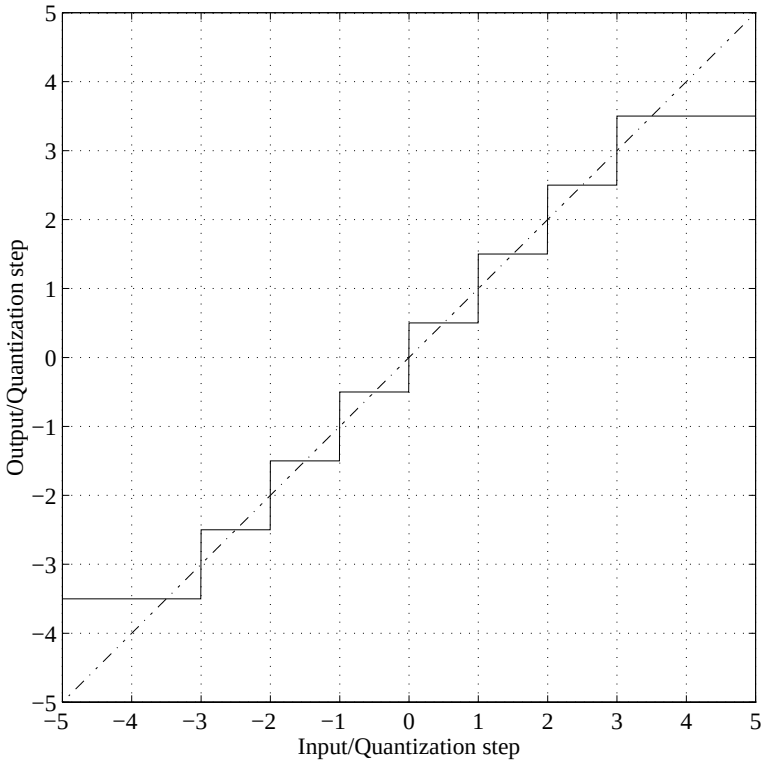
Quantization Noise and Signal to Quantization Noise Ratio

The quantization error is defined to be the difference between the quantized signal $\tilde{x}$ and the input signal x, i.e.

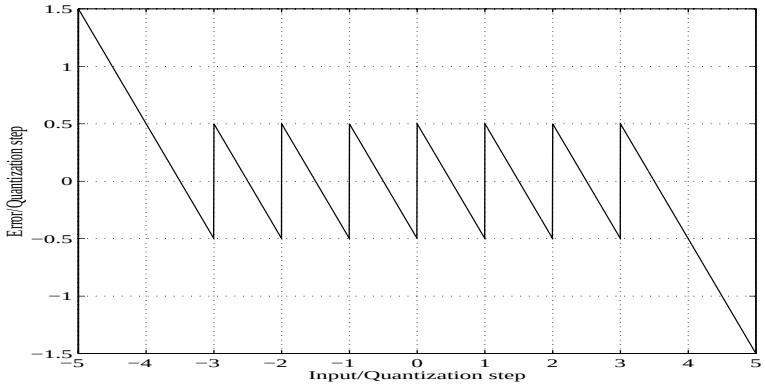
$$e(x) \equiv \tilde{x} - x \tag{2.5}$$

In [1] Bennett demonstrated that when the number of levels in the quantizer is large and the input signal is sufficiently random, the error introduced by quantization is well approximated as a random white noise process uncorrelated with the input signal. Under this assumption, the total quantization noise power is equal to the mean-squared error which is

$$\begin{aligned} MSE &= E[e^2(x)] \\ &= \int_{-\infty}^{\infty} (\tilde{x} - x)^2 p(x) dx \end{aligned} \tag{2.6}$$



(a)



(b)

Figure 2.4: Output vs. input (a) and error vs. input (b) for a uniform mid-riser 3 bit quantizer

where $E[\cdot]$ is the expectation operator and $p(x)$ is the probability density function of the input x. When the input is zero mean the MSE is simply equal to the variance of the error, σ_e^2.

Defining the full-scale input range V_{FS} to be the range of input over which the error is bounded by $\pm\Delta/2$, we have

$$\Delta = \frac{V_{FS}}{2^b} \tag{2.7}$$

where b is the number of bits in the converter.

If the input to the quantizer is a uniform random variable distributed on $[-V_{FS}/2, V_{FS}/2]$, the result of equation 2.6 is

$$MSE_{uniform} = \frac{\Delta^2}{12} \tag{2.8}$$

Since the input signal has zero mean the average signal power is simply the variance of $x = V_{FS}^2/12$ and the signal to quantization noise ratio is

$$\begin{aligned} SNR &= 2^{2b} \\ &= 6.02b \text{ (dB)} \end{aligned} \tag{2.9}$$

For this specific case where the input is uniformly distributed and matched to the full scale range of the quantizer, the error is also uniformly distributed on $[-\Delta/2, \Delta/2]$. Although not strictly correct, this assumption of uniform distribution of error is often retained to compute the SNR for other signals [4]. With this assumption, the error variance is still given by equation 2.8. When the signal is not allowed to overload the quantizer, the peak signal amplitude is $V_{FS}/2$ and the peak signal power $P_{x_{PK}}$ is given by (using equation 2.7)

$$\begin{aligned} P_{x_{PK}} &= (V_{FS}/2)^2 \\ &= (2^b\Delta/2)^2 \\ &= 2^{2(b-1)}\Delta^2 \end{aligned} \tag{2.10}$$

We now define η as the peak to average power ratio of the signal, allowing us to calculate the average power as

$$P_{AVG} = \frac{P_{PK}}{\eta} = \frac{2^{2(b-1)}\Delta^2}{\eta} \tag{2.11}$$

Knowing the average power and the variance of the error signal, the average signal to quantization noise ratio can be calculated

$$\begin{aligned} SNR_{AVG} = \frac{P_{AVG}}{\sigma_e^2} &= \frac{3(2^{2b})}{\eta} \\ &= 6.02b + 4.77 - 10\log_{10}(\eta) \text{ (dB)} \end{aligned} \tag{2.12}$$

This general form allows the approximate computation of SNR for a variety of inputs based upon the peak to average power ratio. When the input is a sinusoid, the peak to average ratio is equal to two. Thus equation 2.12 yields the well-known result

$$SNR_{sinusoid} = 6.02b + 1.76 \text{ (dB)} \tag{2.13}$$

When the input is Gaussian, the peak to average power ratio of the signal does not strictly exist, because the probability that the signal will exceed any value is non-zero. Thus there will always be overload when the input is normally distributed, but the probability of overload can be made arbitrarily small by reducing the input variance.

2.1.4 Sample Rate and SNR tradeoff

In the simple white noise quantization model the power spectrum of the quantization noise is uniform to half the sample rate ($f_s/2$). This means that when a signal is oversampled, that is, the sample rate of the system is much higher than the signal's Nyquist bandwidth, the quantization noise is spread over a larger band. Thus the excess noise may be filtered from the signal and the total quantization noise power can be reduced, improving the SNR. Figure 2.5 illustrates this effect for two A/D converters with the same number of bits operating at two different sample rates. With oversampling taken into account, the complete expression for average SNR is

$$SNR = 6.02b + 4.77 - 10\log_{10}(\eta) + 10\log_{10}\left(\frac{f_s}{2B}\right) \text{ (dB)} \tag{2.14}$$

The improvement realized is 3dB for each octave of oversampling.

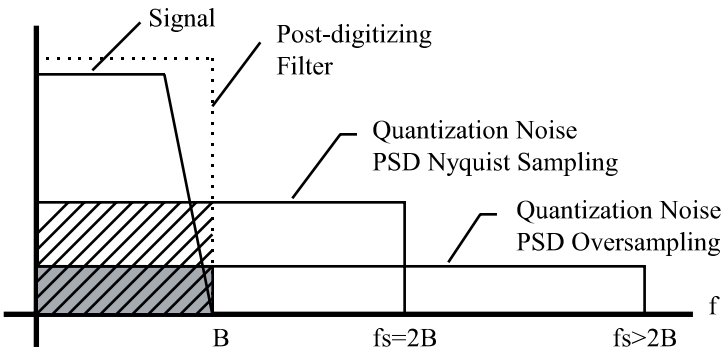


Figure 2.5: Improvement in SNR with oversampling

2.1.5 Power Spectrum of Quantization Error

The actual power spectrum of the quantization error has been studied extensively [1, 5, 3]. The results in the previous section describe the total error power in the Nyquist bandwidth. For narrowband radio applications, it is often important to know the noise and distortion in a band of interest which may be significantly less than the Nyquist bandwidth. The additive white noise model for quantization error is valid when the number of bits is high and the input is "busy" (i.e., exercising most of the codes in the converting and sufficiently random to avoid periodicities in the output error). Figure 2.6 illustrates how the quantization noise spectrum is dependent upon the resolution of the quantizer when the input is a Gaussian low-pass noise sequence with normalized bandwidth of B=0.005. These results were simulated by quantizing a 64K sample Gaussian low-pass noise sequence scaled strictly to lie within the full scale range of the quantizer. The spectrum of the quantization error is estimated using an averaged periodogram with an FFT length of 4096 and a Hanning window. Clearly, the quantization error spectrum is white for a large number of bits but shows significant peaking at low frequencies when the number of bits is less than four. As the bandwidth of the input is decreased, this peaking becomes more pronounced and becomes significant at higher resolutions.

When one or more sinusoids are quantized, harmonic and intermodulation distortion can conspire to cause the quantization error power to be concentrated at discrete frequencies. For periodic inputs such as these, the spectrum of the quantization error can be found by expanding the sawtooth error transfer characteristic in Figure 2.4(b)

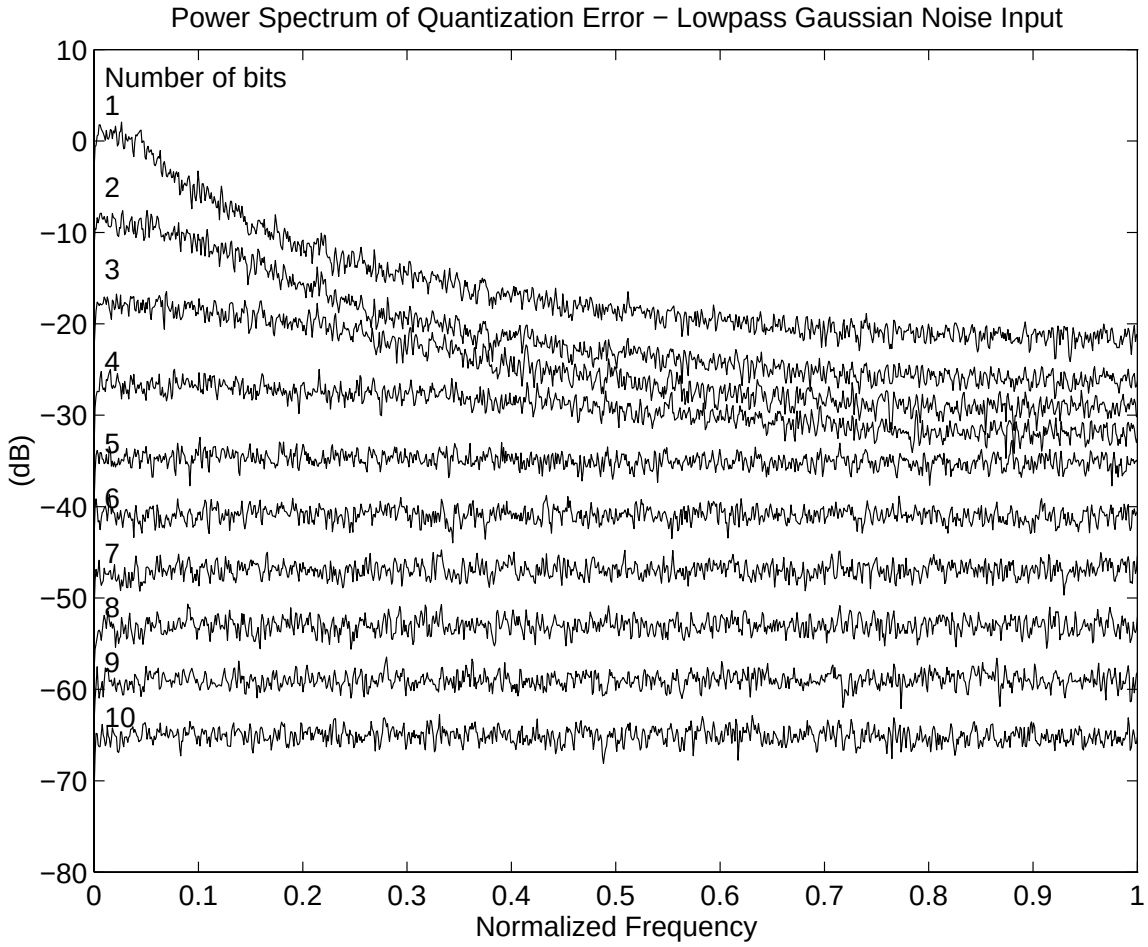


Figure 2.6: Power Spectrum of Quantization Error with Lowpass Gaussian Noise Input

in a Fourier series [6, 7, 8, 9, 10]

$$e(x) = \sum_{n=1}^{\infty} \frac{1}{n\pi} \sin(2n\pi x) \tag{2.15}$$

where the input x is expressed in units of the quantization stepsize Δ for convenience. When the input is a single sinusoid with amplitude A expressed in units of the quantization stepsize and frequency f_c

$$x = A \sin(2\pi f_c t)$$

the quantization error is

$$e(t) = \sum_{n=1}^{\infty} \frac{1}{n\pi} \sin\left(2n\pi A \sin\left(2\pi f_c t\right)\right) \tag{2.16}$$

or

$$e(t) = \sum_{n=1}^{\infty} \frac{2}{n\pi} \sum_{k=0}^{\infty} J_{2k+1}\left(2n\pi A\right) \sin\left(2\pi\left(2k+1\right) f_c t\right) \tag{2.17}$$

Thus the error is seen to consist of odd harmonics only (because of the odd quantizer transfer function) whose amplitudes are given as a sum of Bessel functions. This is intuitively satisfying when one observes that the output error sequence is sawtooth which is slowly frequency modulated by the input sinusoid. When A is large, the signal traverses many levels and the resulting spectrum is approximately white. Ordinary analog components have soft nonlinearities which can be described by Taylor expansions, and their harmonic and intermodulation products increase monotonically[1] with increasing input power. In contrast, the local stair-step discontinuities in the A/D transfer function cause distortion products to vary periodically with increasing signal power, even going to zero for certain input amplitudes. Another feature of nonlinear distortion products from an A/D converter is that higher order products can often be the strongest, and products higher than Nyquist can alias in band to mask weak signals.

As will be explored in further detail in Chapter 5, the quantization noise spectrum from an ideal quantizer can be significantly whitened by dither, whereby a random (or pseudorandom) signal is added to the input signal prior to quantization.

[1]For *nth*-order harmonic and intermodulation products, the distortion increases n dB for every 1dB increase in input power until compression occurs

2.2 Non-ideal distortion

All of the results from the previous section assumed that the quantizer stepsizes were uniform and the signal did not overload the converter. For practical ADC's, the quantizer threshold spacing cannot be perfectly uniform because of imprecise component matching. In radio applications, nonlinear distortion products generated by the conversion process can fall in-band and degrade demodulator performance. Additionally, dynamically varying signals can occasionally cause the full scale range of the quantizer to be exceeded. Jitter in the sample and hold circuit limits the dynamic range performance for high frequency inputs. In this section, we will examine the degradation in performance caused by these limitations.

2.2.1 ADC Nonlinearity

Figure 2.2.1 illustrates a practical analog to digital converter transfer characteristic with errors in threshold levels. These errors are caused by imperfect matching between analog components in the converter. In converters with integral sample and hold circuitry, these errors can also be caused by the nonlinear response of the sample and hold. The difference in step size between adjacent thresholds and the ideal stepsize is termed the differential nonlinearity (DNL)[11]. Another measure of converter linearity which is often specified is the integral nonlinearity (INL), which is defined as the maximum deviation from a straight line drawn between the extremes.

As seen in Figure 2.2.1, the error from a quantizer with threshold errors is no longer bounded by $\pm\Delta/2$. As a result, the total mean-squared distortion is increased. More importantly, the error spectrum can deviate significantly from the simple assumption of additive white noise and can have significant harmonic and intermodulation components when the input consists of sinusoids [12]. The relationship between differential and integral nonlinearity and the output power spectrum is not simple and is not unique (i.e., one cannot obtain the magnitude and location of threshold errors from measurement of the power spectrum). Additionally, spurs added by the digital converter are a function of the input signal frequency and amplitude.

To better characterize converters for radio applications, manufacturers are beginning to specify Spurious Free Dynamic Range (SFDR) instead of static linearity specifications [13]. The single tone SFDR is defined as the difference in dB of an

input tone (typically tested at a worst case of 1dB below full scale to avoid overload) and the largest spur as shown in Figure 2.8. While SFDR and IMD specifications are better than DNL and INL, they do not necessarily provide a good quantitative assessment of the distortion levels which can be produced when digitizing multiple digitally modulated radio channels. This is because the radio signal, being modulated with random data, is more random and does not have the same periodicities in the error signal which give rise to line spectra. A more appropriate specification of A/D converter performance is *Noise Power Ratio* (NPR). Noise power ratio is tested by exciting an A/D with random noise which has been filtered with a notch filter to remove a narrowband portion. At the output, the amount of noise which has filled in the notched frequencies is a measure of the nonlinear distortion. Because the excitation is a random signal, the NPR test more closely mimics the conversion of random inputs.

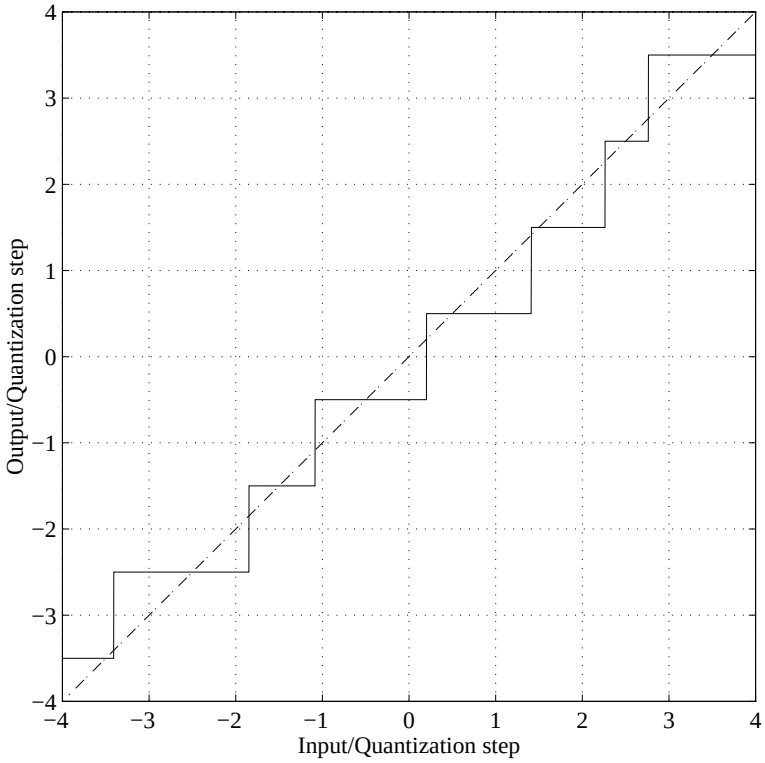
As in the case of ideal quantization, the harmonic and intermodulation distortion arising from threshold errors can be improved with dither.

2.2.2 Overload Distortion

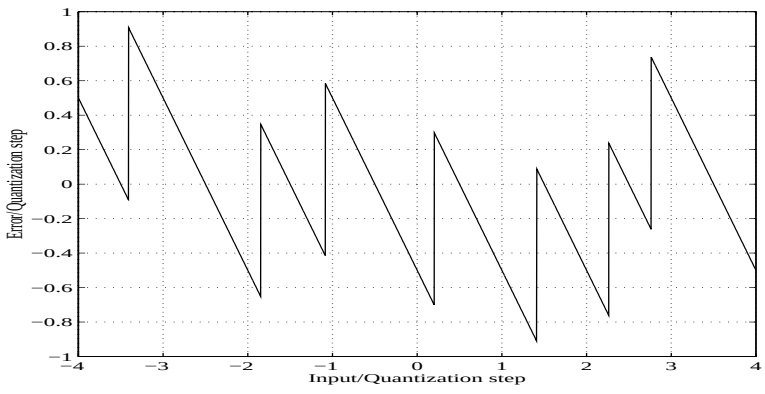
When the input exceeds the full scale range of the A/D, overload distortion results. This distortion manifests itself in both increased mean-squared error (noise power) and severe harmonic distortion (noise concentrated at harmonics of the input). If the pdf of the A/D input is known, the mean-squared error due to overload only can be calculated as

$$MSE_{overload} = 2 \int_{\frac{V_{FS}}{2}}^{\infty} (x - \frac{V_{FS}}{2})^2 p(x) dx \tag{2.18}$$

where $p(x)$ is the pdf of the input to the A/D (assumed symmetric) and the input full scale range extends from $-V_{FS}/2$ to $V_{FS}/2$. The impact of overload is more pronounced for high resolution converters because the MSE due to overload quickly dominates the overall error (granular plus overload) when the number of bits is high. This is illustrated in Figure 2.9 where the analytical SNR is plotted versus the input variance for Gaussian and uniformly distributed inputs quantized with a uniform quantizer with full-scale range ± 1. For a given resolution curve, when the input



(a)



(b)

Figure 2.7: Output vs. input (a) and error vs. input (b) for a 3 bit quantizer with threshold errors

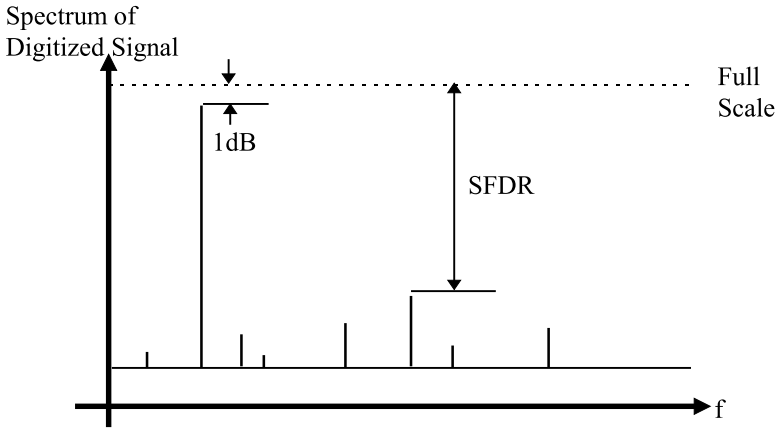


Figure 2.8: A/D Converter Spurious Output and Spurious Free Dynamic Range (SFDR)

variance is low, the SNR is limited by granular noise. As the input variance is increased, the SNR increases due to the increase in signal power until flattening out at some maximum value. As the input variance is further increased, the overload distortion increases and begins to reduce the SNR. For the uniform input, no overload is seen until the input variance is $\frac{(FS)^2}{12}$ which corresponds to the input power at which the peak input is matched to the full scale range of the converter. For the Gaussian input, the transition is more gradual than the uniform case and more dependent on the number of bits. For a given resolution, as the input variance is increased, overload occurs with a higher probability (more area of the Gaussian pdf extends beyond the full-scale range of the converter). For a high number of bits, less overload is required to cause distortion which comparable to the granular error, causing the curves for the high resolution cases to show overload at lower input powers and to have a steeper degradation with increasing overload.

Even more problematic, unlike granular distortion, distortion from overload cannot be modeled as additive white noise. Overload distortion generates significant harmonic and intermodulation distortion. In Figure 2.10, the power spectrum of error when quantizing a lowpass Gaussian input scaled to 20% above full scale range is shown. Compared with Figure 2.6, the overload is seen to add significant distortion at low frequencies when the number of bits is high.

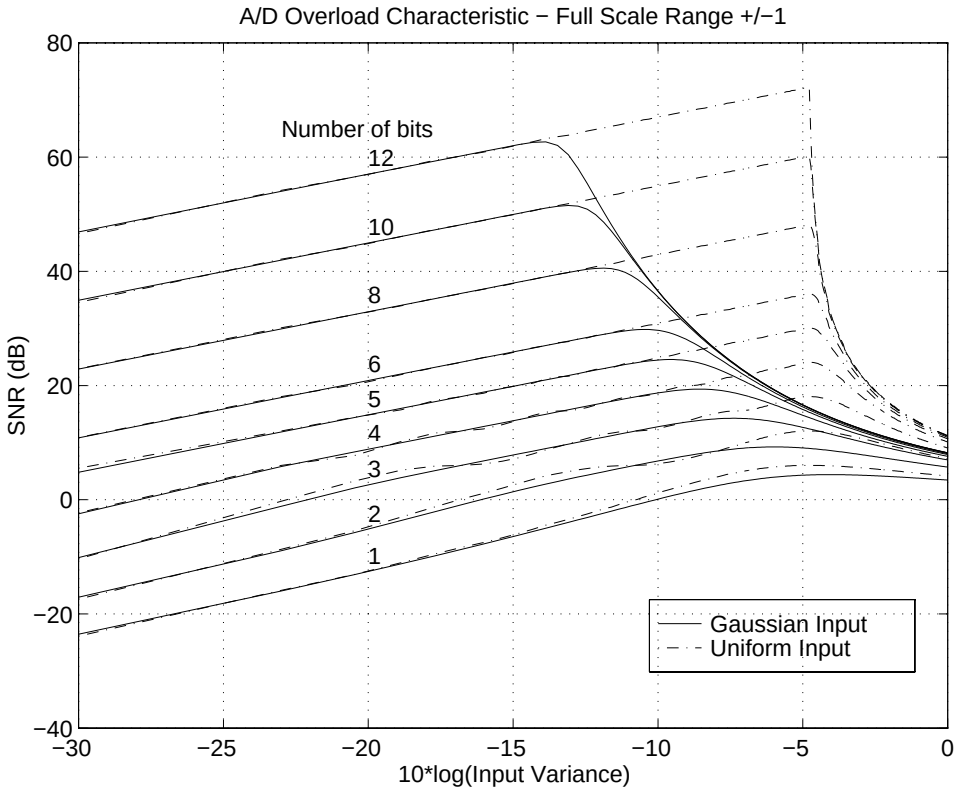


Figure 2.9: A/D Overload Characteristic

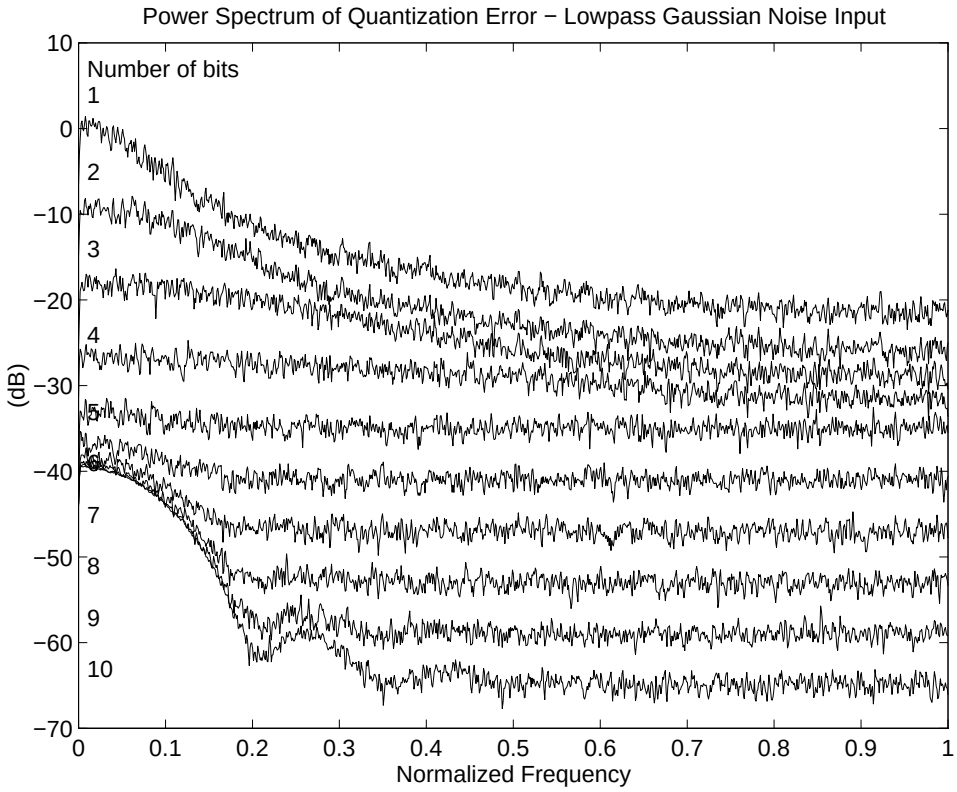


Figure 2.10: Power Spectrum of A/D Output with Overload

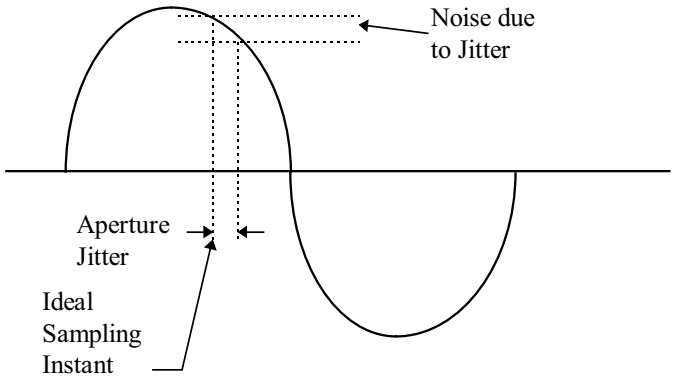


Figure 2.11: Aperture Jitter in a Sample and Hold

2.2.3 Distortion Due to Jitter

In practical sample and hold circuits, the intervals between successive samples are not perfectly constant but vary randomly due to circuit noise. This process, know as aperture jitter, results in an additional noise component in the A/D converter as shown in Figure 2.11. When the input to the A/D is a sinusoid, the relative noise density due to jitter is given by [14]

$$\frac{N_{jitter}}{S} = \frac{8\pi^2 f_o^2 \sigma_a^2}{f_s} \tag{2.19}$$

where N_{jitter} is the noise density in Watts/Hz due to jitter, S and f_o are the power and frequency of the input sinusoid respectively, σ_a is the RMS aperture jitter, and f_s is the sample rate. As seen in both Figure 2.11 and Equation 2.19, at higher input frequencies the effect of input jitter becomes greater (proportional to f_o^2). Also seen in Equation 2.19, oversampling improves the noise due to jitter through averaging(proportional to $1/f_s$).

2.3 A/D Technologies for Radio Applications

In this section, we will briefly describe some of the types of analog-to-digital converters suitable for use in digital radio receivers. Each topology differs in the resolution achieved, the maximum sample rate, the complexity of the implementation and the associated power dissipation.

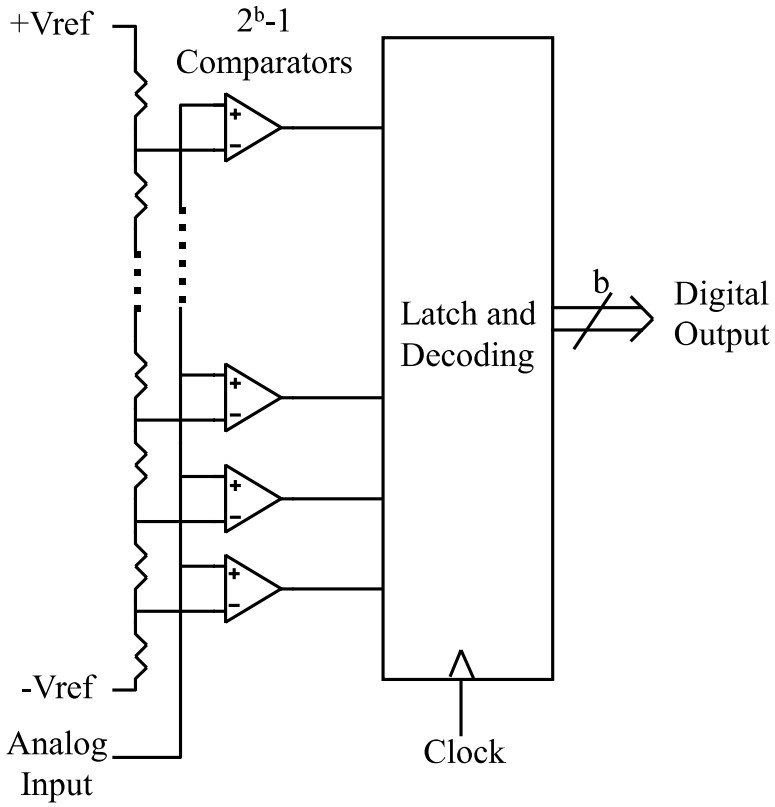


Figure 2.12: Flash A/D Block Diagram

2.3.1 Flash A/D Converters

Perhaps the simplest to conceptualize, the flash A/D consists of $2^b - 1$ comparators with thresholds obtained by taps from a resistive ladder (Figure 2.12). The input is fed to all comparators and those whose thresholds are less than the input voltage have high outputs. This "thermometer code" is then decoded into a Gray code or binary output. Because of its highly parallel architecture, the flash converter is capable of the highest conversion speeds of any converter (as high as 4 Gsamples/second [15]). The exponential increase in complexity with the number of bits results in higher power dissipation than most other converters. The achievable resolution is limited by the matching of converter thresholds from the resistor stick and comparator input devices, as well as dynamic errors in the comparators. With laser trimming, around 12 bits of resolution is possible.

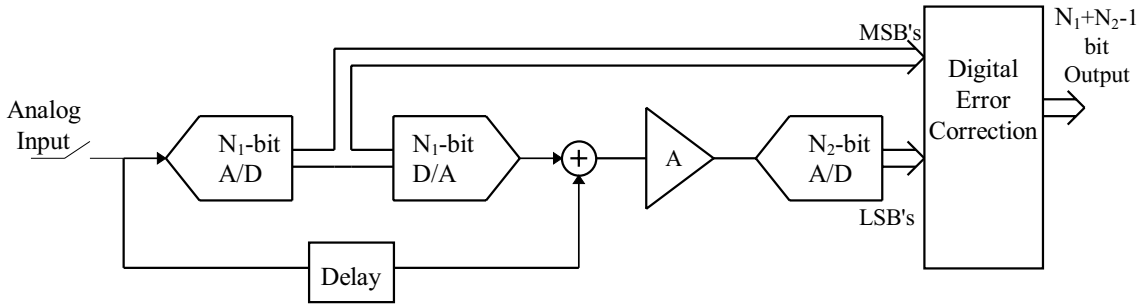


Figure 2.13: Two-step subranging A/D

2.3.2 Subranging A/D Converters

To reduce the number of comparators required in a flash A/D, subranging converters may be used. For example, a two-stage subranging converter first digitizes the input using a lower resolution flash converter (Figure 2.13). The result is converted back to analog using a digital-to-analog converter (D/A) and the difference between the input and the low resolution conversion result is calculated. This residue is amplified by a fixed gain amplifier and converted using a second A/D to obtain the least significant bits (LSB's) of the result. This architecture reduces the number of comparators required and is still capable of very high speed operation. Threshold mismatch in both converters, A/D to D/A mismatch, and gain error in the fixed-gain amplifier all contribute to linearity errors. While flash A/D's exhibit random threshold errors, the linearity errors from subranging converters are repetitive throughout the conversion range because of the structure of the converter. These repetitive threshold errors tend to produce worse harmonic distortion than random errors. Some errors can be compensated in subranging converters by digital error correction techniques, allowing resolutions up to 12 bits. Two-step flash converters are a very attractive architecture for IF sampling receivers because of their high dynamic range and relatively high sample rate. One example is the Analog Devices AD9042, which is a 12bit device with 80dB of dynamic range and a maximum sample rate of 40MHz [16].

2.3.3 Sigma-Delta Converters

The operation of Sigma-Delta converters is substantially different than the converters previously described [17]. As described earlier, higher SNR can be achieved from a

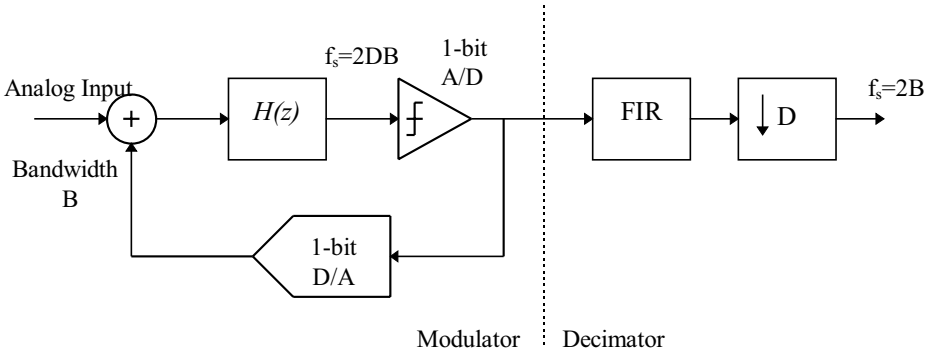


Figure 2.14: Block Diagram of a Sigma-Delta A/D Converter

converter by the use of oversampling. This benefit from ordinary Pulse Code Modulated (PCM) converters is meager, however, with only 3dB improvement in SNR per octave of oversampling. In sigma-delta converters, greater benefit is achieved with oversampling by the use of feedback to shape the noise away from the signal band of interest. A representative block diagram of a sigma-delta converter is shown in Figure 2.14. The converter is composed of two parts: a sigma-delta modulator and a decimating filter. The most common implementation of the modulator uses a sampled data (switched capacitor) filter, a one-bit A/D, and a one bit digital to analog converter (D/A). Sigma-delta A/D converters are capable of very high resolutions and dynamic range. Additionally, the use of oversampling substantially reduces the antialias filter requirements. They are amenable to mixed-signal integration and have relatively low power.

To understand the operation of the sigma-delta modulator, consider a linearized model of the first-order sigma-delta modulator shown in Figure 2.15. The quantizer has been modeled as an additive noise source $E(z)$, and $H(z)$ for a first-order lowpass converter is a simple integrator. At low frequencies, the loop gain of the feedback system is high, and the output is a faithful representation of the input. As the gain of the integrator reduces at higher frequencies, the noise in the output due to quantization increases. The output is described in the z-transform domain as

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1}) \tag{2.20}$$

where it is seen that the input to output signal transfer function is a unit delay while the noise transfer function has a high-pass characteristic. To see the effect of noise

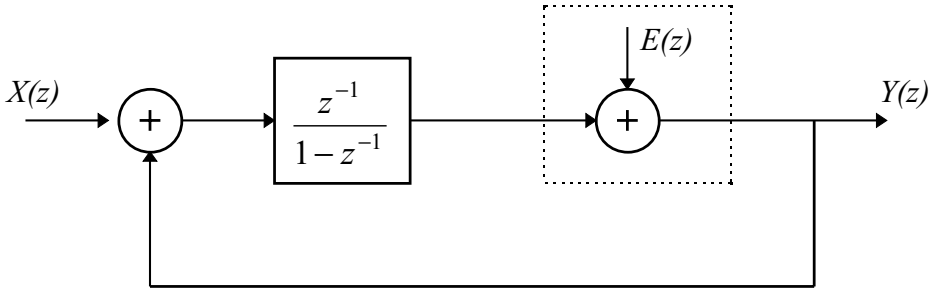


Figure 2.15: Linear Model of a First-Order Sigma-Delta Modulator

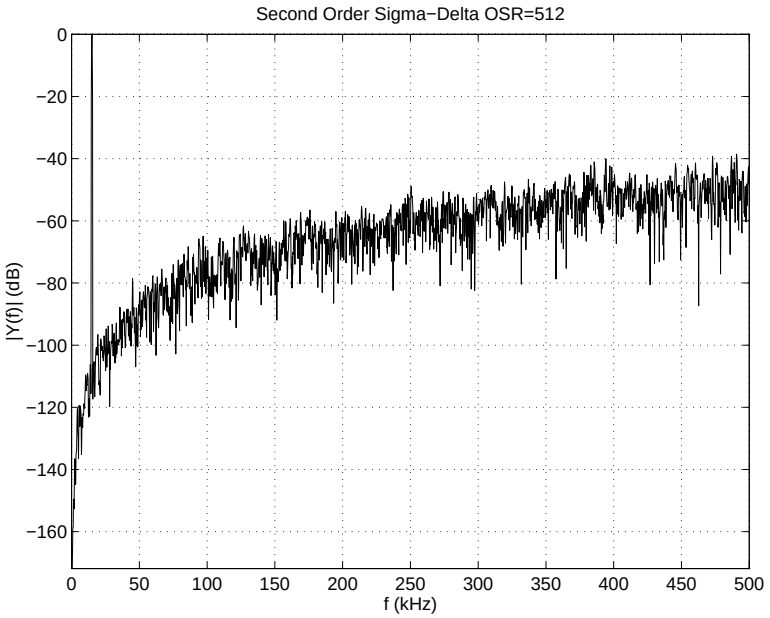


Figure 2.16: Power Spectrum of a Sigma-Delta Converter

shaping, observe Figure 2.16 in which the simulated output spectrum of a second-order sigma-delta converter is plotted for an oversampling ratio (OSR=$f_s/2B$) equal to 512.

To achieve better resolution, higher-order integrators may be used. Figure 2.17 shows the noise transfer function of a first, second, and third-order sigma-delta converter. Improved noise performance results from placing multiple zeros in the noise transfer function at DC. The in-band SNR for an L-th order modulator is given by [17]

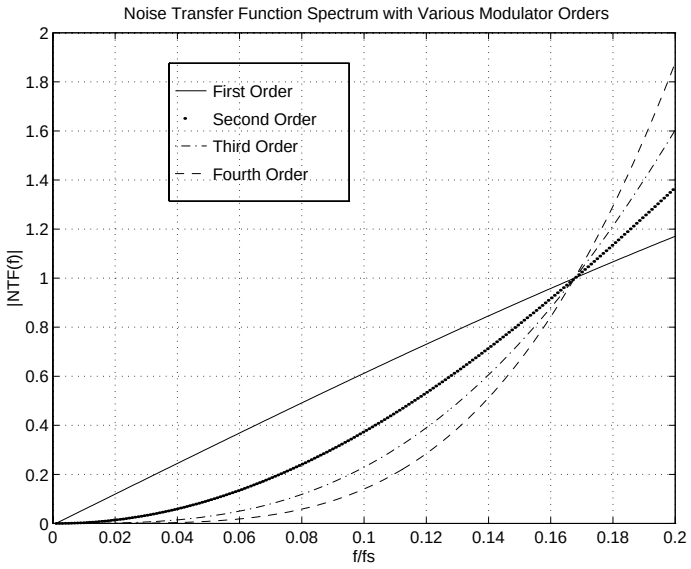


Figure 2.17: Noise Transfer Function with Various Filter Orders

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log\left[\frac{f_s}{B}\right] \quad (2.21)$$

where σ_x^2 is the power of the input signal, σ_e^2 is the quantization noise power, f_s is the sample rate, and B is the signal bandwidth. The SNR improvement with oversampling is $(6L+3)$ dB or $L+1/2$ bits. In practice, first-order modulators are seldom used because they exhibit output noise at discrete frequencies (idle tones). Higher order converters alleviate this problem and offer higher SNR, however stability is more difficult to achieve (and analyze) and they have a higher sensitivity to nonidealities in the analog components comprising the integrator. Lower order modulators may be cascaded [17] to form converters with good SNR performance and good stability.

Because one bit A/D and D/A converters have perfect differential nonlinearity, the dynamic range of sigma-delta converters is very high (from 60 to greater than 100dB), making them attractive for digital radio applications. Sigma-delta converters most often use switched-capacitor integrators, and the slew-rate and settling time limitations of the opamps which comprise them limit typical input frequencies to a few hundred kHz. For radio applications, this has limited the use of such converters to narrowband radios in the baseband portion of the receiver. In [18], an integrated

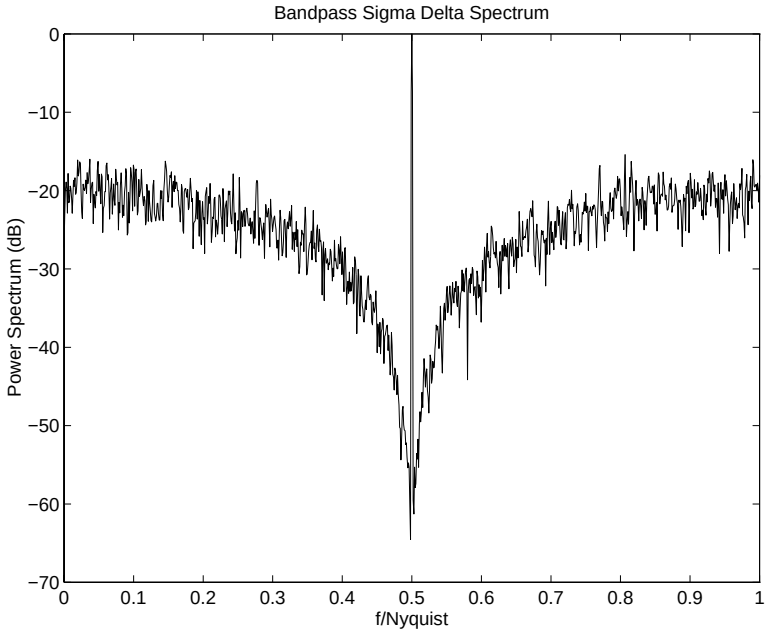


Figure 2.18: Bandpass Sigma Delta A/D Output Spectrum

transceiver which included dual baseband third-order sigma-delta converters with 82dB of dynamic range and a sample rate of 4.86MHz is described. Analog Devices has a similar IS-54 receive chip (AD7013) with dual sigma-delta converters which have 70dB of dynamic range and consume 45mW at 5V. Engineers at Analog Devices have also developed an integrated GSM baseband chip which includes seventh-order baseband sigma-delta converters with an oversampling ratio of 20 with 75dB dynamic range and 94mW power dissipation [19]. Lowpass converters with quadrature sampling clocks have been proposed to implement a direct conversion (zero-IF) receiver [20].

In addition to their high dynamic range, sigma-delta converters have the unique ability to quantize bandpass signals with very high resolution. This is done by altering the frequency response of the noise transfer function to provide high loop gain at some center frequency of interest. As shown in Figure 2.18, this causes the quantization noise to be rejected at frequencies near the center frequency, instead of near DC as with the lowpass sigma-delta converter. Bandpass sigma-delta converters are very promising for radio applications as they are able to convert bandpass modulated signals with high dynamic range at IF in a receiver without having to convert the signal to baseband, thus allowing highly integrated, low cost radio receivers. Bandpass

sigma-delta conversion was first proposed in 1989 by Schreier and Snelgrove [21]. Bandpass converters with second-order switched-capacitor (SC) integrators have been published for GSM with center frequencies of 2.5MHz to 10.7MHz with SNR's from 45-55dB in a 200kHz bandwidth [21, 22]. For IS-54, a bandpass fourth-order converter with integrated digital downconversion was published which achieved 98dB of SNR in a 30kHz bandwidth at a low IF of 1.8MHz [23].

In [24], channel tuning by variation of the sample frequency and noise transfer function was proposed. The use of complex-valued noise transfer functions has been proposed to allow improved stability with higher order noise shaping [25, 26]. Bandpass converters often use a sample rate at four times the IF to facilitate a simple lowpass to bandpass transformation and to allow simplified digital down conversion (as will be elaborated upon in the next chapter). This limits the use of ordinary switched-capacitor sigma-delta converters to low IF frequencies. However, a fourth-order bandpass converter which under sampled a 10.7MHz IF at 4.71MHz while oversampling a 200kHz bandwidth signal was presented in [27]. An alternative to under sampling is to use continuous-time integrators in place of the switched capacitor integrators, as they are capable of higher frequencies. Both Gm-C based resonators [28] and LC resonators [29, 30] have been implemented. The use of SiGe heterojunction bipolar transistor (HBT) has even made possible the prospect of bandpass sigma-delta converters which operate directly on 1GHz carrier frequencies to digitize 10MHz bandwidths with 49dB SNR [31].The disadvantage of continuous-time integrators is the need for off-chip components and resonator tuning. Recently, bandpass converters utilizing second-order bipolar switched-capacitor resonators have demonstrated 40dB SNR in a 1MHz bandwidth at a frequency of 62.5MHz with a sample rate of 250MHz, showing promise for high frequency operation of sampled-data bandpass resonators.

A sigma-delta technique particularly useful for angle modulated signals has been proposed by Galton [32] in which the instantaneous frequency of a modulated bandpass signal is digitized using sigma-delta techniques. The technique is capable of high-frequency operation and exhibits the same noise shaping properties as conventional sigma-delta converters.

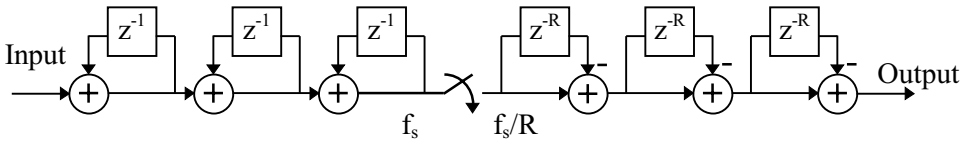


Figure 2.19: Block Diagram of a Third-Order Cascade Integrator Comb (CIC) Filter

Decimation for Sigma-Delta Converters

The sigma-delta modulator is only half of the sigma-delta A/D converter. To reconstruct the digitized signal with high SNR, the out of band quantization noise must be rejected by filtering and decimation from the oversampled rate to the Nyquist rate of the signal of interest. To minimize power and complexity, the Cascaded Integrator Comb (CIC) filter of Figure 2.19 is often used [33]. The filter shown is third order and contains three integrators followed by a decimation by R and three differentiators. The third-order CIC filter has a transfer characteristic

$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}}\right) \tag{2.22}$$

and a frequency response as shown in Figure 2.20. More filtering is often used after the CIC filter to provide additional rejection of adjacent channels and to compensate for the gain droop in the passband from the CIC filter. The advantage of the CIC filter lies in its simplicity; only adders and registers are required, and no full multipliers are needed.

In this chapter we have presented some of the background theory of analog to digital conversion and outlined some of the A/D techniques which are promising for use in baseband and IF digitization. Now we will proceed to examine the nature of the cellular signals we are seeking to digitize, and some digital receiver architectures which include A/D conversion.

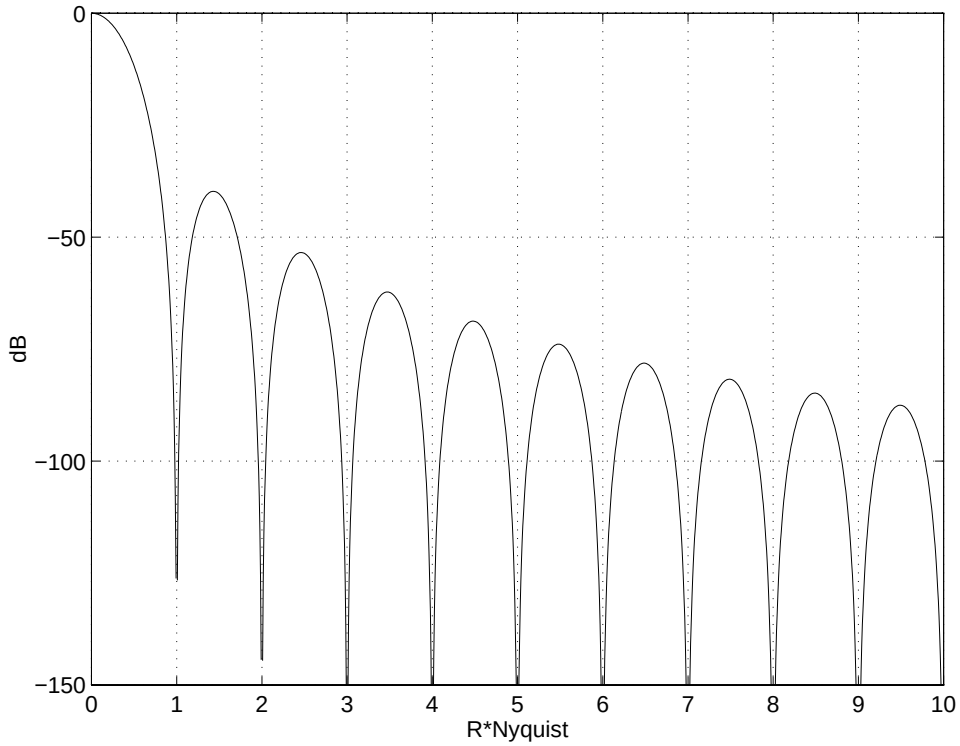


Figure 2.20: Frequency Response of a Third-Order Cascade Integrator Comb (CIC) Filter

Chapter 3

Cellular Radio Signals and Receiver Architectures

The overall receiver architecture in which the analog-to-digital converter operates in a DSP-based receiver makes a great deal of difference in the performance demanded of the converter. Therefore, in this chapter, some digital receiver architectures will be introduced. Additionally, the signal formats and receiver requirements for the most popular cellular standards will be examined.

3.1 Cellular Radio Signals

In this section, we will describe the signal formats for the Advanced Mobile Phone System (AMPS), US Digital Cellular (USDC), Global System for Mobile (GSM), and Code Division Multiple Access (CDMA) standards [34]. This is not intended to be an exhaustive description of each standard, but will instead concentrate on those aspects of each system which impact the performance required of the A/D interface in the receiver.

3.1.1 Advanced Mobile Phone Service (AMPS)

AMPS is the first generation cellular standard in the United States, and uses analog Frequency Modulation (FM) as a signal format. While newer digital standards offer improved performance and capacity, AMPS service will likely persevere in many locations where the cost of system upgrading may not be warranted. Thus AMPS will

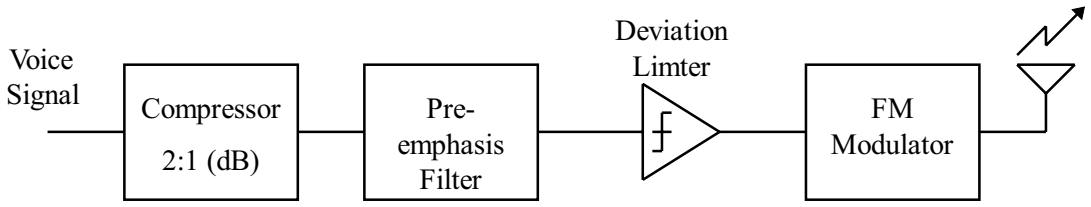


Figure 3.1: AMPS Transmitter Block Diagram

remain the only unifying standard, and newly developed multimode cellular receivers must be capable of demodulating AMPS signals.

A block diagram of the modulation process for AMPS is shown in Figure 3.1. A voice signal is first companded using a compressive amplifier whose output increases 1dB for every 2dB change in input amplitude to limit the dynamic range of the voice signal. The resulting signal is passed through a pre-emphasis filter and deviation limiter before being modulated with an FM modulator. The deviation limiter limits the peak frequency deviation to $\pm 12kHz$. AMPS uses frequency division multiple access (FDMA) with 30kHz channel allocations and frequency duplexing with 869-894MHz for the forward channel and 824-849MHz for the reverse channel.

3.1.2 U.S. Digital Cellular (USDC)

The U.S. Digital Cellular (USDC) standard is a Time Division Multiple Access (TDMA) standard which is implemented as interim standard EIA/TIA[1] IS-54[2], a dual-mode standard which includes USDC and AMPS compatibility to allow service providers to progressively deploy the new digital service. The channel spacing (30kHz) and operating bands are the same as AMPS to allow compatibility. IS-54 uses a variant of differential phase-shift keying known as $\pi/4$ DQPSK which allows simple noncoherent demodulation which is robust in mobile fading channels. The constellation diagram for $\pi/4$ DQPSK is shown in Figure 3.2. While the constellation has eight discrete points, only phase transitions of $\pm\pi/4$ and $\pm 3\pi/4$ are allowed from any point. Pulse-shaping is performed to limit the transmission bandwidth while

[1]Electronic Industry Association/Telecommunications Industry Association

[2]The latest version of the U.S. dual mode cellular standard is IS-136, which makes minor modifications to IS-54 at the network level, but is identical in terms of the air interface.

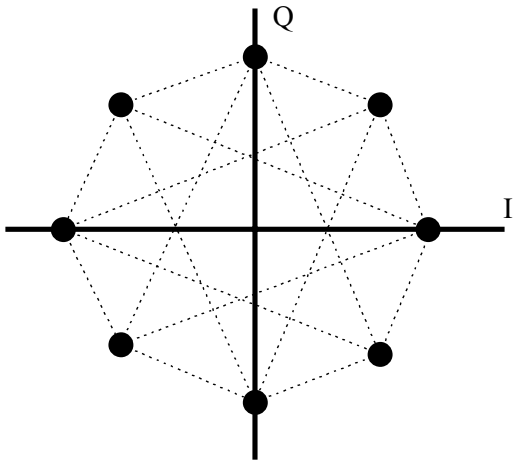


Figure 3.2: Constellation Diagram for $\pi/4$ DQPSK

controlling intersymbol interference (ISI) with a square-root raised-cosine filter with a 0.35 rolloff factor. Three users are supported per carrier using TDMA and the channel symbol rate is 24.3K symbols/s.

3.1.3 Global System for Mobile (GSM)

The GSM system has found wide acceptance abroad as a second-generation digital cellular standard. It uses Gaussian shaped Minimum Shift Keying (GMSK) with a symbol time-bandwidth product of 0.3. GMSK is a power efficient constant-envelope modulation scheme allowing nonlinear amplification with little spectral regrowth. The channel spacing for GSM is 200KHz, with the band from 890-915 MHz allocated for the reverse channel and 935-960 MHz for the forward channel. GSM uses eight 577μs slots per 4.615ms frame, with an aggregate data rate of 270.8kbits/s.

3.1.4 IS-95 CDMA

IS-95 is substantially different than the narrowband standards previously considered. IS-95 is a Direct Sequence Spread-Spectrum (DSSS) Code Division Multiple Access (CDMA) standard which allows co-channel users to be distinguished by unique pseudorandom noise (PN) spreading codes. This allows a frequency reuse of one, which

in addition to Voice Activity Detection (VAD) [3] promises to provide substantial improvements in capacity over competing systems[35].

IS-95 uses different schemes for the forward and reverse links to optimize performance of the system while allowing for simpler mobile hardware (relative to the base) to minimize cost and power. Because we are considering mobile receivers, we shall restrict ourselves to the forward link. The block diagram of the IS-95 forward link transmitter is shown in Figure 3.3[36, 37].

[3]Voice Activity Detection blanks transmission during dead spaces in conversation to improve capacity.

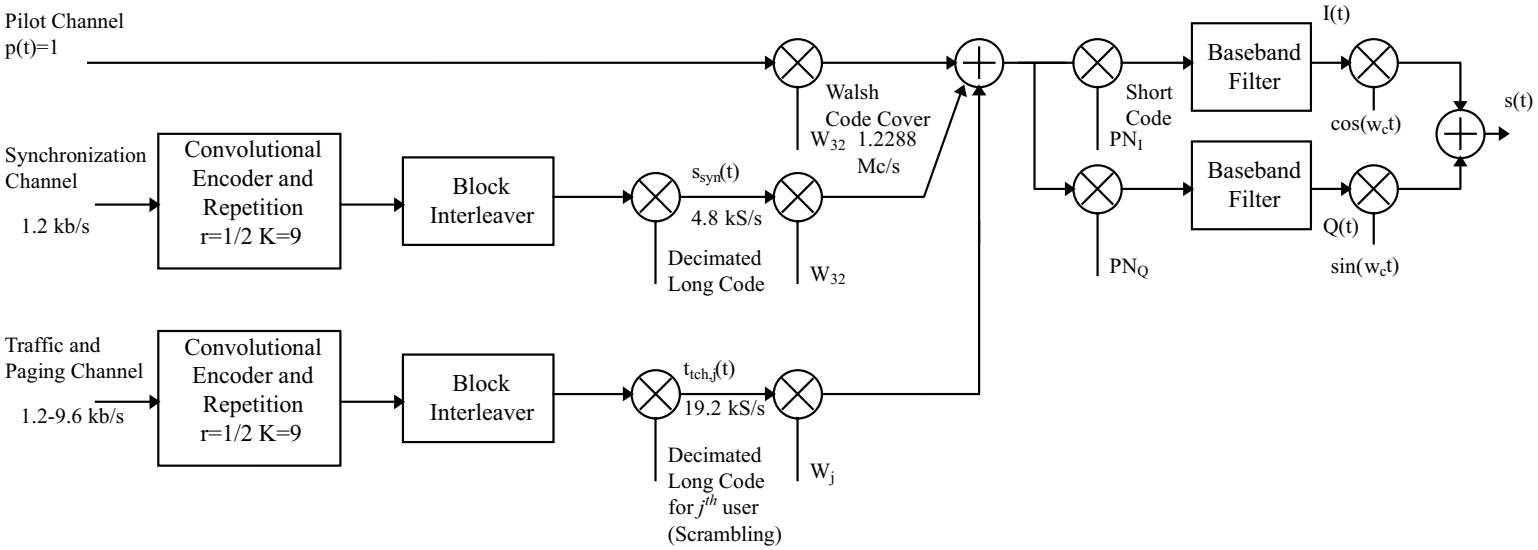


Figure 3.3: IS-95 Forward Channel Processing

The composite transmitted waveform consists of a pilot channel, a synchronization channel, and a traffic and paging channel. The pilot channel is used in carrier acquisition and to allow the receiver to derive an estimate of the channel. The synchronization channel is a dedicated channel to aid synchronization and tracking in the receiver. Up to 63 users are carried by the traffic and paging channels. Users are distinguished by unique Walsh codes, denoted W_j in Figure 3.3. Walsh codes are a class of orthogonal codes which with rectangular pulse shaping and perfect synchronization provide zero cross correlation between the desired user and interfering users at the mobile receiver. In the figure, the traffic channels with rates from 1.2kb/s to 9.6kb/s are first convolutionally encoded with a rate 1/2 constraint length 9 convolutional encoder , packetized into 20-ms blocks, and interleaved with a block interleaver. From the interleaver, a long $(2^{42}-1)$ pseudorandom code is used as a privacy mask but does not spread the data. Each bit stream is then spread with a unique 1.2288Mchip/s Walsh spreading code for a net processing gain of 64 (18dB). The traffic channels are added to the synchronization channel which is spread with W_{32} and the pilot channel which is spread with Walsh code W_0 (an "all ones" sequence). This composite signal is multiplied by distinct short $(2^{15}-1)$ pseudo-noise (PN) sequences PN_I and PN_Q at the same rate, and the resulting signals are input to a quadrature modulator after pulse shaping with root raised-cosine filters with r=0.35. Because each cell uses a different time offset of the short PN code, the Walsh code may be reused in adjacent cells. An additional purpose of the short code is to improve the spectral properties of the signal, as Walsh codes do not have good autocorrelation properties. The resulting complex baseband signal is

$$s(t) = (PN_I(t) + jPN_Q(t)) \left[p(t) \cdot W_0 + s_{syn}(t) \cdot W_{32} + \sum_{\substack{j=1 \\ j \neq 32}}^{63} t_{tch,j}(t) \cdot W_j \right] \quad (3.1)$$

At the receiver the resulting signal is relatively noiselike, with a high peak to average ratio. A three-tap rake receiver is specified at the mobile to provide mitigation of multipath propagation. Sophisticated open loop and closed loop power control is necessary in IS-95 to prevent nearby users from dominating the correlation of the signal received at the base and reducing capacity.

3.1.5 Cellular Signal Environment

If only channel noise corrupted a cellular signal, cellular receivers would not need much dynamic range and only a few bits would suffice to digitize the cellular signal. However, interference and fading due to multipath place increased demands on the receiver. Consider Figure 3.4 which depicts a typical cellular system with idealized hexagonal boundaries. The allocated frequency channels in an AMPS, GSM, or USDC cellular system are divided among a group of cells (termed a cluster) so adjacent cells do not use the same channels. The channel is reused, however, in an adjacent cluster resulting in some amount of co-channel interference. Because this is typically 9-18dB below the desired signal, co-channel interference does not tax the dynamic range of the analog components in a cellular receiver. However, channels at different frequencies are used in adjacent cells and by different mobiles within a cell.

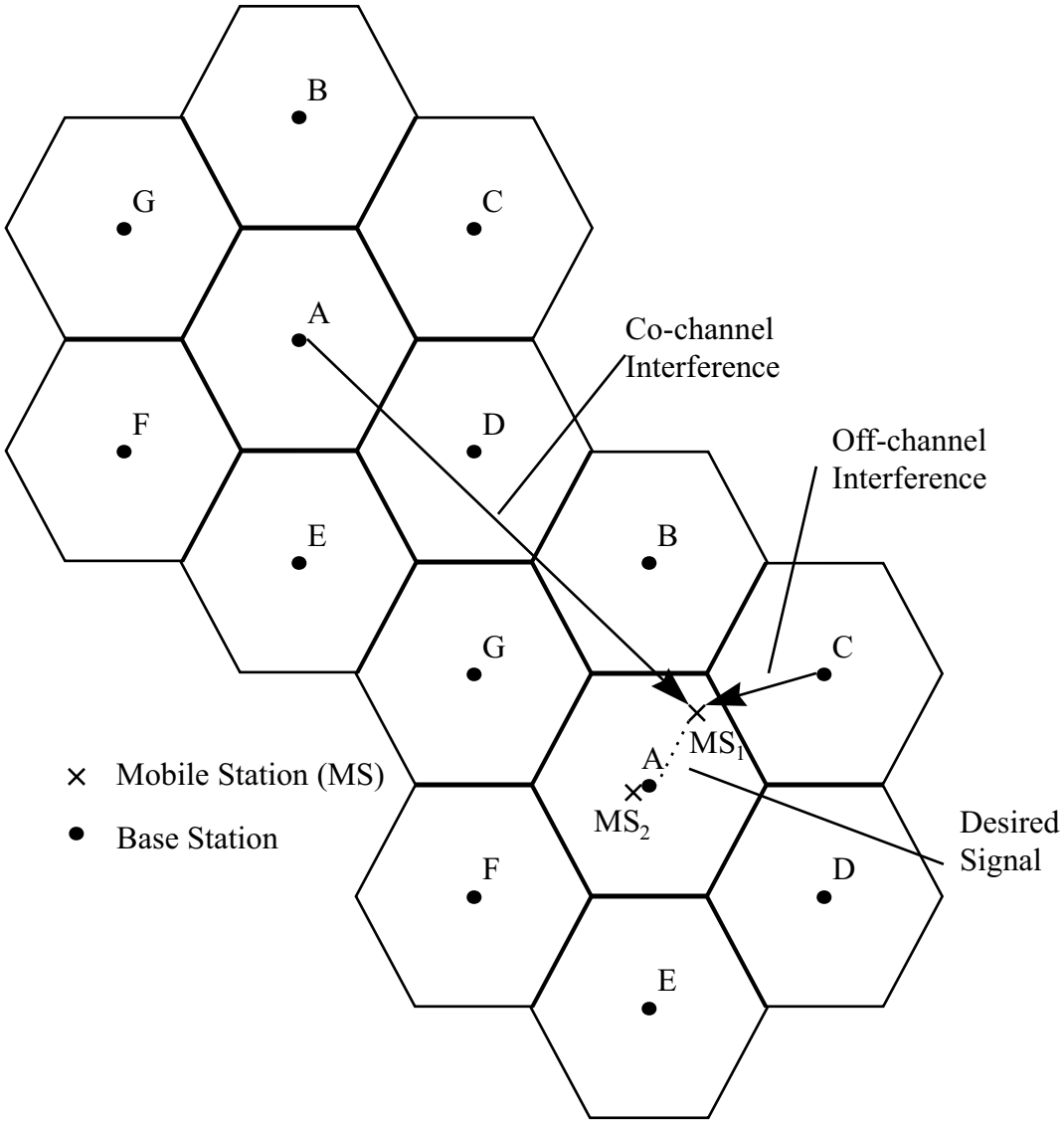


Figure 3.4: Cellular System Layout and Origin of Interference

At the base station "A" in Figure 3.4, the received power from an individual mobile can be predicted with the simple path loss model

$$P_r(d) = P_r(d_o)\left(\frac{d_o}{d}\right)^n \tag{3.2}$$

where P_r is the received power at a distance d, $P_r(d_o)$ is the power at a reference distance d and is a function of the transmitted power and the antenna gain, and n is a path loss exponent which has typical values of 2-4 [34]. Thus the power difference from a nearby mobile can be significantly stronger than a mobile near the cell boundary, with a relative power in dB given by

$$\frac{P_1}{P_2} = 10n\log_{10}\left(\frac{d_2}{d_1}\right) \quad (dB) \tag{3.3}$$

This results in significant off-channel interference which must be rejected by filtering somewhere in the receiver chain prior to demodulation. Smart frequency planning strives to allocate channels within a cell (and where possible, in neighboring cells) as far apart as possible to avoid strong adjacent (nearest neighbor) and alternate (next-nearest neighbor) channel interference[34]. The interference present in a cellular receiver is illustrated in Figure 3.5.

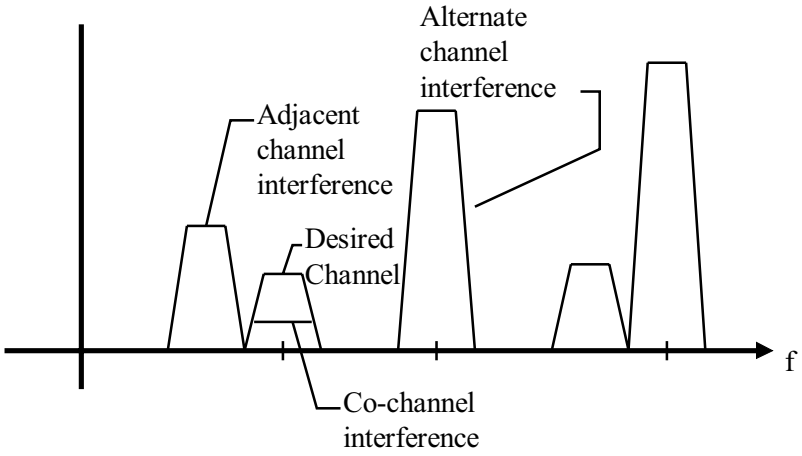


Figure 3.5: Interference in a Cellular Environment

Ideally, the worst case situation for off-channel interference for the mobile receiver occurs when a mobile is at a cell boundary. In this circumstance, the distances between desired and interfering bases are equal[4] and our simple model would predict equal desired and interfering powers. However, because of variations in the channel (i.e., the possibility that the mobile could be partially shadowed from the desired base station), adjacent and alternate interference can be present at levels much higher than the desired signal. The power difference is not as high as is seen in the received signal of the base station, where signals from nearby and distant users can arrive at vastly different power levels (near-far problem). In the final section of this chapter, the interference specifications for the standards under consideration will be reviewed in more detail.

The situation described above does not apply to IS-95 because adjacent cells are able to use the same frequencies. Additionally, mobiles at disparate locations do not present with vastly different power levels at the base because of the use of sophisticated open loop and closed loop power control. A different dynamic range challenge exists for IS-95, however, when an IS-95 system is deployed in an overlay situation in which it must coexists with an existing AMPS installation. In this case, strong narrowband interference can be present in band with the desired spread-spectrum signal. If the front-end of the receiver is linear prior to despreading, the processing gain of the spread spectrum system can reject narrowband interference. However, if the interference causes gain compression in the RF stages or overloads the A/D converter, blocking will occur.

3.1.6 The Mobile Communication Channel

In addition to interfering signals, impairments introduced by nonideal propagation cause difficulties in the design of radio receivers for cellular systems. In particular, fading due to multipath propagation causes fluctuations in the received signal power of narrowband signals (flat fading) and intersymbol interference due to frequency selective fading. The characteristics of the mobile channel vary with the propagation environment and the speed at which the mobile is moving relative to the base. In

[4]No adjacent or alternate channel interference is present from other mobile stations because the standards considered use Frequency Division Duplexing with a 45MHz offset between the forward and reverse channels

dense urban environments with many scatterers, strong multipath components exist and can occur with large delays. For channels in which the delay spread is less than a symbol period (narrowband channels), flat fading occurs and all frequencies of the signal are affected equally. The result is a variation in the received signal envelope which is often modeled with a Rayleigh distribution. A complete channel model is shown in Figure 3.6, where individual multipath components occur with delays $(\tau_1 ... \tau_n)$ and with amplitudes $(a_0, a_1, ..., a_n)$. Each multipath component has a Rayleigh distributed amplitude. Intersymbol interference is mitigated in IS-54 and GSM with the use of adaptive equalization. In IS-95, a three-tap rake receiver in the mobile combines the power from the three strongest multipath components coherently to improve the performance in a multipath channel. In addition, the rake receiver is used to simultaneous receive signals from multiple basestations to facilitate soft handoff.

Frequency-selective fading does not create difficulties for the analog components in the receiver or the A/D converter. However, variations in the received power due to flat fading require that additional dynamic range margin (fade margin) be designed into the receiver. Also, because interfering signals fade independently, the relative interference to desired signal power is time-varying and can cause significant interference problems in the mobile receiver when the desired signal is in a fade and an interferer is unfaded.

3.2 Digital Receiver Architectures

The most commonly used radio architecture is the superheterodyne. In Figure 3.7, a superheterodyne receiver with its essential components is illustrated. The input RF signal is first bandpass filtered to eliminate signals out of the band of interest, most especially the signal at the first image which is twice the IF away from the tuned signal. The signal is then amplified with a low-noise amplifier (LNA) which sets the noise floor of the system and then mixed to an intermediate frequency. By mixing to a fixed IF at a lower frequency, high quality filtering may be performed with an IF filter to provide good adjacent channel selectivity. Also, translation to a lower frequency allows the signal to be digitized with a practical A/D or demodulated more practically in the case of analog demodulation. The signal is then passed through an

Automatic Gain Control (AGC) amplifier whose gain is set with a feedback algorithm to optimize the dynamic range of the system. The signal may be downconverted one or more additional times to allow improved sensitivity and selectivity in the receiver.

At the final IF in a receiver, the signal may be directly demodulated using an analog demodulator, quadrature downconverted and digitized, or directly digitized. While analog demodulation offers the benefits of low complexity and low power for portable applications, it suffers from analog circuit imperfections and the inability to be reconfigured for different modulation schemes. For these reasons, the latter two schemes are of greater relevance.

3.2.1 Baseband A/D Conversion

Figure 3.8 shows a heterodyne receiver with analog quadrature downconversion. The IF signal in this scheme is mixed to baseband with a pair of analog mixers whose reference signals are $cos(2\pi f_{IF}t)$ and $-sin(2\pi f_{IF}t)$ respectively. The baseband signals are then lowpass filtered for antialiasing and/or channel filtering and then digitized with two A/D converters. After conversion, the digital baseband signals can be further processed with additional digital channel filtering. The resulting signals are the in-phase and quadrature (I and Q) components of the modulated signal and hence can be processed digitally to extract the message signal for any modulation scheme.

3.2.2 IF A/D Conversion

Figure 3.9 shows an alternative architecture in which the IF signal is directly digitized. After analog-to-digital conversion, the IF signal is digitally downconverted to baseband I and Q components. This is performed by digital multiplication of the IF signal with quadrature references generated by the Numerically Controlled Oscillator (NCO). Filtering and decimation are performed after downconversion to reject adjacent channel interference.

The primary advantage of the analog quadrature downconversion scheme is that the A/D converters operate at the baseband rate. However, the analog scheme has a serious limitation due to phase and gain imbalances in the analog downconverter and A/D converters. These imbalances can cause significant distortion in the received signal. Because the digital IF scheme performs these functions digitally, no such

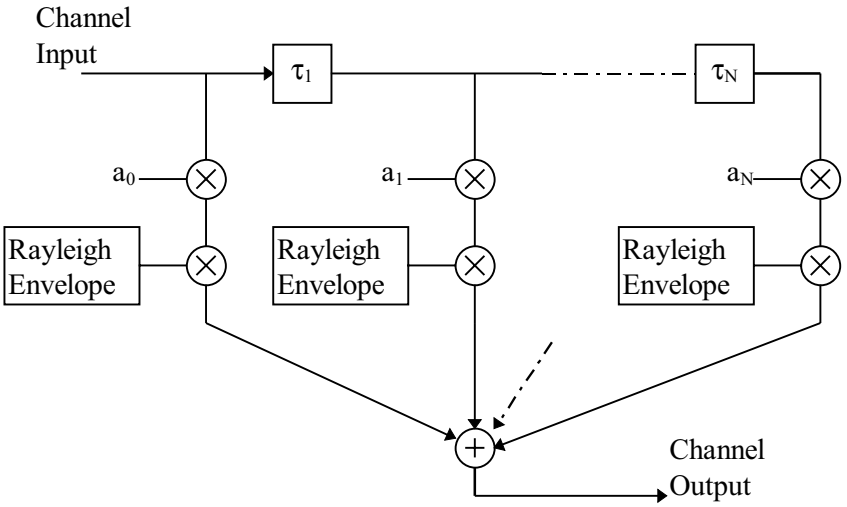


Figure 3.6: Multipath Propagation Model

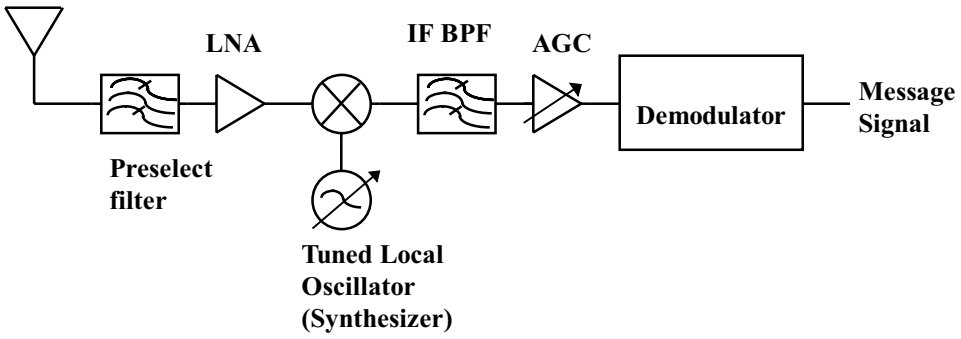


Figure 3.7: The Superheterodyne Receiver

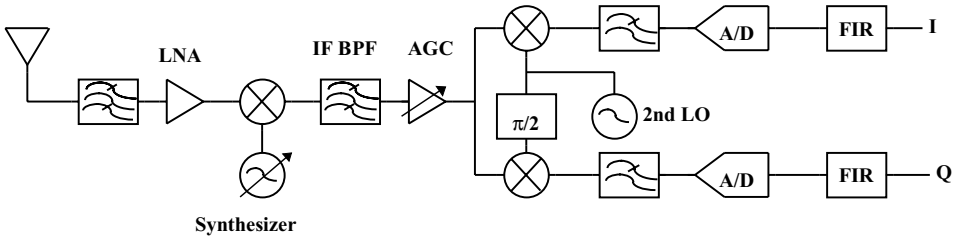


Figure 3.8: Receiver with analog quadrature downconversion and baseband A/D conversion

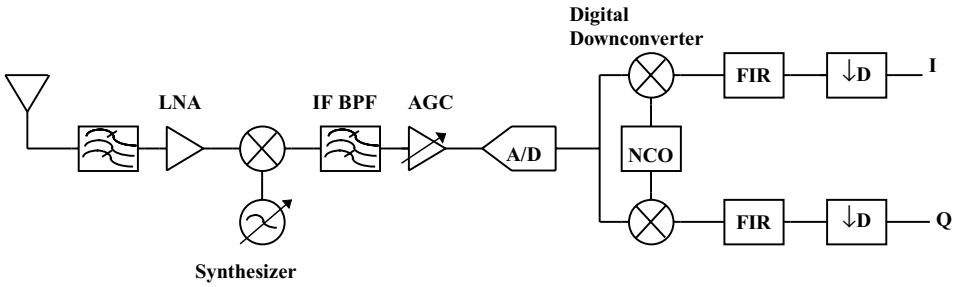


Figure 3.9: Receiver with IF A/D conversion and digital quadrature downconversion

limitation is present. However, the A/D must digitize the high frequency IF signal with high fidelity. The sample rate requirements for digitizing the bandpass IF signal were outlined in Chapter 2.

The digital downconverter using full digital multiplies is relatively complex and power hungry. For select relationships of the IF frequency and the sample rate, significant savings can be obtained [38, 39, 40]. For instance, Figure 3.10 illustrates the case when $f_s = 4f_{IF}$. In this case, the required multiplications reduce to the trivial cases of ± 1 and zero. Because the multiplication by zero need not be done at all, further simplification is possible by alternatively multiplexing the input samples to I and Q multipliers which alternately pass the sample unchanged or invert the sign. The resultant streams are effectively decimated by two from the original rate.

Clearly, sampling at four times the IF frequency is only practical for low IF frequencies which allow for practical A/D converters. By applying the constraints for bandpass sampling outlined in Chapter two and considering the output of the sampling operation to be at a digital IF for which we want $f_s = 4f_{DIF}$, we can derive other possible sample rates for which the simplified digital downconverter works. By choosing

$$f_s = \frac{4}{2n+1} f_{IF} \tag{3.4}$$

the simplified digital downconverter may be used, where n is a positive integer. Choosing n greater than zero allows the A/D converter to sample at a rate lower than the IF while still using the simplified downconversion scheme.

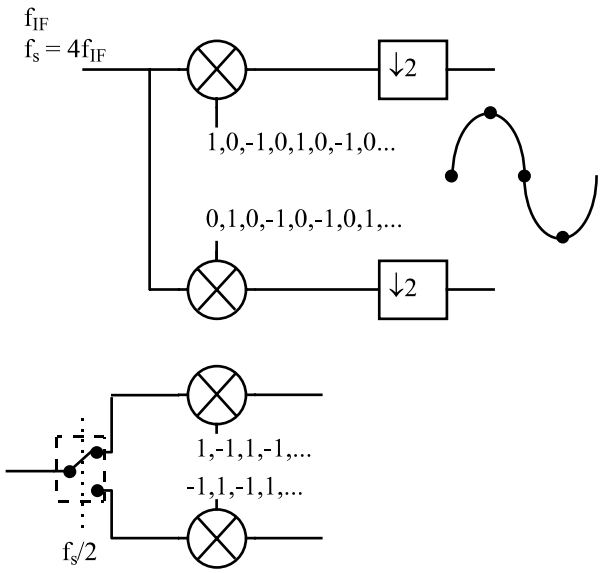
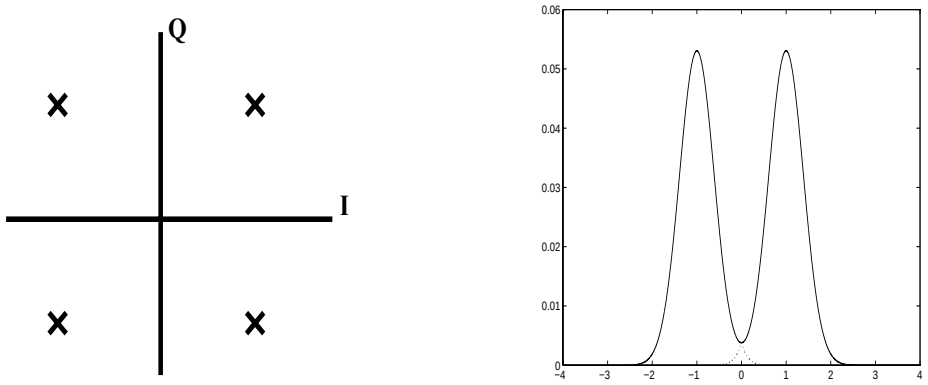


Figure 3.10: Simplified Digital Downconversion

3.3 The role of the A/D converter in a digital receiver

It is important to observe that the resolution required of the A/D converter in the above architectures is highly dependent upon the processing performed upon the signal before and after the A/D, the type of modulation scheme used, and the type of channel model considered. For example, consider a QPSK modulation scheme with the constellation shown in Figure 3.11. Assuming no interference, an additive white Gaussian noise (AWGN) channel, ideal lowpass channel filtering and baseband digitization with ideal sampling at one sample per symbol, the pdf of the input to the digitizer consists of two Gaussians centered about the two states of the symbol as shown in Figure 3.31. Under these assumptions, clearly only two levels (one bit) are required from each quantizer and the quantizer is actually acting as a decision device in this optimal coherent demodulator[41].

The output versus input SNR for the "quantizer" in this case does not provide any insight into the performance of the entire system. Consider, however, the case when adjacent channel interference is introduced and the analog filters are not ideal but allow significant interference into the A/D converter. Prior to detection, the



(a) (b)

Figure 3.11: QPSK (a) signal constellation and (b) pdf of I or Q baseband signal in AWGN Channel

interference can be rejected with digital filtering provided after the A/D converter. Now the SNR for the converter is a more useful metric because the converter is operating as a reconstruction device and cannot perform a simple thresholding of the signal.

3.4 Dynamic Range and Automatic Gain Control

Having examined the hostile signal environment and architecture of cellular receivers, we are now in a position to define the dynamic range requirements and tradeoffs. The general term *dynamic range* actually refers to several different things [42]. The *total* dynamic range is the difference between the maximum and minimum signal at the input of the receiver, i.e.

$$DR_{total} = P_{max} - MDS \tag{3.5}$$

where MDS refers to the Minimum Detectable Signal, equal to the noise floor of the receiver in dBm, P_{max} is the maximum expected input power in dBm and DR_{total} is the total dynamic range in dB. If ideal AGC was used at the front of the receiver, then DR_{total} could be made arbitrarily high.

In calculating the total dynamic range, the maximum and minimum signals are not present simultaneously at the input of the receiver. If however, strong interfering signals are present while we are trying to receive a weak signal, we are interested in

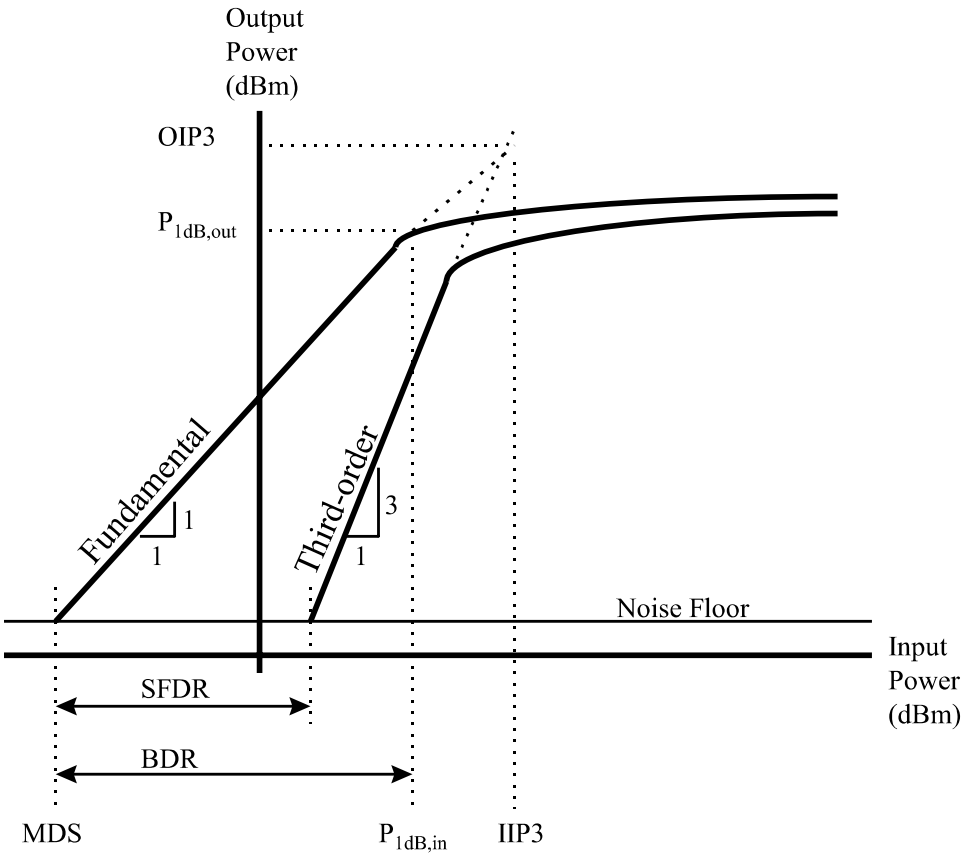


Figure 3.12: Dynamic Range Definitions

the maximum ratio of interfering signal to desired signal that results in acceptable receiver performance. In this case, two other instantaneous dynamic range metrics are useful: Blocking Dynamic Range (BDR) and Spurious Free Dynamic Range (SFDR). For analog receivers (or individual RF components) which can be characterized by an overall compression point and intercept point, Figure 3.12 illustrates the difference between BDR and SFDR. Here the output power versus the input power of the fundamental and third-order products are plotted. $P_{1dB,in}$ and $P_{1dB,out}$ are the input and output 1dB compression points respectively. $IIP3$ is the input third-order intercept point and $OIP3$ is the output referred third-order intercept.

From the geometry of the figure,

$$BDR = P_{1dB} - MDS \tag{3.6}$$

and

$$SFDR = \frac{2}{3} IIP_3 - MDS \tag{3.7}$$

where IIP_3 is the input referred third-order intercept point. During blocking, a strong interferer causes the receiver to be pushed into compression, which reduces the gain to the desired signal. The SFDR characterizes the range of inputs over which the distortion products due to intermodulation remain below the noise floor.

For an A/D converter, the full scale range of the converter is analogous to the compression point. However, because the distortion products do not behave as ordinary power-law devices the converter cannot be characterized by a third-order intercept; therefore Equation 3.7 does not apply.

AGC does not improve the instantaneous dynamic range (BDR and SFDR) of the receiver as diagrammed in Figure 3.13. The gain of the AGC amplifier is set based upon the total envelope of the signal presented to the A/D converter to avoid overload. In case (a), only the desired signal is present and the gain is set at some level G_1 which is assumed to provide a full scale input to the A/D converter. In case (b), strong interference is introduced. To prevent overload, the gain must be reduced and the level of the desired signal is decreased. If the interference reaches a significantly high level, the quantization noise of the A/D converter can mask the desired signal. Filtering prior to the A/D converter (or other dominant nonlinear device) does improve the BDR and SFDR, however.

The influence of flat fading on the performance of the A/D converter when no interference is present can be reduced by the AGC provided that the AGC time constant is small relative to the fade duration. A typical Rayleigh fading envelope is depicted in Figure 3.14. The average time between successive fades is given by the one-half the reciprocal of the Doppler frequency, which is

$$f_d = f_c \frac{v}{c} \tag{3.8}$$

where f_d is the Doppler frequency, f_c is the carrier frequency, v is the velocity of the mobile in the direction of the base and c is the speed of light. Typical values are $v = 100 km/hr$, which gives f_d around 80Hz for signals at cellular frequencies

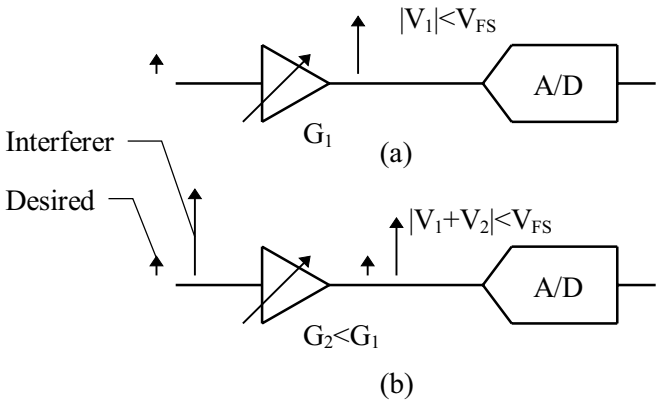


Figure 3.13: AGC Response to a Blocking Interferer

($\tilde{9}$00MHz). Thus successive fades occur about every 6.25ms. If the AGC time constant is much less than this, then the envelope of the desired signal will be better controlled into the A/D. If the AGC is not fast enough to compensate channel variations, the total dynamic range of the A/D must be large enough to accommodate fading and the average gain must be set to keep the signal from excessive overloading as depicted in Figure 3.14.

3.5 Cellular Radio Mobile Receiver Specifications

To ensure proper operation of cellular radio receivers in service, the organizing bodies responsible for each of the cellular standards have created recommendations for cellular radio performance. To asses the performance of A/D converters for each of the standards, we have used these recommendations to define the limits of acceptable performance. Thus we will briefly review the relevant portions of each recommendation, including the manner in which parameters are tested and the specified limit for each.

3.5.1 General Test Methods

All of the standards follow more or less similar procedures for conformance testing. We will concentrate primarily on sensitivity, blocking dynamic range (or selectivity), and intermodulation performance, since the A/D will most strongly impact these

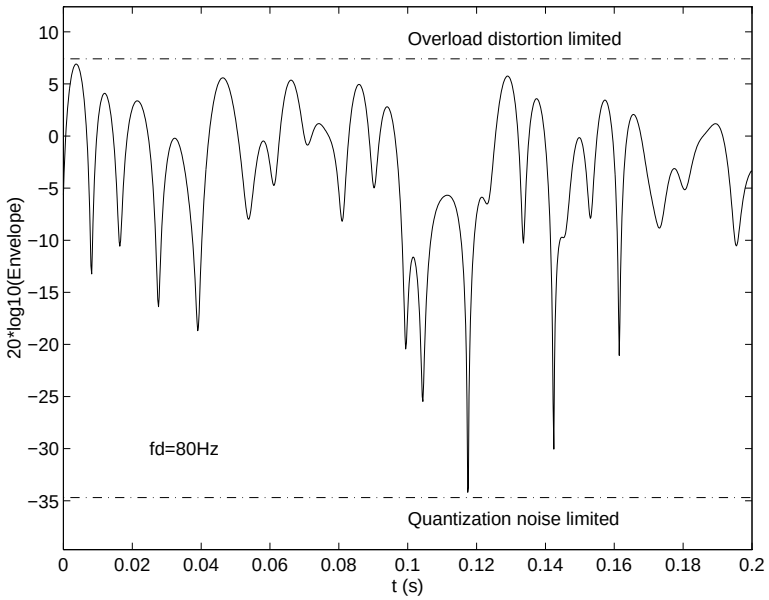


Figure 3.14: Rayleigh Fading Envelope

measures.

In all of the standards, sensitivity is measured by applying a single desired modulated signal to the receiver and increasing its power until some performance level (such as Bit Error Rate (BER)) is met. The sensitivity is defined as the minimum power needed to attain the specified performance. Variations include additional specifications for fading conditions, or that the BER must be better than some value at a specified input power.

The blocking measurement is typically made with a desired signal 3dB higher than the reference sensitivity power. An interfering modulated signal is added at a specified offset, and its power is increased until the reference performance metric (i.e. BER) drops to a specified level. The selectivity (blocking) is defined as the difference in dB between the interfering power at the threshold BER and the reference sensitivity power. Adjacent and alternate channel interference is typically tested, and in some cases farther off-channel blocking is also specified.

The typical intermodulation measurement proceeds similarly to the blocking measurement with a desired input 3dB higher than the sensitivity level. Two equal power

interferers (one CW and one modulated) are input to the receiver at specified frequencies such that their intermodulation products (i.e. $2f_2 \pm f_1$) fall on the signal of interest. There powers are increased until the minimum performance criterion is not met. The intermodulation response is defined as the power of the interferers at the minimum performance criteria and the reference sensitivity.

While the specifications for each of the standards follow in general ways the procedures described above, there are several differences to note. Table 3.5.1 provides a summary of the different cellular specifications. We will briefly point out unique aspects of each of the standards.

Table 3.1: Summary of mobile cellular receiver performance requirements

Parameter		AMPS[43]	USDC[43]	GSM[44]	IS-95[45]
Sensitivity	Limit	-116dBm	-103dBm 8/100km/hr -110dBm static	-104dBm nom (ref+20dB) BER $< 10^{-5}$	-104dBm/1.23MHz
	Criteria	12dB audio SINAD	3% BER	2% BER static 8% BER urban 50km/hr 7% BER rural 250km/hr 9% BER hilly 100km/hr	0.005 FER
	Conditions	1kHz audio input ±8kHz deviation	48.6kB/s $\pi/4$ DQPSK PRBS	GMSK PRBS	Pilot E_c/I_{or}=-7dB[1] Traffic E_c/I_{or}=-15.6dB
Blocking	Limit offset	16dB (± 30kHz) 60dB (± 60kHz)	-94dBm (± 30kHz) -64dBm (± 60kHz)	-38dBm (600-800kHz) -33dBm (800kHz-1.6MHz) -23dBm (1.6-3MHz) -23dBm (>3Mhz)	0.01 FER
	Conditions[2]	Pd=ref+3dB	Pd=-107dBm	Pd=ref+3dB	30dBm tone ± 900kHz offset Pd=101dBm/1.23MHz
Intermod	Limit	65dB close 70dB wide	-45dBm	-43dBm	0.01 FER
	Conditions[3]	I1/I2 ±60/120kHz offset (close) I1/I2 ±330/660kHz offset (wide)	I1/I2 ±120/240kHz offset	I2-I1=800kHz I1 ±800kHz offset	±900/1700kHz offset S/I=-101/-40 S/I=-90/-32 S/I=-79/-21
		I1 CW I2 CW	I1 CW I2 $\pi/4$ DQPSK	I1 CW I2 GMSK	I1 CW I2 CW

[1] E_c = energy per chip, I_{or} = power spectral density of the total transmitted signal

[2] Pd=desired power, ref=reference sensitivity level

[3] I1 = interferer 1, I2 = interferer 2

3.5.2 AMPS

For the AMPS specifications, we have consulted the analog section of the IS-54 mobile receiver recommendations, IS-55-A [43].

Sensitivity

Sensitivity is defined as the minimum RF input level for which 12 dB audio SINAD is achieved. The input is modulated with a 1 kHz sinusoid to ±8 kHz deviation. The sensitivity is specified to be -116dBm or better.

Blocking

Blocking is tested with a 400Hz modulated interferer. Adjacent and alternate channel selectivity is specified at 16dB and 60dB respectively. Narrowband analog receivers can provide significant attenuation at alternate channel offsets with highly selective IF filters.

Intermodulation

Intermodulation response is divided into two classes: close-spaced (60/120 kHz offset) and wide-spaced (330/660 kHz offset) with CW interferers. The close and wide spaced specs are 65 dB and 75 dB respectively.

3.5.3 USDC (IS-54 Digital Mode)

Sensitivity

The reference sensitivity is specified for both a static channel (-110dBm) and a Rayleigh faded channel with speeds of 8 and 100 km/h. The performance threshold is 3

Blocking

The power of the desired user is set at -107dBm. The interference is set at -94dBm for (30kHz) adjacent channel offsets and -65dBm at an alternate (60kHz) offset. The BER standard is 3

Intermodulation

The intermodulation test is performed with a CW tone at an offset of 120kHz and a $\pi/4$ DQPSK interferer at 240 kHz offset both at -45 dBm (65 dB relative to reference sensitivity), and BER must again be less than 3

3.5.4 GSM

The GSM specification (GSM 05.05 [44] is substantially more involved than IS-54 spec, with more conditions tested and the use of more sophisticated fading models. Additionally, different specifications are given for different types of mobile and base stations.

Sensitivity

The GSM standard uses several classes of bits, based upon the importance of each for successful transmission and intelligibility. Different standards are used for sensitivity for each class of bits, with FER specified for coded bits and BER specified for others. To allow more practical simulation, we have restricted our attention to the full rate traffic channel (TCH/FS) class II bits, which are unprotected. The specified performance is summarized in Table 3.5.1. A nominal error rate of 10^{-5} is specified with an input at 20dB above the sensitivity level, and this performance must be maintained up to -15 dBm input level.

Blocking

Blocking performance is tested similar to the general case described above and the performance is summarized in Table 3.5.1.

Intermodulation

Intermodulation is tested with one CW interferer and one GMSK modulated pseudorandom bit stream.

3.5.5 IS-95

Performance requirements IS-95 conformant radios have been gleaned from TIA/EIA/IS-98-A [45]. The criteria to be attained is Frame Error Rate, which is measured using a Cyclic Redundancy Code (CRC).

Sensitivity

Sensitivity is tested by measuring the FER with an input power of -104dBm/1.23 MHz. Success is an FER better than 0.005. The total dynamic range is tested by repeating the test with an input of -25dBm/1.23MHz.

Blocking (Single Tone Desensitization)

Blocking is tested with a CW interferer at $\pm$ 900 kHz offsets with a power of -30dBm. The FER is required to be better than 0.01 with a -101dBm/1.23MHz input.

Intermodulation

Intermodulation spurious attenuation is tested with two CW interferers at 900 kHz and 1.7MHz offsets with a suite of input and interference powers as specified in Table 3.5.1.

With some understanding of the performance required of cellar receivers, cellular receiver architectures, and the cellular environment, we can now proceed to present the results of analysis and simulation of cellular receivers with A/D conversion modeled.

Chapter 4

Analysis and Simulation of Digital Receivers with A/D Conversion

In this chapter, we will establish the A/D performance requirements for cellular receivers. First, a simple linear model will be derived which provides an estimate of the A/D resolution required to achieve acceptable performance when blocking interferers are present. Because the assumptions of the model are often violated in practice, it is necessary to use simulation to investigate the performance of the receivers. Prior to presenting simulation results, some of the issues encountered in modeling A/D converters for simulation are discussed. The remainder of this chapter is devoted to describing Matlab simulations which were performed and presenting the results obtained for each of the standards.

4.1 Linear Analysis

Consider the multimode receiver in Figure 4.1. The analog front end is wideband to pass the widest standard of interest, and channel filtering is done digitally. At the input of the receiver are a desired signal and an off-channel interferer. To avoid overloading the A/D converter, the AGC attempts to regulate the peak signal envelope to be less than the full scale range of the converter. In Figure 4.1, the receiver is shown with the A/D converter modeled as an additive white noise source as presented in Chapter 2 and the receiver front-end is modeled with its equivalent gain and noise figure. The output of the A/D is passed through an ideal channel filter which

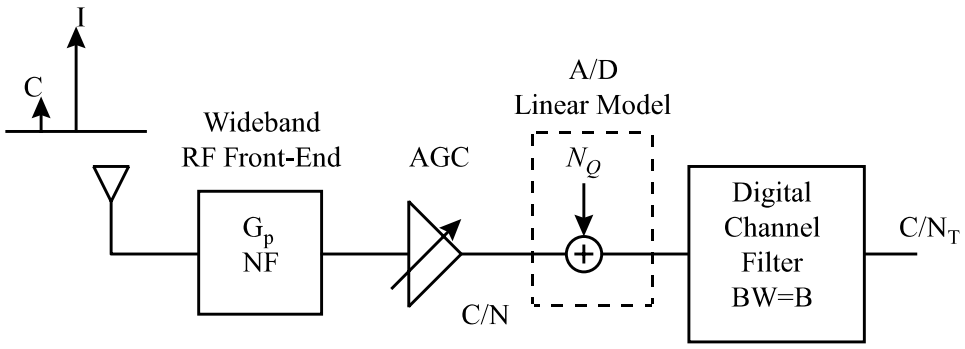


Figure 4.1: Linear Model for a Multimode Receiver

completely rejects the interference prior to demodulation. We are interested in the carrier to noise ratio of the desired signal at the input of the demodulator, denoted $\frac{C}{N_T}$. At the input of the A/D, the peak-to-peak envelope of the composite signal is constrained to be less than or equal to the full scale range V_{FS}. If we define η_T as the peak to average power ratio of the total signal at the input of the A/D converter, we have

$$\eta_T(C+I) = \left(\frac{V_{FS}}{2}\right)^2 \tag{4.1}$$

where C is the average power of the desired signal and I is the average power of the interfering signal.

With the carrier to interference ratio defined as $\frac{C}{I}$ we obtain

$$C = \frac{V_{FS}^2}{4\eta_T\left(1+\frac{1}{(C/I)}\right)} \tag{4.2}$$

The total noise N_T is the sum of channel noise N and quantization noise N_Q

$$N_T = N + N_Q \tag{4.3}$$

therefore the output carrier to noise ratio may be written as

$$\frac{C}{N_T} = \frac{C}{N+N_Q} = \frac{1}{\frac{N_Q}{C}+\frac{1}{(C/N)}} \tag{4.4}$$

where C/N is the carrier to noise ratio at the input of the A/D. From Chapter 2, the quantization noise power in the desired signal bandwidth B is

$$N_Q = \frac{\Delta^2}{12} \cdot \frac{B}{fs/2} \tag{4.5}$$

where Δ is the quantization stepsize given by $\Delta = \frac{V_{FS}}{2^b}$ for an A/D converter with b bits.

By combining 4.2, 4.4, and 4.5 we obtain the final result

$$\frac{C}{N_T} = \frac{1}{\frac{\eta_T(1+\frac{1}{(C/I)})}{3 \cdot 2^{2b}} \cdot \frac{B}{f_s/2} + \frac{1}{(C/N)}} \tag{4.6}$$

An alternative derivation can be performed in which the quantization noise of the A/D converter is used to compute the noise figure of the A/D and the overall noise figure can be computed of the cascade of RF front-end, AGC, and A/D[4, 46]. This is especially useful when the gain, noise figure, and intercept point of the components comprising the receiver are known. However, because the A/D distortion products do not behave as in a normal weakly nonlinear device, it is not possible to compute an overall third-order intercept point for the cascade.

To examine the implications of Equation 4.6, we begin by plotting the output carrier to noise ratio C/N_T versus input carrier to noise ratio C/N without interference ($C/I = \infty$) with $\eta_T = 2$ corresponding to the peak to average ratio of a single sinusoid. The result, shown in Figure 4.2, shows that at very low input carrier to noise ratios, the output noise is dominated completely by the channel noise and is independent of the resolution of the A/D[1]. At high C/N, the performance becomes dominated by the A/D quantization noise and is independent of channel noise. The critical observation is that for the typical region of interest ($C/N \leq 20dB$) for the systems we are considering, very little degradation is seen for resolutions of four bits or less. In Figure 4.2, critical sampling (i.e. $f_s = 2B$) is assumed; higher sampling rates will increase the effective resolution at a rate of 1/2 bit per octave of oversampling.

To examine the effect of interference, we constrain the input carrier to noise ratio to 10 dB and plot output carrier to noise versus carrier to interference ratio in Figure

[1] At very low carrier to noise ratios, the impact of the noise on the total amplitude of the composite signal at the input of the A/D is not negligible as assumed, and the curves will not completely converge.

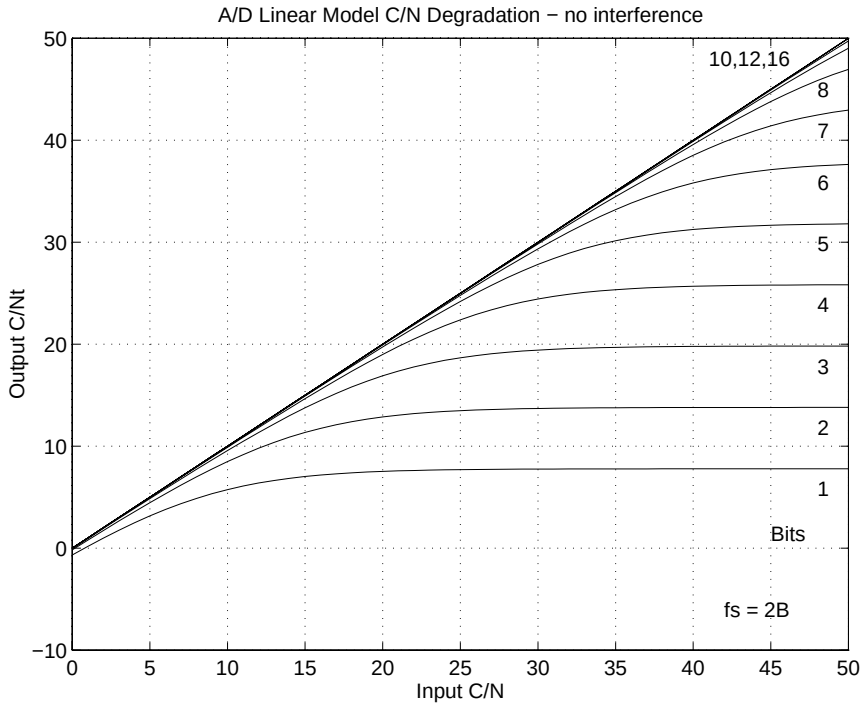


Figure 4.2: A/D C/N degradation as predicted by Equation 4.6

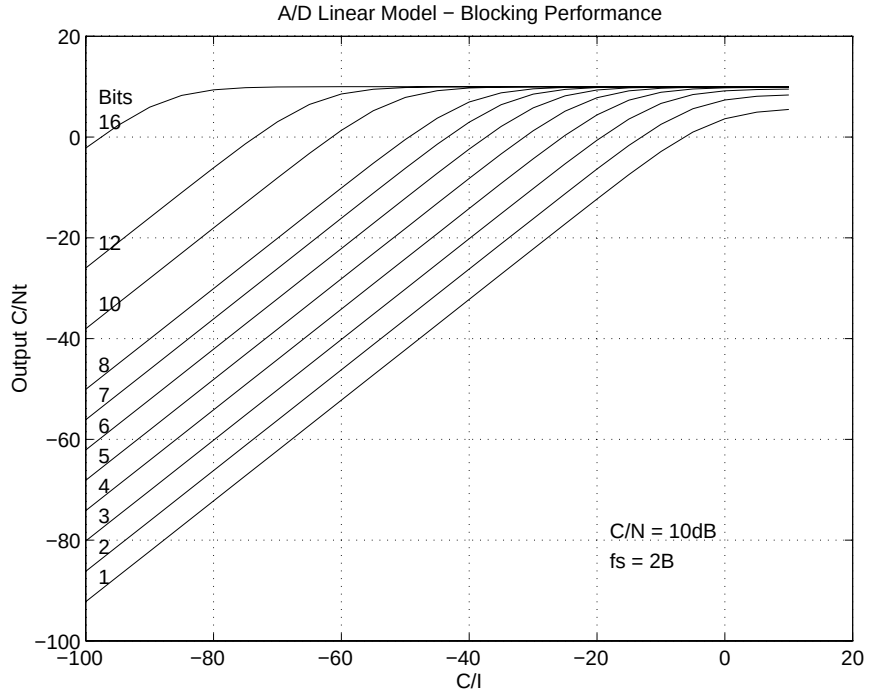


Figure 4.3: C/N degradation with interference as predicted by Equation 4.6

4.3. In this plot, η_T is again equal to two. In reality, the peak to average ratio is not constant verse C/I even if both the desired signal and interferer have equal peak to average ratios[2]. As the interference power is increased, the required resolution to achieve a given output C/N_T for the *desired* signal is increased.

4.2 Limitations of Linear Analysis

While the analytical model described above is useful for obtaining some intuition about the resolution requirements for digital radio under idealized conditions, it is not able to predict the performance when realistic cellular signals and A/D imperfections are present. For example, as first suggested in Chapter 2, the white noise model used for the A/D is not accurate when the number of bits is small or when the A/D has threshold errors (differential and integral nonlinearities). Under these conditions,

[2]When the carrier and interferer are comparable in strength, the peak to average ratio of the composite signal will be higher than either of the constituents.

the A/D generates nonlinear distortion products which concentrate significant distortion at particular frequencies. Additionally, when fading is present, the significant envelope variations at the input of the A/D impact the performance in an unpredictable way. With imperfect AGC, overload may occur in the A/D which generates high amounts of nonlinear distortion. All of these effects are intractable analytically, and simulation must be used to improve our understanding of their impact on system performance.

4.3 A/D Modeling Issues for System Simulation

To efficiently simulate communication systems, modulated radio signals are often represented by their baseband complex envelope[47]. This allows the simulation sample rate to be chosen higher than the Nyquist rate of the baseband signal bandwidth rather than the much higher maximum frequency of the RF or IF signal. Except for a few specialized nonlinearities such as bandpass limiters and square law detectors[48], it is difficult to construct an equivalent baseband model for a nonlinear device operating on a bandpass signal. Thus because an A/D converter has a nonlinear transfer characteristic, a baseband complex envelope simulation in which the in-phase and quadrature components of a modulated signal are separately quantized is not equivalent to quantization at IF. Under the conditions when the quantization noise is well-modeled as additive white Gaussian noise, the two become equivalent.

An additional difficulty arises when we attempt to simulate finite SFDR and intermodulation distortion in A/D converters. By modifying the thresholds of the quantizer in the A/D converter, the differential and integral nonlinearity which give rise to distortion products[3] in the digitized output can be modeled. However, the spurious levels in the output do not uniquely define the quantization thresholds of the A/D converter in general and the distortion in the frequency domain is a function of the magnitude of the input signal, and the magnitude, location, and frequency of threshold errors. Such detail is not typically given in manufacturers' datasheets, and these parameters are subject to change with variations in semiconductor processing, temperature, and operating conditions.

[3]The analog front end (which may include a sample-and-hold) of the A/D converter is an additional source of harmonic and intermodulation distortion and may be separately modeled as a polynomial nonlinearity.

4.4 Simulation Description and Results

In this section we will describe the simulation methodology used to simulate the AMPS, IS-54, IS-95, and GSM standards and present the results obtained. Because it is impractical to simulate all aspects of each standard, an effort was made to retain only as much complexity in each simulation to model the impact of A/D conversion in the receiver. Additionally, simulation of the effect of fading and A/D nonlinearities were limited to IS-54 to limit the overall number of simulations performed to a reasonable number.

4.4.1 AMPS

Description

The AMPS waveform is a frequency modulated signal whose baseband complex envelope is given by

$$g(t) = A_c e^{j2\pi k_f \int_{-\infty}^{t} m(\lambda) d\lambda} \tag{4.7}$$

where A_c is the amplitude of the modulated signal, k_f is the frequency modulation constant, and $m(\lambda)$ is the message signal. The peak deviation is given by

$$\Delta F = k_f V_p \tag{4.8}$$

where V_p is the peak value of the message signal. The modulation index is given by

$$\beta_f = \frac{\Delta F}{B} \tag{4.9}$$

where B is the bandwidth of the modulating signal. The simulation method used is an extension of [49]. For most of the simulations, a sinusoidal message signal with unity amplitude and frequency $f_m = 1$kHz as prescribed in the IS-55 standard is used, with a deviation equal to $\pm 8kHz$. Preemphasis and deemphasis are included in the simulations, with a preemphasis filter characteristic which has a $+6dB$ per octave slope between 300Hz and 3kHz.

To accurately simulate IF A/D conversion, the synthesized baseband complex envelope is used to construct a real signal at IF as

$$s(t) = g_r(t)cos(2\pi f_c t) - g_i(t)sin(2\pi f_c t) \tag{4.10}$$

where $g_r(t)$ and $g_i(t)$ are the real and imaginary parts of the complex envelope respectively and f_c is the carrier (IF) frequency. An artificially low IF of 30kHz is used to keep the processing requirements of the simulation manageable. Additionally, all audio processing is done at an audio sample rate f_{sau} (typically 10kHz) and the result is interpolated to the much higher IF sample rate f_{sfm}.

The effect of channel noise is simulated using a Gaussian random sequence whose variance is given by

$$\sigma^2 = \frac{f_{sfm}A_c^2}{4B_T(C/N)} \tag{4.11}$$

where the fact that the carrier power $C = A_c^2/2$ has been used, and (C/N) is the desired carrier to noise ratio for the signal in a transmission bandwidth B_T (taken to be the 30kHz AMPS channel bandwidth).

The simulation model for the AMPS digital receiver is shown in Figure 4.4. AGC is performed by scaling the received signal to a peak value (taken over the entire simulation length) of one. After A/D conversion, the signal is converted to baseband using a quadrature downconverter. A complex limiter discriminator then demodulates the signal, and the result is decimated to the audio sample rate f_{sau}. Deemphasis, expansion (omitted for sinusoidal modulating signals), and audio filtering are applied to limit the audio noise bandwidth and produce an estimate $\hat{m}$ of the original message signal. Finite precision effects in the digital signal processing subsequent to the A/D converter are not modeled.

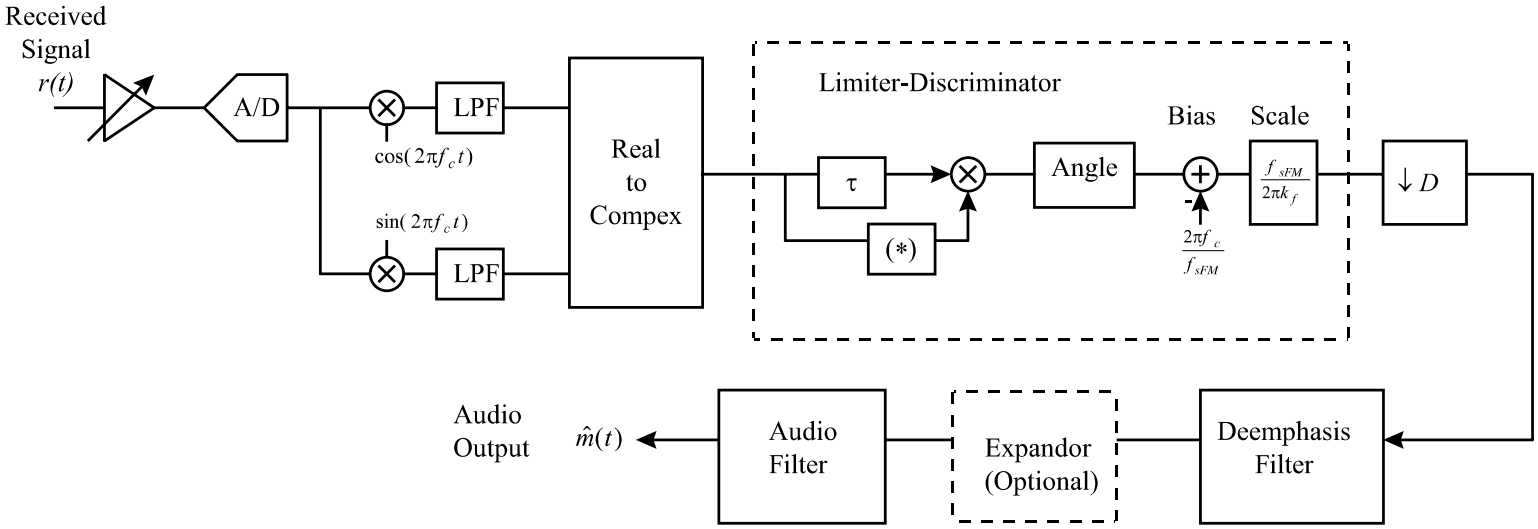


Figure 4.4: AMPS digital receiver simulation model

The performance metric of interest is the output signal to noise ratio. In [49], an autocorrelation technique is used to estimate the SNR at the output. Because of interpolation error and the limited dynamic range of this SNR estimate with moderate record lengths [48], an alternative technique was used for our simulations. A reference output was established by simulating the system without channel noise and without A/D conversion. For subsequent simulations, the mean-squared error of the difference of the output and the reference output without noise is used to calculate the power of the output noise and distortion. This eliminates interpolation errors in the SNR estimate.

Results

In Figure 4.5, the simulation results are shown for the AMPS receiver as the number of bits in the A/D converter is varied. The audio sample rate is 10kHz, and the synthesized IF waveform has a center frequency of 30kHz with a sample rate of 120kHz and a total duration of 1 second. The dashed line indicates the simulated performance with no A/D converter. Some variation is seen in the curves from one value of input C/N to the next. This is especially true near threshold where the SNR begins to be degraded by click noise, but the clicks are relatively infrequent, causing the estimate of SNR to have a high variance when computed over a finite time duration. The plot shows that a four bit A/D has little degradation over the ideal case when perfect AGC and an ideal A/D are used and no interference is present. Also evident is the markedly worse performance of one and two bit converters for carrier to noise ratios below threshold, which is due to nonlinear distortion. The two curves are similar at low C/N ratios because the envelope of the noise dominates the composite input signal at the AGC input, causing the desired signal to only occupy one bit of the full-scale range of the input. Without interference, even one bit conversion gives reasonable performance. This is not surprising, as the FM signal has a constant envelope, and limiting (equivalent to one bit A/D conversion) is used at IF in conventional analog FM receivers.

Limiting is allowed in ordinary receivers provided that filtering has been performed prior to limiting to reject any out of band interference. In the wideband multimode digital radio under consideration, the analog bandwidth is significantly wider than the channel bandwidth, and higher resolution and dynamic range are required. Figure

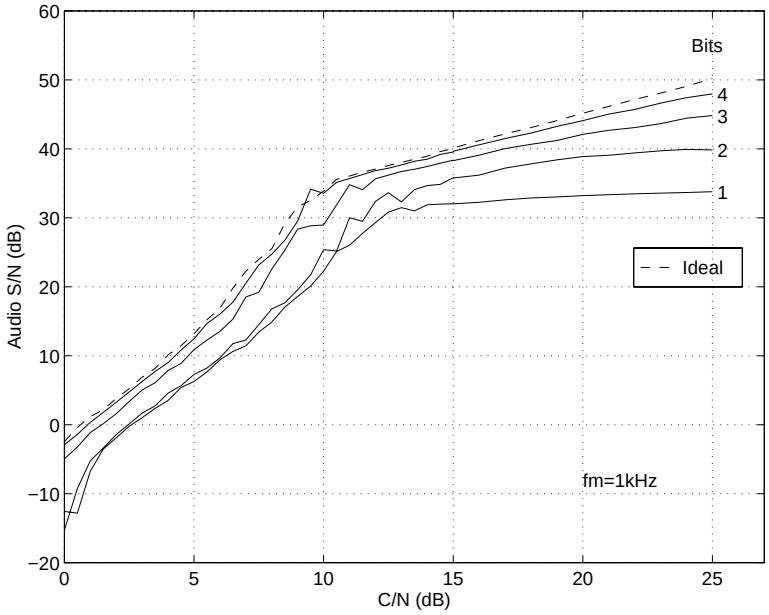


Figure 4.5: AMPS digital receiver performance with varying A/D resolution

4.6 shows the blocking performance of the receiver when interference is present on an alternate channel, i.e. 60kHz away from the desired user with a desired signal C/N of 8dB (3dB above the 5dB sensitivity threshold for 12dB audio SNR without interference) and a sample rate of 300kHz.

For resolutions greater than four bits, the quantization noise spectrum of the ideal A/D is very well approximated as white. Therefore, oversampling is beneficial for reducing the quantization noise floor. This is exploited in the wideband multimode receiver as the sample rate is typically much higher than the channel bandwidth. For the previous simulation with a sample rate of 300kHz, 10dB of signal to quantization noise improvement ($10\log_{10}(300kHz/30kHz)$) is achieved corresponding to an improvement of approximately 1.67bits. The limitation to the improvement with oversampling occurs when the nonidealities of the A/D converter are considered.

Because of the problems described earlier in accurately modeling A/D converter nonlinearities, it is difficult to make generalizations about the effect of nonlinearities on the performance of each system. However, by making some assumptions about the type of converter used we can demonstrate the potential difficulties which may be encountered. Toward this end, a model for a two step flash converter was created

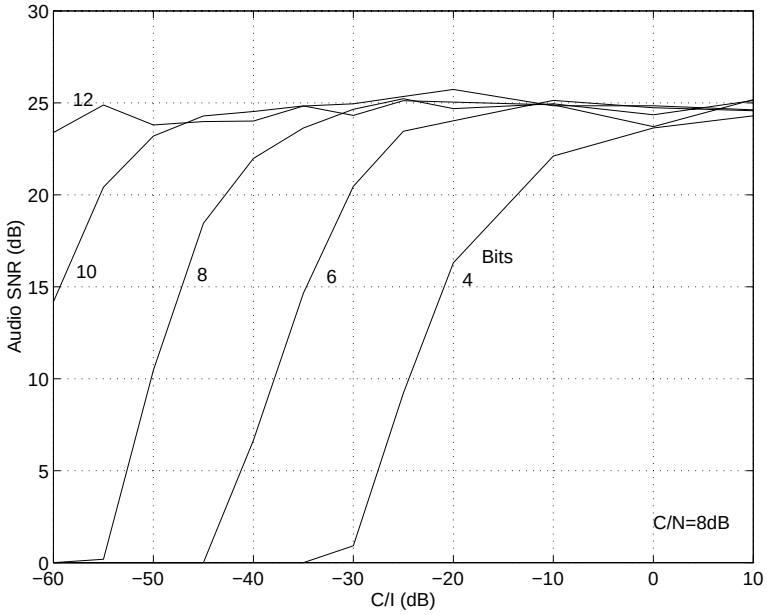


Figure 4.6: AMPS digital receiver performance with alternate channel interference

[4] which includes errors which are typical of such converters. The two step converter was chosen because it is a popular architecture for high speed A/D's and the repetitive nature of its differential nonlinearity (due to the LSB converter being "reused" throughout the range) results in relatively bad harmonic and intermodulation distortion. In Figure 4.7, a the output spectrum of a 10 bit two stage converter with 60dB SFDR is simulated with a desired AMPS signal and two CW interferers at -57dB C/I. Clearly, while the resolution of the converter (as seen by the noise floor) is adequate, significant spectral components are present including one on top of the desired signal which is adequate to block it. Oversampling in this instance will not help, as the discrete spectral components will remain the same even as the noise floor drops.

4.4.2 IS-54 Digital Mode (USDC)

Description

For IS-54 and the other digital standards, Monte-Carlo simulation is performed to estimate the bit error rate (BER) performance. Because many trials must be run

[4]Details of the two-step A/D model are described in Appendix A.

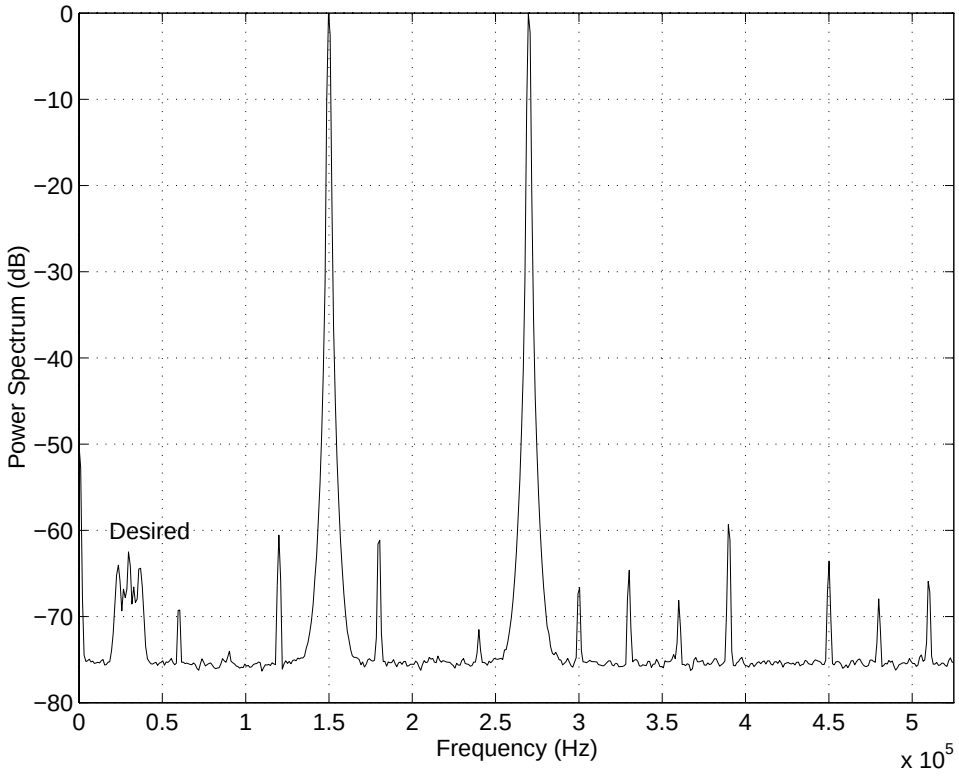


Figure 4.7: AMPS intermodulation test with a nonlinear 10b two-step flash A/D

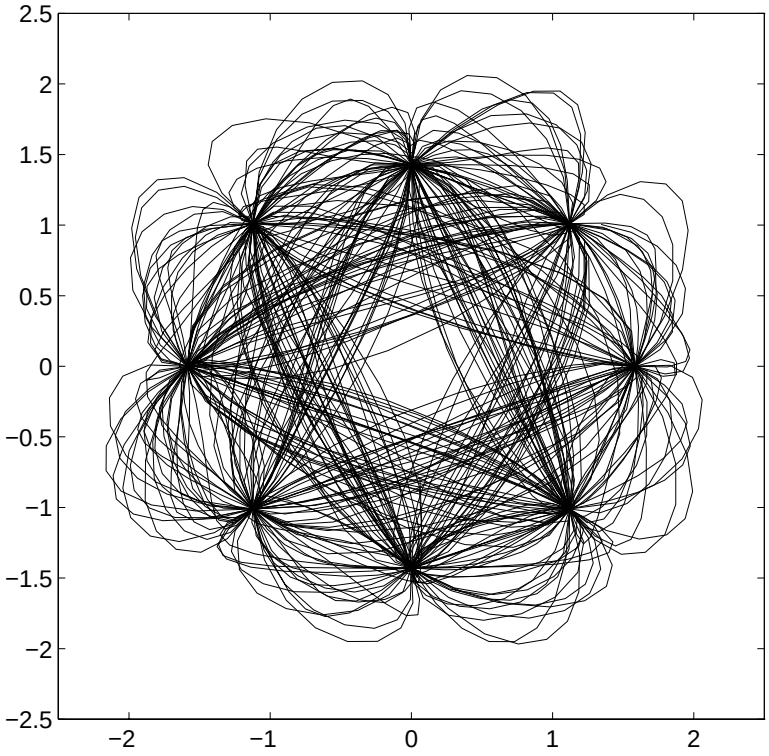


Figure 4.8: IS-54 simulated constellation diagram

to provide a reasonable estimate of BER, the simulations were done with complex baseband equivalents. For bit error rates around 3% (the sensitivity threshold defined in IS-55), the gain due to coding is insignificant. Therefore, coding was not included in an effort to reduce the considerable complexity and simulation time required to simulated BER in a coded system.

The IS-54 transmitter generates a $\pi/4$ DQPSK modulated waveform at a symbol rate of 24.3k samples/symbol with root-raised cosine pulse shaping (rolloff factor = 0.35). A constellation diagram of the synthesized $\pi/4$ DQPSK waveform is shown in Figure 4.8, where eight samples per symbol were used.

The IS-54 simulations were also used as a platform to investigate how flat fading impacts the resolution required of the A/D converter in a digital receiver. Fading was modeled using Clarke's model for Rayleigh fading as described in [34]. The generated complex baseband faded carrier has a Rayleigh envelope distribution and exhibits spreading of the transmitted signal in frequency due to Doppler shift in the carrier

induced by the motion of the mobile receiver. Assuming a uniform distribution of scatterers, the baseband Doppler spectrum is

$$S(f) = \frac{A_o^2}{f_d\sqrt{1-\left(\frac{f}{f_d}\right)^2}} \tag{4.12}$$

where A_o^2 is a function of the antenna gains and the Doppler frequency f_d is

$$f_d = \frac{f_c v}{c} \tag{4.13}$$

where f_c is the RF carrier frequency, v is the velocity of the mobile receiver and c is the speed of light. Normalization is performed to normalize the average power gain of the channel to unity.

The fading generator creates fading waveforms of one second duration at a prescribed sample rate. Because the number of samples in a one second record at the final simulation sample rate would be prohibitively large, the faded carrier was generated at a lower sample rate and subsections of the one second waveform were interpolated for each slot of data simulated. Sections of the fading waveform were selected at 6.667ms intervals for each successive slot corresponding to transmission on the same slot in successive IS-54 frames. This is a more realistic scenario than using adjoining slots of samples from the fading waveform since they tend to be highly correlated. For the simulations without fading, BER was estimated by repeating slots of data until a prescribed number of bit errors was encountered. In the fading simulations, it was found necessary to repeat trials until a number of slot errors (defined as at least one bit error in a slot) were encountered. This is necessary because at the vehicle speeds of interest, the fade duration is comparable to the slot duration. Thus at low Eb/No, all of the bits in a slot may be in error due to a fade. By using slot errors as a stopping criteria for the simulation, we ensure that a representative sampling of the fading channel as well as the noise has been performed.

The channel noise is modeled with a complex Gaussian random sequence. With the power of the complex envelope of the signal normalized to one, the variance for the real and imaginary parts of the complex noise sequence is

$$\sigma^2 = \frac{N_{SS}}{2(Eb/No)} \tag{4.14}$$

were N_{SS} is the number of samples per symbol and Eb/No is the ratio of bit energy to noise power spectral density (SNR per bit).

The simulations use a baseband differentially coherent receiver as shown in Figure 4.9. A square-root raised cosine filter matches the transmitted pulse shape for optimal noise performance and provides an overall ISI-free raised cosine impulse response for the system. Additional wideband filtering is provided to improve the rejection of off-channel interferers while not introducing ISI. The AGC scheme is again to scale the peak of the received signal to unity to avoid overloading the A/D. Because the multimode receiver will utilize a high bandwidth digitizer (high enough to accommodate the highest bandwidth standard of interest), the total noise power can be higher than the narrowband signal power for low carrier to noise ratios. Thus the peak scaling AGC scheme may be overly conservative. We will examine the effect of allowing small amounts of overload of the A/D.

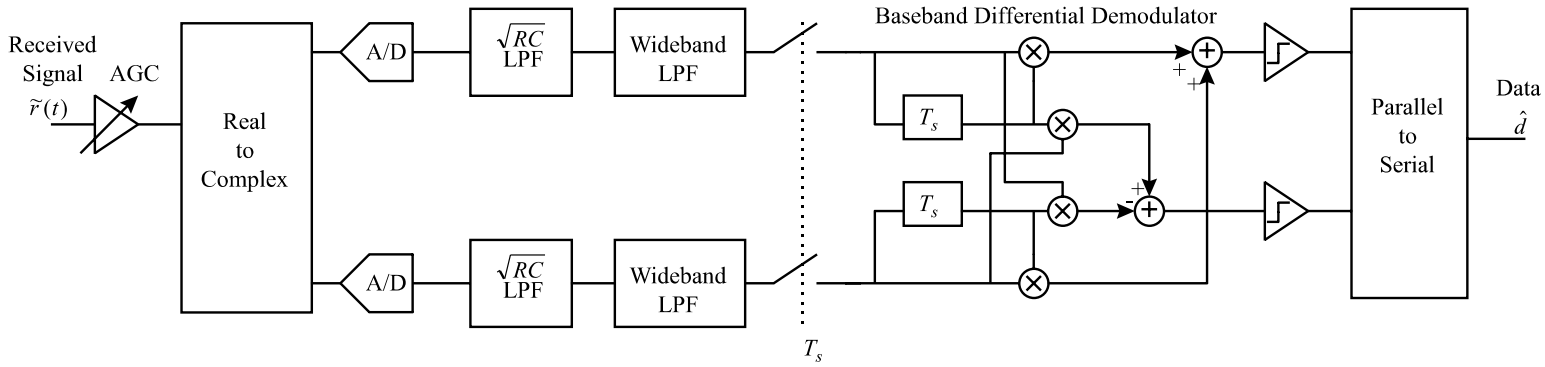


Figure 4.9: IS-54 baseband differential receiver

Results

Figure 4.10 shows the uncoded BER of the IS-54 system for various A/D converter resolutions with a sampling rate of eight samples per symbol and an AWGN channel. As for AMPS, the degradation is imperceptible for A/D resolutions greater than four bits when no interference is present.

Now we examine the blocking performance of the IS-54 digital receiver with an ideal (zero DNL and INL) quantizer. Figure 4.11 shows the BER as the power of an alternate channel interferer is varied while Eb/No is fixed at 8dB. Clearly, the multimode receiver with no analog rejection of alternate channel interference must have an A/D converter with at least eight bits of resolution to achieve the 42 dB blocking specification at 3% uncoded BER.

The effect of A/D overload can be seen in Figure 4.12 in which the peak amplitude of the signal into the A/D is varied. In this plot, Eb/No is fixed at 8 dB and alternate channel interference is present at 42dB greater than the carrier power. The nonlinear distortion products generated when overload occurs cause a dramatic increase in BER, demonstrating the importance of designing the AGC to avoid saturation of the A/D. To guarantee that overload will not occur when the signal fluctuates and with imperfect AGC components, a practical implementation will require the nominal AGC setting to be substantially below full scale.

The simulated performance of IS-54 with Rayleigh fading is seen in Figure 4.13 where the mobile speed is 100km/hr. The AGC gain is recalculated every slot to provide a full-scale peak signal into the A/D, thus modeling the case when the AGC time constant is short. In the actual standard, interleaving and coding provide a substantial performance benefit in a flat fading channel. For reference, the AWGN curve with no A/D conversion is included. Because the average bit error rate is so high, the impact of quantization on the system performance is less pronounced than is seen in AWGN.

4.4.3 IS-95

Description

Frames of 192 bits in length of the IS-95 forward link signal are generated using the scheme depicted in Figure 3.3. For simplicity, the sync channel is omitted and only

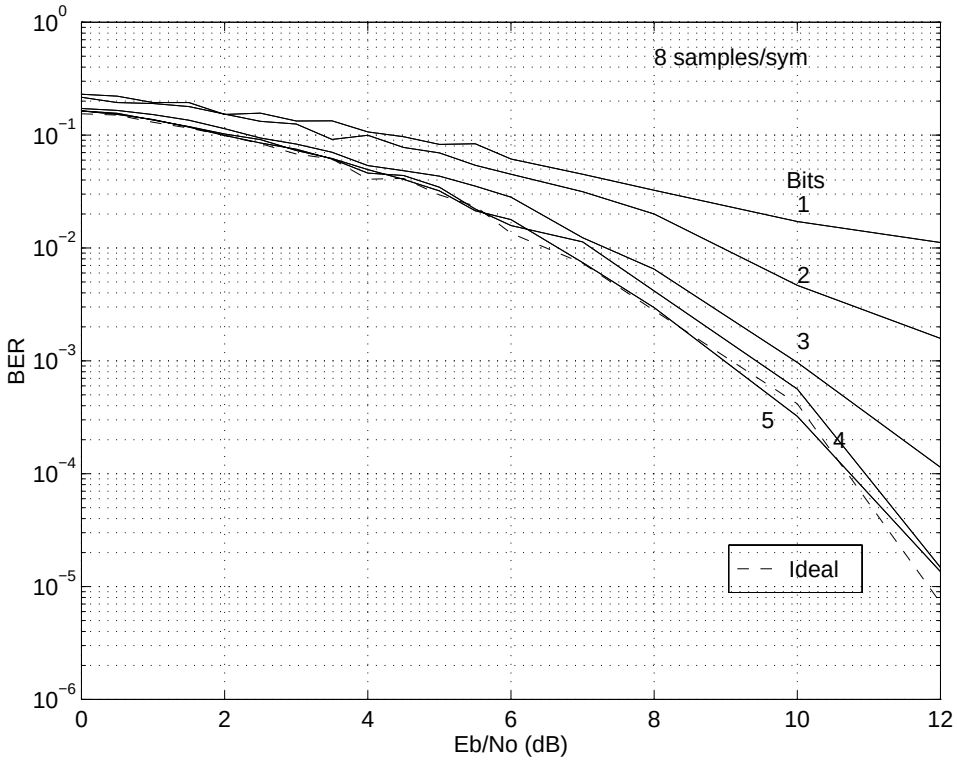


Figure 4.10: IS-54 BER with 1,2,3,4 and 5 bit A/D converter resolution and no A/D (dashed)

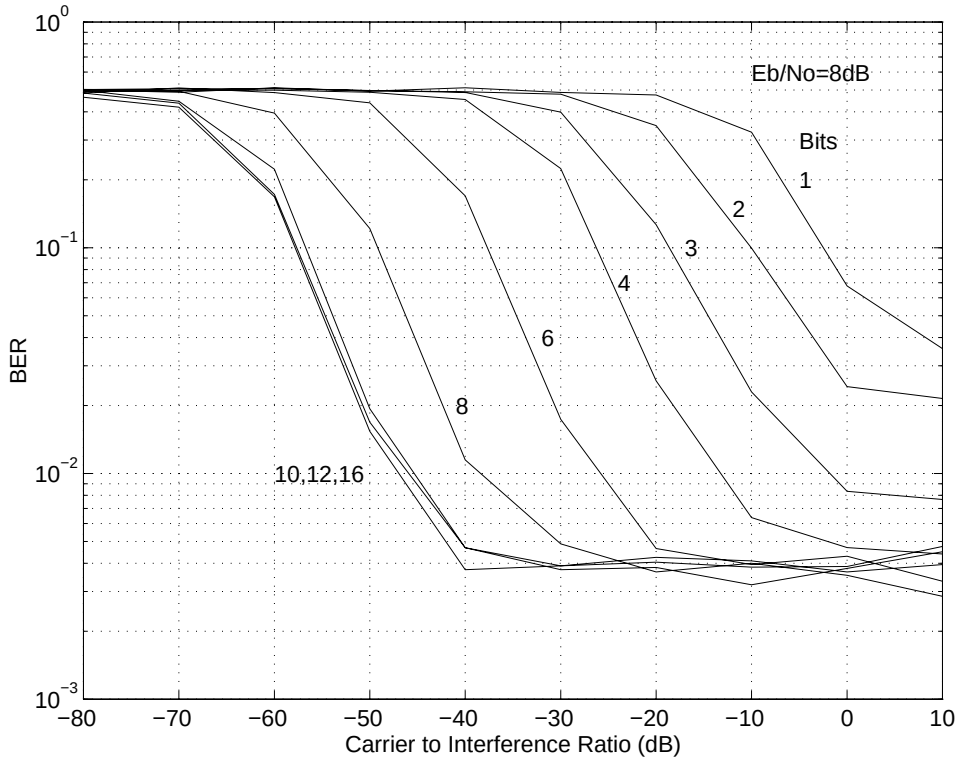


Figure 4.11: IS-54 blocking performance with varying A/D converter resolution

the pilot channel, a desired user, and multiple-access interference (MAI) from up to 62 interfering users with orthogonal Walsh codes are synthesized. Because IS-95 relies heavily on error-correction coding to achieve improved capacity and because the IS-97 specification uses coded frame error rate performance (FER) as its primary performance metric, coding with a rate 1/2 constraint length 9 convolutional code has been included in the simulations. The IS-95 pulse-shaping filters are approximated with a root-raised cosine filter with rolloff factor of 0.35.

The IS-95 receiver simulation model is shown in Figure 4.14. All simulations were performed in an AWGN channel; therefore, only one tap of the mobile three-tap rake receiver is simulated. The receiver first filters the received signal with a root-raised cosine filter which is matched to the chip pulse shaping in the transmitter and produces zero intersymbol-interference at chip intervals at the output. The in-phase and quadrature baseband signals are digitized with two A/D converters, and the delays introduced by filtering are eliminated to ensure the incoming signal is

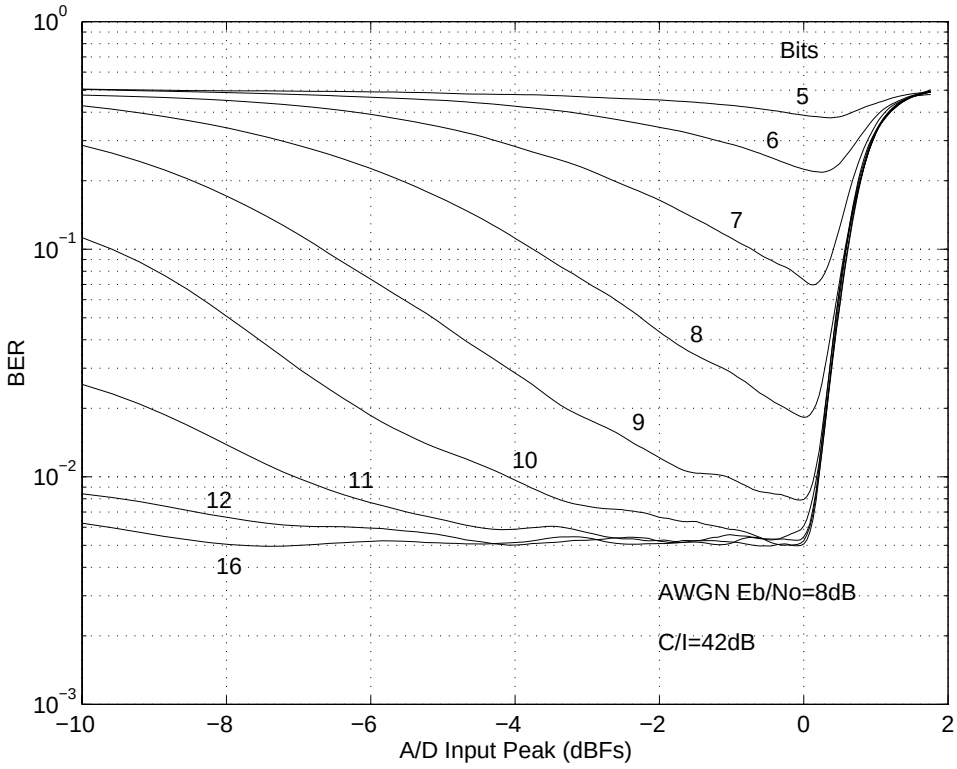


Figure 4.12: Effect of A/D converter overload for IS-54

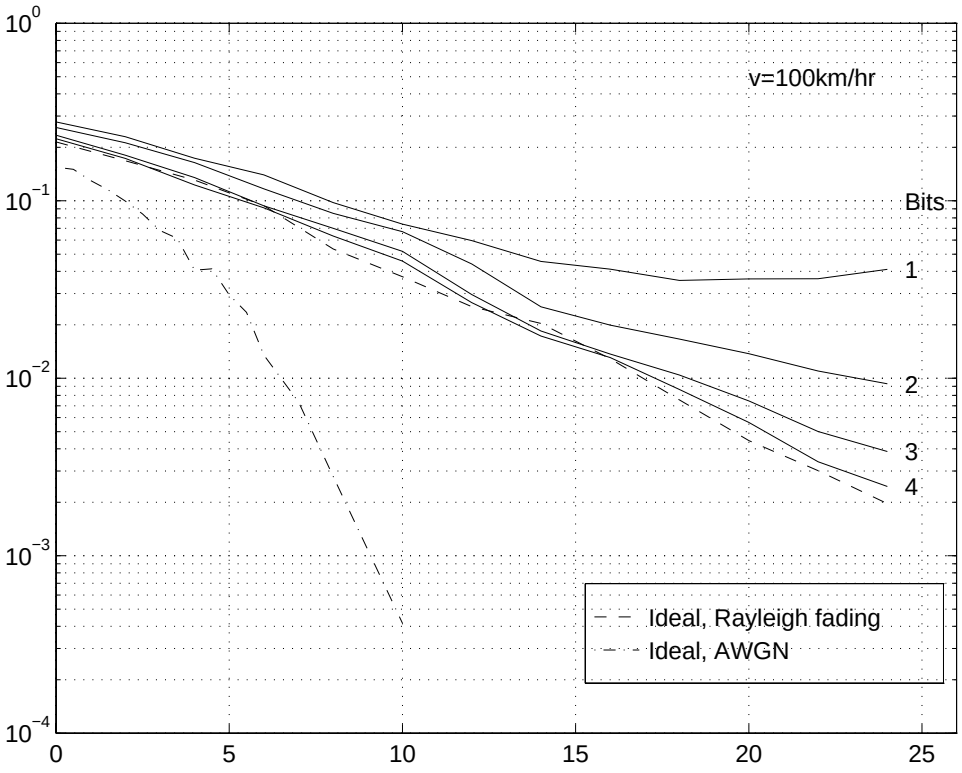


Figure 4.13: IS-54 digital receiver in a Rayleigh flat fading channel v=100km/hr

synchronized with the code. The in-phase and quadrature signals are multiplied with their respective short codes and the results are summed together and correlated with the Walsh code corresponding to the desired user.

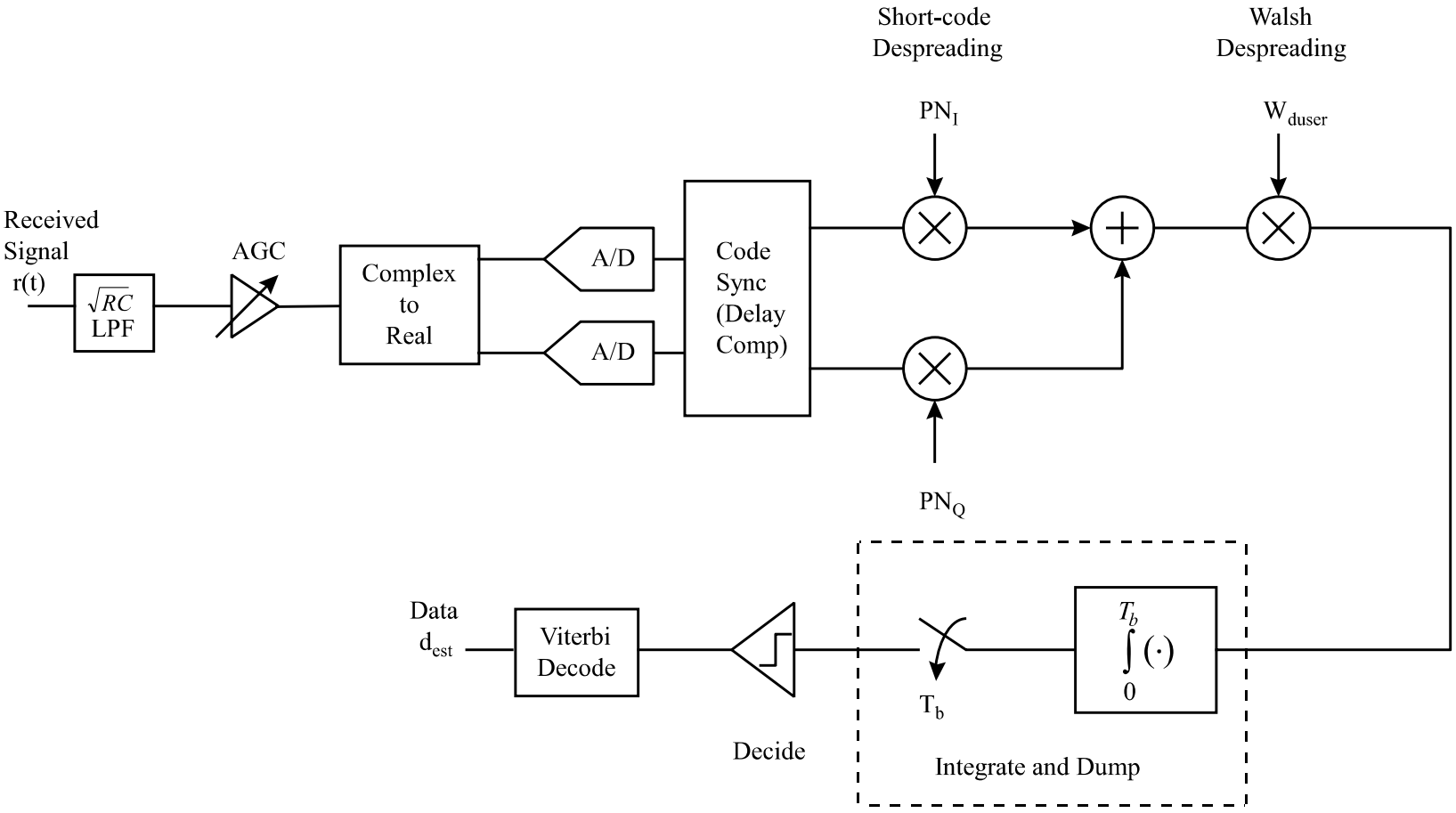


Figure 4.14: IS-95 receiver simulation model

Because the undesired users are spread with orthogonal codes and are synchronous with the desired user, the MAI nominally has zero cross-correlation with the desired user's spreading code and MAI has no impact on the performance of the forward link. However, in a real multipath channel, the delayed multipath components are not synchronous and the cross-correlation is non-zero. Additionally, when chip pulse-shaping is used as in IS-95, the cross-correlation is zero only if the receiver correlates the incoming signal with a pulse-shaped copy of the code. Thus in the simulation, the PN short codes and desired user Walsh codes are pulse-shaped before despreading the received signal.

To complete the correlation process, the signal is passed through an integrate-and-dump filter which dumps at the end of every bit period (64 chips). The correlation result is then compared with a threshold of zero to recover the coded data bits and Viterbi decoding is performed to decode the original data. Because fading channels were not modeled, interleaving is not beneficial and therefore not included in the simulation.

By the Central Limit Theorem, the distribution of the signal at the input of the receiver is approximately Gaussian as the number of users becomes large. Thus we may intuit that allowing some amount of overload may not be catastrophic to the error performance of the system as the probability of a sample exceeding the full scale range (corresponding to the area of the tails of the Gaussian distribution exceeding the full scale range) can be small even when the peak value taken over any frame is significantly above full scale. Also, because of the processing gain inherent in direct-sequence spread-spectrum systems, bit errors are made only when multiple chip errors occur within a bit period causing the integrated bit decision statistic to be in error. Thus we seek an AGC which optimizes the performance degradation caused by overload and the degradation due to quantization noise. To achieve this, we define the *crest factor* γ_F as the full scale power relative to the average power (variance) of the signal at the input of the A/D, i.e. $\gamma_f = \frac{V_{FS}^2}{\sigma_{Vin}^2}$ where σ_{Vin}^2 is the average signal power at the input and V_{FS}^2 is the full scale power. Figure 4.15 illustrates the relationship between the various parameters of the AGC. When the crest factor is equal to the peak to average ratio, no overload occurs. The crest factor is a design parameter of the AGC. Because the full scale range of the A/D converter is fixed, the crest factor determines the setpoint of the average power to be delivered to the A/D.

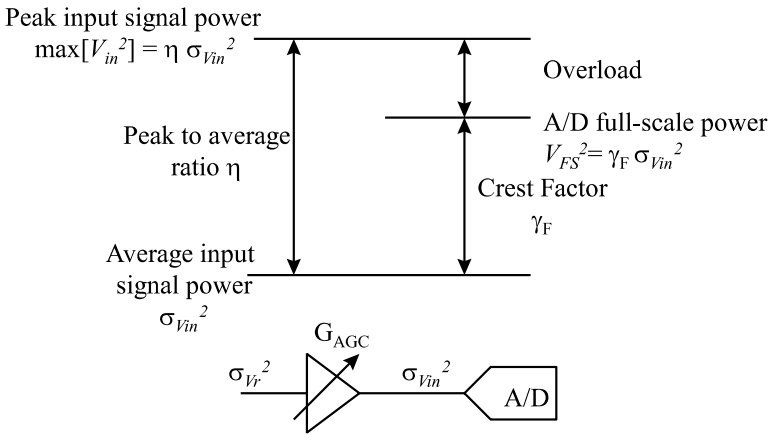


Figure 4.15: Relationship of the peak to average ratio, the full scale range and the crest factor

If the input to the AGC amplifier has power σ_{Vr}^2, the gain factor required of the AGC is

$$G_{AGC} = \sqrt{\frac{V_{FS}^2}{\sigma_{Vr}^2 \gamma_F}} \tag{4.15}$$

While interference from undesired users is orthogonal to the desired signal, the total power of the received signal is increased by the orthogonal MAI. Thus the A/D converter must have higher dynamic range to handle the composite signal when MAI is present. Additionally, because the peak to average ratio of the signal is a function of the number of users in the system, the optimal crest factor for the AGC will be a function of the number of users.

Because in certain applications IS-95 may be overlaid upon existing AMPS service, we are also interested in the performance of the IS-95 receiver in the presence of narrowband interference. For these simulations, we use an AMPS signal at 30kHz offset from the IS-95 carrier with a 1kHz sinusoidal modulating signal.

Results

We begin by examining the choice of AGC parameters to optimize system performance. The fractional overload (fraction of samples exceeding full scale) is shown in Figure 4.16 for one and 63 users plus a pilot channel with and without narrowband

interference at a C/I of 0dB. For a single user without interference, the optimal crest factor for minimum BER was found to be around 4.5dB. For sixty-three users, the best choice of crest factor is around 8dB. These values are used for subsequent simulations. Histograms of the input signal at the input of the A/D in the in-phase arm in Figures 4.17 and 4.18 provide estimates of the pdf of the A/D input signal. In Figure 4.17, the evolution of the pdf is seen as the interference power is increased for the case of a single user plus pilot channel with four samples per chip, a crest factor of 4.5dB, a full-scale A/D range of ± 1, and no noise. With very low interference, a moderate amount of overload is seen. Because the pdf of the composite signal is obtained by convolving the signal pdf and the pdf of the interference, the maximum overload is seen at a C/I of 0dB. At very high interference levels, the pdf approaches that of a sinusoid as expected for narrowband interference. Because the peak to average ratio of the sinusoid is 3dB and the crest factor is set at 4.5dB, no overload is present in the interference dominated case. In Figure 4.18, the number of users is increased to sixty-three while the other parameters are kept the same. Because of the large number of users, the pdf is approximately Gaussian at low interference levels. As the interference power is increased, the overload area does not appreciably increase. To obtain further insight, the peak to average ratio of the IS-95 signal (with the peak taken over one IS-95 frame at 4 samples per chip) is plotted in figure 4.19 versus the carrier to interference ratio. For a single user, a significant increase is seen near 0dB (where the interference is comparable to the total power of the IS-95 signal, and the peak to average ratio approaches 6dB. For a larger number of users, less peaking is seen, and the peak to average ratio increases to a maximum of about 13.5dB.

The IS-95 receiver bit error rate and frame error rate performance with one sample per chip is shown in Figures 4.20 and 4.21 for a pilot channel plus one and sixty-three users respectively. Because only one sample is used per chip, no pulse shaping is performed. Forward Error Correction (FEC) coding is included with a rate 1/2 constraint length 9 convolutional code, and frame errors are declared when one or more decoded bits are in error. The dashed line indicates the reference performance without A/D conversion and shows a frame error rate of 1% is achieved at an Eb/No of around 6dB. For both one and sixty-three users, the plots illustrate that four bits provides negligible degradation in performance. For one user, little degradation is seen for two and three bits. When the number of users is increased to sixty-three,

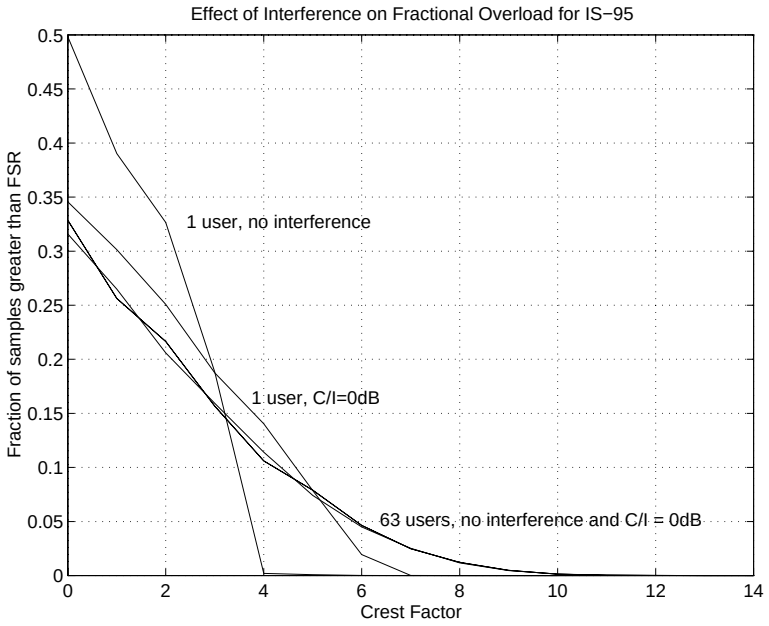


Figure 4.16: Fractional overload of the IS-95 signal with and without interference

more degradation is seen in the lower resolution plots as the power of the desired user is reduced to accommodate the power of the interference.

In Figure 4.22 and 4.23, the simulations are repeated with four samples per chip and pulse shaping. IS-95 receivers typically use 8 samples per chip to aid in code acquisition, but this would make the simulation duration unpractically long. Comparing Figure 4.22 with 4.20, some oversampling gain is seen. For the case with MAI due to additional users in Figure 4.23, the performance diverges from the infinite resolution curve at high Eb/No. This has been found to be due to the loss of orthogonality of the desired user to the MAI when the input signal is quantized. Because the correlating code in the receiver has infinite resolution, its pulse shape is not identical to the received signal which after quantization. This has been observed to cause a lack of orthogonality.

Even with as few as four bits of resolution, the receiver performs close to ideal in the presence of a narrowband AMPS interferer, as shown in for one user in Figure 4.24 and sixty-three users in 4.25 for an Eb/No of 5dB. For simulation efficiency, one sample per chip is used. At carrier to interference ratios below 18dB, the processing gain is inadequate to reject the narrowband interference. As the interference power is

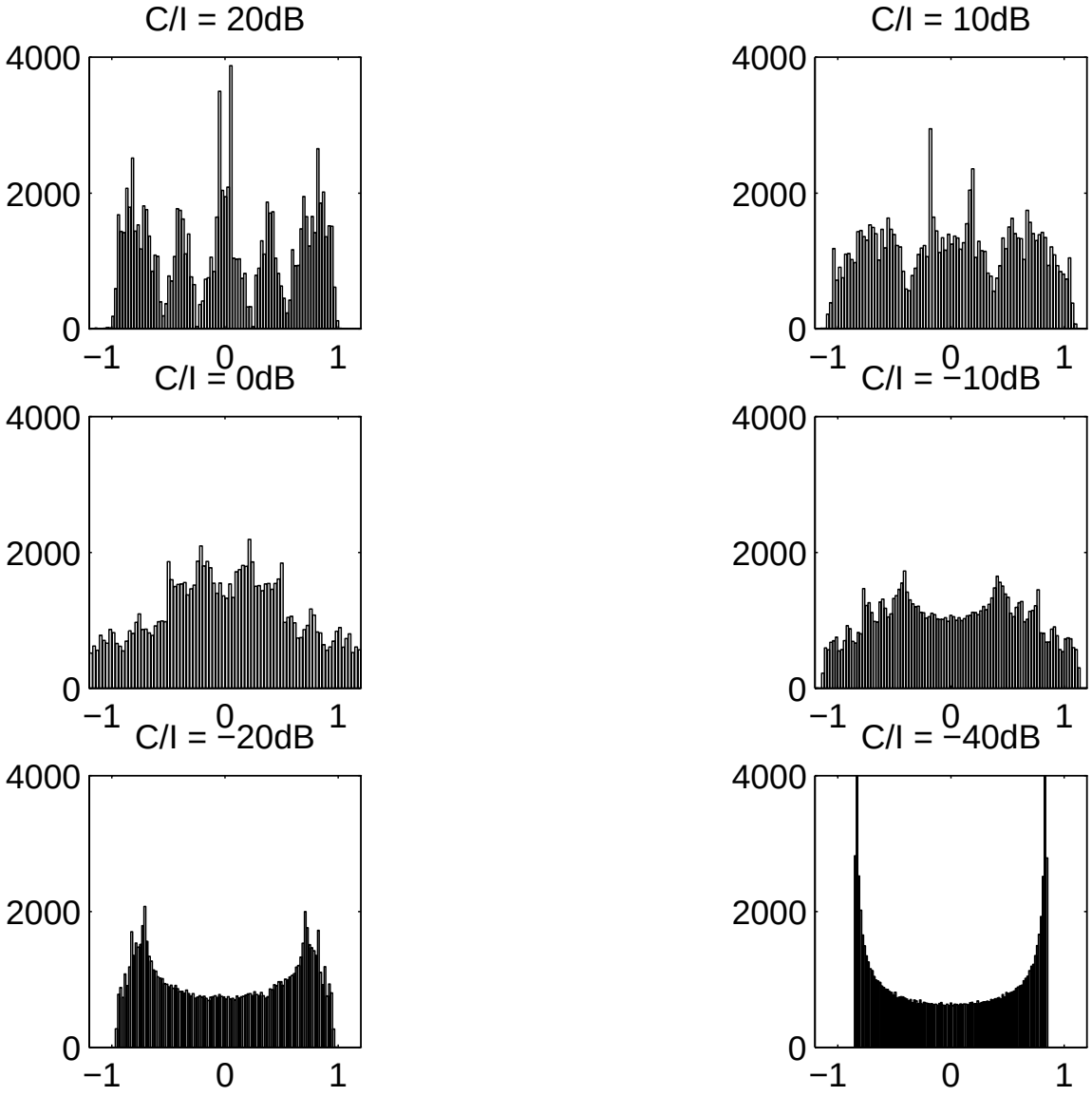


Figure 4.17: Histograms of a single user plus pilot IS-95 signal at the input to the in-phase A/D as the carrier to interference ratio is varied

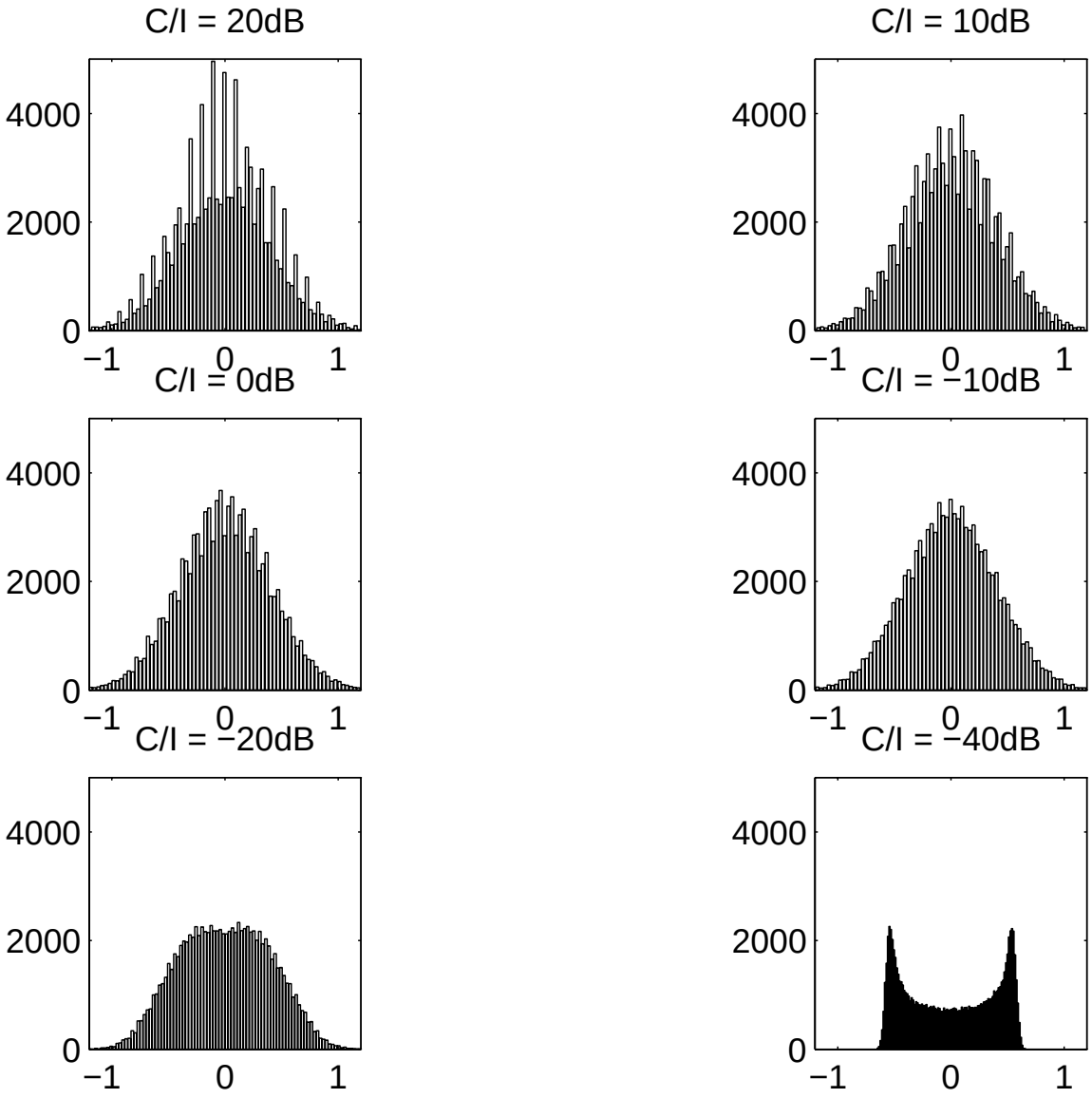


Figure 4.18: Histograms of a 63 user plus pilot IS-95 signal at the input to the in-phase A/D as the carrier to interference ratio is varied

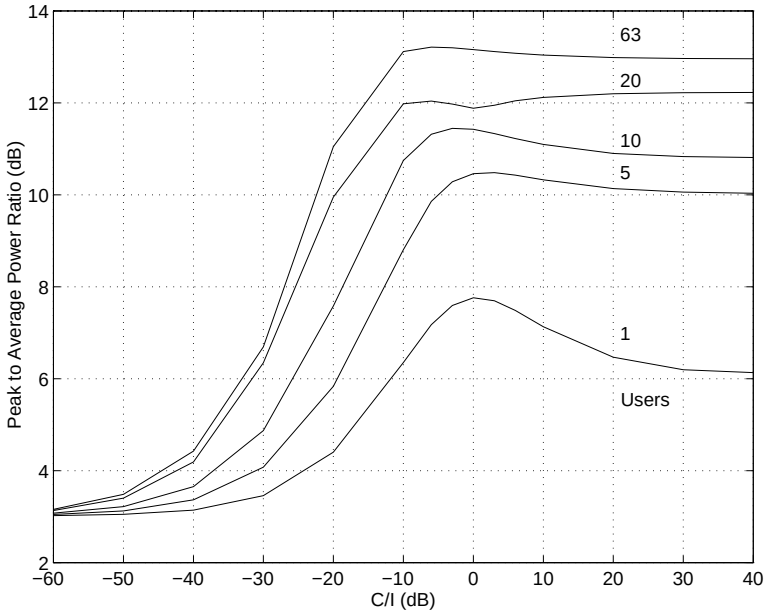


Figure 4.19: Peak to average ratio of the IS-95 signal taken over single frame with 4 samples/chip

decreased, the bit error rate falls until approaching the floor set by the channel noise.

The resolution requirements of spread spectrum systems are less than narrowband systems for a variety of reasons. First, the processing gain of the spread spectrum system provides a direct oversampling benefit, since the quantization error of each chip is averaged over the number of chips in a bit interval. Second, the spread spectrum signal is less sensitive because of its ability to allow a moderate number of chip errors due to overload in a bit interval as described above. Lastly, the noiselike spread spectrum signal causes less harmonic distortion when the number of bits is low or INL and DNL is present in the A/D. As will be described in the next section, the spread spectrum signal can be thought of as possessing an inherent dithering quality which reduces the spurious responses from a nonlinear converter.

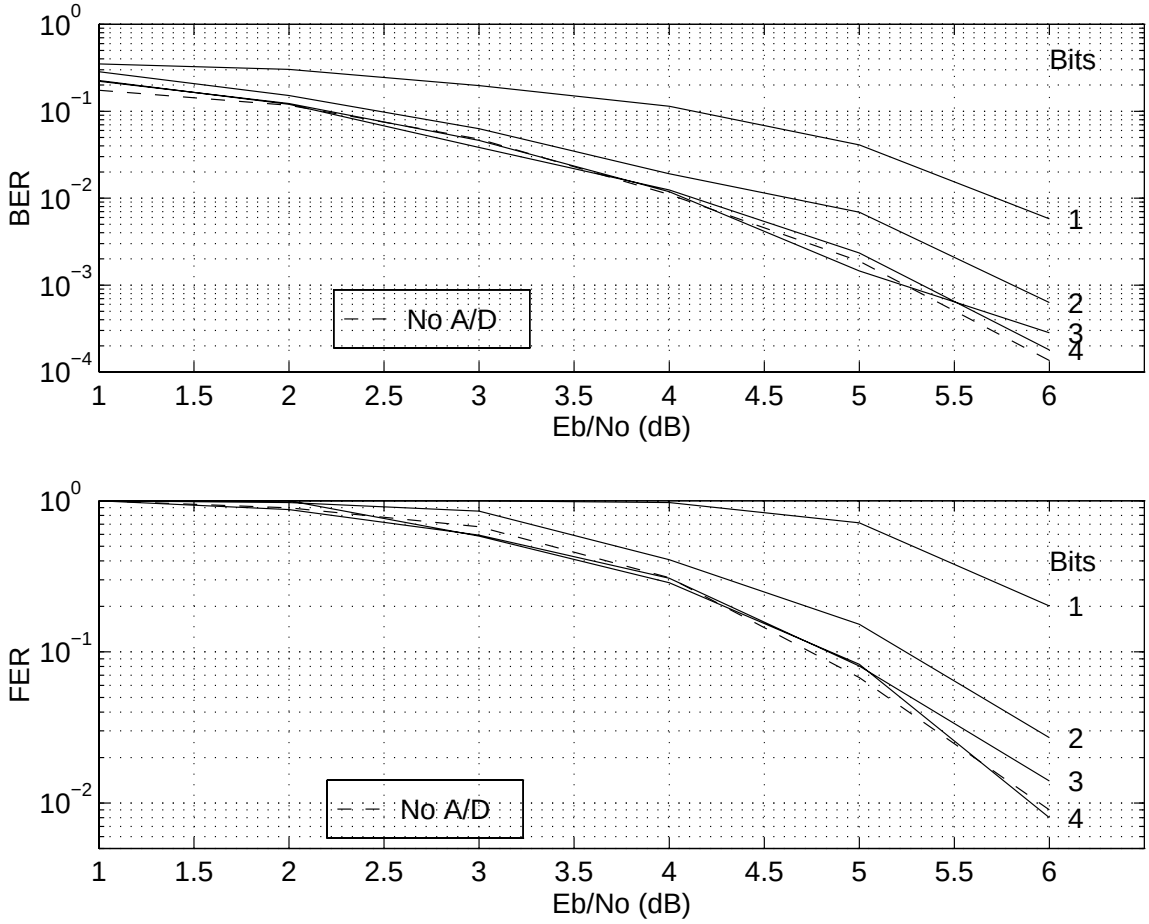


Figure 4.20: IS-95 BER and FER with various A/D resolutions and no A/D (dashed), one user, and one sample per chip

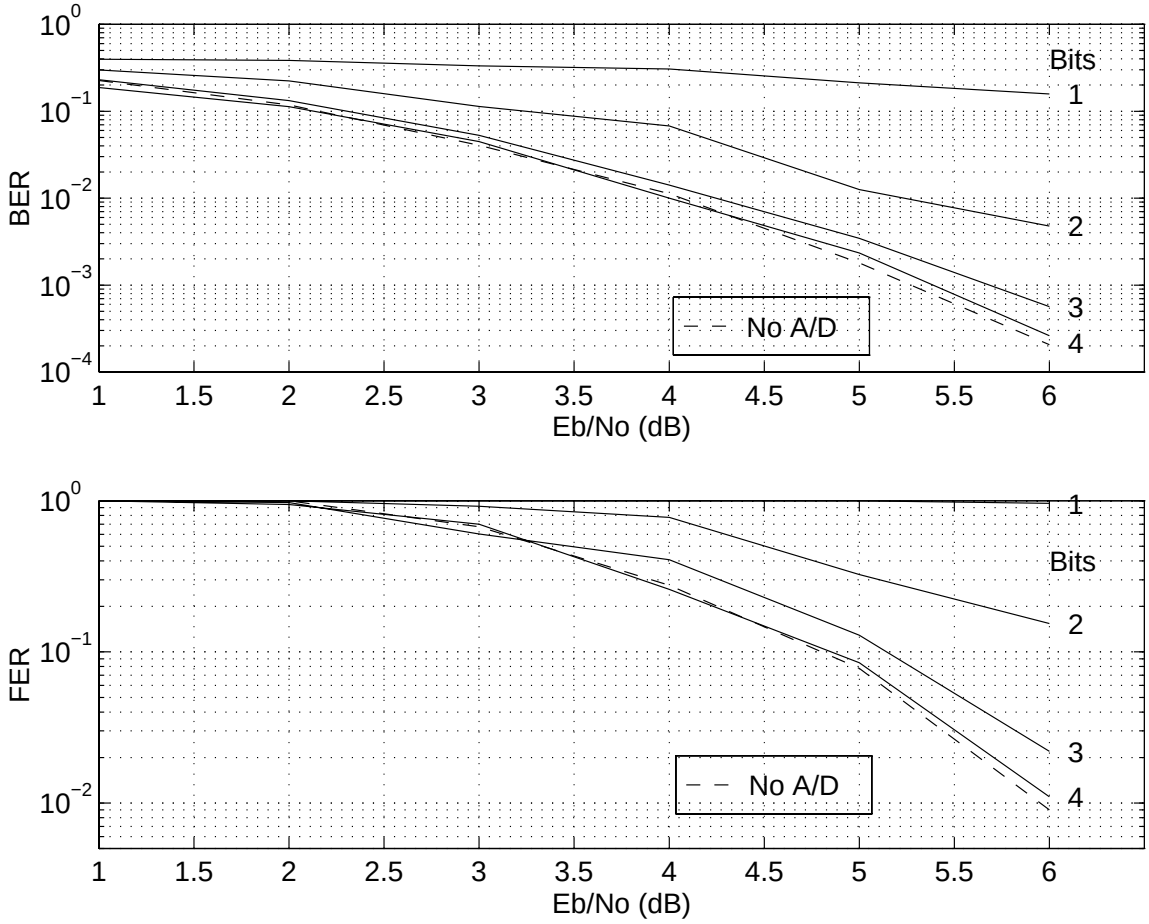


Figure 4.21: IS-95 BER and FER with various A/D resolutions and no A/D (dashed), sixty-three users, and one sample per chip

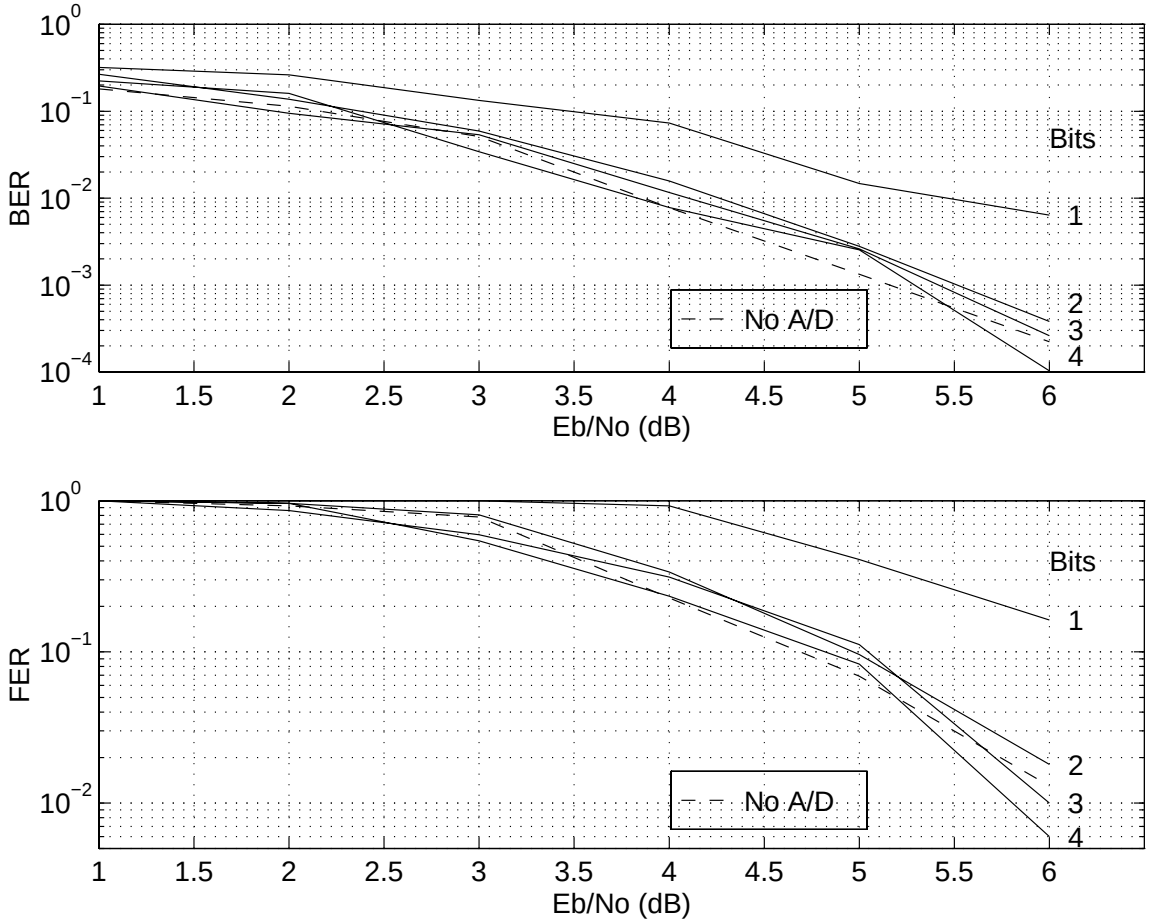


Figure 4.22: IS-95 BER and FER with various A/D resolutions, one user, and four samples per chip

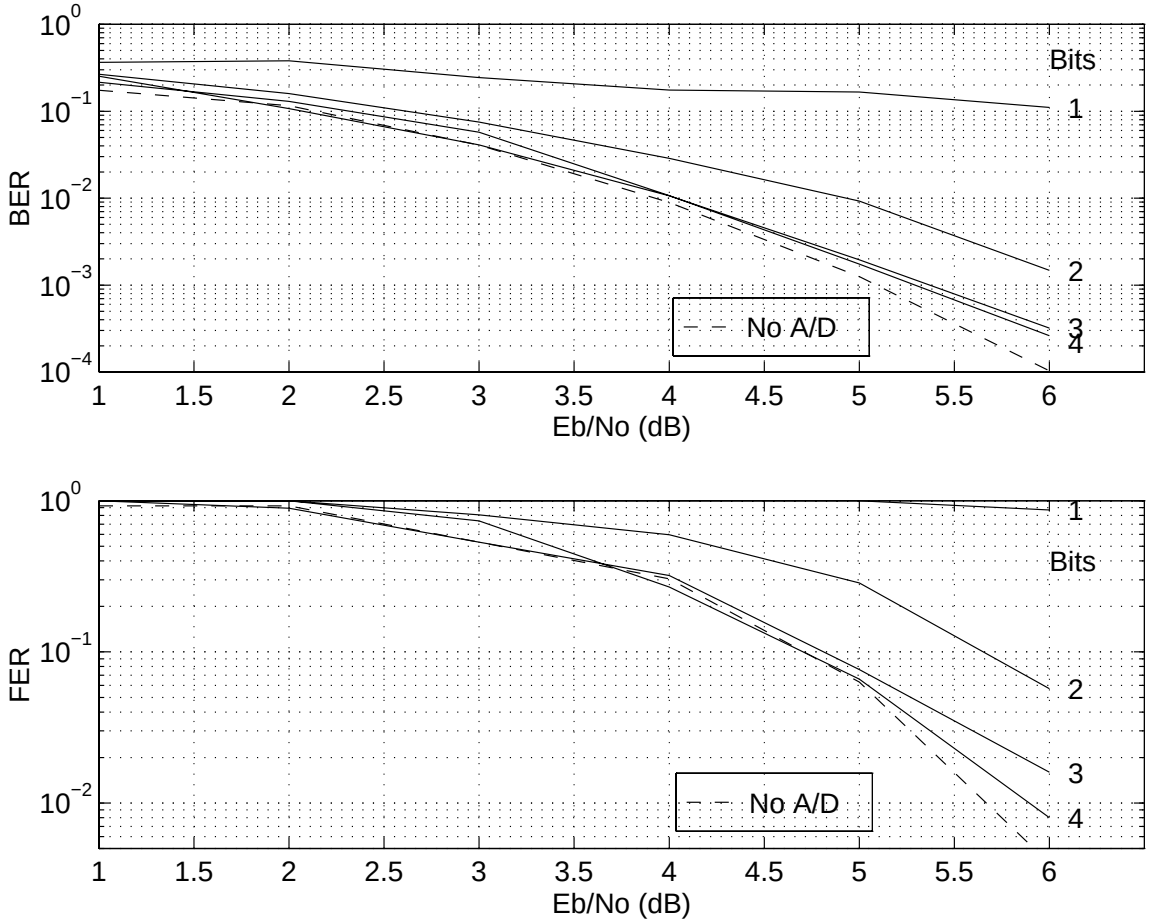


Figure 4.23: IS-95 BER and FER with various A/D resolutions and no A/D (dashed), sixty-three users, and four samples per chip

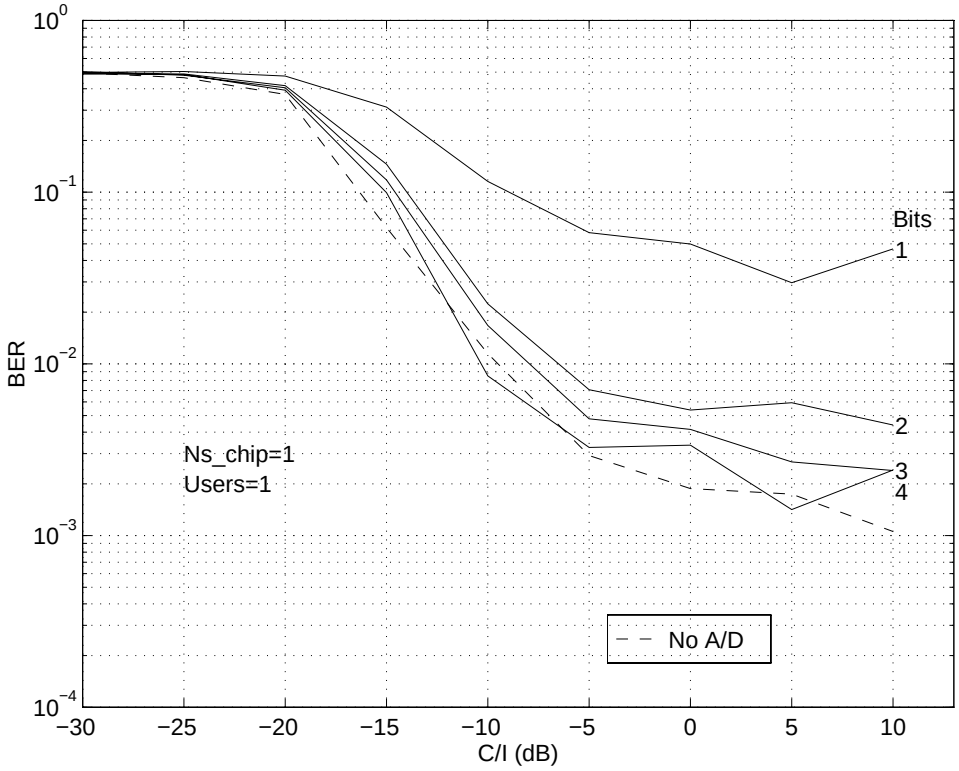


Figure 4.24: IS-95 BER with AMPS cochannel interference, one user, and one sample per chip

4.4.4 GSM

Description

For GSM, the modulation format is Gaussian Minimum Shift Keying (GMSK) with BT=0.3. The baseband complex envelope of GMSK is given by

$$\tilde{g}(t) = A_c e^{j\frac{\pi h R_b}{2}\int_0^t m_f(\lambda)d\lambda} \tag{4.16}$$

where m_f is a polar data stream at a bit rate R_b (270.833kb/s for GSM) which has been filtered by the Gaussian pulse shaping filter and h is the modulation index, equal to 0.5 for MSK. The transmitted GSM spectrum obtained from simulation is shown in Figure 4.26.

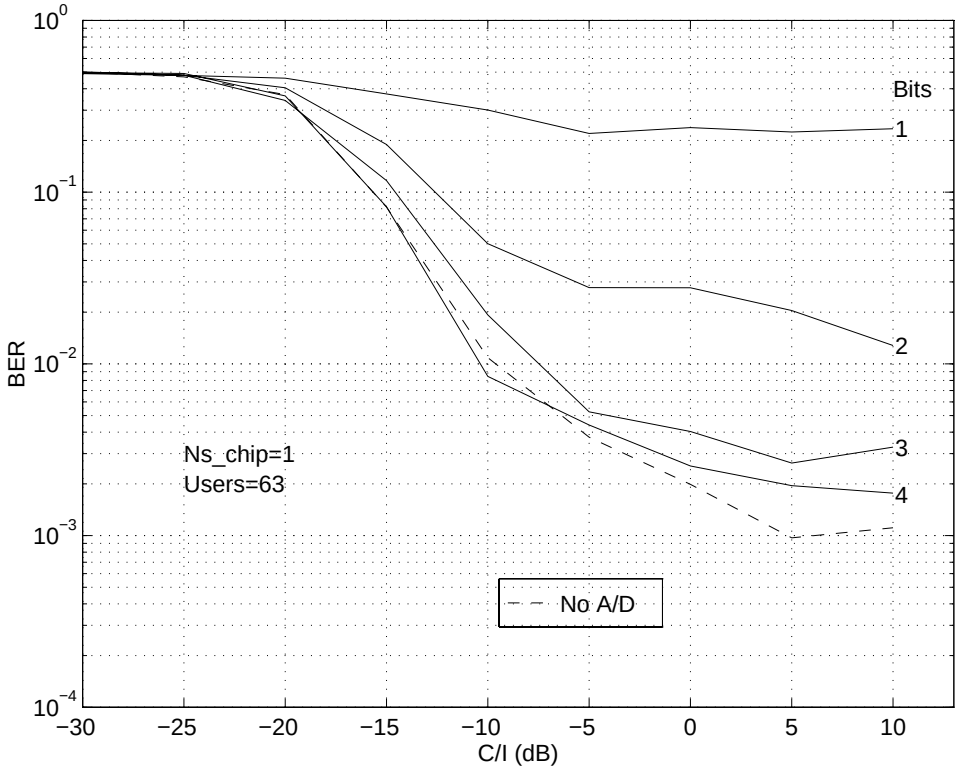


Figure 4.25: IS-95 BER with AMPS cochannel interference, sixty-three users, and one sample per chip

Many options exist to demodulate GMSK, including coherent detection [50], non-coherent limiter discriminator demodulation, and Maximum Likelihood Sequence Estimation (MLSE) using the Viterbi algorithm [51]. The GSM simulations for this work utilized the coherent receiver illustrated in Figure 4.27. Because MSK can be viewed as offset QPSK with cosinusoidal pulse shaping, the receiver uses matched filters with a cosine impulse response . Additional filtering is required to improve the rejection of out of band interference. The eye diagram after filtering is shown in Figure 4.28.

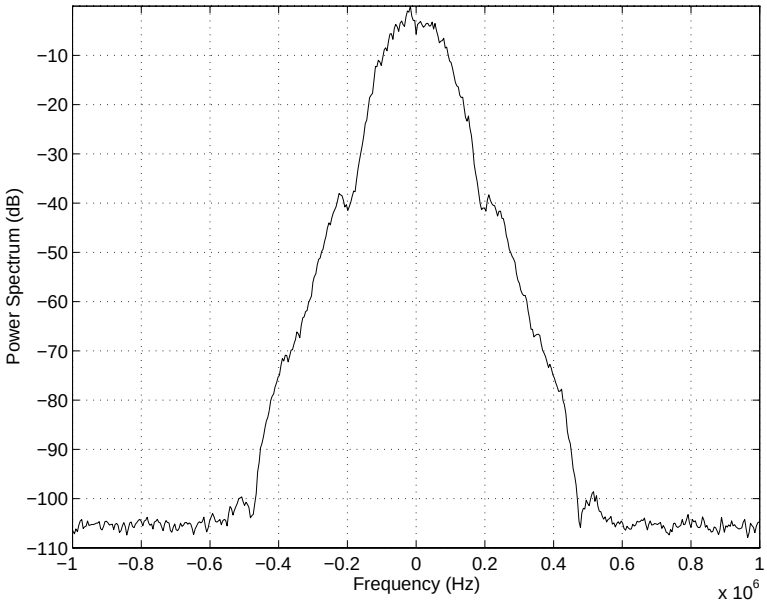


Figure 4.26: Simulated GSM spectrum (GMSK BT=0.3)

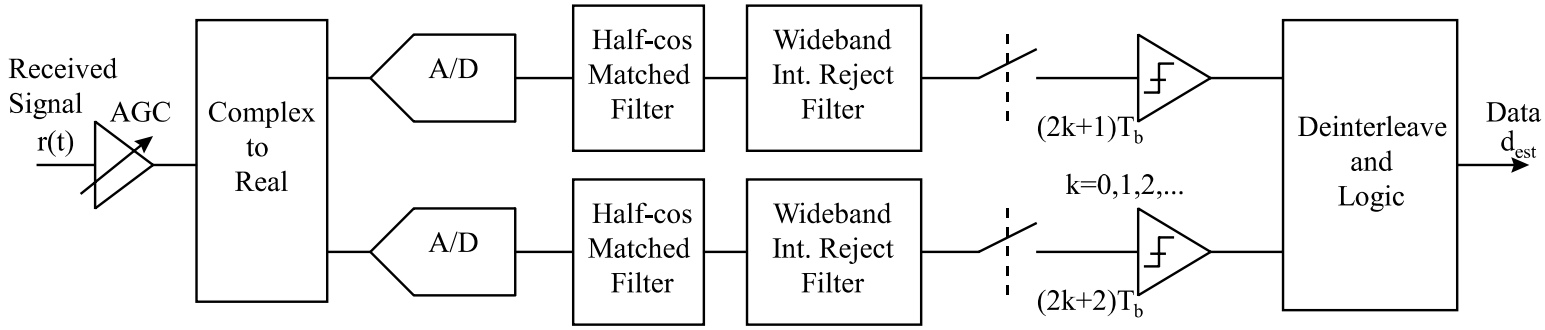


Figure 4.27: Coherent GMSK receiver simulation model for GSM

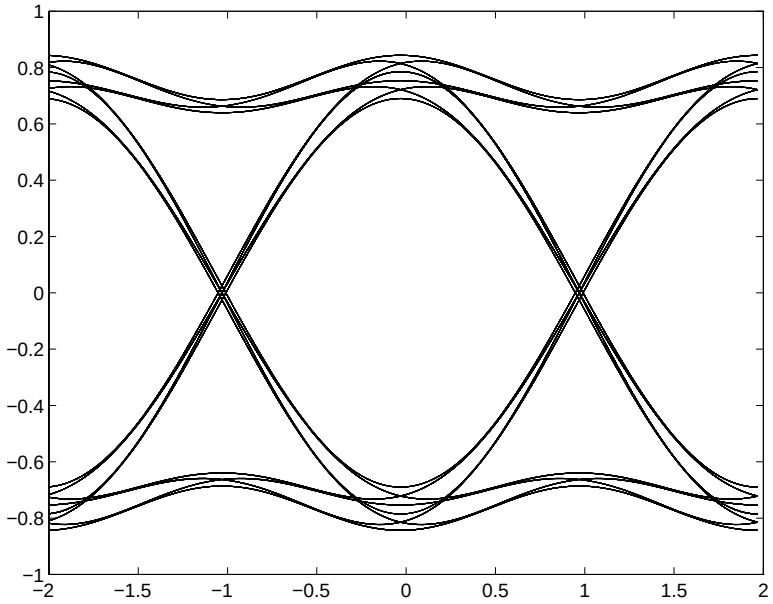


Figure 4.28: GSM receiver eye diagram

The inphase and quadrature signals are then sampled with a one bit period offset and the resulting samples are sent to decision devices. When the original data is directly modulated as in Equation 4.16, additional logic processing is necessary to recover the original data as the I and Q bit streams are differentially encoded and have phase inversions on every other symbol [52].

Because GMSK is a constant envelope modulation scheme, it is relatively robust to quantization errors when no interference is present. However, the blocking and intermodulation requirements for GSM are much more stringent than IS-54, AMPS, or IS-95.

Results

In Figure 4.29, the BER of the GSM receiver is plotted for simulation parameters of 4 samples per symbol and no interference, and 75 errors simulated. Also plotted is the theoretical BER for GMSK with BT=0.3, given by

$$BER = \frac{1}{2} erfc\left(0.949\sqrt{\frac{E_b}{N_o}}\right) \tag{4.17}$$

where the factor of 0.949 is a modification to the minimum distance due for a Gaussian filter with BT=0.3 [53]. The simulated BER shows excellent agreement with the theoretical curve, demonstrating correct operation of the simulation. Once again, the simulated performance with A/D conversion and no interference is close to ideal with as few as four bits. Even with one bit, the performance is relatively good since the constant envelope modulation allows limiting of the input signal.

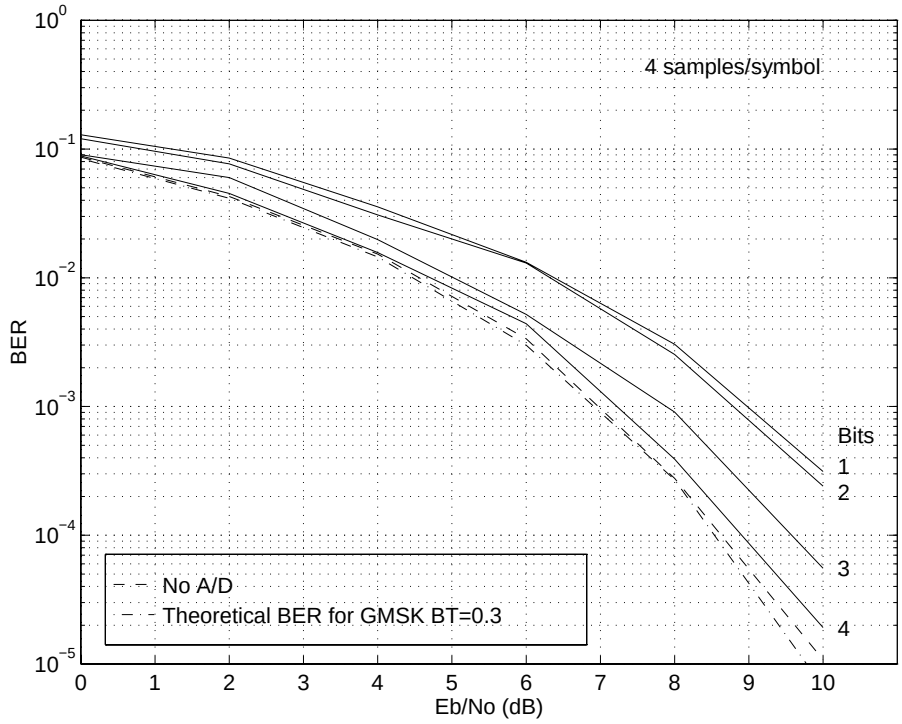


Figure 4.29: GSM simulated and theoretical BER performance with A/D conversion

The GSM specification specifies BER requirements differently based upon the class of bits transmitted, since different classes have differing degrees of error protection. For our simulations without coding, we may use the specification for the unprotected class II full speed control channel bits, which is 2% BER. From Figure 4.29, 2% BER is achieved at an Eb/No of 4dB. In Figure 4.30, we have set Eb/No equal to three dB above the reference sensitivity (7dB) and included a CW interferer at an offset of 800kHz with a carrier to interference power of -68dB and -78dB corresponding to the specified worst case interference for a mobile station at 800kHz and 1.6MHz offsets

respectively. For a sampling rate of 8 samples/bit, 2% BER is not achieved with a 12bit (ideal) converter for the 1.6MHz offset. When the sampling rate is increased to 16 samples/bit, a 12bit ideal A/D converter meets the 2% BER requirement. However, such a converter would require better than 82dB SFDR.

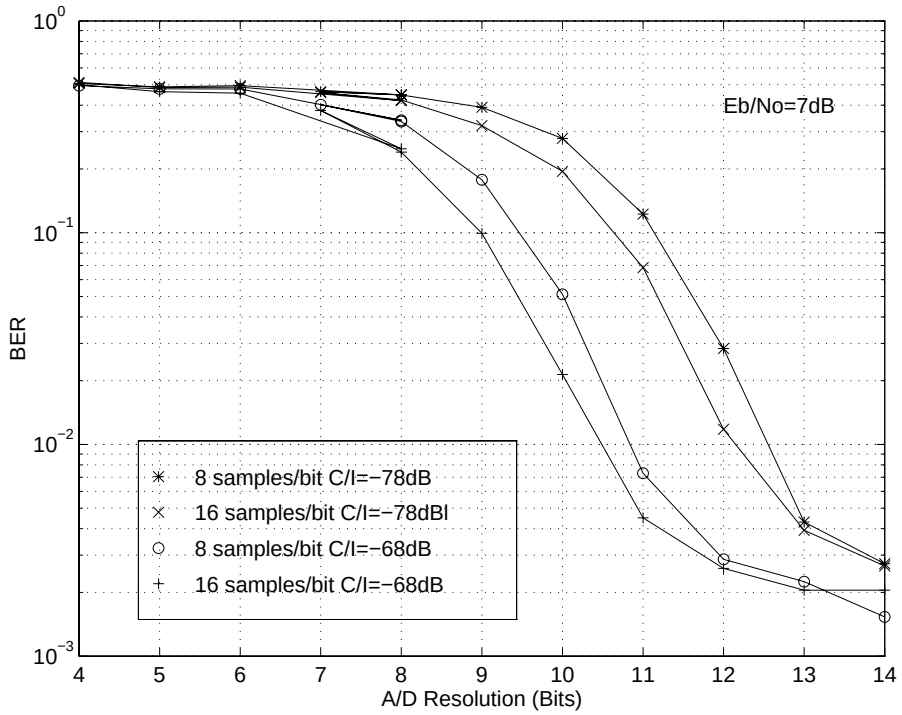


Figure 4.30: GSM BER with C/I=-78dB and Eb/No=7dB

4.5 Summary

The simulations have shown that when an ideal A/D converter model is used in simulation and no interference is present, four or more bits of resolution produce negligible performance loss. However, when interference is present, the narrowband standards require significantly more dynamic range. Also, we have shown that overload distortion in narrowband systems must be avoided because of the catastrophic degradation in error performance when interference is present. Spread spectrum systems such as IS-95 however, can have some amount of overload and still perform well.

Table 4.2: Summary of A/D performance requirements for AMPS, IS-54, IS-95, and GSM for a multimode receiver with 1.25MHz analog bandwidth.

Standard	Threshold Sensitivity	Resolution	SFDR (dB)	IM (dB)
AMPS	5dB C/N	10	57	70
IS-54	5dB Eb/No	8	42	65
IS-95	6dB Eb/No	4	-	-
GSM	4dB Eb/No	11	68	58

We summarize in Table 4.2 the A/D performance requirements for each of the standards for a multimode receiver assuming a 1.25MHz analog bandwidth. GSM has the highest resolution requirement, but AMPS requires very good intermodulation performance. No specification for SFDR and IM for IS-95 is given based on the assumption that the analog selectivity is adequate to reject interference prior to the A/D.

If the bandwidth of the multimode radio is increased to several Mhz, the resolution requirement for GSM goes up to 13 bits because of the higher blocking spec at larger frequency offsets. For comparison, the GSM basestation specification requires the receiver must accept a -13dBm interferer while receiving a signal 3dB above the reference sensitivity level (specified at -104dBm). Thus we would expect a converter with greater than 15 bits would be required for a GSM digital basestation which digitized the entire GSM bandwidth.

In general, the narrowband standards require higher resolution. However, in a multimode receiver with a high sample rate (high enough to digitize IS-95), we can receive substantial oversampling benefit. For example, with a sampling frequency of 2.5MHz, we receive approximately $10\log(2.5x10^6/60x10^3 = 16.2$dB, or about 2.7bits. This oversampling benefit is predicated on the converter being linear, since spurious products will not be reduced by oversampling.

Chapter 5

Dynamic Range Improvement Techniques

From the results of the previous chapter, it is clear that a broadband software radio requires very high dynamic range. One way to improve the dynamic range of the analog to digital interface is to increase the number of bits in the A/D converter. This, however, results in an increase in complexity and power, both of which are undesirable for a mobile receiver. In this chapter, techniques for improving the performance of the analog to digital interface in digital radio receivers will be described. In the first two sections of this chapter, techniques which have been used extensively in the digitization of speech are examined for their applicability to modulated bandpass waveforms with interference. Next, dithering techniques are described which are shown to significantly improve the spurious response of wideband analog to digital converters. Lastly, we describe the development of a novel spread spectrum digitization technique which is readily implemented and offers dynamic range and resolution benefits.

5.1 Nonuniform Quantization and Companding

Uniform quantizers provide minimum mean-squared error (MSE) only when the pdf of the input signal is uniform and fills the full-scale range of the quantizer. When the pdf is nonuniform, improved performance can be obtained by concentrating quantizer levels in areas where the pdf is maximum. In this manner, larger quantization

errors are allowed to occur for inputs with low probability. The well-know Lloyd-Max algorithm [54] allows the computation of quantizer levels for any arbitrary input distribution to minimize the mean-squared error at the output.

While applying these algorithms may seem a natural course to pursue to improve the resolution of A/D converters in radio, several problems exist because of the nature of the wideband radio signal. First, the improvement in MSE over a uniform quantizer is relatively modest. The improvement is a function of the number of levels used, with little improvement seen at low resolutions. For Gaussian distributed inputs, the SNR with an optimal quantizer is approximately [48]:

$$SNR \approx 6.02b - 3.2 \text{ dB} \tag{5.1}$$

when the number of levels is large. For a uniform quantizer with a Gaussian input the SNR is approximately $6.02b - 9$ dB. This difference (about 6dB or 1 bit) may be significant for certain applications. However, in a digital receiver the pdf of the input signal is generally unknown and constantly changing with channel variations and differences in the level of interference, and hence the quantizer thresholds would have to be adapted dynamically. This would be difficult to implement in a high speed A/D converter with many levels. Most importantly, the Lloyd-Max algorithm seeks to minimize the mean-squared error between the output and the total input signal of the quantizer. In a typical wideband radio application, the total input signal consists of a narrowband desired signal and several narrowband interferers. The metric of interest for such an application is the quantization distortion appearing in the band of interest after subsequent digital processing (i.e. filtering). The Lloyd-Max algorithm optimizes the total distortion, but does not stipulate where in frequency the generated distortion products lie.

A more practical method for nonuniform quantization which has been used extensively in speech is instantaneous companding. As shown in Figure 5.1, the input to a uniform quantizer is pre-processed with a monotonic nonlinearity. After quantization, the signal is passed through a nonlinearity with the inverse characteristic to recover an undistorted version of the input signal. The net effect is identical to nonuniform quantization. For speech, a logarithmic compression characteristic is often used. In North America, the standard for companded speech is known as the μ-law quantizer, which has a compression characteristic given by:

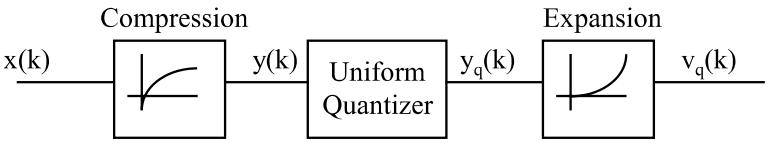


Figure 5.1: Block diagram of quantizer with instantaneous companding

$$y(x) = sgn(x)\frac{\log(1+\mu|x|)}{\log(1+\mu)} \tag{5.2}$$

where μ is a parameter which determines the degree of compression (typically set to 255 for speech). The μ-law companding characteristic is shown in Figure 5.2 for various values of μ. The overall transfer and error characteristic is shown in Figure 5.3 for a 5 bit quantizer with $\mu = 100$. Clearly, the quantization error is small for low level signals and large for higher signals. The primary advantage of companding is that the companded quantizer is relatively insensitive to changes in the pdf of the input signal. Additionally, unlike a uniform quantizer, the range of input power over which the maximum SNR is attained is relatively large, as compared in Figure 5.4. These attributes make companded quantizers especially useful for speech signals, which are nonstationary in nature and spend extended periods of time at low levels.

Unfortunately, logarithmic companding does not seem to work well for narrowband signals in the presence of interference. Two reasons exist for this. First, the compandor characteristic favors signals which dwell at low input levels. While the desired input signal may be at a low level, a simultaneously present strong interferer "carries" the low level signal throughout the quantizer full scale range, including the regions where the quantizer error is high. Therefore, the average distortion can be higher than obtained with uniform quantization. The second problem is the introduction of nonlinear distortion. Ideally, the effect of the compression characteristic can be perfectly inverted since it is monotonic. However, the nonuniform error characteristic in Figure 5.3 generates significant harmonic distortion. Figure 5.5 shows the output power spectra of an 8 bit uniform quantizer and an 8 bit μ-law quantizer (μ=255) when the input consists of a weak sinusoid and a strong interfering sinusoid at a different frequency. In both cases, small-scale dither with a uniform pdf from $\pm$ one-half LSB is added to remove the effect of high-order nonlinearities. The

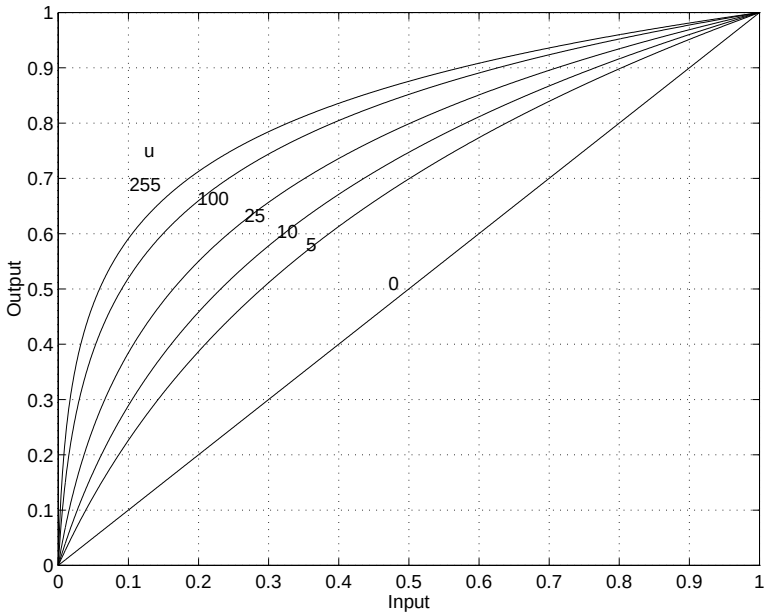


Figure 5.2: Compression characteristic for a μ-law quantizer

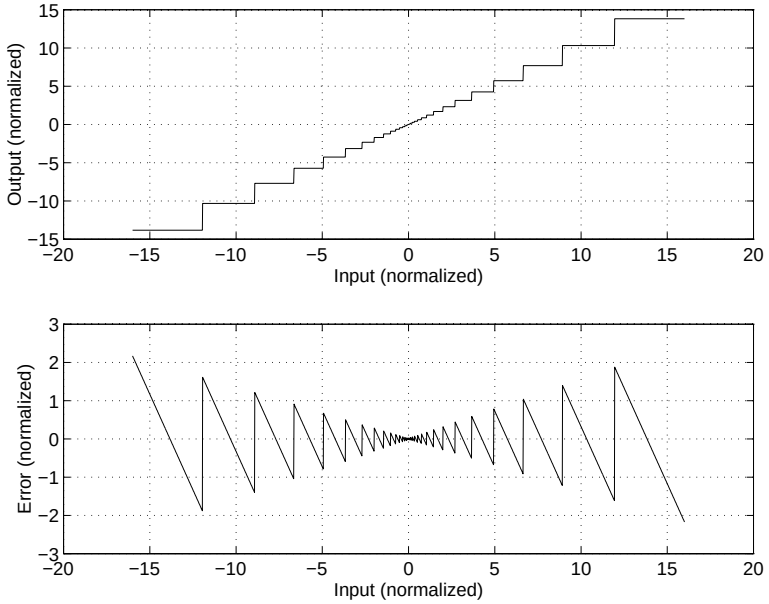


Figure 5.3: Transfer and error characteristic for a 5 bit μ-law quantizer with $\mu = 100$

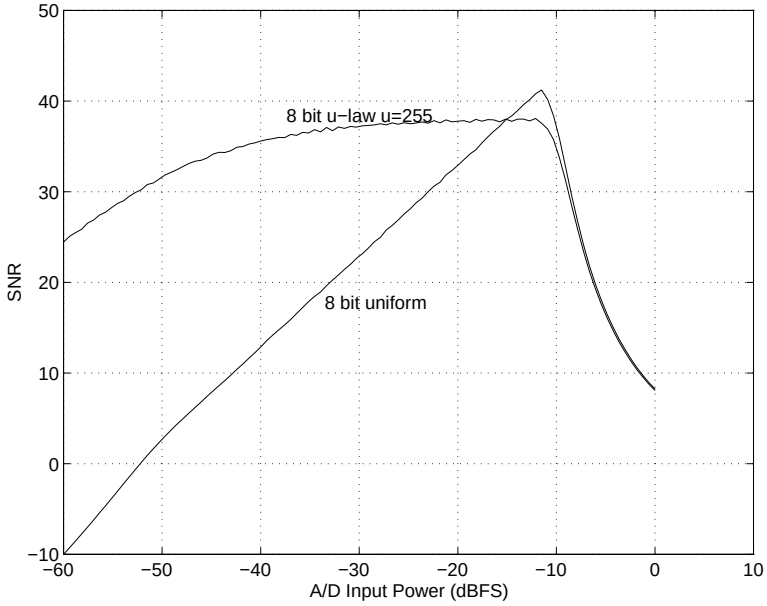


Figure 5.4: SNR comparison for 8 bit μ-law quantizer ($\mu = 255$) and an 8 bit uniform quantizer with Gaussian input as the input power varies relative to full scale

μ-law quantizer exhibits both a higher noise floor and significant spurious outputs. Even with a high number of bits, additional nonlinear distortion will be added due to the inevitable mismatch between the analog encoding characteristic and the digital inverse operation.

5.2 Adaptive Techniques

Adaptive signal processing can employ the power of DSP to overcome the imperfections of the analog front-end, including the A/D converter. In a sense, we may view the analog front-end as an extension of the channel. Although some of the impairments introduced by the analog components are different than are typically found in the channel (i.e. nonlinear distortion), adaptive processing may still be used to compensate for them, either entirely in the digital domain or by adjusting analog circuitry with software based algorithms.

One A/D specific technique which has been proposed is to adaptively trim the A/D converter thresholds to reduce differential and integral nonlinearities, with the

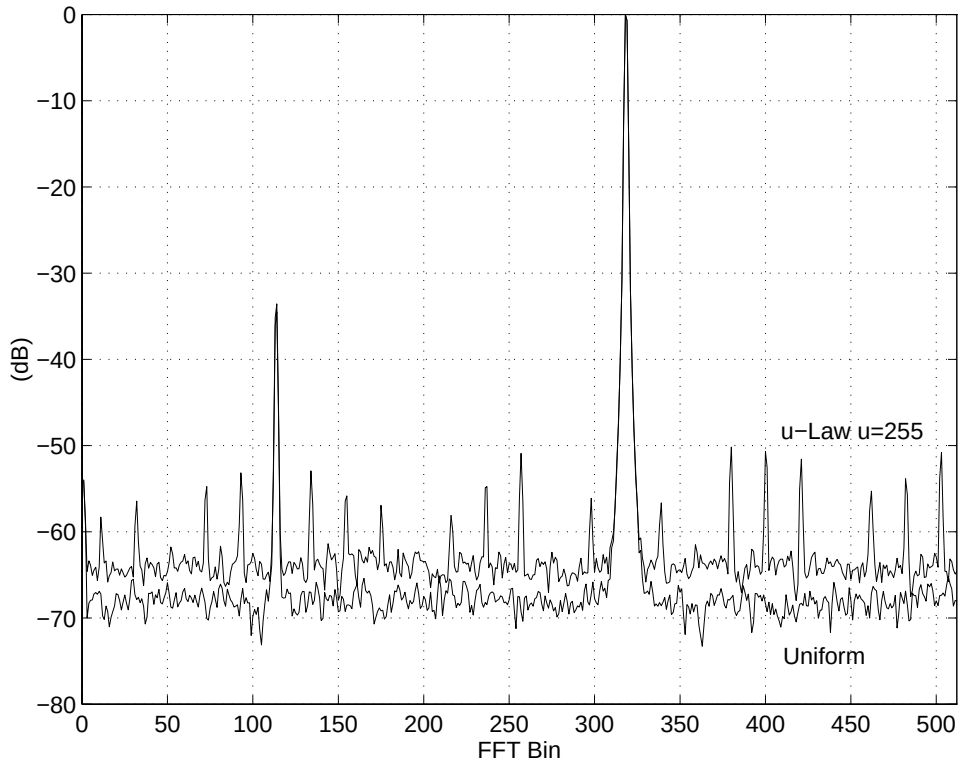


Figure 5.5: Power spectrum of the output of an 8 bit μ-law ($\mu = 255$) and and 8 bit uniform quantizer when the input consists of a strong sinusoid and a weak sinusoid

goal of making the converter uniform [55, 56]. The A/D is trained with a uniformly distributed input and the A/D thresholds are adapted such that the output codes occur with equal probability.

For speech signals, differential quantization exploits the high sample to sample correlation in the speech waveform by using previous samples of the speech waveform to estimate the present value and quantizing the difference. The prediction may be improved by adaptively estimating the parameters of the model which describe the signal. Adaptive prediction has also been used to predict and eliminate radar clutter from the A/D input in radar receivers [57]. Such interference cancelling techniques could be used for cellular radio receivers to adaptively filter strong out of band signals.

An adaptive quantization technique has been proposed for the rejection of narrowband cochannel interference in spread spectrum signals [58, 59, 60]. In this technique, the quantization thresholds of a 2-3 bit converter are adapted to cause threshold transitions to be dominated by changes in the PN code instead of the narrowband interference.

5.3 Dither

Dithering is a process in which a random signal is added to the signal at the input of a quantizer to improve its dynamic range and resolution. Resolution improvement is achieved by the additive dither signal forcing the input signal to randomly cross at least one threshold even when the input signal is below a single quantization step. Thus by averaging at the output of the converter, resolution below an LSB is possible. More importantly for our application, dither decorrelates the quantization noise from the input signal, and therefore whitens the error spectrum when narrowband signals are present at the input.

To elaborate, recall from Chapter 2 that even for an ideal quantizer, the error spectrum is white and the error is uncorrelated with the input only when the number of levels in the quantizer is high, the input exercises many levels in the quantizer, and the input is not periodic[1]. Sinusoidal inputs, being periodic, do not meet this criteria, and exhibit significant harmonic and intermodulation components in the

[1]The last two conditions imply the signal is "rich" in both frequency content and amplitude distribution over the quantizer full scale range

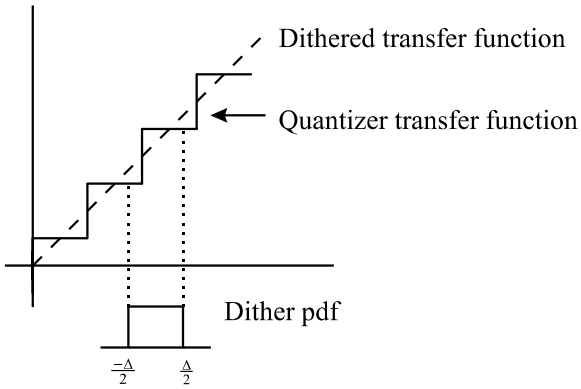


Figure 5.6: Dither as a convolutional process

digitized output[2]. However, when a small amount of noise is added at the input, the spurious outputs fall below the noise floor. Work by Schuchman, Blachman and others [61, 62, 10] has determined that the effect of a nonlinear transfer characteristic on a signal in the presence of noise is equivalent to passing the signal through a new nonlinearity whose transfer function is the convolution of the pdf of the noise and the original transfer characteristic. Figure 5.6 graphically illustrates this process. For an input dither processes uniformly distributed on $[-\Delta/2, +\Delta/2]$, the resulting characteristic is perfectly linear and the converter nonlinearities have been completely eliminated.

Dither with this magnitude is termed small-scale dither. When threshold errors are present in the quantizer, small-scale dither is no longer adequate and large-scale dither techniques must be used. With small-scale dither, the added noise adds 3dB to the quantization noise floor (the added noise is equal in power to the quantizer noise) which is often neglected. Large-scale dither techniques utilizes higher noise power, and the extra noise may not be tolerable at the converter output. Two techniques are commonly used to eliminate the dither signal from the A/D output. The first, depicted in Figure 5.7, is useful for bandpass digitization schemes. Because the efficacy of the dither signal relies on its univariate pdf and not its frequency spectrum, the dither may be added outside of the band of interest where it will be rejected by

[2]In addition to violating the requirement for frequency "richness", periodic input signals sampled with sample rates at integer multiples of the input frequency may have only a small number of discrete sample values, violating the requirement of exercising many levels in the quantizer

digital filtering after digitization. A second technique, shown in Figure 5.8, generates the dither signal digitally using a pseudo-noise generator. The digital noise signal is converted to analog using a D/A converter and later directly subtracted from the digital output of the A/D.

To see the effect of large-scale dither, an eight bit two-step converter with differential and integral nonlinearities was simulated with a sinusoidal input and subtractive dither. The results for various levels of RMS dither (relative to an LSB) are plotted in Figure 5.9. The spectra are computed using an averaged periodogram with FFT length 1024, overlap of 512, and a record length of 2^{14} samples. In the upper right, small-scale dither is seen to provide some benefit in smoothing the localized nonlinearities of the stairstep (ideal) transfer characteristic. However, the lower order distortion terms are not eliminated until the RMS dither level is increased to eight LSB's. Because the total input of signal plus dither must be maintained below the full-scale range of the A/D, there exists an optimum level of dither to add before the signal to quantization noise floor is reduced. This is seen in the bottom right plot in Figure 5.9 when the dither is increased to from 15 to 35 LSB's. Because the performance improvement is a function of the specific converter, it is not possible make quantitative generalizations regarding the benefit of large-scale dither. However, significant improvements in SFDR of 15 to 25 dB have been reported [63, 64].

For wideband radio applications, channel noise alone can provide substantial dithering. For example, consider a single desired signal at full scale power, i.e.

$$C = \frac{\left(2^{b-1}\Delta\right)^2}{2} \tag{5.3}$$

where we have used a peak to average power ratio of 1/2 (sinusoidal). Then, with

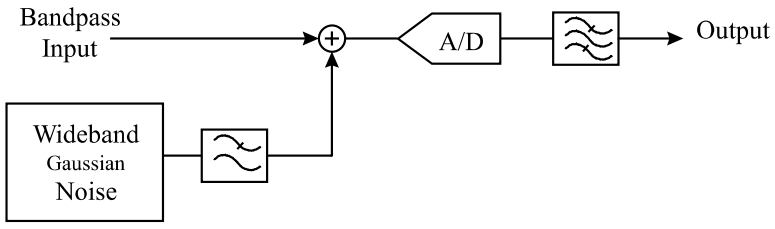


Figure 5.7: Out of band dither block diagram

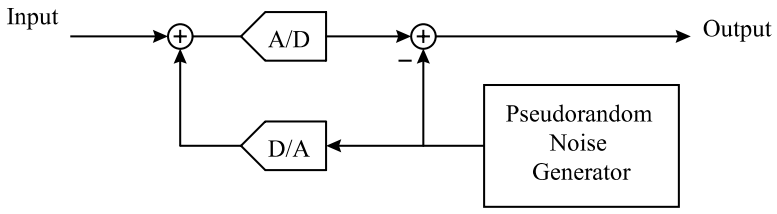


Figure 5.8: Subtractive dither block diagram

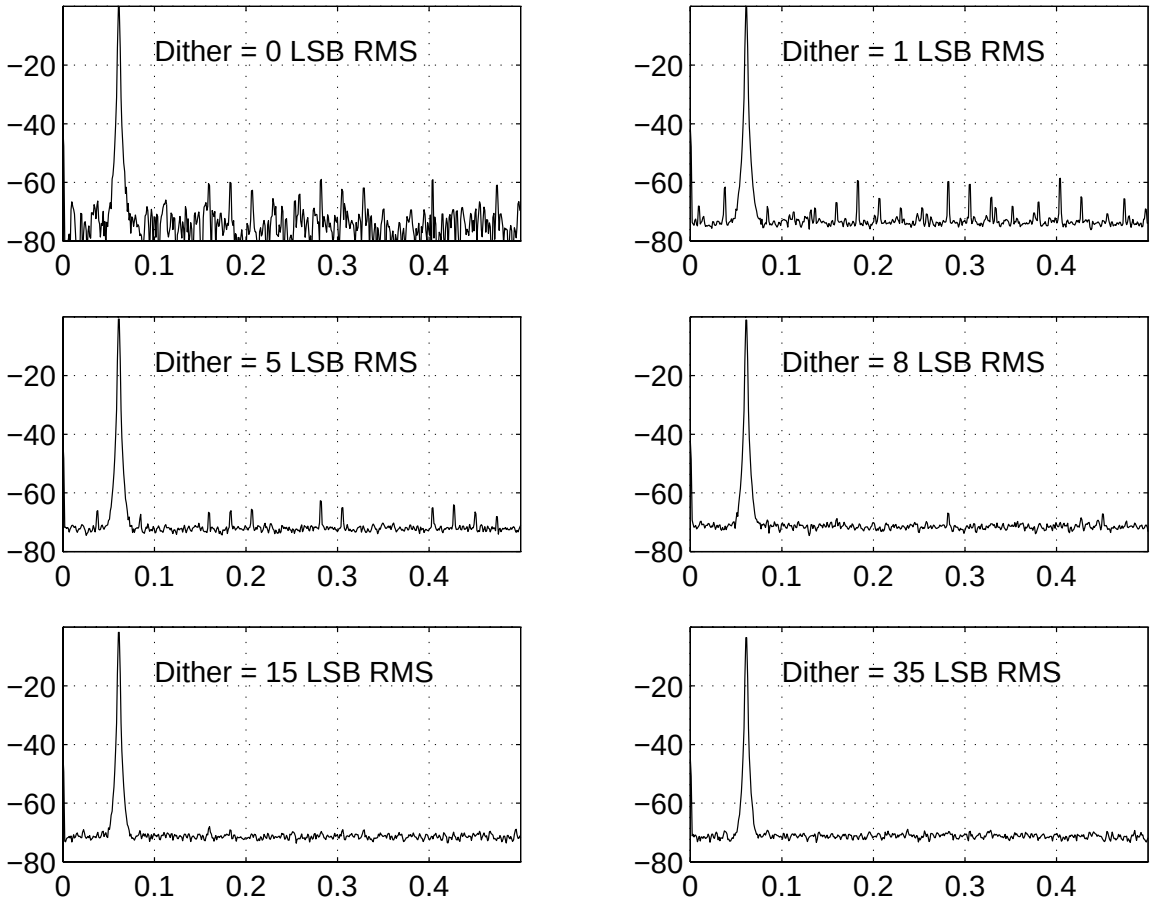


Figure 5.9: Output spectra of an 8 bit nonideal two-step A/D with subtractive uniformly distributed dither with RMS levels of 0,1,5,8,15, and 35 LSB's

simple manipulations similar to those previously performed, the RMS channel noise relative to a quantization step is

$$\frac{\sigma_N}{\Delta} = 2^{b-1}\sqrt{\frac{1}{2}\frac{1}{(C/N)}\frac{fs}{2B}} \tag{5.4}$$

The relative "dither" power is a function of the oversampling ratio ($fs/2B$), since more noise is digitized as the sampling rate increases. For example, with C/N=10dB, fs/2B=10, and a 10bit converter (b=10), equation 5.4 gives $\sigma_N = 362\Delta$ from channel noise alone.

However, when the signal is dominated by interference and the interferer is set to full-scale, equation 5.4 can be modified to give

$$\frac{\sigma_N}{\Delta} = 2^{b-1}\sqrt{2\frac{(C/I)}{(C/N)}\frac{fs}{2B}} \tag{5.5}$$

With the same parameters as above but with a carrier to interference ratio C/I=-60dB, the relative noise power is $\sigma_N = 0.724\Delta$. Since the channel noise is less than a single quantization step, little dithering is accomplished.

Other types of dither signals such as sinusoids have been proposed for improving the dynamic range of A/D converters [65], but are not as effective as random noise. Lastly, we note that dithering is able to smooth out localized nonlinearities, but cannot improve overload distortion or low order (i.e. second and third) smooth nonlinearities as may be introduced in the A/D sample and hold.

In simulating modulated signals, we have noted that harmonic and intermodulation levels predicted with sinusoidal inputs do not predict the distortion well when digitally modulated signals are used as the excitation, even if the sinusoidal tests include small-scale dither. Similar results have been reported on RF power amplifiers, where traditional single and two-tone intermodulation tests have been found inadequate to predict intermod levels and spectral regrowth for IS-54 modulated signals[66]. We suggest that in A/D converters, the randomly modulated digital signal exhibits a certain amount of self-dither, whereby the harmonic distortion levels are reduced due to the random nature of the signal being quantized.

5.4 A Novel Spread Spectrum Quantization Method

Recognizing that dither reduces the spectral artifacts from quantization by randomizing the input, we have invented an alternative method which uses direct sequence spread-spectrum techniques to whiten the input of the A/D. Schemes in which the quantizer thresholds are pseudorandomly shifted from sample to sample have been described [67], but our scheme is unique in that the signal itself is spread and quantized with a specialized quantizer characteristic. The block diagram for the method appears in Figure 5.10. The input signal is sampled at a rate much higher than the signal bandwidth and multiplied by a pseudorandom constant-modulus (± 1) code[3]. Next the signal is quantized with an offset quantization characteristic, depicted in Figure 5.11. For positive inputs, the characteristic is an ordinary midriser quantizer. For negative inputs, a 1/2 LSB shift is introduced resulting in a midtread transfer function. The offset characteristic is essential to the operation of the system, as will become clear shortly. To accommodate the shift, the full scale range of the quantizer is reduced for negative inputs by 1/2 a quantization step[4]. After quantization, the signal is correlated with the pseudorandom code (despread and filtered) to form an estimate of the original signal.

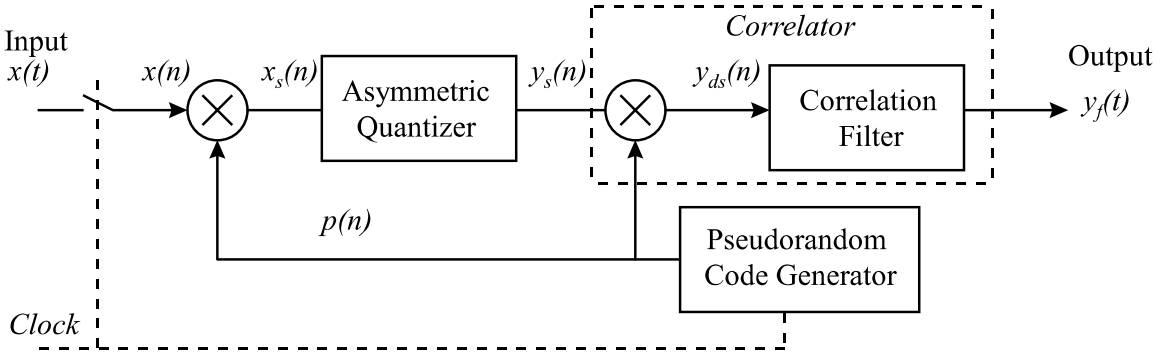


Figure 5.10: Block diagram of the proposed spread-spectrum quantizer

[3]Alternatives of spreading prior to sampling or interpolating after spreading were considered but offer no benefit and have higher complexity. Also, sampling multiple times per chip is not needed and has no benefit

[4]This is not of great consequence, particularly when one considers that the same limitation applies when the additive power of a small-scale dither signal requires the same reduction in signal level to avoid overload.

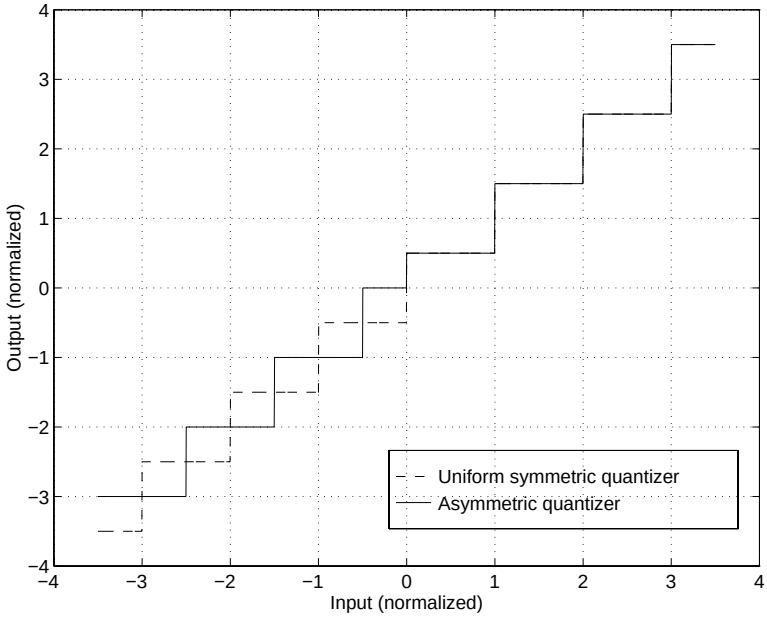


Figure 5.11: Transfer characteristic of the asymmetrical quantizer

The spread input sequence is denoted $x_s(n)$ and is given by

$$x_s(n) = x(n) \cdot p(n) \tag{5.6}$$

where $p(n)$ is a constant-modulus ($p(n) \in [+1, -1]$) spreading code. The quantizer output $y_s(n)$ is given by

$$y_s(n) = x_s(n) + e[x_s(n)] \tag{5.7}$$

where the error is defined exactly as $e = Q[x] - x$ where $Q[x]$ denotes the quantization operation[5]. The signal is despread by multiplying it again with the known spreading code, i.e. $y_{ds}(n) = p(n) \cdot y_s(n)$ and filtered to recover the original signal.

To see why a modified quantizer transfer characteristic is required, note the error obtained from a uniform symmetric quantizer is an odd function, ($e[v] = -e[-v]$). Thus

[5]Note $e[x]$ is the exact deterministic error as a function of input and not the random noise model.

$$
\begin{aligned}
e[x_s(n)] &= e[p(n) \cdot x(n)] \\
&= \begin{cases} +e[x(n)] & \text{for p(n)=+1} \\ -e[x(n)] & \text{for p(n)=-1} \end{cases}
\end{aligned} \tag{5.8}
$$

therefore $e[x_s(n)] = p(n) \cdot e[x(n)]$ and

$$
\begin{aligned}
y_s(n) &= x_s(n) + e[x_s(n)] \\
&= p(n)\{x(n) + e[x(n)]\}
\end{aligned} \tag{5.9}
$$

and

$$
\begin{aligned}
y_{ds}(n) &= p(n) \cdot y_s(n) \\
&= p^2(n)\,(x(n) + e[x(n)]) \\
&= x(n) + e[x(n)]
\end{aligned} \tag{5.10}
$$

The last line in Equation 5.10 is exactly the same sequence as is obtained by directly quantizing the input without spreading. This occurs because the error from the symmetric quantizer is perfectly correlated with the code. To synthesize a better error transfer characteristic, recognize that by necessity, any quantizer input to output characteristic comprised only of risers (unit jumps) and treads (segments with slope zero) must have an error transfer characteristic composed of segments of slope minus one and unit jumps [6]. Also, to remove the correlation with the code, we want the error characteristic to be similar for positive and negative chips. The error characteristic which best achieves this corresponds to the transfer characteristic in Figure 5.11 and is plotted in the top part of Figure 5.12. In the bottom plot of Figure 5.12, the error characteristic (before correlation) for positive and negative chips is plotted separately by reflecting the error about the y axis for negative chips. Because the error no longer is odd, the resulting quantization error sequence is less correlated with the code, and we obtain a randomized error sequence after despreading.

An additional benefit is that the spread spectrum quantizer has twice the resolution of an ordinary quantizer with the same number of levels. This is better understood by separately considering the input to output transfer characteristic for

[6] Recall that $e(x) = Q[x] - x$, i.e. the error is the stairstep minus a ramp with slope one.

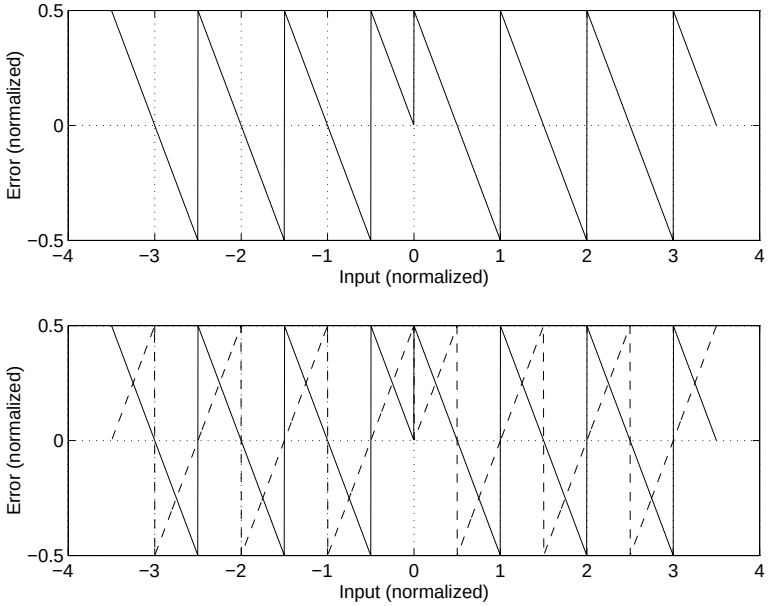


Figure 5.12: Error transfer characteristic for the asymmetric quantizer (top) and error characteristics for positive (solid) and negative (dashed) chips (bottom)

positive and negative chips after despreading. This is shown in Figure 5.13, where the characteristic for negative chips is formed by reflecting the original characteristic about x and y (corresponding to multiplying the input by -1 and output by -1). For simplicity, only the portion for positive inputs is shown. For a low frequency input (one whose input samples are essentially constant from chip to chip), the output sequence switches between the two characteristics, and averaging over multiple chips allows the input sample to be interpolated to twice the resolution as would be obtained with either characteristic alone. The accuracy of the average is affected by the number of chips which occur before the input causes a code transition on the unreflected transfer characteristic, which in turn is determined by the frequency of the input signal. Thus the resolution improvement is a function of the processing gain of the spread spectrum system.

5.4.1 Simulation Results

In Figure 5.14, the transfer characteristic of the system is simulated by stepping the level of a DC signal at the input and averaging the output over the entire record

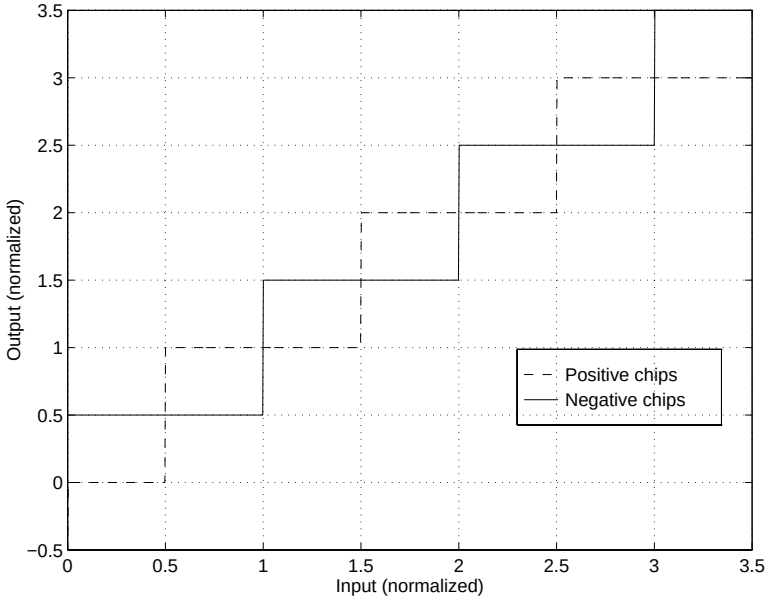


Figure 5.13: Asymmetrical transfer characteristic (positive inputs only) for positive and negative chips

length(1024 samples). The asymmetrical quantizer has 8 levels, and the output consists of 14 levels ($2^4 - 2$). The increase in resolution is slightly less than a factor of two because of the reduction in full-scale range due to the offset in the asymmetrical quantizer. Figure 5.15 shows the response of the spread spectrum quantizer to a sinusoidal input. Segments of the code are seen in the output with amplitude $\Delta/2$ at steps of $\Delta/2$. The lowpass filter in the correlator averages over these local variations and reconstructs the original signal. In Figure 5.15 the reconstructed input is shown when a 20 tap boxcar filter is used as the correlating filter. The boxcar filter (equal coefficients) implements a simple average and was used for simplicity; other reconstruction filters may provide improved performance.

Simulated spectra for an undithered uniform quantizer, a uniform quantizer with 1/2 LSB uniform dither, and the spread spectrum quantizer (SSQ) are shown in Figures 5.16, 5.17, and 5.18 for 2, 4, and 8 bits of resolution respectively. The input is a tone at a frequency of 37/1024, and the spectrum is estimated with an averaged periodogram with a 1024 point FFT and a record length of 2^{14}. Both the spread spectrum quantizer and dither improve the spectrum dramatically. At low resolutions, the spread quantizer shows some residual spectral artifacts. As the number of bits

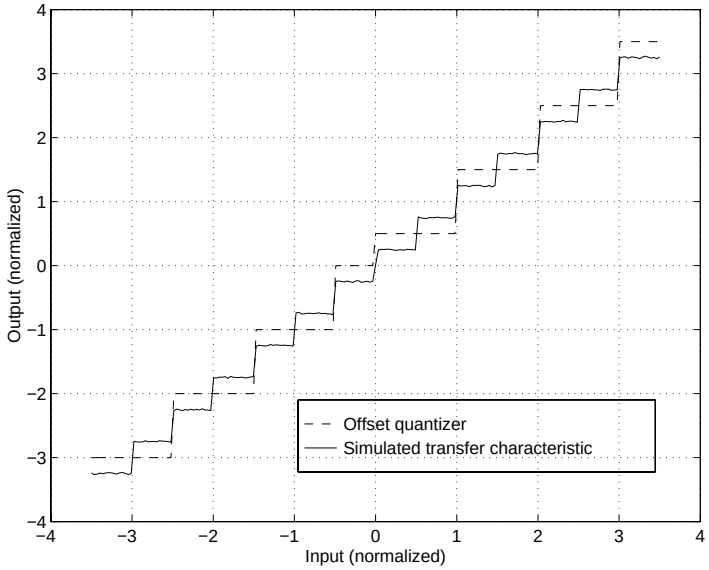


Figure 5.14: Simulated transfer characteristic of the spread-spectrum quantizer

becomes large, the three converters have similar spectra. Note the noise floor for the dithered output is 3dB higher due to the added dither noise.

The autocorrelation of the quantization error for a five bit converter is shown in Figure 5.19. Zero lag is in the middle of the plot, and the regular converter has strong peaks at lags corresponding to the input period. This indicates periodic components in the output which will give rise to line spectra. The spread quantizer has substantially lower autocorrelation for lags greater than zero.

The spectrum of the quantization error with a lowpass random sequence input is shown in Figure 5.20 for a 3 bit converter. The uniform converter has its error concentrated near DC, while the spread quantizer has a nearly white spectrum. The operation of the SSQ is beneficial in that it reduces the peaking of the quantization noise near DC which is the band of interest of the signal.

The mean-squared error (MSE) for both uniform and spread quantizers is shown in Figure 5.21. Because the spread quantizer does not have the low-frequency noise peaking, it exhibits lower noise. When the number of bits becomes large, the peaking at low frequency is less and the difference diminishes.

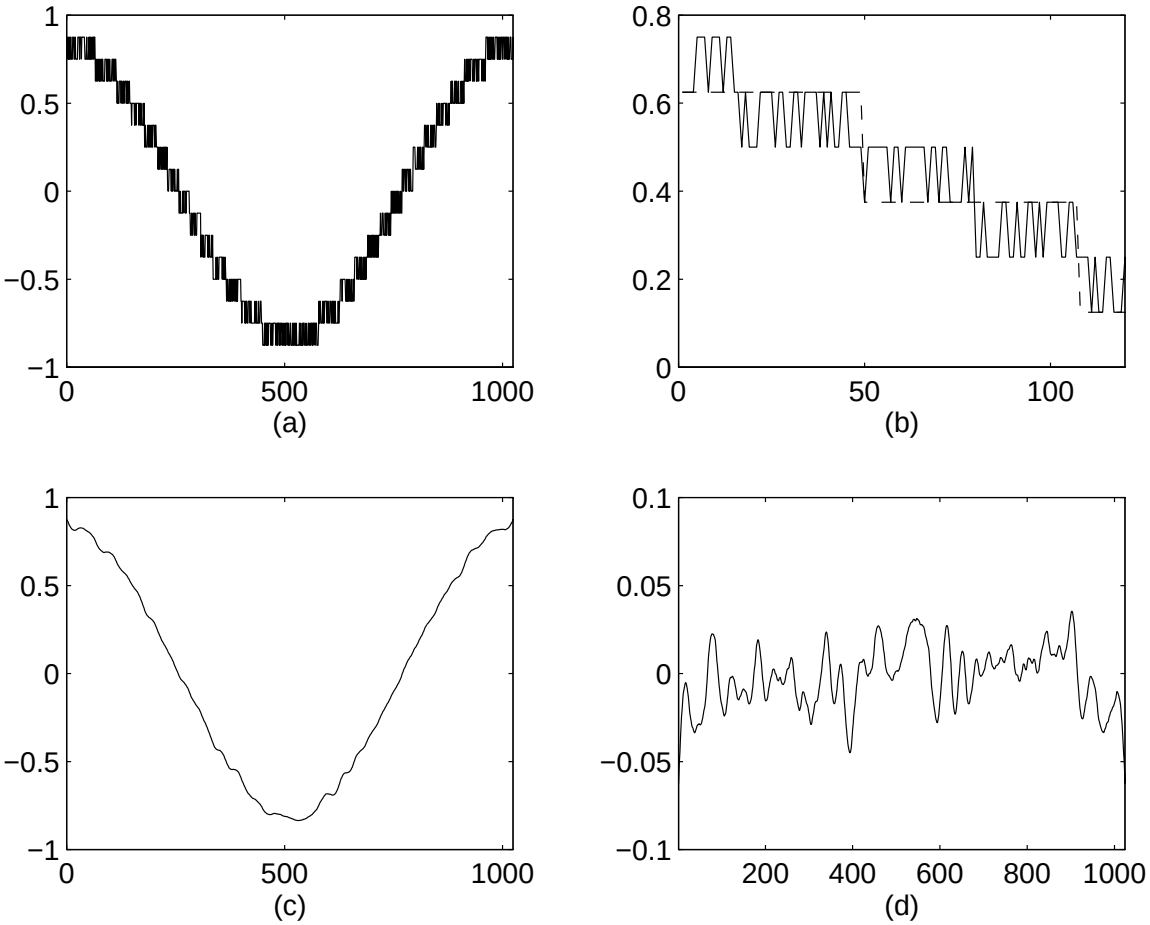


Figure 5.15: (a) Response of the spread-spectrum quantizer to a sinusoidal input, (b) Detail of (a) with ordinary quantizer (dashed), (c) reconstructed output with 20 tap boxcar filter (d) error after reconstruction

5.4.2 Benefits and Limitations

The spreading quantizer does not always seem to perform well with converter nonlinearities. The spreading allows disparate parts of the transfer characteristic to be averaged, but odd order nonlinearities are not compensated. The technique seems more akin to small scale dither than large scale, and as such, may not provide the benefits necessary for improving the dynamic range in a digital radio application. This is not to imply that the spread-spectrum quantization operation is identical to small-scale dither. While both methods randomize the input to the quantizer, dither is an additive process while the spreading quantizer multiplies the input signal with

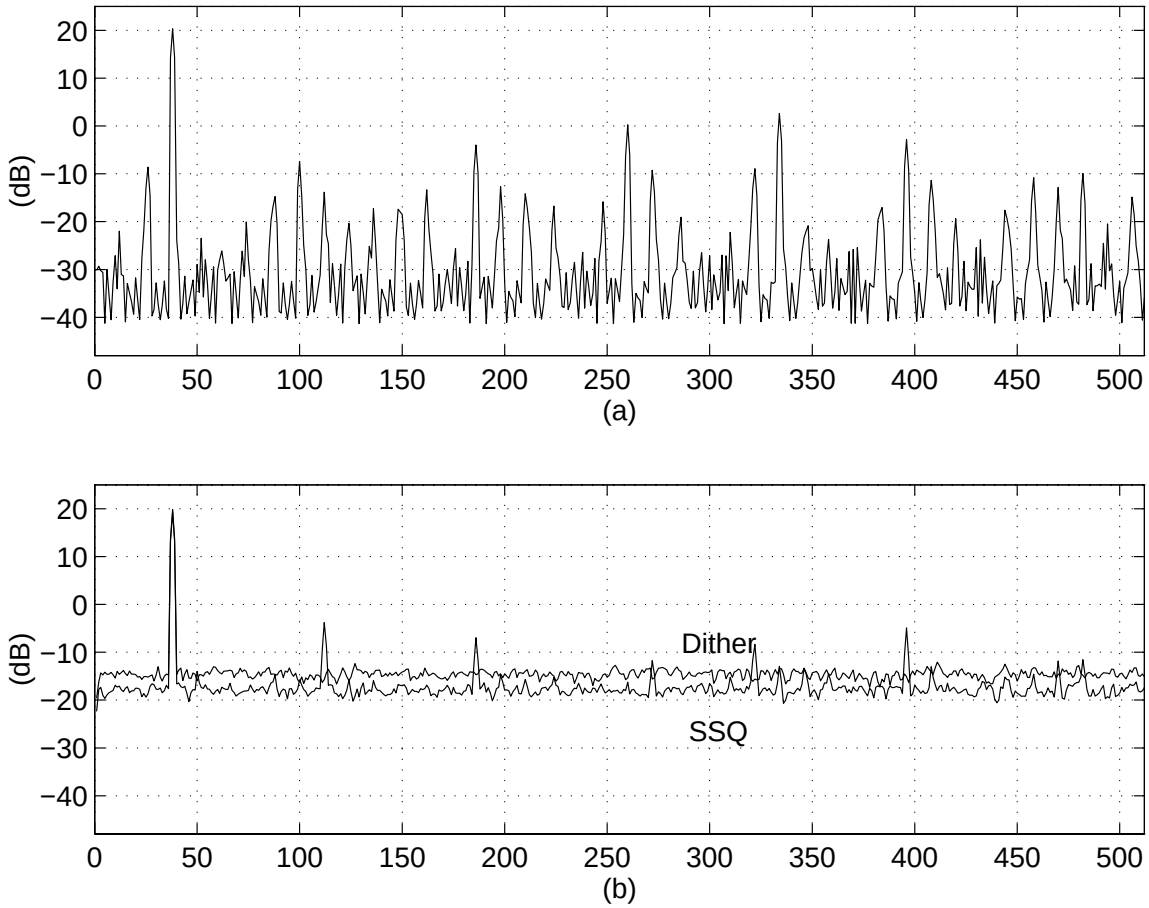


Figure 5.16: Output spectra with a sinusoidal input of an (a) undithered uniform converter and (b) dithered uniform and spread quantizers, 2 bit resolution

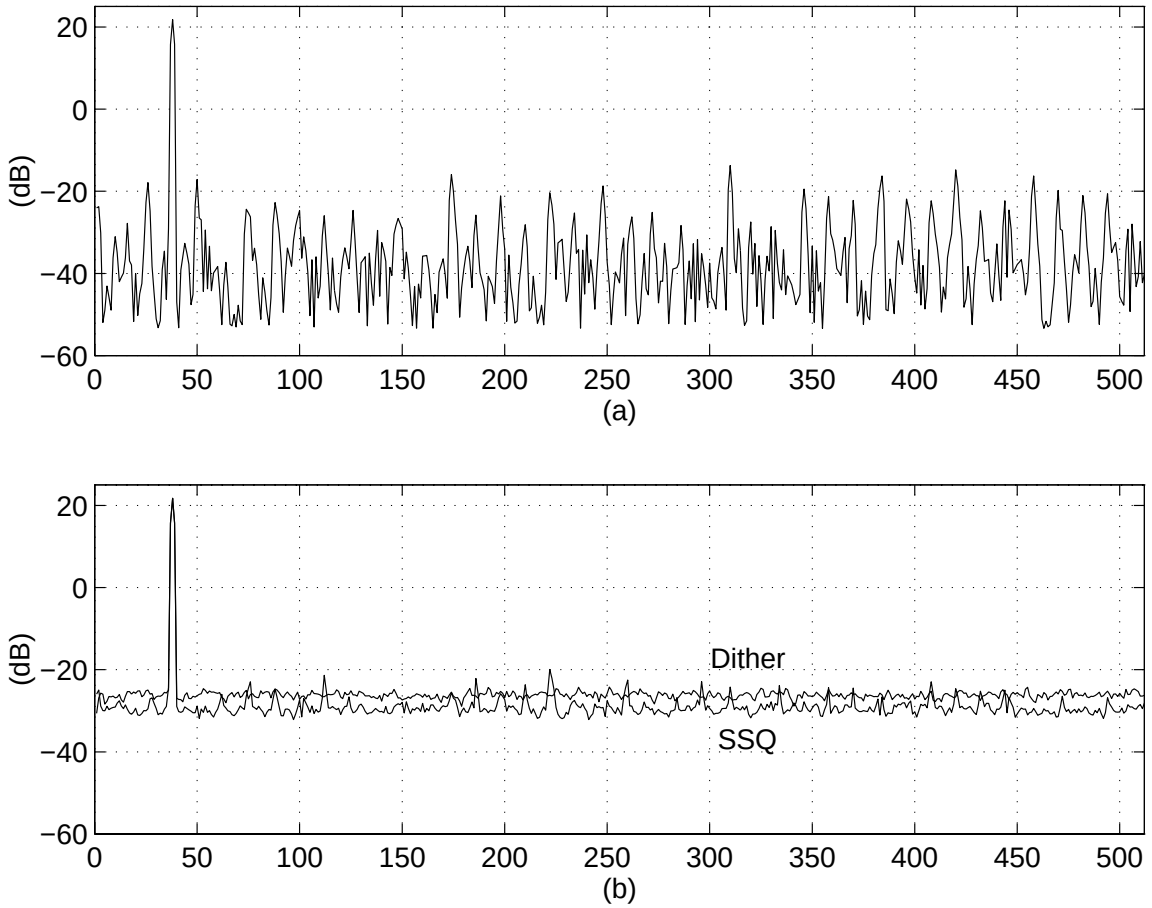


Figure 5.17: Output spectra with a sinusoidal input of an (a) undithered uniform converter and (b) dithered uniform and spread quantizers, 4 bit resolution

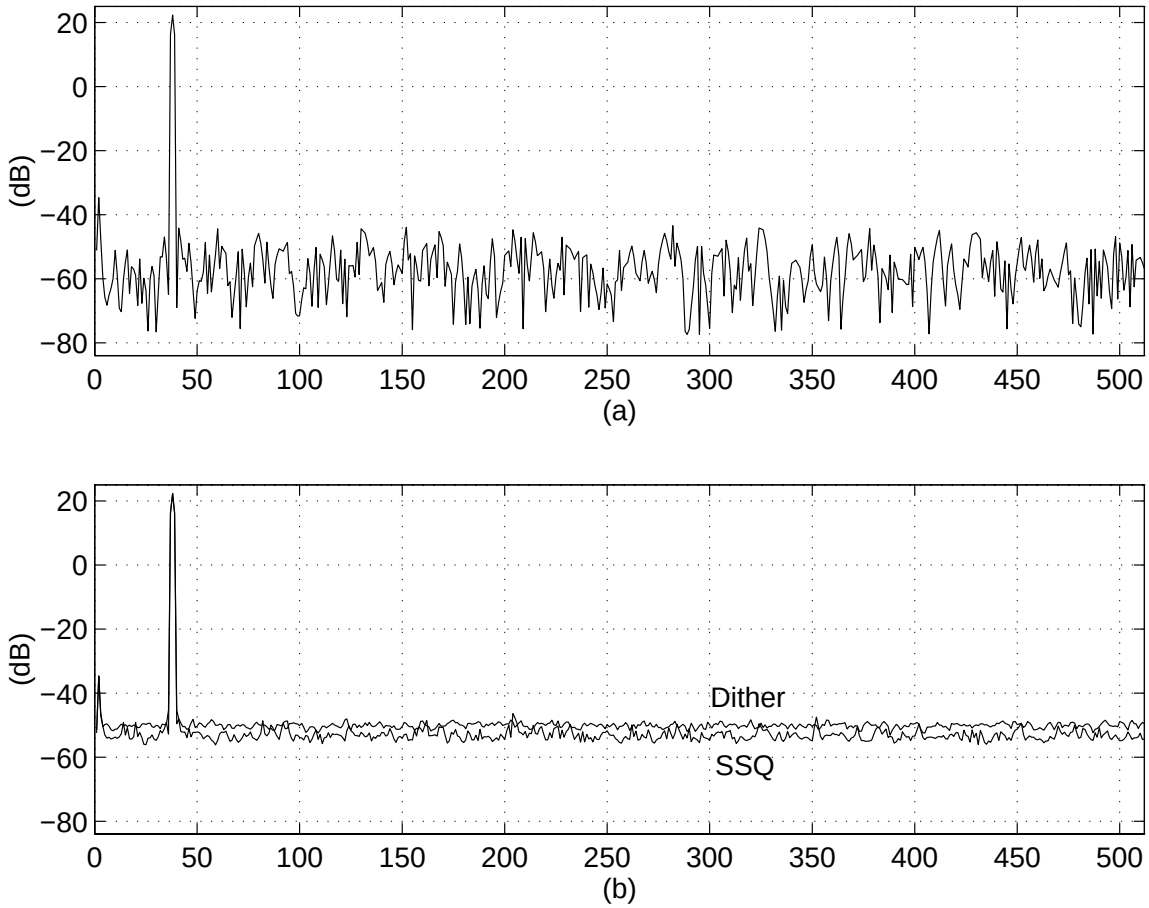


Figure 5.18: Output spectra with a sinusoidal input of an undithered uniform converter (a) and dithered uniform and spread quantizers (b), 8 bit resolution

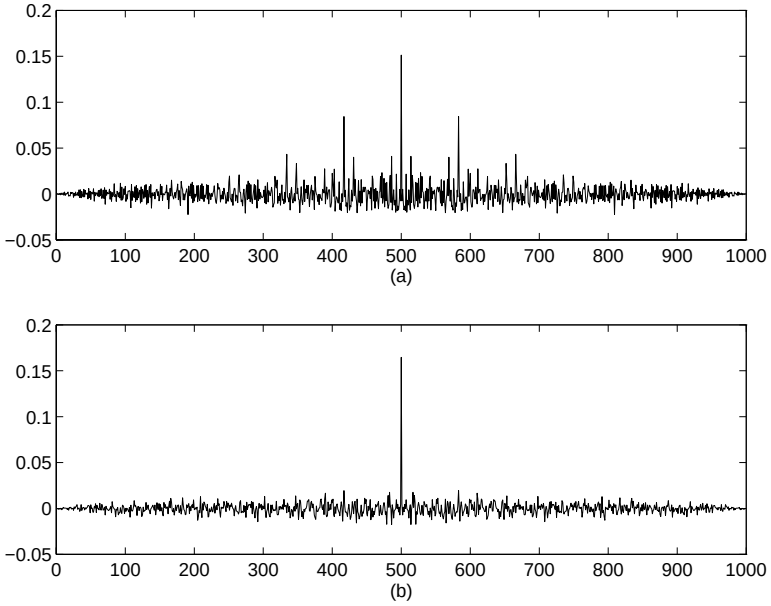


Figure 5.19: Autocorrelation of the quantization error for an 8 bit uniform quantizer and an 8 bit spread quantizer

a random waveform.

One important advantage the spread converter has is its ability to compensate even-order nonlinearities. Included among these are DC offsets, which must be kept low in many applications. DC offsets at the converter input are spread by the code in the correlation process after digitization, and therefore are reduced by the processing gain. In practical A/D's, clock feedthrough and other spurious unrelated to the input are difficult to keep out of the sensitive converter analog front-end. These narrowband products will also be spread and reduced by the processing gain.

The final advantage of the scheme is its ease of implementation. Unlike earlier described dither techniques which require random number generation and a DAC, the spread quantizer needs a code generator and an analog multiply by ± 1. The latter can be accomplished with minimal complexity at high speed by switching differential inputs in accordance with the code. Also, because the code is generated and used locally (as opposed to separately in a transmitter and receiver), no synchronization is required.

In a multimode receiver designed for narrowband and spread-spectrum standards,

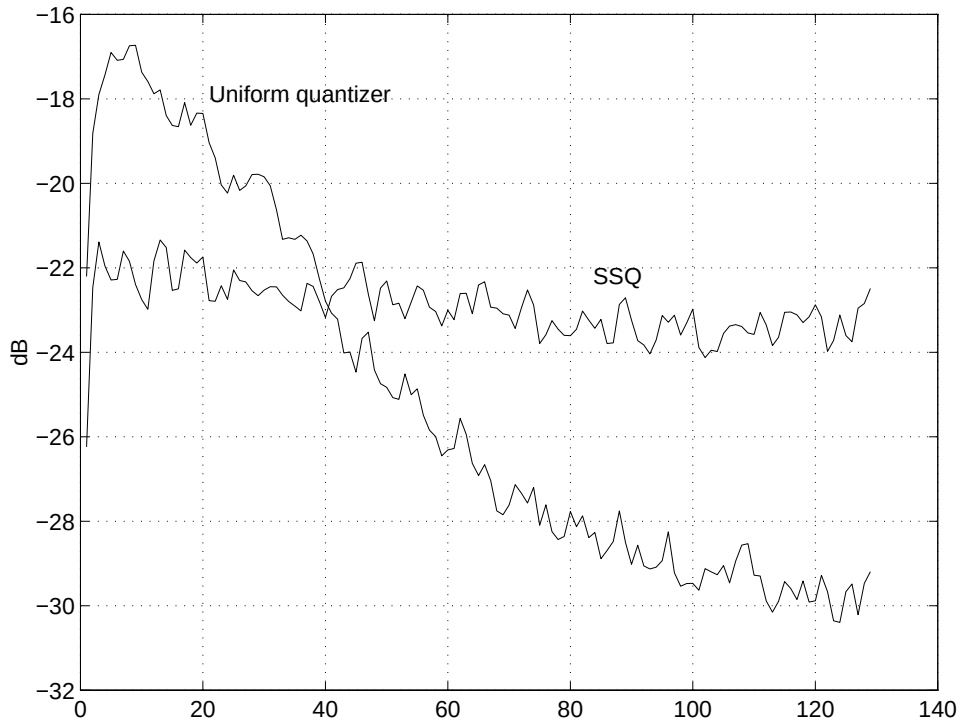


Figure 5.20: Output spectra of a 3 bit uniform converter the spread quantizer with a lowpass Gaussian input, $BW = 800/2^{14}$

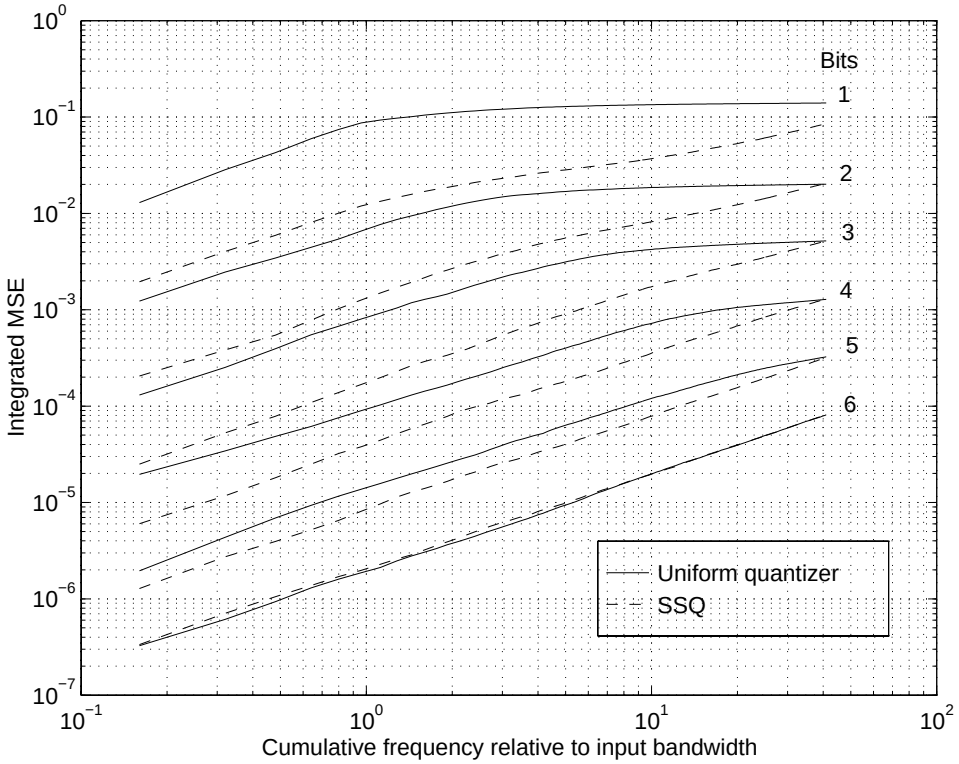


Figure 5.21: Integrated mean-squared error of a uniform quantizer and the SSQ with a lowpass Gaussian input

the receiver will require a correlator to receive the spread-spectrum signal. When the received signal is spread, the input spreader to the SSQ may be disabled and the SSQ correlator may be used for this function.

5.4.3 Extensions

A natural extension of the technique is the use of nonconstant modulus codes to average more portions of the quantizer transfer characteristic and better cancel large-scale errors. This was attempted, but found to give inferior results since the multiplication by the reciprocal modulus (i.e. $1/p(n)$) in the correlation process magnifies the quantization error for code values $\mathrm{p(n)} < 1$[7]. One promising use of nonconstant modulus codes was the ability to partially compensate for overload distortion. This occurs because when an input sample is greater than the full-scale range, samples which are multiplied by codes with small values can be within the full-scale range. These spread samples are digitized without problem. When averaged over many chips, the average overload distortion can be reduced.

The final extension and an important advantage of the technique is the ability to multiplex two or more signals at the input of the A/D using CDMA. This is illustrated in Figure 5.22. Separate inputs are multiplied with distinct spreading codes and summed together at the input of the A/D. After quantization, the individual signals are separated by correlating with their unique codes. If orthogonal codes are used, the constituent signals can be separated perfectly since their code cross-correlations are zero. One benefit of this technique is that all constituent signals use the same quantizer. Therefore, applications which require good matching of A/D converters (i.e. adaptive antenna arrays) could benefit from the technique. As was noted when IS-95 was simulated, the presence of multiple signals at the quantizer input requires the input power of each constituent signal to be reduced to less than full scale, reducing the signal to quantization noise ratio for each individual signal.

[7]Using spreading codes with modulus > 1 does not improve the situation as the full-scale range of the quantizer must be increased accordingly.

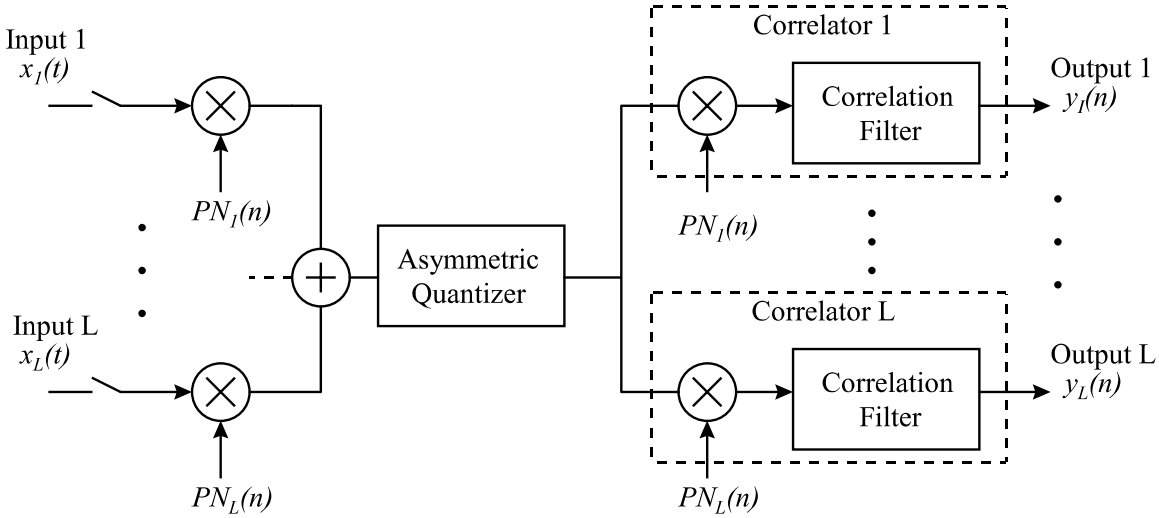


Figure 5.22: Block diagram of code-division multiplexed A/D converter

Chapter 6

Conclusion

We conclude this thesis with a review of the research performed and the observations which be gleaned from it. Promising areas for future research in the areas of analog-to-digital conversion for radio and multimode wireless receivers are also identified.

6.1 Summary of Research

This thesis has focused upon the problem of translating modulated radio signals from the analog domain to the digital domain with high fidelity. We began by reviewing the underlying theory of the constituent operations of A/D conversion, namely sampling and quantization and presented the theory regarding nonlinear distortion introduced by the quantization process. We also presented digital radio architectures and compared IF digitization with baseband digitization. An overview of A/D topologies including flash A/D's, two-step subranging A/D's and sigma-delta converters was presented.

In Chapter 4, we assessed the resolution and dynamic range requirements for A/D converters in receivers capable of demodulating AMPS, IS-54, IS-95 and GSM. A simple analytical model was presented which can be used to predict the degradation in carrier to noise ratio from A/D conversion in the presence of interference when the quantization noise from the A/D can be considered as an additional source of additive white noise and perfect AGC maintains the input signal at the full-scale range of the converter. The model predicts that when no interference is present and the input C/N is less than 20dB, ideal uniform converters with resolutions greater than 4 bits

produce little degradation in C/N.

Simulations of digital receivers with A/D conversion were performed for AMPS, IS-54, IS-95, and GSM. As predicted by analysis, little performance degradation was noted for 4 bits and higher when no interference was present. When interference was present, the linear model continued to predict the performance when ideal converters were used. The importance of good AGC was demonstrated in IS-54 simulations where a small amount of overload was seen to catastrophically degrade BER performance. Forward link IS-95 simulations show that some overload was tolerable when digitizing the noiselike IS-95 signal. The AGC setting which optimizes the BER is a function of the number of users in the system, and the added power from orthogonal MAI decreases the power of the desired user. Simulations indicated that 2-3 bits of resolution is generally adequate. When four or more bits are used, the BER degradation when an AMPS cochannel interferer is present is determined by the processing gain and not limited by the A/D. The resolution requirements for narrowband standards ranged from 8-11 bits with SFDR from 40-70dB.

Lastly, we investigated techniques for improving the dynamic range of digital receivers. Simulations of instantaneous companding proved that the technique is not suitable for narrowband signals with interference because of the generation of significant harmonic and intermodulation distortion. We presented a new spread-spectrum quantization technique which has benefits similar to small-scale dither. Other benefits include the elimination of even order distortion and DC offsets. We have also proposed the use of the spread quantizer for simultaneously digitizing multiple signals by spreading each constituent signal with a unique spreading code.

6.2 Future Work

It became apparent in the course of this work that accurately modeling the nonlinear distortion from A/D converters for system simulation is a difficult (and yet unsolved) problem. Because the level and frequency of spurious products is not simply related to differential and integral nonlinearities or input signal level, it is difficult to make generalizations about the performance of nonlinear converters. The spurious-free dynamic range specified by a converter manufacturer at a single power level provides little usable information for one interested in creating an A/D model for system

simulation. Furthermore, a baseband equivalent model which accurately predicts the performance of IF digitization schemes while allowing efficient baseband simulations is needed.

Bandpass sigma delta conversion is a promising techniques for digitization of bandpass modulated signals in radio receivers. In addition to circuit level work, possible signal processing contributions include improved decimation structures, optimized noise-transfer functions, and adaptation of the noise transfer function. One idea which we began to pursue is the use of sigma-delta converters in a subsampled mode, whereby an IF signal is subsampled relative to the IF frequency but oversampled relative to the signal bandwidth. A second idea is to better exploit the sample rate/resolution tradeoff for the various standards by digitizing the narrowband signals with high resolution and wideband CDMA standard with low resolution.

There are two areas of future research in using adaptive signal processing to improve the ability to convert low-level desired signals in the presence of interference. One is an investigation of the potential of adapting converter thresholds to reject off-channel interference in narrowband signals similar to the technique described in Chapter 5 for direct-sequence spread spectrum signals. The second area is the use of adaptive prediction to predict and subtract interference from a narrowband signal prior to digitization.

From our work, it is clear that the performance of the A/D is strongly dependent on the AGC. A more complete look at the combined AGC-A/D system could yield improved AGC algorithms and higher overall dynamic range.

Appendix A

A Two-step A/D Converter Simulation Model

In Chapter 2, the topology for the two-step flash A/D converter was presented (Figure 2.13). The two-step converter allows high conversion rates with less complexity than fully parallel flash converters. However, the topology of the converter causes the differential nonlinearities (DNL) to be repetitive throughout the conversion range, which give rise to strong spurious outputs. The primary sources of error in the two-step A/D are DNL and INL errors in the constituent A/D converters, DNL, INL, and settling errors in the DAC, and gain errors in the fixed gain amplifier.

To simulate the effect of repetitive threshold errors, we use the simple Matlab model shown in Figure A.1. The first quantizer models the combination of the first A/D and the D/A, since the output of the quantizer is a floating point number with b1 bits of precision. Each of the quantizers has a full-scale range of ± 1, thus the inputs are effectively limited to ± 1. The interstage gain is nominally 2^{b1} to scale the residual of the first conversion to the full scale range. Two sources of error are modeled by the factors α and β. The factor α models a gain error from the D/A, while the factor β models the gain error of the interstage amplifier. To provide the same errors (relative to an LSB) when the number of bits is varied, we write the factors α and β as

$$\alpha = K_1 \cdot 2^{-(b1+b2)} \tag{A.1}$$

and

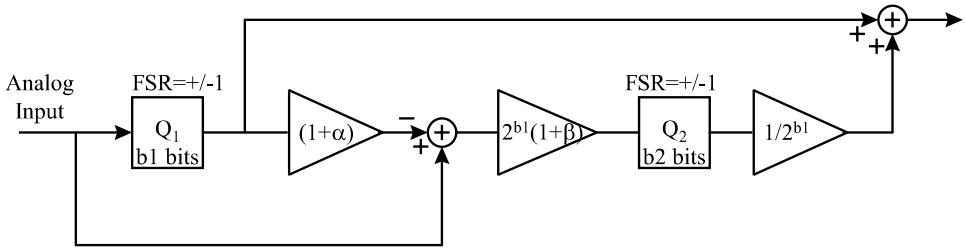


Figure A.1: Simulation model of two-step flash A/D with analog nonidealities

$$\beta = K_2 \cdot 2^{-b1} \tag{A.2}$$

where K_1 and K_2 are constants which affect the level of nonlinearity and may be chosen to match a given converter's characteristics. These gain errors are expressed in this way because the factor α contributes to errors relative to the overall resolution (b1+b2) bits while the factor β is relative only to resolution of the first converter (b1 bits).

Figure A.2 shows an example of the error transfer characteristic created by the two-step converter model when the converter is composed of two 4 bit converters, with $K_1 = 0.1$ and $K_2 = 0.2$. The repetitive nature of the threshold errors is evident.

Since all of the elements of the model are memoryless, the model does not reflect the frequency dependency of the SFDR. Nor does the converter model the effect of error correction which is often found in two-step A/D's. However, the number of bits in the constituent converters and the factors K_1 and K_2 may be adjusted to mimic the performance of any converter whose DNL/INL characteristic or spurious output is known.

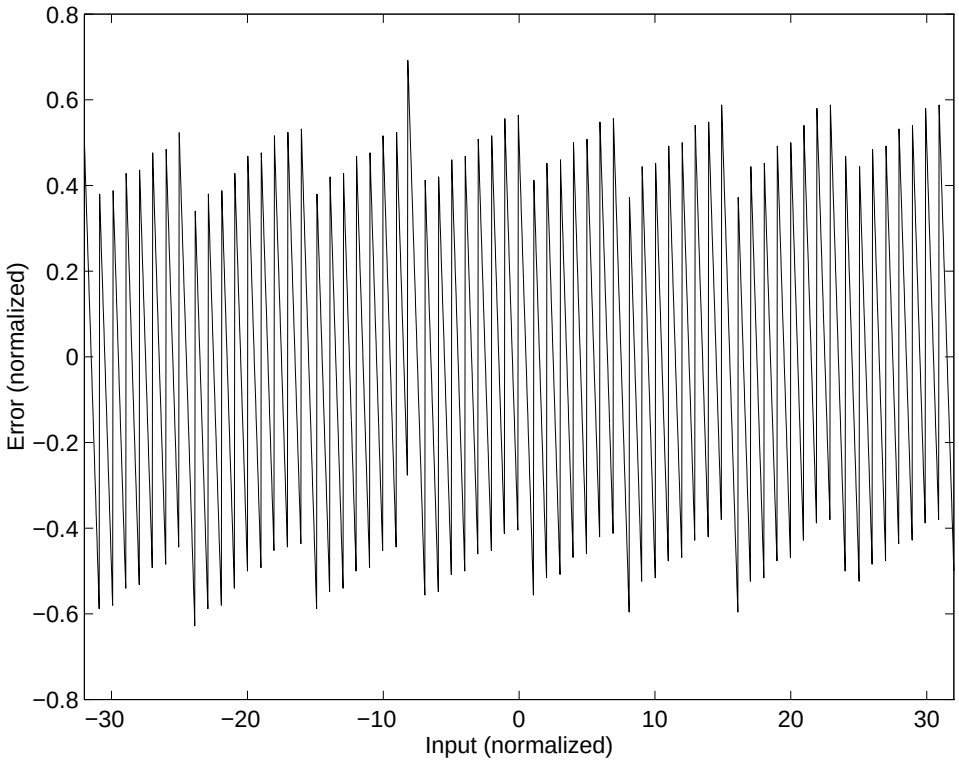


Figure A.2: Error transfer characteristic of the nonlinear two-step A/D with b1=b2=4

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Vita

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