Development of Low-power Wireless Sensor Nodes based on Assembled Nanowire Devices

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(ABSTRACT)

Networked wireless sensor systems have the potential to play a major role in critical applications including: environmental monitoring of chemical/biological attacks; condition-based maintenance of vehicles, ships and aircraft; real-time monitoring of civil infrastructure including roads, bridges etc.; security and surveillance for homeland defense systems; and battlefield surveillance and monitoring. Such wireless sensor networks can provide remote monitoring and control of operations of large-scale systems using low-power, low-cost, "throw-away" sensor nodes. This thesis focuses on two aspects of wireless sensor node development: (1) post-IC assembly of nanosensor devices onto prefabricated complementary-metal-oxide-semiconductor (CMOS) integrated circuits using a technique called dielectrophoretic (DEP) assembly; and (2) design of a low-power SiGe BiCMOS multi-band ultra-wideband (UWB) transmitter for wireless communications with other nodes and/or a central control unit in a wireless sensor network.

For the first part of this work, a DEP assembly test chip was designed and fabricated using the five-metal core CMOS platform technology of Motorola's HiP6W low-voltage 0.18μm Si/SiGe BiCMOS process. The CMOS chip size was 2.5mm $\times$ 2.5 mm. The required AC signal for assembling nanowires is provided to the bottom electrodes defined in the Metal 4 (M4) layer of the IC process. This signal is then capacitively coupled to the top/assembly electrodes defined in the top metal (M5) layer that is also interconnected to appropriate readout circuitry. The placement and alignment of the nanowires on the top electrodes are defined by dielectrophoretic forces that act on the nanowires. For proof of concept purposes, metallic rhodium nanowires (length = 5μm and diameter = 250 nm) were used in this thesis to demonstrate assembly onto the prefabricated CMOS chip. The rhodium nanowires were manufactured using a nanotemplated electroplating technique. In general, the DEP assembly technique can be used to manipulate a wider range of nanoscale devices (nanowire sensors, nanotubes, etc.), allowing their individual assembly onto

prefabricated CMOS chips and can be extended to integrate diverse functionalized nanosensors with sensor readout, data conversion and data communication functionalities in a single-chip environment. In addition, this technique provides a highly-manufacturable platform for the development of multifunctional wireless sensor nodes based on assembled nano-sensor devices.

The resistances of the assembled nanowires were measured to be on the order of 110 Ω consistent with prior prototype results. Several issues involved in achieving successful assembly of nanowires and good electrical continuity between the nanowires and metal layers of IC processes are addressed in this thesis. The importance of chemical/mechanical planarization (CMP) technique in modern IC processes and considerations for electrical isolation of readout circuit from the assembly sites are discussed.

For the second part of this work, a multi-band hopping ultrawideband transmitter was designed to operate in three different frequency bands namely, 4.8 GHz, 6.4 GHz and 8.0 GHz. As a part of this effort, this thesis includes the design of a CMOS phase/frequency detector (PFD), a CMOS pseudo-random code generator and an on-chip passive loop filter, which were designed for the multi-band PLL frequency synthesizer. The CMOS PFD provided phase tracking over a range of -2π to $+2\pi$ radians. The on-chip passive loop filter was designed for a 62° phase margin, 250 μA-charge pump output current and 4 MHz-PLL loop-bandwidth. The CMOS pseudorandom code generator provided a two-bit output that helped switch the frequency bands of the UWB transmitter. With all these components, along with a BiCMOS VCO, a CMOS charge pump and a CMOS frequency divider, the simulated PLL frequency synthesizer locked within a relatively short time of 700ns in all three design frequency bands. The die area for the multi-band UWB transmitter as laid out was 1.5 mm × 1.0 mm.

Future work proposed by this thesis includes sequential assembly of diverse functionalized gas/chemical nanosensor elements into arrays in order to realize highly sensitive "electronic noses". With integration of such diverse functionalized nanoscale sensors with low-power read-out and data communication system, a versatile and commercially viable low-power wireless sensor system can be realized.

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Chapter 1

Introduction

1.1 Background

A sensor is a device that responds to a physical (or chemical) stimulus (such as heat, light, sound, pressure, etc.) and provides a resulting impulse for measurement and control operation. It converts an input non-electrical signal into an electrical signal (or any other type of signal) which identifies and quantifies the input stimulus. For example, a photodetector (consisting of photodiode or phototransistor) conducts current that is proportional to the illuminance of the light incident on it, or a chemical/gas sensor provides electrical response that is proportional the type and concentration of gas/chemical it is exposed to. Some other types of sensors include acoustic (wave velocity, wave amplitude) sensors, thermal (temperature, thermal conductivity) sensors, radiation sensors and mechanical (force, stress, mass) sensors, etc. [1].

The rising demand for automation, security and control of the environment has led to the integration of some of the above-mentioned sensors with electronic circuits that provide novel signal processing and data communication capabilities [2]. Tremendous advances in silicon microelectronics have resulted in the ability to integrate low-cost and low-power electronic circuitry with on-chip sensors on a single silicon chip. These integrated sensor systems consists of a sensor unit, a sensor readout unit, a data conversion unit and a data communication unit. The applications of such integrated

sensor systems have diversified from military, industrial and environmental systems into commercial mass markets like automotive and smart-home systems [3]. This chapter first discusses various integrated sensors and microsystems that have already been demonstrated commercially. This chapter then discusses the applications of integrated sensors in wireless sensor networks. Finally, a thesis overview is presented which also explains the concept proposed in this work in detail.

1.2 Integrated microsystems

Recently, there has been tremendous interest in developing integrated microsystems that include on-chip sensors or actuators, analog readout/control electronics and suitable data communication circuitry [4]. Integrated microsystems have also been enabled in part due to the availability of microelectromechanical systems (MEMS) technologies. MEMS (also called micromachines) combine electrical and mechanical functionalities in a single structure at micro-scale dimensions. MEMS-based sensors and actuators have found application in virtually every sector of industry including automotive, telecommunications, aerospace, data storage and biotechnology. H. Fujita [5] gives a detailed account of the history of MEMS that dates back to the mid-1980s. Progress in MEMS has been realized through the development of fabrication techniques such as bulk and surface micromachining, high aspect ratio plating, wafer bonding, etc. [6]. The major advantage of MEMS-based systems is that they can be integrated with state-of-the-art silicon microelectronics on a very large scale. For example, a widely employed MEMS-based microsystem is an automobile crash-detection device that combines silicon micromachined accelerometers with complementary metal-oxide-semiconductor (CMOS) readout and logic circuitry for triggering airbag deployment [Figure 1.1(a)]. These devices are now integral components in virtually all new automobiles sold. MEMS-based acceleration sensors now claim a 13% market share of the total sensor market [7]. During the last decade, it is estimated that US$55 million to $200 million was spent in Europe per year for MEMS research, of which, roughly half the funds were directed towards automotive applications [8]. The US government agencies including Defense Advanced Research Projects Agency (DARPA) and National Science Foundation have been investing about US$ 30-35 million a year for the past few years in various MEMS-based

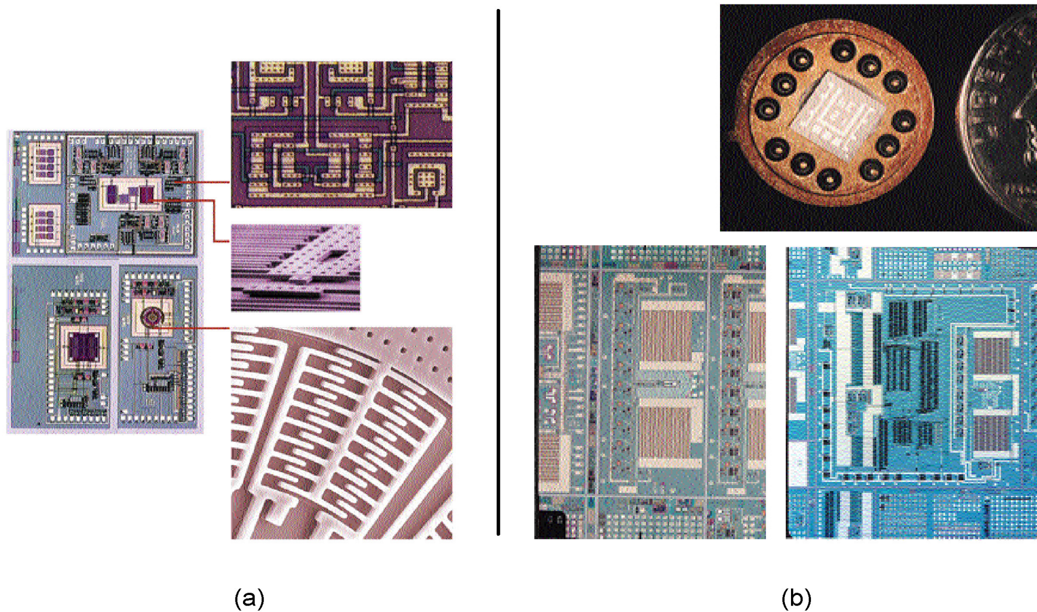


Figure 1.1: Chips that can sense, think, act and communicate — developed by Sandia National Laboratories (from [4].) (a) Integrated accelerometer; (b) Integrated hydrogen microsensor with analog electronics and communication circuitry.

research projects.

Another example of an integrated MEMS microsystem is the digital micromirror device (DMD) used for projection displays (Figure 1.2). The DMD, invented by L. J. Hornbeck of Texas Instruments Inc., has an array of more than 400000 movable mirrors (each roughly 16μm on a side), on a die of size approximately 2.3 cm^2 [9]. Each micromirror in the DMD essentially sits above a CMOS static random access memory (static RAM) cell. The mechanical tilt of each mirror is controlled by electrostatic forces arising based on the data stored in the corresponding memory cell. The motion of the mirrors in response to the stored data modulates the light that is incident on the surface of the mirror from a light source. Light reflected from these mirrors passes through a series of projection lenses to create high-fidelity images on a large screen. The micromirror arrays are fabricated with high yield after the static RAM circuitry has been completed through standard CMOS processing steps at very low-cost. The DMDs have already virtually replaced LCDs in PC projection units and are competing to replace the present day projection TVs [10].

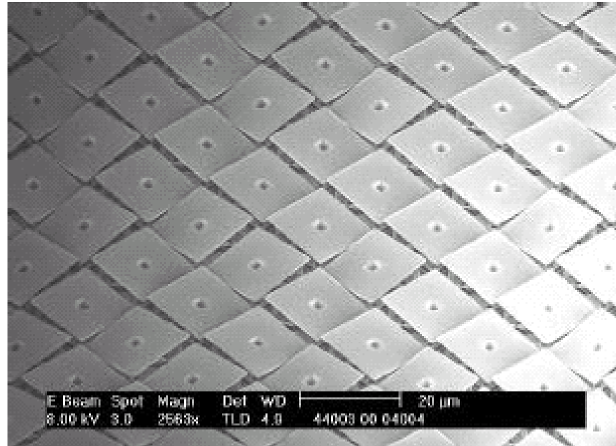


Figure 1.2: SEM picture of a fabricated DMD (from [11].)

Chemical microsensors such as hydrogen microsensors have also been integrated with CMOS electronic circuits as shown in Figure 1.1 (b). The hydrogen microsensor has integrated sensors, heater, thermometer and analog circuitry to measure the concentration of hydrogen in an environment from 1 part per million (ppm) to 100 percent. This approach has helped reduce the manufacturing cost of precision hydrogen sensors from several hundred dollars to about one dollar each. Given this tremendous cost effectiveness, integrated microsystems have been the target of increased research and development.

The "Electronic nose" (Figure 1.3) is yet another type integrated microsystem that integrates chemical/gas sensors on a chip with (CMOS) readout electronics. Such microsystems may have several different chemical/gas sensing mechanisms namely piezoelectric, capacitive, and chemoresistive integrated on the same chip [12] [13]. The piezoelectric[1] sensor in an electronic nose consists of a small polymer-coated miniature quartz crystal microbalance (QCM) connected to metal electrodes. The cantilever beam/QCM device resonates at a characteristic frequency (10-30 MHz) when excited by an externally applied oscillating signal. The polymer detects the presence various chemicals based on the distinctive molecular weight of each compound it is exposed to. When a chemicals get adsorbed onto the surface of the polymer, the mass on the beam increases. By mechanical principle, the resonant

[1] The term *piezoelectric* means the property by which mechanical stress is generated due to an externally applied voltage signal.

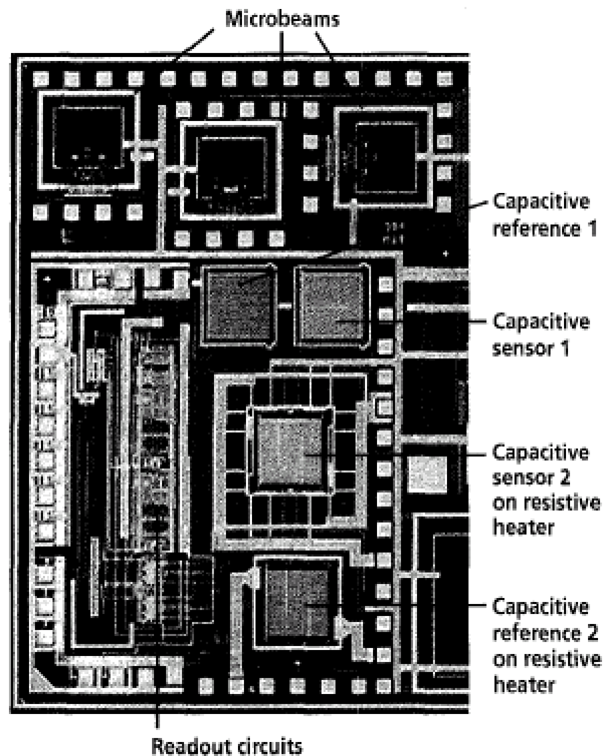


Figure 1.3: Chip micrograph of a fabricated electronic nose in silicon technology. Sensors and readout circuits are integrated on the same chip (from [12].)

frequency of microbeam decreases when a mass is added to it. The shift in resonant frequency depends on the molecular weight of each compound in the chemical that it gets exposed to. Thus, information on the type of chemical detected can be obtained by measuring the shift in resonant frequency.

Capacitive gas/chemical microsensors are commonly implemented in electronic noses. Such sensors are basically capacitors with a polymer layer whose dielectric constant changes as it absorbs gas molecules. The sensing capacitor operates in tandem with a polymer-free reference capacitor, which has the same capacitance as the polymer-coated capacitor before exposure to contaminants. The changes in capacitance are detected by appropriate CMOS readout electronics.

Conducting polymer sensors, or chemiresistive sensors, are also widely implemented in electronic noses. Here, the active material is a conducting polymer whose conductivity (or resistivity) changes as the sensor is exposed to various types of chemicals.

The changes in resistance that depend on the type chemical absorbed by the polymer are detected by a straightforward electronic interface.

A major application for such sensor microsystems is their deployment in wireless sensor networks. Among the major challenges in developing a robust wireless sensor networks is the integration of multifunctional sensors capable of measuring different parameters of interest and a suitable multiple-access radio architecture to transmit data at low-data rates with very low power consumption [14]. The next section describes wireless sensor networks and their applications, and the potential challenges to be met in realizing these networks.

1.3 Wireless sensor networks

A sensor network is formed by multiple sensor nodes performing control and monitoring operations independent of each other, and communicating data between each other (peer to peer) and/or with a central control unit or base station. These sensor nodes enable continuous sensing, event detection, and event identification at low power [15]. Each node may have arrays of sensors measuring different parameters. Figure 1.4 shows a simple conceptual diagram of a wireless sensor network. If a significant event is sensed by a node in the network, it transmits the information to nearby sensor nodes, and/or to a control unit, and ultimately to remote users who store and analyze the received data. Necessary action can be taken locally and/or once the information reaches the control unit or remote users by identifying the specific sensor node that transmitted the information.

Wireless sensor networks have a large range of potential applications in commercial, industrial and military arenas [16], including:

- Condition-based maintenance of vehicles, aircraft, ships, industrial and power generation equipment, etc.;
- Real-time monitoring of the health of civil infrastructure such as roads, bridges, power plants etc.;
- Environmental monitoring for chemical/biological attacks;

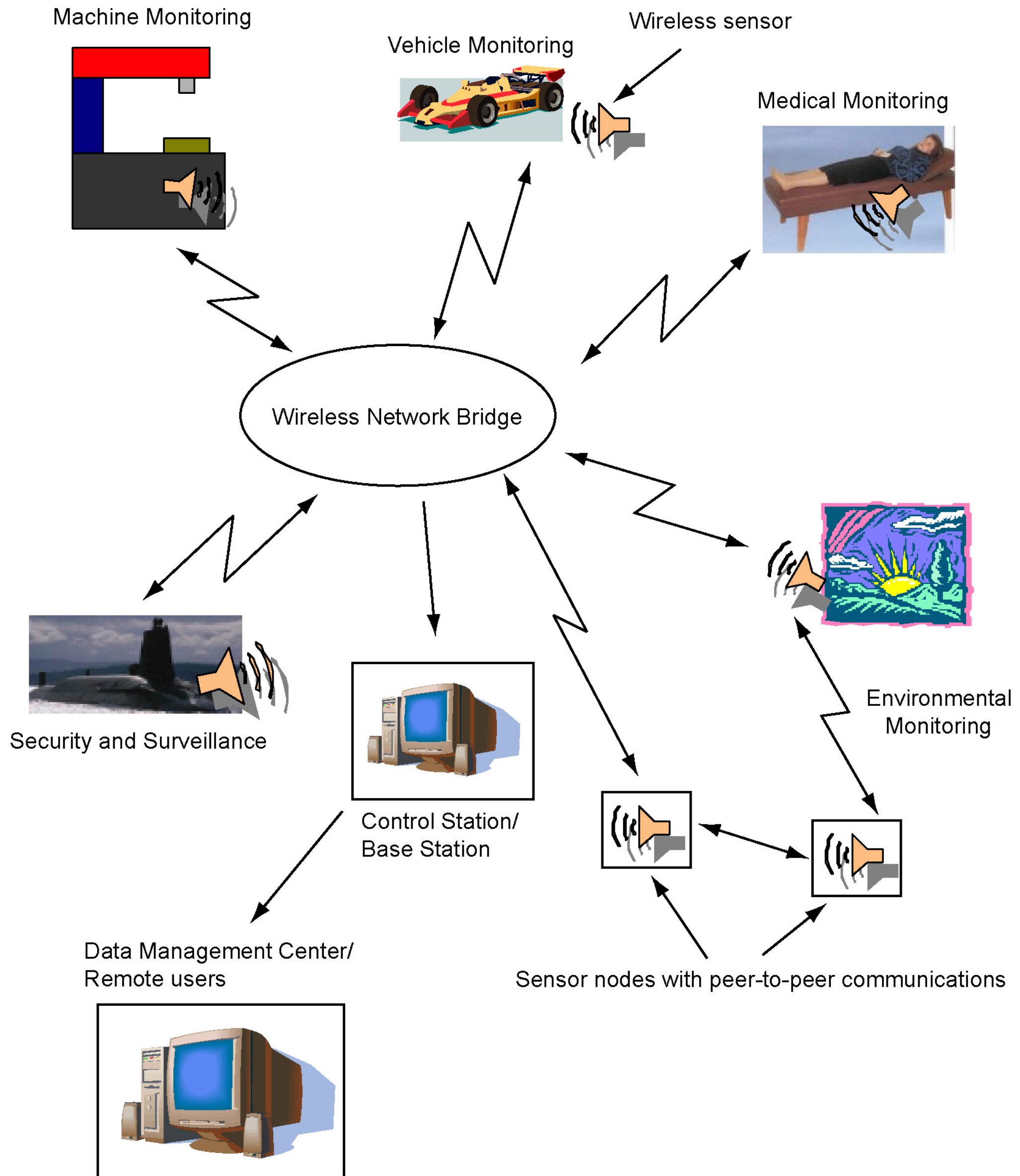


Figure 1.4: Conceptual diagram of a wireless sensor network (after [17]).

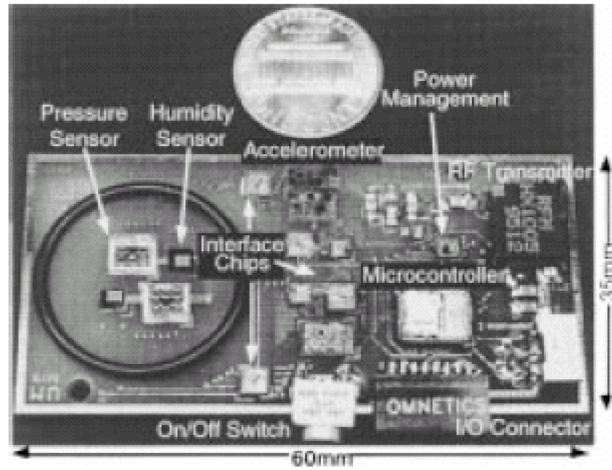
- Medical/health care systems connecting patients, medical staff and professionals for continuous care;
- Monitoring and controlling traffic systems, emergency services;
- Security and surveillance for homeland defense.

There have already been impressive developments in the area of integrated wireless sensor nodes. Some recent examples (Figure 1.5) include University of Michigan's "μclusters" containing pressure/humidity/temperature sensors for environmental monitoring purposes [18], "Smart-Dust" containing optical transceiver, photosensor and CMOS control chip with data conversion circuitry — developed by UC-Berkeley [19], UCLA/Rockwell Scientific Center's WINS node with thermal infrared detectors to detect source signals (seismic, acoustic and infrared etc.) in the presence of environmental noise [15].

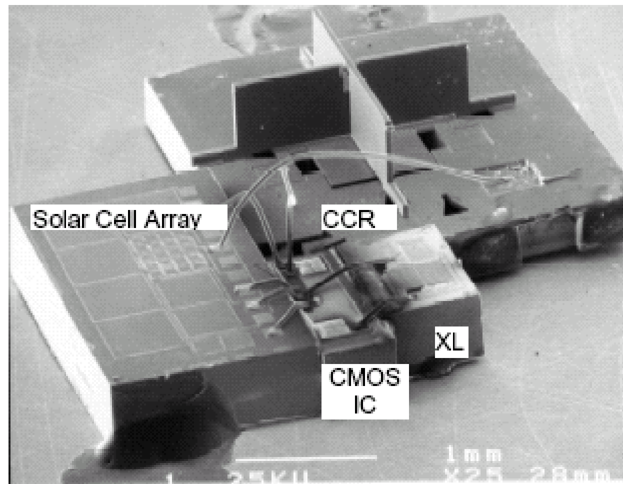
The next two sub-sections discuss the basic communications uplink architecture for wireless integrated sensor microsystems and the basic requirements/challenges to be met in realizing a complete system on a chip for wireless sensor network applications.

1.3.1 Wireless integrated sensor microsystem — On-chip architecture

Figure 1.6 shows the architecture of a basic integrated wireless sensor microsystem [21]. As mentioned above, the ultimate goal is the integration of all sensor node functions on a single chip. First, the sensor information is converted into a suitable electrical parameter by sensor readout circuitry. For example, in a chemiresistive sensor, the change in resistance of a chemically sensitive material can be converted to a voltage using Wheatstone bridge network or in MEMS accelerometers, the change in capacitance due to sensor deflection can be detected as a change in voltage using a capacitive bridge circuits and appropriate analog circuits. The output of the readout circuit is then typically converted to a digital signal using a low-power analog-to-digital (A/D) converter (ADC). Though there are many types of A/D converters such as flash, integrating, folding, pipelined, $\Sigma\Delta$, etc.; a major challenge is the development of a low-power data converter with good resolution and speed [22]. Then, the



(a)



(b)

Figure 1.5: (a) "μ-Cluster" with integrated sensors, readout electronics and RF transmitter on a single chip (from [18].) (b) SEM picture of prototype 16 mm^3 "Smart Dust" consisting of hybridly mounted optical transceiver, photosensor and associated CMOS control chip (from [20].)

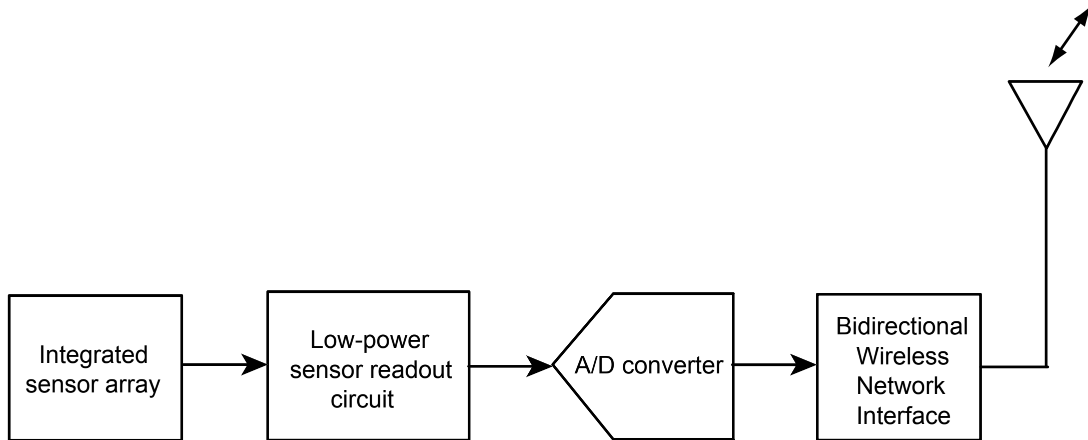


Figure 1.6: Architecture of wireless integrated sensor microsystem.

RF communication interface provides low-power bidirectional network access (transmit/receive) for short-range data communication. When a significant sensor event is detected by a node, it should awake the neighboring nodes to receive the transmission. Once the neighboring nodes receive the information, they should relay the data to other neighboring nodes and then finally to the control unit. In addition, to reduce battery power consumption, the network interface should be configured to operate only in the case of an event detection. The low-power transmitter design for wireless sensor network applications will be introduced in section 1.5.2.

The fundamental requirements for any distributed wireless sensor network can be summarized into two main categories as given below:

1. Requirements for sensor nodes:
    - Low cost sensor nodes and electronics — For on-chip sensor readout and data conversion electronics, modern CMOS/BiCMOS processes should be used to design the circuits targeting low cost. Modern CMOS IC processes also offer low-power consumption capabilities for implementing analog circuitry with high levels of integration [23].
    - Multi-functional sensor nodes — Arrays of diverse-funtionalized sensor elements can be incorporated [18] [21].
    - Sensor nodes should provide reconfigurable signal processing and should have local control and self-monitoring capabilities [24].

2. Requirements for RF communication system:

    - Low-power RF communication system to transmit/receive data at low data rate over short ranges [21].
    - Data communication should be as free as possible from interference and multipath fading — spread spectrum signalling using low-power frequency hopped implementations is desirable due to its interference rejection capability [21]. Data collisions are not a major issue in wireless sensor network applications because of their low-data rate requirements.
    - Multiple access data communication system for bidirectional peer-to-peer communication, etc.

A main aim of this thesis work is to leverage nanotechnology and ultra-wideband communications in the development of a novel platform for integrated wireless sensor microsystems that meet many, if not all, of the challenges described above. In Section 1.5, the proposed system architecture, which is the basis for this thesis work, is introduced. The next section will introduce the concept of integrated nanosystems based on nano-scale sensor devices that can assembled onto prefabricated CMOS circuits using a technique described in Chapter 2. Such integrated nanosystems can potentially replace some of the integrated microsensors discussed earlier in this chapter, providing multifunctional wireless sensor systems.

1.4 Nanotechnology and integrated nano-systems

Nanotechnology is a rapidly evolving field that involves the manipulation and characterization of materials and structures at nanometer-scale dimensions. Just a few years ago nanotechnology was being explored at a pure research/basic science level. Now, nanotechnology has made significant strides into the commercial arena [25]. Nanotechnology broadly includes areas such as Nano-electromechanical Systems (NEMS), Nanoelectronics, Nanobiotechnology, as well as integrated nanosystems which combine functional NEMS or nanosensor devices with silicon microelectronics to provide multiple functionalities using single silicon chip.

Research in nanotechnology has accelerated significantly since the invention of Nobel prize winning imaging techniques such as scanning tunneling microscopy (STM) and atomic force microscopy (AFM). These techniques kick-started the phenomenal growth of nanosystems and offered researchers a way to directly image at the atomic and molecular level. Nanoscale engineering now offers control and manipulative ability over individual atoms and molecules that determine physical, chemical and even biological material properties. For this main reason, the sensitivity of nanoscale sensors can be much greater than the microsensors and other MEMS-based sensors discussed earlier in Section 1.2. The advent of nanotechnology has opened up new possibilities for electronics, medical diagnostics, data storage and sensing systems. They offer potential cost-effective solutions for the development of highly sensitive and highly functional nano-scale sensor devices [26]. In addition, due to the incredibly small device dimensions, a large number of low-power-consuming and diverse-functionalized sensor arrays can be deployed.

Some examples of nanoscale sensor devices include NEMS-based cantilever sensors, chemiresistive sensors. Chemical sensors can be developed using highly precise nanoscale cantilevers which are sensitive to ultra-small masses and forces [27] [28]. These nano-scale cantilever sensors are more sensitive and compact than the microbeams in MEMS-based electronic noses described in Section 1.2. In addition, nanowire and carbon nanotube chemical sensors have also been developed with highly sensitive and selective detection capabilities [29] [30]. Development of other nano-scale sensors like capacitive sensors [31], chemiresistive sensors [32], tin-oxide based sensors [33] [34] have diversified the available sensing mechanisms. As mentioned above, nanoscale control of materials allows the realization of these nanosensor devices with tailored chemical, physical and/or electronic properties.

"Bottom-up" synthesis of nanostructures opens up one more avenue for the development of nanosensor devices. In the traditional "top-down" approach, desired structures are realized by selectively etching regions using lithographically defined wet or dry etching processes. On the other hand, in the "bottom-up" approach, individual atoms and molecules are directly manipulated or self-assembled in precisely defined locations based on the structure needed [25]. The "bottom-up" synthesis of nanostructures includes templated growth techniques such as DNA-templated nanowire growth [35], chemical or electrochemical growth [36] [37] and nanotemplated electro-

plating [38]. These growth techniques can be used to develop semiconducting and sensing nanowires as mentioned in [39]. Such sensing nanowires could be used for various sensing purposes including gas/chemical sensing.

However, the nanoscale sensing structures mentioned above are not useful in practical systems unless they act in conjunction with readout and signal processing circuits. The ability to manipulate the movement of individual functional nanostructures offers potential to integrate them with microelectronics. One promising technique is the *Dielectrophoretic assembly technique* [40]. *Dielectrophoresis* (DEP) is defined as the motion of uncharged, polarizable particles in a non-uniform electric field [41]. The dielectrophoretic forces result from the interaction of the electric field with a charge dipole induced in the particles (e.g. nanowires). This thesis demonstrates the use of this method for the integration of functional nanostructures with CMOS sensor readout and data communication circuits. Chapter 2 will provide a detailed discussion of the theory supporting the DEP technique and illustrates its compatibility with modern silicon IC processes. Given the ultra-sensitivity of nanoscale sensors, and the compatibility of dielectrophoretic assembly technique with IC processes, there is tremendous potential to integrate massive numbers of diverse sensors on a single chip, resulting in a low-cost multifunctional nanosensor node.

1.5 Thesis overview - Proposed system architecture

As discussed above, the primary components in a wireless integrated sensor microsystem are the sensing sub-system with readout and data conversion functions, and the data communication sub-system. A major challenge in developing wireless sensor nodes is realizing a low cost and low-power RF communications system. This section discusses these two sub-systems and presents proposed solutions that will be explored in this thesis.

1.5.1 Proposed sensing system

Tin oxide based gas sensors and nanowire growth techniques have been the subject of research and development for many years [33] [34]. As discussed above, by employing a "bottom-up" synthesis approach, tin oxide nanowires can be fabricated for high-sensitivity gas sensing purposes. In addition, there are various other sensing materials that could be developed and used to provide diverse functionalities to a sensing system. Nanotemplated electroplating is one growth technique that offers capabilities for growing different functional nanostructures. In this growth technique, high aspect ratio cylindrical nanostructures can be grown by using porous alumina membranes, with pores of diameters on the order of few tens of nanometers to greater than 200nm, as templates [38] [39]. Such membranes can be produced through anodization of aluminum in various acids as described by Masuda et. al. [42]. In ambient conditions aluminum surfaces are naturally covered by a thin alumina layer. Anodization, which is performed by applying an electrical current to a part of aluminum in an acid electrolyte leads to a thick alumina layer with a homogenous pores. The homogeneity of the pores depend on the applied electric field strength and the chosen electrolyte.

As an example, the process flow of this technique is illustrated in Figure 1.7 for the growth of nanostructures with central functional segment of tin-oxide (SnO_2) and metal extremities of gold (Au). A thin film of silver (Ag) is evaporated on one side of the membrane before electrodeposition of a thick film of Ag. The pores of the membrane are then filled/electroplated with thin layer of Ag. The membrane is then transferred to an ultrasonic bath where Au, Sn are electroplated into the pores followed by another layer of Au. This bath increases the diffusion rate of plating solution and minimizes surface adsorbants [39]. The pores are now filled with cylindrical functional nanostructures composed of Au/Sn/Au. Finally, the electroplated layer of Ag and the alumina membrane are dissolved in nitric acid and sodium hydroxide respectively and the released nanostructures are rinsed by centrifugation. These nanostructures are then suspended in liquid media such as Isopropanol. Further, tin-oxide functional segment can be obtained by oxidation of Sn segment prior or after release from the membrane. A scanning electron microscope (SEM) picture of a Au/SnO_2/Au nanostructure fabricated using nanotemplated growth technique is shown in the Figure 1.8. This nanostructure development technique can also be

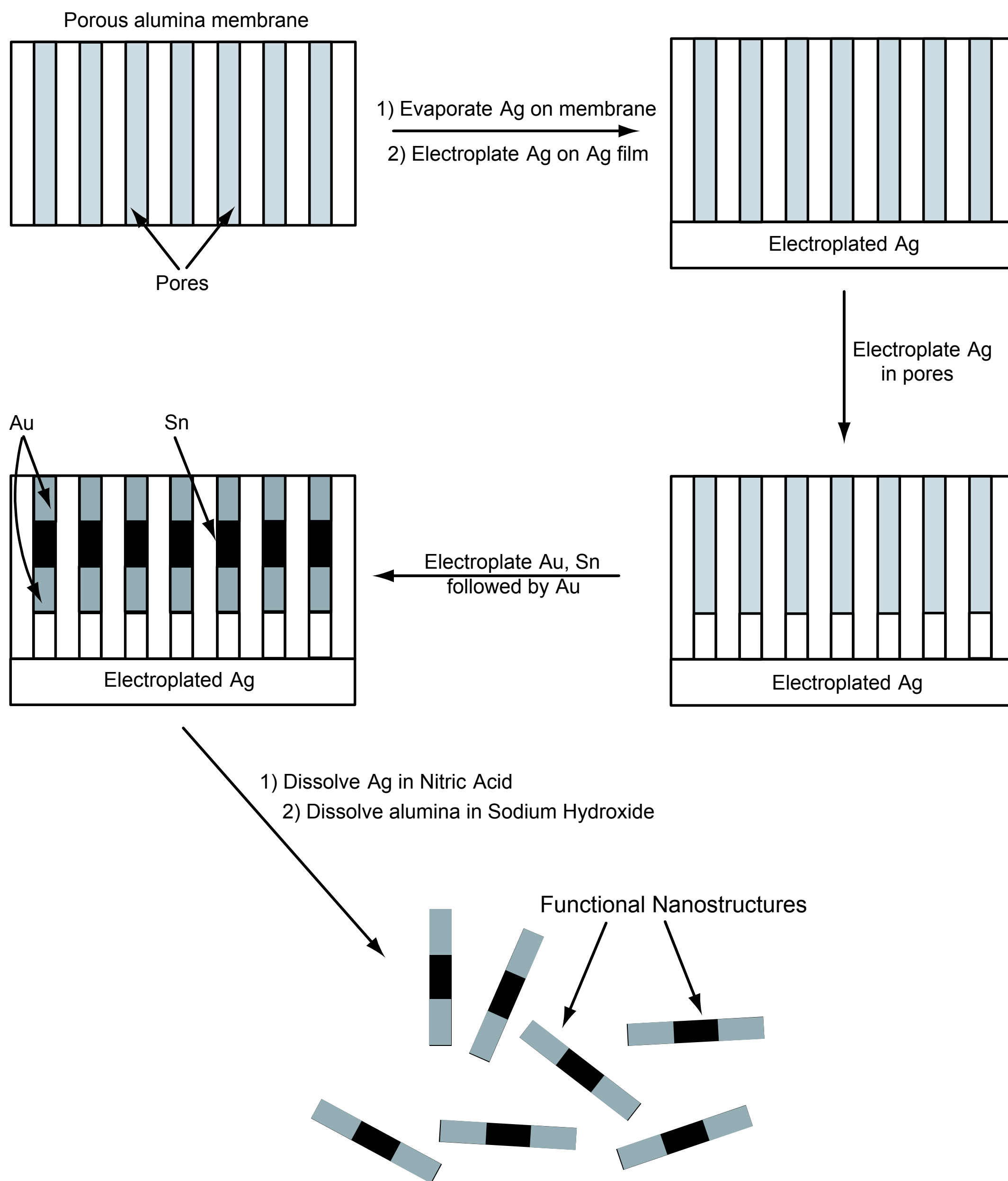


Figure 1.7: Illustration of process flow of nanotemplated growth technique (after [38]).

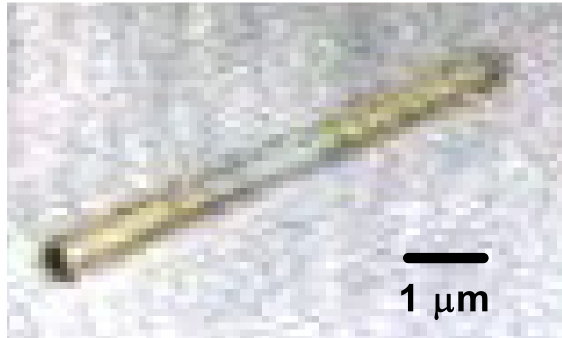


Figure 1.8: A SEM image of a $Au/SnO_2/Au$ nanostructure fabricated using nanotemplated growth technique (from [39].)

used to develop different types of functional nanosensors based on nanowires, carbon nanotubes, etc. [43].

Integration of different nano-scale sensing wires with CMOS circuitry is enabled using the dielectrophoretic assembly technique. Figure 1.9 shows a conceptual illustration of this process. Modern CMOS IC technology can be used to design and fabricate the sensor readout and data conversion circuits. The requisite assembly electrodes can also be fabricated on the same chip using various available interconnect layers. These assembly electrodes can be designed such that the nanosensors, once assembled on-chip, will interface with the readout and data conversion electronics. Based on the parameter being sensed, the readout circuit can be designed appropriately to form the sensing sub-system of a wireless sensor microsystem.

1.5.2 Data communication system

As discussed in the literature, providing low-power, multiple-access data communication systems with low to moderate data rates over short ranges for wireless sensor network applications is a major challenge [21]. Spread spectrum communication systems, namely Direct Sequence spread spectrum (DS-SS) and Frequency-Hopped spread spectrum (FH-SS), are widely used for providing multiple-access capabilities [44]. Other types of spread spectrum communication systems include a Time-hopped spread spectrum system and a hybrid or combination of above mentioned types (for example, DS/FH multiple access). A DS-SS system spreads the information spec-

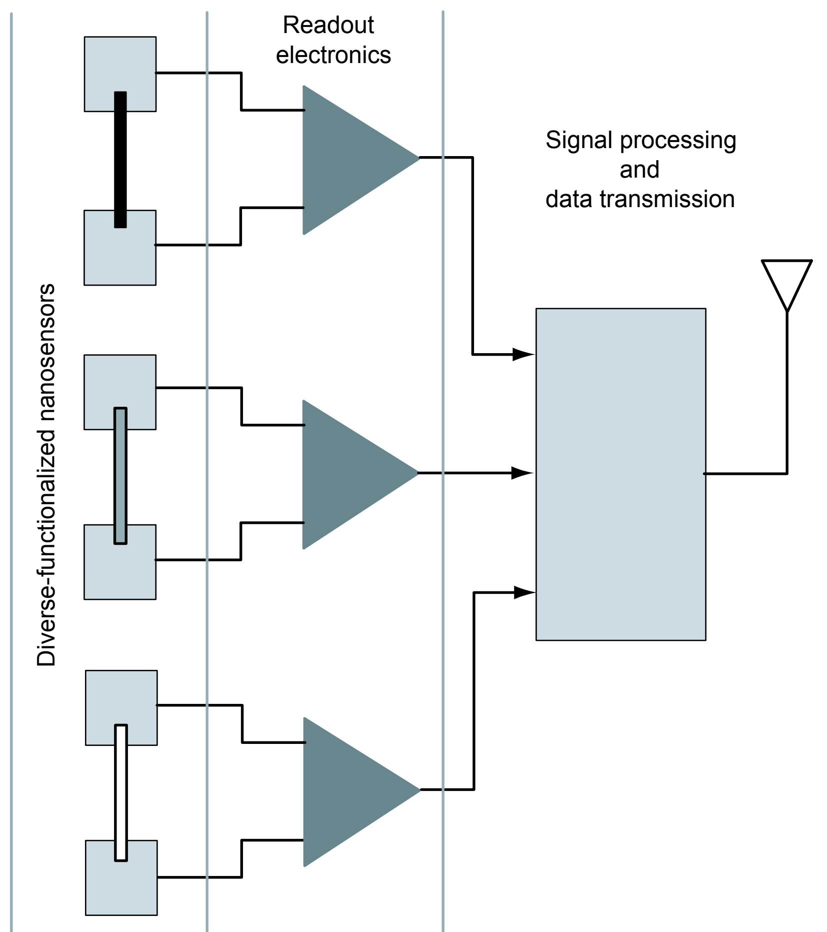


Figure 1.9: Conceptual illustration of a wireless sensor system using nanowires as sensors.

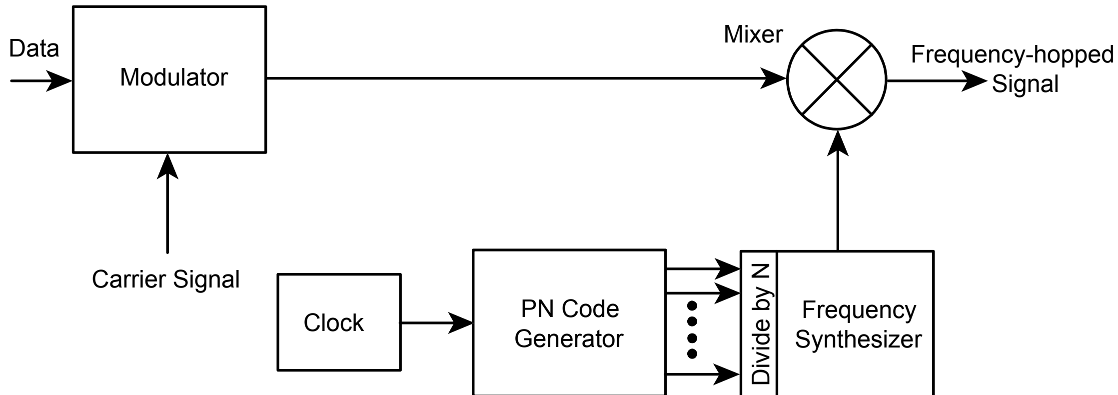


Figure 1.10: Block diagram of a Frequency-hopped transmitter system (after [47]).

trum by multiplying the baseband data pulses with a pseudo-noise (PN) sequence that is produced by a PN code generator. On the other hand, a FH-SS (or multiband-hopped) system employs a periodic change of carrier frequency — a frequency hopping signal is a sequence of modulated data bursts with time-varying, pseudorandom carrier frequencies [45]. The basic architecture of FH-SS transmitter is shown in the Figure 1.10. RF transmitters with a frequency-hopping spread spectrum (FH-SS) communication scheme are a possible solution for wireless sensor networks, as they can operate at low power and are also sufficiently free from interference and multipath fading [46]. In addition, as mentioned in Section 1.3.1, data collisions are not a major issue in wireless sensor network applications because of their low-data rate requirements. FH-SS schemes also allow multiple sensor nodes to share a given frequency bandwidth making it an appropriate scheme for wireless sensor networks. FH-SS are preferred over DS-SS in this applications because it offers flexibility in choosing modulation schemes and require less complex associated circuitry allowing low-power dissipation [47].

An emerging wireless technology that potentially allows interference free data communication is Ultra-wideband (UWB). Ultra-wideband wireless communication has made significant strides over the last few years with the FCC allocating the frequency range from 3.1 GHz to 10.6 GHz for unlicensed use of UWB devices in 2002. Some of the properties of UWB data communication systems are low cost, low power, relaxed phase noise requirements and secure, interference free data transmission [48]. In addition, an important characteristic of UWB signals that may be useful for sensor

network applications is their ability to propagate through obstructions more readily than conventional narrowband signals [49]. Finally, it has also been demonstrated using propagation measurements that certain UWB signals do not suffer from multipath fading even in dense environments [50]. It has been reported in the literature that UWB devices improve network routing strategies because of their ability to precisely determine the position of a single user in a large cluster of users [51]. Consequently, in case of an significant event detected by a sensor node, accurate sensor node position information can be obtained with better control over emitted power using a UWB-based system [52]. A robust data communication system for wireless sensor networks can be developed if frequency-hopping or a multi-band scheme can be incorporated in an ultra-wideband transmitter. Therefore, this thesis work also involves the development of a prototype multi-band ultra-wideband transmitter that allows multiple users share a given bandwidth.

UWB signalling schemes are based on the generation of relatively short pulses in the nanosecond range. As per FCC regulations, an UWB signal should occupy a minimum bandwidth of 500 MHz within the frequency range of 3.1 to 10.6 GHz while meeting spectral mask requirements. The emission limits should be less than -41.3 dBm/MHz [53] . Figure 1.11 shows a pictorial representation of the frequency spectrum available for unlicensed operation of UWB devices.

While sensor networks typically do not require high bandwidth data transmission, it is critical that their transmissions are not plagued by interference and multipath fading. Therefore, the operational efficiency of sensor networks in obstructed environments may be improved with the use of UWB data communication systems.

1.6 Thesis objectives and overview

1.6.1 Sensing system

The first objective of this thesis is to demonstrate that nanowires can be assembled on prefabricated silicon VLSI circuits using the dielectrophoretic assembly technique. Chapter 2 provides the background theory of the dielectrophoretic assembly technique. Chapter 3 focuses on the dielectrophoretic integration of nanowires onto a

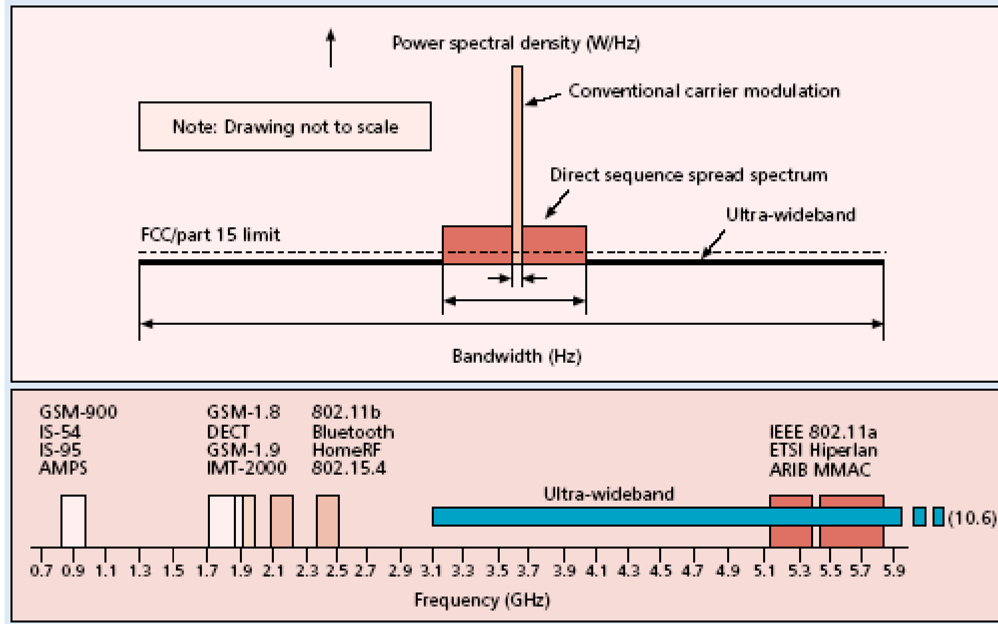


Figure 1.11: Top: Bandwidth comparison of different types of wireless systems. Bottom: UWB spectrum overlay (from [48].)

custom CMOS test chip. As a proof of concept, metallic rhodium nanowires are initially used for the assembly procedure. A detailed explanation of experiments that were performed and subsequent results achieved are given in Chapter 4. Chapter 6 presents conclusions and suggests future improvements on the technology developed in this thesis.

1.6.2 Data communication system

The second objective of this thesis is the development of a suitable design for a multiband ultra-wideband transmitter. The proposed transmitter is based on a PLL frequency synthesizer with a negative-G_M LC voltage controlled oscillator (VCO). The prototype version is designed to operate with three different center frequencies: 4.8 GHz, 6.4 GHz and 8.0 GHz. The architecture and simulated results of the transmitter are discussed in Chapter 5.

1.6.3 IC technology

All the circuits implemented in this thesis are designed using Motorola's HiP6WRF low-voltage $0.18\mu m$ Si/SiGe BiCMOS process. The core IC process is a five-metal process that provides low-threshold-voltage CMOS devices, SiGe hetero-junction bipolar transistors (HBTs), and embedded RF passives with higher performance than those in typical CMOS processes [54]. This process provides different choices in the supply voltage level for active devices, with the lowest voltage level being 1.8 volts.

Chapter 2

Dielectrophoretic Assembly of Nanowires

This chapter provides the background on the dielectrophoretic nanowire assembly technology employed in this thesis. A detailed theoretical explanation of dielectrophoresis and a discussion of prior work on nanowire assembly based on this theory is presented. The term "Dielectrophoresis" was coined by H. A. Pohl (1951), who performed important early electric-field experiments with small plastic particles suspended in insulating dielectric liquids [55]. Pohl discovered that the particles would move in response to the application of non-uniform AC or DC electric fields. The term *dielectrophoresis* comes from a combination of *dielectric*, which means a medium or material in which the constitutive dipoles respond under the influence of electric fields, and the Greek word "phoresis" meaning force.

2.1 Dielectrophoresis – Theory

Dielectrophoresis (DEP) is the motion of an *uncharged* body in a non-uniform electric field due to polarization effects [41]. This is in contrast to *electrophoresis*, whereby a *charged* body experiences motion in an electric field (uniform or non-uniform). In this section, electric-field-induced polarization effects are discussed, serving as the basis for the theory of DEP and the derivation of the classical expression for DEP force.

The discussion focuses on uncharged neutral particles rather than charged particles as this thesis is concerned with the behavior of uncharged polarizable particles in a dielectric medium. Polar particles have permanent positive and negative charges forming a permanent dipole [56]. In a dielectric medium, these dipoles are normally oriented in a random fashion and an external applied electric field results in alignment with the field. On the other hand, non-polar particles do not inherently have a charge dipole unless an external electric field is applied. In this case, the particles become polarized after application of an electric field, i.e. positive and negative charges on the particle redistribute in opposite directions and produce an effective overall dipole which is aligned with the electric field. In both cases, the *dipole moment* is given by:

$$\overline{p} = q\overline{d} \tag{2.1}$$

where, q is the magnitude of one of the two bound charges comprising the dipole in coulombs, and $\overline{d}$ is the vector from the negative to the positive charges in meters. A parameter called polarizability, α, dependent on the dipole moment of the particle can also be defined as:

$$\alpha = \frac{p}{vE} \tag{2.2}$$

or alternatively,

$$p = \alpha \cdot v \cdot E \tag{2.3}$$

where, v is the volume of the particle and E is the applied electric field.

Considering an infinitesimal dipole in a nonuniform electric field (Figure 2.1), equations for the force and torque experienced by the dipole can be derived. If the dipole consists of two equal and opposite charges $+q$ and $-q$ located $\overline{d}$ apart in a nonuniform electric field of strength $\overline{E}$, the force experienced by the dipole will be a non-zero net force since each charge will experience different values of vector field $\overline{E}$ since they are located at different positions in the field. Performing a sum of the forces on the particle, the net force $\overline{F}$ can be given as

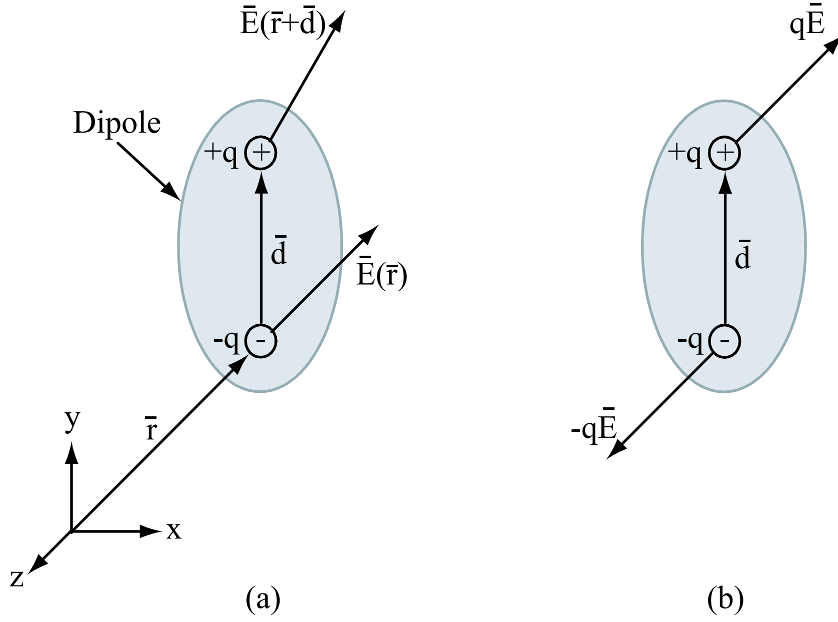


Figure 2.1: Representation of (a) force and (b) torque on an infinitesimal dipole induced by an electric field (after [55]).

$$\overline{F} = q\overline{E}(\overline{r} + \overline{d}) - q\overline{E}(\overline{r}) \tag{2.4}$$

where $\overline{r}$ is the position vector of $-q$. As shown in [55], when $|\overline{d}|$ is small compared to the characteristic dimension of the electric field nonuniformity, equation 2.4 can be simplified using a vector Taylor series expansion of $\overline{E}$ about position $\overline{r}$. Neglecting the higher order terms (d^2, d^3, and so forth) of the expansion, the expression for the force, $\overline{F}$ becomes

$$F = q\overline{d} \cdot \nabla\overline{E} \tag{2.5}$$

As mentioned in [55], If the limit as $|\overline{d}| \to 0$ is taken in such a way that equation 2.1 remains finite, then the final expression for the force on an infinitesimal dipole can be expressed as

$$\overline{F}_{dipole} = \overline{p} \cdot \nabla \overline{E} \tag{2.6}$$

From the above expression it can be observed that the force on a dipole in an electric field is dependent on the *gradient* ($\nabla \overline{E}$) of the electric field. This means that no net force is exerted on a dipole unless the external electric field is *nonuniform*. The force (dielectrophoretic force) due to a nonuniform electric field can result in two types of particle behaviors, *paraelectric* and *apoelectric*, depending on whether the body is neutral or polar. The paraelectric response is usually seen in neutral bodies which become polarized in a nonuniform electric field. The nonuniform field induces a dipole and imposes a net force on the particle towards the region of higher field intensity or electric flux density, defined as number of field lines per square meter and given by $D = \epsilon E$, where ϵ is the dielectric constant of the medium. For this net dielectrophoretic force to arise, the two equally displaced charge distributions of the neutral body should lie in regions of different field strength.

The torque experienced by a dipole due to the externally applied nonuniform electric field can also be derived based on Figure 2.1(b). Assume that the net force couple acts about the center of the dipole. Therefore, the torque is given by:

$$\overline{T} = \frac{\overline{d}}{2} \times q\overline{E} + \frac{-\overline{d}}{2} \times (-q\overline{E}) \tag{2.7}$$

which simplifies to,

$$\overline{T} = q\overline{d} \times \overline{E}. \tag{2.8}$$

Substituting equation 2.1 the final expression for torque is:

$$\overline{T} = \overline{p} \times \overline{E} \tag{2.9}$$

Unlike the force experienced by a dipole (equation 2.6), the torque does *not* depend on the gradient of the electric field. Therefore, it can be concluded that an electric field, either uniform or nonuniform, will impose a torque on a dipole, but a net force can be exerted only in the presence of a nonuniform electric field.

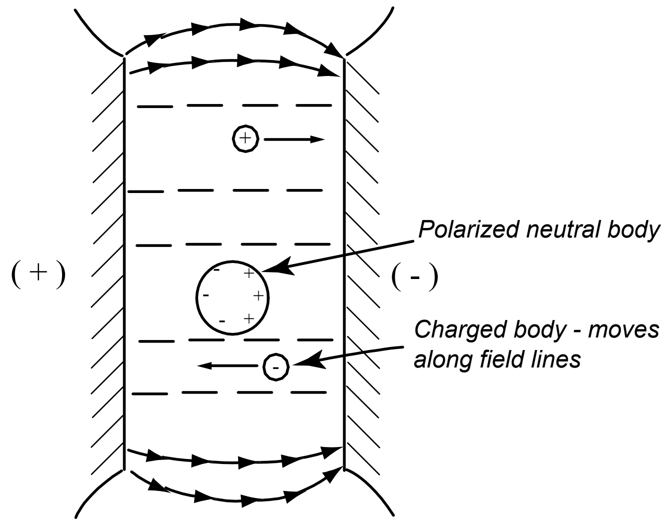
The next subsection discusses the behavior of neutral and charged bodies in response to different types of electric fields. The classical expression for dielectrophoretic force on a dielectric sphere suspended in a fluid dielectric medium will be derived in subsection 2.1.2 based on the above equations.

2.1.1 Physical behavior of neutral and charged bodies in response to applied electric field

Figure 2.2 illustrates the behavior of both neutral and charged bodies in uniform and nonuniform electric fields, respectively. In a uniform electric field, a charged particle moves along the field lines towards the electrode with a charge opposite to that of the particle [Figure 2.2(a)]. However, in the same field, a neutral body merely becomes polarized — negative charge accumulates closer to the positive electrode and positive charge accumulates closer to the negative electrode. This may result in a torque on the body, as explained by equation 2.9, but no net force will arise towards either electrode. However, if the neutral body is spherically symmetric or isotropic in its polarizability, it will not even experience a torque as would be the case with asymmetric or elongated bodies. As shown in the figure, a spherical body merely becomes polarized without any net movement.

In a non-uniform electric field, the behavior of a charged particle does not change — the particle will still move along the field lines as shown in Figure 2.2(b). The neutral body becomes polarized, as discussed above; however, because the field strengths experienced by the two regions of the body are unequal (due to the gradient in nonuniform fields — refer to equation 2.6), a net force is experienced by the body. This force tends to attract the body towards the region of higher flux density. As illustrated in the figure, the spherical polarized body moves towards the negative electrode where the field density is higher.

Dielectrophoresis is also observed in the presence of an alternating nonuniform electric field. Figure 2.3 shows the effect of an alternating non-uniform electric field on charged and neutral bodies. In this case, a charged body experiences a back-and-forth trajectory in the alternating electric field. On the other hand, the two charge regions on the polarized neutral body are equal in amount of charge, but experience a force proportional to the local field, resulting in a net movement towards the region of



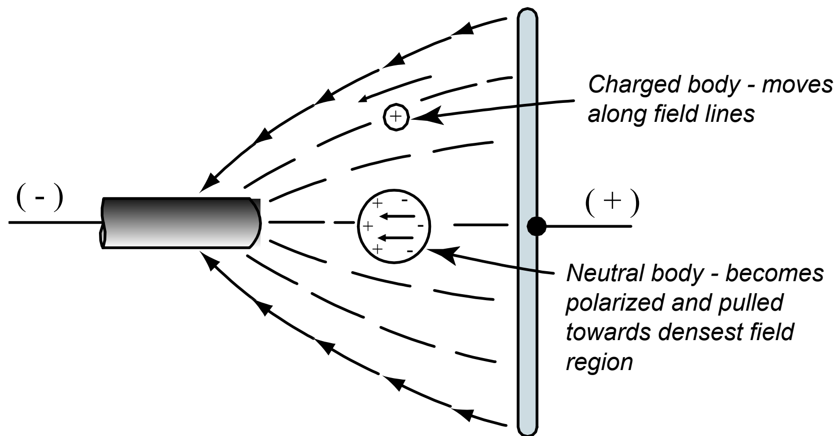
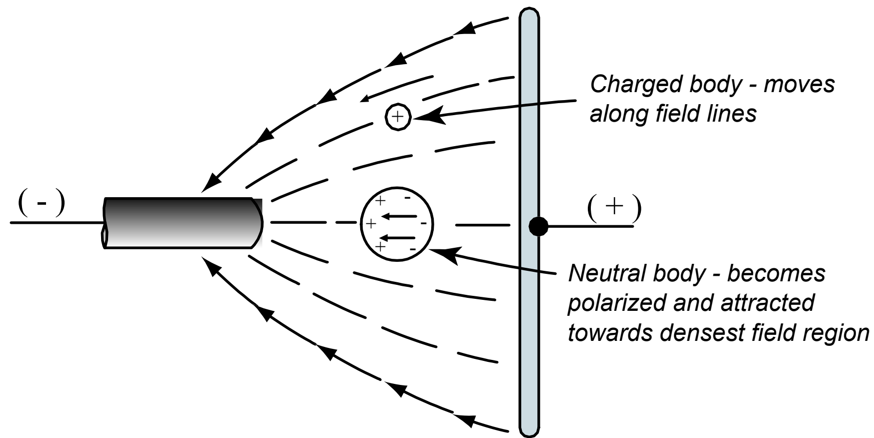
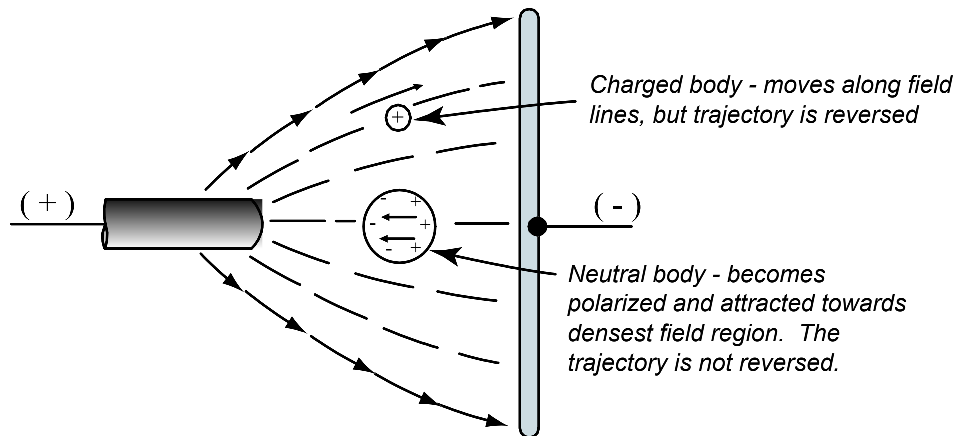


Figure 2.2: Behavior of charged and neutral particles in (a) uniform and (b) nonuniform electric fields (after [41]).



ALTERNATING NON-UNIFORM ELECTRIC FIELD (Positive cycle)



ALTERNATING NON-UNIFORM ELECTRIC FIELD (Negative cycle)

Figure 2.3: Behavior of a charged particle and a neutral particle in an alternating nonuniform electric field (after [41]).

higher field density. While the polarity of the electrodes alternate, the polarization of the neutral body changes accordingly. Thus, even when the field is alternating, the net force always moves the neutral body toward regions of denser field lines.

2.1.2 Dielectrophoretic Force

Dielectrophoretic force can be defined as the force exerted on uncharged dielectric particles with the application of a non-uniform AC or DC electric field by virtue of the particle's polarizability. Equation 2.6 gave a simple expression for force on a dipole that was induced by an externally applied electric field. This expression did not take into account several important factors such as the characteristics of the particle or the medium surrounding the particle. T. B. Jones [55] introduced an *effective moment method* for calculating electromechanical forces and torques exerted on uncharged particles by alternating electric fields. Considering a spherical particle, with permittivity of ϵ_p and a radius R, suspended in a dielectric medium of permittivity ϵ_m, the effective dipole moment due to an alternating nonuniform field E is given by

$$p_{eff} = 4\pi\epsilon_m K(\omega) R^3 E_{rms} \tag{2.10}$$

where E_{rms} is the RMS value of the applied electric field and $K(\omega)$ is known as the Clausius-Mossotti function that determines the frequency dependence of the DEP force. This function is expressed as $K(\omega) = \frac{\epsilon_p^* - \epsilon_m^*}{\epsilon_p^* + 2\epsilon_m^*}$, with complex permittivities, $\epsilon^* = \epsilon - j\sigma/\omega$, and where the factor σ is the respective electric conductivity. By comparing equations 2.3 and 2.10 it can be seen that the polarizability, α, of the spherical particle depends on the Clausius-Mossotti function. It can also be observed that polarizability of a neutral body depends on the complex permittivity of the medium the body is suspended in and that of the body itself. The factor R^3 in equation 2.10 comes from the volume of the sphere.

Using the expression for the effective moment and equation 2.6, the classical expression for DEP force on neutral polarizable particles is given as:

$$F_{DEP} = c\epsilon_0\epsilon_m v \, \mathrm{Re}(K(\omega))\nabla E_{rms}^2 \tag{2.11}$$

where, c is a constant based on the geometry of the particle ($= \frac{3}{2}$ for a sphere), ϵ_0 is the permittivity of free space and v is the volume of the particle ($\frac{4\pi R^3}{3}$ for a sphere).

Based on the expression derived above for the DEP force, the characteristics of dielectrophoretic force and the movement of a neutral body in a non-uniform electric field are discussed in [55] and are summarized as follows:

- Uncharged particles experience a DEP force only when the electric field is nonuniform, i.e., when there is a gradient electric field.
- DEP force is proportional to the permittivity of the medium in which the neutral body is suspended.
- F_{DEP} is independent of the polarity of electric field.
- DEP is observed with both DC and AC excitations.
- DEP force depends on the magnitude and sign of the Clausius-Mossotti function, K.

  — *Positive dielectrophoresis*: Particles are attracted towards regions of higher electric field intensity when $\mathrm{Re}(K(\omega)) > 0$, i.e., ($\epsilon_p > \epsilon_m$).

  — *Negative dielectrophoresis*: Particles are repelled from regions of higher electric field intensity when $\mathrm{Re}(K(\omega)) < 0$, i.e., ($\epsilon_p < \epsilon_m$).
- F_{DEP} is proportional to the volume of the particle (or neutral body).

2.2 Dielectrophoretic assembly technique

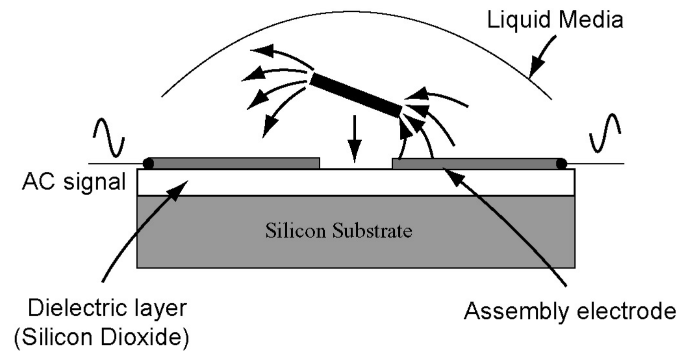
As discussed in chapter 1, templated growth techniques such as nanotemplated electroplating have been demonstrated for the fabrication of metallic and sensing nanowires.

However, such nanowires must be integrated with silicon readout and signal processing circuits to achieve desired functionalities. The ability to manipulate the position of individual functional nanostructures can facilitate their integration into modern CMOS VLSI circuits. In earlier work, including [57] and [58], Atomic Force Microscope (AFM) was used to manipulate and assemble nanotubes across contact pads. However, such techniques are fundamentally research methods and are not amenable to commercial mass-production.

One technique that can overcome manufacturability issues and offer a powerful, low-cost tool for the integration of individual nanostructures is dielectrophoretic assembly. This section provides a detailed discussion of prior efforts using the DEP assembly techniques to manipulate and assemble nanowires onto lithographically defined electrodes. The following section introduces strategies for CMOS VLSI integration leveraging the different metal layers available in modern IC processes to define the requisite electrodes for DEP nanowire assembly.

The DEP-based nanowire assembly technique was previously explored by Smith, *et al.* [40], where nano-scale metallic wires (such as gold) grown by nanotemplated electrodeposition were successfully assembled onto lithographically defined electrodes fabricated on a Si chip. Figures 2.4 and 2.5 illustrate the two approaches employed by Smith *et al.* In the first approach shown in Figure 2.4 (a), AC assembly signal is directly applied to the top metal electrodes (assembly electrodes). As mentioned in previous section, DEP can occur due to both AC and DC excitation. However, AC excitation is generally preferred to avoid undesired electrochemical interactions at the electrodes' surfaces and to suppress undesired electrophoresis.

Nanowires are suspended in a liquid medium such as Isopropanol and are dispensed onto the chip. Once the AC signal is applied, the nanowires become polarized due to charge separation on their surfaces, as was the case with the spherical body discussed in the previous section. Since the nanowires are more polarizable than the surrounding dielectric medium they experience a dielectrophoretic force that produces net movement in the direction of increasing field density, which occurs at the periphery of the assembly electrodes (electric flux density peaks at the edges of the electrodes). When nanowires of length comparable to the electrode gap spacing approach the electrodes, the electric field strength between the electrodes and ends of the nanowires increases proportionally to the inverse of the distance from the electrodes. This is



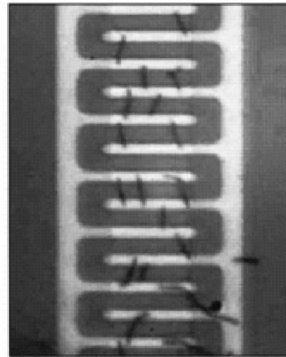
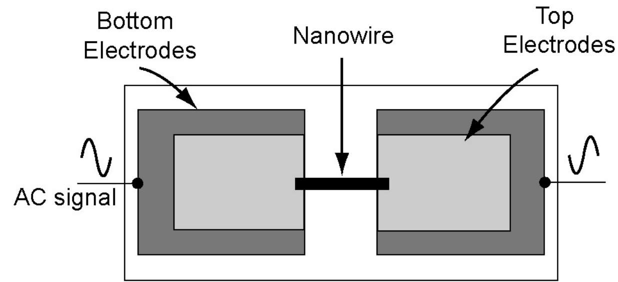


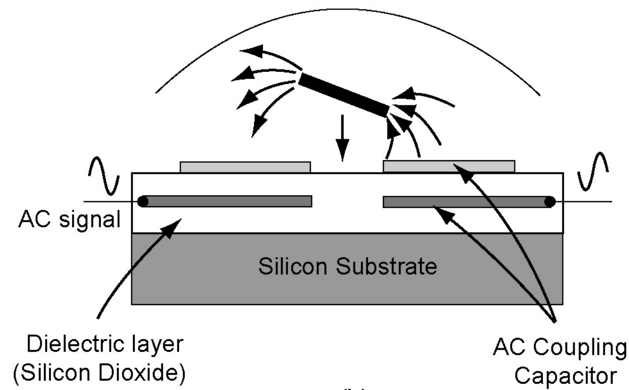
Figure 2.4: Illustration of Dielectrophoretic assembly technique: (a) Cross-sectional view of assembly site — assembly signal provided directly to top electrodes; (b) Gold nanowires are assembled in a random fashion on the interdigitated assembly fingers (from [40].)

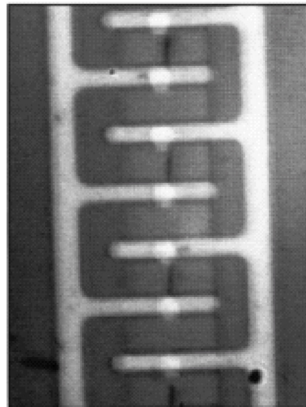
supported by the fact that an applied electric field, E is defined by $\frac{V}{d}$, where V is the potential difference between two electrodes separated by a distance d. Since the distances between ends of the nanowire and periphery of the assembly electrode are on the order of few nanometers, the field intensity is extremely high resulting in large near-field force. This large near-field force results in alignment of the nanowires between the two electrodes.

Figure 2.4 (b) shows the experimental results from the first approach employed by [40], which resulted in random assembly of nanowires at various locations between adjacent electrode fingers. This behavior is attributed to the fact that the electric field strength is a function of position along the inter-digitated electrode fingers during the assembly process. Initially, the field strength at all points along the electrode finger is identical (neglecting fringing fields at ends of the fingers) resulting in equal probability for a nanowire to align anywhere between the fingers. Once a nanowire is assembled, the local electric field strength reduces around the nanowire decreasing the chances of further assembly at that location. However, there may still be effective electric field away from the immediate proximity of the assembled nanowire due to its non-zero resistance, which can result in further nanowire assembly between the same pair of fingers. This activity continues until the nanowires are depleted from the solution, resulting in random placement of nanowires across the structures.

To prevent the uncontrolled assembly and alignment of nanowires a second approach was employed [refer Figures 2.5 (a) and (b)] by [40]. In this approach, two metal electrodes (top and bottom electrodes) were fabricated with a thin layer (100 nm) of silicon nitride acting as the dielectric medium between them. The AC assembly signal is applied to the bottom metal electrodes. The two metal electrodes along with the dielectric medium act as an AC coupling capacitor. When an alternating electric field is applied to the bottom electrodes, the capacitive coupling between the metal electrodes transfers the field to the top electrodes and thus, assembly can be achieved at specific locations on the Si chip. Also, when a nanowire with length comparable to the gap between two adjacent top electrodes bridges the gap, the large localized electric field between them is suppressed resulting in the assembly of just a single nanowire from the solution at a desired location on the chip. Meanwhile, the electric field strength away from the immediate proximity of the assembled nanowire is not as high as in the first approach and thus assembly of additional nanowires between







(c)

Figure 2.5: Illustration of Dielectrophoretic assembly technique: (a) Top view of a typical assembly site; (b) Assembly signal supplied through bottom (coupling) electrodes; (c) Alignment of single nanowires between adjacent pairs of assembly electrodes (from [40].)

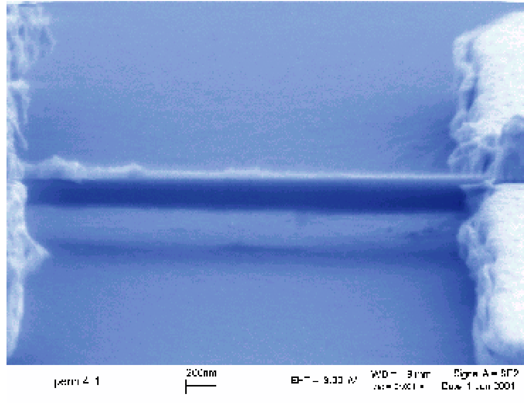
the same fingers is prevented. Figure 2.5(c) clearly shows the difference in degree of alignment between the two approaches. One more advantage of the second approach is that the possibility of burning of electrodes and the nanowires due to excess amount current through them, which eventually results in the first approach, is eliminated completely as there is no shorting of electrodes after the nanowire assembly.

DEP, as mentioned in previous section, is frequency dependent (equation 2.11). P. A. Smith, *et al.*, studied the frequency dependence of nanowire assembly by fixing the voltage between the bottom electrodes at a given value and varying the frequency from 20 Hz to 20 kHz. It was observed that the nanowires showed little field-induced movement at frequencies below 200 Hz and increased movement at higher frequencies. In addition, the alignment time decreased with increasing frequency. This behavior was explained in [40] by the theory that at low frequencies, the polar molecules in the dielectric medium around the nanowire can shield the charge separation on the nanowire leading to degraded assembly forces. At higher frequencies, the polar molecules of the dielectric medium are not able to switch their orientation in the rapidly varying electric field due to their relatively long relaxation times[1] [59]. This would result in greater net polarization of the nanowires and thus stronger assembly forces. On the other hand, the effect of capacitive coupling increases as frequency increases and hence it may result in higher field strength across the assembly electrodes.

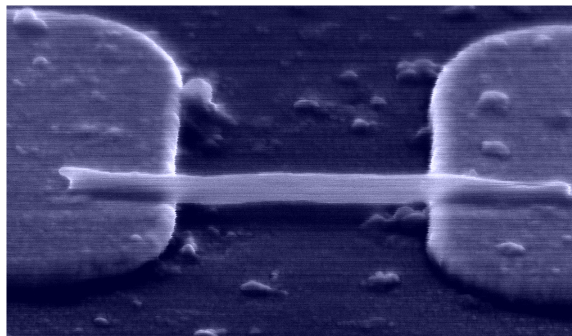
Following the above work, RF-range NEMS were assembled and integrated onto fabricated Si circuits [60]. Metallic rhodium (Rh) nanorods 260nm in diameter and multi-walled carbon nanotubes 250nm in diameter were successfully assembled between gold electrodes. Mechanical resonances of these assembled NEMS devices were also measured. The corresponding SEM pictures are shown in Figures 2.6(a) and (b).

As can be seen, the dielectrophoretic assembly technique described above has tremendous potential to facilitate integration of nanotechnology and modern IC process. The following section describes the compatibility of this assembly technique with modern CMOS IC processes.

[1] The term *relaxation* refers to the molecular process in which a system at equilibrium is constrained to a new position of equilibrium when an external stress is imposed on the system. The time taken by the system to change its position is called the *relaxation time*. In the case of DEP assembly, the external stress is the applied electric field onto dipole/nanowire-containing liquid medium such as Isopropanol.



(a)



(b)

Figure 2.6: DEP assembled mechanically resonant nanowires on Si circuit: (a) A Rh nanowire between gold assembly electrodes (L = 2.5μm and D = 260nm) (from [60]); (b) A multi-walled carbon nanotube (D = 250nm) (from [60]) — Mechanical resonance observed at 1.2 MHz.

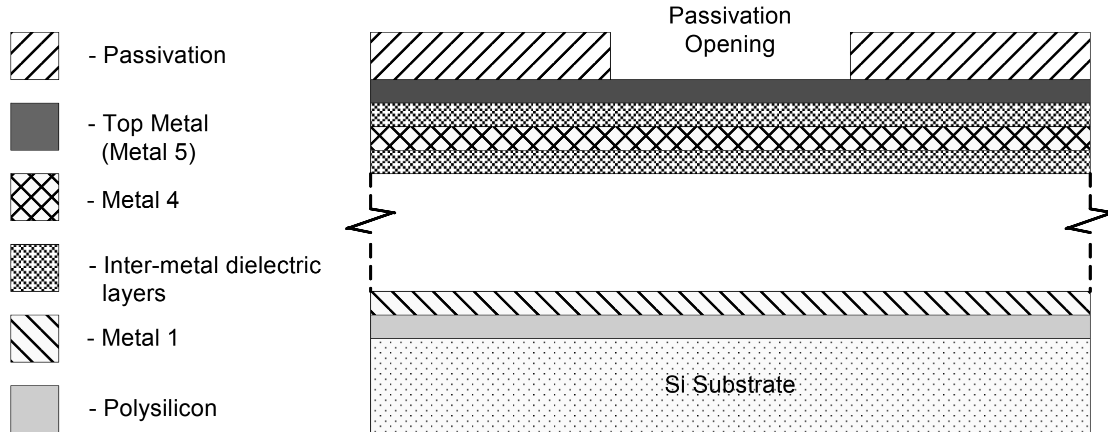


Figure 2.7: Vertical cross-section of different layers available in contemporary CMOS IC processes (thicknesses not to scale).

2.2.1 Compatibility with CMOS IC processes

Modern CMOS IC processes have metal interconnect layers that can be leveraged to enable dielectrophoretic assembly of nanowires. The multiple metal layers available in these processes can be suitably chosen to act as assembly and buried electrodes, to provide distribution of assembly and sense voltage waveforms. Figure 2.7 shows the layer stack of a typical five-metal IC process. In a typical five-metal IC process, the top two metal layers are referred to as metal 5 (M5) and metal 4 (M4), respectively. The assembly electrodes can be defined in the M5 layer and the buried electrodes for applying assembly signal can be defined in the M4 layer. The buried electrodes can be connected directly to contact pads to apply the AC signal using an external source. The M5 layer along with the M4 layer and the inter-metal dielectric layer between them would then act as the AC coupling capacitor required for the DEP assembly technique described above. The protective passivation layer (typically some type of glass [61]) covering the entire chip must be selectively removed over the assembly electrode areas to enable nanowire assembly. Once a nanowire becomes assembled it can be coupled to analog measurement circuitry integrated in the same CMOS process.

Figure 2.8, illustrates the fabrication and assembly of diverse functionalized nanosensors on top metal electrodes on a CMOS chip incorporating operating circuitry. As

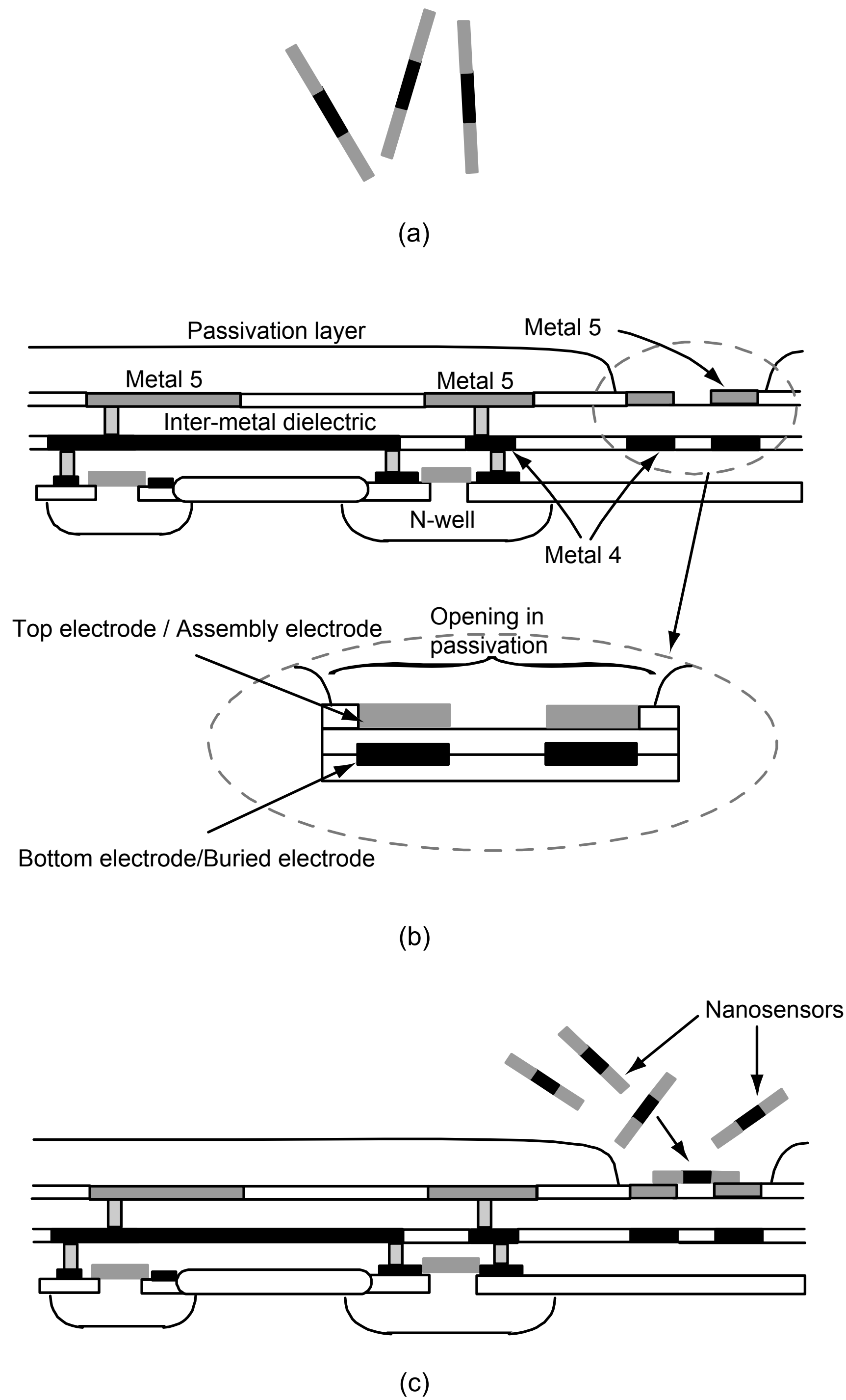


Figure 2.8: Illustration of DEP assembly on CMOS chip: (a) Sensing nanowires suspended in isopropanol; (b) Fabrication of CMOS circuitry and assembly electrodes by the foundry; (c)Assembly and integration of nanosensors using dielectrophoretic assembly technique.

discussed in Chapter 1, nanowires capable of sensing different gases in an environment can be fabricated. Their electrical behavior under exposure to different gases and gas concentrations can be detected with CMOS circuits. The output of the circuits can then be processed digitally and transferred to a communications network for decision and action.

2.3 Chapter summary

This chapter has presented the theory of dielectrophoresis and the technique of dielectrophoretic assembly that will be employed in this work. The use of this DEP assembly technique to integrate nano-scale sensors with modern CMOS IC processes can provide a highly-manufacturable, low-cost platform for the development of integrated sensor nanosystems. The next two chapters form the core of this thesis work discussing the design of a CMOS test chip for nanowire assembly and subsequent assembly experiments and results.

Chapter 3

Design of Assembly Sites and Readout Circuitry

3.1 Background

A primary objective of this thesis is to extend the applicability of the DEP assembly technique to modern CMOS IC processes in order to provide a highly-manufacturable, low-cost platform for the development of integrated nanosensor systems. As discussed in section 2.2.1, the multiple metal layers in modern CMOS processes can be leveraged to define similar excitation and assembly electrodes as in [40] enabling the post-IC assembly of nanowires. Figure 3.1 shows the layout and cross-section of a typical assembly site based on a five-metal IC process and the schematic of a simple resistance measuring readout circuit that includes a Wheatstone bridge network and a CMOS two-stage differential amplifier to amplify the DC output voltage of the bridge network to a measurable level. The assembly electrodes can be defined in the M5 layer and the buried electrodes for distributing the assembly signal can be defined in the M4 layer, creating (along with the inter-metal dielectric layer between these layers) AC coupling capacitors as employed in the DEP assembly technique described in the previous chapter. As shown in the figure, passivation opening can be defined over the assembly electrode areas to enable nanowire assembly. Once a sensing nanowire is assembled and is coupled to a readout circuit, the parameter of interest can be sensed and transmitted using appropriately designed CMOS integrated circuits.

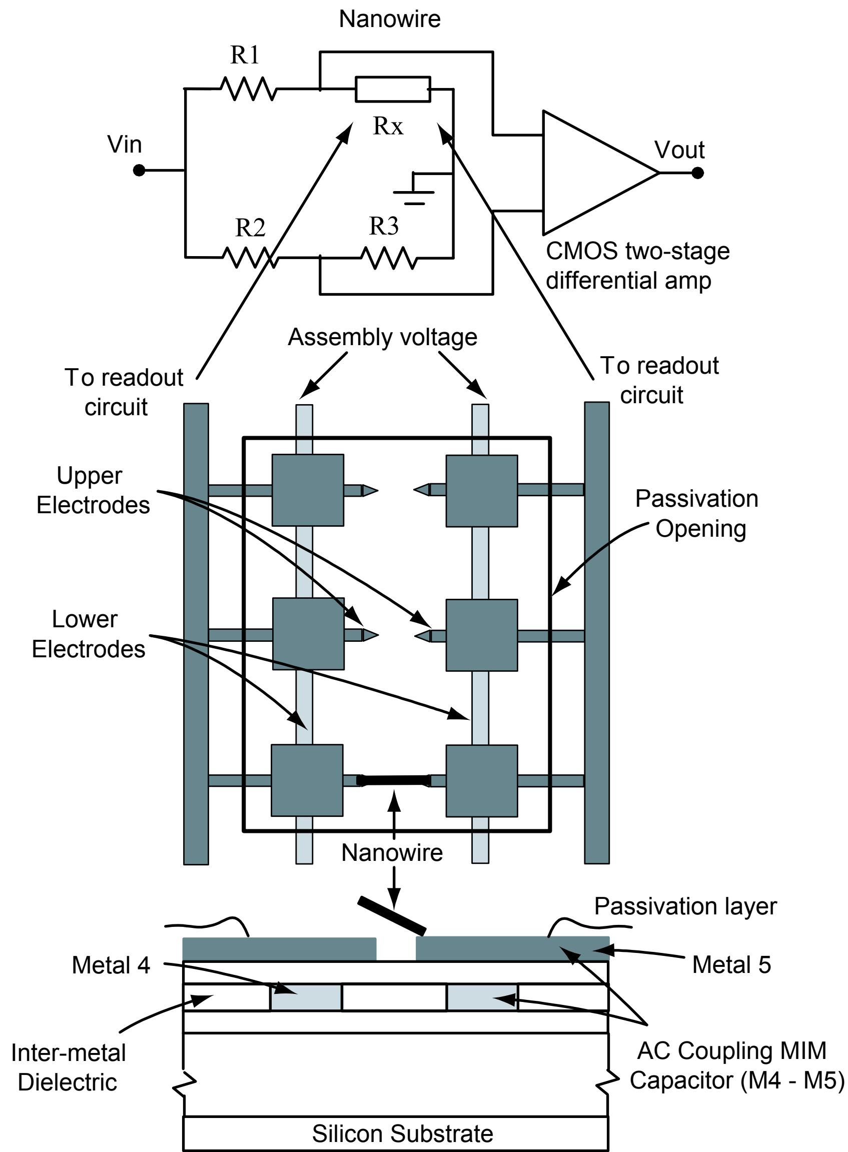


Figure 3.1: Illustration of design concept — layout and cross-sectional view of assembly sites and schematic of readout circuitry.

This chapter describes the layout of nanowire assembly test sites, the design and layout of a CMOS readout circuit and the layout of overall test chip. All the designs were performed using Motorola's HiP6W 0.18-μm Si/SiGe BiCMOS process. This process is a five-metal IC process with the top interconnect metal layer being Metal 5 (M5).

3.2 Layout of nanowire assembly sites

As in many modern VLSI processes, the metal interconnect layers in Motorola's HiP6W 0.18-μm Si/SiGe BiCMOS process are composed of an alloy of copper and aluminum. The top (assembly) electrode structures are fabricated in the M5 layer while the bottom (coupling) electrode structures are in the M4 layer. The dimensions of M4/M5 metal-insulator-metal (MIM) AC coupling capacitors were chosen to result in approximately the same capacitance as employed in [40]. The passivation layer, which is composed of silicon oxynitride (SiON) in this process, is removed over the areas of the assembly electrodes.

An illustration of final back-end-of-line (BEOL) steps of fabrication of a chip in the IC process is shown in the Figure 3.2. All the steps are shown with respect to fabricating sites required for the nanowire assembly process. The standard steps are typically used in the definition of I/O pads for chip bonding/packaging. First, the underlying circuits are fabricated and the M5 layer is planarized inside the areas (shown in Figure 3.1) where passivation openings are defined. The M5 layer is planarized using a Chemical Mechanical Planarization (CMP) technique, after which the SiON passivation layer is deposited all over the chip. Chemical-mechanical planarization process is a means of planarizing and polishing thin layers deposited on silicon wafer substrates [62]. CMP is an important fabrication step in all modern multi-layered integrated circuit processes. This process is usually employed to obtain uniformity in surface topography over the entire fabricated chip and also to prevent the exposure of different metal layers in an integrated circuit to the environment.

Following the passivation layer deposition, the SiON is etched from areas where passivation openings are defined. A 1.6μm total thickness capping layer of aluminum and tantalum is then deposited over the entire chip surface. This capping layer is

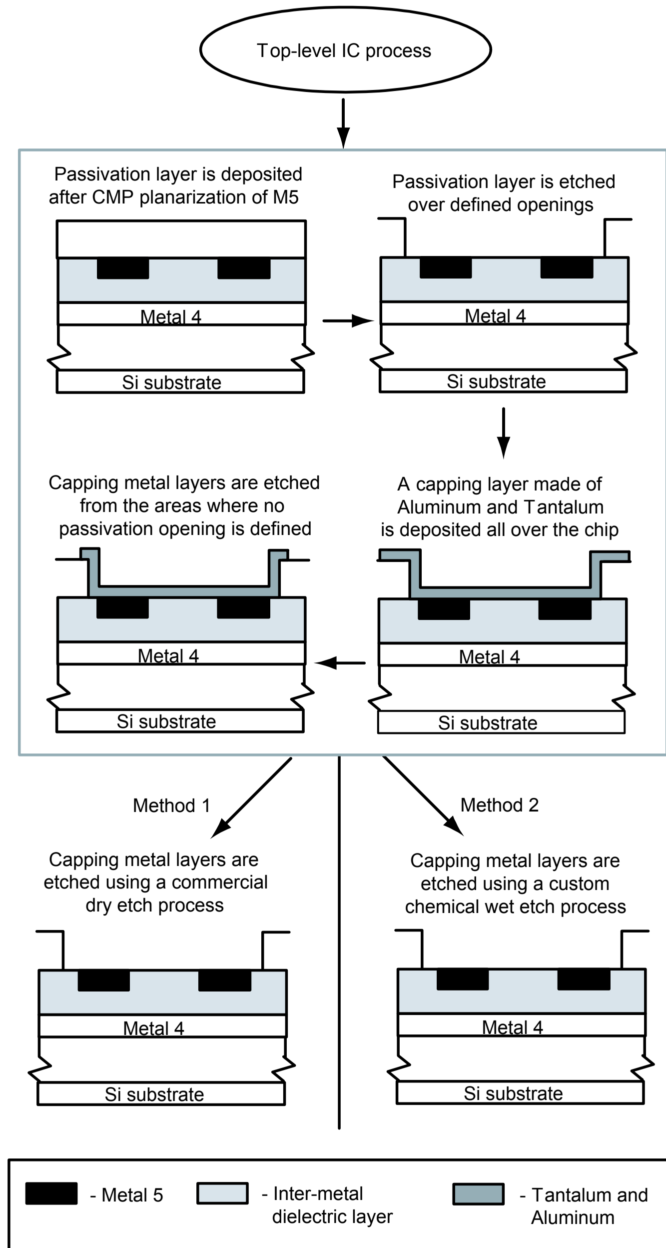


Figure 3.2: An illustration of final back-end-of-line (BEOL) fabrication steps used for defining nanowire assembly sites.

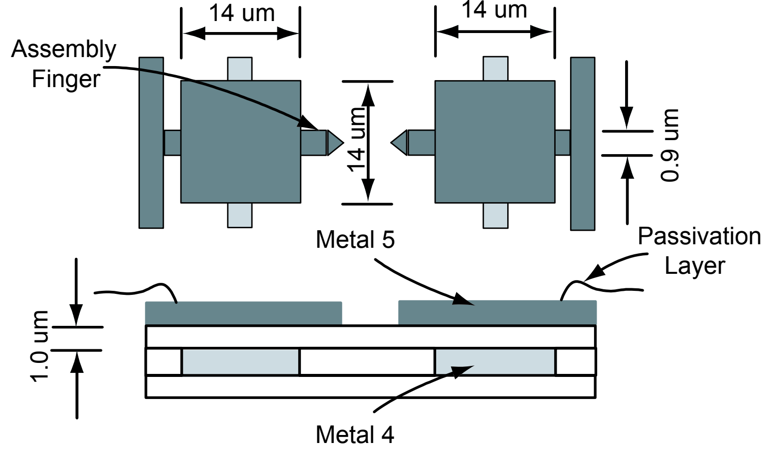


Figure 3.3: Close-up view of nanowire assembly sites with on-chip dimensions.

subsequently removed from the areas where the passivation layer was *not* etched, and thus remains over the assembly sites at this point in the process. Two methods were explored for removal of this metal from the assembly sites. In Method#1, the capping metal layer is removed using a commercial dry etch (plasma etch) process leaving the M5 top electrodes exposed. This processing step is typically used for fabricating edge seal of a chip and was leveraged here for the removal of the capping metal layer over the assembly sites. Here, the passivation openings are denoted by an alternative layer-definition parameter. In Method#2, the capping metal layers of aluminum and tantalum layers were rather etched out of the assembly sites using an in-house wet-etch process. These two processing options yielded different assembly results, which will be discussed in the next chapter along with other results obtained from the assembly experiments.

3.2.1 Design of assembly sites

Figure 3.3 shows a close-up view of a nanowire assembly site indicating various important dimensions. As mentioned above, the dimensions of the assembly and field coupling electrodes were chosen to result in approximately the same capacitance that was employed in [40]. In [40], the dielectric layer between the assembly and the coupling electrodes was composed of Silicon Nitride [relative permittivity (ϵ_{r1}) of $\sim$7.0] and the area of the resulting parallel plate coupling capacitor was $3\mu m$ by $4\mu m$ ($A_1 =$

$12\mu m^2$). The approximate value of coupling capacitance (neglecting fringing fields) is given by:

$$C_1 = \frac{\epsilon_0 \epsilon_{r1} A_1}{d_1} \tag{3.1}$$

where, ϵ_0 is the permittivity of free space (8.854×10^{-12}F/m). The resulting capacitance was about 7.5 fF.

In the IC design process used for this thesis work, the separation distance between M5 and M4 electrodes (d_2) is about 1.0 μm and the relative permittivity of the inter-metal dielectric layer between the electrodes (ϵ_{r2}) is about 4.5. C_2, the coupling capacitance of the assembly site shown in Figure 3.3, can be equated to C_1 to calculate the area of M5/M4 MIM capacitor (A_2) required to result in roughly the same coupling capacitance. The required area, A_2, was calculated to be $\sim 196\mu m^2$. Therefore, $14\mu m \times 14\mu m$-square-shaped MIM coupling capacitors were employed in the CMOS chip design to achieve the desired capacitance. Assembly fingers of width $0.9\mu m$ were connected to the upper capacitor plates to increase the concentration of the applied electric field at the tip of the electrodes in order to enhance the assembly of metallic nanowires.

3.2.2 Layout details

The layout of nanowire assembly sites and the whole CMOS chip was performed using Cadence Virtuoso layout tool [63]. In total, four families of assembly sites were laid out with four different ranges of gap spacing — 1) $3.0\mu m - 3.8\mu m$; 2) $3.8\mu m - 4.6\mu m$; 3) $4.6\mu m - 5.4\mu m$; and 4) $5.4\mu m - 6.2\mu m$. Each of these families had four different circuit configurations — A) Top assembly electrodes directly connected to the I/O contact pads of the chip as shown in the Figure 3.4; B) Top assembly electrodes physically isolated from rest of the assembly site and I/O contact pads as shown in the Figure 3.5; C) Top assembly electrodes directly connected to the readout circuitry through output lines; D) Top assembly electrodes physically isolated from the readout circuit. Layout pictures of last two configurations are associated with the layout of the readout circuit described in Section 3.3. Each of the configuration mentioned above has five sets of assembly fingers altogether with a $0.2\mu m$ increase in gap spacing

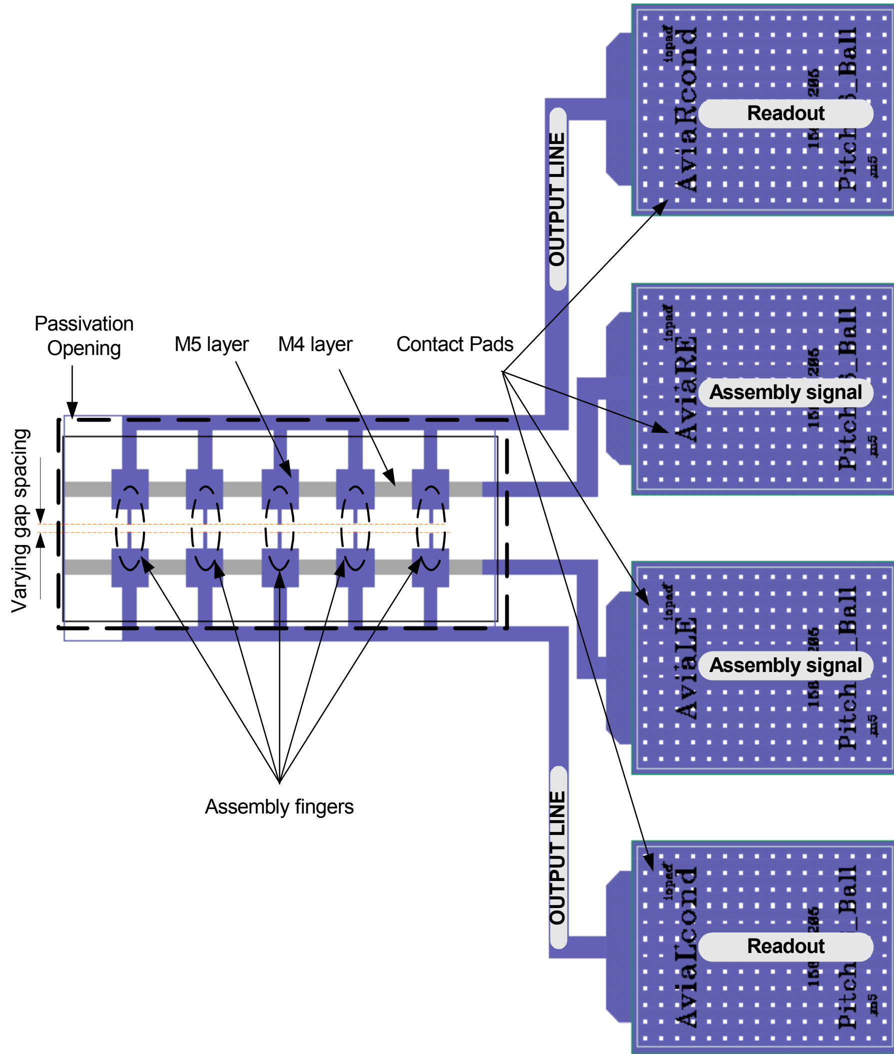


Figure 3.4: Layout of one set of assembly sites (type 1-A) using Motorola's (Now Freescale) HiP6W BiCMOS process. In this case, the gap spacing between assembly fingers varied from $3.0\mu m - 3.8\mu m$ with a $0.2\mu m$ increment from one set of fingers to another.

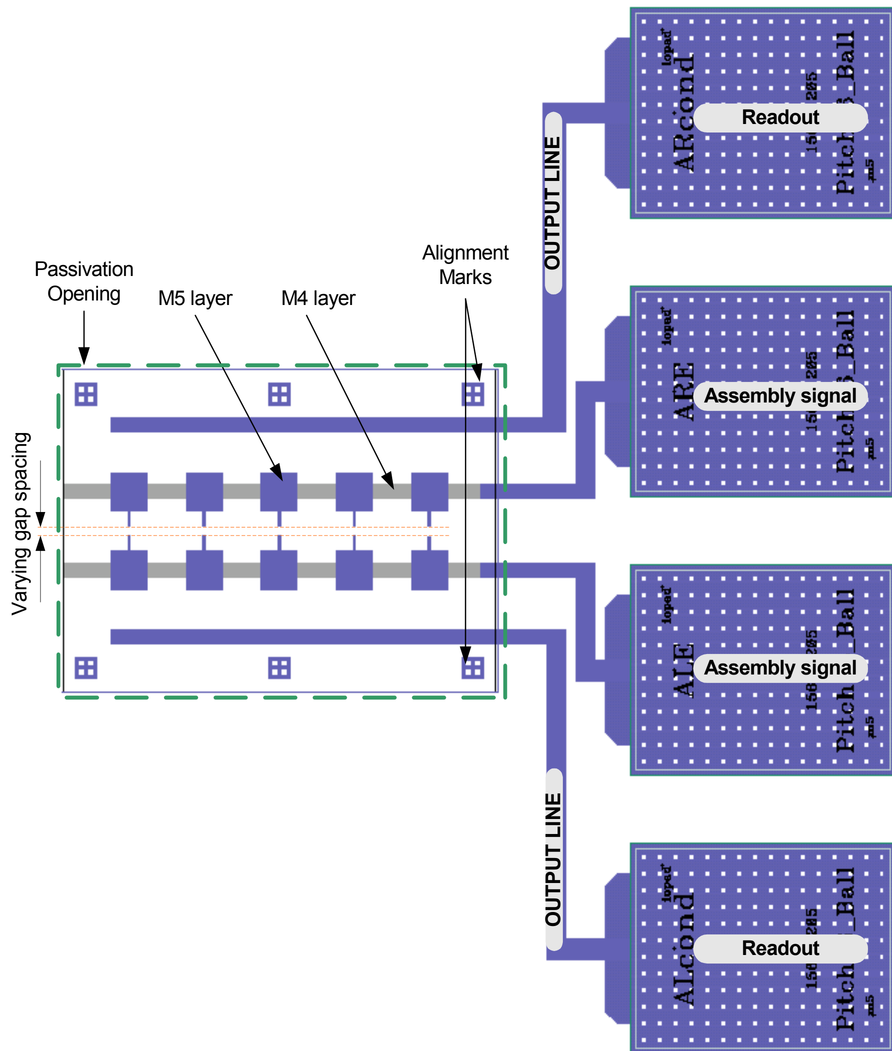


Figure 3.5: Layout of assembly site (type 1-B) requiring post-assembly electron-beam lithography and metallization to connect the nanowires to the I/O contact pads. The cross-in-square alignment marks are seen within the passivation opening.

from one set of fingers to another (refer to Figure 3.4). All the assembly sites are denoted in the same manner as above in section 3.4 which discusses the whole layout of the chip.

In the configuration types B and D, nanowires require post-assembly e-beam lithography (EBL) and metallization step to be connected to the I/O contact pads or to the readout circuit through top assembly electrodes. The cross-in-square-shaped alignment marks are provided in M5 layer within the passivation opening of the assembly site for the EBL step.

3.3 Readout circuit design

For demonstration purposes, the CMOS-based readout circuit chosen to interface with assembled nanodevices was a simple Wheatstone bridge network with a two-stage CMOS differential output amplifier. These simple circuits were designed in the core CMOS technology of Motorola's HiP6W low-voltage 0.18-μm Si/SiGe BiCMOS process. The Wheatstone bridge network consists of three known resistance values (R_1, R_2 and R_3). The CMOS two-stage differential amplifier is included to amplify the output of the resistance bridge to a measurable voltage. A complete schematic of the readout circuit is shown in Figure 3.6.

The unknown resistance (R_X) in this case is the assembled nanowire. The resistance of the nanowire is the parameter of interest, which is measured in the form of a voltage, V_{out}. The relationship between the output voltage, V_{out} and the unknown resistance, R_X is given by the equation:

$$\frac{V_{out}}{V_{in}} = \alpha \left[\left(\frac{R_1}{R_1 + R_2} \right) - \left(\frac{R_X}{R_3 + R_X} \right) \right] \tag{3.2}$$

where, α is the voltage gain of the differential amplifier and V_{in} is the voltage drop supplied across the Wheatstone bridge to ground through resistance R_0 ($= 70\Omega$). The resistance, R_0, ensured proper biasing of the input transistors of the differential amplifier. The supply voltage for the readout circuit is 1.8 Volts. The MOS transistors used in the differential amplifier stages (M_1, M_2, M_3 and M_4) are multi-fingered devices with a total gate width of $100\mu m$ each. The threshold voltages of the MOS

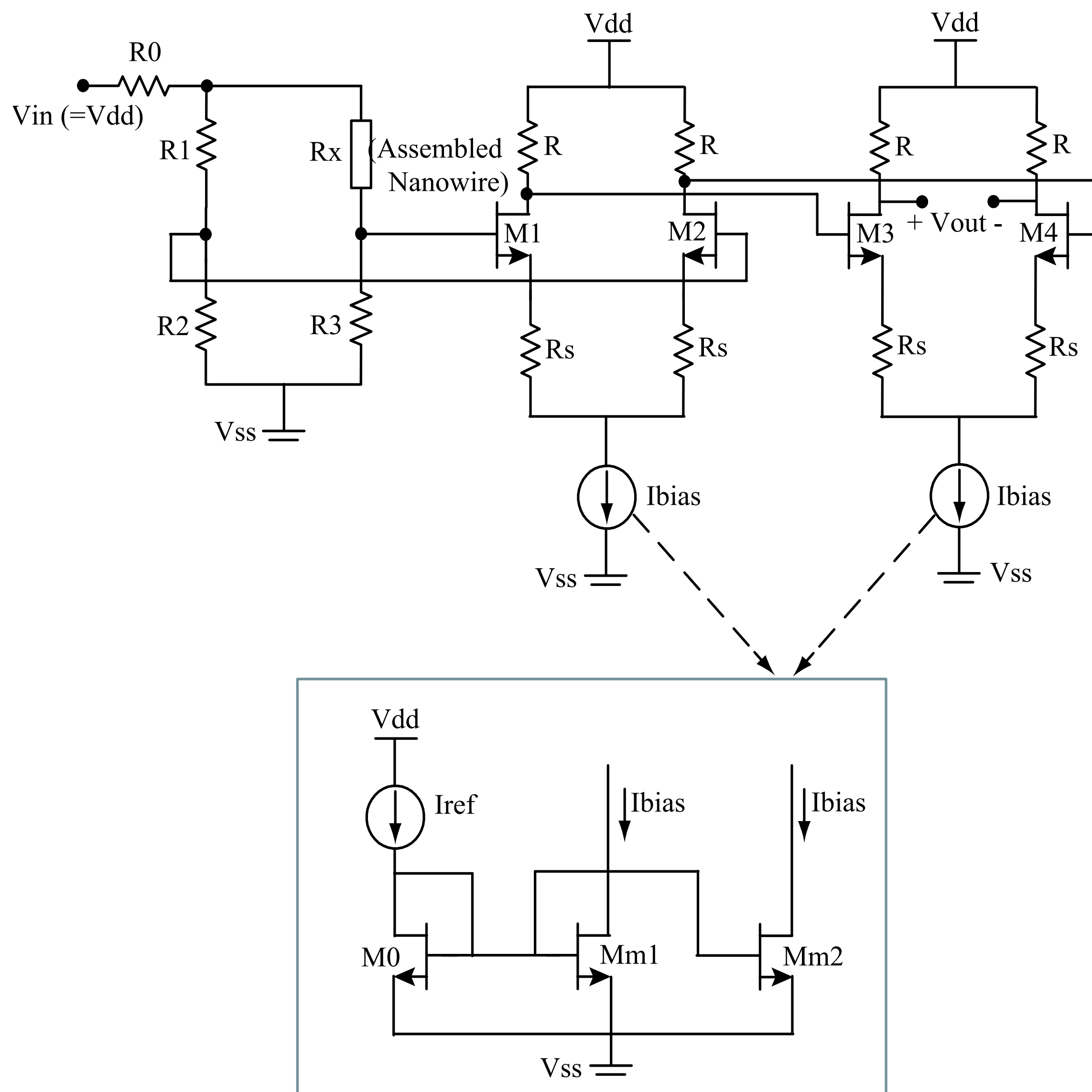


Figure 3.6: Schematic of the readout circuit designed in core CMOS technology of Motorola's HiP6W BiCMOS process. The inset shows the current mirror circuit.

Nanowire (L $\sim 5\mu m$, D $\sim$ 250nm)	**Resistivity,** ρ $(\Omega \cdot m)$	**Resistance,** R (Ω)
Rhodium (Rh)	4.3×10^{-8}	4.3
Gold (Au)	2.2×10^{-8}	2.3
Tin-oxide (SnO_2)	0.25×10^{-5}	255

Table 3.1: Calculated values of resistances for nanowires of different material. The CMOS readout circuit was designed based on these values of resistances.

transistors used in this design were about 350 mV. A bias current (I_{BIAS}) of 270 μA is provided to the differential stages by a CMOS current source (see inset of Figure 3.6). The CMOS current source consists of a basic current mirror network with M_{m1} and M_{m2} supplying the bias current I_{BIAS} to each of the differential amplifier stages. The readout circuit was designed to give measurable differential output voltage (-400mV to +400mV) for a wide range of resistances varying from few milliohms to 500 Ohms. This resistance range was chosen based on the resistances of the nanowires that were available for assembly. Rhodium, gold and tin-oxide (SnO_2) nanowires of length (L) $\sim 5\mu m$ and diameter $\sim$ 250nm were available for the assembly experiments. The values of electrical resistivities at room temperature (ρ, obtained from [64] and [65]) and the corresponding resistances (R) of these nanowires are summarized in the Table 3.1. The resistances are calculated using the formula, $R = \rho \cdot L/A$, where A is the cross-sectional area of the cylindrical nanowire.

Assembly of tin-oxide nanowires (resistance $\sim 250\Omega$) on prefabricated CMOS ICs was the initial focus of this thesis. Hence, the ratio of resistors on each branch of the Wheatstone bridge network was set in such a way that the bridge balances (i.e., produces a zero differential output voltage) when the value of R_X equals 250 Ω. In other words, when $\frac{R_2}{R_1} = \frac{R_3}{R_X} = 100$, the bridge is balanced and $V_{out} = 0$. The value of resistors R_1, R_2 and R_3 were designed to be 100Ω, 1Ω and 25 kΩ respectively. The simulated output of the readout circuit is shown in the Figure 3.7. It can be seen from the simulated output that the all the values of resistances summarized in Table 3.1 were accommodated in the readout circuit design. The resistances R_1 and R_2 of the Wheatstone bridge were made very small compared to R_3 and R_x so that the difference in voltage drop across these two pairs of resistors is large enough to produce a measurable voltage at the output of the differential amplifier. This ensures a larger range of V_{out}.

The layout of the readout circuit is shown in Figure 3.8. The simulated output

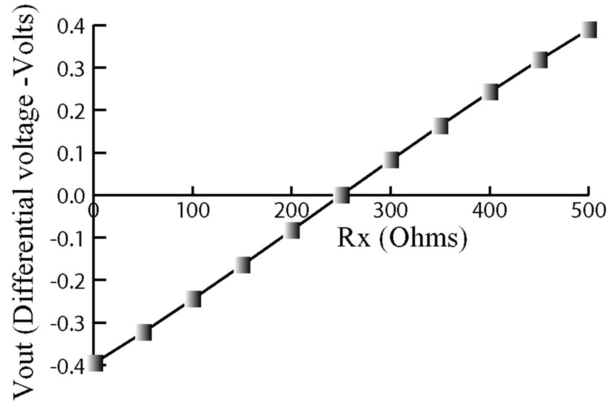


Figure 3.7: Simulated output of the readout circuit showing the variation of output differential voltage with resistance value of R_X.

shown in the figure does not include the parasitics due to metal interconnects of the layout. Accurate parasitic extraction tools were not available at the time chip design was submitted for fabrication. Hence, the sensitivity of the Wheatstone bridge to the layout parasitics was not taken into account; i.e., possible changes in the output of the readout circuit were to be expected.

Some test/calibration circuits were implemented in the chip for measurement purposes by including two layout designs roughly similar to that shown in Figure 3.8. In this case, the passivation layer was not opened for nanowire assembly. Therefore, the resistance, R_x, which is usually the assembled nanowire, was substituted by resistances (100Ω and 400Ω respectively) available in the IC design process. These layouts were included in the chip for testing and calibrating the operation of readout circuit before making measurements on circuits connected to assembled nanowires.

3.4 Final layout of the assembly experiment chip

The overall layout of the assembly experiment chip is shown in Figure 3.9. The die area of the chip is 2.5 mm $\times$ 2.5mm. The figure shows the assembly sites with varying gap spacing between the top electrodes. The layout of assembly sites can be identified using the notations defined in section 3.2.2. For example, layout (1-A) is the set of assembly sites with electrode-gap spacing of $3.0\mu m - 3.8\mu m$ and with

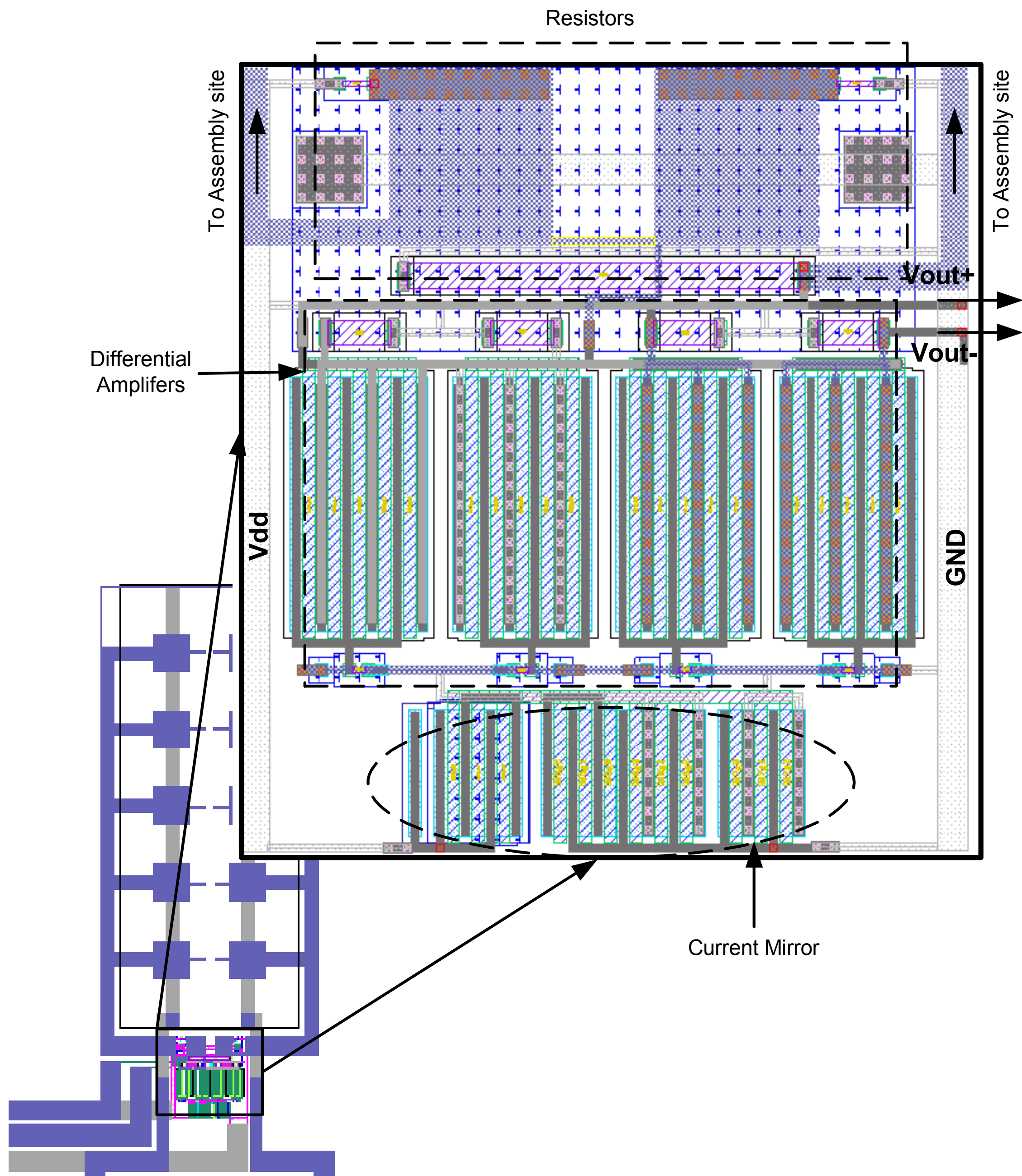


Figure 3.8: Layout of readout circuit connected to a nanowire assembly site.

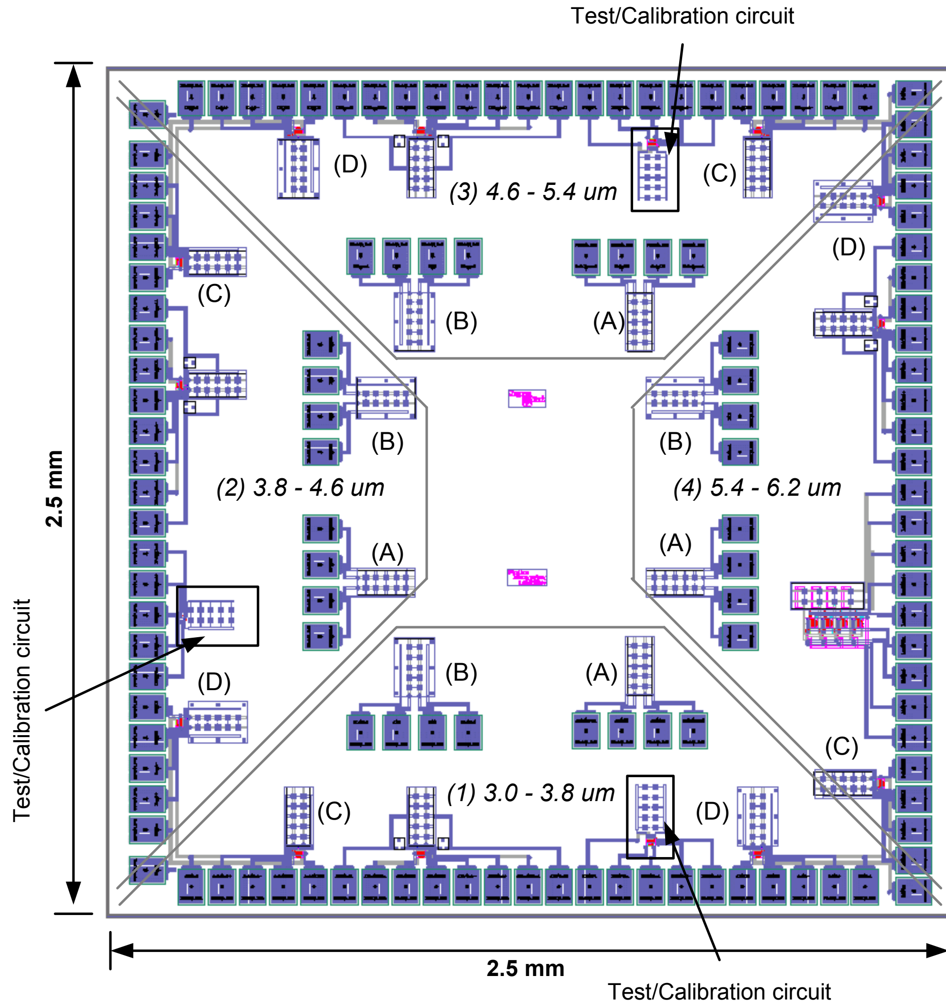


Figure 3.9: Cadence Virtuoso layout of the assembly experiment chip in Motorola's HiP6W process. Die area = 2.5mm × 2.5mm.

the top metal electrodes connected directly to the I/O contact pads. As mentioned earlier, the top metal electrode gap spacing varied by $0.2\mu m$ from one set of assembly fingers to another. The test/calibration circuits can also be seen on the mask.

3.5 Chapter summary

This chapter has presented the layout of an experimental assembly chip for fabrication in Motorola's HiP6W BiCMOS process. The designs incorporate a range of assembly sites, both with and without readout circuits. The readout circuit design includes a Wheatstone bridge network coupled with two-stage CMOS differential amplifier to measure the resistance of assembled nanowire. The next chapter discusses various experiments performed to realize assembly of metallic nanowires on the fabricated CMOS chip.

Chapter 4

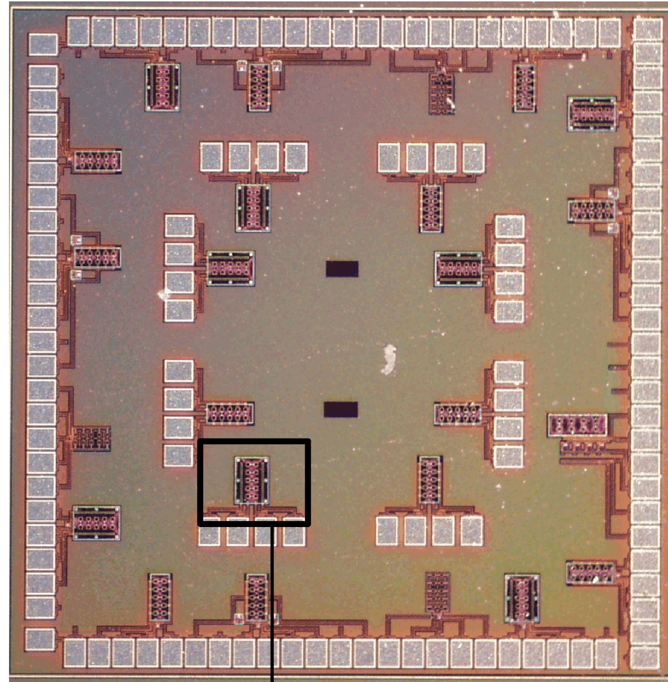
Assembly Experiments and Results

4.1 Background

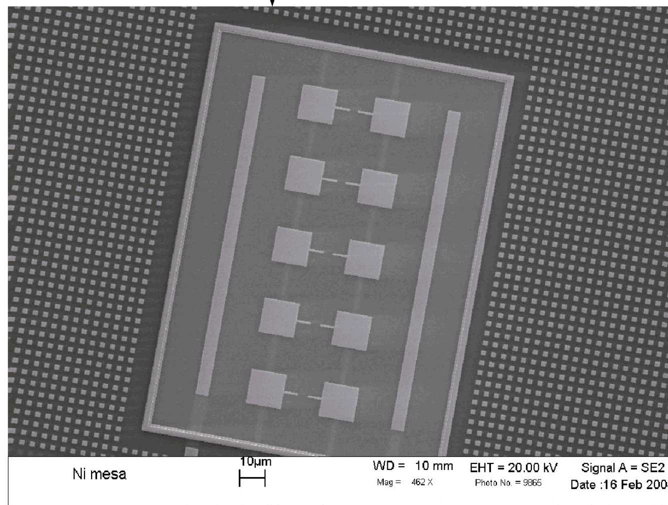
This chapter discusses assembly experiments performed in this thesis work and the corresponding results. The process flow discussed in Chapter 3 was implemented with two final step options for fabricating the assembly sites (see Figure 3.2). In Method#1, the capping metal layer (aluminum and tantalum) is removed using a commercial dry etch (plasma etch) process leaving the M5 top electrodes exposed. In Method#2, the capping metal layer is rather etched out of the assembly sites using an in-house wet-etch process. The wet-etch process implemented in Method#2, will be discussed in this chapter. These two processing options ultimately had different impacts on the viability of the assembly process in CMOS technology.

4.2 Experiment and its set-up

The photograph of the final fabricated chip with the readout circuit and the assembly sites is shown in Figure 4.1(a). A close-up SEM picture of an assembly site is shown in Figure 4.1(b). Figure 4.2(a) shows the experiment set-up for assembly of nanowires and for DC-IV characterization of the assembled nanowires. The corresponding photograph is shown in Figure 4.2(b). All the experiments were performed on a Cascade Alessi 3200 REL probe station. A Topward 8110 function generator was

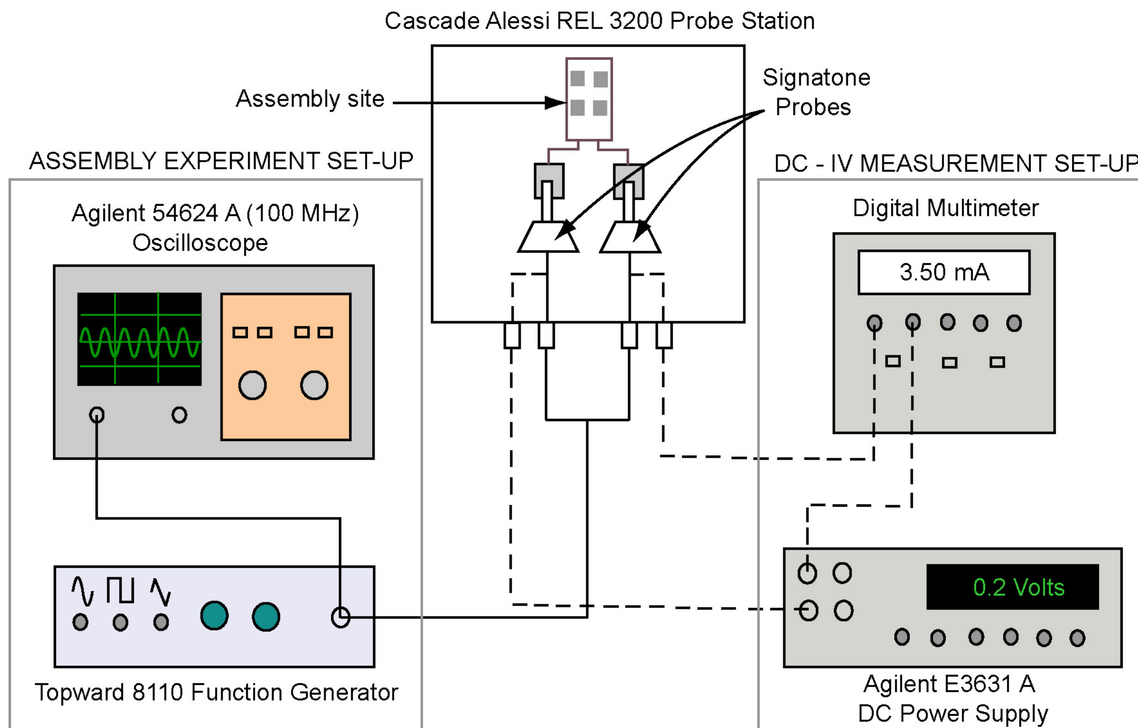


(a)

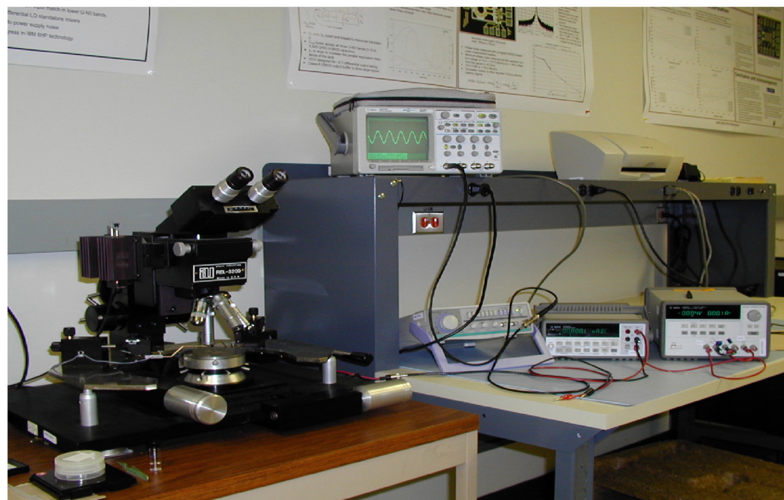


(b)

Figure 4.1: (a) Micrograph of the assembly experiment chip (2.5mm × 2.5mm) fabricated in Freescale Semiconductor's HiP6W BiCMOS process. (b) A close-up SEM picture of an assembly site (not directly connected to the readout circuit in this case) on the fabricated chip.



(a)



(b)

Figure 4.2: (a) Experimental set-up for assembly of nanowires and DC-IV characterization of assembled nanowires; (b) Photograph of the experiment set-up.

used as the AC signal source and Agilent 54624A 100 MHz oscilloscope was used for measuring the signal amplitude level. A standard digital multimeter and a Agilent E3631A DC power supply were used for performing the DC-IV measurements on the assembled nanowire. Signatone micropositioners and tungsten probe tips were used for supplying the assembly signal to the appropriate assembly pads and for providing DC voltage for measuring I-V characteristics of the assembled nanowire.

For proof of concept purposes, all the experiments were conducted using metallic rhodium nanowires suspended in isopropanol. The length of nanowires ranged from $3\mu m$ to $5\mu m$ with a diameter on the order of 250 nm. The nanowires were suspended in a solution of isopropanol (IPA). The signal source was set up for a sinusoidal voltage signal with peak-to-peak amplitude of 15 Volts and a frequency of 500 kHz. A drop of isopropanol containing suspended rhodium nanowires was delivered onto the chip with a pipette and the AC signal was activated and supplied to the bottom electrodes (M5) via contact pads. The AC signal was kept ON for about 3-4 minutes; the signal was deactivated before the IPA dried.

4.3 Results

Assembly experiments were performed on the CMOS test chip. Results using both processing methods #1 and #2 are described in this section. Details on the custom wet-etch used in Method#2 are presented below.

4.3.1 Method # 1

As mentioned in Chapter 3, the fabrication process in Method#1 differs from Method # 2 by an alternative layer-definition parameter for the passivation openings. This processing method is generally employed for fabricating the edge seal of a chip and is typically not used elsewhere on the chip. However, in this work this method was used for the purposes of removing the capping metal over the assembly sites. Assembly experiments were then conducted on assembly sites fabricated by this method using the experiment set-up described earlier. Figure 4.3 shows an SEM picture of rhodium nanowire assembled on a CMOS chip. Although the nanowire was success-

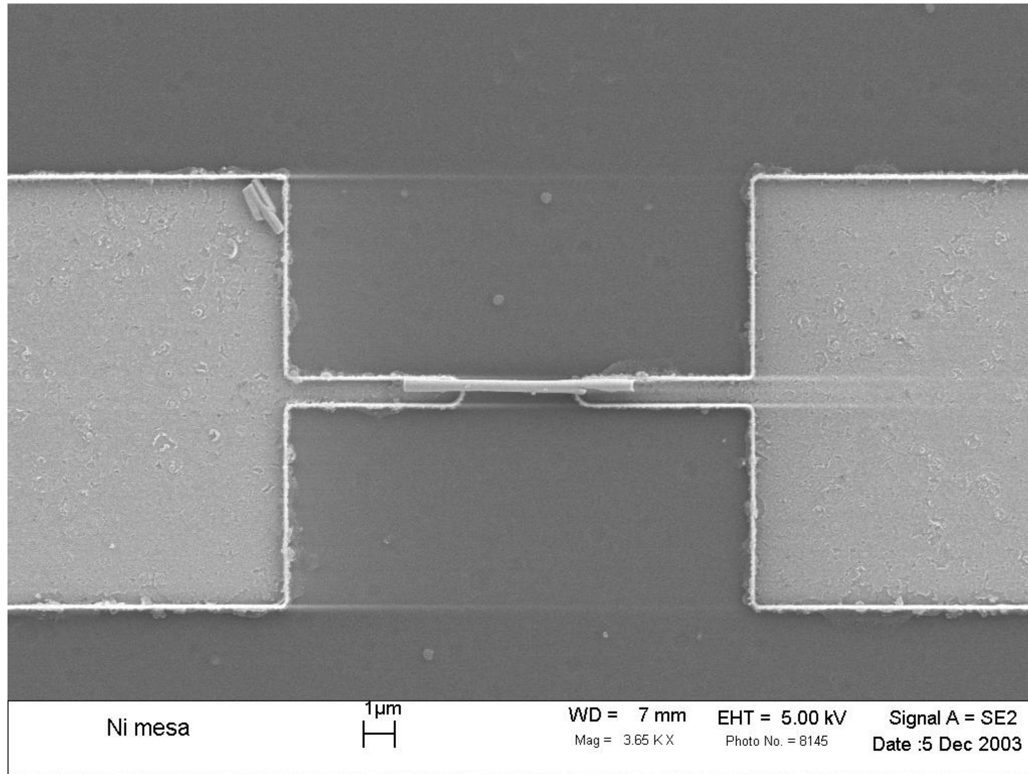


Figure 4.3: SEM picture of a rhodium nanorod assembled on sites fabricated using Method # 1.

fully assembled, there was no electrical continuity between the electrodes through the nanowire (i.e. an open circuit was measured at the contact pads). An SEM picture (Figure 4.4) of these assembly sites revealed the presence of ridges that appear to be responsible for the lack of electrical continuity between nanowires and the metal electrodes.

It appears that the commercial dry etch process for removing the capping Ta/Al layer also attacks the underlying M5 and the inter-metal dielectric layer to a small extent. An illustration of this effect is shown in Figure 4.5. This process results in small loss of planarity in the areas of the M5 layer not protected by the passivation layer, therefore exposing the edges of the M5 layer to the environment. It is believed that the ridges formed are copper oxide resulting from corrosion of the M5 layer edges. Energy dispersive spectroscopy (EDS) testing was attempted using SEM to determine if the ridges were oxidized copper, but the results were inconclusive since the chip

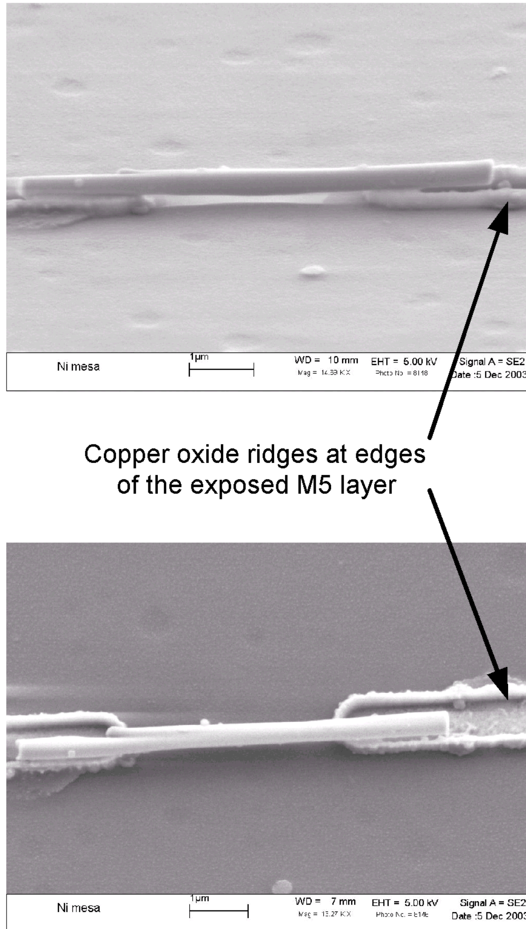


Figure 4.4: Close-up SEM pictures of assembly sites fabricated using Method#1 — the oxidized metal ridges at the edges of the exposed M5 layer indicated with arrows prevent electrical continuity between the nanorod and the top electrodes.

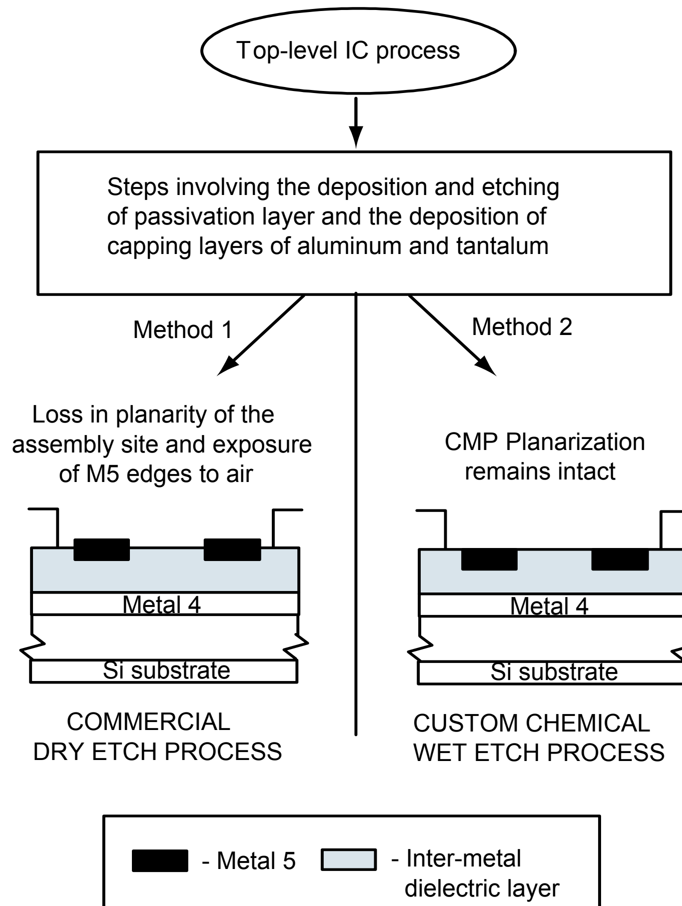


Figure 4.5: Conceptual illustration of two different processes used for etching the Al/Ta capping layer. The commercial dry etch process (Method # 1) causes a loss in planarity of the M5 layer in the assembly site.

predominantly contains metal oxides and the scanning area of the SEM was larger than the features to be analyzed. Still, this oxidation is a logical conclusion since the copper which forms the bulk of M5 oxidizes at a very fast rate compared to other metals (e.g. aluminum) when exposed to the air.

4.3.2 Method # 2

In this alternate method, the capping layer etch over the assembly sites is not performed by the foundry but is rather etched using an in-house wet etch process. An SEM picture of assembly sites in this case immediately after delivery from the foundry

Component	Chemical Formula	% by weight
Phosphoric Acid	H_3PO_4	71
Acetic Acid	CH_3COOH	10
Nitric Acid	HNO_3	2
Potassium Perfluoroalkyl Sulfonates	-	<1
Water	H_2O	17

Table 4.1: Chemical composition of Cyantek corporation's AL-12S Aluminum etchant.

is shown in Figure 4.6. The unetched capping metal layers over the assembly sites can be clearly seen. Figure 4.7 shows a micrograph of assembly sites that are covered with the capping layers.

It is important that the metal etchants employed in the removal of the Al/Ta layer not attack the passivation layer, inter-metal dielectric layers, or the copper of the M5 layer which forms the assembly electrodes. With consideration for the selectivity of etchants on rest of the metals and non-metals on the chip, AL-12S Aluminum etchant[1] was first used for etching the capping aluminum. The chemical composition of this etchant is given in table 4.1. The etch rate of this etchant was specified as 1000nm/min at 70°C. Based on the thickness of aluminum layer in the passivation opening, the etching process was timed and performed at 70°C.

An appropriate etchant for tantalum was identified as 50% weight-to-volume potassium hydroxide (KOH) solution [66]. The etch rate of KOH solution on tantalum is about 10 nm/minute at 80°C. Again, based on the thickness of tantalum layer in the passivation opening, the etching process was timed. Figure 4.5 illustrates the maintaining of CMP planarity in the assembly sites. Figure 4.8 shows the SEM pictures of assembly sites after etching both the metal layers. It can be noticed from the figure that the assembly electrodes (M5 layers) remain intact and highly planarized with the surrounding inter-metal dielectric layer and are unaffected by the wet-etch process. No ridges can be seen at the edges of the M5 layers. This also supports the conclusion that the copper of the M5 layer was oxidizing and forming ridges when Method#1 was implemented.

Assembly experiments were then conducted on sites fabricated using this method. Figure 4.9 shows an SEM picture of a successfully assembled rhodium nanowire across

[1]Manufactured by Cyantek Corporation Inc., Fremont, CA 94539. Website:(http://www.cyantek.com/homepage.html)

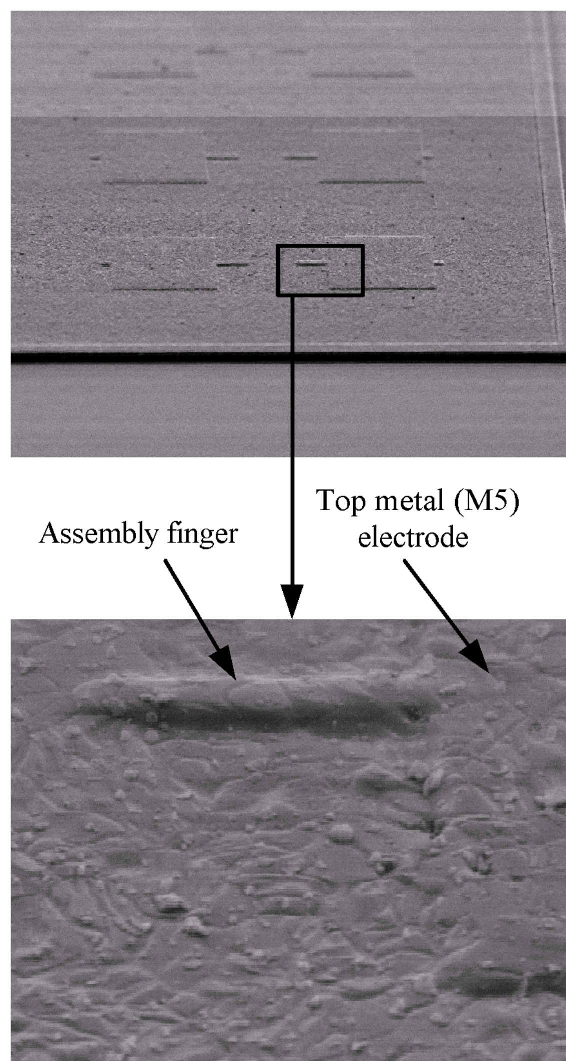


Figure 4.6: SEM pictures of assembly sites covered in the capping layer of aluminum and tantalum.

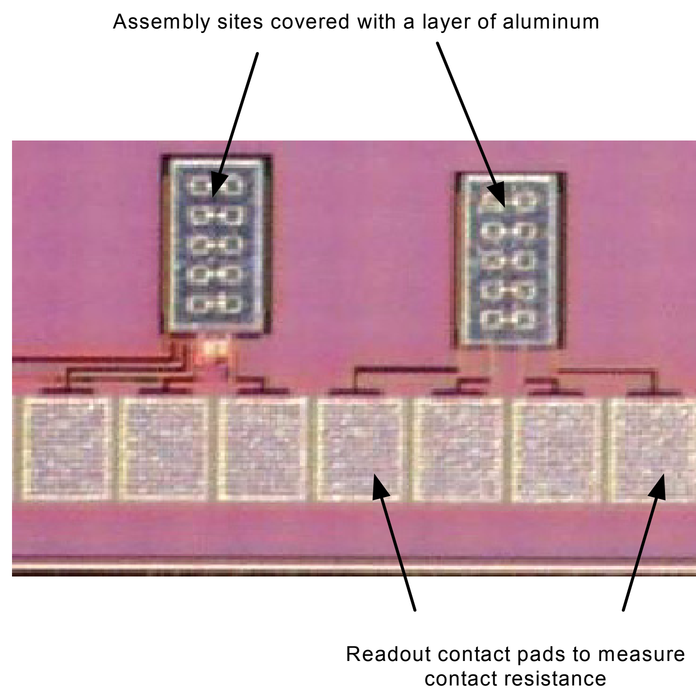
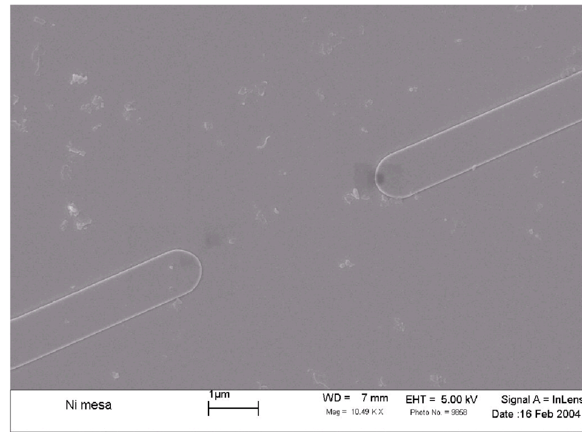


Figure 4.7: Micrograph of two sets of assembly sites. The aluminum/tantalum capping layer can be clearly seen over the defined passivation openings of the assembly sites.

Assembly electrodes after Aluminum etch



Assembly electrodes after Aluminum and Tantalum etch

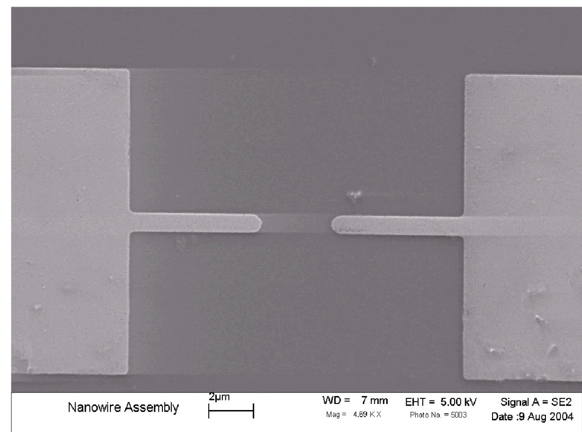


Figure 4.8: SEM pictures of assembly sites after wet-etching the aluminum and tantalum metals inside passivation opening. The absence of oxidation ridges at the metal edges can be clearly seen.

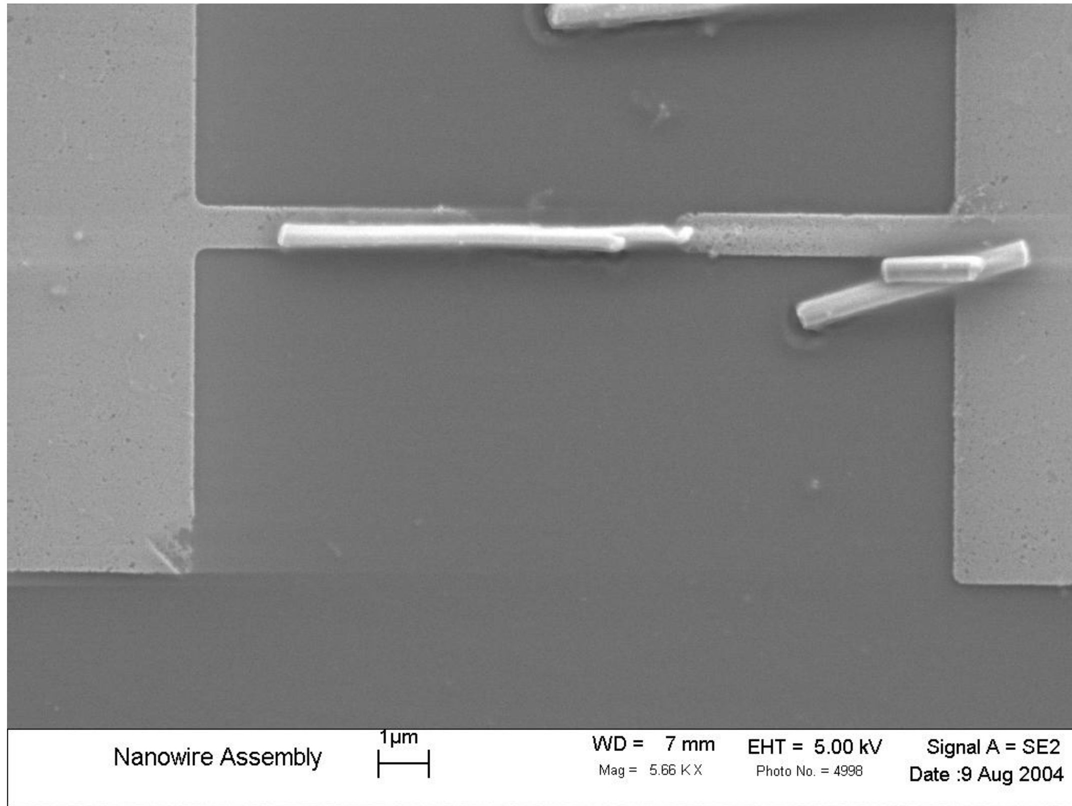


Figure 4.9: SEM picture of an assembled nanowire after wet etching of aluminum and tantalum capping metals. The gap spacing is $3.6\mu m$.

a 3.6 μm-gap. DC I-V characterization of the nanowire was also performed to prove the presence of electrical continuity between the nanowire and the top metal electrode and a resistance of 110 Ω was measured (Figure 4.10). The good electrical continuity further supports the conclusions regarding the metal ridges resulting from Method#1. However, the measured resistance for the rhodium nanowire was higher than the expected value calculated in Chapter 3 (refer Table 3.1). Such deviation in measured resistance is believed to be due to the minimal contact area between the cylindrical nanorod and the top electrodes. Since, this contact area is much less than the cross-sectional area of the rod itself, the flow of carriers into and out of the nanorod was constricted, resulting in a higher-measured resistance.

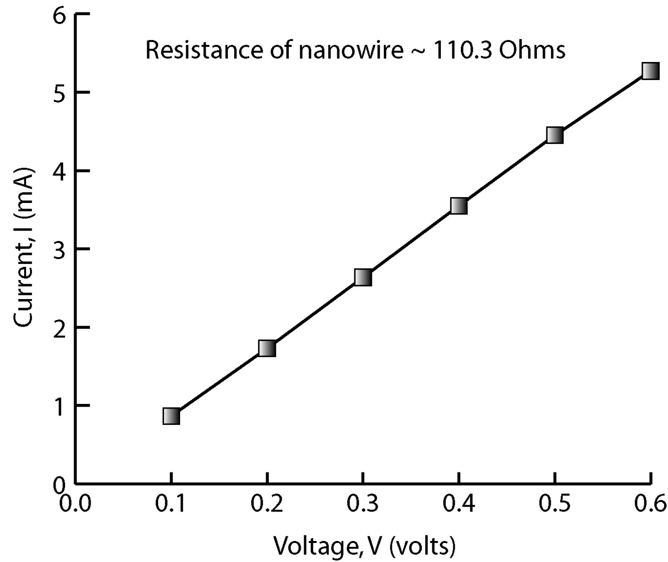


Figure 4.10: DC I-V characteristic of the assembled nanowire.

4.3.3 Integration with CMOS readout circuit

To demonstrate integration with operational CMOS circuitry, assembly experiments were performed on sites connected directly to the Wheatstone bridge and CMOS amplifier circuits shown in Figure 3.1. However, in these attempts, nanowire assembly at the defined electrodes was not successfully achieved for circuits processed using either of the processing methods discussed above. Rather, bunches of nanowires became assembled directly between the I/O pads where the assembly voltage waveforms were applied via probe tips as illustrated in Figure 4.11. The nanowires formed links as shown in the figure and bridged a gap spacing of $20\mu m$ between the I/O contact pads. This behavior is attributed to the degradation of electric field intensity near the assembly electrodes due to a short circuit path through the readout circuitry. In retrospect, it is apparent that the gates of the NMOS transistors (device gate voltage operational limit of 2.8V in this IC technology) in the readout circuits are being exposed to the relatively high assembly voltage magnitudes resulting in gate rupture which in turn creates short circuit paths to ground. This conclusion is supported by measurements that indicate that current consumption of the readout circuitry noticeably increased after an assembly experiment attempt. This underscores the need for some sort of isolation circuitry between the assembly sites and the readout circuitry

in future designs.

Alternatively, the assembly chip layout also included designs without pre-existing interconnects between assembly sites and circuitry [refer to Figure 4.1(b)]. In these designs, assembly sites are initially electrically isolated from the circuitry and require the post-assembly fabrication of additional conducting electrodes between the site and the readout bus electrodes (which can also be used to clamp the ends of the nanowires as discussed in [39]). Successful assembly, clamping, and interconnection was accomplished (Figure 4.12) on those sites by [67]. However, the resistance of the structure exceeded the range of operation of the readout circuits. Such high values of resistance are likely to be dominated by interfacial oxidation between the IC top metal layers and the post-IC deposited metals.

4.4 Summary of results

The experimental procedures used in this work for nanowire assembly were presented. The concept of assembly of metallic nanowires on pre-fabricated CMOS integrated circuits was successfully demonstrated using Motorola's HiP6W technology. The electrical continuity obtained using Method#2 underscores the necessity for maintaining CMP planarization in copper interconnect based VLSI technologies to avoid corrosion of exposed metal edges. *If planarization can be maintained, good electrical continuity between the assembled nanowire and the top metal electrodes can be achieved.* Alternatively, electrical continuity can also be achieved using a post-assembly metallization technique described in [67]. This technique also clamps the assembled nanowire in place to avoid subsequent movement of the device. However, it would be preferable to avoid this post-IC lithography process, particularly when a large number of nanosensors are to be sequentially assembled. Chapter 6 suggests a novel localized solder-like bonding technique as a part of future work to overcome this limitation.

Another important conclusion is the necessity for electrical isolation of readout circuit from the assembly sites. Since, modern IC process operate at lower supply levels than those required for DEP assembly of nanodevices, the readout circuits should include gate protection circuitry. These protection circuits can potentially be realized with

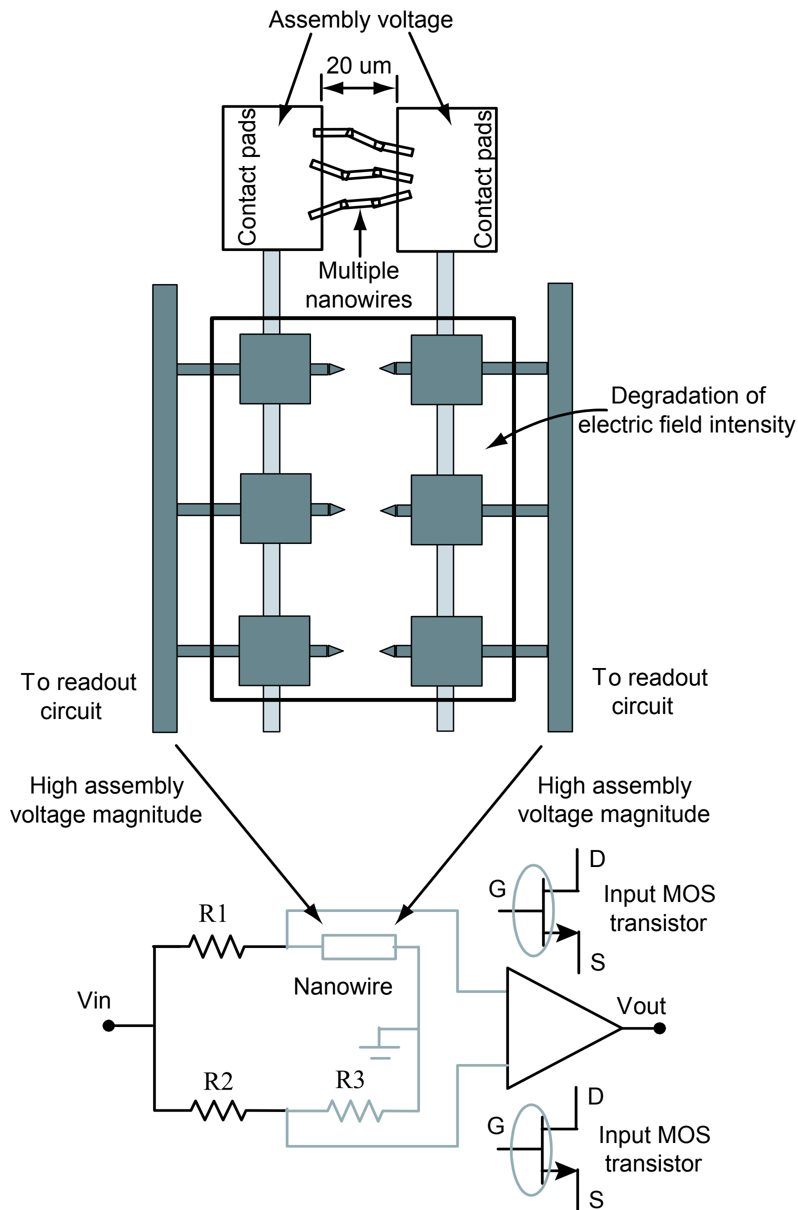


Figure 4.11: Illustration of failure of nanowire assembly on sites connected to the readout circuitry due to gate rupture of input MOS transistors of the differential amplifier stages. Multiple nanowires are assembled between the I/O contact pads (spacing between pads $\sim 20 \mu m$) instead of M5 electrodes.

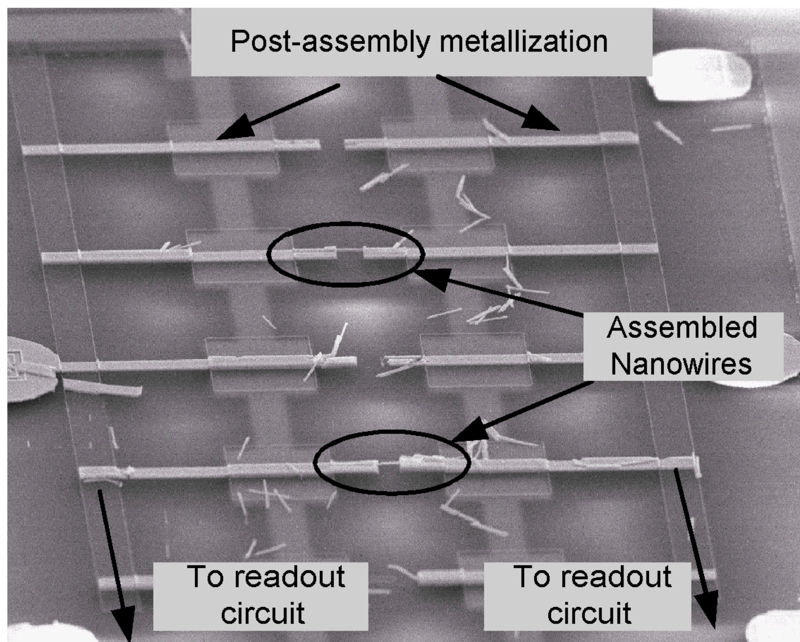


Figure 4.12: SEM picture of assembly sites initially electrically isolated from the readout circuitry. Assembled nanowires are clamped and connected to the readout circuit using a post-assembly e-beam lithography and metallization step (from [67].)

standard electrostatic discharge protection diodes. Alternatively, the readout circuit should initially be isolated from assembly sites and a post-assembly fabrication of readout bus electrodes as mentioned above should be employed.

Based on the results presented in this chapter, the objective of this thesis to demonstrate the assembly of nanowires on a CMOS integrated circuit was successfully achieved. The second objective of this thesis was to design an appropriate RF transmitter for wireless sensor network applications. The next chapter describes the design of an multi-band ultra-wideband transmitter in Motorola's HiP6WRF low-voltage 0.18-μm Si/SiGe BiCMOS process.

Chapter 5

Design of Multi-band Ultra-wideband Transmitter

5.1 Background

As described in Chapter 1, wireless sensor networks have a wide range of potential applications in commercial, industrial and military arenas. Some requirements for the RF communications interface for wireless sensor networks include data transmission at low data rates over short ranges, robust communication in the presence of interference, and multiple access capabilities. Ultra-wideband data transmission has potential to meet these requirements using low-power consuming circuitry at relatively low costs.

Ultra-wideband communication has recently shown significant promise for applications such as high-data rate wireless personal area networks (WPAN) and wide area networks (WAN). However, the properties of UWB signals can also be exploited in wireless sensor networks. While sensor networks typically do not require such high-speed data transmission as the applications mentioned above, it is critical that their transmissions are not plagued by interference. UWB signals are relatively free from multipath fading compared narrowband data transmission systems [68]. Multi-user communications can be achieved through spread-spectrum techniques such as DS-SS and FH-SS [69]. In addition, UWB signals can penetrate some obstructions with lower signal degradation compared to narrowband systems. This chapter provides an

insight into the fundamentals of ultra-wideband signaling, and describes the system-level architecture of a multi-band ultra-wideband transmitter designed for wireless sensor network applications. The transmitter described in this chapter was team-designed in Motorola's HiP6WRF low-voltage 0.18-μm Si/SiGe BiCMOS process as a part of the 2003 Motorola Wireless and Beyond Design Exposition.

5.2 Ultra-wideband radio

Before the details of the ultra-wideband transmitter design pursued in this thesis are presented, the theory of ultra-wideband signalling is discussed in this section. The FCC report and order, issued in February 2002 [70], allocated 7500 MHz of frequency spectrum for unlicensed use of UWB devices in the 3.1 to 10.6 GHz frequency band. As per FCC regulations, an ultra-wideband signal should occupy more than 500 MHz bandwidth in the 3.1 - 10.6 GHz range, while meeting the spectral mask requirements [71]. With such large spectrum allocated for unlicensed usage, significant flexibility is offered in the choice of the communication system architecture and its components. Figure 5.1 shows an example of an ultra-wideband signal in both the time and frequency domains.

In an ultra-wideband radio, information can be encoded in a UWB signal using several methods. Proposed modulation schemes for UWB radio include pulse position modulation (PPM), pulse amplitude modulation (PAM), and binary phase shift keying (BPSK). Figure 5.2 shows UWB pulses with a BPSK modulation scheme. In this case, the polarities of the pulses are switched based on the information to be encoded (0 or 1). It is obvious that, in this method, only one bit per pulse can be encoded because there are only two polarities available modulation states.

5.2.1 Multi-band communication

Sensor networks require multiple access data communication systems owing to the potentially large number of nodes that would be present in such a network. In the past, low-power frequency-hopped spread spectrum (FH-SS) communication systems have been employed for multi-user wireless sensor network applications [72][24]. A

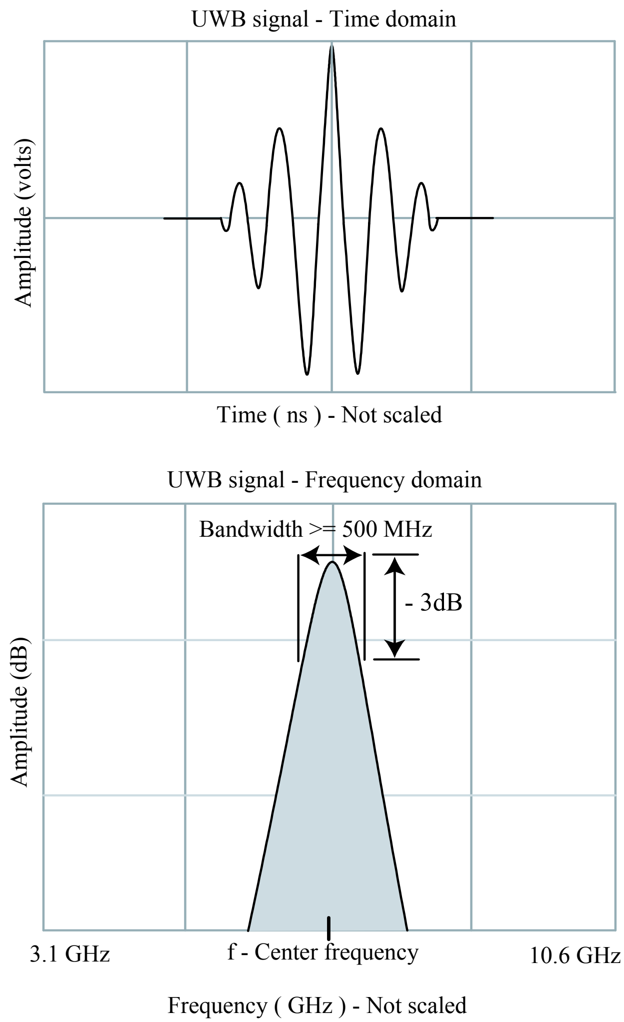


Figure 5.1: An ultra-wideband signal in the time and frequency domain.

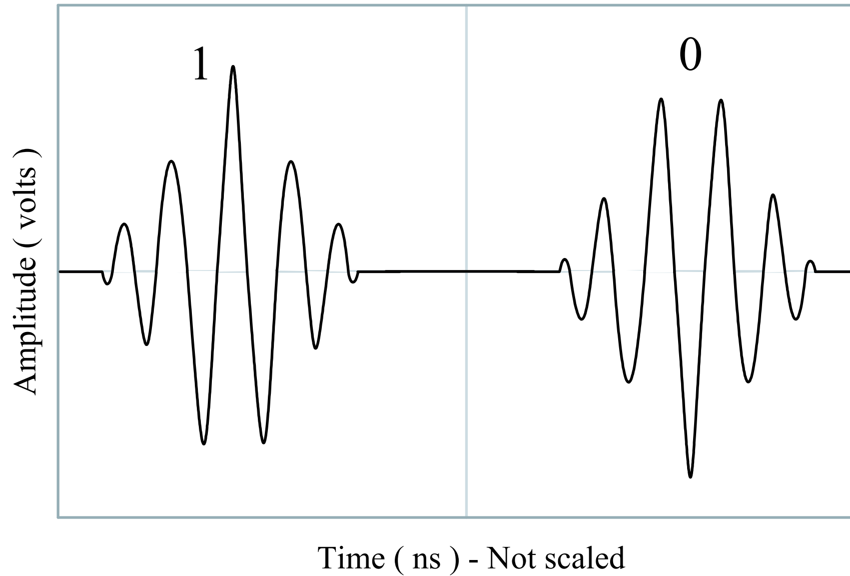


Figure 5.2: Biphase modulation in an ultra-wideband radio.

multi-band approach can be straightforwardly realized with a UWB system because of the large spectrum available for unlicensed usage (A maximum of 15 bands of the minimum 500 MHz bandwidth occupancy can fill the available 7500 MHz UWB spectrum). A frequency hopping scheme can be introduced using this multiband approach by transmitting multiple UWB signals at different center frequencies determined by a PN code [73]. FH-SS schemes allow multiple sensor nodes to share a given frequency bandwidth making it an appropriate scheme for wireless sensor networks. On the other hand, as mentioned in Section 1.3.1, data collisions are not a major issue in wireless sensor network applications because of their relatively low-data rate requirements. FH-SS is preferred over direct sequence spread spectrum (DS-SS) schemes in these applications because it requires less complex associated circuitry leading to low-power dissipation [47]. Figure 5.3 shows an illustration of such system in which different pulses are transmitted in frequency bands that are hopped in a pseudo-random fashion. A similar scheme is incorporated in the transmitter design architecture to be described in the next section.

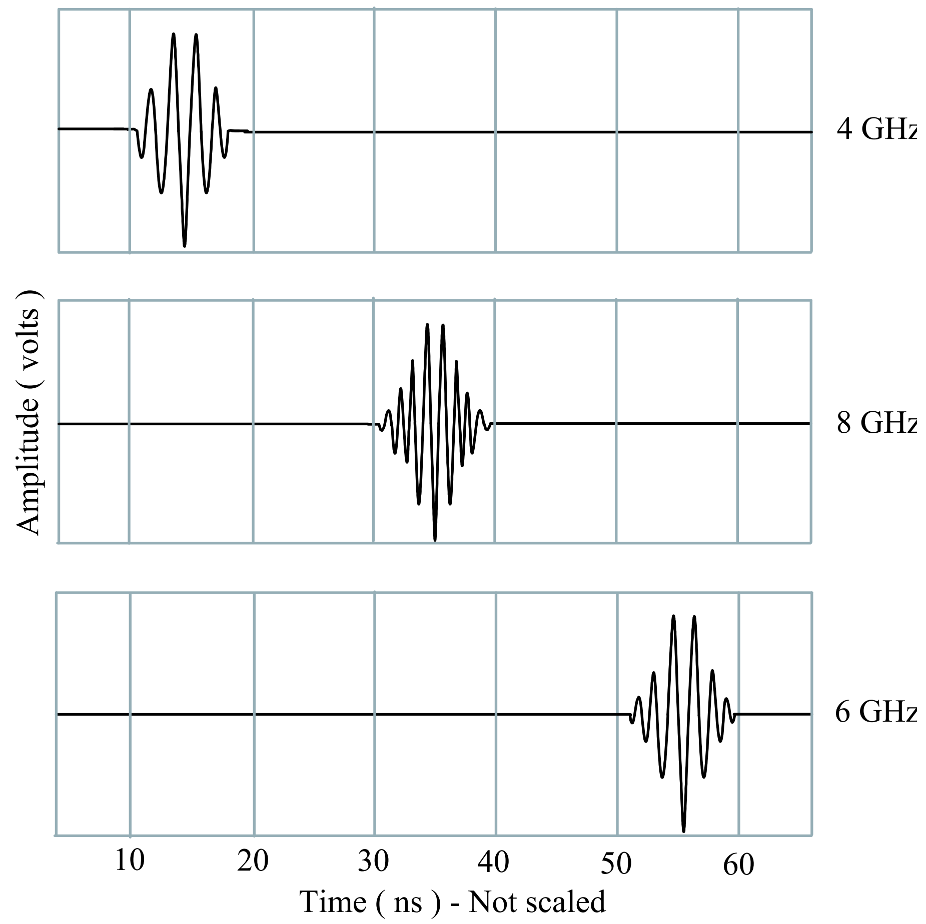


Figure 5.3: UWB multi-band approach with a frequency hopping scheme.

5.3 Design architecture of ultra-wideband transmitter

Figure 5.4 shows the proposed architecture for the multi-band UWB transmitter pursued in this work. The transmitter is composed primarily of four components including: (1) a PLL-based frequency synthesizer which generates different center frequencies under control of a pseudorandom code generator; (2) a pulse generator which produces the required ultra-wideband characteristic signals with a BPSK modulation scheme; (3) an analog to digital converter (ADC) which is used to digitize analog sensor data; and (4) an appropriate transmit power amplifier. For proof of concept purposes the PLL is designed to transmit 3 different center frequencies (For larger scale wireless sensor networks more frequencies will be required). As a part of this thesis work, a CMOS phase-frequency detector (PFD), an on-chip passive loop filter and a CMOS pseudo-noise (PN) code generator was designed. In addition, the overall layout of the transmitter chip was completed using Cadence Virtuoso layout tool. Circuit-level - block-level schematics will be described for the CMOS PFD, the CMOS PN code generator and, the passive loop filter. The corresponding simulation results and the simulation results of the PLL-based frequency synthesizer will also be discussed.

At present, the components inside the dashed-lines (labeled as present work) of Figure 5.4 have been designed and fabricated in Motorola's HiP6WRF low-voltage 0.18-μm Si/SiGe BiCMOS process. The fabricated transmitter chip is now in the packaging stage. The transmitter uses a reference frequency of 100 MHz that will be initially provided by an off-chip crystal oscillator. This reference is provided at one input of the CMOS phase/frequency detector. The PLL was designed to provide stable output at three different frequencies using a switched-tank negative-G_M voltage controlled oscillator (VCO) whose output is then passed to the pulse generator. The objective of the pulse generator is to mask the VCO output with short square-shaped pulses to produce the 500 MHz-wide bandwidth needed for UWB signal transmission, and to modulate the data sent on the pulses. Based on the data input provided to the transmitter, a simple BPSK modulation scheme is implemented here by switching between the (+) and (-) RF outputs of the PLL. A CMOS pseudo-random code generator is used to control the switching of frequency states in the VCO. The

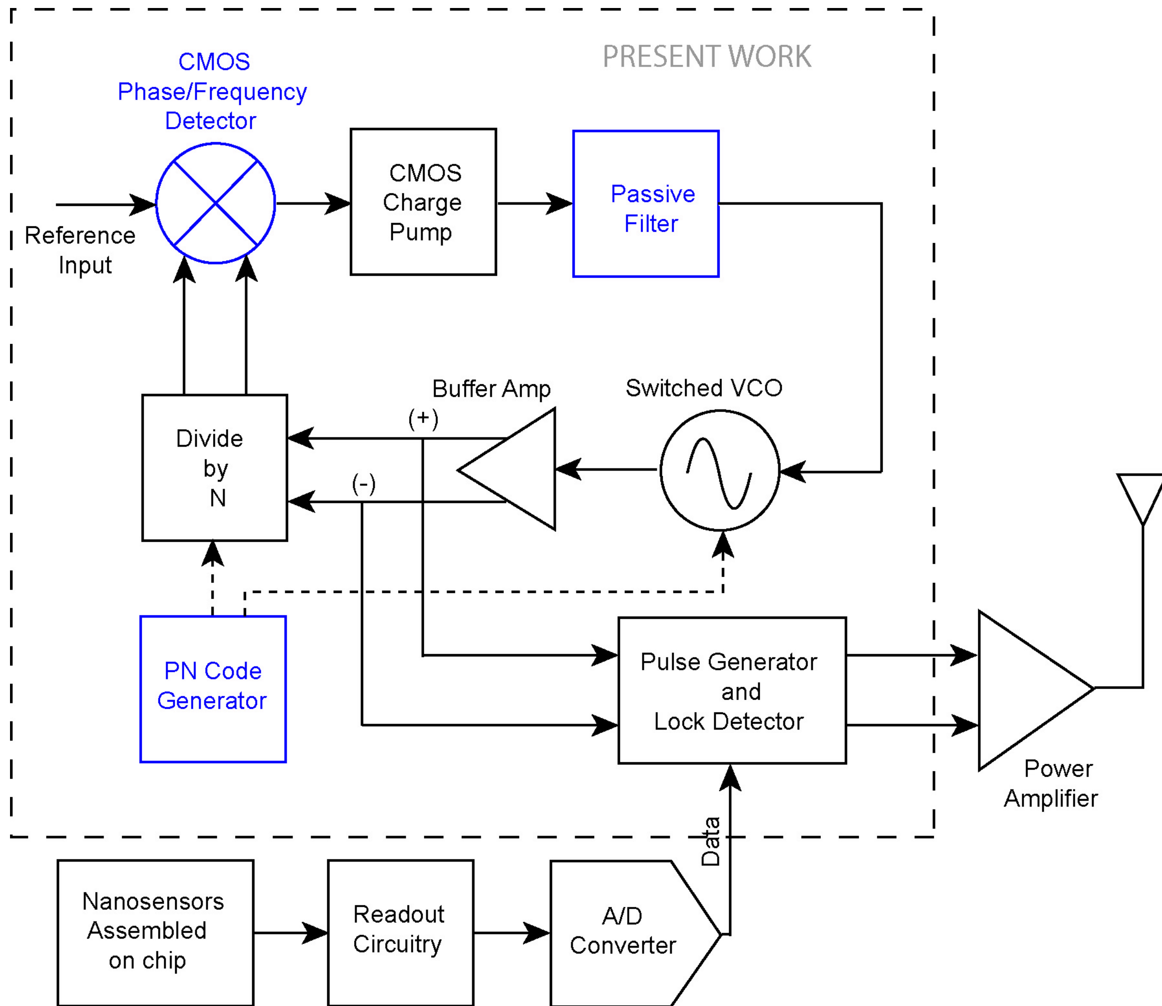


Figure 5.4: Proposed architecture of multi-band UWB transmitter. The highlighted components were designed as a part of this thesis work. In addition, the overall layout of the transmitter was also performed using the Cadence Virtuoso layout tool.

following sections will discuss the individual components of the transmitter from a design perspective.

5.4 Design of PLL-based frequency synthesizer

The two main types of frequency synthesizers are direct digital frequency synthesizers (DDS) and phase-locked loop frequency synthesizers. In a DDS, arbitrary waveforms are created piecewise using digital values of amplitude versus time stored in a look-up table in memory. In the DDS approach, power-consumption is increased due to the usage of large number of components in the look-up table in memory [74]. Such high power consumption and circuit complexity of the DDS is prohibitive for usage in low-power wireless sensor network applications. On the other hand, PLL-frequency synthesizers are relatively well-suited for communication transceivers where high output frequencies are required at low-power. The output frequencies are generated using a VCO with an LC-tank circuit implemented with a set of different capacitive states.

In a PLL-frequency synthesizer, the output frequency (f_{out}) is some integer multiple of a reference frequency (f_{ref}). Figure 5.5 shows the block-level schematic of the PLL frequency synthesizer designed in conjunction with this thesis work. The output of a VCO, which is designed to be the required output frequency, is divided down to the proximity of the reference frequency using a divide-by-N network (a frequency divider) where N is an integer. The phase and frequency of the divided output (f_{div}) is compared with the phase and frequency of the reference input using a phase/frequency detector, and an output based on the deviation of divided output from the reference input is generated. This output is then fed to a *charge pump* which drives the loop filter of the PLL.

The CMOS charge pump implemented in this thesis consisted of two current sources (PMOS and NMOS), one "charging-up" the loop filter capacitor(s) while the other "charging-down" the loop filter capacitor(s). The accumulation-mode varactors used in the VCO tank circuit of the transmitter design presented in this thesis have a capacitance-voltage characteristic such that their capacitances decrease with an increase in the voltage across them. Alternatively, the frequency tuning range is directly

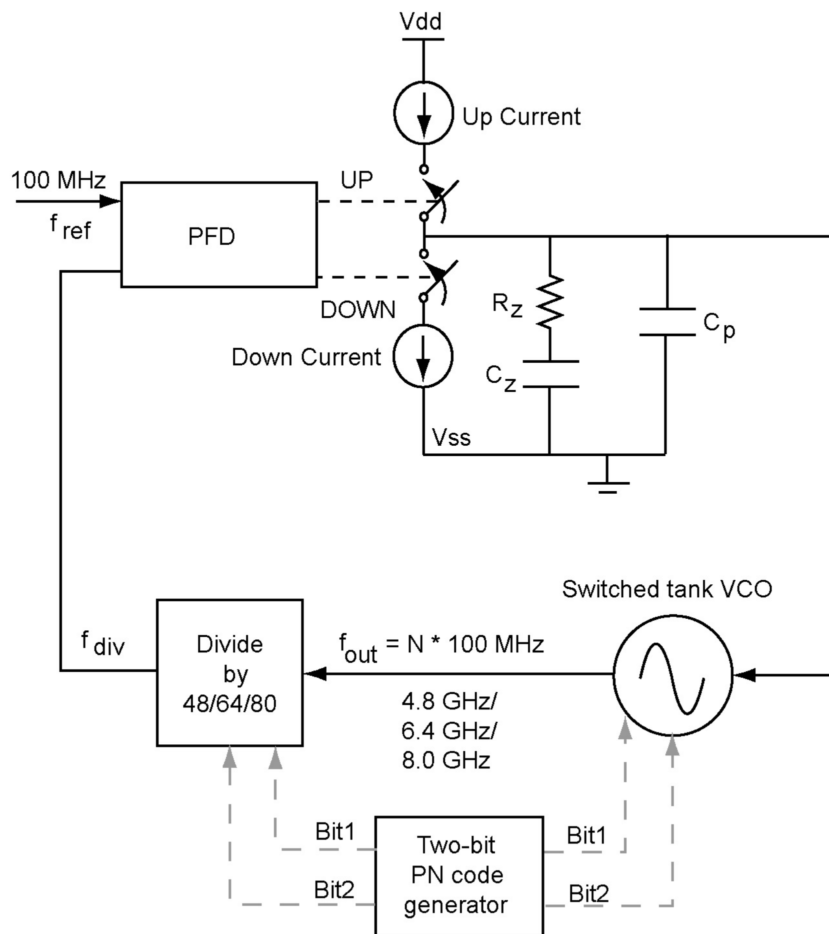


Figure 5.5: Block-level schematic of the PLL-based frequency synthesizer.

related to the applied varactor control voltage, i.e. the higher the voltage, the lower the capacitance and thus the higher the VCO output frequency. When the phase of f_{ref} leads f_{div}, the capacitor is charged up by the current from the PMOS current source. Thus, the control voltage (V_c) provided to the VCO increases, which in turn increases the output frequency of the VCO. Conversely, when the phase of f_{ref} lags f_{div}, the capacitor is discharged by the NMOS current source resulting in a decrease of the control voltage which decreases the frequency output of the VCO. Once f_{div} equals f_{ref} (and they are in-phase), the PLL settles providing a stable output until the next instant when the phase or frequency of f_{div} deviates from f_{ref}.

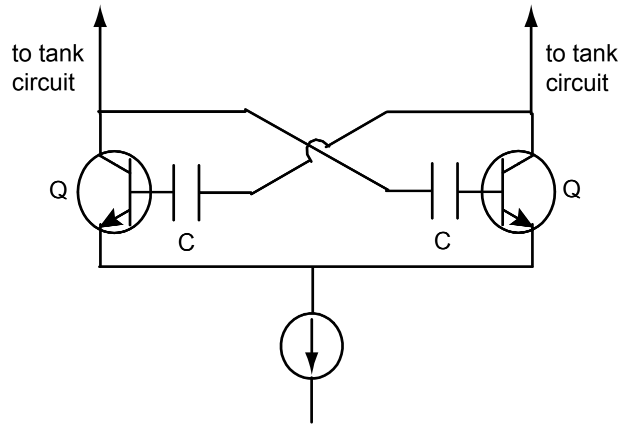
Figure 5.6 shows the schematic representation of the switched-tank VCO design implemented for the UWB transmitter. The VCO is based on a negative -G_m amplifier circuit formed by SiGe HBTs in the active circuit [refer to Figure 5.6(a)]. The amplification provided by this active circuit is necessary to cancel the loss through the tank circuit [75]. In this design, the tank circuit of the VCO consists of three different capacitive states that correspond to three different frequency outputs (4.8, 6.4, and 8.0 GHz) [refer to Figure 5.6(b)]. The three capacitor configurations consist of fixed capacitances (formed by MIM capacitors) for coarse-tuning from one frequency band to another, and tunable capacitances (formed by varactors) for fine-tuning the frequency under PLL control within a single frequency band. The switching between the three different capacitive states of the VCO tank circuit is controlled by CMOS switches. The control voltage, V_c at the output of the PLL passive loop filter is the tuning voltage of varactors. The tuning gain of the VCO is given by

$$K_{vco} = \frac{\Delta f_0}{\Delta V_c} \tag{5.1}$$

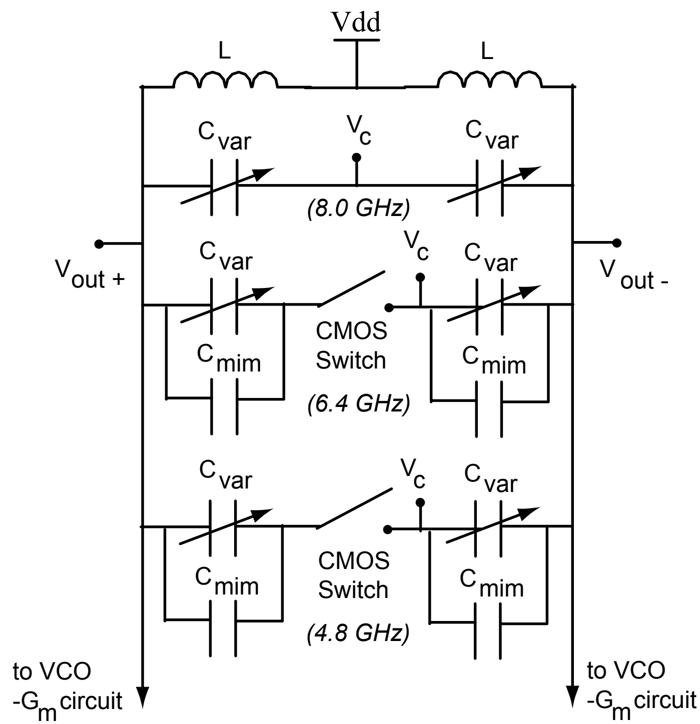
where Δf_0 is the change in VCO center frequency for a given ΔV_c on the varactor control line. However, the effective tuning gain in the PLL will be reduced by the dividing factor (N) of the divider. The effective tuning gain will then be given by

$$K_{vco,eff} = \frac{K_{vco}}{N}. \tag{5.2}$$

Pseudorandom output frequency values can be generated by switching the divider ratio of the frequency divider and the tank circuit capacitance of the VCO simultane-



(a)



(b)

Figure 5.6: Schematic representation of (a) VCO -G_m circuit; (b) VCO switched tank circuit with three capacitor banks controlled by CMOS switches.

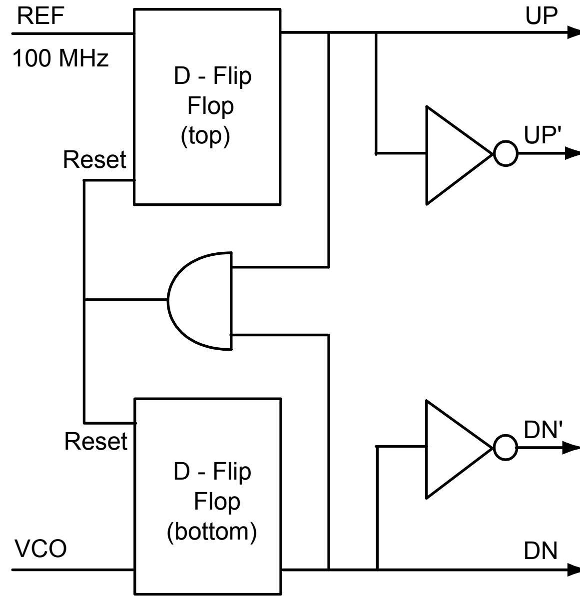


Figure 5.7: Schematic of the CMOS phase/frequency detector.

ously using a simple PN code generator. In this design, the divider ratio N can take on one of three values — 48, 64 and 80 corresponding to VCO output frequencies of 4.8, 6.4 and 8.0 GHz, respectively. A two-bit PN code generator was used to control the switching between different frequency states. The following subsection gives the complete schematic and simulation results of the CMOS phase/frequency detector. An on-chip passive loop filter was designed to realize a third order, type-2 charge pump PLL. The loop filter design will be explained further in subsection 5.4.2. Other components of the transmitter were implemented by the other team members. All the simulations were carried out using Cadence's Spectre RF tool.

5.4.1 Design of CMOS phase/frequency detector and simulation results

The schematic of phase/frequency detector designed during the course of this thesis work is shown in Figure 5.7. This PFD was designed in the core CMOS technology of Motorola's (now Freescale) HiP6WRF low-voltage 0.18-μm Si/SiGe BiCMOS process and was based on the topology described in [76].

Two positive edge-triggered D-flip flops (D-FF) are the main components of this phase/frequency detector design. The 100 MHz reference signal is supplied as an input to one of the D-flip flops while the other flip-flop is supplied with the divided output of the VCO. Each flip-flop gives a high (1) output when it detects a positive going edge at its input. When f_{ref} lags f_{div} in phase, the pulse width of the down (DN) pulses are much greater than those of the up (UP) pulses. This is because the bottom D-FF senses a positive going edge before the top D-FF. As soon as the top D-FF senses a positive edge at its input, the AND gate output goes high and resets both the flip-flops (refer to the simulated PFD output in Figure 5.8). The UP pulses are thus seen as very narrow pulses at the output of top D-FF. The DN pulses connect the NMOS current source of the charge pump into the circuit, discharging the loop filter capacitance and resulting in an average decrease in control voltage provided to the VCO. This decreases the frequency output from the VCO. Conversely, when f_{ref} leads f_{div} in phase, the PFD provides longer UP pulses and narrow DN pulses which on average connects the PMOS current source of charge pump into the circuit. This charges up the loop filter capacitance, and the control voltage provided to the VCO increases causing the VCO to increase its output frequency. The simulated PFD output in this case is shown in Figure 5.9.

When both the inputs to the D- flip flops are equal in phase and frequency, the output is a series of very narrow and equal-sized pulses at both UP and DN outputs. These narrow pulses are due to the delay in the feedback AND circuit. When both UP and DN are simultaneously high, the output of AND gate goes high and resets both the flip-flops. The above described PFD has a linear phase-tracking range of $\pm 360°(\pm 2\pi)$ and can therefore help the PLL settle with a zero phase offset. A larger linear range of phase-tracking in a PFD results in lower final phase offset in the PLL [77]. The gain of the phase detector and charge pump is given by

$$K_p = \frac{I_p}{\Delta\phi} \tag{5.3}$$

where I_p is the charge pump output current and $\Delta\phi$ is the total input change in phase (2π radians in this case).

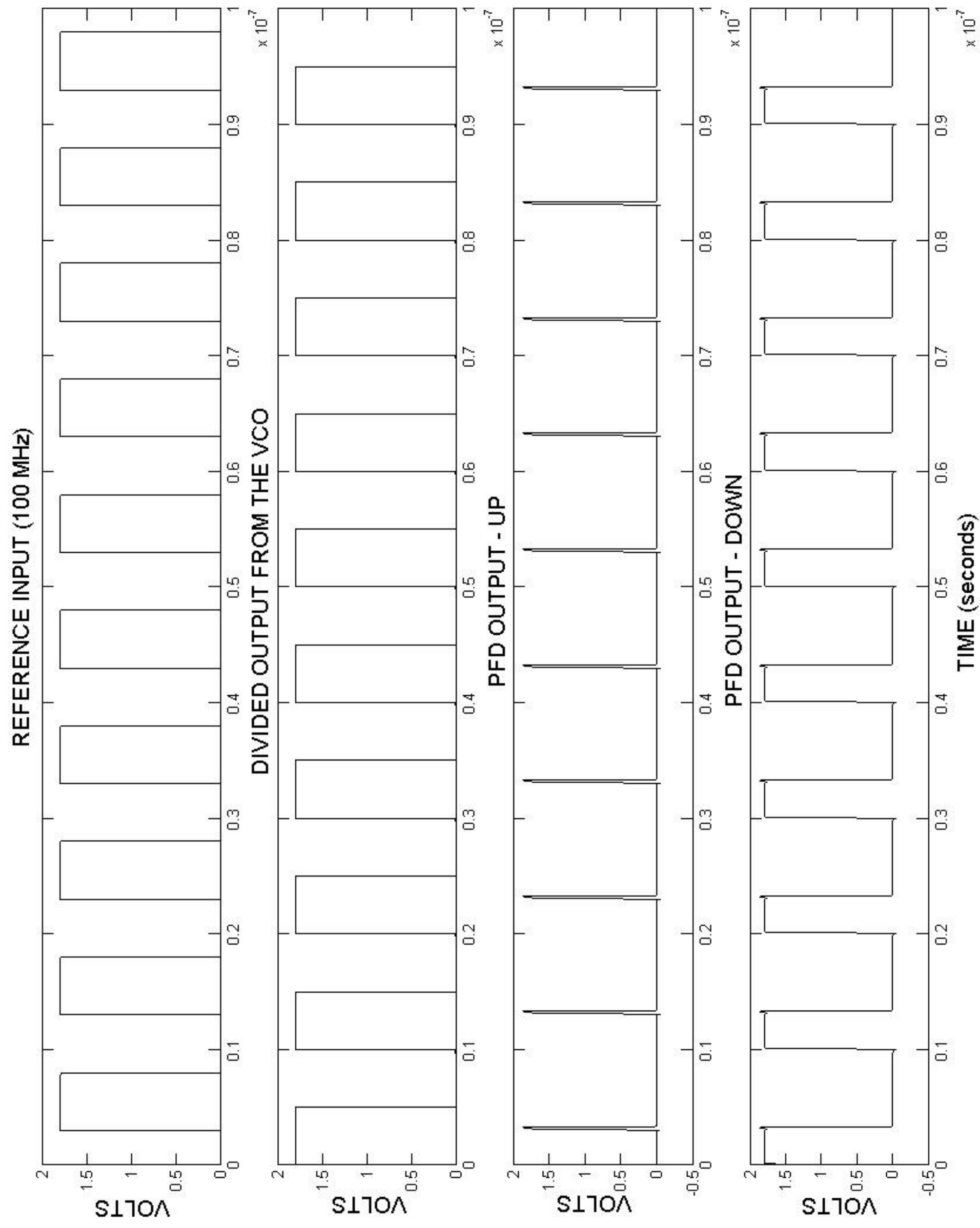


Figure 5.8: Simulated output of the CMOS phase/frequency detector when reference input lags the divided VCO output.

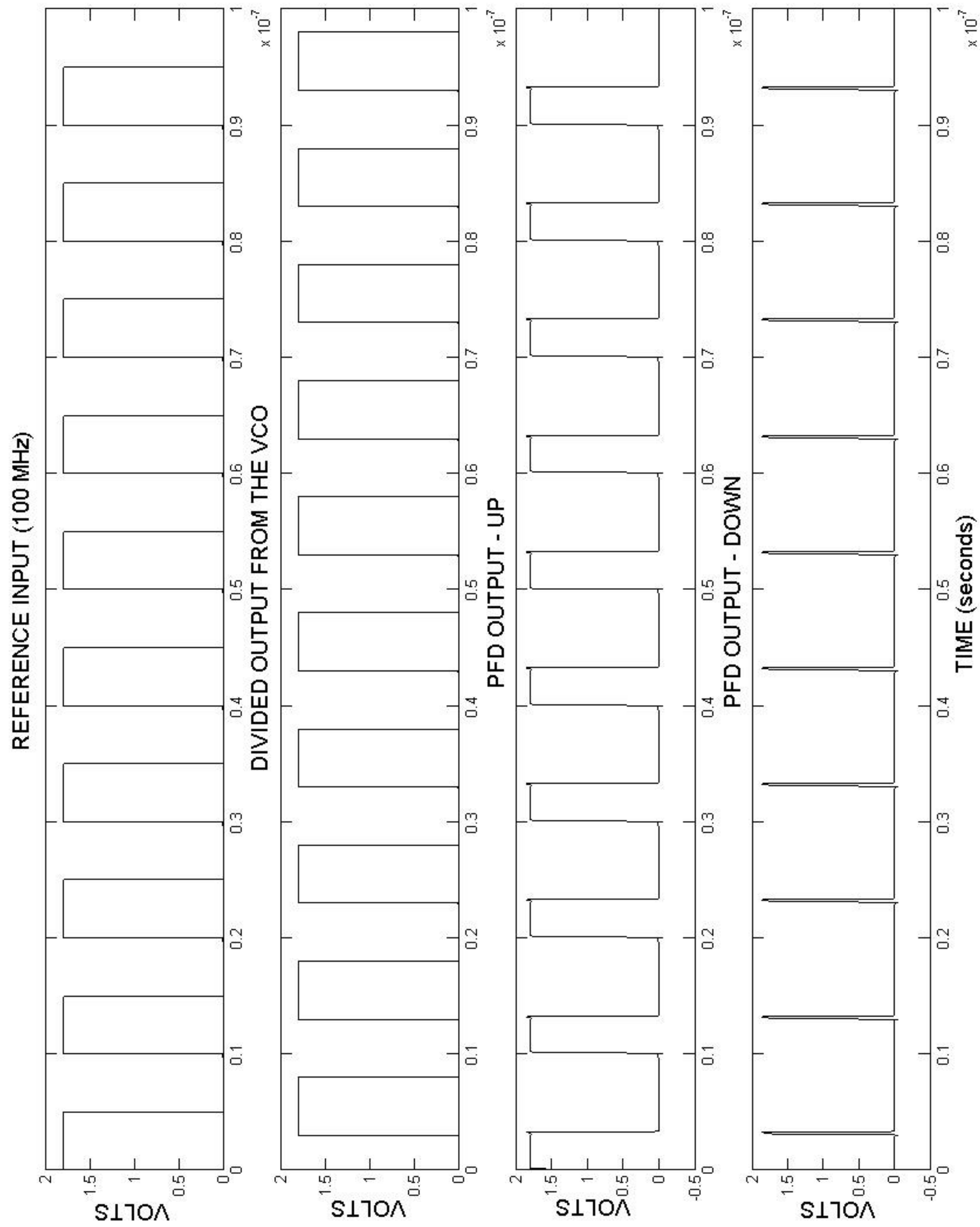


Figure 5.9: Simulated output of the CMOS phase/frequency detector when reference input leads the divided VCO output.

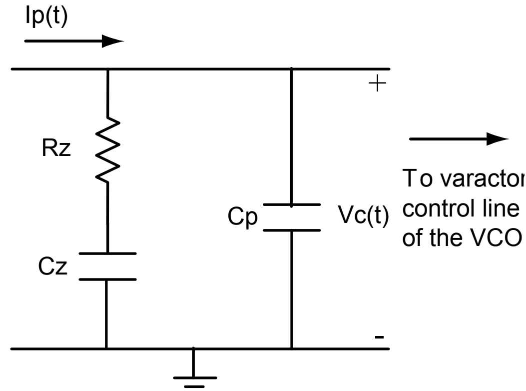


Figure 5.10: Schematic of the third order on-chip passive loop filter design.

5.4.2 Theory and design of on-chip passive loop filter

The loop filter is perhaps the most critical component in a phase-locked loop. It determines the performance and stability of the entire PLL [77]. The choice of loop filter also determines the order and type of the PLL. The two types of loop filters are active and passive loop filters. Active loop filters have greater design complexity and will consume a relatively larger amount of power. In addition, active loop filters may introduce undesired noise in the PLL. On the other hand, charge pump PLLs with passive loop filters are widely preferred for frequency synthesizers because they are simple to design and consume less power. The gain of the loop filter is denoted by K_{LF} and the transfer function is denoted by F(s). Ideally, in case of a passive loop filter the gain, $K_{LF} = 1$. The open-loop transfer function of a PLL is given by

$$G(s) = \frac{KF(s)}{s} \tag{5.4}$$

where K = $K_p \cdot K_{vco,eff} \cdot K_{LF}$. The highest power of the variable s (s=$j\omega$, where ω is the frequency in radians/sec) in the denominator of G(s) denotes the total number of poles in the PLL system and the highest power of the variable s in the numerator denotes the total number of zeroes in the system. The total number of poles in the open-loop transfer function of the PLL determines the order of the PLL, while the number of poles at zero frequency (s=0) determines the type of the PLL [77].

Figure 5.10 shows the configuration of the passive loop filter designed for the PLL-

frequency synthesizer of the UWB transmitter. The transfer function of this loop filter is given by:

$$F(s) = \frac{1 + s\tau_z}{s \cdot (C_z + C_p)\,(1 + s\tau_p)} \tag{5.5}$$

where,

$$\tau_z = (R_z \cdot C_z), \tag{5.6}$$

the zero of the PLL, and

$$\tau_p = 1/\omega_p = R_z \cdot \left(\frac{C_z \cdot C_p}{C_z + C_p} \right), \tag{5.7}$$

the pole of PLL. Therefore, the zero frequency is given by $\omega_z = 1/\tau_z$ and the pole frequency is given by $\omega_p = 1/\tau_p$. The overall open-loop transfer function of the PLL is therefore given by:

$$G(s) = K_p \cdot K_{vcoeff} \cdot K_{LF} \cdot \frac{1 + s\tau_z}{s^2 \cdot (C_z + C_p)\,(1 + s\tau_p)}. \tag{5.8}$$

Using the equations 5.2 and 5.3, the expression for G(s) can be rewritten as:

$$G(s) = \frac{I_p \cdot K_{vco}}{2\pi \cdot N} \cdot \frac{1 + s\tau_z}{s^2 \cdot (C_z + C_p)\,(1 + s\tau_p)}. \tag{5.9}$$

It can be seen from the above equation that the loop filter is a third order passive filter and the type the PLL is 2 (total number of poles = 3, and number of poles at zero frequency = 2). The loop filter shown in Figure 5.10 results in a higher order PLL and therefore spurious suppression capabilities are better than in lower order PLLs [78]. If N is the dividing ratio of the frequency divider, the crossover frequency of the open loop gain of the PLL (also bandwidth of the PLL), ω_c can be defined by:

$$\omega_c = \frac{I_p \cdot K_{vco} \cdot R_z}{2\pi \cdot N} \cdot \frac{C_z}{C_z + C_p} \tag{5.10}$$

The crossover frequency can also be defined as the frequency where the open loop gain of the PLL becomes unity (or magnitude of open loop gain = 0dB). The above expression for crossover frequency can be obtained when equation 5.9 becomes unity. As a general rule of thumb, the zero (equation 5.6) should be placed at one third of the crossover frequency and the pole (5.7) at three times the crossover frequency. This placement guarantees a sufficient phase margin for good loop stability [74]. The design of loop filter for the multi-band UWB transmitter was carried out based on the above theory and general design principles described in [79]. The phase margin of the loop is given by:

$$PM = \tan^{-1}(\tau_z \omega_c) - \tan^{-1}\left(\frac{\tau_z \omega_c}{b+1}\right) \tag{5.11}$$

where $b = C_z/C_p$. The most common measure of stability of a PLL is the phase margin. Unity loop gain and a 360° excess phase shift can lead to oscillations in a loop (Barkhausen criteria) [77]. The gain and phase margins relative to this pair of conditions can therefore be used as a measure of stability. Phase margin is the additional open-loop phase shift necessary to give 180° phase when the open-loop gain is unity. By differentiating equation 5.11 with respect to ω_c it can be shown that the maximum phase margin is achieved when

$$\omega_c = \frac{\sqrt{(b+1)}}{\tau_z}, \tag{5.12}$$

with a corresponding maximum phase margin of

$$PM_{MAX} = \tan^{-1}\left(\sqrt{(b+1)}\right) - \tan^{-1}\left(\frac{1}{\sqrt{(b+1)}}\right). \tag{5.13}$$

It can be seen from the above equation that the maximum phase margin is a function of the ratio of C_z and C_p. When ω_c is set to the value given in equation 5.12, a new relationship can be derived from equation 5.10:

$$\frac{I_p \cdot K_{vco}}{2\pi \cdot N} \cdot \left(\frac{b}{b+1}\right) = \frac{C_z}{\tau_z^2} \cdot \sqrt{b+1}. \tag{5.14}$$

Parameters	Values
Phase Margin	62°
ω_c	$2\pi \cdot 4$ MHz
Charge pump current, I_p	$250\mu A$
b (ratio of capacitors)	15
K_{vco}	$6.0 \times 10^9 radians/\sec/V$
C_z	18.72 pF
C_p	1.24 pF
R_z	8.5 KΩ

Table 5.1: Calculated parameters for the PLL frequency synthsizer.

Using the equations 5.6, 5.7, 5.12, 5.13, and 5.14, an appropriate on-chip passive loop filter was designed for the multi-band UWB transmitter in this work. The charge pump was designed for an output current of $250\mu A$ and the VCO was designed for an approximate gain of 6.0×10^9 radians/sec/V ($\sim 1GHz/V$). The VCO was designed to have approximately equal K_{vco} values over the three different frequency bands (4.8 GHz, 6.4 GHz and 8.0 GHz). The PLL was intended to have an acquisition time of less than $1\mu s$. To attain such short acquisition time, the PLL was required to have a reasonably large bandwidth since acquisition time decreases with increasing bandwidth [77]. A very high bandwidth results in poor noise (phase noise) performance and thus will result in undesired jitters in the PLL. Therefore, an intermediate choice of bandwidth (or crossover frequency) of 4 MHz was made. It is recommended that a PLL have a phase margin of over 60°; this value of phase margin provides better loop stability. Giving adequate consideration to the parasitic impedances in a fabricated IC, a choice of 62° phase margin was made for designing the loop filter.

As indicated by equation 5.13, the phase margin of the PLL is essentially determined by the ratio of capacitors in the loop filter. For a phase margin of 62°, the ratio ($b = C_z/C_p$) of capacitors should be 15. From equation 5.12, the value of τ_z was calculated to be 1.591 $\times 10^{-7}$ seconds. Then, using equation 5.14, the value of C_z was determined to be 18.72 pF. Since b = 15, the value of C_p was found to be 1.248 pF. Using equation 5.6, the value of R_z was determined to be 8.5 KΩ. Table 5.1 summarizes the calculated parameters for the design of the PLL frequency synthesizer in this work.

Using the parameters listed in Table 5.1 in equation 5.9, the open loop gain of the

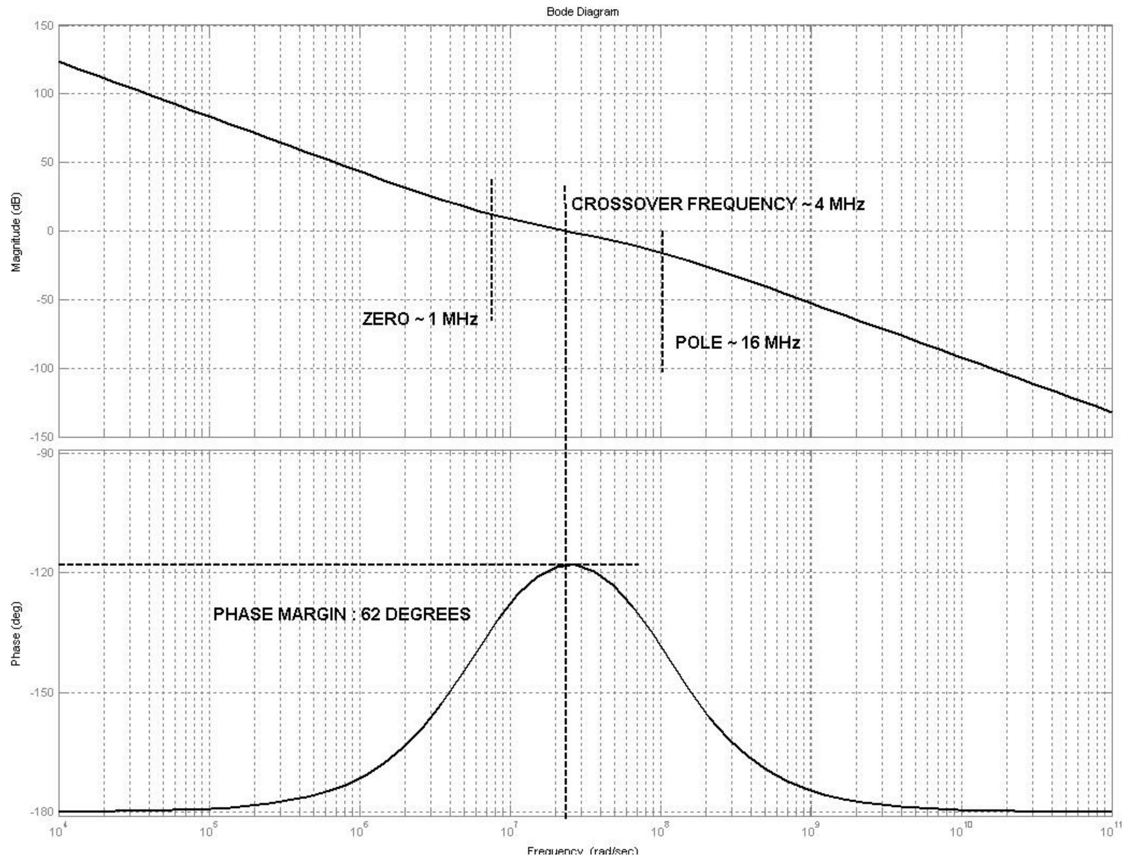


Figure 5.11: Magnitude and phase of open loop gain, G(s) of the PLL.

PLL was plotted using MATLAB. The plot of the magnitude and phase of G(s) of the PLL in the 8.0 GHz frequency band is shown in Figure 5.11. It can be verified from the plot that the phase margin of the PLL is approximately 62°. The zero frequency (1 MHz), the pole frequency (16 MHz) and the crossover frequency (4 MHz) are also shown in the same plot.

5.4.3 Design of pseudorandom code generator

A pseudorandom code (also known as pseudonoise) generator is generally used in spread spectrum communication systems during data transmission and reception. As mentioned in Chapter 1, in a direct sequence spread spectrum system, the PN code generator spreads the information spectrum by multiplying the baseband data

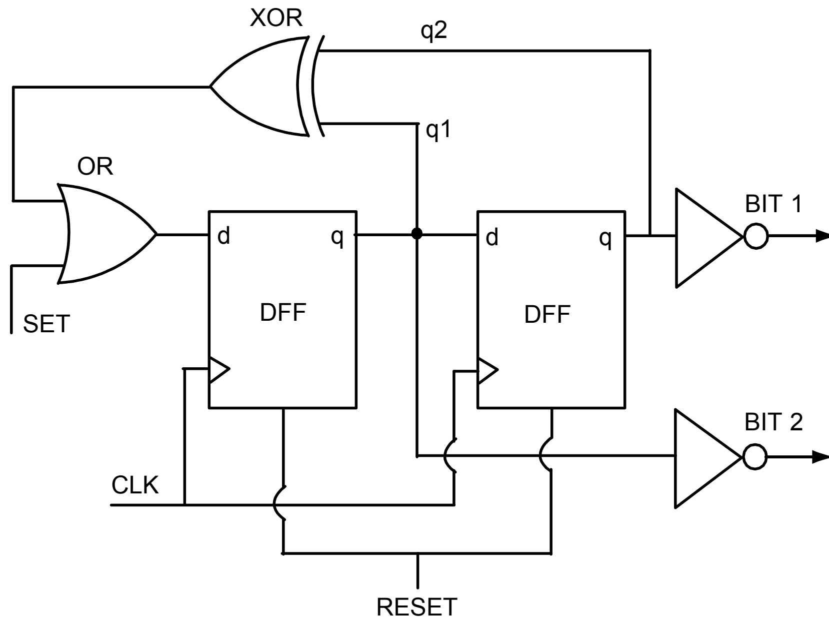


Figure 5.12: Schematic of CMOS pseudorandom code generator.

pulses with the code sequence. On the other hand, in a frequency hopped spread spectrum (or multiband-hopped) system, the PN code generator is used to determine the carrier frequency values.

A pseudorandom sequence is a periodic binary sequence that is usually generated by a feedback shift register. The feedback shift register contains a series of flip-flops (the number of flip-flops being m) based on the number of bits required in the pseudorandom code to be generated. These flip-flops are connected to a feedback logic circuit, the output of which is fed back to the first flip-flop. Each flip-flop is controlled by a clock signal. At each pulse of the clock, the state of each flip-flop is shifted to the next one down the line. Based on the *length* m of the shift register, the initial state of each flip-flop and the feedback logic circuit, the output of the PN code generator forms a particular pseudorandom sequence. The result is then fed back as the input to the first flip-flop, thereby preventing the shift register from emptying.

Figure 5.12 shows the schematic of a simple CMOS PN code generator designed during this thesis work as a part of the multi-band UWB transmitter. The UWB transmitter operates only in three different frequency bands and hence only requires a two-bit PN code sequence to control the switching between the bands. As shown

in the figure, the feedback circuit is formed by a simple XOR logic gate. If the initial state of the first flip-flop is “0” (or low), the shift register will always be empty and no code (or a code containing only 0s) will be produced. For this reason, the initial-state of the first flip-flop must be set to “1” (or high) using the OR gate. Such feedback shift registers which do not permit a 0-output state are said to be *linear* [47]. In this design, the value of SET provided to the OR gate is 1 until the first clock pulse of the D-FFs.

At the first clock pulse, the information from the first flip-flop is transferred to the XOR gate and to the input of the second flip-flop, i.e. Bit2 = 0 and Bit1 = 1 (output of D-FFs inverted using a CMOS inverter). Now, the output of the XOR gate is high. At the second clock pulse, the output of the both the flip-flops go high, with both the output bits going 0. The output of XOR gate then goes low since both the flip-flops are in high-state. During the third clock pulse, the output of first flip-flop becomes 0 and that of the second flip-flop remains 1. The output bits in this case are 1 (Bit2) and 0 (Bit1). Therefore, the output bits take the values 01, 00 and 10 for every three clock periods. This process keeps repeating to produce codes in a pseudorandom fashion. However, this simple PN code generator can produce only a single code and additional logic circuits are required to incorporate more users. The initial value of the second flip-flop alone could be set to 1 to produce a different code. Alternatively, initial values of both the flip-flops could be simultaneously set to 1 to produce a third variation in the code.

Simulation results for the CMOS PN code generator are shown in Figure 5.13. The PN code generator operates at a clock frequency of 1 MHz (or $1\mu s$ clock period). It can be seen that the output bits (Bit1 and Bit2), form a pseudorandom sequence. Each of the states (“00”,“01” and “10”) are used to control the switching of the tank circuit capacitances of the VCO. The three different tank circuit states correspond to 4.8 GHz, 6.4 GHz and 8.0 GHz. When additional frequency bands are incorporated, the length of the PN code will be increased (i.e. the number of output bits must be increased).

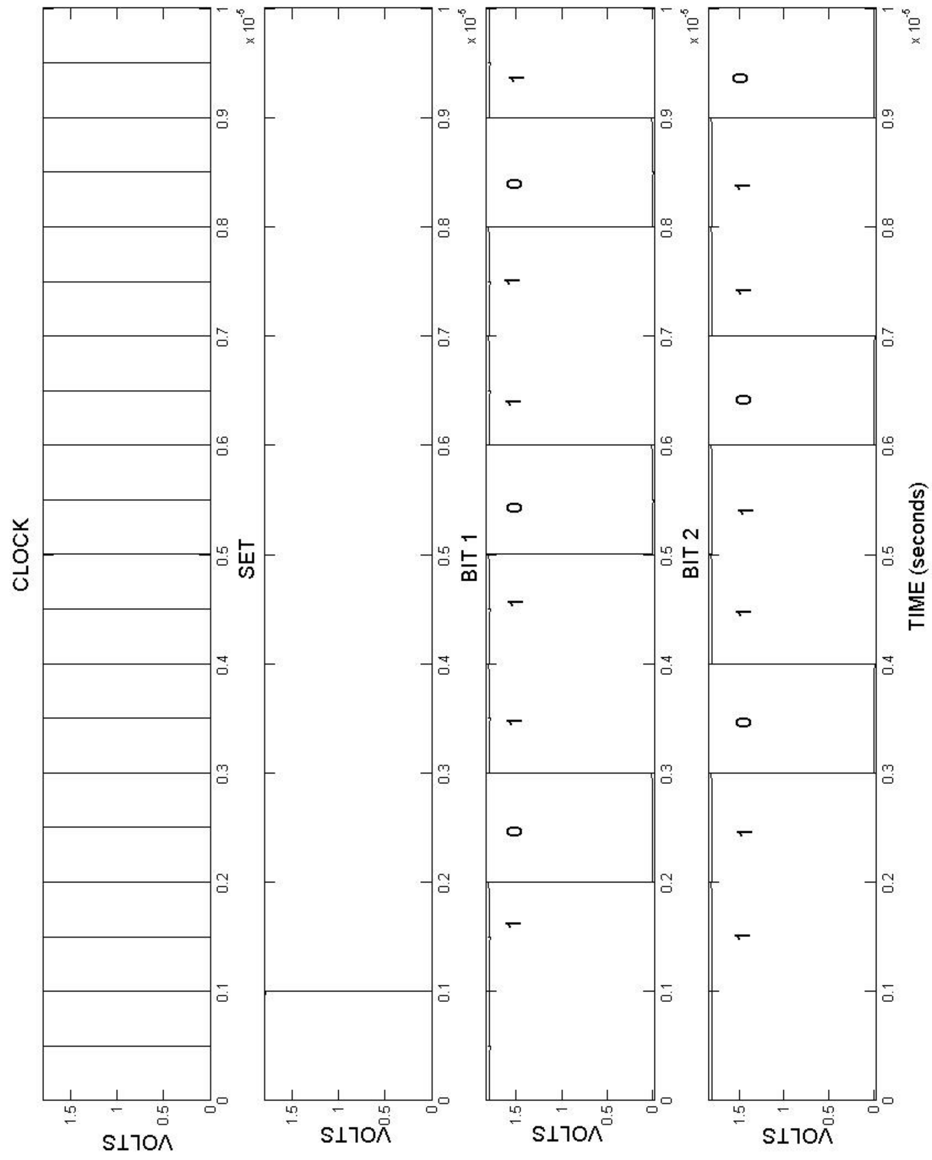


Figure 5.13: Simulation results of the CMOS PN code generator.

5.4.4 Simulation results of the PLL frequency synthesizer

The simulation of the PLL frequency synthesizer incorporating the above CMOS PFD, CMOS pseudo-random code generator, and on-chip passive loop filter designs was performed using Cadence Spectre RF. The control voltage provided to the VCO versus time is shown in Figure 5.14. It can be seen that the PLL locks within 700 ns in all three frequency bands. Figure 5.15 shows the simulated performance of the PLL in the 8.0 GHz frequency band. The output frequency of the VCO is shown along with the 100 MHz input reference to the PLL. It can be observed that the PLL settles with a near-zero-phase and frequency offset. Appendix A describes the procedure used in this thesis to simulate the PLL frequency synthesizer.

5.5 Layout of the multi-band ultra-wideband transmitter

The layout of the multi-band UWB transmitter (Figure 5.16) was performed using the Cadence Virtuoso tool. The dashed boxes in the figure indicated the major sub-blocks of the transmitter: (1) PFD, charge pump and loop filter; (2) lock detector; (3) pulse generator; and (4) switched-tank VCO. The area of the fabricated chip is 1mm $\times$ 1.5mm. The power dissipation of the whole chip was estimated to be approximately 40mW. The components that consume the most significant fraction of power are the prescaler-divider network and the VCO. Future design iterations will seek to reduce these contributions. Table 5.2 gives the list of pins on the chip along with their respective functions. A micrograph of the fabricated multi-band ultra-wideband transmitter is shown in Figure 5.17.

The main features of the layout are as follows:

- Separation of sensitive RF circuits such as the VCO and the pulse generator from the rest of the chip using an isolation wall. This isolation wall is built by stacking multiple metal layers (M1-M3) and connecting all these layers to the substrate through vias. This wall is ultimately connected to separate ground pins to protect the RF circuits from noise and voltage supply fluctuations in the rest of the chip.

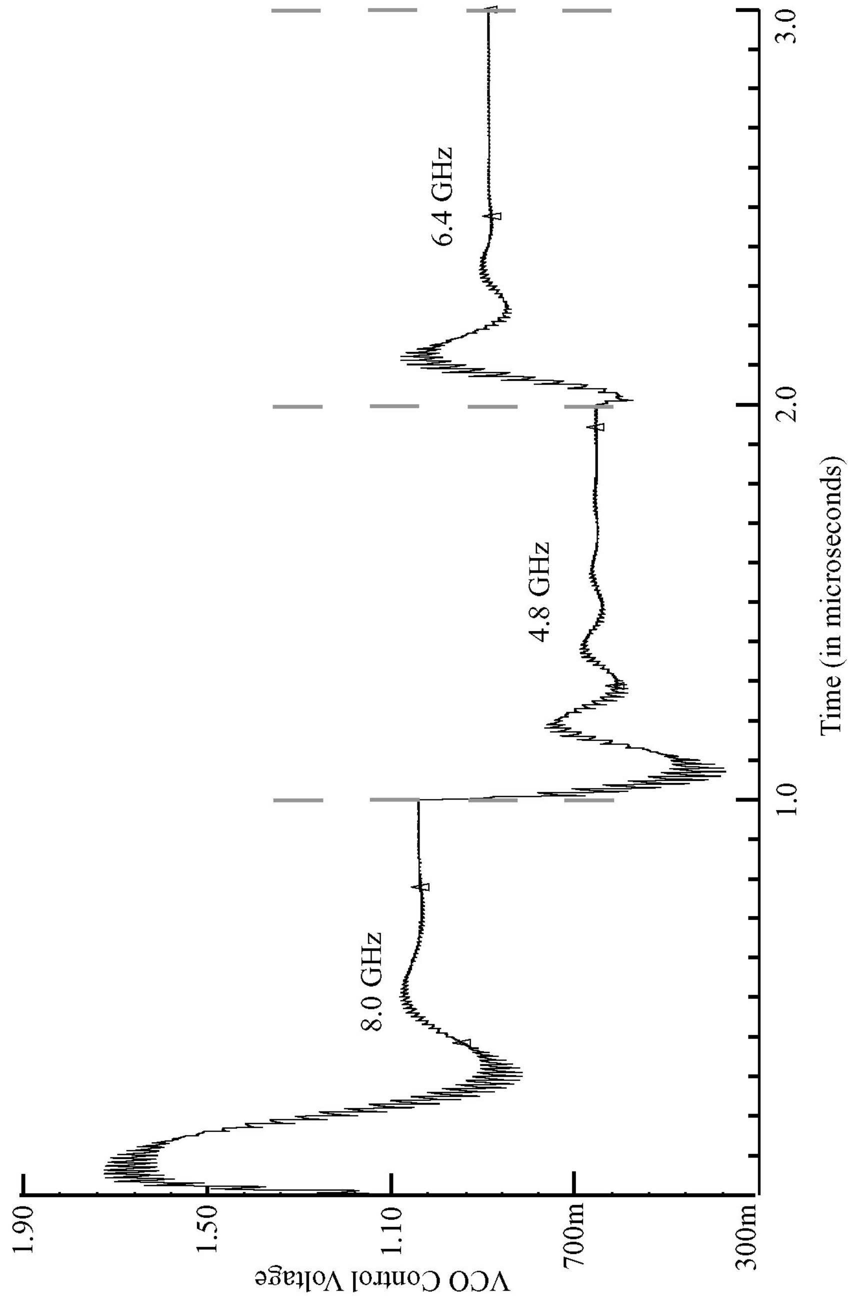


Figure 5.14: Simulation results of the UWB PLL frequency synthesizer showing the variation of control voltage provided to the VCO. The frequency bands are switched every $1\mu s$ to show operation in all three frequency bands.

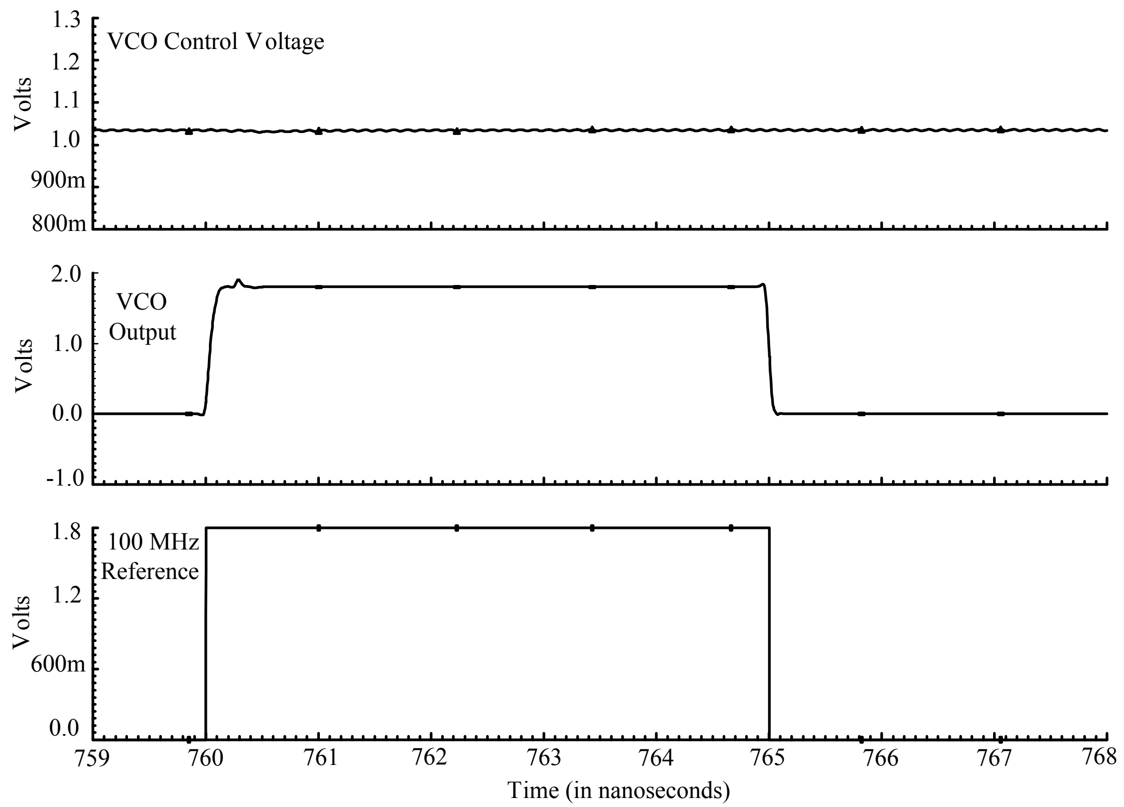


Figure 5.15: Simulation results of the UWB PLL frequency synthesizer in 8 GHz band showing the stabilization of PLL. The PLL settles with zero-phase and frequency offset.

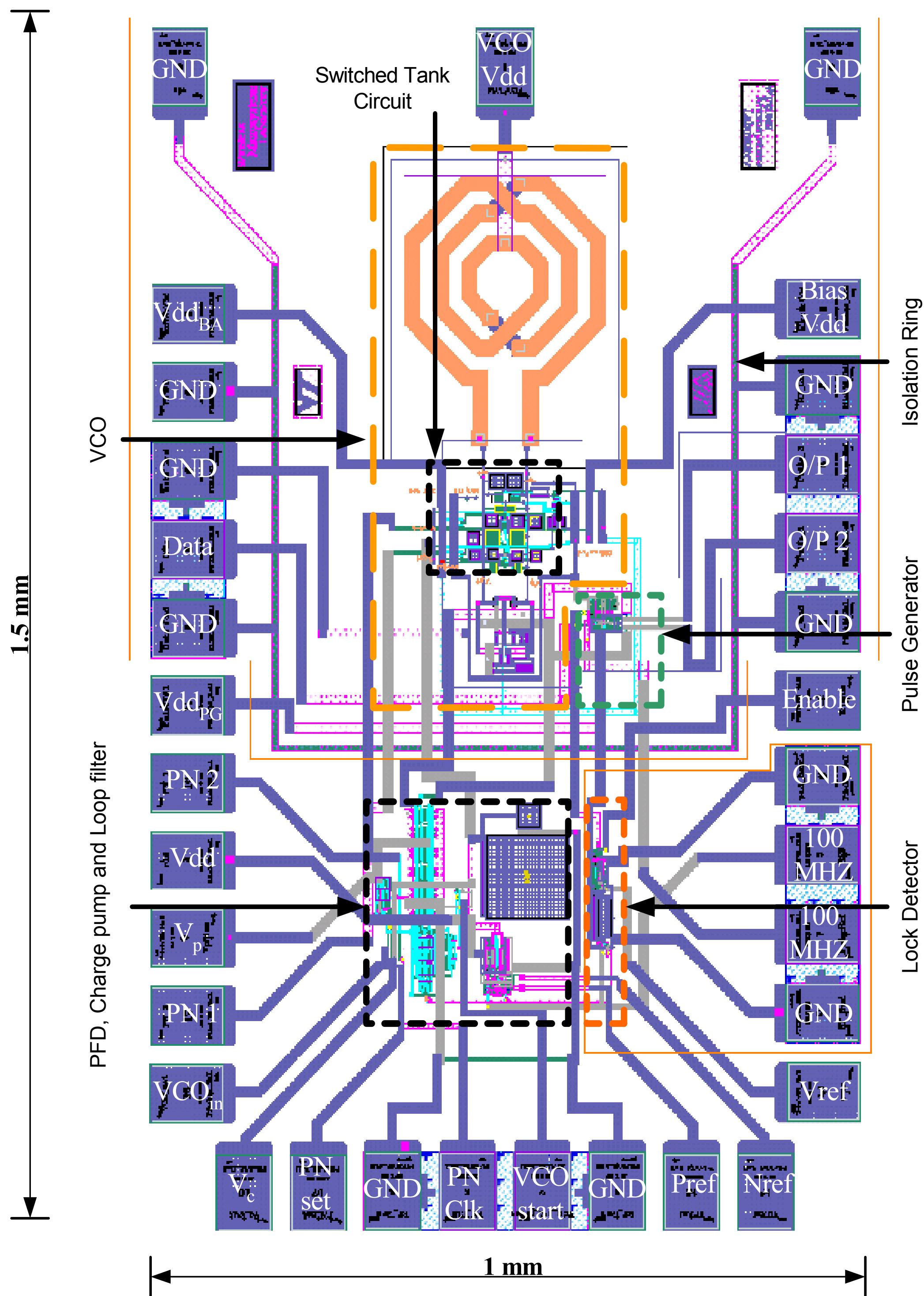


Figure 5.16: Layout of the ultra-wideband transmitter designed for the 2003 Motorola Wireless and Beyond Design Exposition. Estimated die size — 1mm by 1.5mm.

Pin	Details
100 MHz	Crystal reference inputs — one for the PFD and another for the pulse generator
Vdd	1.8 volts supply for the PLL and its associated circuitry
Bias Vdd	1.8 volts supply for the bias circuit of the VCO
Vdd_{BA}	1.8 volts supply for the buffer amplifier circuit
Vdd_{PG}	1.8 volts supply for pulse generator and the lock detector circuits
VCO Vdd	1.8 volts supply voltage for the VCO's tank circuit
V_p	1.8 volts supply to the bias circuit of the prescaler
Data	Data input to the UWB transmitter
O/P 1 and O/P 2	Output of the UWB transmitter
Enable	Enable input of the lock detector
Vref	Reference voltage input to the lock detector
Nref	Reference voltage input of the NMOS current source of the charge pump
Pref	Reference voltage input of the PMOS current source of the charge pump
VCO start	Clock for setting initial state of the control voltage to the VCO
PN Clk	Clock for the CMOS PN code generator
PN Set	Initial input to the shift register of the PN code generator
V_c	Output pin for observing the control voltage to the VCO
VCO_{in}	Initial state of the control voltage to the VCO
PN1	Control input to the switches of the VCO tank circuit (Bit1)
PN2	Control input to the switches of the VCO tank circuit (Bit2)
GND	Substrate ground — Separate pins for the PLL, the lock detector and the rest of the chip

Table 5.2: Pin assignments for the ultra-wideband transmitter.

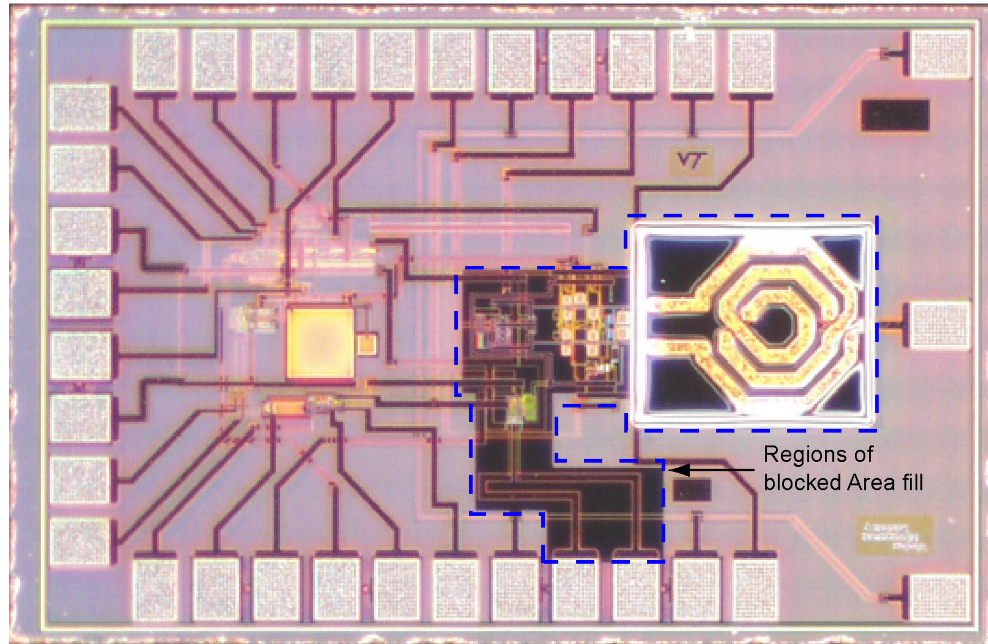


Figure 5.17: Micrograph of the UWB transmitter chip (1.5mm × 1.0mm) fabricated in Motorola's HiP6WRF BiCMOS process.

- Individual VDD and GND pins for the VCO, the pulse generator, the buffer amplifier and, the rest of the transmitter chip. This provides troubleshooting capability in the event particular components do not operate as expected.

- Separate pins for the voltage references in the charge pump's current sources to give external control over the operation of the charge pump for troubleshooting purposes. These pins can be used to provide higher supply voltage (VDD) in case the charge pump's output current has to be increased to enable the PLL to lock. Similarly, separate pins were provided for voltage supply of the bias circuits of the prescaler and the VCO.

- Two input pins for overriding the PN code generator. These pins can be used to bypass the PN code generator to allow direct control of the switching of the VCO capacitor states and the divider network.

- Area fill is a requirement for regions of stacked metal layers throughout the chip (around circuit component layouts) to improve reliability of CMP processing of the fabricated chip. As shown in Figure 5.17, the area fill around the RF

circuits of the transmitter was blocked to protect these sensitive components from potential signal degradation due to these area fill metal layers.

5.6 Chapter summary

This chapter has presented the design of specific components of the multi-band UWB transmitter developed for the 2003 Motorola Wireless and Beyond Design Exposition — namely the CMOS PFD, the on-chip loop filter, and the CMOS pseudorandom code generator. The overall layout of the transmitter chip was also discussed. As proposed in [80], the present transmitter architecture, described in section 5.3, can be integrated with on-chip sensors, an analog to digital converter and a potentially a high efficiency power amplifier to develop a complete transmitter in ultra-wideband technology. In addition, the number of frequency bands of operation should be increased to support multiple access in larger wireless sensor network applications.

Chapter 6

Conclusion and Future work

The objective of this thesis was the development of an integration platform for functionalized nanosensors in order to realize low-power multifunctional wireless sensor nodes. The work in this thesis has focused on two promising technologies, namely dielectrophoretic assembly of nanostructures and ultra-wideband data communications. The dielectrophoretic assembly technique offers a potentially low-cost and highly manufacturable approach for integration of diverse nanosensor devices into CMOS ICs incorporating sensor readout, signal processing and communications functionalities. Ultra-wideband signalling offers significant advantages for wireless sensor networks, and the design of prototype multiband ultra-wideband transmitter was also pursued in this work. This chapter summarizes the significant findings of this work and suggests future research directions.

6.1 Conclusion

6.1.1 Dielectrophoretic assembly of metallic nanowires onto CMOS circuits

The first goal of this thesis was the development of a post-IC assembly technique for the integration of functional nanostructures with standard CMOS circuitry. This integration platform was based on the dielectrophoretic assembly technique. A DEP

assembly test chip was designed and fabricated using the five-metal CMOS platform technology of Motorola's HiP6W low-voltage 0.18μm Si/SiGe BiCMOS process. The overall chip size was ~2.5mm × 2.5 mm. The multiple metal layers available in this process were leveraged to define the excitation and assembly electrodes required for the post-IC assembly of nanowires. The assembly (top) electrodes were defined in the M5 layer and the excitation (bottom) electrodes in the M4 layer. The protective passivation layer covering the chip was selectively opened over the assembly electrode areas to enable the assembly of nanowires. The AC signal required to facilitate nanowire assembly was provided to the bottom electrodes via I/O contact pads. This signal was then capacitively coupled to the assembly electrodes. The placement and alignment of the nanowires on the top electrodes are defined by dielectrophoretic forces that act on the nanowires. For proof of concept purposes, metallic rhodium nanowires (L = 5μm and D = 250 nm) were assembled onto the CMOS test chips using this technique.

In the HiP6W process, aluminum and tantalum capping layers are deposited in the passivation openings as part of the normal I/O pad fabrication process. These layers were removed using two different final step etching techniques. Initially, the capping layers were etched using a foundry dry etch process. However, this resulted in a loss of planarity of the M5 layer, resulting in corrosion (oxidation) of the exposed copper of the M5 layer. Consequently, the nanowires assembled on these M5 electrodes did not show electrical continuity. Subsequently, the capping layer was etched using an in-house custom-wet etch process. This process maintained planarity of the M5 layer and did not result in oxidation ridges at the edges of the M5 layer. Good electrical continuity between the top assembly electrodes and the assembled nanowire was subsequently demonstrated. However, since the contact area between the cylindrical nanorod and the top electrodes is much less than the cross-sectional area of the rod itself, the flow of carriers into and out of the nanorod was constricted, resulting in a higher-measured resistance than predicted. Based on these experiments it is concluded that maintaining CMP planarized layers is critical to avoid corrosion of exposed edges of the top metal assembly electrodes, which in turn allows good electrical continuity with the assembled nanowire.

To demonstrate integration of nanowires with CMOS operating circuitry, assembly experiments were performed on sites connected to a simple readout circuit to measure

the resistance of the assembled nanowires. This circuit consisted of a simple Wheatstone bridge network connected to a two-stage CMOS differential amplifier. However, nanowire assembly was not successfully achieved on sites connected to these circuits. It was concluded that there was a degradation in electric field intensity at the assembly electrodes due to a short circuit path through the readout circuitry. In this case, the relatively high assembly voltage magnitudes resulted in gate rupture of the input NMOS transistors of the readout circuit, which in turn created short circuit paths to ground.

The assembly chip layout also included designs without pre-existing interconnects between assembly sites and circuitry. In these designs, assembly sites were initially electrically isolated from the circuitry and required the post-assembly fabrication of additional conducting electrodes between the site and the readout bus electrodes. Successful assembly, clamping, and interconnection was accomplished on these sites [67]. However, the resistance of the clamped rods exceeded the range of operation of the readout circuits.

Another important conclusion of this thesis is the necessity for electrical isolation of the readout circuitry during the assembly process. Since sub-micron CMOS devices operate at much lower supply levels than those required for DEP assembly of nanodevices, the readout circuits should include gate protection circuitry. Alternatively, the assembly sites should be initially electrically isolated from the readout circuits, and a post-assembly lithography/metallization approach should be used. However, this latter approach increases the complexity of the process technology and may offset manufacturability advantages.

6.1.2 Design of multi-band ultra-wideband transmitter for wireless sensor networks

The prototype design of a multi-band ultra-wideband transmitter for wireless sensor network applications was presented in this thesis. The transmitter was designed using Motorola's HiP6WRF low-voltage 0.18-μm Si/SiGe BiCMOS process and was primarily composed of a PLL frequency synthesizer with: (1) a high-speed CMOS phase frequency detector; (2) a CMOS charge pump; (3) an on-chip passive loop filter; (4) a negative-G_M VCO that capable of generating three different center frequencies based

on three different capacitive states in its tank circuit; and (5) a variable frequency divider (Divide-by-N network). The transmitter also incorporated a pulse generator to produce BPSK modulated ultra-wideband characteristic signals. The frequency bands of operation for this transmitter were 4.8, 6.4 and 8.0 GHz. This thesis work, specifically, included the design of the CMOS PFD, the on-chip passive loop filter, the pseudo-random code generator, and the overall layout of the transmitter.

All designs were simulated using the Cadence Spectre RF tool. The CMOS PFD provided phase tracking over the range -2π to $+2\pi$ radians. Using this PFD, the PLL frequency synthesizer stabilized with zero-phase and frequency offset in all three designed frequency bands. A two-bit CMOS pseudo-random code generator was designed to control the switching of frequency synthesizer between the frequency bands of operation. An on-chip passive loop filter was designed for a phase margin of 62° and a PLL bandwidth of 4 MHz. The loop filter, in conjunction with a charge-pump, provided a third-order, type-2 PLL operation and helped achieve an acquisition time of about 700 ns for all three frequency bands.

The layout of the ultra-wideband transmitter chip was performed using the Cadence Virtuoso layout tool. The die area of the chip was about 1.5 mm $\times$ 1.0 mm. The fabricated chip is currently being packaged for testing purposes. Measurement of the transmitter will be completed by other design team members as part of future work.

6.2 Future work

6.2.1 Dielectrophoretic assembly technique

The most immediate extension of the research work presented in this thesis is to assemble functional chemiresistive nanosensors with operational CMOS readout circuitry such as the resistance bridge described in Chapter 3. In addition, some sort of post-assembly clamping of the nanosensor is necessary to hold the nanosensor in place over long-term operation. In [67], the post-assembly deposition of capping metal layers at ends of the assembled nanowire using e-beam lithography techniques has been explored and demonstrated. An assembled and clamped gold nanowire on a CMOS test chip designed in this thesis work is shown in Figure 6.1. However,

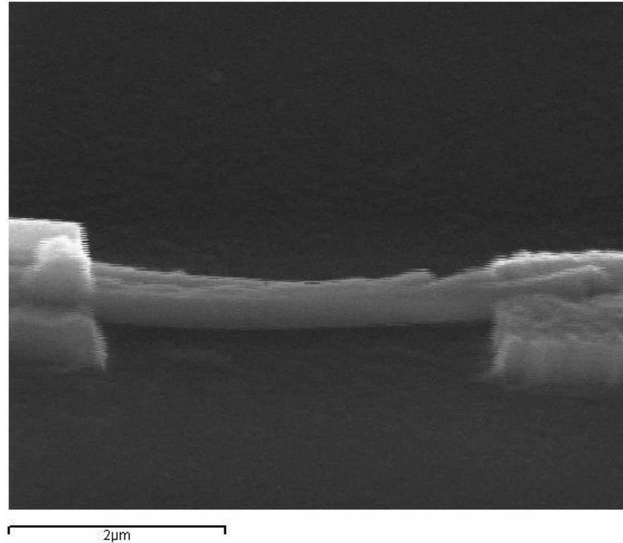


Figure 6.1: SEM picture of a gold nanowire (length $5\mu m$ and diameter about 200nm) assembled and clamped on a CMOS chip (from [67].)

it would be preferable to avoid this post-IC lithography process, particularly when a large number of nanosensors are to be sequentially assembled. Also, there is evidence of poor contact resistance after this process. A novel technique could be leveraged to overcome this limitation is a localized bonding technology such as that discussed in [81]. This technique used integrated heating circuits to reflow localized solder pads. A similar process could be developed to deposit capping metal layers over the ends of the assembled nanosensor.

The operation of the active readout circuit was not successfully demonstrated in this thesis due to gate failures of the input transistors. In the future, gate protection circuitry must be incorporated to protect the input transistors from high voltage swings of the assembly waveform. Alternatively, the readout circuit can be physically and electrically isolated from assembly sites as discussed in Section 4.3.2, and post-assembly lithography techniques used to make the electrical connections.

One more extension of the work presented in this thesis is to develop and assemble arrays of diverse functionalized nanosensors on a reconfigurable CMOS readout circuit. Figure 6.2 shows a conceptual diagram of a diverse-functionalized sensor array (electronic nose) integrated with CMOS circuits. The main idea here is to control the assembly and readout process using CMOS digital circuitry. This digital circuit

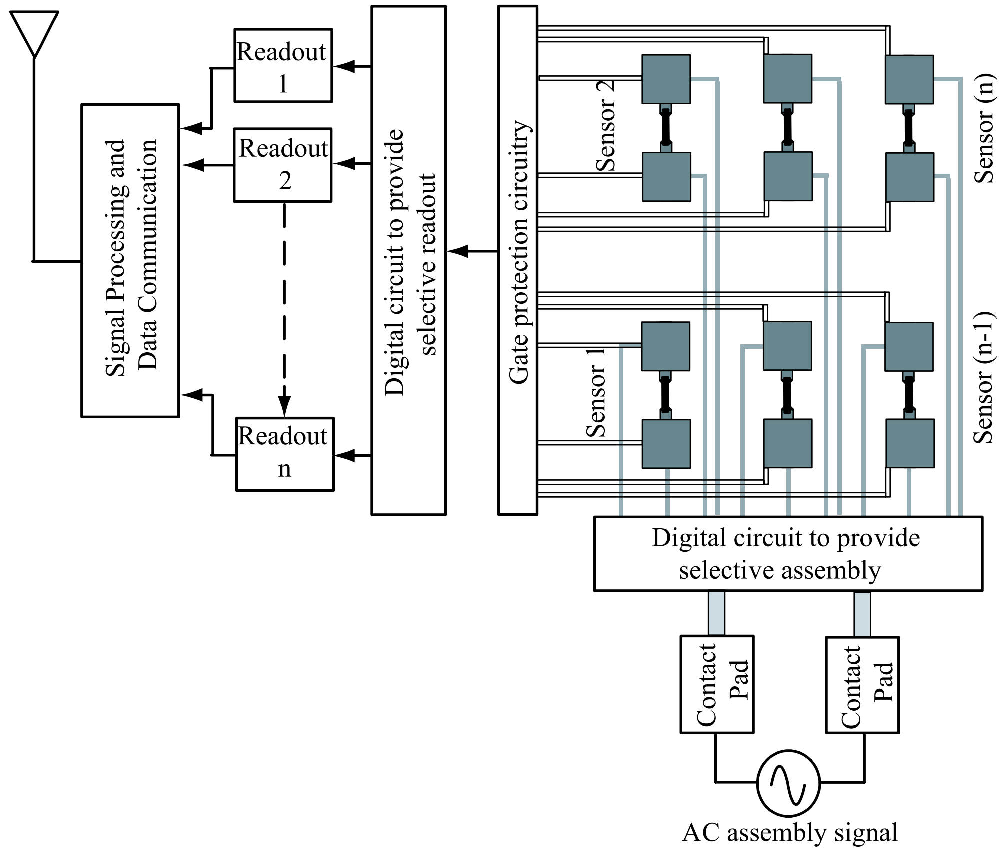


Figure 6.2: Conceptual diagram of diverse-functionalized sensor array with a CMOS digital circuitry controlling the assembly and readout process.

could enable selective assembly of nanosensors. Again, gate protection for the readout electronics must be provided. Subsequently, selective readout can be enabled for individual nanosensors in the array of sensors.

6.2.2 Data communication circuitry for wireless sensor networks

The multi-band hopped ultra-wideband transmitter design presented in this thesis work was a prototype for future wireless sensor network node applications. Measurements on the transmitter are to be completed once the fabricated chip is packaged. The prototype design presented here only hopped over three different frequency bands. However, practical wireless sensor networks would require the sensor nodes

to support many more frequency bands for sufficient multiple access. Future work in this area should be directed towards incorporation of more frequency bands that could support a large number of sensor nodes. This extension would require a more complex switched-tank VCO and pseudo-random code generator control to provide rapid switching between frequency bands. In addition, pulse shaping network should be included to the present design to better confine the transmitted spectra to the desired band. The present design also does not incorporate sensor interface circuitry, A-D converter, power amplifier, etc. Future work should be directed towards the development of an integrated low-power ADC and a high-efficiency broadband power amplifier for ultra-wideband data transmission, and their integration with sensor readout circuitry and sensor system. Consideration of mixed-signal effects in such an integrated sensor/communications environment is also needed.

Appendix A

Simulation of PLL frequency synthesizer

The simulation of PLL was performed in Cadence design suite. Transient simulations were performed and the control voltage provided to the varactors of the VCO was analyzed. The PLL consists of a large number of digital/analog and RF components and therefore the transient analysis in Cadence takes longer time to simulate. To overcome this issue, VerilogA model files for the phase/frequency detector, the charge pump, the VCO and the divider were generated. The simulation times of these verilogA model files were significantly less than those of the real circuit components. A PLL incorporating these verilogA components was first simulated before designing the individual circuit components of the PLL.

In the verilogA model files, the specifics of all the components (for example, charge pump output current, supply voltage, VCO tuning gain, etc.) were incorporated. The model files for the PFD and charge pump, the VCO and the divider are listed below. The specifics for each of these components are highlighted to give a better understanding of the models.

- **VerilogA model for PFD and Charge pump**

```
// These are standard includes that define the
// electrical discipline and constants, such as 'M_PI
```

```
‘include "constants.h"
‘include "discipline.h"
module pfd_cp(cpout, clkout, refclk);
// refclk and clkout are the reference
// and feedback clocks, respectively
input refclk, clkout;
// cpout is the output current of the charge pump
output cpout;
electrical refclk, clkout, cpout;
parameter real vdd=1.8;
// charge pump current
parameter real iout=250u;
// transition time for the charge pump current
parameter real trf=200p from (0:inf);
parameter real td=1p from (0:inf);
parameter real ttol=1p from (0:inf);
parameter integer dir=1;
integer state;
analog begin
// This is a simple implementation of the
// three-state sequential phase detector.
// The cross operator generates events
// whenever the expression argument (in this case,
// the voltage on refclk) crosses zero
```

```
// with the tolerance ttol.
@(cross(V(refclk)-vdd/2, dir, ttol)) begin
if (state >-1) state=state-1;
end
@(cross(V(clkout)-vdd/2, dir, ttol)) begin
if (state <1) state=state+1;
end
// Set the output current of the charge pump
I(cpout) <+ transition (iout*state, td, trf);
end
endmodule
```

- **VerilogA model for VCO**

```
`include "constants.h"
`include "discipline.h"
module VCO(vctrl, vco_out);
output vco_out;
input vctrl;
electrical vco_out, vctrl;
// vmin and vmax are the minimum and maximum
// values of vctrl, respectively
parameter real vmin=0.0;
parameter real vmax=2.5 from (vmin:inf);
// fmin and fmax are the minimum and maximum
// values of the VCO output frequency
```

```
parameter real fmin=250e6 from (vmin:inf);
parameter real fmax=2e9 from (fmin:inf);
// vdd is the supply voltage. The VCO output
// goes between 0 and vdd.
parameter real vdd=2.5;
// tt is the transition time of the VCO output
parameter real tt=0.01/fmax from (0:inf);
// jitter is the rms jitter introduced in the
// VCO, say by sustrate or power-supply noise
parameter real jitter=0 from [0:0.25/fmax);
parameter real ttol=1e-6/fmax from (0:1/fmax);
real freq, phase, dt;
integer n, seed;
analog begin
@(initial_step) seed=-556;
// compute frequency from input voltage
freq=(V(vctrl)-vmin)*(fmax-fmin)/(vmax-vmin)+fmin;
// saturation points for the VCO output
if (freq>fmax) freq=fmax;
if (freq<fmin) freq=fmin;
// phase noise adder
freq = freq/(1+dt*freq);
// phase is the integral of the frequency modulo 2PI
phase=2*‘M_PI*idtmod(freq, 0.0, 1.0, -0.5);
```

```
// jitter is updated twice per period
@(cross(phase+‘M_PI/2,+1, ttol) or
cross(phase-‘M_PI/2,+1, ttol)) begin
dt=1.414*jitter*$dist_normal(seed, 0, 1);
n=(phase >= -‘M_PI/2) && (phase < ‘M_PI/2);
end
V(vco_out) <+ transition(n?vdd:0, 0, tt);
end
endmodule
```

- **VerilogA model for divider**

```
‘include "constants.h"
‘include "discipline.h"
module divider(div_out, div_in);
input div_in;
output div_out;
electrical div_in, div_out;
parameter real vdd=2.5;
// This is the divide-down ratio for the divider
parameter integer ratio=4 from [2:inf);
// dir=1 for positive-edge-triggered latch
// dir=-1 for negative-edge-triggered latch
parameter integer dir=1 from [-1:1] exclude 0;
// transition time for divider output
parameter real tt=100p from (0:inf);
```

```
parameter real td=10p from (0:inf);
parameter real ttol=1p from (0:td/5);
integer count,n;
real dt;
analog begin
@(cross (V(div_in)-vdd/2, dir, ttol)) begin
count = count+1;
if (count >= ratio)
count=0;
n=(2*count >= ratio);
end
V(div_out) <+ transition(n? vdd: 0, td, tt);
end
endmodule
```

A.1 Simulation of verilogA-based PLL

A schematic of the PLL incorporating the verilogA components is shown in the Figure A.1. In this case, all the PLL components were substituted with verilogA components. The required specifics were defined in each component. Before designing the individual components of the PLL frequency synthesizer for UWB transmitter, various simulations were performed on the verilogA-based PLL. For example, the charge pump output current was varied and the loop characteristic was analyzed (refer to simulation results in Figure A.2. The output current of the CMOS charge pump designed for the UWB transmitter was decided based on this simulation result. The higher the current, the faster the acquisition time and hence the CMOS charge pump was designed for an optimum output current of $250\mu A$.

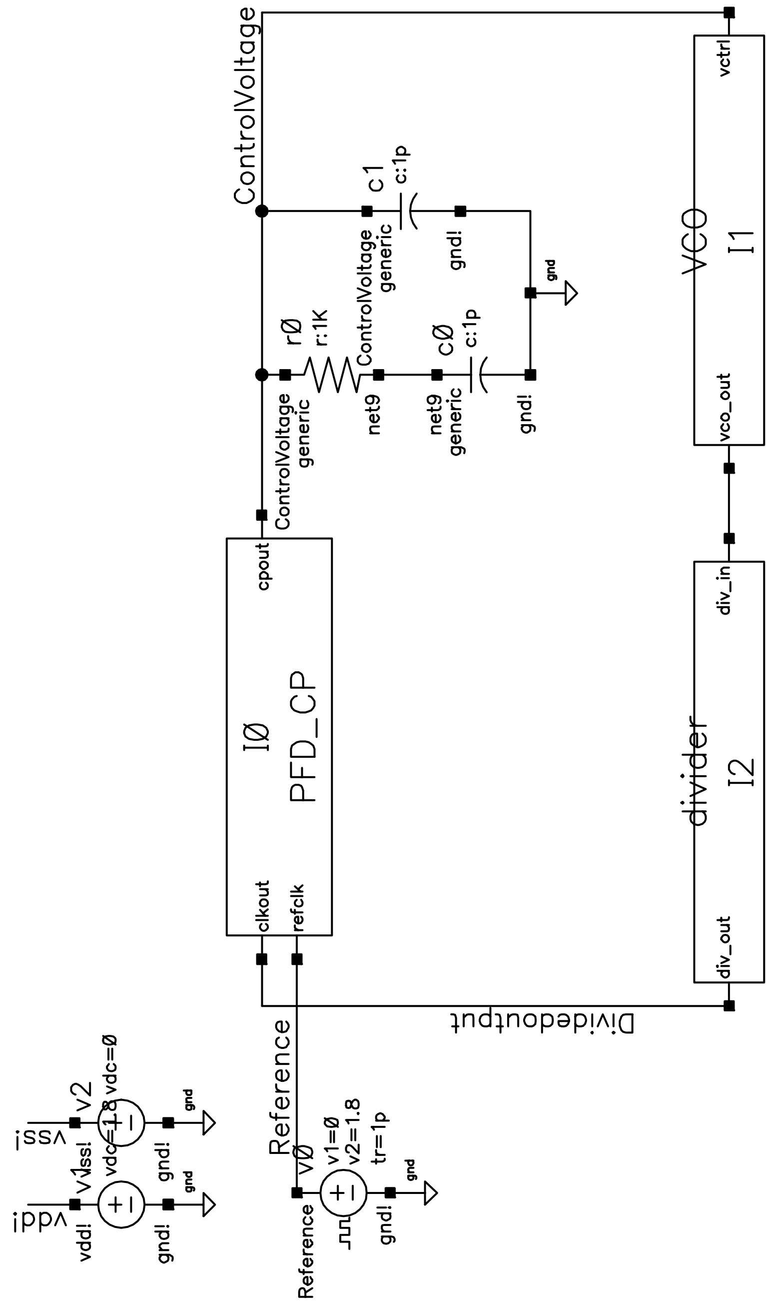


Figure A.1: Schematic of PLL incorporating verilogA components. The PFD, charge pump and the VCO were the verilogA components in this case.

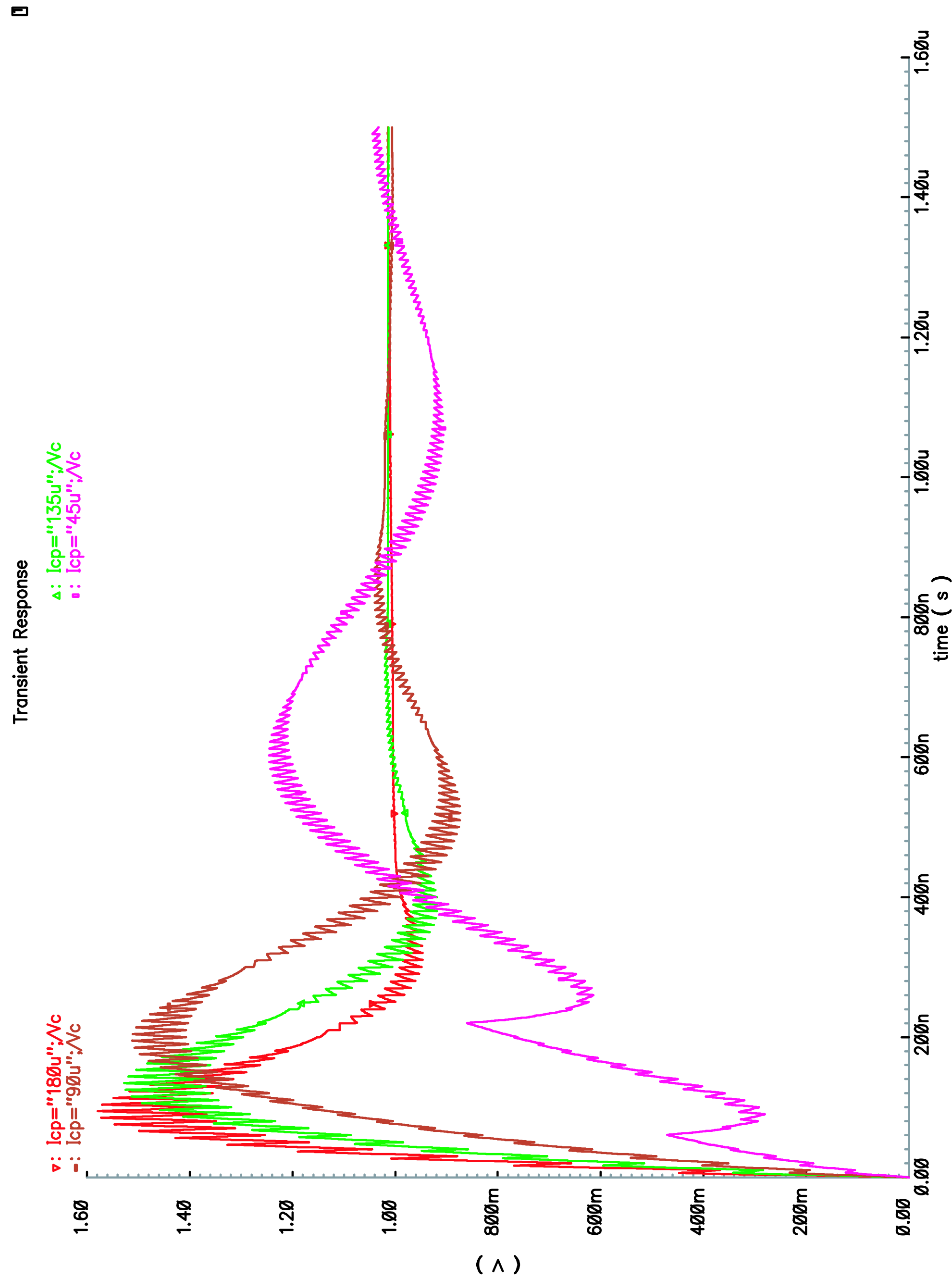


Figure A.2: Simulation result of the verilogA PLL for different values of charge pump output current. The output current of the charge pump designed for the UWB transmitter was determined based on this simulation result.

After the simulation of verilogA-based PLL, the individual components were replaced in order. First, the CMOS PFD was analyzed by incorporating it in a PLL with verilogA based divider and VCO. Transient simulations were performed on this PLL. The performance of the CMOS PFD was then analyzed. The required design changes on the PFD were incorporated based on this simulation results. The performance of negative-G_M VCO designed for the UWB transmitter was then analyzed. The BiCMOS VCO was incorporated in a PLL along with verilogA-based PFD and divider and the loop characteristic was examined. Based on the results, design modifications were implemented in the VCO.

Finally, after analyzing the characteristics of individual circuit components, transient simulations were performed on the PLL incorporating the CMOS PFD, the CMOS charge pump, the negative-G_M VCO and the CMOS divider.

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Vita

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