Investigating Impact of Emerging Medium-Voltage SiC MOSFETs on Medium-Voltage High-Power Applications

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ABSTRACT

For decades, the Silicon-based semiconductors have been the solution for power electronics applications. However, these semiconductors have approached their limits of operation in blocking voltage, working temperature and switching frequency. Due to material superiority, the relatively-new wide-bandgap semiconductors such as Silicon-Carbide (SiC) MOSFETs enable higher voltages, switching frequencies and operating temperatures when compared to Silicon technology, resulting in improved converter specifications. The current study tries to investigate the impact of emerging medium-voltage SiC MOSFETs on industrial motor drive application, where over a quarter of the total electricity in the world is being consumed.

Firstly, non-commercial SiC MOSFETs at 3.3 kV and 400 A rating are characterized to enable converter design and simulation based on them. In order to feature the best performance out of the devices under test, an intelligent high-performance gate driver is designed embedding required functionalities and protections. Secondly, total of three converters are targeted for industrial motor drive application at medium-voltage and high-power range. For this purpose the cascaded H-bridge, the modular multilevel converter and the 5-L active neutral point clamped converters are designed at 4.16-, 6.9- and 13.8 kV voltage ratings and 3- and 5 MVA power ratings.

Selection of different voltage and power levels is done to elucidate variation of different parameters within the converters versus operating point.

Later, comparisons are done between the surveyed topologies designed at different operating points based on Si IGBTs and SiC MOSFETs. The comparison includes different aspects such as efficiency, power density, semiconductor utilization, energy stored in converter structure, fault containment, low-speed operation capability and parts count (for a measure of reliability). Having the comparisons done based on simulation data, an H-bridge cell is implemented using 3.3 kV 400 A SiC MOSFETs to evaluate validity of the conducted simulations.

Finally, a novel method is proposed for series-connecting individual SiC MOSFETs to reach higher voltage devices. Considering the fact that currently the SiC MOSFETs are not commercially available at voltages higher above 1.7 kV, this will enable implementation of converters using medium-voltage SiC MOSFETs that are achieved by stacking commercially-available 1.7 kV MOSFETs. The proposed method is specifically developed for SiC MOSFETs with high dv/dt rates, while majority of the existing solutions could only work merely with slow Si-based semiconductors.

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GENERAL AUDIENCE ABSTRACT

Despite their mature technology and low manufacturing cost, the traditional Si-based power semiconductors had reached their limitations in operation from different points of view. The SiC MOSFETs which are the new generation of power semiconductors however seem to be able to shift the existing boundaries of operation for the Si-based semiconductors, resulting in significant improvement in design and operation of power electronics converters. This dissertation focuses on investigating the impact of emerging medium-voltage SiC MOSFETs on industrial motor drives, which consume over 28% of the total electricity used in the world.

Firstly, the state-of-the-art non-commercial 3.3 kV SiC MOSFETs are characterized. Characterization of the devices is done to extract their key features such as switching and conduction losses, to enable loss calculation and performance evaluation in any target application. Since the mentioned devices are not commercial yet, the gate driving circuitry that can feature the best performance out of them are not commercially available either. Thus, the characterization process starts with design of an intelligent high-performance gate driver for the devices under test. Secondly, total of three topologies that are targeted for the study are discussed and their basics of operation is investigated. For this purpose the cascaded H-bridge, the modular multilevel converter and the 5-L active neutral point clamped converters are designed at three different voltage levels

(4.16-, 6.9- and 13.8 kV) and two power levels (3- and 5 MVA). Selection of different voltage and power levels is done to enable comparison from different aspects as the operating point changes.

Later, comparisons are done between the surveyed topologies designed at different operating points using different semiconductor technologies. The performed comparisons provide an unbiased input for the manufacturers and customers of these converters for selection of the target topology in motor drive application. Also to verify validity of the conducted simulations and calculations, a full-bridge converter cell is experimentally implemented using 3.3 kV 400 A SiC MOSFETs.

Finally, a novel method is proposed for series-connecting lower-voltage SiC MOSFETs to reach higher-voltage devices. As of late 2017, the medium-voltage SiC MOSFETs are not commercially available. Also it is expected that upon commercialization, their price will be multiple times of that of low-voltage SiC MOSFETs. Thus, connecting lower-voltage SiC MOSFETs in series is an effective way of achieving higher-voltage devices and take advantage of superior properties if the SiC MOSFETs, while the availability and high cost problems are taken care of.

To My Happy Family

My devoted parents: ***Yahya Marzoughi*** *and* ***Vajiheh Attarian***

My wonderful wife: ***Marjan Ghodrati***

My best friend and lovely son: ***Keon Marzoughi***

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Chapter 1. Introduction

This chapter presents the motivations, objectives and an overview of this dissertation. Advantages of the wide-bandgap semiconductors over the traditional Si-based semiconductors are surveyed to investigate how they can improve operation of the power electronic converters. Also, an overview of the medium-voltage high-power motor drive application is provided to better demonstrate importance of improvement in converters used for this purpose. Moreover, this chapter provides a review of this field, followed by the dissertation outline and the scope of research.

1.1 The Wide-Bandgap Semiconductors

For decades, the silicon-based semiconductors have been the solution for power electronics applications due to their mature technology and low manufacturing costs. However, these semiconductors seem to be approaching their limits of operation in blocking voltage, working temperature and switching speed [1]. The voltage rating of commercial Si IGBTs is limited to 6.5 kV and at higher voltages, the maximum switching frequency featured by these semiconductors is no more than several hundred hertz. Development of optimal switching schemes such as selective harmonics elimination (SHE) and selective harmonics mitigation (SHM) was mainly due to overcome the restriction in switching performance of Si-based semiconductors for high power converters [2], [3]. Moreover, no Si-based semiconductor is reported to be capable of operating beyond 200°C [4].

Due to superior material properties [5], [6], the wide bandgap semiconductors such as gallium nitride (GaN) and silicon carbide (SiC) enable higher voltages, switching frequencies and operating temperatures when compared to conventional silicon technology. According to Figure 1.1, larger energy gap, higher electron velocity, higher melting point, better thermal conductivity and higher electric field offered by the wide-bandgap materials results in higher operating voltages, higher operating temperatures and higher switching frequencies by the semiconductors made based on them [7].

Since realization of the first SiC MOSFET in 1992 [8], a tremendous amount of attention has been devoted to these semiconductors and at intermediate voltage range from 650 V to 1.7 kV, several generations of SiC FETs are commercially available with current ratings up to hundreds of amperes and specific on-resistances smaller than 4 $m\Omega.cm^2$ [1], [9]. Meanwhile, researchers have been trying to expand the penetration range of SiC MOSFETs to medium voltage range which has

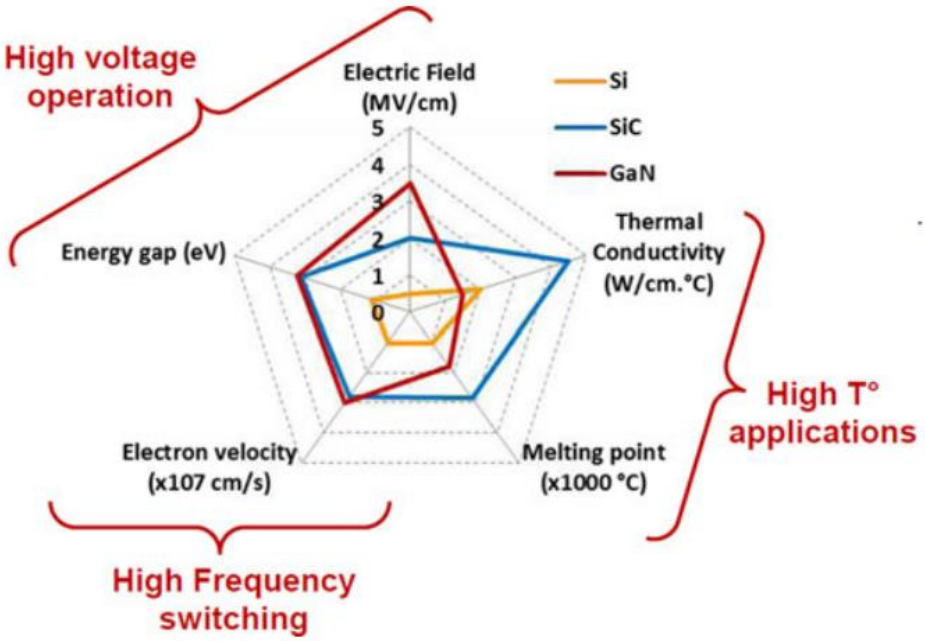


Figure 1.1 Summary of the relevant material properties for Si, SiC and GaN [7].

resulted in laboratory prototypes or sample semiconductors in voltage range of 2.5 kV up to 15 kV and current ratings up to 1500 A.

In 2006, first 10 kV SiC MOSFET was prototyped by CREE at 5 A current rating [10] and later it was extensively characterized and modeled in [11], where device performance in boost converter application was also investigated. In 2011, a 10 kV 120 A SiC MOSFET module was built by a joint group of researchers utilizing 24 SiC MOSFET dice from CREE and a package from Powerex [12] and advantages of SiC MOSFET in solid state power substation application were shown over conventional transformer from power density point of view.

From 2012 to 2014, several efforts were made to realize laboratory SiC prototypes, resulting in 3.3- and 3.4 kV SiC MOSFETs [13], [14]. In 2015, structure and fabrication of 3.3 kV 30 A dice was shown [15]. Then a 400 A module was built based on those dice and its performance was briefly estimated by deriving output characteristic as well as switching waveforms at a single operating point. In 2015, world's first all-SiC traction inverter was demonstrated by fabricating 3.3 kV 1500 A modules composed of 100 A dice inside [16]. Last but not least, CREE introduced 10 kV 240 A and 15 kV 20 A SiC MOSFETs [17], [18]. Figure 1.2 shows the reported non-commercial SiC prototypes by different companies as of 2017.

Besides making improvements to existing topologies, SiC semiconductors can lead to emergence of new topologies that were not feasible due to mentioned restrictions of Si semiconductors. The main application areas of wide bandgap semiconductors is expected to be traction systems, renewable energies and downhole drilling [1], [6]. Higher switching frequencies enabled by using SiC MOSFETs can result in smaller filter size, higher power density and higher

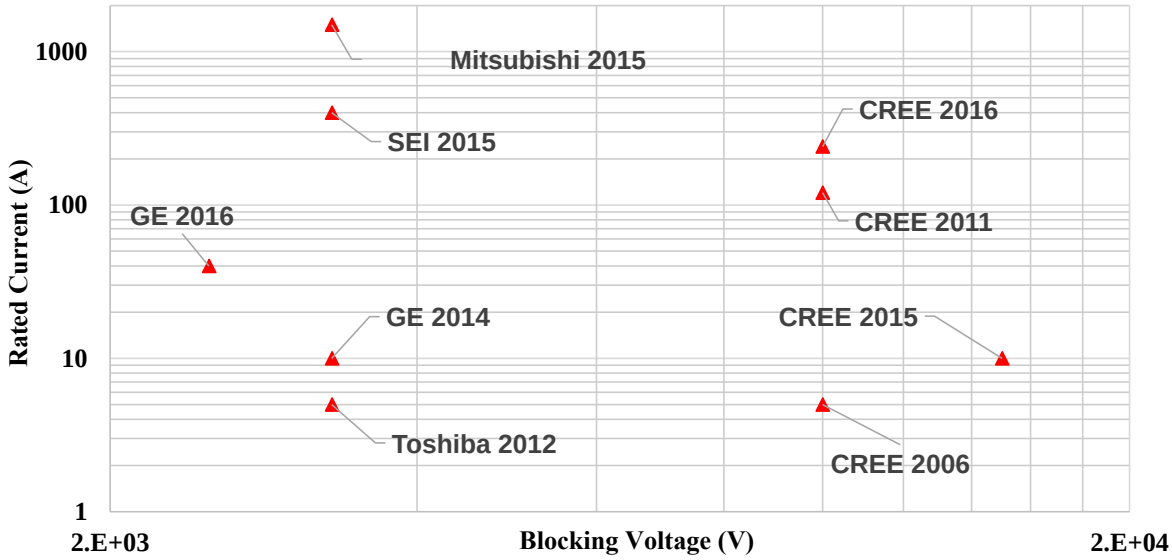


Figure 1.2 A summary of non-commercial SiC MOSFET prototypes at voltages above 1.7 kV.

efficiency for drive systems [19]. In regards to renewable energies and other grid-connected applications, SiC FETs can feature higher efficiency while power quality can also be improved by increasing the switching frequencies [20]. In downhole drilling applications where due to restrictions in cooling the operating temperature is higher, SiC MOSFETs can be game changing devices due to better thermal conductivity and higher maximum operating temperatures [1]. Other than the previously mentioned major fields, several more applications such as dc-dc converters, FACTS and etc. can be listed where wide bandgap semiconductors can have a considerable positive impact.

At the same time with efforts on expanding penetration range of SiC MOSFETs in medium voltages, researchers have been interested in evaluating performance of sample or commercial SiC devices versus existing Si semiconductors in different applications. In [21], authors compared 1.2 kV SiC FETs and Si IGBTs for inverter and DC-DC applications. Reference [22] characterized and modeled Si and SiC semiconductors for optimized design of traction inverters. In [23],

comparison of 6.5 kV Si IGBT and SiC FETs for medium-voltage power electronics applications was done with emphasize on calculating their switching parameters. Reference [24] compared 1200 V Si IGBTs and SiC MOSFETs in matrix converter application, and assessed efficiency and EMI generated by each technology. In [25], authors compared 6.5 kV Si IGBT with Si-PiN diode to 6.5 kV Si IGBT with SiC junction barrier shottky (JBS) diode and 10 kV SiC MOSFET with SiC-JBS diode. System efficiency and leakage current of Si IGBTs and SiC FETs in variable-frequency drive was compared in [26], considering different filtering options.

Until a few years back, price was a main barrier for SiC semiconductors to replace Si IGBTs [21]. However, with considerable developments in the field of SiC MOSFETs, the projected price for a SiC MOSFET in 3.3 kV to 10 kV range by the end of 2018 is as low as 8% of that in 2012 [27] and it will keep continuously reducing in coming years. Thus, it is expected to have commercial medium-voltage SiC MOSFETs in the market in near future. Figures 1.3-1.5

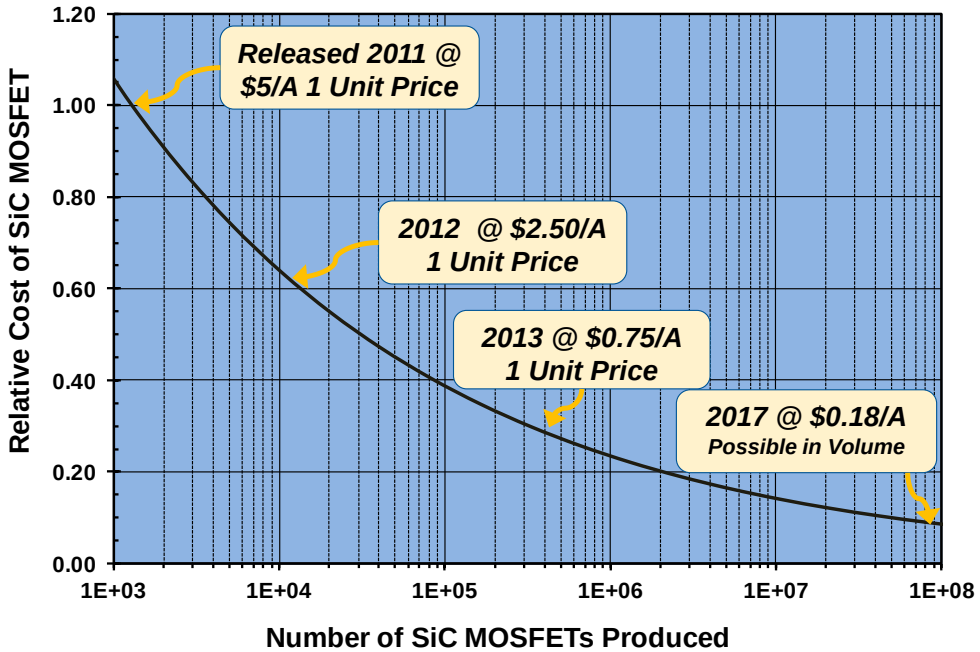


Figure 1.3 Projected relative cost trend for 1.2 kV SiC MOSFETs (Amps at 100˚C) [27].

demonstrate the projected price for SiC MOSFETs at 1.2-, 3.3- and 10 kV voltage rating versus number of MOSFETs produced [27].

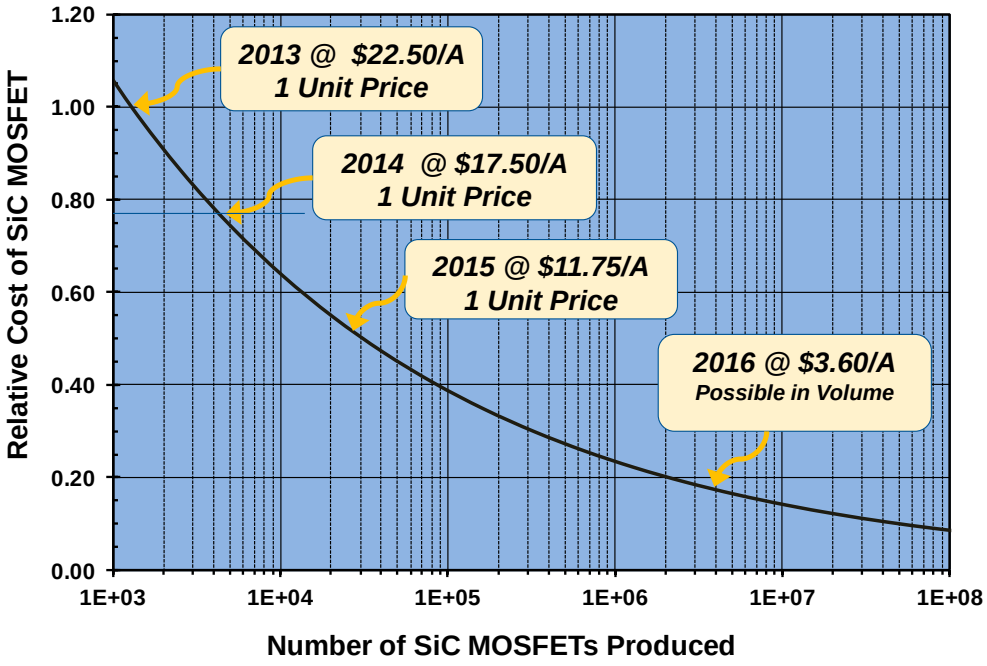


Figure 1.4 Projected relative cost trend for 3.3 kV SiC MOSFETs (Amps at 100˚C) [27].

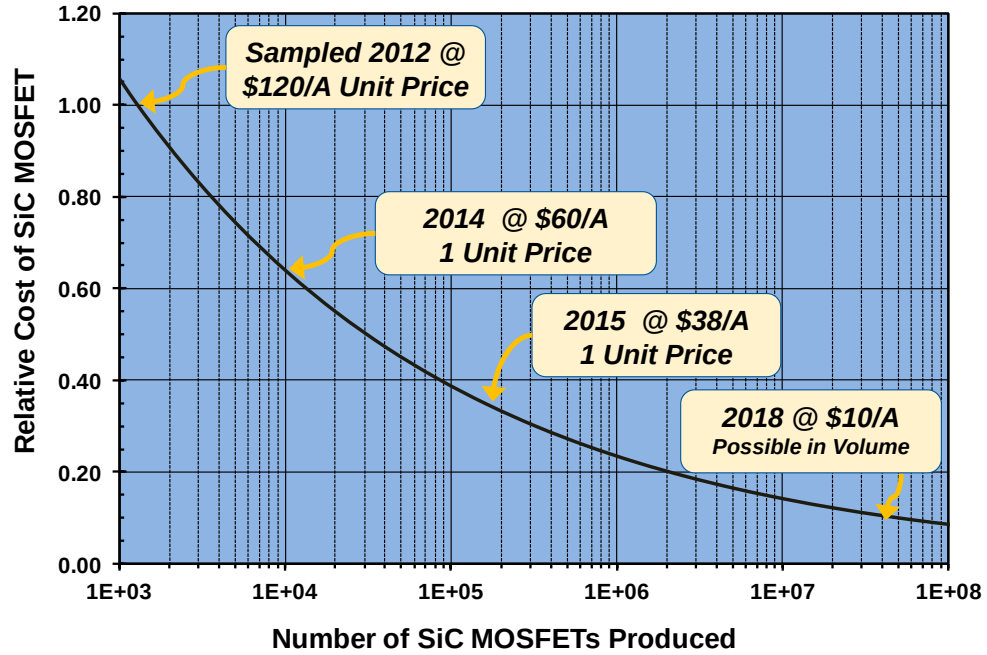


Figure 1.5 Projected relative cost trend for 10 kV SiC MOSFETs (Amps at 100˚C) [27].

1.2 Stacking Individual SiC MOSFETs to Reach Higher Voltages

According to the previous subsection, the non-commercial SiC MOSFET prototypes are already reported up to 15 kV. However, the commercial SiC MOSFETs are not available at voltages beyond 1.7 kV. Stacking individual semiconductors in series or using multilevel converter topologies are two effective ways of reaching higher voltages with low-voltage devices. Although the multilevel topologies offer outstanding features such as low common-mode voltage, low *dv/dt* stress and low propagated electromagnetic interference (EMI) [28], [29], [30], [31], [32], using individual semiconductors in series will result in lower cost and higher efficiency. Also, according to a study by GE using two or more medium-voltage semiconductors in series features better on-resistance and higher current density than using a single higher-voltage device [33].

Figures 1.6 and 1.7 demonstrate the theoretical specific on-resistance and the projected current density for SiC MOSFETs in a blocking voltage range of 1 kV to 100 kV. According to figure 1.6, for a wide range of blocking voltage (approximately for > 2 kV blocking voltage), using two lower-voltage SiC MOSFETs in series will feature better specific on-resistance than using a single SiC MOSFET with higher blocking voltage capability. In a similar way, for a wide range of operating voltages, using five or ten lower-voltage SiC MOSFETs will feature better performance and less conduction losses than using a single higher-voltage device. On the other hand, according to figure 1.7, using several lower-voltage SiC MOSFETs in series will feature higher current density (smaller die size utilization) compared to a single device with larger blocking voltage capability. It is worth to note that other than the mentioned benefits, using lower-voltage SiC MOSFETs will result in smaller switching losses and less initial investment in the system.

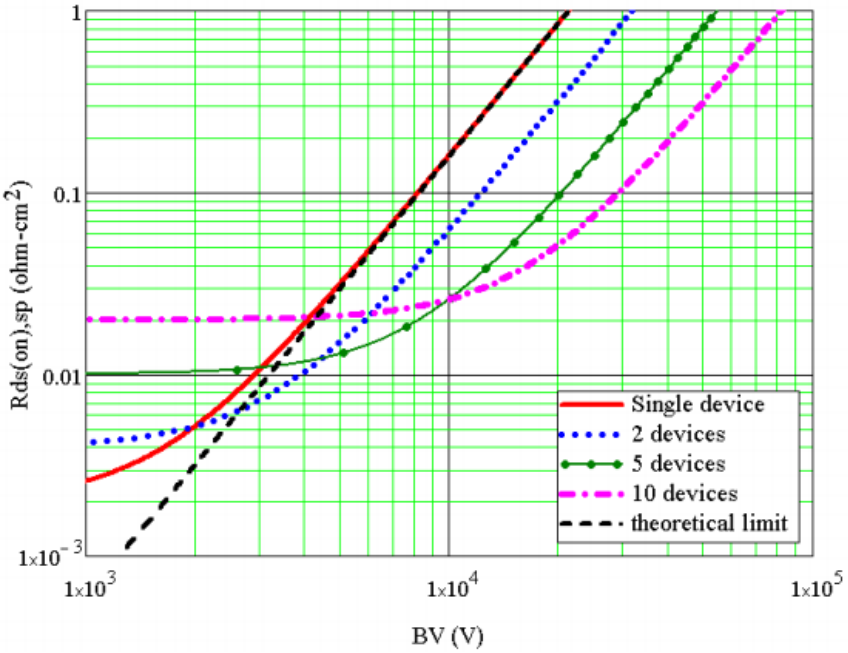


Figure 1.6 Specific on-resistance of SiC MOSFETs versus blocking voltage [33].

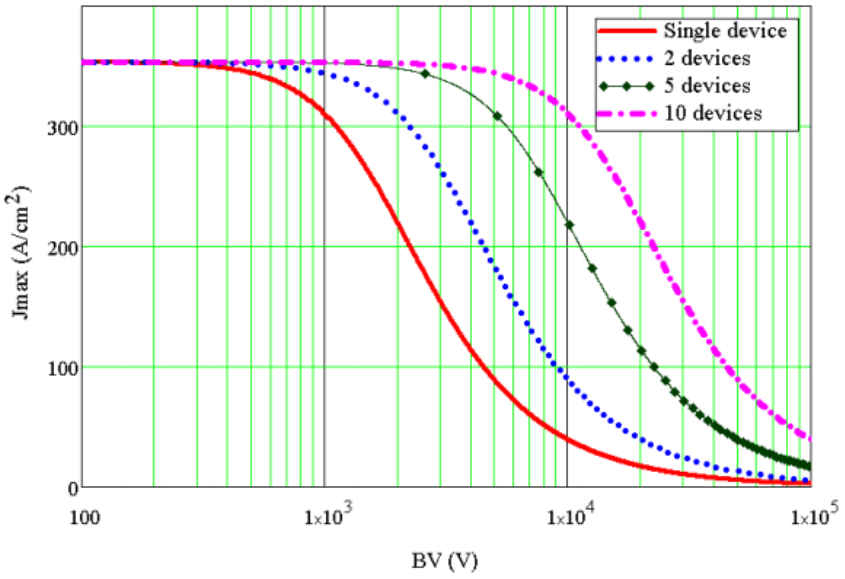


Figure 1.7 Projected current density for SiC MOSFETs versus blocking voltage [33].

The main problem with series-connected semiconductors is inherent unequal voltage sharing among them, which if not controlled, can result in damage to all of the series-connected switches in a stack. According to literature, there are several factors contributing to unequal voltage sharing

among series-connected semiconductors. The two factors that are addressed in most of the literature are mismatched gate drivers and mismatched semiconductors [34], [35], [36]. Mismatch in different parts of the gate driver systems such as isolators, transmitters and receivers can result in time shift for gate driving signals of the stacked semiconductors. It is clear that non-simultaneous switching will result in unequal voltage sharing among series-connected semiconductors. In a similar fashion, mismatch in characteristics of the devices will cause voltage imbalance among them.

A wide variety of voltage balancing schemes are proposed for series-connecting individual semiconductors (mostly for slow Si-based devices). Passive snubbers are among the simplest and most reliable voltage balancing methods for series-connected semiconductors. In [37], a study was done to size an appropriate passive snubber for 1.7 kV SiC MOSFETs connected in series. Another method for sizing passive snubbers for series-connected switches was proposed in [38]. The passive snubber solutions add considerable amount of losses in the system. In order to overcome this problem, in [39] authors proposed a controlled RC passive snubber system in which the capacitors do not completely discharge under main switch turn-on condition, reducing the energy loss. However, this method needs an on-board high-voltage power supply per each stack of semiconductors.

Master-slave switching of the semiconductors connected in series is another method to assure equal voltage sharing among them. Several efforts have been made in this field, resulting in acceptable voltage distribution [40], [41], [42], [43]. However, the master-slave connection methods usually add large propagation delays to the system, since switching of an arbitrary device depends on completely switching of the previous device(s) in stack. Active Miller clamping has

also been used in several literature to balance voltages across stacked Si IGBTs [44], [45]. Although this method results in satisfactory results, but the losses associated with additional Miller capacitors as well as saturation of the IGBTs are considerable.

In [46], researchers of Fuji Electric proposed using chokes at gates of stacked Si IGBTs in order to synchronize them. This method resulted in nearly perfect voltage sharing among stacked Si IGBTs, however it cannot be adopted for SiC MOSFETs since the considerable amount of gate loop inductance added by this method is not compatible with fast-switching SiC MOSFETs. Reference [47] introduced a self-powered gate driving scheme, in which by removing the parasitic capacitances from gates to ground, voltage sharing was significantly improved among three Si IGBTs connected in series. Another paper later discussed the complicated parameter design stage of the same self-powered gate driver scheme [48].

Last but not least, a variety of attempts have been made to achieve voltage balancing among series-connected semiconductors by means of control schemes. These methods are normally referred to as active voltage balancing methods. In [49] and [50], switching speed of the stacked devices are controlled by means of an additional current source/sink stage on the gate driver to feature similar share of the total dc bus. Also, in [51] the authors have tried to use control algorithms in order to realize similar voltage sharing among stacked Si IGBTs. The latter is capable of achieving acceptable voltage balancing among series-connected Si IGBTs at the expense of taking them to saturation (which adds to the system losses).

The common goal in all of the surveyed solutions was to balance the voltages across series-connected switches to enable higher-voltage semiconductors. Due to the mentioned facts on unavailability and high price of the medium-voltage SiC MOSFETs, stacking lower-voltage devices

will be an effective method to take advantages of the SiC MOSFETs in medium-voltage applications.

1.3 Medium-Voltage High-Power Applications

According to a report from ABB [52], the total amount of electricity consumed in the world in 2015 was 21.9 trillion kWh. According to figure 1.8, this amount is predicted to increase in a linear manner until by 2050, the total electricity consumption in the world will be almost double of that in 2015.

Considering the tremendous amount of electricity consumption in the world, it is of great importance that in all stages of generation, transmission and distribution, the electric power is handled at high voltages. This is due to the fact that at constant power, as voltage increases, current (and the corresponding power loss) will reduce. Also according to figure 1.9 which is extracted from the "world bank commodity price data", price of copper has had a huge leap over the past decade. Higher copper price will further dictate utilization of medium- and high voltages in order to reduce the conducted current and its associated losses.

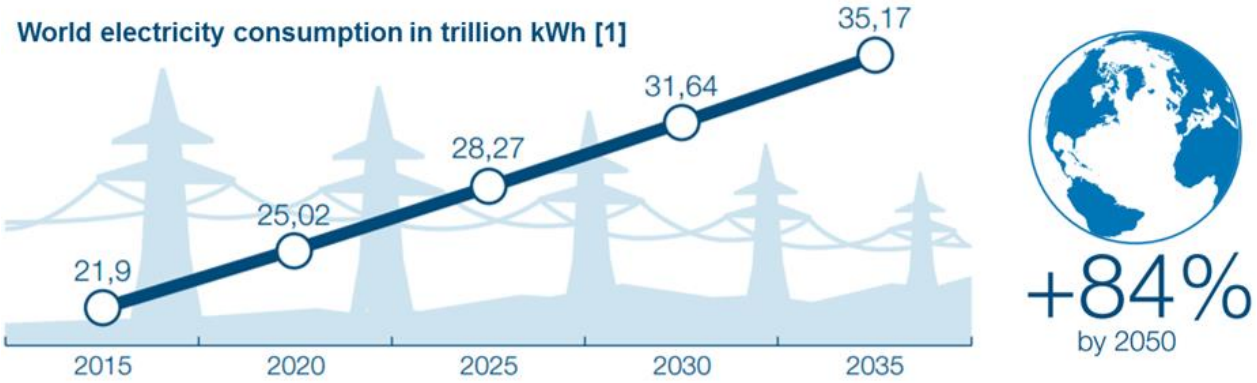


Figure 1.8 The total amount of electricity consumed in the world in trillion kWh. An 84% increase is predicted in worldwide electricity consumption by 2050 [52].

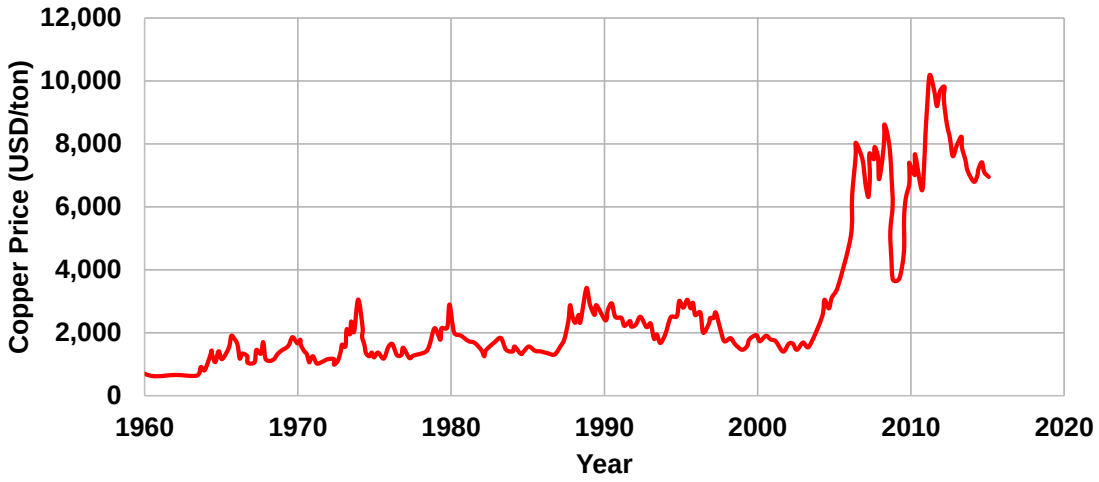


Figure 1.9 Price of copper in USD per ton, where dollar value in each year is normalized to that of 2011.

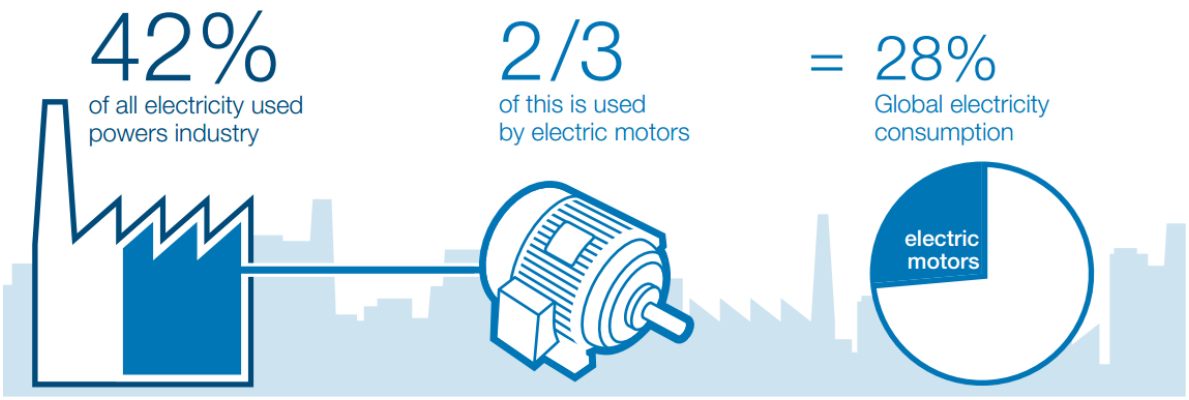


Figure 1.10 Share of the industrial electric motors from the global electricity consumption [52].

Medium- and high voltage are usually achieved by means of the multilevel converters. At medium-voltage range which is the scope of this dissertation, the multilevel converters are used in a variety of applications including industrial drives [53], [54], STATCOM [55], HVDC [56], grid-tied inverter for distributed generation [57], dc-dc power conversion [58] and so on. According to [52], about 28% of the total electricity used in the world is consumed by industrial motors (figure 1.10) and a significant part of this is being consumed by medium-voltage high-power motors.

The power driving the industrial motors has to be processed by motor drive converters. Thus, it can be concluded that a tremendous amount of power in the world is being processed by the medium-voltage high-power multilevel converters used for driving the industrial motors. This is the reason why in this dissertation, the motor drive application is taken as the case study among the medium-voltage high-power applications.

In the area of industrial motor drives, several multilevel voltage source inverter (VSI) topologies are already used in commercial products. For low voltage drives, several topologies like the 2-L VSI (e.g. *Alstom MV500*) and three level neutral point clamped (NPC) converter (e.g. Converteam *MV 7000* and Siemens *Sinamics SM150*) are serving in industry. In higher voltages, the recently patented five level active neutral point clamped (5-L ANPC) topology (used in *ACS2000* series by ABB) and the popular cascaded H-bridge (CHB) converter (e.g. Siemens *Robicon perfect harmony* and Delta Electronics *MVD 2000* series) are employed in commercial products. The 5-L ANPC is used by ABB at 4-6.9 kV range, and as a matter of fact, the CHB converter is the most popular topology in medium voltage range as of now, and it is being commercially manufactured by several vendors from 2.3 kV up to 13.8 kV. Last but not least, the modular multilevel converter (MMC) which is the state-of-the-art topology among multilevel converters has the capability to operate at any given voltage level without any restriction. This converter is already serving in industrial applications such as HVDC, active front-end rectifier for different purposes and motor drive.

In the area of comparing multilevel topologies for motor drive application, several efforts have been made so far. In [59] systematic comparison of four different topologies for direct ac-ac drive was shown for low voltage motor drives. The converters under study were compared from different points of view such as efficiency and weight (for measure of power density). In [53], neutral point

clamped, flying capacitor (FLC) and cascaded H-bridge converters were evaluated to serve as motor drive converter to feed a 4 kV 4.16 MVA motor. Component design, loss calculation and LC filter design were done for the mentioned converter topologies. In a similar fashion to [53], reference [60] compared two-level voltage source converter, three-level NPC, three-level FLC, four-level FLC and five-level CHB converters to realize 2.3 kV 2.4 MVA industrial drive based on 6.5-, 3.3-, and 1.7 kV IGBTs. In [54], the CHB and MMC topologies were compared for motor drive application at medium voltage range. In a similar way later in [61] the CHB, MMC and 5-L ANPC topologies were designed for medium-voltage drives at 4.16, 6.9 and 13.8 kV using Si IGBTs, and efficiency, stored capacitive energy (in J/kVA) and semiconductor utilization of converters were compared. Last but not least, in [62] the modular multilevel converter and the triple-star bridge-cell (TSBC) converter configurations were compared for medium-voltage drive application under different types of loads.

1.4 Dissertation Motivation and Objective

According to the performed literature survey, there was lack of a comprehensive study for evaluation of the topologies used for industrial motor drive application at higher voltages (> 4 kV) in the medium-voltage range. In this dissertation, a comparison is made between topologies used for motor drive application in 4.16-13.8 kV voltage range. For this purpose, the cascaded H-bridge, modular multilevel converter and five-level active neutral point clamped converters are designed to realize medium-voltage high-power industrial drive at 4.16-, 6.9- and 13.8 kV voltages and 3- and 5 MVA output powers. Design is done at different voltage and power ratings so that a comparison can be made among the topologies versus operating condition, to help selection of best converter for given operating point. Also, the design is performed using existing Si IGBTs (both

low-voltage (LV) and MV Si IGBTs for CHB and MMC topologies, and MV Si IGBTs for 5-L ANPC topology as done in industry) as well as the state-of-the-art non-commercial 3.3 kV SiC MOSFETs (introduced in [15] and thoroughly characterized in [63]), in order to find the answer to the following questions: 1- How do the topologies compare to each other when designed using commercially-used Si IGBTs? 2- What is the impact of emerging medium-voltage SiC MOSFETs on medium-voltage drives at different operating points? The converters are fed from a 13.8 kV grid by means of a diode front-end rectifier. Leakage parameters of the transformer used in rectifier stage as well as the switching times and deadtimes of each semiconductors are included in converter models developed in MATLAB environment. In order to have a fair comparison between semiconductor technologies, the electro-thermal properties of the semiconductors are interpolated versus current rating for calculation of the minimum current rating (die size) device for each converter, while satisfying thermal criteria. Based on the design data, converters are compared to each other from different aspects such as efficiency, passive components, semiconductor utilization (total installed die area in converter system), power density, low-speed operation, fault containment and number of parts (for a measure of reliability). Last but not least, based on experimental results achieved from an H-bridge cell made based on the investigated 3.3 kV SiC MOSFETs, validity of converter modeling and thermal calculations are verified.

1.5 Dissertation Outline

This dissertation is organized into eight chapters.

In chapter 2, the state-of-the-art non-commercial 3.3 kV SiC MOSFETs of Sumitomo Electric Industries Ltd. are characterized. In order to assure best performance out of the devices under test,

high-performance gate drivers are designed with embedded protections, high gate current capability, high noise immunity and proper isolation. Since the gate drivers are being designed for operation in medium-voltage dc bus (2 kV dc bus for 3.3 kV semiconductors under test), an exclusive study is done to investigate creepage, clearance and material brakedown requirements on printed circuit board (PCB) design. Following the gate driver design, static and dynamic characterizations are performed under a variety of conditions in order to derive a complete picture of the performance featured by the 3.3 kV SiC MOSFETs under study.

Chapter 3 gives an overview of the converter under study for medium-voltage high-power motor drive application. For this purpose, the basics of operation, modulation methods and control schemes are surveyed for the cascaded H-bridge (CHB), the modular multilevel converter (MMC) and the five level active neutral point clamped converter (5-L ANPC) converters. Also, a novel optimization method is proposed to reduce size of arm inductors and submodule capacitors in case of the modular multilevel converter, which results in reduction of arm inductors up to 90% and submodule capacitors up to 40%.

In chapter 4, the converter modeling and design criteria are explained for the investigated topologies in motor drive application. Also, the electro-thermal properties of the semiconductors (such as switching losses and junction-to-case thermal impedances) are interpolated versus rated current, in order to assure utilization of the minimum current rating switch for the designed converters. This is a necessary step to ensure fair comparison between different converters, as well as different semiconductor technologies. Moreover, the loss calculation method and the approach to calculate the junction temperature of the semiconductors is explained. The criteria for

determining the switching frequency of the converters is adopted from catalogs of commercial motor drive converters, and the data for the designed converters are brought in tables.

Chapter 5 brings the comparison results for the converters under study. The three mentioned converters (CHB, MMC and 5-L ANPC) are compared to each other in terms of efficiency, power density, energy storage requirement, semiconductor utilization, low-speed operation capability, fault containment and parts count (for a measure of reliability). The comparison is done at all of the target voltage and power ratings (3.16-, 6.9- and 13.8 kV voltage ratings as well as 3- and 5 MVA power ratings). The comparison tries to evaluate the target topologies using both conventional 1.7-, 3.3- and 4.5 kV Si IGBTs and the state-of-the-art 3.3 kV SiC MOSFETs. The comparison results can be used as input for selection of the most appropriate topology for a motor drive converter at given operating voltage and power.

In chapter 6, experimental results are brought from an H-bridge cell made based on the investigated 3.3 kV 400 A SiC MOSFET modules, in order to provide proof of validity for the performed converter modeling in simulation environment. A 3.3 kV 1200 A Si IGBT is used in series with the H-bridge cell in order to saturate/cut off the current in case of failure in the system. The H-bridge cell operates in voltage-source inverter (VSI) mode with 7 kW of active power at 0.9 power factor. Using the implemented experimental setup, the converter output data and the thermal calculations are compared to the results achieved from simulations. The achieved results from experiments are very close to the simulated results, and they prove validity of the performed analysis and calculations.

In chapter 7, a novel method is proposed for balancing voltages across fast-switching series-connected SiC MOSFETs. The proposed method takes advantage of a small Miller capacitor to generate additional gate current to SiC MOSFETs to control their switching speed. The amount of losses created in control circuit are negligible, and it is shown by means of experiments that this method does not considerably modify (increase) switching losses of the semiconductors as well. Also, the proposed method is specifically designed for fast-switching SiC MOSFETs, on which majority of the existing voltage balancing schemes cannot be used. 1.7 kV SiC MOSFETs from GE are used as devices under test to prove validity of the proposed voltage balancing technique. First, a valid model is derived in SABER environment for the SiC MOSFETs using double-pulse tests (DPT) in a simple chopper circuit. Then, using the derived model and also considering the parasitic impedances of the circuit, effectiveness of the proposed method is proved via simulations. Finally, a gate driver is designed embedding all required functionalities and protections, as well as the proposed voltage balancing method.

Finally chapter 8 provides conclusions of the work with the summary of actions taken and the directions for future work.

Chapter 2. Characterization of the State-of-the-Art 3.3 kV Full-SiC MOSFETs

The latest generation 3.3 kV full-SiC MOSFETs were provided to Center for Power Electronics Systems (CPES) by Sumitomo Electric Industries Ltd (SEI). Due to lack of commercial gate drivers for the SiC MOSFETs especially at higher voltages, the manufacturers are usually unable to derive a complete picture of the characteristics featured by their prototype semiconductors. In other words, when it comes to SiC MOSFETs, the commercial gate drivers which are mostly developed for Si IGBTs face several limitations including voltage isolation, limited gate-driving current, required protections, dv/dt immunity and footprint (for minimizing gate loop inductance which is critical for SiC MOSFETs). Thus, before performing the study on impact of medium-voltage SiC MOSFETs on medium-voltage high-power motor drive applications, the SiC MOSFETs must be characterized.

The 3.3 kV SiC MOSFETs received from SEI consist of four discrete 30 A MOSFETs in TO-247 package, as well as three 400 A half-bridge modules with free-wheeling diodes (FWD) inside the package. The detailed characterization procedure will be presented in next sections.

2.1 PCB Design Considerations at Medium Voltages

The first step toward characterizing the SiC MOSFETs under study is to design proper gate drivers for them, capable of operating the DUT's at their highest capability while safety of the procedure is guaranteed. Since the gate drivers are being designed for operation at medium-voltage

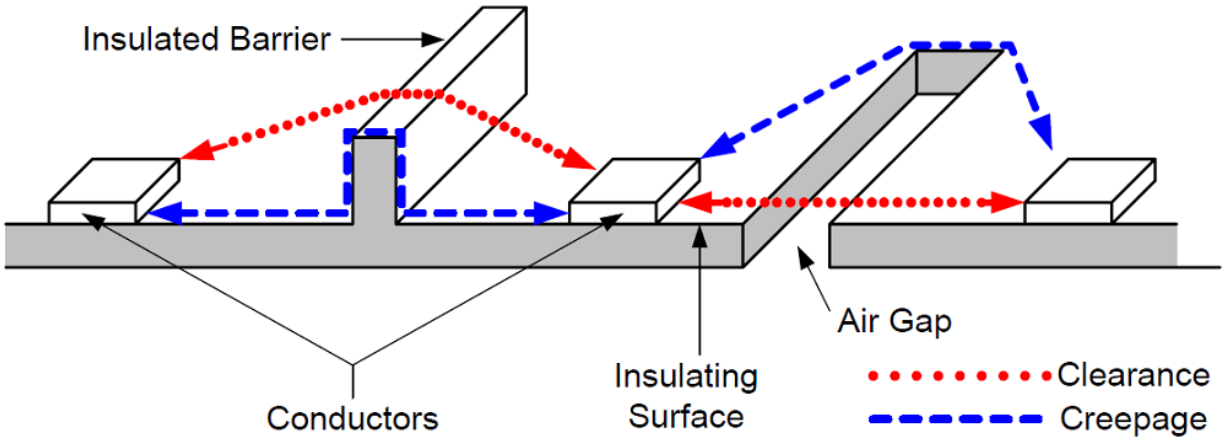


Figure 2.1 Definition of creepage and clearance distances on a PCB. Insulated barriers and keep-out layers can be used to increase the creepage distance.

range, it is vital to investigate creepage, clearance and material brakedown requirements for medium-voltage PCB design.

Figure 2.1 demonstrates creepage and clearance distances on PCB surface. According to their definition, creepage distance is the closest distance between two conductors on a surface while clearance is the closest distance between two conductors via air. When designing a PCB for a medium-voltage application, creepage distance requirements need to be satisfied in order to prevent any failure on it. According to figure 2.1, inserting insulated barrier or using keep-out layers can be used to increase creepage distance on a printed circuit board.

Total of four standards are surveyed in order to specify the minimum creepage distance requirement on the designed PCBs. UL 60950-1, “Information technology equipment safety-part 1: General Requirements” [64], IPC 2221A and IPC 2221B, “Generic PCB design standard for commercial and industrial applications” [65], [66] and finally IPC9592, “Performance parameters for power conversion devices” [67] are surveyed and based on them, 2 mm creepage per 1000 V distance is targeted for the inner and coated layers of the PCBs. It is worth to note that in case of

the uncoated surfaces, the creepage distance needs to be larger. For instance, according to [67] the minimum creepage distance for uncoated surfaces of PCB can be calculated from (2.1).

$$Creepage \ \ (mm) = 0.6 + V * 0.005 \tag{2.1}$$

Where V is the DC or RMS AC voltage between the conductors.

Another main consideration in PCB design for medium-voltage applications is material breakdown. Table 2.1 shows the maximum operating temperature, the nominal brakedown voltage and the aged brakedown voltage (after material aging and also considering manufacturing impurities) for 5 popular materials used to make PCBs [68]. According to a survey, FR-4 material is used by designers on PCBs up to 3 kV. The data from table 2.1 can be used to determine proper thickness the FR-4 material for making the target gate drivers operating at 2 kV dc bus.

The high-voltage nature of the gate drivers also makes it necessary to pay attention to prevent arc-overs and corona. Direct arc-over happens when voltage potential between two conductors exceeds the dielectric's ability to withstand it. Also, corona discharge occurs due to degradation

Table 2.1 The key characteristics of five popular materials used in PCB manufacturing [68].

Material Type	Maximum Operating Temperature (˚C)	Nominal Breaking Voltage (V/mil)	Aged Breaking Voltage (V/mil)
FR-4	105-130	800	150-300
High-temperature FR-4	130-150	800	150-300
BT Epoxy	140-160	1300	400-600
Polyimide	150-190	900	500-700
HVPF	180-200	3000-7000	2000-3000

of the insulation systems in a gradual manner. It is worth to note that the corona is the predominant failure mechanism in high-voltage circuits.

According to [68], in order to reduce the chance of arc-over and corona it is of great importance to restrict the electric field by preventing sharp conductor corners. Figure 2.2 shows examples of bad pad and corner designs where due to existence of high electric fields on the edges of the conductors, chance of failure is high. Also, examples of proper pad and corner design are shown.

Finally, in PCB design it is recommended to keep high-voltage traces away from PCB edges. This is due to the fact that copper is difficult to machine smoothly, so the edges are kept rough. It is recommended by guidelines in [68] to keep high-voltage PCB traces at least 0.001” per 100 V away from the edges, with a minimum of 0.020”.

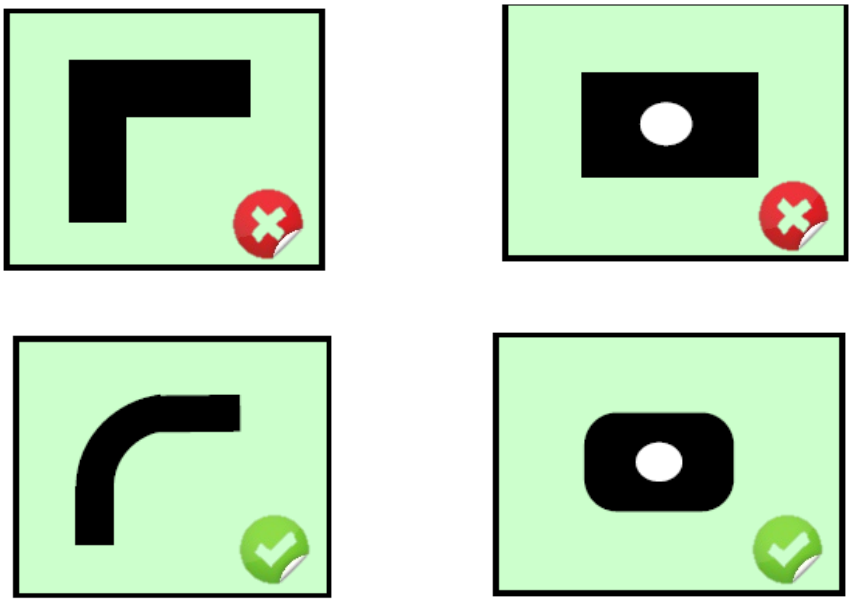


Figure 2.2 Examples of proper and improper pad and route in medium-voltage PCB design [68].

2.2 Circuit Design and Characterization of 3.3 kV 30 A Discrete SiC MOSFETs

This section shows the gate driver design, test setup design and characterization process for 3.3 kV 30 A full-SiC MOSFETs received from Sumitomo Electric Industries Ltd. Total of four discrete MOSFETs are delivered to the Center for Power Electronics Systems in TO-247 package, where the samples are in two types (with small differences in gate structure). Also, the MOSFETs are DMOSFETs with 36 mm^2 of die size. Table 2.1 shows the key parameters of the tested SiC MOSFETs.

As mentioned before, the first step to characterize the SiC MOSFETs under study is to develop a gate driver capable of properly driving the MOSFETs while safety of the tests are guaranteed. Figure 2.3 shows the overall schematics of the gate driver designed for this purpose. As it can be seen, the discrete 3.3 kV 30 A SiC MOSFET in TO-247 package is shown as device under test (DUT). The top switch is a 3.3 kV 30 A schottky barrier diode also provided by SEI, and the load is a 0.9 mH inductor. The inductor EPC together with junction capacitance of the diode will contribute to the switching-on transient [69]. For that reason it is of great importance to minimize the inductor EPC to minimum possible amount. In this work the designed inductor has about 13 pF of EPC which is negligible in front of junction capacitance of the diode which is hundreds of pF

Table 2.2 The key parameters of the SiC MOSFETs under study from SEI.

Part Number	Internal Gate Resistance (Ω)	Recommended Driving Voltages (V)	Nominal Current Rating (A at 25˚C)	Die Area (mm^2)
Type A, #1 (A1)	0.635	-5/+15	30	36
Type A, #2 (A2)	0.647	-5/+15	30	36
Type B, #1 (B1)	1.125	-5/+15	30	36
Type B, #2 (B2)	1.107	-5/+15	30	36

at nominal voltage. Also the inductor saturation current is above 100 A to prevent its saturation under switching transients.

The devices being tested are sample products and like any other device they are prone to failure especially under high-temperature tests. In order to prevent any damage to the setup, measurement units such as the oscilloscope and the user, an IGBT desaturation overcurrent protection is designed and connected in series between the busbar system and main test circuit (figure 2.3). A shunt resistor with 2 GHz bandwidth is used for measurement of the drain current. It is worth to note that the switching waveforms resulting from the DPT are rich in high-frequency harmonics. Thus, it is of great importance to use high-bandwidth measurement methods to capture accurate waveforms for calculation of the corresponding switching losses.

The double-pulse test consists of giving two pulse to gate of the device under test. According to figure 2.4, the first pulse turns the DUT on and inductor current starts rising. Once the inductor

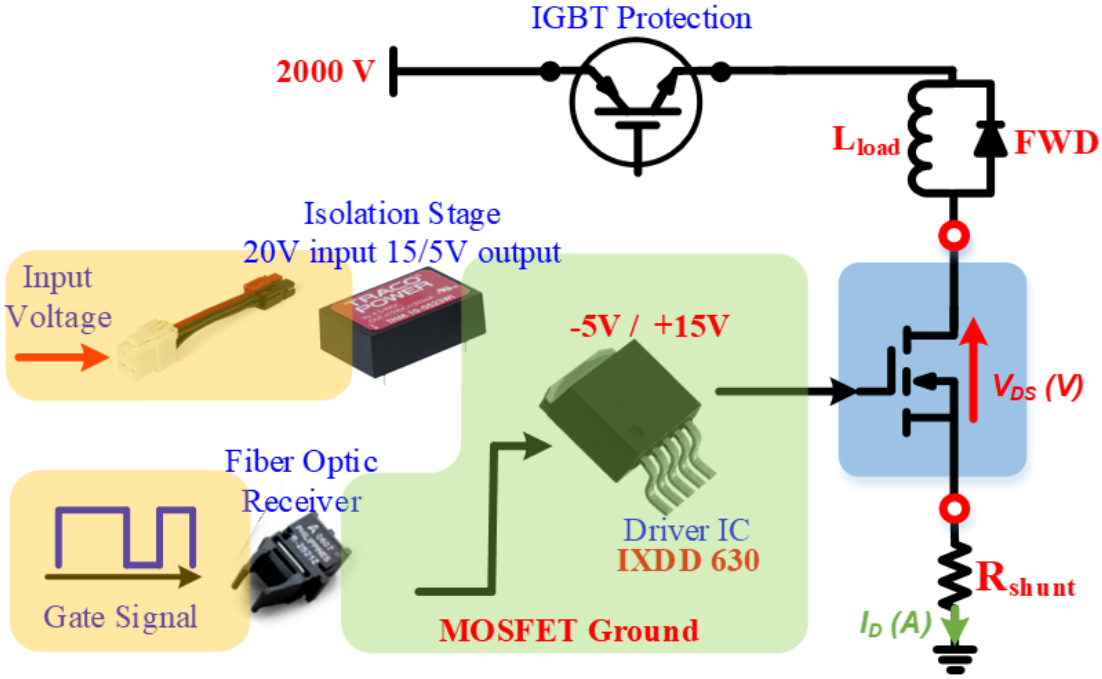


Figure 2.3 Overall schematics of the gate driver and DPT setup for the discrete 3.3 kV SiC MOSFETs.

(load) current reaches a desired value, the DUT is switched off and the turn-off waveforms are captured for calculation of the turn-off losses. After a deadtime (which is enough to damp the switching ringing, but still is short so that the inductor current does not change significantly), the DUT is switched on again to capture turn-on characteristics. Once the turn-on waveforms were recorded, the device can switch off assuming the test is accomplished.

The designed PCBs for double-pulse test and IGBT overcurrent protection are shown in figures 2.5 and 2.6, respectively. It is worth to note here that in order to minimize the gate and power loop inductances for the DUT, repetitive Q3D simulations are done. Also as it can be seen, on order to satisfy the creepage distance requirement keep-out layers are made on both of the PCBs. Finally, the implemented test setup is shown in figure 2.7.

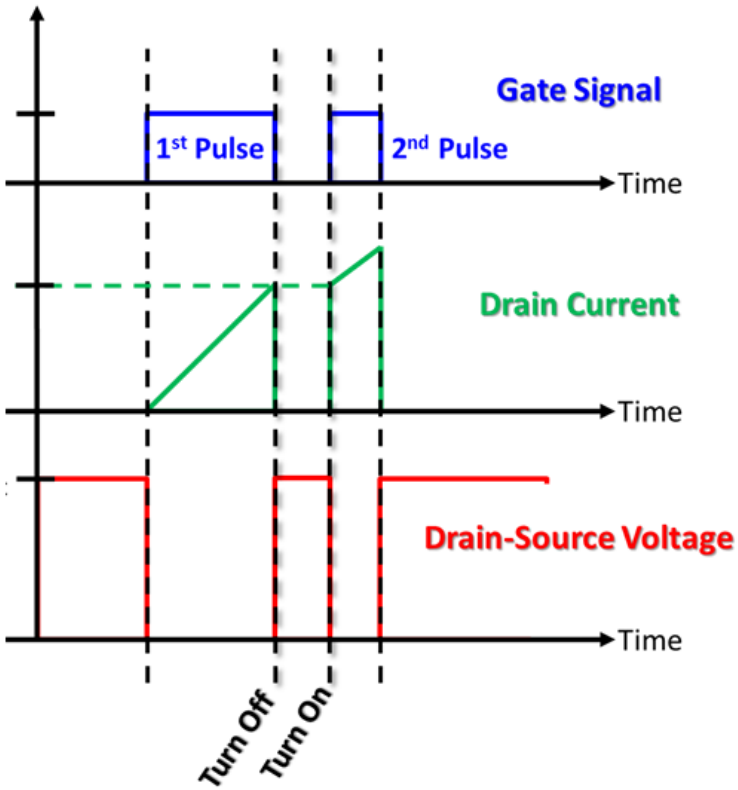


Figure 2.4 Fundamentals of double-pulse test.

2.2.1 Static Characterization of the MOSFETs udner study

All the static characterizations in this section are conducted by B1505A curve tracer from Agilent Technologies from room temperature up to 150°C. For high temperature measurements a hot plate is utilized and the device is mounted on it.

Figure 2.8 shows the drain current (I_D) versus drain-to-source voltage of the MOSFET (V_{DS}) at 25°C and 150°C. The reported output characteristics are measured at 15 V gate-to-source voltage (V_{GS}), and the positive coefficient in on-state resistance is coming from positive temperature coefficient of JFET region resistance and drift layer resistance inside a MOSFET [70]. Comparison of results to those of a 3 kV 30 A Si IGBT counterpart reveal that for the whole range of load

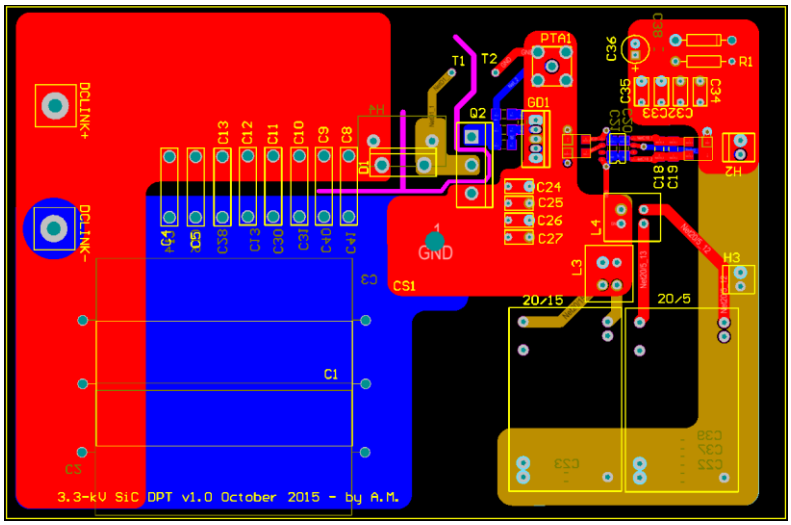


Figure 2.5 PCB designed for the double-pulse tester.

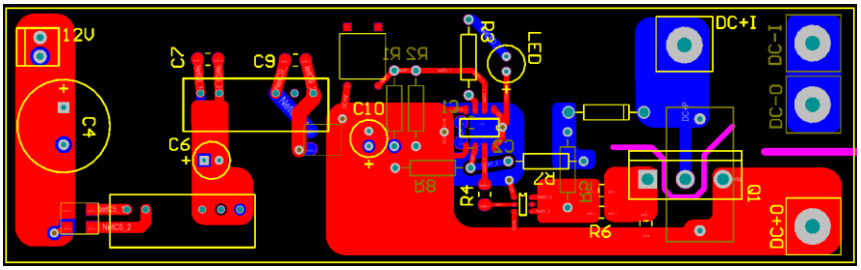


Figure 2.6 PCB designed for the IGBT overcurrent protection circuit.

current, SiC MOSFETs will have smaller conduction loss than Si IGBT. Also the on-state resistance is lower for type A in comparison to type B. Note that the high-temperature output characteristics of the Si IGBT are not included in figure 2.8 since the datasheet was not providing that information.

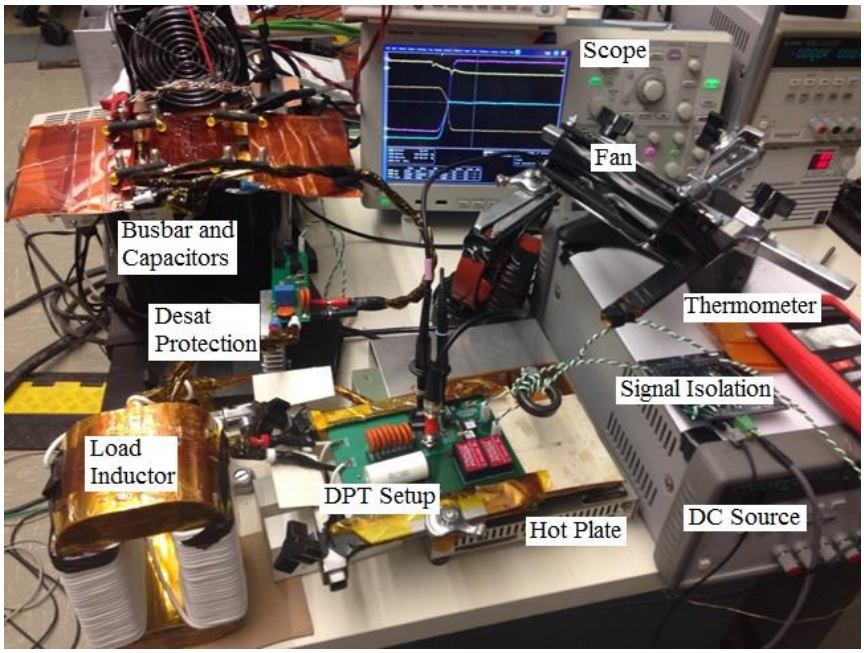


Figure 2.7 The implemented double-pulse test setup with components specified.

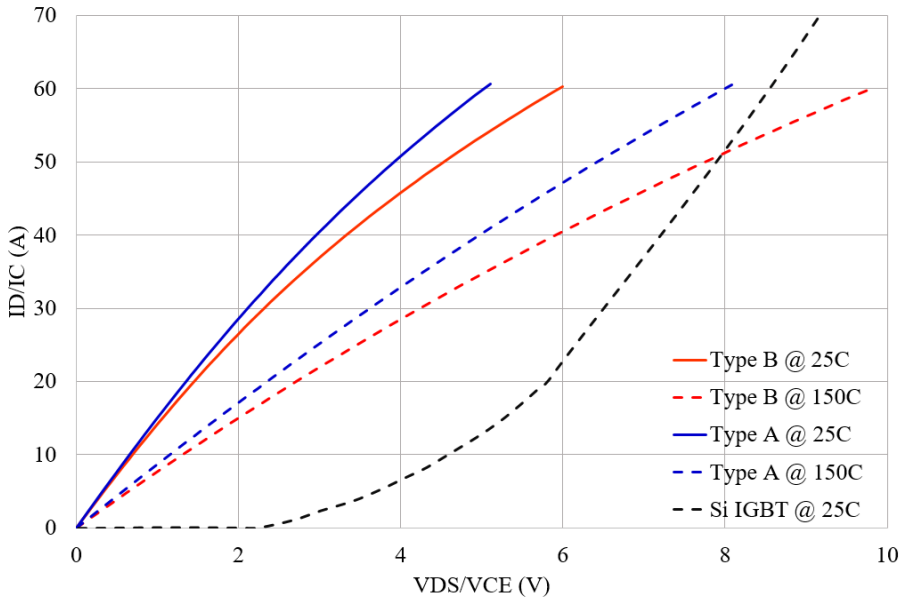


Figure 2.8 Output characteristics of the investigated 3.3 kV 30 A SiC MOSFETs.

The transfer characteristic gives a measure of threshold voltages of the devices, as well as their gain at constant V_{DS}. Transfer characteristics of the MOSFETs at 20 V drain-to-source voltage are shown in figure 2.9 at room and high temperature. The positive temperature coefficient of transconductance (meaning that transconductance increases with increase in temperature) seen from figure 2.9 is due to increase in the MOS channel inversion charge and inversion mobility as temperature increases [71].

The on-state resistances were measured for each of the MOSFETs at two temperatures. The on-state resistances of the DUTs are brought in figure 2.10, where based on data from table 2.2, the specific on-resistance is approximately 24 mΩ.cm^2 and 26.5 mΩ.cm^2 for type A and type B SiC MOSFETs, respectively. On-resistance change with temperature happens in a linear manner, thus for calculating the on-resistance at any given temperature between room temperature and 150°C, interpolation of the results will be the solution.

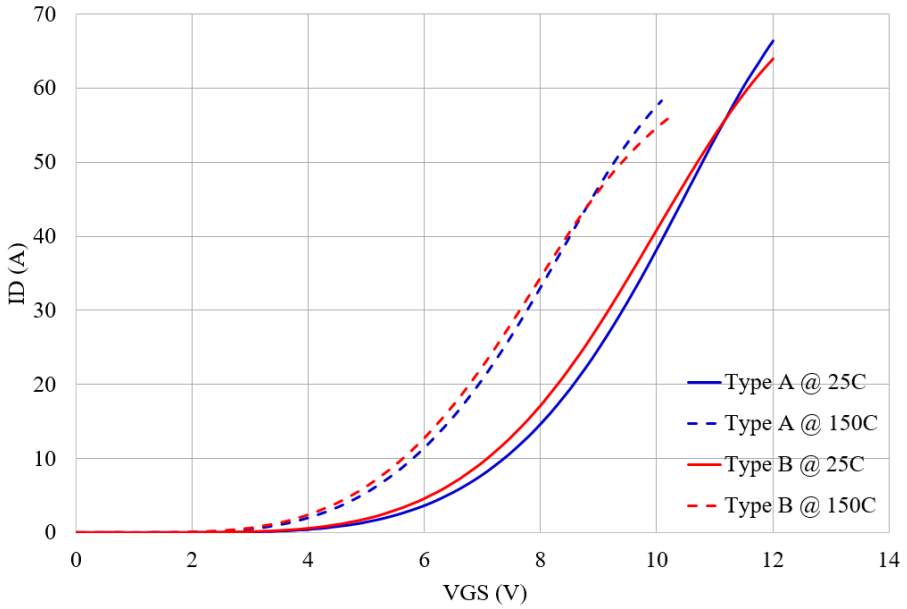


Figure 2.9 Transfer characteristics of the investigated 3.3 kV 30 A SiC MOSFETs.

Figure 2.11 demonstrates a plot of threshold voltages versus temperature for all SiC MOSFETs investigated. In this study, the threshold voltage was defined as the voltage across gate and source where a drain current of 50 mA flows while drain-to-source voltage is 20 V constant.

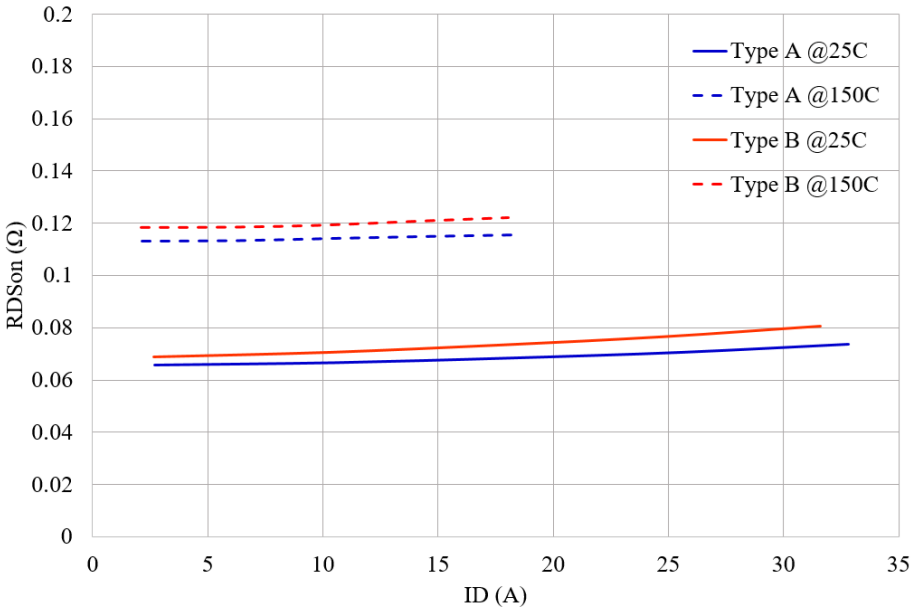


Figure 2.10 Specific on-resistances of the investigated 3.3 kV 30 A SiC MOSFETs.

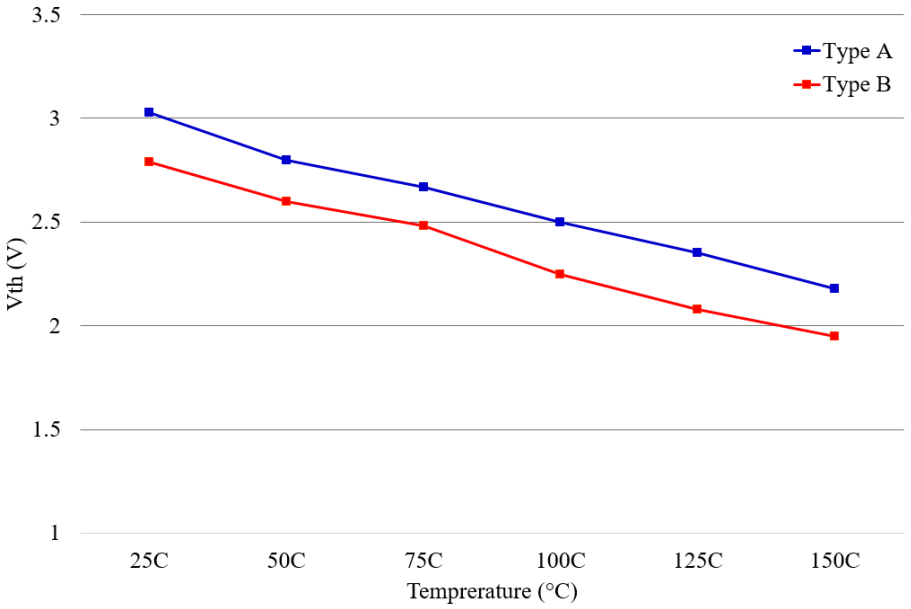


Figure 2.11 Threshold voltages of the investigated 3.3 kV 30 A SiC MOSFETs.

According to figure 2.11, the type B MOSFETs have lower threshold voltages than type A, which makes it more necessary for these devices to be driven by negative bias voltage at turn-off state in order to ensure than no false turn-on will occur. The negative temperature coefficient of threshold voltage for SiC MOSFETs is coming from increase in intrinsic carrier concentration with increased temperature [72].

The junction capacitances of all SiC MOSFET samples were measured using Agilent Technologies B1505 curve tracer under variant DC voltage up to over 1400 V and at 100 kHz frequency. This measurement is done only at room temperature since junction capacitances are temperature invariant [69]. In this study measurement of the input capacitance C_{iss} ($=C_{GS}+C_{GD}$), output capacitance C_{oss} ($=C_{DS}+C_{GD}$) and miller capacitance C_{rss} ($=C_{GD}$) are performed and the results are shown in figure 2.12.

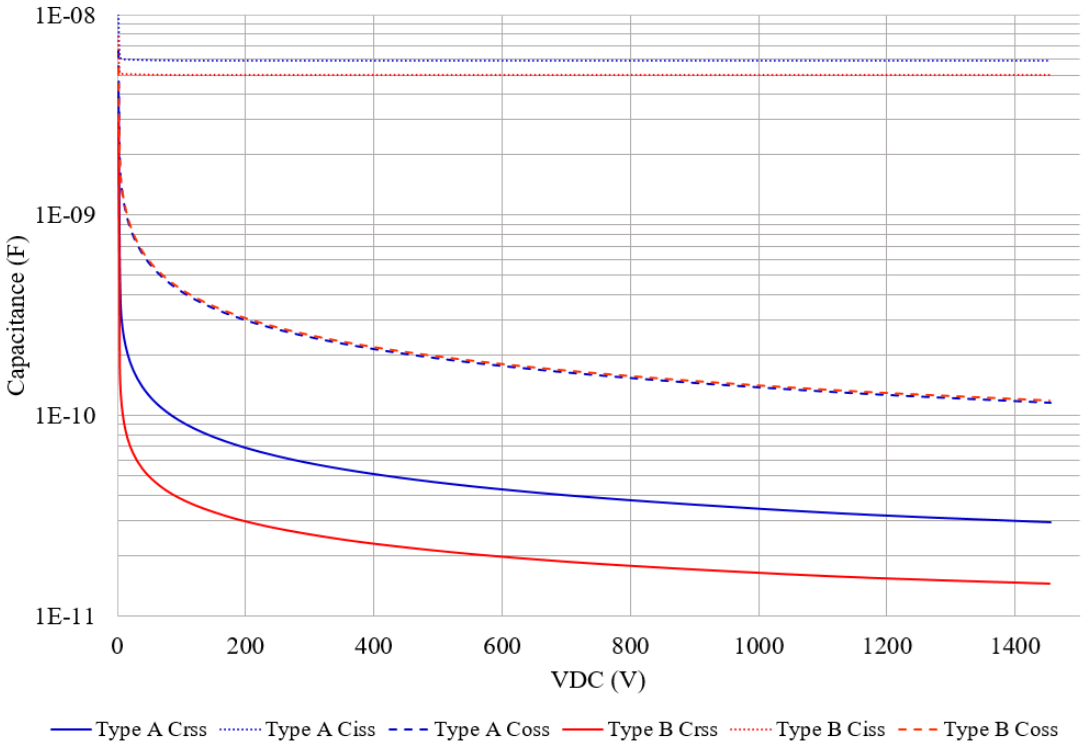


Figure 2.12 Junction capacitances of the investigated 3.3 kV 30 A SiC MOSFETs.

According to figure 2.12, type B MOSFETs have smaller input capacitance than type A, which will feature lower switching losses for them. A smaller input capacitance will result in smaller time constant for the gate loop, and thus resulting in shorter switching times and smaller switching losses. Also from figure 2.12, the output capacitances are the same for all semiconductors, due to similar chip size. The output capacitance mainly contributes to the parasitic ringing during the turn-off transient because during device turn-off the current sees the drain-to-source parasitic inductance in series with the output capacitance. Last but not least, the miller capacitances of both sample types are also shown.

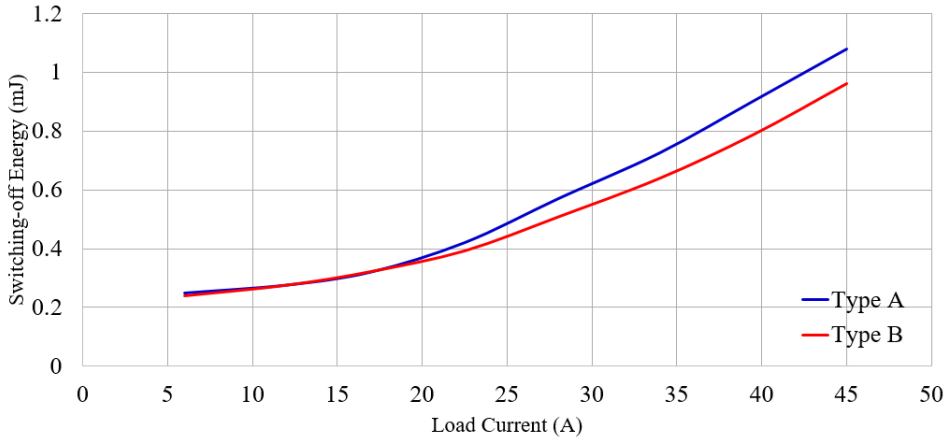
2.2.2 Dynamic Characterization of the MOSFETs udner study

Having double-pulse test setup prepared, the dynamic tests are done on all four samples in hand under different total gate resistances. According to table 2.2, the devices have different internal gate resistances. Thus, setting their external gate resistances to different amounts, four identical total gate resistances of approximately 3.65-, 4.45-, 5.35-, and 6.5 Ω are achieved and the DPT is done under these gate resistances. It is worth noting that in dynamic tests, the load current is increased in a stepwise manner from 5 A to 45 A in order to capture device losses versus current [73], [74]. It is worth to note that the switching speed is not increased by further reducing the gate resistance from 3.65 Ω since it seems at this gate resistance, the switching transient of device voltage is close to its blocking voltage rating.

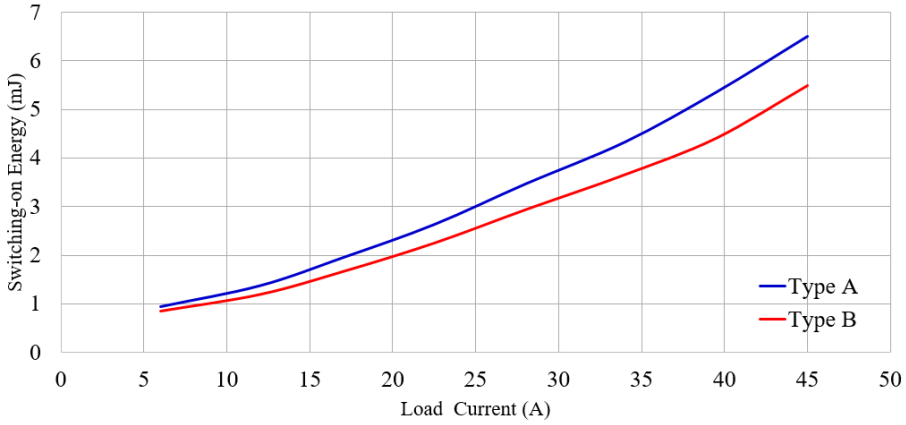
The switching-off and switching-on losses at 3.65 Ω total gate resistance are shown in figure 2.13(a) and 2.13(b), respectively. It is worth to note that the reported switching losses for each type are average of two available samples. As it could be predicted, the turn-off and turn-on losses

of the B type MOSFETs are smaller than that of A type. This is mainly because they have smaller input capacitance, which under the same gate resistance and voltage features smaller losses. Also, the switching-on losses are the dominant ones in case of SiC MOSFETs, so if soft-switching methods are used to eliminate turn-on losses, the converter efficiency can be significantly improved.

So that a comparison can be feasible versus gate resistance change, variation of switching energies versus gate resistance at 25°C and 45 A drain current is shown in figure 2.14. It is worth to mention that smaller gate resistances are prevented since the resulting dv/dt at 3.65 Ω gate



(a)



(b)

Figure 2.13 (a) Turn-off and (b) Turn-on losses of the studied SiC MOSFETs at 3.65 Ω gate resistance.

resistance is close to limits of the driver IC (~50 V/ns). The complete switching parameters are brought in table 2.3 for both types of MOSFETs.

In order to be able to test the devices at high temperatures, a hot plate is used to heat up the DUT. Referring to figure 2.7, the device leads are bent 90 degrees and mounted at the bottom of the PCB, in parallel with it. In this way the DUT can touch the hot plate and heated up in case needed. Also the device leads are as short as possible to make that connection, to minimize additional inductances in switching loop.

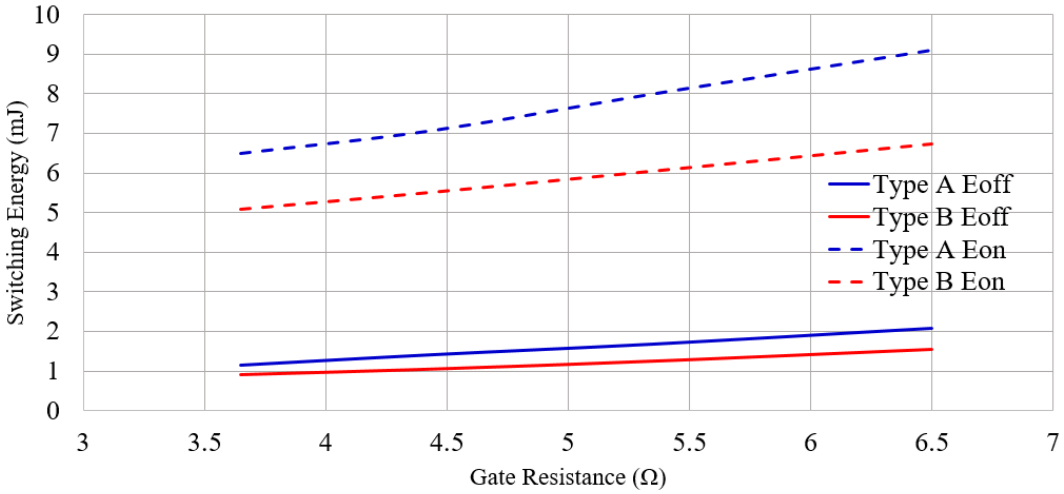


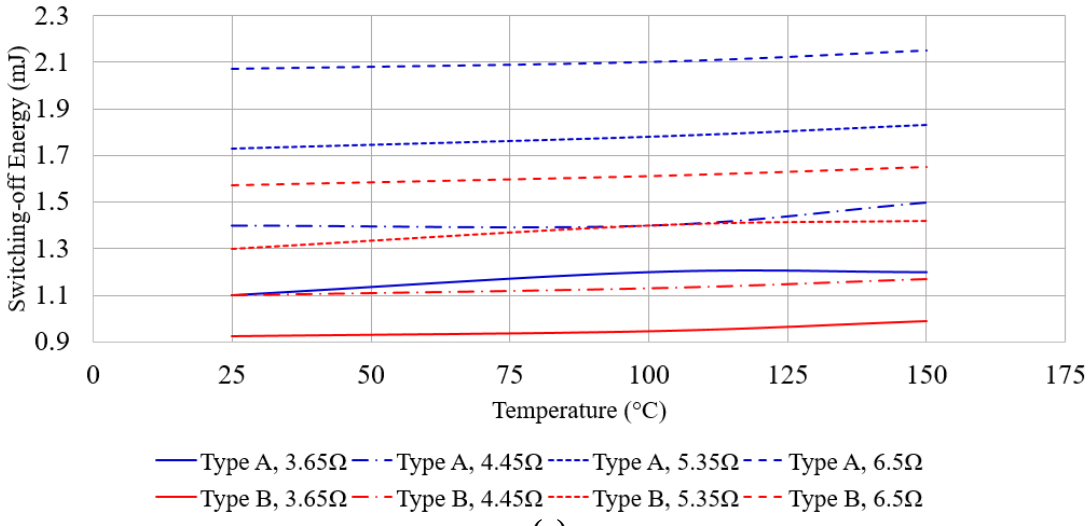
Figure 2.14 Switching losses of the tested SiC MOSFETs versus gate resistance at 45 A current.

Table 2.3 Switching parameters of the SiC MOSFETs under study.

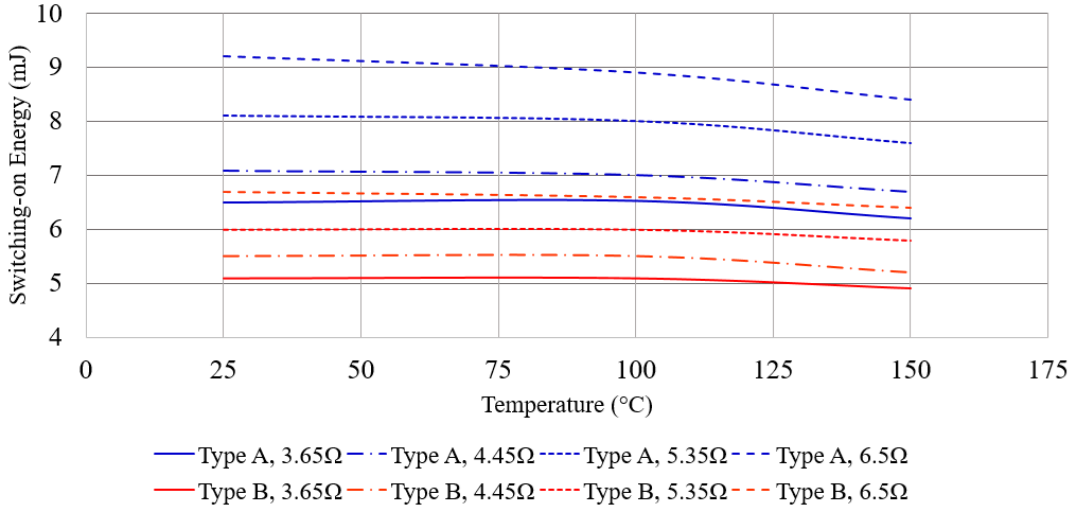
Parameter	Type A	Type B
Turn-off dv/dt	37.03 V/ns	47.69 V/ns
Turn-off voltage rise time	433.2 ns	33.55 ns
Turn-off di/dt	0.68 A/ns	0.76 A/ns
Turn-off current fall time	52.45 ns	47.2 ns
Turn-off time	111.55 ns	89.2 ns
Turn-on dv/dt	15.19 V/ns	2416 V/ns
Turn-on voltage fall time	105.3 ns	66.2 ns
Turn-on di/dt	0.91 A/ns	1.06 A/ns
Turn-on current rise time	39.35 ns	33.7 ns
Turn-on time	196.5 ns	139.5 ns

A thermal pad is applied on the hot plate in order to provide a uni-temperature surface. The temperature is being measured by a thermocouple whose probe is placed adjacent to the device under test. Isolation between device drain and hot plate (which is grounded) is achieved by using a Kapton tape layer on the hot plate applied under the thermal pad.

An important feature of SiC MOSFETs is negligible variation in losses versus temperature. Figures 2.15(a) and 2.15(b) are showing variation of turn-off and turn-on switching losses versus



(a)



(b)

Figure 2.15 Variation of (a) Turn-off and (b) Turn-on losses versus junction temperature at 45 A load current and different gate resistor values.

junction temperature for MOSFETs at three temperatures: 25°C, 100°C and 150°C. As it can be seen, the losses are pretty constant versus junction temperature. expected from a SiC MOSFET, the turn-off losses are slightly increasing and turn-on losses are reducing as temperature increases due to reduction in pleatue and threshold voltages, but the total switching losses are pretty constant. The total switching loss change at 150°C compared to 25°C is about 6%.

Last but not least, figure 2.16 shows switching-on and switching-off losses of 3.3 kV 30 A SiC MOSFETs together with those of Si counterpart. It is clear from this figure that the switching losses in case of SiC MOSFETs is negligible in front of those of Si IGBT. At 30 A load current, total switching losses of Si IGBT is about 8 times of SiC MOSFETs.

2.2.3 Evaluation of the Discrete SiC MOSFETs in a Converter System

So far the static and dynamic characteristics of the MOSFETs were derived and some of the parameters were compared to those of a Si IGBT at similar ratings as the tested SiC MOSFETs. In order to demonstrate outstanding performance of medium-voltage SiC MOSFETs compared to Si IGBTs, this section aims to compare performance of the tested devices to those of Si IGBTs in

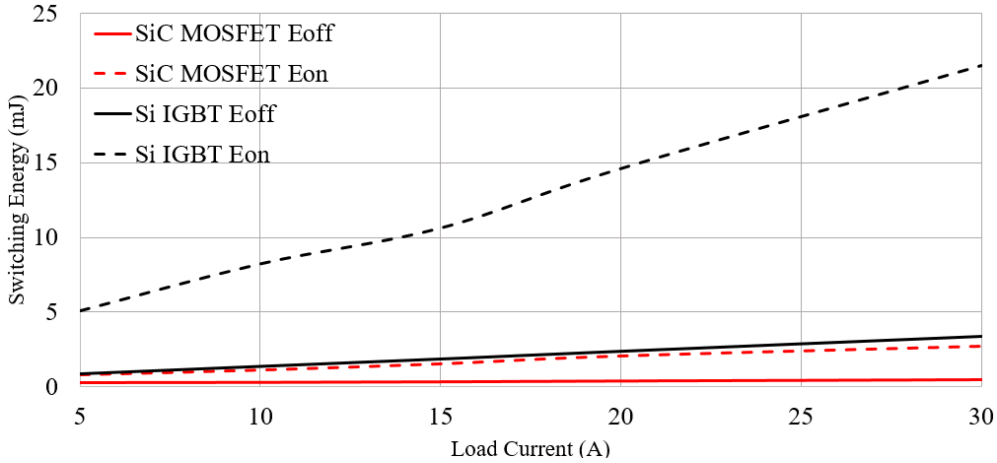


Figure 2.16 Comparison of switching losses between tested type A SiC MOSFETs and traditional Si IGBTs with similar voltage and current ratings.

a converter system. As shown in figure 2.17, a 5 kW boost converter system with 300 V input voltage and 2 kV output voltage is selected for this purpose. The switching frequency for individual semiconductors is set to 5 kHz. This study tries to answer two main questions:

1- At given power rating and switching frequency for converter system, what are system efficiency and volume (for measure of power density) using Si and SiC semiconductors?
2- At given power rating for converter system, what is the maximum switching frequency feasible using each of the semiconductor technologies?

The load capacitor in the boost converter is selected to restrict the voltage ripple to 2% dc value. Inductor is 20 mH and the load is an 800 Ω resistor. Two 1.7 kV 14 A SiC Schottky diodes are also used in series in the converter structure. The capacitor bank is composed of two 5 µF 3 kVDC capacitors in parallel, and the 20 mH inductor with saturation current of around 15-20 A is assumed to be made on AMCC 630 core.

A heat sink is designed in case of each semiconductor assuming 40°C temperature for it, while the ambient air is at room temperature. The maximum junction temperature of the die is restricted

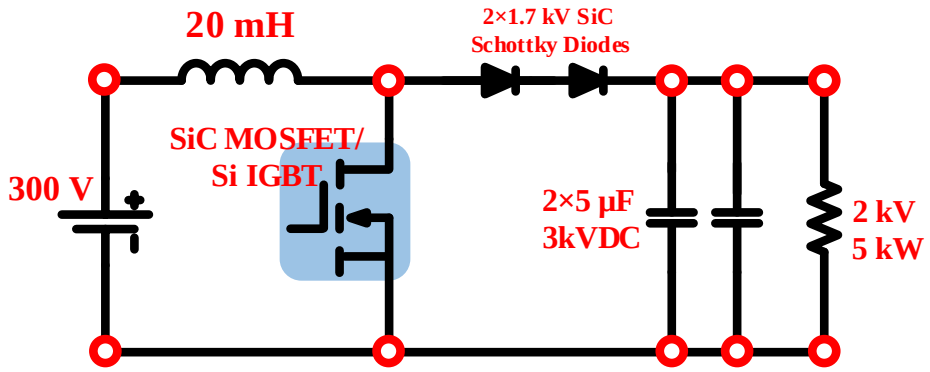


Figure 2.17 Boost converter system topology, used for evaluating the tested SiC MOSFETs versus Si IGBT counterpart.

to 90% of its maximum possible, as normally done in converter design. In this study the maximum junction temperature for Si IGBTs and SiC MOSFETs is 150°C, so the average junction temperature calculated from (2.2) is restricted to around 135°C. Also, the heat sink volume considering a naturally-cooled heat sink with cooling system performance index (CSPI) of 2.55 w/(°C.dm^3) calculated from a typical commercial air-cooled heat sink is estimated from (2.3).

$$T_j = T_{HS} + R_{jc} \times P_{loss} \tag{2.2}$$

$$T_{HS} - T_{amb} = P_{loss} \frac{1}{CSPI.Vol_{HS}} \tag{2.3}$$

where T_j is the average junction temperature of device under test, R_{jc} is junction to case thermal impedance, P_{loss} is total switch loss (conduction and switching) and Vol_{HS} is heat sink volume.

In first case study, the boost converter is continuously operating at 5 kHz switching frequency, delivering 5 kW of power to the load. Total converter losses composed of conduction and switching losses of the IGBT/MOSFET, as well as conduction loss of the SiC PiN diode used are shown in figure 2.18. As it can be seen, using type A MOSFETs features slightly smaller loss due

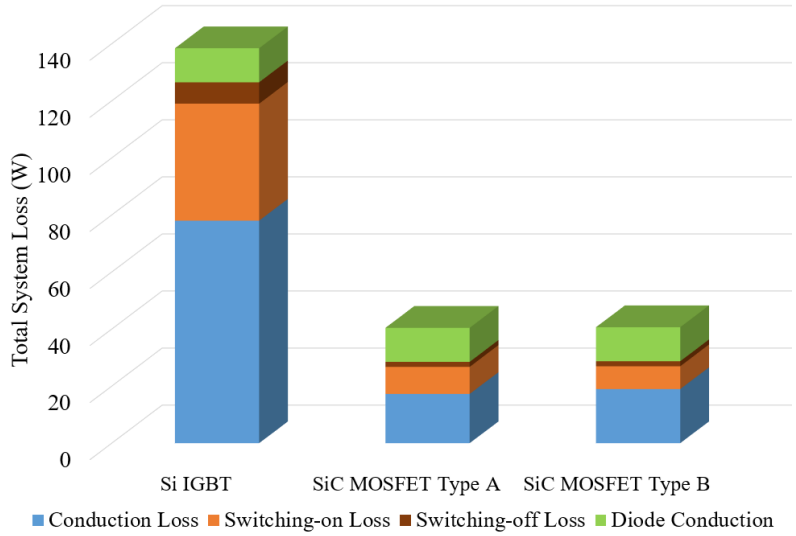


Figure 2.18 Total system losses for the boost converter system using Si IGBTs and SiC MOSFETs.

to their smaller conduction loss. Compared to conventional Si IGBT, both SiC MOSFETs tested feature significantly smaller losses due to both switching and conduction losses being smaller than that of Si. Total system efficiency using SiC MOSFETs is approximately 99.4%, which is significantly larger than 97.5% achieved by Si IGBTs. Also in this case the average junction temperature for Si IGBT is around 124.3°C, while type A and type B SiC MOSFETs are at 59.1- and 59.4°C, respectively.

On the other hand, figure 2.19 shows the converter size in dm^3, composed of the size of naturally-flown air-cooled heat sinks needed for diode and switch, capacitors and inductor. As the results demonstrate, using SiC MOSFETs the total converter size is reduced by 36%, which means the converter made by using SiC MOSFETs will have higher power density by a factor of 57%.

In second case study in order to investigate maximum switching frequency possible for each of the semiconductors, the switching frequency is increased until thermal criteria (~ 135°C junction temperature for switch) comes up. Obviously, in a boost topology the switching frequency does not need to be very high. However, there are certain applications such as grid-tied inverters,

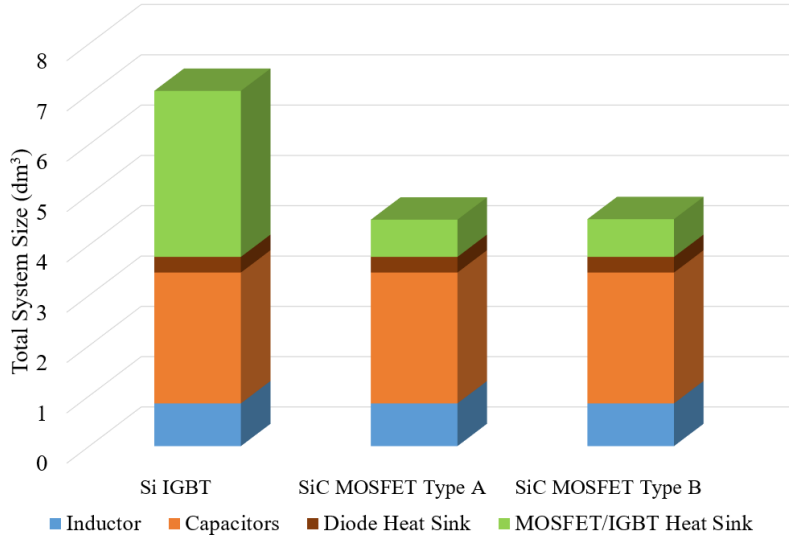


Figure 2.19 Total system volume composed of inductor, capacitor bank, and heat sinks.

motor drives using topologies such as modular multilevel converter and etc. where high switching frequency featured by individual semiconductors can be of interest.

The second study reveals that the maximum switching frequency for Si IGBT, type A SiC MOSFETs and type B SiC MOSFETs is 6.6-, 55.5- and 63 kHz, respectively. These numbers are calculated merely by considering thermal criteria, and does not take into consideration requirements for gate driver capable of such high frequency and so on. As it can be seen, the maximum switching capability of SiC MOSFETs is around 9-10 times of that of Si IGBTs, which can contribute to smaller size of passive elements and achieve higher power quality in several applications [75], [76].

2.3 Circuit Design and Characterization of 3.3 kV 400 A SiC MOSFETs

The 3.3 kV 400 A full-SiC MOSFET modules were also supplied to the center for power electronic systems by SEI. The module is based on the discrete type A MOSFETs investigated in the previous section. The module has free-wheeling diodes embedded inside it. The total chip size for each semiconductor inside the package is 432 mm^2, and the driving voltages are recommended to be -5/+15 V. Figure 2.20 shows the module package together with its pin configuration.

A gate driver needs to be used for the module in hand. When used in medium-voltage applications, the commercial gate drivers in the market need to satisfy three major requirements: isolation, driving current and protection. For isolation purposes on power and signal path, these gate drivers usually rely on isolation from the driver ICs which is limited to a few hundred volts. Also, in order to guarantee fast switching of the device enough gate current needs to be provided by the gate driver. As device current and voltage ratings increase, the junction capacitances

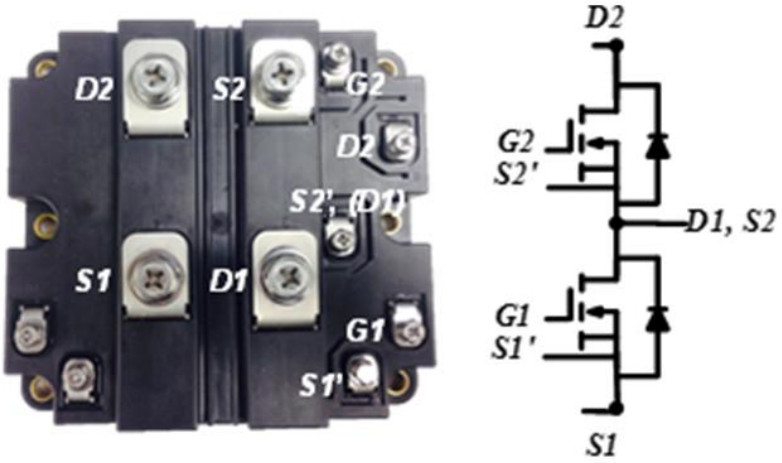


Figure 2.20 3.3 kV 400 A full-SiC MOSFET module with pin configuration diagram.

including the input capacitance increase as well and thus, device gate current requirement becomes higher. Finally, protections provided by the gate driver need to satisfy requirements of the application they are being used in. Other considerations such as *dv/dt* immunity, footprint etc. may also be taken into account when choosing a gate driver.

In order to achieve the best performance from the DUT while safety of the operation is guaranteed, a high performance gate driver is designed by surveying and applying gate driver and medium-voltage PCB design consideration (surveyed in section 2.1). The first step toward gate driver design is determination of required functionalities and protections. For the 400 A module, undervoltage lockout (UVLO), overvoltage lockout (OVLO), soft turn-off, overcurrent protection and active Miller clamping are targeted to be provided by the gate driver.

In case of malfunctioning in a power supply or other components on gate driver causing change in driving voltages, both conduction and switching losses of the MOSFET will change. This can also be detrimental to gate oxide layer, causing damage to the MOSFET. UVLO and OVLO are employed so that the power supply voltage can be monitored.

In case of overcurrent/short-circuit detection, depending on the magnitude of drain current hard turn-off can damage the device because of high voltage overshoot. In order to prevent this, a two-level soft turn-off is being predicted in the gate driver circuit [77]. Desaturation overcurrent protection (also known as DESAT) is the conventional method used for IGBTs, where the emitter current is detected by monitoring the collector-to-emitter voltage. Although DESAT protection is shown not to be as effective on SiC MOSFETs as is on Si IGBTs [78], it is embedded on the gate driver circuit and is sufficient for dynamic tests done in next section.

Last but not least, Miller effect is caused in a half-bridge module (figure 2.20) when positive *dv/dt* is generated across a switch as the result of switching in the other one [79]. The Miller current can create a glitch on gate signal and may lead to simultaneous conduction of both top and bottom switches in the module. Current sink is predicted on gate in order to absorb the miller current, and its capacity can be calculated from multiplication of Miller capacitance and device expected *dv/dt*.

Among commercially available driver ICs satisfying listed requirements, STGAP1S of STMicro is selected for driving the module. This IC has very low propagation delay (~100 ns) and is immune to *dv/dt* up to 50 *V/ns*. A microcontroller is also embedded in the gate driver system for controlling driver IC functionalities. Maximum gate current of the STMicro driver IC is 5 A, but considering gate charge of the MOSFETs (~5 µC), higher gate current is needed for proper switching of the device. On the present gate driver, total of 30 A gate driving current is provided by using three 10 A current boosters.

The required +15/-5 V driving voltages for each channel are provided by using two isolated power supplies with 5 kV isolation in continuous operation. Minimum power rating of the power supplies is calculated to be 9 W based on (2.4), assuming maximum switching frequency of

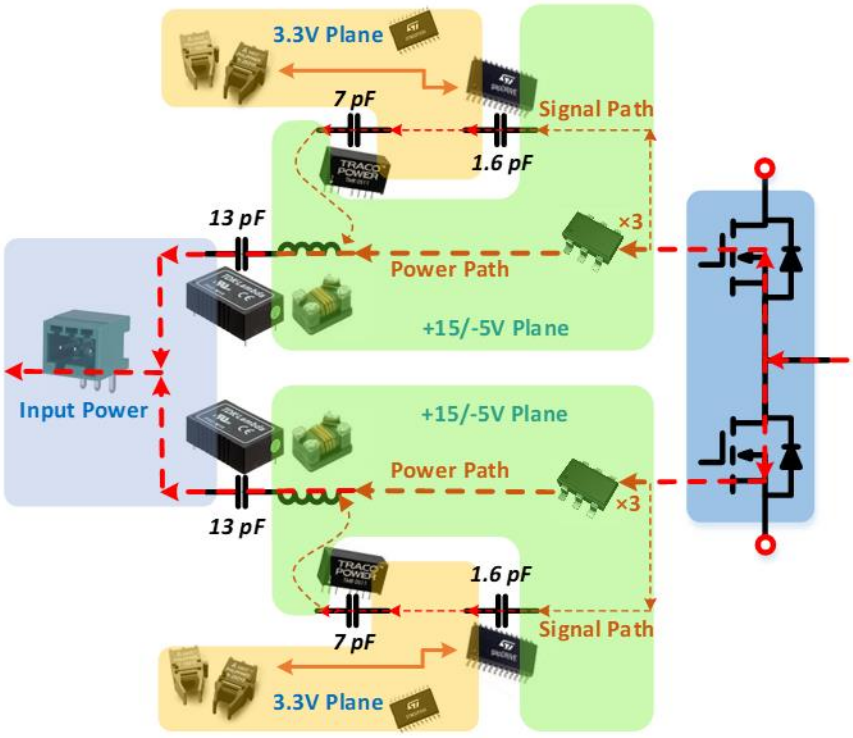


Figure 2.21 Schematics of the gate driver system and noise propagation paths.

100 kHz for the device. In this design a 2 W safety factor for steady-state losses of components on the driver board is assumed.

$$P_{gate} = Q_{gate} . f_{sw} . V_g \tag{2.4}$$

where P_{gate} is the minimum required gate (power supply) power, f_{sw} is switching frequency and V_g is the gate driving voltage. It is worth to mention that the gate driver communication with controller happens via fiber optics.

High *dv/dt* is the main cause of electromagnetic interference (EMI) that can penetrate to the digital controllers and create electromagnetic compatibility (EMC) problems in the system. Figure 2.21 shows overall schematic of the gate driver where noise propagation through power and signal paths are specified. The driver IC has very small isolation capacitance, measured to be 1.58 pF. In order to strengthen the signal path in front of EMI current, an isolated 3.3 V power supply with

minimum possible parasitic capacitance is used for microcontroller and driver IC, which will serve as a secondary isolation barrier for the signal path EMI. The smaller the parasitic capacitance, the less the EMI current will become due to its larger impedance. The main power supplies are also tried to have parasitic capacitance as small as possible. Also, CM chokes are series-connected with the main power supplies in order to provide high impedances at high frequencies. The proposed structure with impedance mismatch between power and signal paths provides higher noise immunity for signal path, which will feature less susceptibility for false turn-on as a result of CM noise [80].

The 6-layer PCB designed for the gate driver system is shown in figure 2.22. Also, the major parts are marked on the PCB. In figure 2.23, functionality of DESAT protection and soft turn-off systems are shown in experiments. DESAT protection level is set to around 500 A, and when

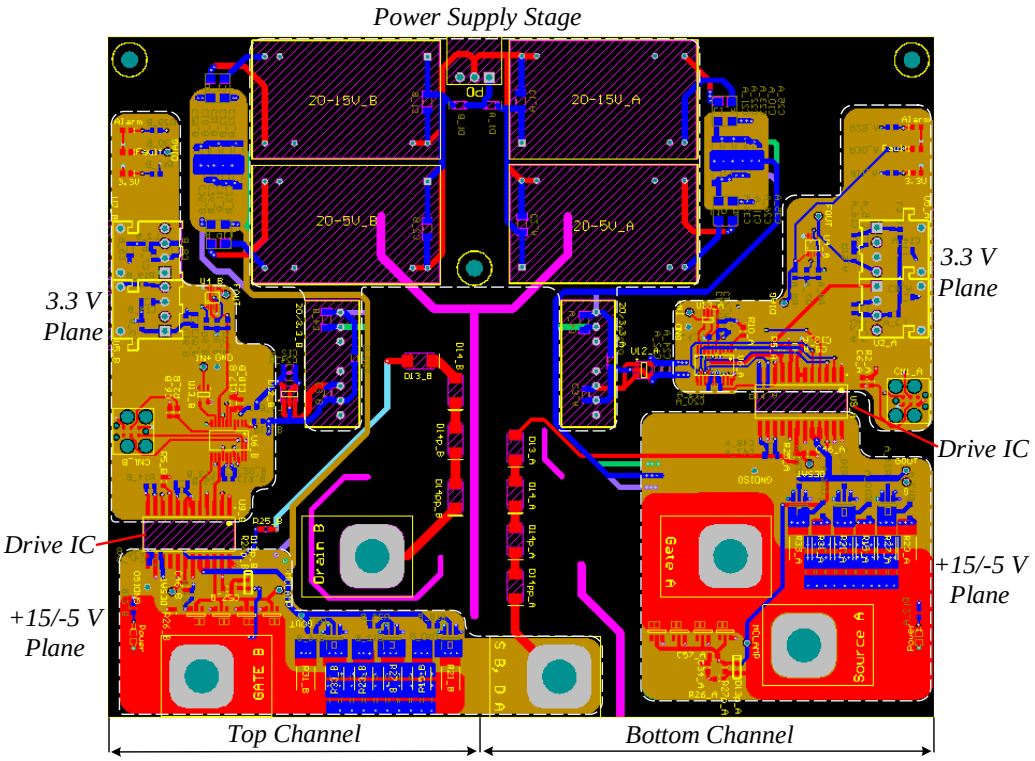


Figure 2.22 The 6-layer PCB layout for the designed gate driver.

triggered the gate driver turns off the MOSFET in two steps. First, the gate voltage (V_{GS}) is reduced to around 8 V, at which the drain-to-source voltage (V_{DS}) rises to a middle level (~ 1 kV) and consequently, the drain current (I_D) slope reduces (since the voltage across load is reduced). Then, the MOSFET is completely switched off. This feature reduces risk of device destruction due to huge voltage overshoot when the MOSFET turns off. It is worth to note that the middle level of gate voltage and time duration of two-level turn-off are both programmable (to higher voltages and shorter times) in the selected driver IC.

Having lower value for middle level of V_{GS} would further reduce V_{DS} overshoot at turn-off, and drain current would also have a two-level nature as done in [77] (reducing from fault current to a smaller current before completely switching off, resulting in safer turn off). However, the employed driver IC in first version of the gate driver was not able to provide small enough voltages at soft turn-off. Having waveforms acquired from first version of the gate driver as input will help selecting a more appropriate driver IC in future versions.

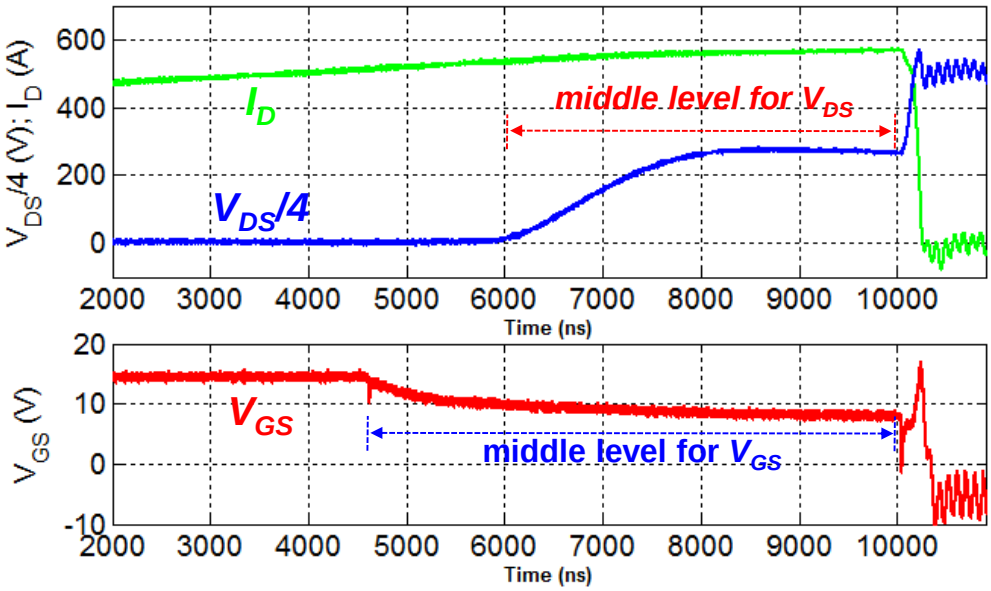


Figure 2.23 DESAT protection and two-level soft turn-off featured by the designed gate driver.

Gate drivers for 3.3 kV (or higher) SiC MOSFETs are not commercialized, but compared to commercial gate drivers for 3.3 kV IGBTs the designed driver features higher gate current, higher channel power (resulting in higher maximum switching frequency), higher *dv/dt* immunity and only 3nH of gate loop inductance where all are essential for SiC MOSFETs. Also required protections are embedded on the designed gate driver.

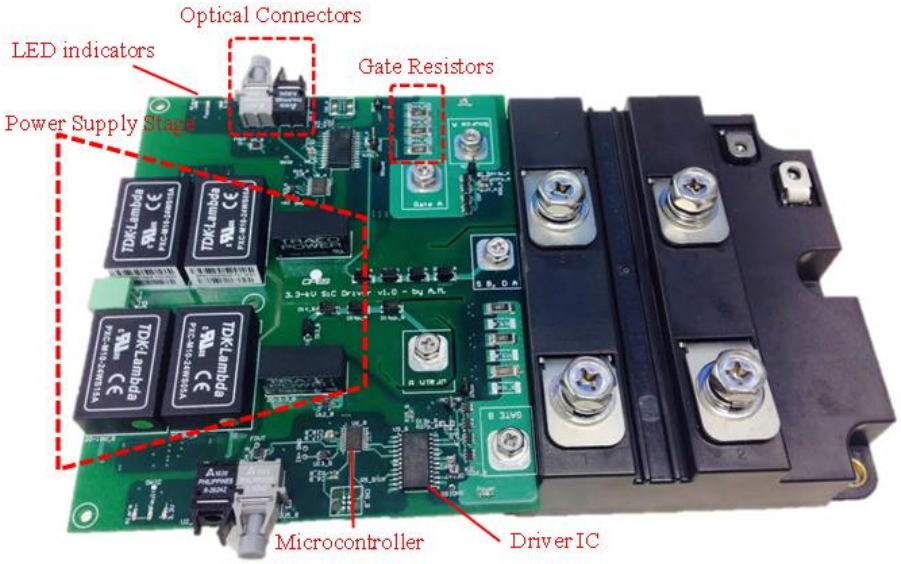
Having the gate driver designed, DPT setup is prepared as shown in figure 2.24 where the gate driver is connected to the device and device is mounted on a hot plate in order to run tests at high temperatures. A thermal pad is applied to the hot plate to create a uni-temperature surface. In order to minimize the effect of stray inductances of cables from power supply, a bulk capacitor bank composed of four 250 µF film capacitors is utilized with busbar connection to the device terminals. The busbar inductance is measured to be 17 nH. Also, three 100nF 3 kV film capacitors are paralleled and used for decoupling purposes. The V_{DS} is measured by P5100 probe of Tektronix with 4.5 kV peak voltage rating and a shunt resistor is used for I_D measurement.

2.3.1 Static Characterization of the 3.3 kV 400 A MOSFETs udner study

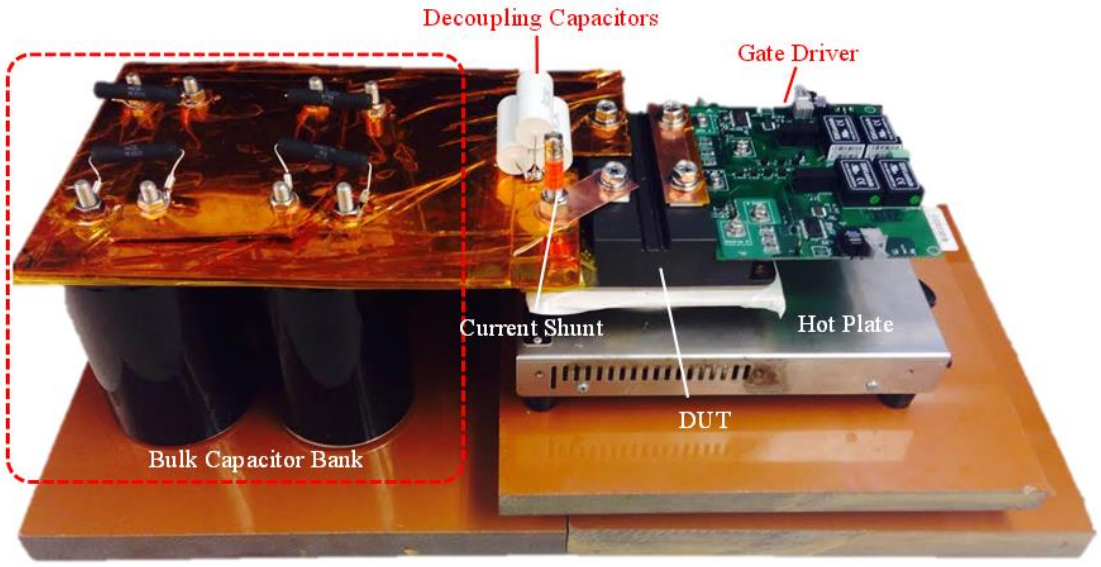
Having the test setup ready for device under test, extensive static and dynamic characterizations are done to capture key data needed for loss calculation of the MOSFETs in any target application. The static characterization is done using B1505 curve tracer of Agilent (now Keysight) Technologies and includes acquisition of output characteristic, threshold voltages, on-state resistances and junction capacitances. All the parameters except junction capacitances are

extracted from room temperature and 150°C, since the junction capacitances are shown to be temperature-invariant [69].

Figures 2.25(a) and 2.25(b) show the output characteristic of the SiC MOSFETs and forward characteristic of the SBD, respectively. For 9 V V_{GS}, the on-state resistance of the MOSFET reduces as temperature increases. However, for higher gate voltages the opposite happens. This is



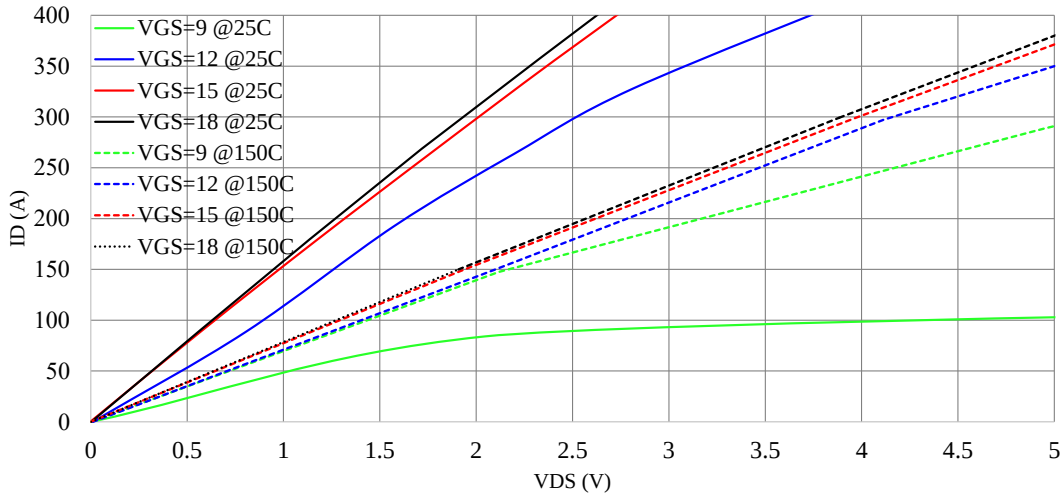
(a)



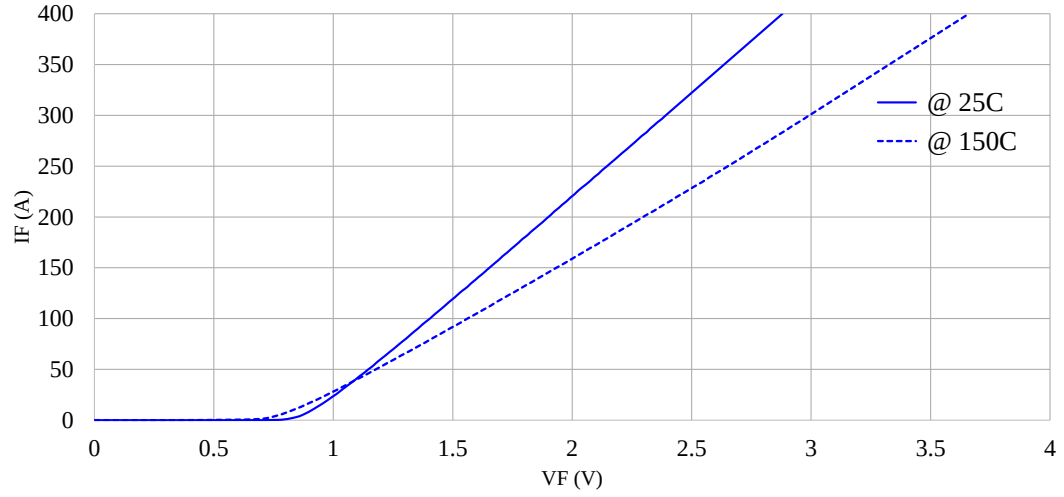
(b)

Figure 2.24 (a) Gate drive mounted on the device and (b) Test bed designed for dynamic characterization.

due to different temperature dependency of three primary resistances within the MOSFET: channel resistance, JFET region resistance and drift layer resistance. At lower gate voltages, the channel resistance is dominant which reduces with increase in temperature [81]. The other two resistances however act in the opposite direction with change in junction temperature and are dominant at higher gate voltages. Also, since the channel resistance is inversely proportional to V_{GS}, the total on-state resistance reduces as driving voltage increases [82].



(a)



(b)

Figure 2.25 (a) Output characteristic of the MOSFETs at different gate voltages and temperature and (b) Forward characteristic of the SBDs Test bed designed for dynamic characterization.

Since larger die size features smaller on-resistance, usually the specific on-resistance is used as the degree of merit when comparing different semiconductors together. Figure 2.26 shows numeric values of both on-resistance and specific on-state resistance of the MOSFETs with recommended V_{GS} of 15 V applied at room temperature and 150°C. As it can be seen, the MOSFETs have almost constant on-resistance versus load current. The increase in on-resistance from 25°C to 150°C is about 75%, which is shown to happen in a linear way for SiC MOSFETs [83]. So interpolation can be used to get the values at any temperature.

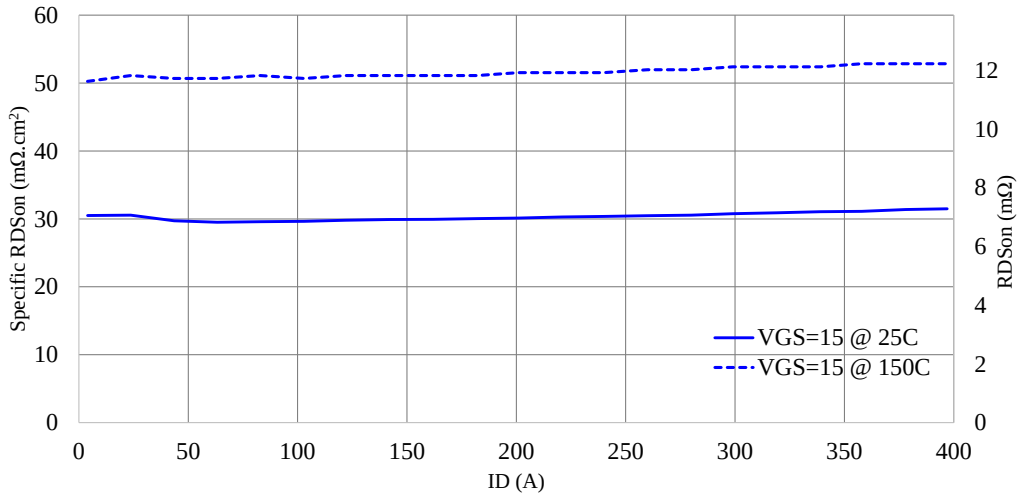


Figure 2.26 Numeric values of on-state resistances at 15 V gate voltage for the MOSFETs.

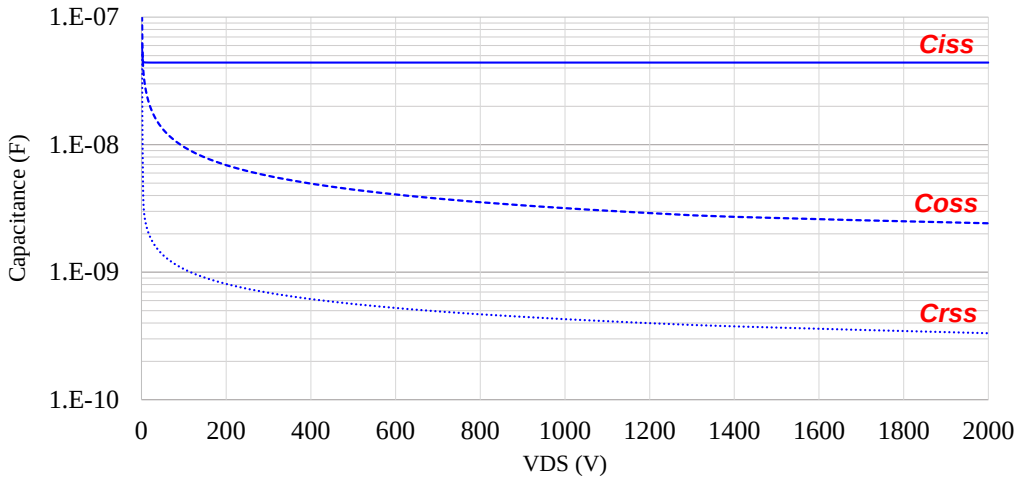


Figure 2.27 Junction capacitances of the module measured at 100 kHz frequency.

The threshold voltage of the MOSFETs under study assuming 10 V V_{DS} and setting the threshold current to 40 mA, is about 2.05 V at 25°C. The threshold voltage linearly reduces to 1.4 V at 150°C due to increase in intrinsic carrier concentration with increased temperature.

Finally, the input ($C_{iss}=C_{GS}+C_{GD}$), output ($C_{oss}=C_{DS}+C_{GD}$) and Miller (C_{GD}) capacitances of the MOSFETs measured at 100 kHz frequency are shown in figure 2.27.

The input capacitance together with input gate resistance are the most important factors contributing to the MOSFET switching losses. The output capacitance at the other hand mainly contributes to the parasitic ringing during turn-off transient, as the current flows through drain-to-source parasitic inductance in series with the output capacitance [83]. Last but not least, the Miller capacitance is the main cause of the Miller effect discussed in previous section. At constant switching speed of a device, the higher Miller capacitance, the more Miller current will be. The Miller capacitance also contributes to the slew rate of the drain-to-source voltage and thereby, impacts switching losses of the MOSFET [69].

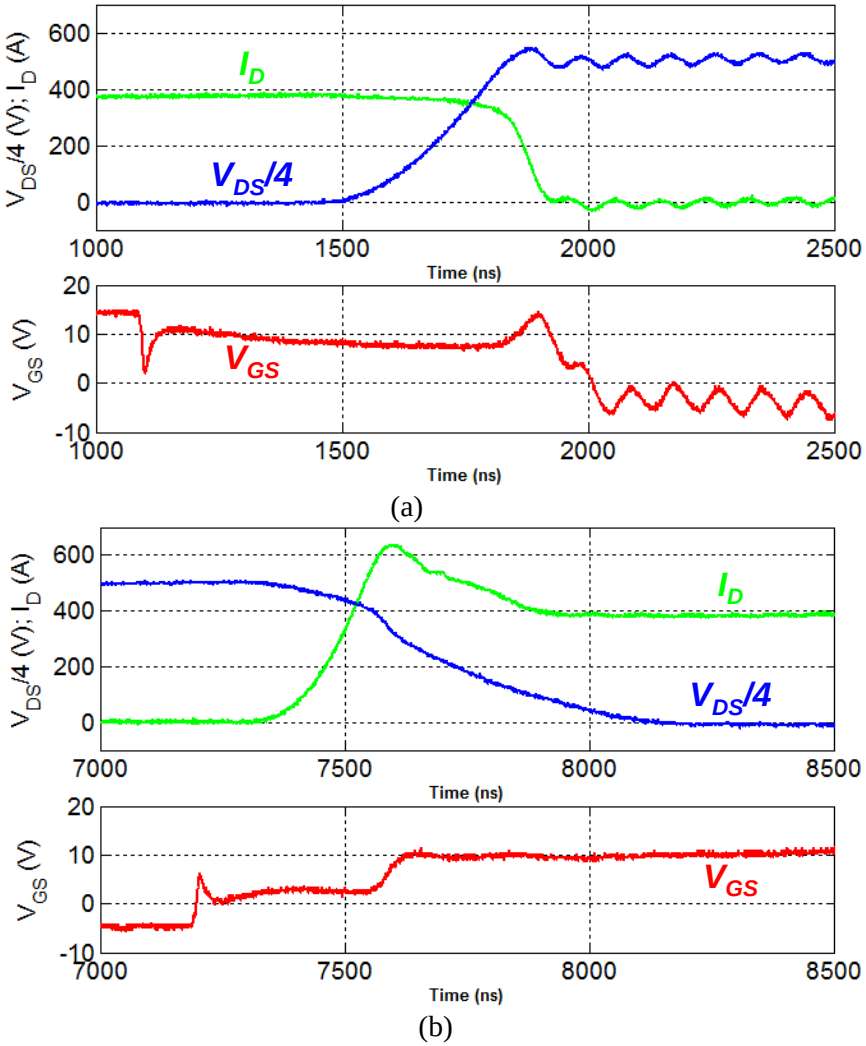
2.3.2 Dynamic Characterization of the 3.3 kV 400 A MOSFETs udner study

For dynamic characterization the double-pulse test is done under different load currents, gate resistances and temperatures. For both static and dynamic characterization, the shown results are average of what is measured from four identical MOSFETs (inside two modules).

The double-pulse test (DPT) experiment is a trusted method for extracting dynamic characteristics of a semiconductor, and is done on the bottom switch of the module under test for calculation of the losses. For the setup shown in figure 2.24(b) the load is composed of two series

connected inductors with total inductance of 150 µH and saturation current larger than 1 kA to withstand peak current overshoot of the MOSFET.

DPT is done at 2 kV dc bus voltage and the drain current is increased from 50 A to 400 A in a stepwise manner with 50 A steps, to capture switching losses versus load current. The external gate resistance is swept down from 5 Ω with steps of 1 Ω. This is continued until 2 Ω gate resistance where the turn-on current overshoot starts increasing significantly (higher than 100% load current), resulting in maximum drain currents close to I_{crm} of the device which is 800 A



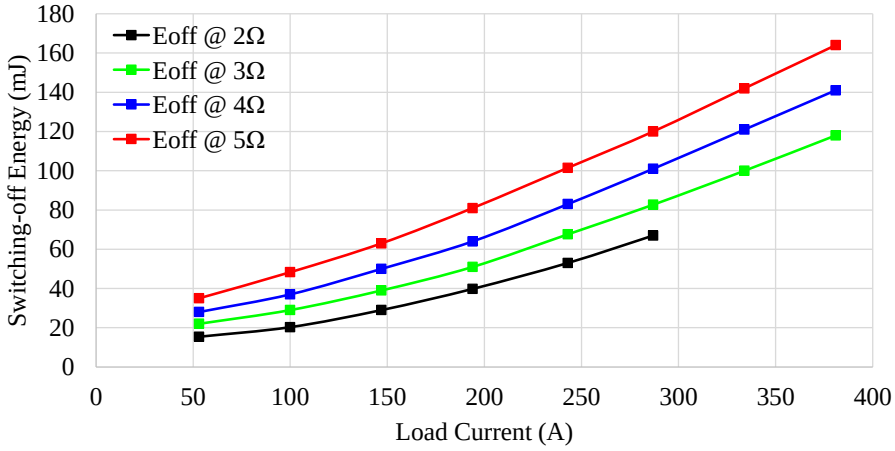
(a)

(b)

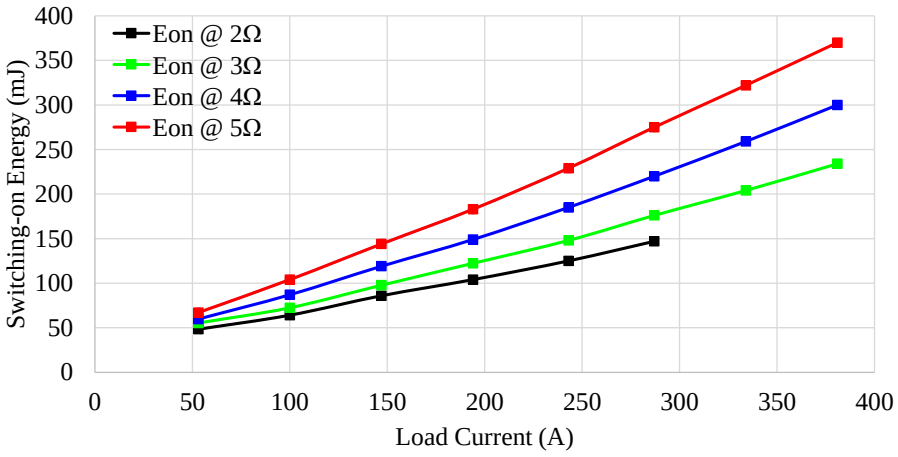
Figure 2.28 (a) turn-off and (b) turn-on switching waveforms captured from DPT at 2 kV 400 A, Rg=3Ω and Tj=25˚C.

according to manufacturer. This is the reason why dynamic tests are not done at gate resistances lower than 2 Ω. Also, at 2 Ω gate resistance load current is limited to 300 A.

The switching waveforms are shown in figures 2.28(a) and 2.28(b). It is worth to note that the measurement point of V_{GS} is on device terminal, between internal and external gate resistances. The voltage drop on external gate resistor is the reason why in the turn-on waveform the gate voltage is around 10 V. The gate voltage becomes 15 V once device input capacitance completely charges and no current flows toward gate of the MOSFET. The *di/dt* and *dv/dt* for the MOSFET



(a)



(b)

Figure 2.29 (a) Switching-off and (b) Switching-on energies of the 3.3 kV 400 A SiC MOSFETs versus load current at room temperature.

are 3.69 A/ns and 10.61 V/ns at turn-off, and 2.88 A/ns and 3.29 V/ns at turn-on, measured at 3 Ω gate resistance and 400 A drain current.

Turn-off and turn-on losses are shown in figures 2.29(a) and 2.29(b) respectively. The turn-on losses are the dominant part of switching losses in SiC MOSFETs and if avoided by soft switching methods, total system efficiency can be significantly improved. The slight difference between nominal load current and measured values in the figures (for instance, 383 A instead of 400 A) is coming from device switching time at turn-on, which is not taken into consideration when setting the gate pulse length in DPT.

The dynamic tests are repeated at 150°C to investigate temperature dependency of losses. The turn-off and turn-on losses corresponding to room temperature and 150°C are shown in figure 2.30 for the case with 5 Ω gate resistance. The high temperature test results demonstrate that the total switching loss change versus temperature for the DUT is about 7%. Low temperature dependency of switching losses in SiC MOSFETs is an outstanding feature of these semiconductors. It is worth to note that variation of switching losses for a typical Si counterpart (3.3 kV 400 A Si IGBT from

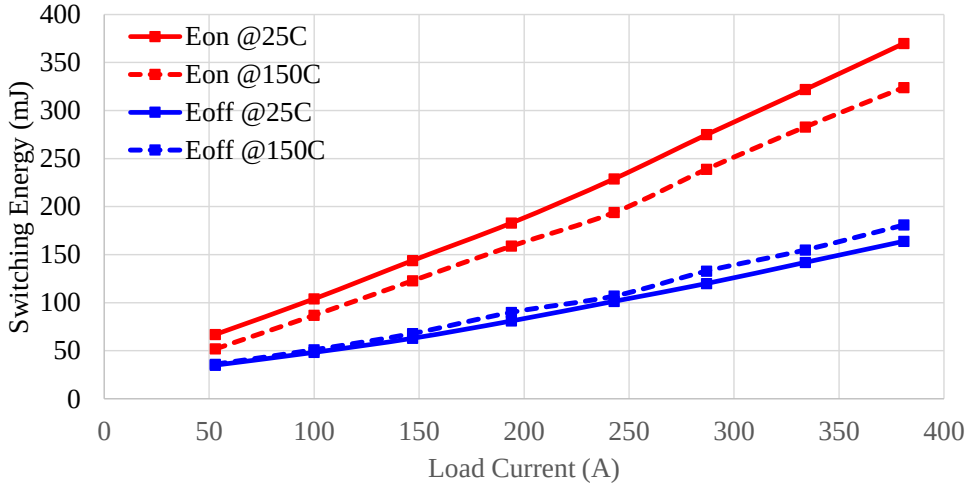


Figure 2.30 Switching-off and switching-on energies of 3.3 kV 400 A SiC MOSFETs at 25˚C and 150˚C temperatures and 5Ω resistance.

Infineon) from 25°C to 125°C is about 35%. Also, as expected from SiC MOSFETs the turn-off loss has slightly increased while the turn-on loss was reduced as temperature increased. This is due to increase in *di/dt* and *dv/dt* rates at turn-on, and their reduction in turn-off which is because of reduction of the plateau and threshold voltages [69].

2.4 Summary

The SiC MOSFETs are not commercialized at voltages higher than 1.7 kV [84], [85]. Thus, gate drivers are not commercially available for them beyond 1.7 kV [86], [87]. In this chapter, gate driver development and test circuit design were shown for SiC MOSFETs at 3.3 kV blocking voltage rating. The required protections and safety considerations were taken into account. Also, the PCB design criteria at medium-voltages was investigated to ensure that corona and arc-over would be prevented. The characterization results shown for the 3.3 kV SiC MOSFETs in this chapter can be used as input to any converter design purpose. The converters designed in next chapters will take advantage of the presented results to investigate impact of the state-of-the-art SiC MOSFETs on medium-voltage high-power motor drive application.

Chapter 3. Converters under Study for Medium-Voltage High-Power Drive Application

As mentioned in chapter 1, a variety of multilevel converters are being commercially used for industrial drive application. It was also discussed that for the medium-voltage range (namely > 4.16 kV motor voltages which is the scope of this study) there are a few converters that can satisfy operation in motor drive application. This chapter introduces the three topologies that are targeted for medium-voltage high-power motor drive application in this study.

3.1 The Cascaded H-bridge Converter

The cascaded H-bridge converter (CHB) is the most popular topology used in medium-voltage high-power motor drive application. The concept of this converter (series-connecting H-bridge cells to achieve higher voltages) was introduced in 1975 via a US Patent [88], and later in 1997 Peter Hammond, *et. al.* proposed it for motor drive application [89]. The main purpose of using this converter topology for motor drive application was to increase power quality of the output waveform by increasing the number of voltage levels.

As of 2017, the CHB converter is being used for motor drives for a wide range of voltages from 2.3 kV up to 13.8 kV. This converter was patented by Siemens, however several companies were producing it under license from Siemens until 2015 when the patent of this converter expired and it became an open-source topology. Some of the manufacturers using the CHB converter in their products include Siemens, Delta Electronics, TMEiC, Yaskawa, Emerson Network Power, LSis, Zhuhai Wanlida and etc.

3.1.1 Circuit Configuration

Figure 3.1 shows the CHB converter in motor drive application. According to this figure, each phase of this converter is composed of *n* cells in series where each cell insists of a 6-pulse diode rectifier and an H-bridge inverter cell (figure 3.2) and has a three-phase input and a single-phase output. In order to provide galvanic isolation for the cells (while their ac side is being fed from the same inputs), a multi-pulse transformer with multiple secondary windings is used. The multi-pulse transformer is being considered as the main disadvantage of this converter, where at higher voltages due to increase in number of secondary windings the transformer cost and complexity

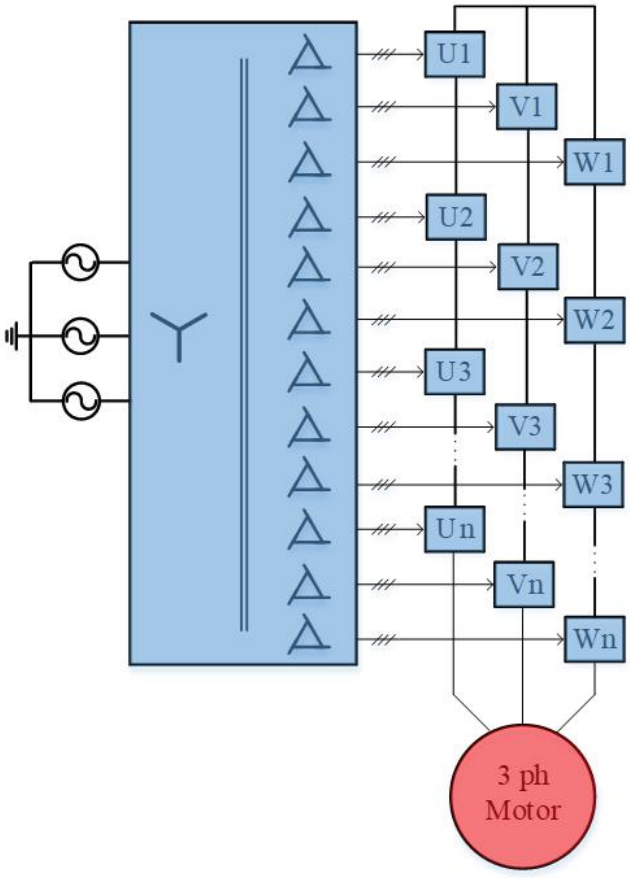


Figure 3.1 The cascaded H-bridge converter in motor drive application.

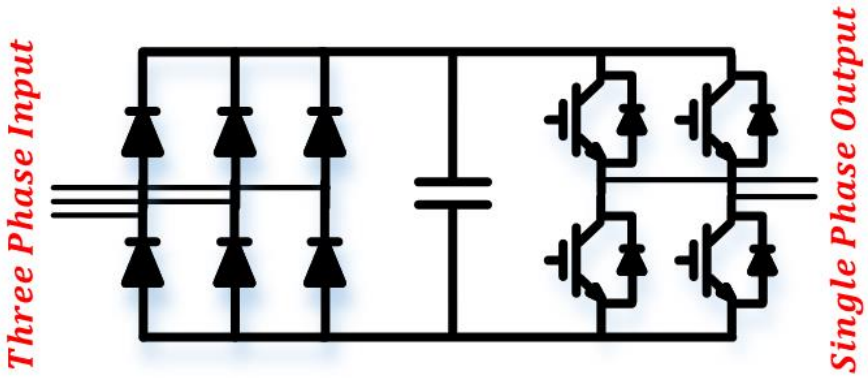


Figure 3.2 Structure of a cell within the CHB converter, where it is composed of a 6-pulse diode rectifier, a capacitive filter and a full-bridge inverter.

increases significantly. According to the drive manufacturers, the transformer cost at high voltages can exceed price of the motor drive system.

Due to high-power nature of the converters under study, the multi-pulse transformer is normally fed from medium-voltage grid. Since the transformer has voltage-reducing functionality, its primary side usually has wye connection. On the other hand, the secondary windings are composed of zigzag windings where by phase shifting them with respect to each other, non-triplen odd-order harmonics can be eliminated from input current. According to [54], order of harmonics that will appear in the primary side of the multi-pulse transformer follows (3.1), where n is the number of 6-pulse diode rectifiers used per phase and k is an integer number.

$$h = 6kn \pm 1 \tag{3.1}$$

Table 3.1 shows the phase angles used for transformer windings, phase shift between windings and the order of first harmonic that appears in input current of the transformer as a function of the number of pulses of the transformer.

Table 3.1 Phase angles, phase differences and the order of first harmonic at the primary side of the multi-pulse transformer as a function of the number of pulses.

Number of Pulses	Typical Phase Angle of Windings	Phase Shift between Windings	Order of First Harmonic at Transformer Primary
12	0˚, 30˚	30˚	11^{th}
18	0˚, ±20˚	20˚	17^{th}
24	±7.5˚, ±22.5˚	15˚	23^{rd}
30	0˚, ±12˚, ±24˚	12˚	29^{th}
36	±5˚, ±15˚, ±25˚	10˚	35^{th}

3.1.2 Modulation and Control

A variety of modulation schemes such as level-shifted PWM (LSPWM) [90], selective harmonic elimination [91], selective harmonic mitigation [92] and phase-shifted PWM (PSPWM) have been used on the CHB converter so far. According to [93], the PSPWM modulation is the most effective

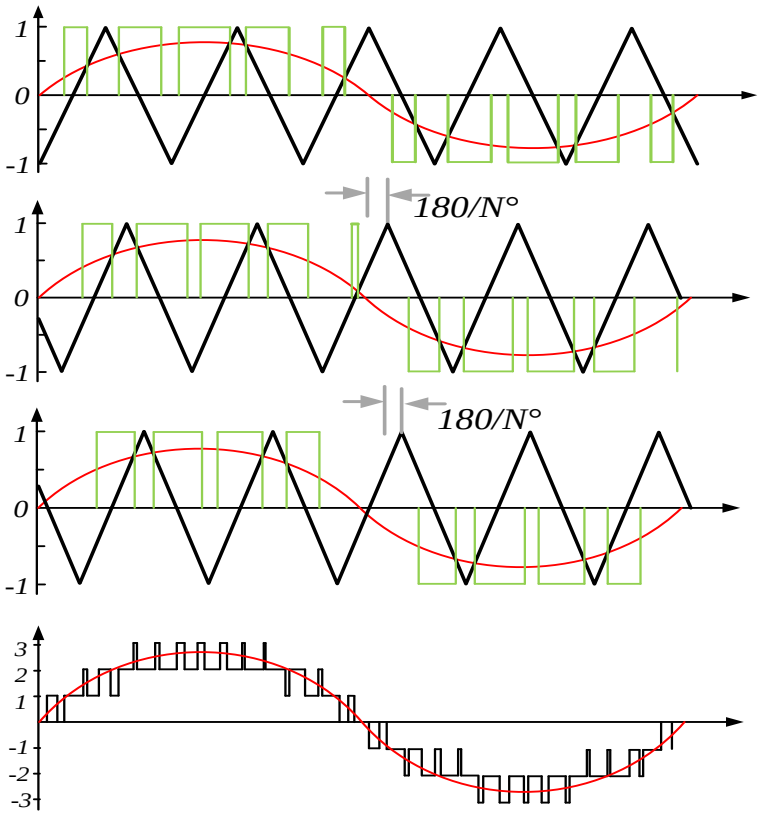


Figure 3.3 The phase-shifted pulse-width modulation (PSPWM) for a CHB converter with *n*=3 cells per phase.

way to use on the CHB converter where equal losses among different cells, equal losses between semiconductors within a cell and an effective output switching frequency of nf_c where n is number of full-bridge cells per phase and f_c is the carrier frequency. Figure 3.3 shows the carrier waveforms of the PSPWM modulation for a CHB converter with three cells per phase.

According to figures 3.1 and 3.2, the dc link voltages in the CHB converter are provided by means of diode rectifiers connected to the multi-pulse transformer's secondary windings. Thus, there is no requirement for controllers on the dc bus voltage. In other words, the only closed-loop controller needed for the CHB converter is the one to control its output voltage.

3.2 The Modular Multilevel Converter

The modular multilevel converter was introduced by Lesnicar and Marquardt in 2003 [94], [95], [96]. This converter does not have any restriction for number of levels in it (e. g. the ac or dc side voltage) and thus, it enables operation at very high voltages. The MMC converter has a patent belonging to Siemens and as of 2017 is commercially used for HVDC plants and AFE applications, as well as motor drive for LNG plants [97].

3.2.1 Circuit Configuration

Figure 3.4 shows the MMC converter in motor drive application. According to this figure, each phase leg of this converter is composed of two arms, where each arm contains an arm inductor and n cells in series. Each cell in the MMC converter can be in half-bridge or full-bridge (H-bridge) configuration. Although using full-bridge cells has shown better short-circuit protection levels in

AFE mode of operation, for inverter applications (such as the motor drive) usually the half-bridge configuration (figure 3.5) is preferred.

The number of diode front-end rectifiers (and the corresponding number of secondary windings of the multi-pulse transformer) in case of this converter are selected to satisfy IEEE 519 [98] for input current of the transformer. As mentioned before, the transformer can have harmonic elimination effect if the secondary windings are properly phase shifted.

Last but not least, there are no dc link capacitors on the common dc link provided by the diode front-end rectifier. Instead, the filter capacitors are placed on the half-bridge cells. This is due to the fact that MMC has shown to be a very sophisticated load for its rectifier. In fact, according to [99] assuming pure sinusoidal output currents to the load, the MMC inverter will derive a pure dc

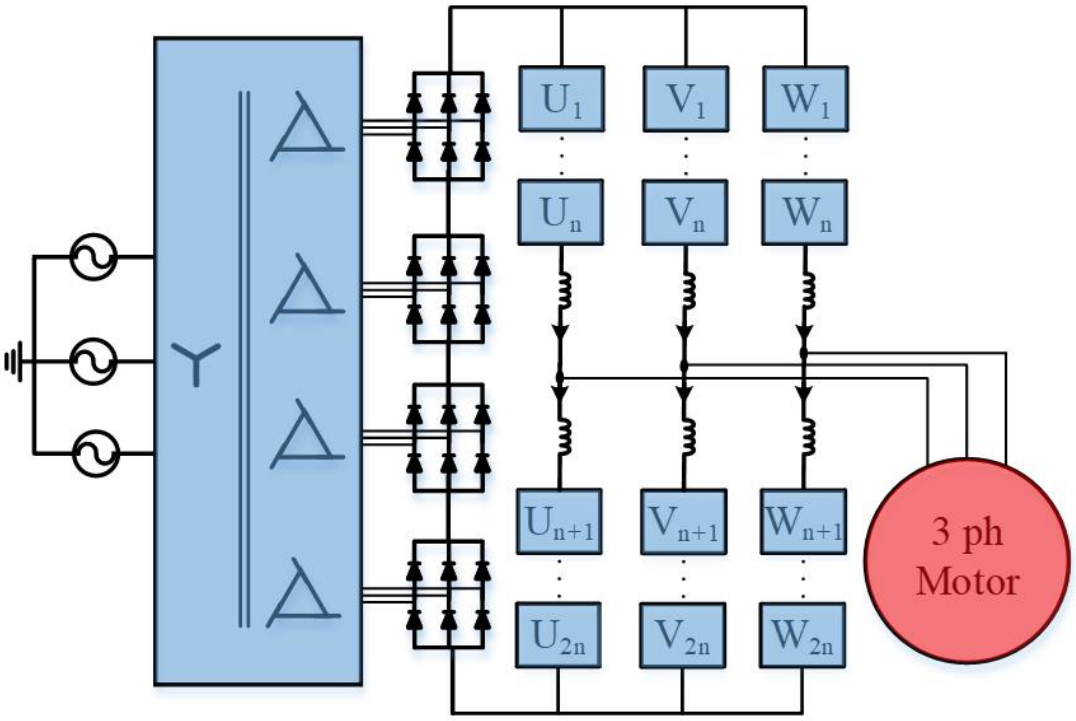


Figure 3.4 The modular multilevel converter in motor drive application. The number of diode frontend rectifiers in this converter are selected merely to satisfy IEEE 519 for input current quality.

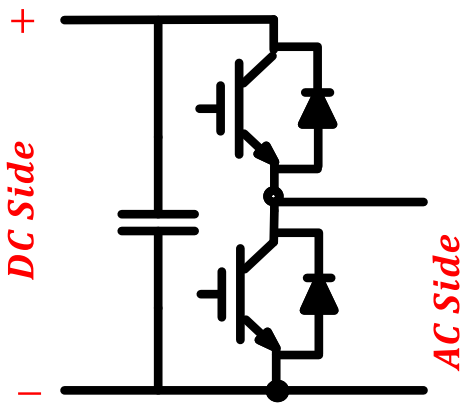


Figure 3.5 Structure of a half-bridge cell within the MMC converter, where it is composed of a half-bridge leg and a capacitive filter.

current from its DFE stage. On the other hand, since the power transfer between ac and dc sides in the MMC converter happens on the cell capacitors, it is necessary to include large capacitors in the cells to restrict ripple. In the inverter mode of operation, the dc current charges the cell capacitors while the output current (which is equally distributed between the top and bottom arms) discharges them and delivers power to the output.

3.2.2 Modulation and Control

For the MMC converter, other than modulation scheme it is necessary to use voltage balancing method between the cells in a phase leg. A variety of modulation/control schemes have been used on the MMC converter so far. In this study, the modulation and control method proposed in [99] are used, where phase shifted carrier waveforms are used and the MMC converter's effective output frequency is equal to $2nf_c$, where n is number of cells per arm and f_c is the carrier frequency.

A phase leg of the MMC converter forms an LC circuit, where the value of C is dependent of the converter's modulation index and L is equal to twice the inductance of an arm inductor (figures

3.6 (a) and (b)). On the other hand, due to fundamental frequency switching in cells as well as fundamental frequency components of arm currents in the MMC converter the circulating current will contain non-triplen even order harmonics (2^{nd}, 4^{th}, …) [100]. It is of great importance to size the passive components of the MMC (inductors and capacitors) to avoid resonance in the circulating current. Proper dimensioning of the passive components in the MMC has been the topic of several studies [101], [102].

3.2.3 Steady-State Analysis of Voltages and Currents in MMC Converter

As mentioned before, the main disadvantage of the MMC converter is its requirement for significant amount of passive components installed in its structure. In order to develop a better

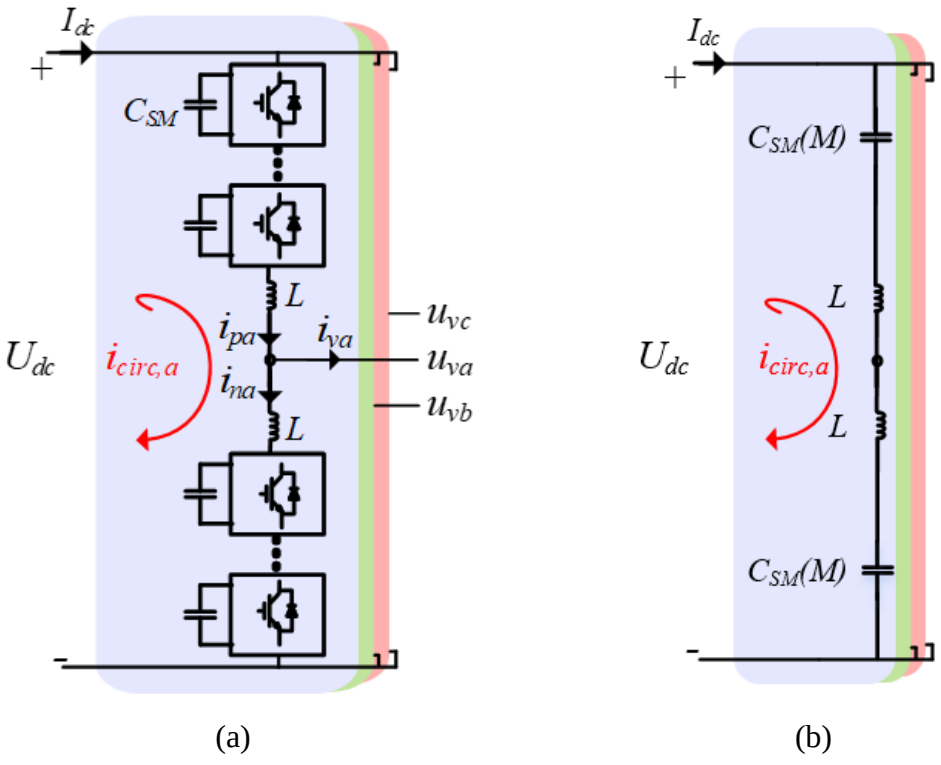


Figure 3.6 (a) Simplified diagram of the MMC converter in inverter mode operation and (b) The equivalent circuit of the MMC in a phase leg.

understanding of the converter and choose proper values for the passive components within the converter, in this section a steady-state analysis is done on the MMC converter based on the well-known average model.

In order to simplify the modeling and the corresponding calculations, two main assumptions are made in this study. First it is assumed that the switching frequency is infinite, and using the averaging model, the submodules in arms are being inserted in a sinusoidal manner with balanced voltages across their capacitors. Second, it is assumed that the modulation reference is pure sinusoidal without harmonic components injected and the voltage balancing is acquired via redundancy in inserting the submodules, without adding additional controller.

In figure 3.6, L is the arm inductance, i_{vj} ($j=a, b$ *or* c) is the output current of the converter in phase j, I_{dc} is the dc bus current and i_{pj} and i_{nj} are the upper and lower arm currents in phase j, respectively. For the arm currents in phase A we have (Note that all equations are being considered for phase A. Other phases can be derived in a similar way):

$$i_{pa} = i_{circ,a} + \frac{1}{2} I_{va} \sin(\omega t + \phi) \tag{3.2}$$

$$i_{na} = i_{circ,a} - \frac{1}{2} I_{va} \sin(\omega t + \phi) \tag{3.3}$$

where I_{va} is the peak magnitude of output current and $i_{circ,a}$ is the circulating current in phase A and can be writen as (3.4):

$$i_{circ,a} = \frac{i_{na} + i_{pa}}{2} \tag{3.4}$$

The circulating current is composed of a dc component (which is one third of the current coming from the dc side) plus even order harmonics. Considering 2nd and 4th harmonics only in the circulating current, it can be written as (3.5):

$$i_{circ,a} = \frac{I_{dc}}{3} + I_2 \sin(2\omega t + \theta) + I_4 \sin(4\omega t + \varphi) \tag{3.5}$$

where I_2 and I_4 are the magnitudes of 2nd and 4th current harmonics, and θ and φ are their phase angles, respectively. It is worth noting that even order harmonics of higher than 4th are usually neglected in circulating current since their magnitude is too small in comarison.

The average duty cycle for upper and lower arm submodules can be written as (3.6) and (3.7), respectively, where m_a is the modulation index. With regard to (3.6) and (3.7), the ac voltage at the submodule ac terminal can be formulated as (3.8) and (3.9). Also the voltage synthesized by the upper and lower arms in phase A can be expressed as (3.10) and (3.11).

$$D_{pa,SM} = \frac{1}{2} - \frac{1}{2} m_a \sin(\omega t) \tag{3.6}$$

$$D_{na,SM} = \frac{1}{2} + \frac{1}{2} m_a \sin(\omega t) \tag{3.7}$$

$$u_{ca,p} = U_{ca,p}(\frac{1}{2} - \frac{1}{2} m_a \sin(\omega t)) \tag{3.8}$$

$$u_{ca,n} = U_{ca,n}(\frac{1}{2} + \frac{1}{2} m_a \sin(\omega t)) \tag{3.9}$$

$$u_{a,p} = n.U_{ca,p}(\frac{1}{2} - \frac{1}{2} m_a \sin(\omega t)) \tag{3.10}$$

$$u_{a,n} = n.U_{ca,n}(\frac{1}{2} + \frac{1}{2} m_a \sin(\omega t)) \tag{3.11}$$

where $U_{ca,p}$ and $U_{ca,n}$ are voltages across submodule capacitors in upper and lower arm submodules and n is the number of submodules per arm. For the submodule configuration shown in figure 3.6, the capacitor current as a function of the arm current at upper and lower arm submodules is as (3.12) and (3.13). The average model of MMC configuration of figure 3.6 is shown in figure 3.7.

According to (3.12) and (3.13) and by replacing the arm currents from (3.2) and (3.3), the capacitor current for upper and lower arm submodules can be calculated as (3.14) and (3.15), respectively. As it can be seen, the capacitor current is a function containing a dc component plus ac components from fundamental frequency up to five times the fundamental frequency. The dc

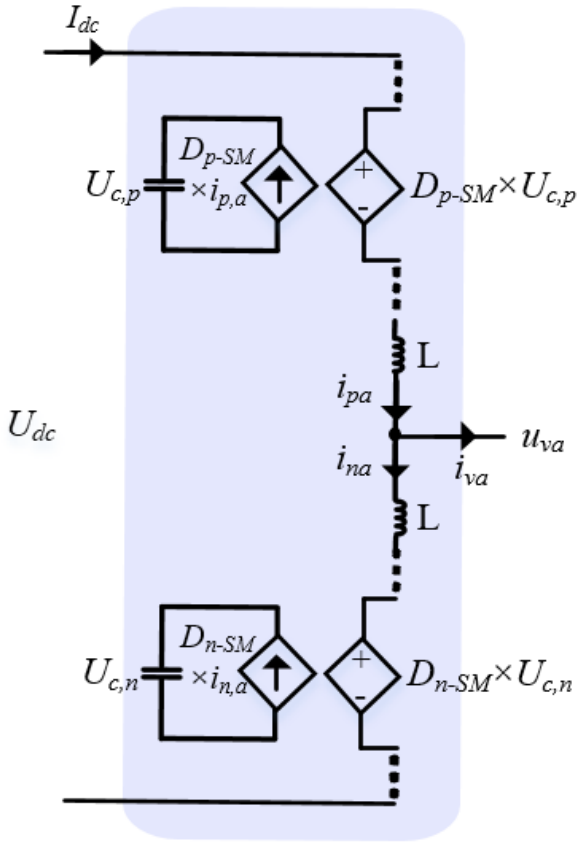


Figure 3.7 Average model representation of the MMC in inverter mode operation.

component of the capacitor current must be zero for stability purposes. So, equation (3.16) can be written for the dc current in MMC converter.

$$i_{ca,p} = i_{pa} \times (\frac{1}{2} - \frac{1}{2} m_a \sin(\omega t)) \tag{3.12}$$

$$i_{ca,n} = i_{na} \times (\frac{1}{2} + \frac{1}{2} m_a \sin(\omega t)) \tag{3.13}$$

$$i_{ca,p} = \frac{I_{dc}}{6} - \frac{m_a I_{va}}{8}\cos\phi - \frac{m_a I_{dc}}{6}\sin(\omega t) + \frac{I_{va}}{4}\sin(\omega t + \phi) - \frac{m_a I_2}{4}\cos(\omega t + \theta) +$$

$$\frac{I_2}{2}\sin(2\omega t + \theta) + \frac{m_a I_{va}}{8}\cos(2\omega t + \phi) + \frac{m_a I_2}{4}\cos(3\omega t + \theta) - \frac{m_a I_4}{4}\cos(3\omega t + \varphi)$$

$$+ \frac{I_4}{2}\sin(4\omega t + \varphi) + \frac{m_a I_4}{4}\cos(5\omega t + \varphi) \tag{3.14}$$

$$i_{ca,n} = \frac{I_{dc}}{6} - \frac{m_a I_{va}}{8}\cos\phi + \frac{m_a I_{dc}}{6}\sin(\omega t) - \frac{I_{va}}{4}\sin(\omega t + \phi) + \frac{m_a I_2}{4}\cos(\omega t + \theta) +$$

$$\frac{I_2}{2}\sin(2\omega t + \theta) + \frac{m_a I_{va}}{8}\cos(2\omega t + \phi) - \frac{m_a I_2}{4}\cos(3\omega t + \theta) + \frac{m_a I_4}{4}\cos(3\omega t + \varphi)$$

$$+ \frac{I_4}{2}\sin(4\omega t + \varphi) - \frac{m_a I_4}{4}\cos(5\omega t + \varphi) \tag{3.15}$$

$$I_{dc} = \frac{3}{4} m_a I_{va}\cos(\phi) \tag{3.16}$$

where *cos(ϕ)* is the MMC load power factor.

Each capacitor's voltage can be derived as a function of its current as in (3.17). So, by integrating capacitor current at different frequencies, the corresponding ripple component of the capacitor voltage can be calculated according to (3.18).

$$U_{c,i} = \frac{1}{C}\int i_{c,i}\,dt \tag{3.17}$$

$$\Delta u_{c,i}^{k\omega} = \frac{1}{C}\int i_{c,i}^{k\omega}\,dt \tag{3.18}$$

where k is an integer from 1 to 5, *C* is the cell capacitance value and Δu at a specific frequency is the capacitor voltage ripple at that frequency. With regard to what mentioned, the capacitor voltage ripple at fundamental frequency in upper and lower arm cells is calculated as in (3.19) and (3.20):

$$\Delta u_{ca,p}^{\omega} = \frac{m_a I_{dc}}{6\omega C}\cos(\omega t) - \frac{I_{va}}{4\omega C}\cos(\omega t+\phi) - \frac{m_a I_2}{4\omega C}\sin(\omega t+\theta) \tag{3.19}$$

$$\Delta u_{ca,n}^{\omega} = -\frac{m_a I_{dc}}{6\omega C}\cos(\omega t) + \frac{I_{va}}{4\omega C}\cos(\omega t+\phi) + \frac{m_a I_2}{4\omega C}\sin(\omega t+\theta) \tag{3.20}$$

By integrating higher order currents passing through the submodule capacitor, the ripple components can be calculated at different frequencies. The expressions for submodule voltage ripple at twice, 3 times, 4 times and 5 times fundamental frequency is brought for upper and lower arm submodule capacitors in (3.21) through (3.28).

$$\Delta u_{ca,p}^{2\omega} = \frac{m_a I_{va}}{16\omega C}\sin(2\omega t+\phi) - \frac{I_2}{4\omega C}\cos(2\omega t+\theta) \tag{3.21}$$

$$\Delta u_{ca,n}^{2\omega} = \frac{m_a I_{va}}{16\omega C}\sin(2\omega t+\phi) - \frac{I_2}{4\omega C}\cos(2\omega t+\theta) \tag{3.22}$$

$$\Delta u_{ca,p}^{3\omega} = \frac{m_a I_2}{12\omega C}\sin(3\omega t + \theta) - \frac{m_a I_4}{12\omega C}\sin(3\omega t + \varphi) \tag{3.23}$$

$$\Delta u_{ca,n}^{3\omega} = -\frac{m_a I_2}{12\omega C}\sin(3\omega t + \theta) + \frac{m_a I_4}{12\omega C}\sin(3\omega t + \varphi) \tag{3.24}$$

$$\Delta u_{ca,p}^{4\omega} = -\frac{I_4}{8\omega C}\cos(4\omega t + \varphi) \tag{3.25}$$

$$\Delta u_{ca,n}^{4\omega} = -\frac{I_4}{8\omega C}\cos(4\omega t + \varphi) \tag{3.26}$$

$$\Delta u_{ca,p}^{5\omega} = \frac{m_a I_4}{20\omega C}\sin(5\omega t + \varphi) \tag{3.27}$$

$$\Delta u_{ca,n}^{5\omega} = -\frac{m_a I_4}{20\omega C}\sin(5\omega t + \varphi) \tag{3.28}$$

According to calculated expressions for the ripple components at different frequencies for upper and lower arm submodule capacitors, the voltage across each capacitor can be written as summation of a dc component plus the calculated ac components. For upper arm submodule capacitors, we have:

$$U_{ca,p} = \frac{U_{dc}}{N} + \Delta u_{c,p}^{\omega} + \Delta u_{c,p}^{2\omega} + \Delta u_{c,p}^{3\omega} + \Delta u_{c,p}^{4\omega} + \Delta u_{c,p}^{5\omega} \tag{3.29}$$

$$U_{ca,n} = \frac{U_{dc}}{N} + \Delta u_{c,n}^{\omega} + \Delta u_{c,n}^{2\omega} + \Delta u_{c,n}^{3\omega} + \Delta u_{c,n}^{4\omega} + \Delta u_{c,n}^{5\omega} \tag{3.30}$$

where U_{dc} is the dc bus voltage of MMC. From the voltages at dc terminal of submodules, the synthesized voltage across the ac side of the submodule can be calculated using the average duty

cycle as (3.8) and (3.9). The total voltage inserted across a phase leg of the MMC converter then will be equal to summation of the individual voltages inserted by the submodules. With respect to the fact that there are a total of *n* submodules per arm, the total voltage across a phase leg can be formulated as (3.31).

$$u_{ph,a} = N.u_{ca,p} + N.u_{ca,n} \tag{3.31}$$

As demonstrated in figure 3.8, the voltage across a phase leg of MMC will be a dc quantity whose magnitude is equal to the dc voltage at the dc side of the MMC, plus harmonics at different frequencies. For each of the harmonic components across the phase leg of the converter, the following equation can be written as (3.32). Later, the circulating current components at different frequencies can be calculated as in (3.33) and (3.34).

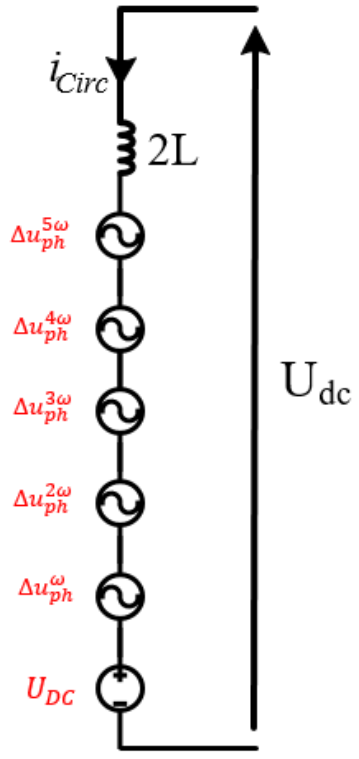


Figure 3.8 Equivalent circuit representation of MMC converter's phase leg.

$$\Delta u_{ph,a}^{k\omega} = N.u_{ca,p}^{k\omega} + N.u_{ca,n}^{k\omega} \tag{3.32}$$

$$i_2 = I_2 \sin(2\omega t + \theta) = -\frac{1}{2L}\int \Delta u_{ph,a}^{2\omega} dt \tag{3.33}$$

$$i_4 = I_4 \sin(4\omega t + \varphi) = -\frac{1}{2L}\int \Delta u_{ph,a}^{4\omega} dt \tag{3.34}$$

Solving the equations (3.33) and (3.34), the magnitude and phase angle of the 2nd and 4th harmonic components in circulating current can be calculated. The magnitude and phase angle of 2nd harmonic component will be as (3.35)-(3.42).

$$I_2 = \frac{\sqrt{(A\cos\phi + B)^2 + (A\sin\phi)^2}}{|D|} \tag{3.35}$$

$$\begin{cases} \theta = \arcsin \dfrac{[A\cos\phi + B]}{\sqrt{(A\cos\phi + B)^2 + (A\sin\phi)^2}} & D > 0 \\ \theta = \arcsin \dfrac{-[A\cos\phi + B]}{\sqrt{(A\cos\phi + B)^2 + (A\sin\phi)^2}} & D < 0 \end{cases} \tag{3.36}$$

$$I_4 = \frac{5m_a^2 N}{|E|} I_2 \tag{3.37}$$

$$\begin{cases} \varphi = -\theta & E > 0 \\ \varphi = \theta & E < 0 \end{cases} \tag{3.38}$$

$$A = \frac{3m_a N I_{va}}{64\omega^2 LC} \tag{3.39}$$

$$B = -\frac{m_a^2 N I_{dc}}{48\omega^2 LC} \tag{3.40}$$

$$D = 1 - \frac{N}{16\omega^2 LC} - \frac{m_a^2 N}{24\omega^2 LC} \tag{3.41}$$

$$E = 960\omega^2 LC - 8m_a^2 N - 15N \tag{3.42}$$

From equations (3.35) and (3.37), the resonance frequencies for 2nd and 4th harmonics at constant value of *L* and *C* will be as (3.43) and (3.44). On the other hand, for a converter operating at constant frequency and having specific capacitance per cell, the arm inductances for which resonance happens in 2nd and 4th harmonics can be formulated as (3.45) and (3.46).

$$\omega_{2nd} = \sqrt{\frac{3N + 2m_a^2 N}{48LC}} \tag{3.43}$$

$$\omega_{4th} = \sqrt{\frac{8m_a^2 N + 15N}{960LC}} \tag{3.44}$$

$$L_{2nd} = \frac{3N + 2m_a^2 N}{48\omega^2 C} \tag{3.45}$$

$$L_{4th} = \frac{8m_a^2 N + 15N}{960\omega^2 C} \tag{3.46}$$

Validation of the derived equations is investigated via a case study in [103]. The derived equations for resonance harmonics will help selecting proper values for passive components within

Table 3.2 Parameters of the MMC converter used for simulation purposes.

Parameter	Symbol	Value
dc link voltage	U_{DC}	4500 V
Load active power	P	0.5 MW
Load power factor	PF	0.9
Number of cells per arm	N	5
Cell voltage	V	900 V
Arm inductance	L	5 mH
Cell capacitance	C	1.6 mF
Output voltage	u	2.3 kV
Output frequency	f	60 Hz
Switching frequency	f_{sw}	1200 Hz

the MMC converter to prevent the resonance phenomenon. For an MMC converter with data shown in table 3.2, the simulated and analytically calculated resonance effect are shown in figure 3.9.

Figure 3.9 shows the RMS circulating current versus arm inductance at given output frequency and cell capacitor values, and the resonance points can be clearly seen from the figure. Note that the calculated resonance points for 2nd and 4th harmonics of the circulating current would be

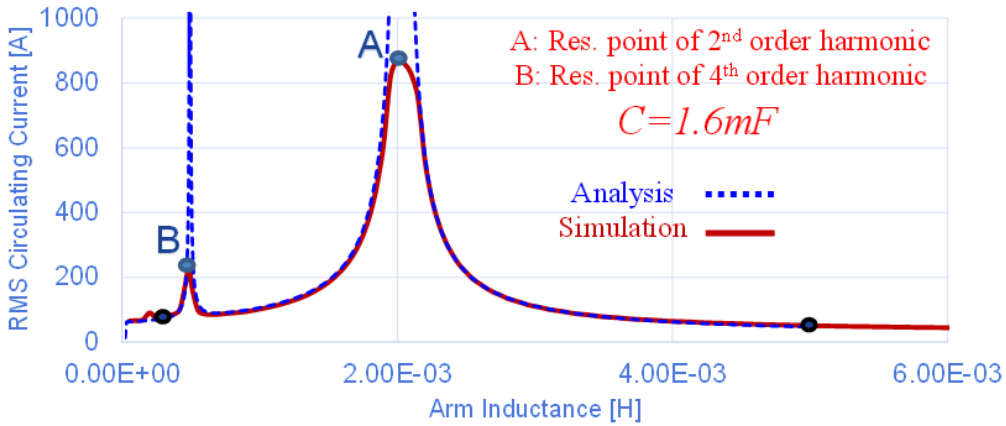


Figure 3.9 RMS circulating current versus arm inductance value for the MMC with parameters given in Table 3.2. The simulated and calculated resonance points show a very close match.

2.10 mH and 0.471 mH, respectively. Last but not least, figures 3.10 and 3.11 provide proof of validation for the equations derived for arm currents and cell (submodule) voltages.

3.2.4 Reduction of Installed Capacitors in Converter Structure

So far accurate equations are derived for voltages and currents in the MMC converter. In this section, a method is proposed to take advantage of the derived equations and minimize the capacitor voltage ripple across cells of the MMC converter. Also, further investigations are done

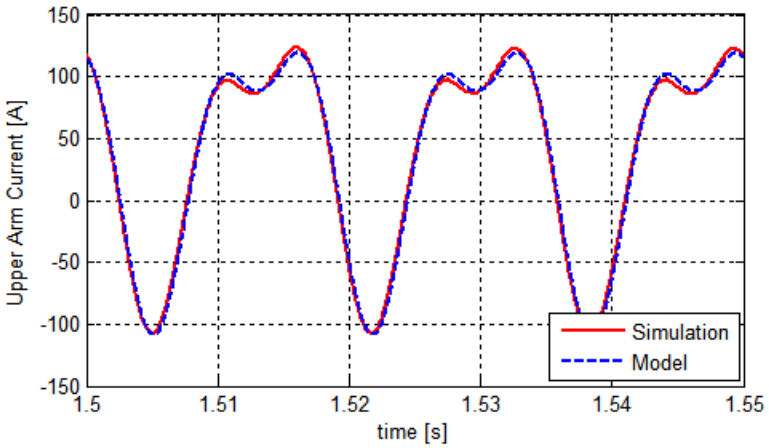


Figure 3.10 Simulated and analytically calculated arm currents for the MMC with parameters of table 3.2.

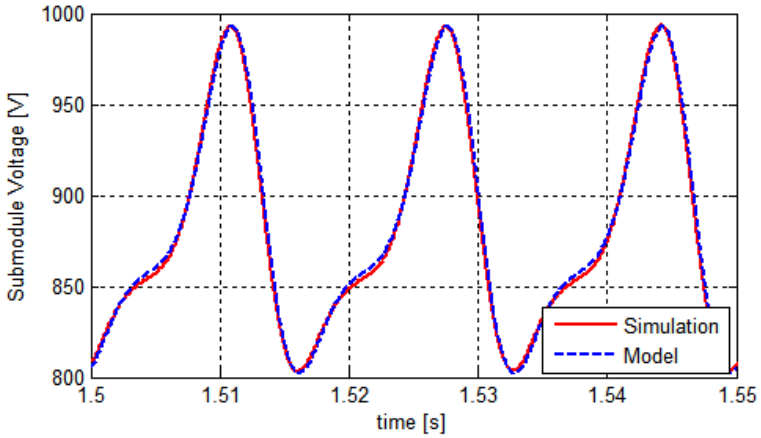


Figure 3.11 Simulated and analytically calculated cell (submodule) voltages for the MMC of table 3.2.

in order to specify the optimum operating point of the MMC in terms of power factor, modulation index and etc.

Equations (3.29) and (3.30) represent the voltages across cell capacitors in the upper and lower arms of the MMC converter, respectively. Due to symmetry of voltages, each of the mentioned equations can be used as the objective function to run a optimization, where the variable parameters are the magnitudes and phase angles of the 2^{nd} and 4^{th} harmonics of the circulating current. Once the optimum circulating current was calculated, any injection method (such as the one introduced in [104]) can be used to inject it within the phase legs of the converter.

The well-known particle swarm optimization (PSO) is used for determination of the best operating point of the MMC [105]. The optimization is performed on the MMC inverter used in previous section, and figure 3.12 is showing the voltages across an arbitrary cells under 4 different conditions: having the natural circulating current, having a dc circulating current (by eliminating the circulating current's ac components), by injecting the optimum 2^{nd} order harmonic and finally by injecting a combination of optimum 2^{nd} and 4^{th} harmonics.

According to figure 3.12, the original ripple across cells of the MMC is 186.6 V peak to peak. Once the circulating current is eliminated, the ripple reduces to 124 V since the components resulting from the circulating current's ac components are eliminated. By injecting an optimum value of 2^{nd} harmonic with the optimum phase angle, the ripple is reduced to 81.8 V (52% reduction compared to the original case) and finally injecting 2^{nd} and 4^{th} harmonics simultaneously results in 78.6 V ripple, which is about 4% more reduction compared to the case where only 2^{nd} harmonic was injected. This is another proof that the main harmonics of the circulating current to consider are the lower harmonics.

In another study, the optimum modulation index for the MMC was investigated. The optimization results showed that the best modulation index to operate the MMC at is about 1.15. Figure 3.13 shows the peak to peak ripple for the same MMC converter for a wide range of modulation index and load phase angle, while at any given point the optimum value of 2nd harmonic is injected. According to this plot, for the cases where active power is higher than the reactive power (for power factors > 0.707), the optimum modulation index is around 1.15. On the other hand, for MMC converters dealing with smaller power factor than 0.707 (such as STATCOM case), the minimum capacitor voltage ripple is achieved at modulation indices around 2. Note that theoretically, any modulation index higher than 1.15 must be realized using full-bridge cells in the converter structure. But in practice due to existence of safety factors for the value of dc link voltage, usually modulation indices higher than unity are realized by means of full-bridge converters.

In order to provide evidence for the above-mentioned claim, a case study is done where for the MMC under investigation in the previous section, the modulation index is increased to 1.15. Figure 3.14 shows the voltage ripple across capacitors of the MMC under the original modulation

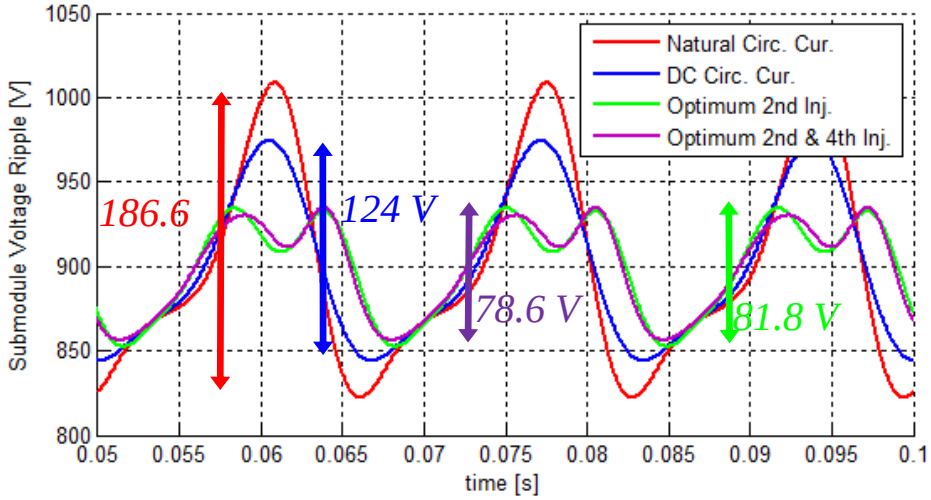


Figure 3.12 Voltage ripple across an arbitrary cell's (submodule's) capacitor under different circulating currents.

index (0.834) and the new modulation index (1.15). As it can be seen, regardless of the circulating current condition (dc or optimum circulating current injected), 1.15 modulation index results in smaller ripple across capacitors compared to 0.834. Also, injecting the optimum 2nd harmonic at 1.15 modulation index results in 85% reduction in capacitor voltage ripple.

3.2.5 Minimization of Passive Elements in MMC AFE Converter

The AFE mode operation of MMC converter has been well addressed in literature [106]. In [107], control and analysis of an MMC AFE using half-bridge cells was shown and the MMC was tested in grid-tied AFE mode. Also, stability analysis was addressed for the converter. Design of a hybrid power source for high-power loads was shown in [108] based on modular multilevel

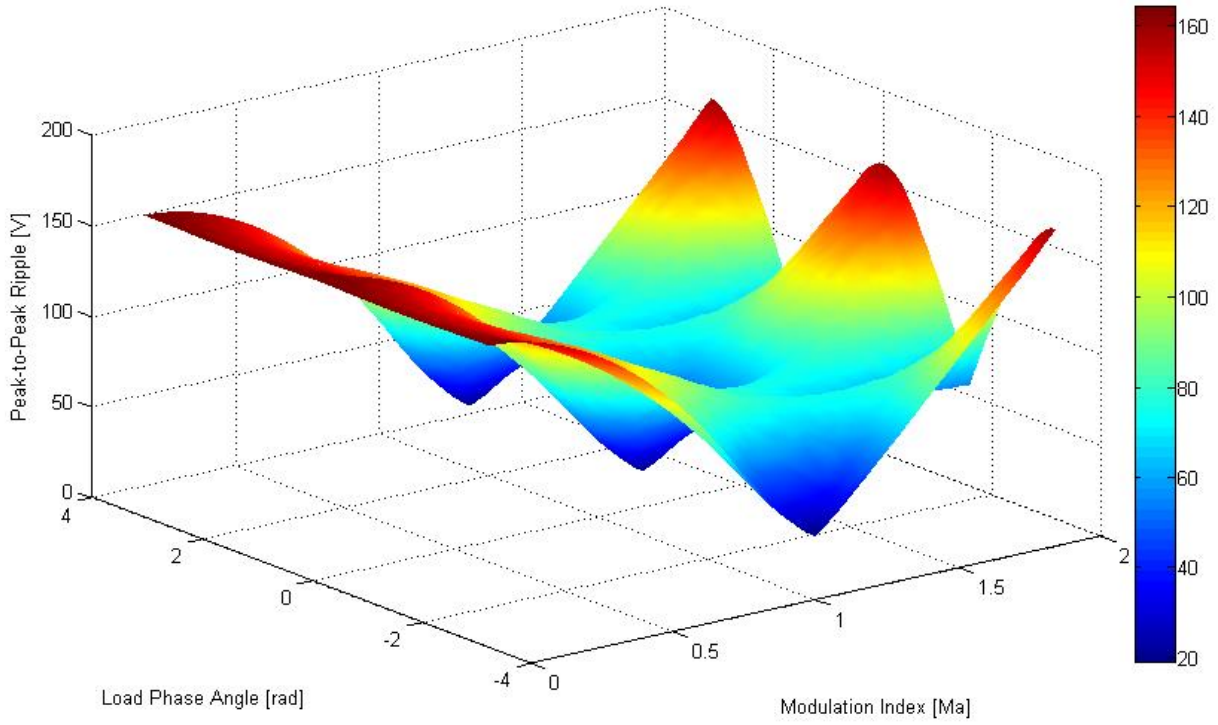


Figure 3.13 Voltage ripple versus modulation index and load phase angle while at any given operating point the optimum 2nd harmonic is injected.

converter in AFE mode operation. Realization of HVDC plants based on modular multilevel converter has been discussed in several other literature.

Despite its unique advantages, the main problem with the modular multilevel converter is bulk size of the passive components used in its structure. As mentioned before, according to data from Siemens more than 2/3 of size of the cells used in the converter is occupied by their capacitors. Also, in MMC AFE the arm inductors take a considerable volume of space. This is mainly because the inductors are usually made on air core to prevent saturation in case of short circuit in the rectifier system. The large-in-size air-core inductors occupy significant amount of space in structure of the MMC converter.

In this section special effort has been made on minimizing the size of passive elements within structure of the modular multilevel converter in AFE rectifier mode of operation. By taking advantage of a hidden optimum design point in the converter structure, size of the arm inductors and submodule capacitors are reduced while no additional complexity is introduced to the system. The proposed method does not need any additional controllers and it is capable of achieving similar

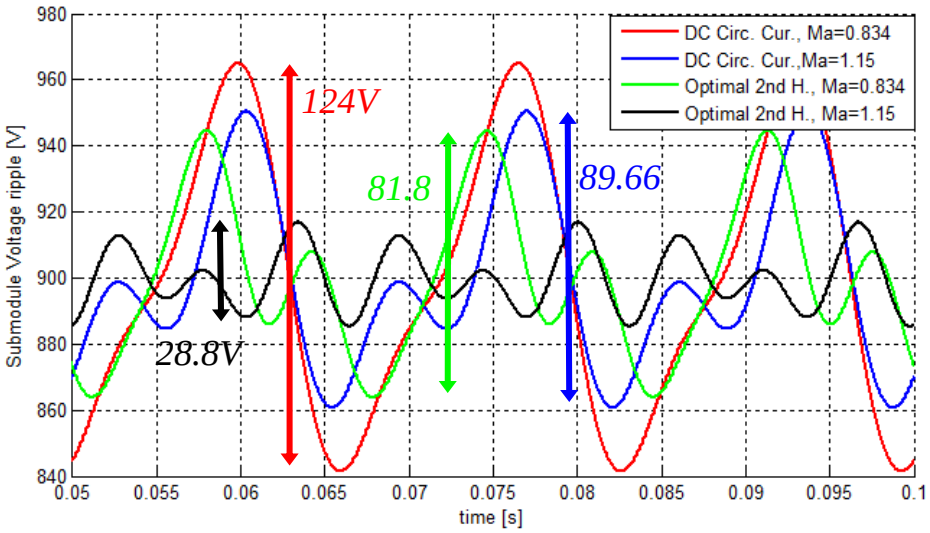


Figure 3.14 Voltage ripple across capacitors under 0.834 and 1.15 modulation indices.

reduction is size of submodule capacitors as done in low-frequency circulating current injection methods. Moreover, using the proposed design guidelines results in reduction of arm inductors in MMC AFE converter by about 90%, and reduction of total installed inductors in converter structure by about 65%. The achieved reduction of passive elements (i.e., arm inductors and cell capacitors) will result in reduction in initial investment needed and will increase popularity of the MMC converter in AFE application.

Figure 3.15 shows the general circuit configuration of grid-connected MMC AFE. In a similar way to the MMC in inverter mode operation, there are a total of six arms in a three phase MMC converter, where each arm is formed by series connection of N identical submodules together with an arm inductor L. The submodules used within the converter can be half-bridge or full-bridge cells. Also, in some cases filter inductors are added between the MMC AFE and the grid to improve power quality and increase short-circuit protection level of the converter.

An important step toward designing MMC converter is to size the arm inductors and the cell capacitors within its structure. Cell capacitor value is usually selected to restrict the voltage ripple across it to a specific amount. The maximum peak-to-peak ripple value across cell capacitors is selected to be 20% peak-to-peak in this study. It is worth to note that the ripple must be restricted so that during turn-off transients, the worse-case voltage (which happens at peak of the voltage across cell and is equal to the dc voltage + peak ripple + turn-off overshoot) must stay within safe operating area for the power semiconductors.

On the other hand, the arm inductors of MMC AFE are sized to satisfy the following requirements:

1- To avoid resonance in circulating current harmonics,

Table 3.3 Parameters of the MMC AFE under study.

Parameter	Symbol	Value
dc link voltage	U_{dc}	4000 V
dc current	I_{dc}	125 A
Converter power factor	PF	1
Number of cells per arm	N	4
Cell voltage	V	1000 V
Load Power	L	500 kW
Cell capacitance	C	1.2 mF
Output voltage	u_{ac}	2.3 kV
Output frequency	f	60 Hz
Switching frequency	f_{sw}	1200 Hz

2- To properly restrict the fault current in case of fault on dc bus of rectifier

In order to satisfy the first term above, the arm inductance must be selected far enough from resonance inductance at operating frequency and the selected cell capacitance. According to the

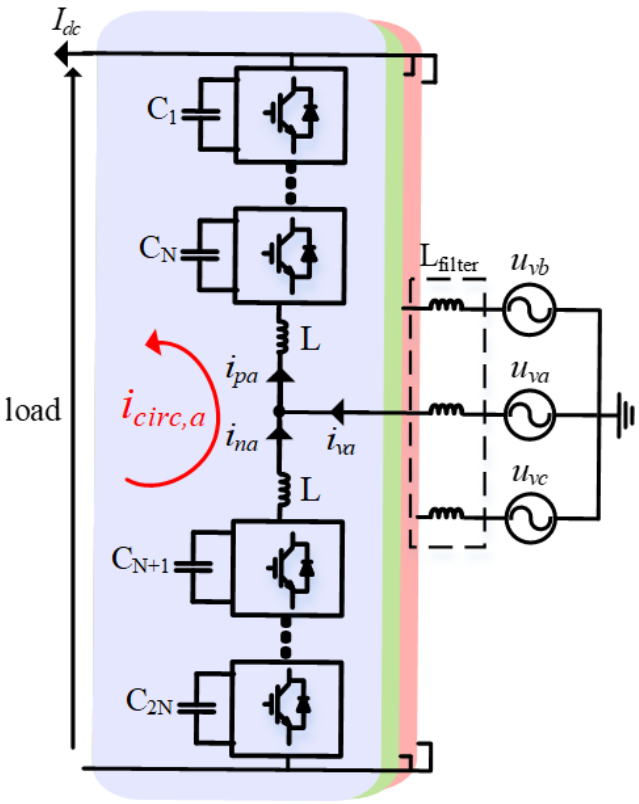


Figure 3.15 The modular multilevel converter in grid-connected rectifier mode operation.

Table 3.4 Specifications of MMC AFE converters designed in literature/industry.

Reference	U_{dc} [kV]	u_{ac} [kV]	P [MVA]	C [mF]	L [mH]	$L/L_{res,2nd}$
[109]	*60*	30	50	2.5	3	2
[110]	*400*	200	450	5	2.5	3.3
[111]	*60*	30	50	3.3	3	3.89
[112]	*20*	10	1	0.82	38.3	8.5
[113]	*8*	4.16	18	10	1.7	4.61
[114]	*400*	125	3.25	3.3	4.67	4.24
[115]	*320*	166	500	10	60	3.33

steady-state analysis performed in the previous section, at constant frequency and cell capacitor value, the resonance inductances for 2nd and 4th harmonics in the circulating current are given as (3.45) and (3.46), respectively.

For the proposed converter in this study whose parameters are given in table 3.3, the simulated RMS circulating current versus arm inductance at constant submodule capacitance (1.2 mF) is shown in figure 3.16. From figure 3.16, the resonance point in 2nd and 4th order harmonics are clear and are marked by A and B, respectively. Also, it can be seen from figure 3.16 that for inductances smaller than resonance inductance of 4th order harmonic (point B) and at inductances a few times

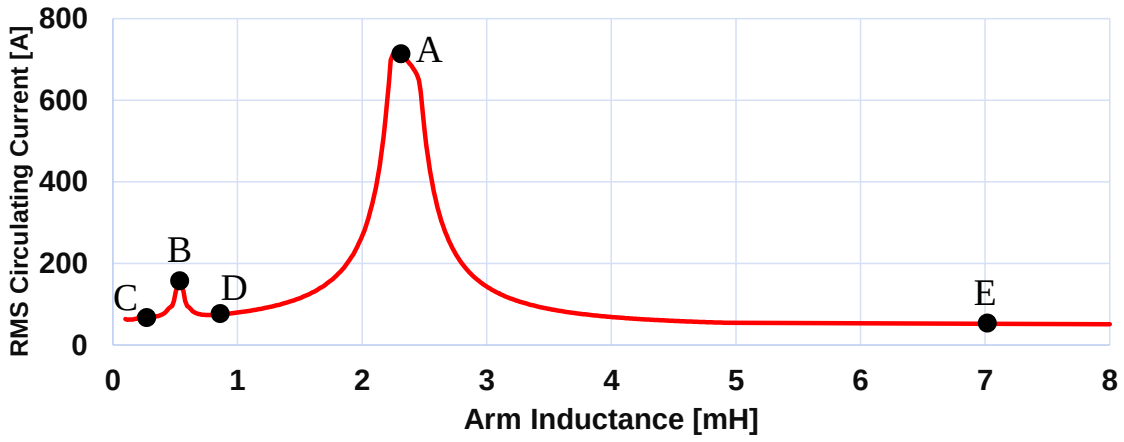


Figure 3.16 RMS circulating current versus arm inductor value for an MMC with parameters shown in Table 3.3.

larger than the resonance inductance in 2nd harmonic (point A), the circulating current is restricted. In other words, choosing the arm inductance to be higher than resonance inductance of 2nd order harmonic or selecting it at lower than resonance inductance of 4th order harmonic will prevent high value in the circulating current. According to a survey whose results are demonstrated in table 3.4, for designed/implemented MMC AFE converters in literature/industry, the arm inductor is selected to be at least 3 times of the resonance inductance of 2nd harmonic. This is done in order to ensure prevention of resonance effect while proper short circuit level is featured.

Summation of two KVLs in upper and lower arms of MMC AFE of figure 3.14 results in the following equation:

$$u_{vj} = e_j + \frac{L}{2}\frac{di_{vj}}{dt} + L_{filter}\frac{di_{vj}}{dt} \tag{3.47}$$

where e_j is known as the internal EMF of MMC and can be written as:

$$e_j = \frac{u_{nj} - u_{pj}}{2} \tag{3.48}$$

where u_{nj} and u_{pj} are the ac voltages synthesized across upper and lower arms in phase j, respectively. Figure 3.17 represents the equivalent circuit of (3.47), where the Thevenin inductance of MMC AFE can be considered as $L_{filter}+L/2$. So, 1 *pu* of installed filter inductance will have the same effect on attenuating input current harmonics as 4 *pu* of installed arm inductance. Also, in case of a fault in the converter structure, the amount of fault current flowing from grid side will be similar having equal Thevenin inductances.

With respect to what mentioned, the first step in reducing the size of passive elements is to move the majority of the inductance from arm to phase. Two designs are done to investigate the feasibility of the proposed method. In the first (traditional) design, the arm inductance is selected to be 7 mH (point E in figure 3.16), which has a similar ratio to the converter's 2nd harmonic resonance inductance as majority of the converters shown in table 3.4. On the other hand, the second design (design with optimized inductances) is using 400 µH of arm inductance (point C in figure. 4.16). In order to make the Thevenin inductances of the two designs similar, in the second design total of three filter inductances with 3.3 mH size are added between the converter and grid.

In order to have a comparison between the designed converters, a set of simulations are done in MATLAB/Simulink environment. Figure 3.18 is showing the grid voltage as well as the input current to the MMC AFE. According to this figure, the input current to the converter has the same THD with both arm inductors used. This is predictable since the Thevenin inductors in both designs are the same. On the other hand, the cell capacitor voltages for both of the designs are shown in figure 3.19, where it can be seen that with similar cell capacitors, the design with optimum inductors features smaller ripple across cells.

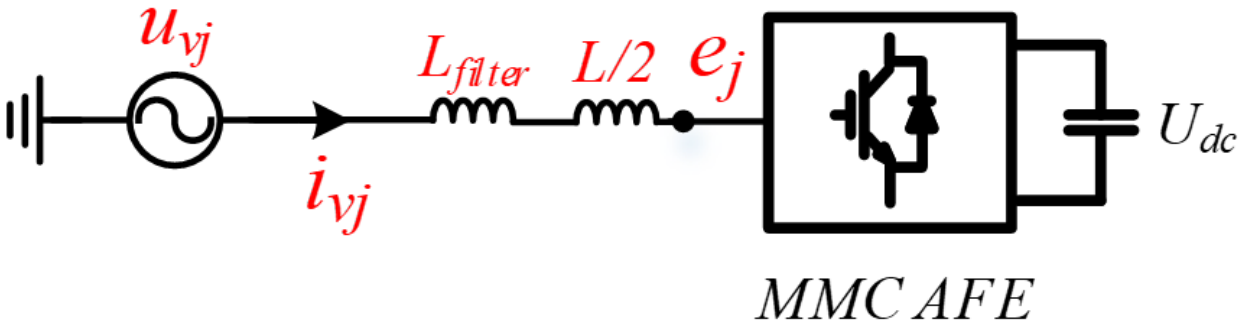


Figure 3.17 Equivalent circuit derived for MMC AFE from (3.47).

According to the calculations performed in previous sections where breakdown of voltage ripple across MMC cells is shown, the main harmonics contributing to voltage ripple are the first and second harmonics. For the design case with 7 mH arm inductors (traditional design), the equations for the first and second harmonic of voltage across cell capacitor are shown in (3.49) and (3.50), respectively:

$$\Delta v_c^{\omega} = [\frac{m_a I_{dc}}{6\omega C} - \frac{I_{va}}{4\omega C} - \frac{m_a I_2}{4\omega C}]\cos\omega t \tag{3.49}$$

$$\Delta v_c^{2\omega} = [\frac{m_a I_{va}}{16\omega C} + \frac{I_2}{4\omega C}]\sin 2\omega t \tag{3.50}$$

On the other hand, for the design case with optimized inductors (with 400 µH arm inductors) the first and second harmonics across cell capacitor are shown in (3.51) and (3.52):

$$\Delta v_c^{\omega} = [\frac{m_a I_{dc}}{6\omega C} - \frac{I_{va}}{4\omega C} + \frac{m_a I_2}{4\omega C}]\cos\omega t \tag{3.51}$$

$$\Delta v_c^{2\omega} = [\frac{m_a I_{va}}{16\omega C} - \frac{I_2}{4\omega C}]\sin 2\omega t \tag{3.52}$$

As it can be seen from equations (3.49)-(3.52), voltage ripple across cell capacitor is coming from different sources. The terms that depend on load current I_{dc} and ac input current I_{va} are common between two designs. However, the components that depend on magnitude of the 2nd harmonic current I_2 appear with different sign in case of the shown designs. According to (3.49) and (3.50), in case of the traditional design the ripple component coming from the circulating current is adding to the main component which depends on the input ac current. On the other hand,

(3.51) and (3.52) show that in case of the design with optimized inductor size the ripple components resulting from the second harmonic of the circulating current are acting against the component coming from the input current.

The difference between the ripple components resulting from the second harmonic in equations (3.49)-(3.52) is attributed to 180˚ difference in phase angle of the second harmonic of circulating current between them. According to [103], for any given arm inductor larger than

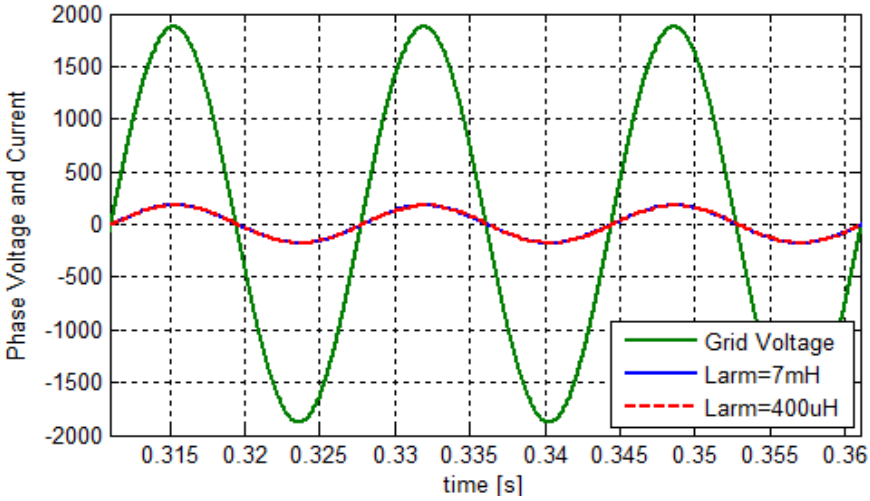


Figure 3.18 Grid voltage and input current to MMC AFE in traditional and proposed designs.

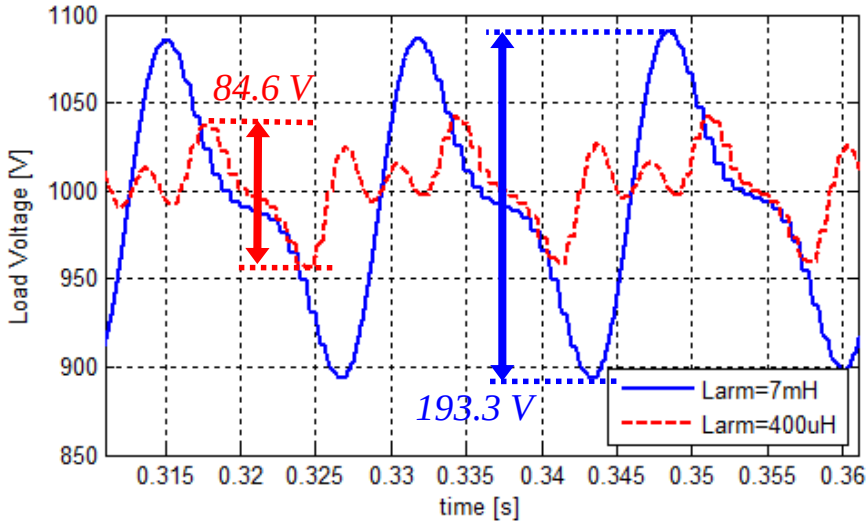


Figure 3.19 Voltage across cell capacitors within two designs performed.

resonance inductor of 2nd harmonic (point A in figure 3.16), the phase angle of the 2nd harmonic circulating current θ is equal to $\pi/2$. However, for arm inductors smaller than the 2nd harmonic's resonance inductance this value is equal to $-\pi/2$, which is the ideal phase angle for 2nd harmonic of the circulating current. In other words, in unity power factor operation of MMC converter (which is typically used in AFE applications) for any arm inductor smaller than resonance inductance of 2nd harmonic, the naturally-existing circulating current is acting toward minimizing the ripple across cell capacitors.

As demonstrated in (3.51) and (3.52), when using an arm inductor smaller than resonance inductance of 2nd order harmonic, the 2nd order current has a positive effect on cell voltage ripple, helping to reduce the size of installed capacitors. This implies that increasing the 2nd order current magnitude will help further reducing the amount of cell capacitance. In other words, while the phase angle of the 2nd harmonic is naturally aligned with its optimum value, increasing its magnitude to the optimum value will result in the same amount of cell voltage ripple reduction that the low-frequency circulating current injection methods can achieve. It is worth noting that in this way the reduction in capacitor size reduction is achieved without using any additional control loops, data storage and etc.

Using the proposed method the optimum design point for the MMC AFE will be somewhere between resonance point of 2nd and 4th harmonics (point D in figure 3.16). In previous section a set of simulations are used to find this optimum design point. However, this article proposes a flowchart to derive the optimum design point. Figure 3.20 shows the proposed step-by-step guideline for selecting the optimum operating point of MMC AFE. Having the converter data and

initial values selected for C and L, the magnitudes and phase angles for 2nd and 4th harmonics of the circulating current can be calculated from (4.35)-(4.42).

The flowchart shown in figure 3.20 will result in the smallest ripple magnitude for a selected cell capacitor C. Once the optimization was done for given capacitor value, the capacitor size can be modified to achieve the desired ripple. For instance, if the optimum value of ripple after optimization was still higher than the target, the value of cell capacitor must be increased and the optimization should be done again. On the other hand, if the achieved ripple was lower than the margins defined for safe operation of the converter, the value of capacitor can be reduced.

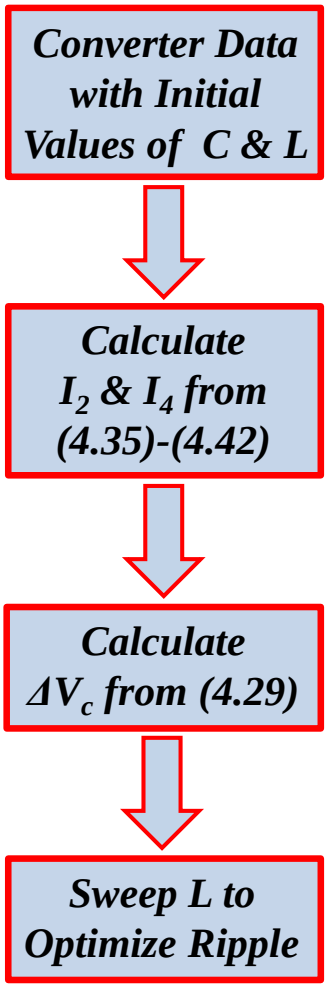


Figure 3.20 step-by-step algorithm proposed for finding the optimum design point in MMC AFE.

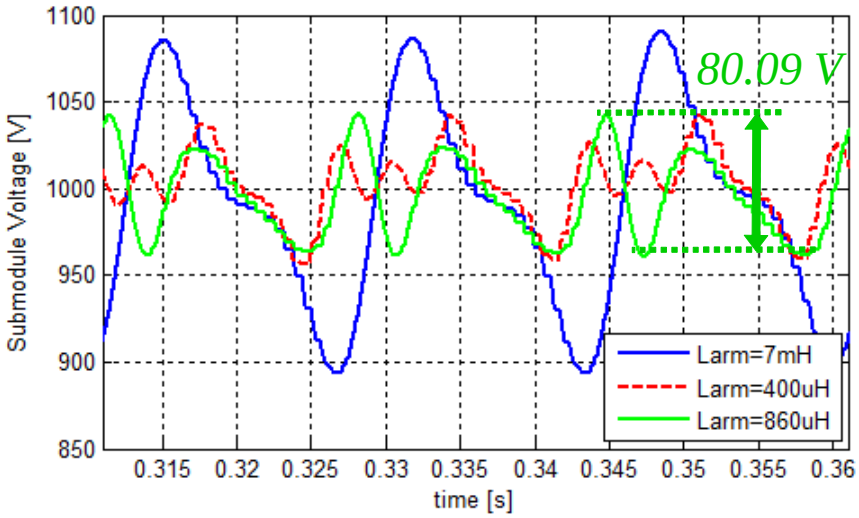


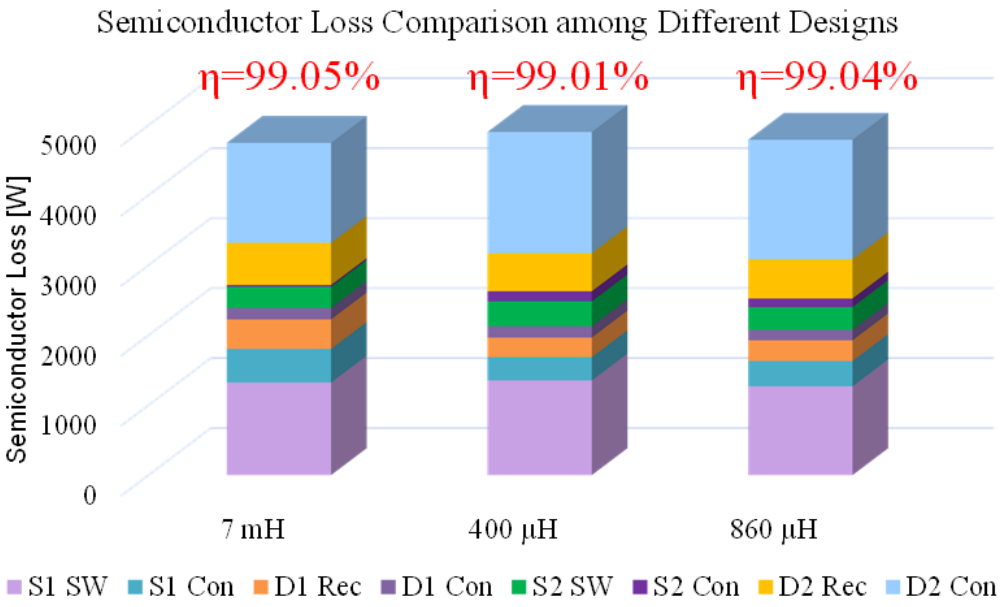
Figure 3.21 Voltage across cell (submodule) capacitors under three different designs proposed so far.

Using the explained optimization guidelines, a third design is proposed for the MMC AFE under study in this article for simultaneous optimization of inductors and cell capacitor voltage ripple. In this way, the arm inductor value is set to 860 µH and the corresponding filter inductor is designed to be 3.07 mH. Figure 3.21 shows comparison of the voltage ripple across capacitors between the three designs performed so far, where it can be seen that the ripple across capacitor voltages is reduced from the original 193 V to around 80 V. Note that this is the same amount of reduction that could be achieved by injecting 2nd order circulating current.

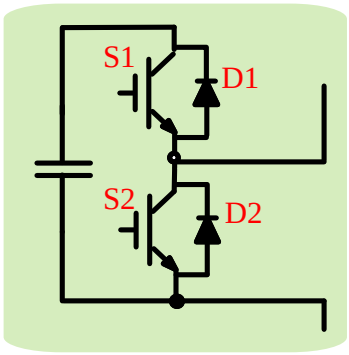
In order to investigate the amount of reduction using the proposed method, a few comparisons are performed. The loss breakdown and efficiencies of all design cases are shown in figure 3.22. According to this figure, there is no significant drop in efficiency of the MMC AFE when using

Table 3.5 Comparison of inductor losses and total copper weight among three designed performed.

Arm Inductance [mH]	Inductor Losses [pu]	Copper Weight [pu]
7	*1*	1
0.4	0.69	0.29
0.86	0.67	0.34



(a)



(b)

Figure 3.22 (a) comparison of losses among three different designs performed and (b) definition of S1, S2, D1 and D2 in the chart above.

the proposed design guideline. Note that the designed converters are using 1.7 kV 150 A Si IGBT of Infineon with part number FF150R17KE4, and the loss calculation method proposed in [116] is used to derive the conduction and switching losses of the semiconductors. Also, it is worth to note that the simulated MMC AFE is using half-bridge cells.

The size and copper loss of inductors installed in the MMC AFE is another important aspect to compare between the designed converters. In case of traditional design the converter needs 6 inductors of size 7 mH. However, for the final proposed design with 860 µH arm inductors and 3 filter inductors with around 3 mH inductance, it is expected to see a significant reduction in total size, weight and loss of the inductors installed in the converter system. Assuming that air-core inductors are designed for arm and filter inductors, table 3.5 shows the losses and copper weight for the inductors installed in the MMC AFE for each of the shown designs (arm inductors and filter inductors). According to the table, the proposed design is capable of achieving the same amount of reduction in cell voltage ripple as achieved by using circulating current injection methods, while the total amount of copper used in the converter is reduced by 65% and copper losses in the inductors are reduced by around 35%.

3.3 The 5-L Active Neutral Point Clamped Converter

The last converter topology considered for medium-voltage high-power motor drive application is the five-level active neutral point clamped (5-L ANPC) converter. This topology was patented by ABB engineers in mid-2000s for expanding penetration range of the well-known neutral point clamped topologies to higher voltages by increasing their number of voltage levels [117]. It is worth to note that the three-level neutral point clamped topology that this converter is based on was introduced by Akagi, *et. al*. in 1980s [118].

3.3.1 Circuit Configuration

Figure 3.23 shows the 5-L ANPC converter in medium-voltage high-power motor drive application. In a similar manner to the MMC topology, this converter needs a simpler diode front-

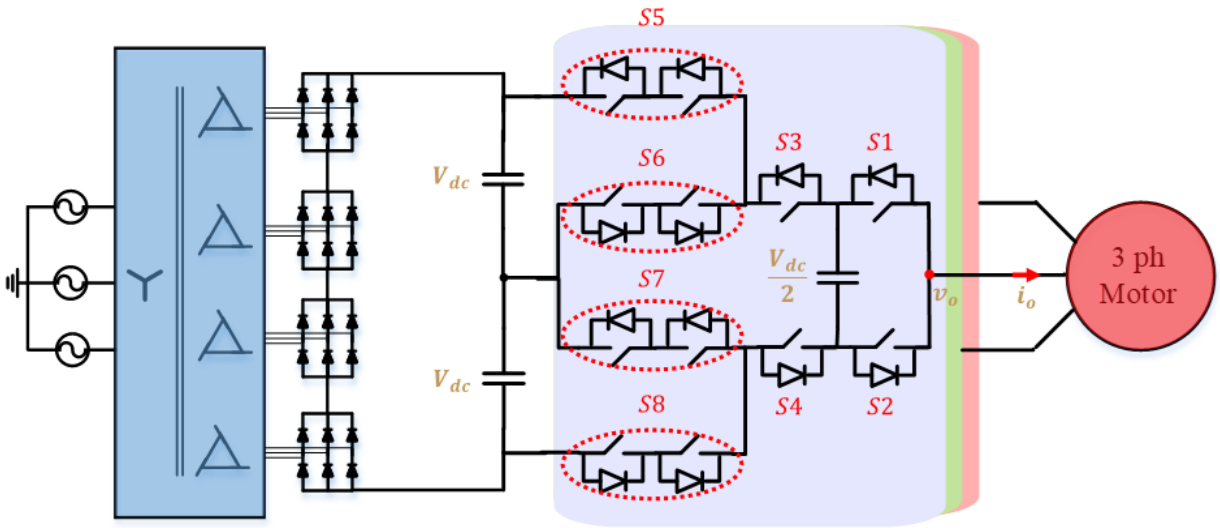


Figure 3.23 The new 5-L ANPC converter proposed by ABB in motor drive application.

end stage where the number of 6-pulse rectifiers are merely selected to satisfy IEEE 519 at the transformer primary side. The 5-L ANPC converter is realized by connecting a two-level cell composed of two switches (S1 and S2) and the floating capacitor to output of a 3-L ANPC converter. Also the inner switches of the converter (S5-S8) are composed of two series-connected power semiconductors in order to satisfy the blocking voltage.

The switches used in structure of this topology are medium-voltage devices. For the converters designed in this dissertation at 4.16- and 6.9 kV voltage rating, 3.3- and 4.5 kV IGBTs/MOSFETs must be used. Using total of 12 switches per phase, the converter features a 9-L line-to-line voltage. Also, it is worth to note that the 5-L ANPC converter proposed by ABB (figure 3.23) has advantages over the regular 5-L ANPC topology (which would be achieve by expanding switches in the 3-L ANPC converter). The ABB-introduced converter needs only two dc link capacitors (featuring a single mid-point for it which needs voltage balancing) while the formal 5-L ANPC would have 4 dc link capacitors and a total of 3 mid points for them. Moreover, the number of

Table 3.6 Switching states and their corresponding output voltage in the 5-L ANPC converter.

Switching State	S1	S2	S3	S4	S5	S6	S7	S8	Output
1	*0*	*1*	*0*	*1*	*0*	*1*	*0*	*1*	$-V_{dc}$
2	*1*	*0*	*0*	*1*	*0*	*1*	*0*	*1*	$-V_{dc}/2$
3	*0*	*1*	*1*	*0*	*0*	*1*	*0*	*1*	$-V_{dc}/2$
4	*1*	*0*	*1*	*0*	*0*	*1*	*0*	*1*	0
5	*0*	*1*	*0*	*1*	*1*	*0*	*1*	*0*	0
6	*1*	*0*	*0*	*1*	*1*	*0*	*1*	*0*	$+V_{dc}/2$
7	*0*	*1*	*1*	*0*	*1*	*0*	*1*	*0*	$+V_{dc}/2$
8	*1*	*0*	*1*	*0*	*1*	*0*	*1*	*0*	$+V_{dc}$

switches for the formal 5-L ANPC would be 20 per phase while the recently-introduced 5-L ANPC needs 12 switches per phase to operate.

Table 3.6 shows the switching states and their corresponding output voltage for the 5-L ANPC converter.

3.3.2 Modulation and Control

A level-shifted modulation method is proposed for the 5-L ANPC converter in [117], where the switching state is defined according to sign of the voltages and currents. Although the dc link voltages in this converter are provided by means of diode front-end rectifiers, control schemes are required for balancing the voltages of the flying capacitor as well as the mid-point of the dc link. table 3.7 shows the selected switching state as a function of different parameters such as the output voltage and current sign and the flying capacitor voltage sign. Note that sign of output voltage reference and output current are defined by their magnitude, and sign of the flying capacitor voltage (V_{fc}) is specified by comparing its voltage and reference, where higher voltage across the capacitor compared to the reference means a positive sign and vice versa.

It is worth to note that other modulation schemes such as the selective harmonic elimination (SHE) [119] are proposed for the 5-L ANPC. However, since balancing of voltages (both for flying capacitor and the mid-point of the dc bus) in this topology depend on the switching frequency, using modulations like SHE which are low-frequency in nature will result in significant increase in size and volume of the capacitors installed in the converter. Note that in this dissertation, switching frequency is set to 2.5 kHz as usually done for 5-L ANPC-based drives [120].

3.4 Summary

This chapter discussed the converter topologies used for medium-voltage high-power motor drive application. Total of three topologies (the cascaded H-bridge converter, the modular multilevel converter and the 5-L active neutral point clamped converter) that are capable of reaching higher voltage in the medium-voltage range were discussed, and their basics were investigated. Also, the problem with the MMC converter in requirement for bulk amount of passive

Table 3.7 Switching states and their corresponding output voltage in the 5-L ANPC converter.

Phase Voltage	Sign (V_{fc})	Sing (i_{out})	Sign (V_{ref})	Switching State
$-V_{dc}$	-	-	-	1
$-V_{dc}/2$	*-1*	*-1*	-	2
$-V_{dc}/2$	*-1*	*+1*	-	3
$-V_{dc}/2$	*+1*	*-1*	-	3
$-V_{dc}/2$	*+1*	*+1*	-	2
0	--	-	*-1*	4
0	-	-	*+1*	5
$V_{dc}/2$	*-1*	*-1*	-	6
$V_{dc}/2$	*-1*	*+1*	-	7
$V_{dc}/2$	*+1*	*-1*	-	7
$V_{dc}/2$	*+1*	*+1*	-	6
V_{dc}	-	-	-	8

components was discussed. In order to develop a better understanding of the converter, a steady-state model was developed for it using the well-known average model. Based on the model, a method was proposed to inject the optimum amount of circulating current components to reduce MMC's capacitance requirement. Moreover, based on the average model derived an optimum point was proposed for the MMC converter in AFE mode of operation to minimize its requirement for passive elements (inductances and capacitances) without adding any additional controller or further complexity to the system.

Chapter 4. Design and Modeling Criteria

This chapter discusses the main considerations in design and simulation of the target multilevel converters for medium-voltage high-power motor drive application. In order to realize close designs to the converters existing in industry, the criteria are tried to be adapted from datasheets of the industrial motor drive converters. The present chapter discusses the converter design criteria as well as assumptions/details in the simulation.

4.1 Considerations for Selecting Switching Frequency

The switching frequency in all converters is selected to restrict the output current THD to 2%, considering harmonics up to the 20^{th} order. This criterion is adopted from catalogs of similar industrial drives, as it was deemed sufficient to characterize their electrical performance given the highly inductive nature of the loads in question. Further, this harmonic range is in agreement with the thermal impact of harmonic currents, as [121] and [122] demonstrated that the harmonics within the 20^{th} order are the main components linked to the overheating of motor windings. In commercial products, the switching frequency of the drives based on the CHB converter is in the range of a few hundred hertz up to around 1 kHz. Similar situation exists for the MMC-based drives. Also as mentioned in previous chapter, the switching frequency used for drives based on the 5-L ANPC topology is about 2.5 kHz [120].

It is worth to mention here that one of the main advantages of wide-bandgap semiconductors over existing Si semiconductors is their high switching frequency operation capability. In case of low-voltage drives as well as grid-tied applications, this capability has significant positive impact

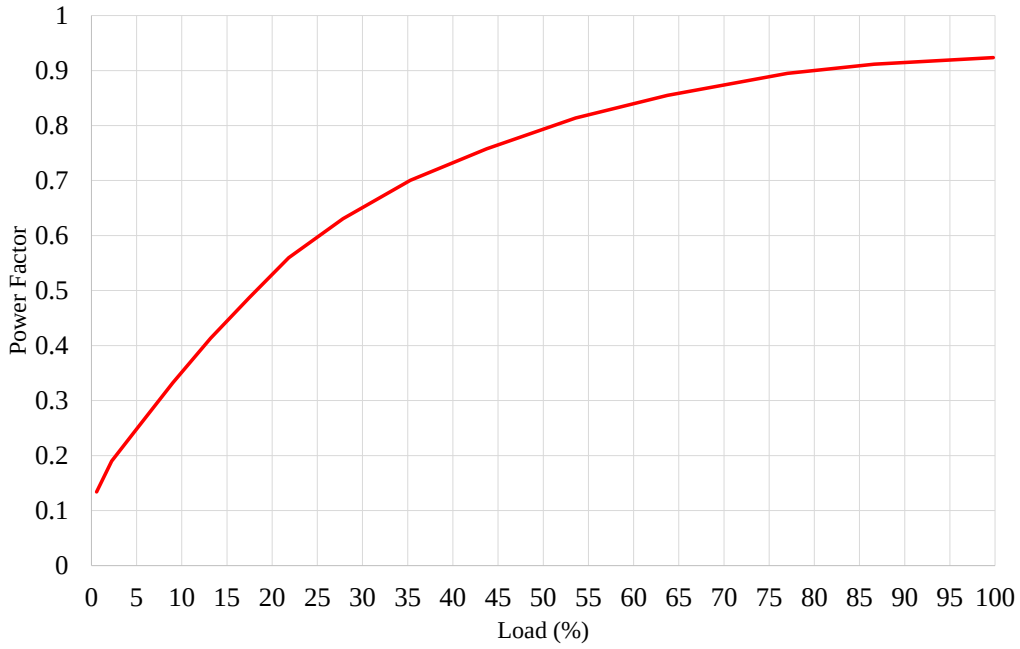


Figure 4.1 Power Factor of a typical high-power induction machine versus its load used as reference for simulations throughout this dissertation.

on efficiency and power density of the system (due to reduction/elimination of passive filters). However, in case of all of the topologies investigated in this study due to lack of load-side filters, increasing switching frequency does not bring about significant benefits. Also, the capacitive filter size in none of the cases reduces significantly by increase in switching frequency.

The motor used in all simulations is an induction machine that has about 0.9 power factor around full load. For power factor at lower frequencies, information from a MW-range motor are used as input where the power factor drops to about 0.2 at close to no-load conditions. Figure 4.1 shows the power factor curve of a high-power induction motor that is used as reference in this dissertation for low-speed operation simulations. An impedance model is used to model the motor and in order to have more realistic waveforms, switching times and the required deadtimes of the

semiconductors (including Si-based IGBTs and SIC MOSFETs) are taken into account in the simulation models.

4.2 Determination of dc Link Voltage and Number of Cells

The first action to be taken when designing a converter for ac drive application is to determine the magnitude of the voltage on its dc side (which is usually provided by diode front-end rectifiers). The minimum dc bus voltage required for CHB, MMC and 5-L ANPC converters operating at $v_{l\text{-}l}$ output ac voltage considering 1/6 of third harmonic injected will be as given in (4.1) and (4.2) [123]. The equations are derived considering that half of the dc link voltage (in case of the MMC and 5-L ANPC converters) or the full dc link voltage (in case of the CHB) must be equal to a minimum of output phase voltage. Assuming third harmonic injection in PWM, the dc voltage utilization increases by 15%, reducing the minimum dc link voltage by the same percentage.

$$v_{dc,CHB} = \frac{v_{l-l}}{\sqrt{2}} \tag{4.1}$$

$$v_{dc,MMC} = v_{dc,ANPC} = v_{l-l} \times \sqrt{2} \tag{4.2}$$

An appropriate percentage of reserve voltage must be considered together with the minimum voltage to guarantee proper operation of the converter under transient conditions and also considering voltage drop on stray impedances and filters (if any used). The amount of the reserve voltage is taken to be 10% in this study based on information from industrial drive vendors.

Full-bridge cells are the building blocks of the CHB topology. Also, the MMC converter is composed of half-bridge cells connected in series. In these modular topologies, the number of cells

must be determined based on the voltage rating of the device used in the structure. For 1.7- and 3.3 kV semiconductors used in CHB and MMC topologies, the dc bus is set to be no more than 1- and 2 kV, respectively, and the number of cells is selected to satisfy this criteria. This is due to the fact that there will be a low-frequency ripple on dc bus in case of each converter, and the voltage overshoot assuming switching even at the peak of capacitor voltage still must stay within safe region for the power semiconductor. On the other hand for 5-L ANPC converter, in a similar way to industrial design 3.3 kV semiconductors are used at 4.16 kV drives, and 4.5 kV rating IGBTs are employed in 6.9 kV.

Six-pulse rectifiers are used as diode front-end in motor drive application for all three converters under study. According to [124], the blocking voltage of the individual diodes used in diode front-end must satisfy (4.3) where v_{grid} is the line side voltage and k is a safety factor that is considered to be 2–2.5 for industrial environments.

$$v_{blocking} = \sqrt{2} v_{grid} \times k \tag{4.3}$$

4.3 Semiconductor Loss Calculation and Heat Sink Design

The method proposed in [116] is used for loss calculation of diodes and switches at different load currents and temperatures. In the mentioned technique, the semiconductor switching and conduction losses are approximated by polynomials as (4.4) and (4.5). Having the instantaneous current being conducted/switched, instantaneous losses are calculated and later integrated to have the average losses over time. Normally datasheets give switching losses at a constant dc bus voltage (for instance, 900V dc bus for 1.7 kV IGBTs and 1.8 kV bus for 3.3 kV IGBTs). If

calculation of losses was needed at a dc voltage other than that, the losses were scaled accordingly as in (4.6).

$$P_{cond} = a_1 i(t) + b_1 i^2(t) \tag{4.4}$$

$$P_{SW} = a_2 i(t) + b_2 i^2(t) \tag{4.5}$$

$$E_{SW,Vbus} = E_{SW,Vref} \times \frac{V_{bus}}{V_{ref}} \tag{4.6}$$

where *i(t)* is the instantaneous current, coefficients a_i and b_i are derived from loss interpolation according to data from datasheet, V_{bus} is the target bus voltage and V_{ref} is the voltage at which the switching losses are given in datasheet. Having the semiconductor losses in hand, the average junction temperature can be calculated from (4.7). The average junction temperature of the semiconductors is restricted to 90% of maximum possible operating temperature, as normally done for similar industrial drives.

$$T_j = T_{HS} + (R_{th,j-c} + R_{th,c-h}) \times P_{loss} \tag{4.7}$$

where T_j is the junction temperature, T_{HS} is the heat sink temperature, $R_{th,j\text{-}c}$ and $R_{th,c\text{-}h}$ are junction-to-case and case-to-heat sink thermal resistances respectively, and P_{loss} is the average loss of the semiconductor. Finally, heat sinks are desinged considering a commercial heat sink with cooling system performance index (CSPI) of 2.48 w/(°C.dm^3), and the heat sink volume is calculated from (4.8). In this equation the heat sink temperature is considered to be 80°C and ambient temperature is 30°C. Also, volume of a fan needed to provide 500 LFM air circulation for the heat sink is considered.

$$T_{HS} - T_{amb} = P_{loss} \frac{1}{CSPI.Vol_{HS}} \tag{4.8}$$

For design purpose, commercial 1.7 kV Si IGBTs (most popular semiconductors used by vendors in CHB- and MMC-based drives) as well as 3.3 kV Si IGBTs (used by Siemens for some CHB-based drives, and by ABB for 4.16 kV 5-L ANPC drives) are selected from Infineon products. In case of 6.9 kV drives based on 5-L ANPC topology, individual semiconductors need to be rated at 4.5 kV. In a similar way, 4.5 kV IGBTs from Infineon are used for this purpose. Last but not least, in order to investigate impact of medium-voltage SiC technology on medium-voltage high-power drives, state-of-the-art non-commercialized 3.3 kV SiC MOSFETs from Sumitomo Electric Industries are used [63]. It is worth to mention here that although at the time this research is being done 1.7 kV SiC MOSFETs are commercially available from Wolfspeed, but due to much higher conduction losses of Wolfspeed's 1.7 kV SiC MOSFETs compared to commercial 1.7 kV Si IGBTs, they do not seem to be a proper option to use in medium-voltage drive application. Also, as will be shown later, when using 1.7 kV semiconductors the switching frequency used for the converters is relatively smaller, where high switching frequency and low switching loss capabilities of low-voltage SiC MOSFETs are not beneficial.

Figure 4.2 shows I-V curves for 1.7 kV IGBT, 3.3 kV IGBT and 3.3 kV SiC MOSFET at 400 A current rating (current ratings are at 25˚C) to give a measure of conduction loss, considering that at given load current the conduction loss would be equal to multiplication of load current and voltage drop across device terminals. The I-V curves are given at the maximum junction temperature at which the semiconductor can operate. As it can be seen, the 3.3 kV SiC MOSFETs features smaller conduction behavior compared to their Si counterpart for the whole shown load

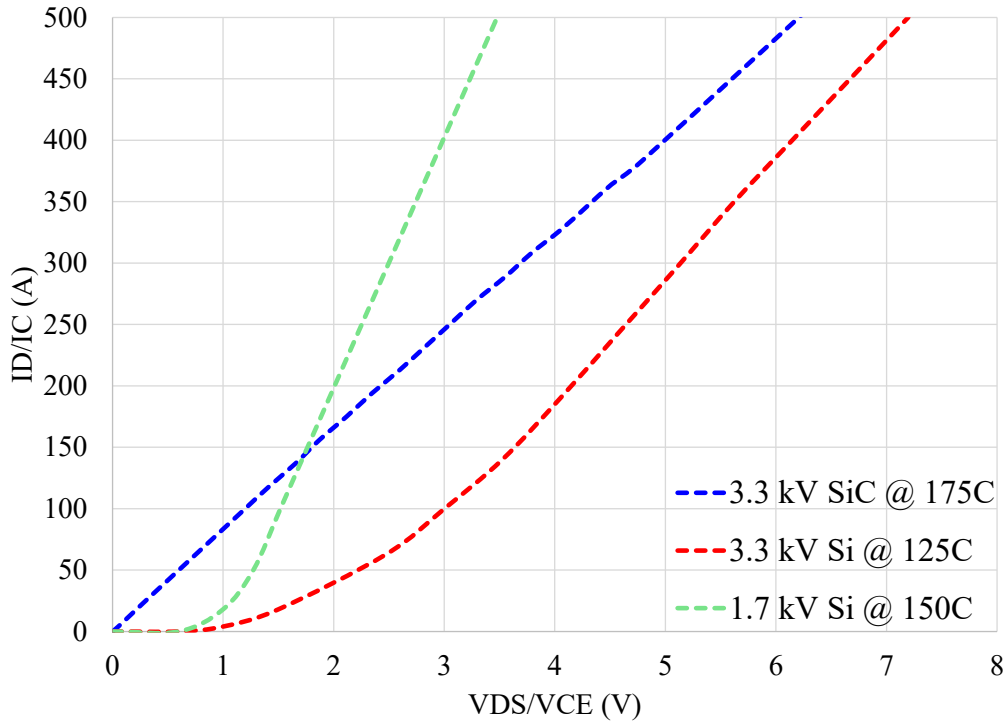


Figure 4.2 Output characteristics of the Si-based IGBTs and the state-of-the-art SiC MOSFETs for a measure of their conduction losses. All devices have 400 A rating at 25˚C.

current interval. Also, the 3.3 kV SiC MOSFETs feature smaller conduction loss compared to 1.7 kV Si IGBTs up to around 150 A load current, which is an outstanding feature of them. Smaller conduction losses of the 3.3 kV SiC MOSFETs is mainly coming from mature technology of their manufacturer (Sumitomo Electric Industries), where compared to other SiC manufacturers, products of Sumitomo Electric feature smallest specific on-resistance [138].

On the other hand, Figure 4.3 demonstrates total switching losses (summation of turn-on and turn-off losses) for the same semiconductors. As it can be seen, the SiC MOSFETs and 1.7 kV Si IGBTs have similar total switching losses, however the switching losses of the 3.3 kV Si IGBTs is about 6-7 times larger compared to the other two.

4.4 Interpolation of Semiconductor Electrothermal Properties

One of the most important factors contributing to a fair comparison between different semiconductor technologies (when investigating impact of SiC MOSFETs on medium-voltage motor drives) is selection of smallest current rating device capable of operating in the converter system. In order to be able to find minimum current rating (die size) of Si IGBTs capable of operation in the defined drive system, conduction and switching losses, thermal resistances and die sizes are continuously interpolated versus current rating. This enables calculation of losses, junction temperature and die size for any given current rating device. For instance, in Figure 4.4 the turn-off energies of 3.3 kV Si IGBTs are shown versus current rating at switching currents from 50 A up to 400 A.

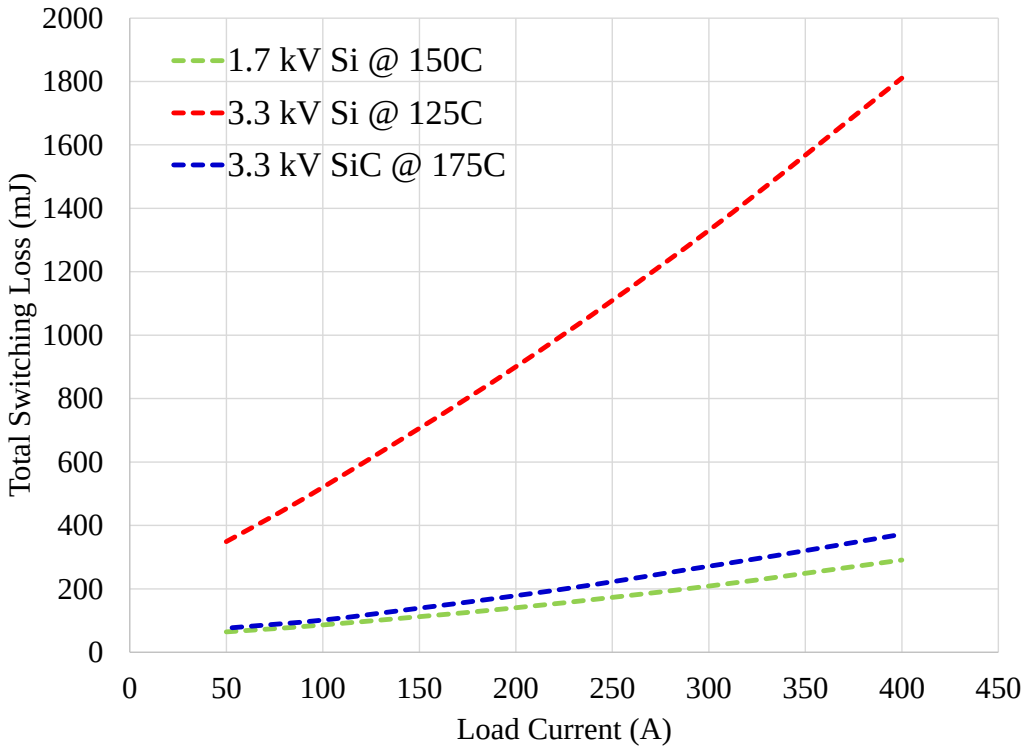


Figure 4.3 Total switching losses of the Si-based IGBTs and the state-of-the-art SiC MOSFETs for load currents up to 400 A. All devices have 400 A rating at 25˚C.

It is worth to note that the increase observed in switching energy versus current rating is due to increase in junction capacitances of the device. Similar interpolations are done for turn-on and conduction losses of the IGBT, as well as conduction and reverse recovery losses of the free-wheeling diode at different temperatures based on loss calculation method proposed in [116]. Figure 4.5 on the other hand shows junction to case thermal resistance of 3.3 kV IGBTs versus current rating which is interpolated in a similar way to enable calculation of thermal resistance for any current rating device. Similar interpolations are done for 1.7- and 4.5 kV IGBTs as well. Also, the estimated die size for 1.7-, 3.3- and 4.5 kV IGBTs in mm^2 versus IGBT current rating is formulated as (4.9)-(4.11), where current ratings are given at 25˚C. Last but not least, package size for devices with different current ratings is interpolated and in next sections, package volume will be used for inverter volume calculation.

$$A_{die-1700} = 0.7762I + 5.24 \tag{4.9}$$

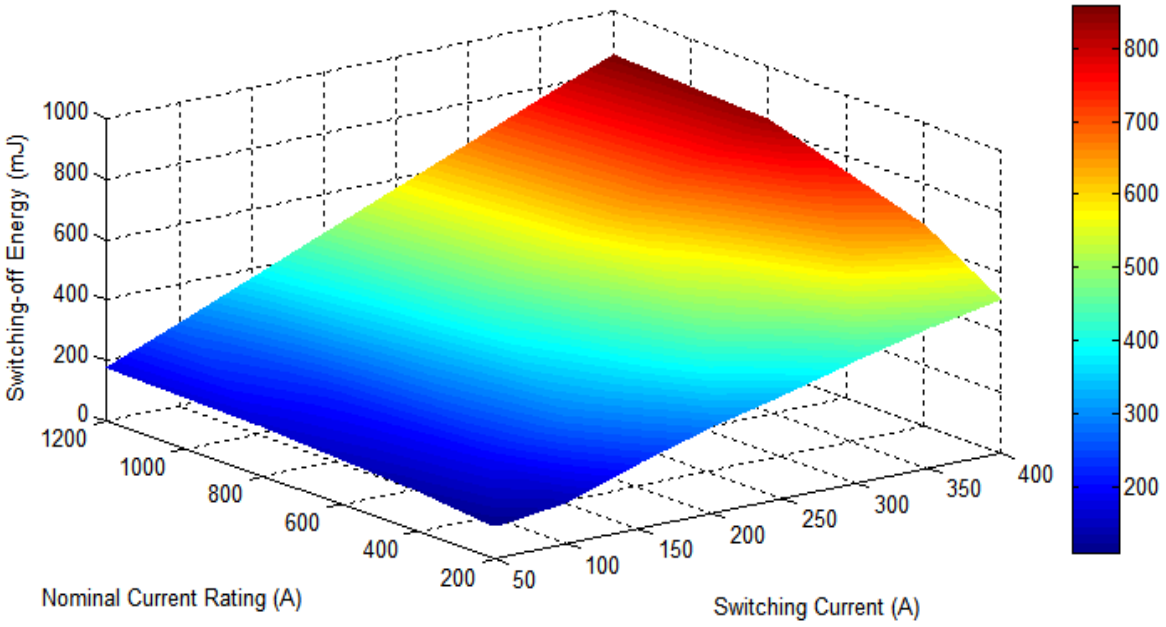


Figure 4.4 Switching losses of 3.3 kV Si IGBTs versus their nominal current rating at different load currents, to enable calculation of switching losses for given current rating IGBT.

$$A_{die-3300} = 1.3749I + 107.84 \tag{4.10}$$

$$A_{die-4500} = 1.4519I + 122.21 \tag{4.11}$$

where I is the current rating of IGBT. Despite Si IGBTs, for 3.3 kV SiC MOSFET existing samples are not enough for interpolation of electro-thermal properties. Thus, estimations are done in order to calculate required electric and thermal specifications of the SiC MOSFETs at current ratings other than 400 A (which is the rating of 3.3 kV SiC MOSFETs tested in [63]). Static characteristics of SiC MOSFETs such as on-resistance and junction-to-case thermal resistance highly depend on the die size (current rating) and can be scaled with current rating as in (4.12) and (4.13). Similar scaling is used for die size, which is 432 mm^2 for 400 A SiC MOSFET.

$$R_{DSon,rated} = R_{DSon,nom}.I_{nom} / I_{rated} \tag{4.12}$$

$$R_{thjc,rated} = R_{th\,jc,nom}.I_{nom} / I_{rated} \tag{4.13}$$

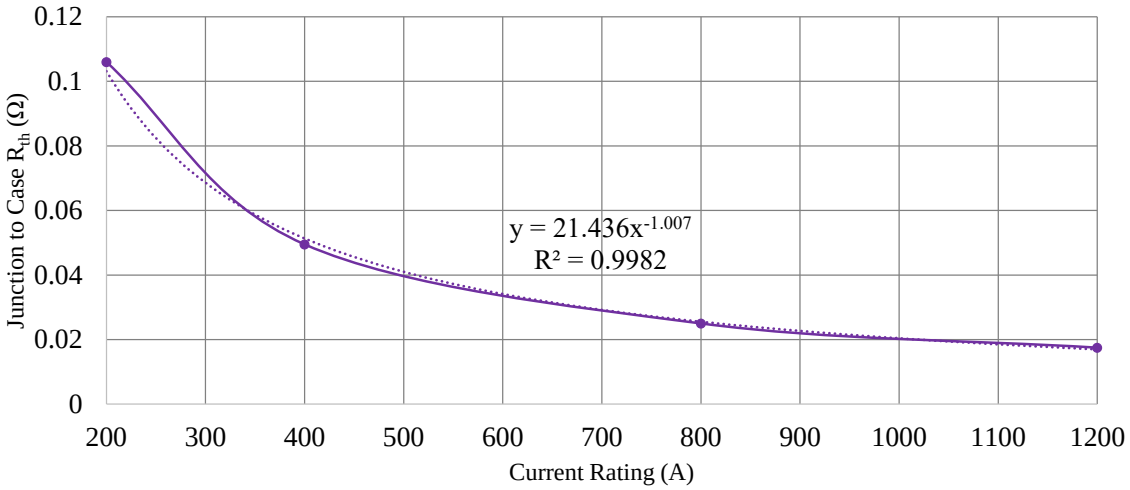


Figure 4.5 Thermal resistance of 3.3 kV Si IGBTs from junction to heat sink versus their current rating.

where I_{nom} is nominal current rating of the MOSFET and I_{rated} is the new rating at which the parameters are required. The switching losses on the other hand are composed of different terms that change in different ways with die size (junction capacitances) and thus, are not straightforward to estimate [126]. Due to the fact that switching losses of SiC MOSFETs are small, and also since variation in switching loss versus die size is not significantly large for a power semiconductor, the switching losses are assumed to remain constant as SiC MOSFET current rating changes. It is worth to mention that the reverse recovery losses of shottky-barrier diodes (SBDs) in SiC modules is neglected since it is negligible compared to MOSFET's switching losses. However, the conduction losses of SBDs are taken into account in loss calculations.

Note that negligible change in switching losses of a power semiconductor versus its current rating can be observed from figure 4.4, where for 6 times (500%) increase in nominal current rating of a Si IGBT, its switching-off loss increases by a factor of around 50%. Also figure 4.6 from [138] (which is showing switching losses of two SiC MOSFETs with same manufacturing technology) demonstrates that for about 37% change in total switching losses when device current rating increases by 350%. Note that in Figure 4.6, Wolfspeed #1 is the 36 A SiC MOSFETs with part number X3M0050090G and Wolfspeed #2 is the 160 A SiC MOSFET with part number C3M0010090D-ES. Other than negligible change is switching losses versus current rating, the fact that majority of the total losses in converters based on SiC MOSFETs is coming from switching losses is another reason that the assumptions made will not introduce significant amount of error to the calculations.

According to manufacturers, the maximum junction temperature for the 1.7 kV Si IGBTs, 3.3 kV IGBTs, 4.5 kV IGBTs and 3.3 kV SiC MOSFETs are 150°C, 125°C, 125°C and 175°C

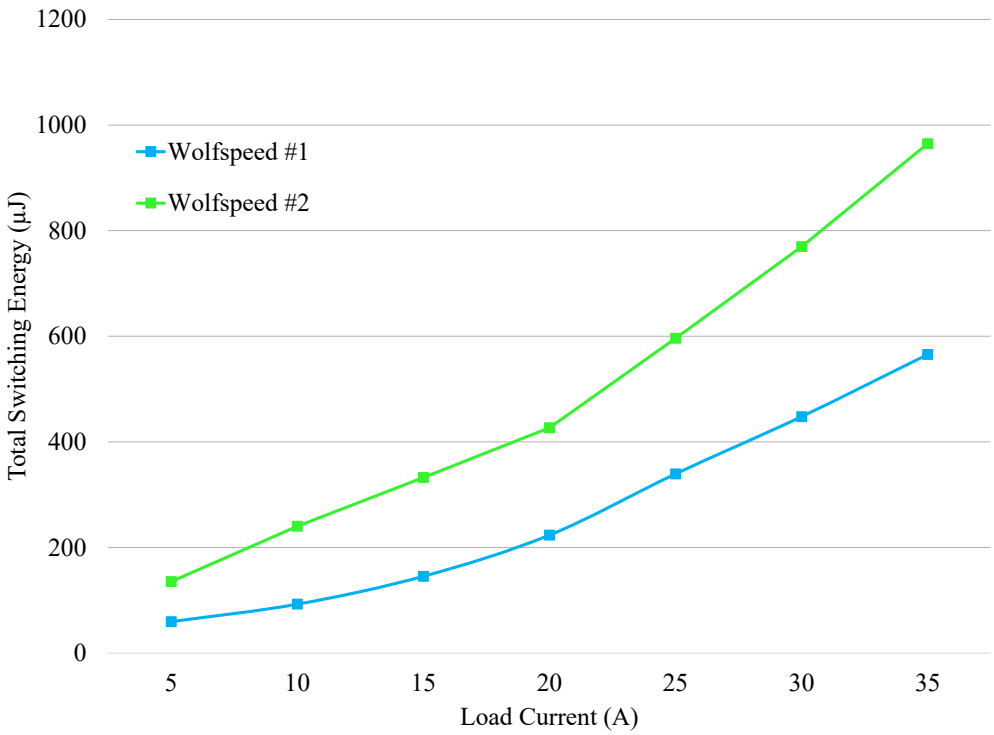


Figure 4.6 Comparison of switching losses between Wolfspeed #1 (900 V 36 A) and Wolfspeed #2 (900 V 160 A) SiC MOSFETs.

respectively. Assuming a heat sink temperature of 80°C which is typical of MV drive systems, average junction temperature of the semiconductors calculated from (4.7), and is restricted to 90% of the maximum possible values in case of each device.

4.5 Dimensioning of the Passive Components

The next step in design process is dimensioning the passive elements of the converters. The filter capacitors that exist in all the converters must be sized according to different criteria. The common considerations in case of all converters are limiting the voltage across IGBTs to safe margins, as well as preventing overmodulation. Considering switching event at the peak of the dc bus voltage, the resulting voltage (dc voltage + ripple + turn-off overshoot) must stay within a safe

range for IGBTs. Thus, summation of dc bus and the ripple on it is usually restricted to around 70% of IGBT's nominal voltage rating. On the other hand, the ripple margins must be defined in a way that switching event at the valley point of voltage does not take the converter to overmodulation, resulting in deterioration of the output voltage.

Other than the common criteria mentioned above, in case of CHB converter the capacitors on the H-bridge cells are selected to restrict the input current THD to borders defined by IEEE 519 standard. Although the maximum ripple across the capacitors must satisfy the above-mentioned criteria as well, the input current quality criteria is usually dominant in case of this topology. It is worthwhile to note that due to operation of the 6-pulse rectifiers of the CHB converter in discontinuous mode (DCM), accurate analytical equations are not available for capacitor bank size needed [127].

On the other hand, the DC bus capacitors of 5-L ANPC converter are selected for input current and output voltage THD satisfaction while the flying capacitors in this topology are sized to restrict the voltage across the outer switches to safe margins. For flying capacitor magnitude, output voltage THD may also introduce restrictions.

Lastly, in case of MMC converter, according to [103] the cell capacitor ripple is restricted to 20%. It is worth noting that in case of MMC converter, submodule voltage ripple will be inversely proportional to the motor speed under constant torque [128]. This makes MMC motor drive inappropriate for applications that require rated torque at lower speeds. However, in case of applications like fans/blowers/centrifugal pumps where the load torque is inversely proportional to a square of speed, the peak voltage across cell capacitors of MMC converter will be even less at lower frequencies than the rated frequency [129]. It should also be noted that the worst case

operating point for fan-like loads for MMC (to specify the design parameters) would be the full-load case, while for high-torque loads the deterministic operation point for converter design would be the startup [130].

The high requirement for capacitances is the main drawback of the MMC topology. In case of MMC converters designed in this study, injection of 2nd circulating current harmonic is used as degree of freedom to reduce capacitor voltage ripple across MMC cells, and thus to reduce the total installed capacitances in converter structure. The injection method explained in chapter 3 is used for this purpose. In addition to the submodule capacitors, the arm inductors of the MMC must be sized. In this study the arm inductors are selected based on the guidelines in [102] and [103], to avoid resonance in circulating current harmonics.

4.6 Multi-pulse Transformer Modeling

In order to realize better approximation of the motor drive converters being used in industry, the leakage impedances of the transformer are also taken into consideration when designing the rectifier stage and sizing the capacitive filters. For this purpose, a model is derived and the leakage inductances of the transformer is estimated based on that. Measurement data from two renown drive manufacturers was used to evaluate validity of the shown model, however, due to non-disclosure agreement (NDA) terms the measurement data are not brought in this dissertation.

For the purpose of modeling the transformer, some information are needed. Transformer rated power, primary side line voltage, secondary side no-load voltage, and frequency are needed to be known and can be determined based on converter specifications. In addition to these, transformer no load current, short-circuit voltage and its X/R ratio in windings are needed to do the modeling.

These values cannot be determined without measurement results. However, according to [123] the data from table 4.1 may be used for transformers of power range 1-10 MVA.

The phase shifting between secondary windings will be no more than 30 degrees. So, every desired phase shift can be achieved using combination of a delta winding which is 0° shifted to the primary winding, as well as a wye winding which is ±30° phase shifted with respect to the primary (figure 4.7). Thus, the turns ratio between windings can be calculated as (4.14) and (4.15), for positive and negative phase shift θ° to the primary side winding, respectively [123].

$$n_{YD,i} = \frac{\tan(\theta_i)}{0.866 - 1.5\tan(\theta_i)} \tag{4.13}$$

$$n_{YD,i} = \frac{\tan(-\theta_i)}{0.866 + 1.5\tan(-\theta_i)} \tag{4.14}$$

where $n_{YD,i}$ is the ratio between wye and delta windings in i^{th} secondary winding. Also the number of turns for primary winding can be calculated from (4.14).

$$n_1 = \frac{U_{N1}}{U_{N20}} \tag{4.15}$$

Table 4.1 Assumptions for transformers in 1-10 MVA power rating range.

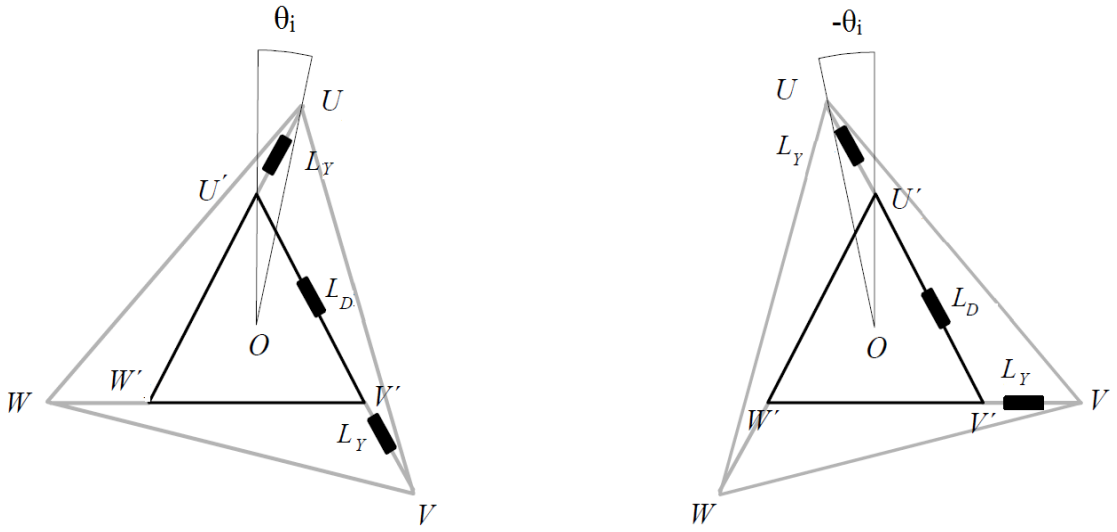
Parameter	Magnitude
No load current [131], [132]	*0.005-0.009 pu*
Short-circuit voltage [123], [133]	*10-20%*
X/R ratio [131], [134]	*20-30*

where U_{N1} is the primary side nominal voltage and U_{N20} is the secondary no-load voltage. With regard to the transformer specifications as well as equations (4.13) and (4.14), the number of turns for delta and wye secondary windings can be calculated from (4.16) and (4.17).

$$n_{D,i} = \frac{1}{\sqrt{[(1+1.5\times n_{YD,i})^2 + (0.866\times n_{YD,i})^2]}} \tag{4.16}$$

$$n_{Y,i} = n_{YD,i} \times n_{D,i} \tag{4.17}$$

Figure 4.8 shows the short circuit behavior of the multi-pulse transformer where according to definition of short-circuit voltage for a multipulse transformer, all secondary windings are. In this figure, $Z_{2,i}$ is the short circuit impedance of the i_{th} secondary winding, resulting from short-circuit of figure 4.7 windings in i^{th} secondary and $Z'_{2,i}$ is the same impedance moved to the primary side.



(a) (b)

Figure 4.7 Secondary windings with (a) $+\theta_i^\circ$ and (b) $-\theta_i^\circ$ phase shift with respect to the primary side winding [123].

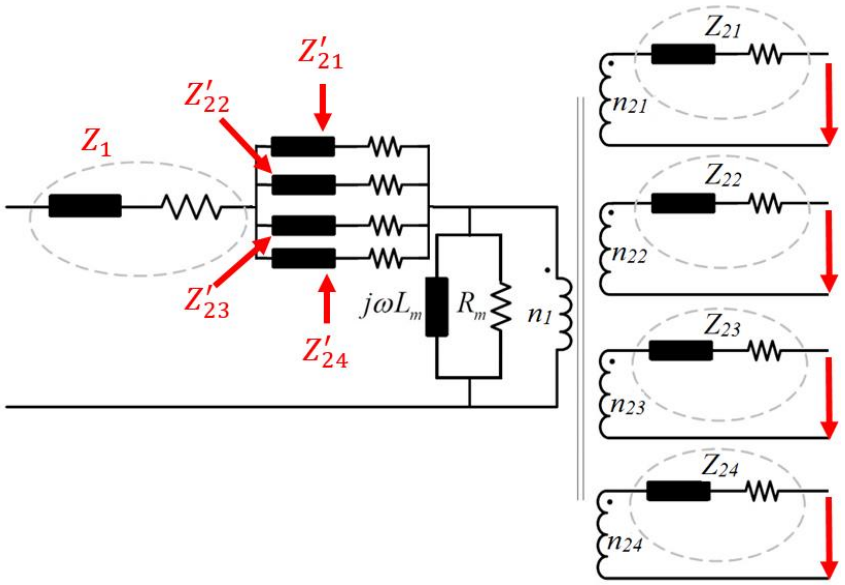


Figure 4.8 Short-circuit behavior of the multi-pulse transformer.

The equivalent impedance resulting from short circuit in delta and wye windings can be calculated from (4.18):

$$Z_{2,i} = \frac{2}{3} Z_{2D,i} + 2Z_{2Y,i} \tag{4.18}$$

Total short circuit impedance of the transformer can be calculated as (4.19). So, the primary side impedance can be calculated from (4.19) with regard to (4.20) to (4.25). Having X/R ratio from table 5.1, primary resistance and inductance will be as (4.20) and (2.21), respectively. With regard to turns ratio, the secondary winding leakage parameters can be calculated in a similar way from (4.22) to (4.23). Note that in (4.22)-(4.25), the N and 1/N coefficients are coming from assuming equal current density in primary and secondary windings. In (4.19), the dominant impedance will be Z1 (especially when the number of secondary windings is large). So, the rest of the impedances can be neglected.

$$Z_{SC} = Z_1 + (Z'_{2,1} \| Z'_{2,2} \ldots \| Z'_{2,n}) \tag{4.19}$$

$$R_1 = \sqrt{\frac{Z_1^{\,2}}{1+(X/R)^2}} \tag{4.20}$$

$$L_1 = \frac{(X/R)}{2\pi f} \times R_1 \tag{4.21}$$

$$R_{2i,D} = (\frac{n_{2i,D}}{n_1})^2 \times N \times R_1 \tag{4.22}$$

$$R_{2i,Y} = (\frac{n_{2i,Y}}{n_1})^2 \times N \times R_1 \tag{4.23}$$

$$L_{2i,D} = (\frac{n_{2i,D}}{n_1})^2 \times \frac{1}{N} \times L_1 \tag{4.24}$$

$$L_{2i,Y} = (\frac{n_{2i,Y}}{n_1})^2 \times \frac{1}{N} \times L_1 \tag{4.25}$$

In equations (4.19) to (4.25), Z_1 is the primary impedance, N is the number of secondary windings, R_1 and L_1 are the primary winding leakage resistance and inductance, $R_{2i,D}$ is the ith secondary's delta connected winding resistance, $R_{2i,Y}$ is the ith secondary's wye connected winding resistance, $L_{2i,D}$ is the ith secondary's delta connected winding inductance and $L_{2i,Y}$ is the ith secondary's wye connected winding inductance.

Table 4.2 Basic Converter Design Data

Quantity	Value
Motor voltage	4.16-, 6.9- and 13.8 kV
Motor power	3- and 5 MVA
Input voltage to transformer	13.8 kV
Output voltage frequency	0-60 Hz
Output voltage THD	2%, considering harmonics up to 20^{th}
Input current THD	5%, according to IEEE519
Load power factor	0.9 around full load
IGBT/MOSFET junction temperature	90% of maximum allowed value
Heat sink temperature	80°C
Ambient temperature	30°C

4.7 Converter Design Data

According to the explained criteria so far (summarized in table 4.2), the converters are designed and the details are shown in tables 4.3-4.6. In the tables the dc link voltage, switching frequency, minimum current rating of semiconductors satisfying operation, number of cells (for MMC and CHB), capacitances installed in structure of the converters, RMS current rating of capacitors and the arm inductors (in case of MMC only) are shown.

In the design process the output frequency of the converter is considered to be at 60Hz. In case of MMC and CHB converters, design in done using both LV and MV Si IGBTs as well as MV SiC MOSFETs. However, in accordance with commercial drives in industry, for 5-L ANPC topology design is performed using 3.3 kV Si IGBTs and 3.3 kV SiC MOSFET for converters at 4.16 kV output voltage, and using 4.5 kV Si IGBTs for converters at 6.9 kV voltage rating. When

Table 4.3 CHB and MMC converters' specifications – 4.16 kV

	3 MVA		5 MVA	
	CHB	MMC	CHB	MMC
dc link voltage	3235.7 V	6471.4 V	3235.7 V	6471.4 V
Switching frequency (using LV/MV switches)	660/1440 Hz	1200/2160 Hz	660/1440 Hz	1200/2160 Hz
Semiconductor rating (using LV/MV Si IGBTs, rated @ 25˚C)	519/1266 A	476/1383 A	550/1932 A	746/1971 A
Semiconductor rating (using MV SiC MOSFETs rated @ 25˚C)	320 A	325 A	530 A	530 A
Number of cells/phase (using LV/MV switches)	4/2	14/8	4/2	14/8
Capacitance per cell (using LV/MV switches)	2.6/1.7 mF	1.62/0.81 mF	4.2/2.75 mF	2.88/1.26 mF
Capacitor RMS current (using LV/MV switches)	320/296 A	102/90 A	504/484 A	156/141 A
Arm inductance (using LV/MV switches)	-	100/350 µH	-	100/150 µH

designing the converters, switching times and required deadtimes are considered for the utilized semiconductors.

4.8 Summary

This chapter presented the criteria used for design of the converters under study. In order to ensure a close design to the converters existing in industry, the criteria was tried to be adopted from datasheets of the existing motor drives, as well as information gathered from manufacturers. It was shown that the switching frequency does not need to be high for converters used for medium-voltage high-power motor drive application, since the motors themselves are big filters. The loss calculation method used was explained in brief and the interpolation procedure for electrothermal properties of the semiconductors was shown. Last but not least, a model was

Table 4.4 CHB and MMC converters' specifications – 6.9 kV

	3 MVA		5 MVA	
	CHB	MMC	CHB	MMC
dc link voltage	5365 V	10731 V	5365 V	10731 V
Switching frequency (using LV/MV switches)	480/1080 Hz	960/1200 Hz	480/1080 Hz	960/1200 Hz
Semiconductor rating (using LV/MV Si IGBTs, rated @ 25˚C)	280/776 A	388/737 A	483/1129 A	544/1188 A
Semiconductor rating (using MV SiC MOSFETs rated @ 25˚C)	200 A	210 A	376 A	345 A
Number of cells/phase (using LV/MV switches)	6/3	22/12	6/3	22/12
Capacitance per cell (using LV/MV switches)	1.4/0.8 mF	0.73/0.36 mF	2.3/1.28 mF	1.38/0.63 mF
Capacitor RMS current (using LV/MV switches)	220/194 A	46/37 A	360/327 A	75/86 A
Arm inductance (using LV/MV switches)	-	700/1000 µH	-	500/650 µH

derived to estimate parasitic impedances of the windings of the multipulse transformer, and the design data were shown following that. The data presented in this chapter will be used for comparison purposes in the next chapters.

Table 4.6 CHB and MMC converters' specifications – 13.8-kV

	3 MVA		5 MVA	
	CHB	MMC	CHB	MMC
dc link voltage	10731 V	21468 V	10731 V	21468 V
Switching frequency (using LV/MV switches)	480/540 Hz	480/480 Hz	480/540 Hz	480/480 Hz
Semiconductor rating (using LV/MV Si IGBTs, rated @ 25˚C)	172/286 A	185/306 A	226/423 A	239/443 A
Semiconductor rating (using MV SiC MOSFETs rated @ 25˚C)	100 A	90 A	125 A	160 A
Number of cells/phase (using LV/MV switches)	11/6	44/22	11/6	44/22
Capacitance per cell (using LV/MV switches)	0.65/0.38 mF	0.337/0.162 mF	1.05/0.65 mF	0.63/0.27 mF
Capacitor RMS current (using LV/MV switches)	90/80 A	28.2/23 A	152/176 A	45.5/47 A
Arm inductance (using LV/MV switches)	-	1900/2500 µH	-	1400/2000 µH

Table 4.5 5-L ANPC converters' specifications

	4.16 kV		6.9 kV	
	3 MVA	5 MVA	3 MVA	5 MVA
dc link voltage	6471 V	6471 V	10731 V	10731 V
Switching frequency (using MV Si IGBTs/MV SiC MOSFETs)	2.5/2.5 kHz	2.5/2.5 kHz	2.5/- kHz	2.5/- kHz
Semiconductor rating (using MV Si IGBTs/MV SiC MOSFETs @25˚C)	1795/330 A	2598/570 A	1929/- A	2540/- A
Bus capacitor	0.25 mF	0.45 mF	0.1 mF	0.18 mF
Capacitor RMS Current	188 A	326 A	120 A	200 A
Flying capacitor	0.15 mF	0.2 mF	0.1 mF	0.15 mF
Capacitor RMS Current	228 A	388 A	141 A	235 A

Chapter 5. Converter Comparison

So far the characterization procedure/results were shown for the utilized semiconductors and the converter design criteria were discussed. Also, the important specifications for the designed converters were shown. In this chapter the topologies are compared from different points of view such as efficiency, energy stored in their structure (J/kVA), installed semiconductor die size, power density, low-speed operation capability, fault containment and number of parts (for measure of reliability). All of the figures demonstrated in next subsections use the same legends. For CHB, MMC and 5-L ANPC converters, blue, red and green colors will be used, respectively. Also, the bars with solid colors are showing designed converters using low-voltage (1.7 kV) Si IGBTs while the striped bars are used for converters designed with medium-voltage Si IGBTs (this includes 3.3 kV Si IGBTs for CHB and MMC converters, and 3.3- and 4.5 kV Si IGBTs for 5-L ANPC at 4.16- and 6.9 kV motor voltage). Finally, the dotted bars are used for designed converters using the state-of-the-art 3.3 kV SiC MOSFETs.

5.1 Efficiency

Efficiency is the most important criteria when selecting a topology for motor drive in general applications. According to ABB's report [52], about 28% of the electricity in the world is being consumed by industrial motors. The fact that the power needed for industrial motors needs to be processed by motor drive converters shows the importance of efficiency in motor drive systems. For the converters under study in this dissertation, figure 5.1 shows the efficiency at different voltage and power levels. The shown results are acquired considering the power loss on power semiconductors in inverter stage.

According to figure 5.1, when designed using LV Si IGBTs the CHB converter is always higher efficient than the MMC. This is simply due to around double number of switches used in structure of MMC converter compared to CHB (this will be discussed in next subsections). On the other hand, the 5-L ANPC is not designed using LV Si IGBTs since it is a topology based on medium-voltage semiconductors.

When designed using the medium-voltage Si IGBTs, in general the CHB and MMC converters feature less efficiency compared to the case with LV Si IGBTs. It is clear that by using MV Si IGBTs, number of cells in modular structures (CHB and MMC) reduces to around half compared to the case with LV Si IGBTs. In order to keep the same power quality, at lower voltage levels (3.16- and 6.9 kV) higher switching frequencies must be used, which results in efficiency drop. However, at 13.8 kV there is no need to use higher switching frequency for similar power quality. In this case, the switching frequency of converters using both semiconductor technologies investigated is defined by other constraints such as bandwidth requirement of the controllers. This

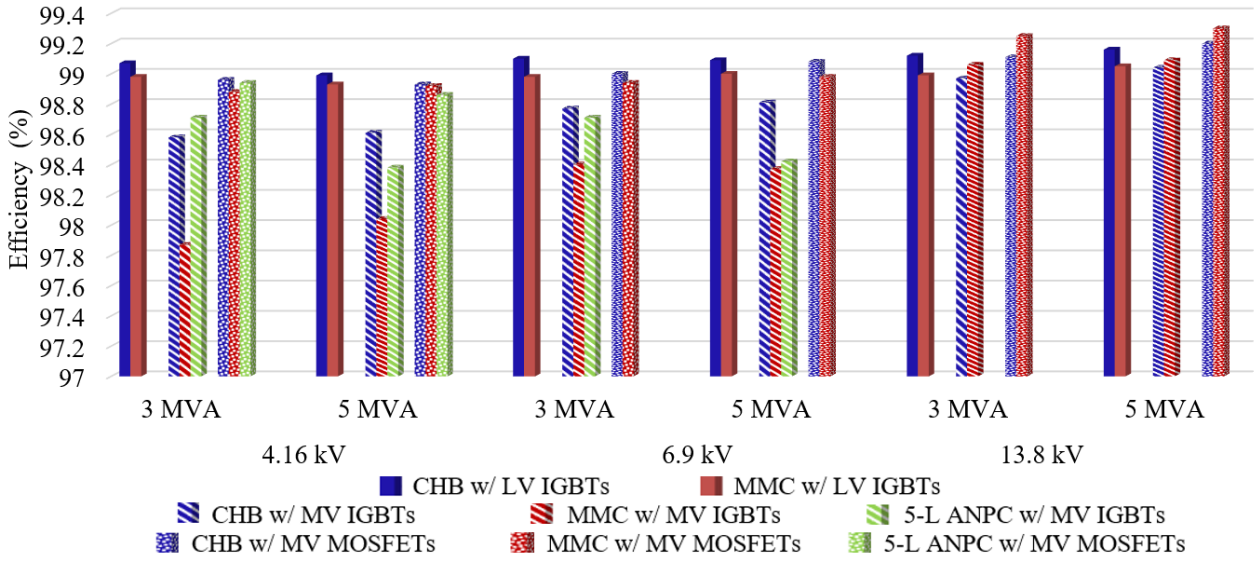


Figure 5.1 Converter efficiency calculated from semiconductor losses of the inverter stage.

is the reason why efficiency of the CHB and MMC converters using LV and MV Si IGBTs is close to each other at 13.8 kV voltage rating. It is worth to mention that in this study the minimum switching frequency is adopted from catalogs of industrial drives at similar operating conditions. Another reason contributing for less efficiency in case of MV Si IGBTs is higher conduction and switching losses of a 3.3 kV Si IGBT compared to two 1.7 kV Si IGBTs at the same current rating (shown in the previous chapter in figure 4.2).

On the other hand when using Si IGBTs, the 5-L ANPC features less efficiency than CHB and MMC converters which is mainly attributed to higher switching frequency in semiconductors of the 5-L ANPC. As the rated power of the converter increases, efficiency of this topology decreases mainly due to increased switching losses at higher currents. This is the main reason why the 5-L ANPC-based drives cover lower powers in medium-voltage range.

Last but not least, when using 3.3 kV SiC MOSFETs for CHB and MMC converters, at 4.16- and 6.9 kV voltage ratings efficiency is smaller compared to the case where LV Si IGBTs are used. One of the reasons contributing for this is that the previously-mentioned higher switching frequency for SiC-based converters at lower voltages. Another reason for smaller efficiency of converters using SiC MOSFETs is that these semiconductors are capable of operating at higher temperatures, and at similar current rating feature smaller thermal resistance from junction to case [1] than Si IGBTs. Thus, at given operating point, the current rating of MV SiC MOSFETs satisfying operating is much smaller than Si IGBTs, resulting in higher conduction losses for them (shown in figure 5.2). Both of these factors pale when the voltage level increases to 13.8 kV, where switching frequency of LV Si-based and MV SiC-based converters becomes equal, and conducted current also becomes smaller. Thus, at 13.8 kV operating point the MV SiC MOSFETs feature

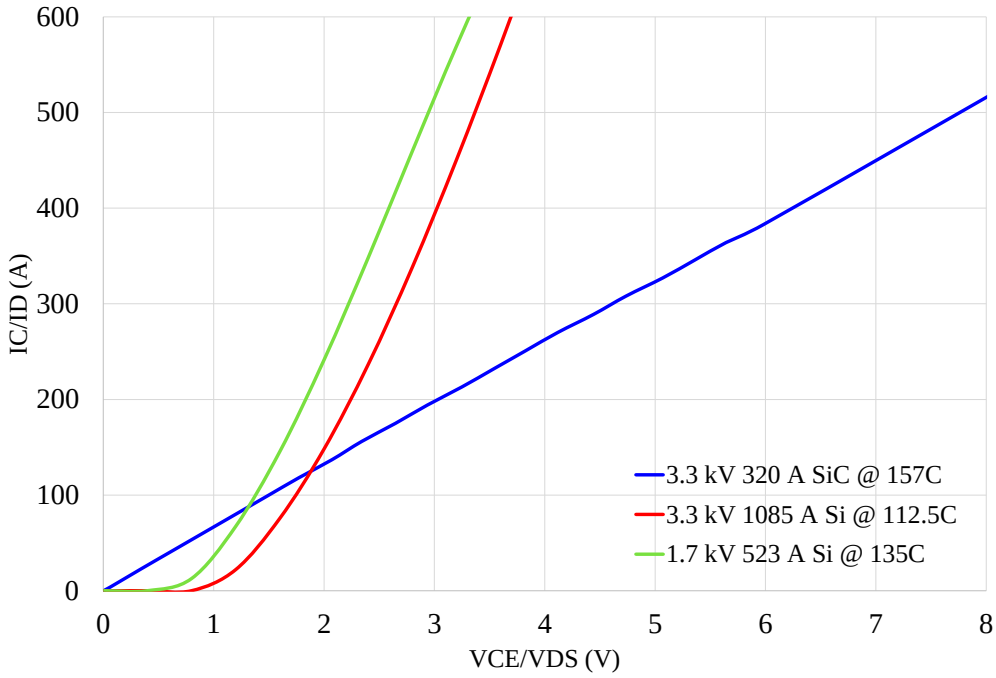


Figure 5.2 I-V curves of the semiconductors used for 4.16 kV 3 MVA CHB converter to show smaller current rating (and thus, higher conduction losses) for SiC MOSFET used.

higher efficiency than the LV Si IGBTs for CHB and MMC converters. On the other hand, the 5-L ANPC converter when it is equipped with SiC MOSFETs features significantly higher efficiency. This is due to the fact that a considerable part of the losses in this converter is related to switching losses of the semiconductors and by using SiC MOSFET which feature significantly smaller switching losses compared to their Si counterpart, efficiency can be improved. According to figure 5.1, by using SiC MOSFETs the 5-L ANPC converter features competitive efficiency to CHB and MMC. It is expected that the maximum power rating at which the *ACS2000* drives of ABB (which are based on 5-L ANPC converter) are available will increase when medium-voltage SiC MOSFETs are used in them. It is worth to mention that according to catalogs, the maximum power rating of current commercial *ACS2000* drives is around 4 MVA.

5.2 Capacitance Requirement

Capacitors installed in motor drive system structures are one of the important aspects directly impacting their footprint and overall power density. They also naturally affect the cost of these units in a significant way. For instance, according to Siemens in case of MMC converters used for different applications about 75% of cell volume is occupied by the capacitors installed inside of it, which is the main drawback and tradeoff of this otherwise flexible and scalable power conversion solution. This study considers energy stored per power rating of drives (J/kVA) as a measure of capacitance requirement for comparison purposes. The total Joule per kVA stored in capacitances of the designed converters is shown in figure 5.3.

As expected and can be seen from figure 5.3, the capacitance requirement of the MMC topology is the highest regardless of the semiconductor type used, which eventually will result in smaller power density for the converter. On the other hand, the 5-L ANPC converter requires smallest capacitive energy stored compared to other topologies. Small capacitance requirement by this topology results in higher power density (discussed in next sections), making the 5-L ANPC converter more attractive. Last but not least, capacitive energy storage of CHB-based drives is in between those based on MMC and 5-L ANPC.

It is worth to note that the J/kVA requirement is similar for converters when MV semiconductors (Si IGBTs or SiC MOSFETs) are used. Also, when using MV semiconductors, compared to the case with LV Si IGBTs, the J/kVA requirement of the MMC converter reduces. This is due to the fact that the MMC is a nonlinear topology, and by cutting number of cells in half when MV semiconductors are used, the arm inductor selected and the corresponding optimum

circulating current that is injected to reduce capacitor bank size change. On the other side, when MV semiconductors are used the J/kVA requirement in case of the CHB converter increases compared to the case with LV Si IGBTs. According to the aforementioned fact, the capacitors of the CHB are sized to satisfy IEEE 519 standard at the multi-pulse transformer's primary side. When reducing the number of cells in half, less number of harmonics are eliminated from transformer's primary side, resulting in larger capacitance requirement to compensate for that. The increase in J/kVA is more obvious in case of 4.16 kV designs, where by reducing number of H-bridge cells in phase from 4 to 2 by using MV switches, lower frequency current harmonics are introduced to the phase current. Since the magnitude of lower-frequency ripple on capacitor voltage and current is higher than the high frequency harmonics, the increase in capacitance requirement is more sensible in this case.

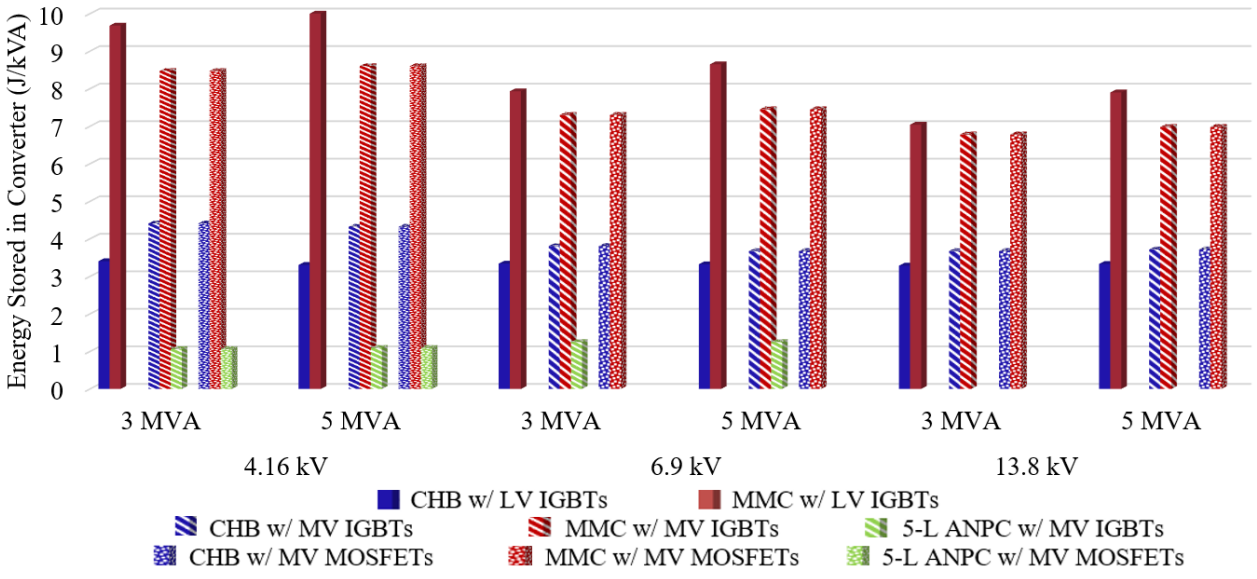


Figure 5.3 Total energy stored in converter capacitors in J/kVA.

5.3 Total Installed Die Size

Current ratings for semiconductors are all given in tables 5.3 to 5.6 for designed converters. However, current rating cannot tell everything on semiconductor utilization of topologies. This is mainly due to the fact that in case of Si IGBTs, for same current rating more die size is installed compared to SiC MOSFETs (due to higher current density and better thermal resistance of SiC material). Also, for the same current rating Si IGBTs of similar technology, at different voltage ratings the die size installed is different. Last but not least, sometimes different vendors have different criteria for specifying current rating of their semiconductors.

Die size of different Si IGBTs were given in (4.9)-(4.11) versus their current rating. On the other hand in case of the 3.3 kV SiC MOSFETs, at current ratings other than 400 A the die size is scaled proportional to current rating and considering that the total die size for 3.3 kV SiC MOSFET at 400 A is 432 mm^2 per switch. For each of the converters at given operating voltage and current, figure 5.4 shows the total die size of switches installed in the structure in cm^2. According to this figure, at all voltage and power levels and using any type of semiconductor, the CHB topology needs smallest amount of die size installed which will result in minimum cost for this topology from semiconductor point of view. Since MMC has almost always about double number of semiconductors in its structure, the total die size for MMC is around twice that of CHB regardless of semiconductor technology. On the other hand due to utilization of higher current rating switches in 5-L ANPC converter, it needs high amount of die size installed using any semiconductor technology.

According to figure 5.4, die size of CHB and MMC converters at given operating point using MV Si IGBTs is higher than when using LV Si IGBTs. This is mainly attributed to higher losses of MV Si IGBTs (which needs higher die area to dissipate the heat) as well as their larger die size at similar current rating. However, in case of all converters, the MV SiC MOSFETs need smallest die size to be installed in the converter structure. According to literature, the SiC material features 3 times better thermal conductivity compared to Si, and also according to figures 5.2 and 5.3, at similar die size both conduction and switching losses of SiC switches are much smaller in comparison. Consequently, the total die size installed in the structure of converters satisfying operating is much smaller according to figure 5.4.

5.4 Total Inverter Volume

An important aspect of comparison between investigated topologies is to consider their power density. In this study, the total volume occupied by converters consisting of volume of power

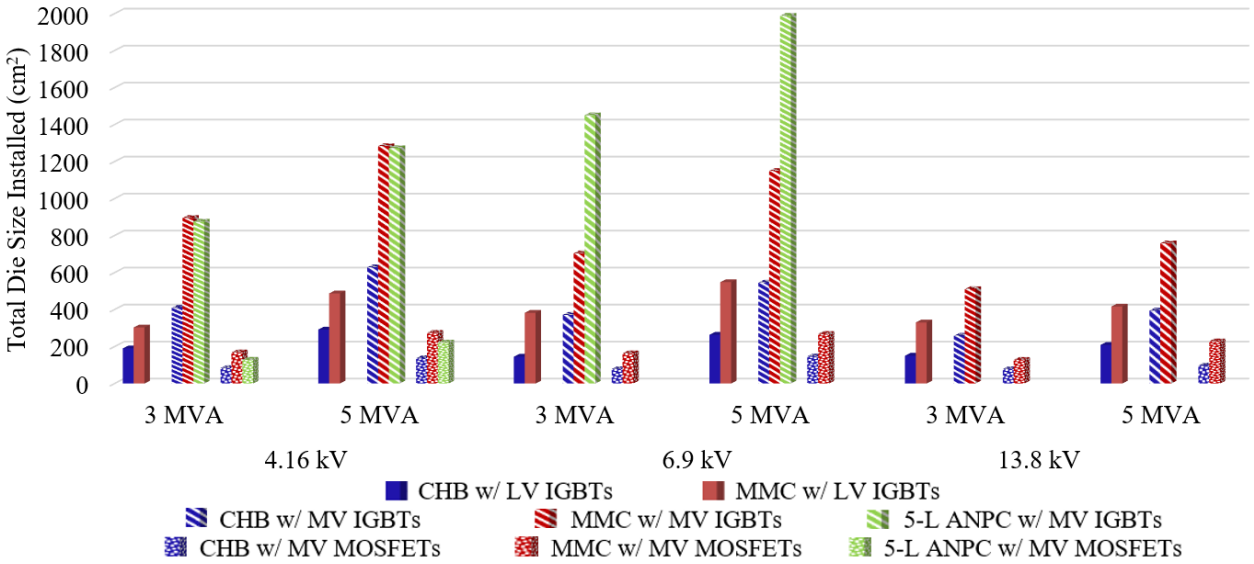


Figure 5.4 Total semiconductor die size installed in converter structure (in cm^2), calculated from power switches.

semicondcutors, heat sinks, fans, capacitors and inductors (just in case of MMC) is used to give a measure of their power density. Figure 5.5 shows total converter volume in dm^3 considering size of the mentioned parts. It is worth to mention that volume of power switches is calculated from datasheets, by interpolating volume of packages versus current rating. Also the heat sinks and fan volume is measured from (4.8), considering a typical heat sink characteristics that is used for similar applications. Last but not least, the capacitor banks are designed using FFLI series of Film capacitors from AVX.

According to figure 5.5, independent from semicondcutor technology used the MMC converter always occupies highest volume. As mentioned in the previous subsections, this is mainly contributed by the capacitors of the MMC. On the other side, the 5-L ANPC converter features smallest foot print, resulting in highest power density for it among the investigated converters.

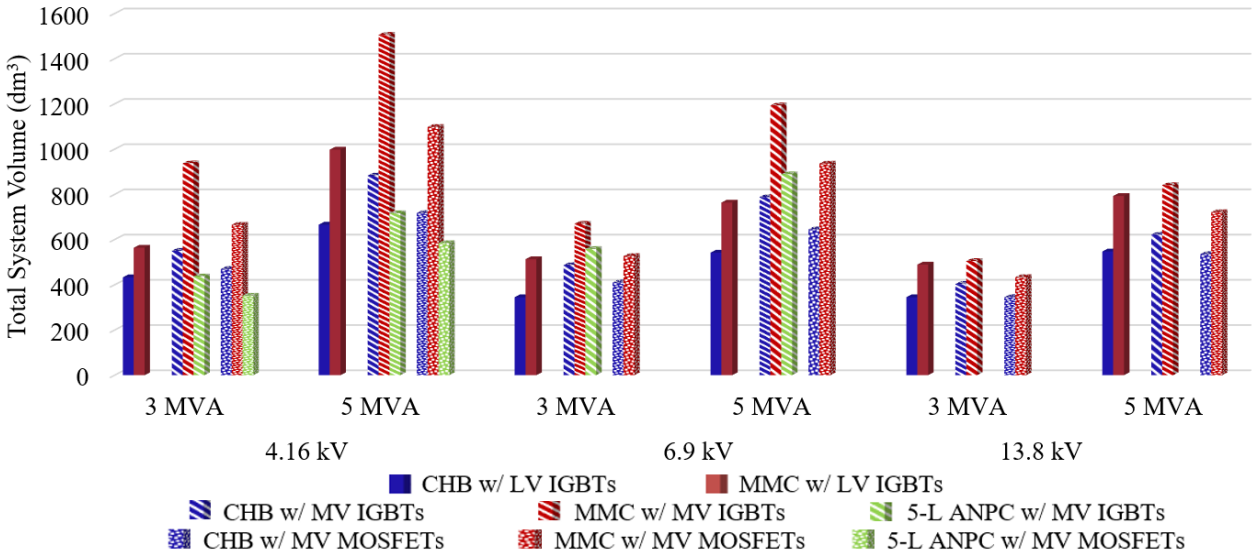


Figure 5.5 Total converter volume in dm^3 consisting of power semiconductors, heat sinks, fans, capacitors and inductors (in any used) volume.

In volume calculation, since a considerable percentage of the calculated size is coming from heat sink and fan, it is natural that this curve shows a meaningful similarity with efficiency curve. According to figure 5.5, using medium voltage SiC MOSFETs features smaller size for the converter compared to 3.3 kV IGBTs. However, when compared to LV Si IGBTs, the 3.3 kV SiC MOSFETs feature higher power density only at the highest investigated voltage level.

It is worth to note here that the volume calculation in this section does not reflect creepage and clearance distances used within different topologies. In real applications, it is expected that the finished volume of the converter will increase proportional to its number of components, which will result in a larger gap between the 5-L ANPC and CHB, and also between CHB and MMC. This is due to largest number of components for MMC and least number of components for 5-L ANPC, as discussed in next subsections

5.5 Low-Speed Operation Capability

Every motor needs to start operation from zero speed and increase its speed up to the nominal value. Also, in some applications such as ship propulsion, the motor needs to drive the load at lower speeds for long times. Thus, the converter that is being selected for motor drive application must be capable of satisfying operation for the whole speed (output frequency) range.

According to literature and the datasheets of industrial motor drives based on CHB and 5-L ANPC converters, these topologies do not face any restriction from thermal or dc link voltage fluctuation point of view for the whole frequency range. Also, from design point of view the worst case to consider for these converters is the full speed. However, it has been well addressed in several studies that the MMC converter faces restrictions at lower speeds when used with high-

torque loads [130]. According to (5.1), the voltage ripple on capacitors of the MMC changes in opposite direction with the output frequency of the converter (speed of the motor). When used to drive loads with constant (or high) torque demand at lower speeds, since the output current stays high (or constant, in case of loads that need constant torque at lower speeds) the ripple increases as speed reduces. However, it is shown in [129] that for some loads such as fans, blowers and centrifugal pumps, since the output torque (phase current) also reduces with reduction in speed, the converter can operate at lower frequencies without any problem.

$$\Delta U_C \quad \alpha \quad \frac{I_{ph}}{\omega C} \tag{5.1}$$

where I_{ph} is the phase current of the motor, ω is output angular frequency and C is capacitance per phase. Injection of high frequency circulating currents is proposed as a solution for solving the high ripple problem at lower frequencies [129], [130], but due to high switching frequency requirement and significant amount of losses created, it can only work for short amount of time (startup) rather than continuous operation at lower frequencies. Also the worst-case operating point for MMC converter in motor drive application where a high-torque load is used is the startup. Thus, in order to satisfy operating under such conditions more semiconductors die size needs to be installed. Figure 5.6 shows the peak voltage across capacitors of different converters designed for 4.16 kV 3 MVA case for both low-torque and high-torque applications. According to this figure, high torque at lower frequencies will interfere with operation of the MMC converter, causing damage to its switches due to overvoltage.

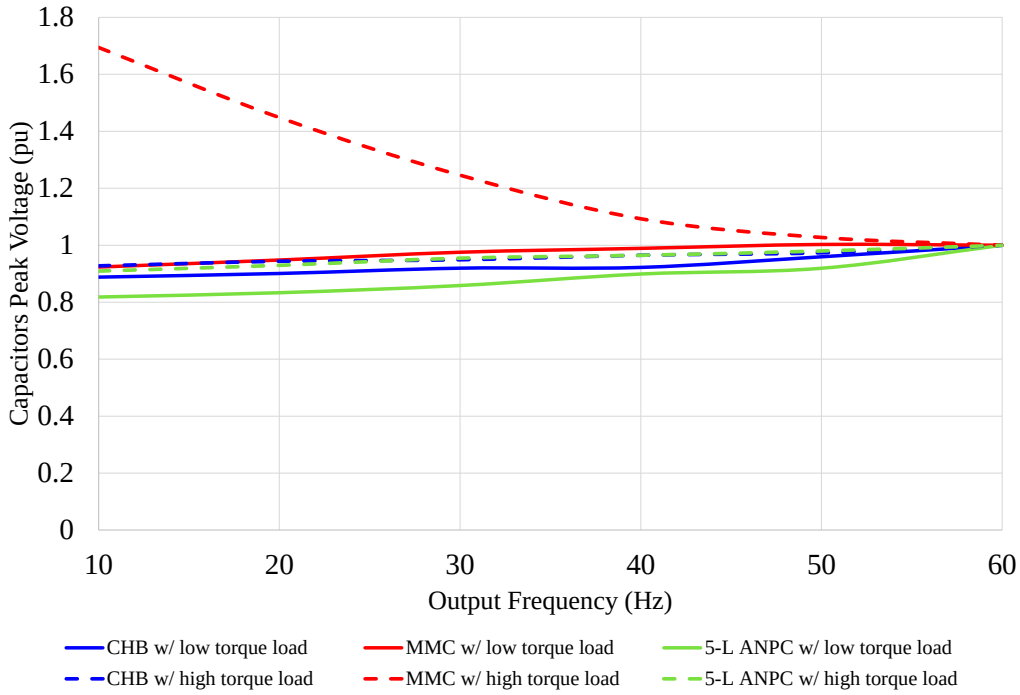


Figure 5.6 Low-frequency operation of the converters designed for motor drive application at 4.16 kV 3 MVA case, under low-torque and high-torque loads.

5.6 Fault-Tolerant Operation Capability

The industrial motors are playing a vital role in the environment that they are being used, and in some applications they are operating non-stop for long times. Since failure in operation of the converter driving a motor can stop the motor from rotating, fault-tolerant operation capability is one of the important aspects in comparison of topologies. Faults can be introduced to the converters due to failure in semiconductors, fans, passive components as well as communication/control units.

According to datasheets of CHB-based drives, if failure happens inside a cell within the converter, the cell will be bypassed and the converter can continue to operate. In this case by modifying the phase angles of the phase voltages of the converter with respect to each other,

symmetrical line voltages can be achieved for the motor (figures 6.7(a) and (b)). Magnitude of the line voltage with one cell bypassed in one of the phases can be calculated from (5.2).

$$v_{l-l,new} = \frac{2n-1}{2n} v_{l-l} \tag{5.2}$$

where n is number of cells per phase and v_{l-l} is the nominal line voltage of the converter. On the other hand, for the MMC converter auxiliary cells are usually placed within the converter phases, so that in case of failure in one cell it can be bypassed and an auxiliary cell can start working instead. This will guarantee uninterrupted operation of the converter without any reduction in the output voltage. Last but not least, despite the modular structures discussed in this study the 5-L ANPC converter does not feature fault-tolerant operation. If one of the semiconductors or its corresponding gate driver/communication fails, operation of the whole converter will be interrupted.

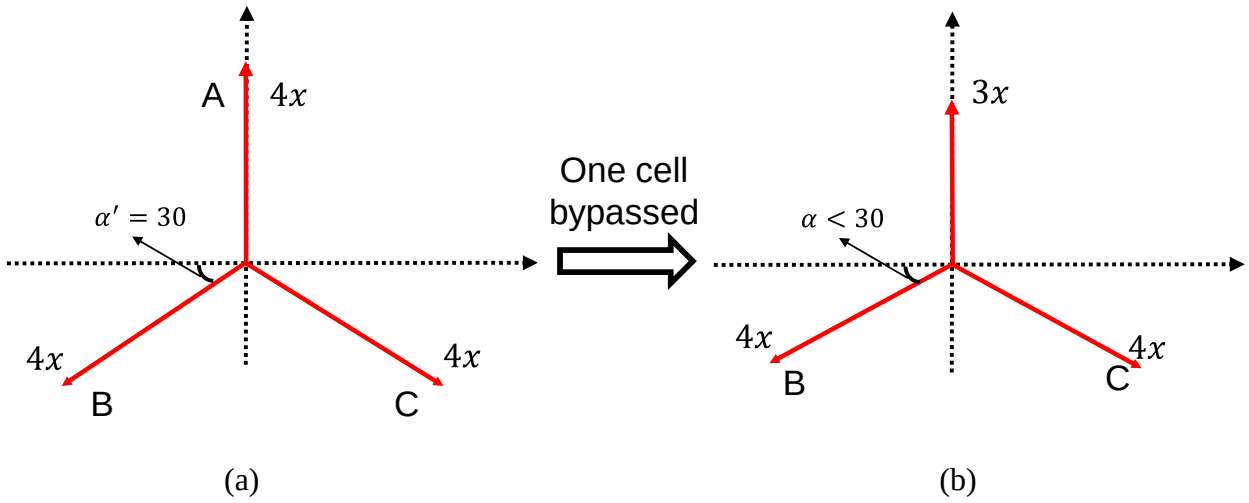


Figure 5.7 Phase voltages and their corresponding phase differences for a CHB converter with 4 cells per phase under (a) normal operating conditions and (b) with one failed cell.

5.7 Number of Components

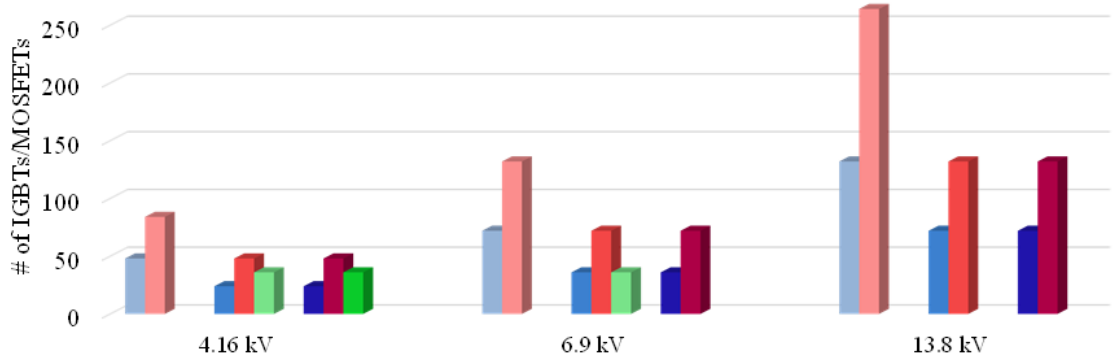
Inherent reliability of a converter system is a function of the number of component used in it. In other words, parts count is the most straightforward method to assess reliability in a system, given the associated higher probability of failure that results from a higher number of system components. A discussion on the reliability of different voltage rating Si or SiC semiconductors is beyond the scope of this study. However, for which the number of semiconductors will be used to compare reliability between the converters under investigation.

Among the converters designed and with respect to data from tables 5.3 to 5.6, the 5-L ANPC requires the least number of semiconductors. In both 4.16- and 6.9 kV voltage levels, this converter needs 12 IGBT/diode modules per phase (resulting in 36 total for three phases). However, this number for CHB at 4.16- and 6.9 kV is 48 and 72, and for MMC it is 84 and 132, respectively. At 13.8 kV a similar ratio exists among the number of switches for MMC and CHB. At this voltage level, MMC needs 264 IGBT/diode pairs, while for operation of CHB 132 pairs are enough. In other words, MMC converter at all voltage and power levels needs highest number of power switches. This is another main drawback of MMC converter, affecting its reliability. It is also clear that the number of gate drivers, communication fibers and etc. in the converters will be equal to number of their semiconductors, which adds more to reliability concerns of converters with high number of switches.

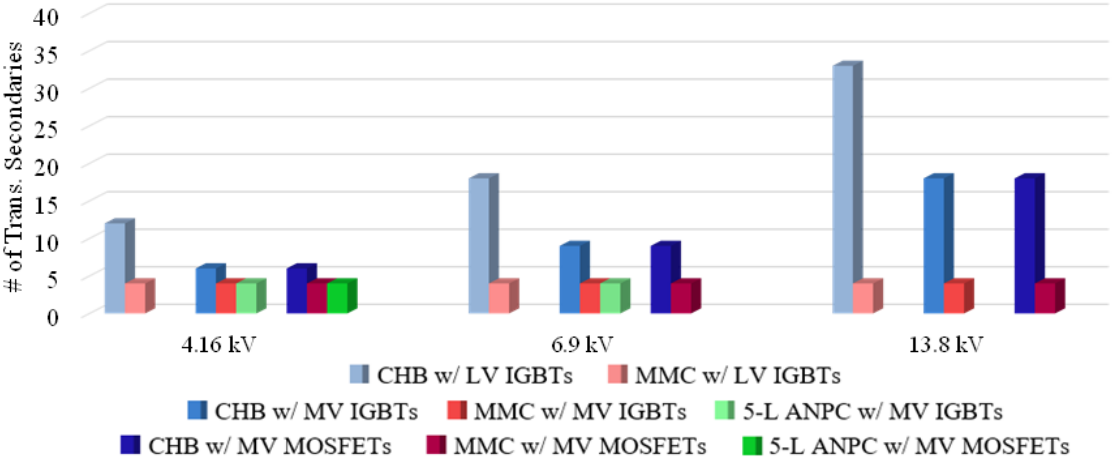
On the other hand since CHB converter needs separated dc link voltages, number of front-end rectifier diodes in it will be higher than that of MMC and 5-L ANPC. Number of diodes used in front-end rectifiers of CHB converter is simply 6 times the number of cells in converter. Thus, for

4.16-, 6.9- and 13.8 kV CHB converters designed in this dissertation, 72, 108 and 198 rectifier diodes are needed while at the same voltage levels for MMC and 5-L ANPC only 24 diodes are required.

Although presspack diodes (which are normally used for DFE stage of medium-voltage drives) are highly reliable and when failing, they are normally shorted (so they do not interfere operation of the converter, if additional diodes are placed in series when designing) but number of diodes is proportional to number of secondary windings in multi-pulse transformer used with



(a)



(b)

Figure 5.8 Number of (a) power semiconductors and (b) secondary windings needed for DFE stage in the designed converters.

drives. Number of transformer secondary windings in CHB converter is equal to the number of H-bridge cells used. Thus, CHB converter has a more complicated transformer. Number of power switches and transformer secondary windings needed for each converter are shown in figures 5.8(a) and 5.8(b), respectively.

As the voltage level increases, CHB requires more and more secondary windings and finally at 13.8 kV, it needs 33 secondary windings on transformer. Large number of secondary windings adds to the complexity of transformer design and implementation, potentially increasing its cost. Also, due to utilization of more insulating material within the converter structure, its size also increases. This is the main reason why some vendors such as Siemens use 3.3 kV Si IGBTs for very high voltage drive systems, resulting in cost reduction of the transformer. It is worth to note that for MMC and 5-L ANPC converters, a total of 4 secondary windings is enough for operation of the converter at any voltage and power level. This number of secondary windings is selected to satisfy IEEE 519 at the primary side without using any additional filters

5.8 Conclusions from Comparisons

So far comparisons were made between the target converters from different points of view. Based on the derived simulation models, inverter stage efficiency, capacitance requirement, semiconductor utilization, power density, low-speed operation capability, fault-tolerant operation and parts count were compared for different converters under study.

According to the results in 4.16-13.8 kV motor voltage range, regardless of the semiconductor technology used the CHB-based drives are almost always the most efficient solution. Considering huge amount of energy processed by the medium-voltage high-power motor drive converters, high

efficiency is a significant advantage that has already resulted in popularity of the cascaded H-bridge converter. The CHB converter also requires smallest die size installed within its structure compared to the other converter topologies. This will naturally result in less initial investment on semiconductors of this topology. From power density point of view, the CHB-based drives feature a moderate footprint among the investigated options. Also, they are tolerant to the faults that may occur within converter structure or communication/control units. However, the biggest disadvantage of the cascaded H-bridge converter is its transformer, which at higher voltages becomes increasingly costly and complicated to make.

MMC on the other hand normally features lower but close efficiency to CHB, while it requires only a single dc bus and in a consequence a simpler front-end diode rectifier. In a similar manner to CHB, MMC converter is also capable of fault-tolerant operation, and can continue to uninterruptedly operate in case of failure in a component inside of it. Lowest power density, largest number of switches installed in structure, large installed die size and problem at low speeds are the drawbacks of the MMC topology in medium-voltage drive application.

Last but not least, the ABB-patented 5-L ANPC converter showed to be a better solution in lower power applications featuring the smallest footprint and competitive efficiency compared to the other investigated converters. Also, the dc bus of this converter can be generated by a simple diode front-end stage, where typically a 24-pulse topology with 4 secondary windings is sufficient to meet input current harmonic distortion requirements without using additional filters. The major shortcomings of this topology are its large installed die size requirement, as well as lack of fault-tolerant operation capability. Also its efficiency faces significant drop as the rated power increases.

From semiconductor point of view, the 3.3 kV Si IGBTs showed to be less than an ideal solution for medium voltage applications, since their featured efficiency was considerably smaller in comparison to the 1.7 kV Si IGBTs. In fact, efficiency of the target converters using 3.3 kV Si IGBTs could be up to 1% smaller than that featured by using 1.7 kV Si IGBTs. Also, power density and semiconductor utilization of the converters were higher when using MV Si IGBTs. These are the main reasons why the commercial drives are mostly based on LV Si IGBTs. On the other hand, the SiC MOSFETs had a positive impact on semiconductor utilization of all converters regardless of voltage and power rating, which was attributed to better thermal conductivity, higher current density and smaller losses of SiC material compared to Si at the same die size. From efficiency point of view, the 5-L ANPC converter based on MV SiC MOSFETs would feature considerably higher efficiency compared to MV Si IGBTs. However, for a wide range of voltage and power, efficiency of MMC and CHB converters based on 3.3 kV SiC MOSFETs was smaller than that featured by 1.7 kV Si IGBTs. Smaller current rating used (due to better thermal conductivity) and higher switching frequency were the main reasons for this phenomenon. The degree of merit derived for power density also changed in a meaningful proportion to efficiency for all converters. The MV SiC MOSFETs featured higher power density for the 5-L ANPC topology, while in case of MMC and CHB, this effect was only visible at higher voltages.

Determination of the most appropriate topology and semiconductor type depends on the application in which the motor drive system is used. For instance, in ship propulsion or some factories power density dominates efficiency, due to restriction/high price of space. On the other hand, for a variety of environments higher efficiency is the most important factor. In this dissertation, detailed comparison results were shown from different aspects, so that one could

select the closest-to-ideal topology and semiconductor for target application. With that in mind, for general purpose applications and with possible commercialization of 3.3 kV SiC MOSFETs it is expected that the 5-L ANPC converter based on SiC MOSFETs becomes the choice of favor at lower voltages and powers in the investigated interval. This is mainly attributed to competitive efficiency and small footprint of this converter in the mentioned range. For a wide range of operating voltage and power, still the cascaded H-bridge converter based on LV Si IGBTs seems to be the best option, due to its highest efficiency, high power density and smallest die size installed.

Finally, at higher end of the investigated interval of motor voltage where the transformer of LV IGBT-based CHB converter becomes a significant impediment, medium voltage SiC MOSFETs can again be game changing. Using MV SiC MOSFETs in the CHB converter can

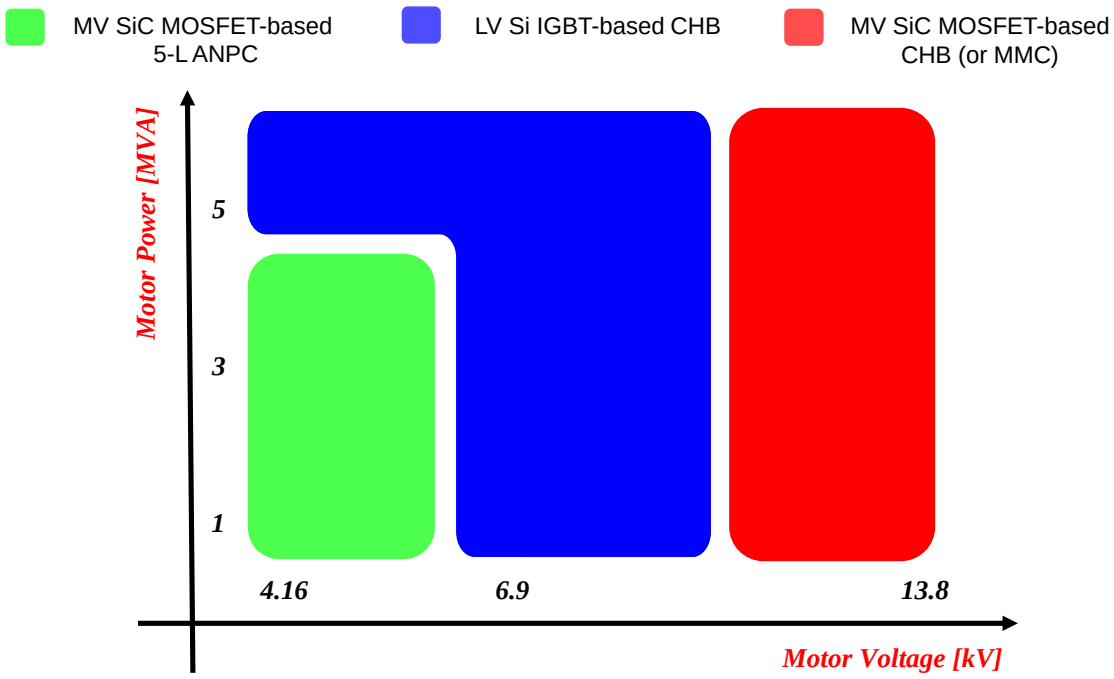


Figure 5.9 Predicted penetration range for SiC MOSFETs in medium-voltage high-power motor drive application.

reduce number of cells and transformer secondary windings in half, and increase efficiency compared to LV Si IGBTs. Depending on type of load, MMC converter based on SiC MOSFETs can also be used at this range, featuring higher efficiency and still simpler transformer than that of CHB converter. Figure 5.9 demonstrates the predicted penetration range for SiC MOSFETs based on characterization results of available semiconductors as of 2017.

5.9 Summary

In this chapter detailed comparison results were shown between the converters under study using Si IGBTs and SiC MOSFETs. The comparison was done taking into consideration aspects like efficiency, power density, semiconductor utilization, energy stored in the capacitors, fault-tolerant operation capability, low-frequency operation and number of components (for a measure of reliability). The comparison tried to compare converters together and also semiconductor technologies together. Based on the performed comparisons, it was concluded that the 5-L ANPC made with SiC MOSFETs converter will be a suitable option for lower voltages and powers in the investigated range. Also, it was shown that for a wide range of voltage and power still the popular CHB converter based on traditional Si IGBTs will feature the best performance. Last but not least, it was concluded that for higher end of the voltage range studied, where the transformer of the CHB converter costs too much, the SiC MOSFETs can be game changing and the CHB converter based on SiC MOSFETs can be the best option from efficiency point of view. It is worth to note that the shown conclusion is for general purpose applications and in some cases like ship propulsion, special consideration like power density or weight can dominate other factors.

Chapter 6. Experimental Validation of the Performed Simulations

The comparison results demonstrated so far were all achieved in simulation environment. In order to provide proof of validation for the simulations, and also considering the fact that the converters under study are not feasible using laboratory equipment, an H-bridge cell is made using 3.3 kV 400 A SiC MOSFETs to bring proof for the converter design and thermal calculations. This chapter shows the H-bridge cell design stage, the achieved results and also the uncertainties existing with the performed modeling/calculations.

6.1 H-bridge Cell Implementation

Figure 6.1 shows the H-bridge cell prepared for experiments. The cell is based on 3.3 kV 400 A SiC MOSFETs discussed throughout the study, and it is made by modifying the double-pulse test setup of figure 2.24. Total of four bulk capacitors, 250 µF 1300 V each, are connected via busbars to support the dc link. Two capacitors are connected in series for satisfaction of voltage rating, and two capacitor branches are paralleled to increase capacitance/reduce ESL. Also resistors are connected in parallel with the capacitors to ensure proper voltage sharing/reduce discharging time at turn-off of setup.

All the connections are made using superconductor capacitor sheets with 60 mils thickness. For decoupling purposes, a total of three 100 nF 3 kVDC film capacitors are connected across the

terminals of the MOSFETs. The gate drives used for the MOSFETs are developed specifically for driving the target SiC MOSFETs and details of design process were shown in chapter 2.

A 3.3 kV 1200 A Si IGBT is connected in series with the H-bridge cell in order to increase safety of operation. Although the gate drivers have DESAT protection capability, the IGBT is tuned (by modifying its gate driving voltage) to saturate the current to around 100 A and cut it (by means of DESAT protection) at around 50 A. The saturation current is set to be higher than the cut-off current so that in case of failure the dc bus current does not increase drastically before the slow-switching IGBT cuts it.

The Si IGBT as well as the SiC MOSFETs are sitting on heat sinks, whose thermal resistance to the ambient air is measured to be 0.174 ˚C/W with air flow in presence of external fans. Note that in order to cool down the bleeding resistors and the power supplies/components in the system,

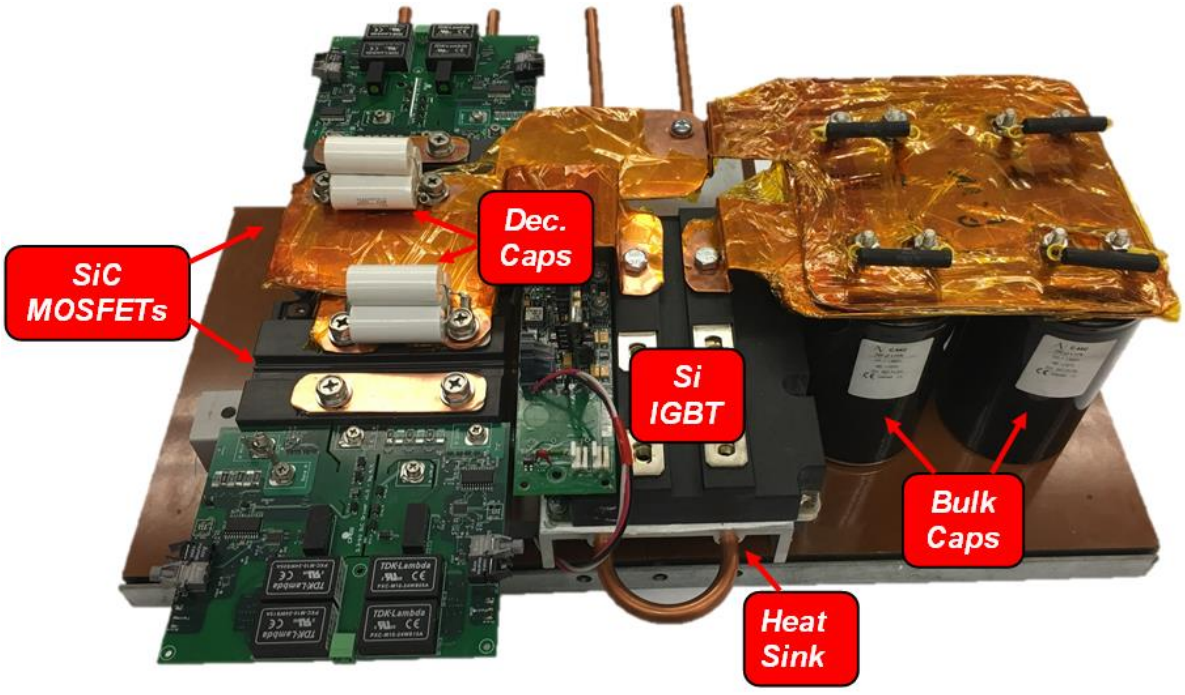


Figure 6.1 Prepared H-bridge cell for experimentally validating the converter modeling and thermal calculations performed throughout the dissertation.

some fans are placed in its vicinity. Thermal resistance of the heat sink is measured in the shown setup, by adding scientific ceramic heaters with part number HS-PS505020. Thickness of the ceramic heaters is 2 mm and four of them are mounted on the heat sink under each SiC MOSFET.

By applying a measured power to the heaters, variation in heat sink temperature is measured and the thermal resistance of the heat sink to ambient air is calculated. It is worth to note that since the heat sink is mostly covered by the devices and their corresponding gate drivers, the thermal resistance value specified in datasheet could not be used for it and thus, measurements are performed.

Other than the heat sink thermal resistance, switching losses of the devices are also measured for thermal calculations. It is well addressed in [69] that change in power loop inductance can cause considerable changes to switching losses of fast-switching SiC MOSFETs. Since in the setup shown in figure 6.1 an IGBT is connected in series with the H-bridge cell (adding ~90 nH to the power loop inductance) the switching losses reported in [63] cannot be used for loss calculation. Thus, the double-pulse test procedure explained in [63] is repeated on the shown setup to measure switching losses of the SiC MOSFETs. Note that at lower currents (where the H-bridge cell is operating at) the measured losses from H-bridge cell and the double-pulse tests in chapter 2 were close, since the switching energy at lower currents is mostly provided by the decoupling capacitors and has less dependency on the stray inductances of the bus.

The dc voltage across the capacitors is measured by means of a bench-top multimeter and the output ac voltage is measured by P5210 differential probe. On the other hand, the load current is measured by means of a TCP0030A current probe with 30 A maximum current rating.

Table 6.1 Parameters of the implemented H-bridge cell.

Parameter	Symbol	Magnitude
dc bus voltage	V_{DC}	*2 kV*
Modulation index	M	*0.9*
Output frequency	f	*60 Hz*
Carrier frequency	f_{cr}	*4 kHz*
Load power factor	PF	*0.9*
Load active power	P	*7 kW*

The main parameters of the H-bridge cell are shown in table 6.1. According to the table, the input dc voltage is set to 2 kV and it is being provided by means of a 3 kV 100 kW Magna power supply. The load is composed of resistors and inductors in series, featuring 0.9 power factor. Load active power is 7 kW and switching frequency of the SiC MOSFETs is set to 4 kHz. It is worth to note that in the experiments, the switching frequency is set to a higher value than the investigated motor drive topologies to feature a reasonable power quality at output of a single H-bridge cell. Also, the limit on active power is posed by the resistive load bank. The phase-shifted pulse-width modulation (PSPWM) is used for modulation of the H-bridge cell.

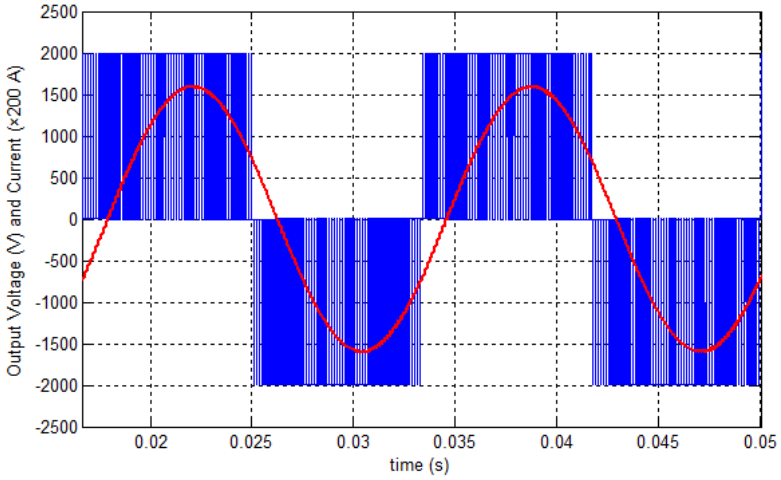
6.2 Test Results Using the H-bridge Cell

6.2.1 Proof of Converter Modeling

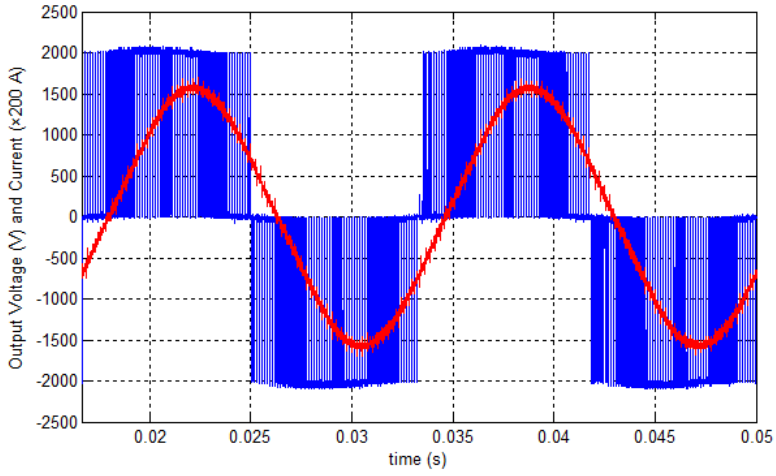
The output waveforms of the H-bridge cell resulting from simulations and experiments are shown in figures 6.2(a) and 6.2(b), respectively. In a similar manner to the simulations, the switching times and deadtimes are applied to the device model. Also the leakage parameters connecting different parts of the system (including ESL of the busbars and stray impedance of the cables from H-brdige cell to the load) are all measured and included in the simulation model.

Figures 6.3(a) and (b) demonstrates the output voltage waveform harmonic spectrum, where it can be seen that the simulations are well capable of predicting the experimental results.

According to figure 6.3, both magnitude and total harmonic distortion (THD) of the output voltage resulting from simulations are close approximation of those from the experiments. In both simulation and experiment results, the first set of major harmonics to appear are sidebands around 8 kHz (2×4 kHz carrier frequency) as expected from PSPWM modulation on H-bridge cells. It is

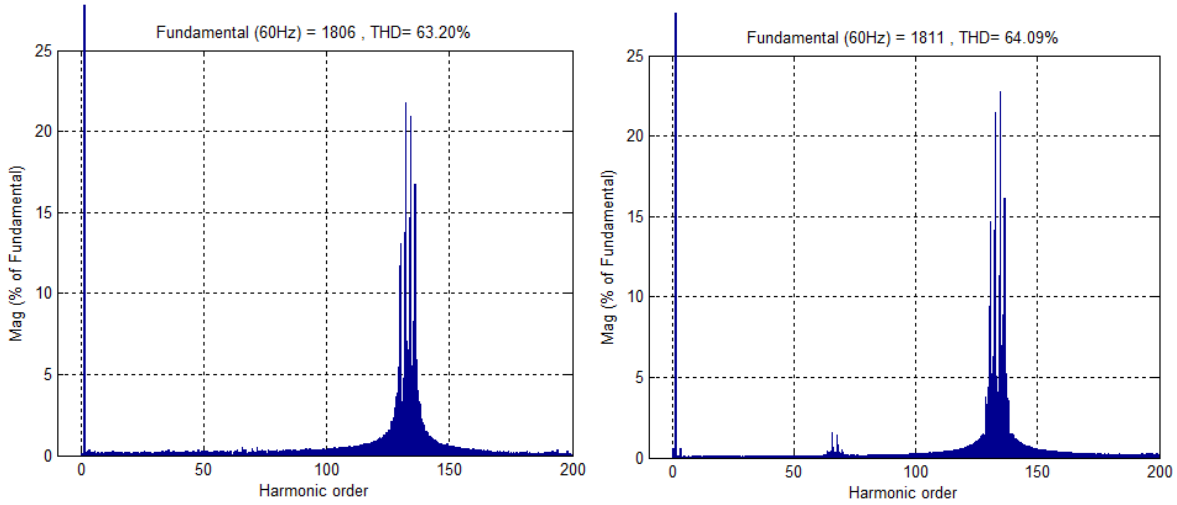


(a)



(b)

Figure 6.2 (a) simulated and (b) experimental results captured from the H-bridge cell at 2 kV dc bus voltage and 7 kW active power at 0.9 power factor.



(a) (b)

Figure 6.3 THD for (a) simulated and (b) experimental ac voltage at the H-bridge cell.

worth to mention that in the experimental results there are harmonics as sidebands around carrier frequency (4 kHz) with magnitude less than 1.4% of fundamental. These harmonics are existing due to several factors such as non-perfect deadtime compensation, switching noise being propagated on the measurement probes and etc.

6.2.2 Proof of Thermal Calculations

Figure 6.4 is showing the heat sink temperature captured by thermal camera, once the H-bridge was running for long enough time and the heat sink temperature had reached its steady-state value. According to the thermal camera, temperate on the heat sink is around 35.1-35.5˚C, while the ambient air temperature is measured be ~21˚C. On the other hand, the calculated losses for each module inside the H-bridge cell was about of 39.5 W.

According to (6.1) and considering the measured heat sink thermal resistance to the ambient air (0.174 ˚C/W), the calculated heat sink temperature would approximately be 34.5 ˚C.

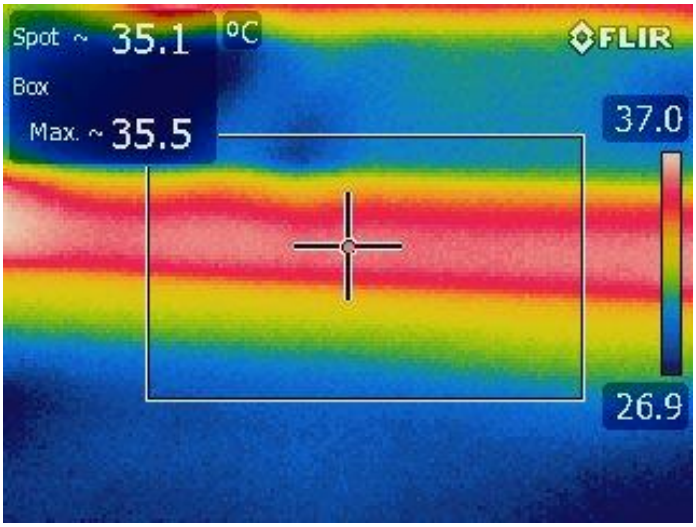


Figure 6.4 Temperature measured from the heat sink under SiC MOSFETs.

$$T_{HS} = T_{amb} + P_{loss}.R_{th,H-A} \tag{6.1}$$

where $R_{th,H-A}$ is the measured thermal resistance from the heat sink to the ambient air. The reported experiments are conducted on a single H-bridge cell with scaled-down power level (considering power restrictions in a research lab environment). However, validity of converter modeling in MATLAB environment as well as the conducted thermal calculations can be generalized to large scale converters.

6.3 Assumptions Capable of Introducing Error to the Study

So far the converters are designed using simulations in MATLAB environment and comparisons are made based on them. Although the performed experiments proved validity of converter modeling and thermal calculations in MATLAB environment, there are assumptions made in the study that can slightly impact the results achieved from simulations and introduce uncertainty to the designs/comparisons. In the following subsections, the most important factors will be discussed.

6.3.1 Different Commutation Loops in the Converters

The losses calculated from the power semiconductors are composed of conduction and switching losses. The conduction losses of the semiconductors depend on their static characteristics (e.g. R_{DSon}) and do not change with converter configuration. However, the switching losses are a function of the commutation loop and are subject to change with change in converter configuration [69].

As shown in chapter 2, the performed switching loss calculations on the 3.3 kV 400 A SiC MOSFETs under study relies on double-pulse test results in half-bridge configuration of semiconductors. Moreover, as mentioned before in chapter 5 in case of Si IGBTs the conduction and switching losses are calculated based on data from datasheets. Usually, datasheets of semiconductors also give the switching losses in half-bridge chopper cell configuration.

The commutation loops within the CHB and MMC converters are similar to that of the circuit used for double-pulse tests. However, for the 5-L ANPC converter shown in section 3.3 the commutation loop of semiconductors are different than a half-bridge phase leg, which will cause changes to their switching losses in comparison to the double-pulse test results.

The effect of commutation loop inductances on switching losses are more significant on SiC MOSFETs due to their faster switching speeds. In this dissertation due to unavailability of enough 3.3 kV 400 A SiC MOSFET samples, the double pulse tests are not repeated in the 5-L ANPC converter configuration and instead, the switching losses calculated from half-bridge circuit are used for calculation of switching losses for the 5-L ANPC converter. Depending on manufacturing

quality and the parasitic inductances of the busbars within structure of the 5-L ANPC converter, this assumption will impact the losses and efficiency calculated for the 5-L ANPC topology.

6.3.2 A Single Heat Sinks Used for Calculation of Converter Volume

In section 5.4, volume of the converters are compared to each other considering the finished size of power semiconductors, heat sinks, fans, capacitors and inductors (inductors are used in structure of the MMC converter only). In this comparison, the capacitor banks of each converter are designed using the best combination of FFLI film capacitors from AVX. Also the inductors of the MMC converter are designed using the smallest possible AMCC cores.

On the other hand, in order to estimate the total volume of heat sinks used in structure of each converter, the study was done considering a single heat sink's specifications. In this way, for semiconductors inside each converter the volume of the selected heat sink was scaled to feature the desired temperature on it (which was set to 80˚C) and the resulting volume was used for comparison purposes. Note that volume of fans needed for the converters was calculated in a similar fashion.

Although the used approach gives an estimation of the heat sink volume installed in each converter, it is prone to uncertainties. According to information from drive manufacturers as well as the datasheets of commercial motor drive converters, the heat sinks used for each topology will depend on different factors including type of semiconductors used (module or discrete), converter packaging and etc. Accordingly, the type and finished volume of the heat sinks as well as the associated fans will be prone to change.

6.3.3 Impact of Creepage and Clearance Distances between Components on Converter Volume

The calculated converter volume in section 6.4 considers all of the major components used in their structure. However, the calculation does not reflect impact of the creepage and clearance distances that are necessary between different components inside the converters.

It is clear that conductor parts within structure of the multilevel converters will be sitting on different potentials. This makes it necessary to consider appropriate creepage and clearance distances between the components within converter structure. Accordingly, the converters with more number of components will have more increase in their size/volume.

Since the MMC converter has larger number of components compared to CHB and 5-L ANPC, it is expected that the finished volume of it will experience further increase compared to the other topologies. On the other hand, the 5-L ANPC converter has the least number of components in its structure and thus, it will have least increase in its volume due to creepage and clearance distances. Accordingly, it is expected that when comparing the finished volume, the order of converters will not change (the MMC will still feature the highest volume while the 5-L ANPC will benefit from highest power density) but the finished volume for each of them will be higher than numbers shown in figure 5.5.

6.3.4 Constant Switching Losses Assumed for SiC MOSFETs versus Current Rating

Section 5.4 discussed that in order to have a fair comparison between different types of semiconductors (Si IGBTs and SiC MOSFETs), it is of critical importance to choose the smallest current rating device of each type for a given converter. For this purpose, the electro-thermal

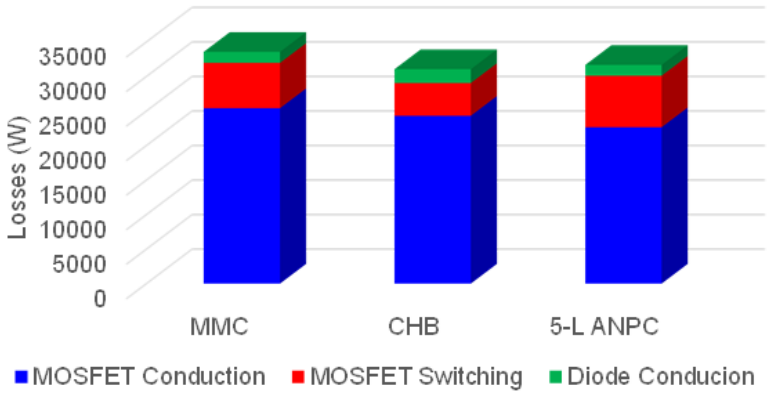


Figure 6.5 Breakdown of converter losses for 4.16 kV 3 MVA case using 3.3 kV SiC MOSFETs.

properties of the Si IGBTs were interpolated among the abundant commercial options available. However, in case of SiC MOSFETs this could not be done as all three available samples were rated at 400 A.

The assumption made on constant switching losses of SiC MOSFETs as the current rating of the device changes can introduce slight error to the calculated losses. However, the amount of error introduced by this assumption is expected to be negligible. It was shown in figure 4.4 that once current rating of a Si IGBT increases by 500%, the switching losses experience about 65% increase. Also Figure 4.6 showed that for two SiC MOSFETs that have the same structure but different current rating, 350% increase in current rating creates about 60% difference for them in terms of switching losses.

On the other hand, figure 6.5 shows that for the designed converters at 4.16 kV 3 MVA using SiC MOSFETs, the switching losses compose less than 23% of the total converter losses (where the highest percentage for switching losses happens in case of the 5-L ANPC converter due to its high switching frequency. Also, higher-voltage cases have smaller ratio of switching losses to the total losses). Also, according to table 4.6 the current rating of SiC MOSFETs used for the 5-L

ANPC converter at 4.16 kV 3 MVA is scaled down to 330 A. Assuming a similar (and linear) variation in switching losses of the 3.3 kV SiC MOSFETs as that of the 900 V devices discussed in figure 4.6, the total error introduced to switching losses will be less than 2%.

6.4 Summary

This chapter provided experimental proof for the performed converter modeling and thermal calculations. Since the converters under study are not feasible in laboratory environment, an H-bridge cell (as building block of the CHB converter) is made and tested at the maximum possible power rating. Then, the test results were used to investigate validity of converter modeling and thermal calculations. According to the presented results, the MATLAB simulations are well capable of predicting converter's output spectrum as well as the semiconductor losses. Last but not least, this chapter discussed the most important possible causes of error to the performed simulations/comparisons.

Chapter 7. Stacking 1.7 kV SiC MOSFETs in Series to Achieve 3.3 kV Switches

As mentioned in Chapter 1, the SiC MOSFETs are not commercially available beyond 1.7 kV. Stacking lower-voltage SiC MOSFETs is an effective way of achieving higher voltage SiC MOSFETs to take advantage of their outstanding features at higher voltages. However, the main problem to do so is voltage sharing between the series-connected MOSFETs. Chapter 1 discussed the two reasons that are widely believed to cause voltage imbalance between series-connected semiconductors. This includes mismatch in gate signals as well as mismatch between device characteristics.

In this chapter, the main reason responsible for unequal voltage sharing among series-connected power semiconductors is shown. Also, a novel method is proposed to balance the voltages across them without adding considerable amount of losses to the devices and the gate driver system. The proposed method is validated via simulations and experiments, and a gate driver is designed for 1.7 kV 550 A SiC MOSFETs of GE embedding the proposed method together with a closed-loop control method for its operation.

7.1 Unequal Voltage Sharing Among Stacked Semiconductors

The most important factor contributing to unequal dynamic voltage sharing among series-connected devices is the parasitic capacitances from gates to ground, and was first addressed in [135]. According to figure 7.1 where a 3.3 kV switch is composed of two SiC MOSFETs

connected in series, there is a specific capacitance from gate of each semiconductor to the ground. This capacitance is composed of parasitic capacitance of power supply used for gate driver, as well as the parasitic capacitance inside the module package from gates to the baseplate, where the baseplate is usually grounded (if the stacked devices were inside a module).

If well-matched devices and gate drivers used, during the turn-off process equal currents will flow to gate drivers ($i_{d1}=i_{d2}$). However, due to positive *dv/dt* at gates (since the gates are well coupled to sources for both dc and high-frequency components), a secondary gate current will flow from gates to ground. According to figure 7.1, since *dv/dt* at gate of the top MOSFET is larger than that of the bottom one, i_{c2} will be larger than i_{c1}. At turn-off of the device, these currents are

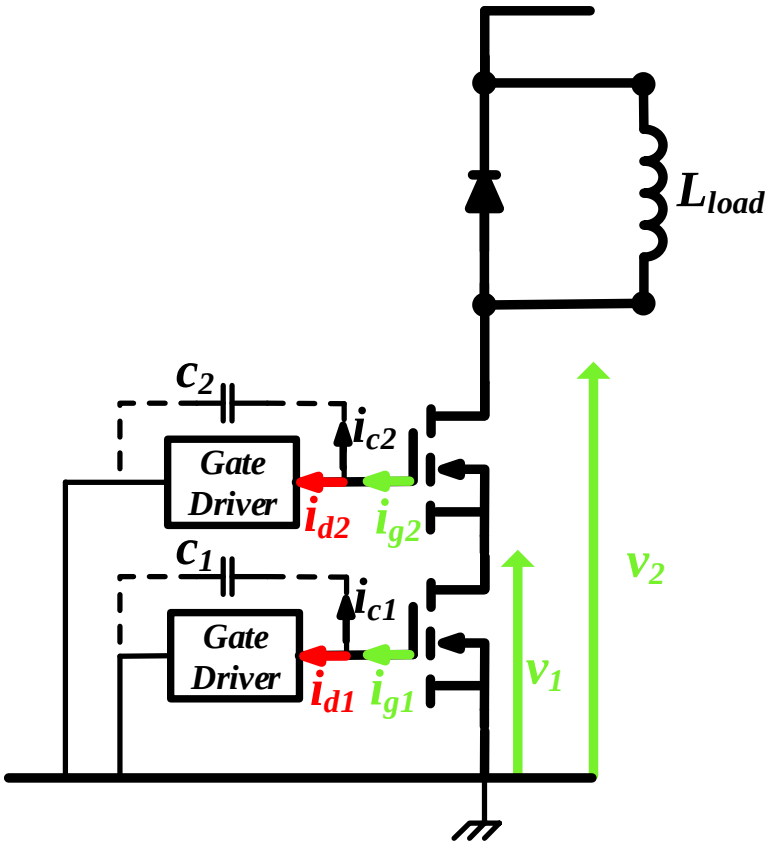


Figure 7.1 Series-connected SiC MOSFETs in a chopper circuit.

derived from gates in addition to the current derived by the gate driver. This means that the total gate current for the top MOSFET at turn-off will be larger than the bottom one ($i_{g2}>i_{g1}$), resulting in faster turn-off for it. Faster turn-off switching will result in higher share of the total dc voltage for top MOSFET. This mechanism can be generalized to any number of semiconductors stacked in series.

7.2 Natural Voltage Sharing between Two Stacked SiC MOSFETs

In this section, tests are done on a stack of SiC MOSFETs in order to see the natural voltage sharing among them. The non-commercial 1.7 kV SiC MOSFET from General Electric (GE) is under study in this chapter [136] for stacking and realization of higher-voltage devices. Figure 7.2 shows the MOSFETs where a GE-developed gate driver is mounted on it.

In order to investigate the natural behavior of the device under test when connected in stacked mode, a setup is prepared in this section and tests are done in order to see the natural static and dynamic voltage sharing without using snubbers. The setup is similar in principles to the one made in previous section, except that two MOSFETs inside a module are used as bottom switch, and

Figure 7.2 The 1.7 kV SiC MOSFET module from GE used for stacking purpose [136].

body diodes of two other MOSFETs inside another module are used as the top switch. The test setup is shown in figure 7.3.

The DUT is being driven by a GE gate driver. Due to lack of enough gate drivers at the time this test was being conducted, the switches inside the top module are kept off by applying a constant -5 V via two isolated dc-dc power supplies with enough isolation voltage. The decoupling capacitor is changed, and a 330 nF capacitors is used since in the new setup the power loop inductance is larger.

The DC bus voltage is set to 1000 V. This is to prevent any possible failure in case of worst case voltage sharing among two stacked devices under test. Figure 7.4 shows the static voltage sharing among MOSFETs where there is around 55 V difference between two MOSFETs. This

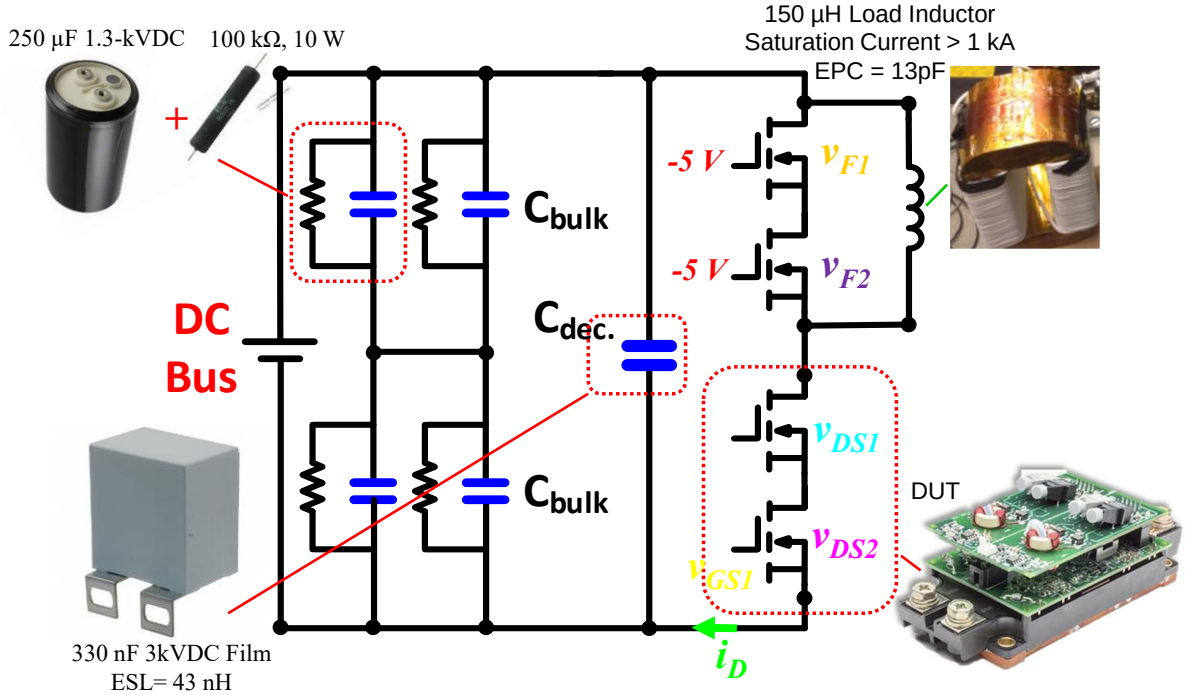


Figure 7.3 Schematics of the DPT setup for stacked SiC MOSFETs.

difference in mainly coming from different capacitances of the devices, as the static voltage sharing among series-connected devices is a capacitive voltage sharing.

On the other hand, right after switching instant (turn-off) the dynamic voltage sharing is measured which shows significantly larger difference in voltage across the two devices under test compared to static case. Figure 7.5 shows the dynamic voltage sharing where there is approximately 188 V difference in voltage of top and bottom devices. For the reasons explained in previous sections, the top MOSFET always gets higher voltage than the bottom one.

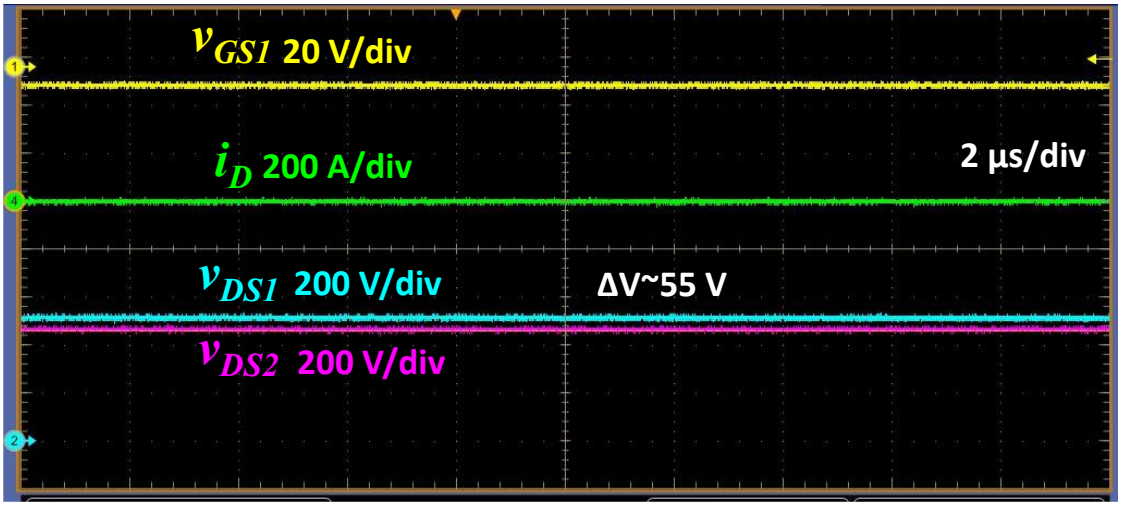


Figure 7.4 Natural static voltage sharing among two 1.7 kV SiC MOSFETs connected in series.

It is worth to note that the gate resistances used for this set of tests in stacked mode are 5 Ω (for both turn-off and turn-on). Although this gate resistance seems to be too large for the SiC MOSFETs under study, but as it can be seen from figure 7.5 the ringing at device turn-off is still too large due to existence of large loop inductances. This is inevitable when connecting several semiconductors in series, adding up their parasitic components. Based on the switching parameters shown in figure 7.6, the commutation loop inductance is estimated to be around 88 nH for the setup shown in figure 7.3.

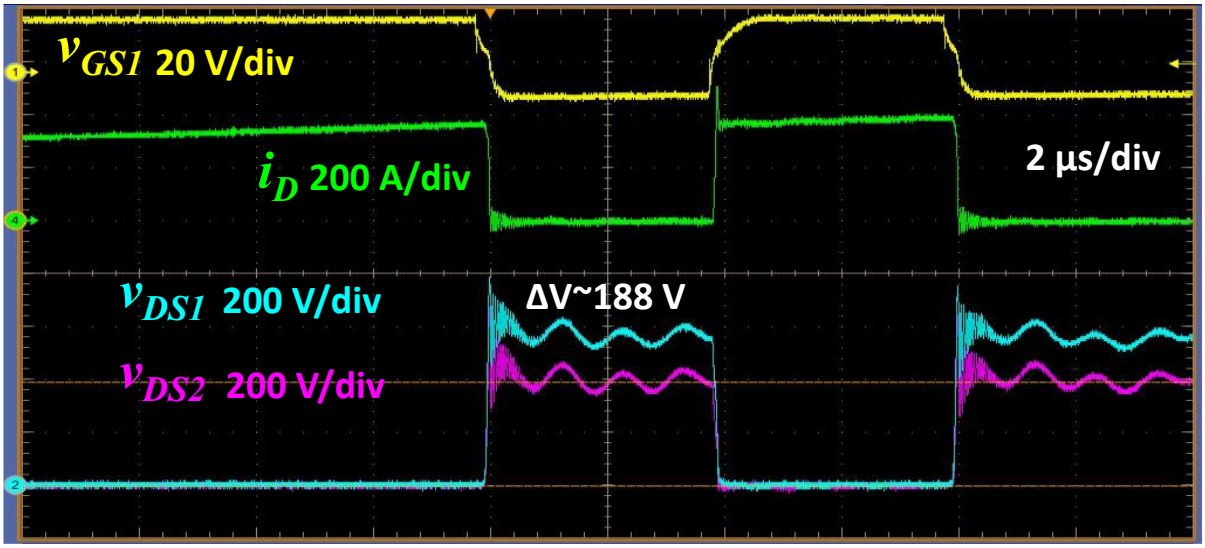
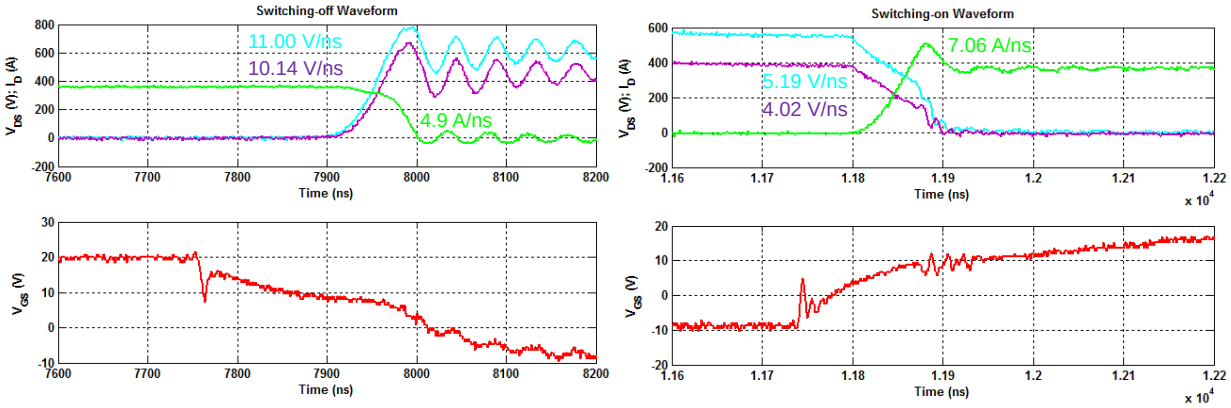


Figure 7.5 Natural dynamic voltage sharing among two 1.7 kV SiC MOSFETs connected in series.



(a) (b)

Figure 7.6 (a) Swithing-off and (b) Switching-on waveforms of the stacked switches.

7.3 Proposed Voltage Balancing Method

This section shows the fundamentals of the proposed solution for voltage balancing among stacked SiC MOSFETs, as well as the closed-loop realization on a gate driver.

7.3.1 Proposed Active dv/dt Control for Voltage Balancing among Stacked SiC MOSFETs

According to section 7.1, the main cause of unequal voltage sharing among stacked power semiconductors is the parasitic capacitance from gates of the devices to the ground. At turn-off of the devices where there is positive dv/dt across the gates, this capacitance conducts some current to ground which has to be derived from the gate. Since the amount of current derived from gates are not similar (due to different dv/dt rates at gates), the switching-off speed and consequently the final value for the voltage across devices are different.

In this section a novel method is proposed for balancing voltages across stacked semiconductors. The proposed method tries to compensate for the additional gate current due to existence of the parasitic gate-to-ground capacitors, so that equal voltage sharing can be achieved.

According to figure 7.7, at turn-off event of the main device an auxiliary current is derived by means of a small capacitor C_M and thanks to the well-known Miller effect. Once the Miller current is derived, the aim is to direct part of it to gate of the SiC MOSFET to slow it down and compensate for the current through parasitic capacitors (i_{c2} in figure 7.7). it is worth to note that the bottom MOSFET's switching speed is set merely by its gate resistance, and thus there is no need to use an auxiliary circuit on it to modify its switching speed. This is due to nearly zero dv/dt at its gate at turn-off event.

The current division is realized by means of four identical bipolar junction transistors (BJTs). By modifying v_{CTRL}, the gate voltage of Q_1 in figure 7.7, i_c is shared between Q_1 and Q_2. If v_{CTRL} is set to zero, Q_2 will conduct all of i_c. On the other hand, if Q_1 is completely switched on by providing 1 pu of V_{CTRL}, the Miller current will be shared between Q_1 and Q_2.

Q_3 and Q_4 on the other hand form a current mirror, where Q_4 copies the current conducted by Q_3. Since Q_1 and Q_3 are connected in series, this means that the amount of current flowing to gate of the main MOSFET will be i_2-i_1. If V_{CTRL} is set to zero, the auxiliary gate current i_G' in figure 7.7 will be equal to i_c, resulting in slowest switching speed for the main MOSFET. However, if V_{CTRL}

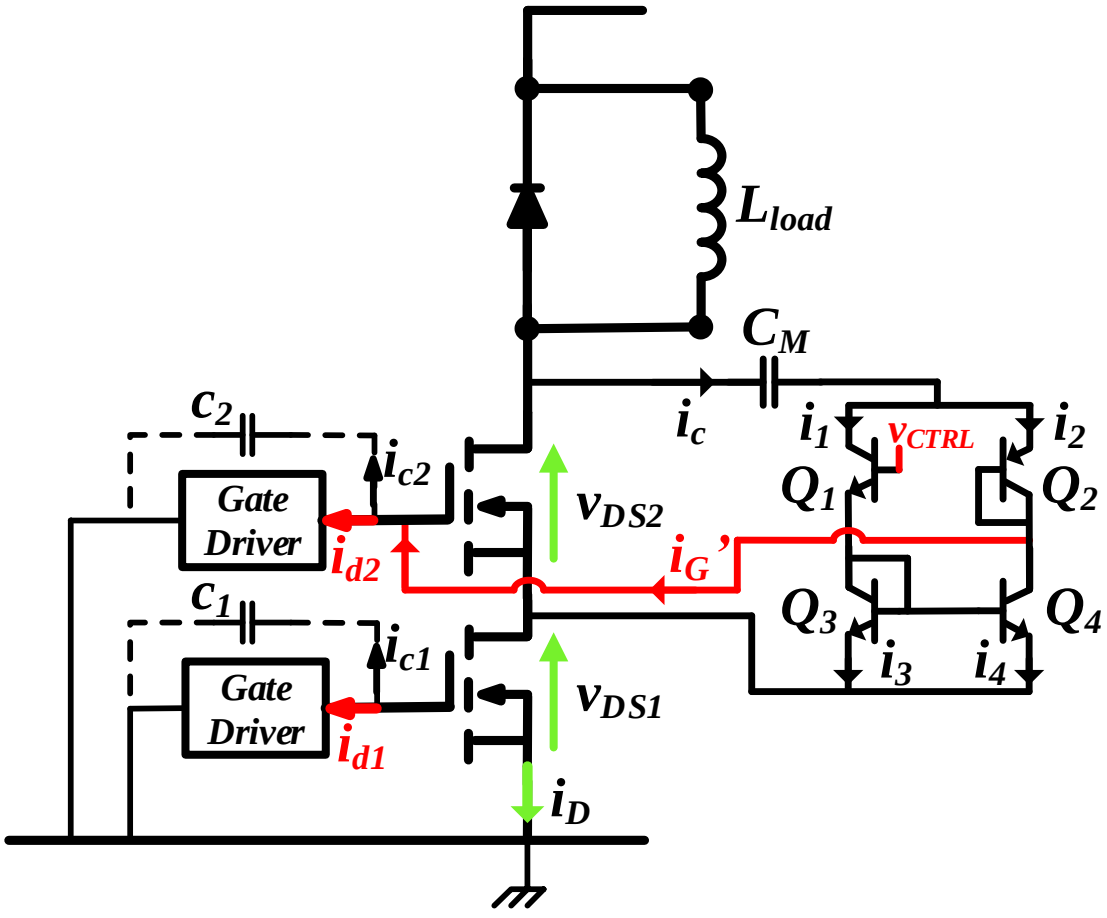


Figure 7.7 Proposed active dv/dt control method for balancing voltages across stacked SiC MOSFETs.

is set to 1 pu, i_G' will be equal to zero, resulting in fastest (around original) switching speed of the main SiC MOSFET.

Since the top MOSFETs always get higher share of the total dc bus voltage by the parasitic gate capacitances via their higher *dv/dt* at their gate, slowing down the higher-order devices by this method can result in equal voltage sharing among them. It is worth to note that higher voltage for higher-order devices in stacks composed of more than two SiC MOSFETs can be seen from results of [33], [35], [39].

Magnitude of the Miller capacitor C_M depends on gain of the BJTs as well as the switching speed in main MOSFETs. For a given system and depending on the magnitude of auxiliary gate current i_G' needed, the Miller capacitor can be sized. Also, BJTs should be sized to prevent saturation. In theory, the proposed method can be used for any number of SiC MOSFETs connected in series.

7.3.2 Closed-Loop Realization of the Proposed Method

Figure 7.8 demonstrates the overall schematics for the gate driver embedding the closed-loop controller targeted for the stacked SiC MOSFETs in this project. Note that an analog realization of the closed-loop controller is targeted based on the requirements from the sponsor.

According to figure 7.8, each channel of the gate driver is composed of a driver IC that received the PWM signal and switches the MOSFET in accordance to that. The selected driver IC is IXDD630 of IXYS. The PWM signal is received on the gate driver board by means of fiber optic receivers, and in order to remove the possible high-frequency noise from it, an optocoupler with part number ISO7221 is used between the fiber optic receiver and the driver IC.

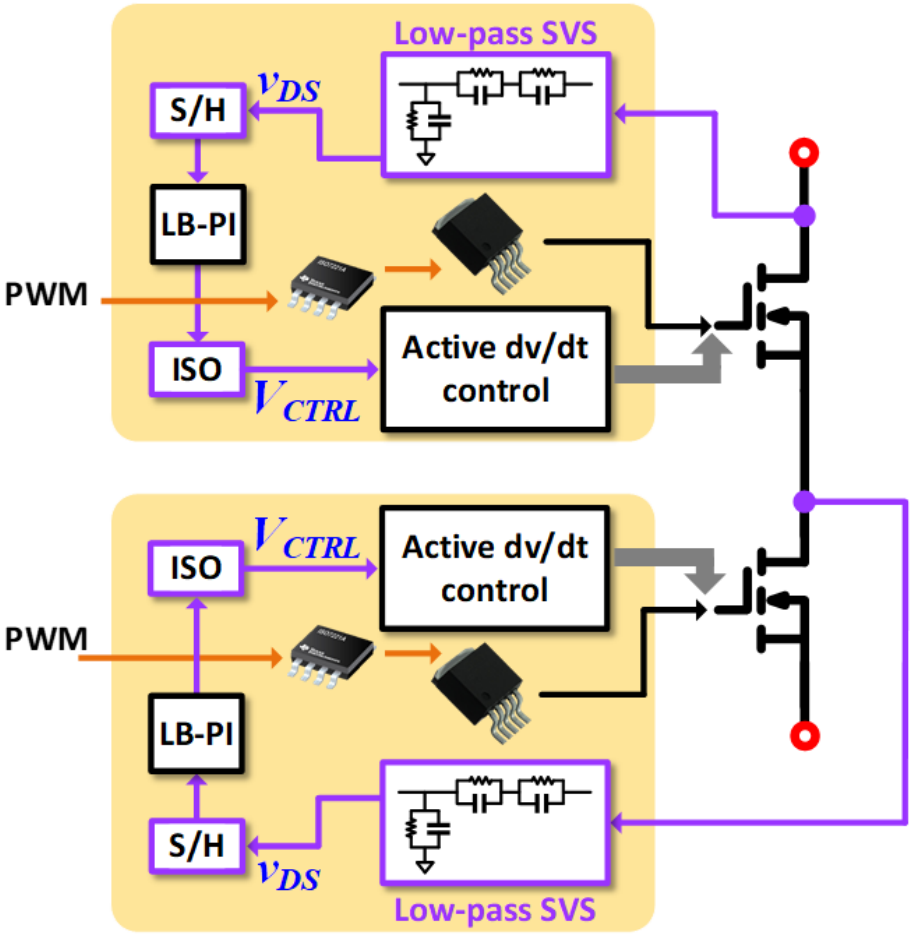


Figure 7.8 Proposed schematics for the gate driver embedding the active dv/dt control scheme.

The necessary protections for the designed gate driver seem to be the overcurrent protection as well as Miller clamping. As mentioned before in chapter 2, it is well addressed in literature that the DESAT overcurrent protection is not as effective on SiC MOSFETs as it is on Si IGBTs [78]. Also, in case of stacked power semiconductors if the protection on one device works while the others are not triggered (due to mismatch in DESAT controller performance), the whole stack will be in danger of failure. Thus, for overcurrent protection it is assumed that an external circuit will detect the phase leg current, and a corresponding signal will be provided to the gate driver to demonstrate overcurrent fault. There is a second fiber optic receiver on each channel which

receives an active-low signal for EN (enable) pin of the IXDD driver IC. If the external current detector (which can be a simple comparator IC with input from a rogowski current sensor and output to fiber optic transmitters) detects overcurrent, all of the devices in the stack will receive turn-off signal simultaneously. Also, the active-low nature of the EN signal for the driver IC makes it easy to bypass the overcurrent protection and run the system with no input to the corresponding fiber optic receiver.

Another protection embedded on the designed gate driver is Miller clamping. The Miller effect in half-bridge configuration of power semiconductors was explained in chapter 2. In order to guarantee safe operation of the stacked switches in half-bridge configuration, a Miller clamping mechanism as shown in figure 7.9 is used on the gate driver. In this circuit, a NAND IC is used to inverse the gate signal and provide the base signal of a current-sinking BJT (with part number ZXGD3006 inside soc23 package). By using an RCD network, the turn-off of the base signal is synchronized with turn-on of the main MOSFET (in order not to interrupt device turn-on). However, the turn-on signal of the BJT base is slightly delayed compared to turn-off signal of the

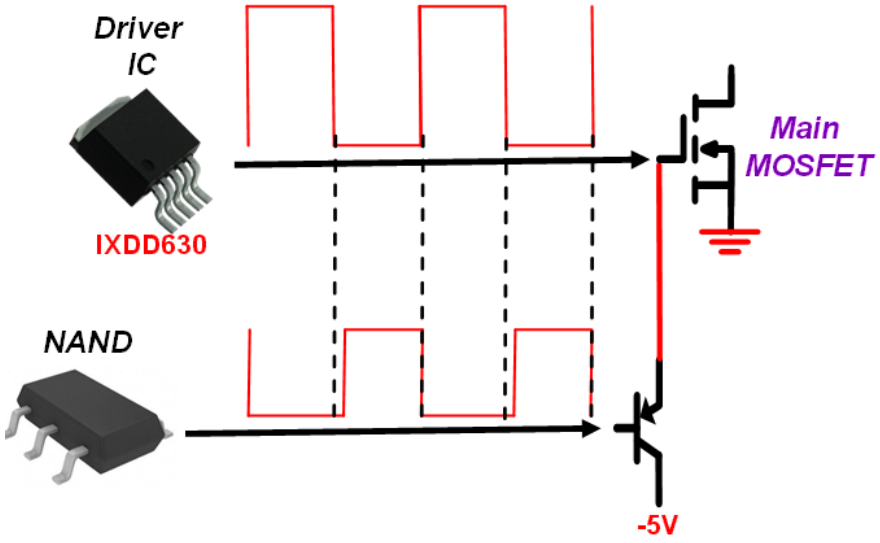


Figure 7.9 The Miller clamping mechanism of the designed gate driver.

main MOSFET. This is done in order to start the Miller clamping effect with enough delay to ensure turn-off of the main MOSFET (in a similar way, to ensure the Miller clamping circuit will not slow-down main MOSFET's turn-off). The PNP BJT clamps the gate of the main MOSFET to the negative gate driving rain (-4 or -5 V).

Each channel on the gate driver has a low-pass switch voltage sensor (SVS) for voltage measurement. In other words, measurement of the drain-source voltage for each MOSFET is being done on its corresponding gate driver. The schematics of the SVS is shown in figure 7.10, where the sensor is composed of series-connected RC branches. In the shown schematics, the values for series-connected resistors blocking the high voltage (Rs) and the resistor for measurement point (Rm) is selected to feature the desired gain. In the current design, the featured gain for V_{DS} measurement is about 1/300, resulting in 5 V measured voltage for 1500 V across drain-source.

On the other hand, the value of the measurement point capacitor (Cm) is selected to buffer the measured value and remove its high-frequency components. Without the series-connected

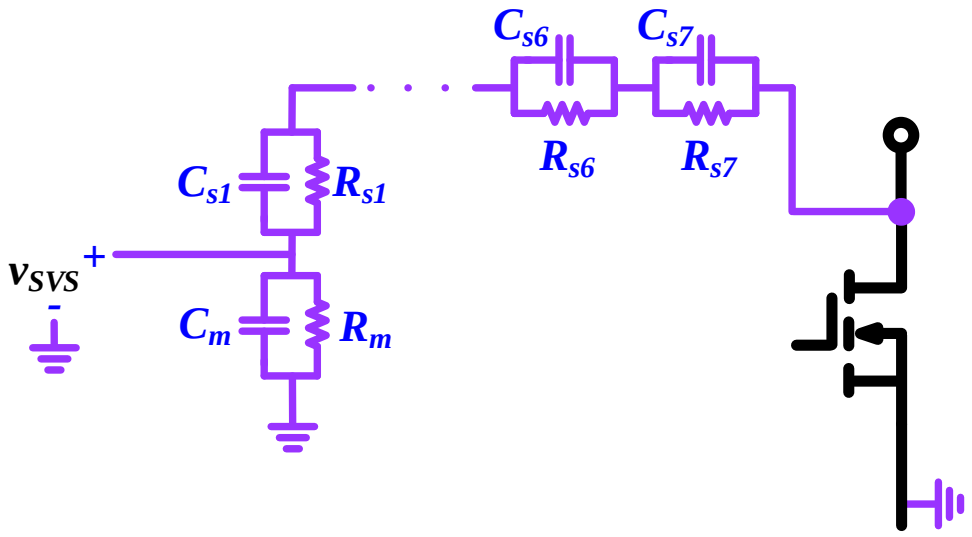


Figure 7.10 The overall schematics of the switch voltage sensor (SVS).

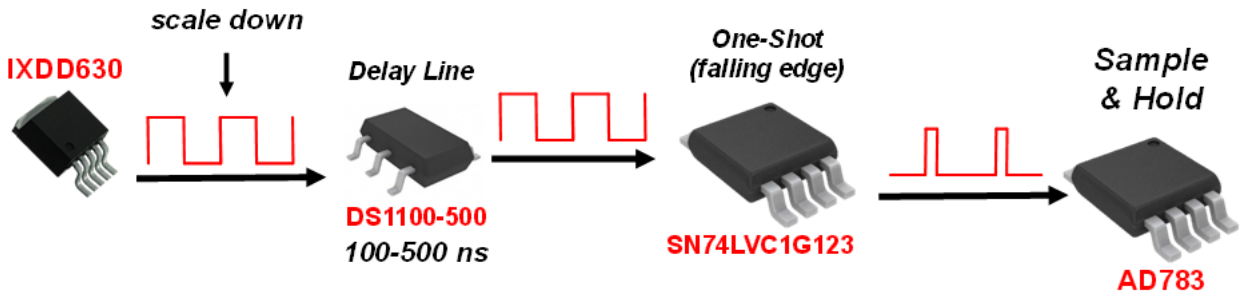
capacitors (Cs) the resulting RC network would be a very low-bandwidth measurement method, resulting a several µs for the measured voltage to reach its steady-state value. For this purpose, the capacitors (Cs) are paralleled with the resistors (Rs). The selected capacitors and resistors are all surface-mount components in 0603 package. The voltage rating of resistors is 400 V and the voltage rating of capacitors is 250 V. This is the reason why total of 7 RsCs branches are connected in series for the 1.7 kV SiC MOSFETs. A signal buffer (an op-amp with part number OPA2830) is used to buffer the measured signal.

Having the measured drain-source voltage, a sample-and-hold (S/H) unit is placed to sample the voltage for control purposes. Among abundant options for the S/H IC, AD783 of Analog Devices is used, which has significantly short sampling time. According to the datasheet, the sampling time for the selected IC is typically less than 250 ns. Also, drop rate of the sampled signal is 0.02 µV/µs. Despite the mentioned advantages, a problem with the selected S/H IC is its input voltage range. As explained before, the measured V_{DS} will be in 0-5 V range, while the signal input of the S/H IC is in -2.5 to +2.5 V range. This makes it necessary to use a secondary op-amp and subtract 2.5 V from the measured V_{DS}. Also after sampling was performed, another op-amp will need to add 2.5 V to the sampled signal, to make sure it equals the original measured V_{DS}.

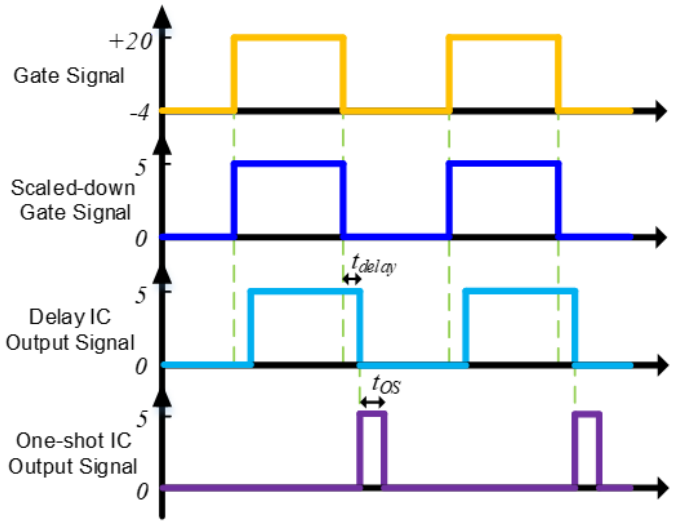
The timing schematics for the sample-and-hold architecture is shown in figure 7.11(a). According to this diagram, first the gate signal is scaled-down by means of resistors and a diode in order to change the gate driving signal scale. The gate driving signal is usually -4/+20 V or -5/+19 V, and this needs to be changed to 0/5 V so that the voltage magnitude does not damage the ICs. Once the gate voltage magnitude was scaled down, a delay IC is used to give the desired

amount of delay to the signal. The purpose of delaying the gate signal is to ensure that the MOSFET has turned completely off, to start sampling its drain-source voltage.

The used delay IC is DS1100-500, which has an input and a total of 5 outputs. The outputs have 100-, 200-, 300-, 400- and 500 ns delay with respect to the input signal. The output of the delay IC is fed to a one-shot multivibrator IC (SN74LVC1G123 of Texas Instruments) to produce a pulse at falling edge of the delayed gate signal. The pulse is fed to the S/H IC as sampling command, and its width (which is tunable by means of a resistor and a capacitor) is set to 400 ns



(a)



(b)

Figure 7.11 (a) The overall mechanism of sample-and-hold command generation on the gate driver and (b) Timing diagrams of the signals in S/H procedure.

to ensure a successful sampling by the S/H IC. The time sequence of the explained procedure is shown in figure 7.11 (b).

Having V_{DS} measured and sampled, a PI controller is used to generate the appropriate V_{CTRL}. Also, once the base voltage for Q_1 was generated, it needs to be isolated since according to figure 7.7 Q_1's emitter is not sitting on main MOSFETs source (considering that the ground for all calculations and measurements is source of the MOSFET). The PI controller is realized by means of an isolated error amplifier IC with part number ADUM3190, and its output is fed to the BJT's base after being buffered by an op-amp stage. Also, since the IC's output voltage is in the range

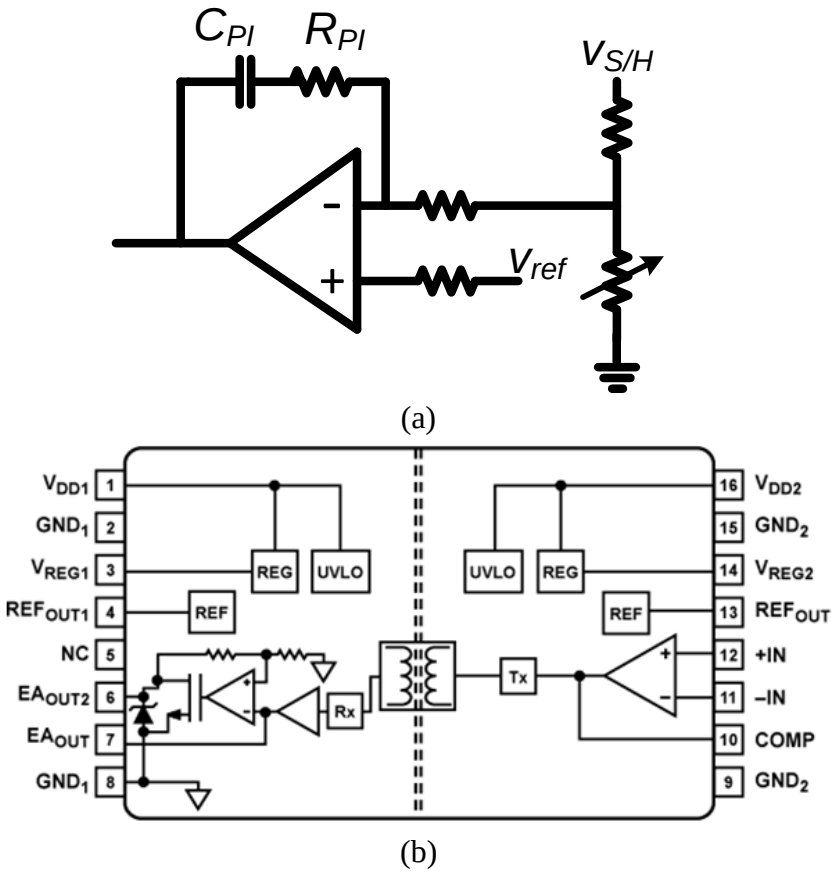


Figure 7.12 (a) Realization of an analog PI controller using an op-amp and (b) Pin configuration of the selected IC with part number ADUM3190 with internal isolation of the output value.

of 0-2.4 V, the op-amp is used and set to have a gain of 2, so that the base voltage for BJT lies in 0-4.8 V. The schematics of the PI controller as well as the pin configuration for ADUM3190 IC are shown in figures 7.12(a) and 7.12(b), respectively.

Last but not least, the maximum and minimum values of V_{CTRL} are controlled on the gate driver board. Definition of minimum and maximum values for V_{CTRL} is to avoid significant imbalance among the devices in series for a given value of Miller capacitor C_M. The minimum value for V_{CTRL} is generated on the board by means of a resistive divider circuit, and is controllable with a trimmer. Thus, when the gate driver board gets powered on, the minimum value of V_{CTRL} gets generated. On the other hand, the maximum value of V_{CTRL} is controlled by a zener diode. Figure 7.13 shows the circuit configuration that is used on the gate driver board.

Figure 7.14 summarizes the schematics of the gate driver designed and implemented embedding the proposed active dv/dt controller. Note that both top and bottom channels include the closed-loop controller and active dv/dt voltage balancing systems. Although no controller is needed for the bottom switch when stacking two SiC MOSFETs (as done in this dissertation), the two channels are made symmetric for possible extension of switches in stack in future.

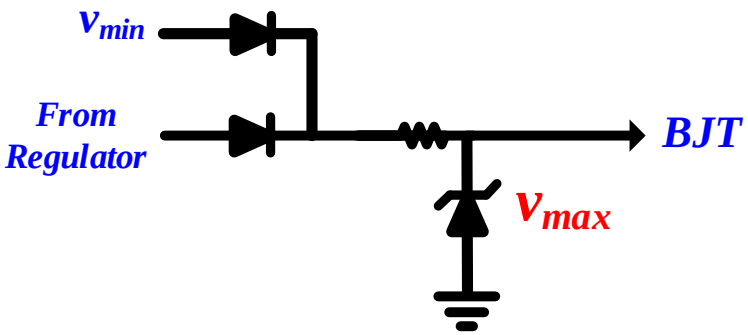


Figure 7.13 Circuit configuration used on the gate driver board for controlling V_{CTRL}.

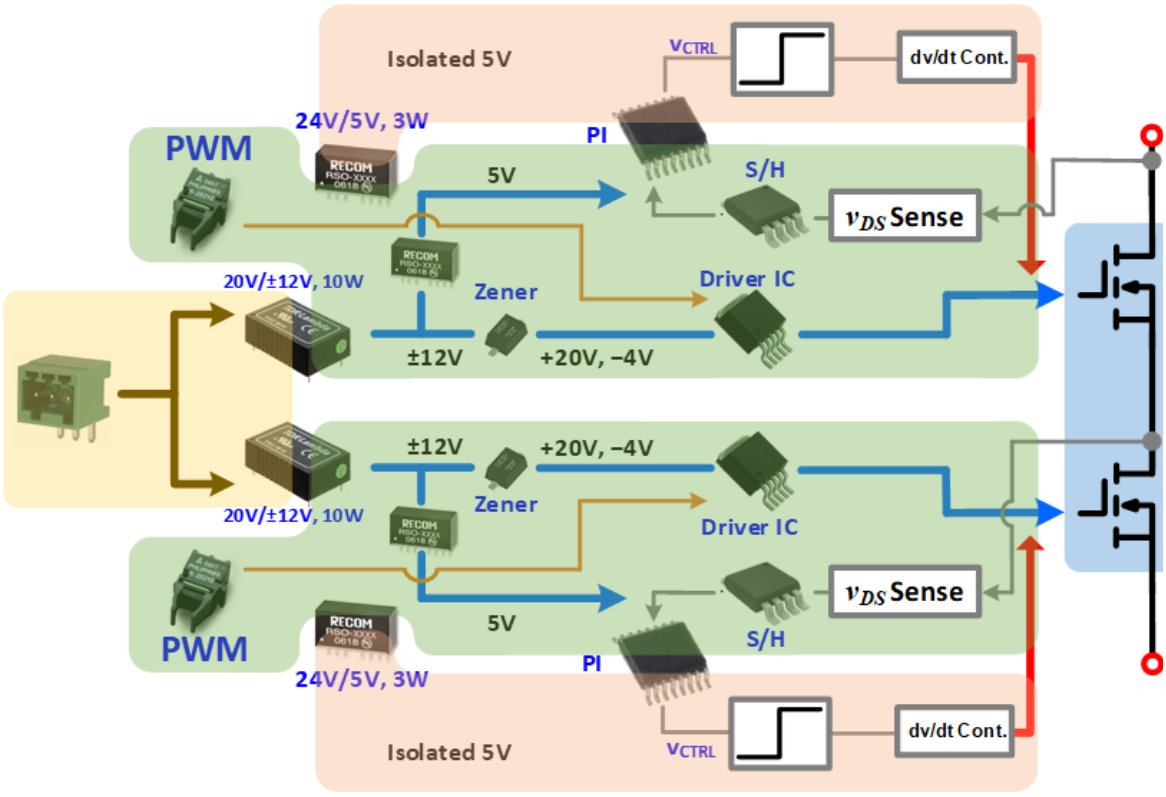


Figure 7.14 Overall schematics of the designed gate driver, embedding closed-loop controller and active dv/dt voltage balancing circuits.

7.4 Simulation Verification Results

In order to investigate feasibility of the proposed method, a set of simulations are done in SABER environment. In the first step using SABER Power MOSFET tool, an accurate model is derived for a 1.7 kV SiC MOSFET. Due to unavailability of switch internal structure for the SiC MOSFET from GE, the model is developed using 1.7 kV 325 A SiC MOSFET of Wolfspeed with part number CAS300M17BM2. Later, the model is used for simulation of the voltage sharing between two stacked SiC MOSFETs. Finally, by employing the proposed voltage balancing method in simulation environment, its effectiveness is investigated.

Figure 7.15 shows the simulated and experimental results for a switching transient in a simple chopper circuit, where the waveforms resulting from simulations for V_{GS}, V_{DS} and I_D are in close match with the experimental waveforms.

Having the model derived in previous part, the setup of figure 7.3 for stacked SiC MOSFETs is simulated in SABER environment. Total of two simulation case studies are defined, where in the first simulation by setting an appropriate value for the parasitic capacitance of gates to ground, the shown voltage imbalance of figure 7.6 is replicated. The capacitor value is selected based on trial and error, since the modules used for experiment and the one used for simulations are not the same type. Note that utilization of GE's 1.7 kV SiC MOSFET for experiments was due to request from sponsor of the project.

Figure 7.16 shows the simulated values for different quantities of the stacked SiC MOSFETs in series-connected mode. By adding 22 pF of parasitic capacitance between the gate of each MOSFET and the ground, the same voltage imbalance as shown in figure 7.6 is achieved.

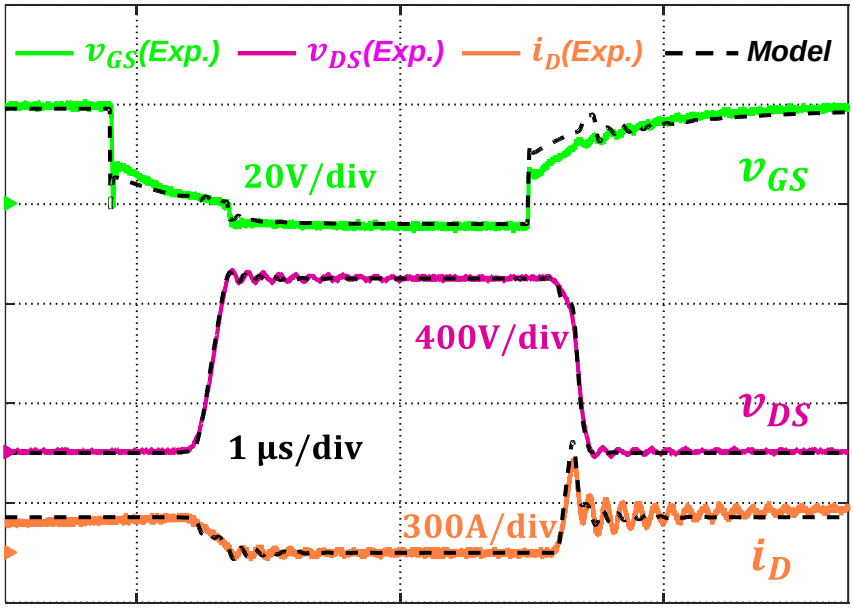


Figure 7.15 Simulated and Experimental waveforms for the 1.7 kV 325 A SiC MOSFET of Wolfspeed.

In the second simulation, the voltage sharing among two 1.7 kV SiC MOSFETs is shown while the proposed method is applied. A 100 pF Miller capacitor is added to the system and the rest of the circuit including V_{DS} measurement, sample-and-hold and PI controller are built in SABER environment. Figure 7.17 shows the voltages for the top and bottom MOSFETs where the dc voltages are balanced within a few switching cycles.

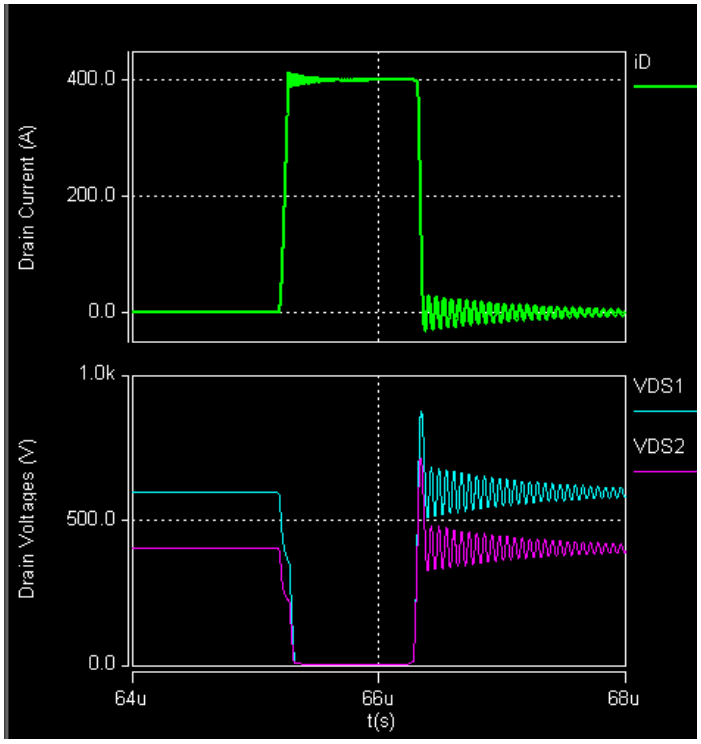


Figure 7.16 Simulated results for natural voltage sharing among two SiC MOSFETs stacked.

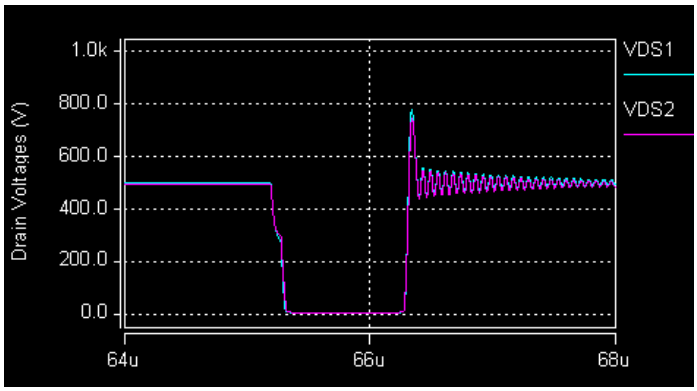


Figure 7.17 Simulated results for the active dv/dt control resulting in nearly perfect voltage sharing for two SiC MOSFETs connected in series.

Note that in the simulations, other than the leakage capacitances from gates to ground, some additional details are added to the simulation in order to feature a closer approximation of the experimental system under study. For this purpose, the parasitic inductances of the busbars connecting the devices together, ESR and ESL of the capacitors used in the setup and etc. are taken into consideration. The shown simulation results provide proof of validity for the proposed method of this chapter.

7.5 Experimental Verification Results

7.5.1 Gate Driver Design

A 6-layer PCB is designed for GE's 1.7 kV SiC MOSFET (figure 7.2) embedding the functionalities discussed so far. Since the PCB is designed for dc voltages around 2 kV, in a similar fashion to PCBs designed in chapter 2 the medium-voltage design guidelines are taken into consideration for it. Also, since it was of great importance not to extend the PCB out of DUT's borders, the PCB is designed in two stories where the power supplies and the fiber optic receivers are moved to the top board, while the gate driving parts, signal measurement/processing parts and the active dv/dt controller are embedded on the bottom board.

Figure 7.18 is showing the designed PCB for the discussed gate driver system. As it can be seen, there are keep-out layers on the PCB in order to increase the creepage distance between components as well the two channels. Also figure 3.19 shows the 3D view of the designed PCBs for top and bottom board. Note that the keep-out layers are not demonstrated in figure 7.19.

On the designed PCB, a special effort is done to make the signal routes (carrying gate signals and the measurement data) as short as possible. Also, for all of the voltages that are being

transferred from the top board to the bottom one using 20-pin connectors, decoupling capacitors are used on the bottom board in order to remove any high-frequency noise component.

7.5.2 Experimental Setup Implementation

The setup built based on the schematics shown in figure 7.3. As shown in figure 7.20, the capacitors are placed in closest possible vicinity to the devices under test and they are connected via busbars made with superconductor copper with 60 mils (1.5 mm) thickness. Also, garolite

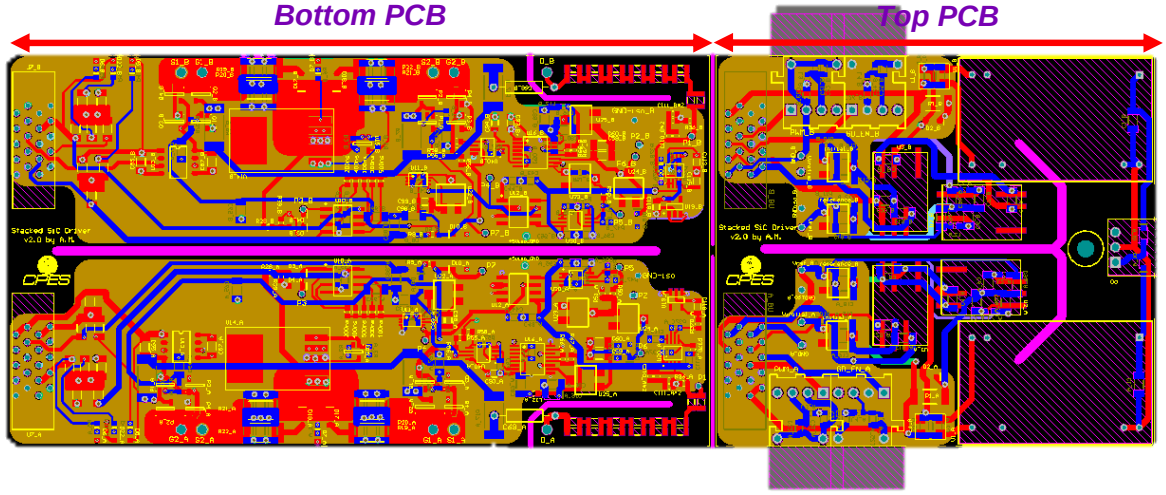


Figure 7.18 The 6-layer 2-story PCBs designed for GE's stacked SiC MOSFETs.

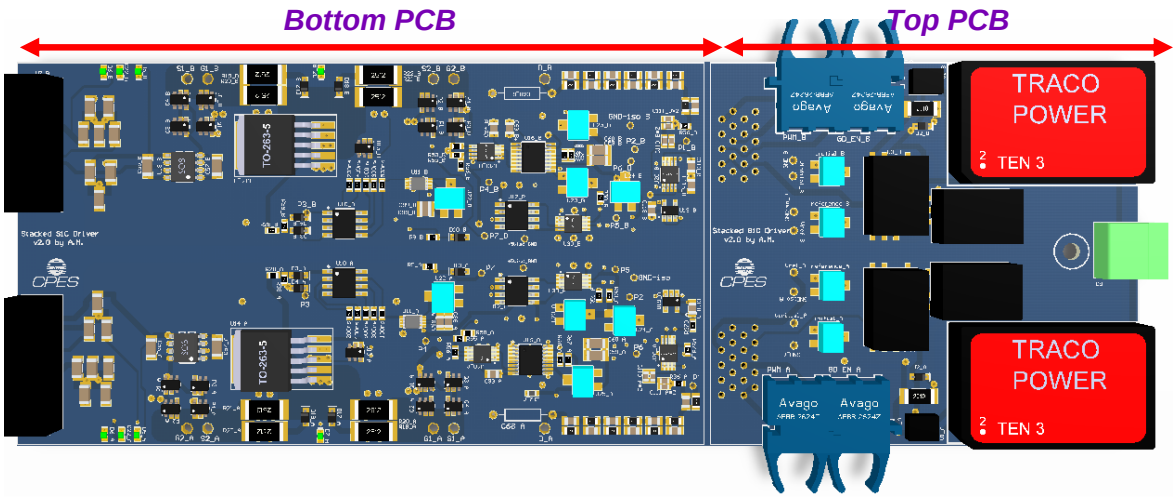


Figure 7.19 3D schematics of the designed PCBs.

layers are placed on top and beneath the busbars to provide further mechanical strength and electrical insulation for them. In parallel with each capacitor, a 100 kΩ 10 W resistor is connected for better voltage sharing and faster discharge when system turns off.

As mentioned before, both static and dynamic voltages must be balanced between the stacked power semiconductors. The proposed method works for dynamic voltage sharing, while for static voltage sharing a 50 kΩ resistor is connected in parallel with each MOSFET. These resistors can be seen in figure 7.20.

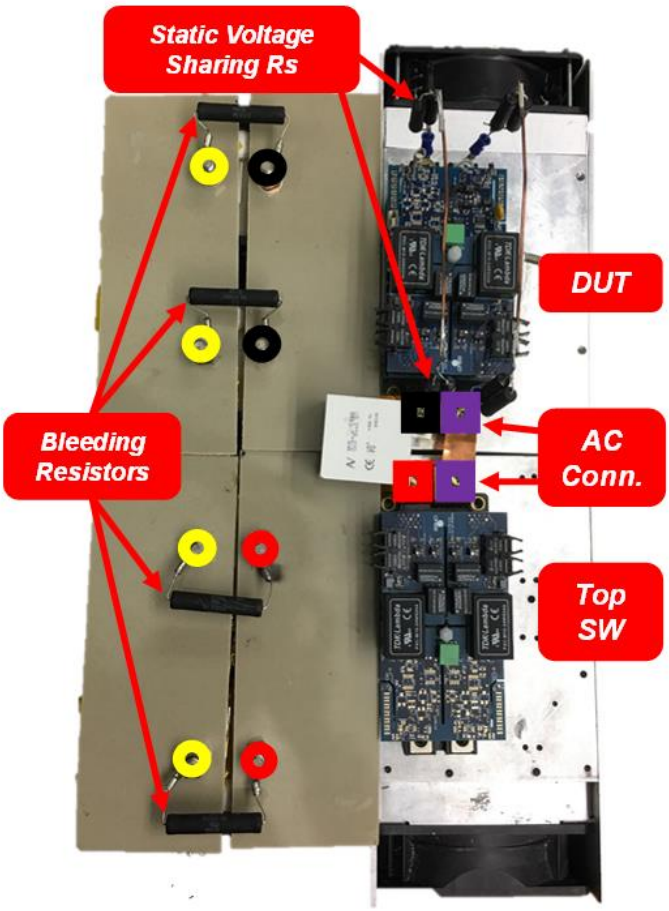


Figure 7.20 Implemented setup using the designed gate drivers. The positive, negative and mid points on the capacitor terminals are shown in red, black and yellow colors, respectively. Also device AC terminals are shown in purple.

In figure 7.20, the positive, negative and middle point of the busbars are specified with red, black and yellow colors, respectively. Also, the module containing the top and bottom MOSFETs is specified with DUT, while the top switches (diodes) are within the module which is specified with “Top SW”.

Last but not least, the switches are mounted on heat sinks. This is mainly done in order to adjust the profile of the devices to feature minimum distance from the capacitors. As a result, the stray inductances of the busbars from capacitors to the devices will be smaller. Otherwise double-pulse test is a low-power test in nature, and it does not need heat sinks for the devices under test.

7.5.3 Experimental Results

In the first step toward getting the experimental results, the system experimental setup and the gate driver are debugged. Figure 7.21 shows the functionality of the ICs responsible for generating sample-and-hold command. According to this plot, the gate signal is properly scaled down and delayed by the delay IC. Also, the one-shot IC creates a sharp pulse at the down-falling edge of the gate signal. The selected delay as well as the one-shot IC’s pulse width are set to be 400 ns.

On the other hand, the drain-to-source voltage measured on the gate driver is shown in figure 7.22. This figure demonstrates a pulse given to gate of the both top and bottom MOSFETs as well as the measured voltage. As it can be seen, at both turn-on and turn-off switching the measured voltage is capable of reaching its steady state value within 300 ns, thanks to the designed on-board V_{DS} measurement system. Also, the voltage gain is measured to be the target 0.00338.

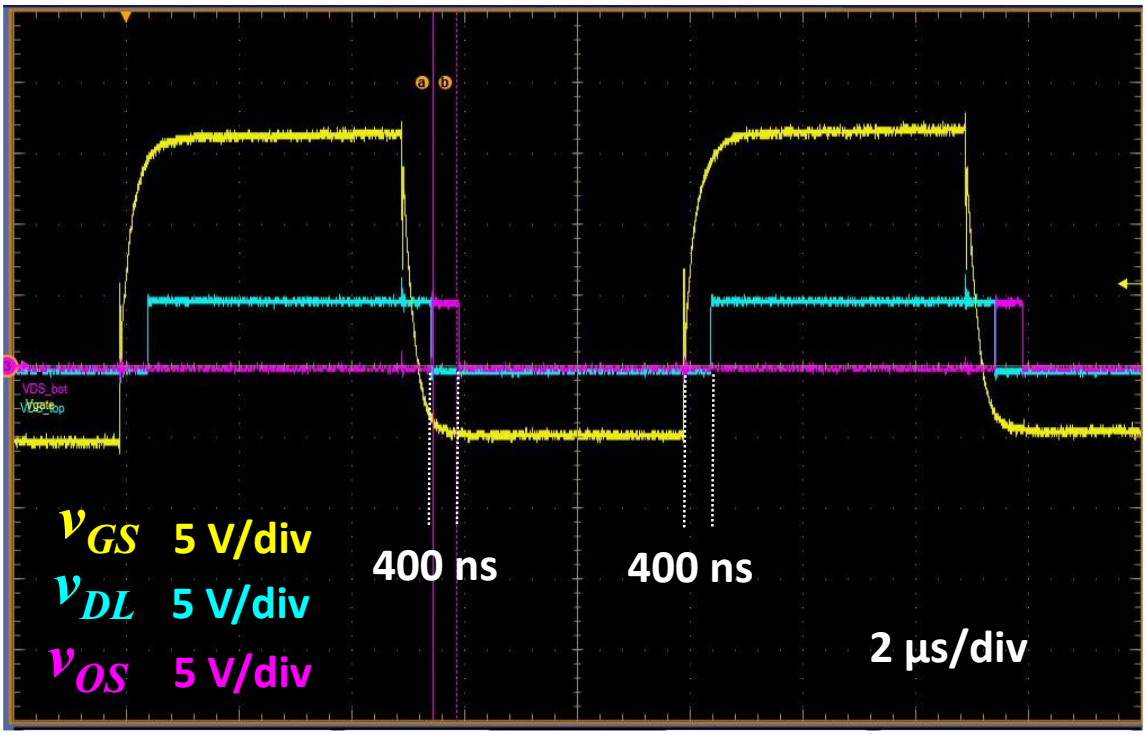


Figure 7.21 The gate signal of the MOSFET (V_{GS}), the scaled-down and delayed gate signal (V_{DL}) and the sampling command generated by the one-shot IC (V_{OS}).

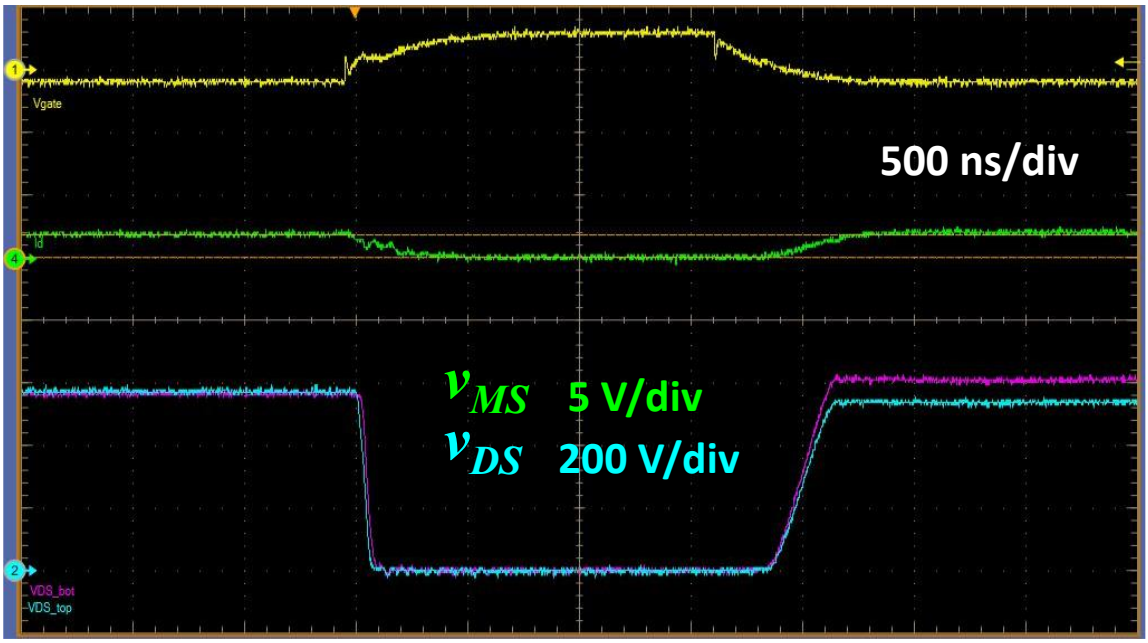


Figure 7.22 The gate signal of the MOSFET (V_{GS}), the drain-to-source voltage of the MOSFET (V_{DS}) and the measured drain-to-source voltage on the gate driver (V_{MS}).

Once the gate driver system and the double-pulse test setup were debugged, two test scenarios were defined and completed in order to experimentally demonstrate effectiveness of the proposed method for voltage balancing among stacked semiconductors. First, the tests are done in open-loop mode where the value of V_{CTRL} is controlled by the trimmer placed on the top board. Next, the tests are done in closed-loop mode where the closed-loop controller sets the value of V_{CTRL}.

Figure 7.23 shows the voltage sharing among top and bottom MOSFETs in a stack while the value of the Miller capacitor is set to 100 pF. In order to achieve the results of figure 7.23, a pulse train with total of 16 pulses with 50% duty cycle are fed to gate of the top and bottom MOSFETs. Time period of each gate pulse is 2.5 µs and thus, considering approximately 145 µH inductance for the load inductor, the final drain current is about 250 A.

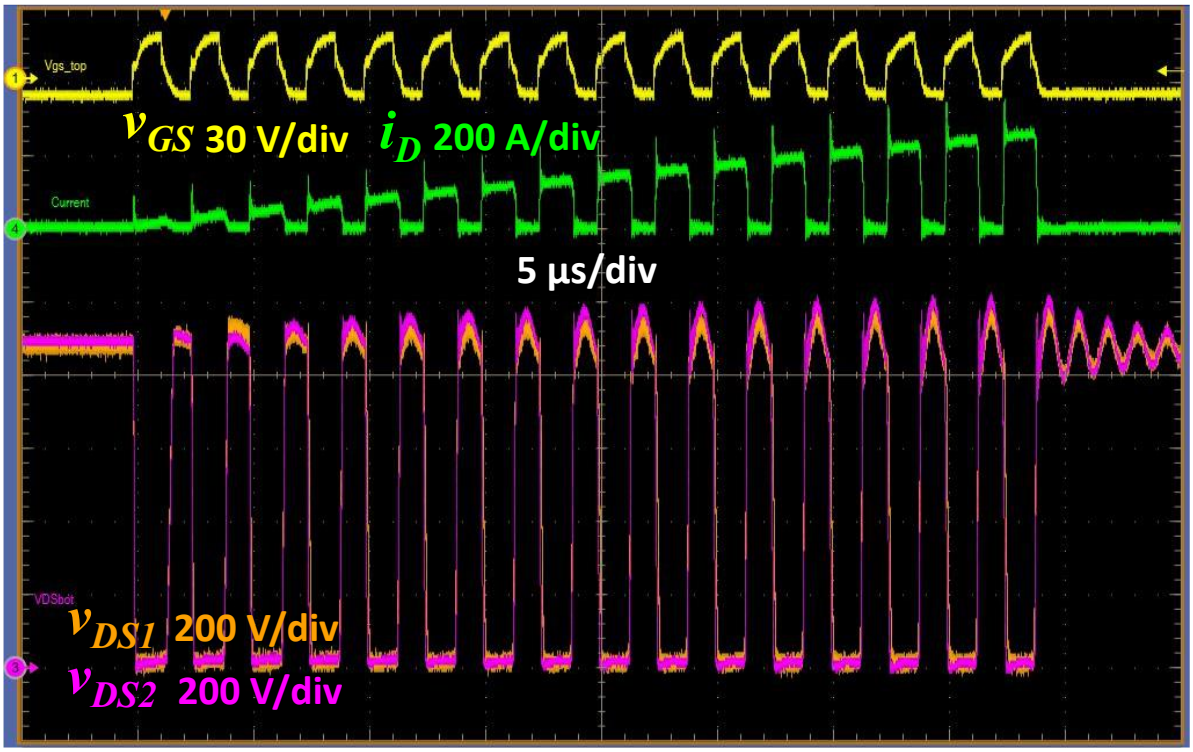


Figure 7.23 Voltage sharing between the top (V_{DS1}) and bottom (V_{DS2}) MOSFETs in stack while the Miller capacitor value is set to 100 pF and the value of V_{CTRL} is 1.385 V.

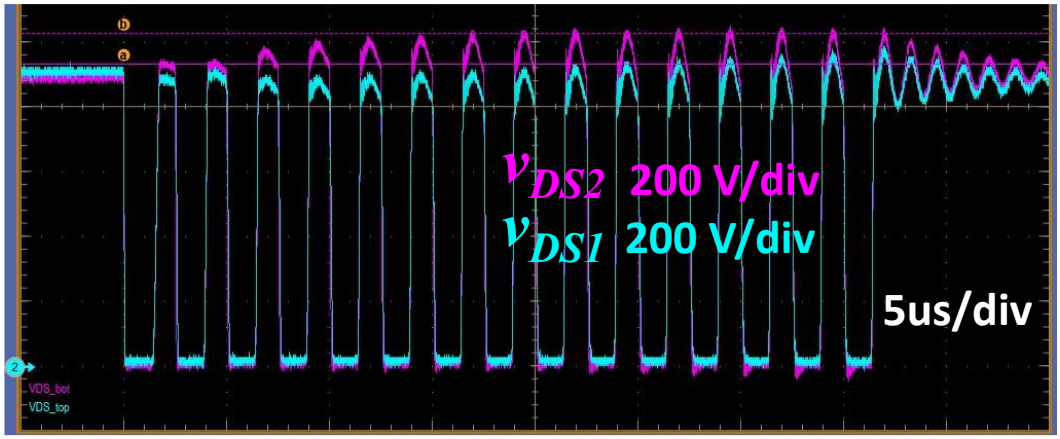
According to figure 7.23, for a wide range of drain current up to around 250 A, the voltages across top and bottom MOSFETs are falling within 10% range from each other (which is the criteria by the sponsor of the project). The worst-case voltage imbalance observed from figure 7.23 is measured to be about 44 V. Note that for the setup shown in figure 7.20, a low-voltage passive probe is used for measuring the gate signal. Two P5100 passive probes are used for measurement of the drain voltages (where voltage across the top MOSFET is calculated by a math function) and finally the drain current is measured by a 600 A rogowski current probe.

It was mentioned before that the proposed method comes with the advantages of capability to work with fast-switching SiC MOSFETs and low additional losses (which will be discussed later). As it can be concluded from figure 7.23, a single value for V_{CTRL} is enough to guarantee voltage balancing to ±5% margins for the whole current range. This is another advantage of the proposed since a variety of voltage balancing schemes need additional considerations/updates as the switch current changes.

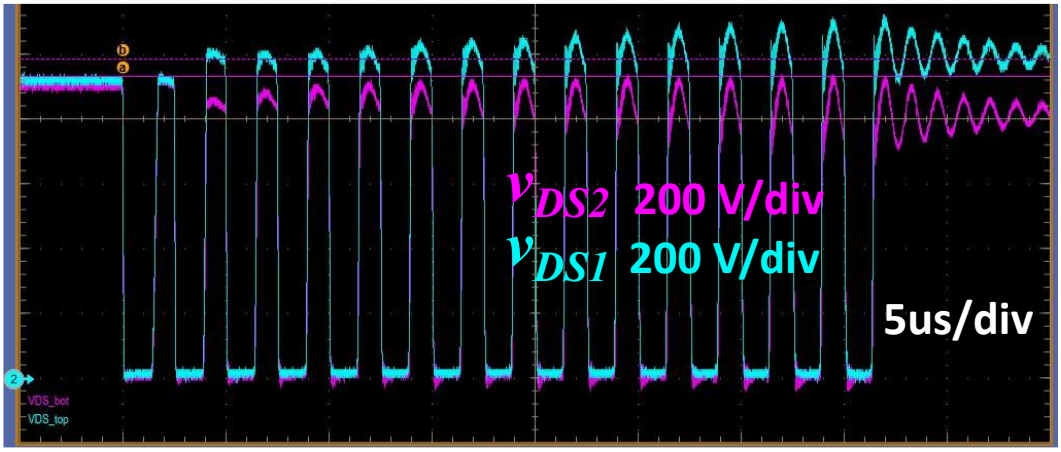
Note that at the beginning the Miller capacitor value is selected to be very small (10 pF in this study) and then it was increased in steps until the amount of the injected Miller current guarantees safe operation of both top and bottom devices for the whole range of V_{CTRL}. This is important so that until the closed-loop controller achieves its steady-state condition, the stacked devices continue to switch safely. In other words, it is expected to PI controller to be saturated at the beginning of operation, and this should not take the system to instability.

Figure 7.24 shows the experiments performed for selection of the Miller capacitor, where for the selected 100 pF capacitor the value of V_{CTRL} is varied from 0 V up to nearly 4 V, and the voltage imbalance between top and bottom MOSFETs in none of the cases is extreme enough to break the

stack. As it can be seen, in case of 0 V for V_{CTRL} where majority of the Miller current is flowing to gate of the top MOSFET by Q_2, the top MOSFET is slowed down and the voltage across the bottom MOSFET becomes larger. On the other hand, in case of 7.9 V voltage for v_{CTRL}, (assuming around 0.7 V drop on the diode that is demonstrated in figure 7.13, the actual base voltage would equal 3.2 V) the voltage across the top MOSFET is larger than the bottom one. However, none of the cases leads to damage to one of the MOSFETs and this will guarantee that the closed-loop controller will have enough time to balance the voltage across devices.



(a)



(b)

Figure 7.24 Voltage sharing between the top (V_{DS1}) and bottom (V_{DS2}) MOSFETs in stack under (a) V_{CTRL} equal to 0 V and (b) V_{CTRL} equal to 3.9 V.

In the next experiment, the voltage balancing is achieved by means of the closed-loop controller. The maximum value set for V_{CTRL} according to the configuration shown in figure 7.13 is 4 V, and there is no minimum value defined for it.

The closed-loop test results are shown in figure 7.25. According to this figure, the pulse train is different than the one used for open-loop tests. Total of 23 pulses with 5% duty cycle are fed to the gates, so that the closed-loop controller would have time to balance the voltages among top and bottom devices.

At the gate driver's startup (also even after a fairly long time where the S/H IC's output discharges), the measured V_{DS} on the gate driver board equals 2.5 V (0 V from output of the sample-and-hold IC plus 2.5 V from the adder cascaded with it). One the other hand, in case of

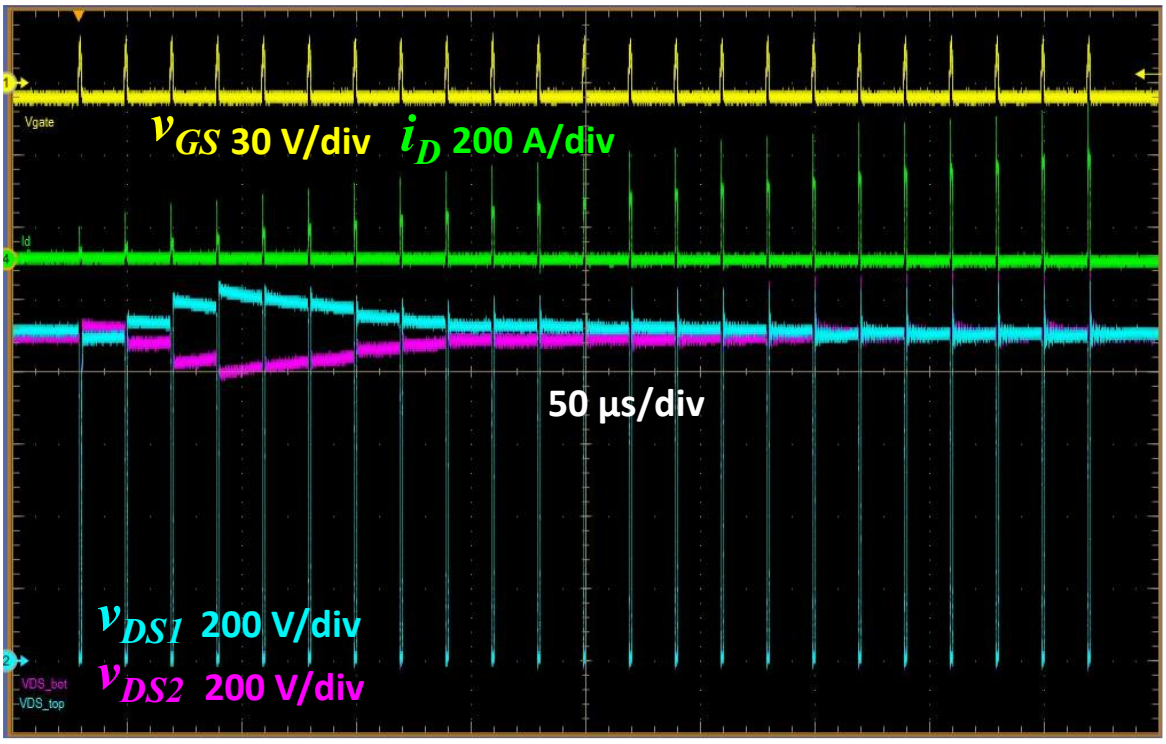


Figure 7.25 Voltage sharing between the top (V_{DS1}) and bottom (V_{DS2}) MOSFETs in stack while the Miller capacitor value is set to 100 pF and the value of V_{CTRL} is being controlled by the closed-loop controller.

completely balanced voltages between the MOSFETs this values must be 3.05 V. So at the startup condition, the PI controller (which has been integrating the difference between the constant reference voltage and the existing 2.5 V) is saturated and the corresponding V_{CTRL} is around 4 V. As explained before at high base voltage for Q_1, it is expected that the Miller current derived by the 100 pF capacitor will not impact the switches significantly. In other words, minority of the Miller current will be directed to gate of the top MOSFET.

Within first 4 switching cycles of figure 7.25 and as device dv/dt rate increases (by increase of its drain current according to (7.1) [137]), the voltage imbalance in increasing. It is clear that as dv/dt of the MOSFETs increases, the current through their parasitic gate-to-ground capacitor will also increase and it will cause further imbalance. However, after the fourth switching cycle the controller's impact becomes obvious where by reducing the value of V_{CTRL}, top MOSFETs voltage starts reducing.

$$\frac{dV_{DS}}{dt} = \frac{(I_D + gm.(V_{th} - U_t)}{(C_{GD}.(1 + R_G.gm) + C_{DS})} \tag{7.1}$$

where I_D is the drain current, gm is the transconductance, R_G is gate resistance and C_{GD} and C_{DS} are the Miller and drain-to-source capacitances of the device, respectively. Note that figure 7.26 shows the experimental proof for dependency of voltage imbalance on drain current, where the same pulse train is fed to gates of the top and bottom MOSFETs under 1.2 kV dc bus (to ensure no failure would happen in case of worst-scenario voltage sharing). As it can be seen from this figure, the voltage sharing has a meaningful relation with the drain current and it

As it can be seen from figure 7.25, within 6 switching cycles (120 µs) from the beginning of the pulse train, the voltage imbalance between two MOSFETs gets balanced to ±10% range. Also,

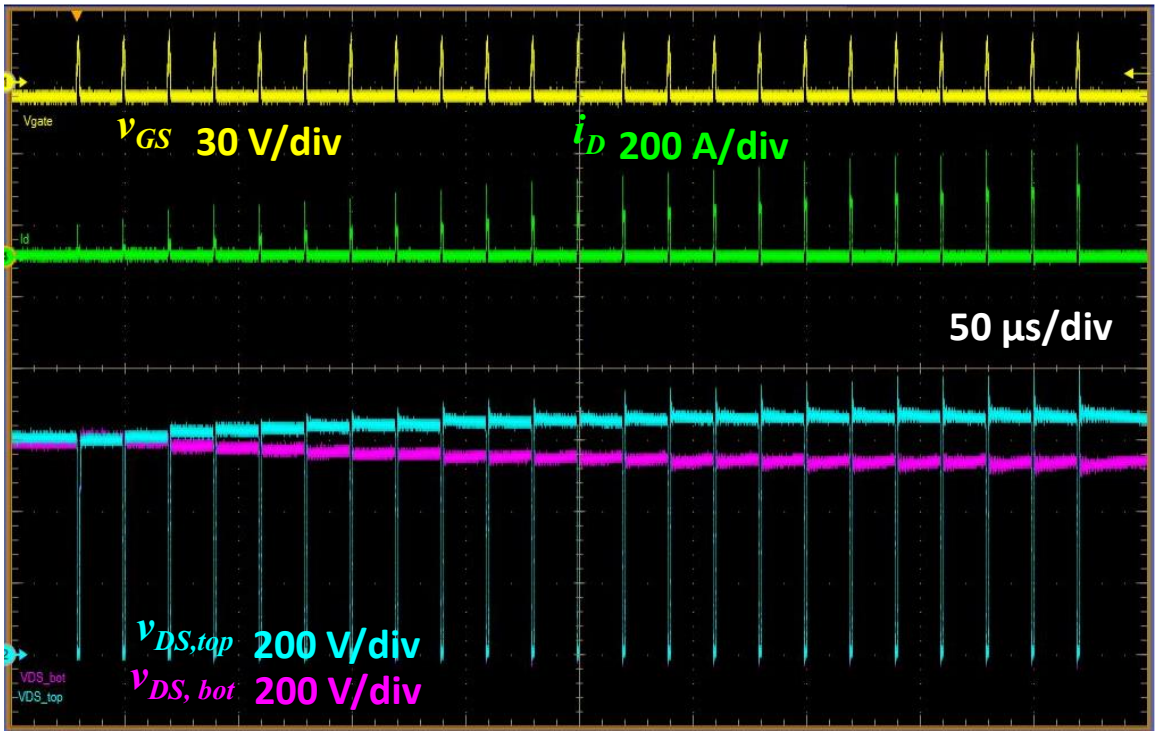


Figure 7.26 Natural voltage sharing among the top and bottom MOSFETs in the stack as a function of drain current.

the steady-state error of this method seems to be almost zero, while majority of the voltage balancing schemes cannot achieve this. Figure 7.27 zooms into the last pulses in the pulse train shown in figure 7.25 to prove this.

So far voltage balancing among the devices under test were discussed. It is of great importance to ensure that the voltages are properly balanced across the top switches (body diodes of the top SiC MOSFETs). In order to investigate this, an experiment is conducted and while switching the bottom devices, voltage sharing among the top devices is measured. According to figure 7.28, the voltages across the top diodes are always within ±10% range, although there is no voltage balancing method used for them (neither static voltage balancing resistors, nor dynamic voltage sharing scheme). Note that V_{F1} and V_{F2} in figure 7.28 are the voltages across top and bottom diodes and are specified in figure 7.3. Voltage balancing among diodes is good because of their natural

commutation. In other words, when the diodes turn-off, there is no parasitic current contributing to the turn-off process (like in case of the MOSFETs as explained before). This is another proof that the main factor contributing to unequal voltage sharing among stacked semiconductors is the parasitic capacitance from gates to ground.

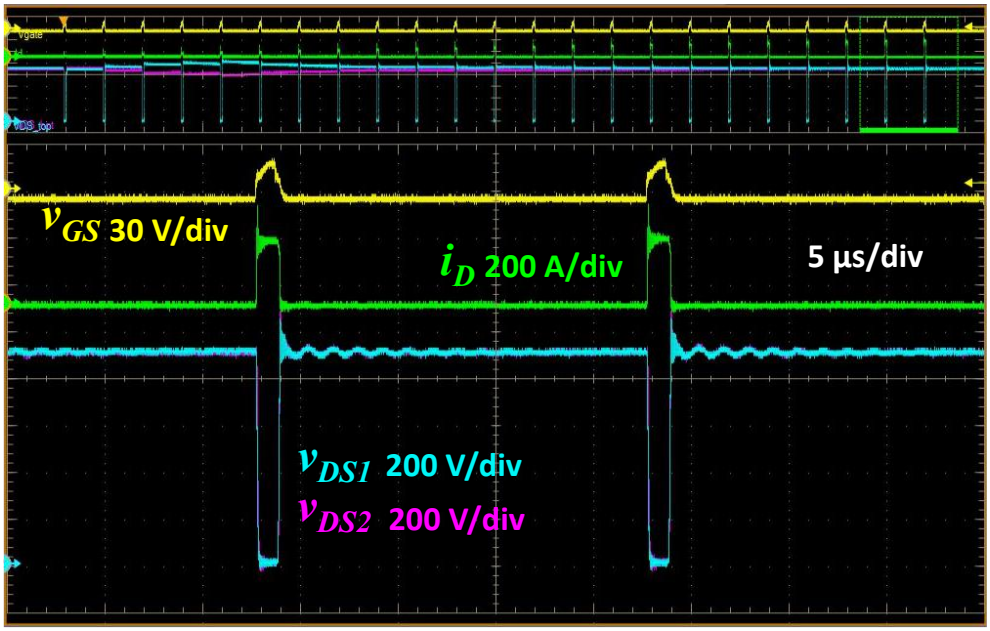


Figure 7.27 Zoomed-in voltage sharing between the top (V_{DS1}) and bottom (V_{DS2}) MOSFETs.

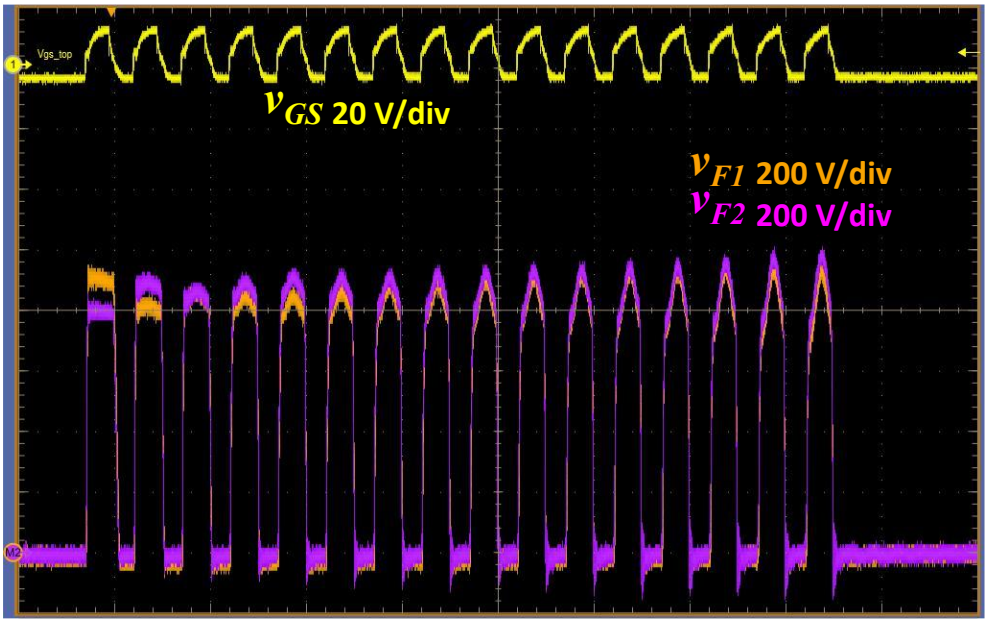


Figure 7.28 Voltage sharing among diodes in the top switch while no voltage balancing scheme is used.

Table 7.1 Switching losses measured from the top and bottom MOSFETs at 1800 V total dc link voltage and 240 A drain current.

Device	Parameter	Value
Top MOSFET	E_{on}	9.92 mJ
	E_{off}	10.84 mJ
Bottom MOSFET	E_{on}	7.85 mJ
	E_{off}	10.17 mJ

Last but not least, as mentioned before the proposed method does not modify switching losses of the devices in a considerable way. Table 7.1 shows the measured losses at turn-off and turn-on switching at 250 A drain current, where it can be seen that both the turn-off and turn-on losses between top and bottom MOSFETs are very close to each other. Assuming that the losses of the bottom MOSFET are not modified by any external means, the top MOSFET's total switching loss is increased by less than 15% compared to the bottom MOSFET (less than 7.5% change in switching losses for the two MOSFETs in the stack). Figure 7.29 shows the turn-off waveforms where similar slew rates for the top and bottom MOSFETs' V_{DS} can be observed.

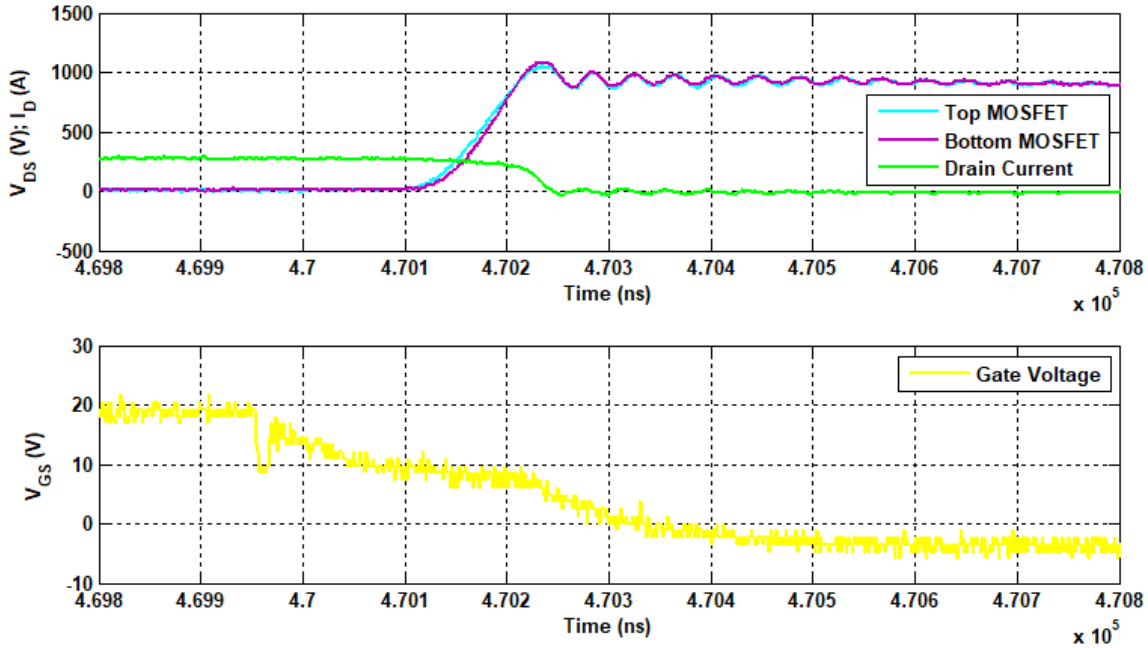


Figure 7.29 Switching-off waveforms of the top and bottom MOSFETs in the stack, showing close slew rate for their V_{DS} resulting in minimum variation of losses for the devices.

7.6 Comparison of stacked and single 3.3 kV SiC MOSFETs

So far a reliable 3.3 kV SiC MOSFET was shown by series-connecting the 1.7 kV SiC MOSFETs from GE. As mentioned and according to [33], when stacking SiC MOSFETs it is expected to achieve deices with better performance from R_{DSon}, current density, switching loss and finished price points of view. It is clear that this can only be true once the devices under test have similar manufacturing technology. In this section the 3.3 kV SiC MOSFET of Sumitomo Electric Industries is compared to the achieved 3.3 kV SiC MOSFETs by stacking two 1.7 kV SiC MOSFETs in series.

Figure 7.30 shows the on-resistance of the two 3.3 kV MOSFETs at 400 A current rating for them. Note that the on-resistances of the 500 A MOSFET from GE are addressed in [136], and in order to derive the estimated on-resistance for a 400 A MOSFET, the results from [136] are scaled

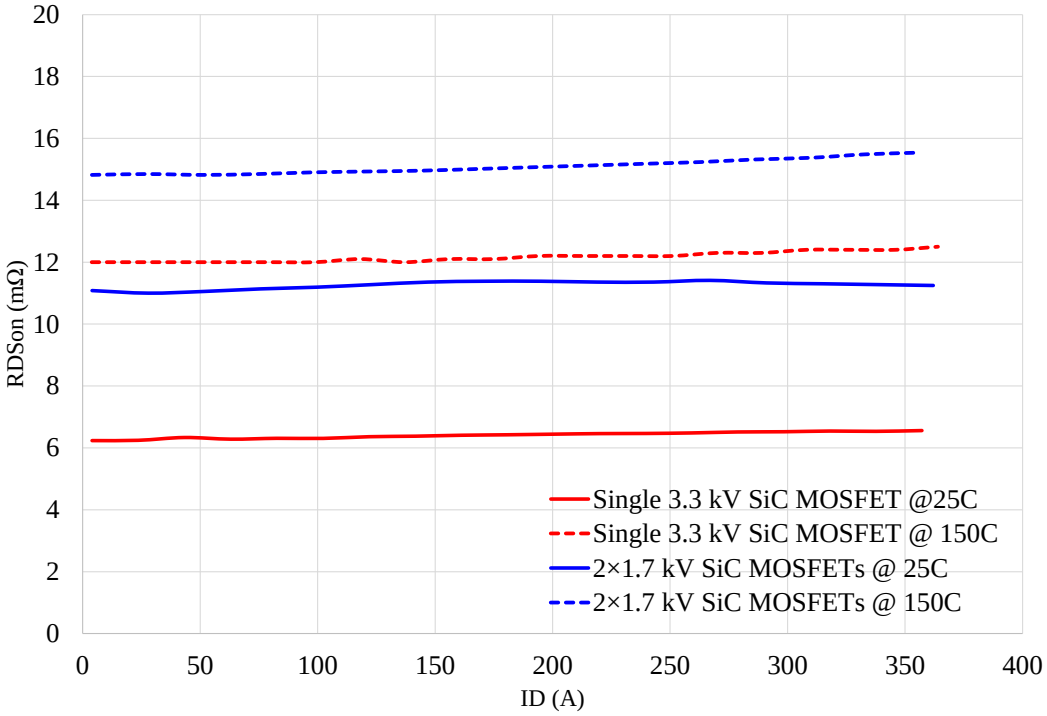


Figure 7.30 Specific on-resistances of the stacked and single 3.3 kV SiC MOSFETs at 400 A rating.

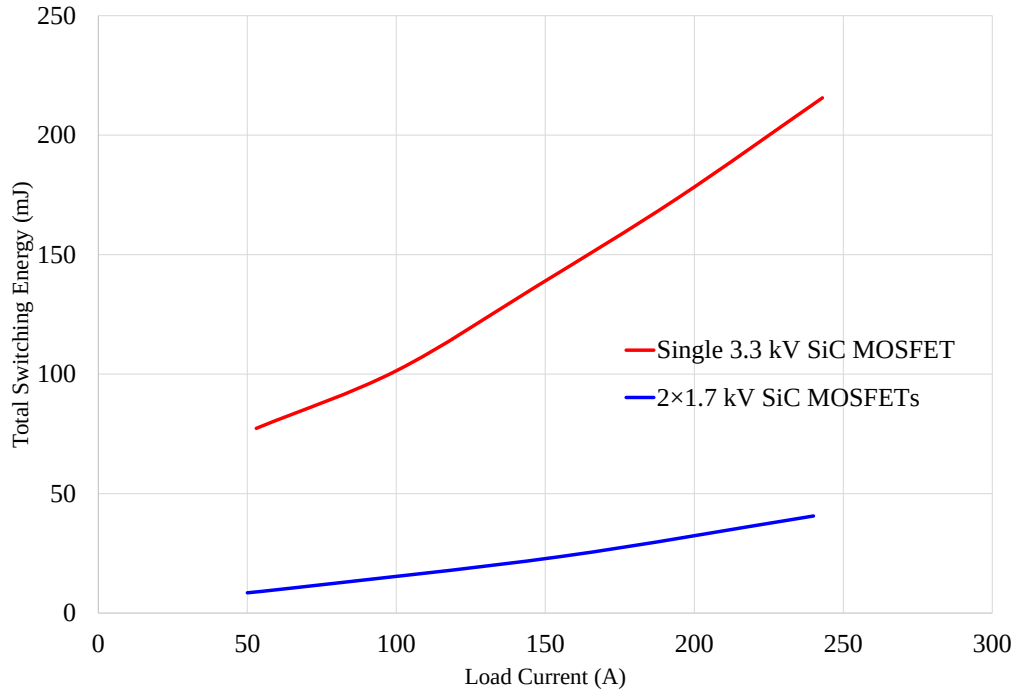


Figure 7.31 Total switching losses of the stacked and single 3.3 kV SiC MOSFETs at room temperature.

linearly. As it can be seen, despite expectations the 3.3 kV SiC MOSFET of SEI features better on-resistance than the stacked SiC MOSFETs. The main reason for this is coming from different technology of manufacturing semiconductors between GE and SEI. Smaller R_{DSon} of SEI's MOSFETs is not only in case of their 3.3 kV SiC MOSFETs. In fact, according to [9] and [138] for 1.2 kV SiC MOSFETs the product of SEI has the smallest R_{DSon} among 8 different MOSFETs from 5 different manufacturers. To be more specific, SEI's MOSFET at 1.2 kV features 65% of the specific R_{DSon} as the GE semiconductor. The specific R_{DSon} value for SEI semiconductor is 3.6 $m\Omega.cm^2$ while this number for the GE MOSFET is about 5.52 $m\Omega.cm^2$ at room temperature.

On the other hand, figure 7.31 shows the total switching losses for the two SiC MOSFETs at room temperature. According to this figure, the series-connected SiC MOSFET features much smaller switching losses compared to the single 3.3 kV SiC MOSFET of SEI. It is worth to note

that the losses of the stacked switch are calculated by summation of turn-on and turn-off losses from the top and bottom MOSFETs inside the package.

Since the switching frequency of the converters in motor drive application does not need to be high (this was be discussed in details in chapter 4), the main component contributing to the converter losses is the conduction losses. That is the reason why the stacked SiC MOSFETs feature higher total losses than the single 3.3 kV SiC MOSFET of SEI and thus, the simulations/design will be carried out merely by using single 3.3 kV SiC MOSFET modules characterized in chapter 2.

7.7 Summary

In this chapter a novel method was proposed to balance voltages across stacked power semiconductors. In order to develop understanding of the main reason behind unbalanced voltages across stacked switches, a deep literature survey was performed where the main reason for this phenomenon was explained. It was shown that an additional gate current flowing through the parasitic gate-to-ground capacitors was the main reason behind imbalanced voltage balancing. Then, a novel method was proposed in order to compensate for the parasitic gate current, where no significant losses were added to the system. This makes the proposed method outperform majority of the existing voltage balancing schemes where additional losses are generated either on the device under test or in the voltage balancing circuit. Following simulations via a model derived in SABER environment, a gate driver was designed embedding the proposed scheme and experimental results were shown to prove feasibility of the introduced technique to balance voltages across series-connected power semiconductors.

Chapter 8. Conclusion

8.1 Summary

With introduction of the wide-bandgap materials such as SiC and GaN, the existing boundaries of operation for traditional Si-based semiconductors seem to be vanishing. The SiC MOSFETs have been proven to be game changing devices in a variety of applications, thanks to their superior material properties.

This dissertation tried to investigate impact of emerging medium-voltage SiC MOSFETs on medium-voltage high-power applications. For this purpose, in chapter 2 the state-of-the-art SiC MOSFETs at 3.3 kV 400 A rating were characterized. Due to unavailability of commercial gate drivers to effectively drive these MOSFETs (since the commercial gate drivers are mostly developed for slow-switching Si IGBTs/MOSFETs), a high-performance gate driver was developed for the MOSFETs under study. Full characteristics of the 3.3 kV 400 A SiC MOSFETs were derived by switching them at the boundaries of operation (as fast as possible) for use in converter design and comparison.

Having the characterization results from SiC MOSFETs, the converter design was done. Three converters that are being commercially used for motor drive applications in medium-voltage high-power range were selected for the study. This includes the cascaded H-bridge (CHB), the modular multilevel converter (MMC) and the five-level active neutral point clamped converter (5-L ANPC) converters. For each converter, closest design to the commercially existing converters

was targeted by adopting design considerations from available catalogs. Also, optimizations were performed on the MMC converter to minimize size of capacitors installed in its structure.

In order to have a compassion between the SiC MOSFETs and Si IGBTs, converter design was performed in chapter 4 using both commercial Si IGBTs as well as the state-of-the-art SiC MOSFETs. The converter design criteria were adopted from datasheets of industrial motor drives available to feature as close design as possible to the existing converters in the market. Also a total of 6 different operating points were selected (3.16-, 6.9- and 13.8 kV voltage ratings and 3- and 5 MVA power ratings) for design so that the changes in properties of the converters could be elucidated versus operating condition.

Based on the converter design, in chapter 5 a comprehensive and unbiased comparison was done between the converters under study from different aspects. The comparison consists of evaluations of converters' efficiency, power density, semiconductor utilization, required capacitive energy storage, low-frequency operation capability, operation under fault containment and number of parts (for a measure of power density). The comparison data can be used as input for selection of the best topology for a target environment and operating conditions.

Later, in chapter 6 design and implementation of an H-bridge cell was shown based on the studied 3.3 kV 400 A SiC MOSFETs to prove validity of converter modeling and performed thermal calculations. The H-bridge cell was tested at 2 kV dc bus and the maximum current rating possible in laboratory environment. The results showed a very close approximation of the experimental results by the performed simulations. Also in chapter 6 the possible uncertainties with the performed study were discussed.

Last but not least, other than characterization of individual 3.3 kV SiC MOSFETs, in chapter 7 an effort was made to realize 3.3 kV SiC MOSFETs by stacking individual 1.7 kV SiC MOSFETs. In order to achieve this goal, first the main cause of voltage imbalance among series-connected semiconductors was discovered and it was shown that the parasitic capacitances from gates of the devices to ground does affect switching speed (and voltage sharing) among them. As emphasized in chapter 3, this had widely been missed by the researchers in this area, as majority of literature have attributed unequal voltage sharing among stacked semiconductors to mismatch in gate driver system and the devices themselves. A novel method was proposed to overcome the issue and simulation/experimental results were provided to prove its effectiveness in nearly perfectly balancing voltages among series-connected SiC power MOSFETs without adding significant losses to the system.

8.2 Future Work

The following future research directions are identified during the discussed studies.

According to information from motor drive manufacturers, the number of sales for regenerative motor drive converters in 2016 has increased by 300% compared to 2012. This is due to increase in electricity price as well as more strict laws by governments toward reducing emissions. The studies performed in this dissertation took into consideration a diode front-end stage for all of the converters. However, the MMC and 5-L ANPC converters can be realized in back-to-back configuration, featuring regeneration of energy when the motor brakes. On the other hand, the cascaded H-bridge converter with power regeneration capability (by replacing the 6-pulse diode front end stage of the cells with an H-bridge cell) is under study by some motor drive manufacturers. Considering the mentioned facts, a similar study can be done between the same converter topologies with power regeneration capability.

According to [139], General Electric has recently patented a converter that can be used in medium-voltage high-power range for motor drive applications. To be more specific, the converter introduced by GE will be a rival to the 5-L ANPC converter patented by ABB. A study can be done to compare the GE-patented converter versus the other three converters that were discussed throughout this dissertation.

A novel method was proposed in this study to stack individual 1.7 kV SiC MOSFETs in series to reach higher-voltage devices. By means of simulations and experiments, nearly perfect voltage balancing among the series-connected semiconductors was demonstrated. This method can be extended to series connect more than two devices in series to show its effectiveness and also to take advantage of its outstanding performance.

Last but not least, Sumitomo Electric Industries is working on improvement of their 3.3 kV SiC MOSFETs. According to information from the Japanese company, the new generation of discrete 3.3 kV SiC MOSFETs will be available early 2018, and the modules based on them will be available no later than the end of 2018. Since the studies 3.3 kV SiC MOSFETs are still at early stages of development (while the Si IGBTs already have a mature manufacturing technology), it is expected that improvement in SiC MOSFET technology will significantly impact the shown comparison results. A similar study can be done in near future using newest generation SiC MOSFETs of SEI to update the results. Also, according to the manufacturers 3.3 kV SiC MOSFETs will soon become available from Wolfspeed (Cree) and GE as well, which can be included in the new study.

Appendix A. Characterization and Comparison of Latest-Generation 900 V and 1.2 kV SiC MOSFETs

The device characterization reported in chapter 2 was started with lower-voltage SiC MOSFETs. Total of 6 SiC MOSFETs from four well-known manufacturers (Wolfspeed or Cree, Monolith Semiconductor, ROHM and Sumitomo Electric Industries) were characterized under similar conditions, where each device was state-of-the-art product of the corresponding company. Also, several of the devices were not yet commercialized at the time of performing the study.

A.1 Devices under Test

A total of six SiC MOSFETs are under test in this article. Table A.1 indicates the part number, nominal blocking voltage, continuous current rating (at room temperature), maximum operating junction temperature, the chip area as well as recommended gate-to-source driving voltages for all the devices. The 36 A device from Wolfspeed (marked as Wolfspeed #1) is packed in TO-220 package and the rest of the MOSFETs are in TO-247 packaging. Both Wolfspeed MOSFETs are rated at 900 V, while the rest of devices under test are rated for 1.2 kV. From structure point of view, the SiC MOSFET from SEI is a VMOSFET while the rest of the devices under test (DUTs) are DMOSFETs.

It does worth to mention that at the time of this research, except Wolfspeed *X3M0050090G* (marked as Wolfspeed #1) and ROHM *SCT3080KL*, the rest of SiC MOSFETs were not commercialized. The characteristics of the non-commercialized devices are extracted using samples provided to the Center for Power Electronics Systems (CPES) by the manufacturers.

Table A.1 Key Parameters of the devices under test.

Device	V_{DS} (V)	$I_{D,cont}$ (A)	T_{max} (°C)	Die Area (mm^2)	V_{GS} (V)
Wolfspeed #1 *X3M0050090G*	*900*	*36*	*150*	*7.56*	*-4/+15*
Wolfspeed #2 *C3M0010090D-ES*	*900*	*160*	*175*	*31.65*	*-4/+15*
ROHM *SCT3080KL*	*1200*	*31*	*175*	*7.75*	*-2/+18*
SEI *XSM3012J-ST01*	*1200*	*30*	*175*	*9*	*-5/+15*
Monolith #1 *MSA12N080A*	*1200*	*36*	*175*	*10*	*-5/+20*
Monolith #2 *MSA12N025A*	*1200*	*120*	*175*	*31*	*-5/+20*

A.2 Static Characterization

All the static characterizations are done by using B1505 curve tracer from Keysight Technologies. This process includes acquisition of output characteristic, transfer characteristic, threshold voltage, specific on-state resistance and junction capacitances for each of the devices. All of the mentioned characteristics except the parasitic junction capacitances are measured from room temperature up to 150 °C, since it has been shown in [69] that junction capacitances are temperature invariant. Based on variation of results with temperature change, an assessment can be made on temperature dependency of the static parameters. For high temperature measurements a hot plate is utilized and the device is mounted on it.

A.2.1 Output Characteristiscs

Figure A.1 shows the drain current I_D versus drain-to-source voltage of the MOSFET V_{DS} for all devices under test at 25 °C and 150 °C. Recommended driving voltages are fed to devices when capturing the output characteristics. From the output characteristic, an estimation of on-state resistances can be made. According to the figure, the Wolfspeed #2 semiconductor features the

smallest on-state resistance compared to the other devices while the ROHM semiconductor has the highest on-resistance.

The shown results reveal that as temperature increases, the on-state resistance increases. This is due to the fact that the JFET region resistance and drift layer resistance (which are the dominant resistances of SiC MOSFETs for a wide range of operating conditions except at low gate-to-source voltages) both increase as temperature increases. It does worth to mention at low gate voltages the channel resistance dominates the on-state resistance.

A.2.2 Transfer Characteristiscs

The transfer characteristic gives a measure of threshold voltages of the devices, as well as their gain at constant V_{DS}. Transfer characteristics of the MOSFETs at 20 V drain-to-source

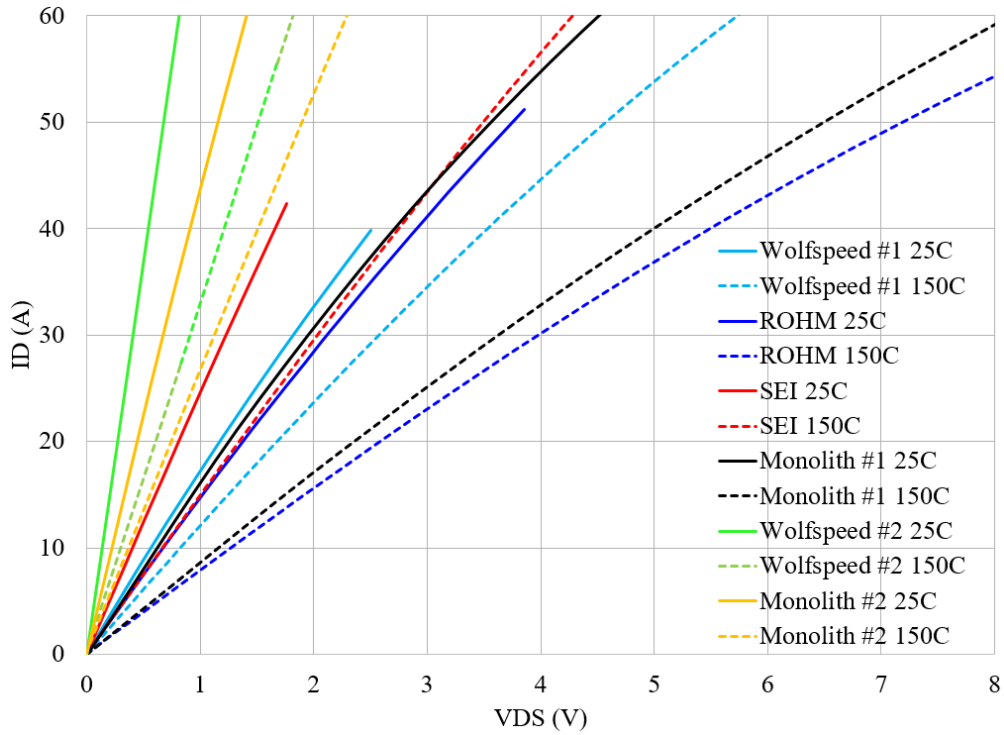


Figure A.1 Output characteristics of the device under test. To capture the output characteristics the recommended values of V_{GS} is applied to all devices.

voltage are shown in figure A.2 at room temperature as well as 150 °C. The positive temperature coefficient of transconductance (meaning that transconductance increases with increase in temperature) seen from figure A.2 is due to increase in the MOS channel inversion charge and inversion mobility as temperature increases. From this curve, smallest threshold voltage is expected from the Wolfspeed #2 MOSFET, while the ROHM semiconductor is featuring highest threshold gate-to-source voltage.

A.2.3 Specific On-State Resistance

The on-state resistances are measured for each of the MOSFETs at two temperatures. Then, the resistance results are normalized with respect to die size of the corresponding devices. This is important to do since for a given semiconductor technology, smaller die size results in a larger

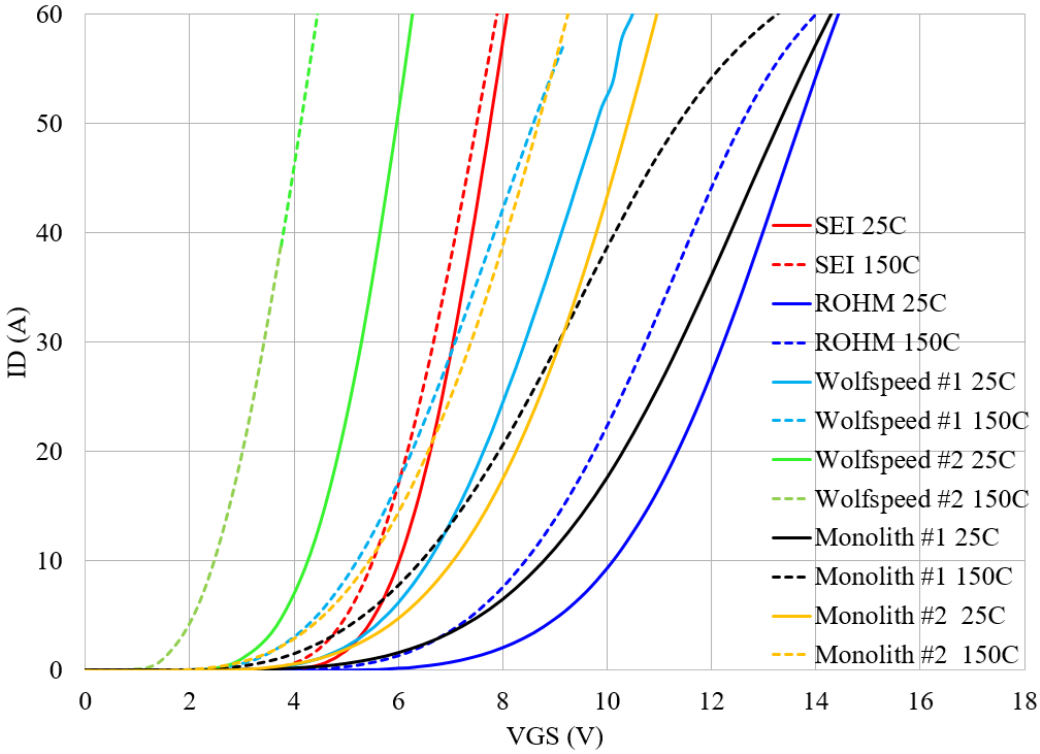


Figure A.2 Transfer characteristics of the devices under test. Drain-to-source voltage is set to 20 V when capturing the transfer characteristics.

resistance. Thus the appropriate way is to normalize the on-resistance with respect to die area and derive the degree of merit of semiconductors based on their die size. A part of the total die area should be used for edge termination as well as bonding pads, and the percentage of active area to the total die size varies for devices with different current rating. But since in this work the authors did not have access to active areas of all semiconductors, the calculation is done by using the total die area given in table A.1 in case of each device. However this will penalize the lower current rating devices more compared to the large current rating devices, since the percentage of active area in a small die is lower compared to a large die.

The specific on-state resistances versus drain current are shown in figure A.3 in $m\Omega \times cm^2$ for both room temperature (solid lines) and 150 °C (dashed lines). It is worth noting that in a similar way to output characteristic acquisition, here the recommended V_{GS} of the devices is applied to devices under test. As it can be seen, the SEI MOSFET proves to have the smallest specific on-state resistance with a value around than 3.6 $m\Omega \times cm^2$. Wolfspeed #2 MOSFET also has specific on-resistance smaller than 4 $m\Omega \times cm^2$ which indicates significant improvement compared to previous generations of SiC MOSFETs at similar voltage and current rating.

Change in on-resistance of SiC MOSFETs at 150 °C compared to 25 °C is typically about 50%. Compared to the typically larger than 100% temperature dependency of on-resistance in Si-based power MOSFETs, SiC MOSFETs will feature less change in conduction losses as temperature varies. It does worth to note that change in on-resistance from room temperature to 150 °C happens in a linear manner. Thus, interpolation of results can be used in order to derive the specific on-resistance at any given temperature.

A.2.4 Threshold Voltages

Figure A.4 demonstrates the plot of threshold voltages versus temperature for all SiC MOSFETs investigated. The threshold voltage in this study is defined as the voltage across gate and source of the MOSFET so 50 mA of drain current flows through drain, while V_{DS} is set to 20 V. The threshold voltage is measured for each of the MOSFETs at six different temperatures from 25 °C up to 150 °C in order to better assess its temperature dependency.

The Wolfspeed #2 MOSFET has the smallest threshold voltage which makes it more critical for it to be driven by negative voltage at turn-off state in order to prevent false switching. The negative temperature coefficient of threshold voltage for SiC MOSFETs is coming from increase in intrinsic carrier concentration with increased temperature. The SEI MOSFET which is a

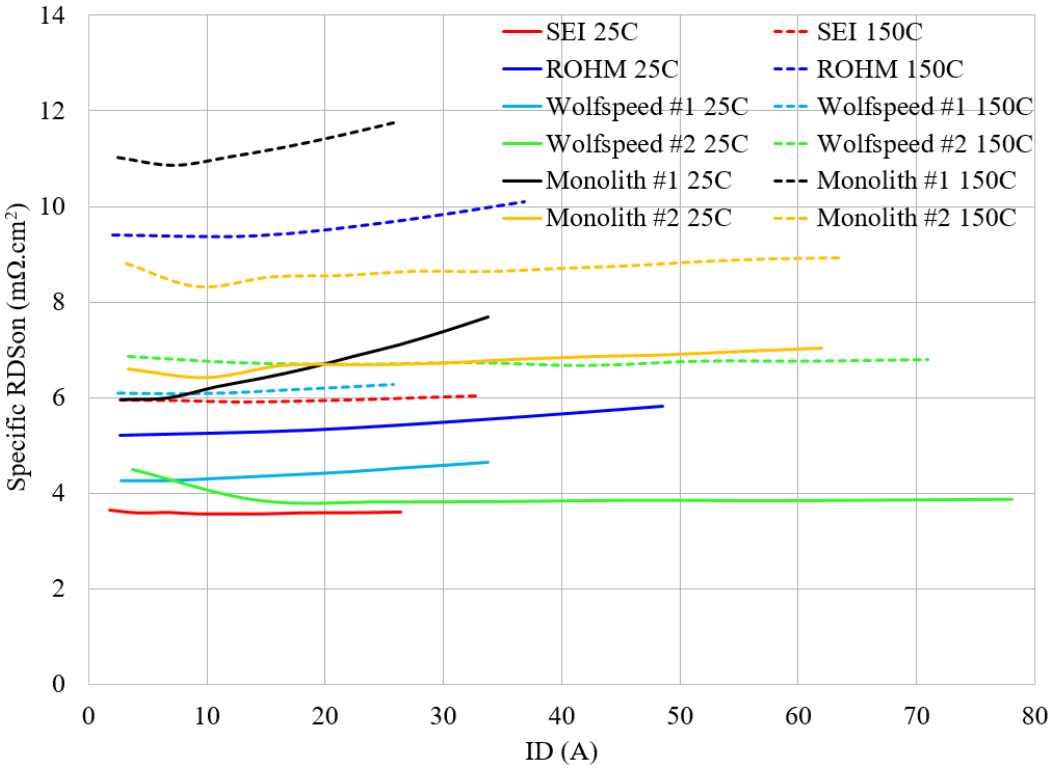


Figure A.3 Specific on-state resistances at 25°C and 150°C for all SiC MOSFETs under study while they were fed with their recommended gate voltages.

VMOSFET shows less dependency of threshold voltage versus temperature in comparison to the other devices which are DMOSFETs. The threshold voltage reduces approximately about 25% for Wolfspeed, ROHM and Monolith MOSFETs at 150 °C with respect to 25 °C while this change is only 12% for the SEI MOSFET.

It does worth to mention that sometimes in order to compare threshold voltage of devices with different current rating, the threshold current is scaled proportional to the nominal current rating of the devices. In such case, for instance the threshold current of Wolfspeed #2 MOSFET had to be increased compared to that of Wolfspeed #1, and then Wolfspeed #2 would feature similar threshold voltage as Wolfspeed #1. However, in this article the threshold current is set to a constant value for all devices under test regardless of their current rating.

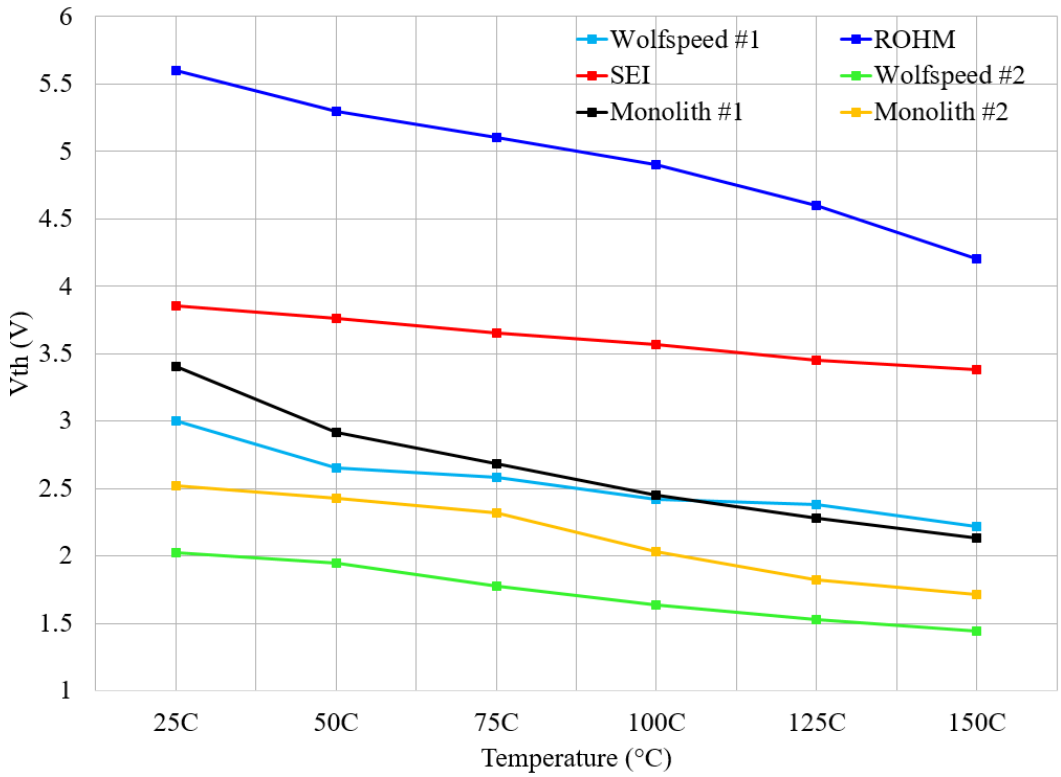


Figure A.4 Threshold voltages versus temperature from 25°C up to 150°C.

A.2.5 Junction Capacitances

The junction capacitances of all SiC MOSFET samples are measured under variant DC voltage up to 600 V at 100 kHz frequency. In this study measurement of the input capacitance C_{iss} ($=C_{GS}+C_{GD}$), output capacitance C_{oss} ($=C_{DS}+C_{GD}$) and Miller capacitance C_{rss} ($=C_{GD}$) are performed and the results are shown in figure A.5.

According to figure A.5, the input capacitance is the smallest for the Wolfspeed #1 and ROHM MOSFETs. The input capacitance together with the input gate resistance are the most important factors contributing to switching losses, thus the mentioned power MOSFETs will benefit from smaller input capacitance. From this point of view the Monolith #2 device has the highest capacitance which is primarily coming from its larger die due to higher current rating.

Regarding the output capacitance, the value is larger for the Wolfspeed #2 and Monolith #2 devices due to their higher current rating, while for the rest of the MOSFETs the output capacitance is similar. According to literature discharging and charging of the drain-to-source capacitance at turn-on and turn-off of the DUT will contribute to switching-on and switching-off losses, and will increase the turn-off losses and reduce the turn-on losses with the same magnitude. However, the total switching loss is free of this bias.

Last but not least, the miller capacitance is the least for Wolfspeed #1 MOSFET while the other devices have miller capacitances not far from each other. The miller capacitance is the main cause of miller effect and false turn-on when the devices are connected in phase-leg configuration.

Also this capacitance will contribute to slew rate of drain-to-source voltage and thus will affect the switching losses. Higher miller capacitance increases both turn-on and turn-off losses.

A.3 Test Circuit Design and Dynamic Characterization

In this section the designed dynamic test circuit together with protection and measurement methods used will be presented. The well-known double-pulse test (DPT) technique is used to extract dynamic behavior of the semiconductors under test and the overall schematic of the DPT circuit is shown in figure A.6(a). The top switch for testing the discrete MOSFETs is a schottky barrier diode. For SiC MOSFETs in 30-40 A current rating range, Cree *C4D10120* diode is used as the top switch. However, for larget-than-100 A SiC MOSFETs from Wolfspeed and Monolith, diode with part number *C4D20120* from Cree with higher current rating is utilized. Since in real

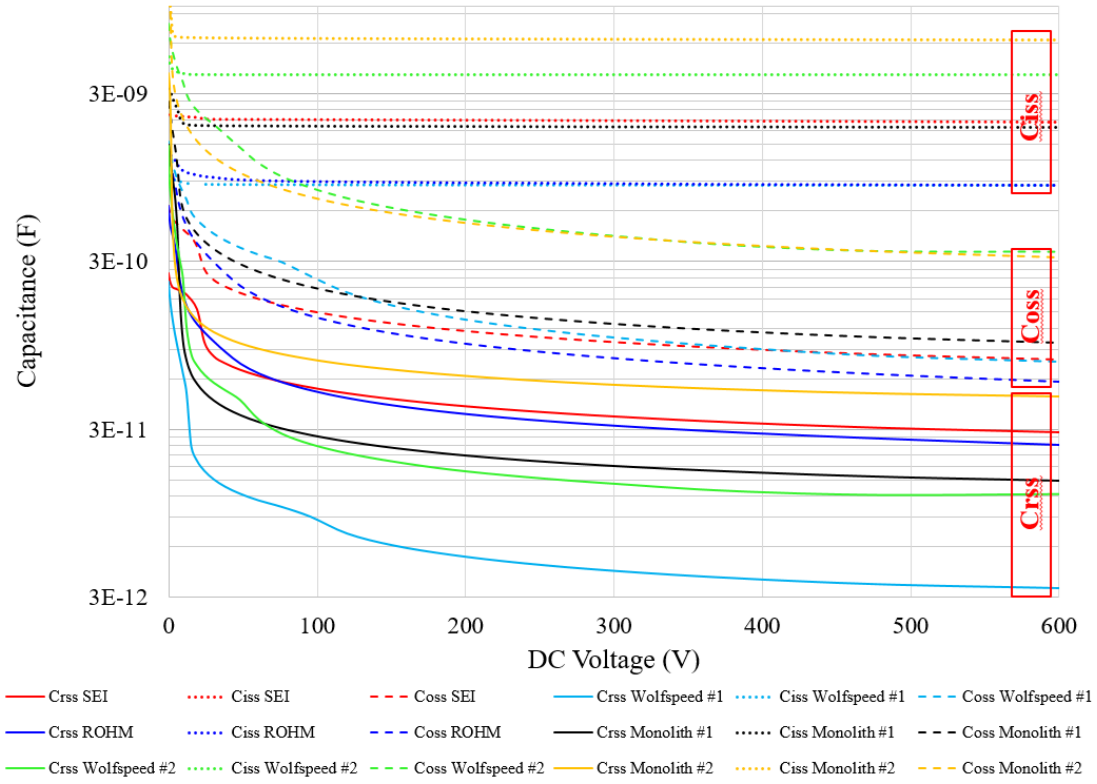
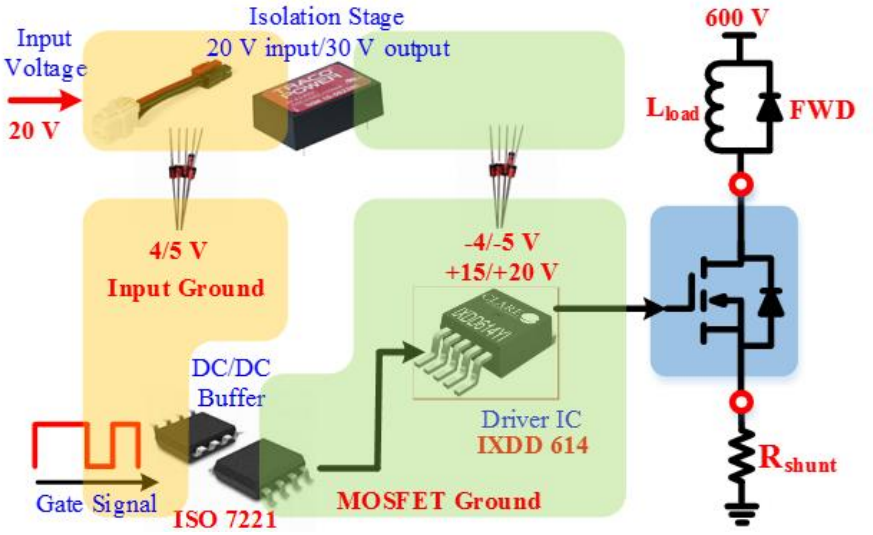


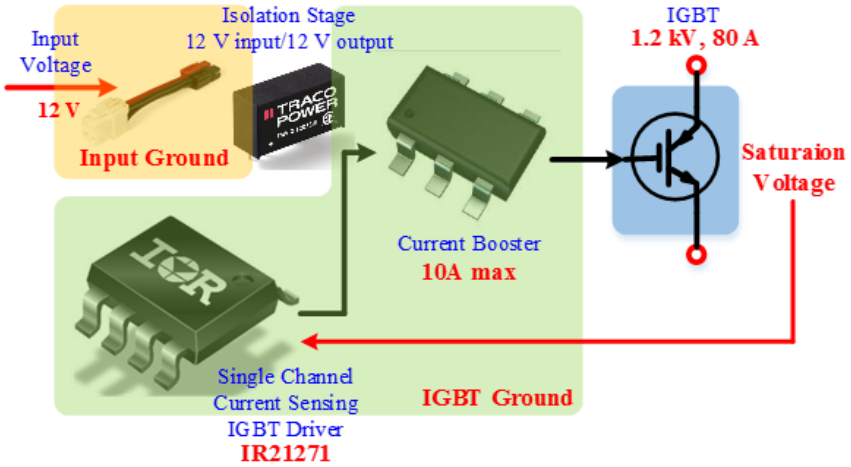
Figure A.5 Junction capacitances as a function of dc voltage measured at 100 kHz frequency.

applications, top switch current rating is selected proportional to current rating of the device, using different diodes does not introduce inequality in test condition for devices under test. An inductive load is used for testing the devices. The resistor in series with the switch is a current measurement shunt which is used to capture the drain current waveform.

Driving each device with its recommended gate-to-source voltage is one of the important aspects of providing equal condition for devices under test. In order to achieve this, the gate driver



(a)



(b)

Figure A.6 (a) Overall test circuit schematics and (b) IGBT DESAT protection.

circuit must be able of providing variable driving voltages. According to figure A.6(a), a combination of zener diodes and an isolated DC-DC power supply from Traco Power are used to provide the variable voltages needed. The gate signal is being created by Tektronix AFG3102 dual-channel function generator, and on the PCB it is being isolated and buffered via ISO 7221 optocoupler. The mentioned DC-DC buffer needs isolated supply voltages for primary and secondary sides, thus the primary side voltage is being generated directly from the input voltage using a zener diode.

The dc-dc converter of Traco Power has a 30 V output voltage (2×15 V in series). Summation of positive and negative gate voltages (for example 20 V for summation of 5- and 15 V in case of the SEI MOSFET) is created out of the 30 V DC-DC converter output by using a zener diode. Then using another zener diode stage, the resulting voltage (20 V in this example) is divided into positive and negative voltages (+15 V and -5 V with respect to device source in case of the SEI MOSFET). The gate driving voltages are biased and decoupled with four capacitors with magnitudes of 6.8 μF, 470 nF, 100 nF and 10 nF in closest proximity of the driver IC. Finally, IXDD614 high-speed high-current gate driver IC which can source or sink up to 14 A current is selected to be used in the gate driver circuit. The output stage of this IC is a PMOS-NMOS totem-pole with matched turn-on and turn-off resistances of around 0.16 Ω.

Like any other semiconductor, the devices under test are prone to failure especially under high-temperature dynamic tests. In order to protect the setup as well the oscilloscope channels from DUT's possible failure, an external IGBT desaturation overcurrent protection is utilized with the test system. Using external protection is due to the fact that different DUTs have different output characteristics. Also, it is shown that desaturation protection is not as effective on SiC

MOSFETs as it works for Si IGBTs [24]. The used IGBT has proper current rating and a current-sensing single-channel driver IC is used to drive it as shown in figure A.6(b).

The dc bus in double-pulse test is 600 V in case of all devices under test. In final design, four bulk capacitors are placed on the protection board in order to minimize stray inductances on power loop caused by the wires between power supply and the test setup. Placement of the bulk capacitors on the protection PCB rather than the double-pulse tester is because in case of failure on the tester board, the energy stored in capacitors itself can increase the inductor current in a considerable way and may take the inductor to saturation, causing damage the current shunt and the scope channel.

For decoupling purposes a combination of film and ceramic capacitors are placed on the DPT PCB. Three 100 nF 1 kVDC film capacitors as well as one 330 nF 1 kVDC film capacitor are placed for decoupling the 600 V DC bus. Also ten 100 nF 1 kVDC ceramic capacitors are placed in maximum proximity to the switch via planar connections, in order to provide better decoupling for the high-frequency components of switching current.

According to figure A.6(a), the load is a 1 mH inductor. The inductor EPC together with junction capacitance of the diode will contribute to the switching-on transient. For that reason it is of great importance to minimize the inductor EPC to minimum possible amount. In this work the designed inductor has about 14 pF of EPC which is negligible compared to junction capacitance of the diodes used.

Three SMD resistor slots are placed on the PCB for providing gate resistances and also to minimize gate loop inductance. Also an additional resistor slot is series connected with a diode in order to make the double-pulse tester capable of having separate turn-on and turn-off gate

resistances, in case of need. Since the *dv/dt* rates are expected to be high, when designing the board the common-mode immunity of the system is reinforced by using CM chokes with an impedance of 800 Ω at 100 MHz. Once the signal and power stages of the double-pulse tester were designed, the PCB was made. When designing the PCB repetitive Q3D simulations were done in order to minimize the gate and power loop inductances as well as parasitic capacitances. The achieved gate and power loop inductances on the designed PCB were measured to be around 4.3- and 9.8 nH, respectively. The designed PCB for the double-pulse tester is shown in figure A.7.

The waveforms resulting from double-pulse test are rich in high-frequency harmonics. Thus, accurate loss calculation requires utilization of high-bandwidth measurement methods for the waveforms. In this work a 100 mΩ shunt resistor with 2 GHz bandwidth is utilized in order to measure the drain current. For gate-to-source and drain-to-source voltages at the other hand, a low-voltage passive probe with 1 GHz bandwidth and the P5100 high-voltage probe of Tektronix with 250 MHz bandwidth are used, respectively.

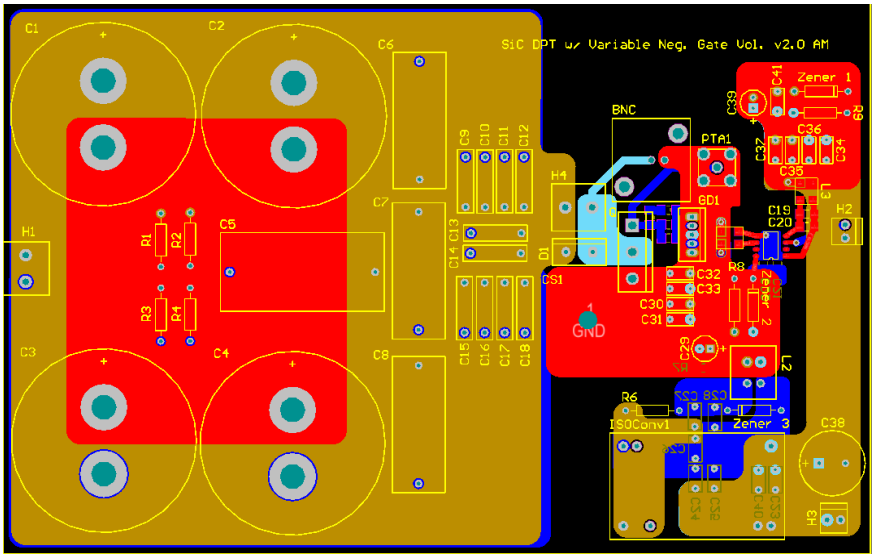


Figure A.7 Designed 4-layer PCB for double-pulse tester.

Table A.2 Internal, external and total gate resistances used in DPT.

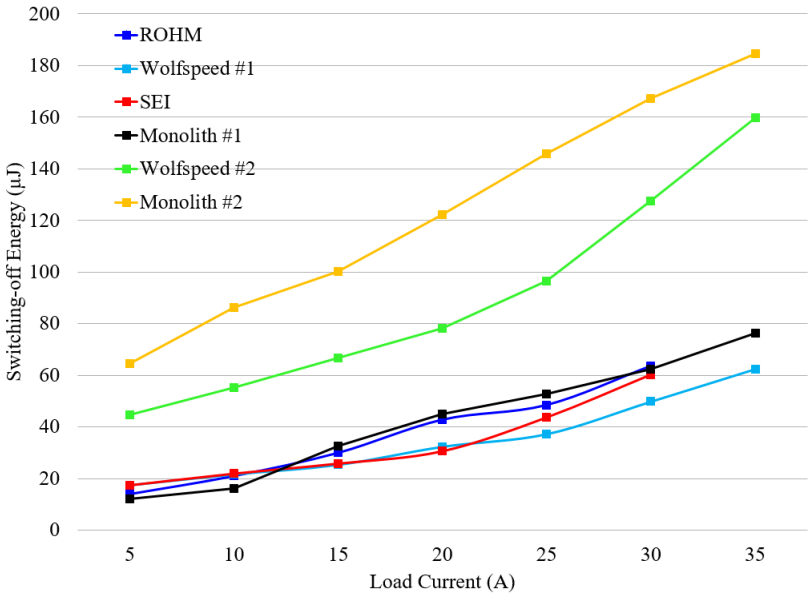
Device	$R_{g,int}$ (Ω)	$R_{g,ext}$ (Ω)	$R_{g,tot}$ (Ω)
Wolfspeed #1 *X3M0050090G*	*4.21*	*2.8*	*7.01*
Wolfspeed #2 *C3M0010090D-ES*	*2.03*	*3.1*	*5.13*
ROHM *SCT3080KL*	*12*	*0*	*12*
SEI *XSM3012J-ST01*	*4.04*	*2.3*	*6.34*
Monolith #1 *MSA12N080A*	*1.44*	*4.1*	*5.54*
Monolith #2 *MSA12N025A*	*0.78*	*4*	*4.78*

A.3.1 Room Temperature DPTs

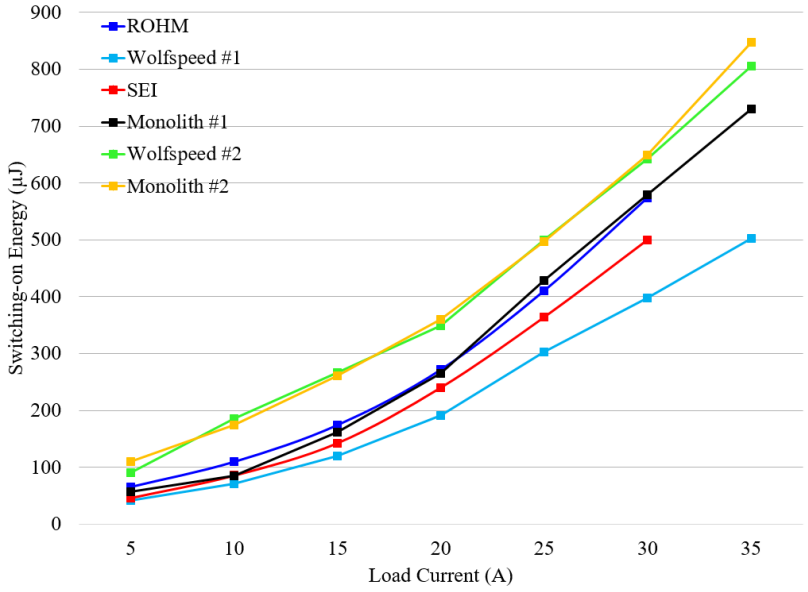
Having double-pulse test board prepared, the dynamic tests are done on all six devices under test. Table A.2 shows the internal gate resistance measured for each of the SiC MOSFETs using Agilent 4294A impedance analyzer while the drain and source terminals were isolated. The third column of the table is showing the external gate resistance selected in case of each device. The external gate resistances are selected to feature fastest switching speed for each of the devices before significant switching transients start to show up. It does worth to mention that the ROHM device has the largest internal gate resistance, and even by applying zero external gate resistance its switching transients are not as big as the other MOSFETs. Finally last column of table A.2 shows the total gate resistance in case of each MOSFET.

In case of each power MOSFET, the double-pulse test is done from 5 A load current up to device nominal current or 100 A, whichever happens first. For better resolution of dynamic test results at lower currents, figures A.8(a)-A.8(c) demonstrate switching-off, switching-on and total switching losses of all devices under test up to 35 A load current. Then, in figure A.9 the turn-off

and turn-on switching losses are shown for the Wolfspeed #2 and Monolith #2 power MOSFETs up to 100 A.



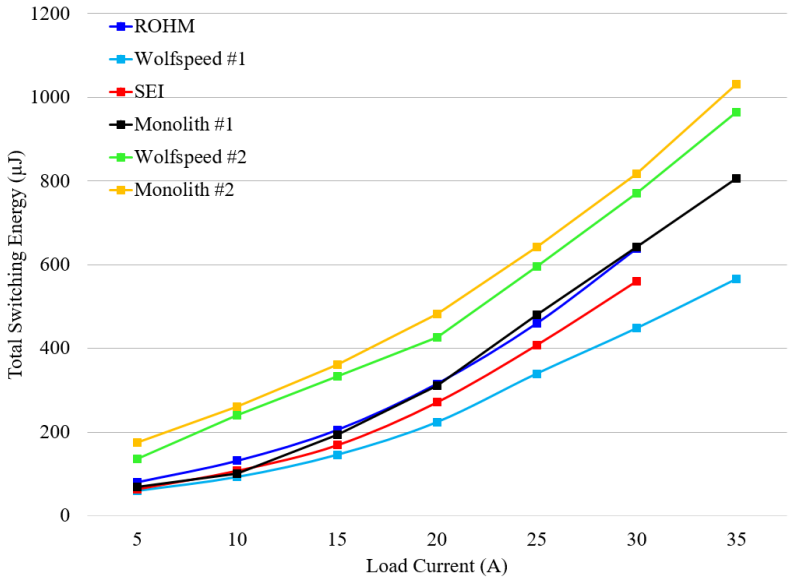
(a)



(b)

Figure A.8 (a) switching on and (b) switching off losses for all SiC MOSFETs using parameters shown in table A.2 and room temperature.

According to figure A.8, the Wolfspeed #1 MOSFET features the smallest switching losses among all devices under test at both turn-off and turn-on. This is mainly attributed to small input and miller capacitances of the Wolfspeed #1 device compared to the others, although it has a large (total) input gate resistance.



Continued: Figure A.8(c) Total switching loss for the SiC MOSFETs

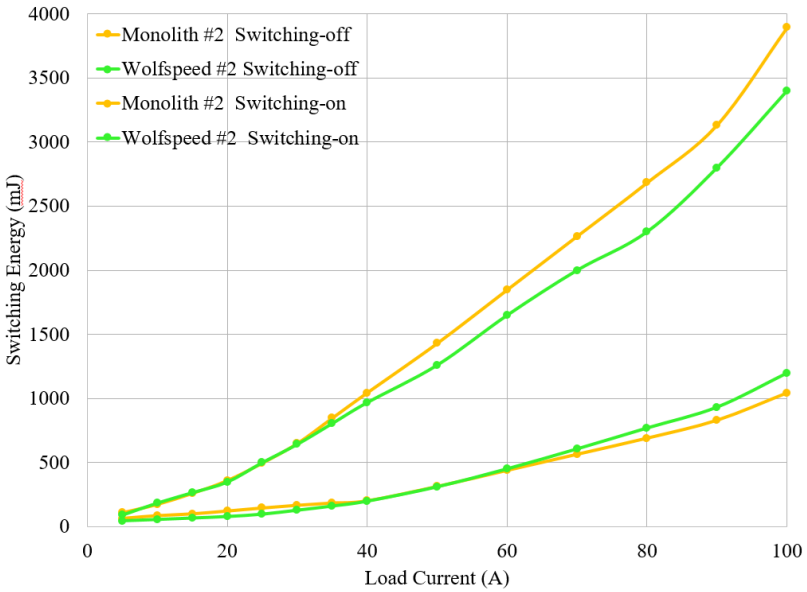


Figure A.9 switching on and switching off losses for Wolfspeed #2 and Monolith #2 SiC MOSFETs versus load current using parameters of table A.2 at room temperature.

On the other side, the Wolfspeed #2 and Monolith #2 power MOSFETs have larger switching losses, which is due to their larger current rating (larger die) resulting in larger parasitic capacitances. As mentioned before, larger parasitic capacitances slow down the switching transients of the device and increase the switching losses.

Although the ROHM semiconductor has input capacitance as small as the Wolfspeed #1 MOSFET, but its larger input gate resistance causes larger switching losses when compared to the Wolfspeed #1 case. The Monolith #1 power semiconductor features around the same switching losses as ROHM MOSFET since it has larger input capacitance but smaller gate resistance, and the turn-off and turn-on losses of the SEI MOSFET are larger than Wolfspeed #1 but smaller than the other devices.

Figures A.8 and A.9 reveal that the majority of switching losses in SiC MOSFETs is caused when switching on. Thus, by using soft switching methods and eliminating turn-on switching losses, total system efficiency can be significantly improved.

A.3.2 High-Temperature DPTs

In order to be able to test the device at high temperatures, a hot plate is used to heat up the DUT. Referring to figure A.10, the device is bent 90 degrees and mounted at the bottom of the PCB. In this way the DUT can touch the hot plate and heated up for high temperature tests. Also the device leads are as short as possible to minimize additional inductances in gate and power loops. A fan is used to cool down the PCB and the components on it, so they do not experience high temperatures when the device is being heated up to 200 °C.

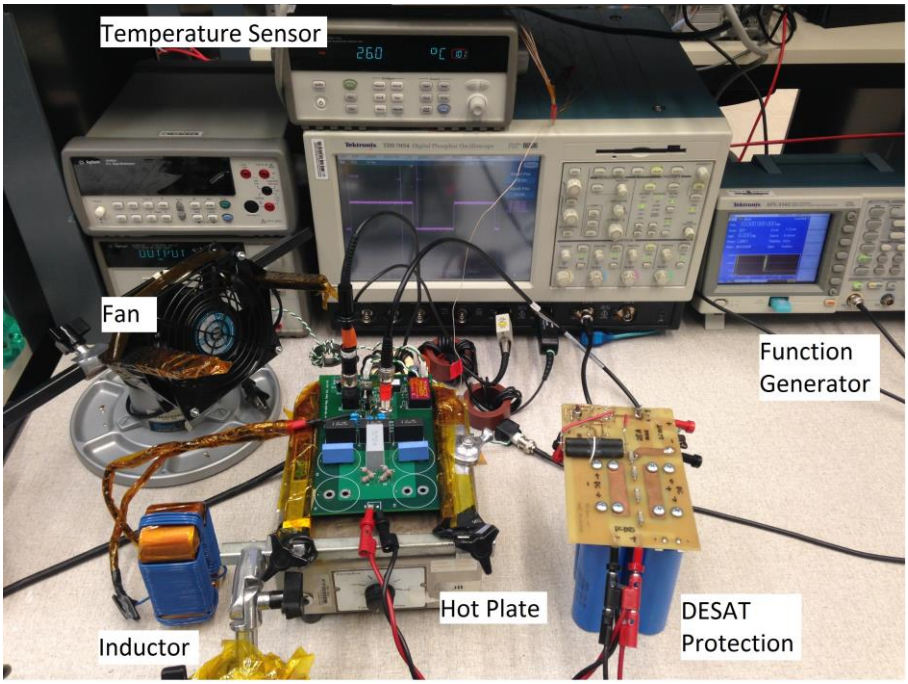


Figure A.10 Test setup for high-temperature double-pulse tests.

For high-temperature DPT, the hot plate needs to be isolated from the DUT. This is regarding the fact that normally case of the devices which is supposed to touch the hot plate is connected to drain, while the hot plate is grounded. A layer of Kapton tape is applied on the hot plate in order to provide isolation. For better thermal conductivity and also to create uni-temperature surfaces, a layer of thermal pad is applied both under and above the Kapton tape.

The high-temperature tests are done at three temperatures other than the room temperature: 100 °C, 150 °C and 200 °C. Although the devices under test are not capable of continuous operating at 200 °C, it is assumed that heating up the device to 200 °C for a short time and triggering it twice at that temperature cannot change device properties in a significant way. High temperature tests are performed at 5 A up to 20 A with steps of 5 A, and higher load currents are avoided for higher reliability and safety purposes.

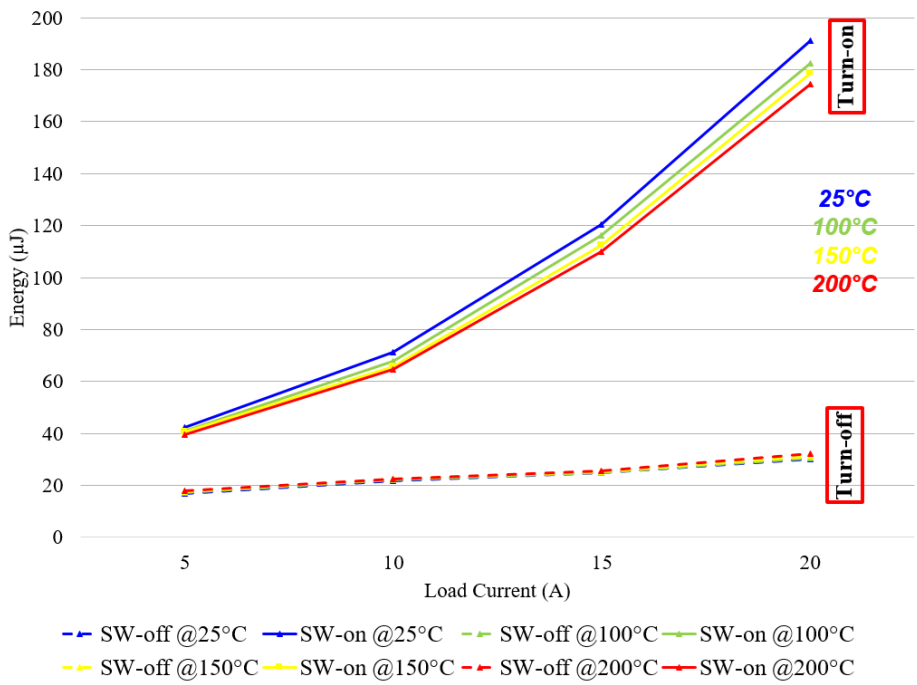
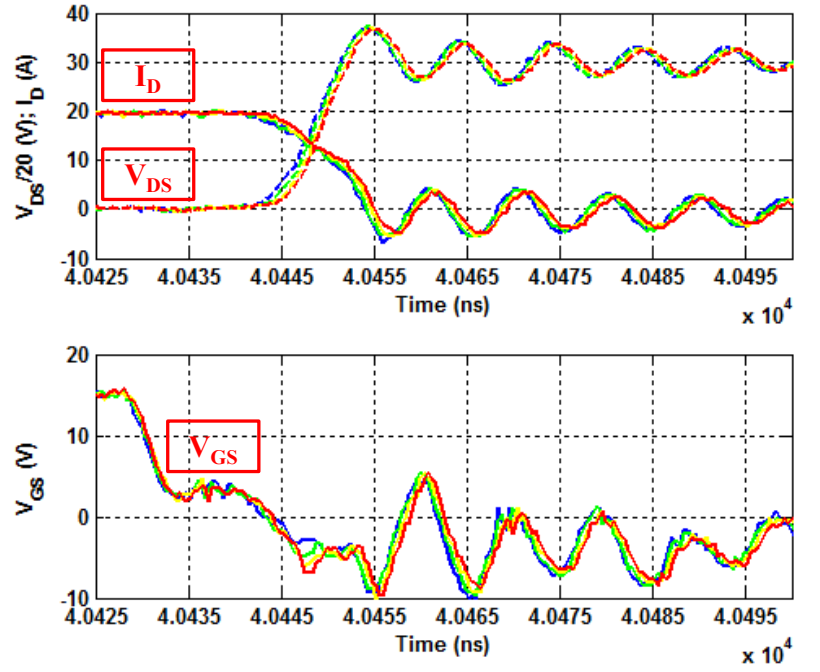
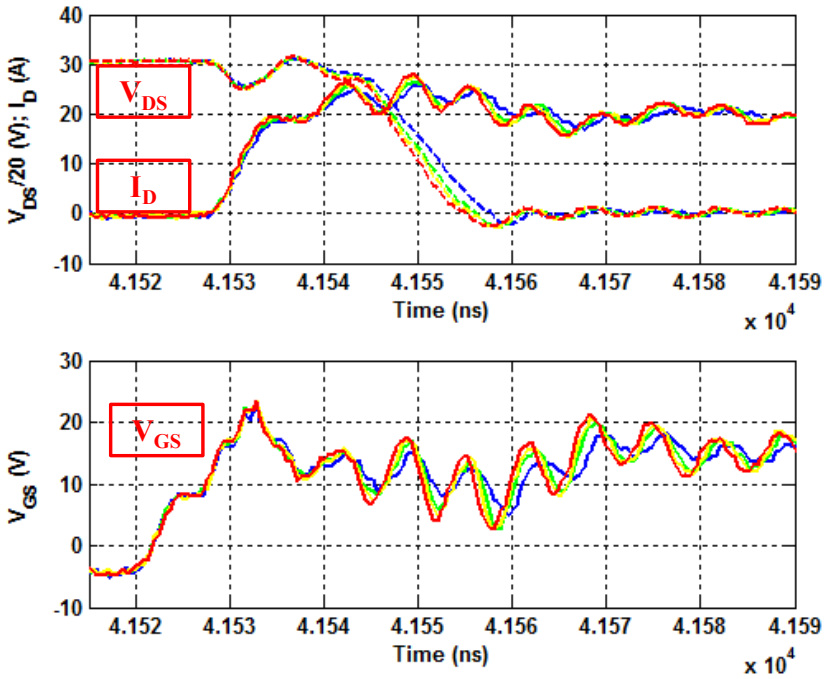


Figure A.11 Turn-on and turn-off switching losses versus junction temperature for the Wolfspeed X3M0050090G SiC MOSFETs under 25 °C (blue), 100 °C (green), 150 °C (yellow) and 200 °C (red).

High-temperature test results reveal that temperature dependency of switching losses is negligible for SiC MOSFETs, as an outstanding feature contributing to easier system design and more reliable operation. Figure A.11 shows for instance, switching-off and switching-on losses for the Wolfspeed #1 MOSFET as reference where total switching loss change at 200 °C compared to 25 °C is about 6%. Also as expected, the turn-off losses of SiC MOSFET increase and turn-on losses reduce as temperature increases. This is mainly due to reduction of plateau and threshold voltages as temperature increases, causing faster switching transients for turn-on case and slowing down turn-off process. Figure A.12 shows switching waveforms in case of Wolfspeed #1 DUT where effect of temperature on switching transients can be seen.



(a)



(b)

Figure A.12 (a) Switching-off and (b) Switching-on waveforms for Wolfspeed #1 MOSFET under 25 °C (blue), 100 °C (green), 150 °C (yellow) and 200 °C (red).

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