Weight Estimation of Electronic Power Conversion Systems

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ABSTRACT

Electronic power conversion systems with large number of power converters have a variety of applications, such as data center, electric vehicles and future smart "nanogrid" in residential home. Those systems could have very different architectures. For example, one system could be based on ac, dc or hybrid power distribution bus, and the bus voltage could be different. Also those systems have great need to develop low-cost architectures which reduce weight, increase efficiency and improve reliability of the system. However, how to evaluate different architectures and select a better one is still not clear.

This thesis presents a procedure to estimate weight of electronic power conversion systems, which provides an angle to evaluate different system architectures. This procedure has three steps. Step I, according to application of the system and system structure, determines the electrical and environmental specifications for each converter in the system. Step II studies the design procedures for each converter in the system and determines parameters such as the wire gauge and length of cable; the parameters of the passive components, such as inductance and capacitance; the parameters of the power switch, such as the voltage rating, current rating and loss; and parameters of the cooling system, such as the thermal resistance of the heat sink. Step III, according to the converters' parameters, carry out the physical design and selection of sub-components such as the inductor and heat sink to get the components' weight; the sum of those components' weight is the estimated system weight. This procedure has also been implemented in the form of software – system weight estimation tool. Using this software, weight of sample systems with ac dc bus and two different bus voltages have been estimated and compared.

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Chapter 1 Introduction

I. Scope and Motivation of this Work

This research estimates weight of electric power conversion systems using computer software. Today, more and more power electronic converters are penetrating electric power system which makes the system turning to be electronic. It was reported [1] that electronic power conversion system offers a high potential for cost saving, great improvement in system's efficiency, reliability, smaller size and lighter weight with continuous growth of system complexity. Fig. 1-1 shows the architecture of an electric power system composed of four main stages. The first stage represents electrical power sources. Electrical power can be generated from a battery or a high voltage storage system as in electric and hybrid-electric vehicles. It can also be a generator as in an aircraft power system, photovoltaic arrays for space station power system or future residential home 'nanogrid'[2]. Also, more and more systems begin to have multi-sources. The second stage is power bus which can be ac or dc with certain voltage. The third stage is made up of different power electronic converters in the form of ac-dc, dc-dc, dc-ac and ac-ac converters. The last stage is the load. The load can be electric machines, air-conditioning systems, electronics equipment and lighting loads.

Due to the size and complexity of most of these power systems, design of the system is still facing the following questions. The first one is how to select system structure [2]-[3]. A system could let the source power delivered to the load via ac bus or dc bus or a hybrid one. Which form is more beneficial is still not clear. The second question is how to select bus voltage. Industry is continuously seeking for higher bus voltage, but what is the impact of increasing bus voltage especially to power converters is not been well addressed. The third question is how to understand the impact of system design constraints to system design results. For example, when power quality of system changes, how the system will be changed. Also, is there an easy way to evaluate systems with different structures and other characteristics? Can we compare different system architecture to select a better one before carrying out detailed design? All these questions become the motivation of this study which is to develop a procedure to estimate weight of the

system can do comparison. This gives a very important aspect to evaluate different system architectures. Because power conversion system weight is very important for transportation application and also weight can be transfer to cost which is a very important attribution for any applications

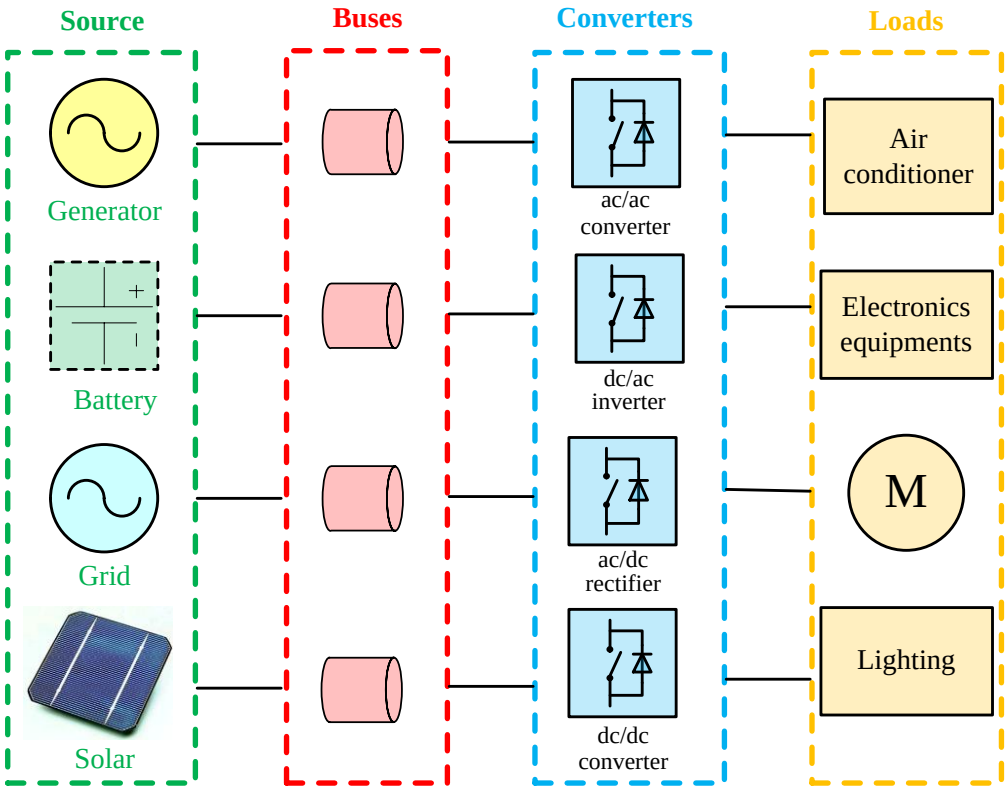

Fig. 1-1 Electronic power conversion system.

System components which have been studied includes bus feeder, source side and load side power converters. Design methodology and weight estimation of each component are studied. The procedure of design and weight estimation is realized using computer software which makes system structure comparison more easily.

II. Literature Review

A. Electronic Power Conversion System Design and Evaluation

Comparison and design of different electronic power conversion system have been discussed for a long time. Looking at the latest research, [2] discussed possible future ac and dc electronic

power conversion system architectures especially in the presence of renewable energy sources. Ideas for modeling, analysis and system-level design including power flow control, protection, stability and subsystem interaction are presented in [2]. Back to 1992, ac-bus and dc-bus based architectures have been discussed for telecom and mainframe computer applications in [4], and the integration issues related to paralleling and cascading of dc/dc converters have been explained. In 1994, K. K. Afridi discussed similar issues for automobiles [5]. P. Wheeler discussed the applications of power electronics converter in aircraft application, also different system structures have been mentioned [3]. In [6], design optimization of subsystems in a 270 V dc bus based modern aircraft power distribution system has been studied. Effort of [2]-[6] have been put on discussion of design, control and comparison of systems in electrical performance, there's no direct evaluation of weight has been addressed. Jie Chang discussed variable-frequency (VF) ac bus architecture for aircraft [7]. Evaluation of the system is based on cost index which is defined as the throughput of total kilowatts times the number of stages of power conversions from source. Based on cost index VF ac bus architecture is compared with conventional constant-frequency (CF) system. In 1998, K. K. Afridi evaluated several automotive electrical system architectures in terms of cost, weight and average power consumption [8]. Systems which Afridi had studied included only one or two converters in low power range. The models for estimation of system converters' cost weight and power loss are not based on detailed design but using linear approximation from commercial product data. His procedure is hard to be implemented to other applications and the models do not give deep insight of cost and weight distribution.

B. Power Converter Design and Weight Estimation

Weight of power converter gain special interest from transportation applications. In 2004, Cuzner evaluated the contribution of shipboard interface requirements to the total size and weight of a variable speed electric drive system by measuring weight of different commercial products [9]. Also in 2004, Busquets-Monge gave an automated design optimization approach of a 1.15 kW boost power factor correction (PFC) circuit [10]. In his study, PFC converter's weight and cost are evaluated, but, his procedure is based on very detailed design of each components. Database of converter sub-components such as inductor core, capacitor and heat sink are needed.

Approaches in [9] and [10] are good for comparison and discussion on a typical issue but they are not good methods which can be used in system level. Instead, a generic method of estimation power converters and other components' weight is preferred for system evaluation and comparison. This method should represent the essence of power converter's working principle and estimate its weight by study the physical structure and material of sub-components simple database can be used when it is necessary. There's no need to mention the enormous effort which had been devoted in the research of design power converters. While, the study of increasing, identifying and quantifying power density of converters gives the clue of realizing this method. A systematic methodology of topology evaluation has been introduced by Rixin Lai [11]. He discussed the design procedures of different three-phase ac-ac converters and compared them in term of weight. The work is dealing with one application but these procedures can be used for reference. T. Friedli also did similar work in 2010. He comprehensively compared three-phase ac-ac matrix converter and voltage dc-link back-to-back converter [12]. In his work volume and weight of inductor and capacitor has been estimated. Heldwein estimated the impact of electromagnetic compatibility (EMC) filter on the power density of three-phase sparse matrix converter and three-phase pulse width modulation (PWM) converter [13]. Drofenik described a procedure of design forced air cooling system. Converter power density limits for forced convection cooling has been discussed [14]. Cooling system performance index has been introduced which can be used to estimate forced air cooling system weight. Kolar investigated the volume of cooling system and main passive components for the basic forms of power electronics energy conversion in dependency of switching frequency [15]. Power density estimation has been done by scaling of cooling and passive components. The concepts and procedures in his study are valuable for this research.

In the study of Busquets-Monge, computer software has also been developed to make the design easy and fast [10]. Also, in Afridi's work, software is developed to evaluate and compare different automotive electrical power systems [16].

III. Objectives

The main objective of this research is to develop electronic power conversion system components weight estimation procedure and system level weight evaluation tool to compare systems with different structure and parameters. The weight estimation procedure and evaluation tool can be used for a variety of applications like automotive, ship spacecraft or aircraft. The research focused on investigating design and weight estimation procedure of power converters and other components used in the system such as bus cable and transformer. The main challenge is to have the proper procedure realized in computer software which makes it possible to be implemented in system architecture evaluation and comparison.

IV. Technical Approach

A typical electronic power conversion system consists of several cables, filters and power electronics converters. Estimation of system weight should consider system power level, voltage rating, power quality, electromagnetic interface (EMI), interface stability and environmental constraints such as temperature and altitude. The approach been used in this study has three steps. Step I, according to application of the system and system structure, determines the electrical and environmental specifications for each components in the system. Step II studies the design procedures for each component in the system and determines parameters such as the voltage, current rating of power device, inductance and capacitance of passive components and thermal resistance needed for cooling system. Step III, according to the component parameters, carry out physical design and selection of sub-components such as the inductor and heat sink to get the components' weight; the sum of those components' is the estimated system weight.

V. Thesis Outline and Summary of Contributions

Chapter 2 of the thesis discusses the design aspects of the major system components. Those system components including three-phase two-level PWM boost rectifier, three-phase three-level PWM Vienna rectifier, voltage source inverter, single-phase PFC, full bridge based dc-dc converter, autotransformer and bus cable. The design procedures are mainly learned from

literatures. Modifications and verification are made to make the procedure to be realizable in software.

Chapter 3 focuses on weight estimation of components. Weight of power converter consists of weight of power device, passive components (such as inductor, transformer and capacitor) and cooling system (heat sink and fan). Weight of power device is available from datasheet, so a small database of typical power device is formed. Inductor and transformer weight is estimated by doing detailed physical design; design procedure is discussed in this chapter. Capacitor weight is estimated by linear approximation of commercial product data. Physical design of forced air cooling system is used to estimate weight of heat sink and fan.

Chapter 4 describes the development of weight estimation tool. This tool is computer software written in MATLAB. It provides the ability to allow user enter system parameters and estimate weight of ac and dc bus based systems. By using this tool, sample system which is used in a data center is study. Weight estimation results for sample system using ac and dc bus and two different bus voltages are presented. Impact of increasing bus voltage on power converter is addressed.

Finally, chapter 5 states the main conclusions of this thesis in addition to some proposed future work. Design of typical power converter and components used in electronic power conversion system are studied. A weight estimation procedure for power converter and system is developed to evaluate the weight of system for different structure and parameters. Sample system with different structure and bus voltages are studied. Impact of rising bus voltage on power converters is discussed. Computer software is developed to make the weight estimation and evaluation easy to be carried out.

Chapter 2 System Components Design

I. Introduction – System Components Description

As illustrated in Fig. 2-1, one typical electronic power conversion system has multi-source and different ac and dc loads. Then, ac-ac, ac-dc, dc-ac and dc-dc converters are needed for power conversion. In this study, three-phase two-level PWM boost rectifier and three-phase three-level Vienna rectifier are selected. They are the most commonly used converters which serve the function of converting three-phase ac power to dc power. Both of them can be a front-end of motor drive. The first also has the re-generation ability can be used to generate voltage for a dc bus feeding multi-load. The second one does not have re-generation function but it can provide both positive and negative dc voltage. Single-phase power factor correction (PFC) circuit is widely used in single-phase application as the front-end of dc-dc converts. Voltage source inverter (VSI) is the most commonly used topology in motor drive. Finally a full-bridge base dc-dc converter is studied because it can be used to connect different dc buses or charge battery. Bus cable is also been studied.

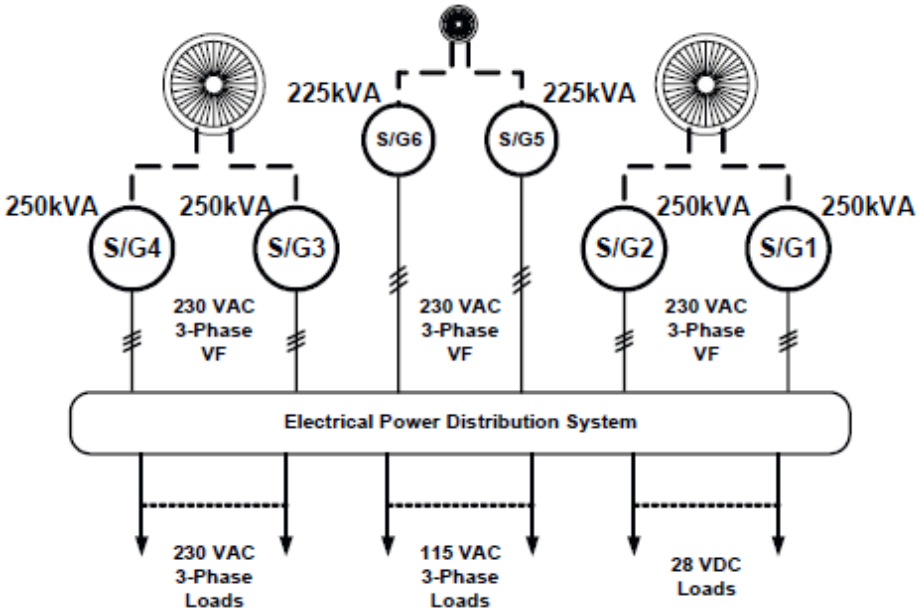

Fig. 2-1 Boeing 787 power distribution system[3].

II. Power Converter Design Procedure

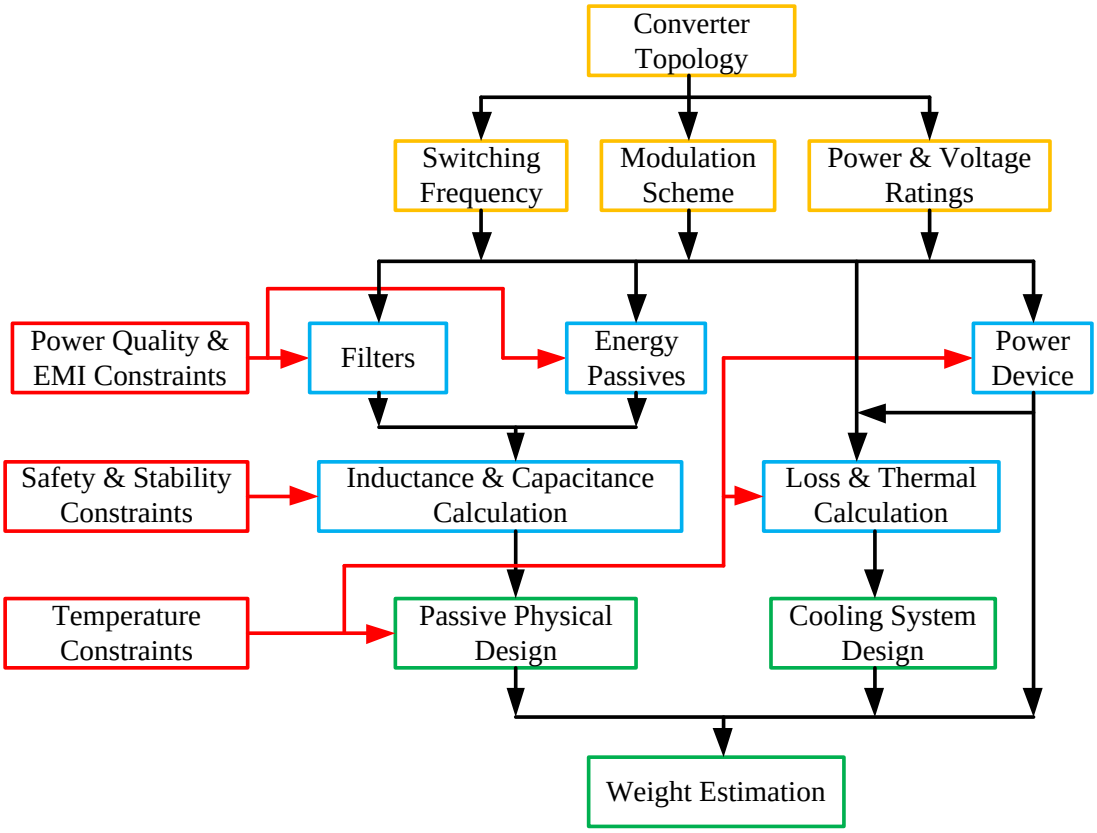

Fig. 2-2 Power converter design procedure.

The flowchart in Fig. 2-2 shows the power converter design procedure. For a given topology, the design input is switching frequency, modulation scheme, power and voltage ratings. First, power devices are selected according to the power and voltage rating, one can use IGBT or SiC devices. Second, for given switching frequency and modulation scheme according to power quality and EMI constraints input filter and energy passive components such as input inductor and output capacitor are designed. Third, according to interface stability and safety constraints, inductance and capacitance for passive components are calculated; according to temperature constraints power device loss and cooling system thermal resistance are calculated. Finally, the physical design is performed for each component, including the inductors, capacitors, power devices, and cooling systems. Converter weight is then evaluated by adding all the components' weight together.

III. Three-phase Two-level PWM Boost Rectifier

The schematic of three-phase two-level PWM boost rectifier is shown in Fig. 2-3. The design of this converter including design of input EMI filter (calculation of L_{cm}, L_{dm}, C_x and C_y), boost inductor L_{ac}, power stage, thermal resistance of heat sink and dc-link capacitor C_{dc}. The following discussion begins with design of power stage.

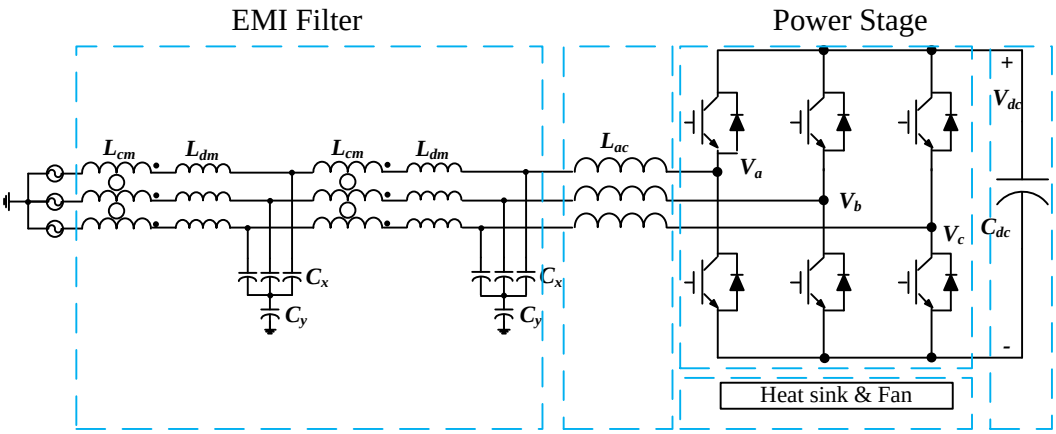

Fig. 2-3 Three-phase two-level PWM boost rectifier.

A. Power Stage Design

The working principle of PWM boost rectifier is can be explained using Fig. 2-4. By using PWM control, the full bridge generates PWM voltage (with magnitude of dc-link voltage V_{dc}) V_{ab} which fundamental signal is sinusoidal and has the same frequency as source voltage V_s. The input current i_s is controlled to be in phase with V_s.

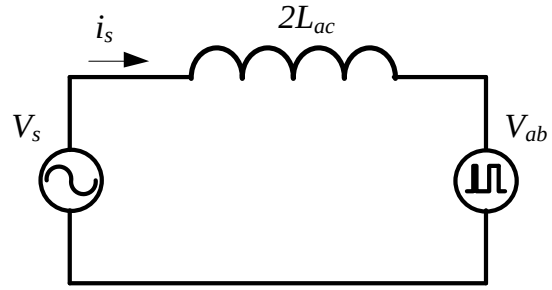

Fig. 2-4 Principle of three-phase two-level PWM boost rectifier.

Let M to be modulation index, which is defined as:

$$M = \frac{V_s}{V_{dc}} \tag{2.1}$$

Value of *M* should less than 1 which is essential the requirement of boost type converter and the typical value of are around 0.86 in order to give certain margin for transient.

i) Power Device Rating Selection

Voltage rating of power device is set to be around two times of dc-link voltage. And current rating is set to be around two times of input phase current root mean square (rms) value.

ii) Device Loss Model

Power loss of active switch including conduction loss turn on loss and turn off loss as shown in Fig. 2-5, when turn on signal of switch rises from low to high, voltage cross the switch falls and current through the switch goes up, the overlap of voltage and current generates turn power loss; when switch is on, it can be modeled as a on resistor series with a voltage source as shown in Fig. 2-7, current through this model generates conduction power loss; when turn on signal of falls from high to low, voltage cross the switch rises and current through the switch goes down, the overlap of voltage and current generates turn off power loss [17].

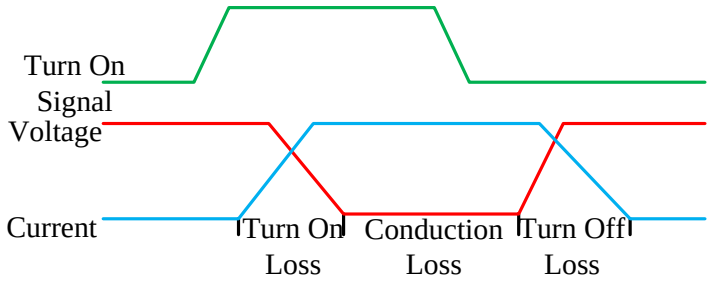

Fig. 2-5 Conduction, turn on and turn off loss of active switch.

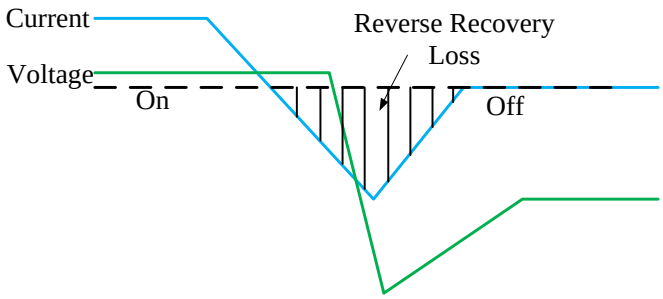

Fig. 2-6 Reverse recovery loss of diode.

When diode is turned off, the energy stored in the junction capacitor need to be released and this forced the current through diode goes to reverse direction for a short period of time when the reverse voltage cross the diode is building up as shown in Fig. 2-6. This overlap of current and voltage generates power loss.

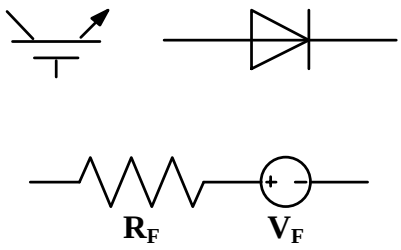

Fig. 2-7 Device on state model.

If we define the voltage cross power device during on state is u and the current through it is i, the relationship can be represented as:

$$u(t) = U_F + R_F \cdot i(t) \tag{2.2}$$

If the conduction time is t_{on}, then the energy E_{con} during device conduction period is:

$$E_{con} = \int_0^{t_{on}} u(t) \cdot i(t) dt \tag{2.3}$$

If we define tested turn on energy as E_{on_t} and the voltage and current of the device during test as U_t and I_t, turn on energy E_{on} can be represented as:

$$E_{on} = E_{on\_t} \frac{u \cdot i}{U_t \cdot I_t} \tag{2.4}$$

If we define tested turn off energy as E_{off_t}, turn off energy E_{off} is:

$$E_{off} = E_{off\_t} \frac{u \cdot i}{U_t \cdot I_t} \tag{2.5}$$

If we define tested diode revers recovery energy as E_{rr_t}, reverse recovery energy E_{rr} is:

$$E_{rr} = E_{rr\_t} \frac{u \cdot i}{U_t \cdot I_t} \tag{2.6}$$

Note that these relationships are all linear.

iii) Loss Calculation for Boost Rectifier

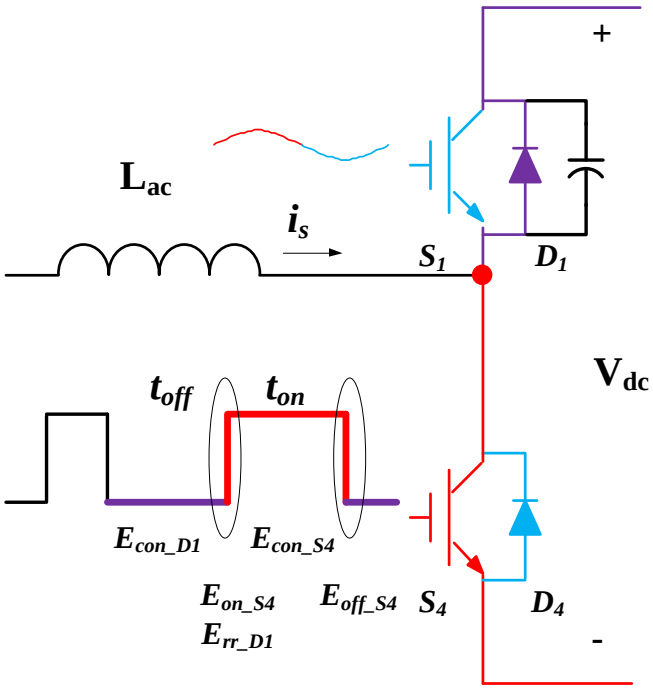

Fig. 2-8 Loss mechanism of boost rectifier in one switching cycle.

To illustrate the loss calculation mechanism of boost rectifier discussed in this section, Fig. 2-8 shows one phase-leg on and off status in one switching period when phase current is flowing from inductor to the middle point of phase leg. When switch S_1 is on and S_4 is off, current is flowing through diode D_1, which generates diode conduction energy E_{con_D1}; when S_1 is off, S_4 is on, current is flowing through S_4, which generates switch conduction loss; when S_4 is turning on

and D_1 is turning off, turn on energy is generated on S_4, reverse recovery energy is generated on D_1; when S_4 is turning off, turn off energy is generated on S_4. Because there's no current in S_1 so no loss is generated from S_1.

Modulation scheme sets the switching pattern of the power switch, and different patterns have different conduction and switching loss.

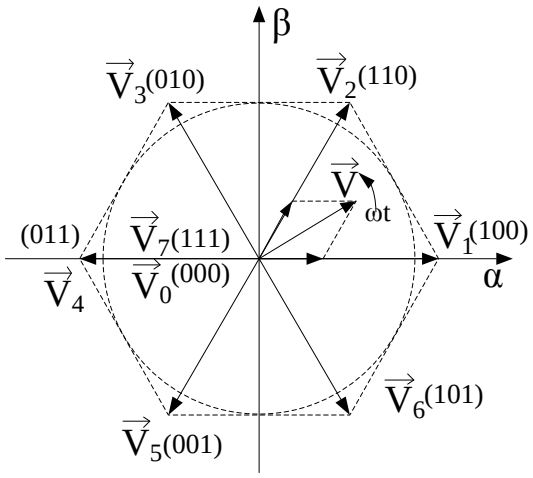

Fig. 2-9 Space vector modulation.

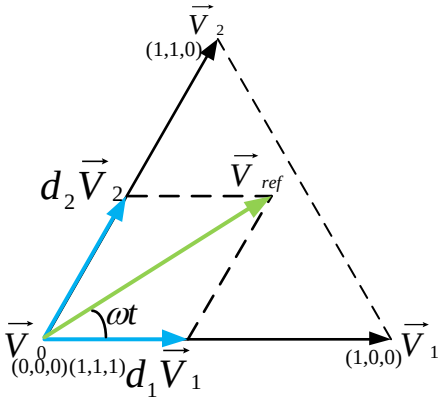

Fig. 2-10 Vector sysnthesis.

Fig. 2-9 and Fig. 2-10 show a diagram of space vector modulation and the vector synthesis. The reference voltage V_{ref} rotates through the $\alpha\beta$ coordinates. In order to synthesize the voltage vector, we first determine V_{ref}'s location in the six sectors hexagon, and then calculate the related duty cycles according to the angle between V_{ref} and the first vector of that sector. The duty cycles for each voltage vector in the first sector are given as:

$$\begin{cases} d_1 = \dfrac{V_m}{V_{dc}} \sin(60° - \phi) \\ d_2 = \dfrac{V_m}{V_{dc}} \sin\phi \\ d_0 = 1 - d_1 - d_2 \end{cases} \tag{2.7}$$

In (2.8), V_m is the amplitude of the target line-to-line voltage in the ABC coordinates, and d_1, d_2 and d_0 represent the duty cycles for V_1, V_2 and V_0, respectively. For the zero vectors V_0, we have two choices: [*111*] and [*000*] (*1* means that the top switch is on while *0* means the bottom switch is on). They have the same effect for the vector synthesis, so the same output voltage vector may be synthesized with different vector combinations and different placement of vectors. In particular, different placement of the zero vectors leads to different kinds of space vector modulation which lead to different power loss of power device. For detailed calculation of duty cycle for different modulation, one can refer to [18].

iv) Extract Loss Parameters from Device Datasheet

Usually, power device loss estimation is using loss related parameters in device datasheet. Datasheet provide tested turn on energy loss per pulse (E_{on_t} in Fig. 2-11) as well as turn off and diode revers recovery energy (E_{off_t} and E_{rr_t} in Fig. 2-11). Also datasheet indicted the test condition I_t and U_t.

Einschaltverlustenergie pro Puls turn-on energy loss per pulse	I_C = 50 A, V_{CE} = 600 V, L_S = 30 nH V_{GE} = ±15 V, di/dt = 1300 A/µs (T_{vj}=150°C) R_{Gon} = 15 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{on}	E_{on_t}	4,50 6,50 7,50	mJ mJ mJ
Abschaltverlustenergie pro Puls turn-off energy loss per pulse	I_C = 50 A, V_{CE} = 600 V, L_S = 30 nH V_{GE} = ±15 V, du/dt = 3800 V/µs (T_{vj}=150°C) R_{Goff} = 15 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{off}	E_{off_t}	2,50 4,00 4,50	mJ mJ mJ
Abschaltenergie pro Puls reverse recovery energy	I_F = 50 A, - di_F/dt = 1300 A/µs (T_{vj}=150°C) V_R = 600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{rec}	E_{rr_t}	2,00 3,20 3,60	mJ mJ mJ

I_t U_t

Fig. 2-11 Find turn on turn off and reverse recovery energy data from datasheet.

Device on linear approximation model can be also extracted from datasheet as shown in Fig. 2-12 and Fig. 2-13.

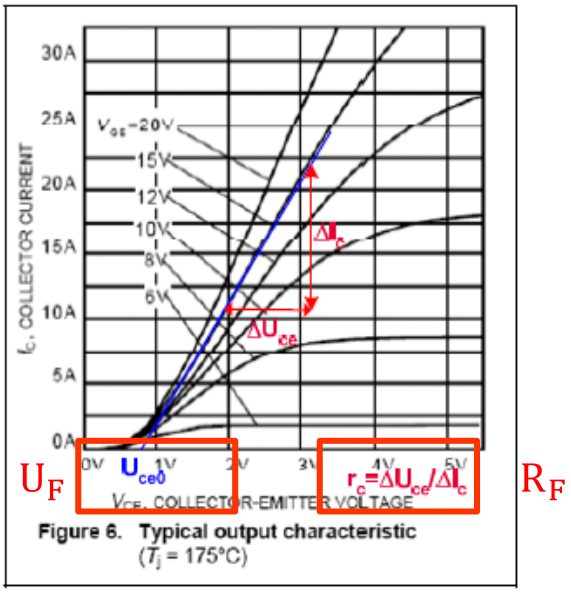

Fig. 2-12 Find linear approximation of IGBT forward voltage and on resistance.

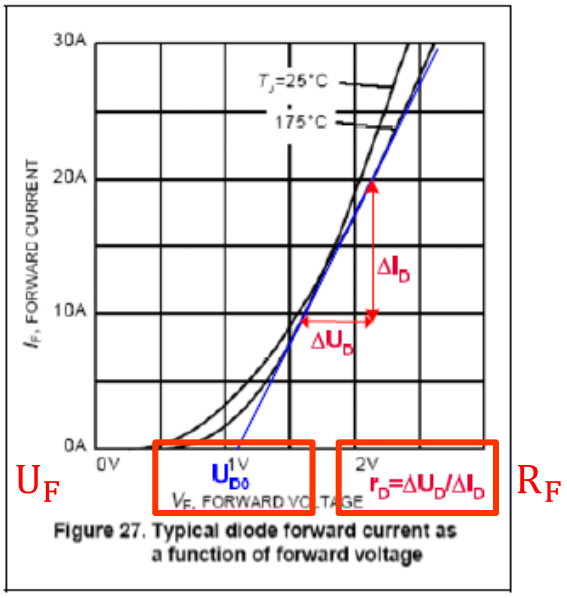

Fig. 2-13 Find linear approximation of diode forward voltage and on resistance.

B. Thermal Calculation

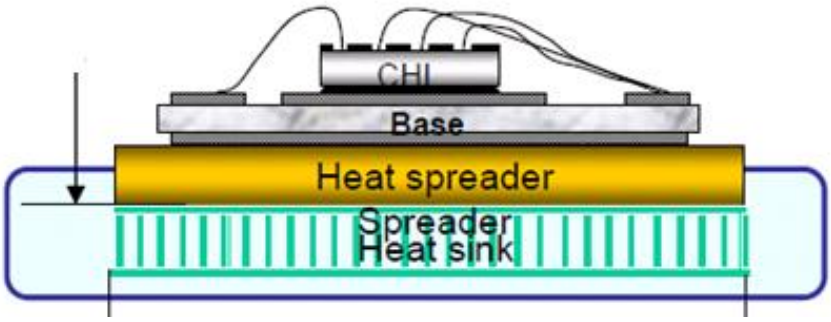

Fig. 2-14 Device loss spread mechanism.

To calculate the thermal resistance of the heat sink, a 1-D equivalent thermal model, consisting of equivalent thermal resistance of device package, heat sink, and other thermal interface materials, should be sufficient. Fig. 2-14 illustrate the thermal path of typical device. Fig. 2-15 shows the equivalent circuit of this thermal path.

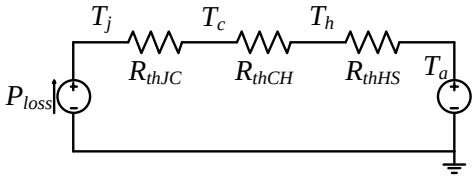

Fig. 2-15 1-Dimensional thermal model.

In Fig. 2-15, P_{loss} is the power loss generated by the die, R_{thJC} is the thermal resistance from junction to case, R_{thCH} represents the thermal resistance of the insulation pad, R_{thHS} is the thermal resistance of heat sink to the air, and T_a is the ambient temperature, T_j is the device junction temperature T_c is the case temperature, T_h is heat sink temperature.

In this work it is assumed that the temperature is uniform for the whole heat sink, and that the temperature T_h of the heat sink is chosen to guarantee that the junction temperature of each device mounted on it will not exceed its physical limit. This relationship is given by

$$T_j = P_{loss} \cdot (R_{thJC} + R_{thCH}) + T_h \le T_{limit} \qquad (2.8)$$

P_{loss} is power losses from the device, respectively; and T_{limit} is the upper limit for the operating temperature for that device. With the upper limit for the device, an acceptable heat sink temperature may be readily found.

The required thermal resistance for the heat sink is given by

$$R_{thHS} = (T_h - T_a) / P_{loss} \tag{2.9}$$

Extract Thermal Parameters from Datasheet as shown in Fig. 2-16.

Innerer Wärmewiderstand thermal resistance, junction to case	pro Diode / per diode	R_{thJC}			0,31	K/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,13		K/W

Fig. 2-16 Find device thermal resistance from datasheet.

C. Boost Inductor Design

The design of the boost inductor considers: 1) harmonics; 2) instantaneous current peak; 3) EMI; and 4) inrush current.

In our design procedure, the circuit and modulation are assumed to be symmetrical. Ideally there will not be any low-frequency harmonics except the switching ripple and the related side band. But if the switching frequency is so low that the switching harmonics directly enter the frequency range of the power quality (PQ) standard, an additional large filter is required to damp the switching ripple to meet the requirement. This is true for any high-power application in which the switching frequency cannot be higher than the PQ standard range. But for low power, we should select a switching frequency higher than the PQ standard range.

Since the phase-leg voltage harmonic is the source of current ripple, we determine the required boost inductance with the result of the spectrum analysis and the corresponding harmonic requirement for a given switching frequency. For the two-stage input filter structure, the relationship between the current harmonic and the filter parameters is given by:

$$I_h = \frac{u_h}{\omega L \left| 2 - \omega^2 LC \right|} \tag{2.10}$$

In addition to the harmonics requirement, the instantaneous current peak should be limited within a reasonable range to guarantee the proper control and protection of the circuit.

An inductor current ripple is affected by the switching patern. Fig. 2-17 shows the current ripple of a boost inductor in one switching cycle for discontinuous SVM, Fig. 2-18 shows the

diagram and equation for calculation of the ripple, and Fig. 2-19 gives the results for one line cycle. Along with the fundamental value, the total inductor current is shown in Fig. 2-20, and the inductance is selected to let the ripple peak-to-peak value reach half of the fundamental peak value.

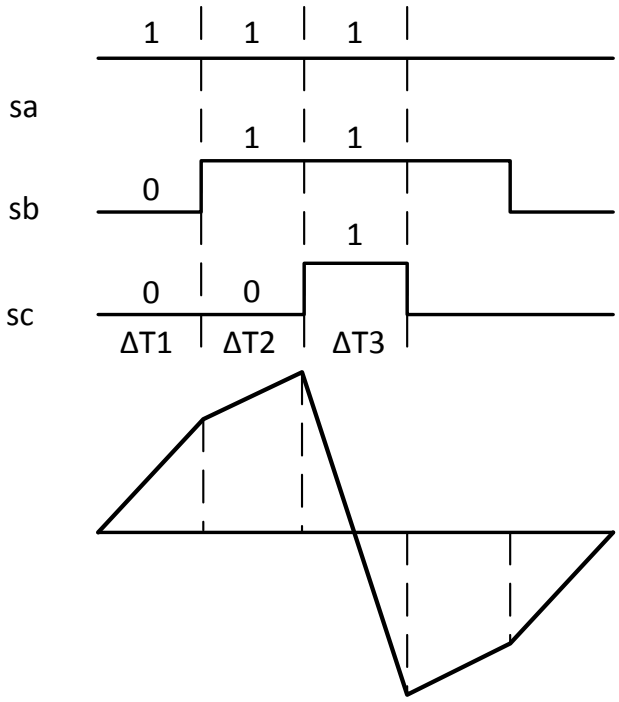

Fig. 2-17 Boost inductor current ripple in one switching cycle.

$$\Delta i = \frac{v_L}{L}\Delta t \tag{2.11}$$

$$v_L = v_{AO} - v_{aN} - v_{NO} \tag{2.12}$$

$$v_{AO} = s_a \cdot V_{dc} \tag{2.13}$$

$$v_{NO} = \frac{s_a + s_b + s_c}{3} V_{dc} \tag{2.14}$$

$$L = \left(1 - \frac{3}{4} M\right) \frac{V_{ac\_p}}{f_{sw} I_{rpp}} \tag{2.15}$$

$$L = \frac{1}{2}\left(1 - \frac{3}{4} M\right) \frac{V_{ac\_p}}{f_{sw} I_{rpp}} \tag{2.16}$$

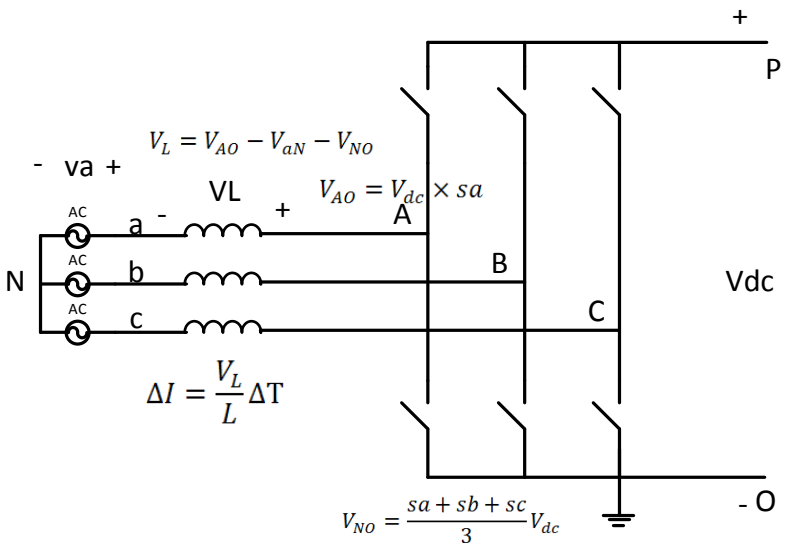

Fig. 2-18 Calculation of boost inductor current ripple.

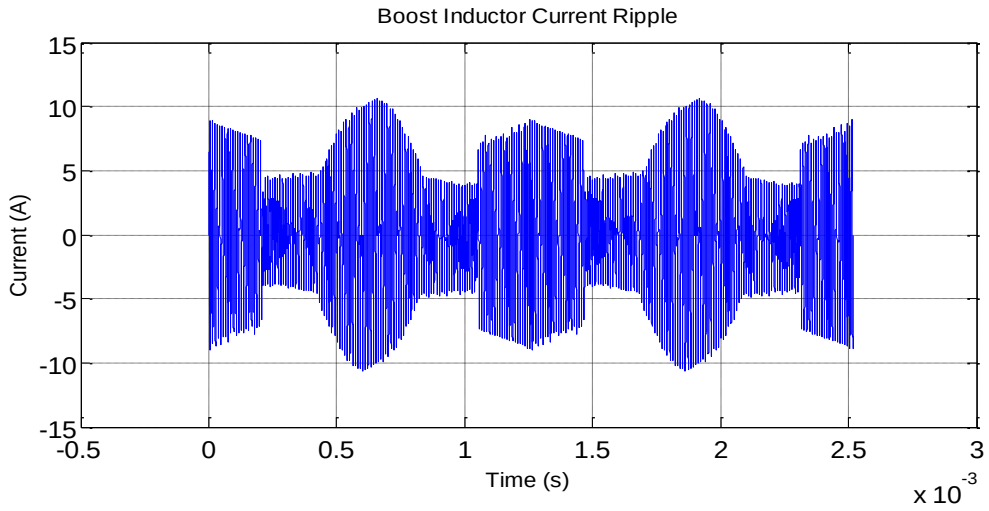

Fig. 2-19 Boost inductor current ripple.

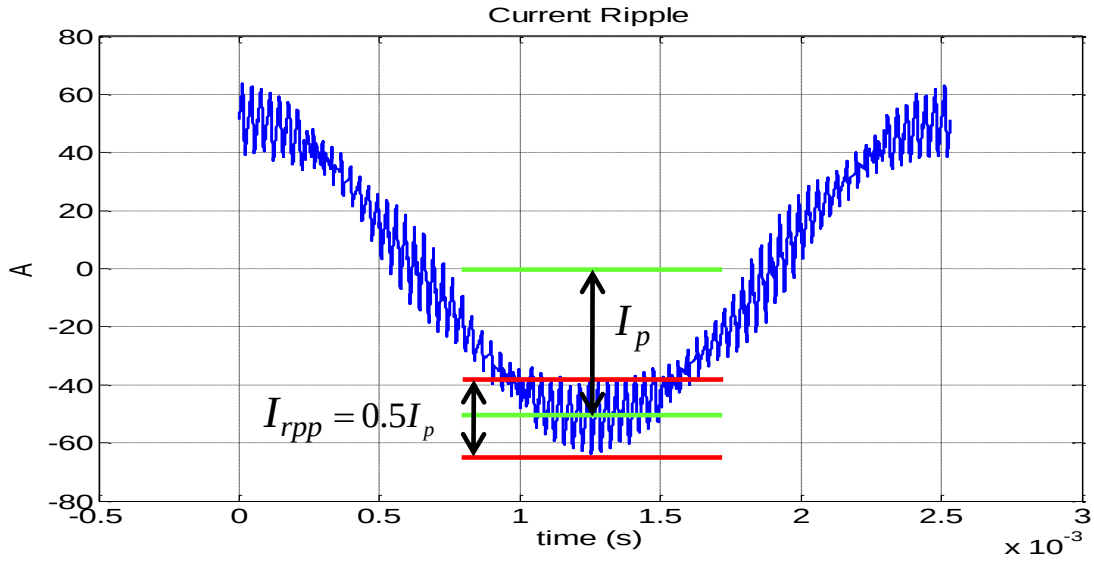

Fig. 2-20 Boost inductor current.

D. Dc-link Capacitor Design

A dc-link capacitor is utilized to maintain the dc-link voltage for robustness and operation requirements. In the back-to-back VSI, this capacitor can be minimized if the rectifier is controlled fast enough to match the inverter power consumption at all times. In addition, the lower limit of the capacitance can be investigated in terms of energy storage [19]. In this report,

only the extreme cases are considered for simplicity. We assume the controller does not work properly in one switching cycle, so the rectifier input power is zero while the inverter output power reaches its maximum. The relationship between the capacitance and the voltage dip is given by:

$$C = \frac{P_{\max}}{(U_0 \Delta U - \frac{1}{2}\Delta U^2) f_s} \tag{2.17}$$

Where f_s is the switching frequency, U_0 is the dc-link voltage, and ΔU denotes the dc-link voltage dip. The permissible voltage dip can be determined by the operation requirement. For example, the dc-link voltage of a boost rectifier cannot be lower than the peak line-to-line voltage for normal operation.

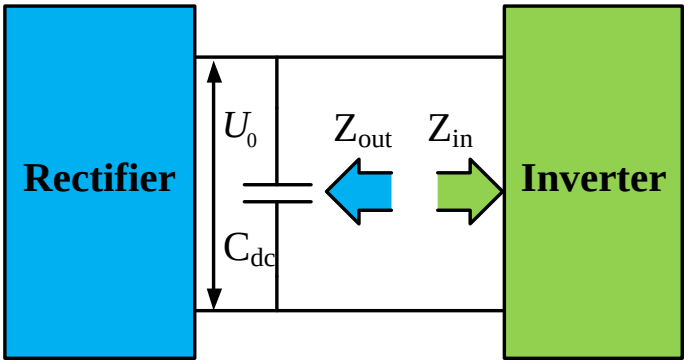

Fig. 2-21 Cascaded subsystems of rectifier and inverter.

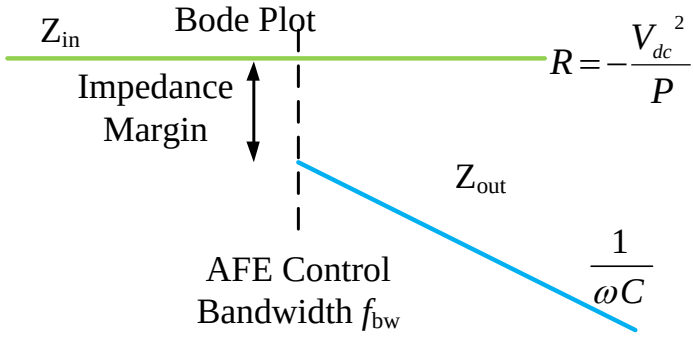

Fig. 2-22 Inverter input impedance and rectifier output impedance.

If the rectifier delivers maximum input power without any output power, we can obtain

$$C = \frac{P_{\max}}{(U_0 \Delta U + \frac{1}{2}\Delta U^2) f_s} \tag{2.18}$$

ΔU is the voltage rise. The voltage rate of the switching device is usually a constraint for the peak voltage rise.

Another consideration for the dc-link capacitor is the system stability. The rectifier and the inverter are two cascaded subsystems, as shown in Fig. 2-21. In order to avoid interaction between the two systems, the output impedance of the rectifier should be lower than the input impedance of the inverter [20]. The inverter can be considered as a constant power load. For VSI, its input impedance can be given by:

$$R = -\frac{V_{dc}^{\ 2}}{P} \tag{2.19}$$

P and V_{dc} indicate the power of the inverter and the dc link voltage, respectively. Fig. 2-22 illustrates the impedance relationship in a bode plot. We assume that the output impedance is very low in the control bandwidth and that the dc link capacitor is dominant outside the bandwidth. Then the constraint for dc link capacitance is given by

$$20\lg(-R) - 20\lg(\frac{1}{2\pi f_{BW} C}) \geq Z_m \tag{2.20}$$

f_{BW} is the control bandwidth, and Z_m is the impedance margin. Then we can decide the minimum capacitance using the equations above and the specific system requirements.

E. Input EMI Filter Design

The front-end system with a line impedance stabilization network (LISN) is shown in Fig. 2-22. All commercial motor drives are required to meet the EMI standard in a wide frequency range to guarantee the stability and reliability of the whole system. For the input filter design, we mainly focus on the RF conducted emission, which ranges from 150 kHz to 30 MHz [21].

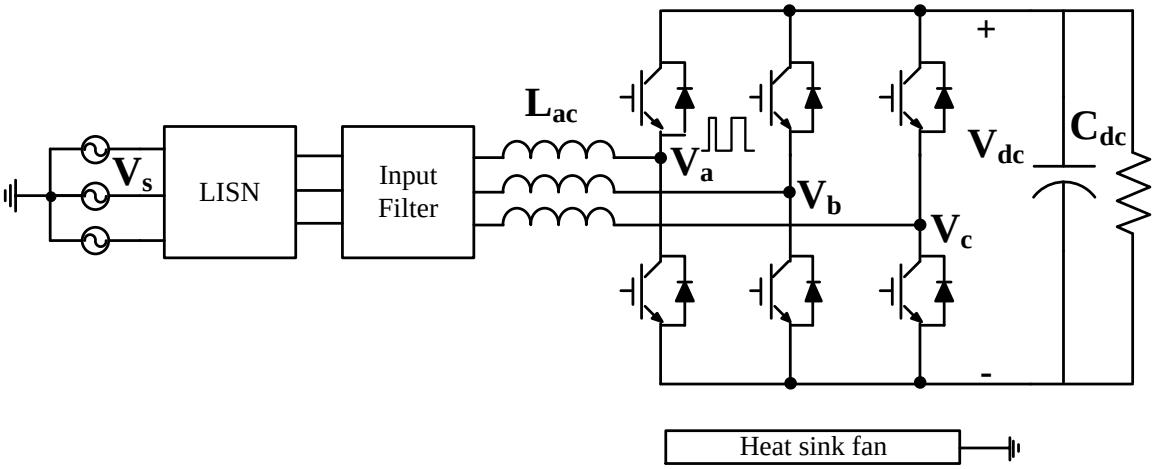

Fig. 2-23 Three-phase two-level boost rectifier with LISN and input filter.

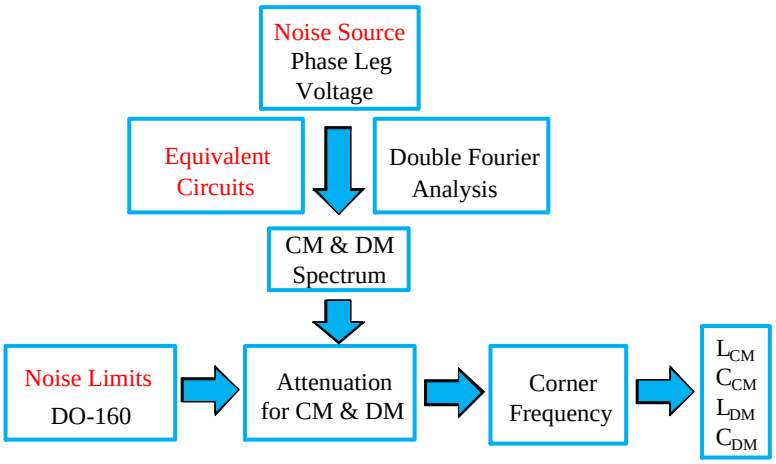

Fig. 2-24 EMI filter design procedure.

In order to design a filter to meet this requirement, design procedure as shown in Fig. 2-24 is used [22]. First, we need to identify the noise source, in three-phase PWM EMI nose is generated by pulsating phase-leg voltage [13]. Different modulation scheme leads to different phase-leg voltage harmonic spectrums. Double Fourier Integral Transform (DFIT) is applied to determine the harmonic spectrum of phase-leg voltage. This procedure is easy to be implemented in computer program [11] [18].

Using DFIT, harmonic components can be expressed in the following complex form [18]:

$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{y_r}^{y_f}\int_{x_r}^{x_f} V_{dc} e^{j(m\omega_s t + n\omega_0 t)} d(\omega_s t) d(\omega_0 t) \tag{2.21}$$

In (2.21), V_{dc} is the voltage across the dc link, ω_s is the switching frequency, and ω_0 is the fundamental frequency. The outer integral limit y_f and y_r together with the inner integral limit x_f and x_r are determined by the modulation scheme.

Two kinds of space vector modulations schemes are addressed in this section: center-aligned continuous modulation (SVM) and center-aligned discontinuous modulation (DPWM). Based on the data in [18], the phase-leg voltage spectrum of phase a phase-leg voltage V_a can be obtained for both modulation schemes. The spectrums of phase b and phase c can be directly achieved by phase-shifting phase a by 120 ° and 240 °, respectively. We can take a 10 kW converter as an example; the input voltage is 230 V/400 Hz, the dc link voltage is 650 V, and the switching frequency is 20 kHz. The spectrum with SVM is shown in Fig. 2-25 and Fig. 2-26 for DPWM.

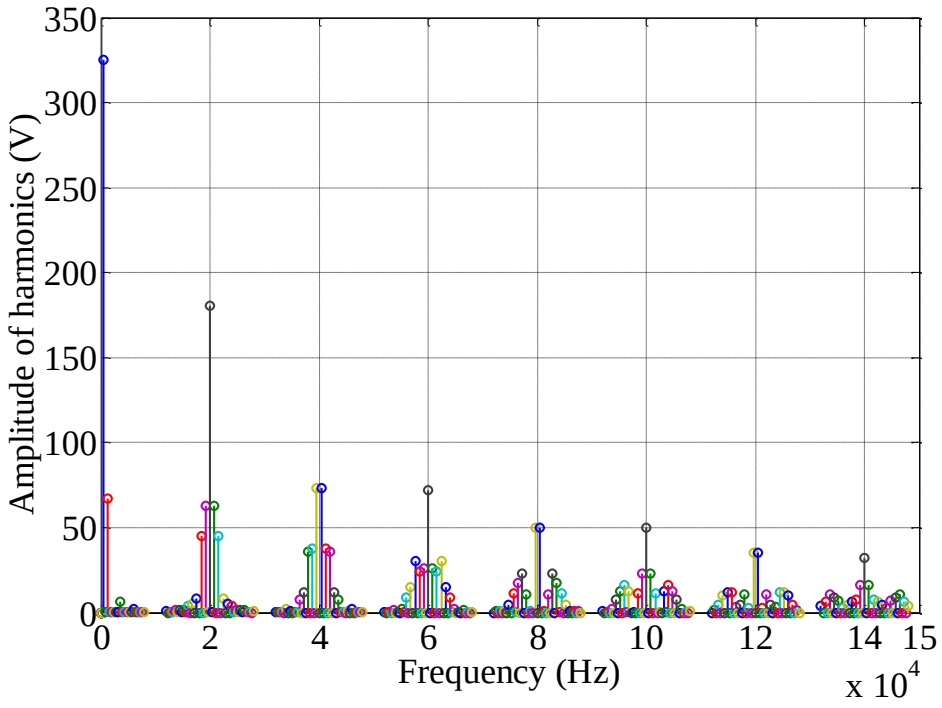

Fig. 2-25 Spectrum of phase a voltage for SVM.

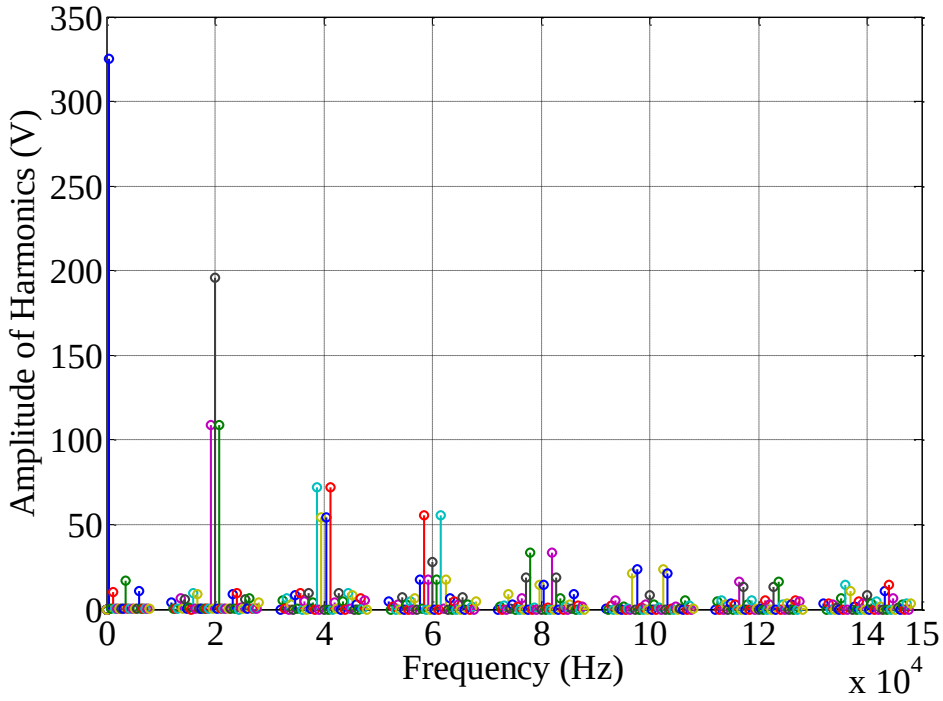

Fig. 2-26 Spectrum of phase a voltage for DPWM.

For the ideal symmetrical three-phase system, the same frequency harmonic components for each phase are either in phase or are in 120° phase shift with each other. The in-phase components form the common-mode (CM) voltage across the dc-link neutral point and the input source ground, while the phase-shift components form the differential-mode (DM) voltage source. They are given by:

$$V_{CM} = \frac{V_a + V_b + V_c}{3}$$
$$V_{DM} = V_{(a,b,c)} - V_{CM} \tag{2.22}$$

V_a, V_b and V_c are the phase-leg voltages. Then the spectrum for both the DM noise source and CM noise source are calculated using DFIT. Fig. 2-27 shows the spectrum of DM voltage; Fig. 2-28 shows the spectrum of CM voltage. The calculation parameters are the same as of Fig. 2-25 and Fig. 2-26. The calculation results are compared with simulation results, although the magnitude has some error but the calculation algorithm captures the same critical frequency point for EMI filter design.

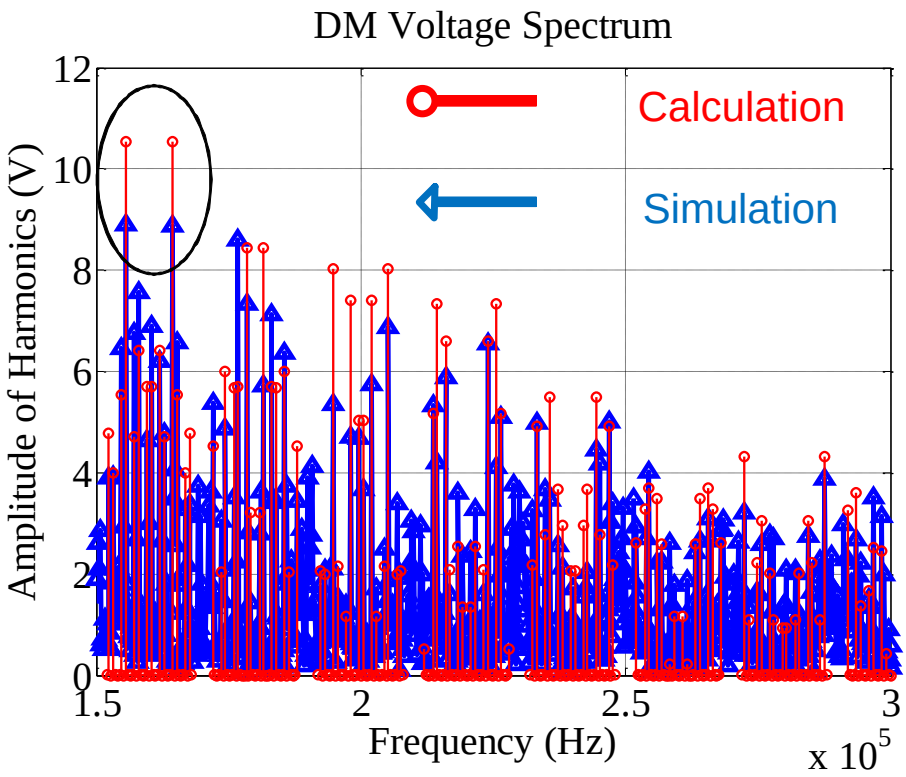

Fig. 2-27 DM voltage spectrum comparison.

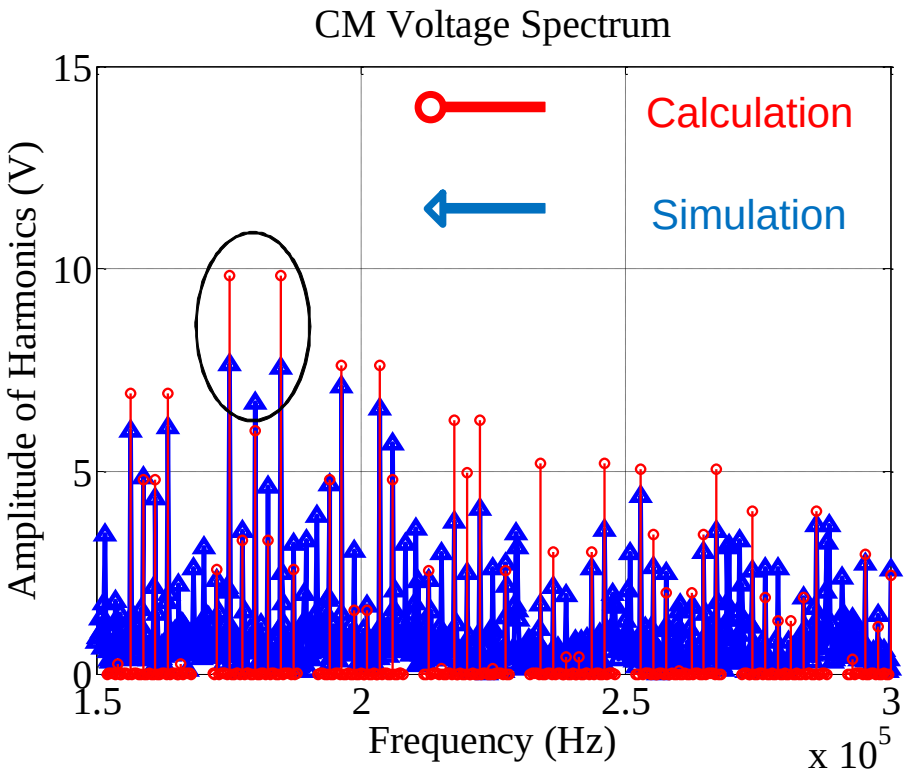

Fig. 2-28 CM voltage spectrum comparison.

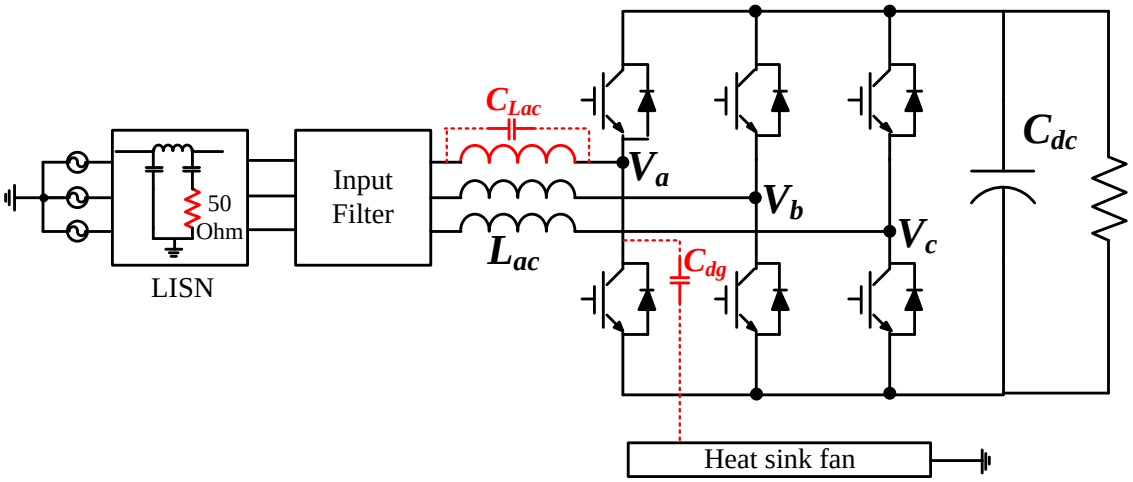

Fig. 2-29 Important parasitic in the EMI path of boost rectifier.

Circuit parasitic is the key components in the noise path. In Fig. 2-29, two most important parasitic are shown. One is the capacitor from device collector to heat sink (which is grounded) C_{dg} which is the most important CM noise path. The other is boost inductor (L_{ac}) self-capacitor C_{Lac}, through this capacitor, high frequency noise can propagate to source side.

In order to estimate EMI noise, C_{dg} and C_{Lac} need to be modeled. As shown in Fig. 2-29, C_{dg} is the capacitor between power devices we assume this capacitance is infinite big which can be considered as short in the EMI standard frequency range. This assumption essentially wants to consider the worst case for CM noise estimation. Boost inductor self-capacitor can be estimated by consider the turn-to-turn and turn-to-core capacitor. As shown in Fig. 2-30, C_{tt} is the turn-to-turn capacitor, the self-capacitance of inductor which has winding bigger than 10 turns is [23]:

$$C_s = 1.366 C_{tt} \tag{2.23}$$

And C_{tt} is:

$$C_{tt} = \varepsilon_0 l_t \frac{2\varepsilon_r \arctan\left[\dfrac{(-1+\sqrt{3})\left(2\varepsilon_r + \ln\dfrac{D_o}{D_c}\right)}{\left(1+\sqrt{3}\right)\sqrt{\ln\dfrac{D_o}{D_c}\left(2\varepsilon_r + \ln\dfrac{D_o}{D_c}\right)}}\right]}{\sqrt{2\varepsilon_r \ln\dfrac{D_o}{D_c} + \left(\ln\dfrac{D_o}{D_c}\right)^2}} \tag{2.24}$$

In (2.24), ε_0 is the vacuum permittivity. ε_r is the relative permittivity. l_t is the mean length per turn. D_o is the outer diameter of magnetic wire. D_c is the inner diameter of magnetic wire.

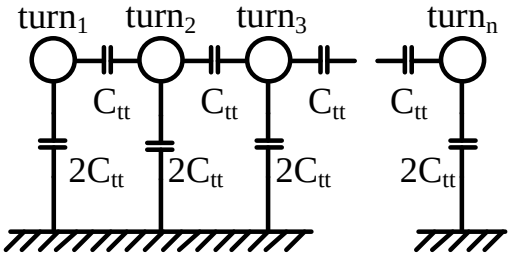

Fig. 2-30 Estimate boost inductor's self-inductance.

EMI test is carried out using LISN, so impedance of LISN is also critical for estimate noise, here LISN impedance is modeled as a 50 Ω resistor.

After the parasitic have been modeled, the equivalent circuit can be drawn as shown in Fig. 2-31 for DM and Fig. 2-32 for CM.

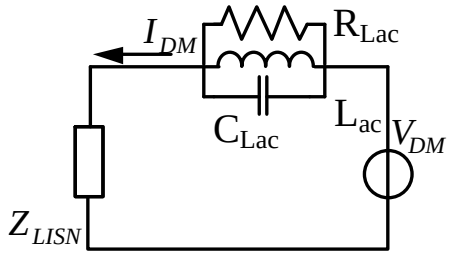

Fig. 2-31 DM equivalent circuit of three-phase boost rectifier.

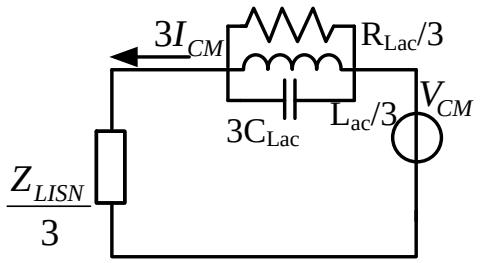

Fig. 2-32 CM equivalent circuit of three-phase boost rectifier.

Compare with the EMI standard, required attenuation $V_{req,DM}$ and $V_{req,CM}$ can be calculated as follows:

$$V_{req,DM}(dB) = V_{DM}(dB) - I_{Limit} \cdot Z_{LISN}(dB)$$
$$V_{req,CM}(dB) = V_{CM}(dB) - I_{Limit} \cdot Z_{LISN}(dB) \quad (2.25)$$

In (2.23), I_{Limit} is the noise current limit defined in standard.

Corner frequency need for the EMI filter can be calculated by drawing the 40 dB/dec slope line that is tangent to the required attenuation according to [22]. For the two-stage filter, 80 dB/dec slope line is needed.

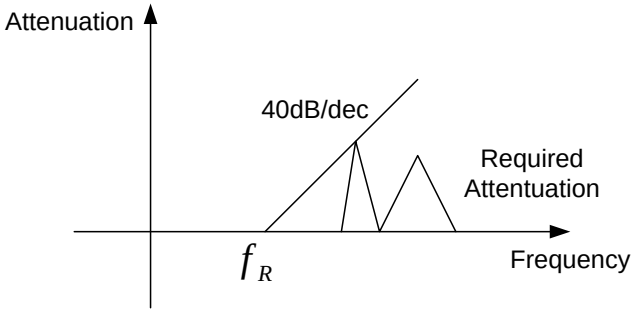

Fig. 2-33 Find corner frequency of filter.

The relationship between inductance capacitance and corner frequency is (2.24) for one-stage filter and (2.25) for two-stage filter.

$$L_{CM} = \left(\frac{1}{2\pi f_{R,CM}}\right)^2 \frac{1}{C_{CM}} \quad (2.26)$$

$$L_{CM} = \frac{3+\sqrt{5}}{2}\left(\frac{1}{2\pi f_{R,DM}}\right)^2 \frac{1}{C_{CM}} \tag{2.27}$$

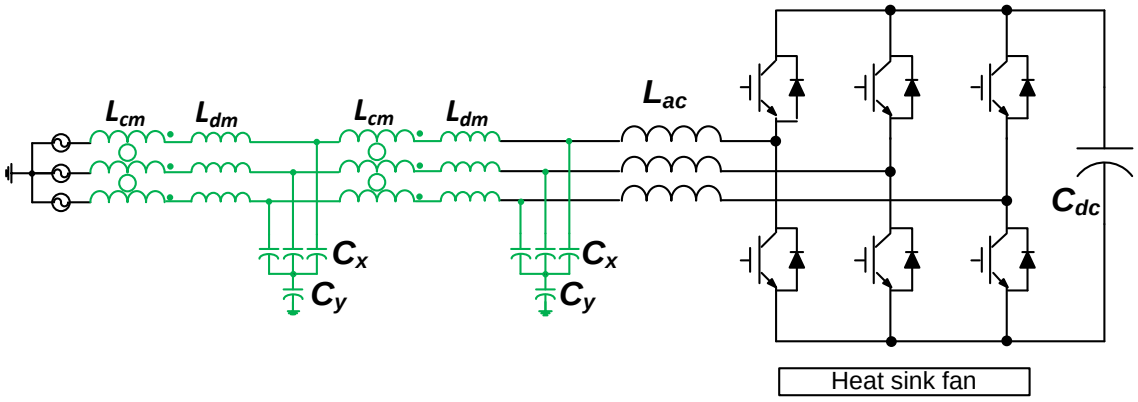

Fig. 2-34 Three-phase two-level boost rectifier with two-stage input EMI filter.

Fig. 2-34 shows the boost rectifier with a two-stage input EMI filter. The selection of capacitors in the filter follows the following rules.

For CM capacitor C_y, earth leakage current thought the capacitor should be considered, for different application the maximum leakage current is limited differently, one typical limit is 3.5 mA. The maximum total capacitance between phase and the protective earth is 44 nF. In this study C_y is set to be 6.8 nF.

For DM capacitor C_x, total input capacitance is limited for some application in order to not let the total input line-to-line capacitance too big, C_x is set to be 1uF in this study.

IV. Three-phase Three-level PWM Vienna Rectifier

Three-phase three-level PWM Vienna rectifier [24] is a unidirectional three-level rectifier which offers the following advantages as compared to two-level converters [25]:

1. Lower harmonic level of the mains current.

2. Lower blocking voltage stress on the power semiconductor devices (only half of the conventional two-level voltage source rectifier).

3. Inherent higher reliability, since it is not prone to the shoot-through characteristic failure of voltage-source topologies, and there is no need for dead time application and consequently for dead time compensation.

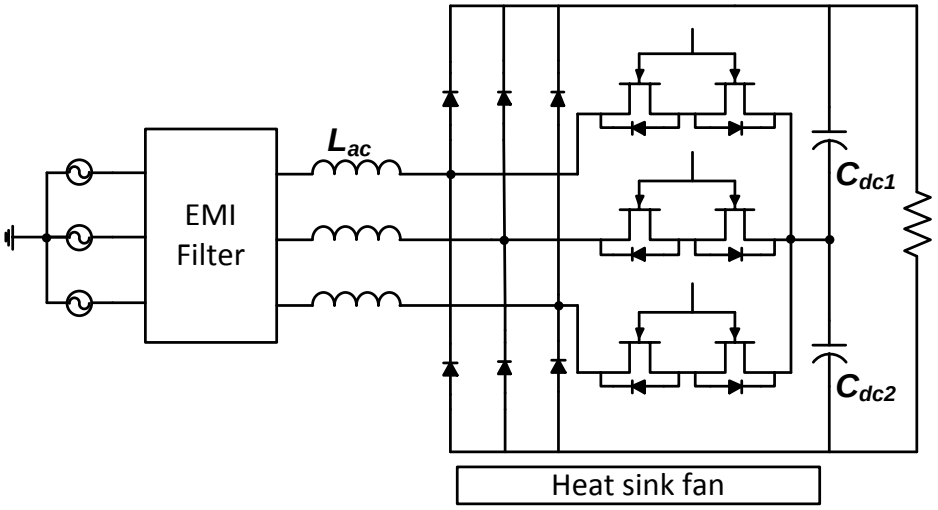

Fig. 2-35 Three-phase three-level PWM Vienna rectifier.

Vienna rectifier brings with itself some operational and design challenges. It is a current-dependent forced commutated voltage-source rectifier, which is its input voltage generation is dependent on not only the switches status but also on the current direction.

Vienna rectifier has only three switches; one per phase-leg. If the switch of one phase is on, then that phase is clamped to the neutral point of the dc-link. Otherwise the voltage of that phase is determined by the current direction. If the input current is positive, the upper diode of that phase will be on and the phase-leg will be clamped to the positive dc-link rail. If the input current is negative, the bottom diode will be on and the phase-leg will be clamped to the negative dc-link.

The design of Vienna rectifier can use the same procedure as discussed in previous section for boost rectifier. Components need to be designed are input EMI filter, input inductor, power stage, cooling system and dc-link capacitor. The different is Vienna rectifier has different modulation scheme and two dc-link capacitor [26] [27].

Modulation scheme influence not only loss calculation (calculation of device on time and switching pattern) but phase-leg voltage waveform and spectrum which are critical to determine

input inductor current ripple and EMI noise. Fig. 2-36 shows the spectrum of Vienna rectifier with continuous modulation scheme [28] [29][30].

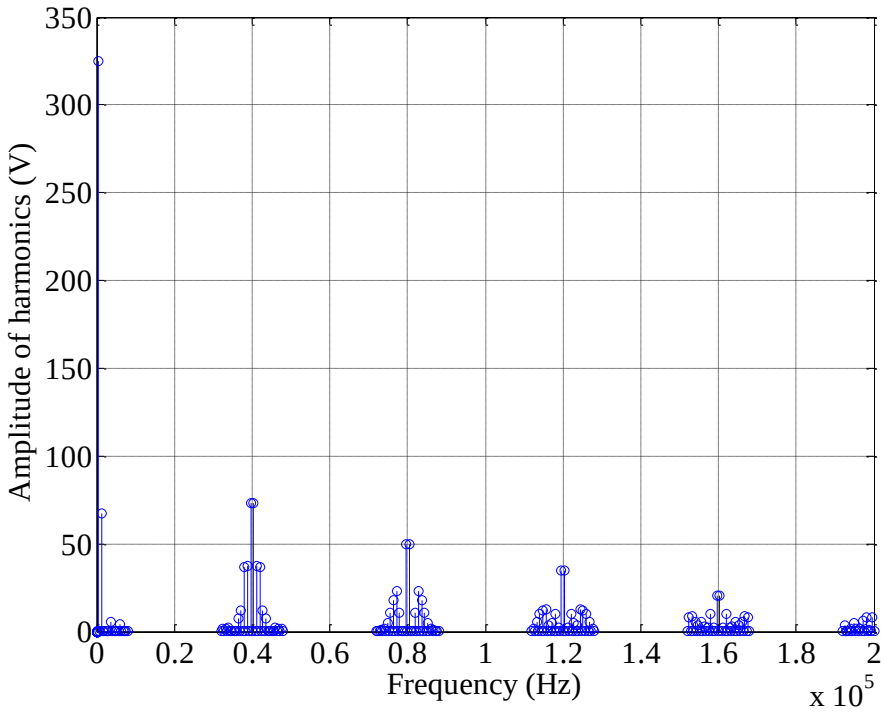

Fig. 2-36 Spectrum of the phase-leg voltage for Vienna rectifier.

V. Voltage Source Inverter

The two-level voltage source inverter (VSI) is the most popular topology used in motor controllers. A typical system structure is shown in Fig. 2-37, in which the motor controller can be integrated with the motor, or it can feed the motor via an output filter and long cable.

Design of system as shown in Fig. 2-37 including input filter, dc-link capacitor, power stage, cooling system output filter and cable. Dc-link capacitor, power stage and cooling system design can refer to the design procedure of three-phase two-level PWM boost rectifier. Input filter, output filter will be discussed in this section.

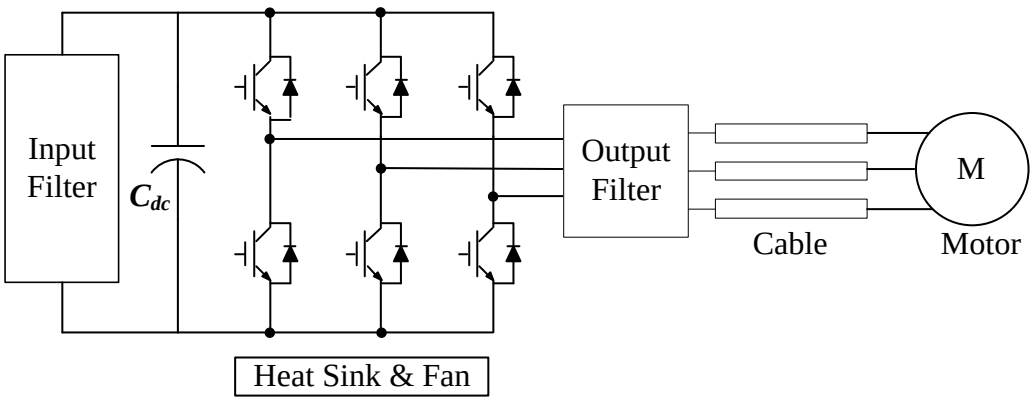

Fig. 2-37 VSI with input and output filter.

A. Input Filter Design

Input filters are needed for both low-frequency harmonics and EMI. Dc-side filters are still needed because of phase-leg voltage noise, but the calculation of DM current is different as the ac side input EMI filter design of boost rectifier.

Dc-side current is formed by the switching function and the ac-side current:

$$i_{dc}(t) = s_a(t) \cdot i_a(t) + s_b(t) \cdot i_b(t) + s_c(t) \cdot i_c(t) \tag{2.28}$$

s_a, s_b and s_c are switching functions determined by modulation scheme; ia, ib and ic are phase a, phase b and phase c current. This relationship is in time domain. In frequency domain, this relationship can be connected using convolution [31]:

$$I_{dc} = DFIT(s_a) \otimes DFIT(i_a) + DFIT(s_b) \cdot DFIT(i_b) + DFIT(s_c) \cdot DFIT(i_c) \tag{2.29}$$

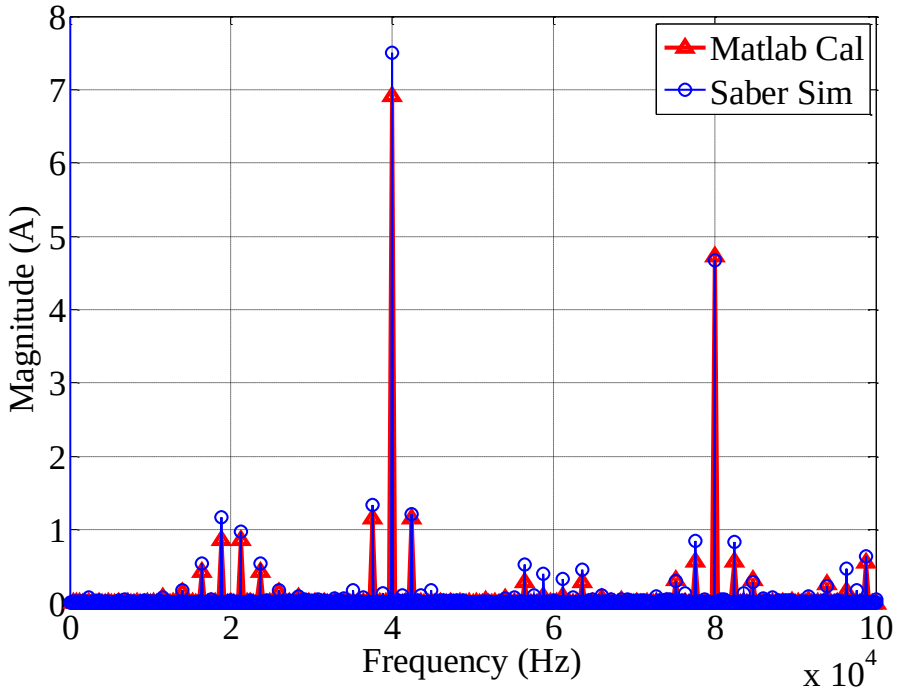

Fig. 2-38 Calculation results for dc current in low frequency range.

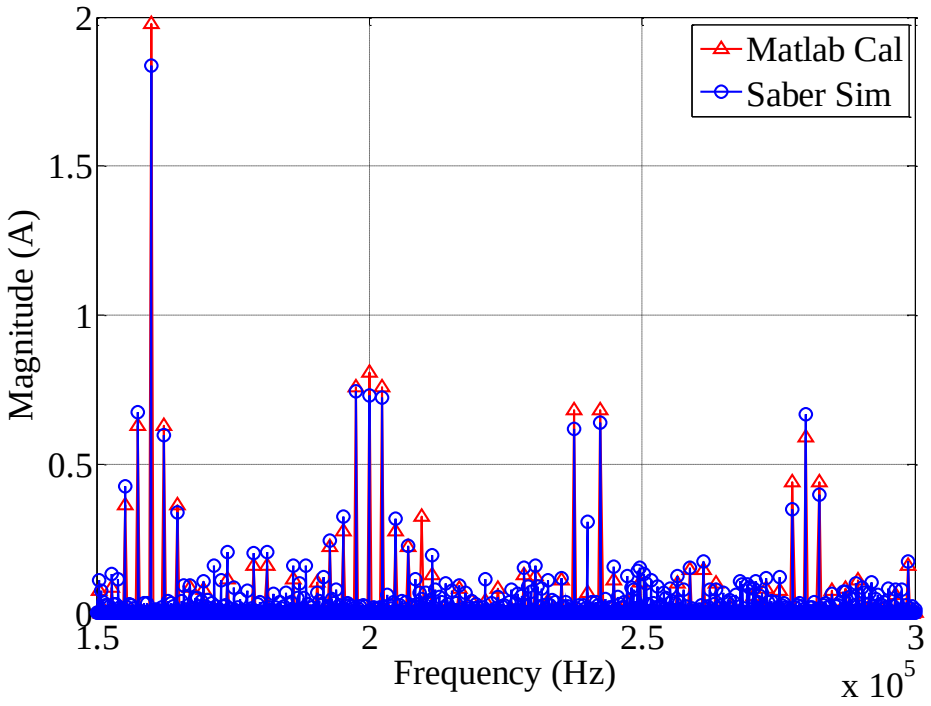

Fig. 2-39 Calculation results for dc current in EMI frequency range.

DFIT calculation of switching function and ac side phase current are the same as discussed in boost rectifier section. Fig. 2-38 shows the calculation results for dc current in low frequency range for SVM. The results are compared with simulation. Fig. 2-39 shows the calculation results in EMI frequency range for SVM. Comparing with simulation results, the calculation captured critical frequency point of noise. After getting the noise current spectrum, DM filter can be designed using procedure in Section III.

For CM, the procedure is the same as Section III. Equivalent circuit used for dc side CM is:

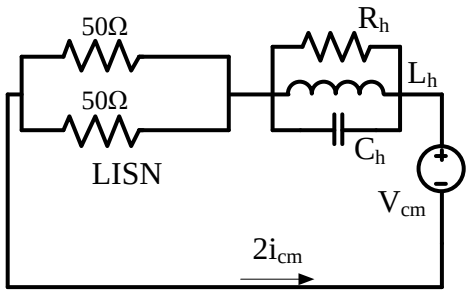

Fig. 2-40 VSI input CM equivalent circuit.

In Fig. 2-40, L_h is the inductor of low frequency harmonic filter.

Fig. 2-41 shows the structure of input filter.

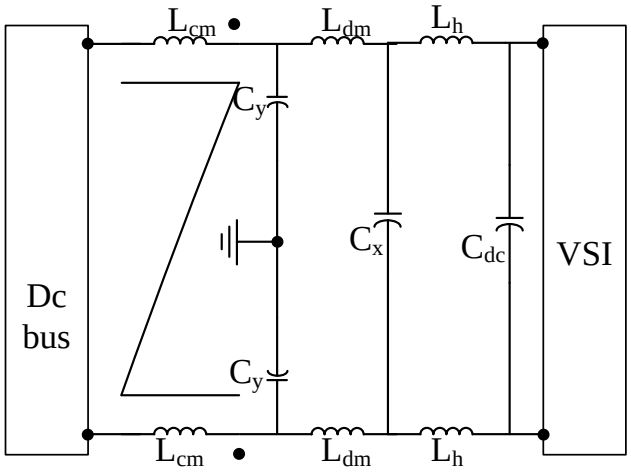

Fig. 2-41 Input EMI and low frequency current harmonic filter of VSI.

B. Output Filter Design

The motor controller system–which includes the VSI, output filter, long cable and motor–is shown in Fig. 2-42. Any commercial motor drives which have a long cable feeding the motor must meet the EMI standard when measuring the CM and DM current in the cable.

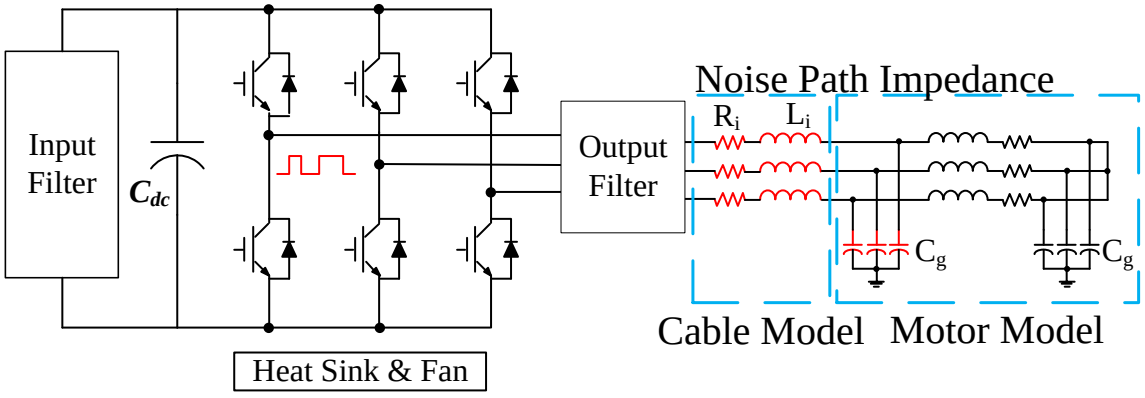

Fig. 2-42 VSI output filter and cable.

Again, like the design of the input EMI filter for active front end system, in order to design a filter to meet the standard, we need to figure out the source and the path of the EMI noise. Still, the noise source is the voltage of phase-leg. DFIT is used to get the spectrum of CM and DM voltage. But the noise propagation path to the motor side is different from what have been discussed in boost rectifier. In Fig. 2-42, L_i and R_i are the self-inductance and resistance of the cable they are on the way of both CM and DM noise path, L_i can be calculated as:

$$L_i = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{R_c}+\sqrt{\left(\frac{l}{R_c}\right)^2+1}\right)+\frac{R_c}{l}-\sqrt{\left(\frac{R_c}{l}\right)^2+1}\right] \tag{2.30}$$

In (2.30), l is the length of the cable, R_c is the radius of the conductor, and μ_0 is the permeability of vacuum space.

R_i can be calculated as:

$$R_{20} = \rho_{20}\frac{l}{A} \tag{2.31}$$

$$R_T = R_{20}(1+\alpha(T-20)) \tag{2.32}$$

In (2.31) and (2.32), R_T is the cable self-resistance, l is the length of the cable, ρ_{20} is the cable material resistivity; the cable material can be aluminum or copper. α is the temperature coefficient of aluminum or copper.

C_g is the parasitic capacitance from motor shaft to ground; 10nF is used for this value.

Equivalent circuit for DM and CM are shown in Fig. 2-43 and Fig. 2-44. Other procedure of design is the same as which has been discussed in boost rectifier.

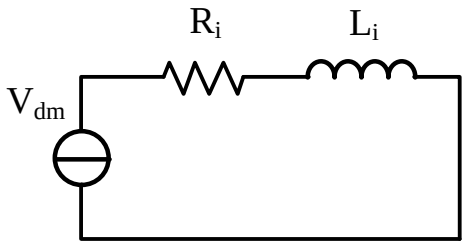

Fig. 2-43 VSI output side DM equivalent circuit.

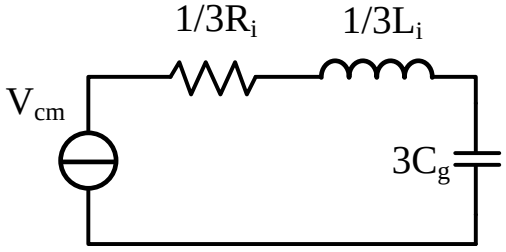

Fig. 2-44 VSI output side CM equivalent circuit.

VI. Single-phase Power Factor Correction Circuit

Single-phase power factor correction circuit (PFC) is critical for ac/dc power conversion from the line voltage, particularly for electronics equipment. There are many topologies can achieve power factor correction, this report focuses on the most commonly used topologies to design a CCM single-phase boost PFC.

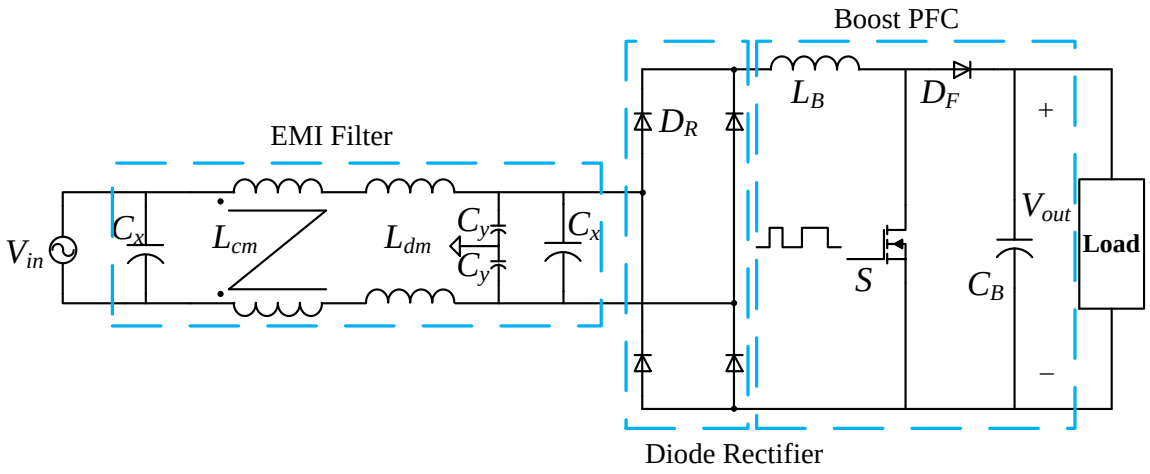

Fig. 2-45 Single-phase boost PFC.

A. Power Stage Design

Power stage design includes power device selection, loss calculation and thermal calculation.

i) Power Device Selection

Two kinds of switch can be used, IGBT and MOSFET. With new-generation technologies, the speed of IGBTs has increased a great deal; an IGBT's maximum switching frequency is much lower than that of a MOSFET. Therefore, if a MOSFET is used, the boost inductor and filter size can be significantly reduced. Thus a MOSFET is selected for this application. A hard-switching PWM technique is used in this application.

The steady-state voltage stress of the MOSFET is V_B which 400 V in this application is. Then a 600 V MOSFET can be used, considering its voltage margin and low on-resistance. The current rating of the MOSFET is selected as 1.5 times the RMS current through the switch.

The following equation is used to calculate the maximum RMS current through the MOSFET.

$$I_{sw\_RMS} = \sqrt{\frac{\int_0^{\pi}\left(1-\frac{V_{in(\min\_pk)}}{v_B}\sin(\omega t)\right)\cdot\left(I_{LB(\max\_pk)}\cdot\sin(\omega t)\right)^2 d(\omega t)}{\pi}} \qquad (2.33)$$

$$I_{LB(\max\_rms)} = \sqrt{\left(\frac{I_{in}}{\sqrt{2}}\right)^2 + \left(\frac{1}{2\sqrt{3}}\Delta i_{LB(\max)}\right)^2} \tag{2.34}$$

The employment of silicon carbide (SiC) Schottky diodes can effectively eliminate turn-on losses because they show virtually no reverse-recovery behavior [32] [33] [34]. In this study, SiC diode is used for boost converter freewheeling diode.

The steady-state diode reverse voltage stress is V_B, which is 400 V. Thus a 600 V diode can be used.

The current rating of the SiC diode is selected to be 1.5 times the average current through the diode. The average diode current is used because the conduction loss on the diode is determined by the average current through the diode, and it is:

$$I_{d(\max\_ave)} = \frac{1}{\pi}\cdot\int_0^{\pi}\frac{V_{in(\min\_pk)}}{V_B}\cdot\sin(\omega t)\cdot I_{LB(\max\_pk)}\cdot\sin(\omega t)d(\omega t) \tag{2.35}$$

The voltage stress of rectifier bridge diode is $V_{in(\max\_pk)} = 173V$, so a 300V-rating diode is chosen.

The average current through the diode is:

$$I_{rd\_ave\max} = 0.5\frac{I_{in(\max\_pk)}}{\frac{\pi}{2}} \tag{2.36}$$

ii) Loss Calculation

Device losses include conduction loss and switching loss. Below, the losses of power MOSFETs, SiC Schottky diodes, and rectifier diodes are calculated.

Diode conduction loss is modeled as a resistor in series with a voltage source.

The switching losses of the rectifier diode are small enough to be neglected due to the low switching frequency, which is double the line frequency.

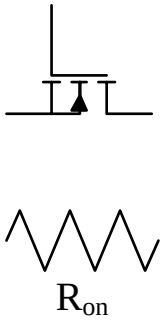

Fig. 2-46 MOSFET on state loss model

The MOSFET conduction loss is modeled as a resistor that is dependent on the junction temperature of the MOSFET.

The MOSFET switching losses include three parts; turn-on energy losses, turn-off energy losses, and the charge accumulated in C_{oss} during the off state (this charge energy is lost during turn-on). During each switching period, these energy losses can be expressed as:

$$E_{on} = \frac{1}{2} \cdot V_{off} \cdot I_{LBon} \cdot t_r \tag{2.37}$$

$$E_{mos\_C_{oss}} = \frac{2}{3} \cdot C_{oss} \cdot V_{off}^2 \tag{2.38}$$

$$E_{off} = \frac{1}{2} \cdot V_{off} \cdot I_{LBoff} \cdot t_f \tag{2.39}$$

In (2.37), (2.38) and (2.39), V_{off} is equal to output voltage V_B, and I_{LBon}, I_{LBoff} depend on the input current and boost inductor current ripple, they are:

$$I_{LBon} = i_{in}(t) - \frac{1}{2}\Delta i_{LB}(t) \tag{2.40}$$

$$I_{LBoff} = i_{in}(t) + \frac{1}{2}\Delta i_{LB}(t) \tag{2.41}$$

An Infineon 600VCoolMos is used for evaluation. The conduction losses of the SiC Schottky diode are modeled the same as that of the rectifier diode; no reverse-recovery losses are

considered for this kind of diode because there are nearly no visual reverse recovery loss. A 600V Schottky diode from Cree is used for loss evaluation.

iii) Thermal calculation

For calculating the heat sink thermal resistance, a 1-D equivalent thermal model should be sufficient, so the procedure is the same as been discussed in three-phase two-level PWM boost rectifer.

B. Boost Inductor Design

The design of the boost inductor is one of the main challenges in the PFC circuit, and it has been discussed in [35].

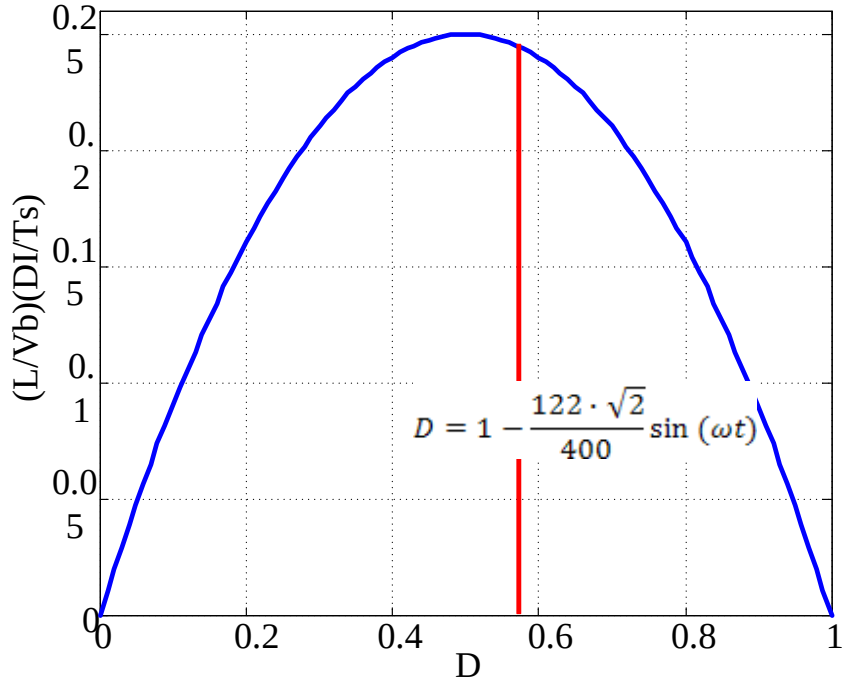

Fig. 2-47 Boost inductor current ripple vs. duty ratio.

Because the PFC switching duty cycle is not constant during a half-line cycle, the instantaneous current ripple also varies from point to point. It can be proven that the maximum inductor current ripple in a boost PFC converter occurs when the duty-ratio is 0.5 as shown in Fig. 2-47. It can be seen that if the duty ratio is less than 0.5, the maximum duty ratio gives the

maximum current ripple. Moreover, to keep the same input power, the input current will reach its highest value at the lowest input voltage; thus the lowest input voltage should be used in the calculation. For a boost PFC converter, the duty-ratio can be calculated by:

$$D = 1 - \frac{V_{in(pk)}}{V_B}\sin(\omega t) \tag{2.42}$$

The boost inductance can be derived as:

$$L_B \frac{\Delta i_{LB}}{\Delta t} = v_{LB} \tag{2.43}$$

$$L_B = \frac{D \cdot (1-D) \cdot V_B}{f_s \cdot \Delta i_{LB}} \tag{2.44}$$

When the duty ratio reaches 0.5, then:

$$L_B = \frac{0.25 V_B}{f_s \cdot \Delta i_{LB(\max)}} \tag{2.45}$$

The maximum allowed peak-to-peak current ripple $\Delta i_{LB(\max)}$ depends on the constant ripple factor:

$$k_{ripple} = \frac{\Delta i_{LB(\max)}}{I_{in}} \tag{2.46}$$

In (2.46), I_{in} is the input current amplitude.

In principle, the selection of the ripple factor k_{ripple} will have an influence on the losses, the EMI filter requirements, and the inductance volume; and the selection of k_{ripple} should therefore be carefully selected for CCM operation. [36] gives an optimization of k_{ripple} regarding the inductance volume, and shows that an optimal value for k_{ripple} regarding minimal inductor volume can be found for a specific switching frequency. However, if the converter efficiency is not of major importance and the losses can be transferred effectively to the heat sink, the main tradeoff in the selection of k_{ripple} appears between the inductor volume and the input-filter

volume. It is advisable to choose a ripple factor of at least $k_{ripple} > 0.4$ in order to achieve minimum total volume.

The peak inductor current can be calculated by the sum peak value of line frequency and peak value of ripple current:

$$I_{LB(\max\_pk)} = I_{in} + \frac{1}{2}\Delta i_{LB(\max)} \tag{2.47}$$

The maximum RMS value of inductor current can be estimated by counting both the line frequency and the maximum ripple RMS value.

$$I_{LB(\max\_rms)} = \sqrt{\left(\frac{I_{in}}{\sqrt{2}}\right)^2 + \left(\frac{1}{2\sqrt{3}}\Delta i_{LB(\max)}\right)^2} \tag{2.48}$$

C. Output Capacitor Design

The objective is to select the smallest PFC output capacitance that provides good attenuation of the 2nd harmonic ripple and minimizes interactions with the load.

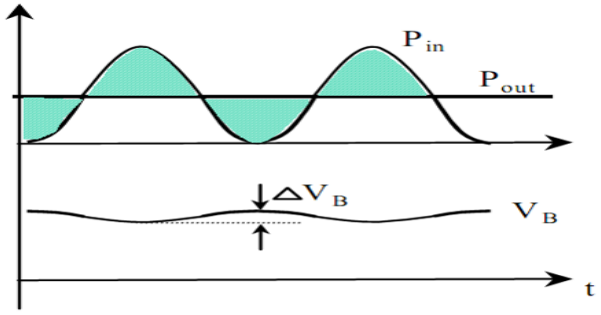

Fig. 2-48 Single-phase PFC output capacitor voltage ripple.

As shown in Fig. 2-48, the voltage ripple on the output capacitor C_B is caused by the difference between instantaneous input power P_{in} and output power P_{out}. For a power factor correction converter, if the input current has a perfect sinusoidal waveform, the input power will also have a pulsating waveform. However, if the output power is regulated, there will always be a difference between input and output power, as shown in the shadowed area in Fig. 2-48. This difference in power is stored on the output capacitor and causes capacitor voltage ripple ΔV_B.

This voltage ripple depends on the capacitor value C_B and the output power P_{out}, and the angular mains frequency ω according to:

$$\Delta V_B = \frac{P_{out}}{2\omega \cdot C_B \cdot V_B} \tag{2.49}$$

The output capacitor voltage ripple is selected as $\Delta V_B = 10\% V_B$, which is a practical value.

Another important aspect for selection of the output capacitor is the maximum capacitor current ripple. For a switching frequency much higher than the line frequency, the global RMS current, which is critical for capacitor selection, can generally be derived via the integration of the local RMS value $i_{C,rms}^2$, which is given by:

$$i_{C,rms}^2(\omega t) = \frac{1}{T_s}\int_0^{T_s} i_C^2(t)dt \tag{2.50}$$

Then over the line period,

$$I_{C,rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} i_{C,rms}^2(\omega t)d(\omega t) \tag{2.51}$$

Depending on the specific topology and operating mode, the evaluation of this formula can lead to very complex analytical calculations. According to [37], for both CCM and DCM operation, the output capacitor RMS current shows a basic dependence only on the output current I_0 and the voltage transfer ratio α as follows:

$$I_{C,rms} = I_0 \cdot f(\alpha) \tag{2.52}$$

$f(\alpha)$ has been fitted to the shown analytically calculated curves with least-square approximations of higher order type

$$f(\alpha) = k_0 + k_1 \cdot \alpha + k_2 \cdot \alpha^2 + k_3 \cdot \alpha^3 + k_4 \cdot \alpha^4 \tag{2.53}$$

For CCM, when $0 \le \alpha \le 1$:

$$
\begin{aligned}
k_0 &= 4.3 \\
k_1 &= -9.7 \\
k_2 &= 10.7 \\
k_3 &= -4.4 \\
k_4 &= 0
\end{aligned}
\tag{2.54}
$$

D. Input EMI Filter Design

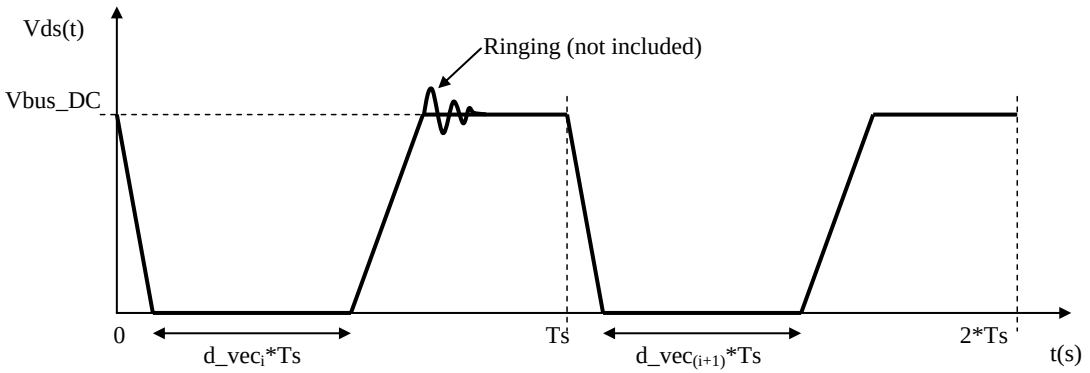

Fig. 2-49 Time domain waveform of equivalent voltage source of boost PFC.

We can appropriately characterize this voltage source in the frequency domain using the Laplace transform, and then applying the appropriate conversion to the Fourier representation:

$$
V_{noise} = 2 \cdot fline \cdot \left[\frac{Vbus\_DC}{p_n} \cdot \left(1 - e^{\left(-\frac{Tline}{2} \cdot p_n \right)} \right) + \sum_{k=1}^{num} \left(\frac{vout_k}{Tfall_k \cdot p_n^2} \cdot \left(-e^{-(k-1) \cdot Ts \cdot p_n} + e^{-((k-1) \cdot Ts + Tfall_k) \cdot p_n} \right) + \right. \right.
$$

$$
\left. \left. + \frac{vout_k}{Trise_k \cdot p_n^2} \cdot \left(e^{-((k-1)+d\_vec_k) \cdot Ts \cdot p_n} - e^{-(((k-1)+d\_vec_k) \cdot Ts + Trise_k) \cdot p_n} \right) \right) \right] \tag{2.55}
$$

By calculation the spectrum of waveform shown in Fig. 2-49 is shown in Fig. 2-50.

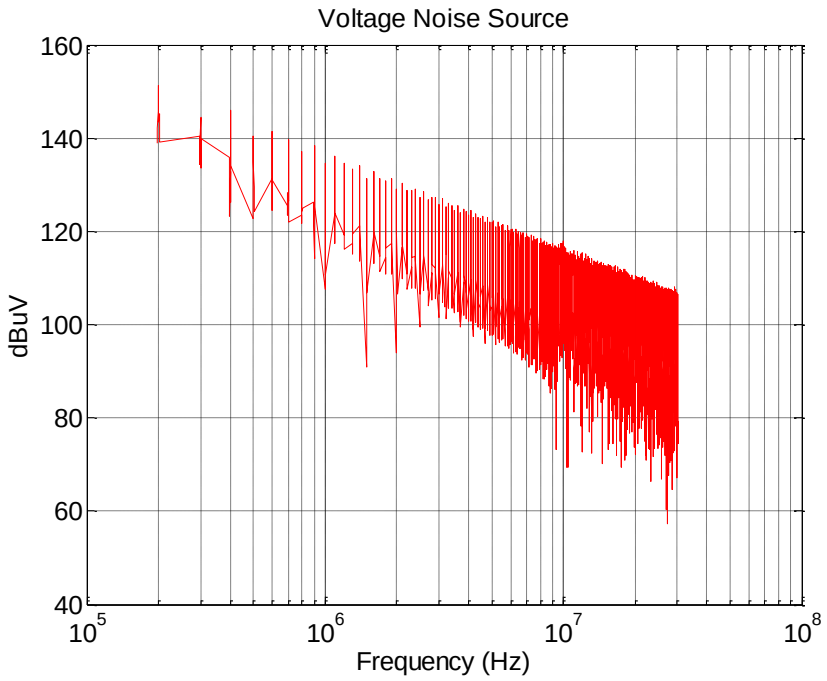

Fig. 2-50 Spectrum of equivalent voltage source of boost PFC converter.

The important parasitic of boost PFC are device drain to ground capacitor and boost inductor self-inductance as shown in Fig. 2-51. This is the same as three-phase two-level PWM boost rectifier; the procedure can be used here.

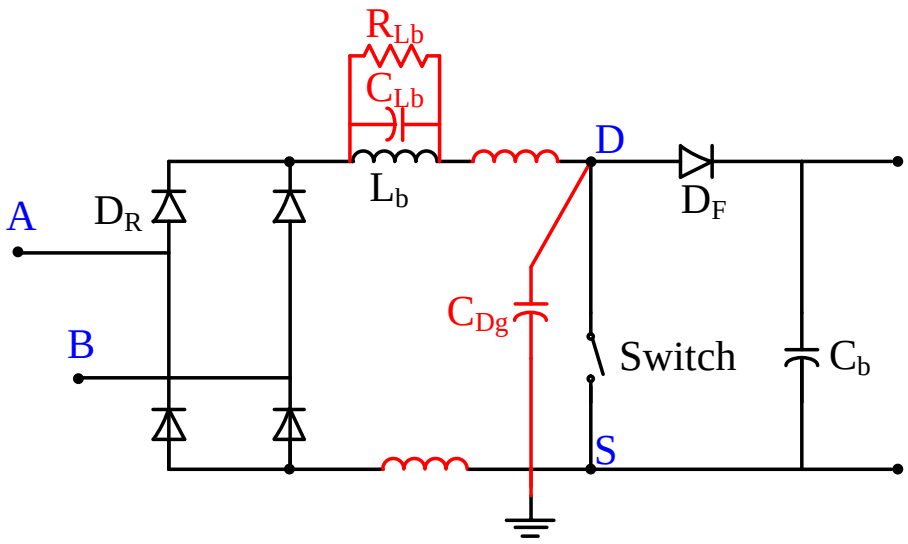

Fig. 2-51 Boost PFC with critical parasitic.

Hence, by using equivalent circuits shown in Fig. 2-52 and Fig. 2-53, the noise current on the LISN can be easily calculated.

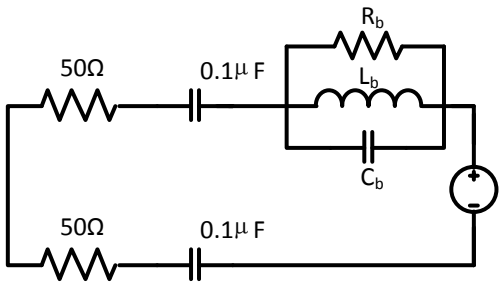

Fig. 2-52 Single-phase PFC DM equivalent circuit.

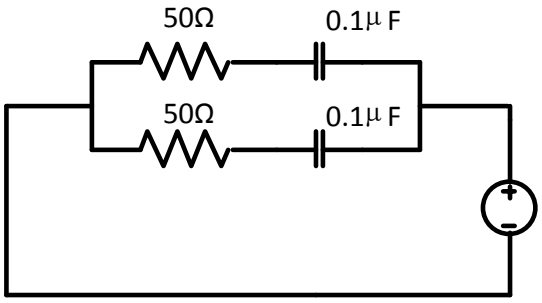

Fig. 2-53 Single-phase PFC CM equivalent circuit.

VII. Dc-dc Converter

The dc-dc converter been designed here is a full bridge topology as shown in Fig. 2-54. This kind of dc-dc converter is widely used in as battery charger or generates a dc bus from another dc bus [38] [39]. The power level of this dc-dc converter is from 1 kW to 3 kW, full bridge is the most common used topology for this kind of application. As shown in Fig. 2-54, the primary stage is an active bridge using MOSFET; IGBT may also be used for higher voltage application. The secondary stage is a diode base full bridge rectifier, the two stages is connected by a high frequency transformer. This converter can be used to connect two dc buses, so both input and output need EMI filter. The design of this converter including design of input and output EMI filter, power stage, output ripple filter and high frequency transformer.

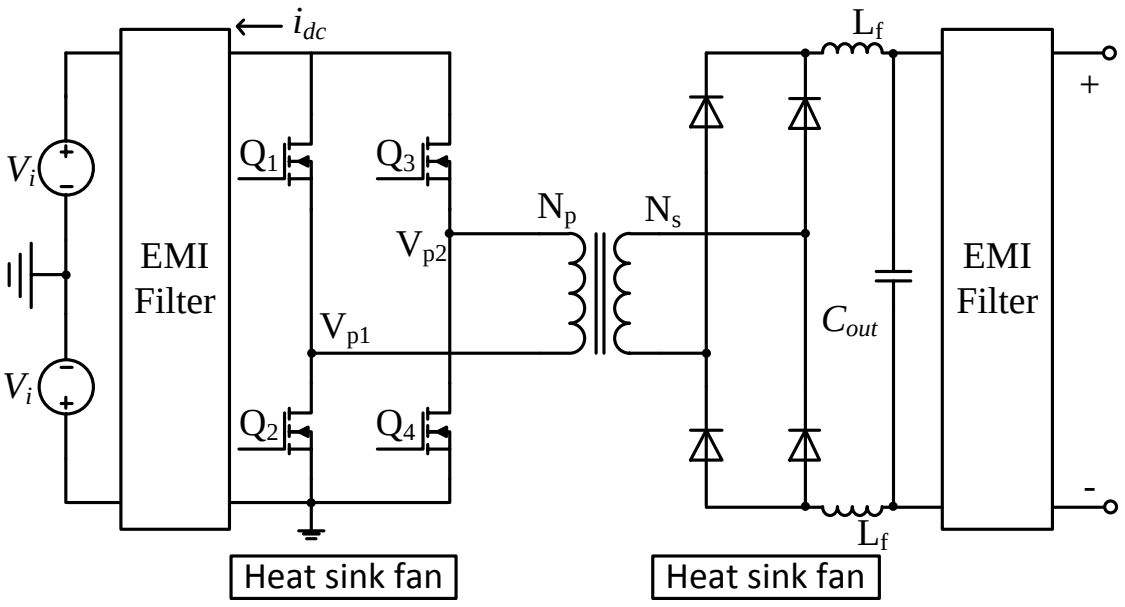

Fig. 2-54 Full bridge dc-dc converter.

Fig. 2-55 shows the gate signal for the full bridge MOSFETs, and transformer primary and secondary side voltage. When clock signal rising edge is detected, MOSFET Q_1 and Q_4 are turned on for t_{on} time $t_{on} < 0.5T_s$; when clock signal falling edge is detected, MOSFET Q2 and Q3 are turned on for t_{on} time. By doing this switching pattern, voltage of the transformer primary side is, as V_p in Fig. 2-55 shows, alternating rectangle signal. Assume transformer turn ratio is N_s/N_p, then after diode rectifier the voltage is, as V_{out1} in Fig. 2-55 shows, rectangle signal which has a duty ratio of $2t_{on}/T_s$. and the average value of this voltage is:

$$V_{out} = \frac{t_{on}}{0.5T_s}\frac{N_s}{N_p}V_{dc} \qquad (2.56)$$

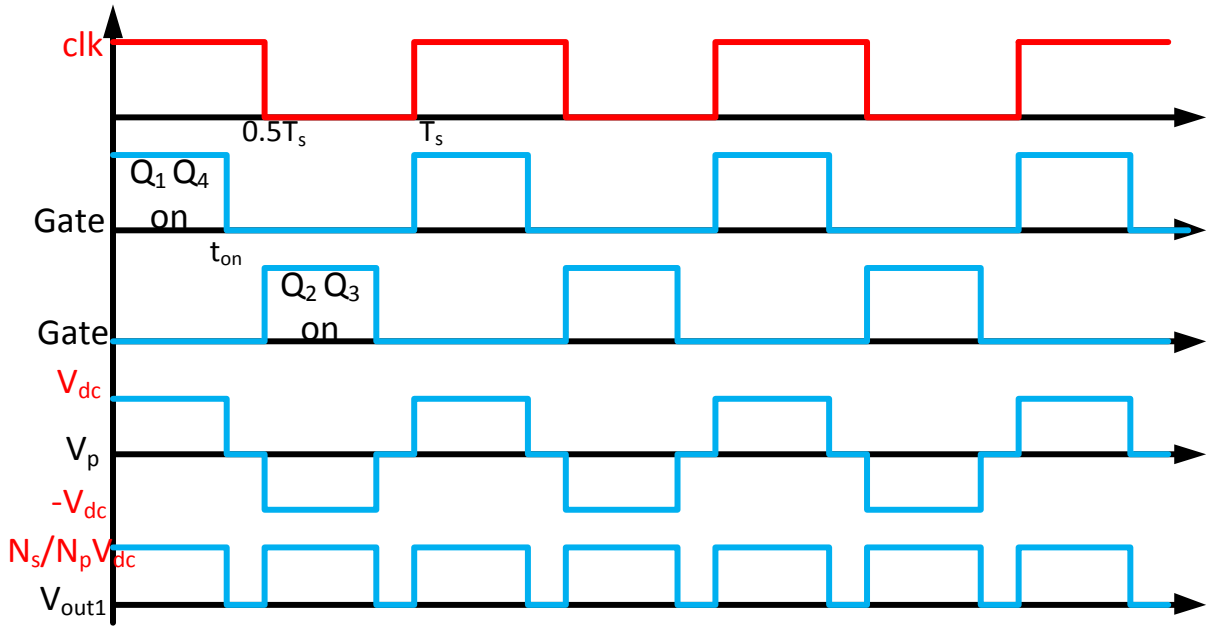

Fig. 2-55 Full bridge dc-dc converter working waveforms.

A. Power Stage Design

Power stage design includes selection of power device, loss and thermal calculation.

i) Device Selection

For full bridge primary side, MOSFET is used; SiC diode is used for secondary side diode rectifier-bridge. Device rating is selected according to blocking voltage need and continuous current flowing through the device. The voltage rating is set to be around two times of blocking voltage and the current rating is around two time of nominal current value. For some low voltage (either input side or output side) parallel of devices may be used. In this study, CoolMOS from Infineon and SiC diode form CREE are used. the extraction of device data can be done using the same procedure in the three-phase two-level PWM boost rectifier section. Data base of device parameters is built.

ii) Loss Calculation

Linear approximation is used for device loss models and they are the same as discussed in Section VI.

Let the P_Q be MOSFET conduction loss, it can be calculated using MOSFET on resistance R_{on} and rms current I_{rms}:

$$P_Q = R_{on} I_{rms}^2 \tag{2.57}$$

Turn on energy of MOSFET is:

$$E_{on} = \frac{1}{2} V_{off} I_{on} t_r \tag{2.58}$$

Voff is MOSFET blocking voltage when off; Ion is the current value when MOSFET is turned on; tr is MOSFET turn on time.

Charge energy accumulated in C_{oss} during the off state:

$$E_{mos\_Coss} = \frac{2}{3} C_{oss} V_{off}^2 \tag{2.59}$$

Coss is MOSFET output capacitance.

Turn off energy of MOSFET:

$$E_{off} = \frac{1}{2} V_{off} I_{on} t_f \tag{2.60}$$

Tf is MOSFET turn on time.

MOSFET rms current I_{rms}:

$$I_{rms} = \frac{I_{load}}{\frac{N_p}{N_s}} \sqrt{\frac{D}{2}} \tag{2.61}$$

N_p/N_s is the transformer turn ratio.

I_{load} is converter output current.

Turn on current of MOSFET:

$$I_{on} = \frac{I_{load} - 0.5 \cdot \Delta I}{\frac{N_p}{N_s}} \tag{2.62}$$

Turn off current of MOSFET:

$$I_{on} = \frac{I_{load} - 0.5 \cdot \Delta I}{\frac{N_p}{N_s}} \tag{2.63}$$

Conduction loss of diode:

$$P_D = \left(V_{Frd} + R_{onrd} \cdot I_{avg}\right) I_{avg} \tag{2.64}$$

V_{Frd} is the forward voltage of diode; R_{onrd} is the diode on resistance; I_{avg} is the diode average current.

iii) Thermal Calculation

For calculating the heat sink thermal resistance, a 1-D equivalent thermal model should be sufficient, so the procedure is the same as been discussed in three-phase two-level PWM boost rectifer.

B. Transformer Design

For transformer design, the first task is to determine the turn ratio. It can be got from output voltage (2.56). In (2.56), set $\frac{t_{on}}{0.5T_s}$ to be 0.8, which means the duty cycle is 0.4. Consider transformer leakage inductance will cause secondary side duty cycle loss the maximum duty cycle in the secondary side is set to be 0.75. Then the transformer turn ratio is:

$$\frac{N_p}{N_s} = \frac{t_{on}}{0.5T_s} \frac{V_{dc}}{V_{out}} \tag{2.65}$$

C. Output Ripple Filter Design

Ripple filter is used to limit output current switching ripple and output voltage switching ripple. Fig. 2-54 shows the circuit schematic.

The output current switching ripple is:

$$\Delta I = \frac{\Delta T \cdot V_{Lf}}{L_f} \tag{2.66}$$

L_f is the inductance of the filter, V_{Lf} is the voltage cross the inductor, ΔT is the equivalent turn on time on the secondary side.

So inductance is:

$$L_f = \frac{\Delta T \cdot V_{Lf}}{\Delta I} \tag{2.67}$$

V_{Lf} is:

$$V_{Lf} = V_s - V_{out} \tag{2.68}$$

ΔT is:

$$\Delta T = D_{max\_s} \cdot \frac{T_s}{2} \tag{2.69}$$

V_s is the transformer secondary side voltage, V_{out} is the output voltage of converter.

D_{max_s} is set to be 0.75 and ΔI is 10% of normal output current.

The capacitance of the filter is:

$$C_{out} = \frac{\Delta T \cdot \Delta I}{\Delta V} \tag{2.70}$$

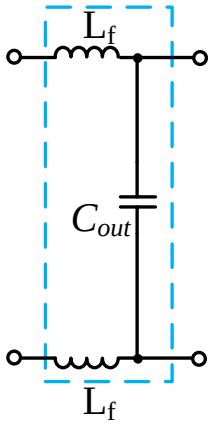

Fig. 2-56 Output ripple filter.

D. Output EMI Filter Design

Noise source is the pulsating full bridge middle point V_{p1}, V_{p2} shown in Fig. 2-57. And the important parasitic in the noise propagation path are MOSFET drain to ground capacitance C_{dg}; capacitance between transformer primary and secondary winding C_{12}; capacitance of primary and secondary winding; primary and secondary leakage inductance L'_{11}, L'_{12}; primary and secondary leakage inductance self-capacitance C_1 and C_2; output ripple filter inductance L_f, inductor self-capacitance C_{Lf} and output capacitor C_{out}.

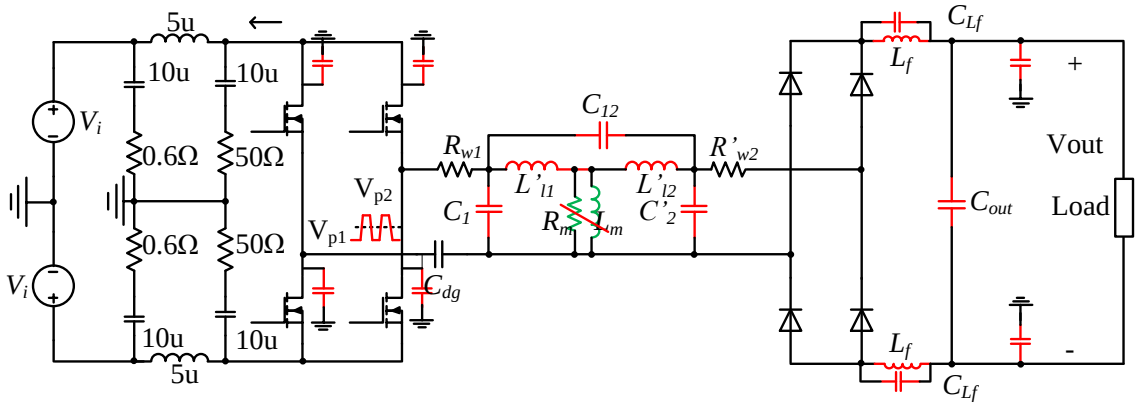

Fig. 2-57 Full bridge circuit diagram with parasitic.

From this circuit diagram, EMI noise source and equivalent circuit for CM and DM can be identified.

CM and DM voltage definitions are:

$$V_{CM} = \frac{V_{p1} + V_{p2}}{2} \tag{2.71}$$

$$V_{CM} = V_{p1} - V_{p2} \tag{2.72}$$

Consider the PWM pattern and certain gate single delay (right phase leg behind left one), the waveforms of CM and DM voltage are shown as:

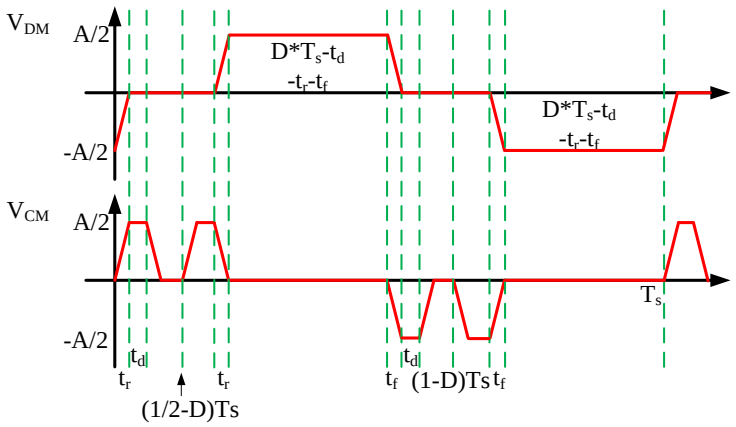

Fig. 2-58 DM and CM voltage waveforms of full bridge dc-dc converter.

Spectrum of CM and DM voltage can be calculated using Fourier Analysis:

$$f(t) = \sum_{n=-\infty}^{\infty} C_n e^{jn\omega_0 t} \tag{2.73}$$

$$C_n = \frac{1}{T}\int_0^T f(t) e^{-jn\omega_0 t} dt \tag{2.74}$$

The calculation results are:

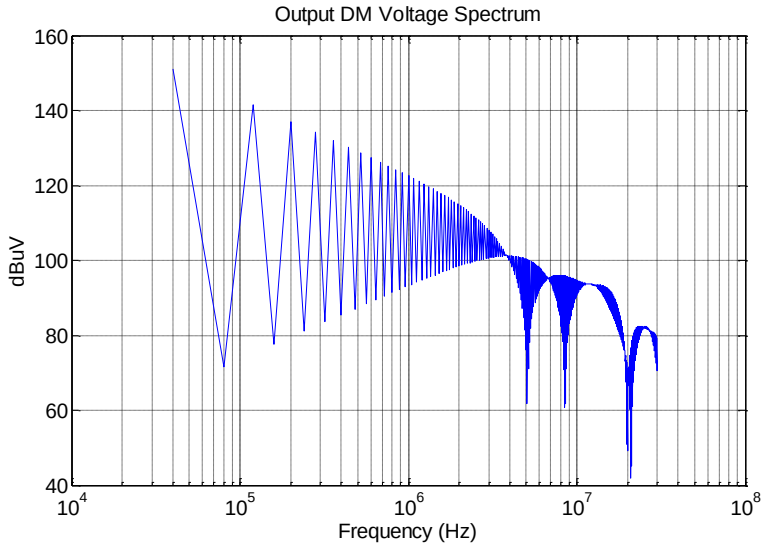

Fig. 2-59 Output side DM voltage spectrum of full bridge dc-dc converter.

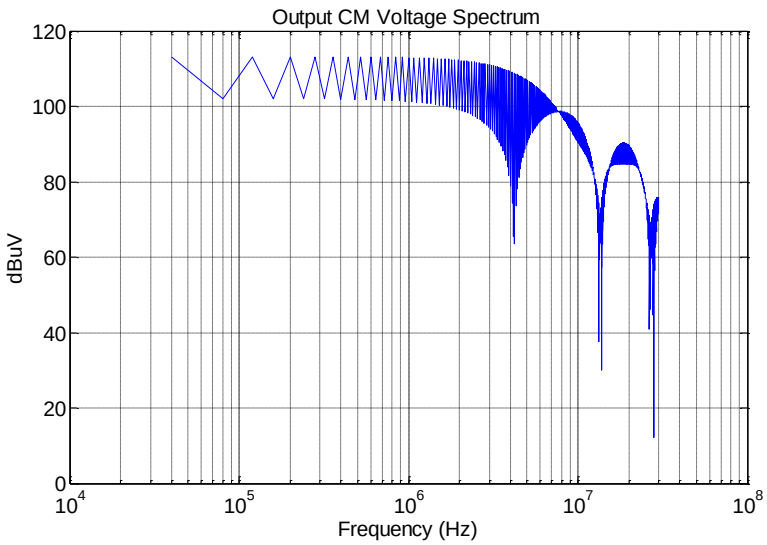

Fig. 2-60 Output side CM voltage spectrum of full bridge dc-dc converter.

Parasitic such as $C_{dg,}$ C_1, C_2 and C_{Lf} modeling methods is the same as discussed in previous sections.

With the parasitics, CM and DM equivalent circuit are:

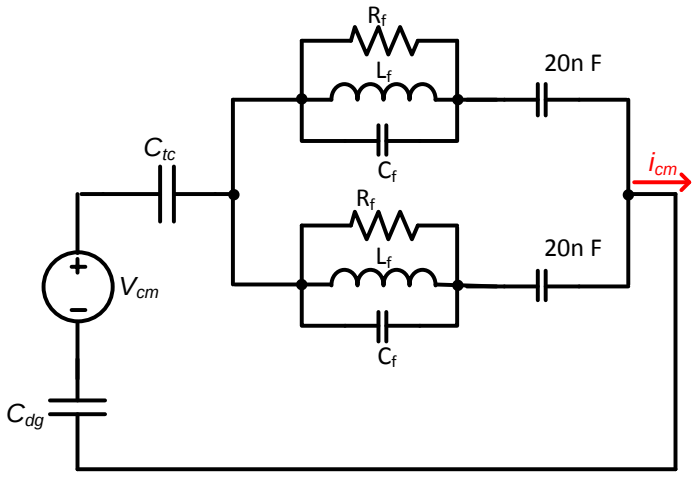

Fig. 2-61 Output side CM equivalent circuit of full bridge dc-dc converter.

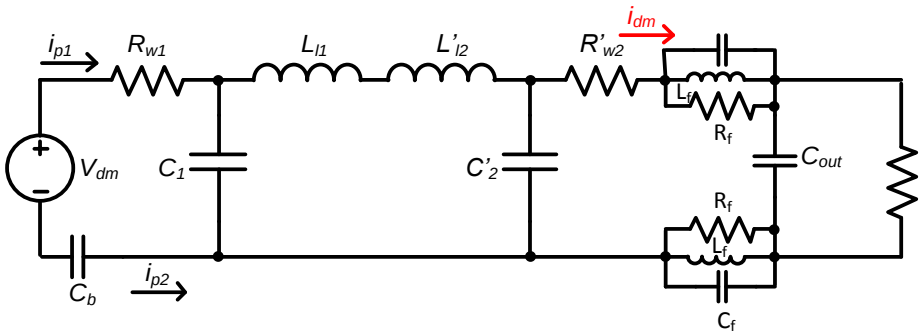

Fig. 2-62 Output side DM equivalent circuit of full bridge dc-dc converter.

Design of filter follows the same procedure as previous circuit discussed.

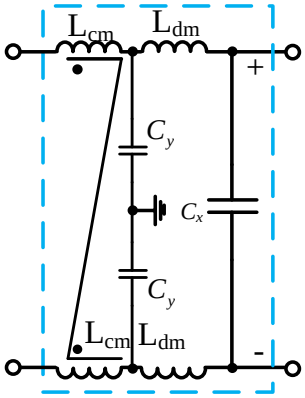

Fig. 2-63 One-stage LC EMI filter.

E. Input EMI Filter Design

For input side EMI filter, CM equivalent circuit is shown in Fig. 2-64.

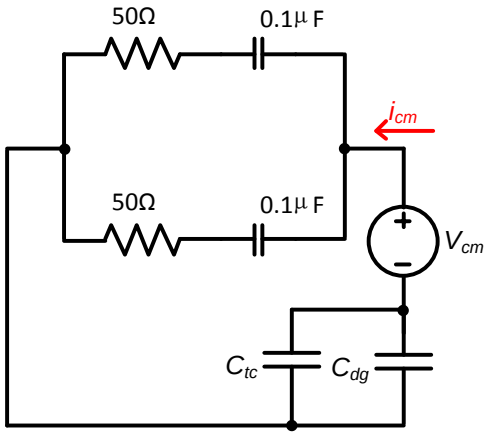

Fig. 2-64 Input side CM equivalent circuit of full bridge dc-dc converter.

For DM, equivalent circuit is shown in Fig. 2-65.

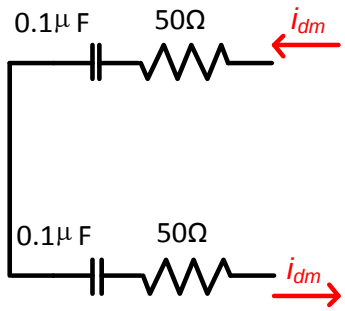

Fig. 2-65 Input side DM equivalent circuit of full bridge dc-dc converter.

Input side DM current is calculated from output side:

$$i_{dc} = s_{p1} \cdot i_{p1} + s_{p2} \cdot i_{p2} \tag{2.75}$$

$$s_{p1} + s_{p2} = 1 \tag{2.76}$$

s_{p1} and s_{p2} are the switching function of p1 and p2 leg. Sum of i_{p1} an i_{p2} are zero.

In frequency domain, spectrum of i_{dc} can be calculated as:

$$FFT(i_{dc}) = 2FFT(s_{p1}) \otimes FFT(i_{p1}) - FFT(i_{p1}) \tag{2.77}$$

The filter used for input EMI filter is shown in Fig. 2-66.

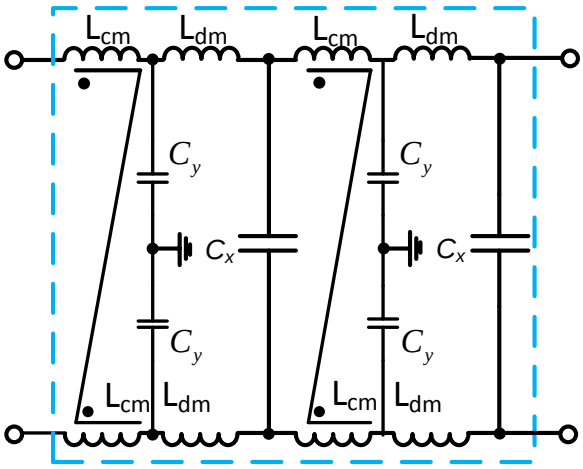

Fig. 2-66 Input EMI filter of full bridge dc-dc converter.

VIII. Summary

This chapter discussed the design procedure of five power converters commonly used in various electronic power conversion systems. They are three-phase two-level PWM boost rectifier, three-phase two-level PWM Vienna rectifier, voltage source inverter, single-phase PFC and full bridge dc-dc converter. Analytical design algorithm of power stage, energy storage passive components, cooling system and input output EMI filters for each converter have been discuss. Those algorithm can be programmed in computer software.

Chapter 3 Components Weight Estimation

I. Introduction

This chapter discuss how to estimation converter's weight by estimating sub-components' weight including power device, passive components such as inductor capacitor, cooling system weight including heat sink and fan. For some components such as power device and fan, small data base are built; for capacitor, linear relationship are found between weight and capacitance for film capacitor; for inductor transformer and heat sink, weight is calculated by physical design.

II. Power Device

Power devices used in study are IGBT, MOSFET, and diode.

IGBT module is used in three-phase two-level PWM boost rectifier and voltage source inverter.

Weight data based is built using Infineon 1200V six pack IGBT4 module.

TABLE 3-1 INFINEON 1200 SIX PACK IGBT WEIGHT

I_{rated} (A)	25, 35	50, 75	100, 150, 200	225, 300, 450
Package	AG-EASY1B	AG-ECONO2	AG-ECONO4	AG-ECONOPP
Weight (g)	24	180	400	930

MOSFET is used in three-phase three-level PWM Vienna rectifier, single-phase PFC and dc-dc converter. In this study, all the MOSFETs been used are from Infineon and have the same package type TO-220 which weight is 2.26 g.

SiC diode is used for single-phase PFC and full bridge dc-dc converter, all the SiC diodes are used from CREE and have the same package type TO-220 which weightis 2.0g.

Full brige diode rectifier module is used as front rectifier of single-phase PFC and the weight is list in the following table.

TABLE 3-2 FULL BRIDGE DIODE RECTIFIER

Pat No.	dfs	3n252	3kbp08m	gbl005	gbpc6	gbu8a
Weight	0.4	1.9	1.9	2.2	3.2	3.9

III. Passive components

A. Film Capacitor

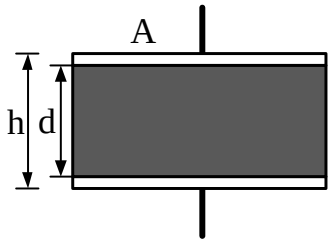

Fig. 3-1 Structure of film capacitor.

Fig. 3-1 shows the structure of the film capacitor, where the volume is dominated by the dielectric material [15]. One can do some simple derivation to determine the volume of the is:

$$V = A \cdot h \approx A \cdot d \tag{3.1}$$

The capacitance of the capacitor is:

$$C = \varepsilon \frac{A}{d} \tag{3.2}$$

The energy stored in the capacitor is:

$$W = \frac{1}{2} C U^2 = \frac{1}{2} \varepsilon \frac{A}{d} U^2 = \frac{1}{2} \varepsilon \frac{V}{d^2} U^2 = \frac{1}{2} \varepsilon V \left(E^*\right)^2 \tag{3.3}$$

One can see that the volume of the film capacitor is proportional to the energy stored in the capacitor. If the voltage is fixed, then the volume is proportional to the capacitance.

For 1100 V film capacitor from EPCOS, the following approximation is made:

$$W(g) = 3.61C(\mu F) \tag{3.4}$$

The X capacitor used in EMI filter is 1uF, Y capacitor is 6.8 nF their weight is approximated as 10g consider they are very small.

B. DM Inductor

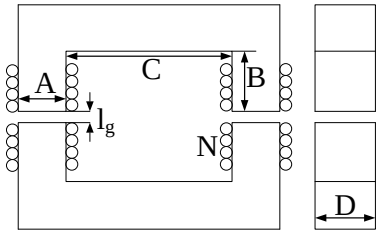

Fig. 3-2 CC core inductor.

A single-phase CC core structure, as shown in Fig. 3-2, is used to design the boost inductor in three-phase two-level PWM boost rectifier, three-phase three-level PWM Vienna rectifier, single-phase boost PFC and DM inductor for all EMI filters.

Once the core is selected, the inductance can be calculated by:

$$L = \mu_0 \cdot \frac{N^2 \cdot A_c}{l_g} \tag{3.5}$$

In (3.5), μ_o is the permeability of free space, N is the number of winding turns, A_c is the cross-section area of the core, and l_g is the gap length of the inductor.

The rated magnetic flux density of the core is calculated with the peak current I_{pk}, such that

$$B_{rated} = \frac{L \cdot I_{pk}}{N \cdot A_c} \tag{3.6}$$

The peak current must be smaller than the saturation flux density B_{sat} of the core.

The selection of the wire cross-section area should agree with

$$A_W \geq \frac{I_{rms}}{J_{MAX}} \tag{3.7}$$

In (3.7), J_{MAX} is the maximum current density constraint, and J_{rated} is the rated current density of the wire. The winding filling feasibility should be checked by:

$$K_u \cdot W_A > N \cdot A_w \tag{3.8}$$

In (3.8), W_A is the window area of the selected core, A_w is the cross-section area of the winding wire, and K_u is the fill factor for the wire fitted in the core window area.

The temperature rise is also a constraint for the inductor design. It is given by an empirical equation as:

$$\Delta T = 450 \cdot (\frac{P_{loss}}{A_t})^{0.826} \tag{3.9}$$

In (3.9), A_t is the equivalent heat dissipation area. P_{loss} includes the winding loss and the core loss, which is given by:

$$P_{loss} = P_{core} + P_{winding} \tag{3.10}$$

$$P_{winding} = I_{rms}^2 R \tag{3.11}$$

$$P_{core} = k \cdot f^a \cdot dB^b \cdot V_{core} \tag{3.12}$$

In (3.10), P_{core} is core loss, $P_{winding}$ is winding loss. In (3.11), I_{rms} is the winding current rms value. R is the winding resistance. In (3.12), dB is the variation of flux density, f is the frequency of flux dB, V_{core} is the volume of the core, k, a and b are the coefficients related to core material.

The total weight of the inductor is given by:

$$W_L = N \cdot MLT \cdot A_w \cdot \rho_w + V_{core} \cdot \rho_{core} \tag{3.13}$$

In (3.13), MLT is the mean length of the winding turns, and ρ_w and ρ_{core} are the densities for the wire and the core, respectively.

Instead of using commercial core, core dimension A, B, C, D and l_g are designed. Standard round magnetic wire are used, a small data base of core material and wire parameters are built.

TABLE 3-3 CORE AND WIRE PARAMETERS IN THE DATA BASE

Core loss parameter	k, a, b
Saturation flux density	B_{sat}
Permeability	μ_r
Core material density	ρ
Diameter of wire	D
Resistance per meter of wire	R
Insulation thickness of wire	d
Permittivity of Insulation	ε_r

C. CM Inductor

For the CM inductor, toroidal core based CM choke is designed as

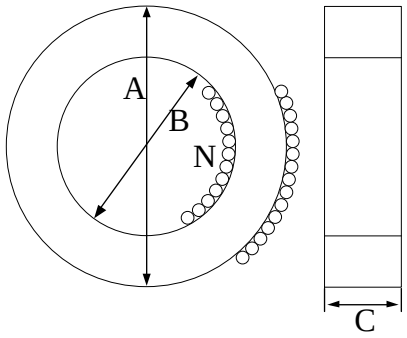

Fig. 3-3 Toroidal core inductor.

During the design of the common-mode choke, the following assumptions are made [13]:

1) Possible asymmetries, parasitic capacitances, and the effect of the tolerances are neglected;
2) The ambient temperature equals 45 ℃, and the maximum termperature rise is 100 ℃; and

3) A single winding layer is allowed to reduce parasitics.

Equations for the CM choke inductor design are listed below. The first step is to select a core size; then the self- inductance is given by:

$$L_{cm} = \mu_r \cdot \mu_0 \cdot \frac{A_c}{l_e} \cdot N^2 \tag{3.14}$$

In (3.14), μ_r is the initial permeability of the core material, μ_o is the permeability of free space, N is the number of winding turns, A_c is the cross-section area of the core, and $l_e$is the mean length of the core magnetic loop. L_{cm} is frequency dependent, as the permeability of the core material will vary with the frequency.

The next step is to calculate the maximum number of turns that will fit on this core. In order to constrain the intra-winding capacitance, we only consider a single-layer winding structure, which means that all the windings are wound around the core without overlapping. The maximum turns N_f is given by:

$$N_f = \frac{\pi(D_{ic} - D_w)}{3D_w\delta} \tag{3.15}$$

In (3.15), D_{ic} is the inner circumference of the core, D_w is the diameter of the wire, and δ is the filling factor, which is usually set to be 1.15. The number of winding turns should be less than N_f.

The leakage inductance L_{dm} is given by [40]:

$$L_{dm} = \mu_{effective} \cdot \frac{0.4\times10^{-8}\pi \cdot N^2 \cdot A_c}{l_e \cdot \sqrt{\left(\frac{\theta_1}{360} + \frac{\sin(\frac{\theta_1}{2})}{\pi}\right)}} \tag{3.16}$$

$$\theta_1 = 360\frac{N \cdot D_w \cdot \delta}{\pi \cdot (D_{ic} - D_w)}$$

$$\mu_{effective} = 2.5 \cdot \Gamma^{1.45} \quad (\mu_r > 5000)$$

$$\Gamma = \sqrt{\frac{\pi}{A_c}} \frac{l_e}{2}$$

In (3.15), θ_1 is the angle that a winding subtends on the core, Γ is a coefficient representing the core shape, $\mu_{effective}$ is the effective permeability of the DM flux path.

Loss of the common-mode choke includes the winding loss and core loss. Because of the three phases, the winding loss consists of three parts. Each part is calculated as:

$$P_{Cu} = I_{L,rms}^2 \cdot R_{Cu}$$

$$R_{Cu} = \frac{\rho_{Cu} \cdot l_{Cu}}{A_{Cu}} \tag{3.17}$$

The core loss is mainly caused by the common-mode choke leakage inductance, and can be calculated using the Steinmetz equation as shown in the DM inductor section.

The flux density saturation constraint, winding filling feasibility constraint, and temperature rise constraint need to be considered.

$$B_{leakage} = \frac{L_{DM} \cdot I_{pk}}{N \cdot A_c} < B_{sat}$$

$$K_u \cdot W_A > N \cdot A_W \tag{3.18}$$

$$\Delta T = 450 \cdot \left(\frac{P_{loss}}{A_t} \right)^{0.826}$$

Also, core dimension A, B, C are designed. Standard round magnetic wire are used, a small data base of core material and wire parameters are built. The parameters are shown in TABLE 3-3.

D. Transformer

EE core is used for transformer design as shown in Fig. 3-4.

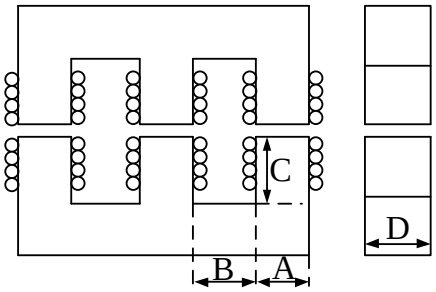

Fig. 3-4 EE core transformer.

Transformer design using area product equation:

$$A_p = \frac{kVA \times 1 \times 10^4}{1.5 K_f K_u B_m J f} \tag{3.19}$$

Primary winding number of turns:

$$N_p = \frac{V_{p\_ll} \times 1 \times 10^4}{K_f B_m A_c f} \tag{3.20}$$

Also, core dimension A, B, C D are designed. Standard round magnetic wire are used, a small data base of core material and wire parameters are built. The parameters are shown in TABLE 3-3.

IV. Cooling System

Forced-air cooling is considered in this study, and the structure of heat sink-fan system is shown in Fig. 3-5.

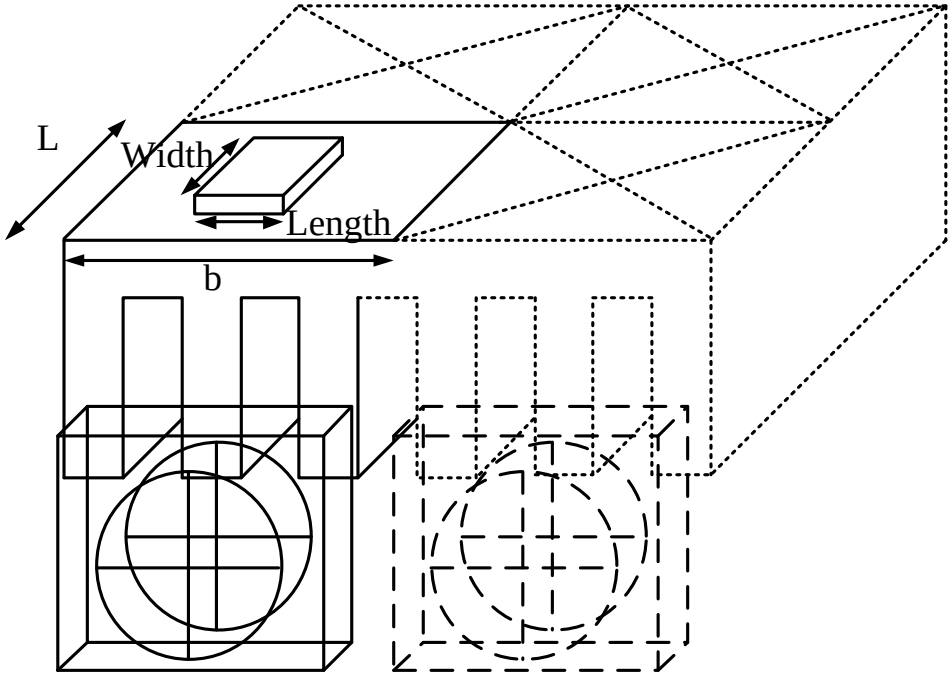

Fig. 3-5 Forced air cooling system.

As Fig. 3-5 shows, a flat-fin heat sink is used. The size of the heat sink and fan are chosen according to device module size.

A. Heat Sink

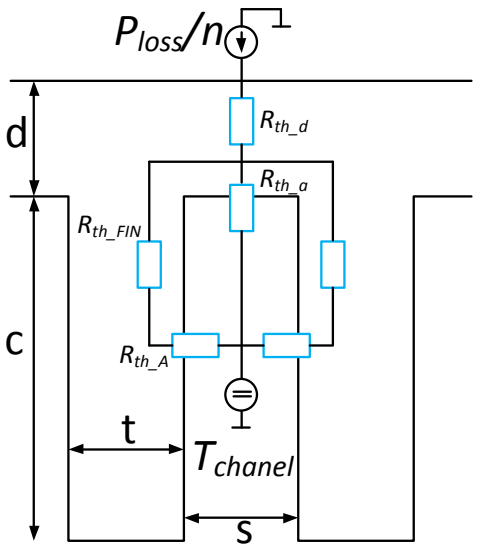

Fig. 3-6 Heat sink thermal resistance.

Heat sink thermal resistance can be calculated by [41]:

$$R_{th\_HS} = \frac{1}{n}\left(R_{th\_d} + \frac{1}{2}\left(R_{th\_FIN} + R_{th\_A}\right)\right) + \frac{0.5}{\rho_{air} c_{p,air} V} \tag{3.21}$$

ρ_{air} is the air density; $c_{p,air}$ is the specific thermal capacitance of air; V is air volume flow.

$$R_{th\_A} = \frac{1}{h \cdot L \cdot c} \tag{3.22}$$

h is convective heat transfer coefficient, L is heat sink channel length in air flow direction.

$$R_{th\_FIN} = \frac{\frac{1}{2}c}{\frac{1}{2}t \cdot L \cdot \lambda_{HS}} \tag{3.23}$$

λ_{HS} is thermal conductivity of heat sink material.

$$R_{th\_d} = \frac{d}{\frac{1}{n} A_{HS} \lambda_{HS}} \tag{3.24}$$

A_{HS} is the size of heat sink base plate.

$$h = \frac{Nu_m \cdot \lambda_{air}}{d_h} \tag{3.25}$$

Nu_m is Nusselt number. λ_{air} is thermal conductivity of air. d_h is hydraulic diameter of one channel.

$$k = \frac{s}{b/n} \tag{3.26}$$

$$d_h = \frac{2s \cdot c}{s + c} \tag{3.27}$$

$$k \cdot \Delta p_{Fan}(V) = \Delta p_{lam}(V_{lam}) \tag{3.28}$$

Δp is pressure drop in one channel.

$$\Delta p_{lam}(V) = \frac{48\rho_{air} v_{air} L}{n(s \cdot c) d_h^2} V \tag{3.29}$$

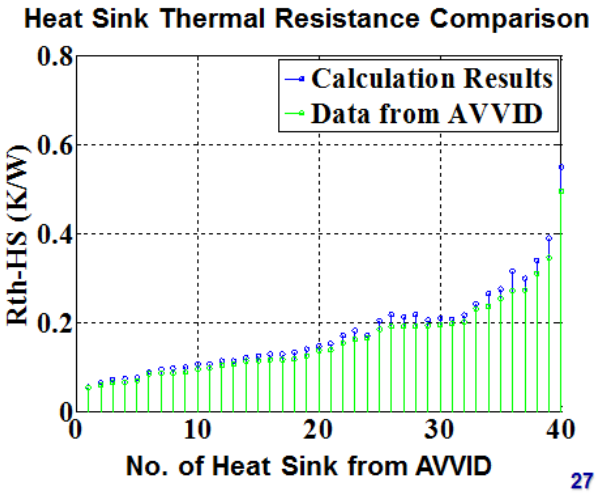

Fig. 3-7 Verification of heat sink design algorithm.

Fig. 3-7 shows a verification of the heat sink design method from [41] by calculating the thermal resistance of 40 heat sinks, and shows very good accuracy.

B. Fan

In forced air cooling system, fan operation point shows at around 80% of its maximum value, this assumption is made to avoid sovling the fan operation point as well as built the fan performance curve data bas.

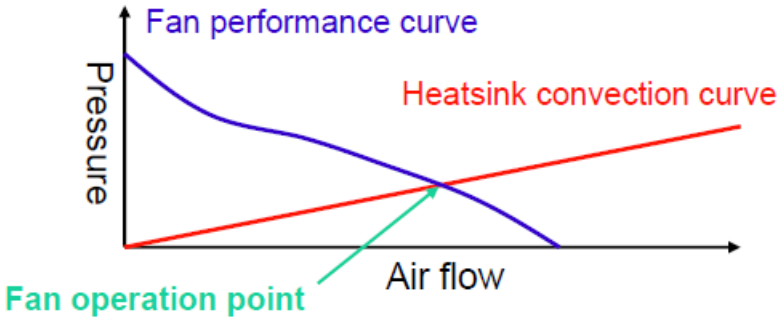

Fig. 3-8 Fan operation point.

Relationship between fan size and fan weight is set by using a serise of 12V dc fan from one manufancture.

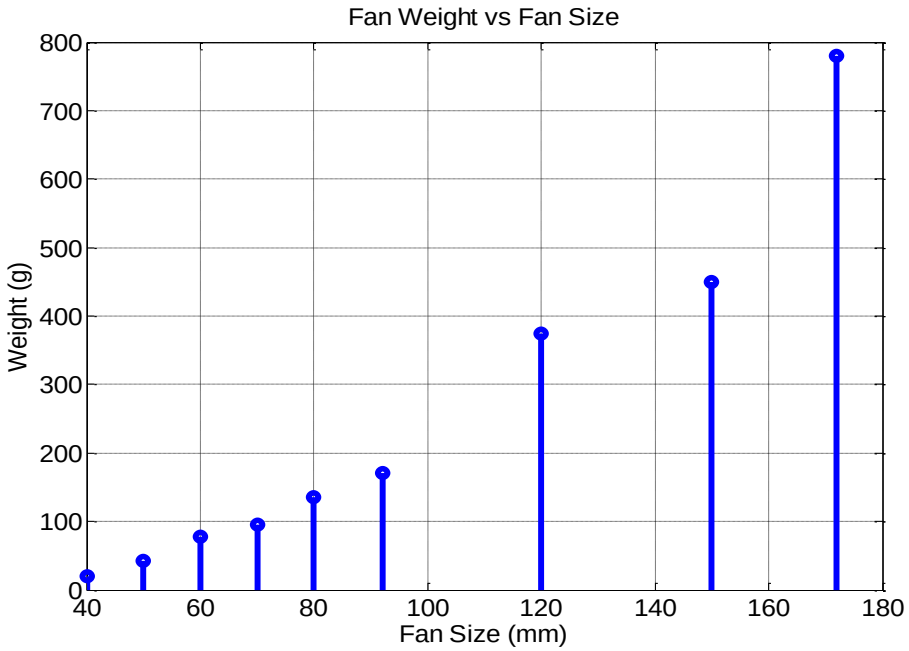

Fig. 3-9 Fan size and weight.

V. Verification

Two hardwares are measured for verification.

A. Case 1

The first hardware is a three-phase two-level PWM boost rectifier shown in Fig. 3-10. Real hardware picture is shown in Fig. 3-11, one phase-leg is shown.

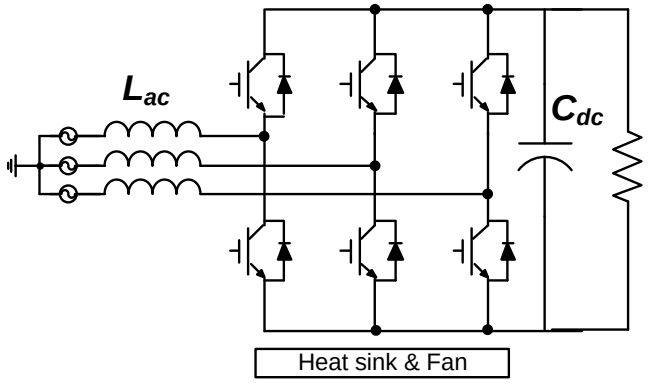

Fig. 3-10 Three-phase two-level PWM boost rectifier without EMI filter.

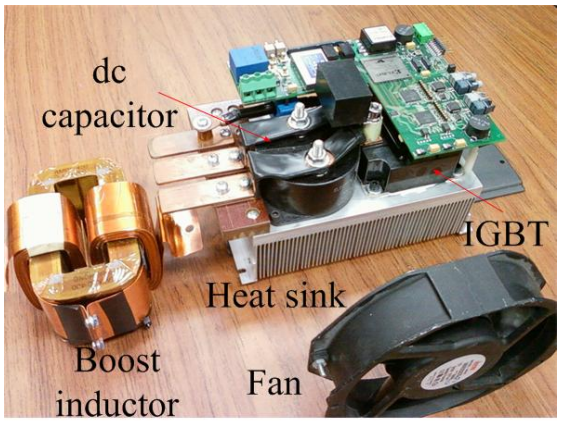

Fig. 3-11 One phase-leg of three-phase two-level PWM boost rectifier.

TABLE 3-4 CASE 1 RESULTS

	Hardware	Estimated
P (kW)	100	100
V_{in} (V) (line-line rms)	480	480
V_{dc} (V)	800	800
f_{line} (Hz)	60	60
f_{sw} (kHz)	20	20
L_{boost} (μH)	186	152
C_{dc} (μF)	105	83
Modulation	SVM	SVM
IGBT	PM300DVA120	FS300R12PT4
Loss(W)per module	1015	915
R_{thHS}(K/W)	0.028	0.073
Weight Inductor(kg)	12.9	12.3
Weight Cooling (kg)	8.7	3.7
Weight IGBT (kg)	2.2	1.0
Weight dc Cap (kg)	0.9	0.3
Sum (kg)	24.7	17.3

B. Case 2

The second hardware is a three-phase three-level PWM Vienna rectifier plus a voltage source inverter shown in Fig. 3-12. Real hardware picture is shown inFig. 3-13, one phase-leg is shown.

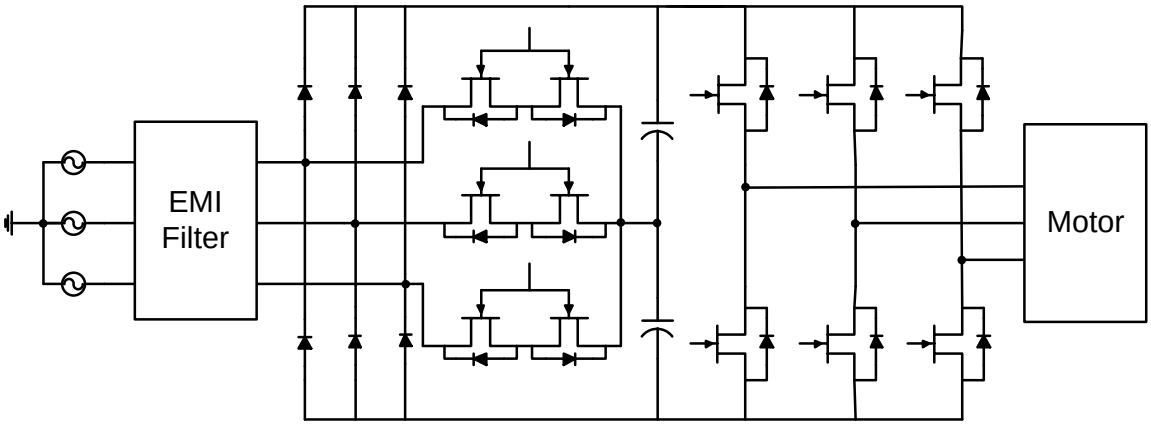

Fig. 3-12 Three-phase three-level Vienna rectifier with VSI.

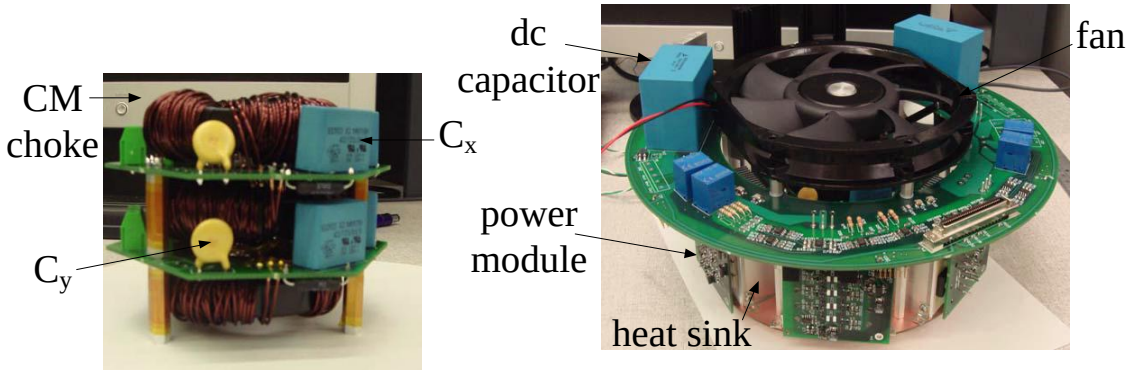

Fig. 3-13 EMI filter and converter of Vienna plus VSI converter.

TABLE 3-5 CASE 2 RESULTS

	Hardware	Estimated
P (kW)	10	10
V_{in} (V) (phase rms)	230	230
V_{dc} (V)	650	650
f_{line} (Hz)	400	400
f_{sw} (kHz)	70	70
L_{cm} (mH)	12	7.5
L_{dm} (µF)	100	79.4
C_x (µF)	1	1
C_y (nF)	10	6.8
C_{dc} (µF) (two series)	35	20
Modulation	SVM	SVM
Power Device	SiC JFET Diode	SiC JFET Diode
Loss(W) Vienna +VSI	150+134	142+125
R_{thHS}(K/W)	0.45	0.51
Weight Filter (kg)	0.513	0.432
Weight Cooling (kg)	1.198	1.052
Weight Device (kg)	0.120	0.120
Weight dc Cap (kg)	0.204	0.072
Sum (kg)	2.035	1.676

Chapter 4 Weight Estimation Tool and Sample System Comparison

I. Introduction

One of the objective of this study is to develop a software tool to automatically evaluate the system weight and compare different system structures. This tool should provide functions of estimating the weight of system and components then making a comparison between different architectures (e.g. between ac and dc). Users can input information such as the power and voltage rating, line frequency, physical parameters such as length, and environmental parameters such as altitude and temperature. This chapter introduces the weight estimation tool developed in MATLAB using algorithm discussed in the previous chapters. Then, weight of power distribution systems for data center with ac and dc bus are estimated and compared as an example.

II. Weight Estimation Tool

The weight estimation tool is build using MATLAB. As shows, the graphic user interface (GUI) of this tool has two parts.

The upper part of the screen is the system parameter setting panel, which includes four tabs; ‘AC SYSTEM’, ‘DC SYSTEM’, ‘INTRODUCTION’ and ‘LOGO’. On the ‘AC SYSTEM’ and ‘DC SYSTEM’ tabs, the system schematics are displayed, and each component’s parameter setting buttons are listed.

The bottom part of the screen is used to display weight estimation results. There are three tabs; ‘AC SYSTEM RESULTS’, ‘DC SYSTEM RESULTS’ and ‘ABOUT’. By pushing the button ‘Get Results’, user can have system components’ weight estimation results displayed in this area.

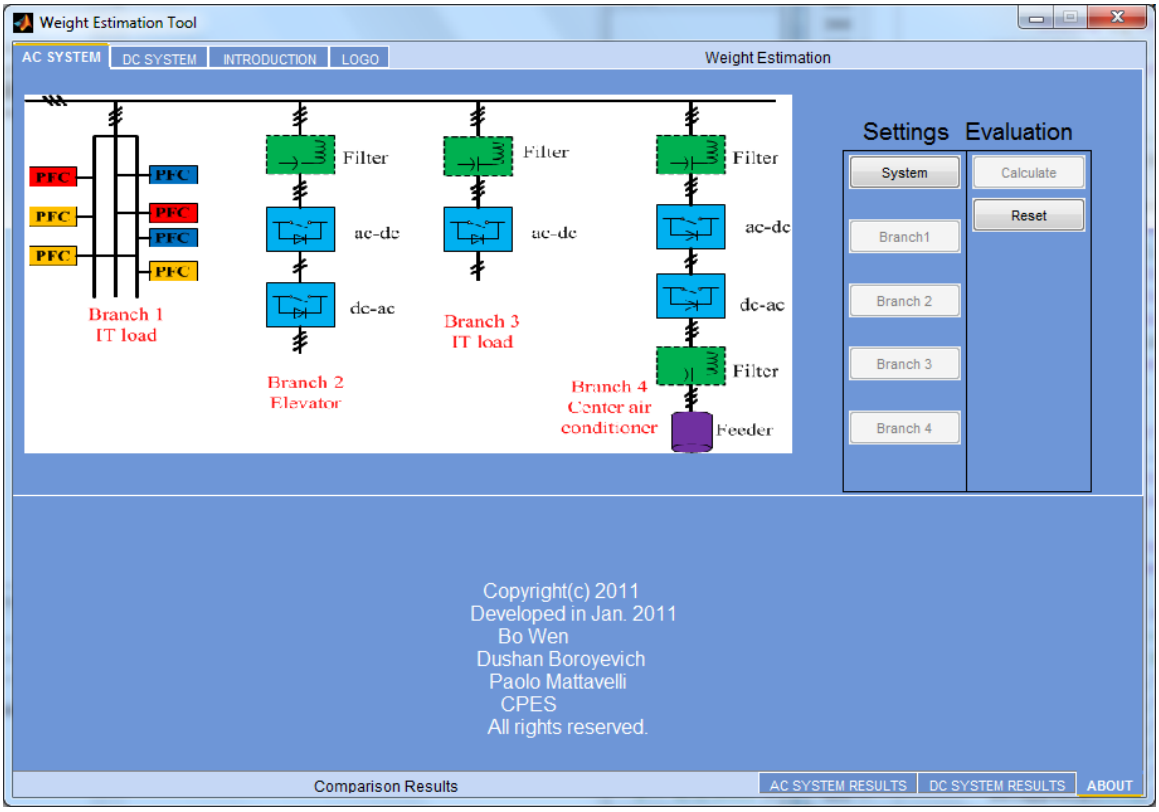

Fig. 4-1 GUI of weight estimation tool.

III. Sample System Comparison

In this part, the example is to compare ac and dc power distrubtion systems for data center application. There are three kinds of load, information technology (IT) equipment, elevator and airconditioner. For fair comparison, both systems have the same source which is the 220V 50 Hz ac utility, both systems have the same load rating. Total IT equipment power is 60 kW; elevator power rating is 10 kW; airconditioner power rating is 100 kW. Fig. 4-2 shows the structure of ac system. In ac system, 50 kW IT load is fed from 50 1 kW PFCs, another 10 kW is fed from three-phase three-level Vienna rectifier. Fig. 4-3 shows the structure of dc system. In dc system, utility power is rectified by a 180 kW three-phase two-level boost rectifier, the dc bus voltage is 600 V. 60 kW IT load is feeded from dc-dc converter. The detailed parameters of ac and dc systems are listed in

TABLE 4-1 and

TABLE 4-2.

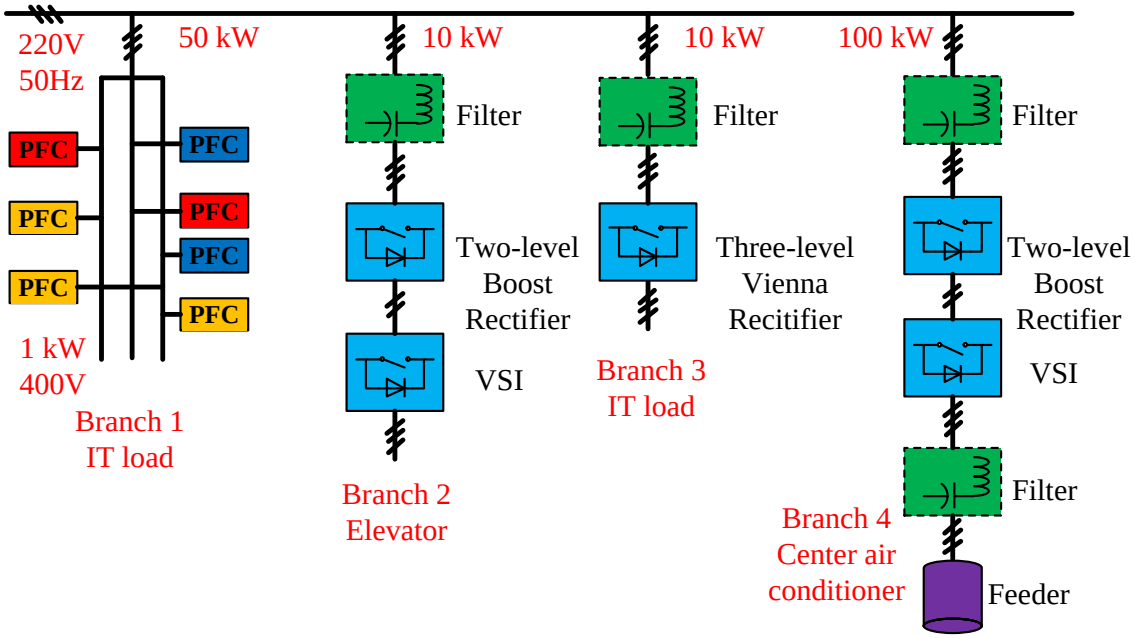

Fig. 4-2 Ac system of data center application.

TABLE 4-1 AC SYSTEM PARAMETERS

Line Frequency	50 Hz
Ac Bus Voltage	220 V rms
$T_{ambient}$	40 ℃
Branch 1 PFC	1 kW, V_{out} 400 Veach, total 50
Branch 2 Rectifier	10 kW, V_{dc} 600 V, f_{sw} 40 kHz
Branch 2 Inverter	10 kW, V_{out} 220 V rms, f_{out} 50 Hz, f_{sw} 40 kHz
Branch 3 Rectifier	10 kW, V_{out} ±400 V, f_{sw} 70 kHz
Branch 4 Rectifier	100 kW, V_{dc} 600 V, f_{sw} 20 kHz
Branch 4 Inverter	100 kW, V_{out} 220 V rms, f_{out} 50 Hz, f_{sw} 20 kHz, feeder 50 feet

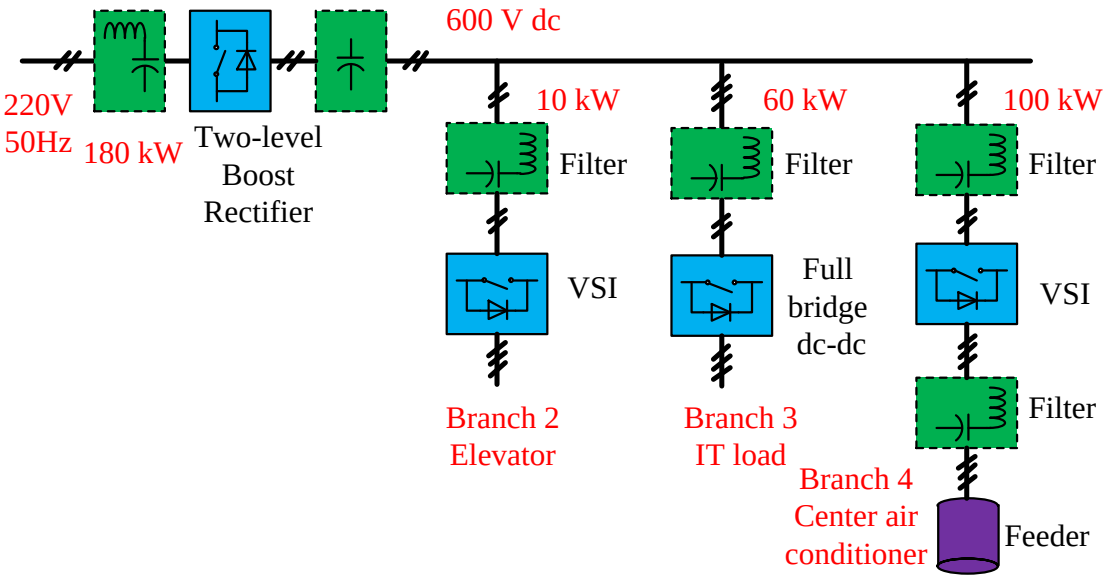

Fig. 4-3 Dc system of data center application.

TABLE 4-2 DC SYSTEM PARAMETERS

Line Frequency	50 Hz
Dc Bus Voltage	600 V
$T_{ambient}$	40 ℃
Bus Rectifier	180 kW, V_{dc} 600 V
Branch 2 Inverter	10 kW, V_{out} 220 V rms, f_{out} 50 Hz, f_{sw} 40 kHz
Branch 3 dc-dc	60 kW, V_{out} 400 V, f_{sw} 40 kHz
Branch 4 Inverter	100 kW, V_{out} 220 V rms, f_{out} 50 Hz, f_{sw} 20 kHz, feeder 50 feet

TABLE 4-3 AC AND DC SYSTEMS WEIGHT ESTIMATION RESULTS COMPARISON

	ac (kg)	dc (kg)
Bus rectifier	0	34.69
Branch 1	42.41	0
Branch 2	2.91	2.53
Branch 3	1.88	14.05
Branch 4	31.72	13.62
Sum	78.92	64.89

TABLE 4-3 shows the comparison results, dc system is lighter than ac system.

As the electrical power consumption increases, increasing the distribution voltages can reduce the current for a given distribution power, leading to smaller wire size. The classical example is automobile electrical system [8]. In the 1920s, the mean power demand of a internal-combustion-engine automobile was less than 100W. this power demand was met by a 6 V lead-acid battery. After Second World War, the battery voltage was increased to 12 V. From the late 90s, automobile industry is discussing to increase the voltage to 42 V.

While the higher voltages are generally beneficial to reducing the cable at the distribution voltage level, their impact on other components are not clear. Power converters are the major part of electronic power system, many components, such as power semiconductors, are voltage sensitive. Using the weight estimation procedure discussed in this study, the following example shows the impact of higher bus voltage on a motor drive. The specifications are:

TABLE 4-4 MOTOR DRIVE SPECIFICATIONS

Line Frequency	50 Hz
Power	50 kW
Dc Bus Voltage	400 V (Case 1), 600 V (Case 2), 800 V (Case 3)
Ac Voltage	146 V rms (Case 1), 220 V rms (Case 2 & 3)
Output cable	50 feet

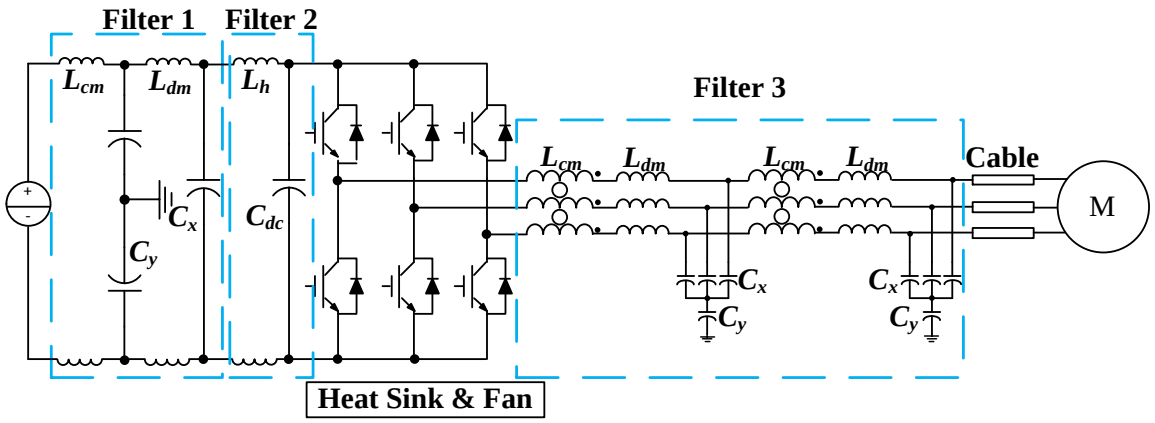

Fig. 4-4 Motor drive with input and output filter.

TABLE 4-5 WEIGHT BREAK DOWN OF 50 KW MOTOR DRIVE

	Filter1	Filter2	Device	Cooling System	Filter 3	Cable
Case 1	0.935 kg	0.235 kg	1.020 kg	1.291 kg	1.446 kg	2.152 kg
Case 2	0.746 kg	0.124 kg	0.480 kg	1.050 kg	0.964 kg	1.420 kg
Case 3	0.609 kg	0.082 kg	1.020 kg	2.637 kg	1.196 kg	1.420 kg

In TABLE 4-5, case 1 is with 146 V rms ac and 400 V dc voltage, the sum of components' weight is 7.079 kg; case 2 is with 220 V rms ac and 600 V dc voltage the sum of components's weight is 4.784 kg; case 3 is with 220 V rms and 800 V dc voltage the sum of components's weight is 6.964.

For case 1 1200 V IGBT FF200R12KT4 is used; for case 2, 1200 V IGBT FF150R12KT4 is used, for case 3, 1700 V IGBT FF150R17KE4 is used due to the increased dc voltage.

From case 1 to case 2, modulation index of VSI is keep the same as 1.03, so both ac and dc voltage are increased. The increase of dc voltage will increase the EMI noise source, but because of the corresponding decrease of current, weight of filters decrease. Also due to the decrease of current, samller current rating device is used, samller gauge wire is used for output cable, these components' weight decrease.

From case 2 to case 3, ac voltage is keeped to be 220V rms, dc voltage is creased from 600 V to 800 V. EMI noise source will increase, but for dc filter, the weight is decreasing due to the decreasing of current; for ac filter current is not decreasing, so weight of EMI filter increases. 1700 V IGBT has bigger weight compare to the same current rating 1200 V IGBT, and bigger loss, so cooling system weight also increases. Cable weight is the same for both case 2 and case 3 due to the same ac side current.

Power density (50 kW divided by component's weight) of filter 1 plus filter 2 for case 1 is 42.73 kW/kg; for case 2 is 57.47 kW/kg; for case 3 is 72.36. Power density of filter 3 for case 1 is 34.59 kW/kg; for case 2 is 51.86 kW/kg; for case 3 is 41.81. Power density of device plus cooling system for case 1 is 21.63 kW/kg; for case 2 is 32.67 kW/kg; for case 3 is 13.67 kW/kg. From these data one can find that increasing bus voltage gives benefit of increasing filter power density, power stage power density will be increased if the same voltage rating devices are used. If device voltage rating goes high, power stage power density will decrease. This is because of higher weight of higher voltage rating power device and its bad loss and thermal performance.

Chapter 5 Summary and Conclusion

A procedure of estimate weight of power converter has been developed. Weight estimation of power conversion system has been realized in software. Sample systems with ac and dc bus have been compared. The results show dc bus system is lighter than ac bus system. Power density of converter without filter changes mainly along with power ratings not voltage level. Lower power rating gives bigger power density.Power density of EMI filter increases when voltage level increases, but decreases when power level increases.

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