A 5-6 GHz Silicon-Germanium VCO with Tunable Polyphase Outputs

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(ABSTRACT)

In-phase and quadrature (I/Q) signal generation is often required in modern transceiver architectures, such as direct conversion or low-IF, either for vector modulation and demodulation, negative frequency recovery in direct conversion receivers, or image rejection. If imbalance between the I and Q channels exists, the bit-error-rate (BER) of the transceiver and/or the image rejection ratio (IRR) will quickly deteriorate. Methods for correcting I/Q imbalance are desirable and necessary to improve the performance of quadrature transceiver architectures and modulation schemes.

This thesis presents the design and characterization of a monolithic 5-6 GHz Silicon Germanium (SiGe) inductor-capacitor (LC) tank voltage controlled oscillator (VCO) with *tunable* polyphase outputs. Circuits were designed and fabricated using the Motorola 0.4 μm CDR1 SiGe BiCMOS process, which has four interconnect metal layers and a thick copper uppermost bump layer for high-quality radio frequency (RF) passives.

The VCO design includes full-wave electromagnetic characterization of an electrically symmetric differential inductor and a traditional dual inductor. Differential effective inductance and Q factor are extracted and compared for simulated and measured inductors. At 5.25 GHz, the measured Q factors of the electrically symmetric and dual inductors are 15.4 and 10.4, respectively. The electrically symmetric inductor provides a measured 48% percent improvement in Q factor over the traditional dual inductor.

Two VCOs were designed and fabricated; one uses the electrically symmetric inductor in the LC tank circuit while the other uses the dual inductor. Both VCOs are based on an identical cross-coupled, differential pair negative transconductance ($-G_M$) oscillator topology. Analysis and design considerations of this topology are presented with a particular emphasis on designing for low phase noise and low-power consumption. The fabricated VCO with an electrically symmetric inductor in the tank circuit

tunes from 4.19 to 5.45 GHz (26% tuning range) for control voltages from 1.7 to 4.0 V. This circuit consumes 3.81 mA from a 3.3 V supply for the VCO core and 14.1 mA from a 2.5 V supply for the output buffer. The measured phase noise is -115.5 dBc/Hz at a 1 MHz offset and a tank varactor control voltage of 1.0 V. The VCO figure-of-merit (FOM) for the symmetric inductor VCO is -179.2 dBc/Hz, which is within 4 dBc/Hz of the best reported VCO in the 5 GHz frequency regime. The die area including pads for the symmetric inductor VCO is 1 mm $\times$ 0.76 mm. In comparison, the dual inductor VCO tunes from 3.50 to 4.58 GHz (27% tuning range) for control voltages from 1.7 to 4.0 V. DC power consumption of this circuit consists of 3.75 mA from a 3.3 V supply for the VCO and 13.3 mA from a 2.5 V supply for the buffer. At 1 MHz from the carrier and a control voltage of 0 V, the dual inductor VCO has a phase noise of -104 dBc/Hz. The advantage of the higher Q symmetric inductor is apparent by comparing the FOM of the two VCO designs at the same varactor control voltage of 0 V. At this tuning voltage, the dual inductor VCO FOM is -166.3 dBc/Hz compared to -175.7 dBc/Hz for the symmetric inductor VCO — an improvement of about 10 dBc/Hz. The die area including pads for the dual inductor VCO is 1.2 mm $\times$ 0.76 mm.

In addition to these VCOs, a tunable polyphase filter with integrated input and output buffers was designed and fabricated for a bandwidth of 5.15 to 5.825 GHz. Series tunable capacitors (varactors) provide phase tunability for the quadrature outputs of the polyphase filter. The die area of the tunable polyphase with pads is 920 μm $\times$ 755 μm. The stand-alone polyphase filter consumes 13.74 mA in the input buffer and 6.29 mA in the two output buffers from a 2.5 V supply. Based on measurements, approximately 15° of I/Q phase imbalance can be tuned out using the fabricated polyphase filter, proving the concept of tunable phase. The output varactor control voltages can be used to achieve a potential $\pm 5°$ phase flatness bandwidth of 700 MHz. To the author's knowledge, this is the first reported I/Q balance tunable polyphase network.

The tunable polyphase filter can be integrated with the VCO designs described above to yield a quadrature VCO with phase tunable outputs. Based on the above designs I/Q tunability can be added to VCO at the expense of about 6 mA. Future work includes testing of a fabricated version of this combined polyphase VCO circuit.

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Chapter 1

Introduction

Mobile communication systems are moving rapidly from supporting voice only towards integrating digital data and multimedia transmissions as well. Thus, the projected applications for wireless technology are expanding beyond simple cellular phone handsets to include: wireless internet connectivity in automobiles, cellular handsets, and personal data assistants (PDAs); position location and navigation for on-board computers in automobiles; wireless data networks; and wireless computer peripherals [1]. The push for wireless capabilities in the consumer market, in particular, is therefore accompanied by the demand for low-cost, wireless transceivers.

Over the past three decades, the number of transistors in silicon (Si) based integrated circuits (ICs) has doubled about every 18 months. This well-known trend is referred to as "Moore's law," after Gordon E. Moore of the Intel Corporation. Moore recognized the trend in 1965 and saw nothing to inhibit the same rate of growth for at least five years from that time [2]. However, the trend has continued into the 21st century. Moore's primary intent for predicting future levels of integration was to push the improvement of the microprocessor. Thus, the research and development investments to keep on track with Moore's law have typically focused on digital applications. The corresponding economy-of-scale for Si digital ICs has, therefore, dramatically reduced the cost of microprocessors. On the other hand, Si has not been the ideal semiconductor for high frequency analog applications. Radio frequency ICs (RFICs) and monolithic microwave ICs (MMICs) have historically used compound semiconductors synthesized from elements in columns III and V of the periodic table (III-V semi-

conductors). III-V semiconductors have characteristically high electron mobilities and are readily grown as semi-insulating substrates — features which are ideal for high frequency applications. However, high-speed analog and wireless ICs have recently sought to take advantage of the same Si economy-of-scale in an effort to reduce cost. The potential for high integration and lower cost has spurred research and advances in Si-based technologies that include both bipolar and submicron complementary metal-oxide silicon (CMOS) devices (BiCMOS technologies). The relatively recent introduction of the silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) further enhances BiCMOS technologies.

The ongoing push for higher levels of RF integration is the primary factor driving down the cost of wireless receivers. For example, to reduce the production cost of a wireless handset, designers aim to integrate more of the receiver architecture onto a single chip, thus reducing the total number of parts on the bill of materials. Direct conversion receivers (DCRs) and low intermediate-frequency (low-IF) receivers offer the prospect of integrating the RF front-end on chip with baseband digital signal processing (DSP) and microprocessor control [3],[4],[5]. Advancements in Si RFICs, coupled with the continued increase in speed and density of digital ICs, has placed within reach the very real possibility of a single-chip radio transceiver [6].

One frequency regime of current interest for fully-integrated RF transceivers is the Unlicensed National Information Infrastructure (U-NII) band — 300 MHz of spectrum located at 5.15-5.35 GHz and 5.725-5.825 GHz. The Federal Communications Commission (FCC) allocated this band in 1997 for short-range, wireless data transmission in the United States. Two years later, the Institute of Electrical and Electronics Engineers (IEEE) established the IEEE 802.11a standard for wireless local area networks (WLANs) in the U-NII band. The possibility of ubiquitous and untethered ethernet connectivity has created a growing demand for low-cost wireless transceivers in this spectrum.

Given the context of low-cost RF transceivers in the 5-6 GHz range, this chapter first provides an overview of receiver architectures that facilitate higher levels of integration. As this thesis will focus on one critical component, the voltage controlled oscillator (VCO), the second section of this chapter discusses major aspects of VCO design. Finally, this chapter concludes with the basics of SiGe heterojunction bipolar transistors (HBTs), the device technology used in this work.

1.1 Receiver architectures

The traditional superheterodyne receiver down-converts a RF signal to baseband in two or more mixer stages. Each mixer stage converts the received signal to an intermediate frequency (IF) for filtering and amplification before final mixing to baseband. Typically, a superheterodyne architecture has two IFs before converting to baseband (e.g. 70 MHz and 455 kHz). The IF is defined as:

$$f_{IF} = |f_{RF} - f_{LO}|, \tag{1.1}$$

where f_{RF} and f_{LO} are the frequency of the RF and local oscillator (LO) mixer input signals, respectively. A major limiting factor in achieving high levels of integration with this architecture is the presence of *image* frequencies resulting from mixing to each IF stage. An image is defined as a frequency other than the signal of interest that mixes to the same IF as the desired signal. Down-conversion of two different frequencies to the same IF occurs because the mixer does not recognize the *polarity* of the frequency difference between the RF and LO. Therefore, if the RF signal is located one IF higher than the LO (low-side injection), the image frequency is located at:

$$f_{im} = f_{LO} - f_{IF} = f_{RF} - 2f_{IF}. \tag{1.2}$$

If the RF signal is located one IF lower than the LO (high-side injection), the image frequency is located at:

$$f_{im} = f_{LO} + f_{IF} = f_{RF} + 2f_{IF}. \tag{1.3}$$

The processes of image rejection and channel selection require filters with steep roll-off and very high out-of-band rejection to attenuate unwanted signals before mixing in the superheterodyne architecture. These filters require resonators with high Quality (Q) factors and multiple poles to meet the stringent filter requirements. The low Q factor of on-chip inductors results in prohibitively high passband insertion loss for multiple-poled integrated inductor and capacitor (LC) filters. Furthermore, since monolithic inductors and capacitors require a great deal of die area, multiple pole LC filters quickly become excessively large for on-chip integration.

1.1.1 Direct Conversion Receivers (DCRs)

An alternative to the multi-stage down-conversion of the superheterodyne approach is to mix directly from RF to baseband (i.e., $f_{LO} = f_{RF}$). This approach is called direct conversion, homodyne, or zero-IF. A great deal of recent research has been focused on DCRs [7],[8],[9]. Since the signal is its own image, off-chip image rejection filters can be eliminated. In addition, channel selection can be performed at baseband, further reducing filter requirements. The elimination of off-chip filters allows DCRs to attain a higher level of integration for the RF front-end.

Despite the above advantages, DCRs present several obstacles making them challenging to implement [10]. One of these problems is known as *self-mixing*. LO leakage from the mixer can be reflected back into the mixer from the output of the LNA, the IC package, the antenna, or even the environment around the receiver. For fundamental direct conversion, the LO is at the same frequency as the RF signal, so these LO reflections combine with the RF signal, pass through the LNA, and self-mix to create a DC offset. Self-mixing can also occur when a large interferer leaks from the RF path to the LO input of the mixer. These DC offsets may be difficult to eliminate; in some cases they may vary with time due to changes in the LO reflections or interferers as the receiver itself or objects in the surrounding environment move.

In addition, low frequency noise makes it difficult to achieve low noise figures in direct conversion receivers. The low frequency noise of transistors is called "$1/f$ noise" because it has a $1/f$ slope versus frequency. For DCRs, this results in higher receiver noise figures because the output frequency of the mixers lies within the $1/f$ noise region. More noise at the receiver output requires more gain and lower noise figure in the components at the input to attain the required overall noise figure for a particular application.

Another implementation challenge for DCRs is in-phase and quadrature (I/Q) mismatch. Direct conversion requires the signal to be down-converted into separate I and Q channels to recover the negative and positive frequency components of the signal. If the gain and phase of these two channels are not identical, the output of the receiver will have an I/Q mismatch, resulting in errors in the recovery of the transmitted data. The effects of I/Q mismatch are discussed in greater detail in Section 1.1.3.

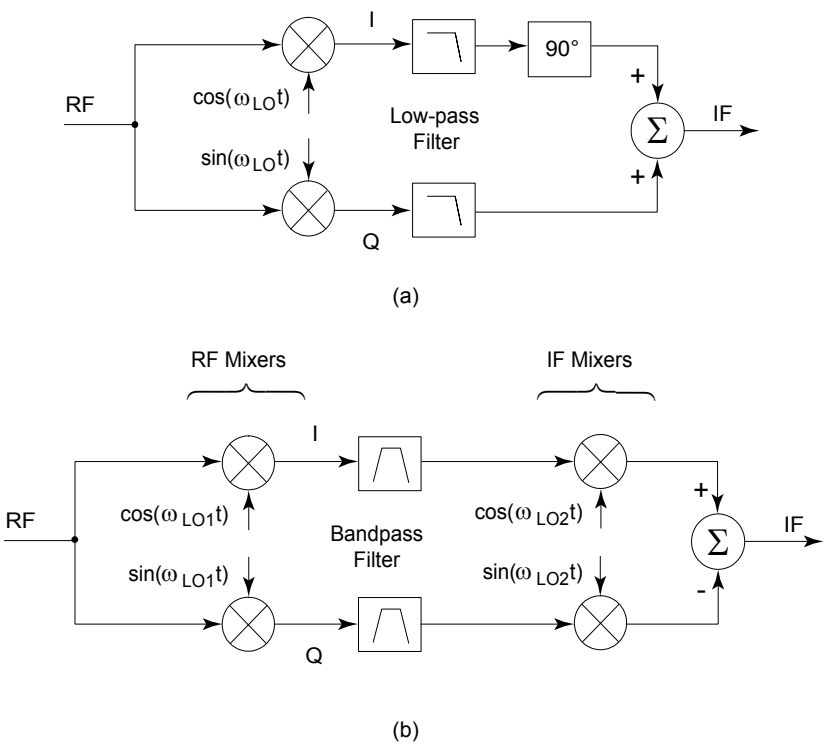

Figure 1.1: Block diagrams of the (a) Hartley and (b) Weaver image rejection architectures.

1.1.2 Low-IF or Digital-IF Receivers

The low-IF receiver is an alternative to the DCR which avoids the problems of DC offsets and $1/f$ noise, but which still allows high degrees of integration [3],[4]. As in a superheterodyne receiver, the RF and LO inputs to the down-conversion mixer of a low-IF receiver differ in frequency by a non-zero IF. However, low-IF receivers have an IF low enough to be easily sampled by an analog-to-digital converter (ADC). Thus, this approach is sometimes called digital-IF. Once in the digital domain, the signal can be filtered and converted to baseband using a DSP.

On the other hand, low-IF receivers, while avoiding DC offset issues, have the same image problem as superheterodyne architectures. Image canceling architectures, such as the Hartley or the Weaver (Figure 1.1), can be used for low-IF receivers to avoid the need for expensive off-chip image-reject filters. These image rejection architectures are not typically used for conventional receivers due to design limitations involving the bandpass and lowpass filters (Figure 1.1). Inductor and capacitor values for passive

filters at the IF are too large to be implemented on chip, so operational amplifier based active filters should be used. However, traditional IFs oftentimes exceed the slew rate limitation and/or unity gain frequency of standard operational amplifiers. By decreasing the IF to a suitable range for the operational amplifier, active filters can be used in low-IF receivers to implement either the Hartley or Weaver image rejection architectures.

Mathematically, both of these architectures rely on the following two trigonometric identities:

$$2\cos(\omega_{LO})\cos(\omega_{RF}) = \cos(\omega_{LO} + \omega_{RF}) + \cos(\omega_{LO} - \omega_{RF}) \tag{1.4}$$

$$2\cos(\omega_{LO})\sin(\omega_{RF}) = \sin(\omega_{LO} + \omega_{RF}) - \sin(\omega_{LO} - \omega_{RF}) \tag{1.5}$$

Both the Hartley and Weaver architectures take advantage of the polarity difference in equations 1.4 and 1.5 by using quadrature mixers to process the signal and image differently. As will be described below, in each case the down-conversion process preserves the input signal and cancels the image.

Hartley Architecture

The Hartley architecture employs quadrature mixers that separate the signal into I and Q channels. The branches undergo a relative 90° phase shift and the two channels are summed to produce an image-free output [Figure 1.1(a)]. The 90° phase shift is implemented in practice with an *RC-CR* or polyphase network.

Assuming low-side injection, the input is $x(t) = A\cos(\omega_S t) + B\cos(\omega_{im} t)$, where $\omega_{im} = \omega_S - 2\omega_{IF}$ and ω_S is the signal frequency. After mixing with the quadrature LO, the output of the low-pass filters is:

$$x_{I\ LPF}(t) = \frac{A}{2}\cos(\omega_S - \omega_{LO})t + \frac{B}{2}\cos(\omega_{LO} - \omega_{im})t \tag{1.6}$$

$$x_{Q\ LPF}(t) = \frac{A}{2}\sin(\omega_S - \omega_{LO})t - \frac{B}{2}\sin(\omega_{LO} - \omega_{im})t. \tag{1.7}$$

Using the trigonometric identity, $\cos(\omega + 90°) = \sin(\omega)$, the 90° phase shift converts

equation 1.6 to:

$$x_{I\ 90}(t) = \frac{A}{2}\sin(\omega_S - \omega_{LO})t + \frac{B}{2}\sin(\omega_{LO} - \omega_{im})t. \tag{1.8}$$

Finally, summing equations 1.7 and 1.8 results in an image-free output:

$$x_{IF}(t) = A\sin(\omega_S - \omega_{LO})t. \tag{1.9}$$

The image rejection ratio (IRR), a measure of the receiver's ability to suppress images, depends on the accuracy of the 90° phase shift over the signal bandwidth and the gain balance of the I and Q channels.

Weaver Architecture

The Weaver architecture also has quadrature mixers for separate I and Q channels, but uses two IF stages [Figure 1.1(b)]. A second set of mixers is used to process the image through the I and Q channels so that it is cancelled out at the output summer at the second IF. In a sense, the second stage of I and Q mixing provides the 90° phase shift function present in the Hartley architecture.

Figure 1.2 shows a graphical frequency analysis of the image rejection process. The RF signal (f_s) and image ($f_{im1} = f_{LO1} - f_{IF1}$) are converted to the first IF ($f_{IF1} = f_s - f_{LO1}$) by quadrature mixers without any image filtering. At this point, the image and the signal are at the same frequency. However, in the Q channel, the signal and image are located on the imaginary axis and have opposite polarities. A bandpass filter is often used to pass the desired mixing product and attenuate a secondary image ($f_{im2} = 2f_{LO2} - f_s - 2f_{LO1}$), which is caused by the second pair of quadrature mixers. At the second IF ($f_{IF2} = f_s - f_{LO1} - f_{LO2}$), the signal, first image, and second image are located at the same frequency and have the same polarity in the I channel. Meanwhile, in the Q channel, the second set of mixers converts the signal, first image, and second image from the imaginary axis back to the real axis. Most importantly, the signal and second image continue to have opposite polarity to the first image. The Q channel is then subtracted from the I channel to cancel the first image. The IRR of the Weaver architecture depends on the gain and phase balance of the I and Q channels. It should be noted that the only protection the Weaver architecture

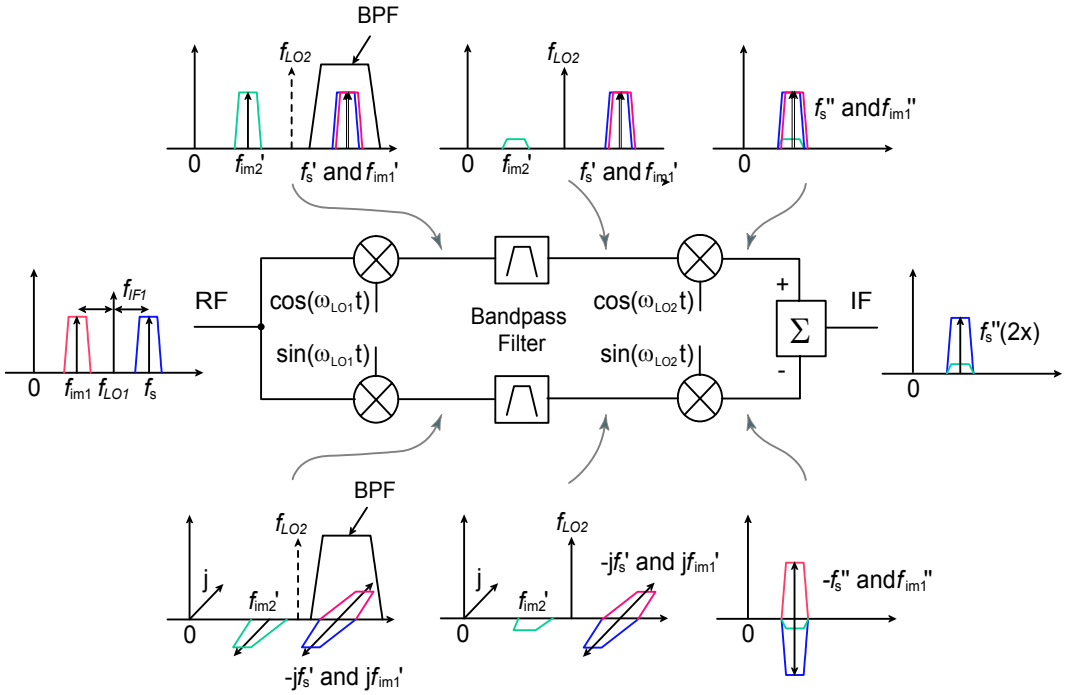

Figure 1.2: A graphical analysis of the Weaver image rejection architecture.

provides against the second image is either the out-of-band rejection of the filters shown in Figure 1.2 or, if possible, frequency planning to position the second image where no signal exists.

1.1.3 In-phase and Quadrature (I/Q) Balance

I/Q imbalance is caused by both gain error, ϵ, and phase error, θ. For example, a quadrature phase shift keyed (QPSK) input signal to a DCR can be represented as [11]:

$$x(t) = a\cos\omega_C t + b\sin\omega_C t, \tag{1.10}$$

where ω_C is the carrier frequency and a and b are ± 1, representing a stream of binary data. The RF signal experiences gain and phase error as it is amplified and converted to baseband. I/Q gain and phase error in the quadrature LO signal to the RF mixer can be represented by the following equations [11]:

$$x_{LO\ I}(t) = 2\cos\omega_C t \tag{1.11}$$

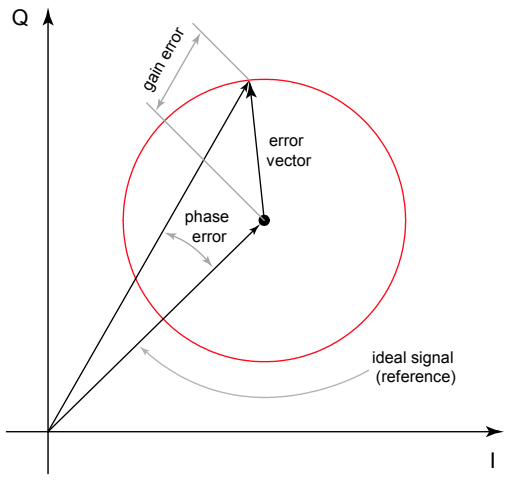

Figure 1.3: First quadrant of a signal constellation graph showing I/Q mismatch with gain and phase error.

$$x_{LO\,Q}(t) = 2(1+\epsilon)\cos(\omega_C t + \theta) \tag{1.12}$$

where the factors of 2 are included to simplify the development. After the RF signal is converted to baseband and filtered, the gain and phase error are manifested in the received data as [11]:

$$x_I(t) = a \tag{1.13}$$

$$x_Q(t) = b(1+\epsilon)\cos\theta + a(1+\epsilon)\sin\theta. \tag{1.14}$$

When equations 1.13 and 1.14 are plotted on a signal constellation graph, the effects of gain and phase error can be seen (Figure 1.3). The constellation points can move closer to the edges of the respective decision regions, reducing the amount of noise needed to result in a bit decision error. As a result, the bit-error-rate (BER) directly increases with the introduction of gain and phase imbalance in the I and Q channels.

A system level simulation of the Weaver architecture [Figure 1.1(b)] reveals some interesting relationships between the I/Q phase error of the two LO sources. As shown in Figure 1.4, the image rejection quickly deteriorates if the phase error of ω_{LO2} varies from 0° with no phase error in ω_{LO1}. However, if the phase error of ω_{LO1} is *tuned* to track the phase error of the ω_{LO2}, the quality of the image rejection is maintained. Image rejection remains within 3 dB of its minimum for I/Q phase errors up to 40° when such compensation is used. Without compensation, the image

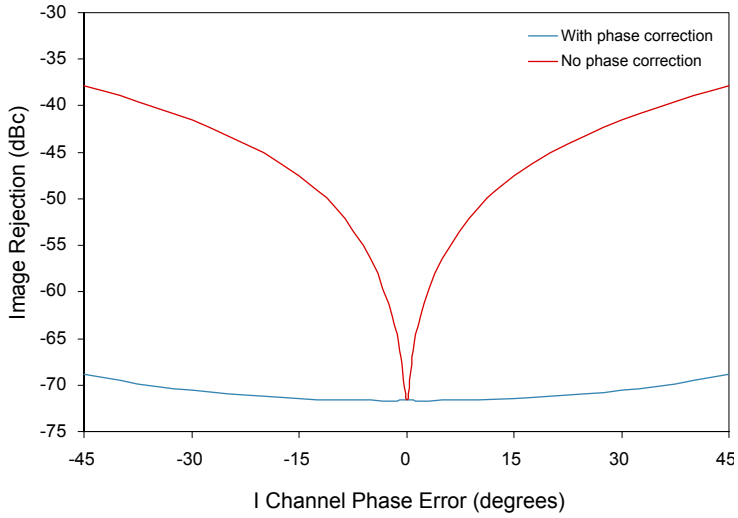

Figure 1.4: Image rejection with and without I/Q phase correction from a system level simulation of a Weaver architecture receiver.

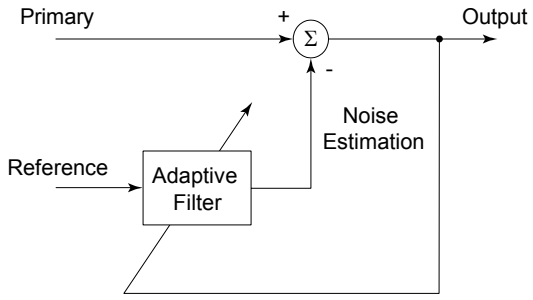

Figure 1.5: Block diagram of noise cancellation using an adaptive filter (after [15]).

rejection varies by 3 dB for phase errors less than 1°.

Several DSP based approaches to compensate for I/Q imbalance have been proposed [12],[13],[14]. I/Q imbalance compensation algorithms normally use adaptive interference cancellation to subtract an interference component from the desired signal component in baseband. The interference component is obtained by adaptive filtering an uncorrelated reference signal (Figure 1.5). In quadrature receivers, the two channels can serve as the primary and reference signals in Figure 1.5 to determine the I/Q imbalance interference component. For example, if the I channel is the primary input, the Q channel is the reference, or vice versa.

An analog approach to I/Q phase balance is potentially desirable for several reasons.

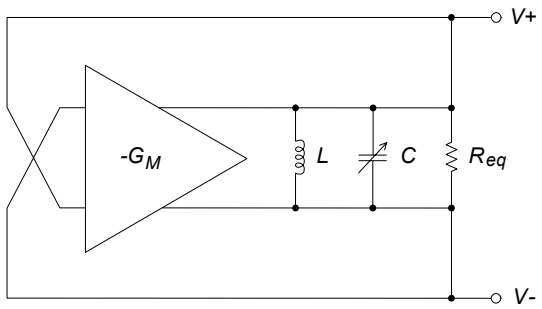

Figure 1.6: Block diagram of a negative transconductance ($-G_M$) voltage controlled oscillator.

The adaptive filters needed to correct gain and phase balance are iterative. Thus, the multiple iterations required before phase balance is acquired introduce latency into the system. Analog tuning of the I/Q phase balance would reduce the DSP computation requirements and could reduce overall power consumption of an integrated RF receiver. *Therefore, a primary goal of this thesis is to design a phase tunable VCO which can be used to eliminate I/Q phase error in low-IF receivers and DCRs or to improve the IRR in a Weaver or Hartley image rejection receiver.*

1.2 Voltage Controlled Oscillator (VCO) Design

The receiver architectures described in the previous sections rely on high frequency VCOs to generate various LO signals (both I and Q). A common VCO topology is the negative transconductance ($-G_M$) oscillator. A basic block diagram of a $-G_M$ oscillator is shown in Figure 1.6. There are two parts of the oscillator: a $-G_M$ circuit and a parallel LC resonant "tank" circuit. An ideal tank circuit has no loss; if energy is input into the system, it will oscillate forever at a resonant frequency given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{1.15}$$

By tuning the tank capacitance (e.g. using a varactor) the frequency of oscillation can be varied. Real tank circuit implementations have loss associated with the inductor and capacitor (varactor), represented by the parallel equivalent resistance, R_{eq}, in Figure 1.6. The $-G_M$ amplifier provides negative resistance to cancel this loss and

allow sustained oscillation of the tank circuit. The average value of the negative resistance of the $-G_M$ amplifier is given by [16]:

$$\overline{-R_D} = -1/G_M = V_1/I_1$$

where V_1 is the peak voltage of the fundamental at the input and I_1 is the peak current of the fundamental at the output of the active elements. The value of this negative resistance must be *less than* the equivalent parallel resistance of the tank circuit to sustain oscillation. The *startup safety factor* is often used as a thumb rule to ensure oscillation in the circuit:

$$\alpha = \frac{R_{eq}}{\left|\overline{-R_D}\right|}. \tag{1.16}$$

The safety factor, α, should be at least 2 for integrated oscillators [17]. VCO design, therefore, consists of designing the tank circuit to tune over the required frequency span and the $-G_M$ amplifier to supply the necessary negative resistance to sustain oscillation.

This section discusses three constraints that govern the design of the LC tank and $-G_M$ circuits. First, the aforementioned push toward higher levels of on-chip integration may require that noisy, synchronous digital circuits be fabricated on the same chip as noise-sensitive analog and RF circuits. Therefore, VCO designs that are much less sensitive to substrate or supply noise are required. Second, tight restrictions on adjacent channels within the crowded frequency spectrum have mandated wireless standards with very low phase noise requirements for the signal generators. Third, battery life is a major concern for mobile units, so the design must have low current consumption. The VCO topology used in this work is presented in the context of these three constraints.

1.2.1 Substrate and Supply Noise Immunity

In synchronous digital circuits, a clock governs the switching of transistor networks (gates). This leads to a large number of transistors across the entire chip switching at approximately the same time. Since CMOS transistors draw the most current when they are in the process of switching, the voltage rails become very noisy during

clock transitions as current draw from the CMOS circuits spikes. This poses no real problem to traditional digital circuits that have a high degree of noise immunity. However, analog circuits, which depend on the stability of voltage supply rails to maintain constant bias points, suffer from the introduction of supply noise from on-chip digital circuits. To alleviate this problem, analog circuits may share the same ground but typically have a separate, low-noise supply rail [18].

Another problem for analog circuits is presented by electromagnetic interference coupled into the substrate by signal traces as well as other transistors. The rapid and continuous switching of on-chip logic gates exacerbates the substrate noise problem. Substrate noise degrades RF signal quality when it is coupled into the analog portion of the circuit.

Differential designs are widely employed in the analog part of a system to cancel out noise. Within localized regions of the IC, substrate and supply noise are approximately the same on both the positive and negative outputs of differential circuits. Therefore, noise is suppressed in the differential output signal. This cancellation is called *common-mode rejection* and is a major advantage of differential topologies.

Differential VCOs are more complex than their single-ended counterparts, since they require twice the number of transistors to produce positive and negative outputs. The increased number of devices also increases power consumption and noise. Nevertheless, since on-chip mixers (e.g. Gilbert Cells) are typically differential, a differential output is required of the signal generator. Despite the added complexity and higher power consumption, differential VCOs are typically employed in RFICs to take advantage of common-mode noise rejection, and to avoid the need for single-ended-to-differential circuits to interface with the other components of the RF system.

1.2.2 Phase Noise

The output of an ideal oscillator can be described by the following equation:

$$v(t) = A\cos(\omega_0 t + \phi) \tag{1.17}$$

where A is the amplitude of oscillation, ω_0 is the frequency of oscillation, and ϕ is the phase offset. However, the active and passive devices used to implement a real

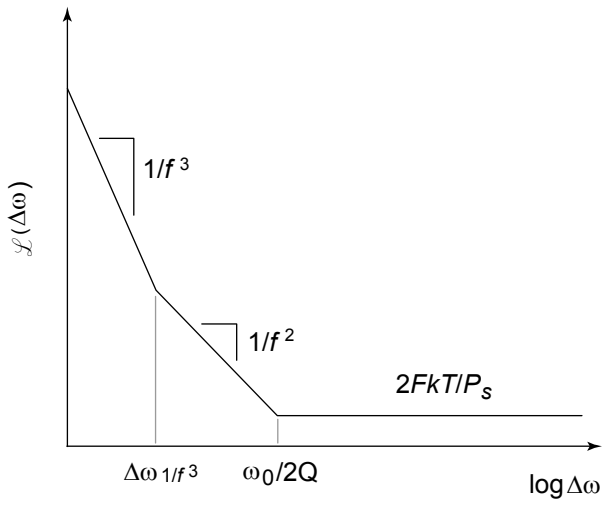

Figure 1.7: Oscillator phase-noise spectrum.

oscillator introduce random noise into both the amplitude and phase of the output. The introduction of noise changes equation 1.17 to:

$$v(t) = A(t)\cos(\omega_0 t + \phi(t)) \tag{1.18}$$

Frequency is the time derivative of the total phase, so the output spectrum of the oscillator will have sidebands because of random variations in the phase. This is known as *phase noise*. The amplitude noise can also manifest itself as phase noise due to the non-linear, amplitude-limiting nature of an oscillator. Thus, both sources of noise serve to widen the phase-noise spectrum of the oscillator.

Figure 1.7 shows an oscillator phase-noise spectrum as predicted by Leeson [19]. Three distinct regions of the spectrum exist: the $1/f^3$ sloped region; the $1/f^2$ sloped region; and the noise floor region. The boundary separating the noise floor from the $1/f^2$ region occurs at approximately $\omega_0/2Q$. The tank circuit filters, or shapes, the integrated noise spectrum below this frequency. At this frequency, however, the $1/f^2$ sloped region intersects the phase noise floor of the circuit, which is constant versus frequency. The boundary at $\Delta\omega_{1/f^3}$ is related to the $1/f$ corner frequency of the active device(s) of the oscillator, which occurs where the $1/f$ noise intersects the high frequency shot or channel noise of the device.

Phase noise is measured as a power spectral density in units of decibels below the car-

rier per Hertz (dBc/Hz) reported at some offset frequency from the carrier frequency. For example, the IEEE 802.11a standard requires signal generators to have a phase noise less than -107 dBc/Hz at a 1 MHz offset from the carrier [20].

The origin of phase noise has been described by Leeson using assumptions of a linear, time-invariant system. Leeson's well-known equation for phase noise is [19]:

$$\mathcal{L}(\Delta\omega) = 10\log\left\{\frac{2FkT}{P_s}\cdot\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\omega_{1/f^3}}{\Delta\omega}\right)\right\} \tag{1.19}$$

where F is the device excess noise factor, k is Boltzmann's constant, T is the temperature, P_s is the average power dissipated in the resonator, and ω_{1/f^3} is related to the $1/f$ noise corner frequency. F and ω_{1/f^3} are not typically known in advance, so they are usually fitted to measured data. Therefore, this model typically does not predict measured phase noise results very well.

Since oscillators are fundamentally non-linear circuits, the assumption of linearity must be examined carefully. The amplitude is limited and controlled in the oscillator by a combination of the non-linear devices and supply voltage. However, the noise in equation 1.18 is relatively small compared to the output signal swing. These small perturbations in the signal swing can be assumed to be linear with respect to the noise-to-phase transfer function, even though the large signal output amplitude control is non-linear [21]. Therefore, the principle of superposition is a valid assumption for the relationship between noise and phase.

The assumption of time-invariance in standard phase noise models must also be examined. It has been shown that amplitude noise is converted to phase noise differently if it is injected at a time when the output is near zero as opposed to a time when the output is at a maximum [22]. Figure 1.8(a) shows how the injection of an amplitude perturbation, ΔV_n, to the output of a lossless LC tank at the maximum has a smaller effect on the zero-crossing phase than the same perturbation when the waveform is near zero [Figure 1.8(b)]. Therefore, time-invariance is a poor assumption for the noise-to-phase transfer function.

To account for the time-invariance of the noise-to-phase conversion, an impulse sensitivity function (ISF) can be obtained for the output waveform of the oscillator. The ISF, typically obtained via simulation, weights the effect amplitude noise has on the

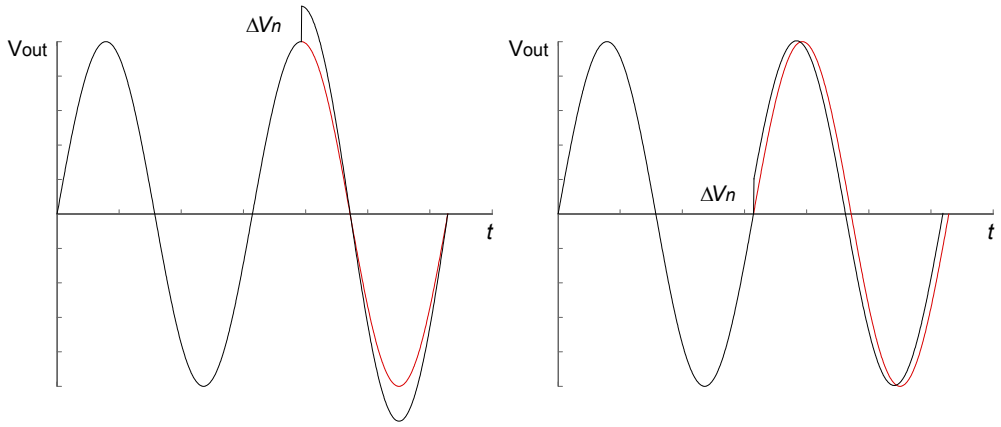

Figure 1.8: Time variance of phase noise is shown by injecting ΔV_n to the output of a lossless LC tank oscillator at different times in the cycle (after [22]).

phase depending on the time at which the noise impulse occurs. Since it has a period related to the oscillator frequency, it can be expressed as a Fourier series [22]:

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau) \tag{1.20}$$

where the Fourier coefficients, c_n, are real. Equation 1.20 can be used to find the unitless impulse response of the noise-to-phase transfer function [22]:

$$h(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau). \tag{1.21}$$

where q_{max} is the maximum charge displacement across the tank capacitor of the oscillator and is necessary in this equation to make the transfer function independent of the output amplitude.

The time varying phase from equation 1.18 is found by convolving the noise-to-phase transfer function from equation 1.21 with the equivalent noise current source [22]:

$$\phi(t) = \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^{t} i_{noise}(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i_{noise}(\tau) \cos(n\omega_0 t) d\tau \right] \tag{1.22}$$

A Fourier series can be used to represent the equivalent noise current:

$$i_{noise}(t) = I_0 + \sum_{m=1}^{\infty} I_m \cos[(m\omega_0 + \Delta\omega)t] \tag{1.23}$$

where $\Delta\omega$ is an offset frequency added to allow calculation of phase noise at offsets from the carrier in the final results. The Fourier coefficients, I_0 through I_m, are related to the noise current spectral density in a 1 Hz bandwidth, $\overline{i_n^2}/\Delta f$.

If equation 1.23 is then substituted into equation 1.22, the only term from the infinite sum that contributes to the excess phase is the case where $n = m$. In a sense, this result corresponds to frequency conversion that occurs in a heterodyne receiver [21]. Essentially, the c_n coefficients of the noise-to-phase transfer function act as an LO signal to down-convert noise at the nth harmonic to two sidebands at $\pm\Delta\omega$ from the oscillation frequency. This down-converted noise has a constant power spectral density versus offset frequency. However, the down-converted noise has a $1/f^2$ slope in the phase-noise spectrum because of the bandpass frequency characteristic of the tank circuit, which ideally attenuates the noise power contribution from each harmonic at 20 dB per decade increase of $\Delta\omega$.

Furthermore, $1/f$ noise from the active devices is up-converted by the c_0 coefficient from equation 1.22. The $1/f^3$ region of Figure 1.7 is created by up-converted $1/f$ noise at offsets from the carrier below the $\Delta\omega_{1/f^3}$ corner frequency combined with the $1/f^2$ sloped noise from down-converted noise around the harmonics.

Using the representation for $\phi(t)$ in equation 1.22, the phase noise power spectral density in the $1/f^3$ region of Figure 1.7 can be more accurately predicted by [21]:

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}c_0^2}{8q_{max}^2\Delta\omega^2}\frac{\omega_{1/f^3}}{\Delta\omega}\right) \tag{1.24}$$

Phase noise in the $1/f^2$ region is predicted by [21]:

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma_{rms}^2}{2q_{max}^2\Delta\omega^2}\right) \tag{1.25}$$

where Γ_{rms} is the rms value of the ISF given in equation 1.20.

The implications of equations 1.24 and 1.25 for oscillator design are significant. First, the tank circuit R_{eq} is responsible for a significant part of the noise current spectral density, $\overline{i_n^2}/\Delta f$. Since R_{eq} is typically limited by low-Q inductors in integrated VCOs, increasing the Q of the tank inductor is essential to the design of a low-noise oscillator. This has traditionally been a problem for Si ICs, because standard Si processes use a low-resistivity substrate. Aspects of inductor design for higher Q will be discussed in detail in Chapter 2. Second, the presence of q_{max} in the denominator of both equations 1.24 and 1.25 implies that the signal amplitude of the oscillator should be maximized to obtain lower phase noise. This stems from the assumption that voltage amplitude noise is assumed to be small compared to the output. Large oscillation amplitudes minimize the percent change noise has on the output waveform. Third, equation 1.24 shows that choosing devices with a low $1/f$ corner frequency can reduce the close-in phase noise of the $1/f^3$ region of Figure 1.7. Finally, the ISF can be optimized to improve phase-noise performance by using differential and complementary VCO designs [23],[24]. Ideally, the transistors should supply short pulses of current to restore energy to the tank circuit at the time when the ISF is the smallest. This will be explored in greater detail in Chapter 3.

1.2.3 Power Consumption

The two obvious ways to reduce VCO power consumption are: (1) reduce the supply voltage, and (2) reduce the current consumption. This section discusses aspects of both low-voltage and low-current design for VCOs.

Supply voltage is one of the foremost IC design considerations. Batteries are available with discrete voltages, so the lowest supply voltage for the given technology which permits suitable circuit performance is typically selected for the design. The supply rail must have a high enough voltage such that all the transistors in the design can operate with stable bias conditions. For bipolar designs, each transistor needs a sufficient base-emitter voltage (V_{BE}) to turn the device on and a sufficient collector-emitter voltage (V_{CE}) to keep the device out of saturation. This limits the number of transistors that can be "stacked" between the rail and ground. This limitation is referred to as "headroom." The current source transistors typically suffer most from limited headroom, since they are usually the closest to ground in a transistor

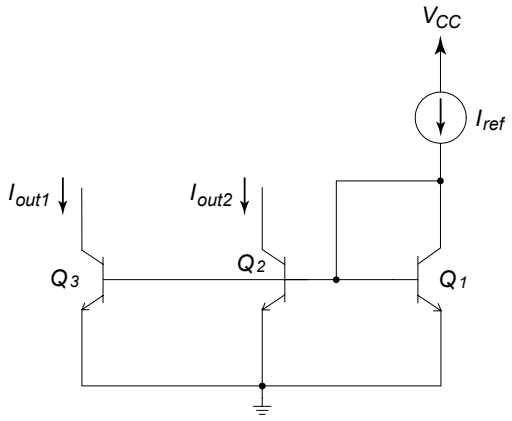

Figure 1.9: Schematic of a current mirror with two outputs.

stack. They are not required to provide gain (or negative transconductance) so designers will pull as much V_{CE} as possible from these devices to maximize available V_{CE} for other devices. However, if the collector voltage drops too much for the bias transistors, the base-collector junction will become forward biased, pushing the devices into saturation. If the transistors operate in the saturation regime, the current they provide can vary drastically for very small changes in collector voltage. This can have severe consequences on circuit performance.

Power consumption is reduced further by designing for minimal current. Several design techniques can be used to minimize current in the bias transistors of an oscillator. The number of current references can be reduced by daisy chaining multiple output devices to one reference (Figure 1.9). This minimizes the number of current paths from power to ground. In addition, the ratio of the device sizes in the current mirror should be scaled to minimize the amount of current not directly used to DC bias the $-G_M$ circuit.

Another major factor in lowering current consumption is the design of output buffers for the oscillator. The oscillator should have a large output signal swing to minimize phase noise and provide sufficient switching drive to subsequent mixers. However, this large signal output may compress traditional buffers. Buffers that can handle large signal input drives usually consume much more current than the oscillator itself, which substantially increases overall power consumption.

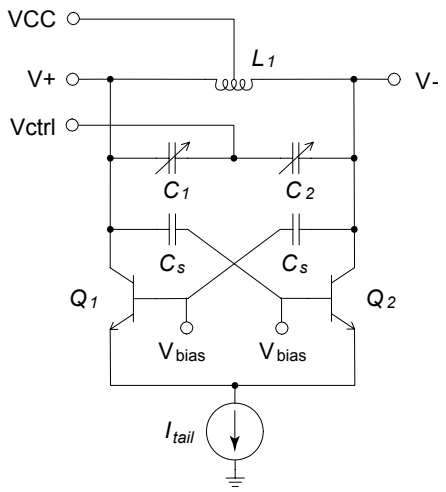

Figure 1.10: Schematic of the cross-coupled, differential pair oscillator.

1.2.4 Cross-coupled, $-G_M$ Oscillator

A common topology for RFIC voltage controlled oscillators is the cross-coupled, differential LC oscillator (Figure 1.10). As mentioned previously, in addition to superior common mode noise immunity over single-ended topologies, the differential output can be used to drive the LO port of the widely used double-balanced Gilbert cell mixer. This VCO topology will be the basis for the work in this thesis.

Bipolar transistors (Q_1 and Q_2) offer three advantages over field-effect transistors (FETs) in oscillators. First, the typically lower $1/f$ noise and corner frequency of bipolar devices results in superior phase noise in the $1/f^3$ region compared to equivalent FET devices. The origin of $1/f$ noise is generally attributed to carrier surface trapping due to defects in the semiconductor material [25],[26]. FET structures typically have higher $1/f$ noise, since trapping occurs more readily during lateral carrier transport along rough surface interfaces in the channel [27]. In contrast, the probability of carrier trapping in integrated bipolar devices is reduced because transport occurs vertically through the surface interfaces [28]. Second, shot and thermal noise of bipolar transistors are lower than the channel noise of FETs. This reduces the broadband noise at harmonics of the output frequency which are frequency translated to phase noise in the $1/f^2$ region. Third, bipolar transistors have a higher transconductance per milliampere (g_m/mA) than FETs, although submicron FETs

are closing the gap [29]. Higher g_m/mA allows the VCO of Figure 1.10 to consume less power than a FET based design with the same oscillation amplitude and tank circuit parallel equivalent resistance.

If Q_1 and Q_2 are directly coupled, saturation will result in a low oscillation amplitude. For example, when the collector voltage of Q_1 reaches its maximum, if the voltage difference between the V^+ node and the V^- node exceeds the forward-bias voltage of the collector-base junction of Q_2, then Q_2 will saturate. This problem is avoided by AC cross-coupling the differential pair with capacitors (C_S), thereby providing an independent bias for the bases (Figure 1.10). The additional cross-coupling capacitors lower the oscillation frequency, so the tank varactors must be resized to compensate. For AC-coupled differential pair oscillators, only I_{tail}, the supply voltage, and the tank circuit Q are variables in the nonlinear control of the oscillation amplitude.

1.3 Silicon-Germanium (SiGe) Technology

Two simultaneous trends in the present semiconductor market suggest that SiGe BiCMOS may be the technology of choice for low-cost, high-performance RFICs. The first is the ongoing drive towards greater integration. In this technology, high performance SiGe transistors are directly available with submicron metal-oxide silicon field-effect transistors (MOSFETs), allowing for RF and digital circuits to be designed and fabricated on the same chip. Thus, SiGe processes are often employed to integrate high performance RF circuits with state-of-the-art high speed digital signal processing and control.

The second trend is the continued improvement in SiGe device performance, given, primarily, by two figures-of-merit. First, the small-signal, unity-current-gain frequency (f_T) is an indicator for the maximum frequency at which the transistor can be used as an amplifier and is given by:

$$f_T = \frac{1}{2\pi}\left[\frac{1}{g_m}\left(C_{eb} + C_{cb}\right) + \tau_b + \tau_e + \tau_{bc}\right]^{-1} \tag{1.26}$$

where C_{eb} (or C_π) is the emitter-base junction parasitic capacitance, C_{cb} (or C_μ) is the collector-base parasitic capacitance, τ_b is the base transit time, τ_e is the emitter

delay time, and τ_{bc} is the base-collector junction depletion layer transit time. A second figure-of-merit, the maximum oscillation frequency (f_{MAX}), is given by:

$$f_{MAX} = \sqrt{\left(\frac{f_T}{8\pi r_B C_{cb}}\right)} \tag{1.27}$$

where r_B is the parasitic base resistance. Often, f_{MAX} is a more useful indicator of the device RF performance, since it includes the parasitic r_B. State-of-the-art SiGe HBTs have f_T and f_{MAX} values on the order of those for equivalent III-V technologies, such as gallium arsenide (GaAs) and indium phosphide (InP) (i.e., greater than 250 GHz) [30],[31],[32]. This indicates that SiGe HBT devices can be used for applications approaching the millimeter wave region (30-50 GHz). It should be stressed that f_T and f_{MAX} serve as figures-of-merit; a combination of many factors determines the actual device performance in practical applications.

The drive for companies to economize, coupled with lower cost and comparable performance to III-V devices, has recently enabled SiGe to make inroads in semiconductor markets previously dominated by III-V technologies. SiGe ICs have become competitive with and even out-perform III-V circuits in some ways. For, example, SiGe was recently used to produce the lowest reported minimum stage delay of an emitter coupled logic (ECL) ring oscillator, surpassing the previous standard set using InP [33].

The two major disadvantages of SiGe technologies have been lossy passives and low break-down voltages. First, loss in passives comes as a result of the standard low-resistivity Si substrate which allows submicron CMOS to coexist with SiGe transistors. The semi-insulating substrate of III-V technologies has traditionally allowed much higher Q factors for monolithic inductors. However, thicker metals and higher-resistivity substrates in some SiGe processes have recently permitted Q factors on the order of those achievable in III-V processes. Second, low break-down voltages of SiGe transistors limits their use as power amplifiers (PAs), an essential component of any transmitter. However, research and development is currently underway to improve the high-power capabilities of SiGe devices [34].

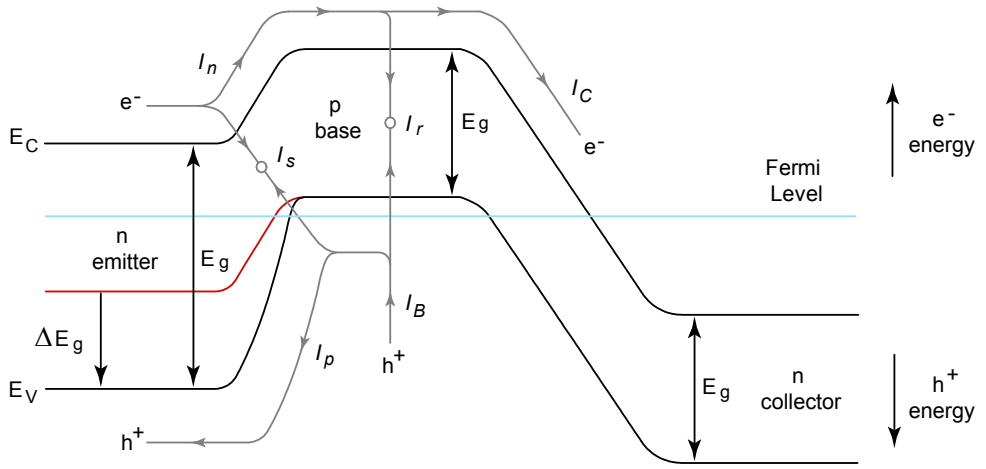

Figure 1.11: Bandgap diagram of a traditional wide-bandgap emitter *npn* HBT (after [36]).

1.3.1 Wide-Bandgap Emitter HBTs

The definition of a *heterojunction* is a *p*-*n* junction where the bandgaps of the *n*-material and *p*-material differ. Si, located in column IV of the periodic table, is an elemental semiconductor. The traditional Si bipolar junction transistor (BJT) is a *homojunction* device, meaning that the base, collector, and emitter all have the same bandgap (approximately 1.12 eV). The idea of a heterojunction bipolar transistor (HBT) dates back to one of the original patents by William Shockley for the solid-state transistor in 1948. Although the advantages of an HBT (to be discussed below) were long recognized, the technology capable of implementing them was not available until the 1970s [35],[36]. In addition, until the early 1990s, the only available HBTs used III-V semiconductor materials.

In a *npn* homojunction device, the forces acting on electrons and holes are equal and opposite. Traditional *npn* heterostructure devices allow the forces on electrons and holes to be engineered by adjusting the bandgap of the emitter with relation to the base (ΔE_g). Figure 1.11 shows how the potential barrier for hole back-injection into the emitter from the base in an *npn* device is larger than the potential barrier for electron injection into the base. Reduced hole back-injection current (I_p) decreases the base current (I_B) of the wide-bandgap emitter transistor with relation to I_C due to emitter electron-injection current (I_n). In addition, the emitter recombination current (I_s) is reduced by decreasing I_p, which in turn increases I_n and I_C. Thus,

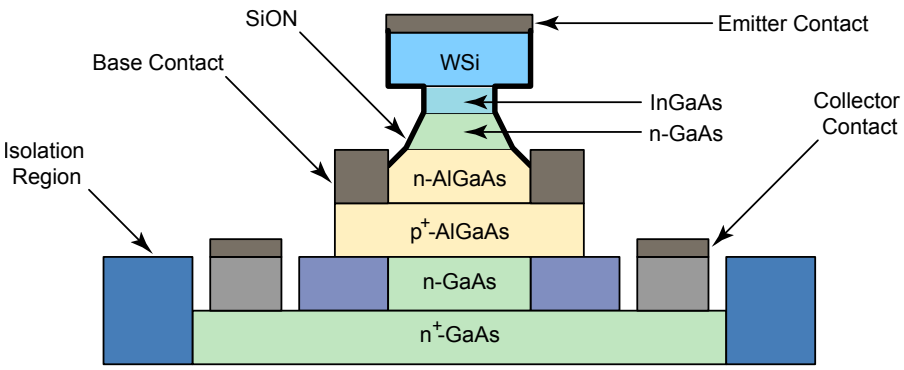

Figure 1.12: Cross section of an AlGaAs/GaAs HBT (after [37]).

the device current gain (β) increases according to the following ratio:

$$\beta = \frac{I_C}{I_B}. \tag{1.28}$$

The device cross section of a typical self-aligned AlGaAs/GaAs wide-bandgap emitter HBT is shown in Figure 1.12. In this structure, the vertical dimensions of the emitter, base, and collector are all determined by epitaxial growth and the horizontal dimensions are fully and mutually self-aligned.

A complex relationship exists between C_{eb}, r_B, the emitter and base doping levels, and the area of the base-emitter p-n junction. This relationship allows the advantages of the wide-bandgap emitter to extend beyond simply increasing β. In general, the injection efficiency and device β suffer for low emitter doping levels in bipolar devices [36]. However, in a HBT, higher β permits much lower emitter doping levels without compromising injection efficiency. Consequently, C_{eb} is decreased by lowering the emitter doping concentration, allowing the device to be re-optimized for higher f_T at a given β (equation 1.26). The emitter area can also be expanded to increase I_C, since C_{eb} is significantly lowered by reducing the doping concentration [35].

Lowering the doping level in the emitter allows further device optimization, in light of the junction capacitance properties of an asymmetrically doped p-n junction. For example, if the emitter has a much lower doping concentration than the base, then C_{eb} will depend only on the lower doping of the emitter [36]. This principle allows doping concentrations in of the p^+-AlGaAs base to be set much higher, lowering r_B without

affecting C_{eb}. Low r_B is desirable because it improves the gain, noise performance, and f_{MAX} of the device (equation 1.27).

Widening the bandgap of the emitter, therefore, can be utilized to dramatically improve the high frequency performance of the device. Superior performance has lead to wide-spread use of these devices in some applications. For example, the III-V HBT has become the dominant device for PAs in mobile wireless applications due to high breakdown voltages and power densities (W/mm^2), in addition to the aforementioned improvements in f_T and f_{MAX} values.

1.3.2 SiGe HBTs

Si and Ge are both column IV semiconductors. However, Ge has a substantially lower bandgap of approximately 0.66 eV [38]. Thus, the introduction of Ge into Si to create a $Si_{1-x}Ge_x$ alloy results in a material with a *smaller* bandgap than pure Si. The bandgap of the alloy is dependent on the fractional concentration of Ge (given by $x \leq 1$), with the bandgap being smallest when the concentration of Ge is the greatest. Therefore, SiGe HBTs have *bases* that are engineered to have narrower bandgaps than the emitters.

For example, an *npn* SiGe HBT is created with an n+-poly-Si/p-SiGe emitter-base junction and a p-SiGe/n-Si base-collector junction with an implanted n-Si collector region (Figure 1.13) [39]. SiGe HBTs can certainly be fabricated using a mesa-type structure as shown in Figure 1.12. However, these structures are not compatible with thermal processing cycles needed in CMOS technologies, so such HBTs cannot be integrated in BiCMOS processes. On the other hand, the structure in Figure 1.12 is compatible with the CMOS processing steps; thus, this SiGe HBT structure can be fabricated alongside submicron FETs [40].

The concentration of Ge in the base is typically graded (Figure 1.14), with the highest concentration at the base-collector junction to lower the bandgap closer to the collector. Figure 1.14 shows that the bandgap is essentially unchanged at the emitter, so the emitter-base junction is approximately the same as that of a conventional homojunction Si BJT. Unlike wide-bandgap emitter HBTs, I_B of an *npn* SiGe HBT is not changed by the heterostructure, since hole back-injection from the base is determined

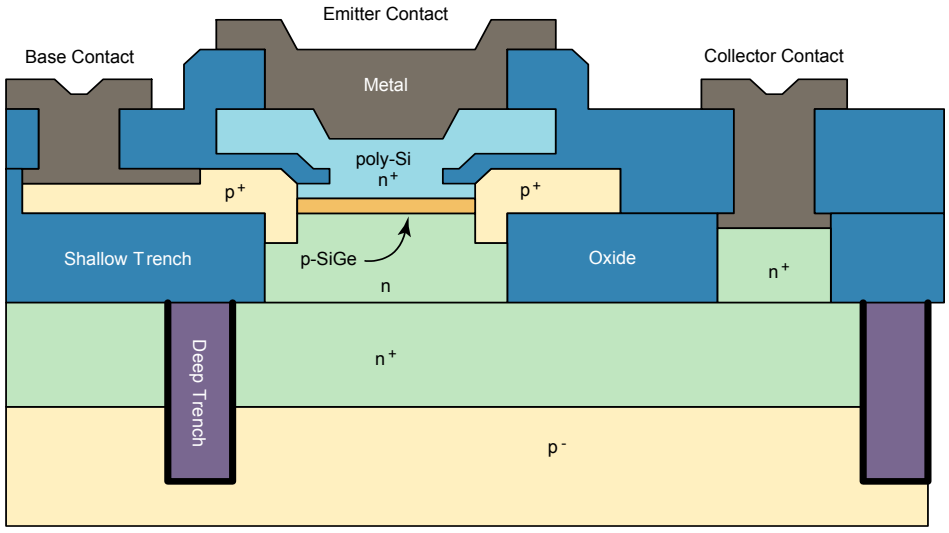

Figure 1.13: Cross section of an implanted-collector SiGe HBT (after [41]).

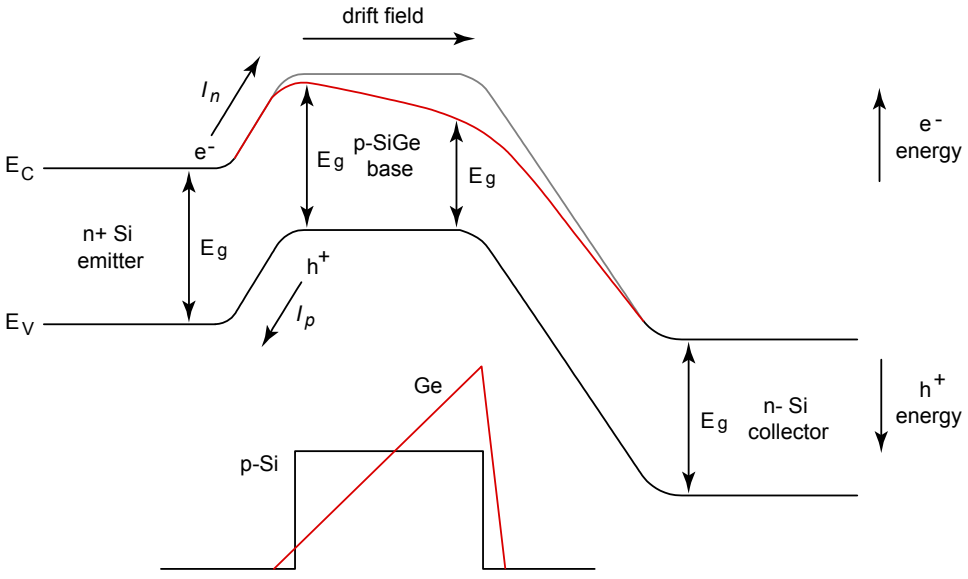

Figure 1.14: Bandgap diagram of Si and SiGe HBT. The red line represents the changed conduction band caused by adding Ge to the base. Below the bandgap diagram is the corresponding Ge concentration profile (after [42]).

by the unchanged relative valence bands of the emitter and base. Therefore, the improvement in β of SiGe HBTs does not come from reduced I_B. On the other hand, grading the bandgap of the base lowers the potential barrier for electron injection into the base from the emitter, thereby improving the collector efficiency for a given emitter-base forward bias. The increase in collector current for a fixed bias translates to an increase in the current gain (β) and Early voltage (V_A) of the device [42].

The Ge gradient also creates a drift field which accelerates electrons in the base traveling from the emitter to the collector, lowering τ_b. Furthermore, τ_e is reduced, since it is inversely proportional to β [42]. Lowering both τ_e and τ_b increases f_T according to equation 1.26. Furthermore, as in III-V HBTs, r_B is lowered by increasing the doping level of the base relative to the emitter to improve the gain and noise performance of the device.

An important measure of noise performance is the minimum noise figure (NF_{min}), which is determined by broadband noise sources in the transistor. Broadband noise in bipolar transistors is primarily attributed to base and collector shot noise and thermal noise. These noise sources are reduced by a combination of decreasing r_B and increasing f_T and β [39]. Since all three of these quantities are optimized by the HBT structure, current SiGe devices can have NF_{min} as low as 0.4 dB [43]. State-of-the-art SiGe HBTs have NF_{min} approximately 1 to 2 dB lower than the best III-V HBTs, III-V FETs, and CMOS devices [44]. In addition to low broadband noise, it has been shown that the low frequency $1/f$ noise of SiGe HBTs is comparable to the best Si BJT devices and exceeds that of MOSFETs, GaAs HBTs, GaAs high electron-mobility transistors (HEMTs), and GaAs metal semiconductor field-effect transistors (MESFETs) by several orders of magnitude [39],[45],[46]. For example, at 10 Hz, the mean square $1/f$ noise of SiGe HBTs has been shown to be 10^{-18} A^2/Hz compared to 10^{-16} A^2/Hz for Si n-FET devices [39]. Superior $1/f$ noise and NF_{min} make SiGe HBTs excellent devices for low-phase noise RF oscillator designs.

1.4 Objective and Overview of Thesis

The objective of this research is to demonstrate the concept of a quadrature LO source with analog tunable I/Q balance which could potentially be used to improve

the performance of I/Q channel receivers and the image rejection of the Weaver architecture. Analog tunability of quadrature output phase has not been previously explored in the literature. Three areas determine the feasibility of tunable output phase, namely: phase flatness, phase tuning range, and overall power consumption. This thesis analyzes a 5-6 GHz SiGe VCO with tunable I/Q balance in terms of these three areas.

As part of this work, two VCOs were designed. The first VCO uses an electrically symmetric inductor, which has a Q factor approximately 50% higher than the traditional dual inductor structure used in the tank circuit of the second VCO. Aside from the tank inductors, the two VCOs are identical. Therefore, this thesis also investigates the improvement in phase noise performance obtained by using the higher Q electrically symmetric tank inductor. The VCO with the symmetric inductor was combined with a tunable polyphase filter to create a quadrature LO source with tunable I/Q balance. Circuits were designed and fabricated using the Motorola 0.4 μm CDR1 SiGe BiCMOS process. This process has four aluminum metal layers and a thick uppermost (bump) copper layer for high performance RF passives.

This chapter has introduced background information regarding the motivation, application, and design of a quadrature VCO with tunable phase outputs. A brief overview of the advantages of SiGe BiCMOS, the technology used for this work, has also been presented. Chapter 2 discusses the design and characterization of monolithic inductors, specifically for application in differential VCOs. Design procedures for optimizing Q factor, as well as simulation and characterization of differential inductors are the focus of the material presented. Design and simulation of the $-G_M$ LC VCO using SiGe HBTs is presented in Chapter 3. Chapter 4 covers the design and simulation of a tunable polyphase network. Measured results for the fabricated VCO and polyphase are presented in Chapter 5. Chapter 5 also includes information on fabrication and packaging to facilitate accurate RF test and measurement. This thesis concludes with an evaluation of circuit performance, as well as a discussion on future work and possible improvements to the VCO design with tunable quadrature phase outputs.

Chapter 2

Monolithic Inductor Design

Monolithic inductors perform critical roles in integrated RF systems as components in matching, biasing, and resonant filtering networks. While the drive towards higher levels of integration has brought about significant performance improvements in recent years, on-chip inductors (particularly in Si technologies) still lag behind the more expensive, off-chip, surface mount alternatives. On-chip inductors in Si technologies can have Quality (Q) factors that range from 3 to 20 compared to several 100s for off-chip inductors. Acceptable performance can be obtained from on-chip inductors if the major loss and parasitic capacitance contributions are considered.

This chapter reviews the basic loss mechanisms and the equations used to characterize Q factor and effective inductance value for planar spiral inductors on lossy Si substrates. Design considerations for differentially excited monolithic inductors which can help improve Q factor are also discussed. Finally, full-wave electromagnetic simulations used to characterize and optimize the inductors for this work are presented.

2.1 Quality (Q) Factor

The Q factor is defined by the following ratio:

$$Q = 2\pi f \frac{average\ energy\ stored}{energy\ dissipated\ per\ second}. \tag{2.1}$$

For an inductor of a given value, the Q factor is a measure of the total loss associated with the coil. The Q of monolithic inductors is limited by losses in the spiral conductor, electric coupling to the substrate, and magnetic coupling to the substrate.

2.1.1 Conductor Loss

Loss in a conductor can be generally described by the following equation:

$$R = \frac{\rho_{film}}{t}\frac{L}{W}, \tag{2.2}$$

where ρ_{film} is the thin film resistivity of the metal, t is the metal thickness, and L and W are the trace length and width, respectively. Often, the quantity ρ_{film}/t is expressed as *sheet resistance*, with units of $\Omega/\square$. In some cases, thin film resistivity can also be represented by its inverse, conductivity ($\sigma = 1/\rho_{film}$). Loss can, therefore, be minimized by using metals with very low resistivity, increasing the cross sectional area of the trace ($t \cdot W$), or reducing the overall trace length.

Two metals are primarily used for interconnects in Si IC processes. Aluminum has been used in Si processes for decades because it is inexpensive, does not corrode easily, and is process-compatible with CMOS. However, compared to other metals, aluminum has a somewhat higher bulk resistivity of 2.62 $\mu\Omega \cdot cm$. Copper, which has a lower bulk resistivity around 1.72 $\mu\Omega \cdot cm$, is currently in widespread use for many digital CMOS and analog/RF BiCMOS processes. It should be noted that the thin film resistivity may be significantly higher than the bulk resistivity due to scattering of electrons by the defects, grain boundaries, impurities, and rough surfaces of the film. In addition, the thin film resistivity increases dramatically as metal thickness decreases, partly because surface roughness approaches the same order of magnitude as the film thickness itself [47]. Traditional CMOS aluminum layers are typically very thin (under 1 μm). Small cross-sectional areas of these metal layers yield relatively high conductor loss in spiral inductors. Thin traces on standard interconnect layers can be *strapped* together by multiple vias, to increase the effective thickness (t_{eff}) of the conductor beyond the standard thickness of the metal layer [Figure 2.1(a)] [48]. However, the advent of thick metal deposition processes has largely obviated this strapping approach. Thick aluminum or copper

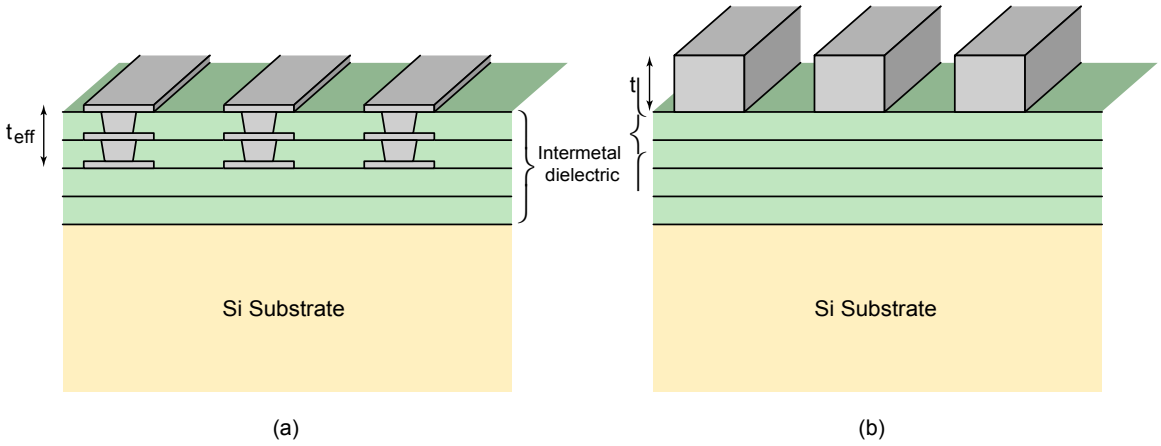

Figure 2.1: Cross section of two approaches for analog/RF interconnects: (a) mutltiple metal layers strapped together by vias and (b) thick bump layer metal.

technologies are available for analog designs to reduce conductor loss in passives [49],[50]. Some processes employ copper for all interconnect layers, while others have a thick copper layer as the uppermost metal and aluminum (or other metal) for underlying interconnects. A thick uppermost copper layer is sometimes referred to as a "bump" layer, since it actually protrudes from the otherwise flat final passivation layer of the completed IC. These bump layers can be much thicker than standard interconnect metal layers because the restrictions due to planarization by chemical mechanical polishing (CMP) are loosened [Figure 2.1(b)]. Increased thickness leads to much lower series resistance in the spiral and higher Q for two reasons: (1) the cross sectional area of the conductor is increased and (2) the thin film resistivity is improved (reduced). The process used for this work (Motorola CDR1) has a $\sim$10 μm thick copper bump layer for high Q inductors [50].

The second way to minimize conductor loss is to modify the planar spiral geometry. Ideally, very wide traces should be used to maximize the amount of conductor for a given thickness of the metal layer. A structure with the maximum amount of conductor in the shortest possible length is desired. The circular spiral is ideal in this regard; however, the octagonal spiral is more commonly used because of its layout simplicity. Octagonal spiral layouts only require 45° bends of the conductor, rather than the smooth, continuous curve of a circle. Despite their increased area for a given inductance over circular and octagonal spirals, square spirals have been typically

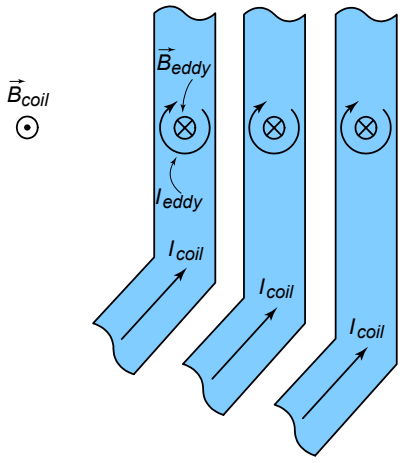

Figure 2.2: Eddy currents (I_{eddy}) generated by the magnetic field of the coil (B_{coil}). The $\otimes$ and $\odot$ symbols represent currents flowing into and out of the page, respectively. (after [52]).

used because they only require 90° bends of the conductor traces. This structure is mandated by mask generation systems that require Manhattan style layouts (i.e., only 90° bends used, like the streets of Manhattan, NY) [51]. The process used for this work does allow circular structures that fall on a 50 nm grid. However, the process also has automated layout generation and modeling (parameterized cells) of a range of octagonal spiral inductors. For these reasons, the octagonal spiral inductor was used for this work.

Conductor loss also arises when the magnetic field of the inductor penetrates the turns of the spiral to induce swirling eddy currents according to Faraday's law (Figure 2.2) [52]. These eddy currents have a small component in the same direction as current flow in the inductor. However, the majority of the eddy current flow is in directions other than that of the inductor coil currents. As a result, the coil current is crowded to the side of the conductor with the same directional component, minimizing the effective trace width that the coil current occupies and increasing the loss. As frequency increases, this current crowding effect becomes more pronounced.

The inner-most turns of the inductor suffer the most from swirling currents, since the magnetic field is greatest at the center of the coil. It has been shown, using finite-element simulations of a nine turn inductor, that resistance at 2 GHz in the outer coil increased 18% from its low frequency value. In contrast, the resistance

of the innermost coil increased 480% over the same range [52]. Consequently, the innermost coils are typically eliminated to leave a large "hollow" area at the center of the inductor. Since the inner turns contribute minimally to the total inductance, hollow coils have much higher Q factors without a significant increase in the outer diameter of the coil.

2.1.2 Shunt Parasitic Capacitance

As shown in Figure 2.1, the metal spiral of the inductor is isolated from the semiconductor substrate (typically at ground potential) by one or more dielectric layers used to separate interconnect layers (inter-metal dielectrics). This creates a parasitic shunt capacitor that can be roughly approximated by the following equation:

$$C = \frac{A\epsilon}{d} \tag{2.3}$$

where A is the total area of the metal traces, ϵ is the dielectric permittivity, and d is the thickness of the dielectric.

The parallel parasitic capacitance plays a major role in determining the self-resonant frequency (f_{sr}) of the inductor (i.e., the frequency at which the inductor has a zero net reactance). Beyond f_{sr}, the planar spiral becomes capacitive. The parasitic capacitance limits the maximum size of monolithic inductors to a few nanohenries (nH), since large inductance values require more area (A). Furthermore, the parasitic capacitance contributes to the loss of the inductor by AC coupling RF energy from the coils into the substrate (as will be discussed in the next sub-section). The Q factor versus frequency curve slopes downward to zero at the f_{sr}, so controlling the parasitic capacitance is also essential to designing the inductor for high Q.

Reducing the conductor width, and thereby reducing the inductor area, minimizes this parasitic capacitor. However, as discussed previously, conductor loss is increased when narrow traces are used. The designer must balance both the parasitic shunt capacitance and conductor loss when selecting a conductor width. This tradeoff underscores the advantage of circular and octagonal spirals over square spirals. For example, for a given operating frequency above f_{sr}, the conductor width can be increased, thereby decreasing f_{sr}, as long as the peak Q factor is not affected. There-

fore, the reduction in overall trace area of circular and octagonal spirals allows wider traces to be used in order to reduce conductor loss.

The parasitic capacitance can also be reduced by increasing the dielectric thickness, d, in equation 2.3 and printing the inductor on the uppermost possible metal layer. If several metal layers are strapped together by multiple vias, careful consideration should be given to the thickness of the remaining dielectric between the lowest metal layer of the inductor and the substrate. For, example, binding all the metal layers together for an ultra-thick conductor may reduce conductor loss, but it will also substantially increase the shunt parasitic capacitance coupling to the substrate. In this case there is a trade-off between conductor loss and parasitic capacitance for the inductor design. This trade-off does not occur for inductors using thick bump metal layers a fixed distance above the substrate.

There is also parasitic capacitance between the vertical faces of the interwinding traces or between overlapping traces at cross-under points of the inductor. This capacitance also contributes to decreasing the f_{sr}, though the effects are typically small compared to the parasitic capacitance with the substrate in Si technologies. The interwinding capacitance can be minimized by increasing the spacing between the coils of inductor; however, this reduces the effective inductance of the coil, requiring a larger coil for a given inductance value. Typically, the smallest spacing available for the process is chosen to minimize the overall area of the inductor, regardless of the effect on the interwinding capacitance.

2.1.3 Substrate Loss

Substrate loss is the dominant factor resulting in low inductor Q factors in a standard Si processes. This section discusses two types of loss in the substrate: electric (capacitive) loss and magnetic loss.

The primary source of electric loss in the substrate is RF energy coupled through the shunt capacitance of the inductor into the substrate. Si CMOS substrates are typically doped to have a lower bulk resistivity in order to reduce the possibility of latch-up in digital CMOS circuits. The low-resistivity substrate also improves noise isolation between digital and analog circuits, since hot-electron induced noise

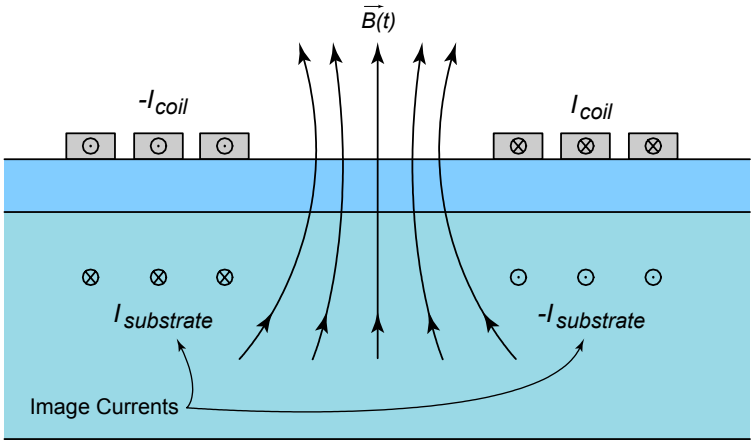

Figure 2.3: Image currents in the substrate induced by the time varying magnetic field of the coil. The $\otimes$ and $\odot$ symbols represent currents flowing into and out of the page, respectively (after [52]).

currents in the substrate are diminished [52]. Unfortunately, the low-resistivity substrate also appears as a resistor between the parasitic capacitance and ground. In the past, GaAs has been used almost exclusively for RF/microwave ICs since it has a semi-insulating (high-resistivity) substrate. For GaAs, the parasitic resistor representing substrate loss is very large, so the parasitic shunt capacitance appears to be terminated by an open circuit to RF signals. Since Si is typically a low-resistivity substrate, the substrate resistor connecting the parasitic capacitance to ground is relatively small, allowing more of the signal to be coupled into the substrate. High resistivity substrates and wells, or micromachining techniques can be used to reduce substrate loss in Si technologies; however, these techniques are non-standard for IC process flows.

The other type of loss in the substrate is magnetic loss. The magnetic field from the inductor encircles the current carrying wires, as described by Ampere's law. Lenz's representation of Faraday's law states that an opposing image current is induced in any conductor within the magnetic field to resist a change in the field. As the time-varying, RF current flows in the inductor, image currents are induced in the Si substrate in the opposite direction (Figure 2.3). The Si substrate acts much like a transformer to couple energy from the inductor into the substrate. More than 60% of the loss in the inductor can be attributed to this parasitic transformer [53]. As with the parasitic shunt capacitance, the effect of the parasitic transformer can be

minimized by decreasing the diameter of the coil [52]. For smaller coils, the magnetic flux lines into the substrate are less dense, thereby inducing less image current. Conceptually, moving the spiral farther from the substrate would tend to reduce the effect of the parasitic transformer, since the magnetic field decreases in strength at greater distances from the coil. However, the relatively small changes in distance between standard interconnect metal layers, is not large enough to make a significant difference in the strength of the magnetic field penetrating the substrate [52]. In contrast, high-resistivity substrates prevent image currents from being induced, which greatly benefits the Q factor.

As mentioned previously, the magnetic flux lines are most dense in the center of the inductor spiral. Therefore, it is critical to keep the area under the center of the coil free from any interconnect traces or active devices. Anything located inside the spiral will tend to couple energy away from the inductor and increase the loss beyond that due to the image currents in the substrate. The return path of the magnetic flux lines are located on the outside of the spiral. Though these flux lines are much less dense than those inside the coil, it is still a good idea to locate interconnects and active devices a fair distance away from the coil. For the technology used for this work, it is recommended that a distance of 100 μm be used between the outside diameter of the coil and the nearest metal trace or active device.

2.2 Inductor Model and Characterization

Inductor characterization depends on the specific application. Three different uses for inductors in RF circuits are shown in Figure 2.4. The first [2.4(a)] is a shunt connection typically used for degeneration, impedance matching, or loading. This configuration is characterized as single-ended, or unbalanced, since one port of the inductor is connected to AC ground (this is sometimes accomplished by way of a shorting capacitor at DC bias nodes). The second [2.4(b)] is a series connection, which is useful for impedance matching in amplifiers or mixers. The third [2.4(c)] is a differential excitation, commonly used in differential oscillators, differential amplifiers, and mixers. For example, the VCO in Figure 1.10 requires this inductor topology for the resonant tank circuit. This configuration requires precise symmetry between the two sides of the inductor to set up a virtual ground at the plane of symmetry.

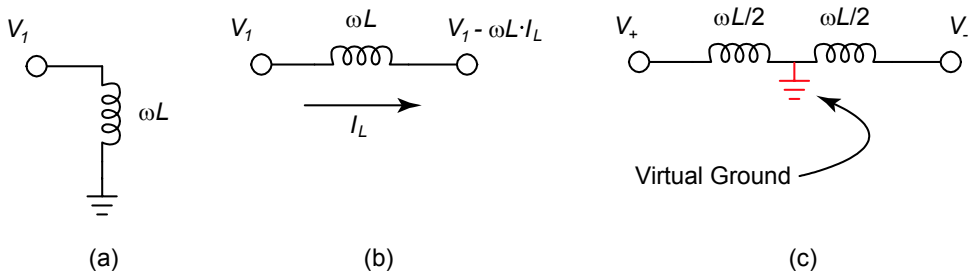

Figure 2.4: Three possible uses for inductors in RF circuits (a) shunt (b) series, and (c) differential.

A lumped element model is useful for accurate simulation of monolithic inductors. Figure 2.5 shows a detailed model for an inductor on Si substrates that takes into account the effects described in Section 2.1 [53]. The inductance of the coil is modeled by the series inductor (L) between ports 1 and 2. The parasitic capacitive coupling into the substrate and the associated losses are represented by the shunt capacitors (C_{OX} and C_{sub}) and resistors (R_{sub}). Trace conductor loss is characterized by a resistor (R_s) in series with the inductor. The loss due to image currents magnetically induced into the substrate is represented by the transformer coupled to a resistor ($R_{sub(m)}$). The cross under and interwinding capacitance is represented by C_p.

The model of Figure 2.5 can be represented by a π-equivalent Y-parameter network (Figure 2.6). The impedance of differentially excited inductors, such as the structure in Figure 2.4(c), is measured between ports 1 and 2 of Figure 2.6, rather than with a simple one-port measurement of the input impedance with port 2 grounded. For this reason, inductance and Q factor are calculated differently for differential inductors than for traditional single-ended configurations [51]. Appendix A gives a detailed development of how this network is simplified for both the single-ended and differential cases in order to determine the Q factor and inductance.

As shown in Appendix A, neither port of the differential inductor is grounded, so the impedance seen between the two terminals of the inductor is defined as:

$$Z_{in} = R + jX = \frac{Y_{11} + Y_{22} + 2Y_{12}}{Y_{11}Y_{22} - Y_{12}^2}. \tag{2.4}$$

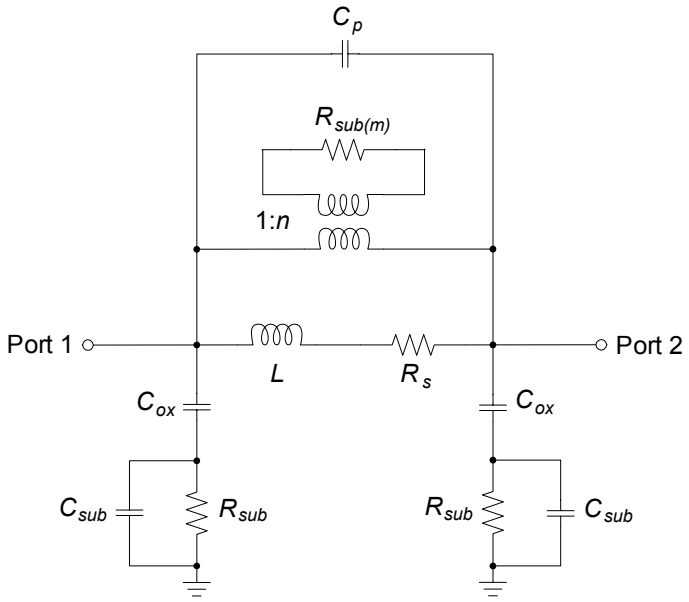

Figure 2.5: A lumped element model for monolithic inductors on Si substrates (after [53]).

Using equation 2.4, the differential inductance is then defined as:

$$L = \frac{X}{2\pi f} = \left(\frac{1}{2\pi f}\right)\left[\mathrm{Im}\left(\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right)\right], \tag{2.5}$$

and the differential Q factor is defined as:

$$Q = \frac{X}{R} = \frac{\left[\mathrm{Im}\left(\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right)\right]}{\left[\mathrm{Re}\left(\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right)\right]}. \tag{2.6}$$

Measuring an inductor differentially typically results in Q factors slightly higher than the single-ended case (3-5%) [51].

2.3 Electrically Symmetric Differential Inductors

One method to construct a monolithic differential inductor is to use two inductors, each of half the total inductance value, placed side by side and connected at the common node by an underpass on a lower metal layer [Figure 2.7(a)]. In this thesis,

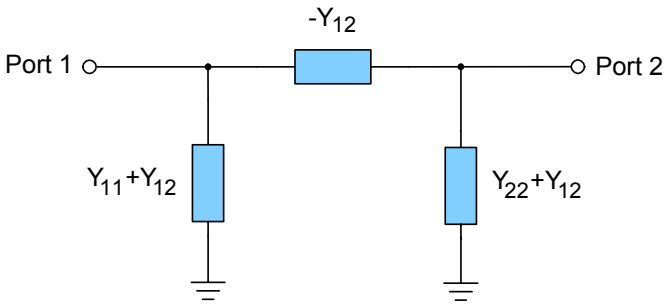

Figure 2.6: A π-eqivalent Y-parameter network of the lumped element model for monolithic inductors on Si substrates (see Figure 2.5) [51].

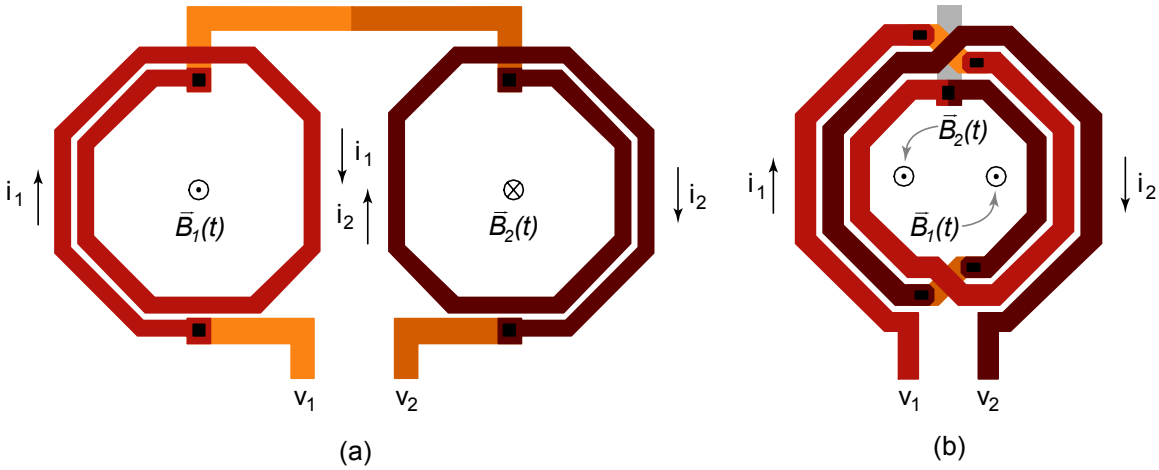

Figure 2.7: Magnetic fields created by the current running through the differentially excited inductor for (a) dual inductor (b) symmetric inductor. The $\otimes$ and $\odot$ symbols represent magnetic fields flowing into and out of the page, respectively.

this layout is referred to as a "dual inductor." While the coils are geometrically symmetric, they are not electrically symmetric. The two inductors individually operate in a single-ended fashion, much like those represented in Figure 2.4(a) and (b), until they meet at the common node. The main disadvantage of the dual inductor layout for differential excitation is that the currents (i_1 and i_2) in the two coils of the dual inductor flow in the opposite directions where the two coils are adjacent. As a result, the induced magnetic fields [$\overrightarrow{B}_1(t)$ and $\overrightarrow{B}_2(t)$] are oriented in opposite directions. These opposing magnetic fields lower the mutual inductance of the dual inductor, thereby reducing the net reactance without affecting the resistance. Since Q factor is the ratio of the reactance and resistance, the Q is effectively lowered by

these opposing magnetic fields. This effect can be minimized by increasing the gap separating the two coils. However, this results in an increase in die size for a small increase in Q — rarely a viable solution.

The magnetic fields of the dual inductor structure could be oriented in the same direction by reflecting one of the coils in Figure 2.7(a) about its vertical axis. In this case currents would flow in the same direction where the coils are adjacent, enhancing mutual coupling. However, this configuration is not desirable because the inductor is no longer geometrically symmetric. This asymmetry obscures the location of the virtual ground point. Furthermore, this solution offers no significant reduction in die area over the dual inductor in Figure 2.7(a).

Figure 2.7(b) shows an inductor with both geometric and electrical symmetry [54]. In this thesis, this layout is referred to as a "symmetric inductor." Current in adjacent coils flow in the same direction so that the induced magnetic fields are oriented in the same direction. Furthermore, the two halves of the inductor are arranged so that currents from the positive and negative inputs flow in neighboring coils, a truly odd-mode structure. Interwinding the differential inductor provides a better match between the two halves of the coil, resulting in equivalent substrate parasitics. Finally, Figure 2.7 emphasizes the dramatic decrease in the chip area ($\gtrsim 50\%$) required for symmetric inductors of the same value.

Past research has shown the improvement in Q factor for symmetric inductors [55],[56]. Theoretically, two times the Q factor is possible with the symmetric inductor, although Qs from 30% to 50% higher than a dual inductor equivalent are realized in practice [54]. The symmetric inductor requires twice the number of vias and underpasses to intertwine the two coils and make the common node available to the exterior of the coil (e.g., for biasing). Loss associated with these vias mitigates some of the Q improvement. Strapping two layers of metal together with multiple vias can minimize loss in the underpasses that connect opposite halves of the coil. However, strapping the two layers together is not necessary for the common node underpass that will be at AC ground, since this trace carries minimal RF signal. Regardless, the benefit of orienting the two magnetic fields in the same direction far outweighs these additional sources of loss, as shown by the net improvement in Q factor.

2.4 Inductor Simulations

2.4.1 Selection of Inductor Dimensions

Sonnet em [57], a full wave electromagnetic solver, was used to simulate the tank circuit inductors for the VCO designs in this thesis (Figure 1.10). Three meshing schemes for the inductor metal are available from Sonnet. The first is the traditional square mesh. This mesh often requires many cells to accurately represent objects with angles other than 0° or 90°. A second option is the diagonal mesh, which allows arbitrary angles to be more accurately represented using approximately the same number of cells as the square mesh. Both of these traditional meshes can require large amounts of memory to solve Maxwell's equations for complex structures such as the differential inductor. The third method, "conformal" meshing, is currently in beta testing [58]. This mesh was designed specifically to reduce the number of cells required to accurately simulate meandering lines such as the coils of spiral inductors. The accompanying reduction in memory requirement dramatically reduces computation time, making iterative design more feasible. Unfortunately, the beta version of conformal mesh available when the VCOs were being designed was found to be less accurate than the diagonal and rectangular mesh for Q calculations. Thus, long computation times were required (e.g. days versus hours), and, consequently, exhaustive iterative design was not done to select the final inductor dimensions.

The technology design kit for this work contains automated layout parameterized cells (p-cells) for octagonal symmetric inductors with three input parameters: trace width; coil spacing; and inner diameter. The dimensions selected for the inductor represent design decisions based on the trade-offs discussed in Section 2.1. The minimum coil spacing for the inductor (7 μm) was selected. Small coil spacings increase the mutual inductance of the coils and decrease the outer diameter, though at the expense of increased inter-winding capacitance (Section 2.3). Thus, Q factor is increased for small coil spacings by reducing the effective area of the inductor for a given inductor value, though f_{sr} may be lowered as a result. A trace width of 15 μm was selected over the maximum trace width for the copper bump layer for the process (20 μm). The decision was made based on the assumption that, at the maximum trace width, the substrate losses for the larger inductor area would begin to outweigh the benefits

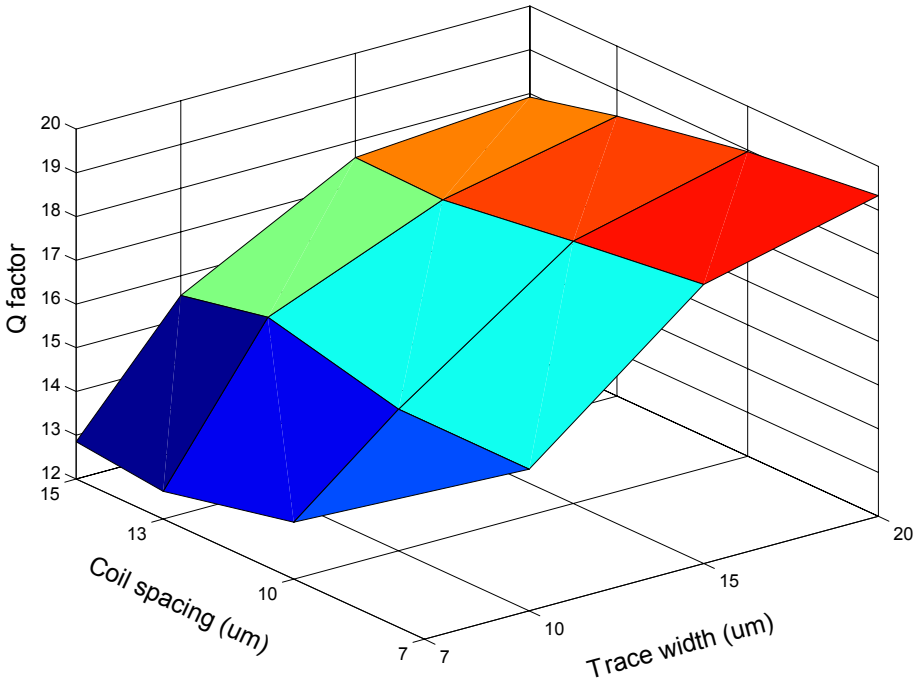

Figure 2.8: Plot of Q factor for various trace widths and coil spacings from electromagnetic simulations of a symmetric inductor with a value of approximately 2.3 nH.

of reducing conductor losses with wide traces.

Several months after the final designs were submitted for fabrication, Sonnet released an updated and improved algorithm for the conformal mesh. The disagreement with the standard diagonal and rectangular meshes was reduced, enabling the use of conformal mesh for accurate, iterative inductor simulation. With the updated version of Sonnet em, several specific cases with various the trace widths, coil spacings and inner diameters were simulated to evaluate the design decisions made for the final inductor. The trace width was varied from 20 μm down to 7 μm. Coil spacing was swept from 7 μm up to 15 μm. The inner diameter parameter was adjusted to maintain a total effective inductance value of $\sim$2.3 nH for different trace widths and coil spacings.

Figure 2.8 shows the change in Q that results from increasing trace width and coil spacing. The highest Q is obtained for the maximum trace width (20 μm) and the smallest coil spacing (7 μm). Contrary to previous assumptions, the Q at the largest trace width does *not* suffer from the increased substrate effects. The Q at a trace

width of 15 μm is approximately 5% lower than that of an inductor with 20 μm trace width. Though the selected inductor dimensions provide a Q very near the maximum available, the inductor design could clearly have benefitted from simulations of an exhaustive sweep of inductor dimensions. It should be noted, however, that at a coil spacing of 7 μm, the 15 μm trace width reduces the area of the inductor by 20% over the 20 μm trace width, which did help with fitting all the required circuits in the available reticle, since several copies of the inductor were required.

2.4.2 Inductor Design Simulations

Several process parameters play a critical role in accurate inductor simulation. Specific information on the substrate and inter-metal dielectric layers cannot be presented in this thesis as it is Motorola proprietary information. However, their general effect on the inductor simulations should be discussed. Thickness, relative dielectric permittivity (ϵ_r), and loss tangent ($\tan\delta$) are essential parameters for the layers separating the metal traces and the the substrate. These dielectric parameters determine the parasitic shunt capacitance described in Section 2.1.2. The thickness and conductivity of the substrate is critical for accurate simulation of image currents and other substrate losses. The thin film conductivity of the metals for each layer is also necessary to account for conductor loss. Each of these parameters was obtained from the CDR1 design manual and included in Sonnet layer definition files.

Two inductor designs were simulated and compared using Sonnet. The first was a symmetric inductor to be used in the VCO tank circuit. An equivalent dual inductor was also simulated for comparison in an otherwise identical VCO circuit (Figure 1.10). Both of the inductors were laid out in Cadence Virtuoso [59] and exported to Sonnet.

Symmetric Inductor Simulations

Both conformal and diagonal meshing schemes were used to simulate the symmetric inductor. The S-parameters from the simulations were used in conjunction with equations 2.5 and 2.6 to calculate the resulting differential effective inductance and Q factor. Figure 2.9 compares the results for both types of meshing. Though the results are not identical, both meshing schemes yield approximately the same curves

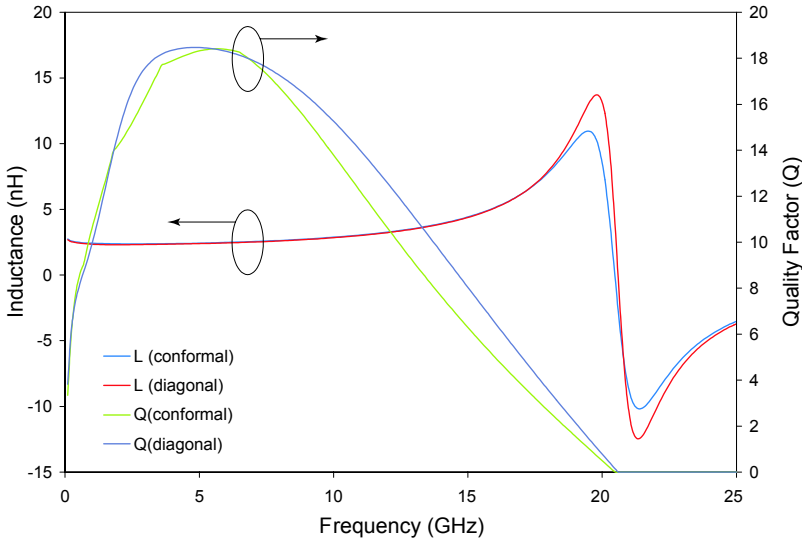

Figure 2.9: Inductance and Q factor results from Sonnet simulations for the symmetric inductor.

for Q factor and effective inductance. Thus, the major benefit of a conformal mesh simulation is that it requires only $1/10^{\text{th}}$ the simulation time to obtain nearly the same results as the traditional diagonal mesh simulations. This dramatic decrease in simulation time makes it practical to perform parameter sweeps to arrive at an optimal inductor geometry, as presented in Figure 2.8. Based on the conformal mesh simulations at 5.25 GHz, Sonnet predicts a Q of 18.4 and an effective inductance value of 2.4 nH.

Dual Inductor Simulations

An equivalent dual inductor was also simulated in Sonnet using both meshing schemes. Figure 2.10 shows the differential inductance and Q factor from both meshing schemes. The results from conformal and diagonal mesh simulations are nearly identical for the dual inductor. Based on the conformal mesh simulations at 5.25 GHz, Sonnet predicts a Q of 11.8 and an effective inductance value of 3.1 nH.

A difference in the relative number of conformal mesh cells used between the symmetric and dual inductor cases may explain the improved correlation of simulated data for the dual inductor. Each of the turns of the dual octagonal inductor was

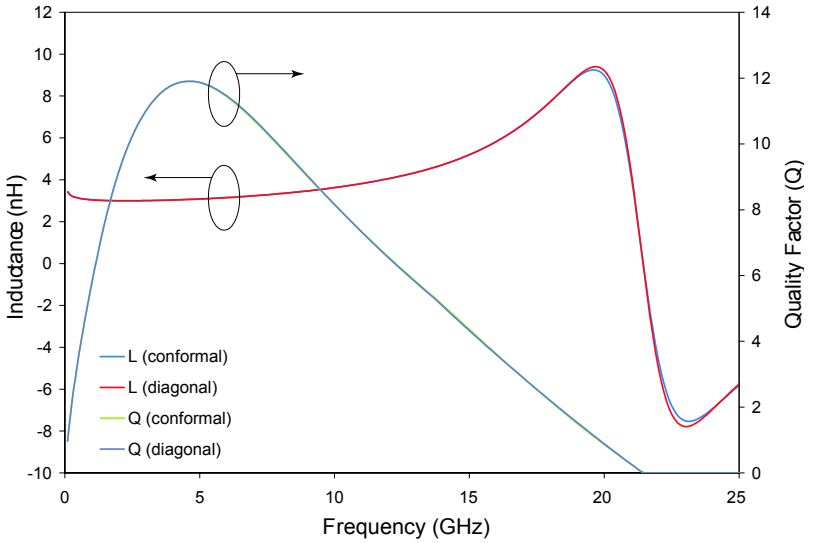

Figure 2.10: Inductance and Q factor results from Sonnet simulations of the dual inductor.

broken into eight metal subsections. Only the sections that were at 45° angles used conformal meshing, since the major time saving advantage of conformal mesh is with shapes that do not lie on a Manhattan grid. For the conformal mesh simulations, much of the inductor is still simulated using the diagonal mesh. In the symmetric inductor case, the coils are treated as one continuous piece of metal, so most of the inductor is simulated using the conformal mesh. Simulation time was decreased for the conformal mesh simulations of the dual inductor by ∼75%, though the ratio of conformal to diagonal mesh cells was less.

Q Factor Comparison

Figure 2.11 compares the simulated Q factors of the symmetric and dual inductors. At 5.25 GHz, the symmetric inductor has a Q of 18.4 and the dual inductor has a Q of 11.8. The symmetric inductor layout improves the simulated Q factor by 64% over the dual inductor case, which is comparable to other reported results [54]. Interestingly, the dual inductor has a higher f_{sr} than the symmetric inductor. This implies that the symmetric inductor has slightly higher parasitic capacitance than the dual inductor, most likely due to increased cross-under capacitance.

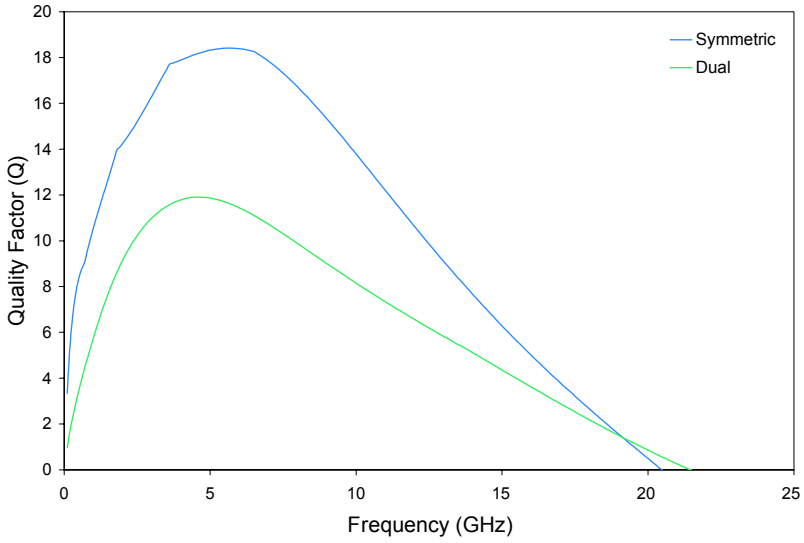

Figure 2.11: Simulated Q factor for the symmetric and dual inductors

2.5 Summary

This chapter has presented information on the loss mechanisms of monolithic inductors on Si substrates. The symmetric inductor, with an approximately 50% improvement in Q factor and more than 50% reduction in die area over the equivalent dual inductor, was discussed. Iterative simulations of various symmetric inductor dimensions were used to find optimal dimensions to maximize Q, given the area constraints of the final circuit. Results from full-wave, electromagnetic simulations showed that a symmetric inductor has an effective inductance of 2.4 nH and a Q of 18.4 at 5.25 GHz. Similar simulations of an equivalent dual inductor resulted in an effective inductance of 3.1 nH and a Q of 11.8 at 5.25 GHz. VCO designs based on both of these inductor structures are discussed in the next chapter.

Chapter 3

VCO Design

As discussed in Chapter 1, VCO design can be separated into two sections: the passive tank circuit and the active $-G_M$ circuit. This chapter first discusses several important trade-offs which influence design decisions for these circuits. The remaining sections of this chapter cover the simulated performance of the VCOs designed in this work, output buffer design, and the layout of the VCOs and output buffers.

3.1 Tank Circuit Design

Factors in the design of the tank circuit inductor to maximize Q factor were discussed in Chapter 2. This section focuses on the trade-offs between the relative size of the tank inductor and the varactors. A varactor is a tunable capacitor realized using either a p-n junction diode or a MOS gate capacitor. A brief discussion of the varactors used in this work is also included.

3.1.1 Inductor Value and Tuning Range

Large inductors are desired for their higher equivalent parallel resistance, R_{eq}, as shown by the following relationship [17]:

$$R_{eq} = Q2\pi f_0 L. \tag{3.1}$$

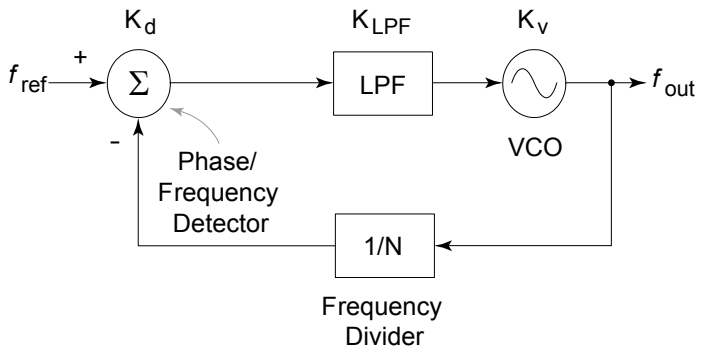

Figure 3.1: Block diagram of a phase locked loop.

As discussed in Chapter 1, the absolute value of the negative resistance, $|-1/G_M|$, of an oscillator must be *less than* the R_{eq} of the tank circuit in order to sustain oscillation. Therefore, a larger R_{eq} requires less negative resistance from the $-G_M$ circuit for oscillations to occur, thereby reducing the current consumption of the oscillator. Furthermore, the excess negative resistance (above that which is needed to overcome loss in the circuit) increases the output amplitude. Continually increasing negative resistance, however, does not mean continuously increasing output amplitude. The supply voltage and nonlinear amplitude control of the oscillator ultimately control the maximum amplitude. Nevertheless, when R_{eq} is decreased, the oscillator can have a higher output amplitude for a given negative resistance.

Meanwhile, large inductors also have lower f_{sr} and require a correspondingly smaller tank capacitance for oscillation at a given f_0 (see equation 1.15). Therefore, the size of the inductor is usually determined by the size of the tank capacitors and varactors which provide the precise amount of tuning for the frequency band of the design.

The tuning range and varactor size often determine the usability of the oscillator. For instance, a VCO is typically used as a component within a phase-locked loop (PLL) (Figure 3.1). A PLL takes an input reference frequency and generates a control voltage that forces the output of the VCO to track the reference phase or frequency. The reference is typically produced by a very frequency stable crystal oscillator at a much lower frequency. A frequency divider can be used to translate the output of the VCO to the same frequency range as the reference. Phase locking corrects the problem of frequency drift inherent in free running oscillators [17].

In PLL design, the VCO gain, K_v, is a useful quantity describing the tuning sensitivity and is given by the following equation:

$$K_v = \frac{\Delta f_0}{\Delta V_{ctrl}} \tag{3.2}$$

where ΔV_{ctrl} is the change in control voltage required to produce a corresponding change in output frequency, Δf_0. Depending on the application, PLLs are often required to tune across a wide bandwidth. A VCO for IEEE 802.11a is required to tune from 5.15 to 5.825 GHz. If the varactor tunes the VCO over this band for a 2 V change in bias, K_v is 338 MHz/V. Unfortunately, it is very difficult to design a PLL using a VCO with such a high K_v because very small changes in control voltage (possibly due to noise) can produce drastic changes in output frequency.

Typically, a VCO used in an application requiring a large tuning range over several bands will employ digitally switched capacitors for coarse band tuning and a varactor for fine tuning across a given band [43]. This technique lowers the effective K_v, allowing the VCO to operate stably within a PLL.

In this work, the VCO is intended to drive a tunable polyphase filter on-chip. For simplicity, the VCO tank circuit was designed with two series connected varactors (see Figure 1.10) that provide tuning across all three of the U-NII bands from 5.15 to 5.825 GHz, rather than employing the added complexity of switched fixed capacitors and varactors that tune across the three U-NII bands individually. Though this large K_v is not desirable for PLL applications, the proof-of-concept of tunable phase outputs is the primary purpose of this work.

3.1.2 Varactors

The varactors used in this work are *accumulation-mode* devices. These devices are similar to PMOS transistors except that the source and drain regions are $n+$ diffusions in an n-well and the gate is a $n+$ polysilicon gate (Figure 3.2). The two $n+$ regions are tied together to create one node of the varactor, while the gate serves as the other node. The highest capacitance is obtained when the device operates in the accumulation regime (i.e., a positive gate bias with respect to the bulk attracts excess electrons to the interface of the substrate and gate oxide), whereas the lowest

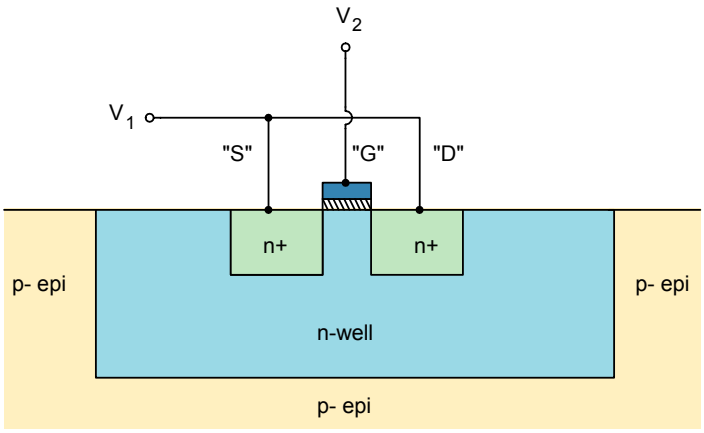

Figure 3.2: Cross section of an accumulation Mode varactor (after [17]).

capacitance is obtained when the device operates in the depletion regime (i.e., a negative gate bias with respect to the bulk pushes the electrons deeper into the substrate, depleting the channel).

MOS varactors typically have very steep "DC" C-V tuning characteristics [60]. However, if a MOS varactor is used in a differential VCO, the large signal output across the device modulates the capacitance in the time domain, "smoothing" the DC small signal tuning characteristic [61]. For this reason, the VCO tuning characteristic is typically more gradual than the DC C-V tuning characteristic of the varactors. The Motorola CDR1 varactor DC/small-signal tuning curve is shown in Figure 3.3. The capacitance tuning range is 115% for bulk-to-gate voltages (V_{bg}) from -0.8 to 1.7 V. Using equation 1.15, the expected frequency tuning range of the VCO is 49% if the varactor alone is considered. In practice, the tuning range will be lower due to parasitic and fixed capacitance in the VCO.

3.2 $-G_M$ Circuit Design

The primary goal for designing the $-G_M$ circuit is to cancel the R_{eq} of the tank circuit, while providing low noise and high oscillation amplitude with acceptable current consumption. Section 1.2.2 describes how up-converted $1/f$ noise manifests itself in the close-in phase-noise spectrum. Therefore, reducing $1/f$ noise is a con-

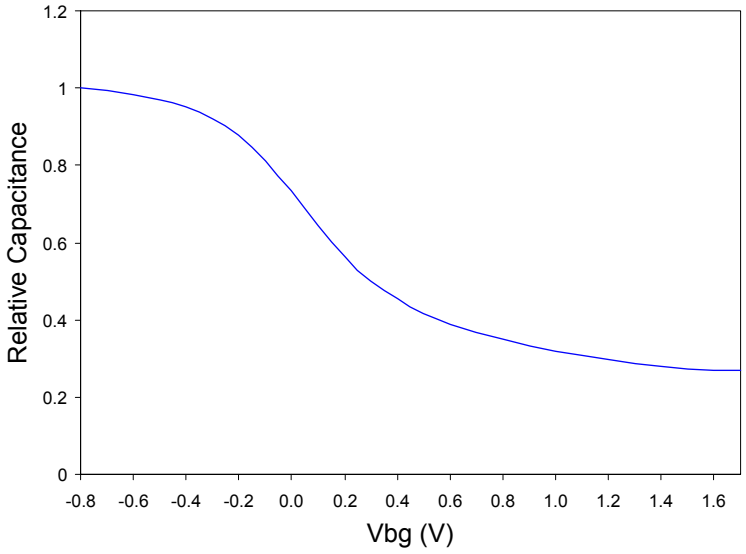

Figure 3.3: "DC"/small-signal tuning characteristic of the accumulation mode varactor used in the VCO of this work.

cern while designing the $-G_M$ circuit. In addition, the oscillation amplitude and negative resistance of the circuit are determined by the bias point of the transistors. Thus, trade-offs involving device size and transistor biasing play a critical role in well designed $-G_M$ circuits for RF oscillators.

3.2.1 Device Size Trade-Off

It has been shown that increasing emitter area of Si/SiGe bipolar transistors lowers the $1/f$ noise for the same base current [62],[63]. However, the current required to bias for peak f_T also increases with device size (Figure 3.4). Therefore the device should be large to minimize $1/f$ noise, but not so large that the power consumption suffers in order to bias for peak f_T. For this work, the emitter area ($L_e \times W_e$) was chosen to be relatively large at 0.4 μm $\times$ 10 μm.

Emitter area also affects the transconductance of the device. The I_C for an *npn* device at a particular V_{BE} is given by the equation [64]:

$$I_C = \frac{qAD_n n_{po}}{W_B} e^{V_{BE}/V_T}. \tag{3.3}$$

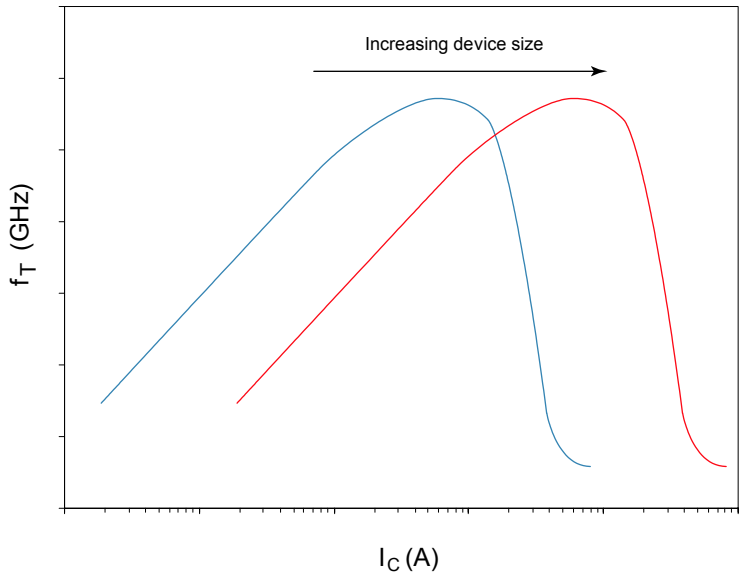

Figure 3.4: Generic plot of a HBT device f_T versus I_C showing the effect of increasing device size.

where q is the fundamental charge of an electron, A is the area of the emitter, D_n is the diffusion constant for electrons, n_{po} is the equilibrium concentration of electrons, W_B is the metallurgical width of the base, V_{BE} is the base-emitter bias voltage, and V_T is the thermal voltage (kT/q). By increasing A, the I_C for a given bias point is increased. This increase in I_C leads to higher transconductance, as given by the following equation:

$$g_m = \frac{I_C}{V_T} \tag{3.4}$$

Therefore, a larger emitter area reduces close-in phase noise by increasing the oscillation amplitude and by reducing the $1/f$ noise of the device.

3.2.2 Transistor Biasing

Bias Point

The $1/f$ noise is proportional to approximately I_B^2 [62],[63],[65]. So, low phase noise can be achieved by biasing the transistor at a low I_C, since I_B and I_C are related by the β factor. Power consumption also benefits from low bias points, extending

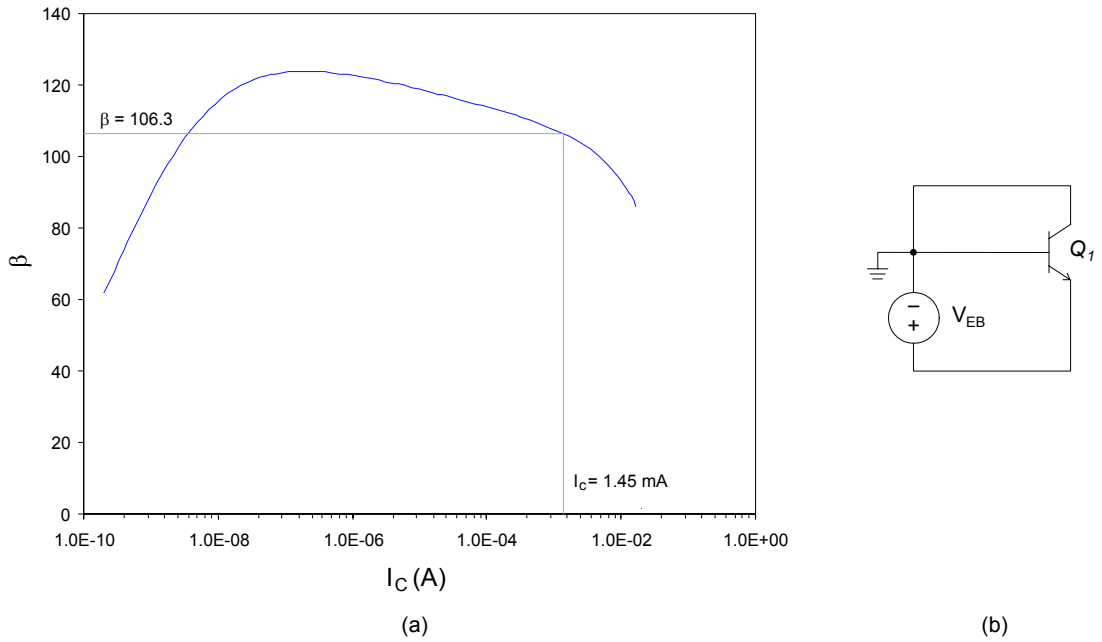

Figure 3.5: (a) Device β versus I_C for a Motorola CDR1 SiGe HBT with emitter dimensions of 0.4 μm $\times$ 10 μm. (b) Test circuit for measuring the Gummel and β curves of a bipolar device.

battery life for mobile units. Unfortunately, a low I_C produces low output oscillation amplitudes. Section 1.2.2 describes how a high output amplitude is desired for low phase noise since it is measured as a ratio of the noise to the carrier amplitude (dBc).

Figure 3.5(a) shows β as a function of I_C for the devices used in this work. This β curve is obtained by sweeping the emitter-base voltage of the circuit in Figure 3.5(b) and measuring the I_B and I_C Gummel curves. The device β peaks at just over 120 when I_C is on the order of several hundred nanoamps. Ideally, the device should be biased for the peak β to maximize the trade-off between high I_C (to increase the output amplitude) and low I_B (to decrease $1/f$ noise). However, the maximum β for the Motorola CDR1 HBT occurs for an I_C that is far too low to provide sufficient $-G_M$ to offset the loss in the tank circuit. Therefore I_C must be selected after the point where enough transconductance is provided, but before the sharp roll-off of the β curve. For this work, I_C was selected at 1.45 mA ($\beta = 106.3$), since this bias point provides a high oscillation amplitude without a tremendous sacrifice of the peak β of the device. This bias current occurs just before the β curve of Figure 3.5 begins its sharper descent.

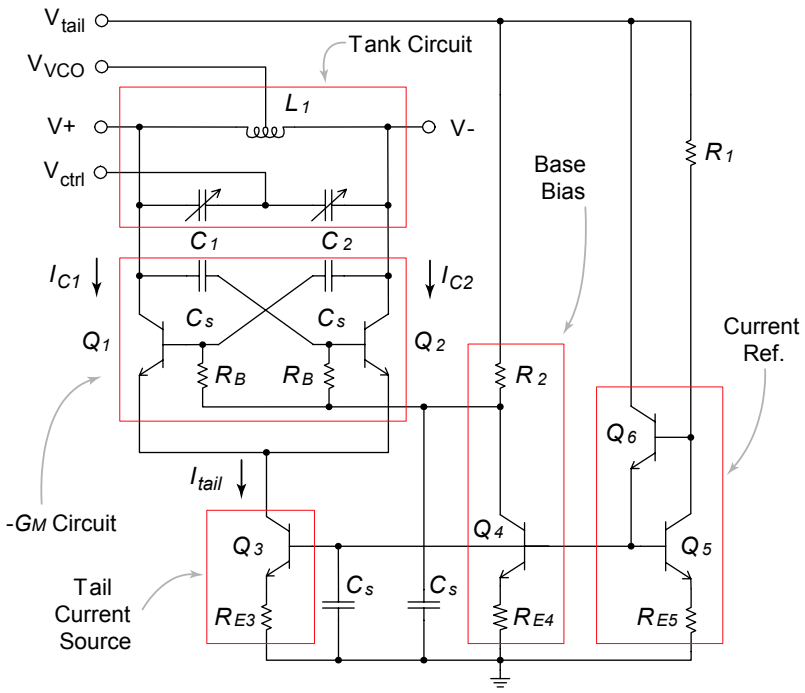

Figure 3.6: Schematic of the VCO and bias circuit.

Bias Circuit

Figure 3.6 shows the complete VCO and bias circuit used in this work. The bias network consists of a current mirror with two output devices to provide the base bias voltage and the tail current of the $-G_M$ circuit. The bias currents, I_{C1} and I_{C2}, are set in both transistors of the cross-coupled differential pair (Q_1 and Q_2) by the tail current provided by the output of the current mirror consisting of transistors Q_3 and Q_5. These transistors were designed to have a mirror ratio of approximately 16:1 to minimize the DC current not directly used by the $-G_M$ circuit (i.e., consumed by the reference circuit).

Q_6 improves the gain for the mirrored currents in Q_3 and Q_4 [64]. Figure 3.7(a) shows a simplified ideal current mirror which uses a diode-connected reference transistor (Q_{m1}). In this circuit, Q_{m1} and Q_{m2} have the same emitter areas, so the collector current of Q_{m2} exactly mirrors the collector current of Q_{m1}. The reference (I_{ref}) must supply base current to Q_{m1} and Q_{m2} in addition to the collector current of Q_{m1}, due to the finite β of the transistors. Thus, the current supplied by Q_{m2} is lower than

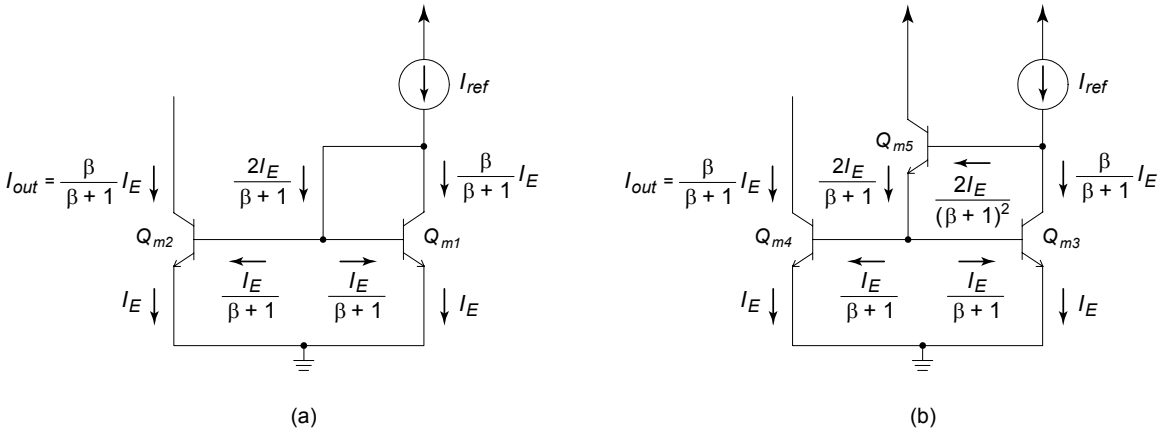

Figure 3.7: Schematic of (a) a simple bipolar current mirror taking into account the finite β of the transistors and (b) a bipolar current mirror with β compensation (after [64]).

the reference current by the amount of base current required for both transistors in the mirror. When more output transistors are added to the mirror, more and more base current is taken from I_{ref}. For the case when Q_{m1} and Q_{m2} are the same size, the current gain of the mirror is given by [64]:

$$\frac{I_{out}}{I_{ref}} = \frac{\beta}{\beta + 2} = \frac{1}{1 + 2/\beta} \tag{3.5}$$

The problem is the same when the aspect ratio of the two transistors is greater than one, except that the currents in Q_{m2} are multiplied by a scaling factor.

In the modified current mirror circuit of Figure 3.7(b), the current gain of Q_{m5} reduces the amount of reference current required to supply base current to the transistors. Q_{m5} is commonly called a "beta helper," since the current gain of the mirror is limited by the finite β of the transistors. By adding the beta helper, the current gain error in the denominator of equation 3.5 is reduced from $2/\beta$ to $2/\beta^2$ [64].

Examining the VCO bias circuit in Figure 3.6, the base bias voltage (V_{BB}) of transistors Q_1 and Q_2 is set using a second current mirror consisting of transistors Q_4 and Q_5. The current drawn by Q_4 and the the size of R_2 provide the voltage drop from the supply voltage for the desired V_{BB}. R_B is a large resistor (2 kΩ) used to limit RF leakage from the oscillator into the bias circuit.

The emitter degeneration of Q_3, Q_4, and Q_5 (R_{E3}, R_{E4}, and R_{E5}) aids in increasing the output impedance of the current mirrors. For example, an approximation for the output resistance of the degenerated tail current source (Q_3) is found using the small signal output resistance of the device (r_o) [66]:

$$r_o' \simeq r_o \left(1 + \frac{I_{C3} R_{E3}}{V_T}\right). \tag{3.6}$$

The output resistance of the device is approximated by $r_o \simeq V_A / I_C$, where V_A is the Early voltage. For example, using the Early voltage of the Motorola CDR1 HBT (95 V), a tail current of 2.8 mA and an emitter degeneration resistance of 30 Ω, the small signal output resistance of the tail source is increased by a factor of 4.2 from 34 kΩ to 140 kΩ.

The increase in output impedance of the mirror provides stability to the output current. The collector current of a finite output resistance *npn* bipolar transistor increases gradually for larger values of V_{CE}. By increasing the output resistance of the mirror, the collector current remains more constant for increasing V_{CE}. Ideally, the tail current is supplied to the $-G_M$ circuit at a virtual ground point in the VCO circuit. However, device mismatch can offset the virtual ground, permitting RF voltage swing from the $-G_M$ circuit to affect the collector voltage of Q_3. Adding emitter degeneration reduces the influence of a changing V_{CE} on the DC current supplied by Q_3.

The main benefit of stabilizing the current supplied by Q_3 is the potential for lower phase noise. Any fluctuations in the DC tail current will change the peak output voltage of the VCO in a similar manner to the voltage noise injected to the output swing of a lossless LC tank circuit shown in Figure 1.8. As discussed in Section 1.2.2, amplitude noise is translated to phase noise through the nonlinear amplitude control of the VCO.

3.3 VCO Simulations

The VCO was simulated using SpectreRF, a component of the Cadence Design System [59]. Typically, the initial simulations of an oscillator are used to verify the

proper frequency and amplitude of the output waveform in the time domain. These simulations are used to fine tune performance based on the trade-offs described in Sections 3.1 and 3.2. In addition to the time-domain analysis, non-linear simulations are required to predict oscillator phase noise.

Two VCOs were simulated in this work. Both VCOs are identical except that the first uses a symmetric differential inductor and the second uses a dual inductor in the tank circuit (see Chapter 2). The difference in overall VCO performance due to the 50% difference in Q factor is compared in this section. The S-parameters generated from full-wave electromagnetic simulation are used in SpectreRF to simulate the VCOs. These S-parameters allow more accurate simulation of the parasitic capacitance and resistance than the generalized models of the p-cell inductors included with the design kit.

3.3.1 Transient Simulation

For the symmetric inductor VCO transient simulations, the tank varactor control voltage is set to 2.5 V, tuning the oscillator to the low end of the frequency tuning range. Figures 3.8 and 3.9 show the steady-state voltage and current waveforms at the collectors of Q_1, Q_2, and Q_3 from Figure 3.6 (i.e., the V^+ and V^- terminals and the collector of the tail current bias transistor of the VCO). These plots show that the $-G_M$ transistors turn off fairly well during their negative V_{CE} half cycles and that the current waveforms have little harmonic content when the transistors conduct. Furthermore, V^+ and V^- can swing above the rail voltage due to the inductive load provided by the tank circuit inductor. Figure 3.9 shows the relationship between the tail current and the collector currents in Q_1 and Q_2.

Recalling that the zero crossing points of an oscillating, lossless LC tank circuit are minimally affected by voltage noise injected in the system when the output is maximum (Figure 1.8), the waveforms in Figures 3.8 and 3.9 suggest that the cross-coupled, differential pair oscillator will have good phase noise performance. The transistors inject the majority of their noise into the oscillating tank circuit when they turn on to conduct current. Figure 3.10 plots the collector current spikes from Q_1 and Q_2 along with the differential output voltage swing. The current spikes occur just after the maxima and minima of the output swing, so very little current

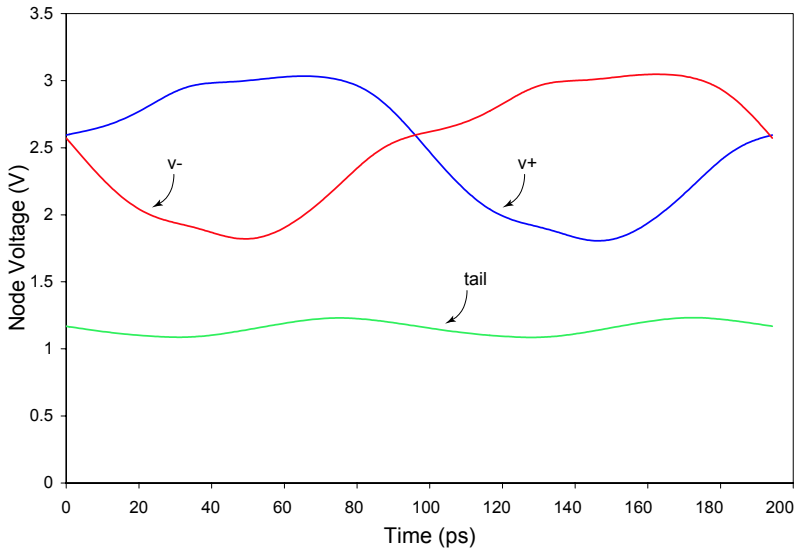

Figure 3.8: Voltage waveforms from time domain simulations of the VCO with a symmetric inductor.

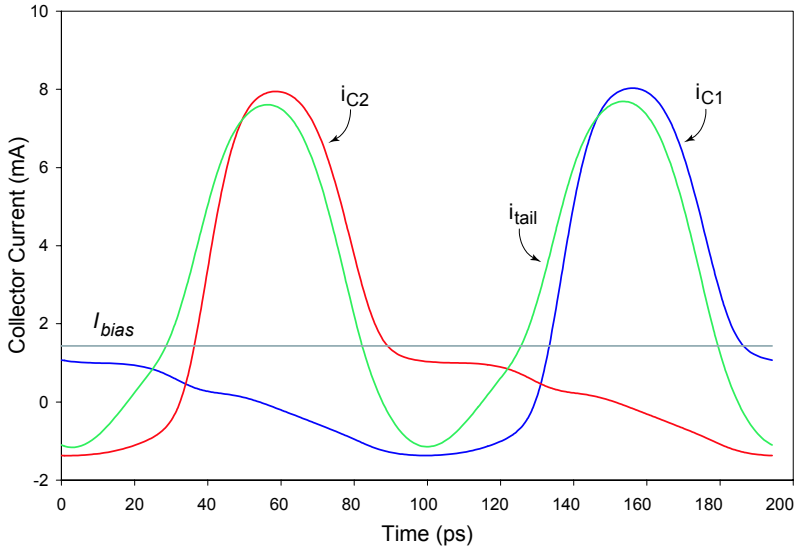

Figure 3.9: Current waveforms from time domain simulations of the VCO with a symmetric inductor. The I_{bias} of a single device is shown, for reference.

is conducted at the zero crossings of the waveform, when the noise-to-phase transfer function is most sensitive.

Similar results were obtained from the dual inductor VCO simulations. Figure 3.11 shows the collector currents from Q_1 and Q_2 of the dual inductor VCO along with the differential output voltage. The current spikes occur at the same times as in the symmetric inductor VCO simulations; however, the peak current is approximately 2 mA lower for the dual inductor VCO. Also, it is clear that the dual inductor permits more harmonic content in the collector current waveforms (note the "shoulder" before each current peak). The lower Q tank circuit allows more harmonic content through a wider bandwidth than the symmetric inductor tank circuit. As a result the transistors conduct current for more of the cycle in the dual inductor VCO, degrading the phase noise performance.

The peak output voltage is also slightly lower for the dual inductor VCO than for the symmetric inductor VCO, since loss in the tank circuit is higher. The output oscillation amplitude can be approximated at high frequencies by [23]:

$$V_{out} = I_{tail} \cdot R_{eq} \tag{3.7}$$

where I_{tail} is the DC current of the tail bias and R_{eq} is the equivalent parallel resistance of the tank circuit. By raising the Q factor and thus R_{eq}, the VCO can oscillate at a higher output voltage for the same tail current. The higher output swing aids in reducing the phase noise. Since the Q of the inductor dominates the overall Q of the tank, the R_{eq} for the two tank circuits can be approximated from the Q factors of the inductors using equation 3.1.

Figure 3.12 compares the output voltage of the dual and symmetric inductor VCO simulation. The difference in output voltage amplitude is only 8%, though estimations from equation 3.7 predict a 20% difference. This discrepancy is most likely due to neglecting the finite Q of the varactors and the loss in the interconnects to the tank circuit in this rough estimation. The two VCOs have different periods for the same varactor control voltage due to the difference in inductance value for the two inductors (Figures 2.9 and 2.10). The frequency of the symmetric inductor VCO is 5.15 GHz, whereas the frequency of the dual inductor is 4.59 GHz.

The VCO tuning characteristics for both VCOs were extracted by simulating at var-

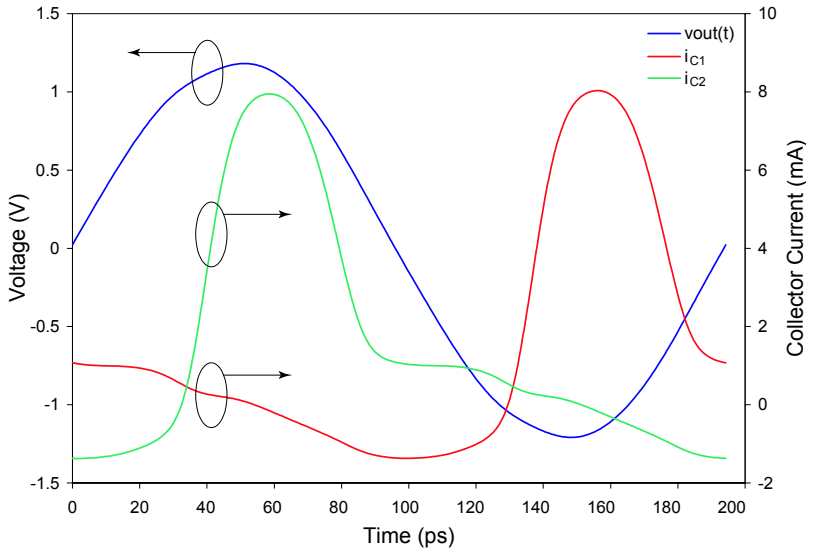

Figure 3.10: Plot of the collector current waveforms with the differential output voltage swing from time domain simulations of the VCO with a symmetric inductor.

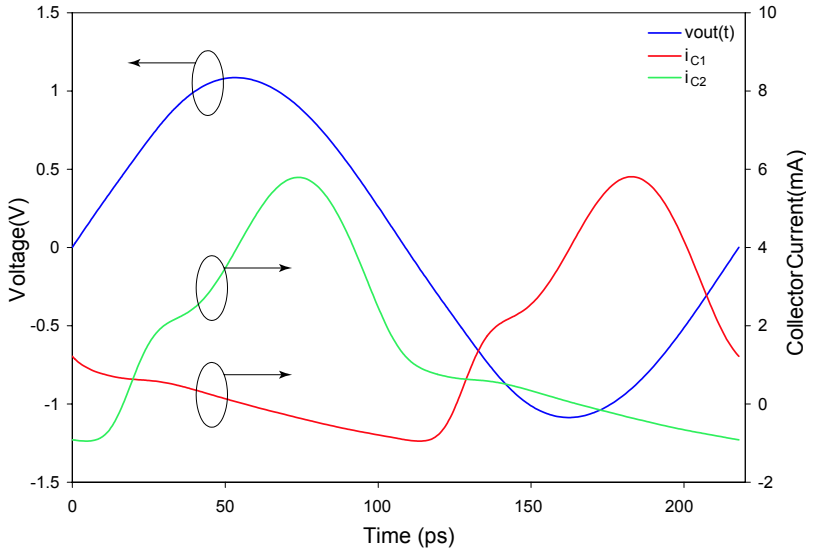

Figure 3.11: Plot of the collector current waveforms with the differential output voltage swing from time domain simulations of the VCO with a dual inductor.

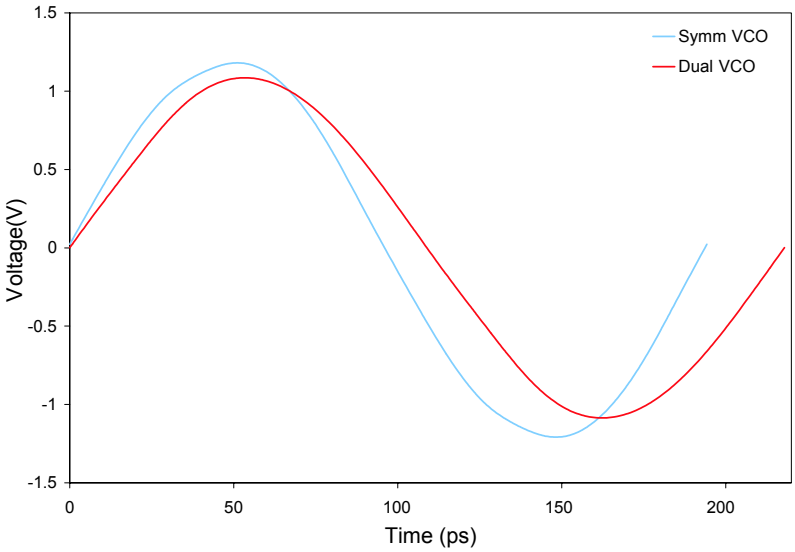

Figure 3.12: Comparison of the differential output voltage swing of the dual and symmetric inductor VCOs for tank varactor control voltages of 2.5 V.

ious varactor tuning voltages. Figure 3.13 shows that the expected tuning range of the symmetric inductor VCO is from 4.64 to 6.31 GHz for tuning voltages from 0.7 to 3.2 V. Using the linear tuning range of the VCO from 1.9 to 2.7 V, the K_v of the symmetric inductor VCO is 1.15 GHz/V. As for the dual inductor VCO, the slightly larger inductance value in the tank circuit lowers the tuning characteristic compared to the symmetric inductor VCO. The simulated tuning range of the dual inductor VCO is from 4.06 to 5.96 GHz for tuning voltages from 0.7 to 3.2 V. In the linear range of the tuning curve, the K_v is 1.36 GHz/V. The simulated tuning range of the symmetric inductor VCO (31%) and the dual inductor VCO (38%) are slightly more than half the expected tuning range of 49% calculated from the varactor tuning range (see Section 3.1.2). This implies that the combination of parasitic and fixed capacitance in both VCOs is on the order of the capacitance of the varactor [17]. The larger tuning range of the dual inductor is most likely due to the higher f_{sr} (i.e., lower parasitic capacitance) as shown previously in Figure 2.11. As discussed in Section 3.1.2, the slope of the tuning curve shown in Figure 3.13 is more gradual than the DC C-V characteristic of the varactor in Figure 3.3. The linear region of the VCO tuning curve extends across 1.0 V, rather than 0.5 V as was the case with the varactor DC/small-signal tuning curve.

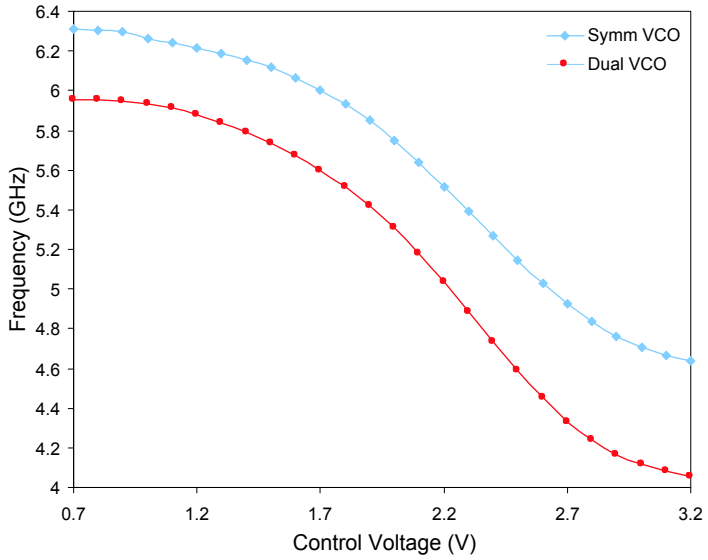

Figure 3.13: Plot of the tuning characteristic for both the symmetric and dual inductor VCOs.

3.3.2 Non-Linear Simulations

Phase noise characterization requires that the non-linear, frequency translation effects of the oscillator be accounted for. The non-linear simulator for SpectreRF is Periodic Steady State (PSS). This non-linear simulator first determines the steady-state solution of the oscillator in the time domain using a shooting method [67]. A shooting method determines initial conditions which lead directly to steady-state operation of the circuit. PSS requires an initial estimate for the output frequency of the oscillator, usually obtained from transient simulations. The simulator then iterates to solve for the actual operating frequency of the oscillator in addition to the steady state initial conditions.

Once the time varying steady-state circuit conditions are obtained over an entire period, non-linear effects such as phase noise can be simulated. Traditional small-signal analyses in SPICE find small perturbations from the fixed DC operating point of the circuit. Similarly, PSS performs small signal analyses to the *time varying* operating point obtained using the shooting method. Using noise as a small signal input to the time varying operating point of the oscillator, the phase noise can be calculated using linear, time varying analysis [68].

VCO	V_{OUT} (V)	I_{DC} (mA)	Phase Noise at 1 MHz Offset (dBc/Hz)	Tuning Range (GHz)
Symmetric	1.18	2.5	-118	$4.64 - 6.31$
Dual	1.09	2.6	-118	$4.06 - 5.95$

Table 3.1: Various simulated characteristics of the symmetric and dual inductor VCOs. The DC currents are for a supply voltage of 2.5 V and the frequency tuning ranges are for tank varactor control voltages from 0.7 to 3.2 V.

One significant disadvantage of PSS analysis is that distributed element networks, such as S-parameter blocks, require infinite dimensional state vectors [68]. Distributed element networks must be either modeled as a network of lumped elements or converted to the time domain using a Fast Fourier Transform before simulation. Thus, S-parameter data from electromagnetic simulation of inductor structures (as in Chapter 2 Section 2.4) cannot be directly used as an N-port block in PSS simulations. However, a circuit block is available from Motorola CDR1 support that translates S-parameter files to a linear model compatible with PSS simulations. The non-linear simulated data presented in this thesis uses this circuit block in conjunction with the Sonnet simulated S-parameters of the inductors. The Harmonic Balance Analysis simulator, available in Agilent Advanced Design System (ADS) [69], is preferred for nonlinear simulation of distributed networks; however, the Motorola CDR1 design kit does not support ADS models.

Contrary to expectations, PSS simulations of both the symmetric and dual inductor VCOs resulted in nearly the same phase-noise spectrum (Figure 3.14). Based on an expected 50% improvement in Q factor alone, Leeson's equation predicts that the improvement in phase noise for the symmetric inductor over the dual inductor is proportional to $10\log(1/Q^2)$, or 3.5 dBc/Hz. However, the phase noise difference is likely greater than 3.5 dBc/Hz for these two VCOs because, in addition to a higher Q inductor, the output power is greater for the symmetric inductor VCO (see equation 1.19). SpectreRF PSS predicts that both VCOs have a phase noise of -118 dBc/Hz at 1 MHz offset and -98 dBc/Hz at 100 kHz offset, exceeding the IEEE 802.11a phase noise specification of -107 dBc/Hz at a 1 MHz offset from the carrier. The results of the linear and non-linear VCO simulations are summarized in Table 3.1.

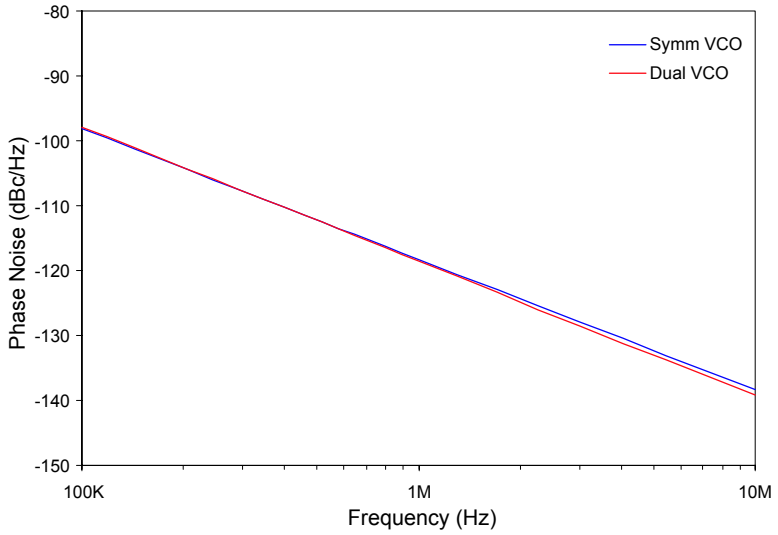

Figure 3.14: Simulated phase noise of the symmetric and dual inductor VCOs.

3.4 VCO Output Buffer Design

The output of the symmetric inductor VCO is a 1.2 V peak sine wave delivered into a 2 kΩ differential load, or −1.4 dBm. The initial design for the output buffer was an HBT differential pair with no input or output impedance matching. Unfortunately, large signal inputs from the VCO to the differential pair compress the buffer and clip the sine waves. Since the VCO is intended for use as the LO pump for a balanced mixer, the distortion of the waveform is not necessarily a problem; the ideal input for a mixer is actually a rail-to-rail square wave that switches the mixing core abruptly. However, the simulations of the differential pair buffer connected directly to the VCO output show that the peak voltage drops from 2.4 V differential at the output of the VCO to 1.6 V differential at the output of the buffer. The less than unity voltage gain of the buffer is a result of operating the amplifier well into the compression region. A buffer that maintains approximately the same voltage level as the VCO output is obviously more desirable.

This work uses a pair of class-B, push-pull, CMOS buffers because their compression points are much higher than that of a simple differential pair. The buffer is designed and laid out in a manner similar to a digital inverter, except that the gates must be DC biased so that both the NMOS and PMOS transistors operate in the saturation

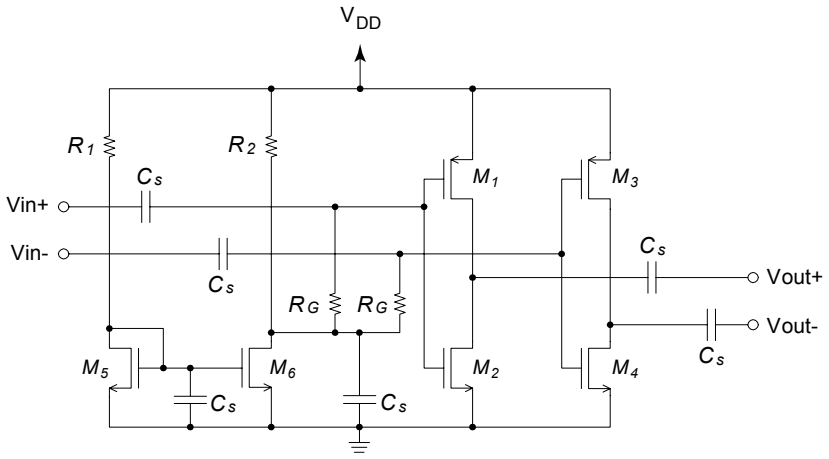

Figure 3.15: Schematic of the VCO output buffer.

regime when no RF signal is applied (Figure 3.15). This sets the input DC bias voltage to the DC output voltage, as long as the two transistors have matched process transconductance parameters, given by:

$$k' = \frac{\mu C_{ox}}{2}\frac{W}{L}$$

where μ is the carrier mobility of the material, C_{ox} is the gate oxide capacitance, and W and L are the gate width and length, respectively. The difference in carrier mobilities (μ_n and μ_p) requires that the transistor gate lengths be scaled to balance the DC input and output voltages. As the RF signal modulates the gate voltages around this DC bias point, the NMOS and PMOS transistors alternate between the saturation regime and the linear regime, creating a push-pull effect which produces the output signal. Simulations show that the CMOS class-B buffer for this work has an input referred 1 dB compression point at approximately 2 dBm while the differential pair buffer has an input referred compression point around -20 dBm (Figure 3.16). The primary cost for the higher compression point with the class-B buffer is higher power consumption.

An HBT differential pair buffer is desirable for lower power consumption and higher gain than a class-B, push-pull, CMOS buffer. A potential solution to the problem with the HBT buffer and the high signal level of the VCO output is to attenuate the signal using a capacitive divider (Figure 3.17). With a signal level below the

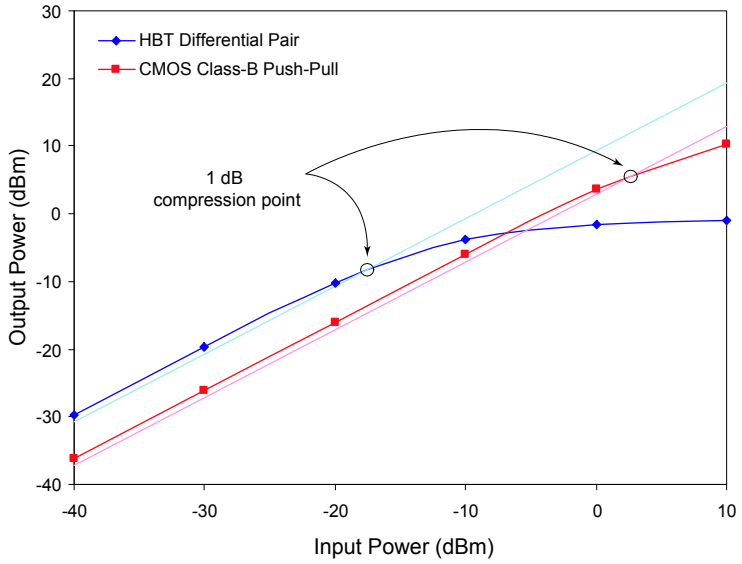

Figure 3.16: 1 dB compression curves of the HBT differential pair buffer and the class-B, push-pull CMOS buffer.

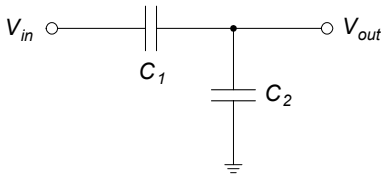

Figure 3.17: Capacitive divider that can be used to attentuate the VCO output before the buffer.

compression point of the buffer, the signal can be fed to an HBT differential pair. The output node in Figure 3.17 should be biased with a low-noise source, since any noise at this node could couple back into the oscillator and increase the phase noise.

Though, in a sense, the generation of a high output power signal in the oscillator is wasted by using the attenuator, a design with a high-gain, HBT differential pair buffer can potentially consume less power than those with buffers with a higher compression point. This allows the VCO core to be designed with a high amplitude output swing for low-phase noise performance and the output buffer to be designed for low-power consumption. Future revisions of the VCO in this work will utilize such a capacitive divider topology.

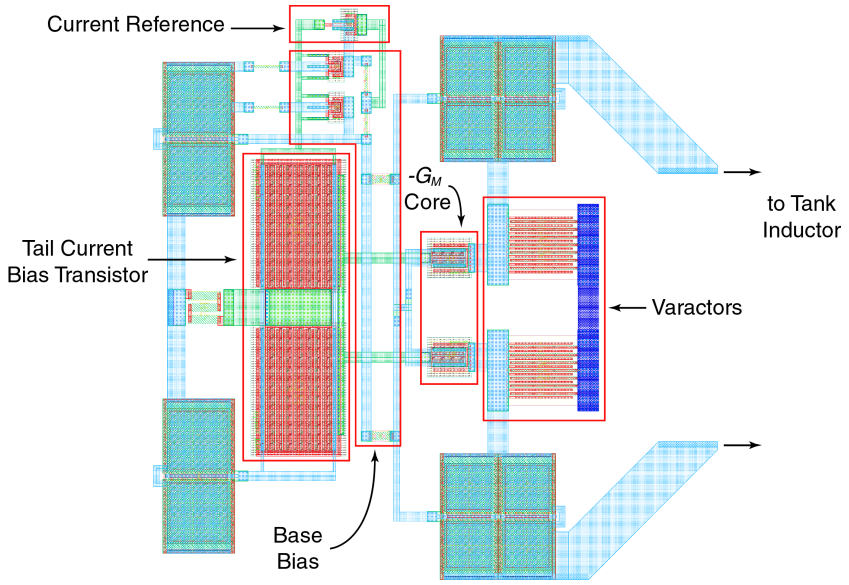

Figure 3.18: Layout of the core VCO used in the symmetric and dual inductor VCOs. Die area occupied is 190 μm $\times$ 192 μm.

3.5 VCO Layout

The two VCO designs are identical aside from the different tank inductor implementations. For proper comparison, both VCOs use the same layout for the $-G_M$ circuit, bias circuit, and tank varactors. Figure 3.18 shows the layout of the VCO core common to both designs. The layout is symmetric about the x-axis of the figure to improve the differential performance of the VCO. The only exception to this symmetry is the current reference and base bias transistors located at the top of Figure 3.18. The outputs of the VCO are taken from the upper plates of the AC coupling capacitors of the $-G_M$ transistors at the upper and lower right corners of the figure. The wide diagonal traces on the right side of the figure connect the circuit with either the symmetric or dual inductor in the final VCO layouts. The area of this portion of the VCO is 190 μm $\times$ 192 μm.

Figures 3.19 and 3.20 show the buffered, symmetric inductor and dual inductor VCO layouts with pads, respectively. The V^+ and V^- output buffers are placed along either side of the VCO core. These buffers have input and output DC blocking capacitors. The input blocking capacitors allow the buffer to be biased for class-B operation while

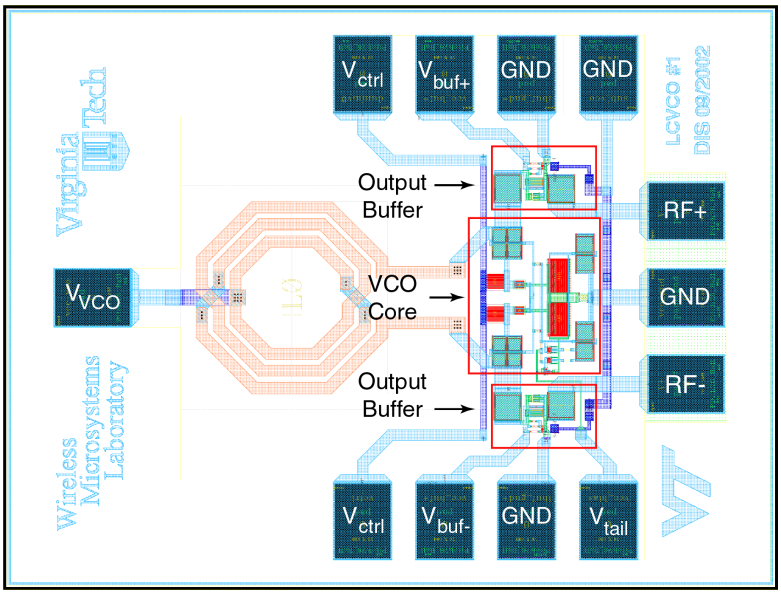

Figure 3.19: Buffered symmetric inductor VCO with pads. The total die area (including pads) is 1 mm × 0.76 mm.

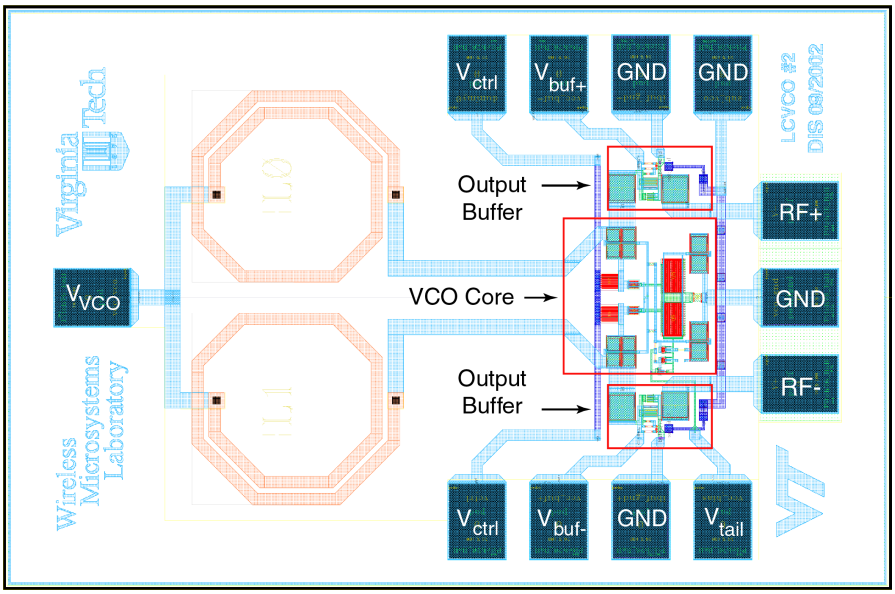

Figure 3.20: Buffered dual inductor VCO with pads. The total die area (including pads) is 1.2 mm × 0.76 mm.

the output blocking capacitors are included to facilitate integration with a tunable polyphase circuit (to be discussed in the Chapter 4). The only difference between these two layouts is the tank inductor. All the pad locations except for the V_{VCO} pin are identical in both layouts. In the dual inductor VCO, the die must be stretched to accommodate the larger area of the dual inductor, so the V_{VCO} pin is located an additional 150 μm further from the other pads compared to the symmetric inductor VCO.

Four separate supply voltage pads exist for both layouts. The V_{tail} pad is connected to the supply rail for the current mirror which provides the tail current of the VCO. Both the V_{buf+} and V_{buf-} pads are connected to the supply rails of the positive and negative output buffers, respectively. The fourth power supply pad, V_{VCO}, provides power to the $-G_M$ cross-coupled differential pair through the tank inductor. On the right side of the chip, the differential RF output bond pads (RF^+ and RF^-) and interconnects from the output buffers are laid out symmetrically to provide the same phase offset for both outputs. Moreover, the pads are located so that bond wires of equal lengths can be extended from the pads to the package pins.

At the time this work was performed, the Motorola CDR1 design kit for Cadence had limited support for parasitic extraction of the layout. Rather than alter the design based on the results of a somewhat unreliable extraction tool, the design was submitted based on the simulations presented in Section 3.3. Since these simulations use the S-parameters from electromagnetic simulation of the inductor, the design takes into account the parasitic capacitance and resistance of the inductor, but not those of the interconnect routing in Figures 3.19 and 3.20.

3.6 Summary

This chapter has presented the design, simulation, and layout of two differential VCOs. The VCOs are identical except that one uses the symmetric differential inductor and the other uses the dual inductor, which were presented in Chapter 2. Simulations of the symmetric inductor VCO predict a differential output amplitude of 1.18 V compared to 1.09 V for the dual inductor VCO. Spectre PSS simulations also predict that both VCOs will have a phase noise of -118 dBc/Hz at a 1 MHz

offset from the carrier for both VCOs (these results are not believed to be accurate). The symmetric inductor VCO has a simulated tuning range from 4.64 to 6.31 GHz for tuning voltages from 0.7 to 3.2 V. In comparison, the dual inductor VCO has a simulated tuning range from 4.06 to 5.95 GHz over the same range of control voltages. The symmetric VCO design is intended to be coupled with a tunable polyphase circuit (presented in the next chapter) to realize a quadrature VCO with phase tunable outputs.

Chapter 4

Tunable Polyphase Filter Design

This chapter presents the circuit design and layout of a *tunable* polyphase filter. As described in Chapter 1, LO sources with tunable phase outputs can potentially be used to improve image rejection in Weaver or Hartley architectures, or eliminate I/Q phase error in direct conversion or low-IF receivers. The tunable polyphase design presented here is subsequently integrated with the symmetric inductor VCO design from Chapter 3 to realize a phase-tunable quadrature output VCO.

4.1 Polyphase Filters and *RC-CR* Networks

Polyphase filters are derived from the classical *RC-CR* phase-shift network shown in Figure 4.1(a). This circuit has two voltage transfer functions, one for each output referenced to the input. The $V_{1,in}$ to $V_{1,out}$ transfer function is:

$$F_{11}(\omega) = \frac{V_{1,out}}{V_{1,in}} = \frac{1}{1 + j\omega RC} \tag{4.1}$$

and the $V_{1,in}$ to $V_{2,out}$ voltage transfer function is:

$$F_{21}(\omega) = \frac{V_{2,out}}{V_{1,in}} = \frac{-j\omega RC}{1 + j\omega RC}. \tag{4.2}$$

A 90° difference in the two output phases exists for all input frequencies due to the $-j$ term in the numerator of equation 4.2. There is, however, only one frequency

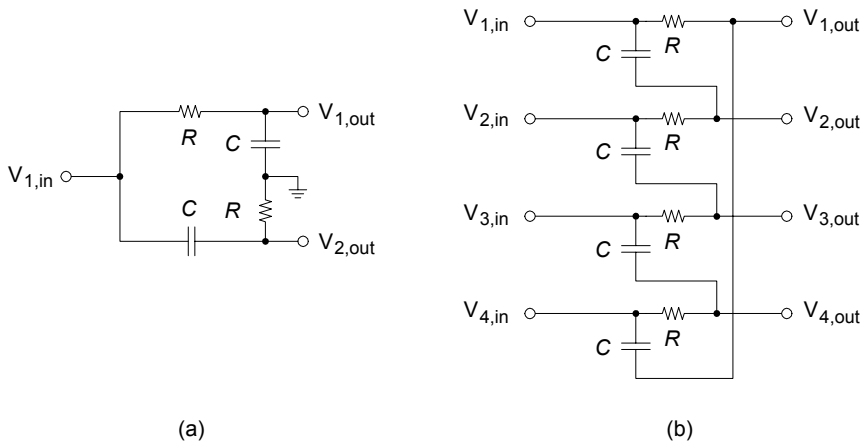

Figure 4.1: Schematic of (a) a *RC-CR* network and (b) a polyphase network.

at which the output amplitudes are equal (i.e., $\omega_0 = 1/RC$). At this frequency, the output phases are shifted by $\pm 45^\circ$ with respect to the input, and the output magnitudes are both equal (i.e., $V_{1,out} = V' \angle -45^\circ$ and $V_{2,out} = V' \angle +45^\circ$).

Figure 4.1(b) shows a single-stage polyphase filter. If the $V_{2,in}$ and $V_{4,in}$ nodes are grounded while the $V_{1,in}$ and $V_{3,in}$ nodes are driven by a differential signal, this circuit is essentially a fully-differential version of the *RC-CR* network shown in Figure 4.1(a). A simple way to understand how this circuit works is to assume (as shown in the *RC-CR* network) that at the frequency $\omega_0 = 1/RC$, the phase shift due to a path through a resistor to an output is -45°, whereas the phase shift due to a path through a capacitor to an output is $+45^\circ$. The output phases are found by adding the phase shift of the resistors and capacitors to the input phases of the $V_{1,in}$ and $V_{3,in}$ nodes (0° and 180°, respectively). Since the $V_{2,in}$ and $V_{4,in}$ nodes are grounded, they do not provide a phase shift to the output. Using this technique, the phases of the four outputs at $\omega_0 = 1/RC$ are:

$$\angle V_{1,out} = 0^\circ - 45 = 315^\circ \tag{4.3}$$

$$\angle V_{2,out} = 0^\circ + 45 = 45^\circ \tag{4.4}$$

$$\angle V_{3,out} = 180^\circ - 45^\circ = 135^\circ \tag{4.5}$$

$$\angle V_{4,out} = 180^\circ + 45^\circ = 225^\circ. \tag{4.6}$$

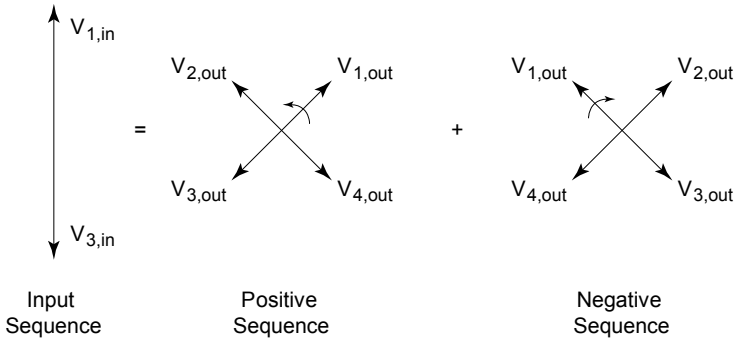

Figure 4.2: Illustration of quadrature generation from a single differential input signal (after [70]).

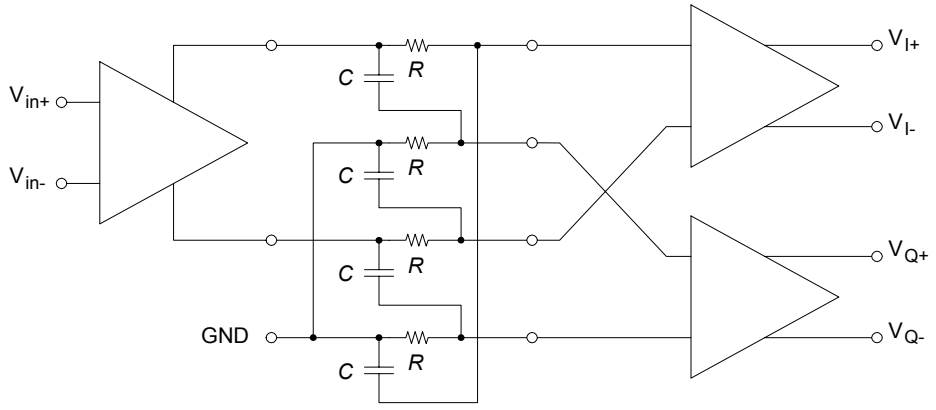

Figure 4.3: Block diagram of a buffered single-stage polyphase filter.

For a more detailed discussion, Appendix B presents the frequency dependant equations for the output phase, based on the derivation of the voltage transfer function matrix of the polyphase and *RC-CR* networks.

From equations 4.3 through 4.6, a single differential input signal is decomposed by the polyphase into a *positive* and a *negative* rotating quadrature sequence (Figure 4.2). The polyphase network rejects the negative rotating sequence and passes the positive sequence to the output if the input frequency is at the $1/RC$ pole. Thus, in addition to quadrature signal generation, the polyphase filter can be used directly for image rejection [70].

The polyphase network introduces frequency dependant loss, requiring the use of differential buffer amplifiers to maintain signal strength (Figure 4.3). The nonlinearity

of the buffers can result in amplitude to phase distortion, limiting the exact quadrature phase difference between output nodes to frequencies near $\omega_0 = 1/RC$. The phase flatness versus frequency can be improved by using multiple polyphase stages and staggering the $1/RC$ poles; however, adding such stages increases loss, so the gain requirements and power consumption of the buffers will also increase [71]. If input and output buffers are used, the gain can be distributed between them to reduce the requirement from any individual buffer.

The input impedance of the filter also depends on the frequency. Both the shunt capacitors and the series DC blocking capacitors before the buffers at the output give the polyphase a highly capacitive input impedance. At the pole frequency, the input impedance of one input reduces to $R \parallel (1/j\omega C)$. As a rule of thumb, the poles should be placed such that the lowest impedance is at the input and the highest impedance is at the output to reduce cascaded loss [70]. Since the polyphase input impedance can be very low, a buffer serves to de-couple the input of the polyphase from the driver circuit.

Another design issue for these networks is component mismatch in the four paths, which can create gain and phase imbalance in the quadrature outputs. While components with large areas decrease the impact of mismatch, the *parasitic* capacitance and resistance can have a much larger effect on output imbalance. Minimization of these parasitics requires careful attention to layout symmetry.

4.2 Tunable Phase Outputs

DC bias requirements at the inputs of the output buffers require that series blocking capacitors be used at the output of the *RC-CR* network. The transfer function of these series capacitors with an equivalent load resistance R_L is:

$$G(\omega) = \frac{j\omega R_L C_s}{1 + j\omega R_L C_s}. \tag{4.7}$$

The phase angle of this transfer function is:

$$\angle G(\omega) = 90^\circ - \tan^{-1}(\omega R_L C_s). \tag{4.8}$$

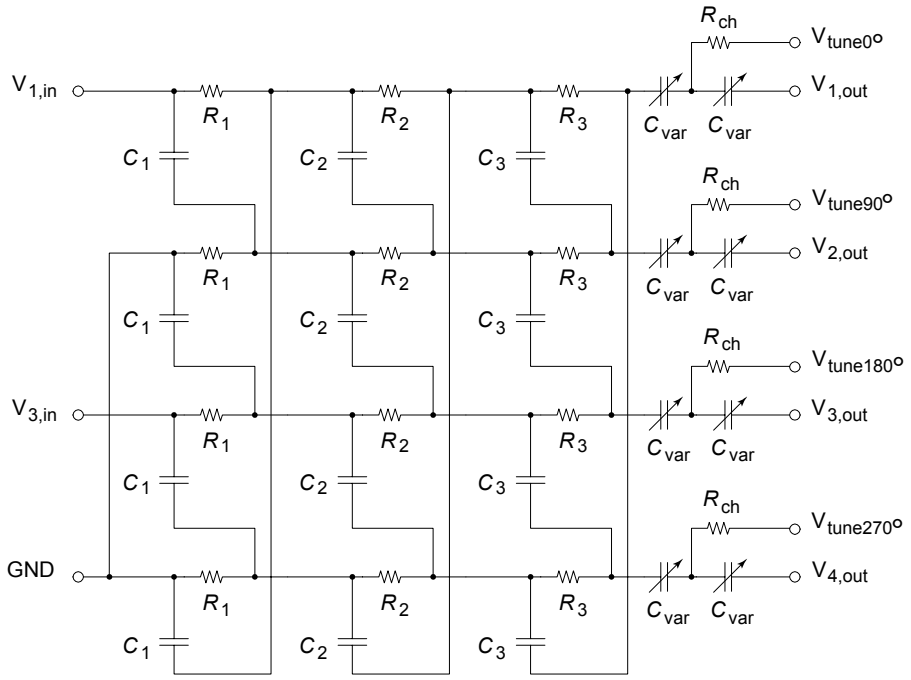

Figure 4.4: Schematic of a three pole polyphase filter which can be used for tunable quadrature phase generation.

The transfer function of each output path of the polyphase is multiplied by equation 4.7 to give the overall transfer function. Typically, the value of C_s is adjusted during the design of the filter so that the phase difference of the four outputs is exactly 90° at the center frequency of the polyphase.

If tunable capacitors (varactors) are used in the place of these series output capacitors, the phase can be *tuned* in the circuit post-fabrication. Figure 4.4 shows a three-pole polyphase filter with a series varactor at each of the four outputs. The capacitance is tuned by four output phase control voltages (V_{tune0}, $V_{tune180}$, V_{tune90}, and $V_{tune270}$). The resistors (R_{ch} = 100 kΩ) in series with the phase control voltage nodes prevent RF leakage into the DC supply path.

All four varactor control voltages can be tuned together using the same voltage in order to adjust the *frequency* at which all the output phases differ by exactly 90°. Tuning the V_{tune0} and $V_{tune180}$ control voltages to the same voltage while separately tuning the V_{tune90} and $V_{tune270}$ control voltages together to a different voltage changes the I/Q phase balance of the outputs. Similarly, tuning all of the control voltages

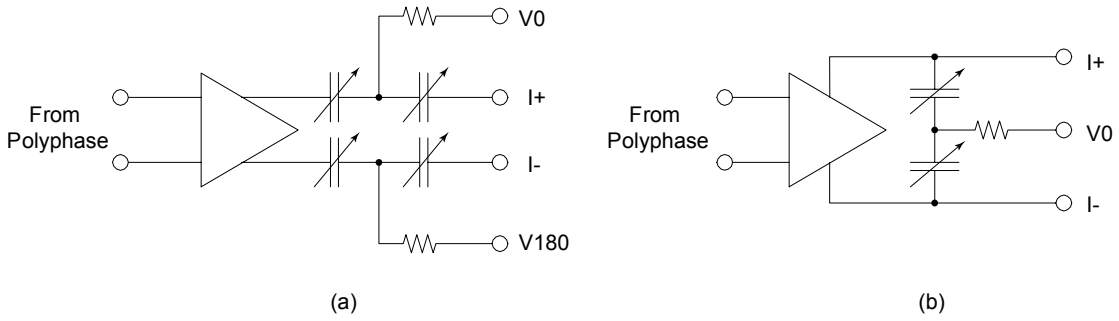

Figure 4.5: Alternate tunable phase configurations after the polyphase output buffers include (a) series varactors and (b) parallel varactors.

independently allows relative phase tuning of the positive and negative outputs of both the I and Q channels in addition to I/Q phase tuning.

Another possibility for tunable phase is to include the series varactors *after* the polyphase output buffers [Figure 4.5(a)]. This approach exposes the varactors to large signal swings, which may be desirable to smooth the tuning range of the output phase [61]. The varactors can also be placed in parallel with the differential output buffer [Figure 4.5(b)]. This implementation exposes the varactors to the full swing of the output differential signal, as in the case of the varactors in the tank circuit of the differential VCO in Figure 1.10. Simulations show that parallel varactors can provide as much as twice the tuning range as the series equivalent. However, parallel varactors do not allow the independent differential signal path tunability available in the series varactor approaches.

4.3 Circuit Design and Simulation

4.3.1 Three-Stage Polyphase

The design of a tunable polyphase (as shown in Figure 4.4) consists of selecting the frequencies of the three poles for optimal phase flatness across the band of interest and selecting the appropriate varactor size to provide sufficient phase tuning range. For multiple stage polyphase filters, it has been suggested that two of the poles be placed at the edges of the frequency passband and the remaining poles should

be equally spaced along the logarithmic frequency axis [70]. This pole placement essentially gives the filter an equiripple response. Therefore, a three-pole polyphase designed for operation across all three of the U-NII bands should have poles located at 5.15 GHz, 5.477 GHz, and 5.825 GHz. For the polyphase design in this thesis, the capacitors C_1, C_2, and C_3 were chosen to be 500 fF in order to set the size of the resistors around 50 Ω. An advantage of using small resistance values is that the Motorola CDR1 process has a low value resistor with a fairly large area, thereby reducing component mismatch. The exact value of the resistors R_1, R_2, and R_3 were calculated using $R_n = 1/\omega_n C_n$.

The maximum capacitance of the varactors, C_{max}, is set by two factors: the desired phase tuning range and the required area. The gate area was selected via simulation to give the varactor a C_{max} of 730 fF, in order to achieve ±4° of I/Q imbalance tuning. Larger varactors would provide a greater tuning range; however, ±4° is sufficient to correct for typical I/Q phase imbalances.

SpectreRF frequency domain simulations of the unbuffered polyphase show the generation of perfect quadrature phases at the outputs with all four output phase control voltages set to zero (Figure 4.6). Taking the difference between the neighboring curves in this plot shows the I/Q phase imbalance versus frequency (Figure 4.7). Simulations predict that I/Q imbalance will vary less that 0.004° for frequencies from 5 to 6 GHz. It is not expected that the fabricated circuit will have the bandwidth predicted by these simulations since parasitic resistances and capacitances are not included. Moreover, the buffers will reduce the phase flatness bandwidth substantially by converting amplitude imbalance to phase imbalance. The polyphase is driven with 50 Ω sources and loaded with 1 kΩ resistors. With these input and output impedances, the combined gain requirement for the input and output buffers to overcome simulated loss in the polyphase filter is 11.5 dB.

Figure 4.8 shows the simulated tunable output phase of the 3-pole filter. The plot shows the I/Q phase imbalance for various polyphase varactor output control voltages up to 1.25 V. Beyond 1.25 V, the output phase changes negligibly due to the small-signal tuning characteristic of the varactors (see Figure 3.3). If all four output varactor control voltages are set to zero, the I/Q imbalance is zero (i.e., exactly 90° phase difference between I and Q channels). However, if the Q channel output varactor control voltages are held constant at 0 V while the I channel output varactor

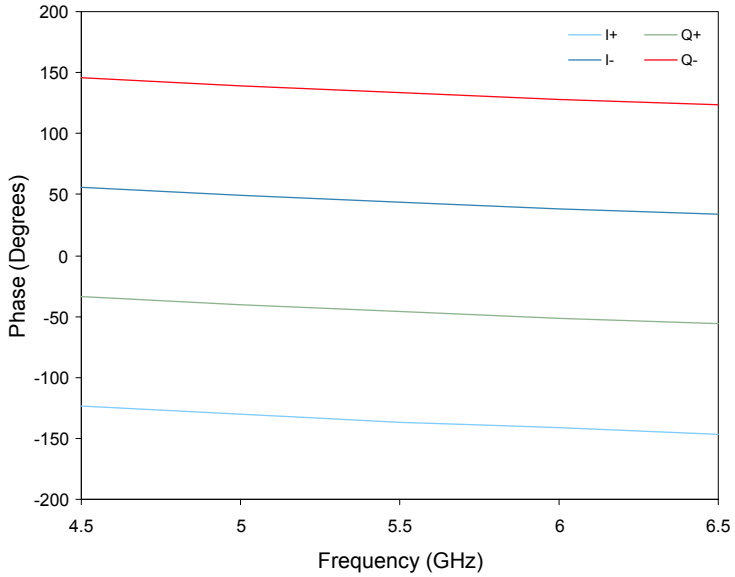

Figure 4.6: Simulated output phase versus frequency of the tunable three-pole polyphase filter. The output phase control voltages are all set to 0 volts.

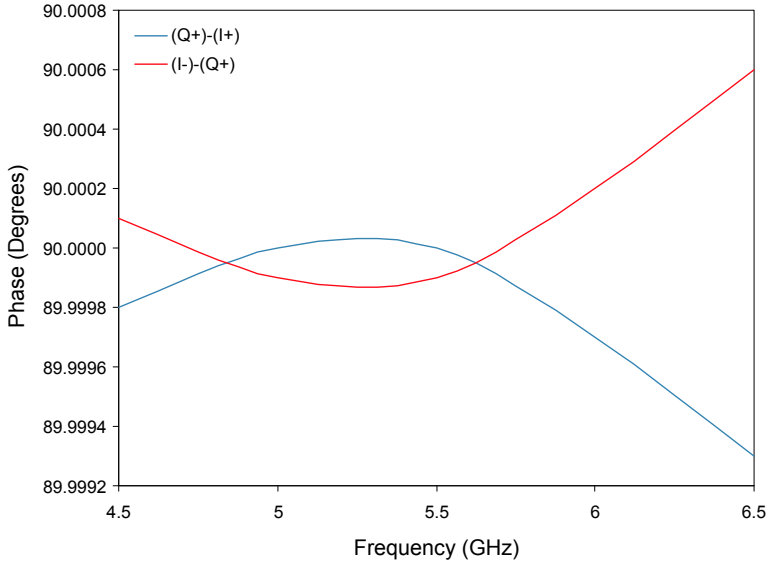

Figure 4.7: Simulated I/Q imbalance versus frequency for all output phase control voltages set to 0 volts.

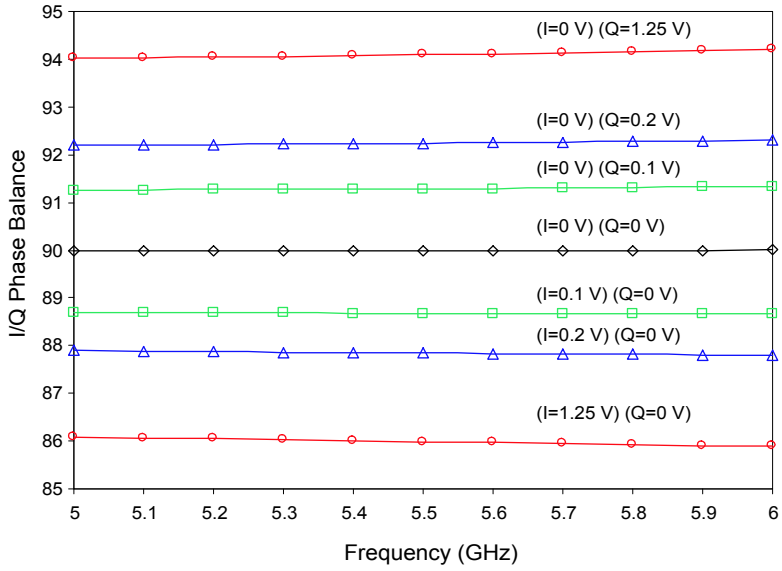

Figure 4.8: Simulated tunable I/Q imbalance versus frequency for several I and Q output phase control voltages.

control voltages are increased, the phase error increases to a maximum of $+4°$. In contrast, the phase imbalance decreases to a minimum of $-4°$ by holding the I channel output varactor control voltages constant at 0 V while increasing the Q channel control voltages. This bidirectional phase tunability allows the polyphase network to compensate for a total of $8°$ of phase imbalance.

4.3.2 Polyphase Output Buffers

Two circuits employing tunable polyphase filters were designed: a stand-alone polyphase with integrated input and output buffers; and a symmetric inductor VCO integrated with the buffered tunable polyphase. To facilitate characterization of the stand-alone polyphase, the polyphase input buffers were chosen to be identical to the VCO output buffers described in Section 3.4 (Figure 3.15). This allows the performance of the stand-alone polyphase to be tested under similar conditions to the integrated VCO and polyphase.

The polyphase output buffer is a HBT differential pair design (Figure 4.9). Low-threshold voltage NMOS transistors bias the differential pair in order to increase

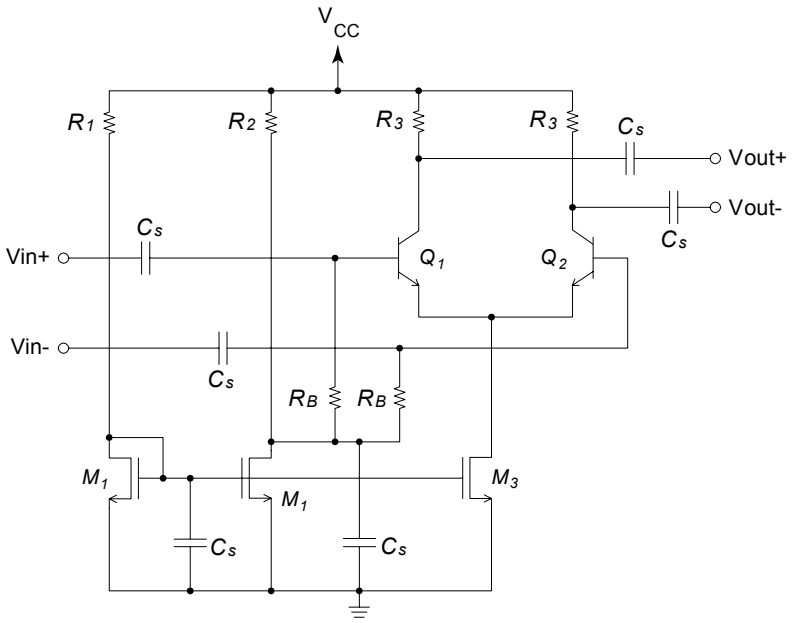

Figure 4.9: Schematic of the polyphase output buffer.

Buffer	Power Gain (dB)	1-dB Compression (dBm)	DC Current (mA)	DC Power (mW)
Input	13.76	2.21	16.0	40.4
Output	11.47	−19.95	2.74	6.86

Table 4.1: Simulated characteristics of the input and output buffers for the three-pole polyphase filter.

headroom for the HBTs. Power consumption and device size were selected to compensate for the predicted 11.5 dB of loss though the filter. Two instances of this buffer are required since the polyphase has differential I and Q channel outputs. Thus, small overall area and low power consumption are critical.

As with the VCO output buffer, Periodic Steady State (PSS) simulations in Spectre are useful for this buffer to ensure a relatively clean sinusoidal output for the expected drive level. The simulated results of both the input and output buffers for the polyphase filter are given in Table 4.1. It should be noted that the input buffer provides over 13 dB of power gain, but −2.02 dBV voltage loss. This occurs because of the impedance change from 1 kΩ single-ended at the buffer input to 50 Ω single-ended at the output.

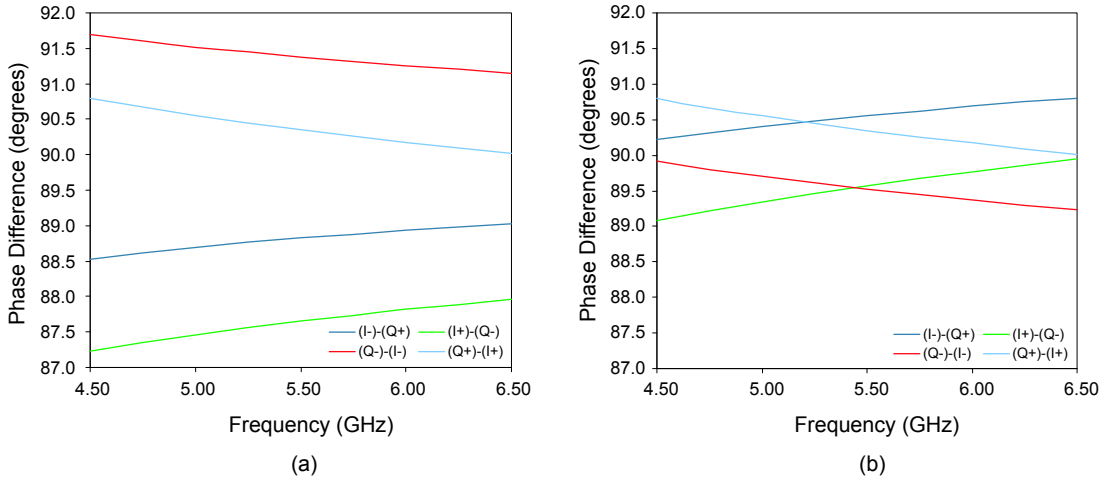

Figure 4.10: (a) Simulated output phase differences of buffered polyphase with all the output varactor control voltages set to 0 V. (b) Simulated output phase differences with the polyphase output varactor control voltages optimized to minimize I/Q imblance over the 5-6 GHz band.

Simulations of the buffered polyphase show the effect of amplitude to phase distortion on the I/Q imbalance as described in Section 4.1. The phase imbalance and flatness versus frequency are shown in Figure 4.10(a) for the case where all the output phase control voltages are set to 0 V. The phase slope is substantially increased to $+1.5°$ for Q channel phase errors and $-2.5°$ for the I channel phase errors from 5.15 to 5.825 GHz. This phase error is quite large compared to the unbuffered polyphase simulations shown in Figure 4.7. However, the tunable phase outputs can be used to mitigate the I/Q imbalance of the polyphase. For example, Figure 4.10(b) shows the reduction of the I/Q phase imbalance to less than $\pm 1°$ over the band of interest by setting $V_{tune0} = 0$ V, $V_{tune90} = 0.11$ V, $V_{tune180} = 0$ V, and $V_{tune270} = 0.2$ V. The difference in the V_{tune90} and the $V_{tune270}$ control voltages tunes out the differential imbalance of the Q channel outputs. The offset from 180° phase difference between Q^+ and Q^- is most likely introduced by the two CMOS class-B input buffers, which are not truly differential. A differential pair buffer at the input would reduce this imbalance and allow more of the phase tuning range to be used toward balancing the I/Q phase mismatch.

The same techniques used to reduce phase imbalance can be used to intentionally create an *imbalance* at the polyphase output to match phase differences generated in

other sections of the RF system and at other frequencies. For example, as discussed in Chapter 1, this induced imbalance can be used to improve the image rejection ratio (IRR) of a Weaver architecture.

The simulated $\pm 5^\circ$ phase flatness bandwidth of the buffered polyphase filter is much greater than the 2 GHz band covered by the SpectreRF simulation [Figure 4.10(b)]. However, it is not likely that the fabricated polyphase will have such a large phase flatness bandwidth. As with the VCO (see Chapter 3 Section 3.5), the polyphase was not simulated with parasitic extraction due to limitations with the tools, so these simulations are overly optimistic.

4.3.3 VCO and Tunable Polyphase Circuit

A quadrature VCO with tunable polyphase outputs was created by connecting the output of the symmetric inductor VCO [Figure 2.7(b)] to the input of the three-stage polyphase with output buffers. In this design, the output buffer of the VCO serves as the input buffer for the polyphase. The primary purpose of the buffer is to prevent the low input impedance of the polyphase from loading down the VCO output tank circuit.

Figure 4.11 shows the simulated quadrature output waveforms of this polyphase VCO. The simulated peak output is approximately 0.3 V lower in the VCO with polyphase outputs than in the symmetric inductor VCO because the loss through the polyphase is not completely compensated by the gain of the buffers. The simulated DC current consumption of this VCO with polyphase outputs is 23.98 mA, which is the sum of the current from the symmetric inductor VCO, the input buffer, and two instances of the output buffer. As with the symmetric and dual inductor VCOs, power consumption could be reduced in this circuit by using a capacitive divider at the output of the VCO followed by a differential pair buffer at the input of the polyphase.

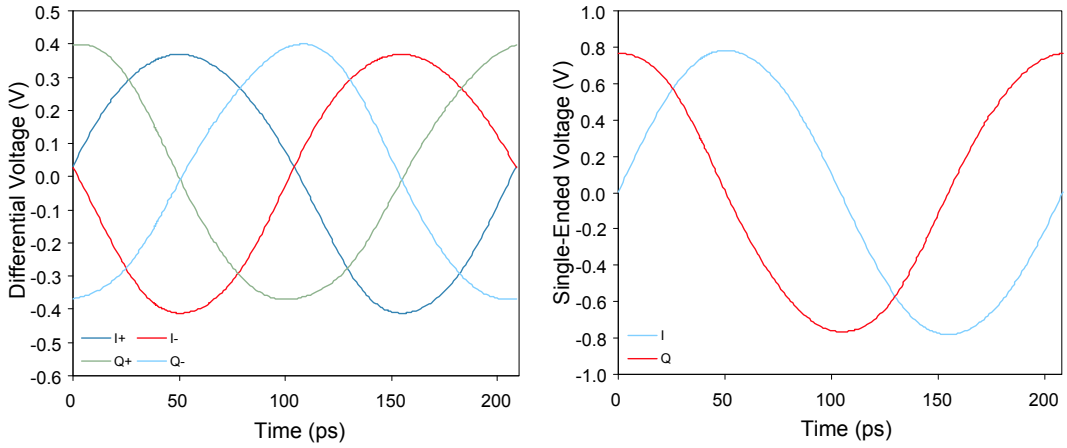

Figure 4.11: Simulated (a) waveforms from the the four individual outputs of the polyphase and (b) differential waveforms of the I and Q channels at output of the quadrature VCO with phase tunable outputs.

4.4 Circuit Layout

4.4.1 Three-Stage Polyphase

Parasitic resistances and capacitances in the polyphase layout will shift the poles of the filter and degrade the phase flatness versus frequency. Conductor loss of the interconnect metal creates parasitic resistance, and the dielectric between the traces and the substrate or between two overlapping traces creates parasitic capacitance. Parasitic extraction can be used to factor these resistances and capacitances into the design and achieve the desired bandwidth. However, these parasitics will, nevertheless, create I/Q phase imbalance at the outputs if they are different for each path through the circuit. Therefore, a layout which creates equal parasitics for each path through the polyphase is necessary to minimize imbalance.

Figure 4.12 shows the layout for the three-pole polyphase filter with tunable outputs. This layout emphasizes equalizing the parasitics for each path through the circuit. For example, the input and output metal traces are intertwined with vias and underpass metal so that each trace sees the same parasitic capacitance. The inner traces see parasitic capacitance from the left and right, while the outer traces only see parasitic capacitance from one side. Weaving the traces gives each path the same total distance

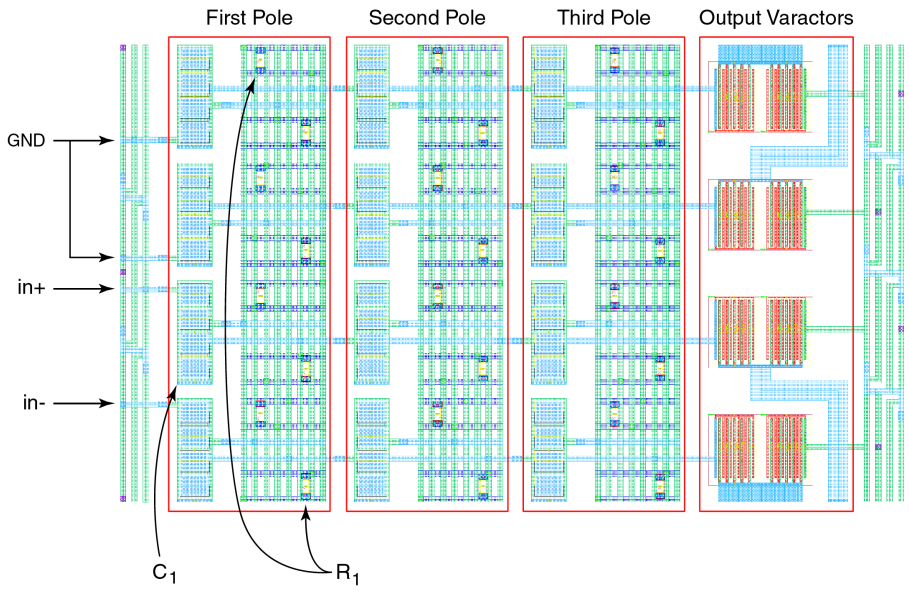

Figure 4.12: Layout for the three-pole polyphase filter. For reference, the location of C_1 and R_1 from the $V_{1,in}$ node in Figure 4.4 is labeled. Die area occupied is 276 μm $\times$ 161 μm.

spent as both an inner and an outer trace.

The resistors in Figure 4.4 are each doubled and implemented as a parallel combination to increase the layout area of each resistor, thereby decreasing the impact of component mismatch. Unfortunately, this parallel combination increases the number of traces required to connect the resistors and capacitors, making trace overlaps unavoidable. To equalize the parasitic effect of overlapping traces, a grid of vertical and horizontal running interconnects is laid out. Vias connect the resistors to horizontal traces which connect the resistors to the subsequent stage. Similarly, vertical traces connect the two resistors in parallel. The grid presents an equal number of overlaps for each of the traces connecting the resistors and capacitors of the stage.

The output varactors are located at the far right of Figure 4.12. Each of the output pairs of varactors are connected at a center node where the DC tuning voltage is applied (Figure 4.4). Large off-chip resistors are necessary to prevent RF signals from leaking out the DC tuning voltage lines. Without these resistors, the RF signal would shunt to ground through the DC supply rather than into the second series varactor and on to the output buffers.

4.4.2 Tunable Polyphase

A stand-alone tunable polyphase was laid out for characterization purposes. Figure 4.13 shows the die layout, including the input and output buffers, the three-pole polyphase filter, and the bonding pads, for this circuit. The two differential inputs are located on the left side of the chip (labeled in^+ and in^-) and the quadrature outputs are located on the right (labeled Q^+, Q^-, I^+, and I^-). These pads are placed so as to minimize differences in bond wire lengths between the four output paths, and between the differential input paths to pins of the package. The output phase control voltage bond pads are located on the top and bottom of the chip (labeled V_0, V_{180}, V_{90}, and V_{270}).

A ring of grounded substrate ties surrounds the polyphase filter. These ties help maintain the substrate at a constant ground potential and limit noise currents from propagating into the capacitors and interconnects of the polyphase filter.

4.4.3 VCO with Tunable Polyphase Outputs

The layout of the VCO with polyphase outputs is created by combining the layout of the symmetric inductor VCO shown in Figure 3.19 and the layout of the standalone polyphase shown in Figure 4.13, except that the input buffer of the polyphase is omitted. Instead, the class-B output buffers of the VCO are routed directly to the inputs of the polyphase.

The layout of the VCO with polyphase outputs is shown in Figure 4.14. For the most part, the pad locations are maintained at the same locations in the VCO with polyphase outputs as were used in the individual symmetric inductor VCO and the tunable polyphase layouts. Where the two circuits are connected, the input buffer bias pads from the stand-alone polyphase (labeled V_{ibuf} in Figure 4.13) are eliminated. The remaining pads from the polyphase filter layout maintain the same order, but are shifted slightly to allow equal spacing between each pad.

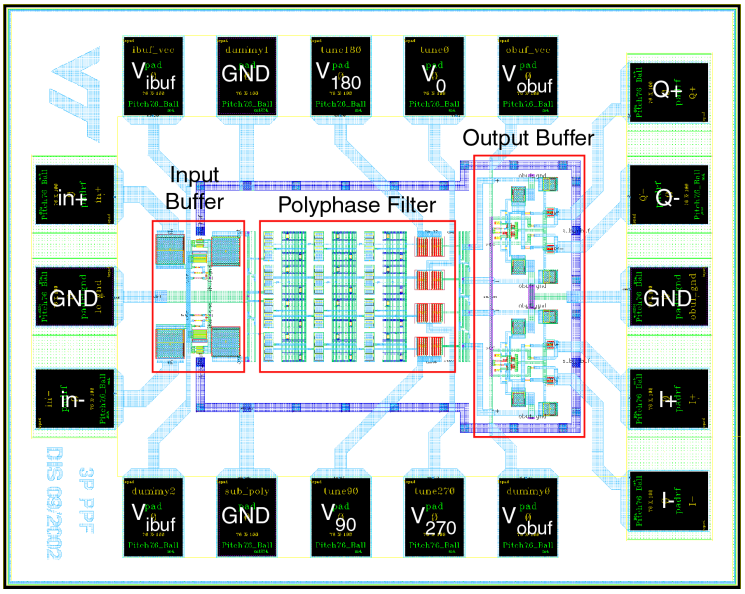

Figure 4.13: Layout of the standalone polyphase filter with tunable outputs. The total die area (including pads) is 920 μm $\times$ 755 μm.

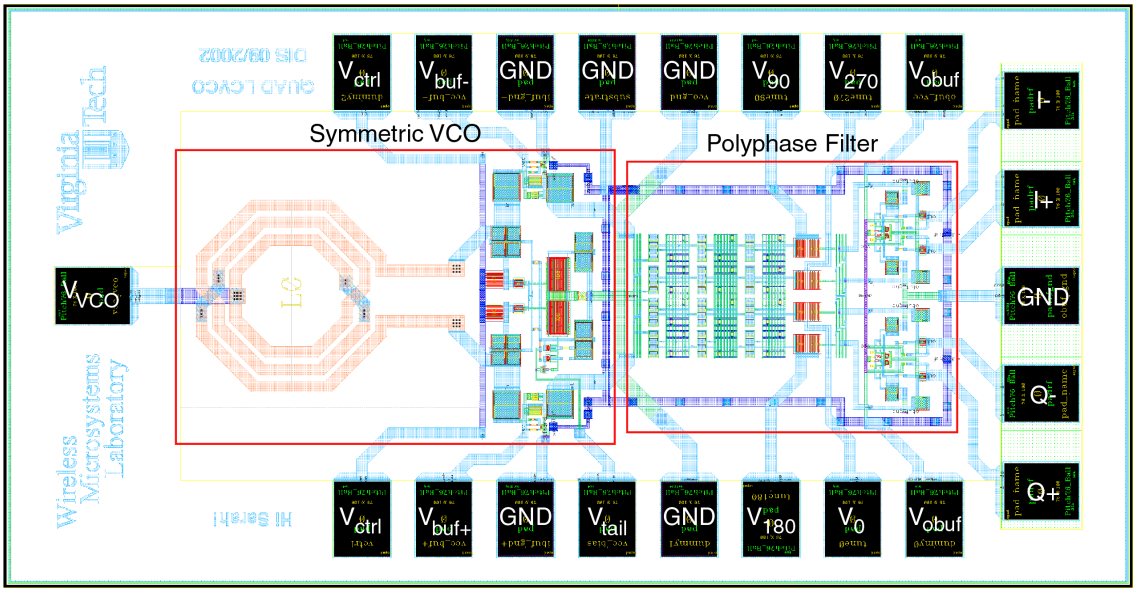

Figure 4.14: Layout of the quadrature VCO combining the symmetric VCO and tunable polyphase filter. The total die area (including pads) is 1.47 mm $\times$ 0.76 mm.

4.5 Summary

This chapter has presented the design and simulation of a tunable three-pole polyphase filter. The simulated results of the unbuffered polyphase network predict that the polyphase filter should be able compensate for a total I/Q imbalance of 8°. This tunability allows the buffered polyphase filter to achieve less than ±1° phase imbalance over the 5-6 GHz bandwidth of interest. In contrast, this tunability can also be intentionally introduced to compensate for phase error in other sections and frequencies of the RF system (e.g., the Weaver architecture). Furthermore, this chapter has presented layout techniques used to equalize parasitics and reduce I/Q imbalance in the polyphase filter. The polyphase design is used in a stand-alone polyphase filter circuit, and in conjunction with the symmetric inductor VCO of Chapter 3 to create a VCO with tunable polyphase outputs. Characterization of the fabricated circuits (including the tunable polyphase filter) will be presented in the next chapter.

Chapter 5

Fabrication and Measurements

Four test circuits, representing the major circuit blocks described in Chapters 3 and 4, were fabricated on one reticle of a Motorola 0.4 μm CDR1 SiGe BiCMOS fabrication run: (1) symmetric inductor VCO (Figure 3.19), (2) dual inductor VCO (Figure 3.20), (3) stand-alone tunable polyphase filter (Figure 4.13), and (4) quadrature VCO with tunable polyphase outputs (Figure 4.14). *This chapter will refer to the quadrature VCO with tunable polyphase outputs as the "polyphase VCO."* In addition to these four circuits, area on another die was set aside for stand-alone symmetric and dual inductors with pads for characterization via on-wafer probing. This chapter covers the packaging of the four circuits for test and measurement, measured data from on-wafer probing of the inductor sites, and measured data from the packaged VCO and polyphase parts.

5.1 Packaging and Test Boards

The four VCO and polyphase die were packaged in Amkor 4 mm $\times$ 4 mm MicroLeadFrame (MLF) packages with 2.3 mm $\times$ 2.3 mm die flags and either 12, 16, or 20 pins. Bond wire diagrams for each of the four parts were specified with equal bond wire lengths for the RF inputs and outputs. Unfortunately, the lot of polyphase VCO parts were irrecoverably damaged by the vendor during the packaging process. Efforts are currently underway to recover some samples of this circuit from an unsawed wafer section.

The initial packaging plans for the symmetric and dual inductor VCOs called for smaller, eight-pin, 3 mm $\times$ 3 mm packages; however, it was subsequently determined that a larger 4 mm $\times$ 4 mm package was needed to accommodate the down bonds. The larger package has a minimum of 12 pins, so the bond wire pinouts for the VCOs were adjusted in process by the vendor. As a result, the differential outputs of the symmetric and dual inductor VCO packaged parts unfortunately do not have the equal bond wire lengths as was specified in the initial designs.

Figure 5.1 shows the final (vendor modified) bond wire diagrams of each of the four packaged parts. The symmetric and dual inductor VCOs have identical pinouts and bond wire lengths to facilitate comparison of the measured results. Likewise, the bond wires of the RF outputs of the stand-alone polyphase filter and the polyphase VCO are similar. However, since the polyphase VCO has five pins per side and the polyphase filter has four pins per side, the spacing of the RF output bond wires differs slightly for the two parts.

The test boards were fabricated through Motorola SPS on two layer material: a top layer of 0.02 inch (0.508 mm) Rogers R4003 and a bottom layer of 0.034 inch (0.8636 mm) FR4. The board is plated with 1 oz. copper. Both the symmetric and dual inductor VCOs have identical board layouts, so only three test board designs were required for the four packaged parts (Figure 5.2). As with the RF input and output bond wires, the RF output traces of the polyphase and polyphase VCO are identical except for the pin spacing of the package. A through calibration standard for the RF traces on each of these boards was made by directly connecting the RF^+ and RF^- traces at the pin location. An S_{21} measurement of these standards allows the loss from the boards to be deembedded from the measurements. The in^+ and in^- input traces of the polyphase filter board are identical to the Q^- and I^+ output traces, reducing the number of calibration standards required.

5.2 On-Wafer Inductor Characterization

The unsawed wafer section with symmetric and dual inductor structures (Figure 5.3) was probed using two GSG RF probes. Appendix C contains the Matlab code based on the development in Appendix A which was used in this work to calculate the

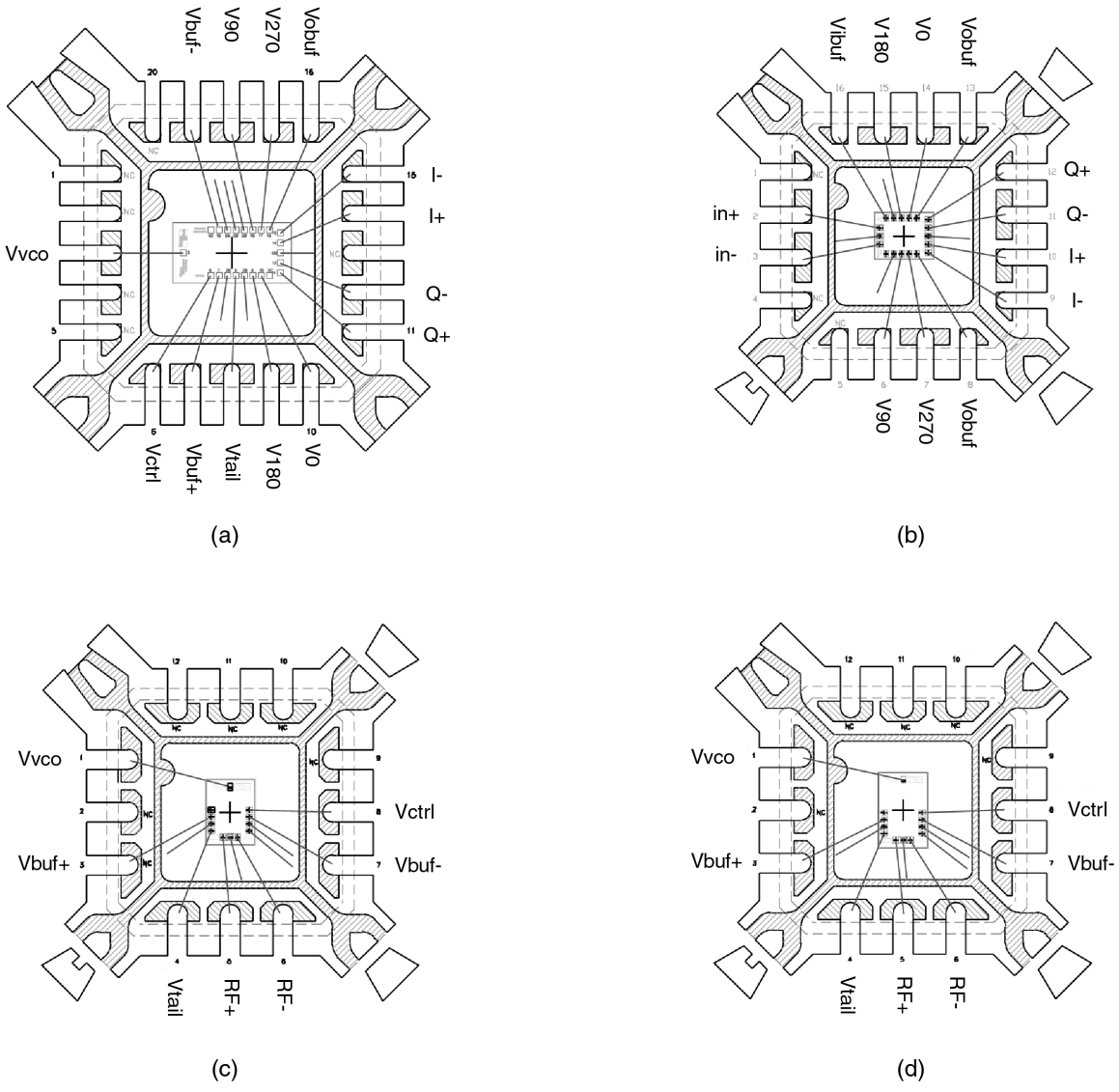

Figure 5.1: Bond wire diagrams of the (a) quadrature VCO with tunable polyphase outputs, (b) standalone tunable polyphase, (c) symmetric inductor VCO, and (d) dual inductor VCO.

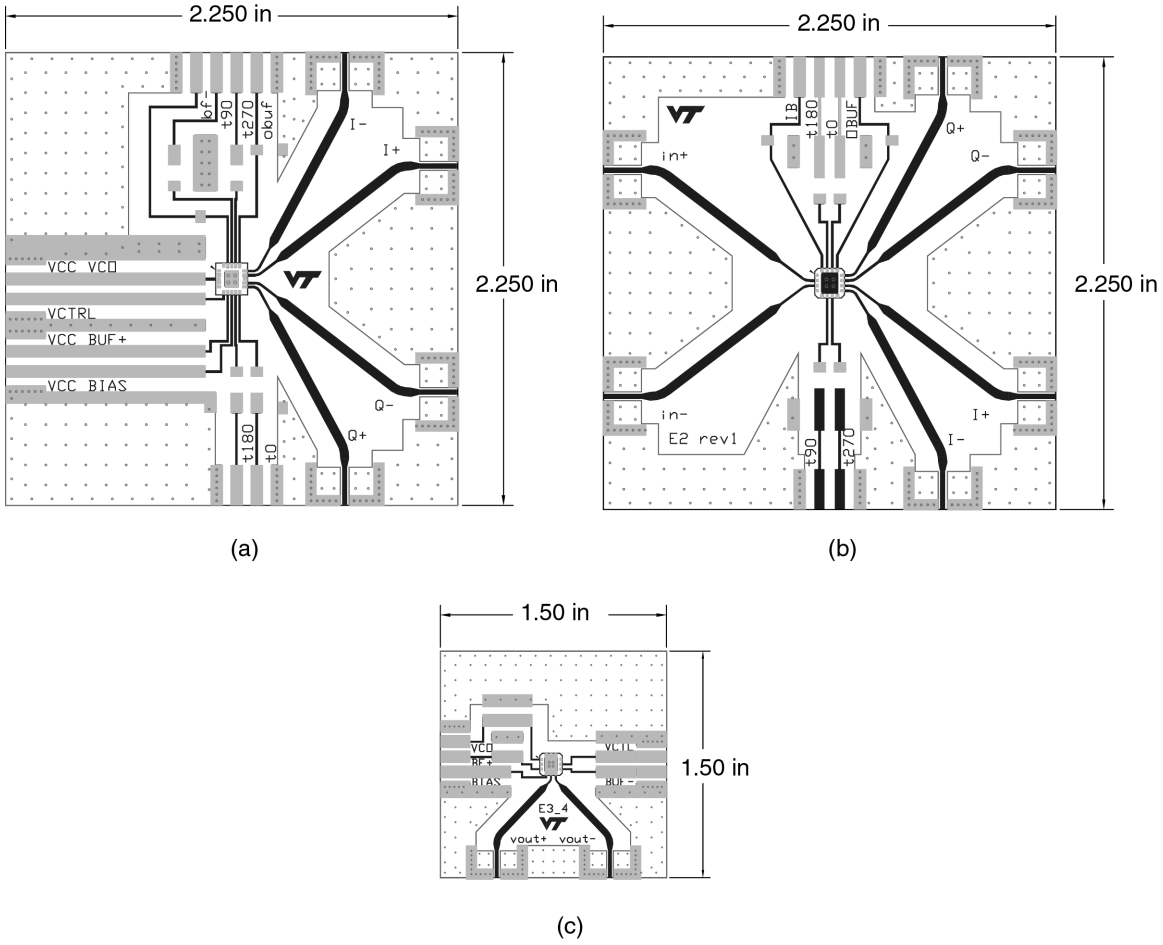

Figure 5.2: Board designs for the (a) polyphase VCO and (b) the standalone, tunable polyphase. The I/Q output traces are identical at the board level. (c) Board layout for the symmetric and dual inductor VCOs.

effective inductance and the differential Q factor from the two-port S-parameters of each structure.

The probe pads add considerable loss to the measurements because they act as large shunt capacitors coupling some of the RF signal into the lossy Si substrate. Unfortunately, due to space limitations, deembedding standards for the pads were not included on the fabricated die. Therefore, to attempt to remove the effect of the pads from the measured data, the S-parameters of open and short circuited pad standards were simulated in Sonnet and then deembedded in Matlab. The shunt loss is deembedded by subtracting the Y-parameters of the open pad structure from the total

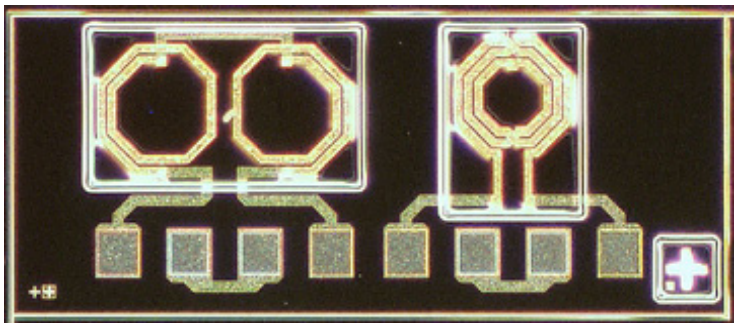

Figure 5.3: Photo of the symmetric and dual inductor structures.

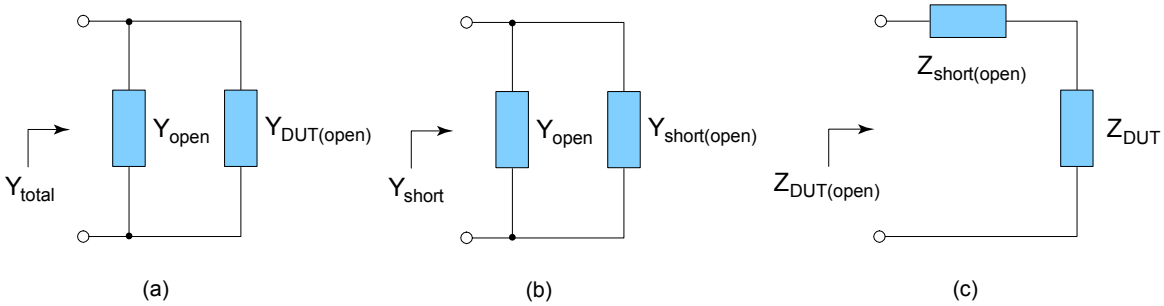

Figure 5.4: Procedure used for deembedding open and short pad standards. First, (a) the Y-parameters of the open standard are subtracted from the total measured data, and (b) the Y-parameters of the open standard are subtracted from the Y-parameters of the short standard. Second, (c) the Z-parameters of the open-corrected short standard are subtracted from the Z-parameters of the open-corrected device under test (DUT).

measured Y-parameters of the device under test (DUT) [Figure 5.4(a)]. In addition, the Y-parameters of the open standard must be subtracted from the Y-parameters of the short standard [Figure 5.4(b)]. After converting these results to Z-parameters, the series loss of the pads is removed by subtracting the open-corrected Z-parameters of the shorted pad structure from the open-corrected Z-parameters of the DUT [Figure 5.4(c)] [72].

Figure 5.5 shows the measured effective inductance and Q factor of seven *symmetric* inductor sites with the pad parasitics deembedded. These seven measurements were averaged and compared to the results of the Sonnet simulations from Chapter 2 (Figure 5.6). The self-resonant frequency (f_{sr}) of the measured inductor is 17.2 GHz, approximately 3 GHz lower than predicted by Sonnet [Figure 5.6(a)]. Therefore, the

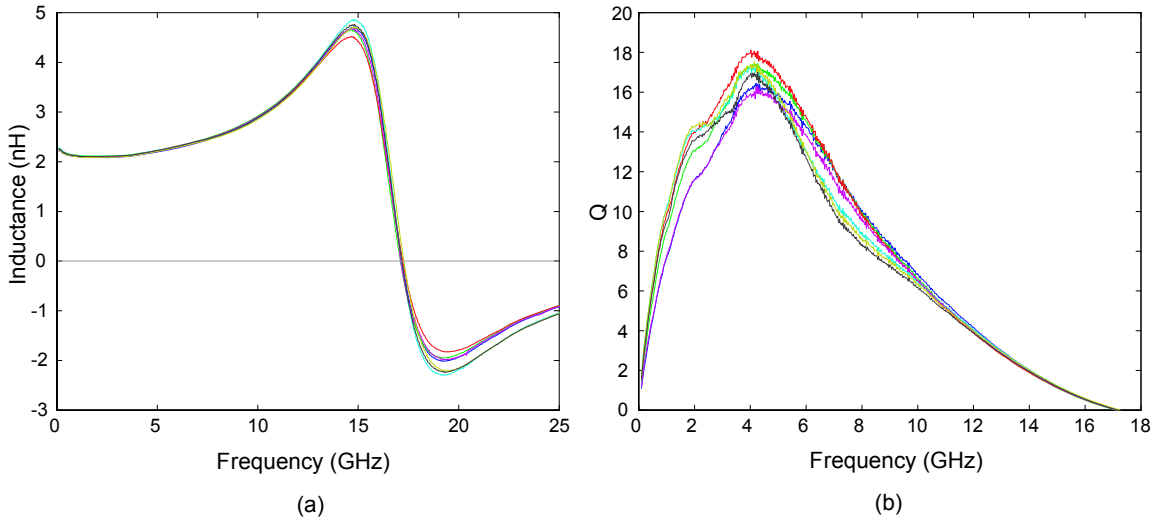

Figure 5.5: Measured (a) effective inductance and (b) Q factor versus frequency for the seven symmetric inductor sites.

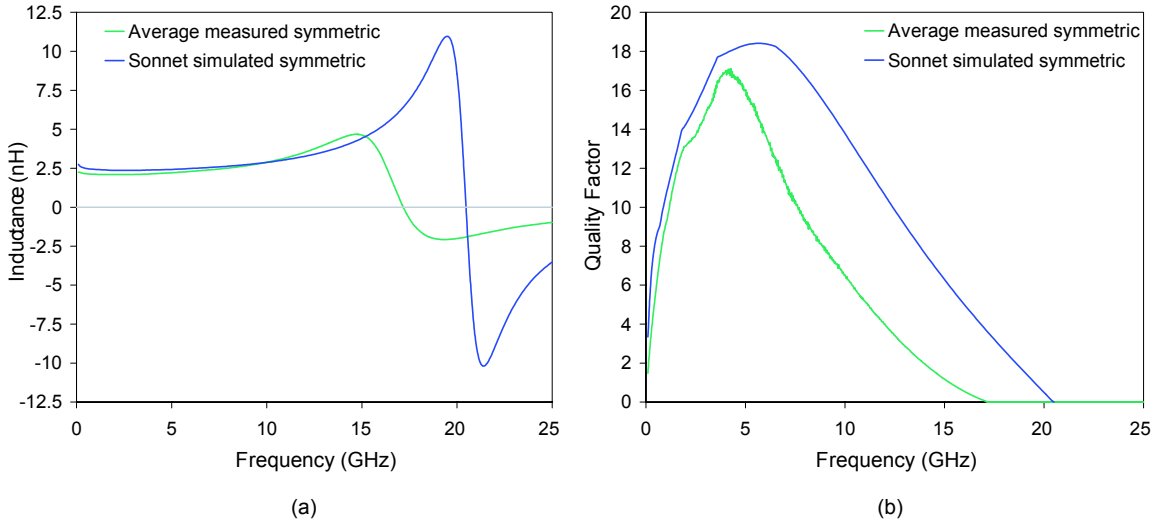

Figure 5.6: Comparison of the average measured and simulated (a) effective inductance and (b) Q factor versus frequency for the symmetric inductor.

fabricated inductor has more parasitic capacitance than what was predicted by the simulation. Although the agreement between the effective inductance values below self-resonance is quite good, it is expected that the higher parasitic capacitance of the integrated inductor will result in a higher overall tank capacitance and a lower VCO output frequency and tuning range. In addition to the lower f_{sr}, another effect of higher measured parasitic capacitance is lower Q factor at high frequencies. The peak Q factor occurs very near the target frequency for the symmetric and dual inductor VCO designs. While the measured Q factor agrees well with simulation up to approximately 4 GHz, it drops off more sharply beyond the peak Q at 4.3 GHz [Figure 5.6(b)]. One source of error is the simulated open and short calibration standards, which most likely underestimate the capacitive loss of the pads at high frequencies. The measured results could, therefore, agree more closely with the simulated results if the deembedded pad data had been obtained from measured structures rather than electromagnetic simulation.

The deembedded effective inductance and Q factor of seven *dual* inductor sites were also measured, averaged, and compared to the respective Sonnet simulated data in Figure 5.7. Figure 5.7(a) shows that the measured and simulated effective inductance differ by approximately 500 pH for frequencies below 10 GHz. This may be due to the mutual inductance of the dual spiral structure being lower for the fabricated inductor than predicted by simulation, thereby lowering the effective inductance of the measured circuit. The measured and simulated Q factor curves follow the same trends as those of the symmetric inductor. Again, beyond the peak at 4.3 GHz, the measured Q factor drops off more sharply than predicted by simulations, although the f_{sr} is approximately the same. However, the correlation between the measured and simulated Q values is excellent at lower frequencies. This is likely a result of deembedding the pads with simulated data.

Figure 5.8 compares the averaged measured results of the dual and symmetric inductors. The effective inductance of the symmetric inductor is approximately 300 pH lower than that of the dual inductor for frequencies below about 10 GHz [Figure 5.8(a)]. The higher inductance of the dual structure will lower the output frequency of the VCO with the dual inductor tank circuit. Most importantly, measured results in Figure 5.8(b) confirm a 48% improvement in Q factor at 5.25 GHz, from 10.4 for the dual inductor to 15.4 for the symmetric inductor. The comparison is not ex-

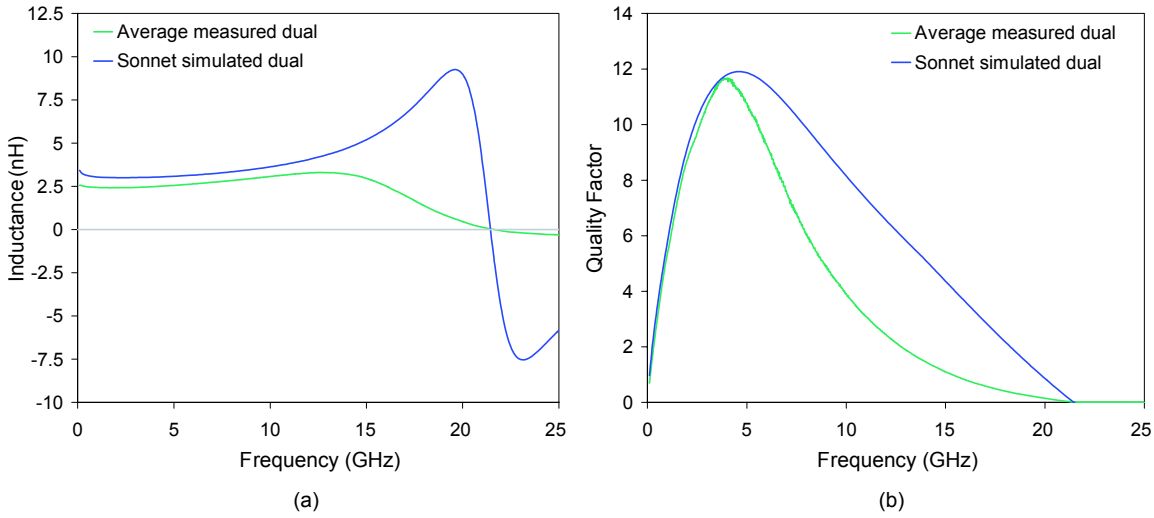

Figure 5.7: Comparison of the average measured and simulated (a) effective inductance and (b) Q factor versus frequency for the dual inductor.

act, however, since the measured effective inductance of the dual inductor is slightly higher than that of the symmetric inductor.

5.3 VCO Measurements

Figure 5.9 shows the test setup for the VCO spectrum and tuning characteristic measurements. The RF^- output port of the VCO is terminated with a 50 Ω load, while the RF^+ output port is connected to the spectrum analyzer with a 50 Ω characteristic input impedance. This single-ended measurement of the VCO spectrum results in an output power that is 3 dB less than would be the case with a differential output. However, phase noise measurements using a single-ended approach yield the same results as those using a balun to take the difference of the VCO outputs prior to the phase noise measurement system. This holds since phase noise is measured as a ratio of noise (at a particular offset) to the signal amplitude (or dBc), both of which suffer the same 3 dB drop due to the single-ended measurements.

A regulated battery supply is used to reduce externally induced phase noise [73]. The supply board has two independently adjustable outputs, one for the output buffers and a second for the tail current and $-G_M$ supply through the tank inductor. The

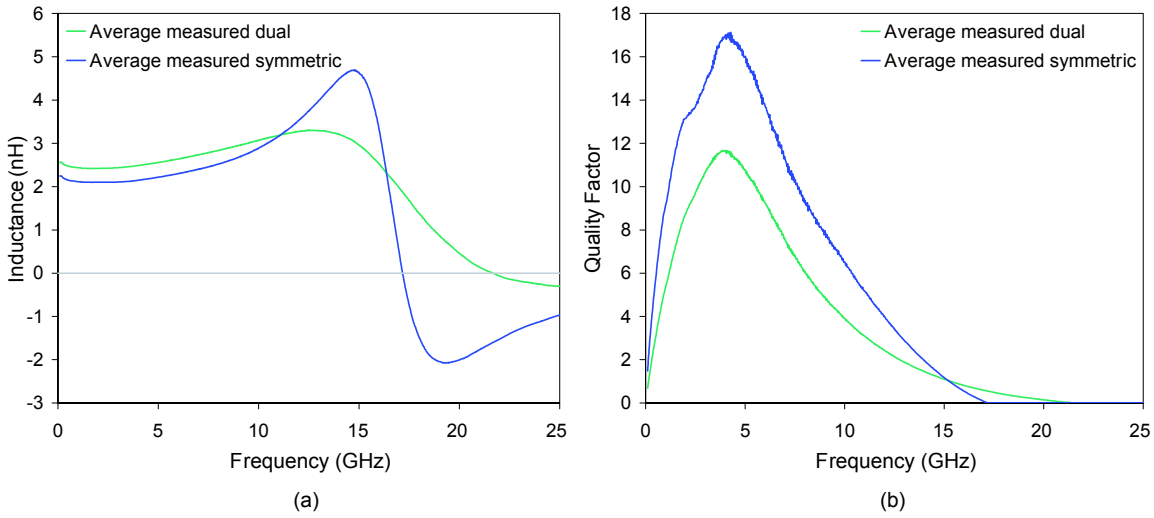

Figure 5.8: Comparison of the (a) effective inductance and (b) Q factor versus frequency for the average measured symmetric and dual inductors.

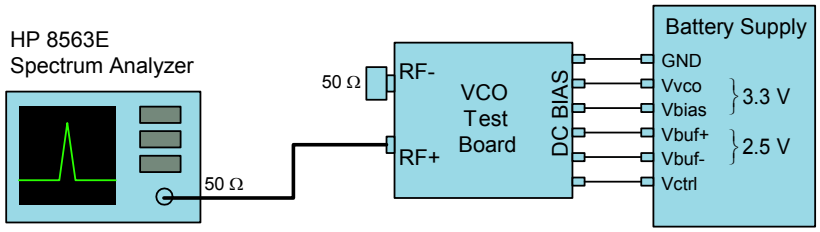

Figure 5.9: Test equipment setup for VCO spectrum and tuning characteristic measurements (after [17]).

best results were obtained by setting the tail and $-G_M$ supply to 3.3 V, rather than the 2.5 V rail used in simulation. In contrast, the complementary structure of the output buffers performed best by using a 2.5 V supply, as used in simulation. All the measured results presented in this section were taken using this biasing scheme.

5.3.1 Symmetric Inductor VCO

Figure 5.10 shows a die photo of the fabricated symmetric inductor VCO. The fabricated symmetric inductor VCO circuit consumes 3.81 mA from a 3.3 V supply for the VCO and 14.1 mA from a 2.5 V supply for the output buffer (47.8 mW total). The buffer current is very high and could be improved with a different design (as discussed

in Section 3.4). Less current is consumed in the buffer than predicted by simulations. However, increasing the supply voltage of the buffers to obtain the same current as in the simulation actually results in a lower output power. This is a consequence of the need to bias the gates of the class-B buffer PMOS and NMOS transistors at half the supply voltage. Increasing the supply changes these gate bias operating points from being at half the supply rail (see the schematic in Figure 3.15).

The measured output spectrum of the symmetric inductor VCO for a tank varactor control voltage of 0 V is shown in Figure 5.11. The output frequency is 5.42 GHz, which is approximately 1 GHz lower than predicted with SpectreRF simulations for the same VCO control voltage (6.31 GHz). However, a lower output frequency was expected, as discussed in Section 5.2, since the parasitic capacitances of the measured inductors are higher than predicted by electromagnetic simulations in Sonnet. Furthermore, as discussed in Chapter 3, SpectreRF simulations were not performed on the extracted layout, which would have included the parasitic capacitances of the interconnects. Using equation 1.15 in conjunction with the simulated and measured inductances of the symmetric inductor (2.4 nH and 2.2 nH, respectively), this change in resonant frequency implies an additional equivalent parasitic capacitance of 127 fF in the fabricated circuit. The differential output power is 1.17 dBm (3 dB higher than the single-ended spectrum measurement shown in Figure 5.11).

The measured frequency tuning characteristic, obtained using the HP 8563E spectrum analyzer, is shown in Figure 5.12. The tuning range of the symmetric inductor VCO is 26% (4.19 to 5.45 GHz), which is 5% lower than predicted by simulations (31%). K_v is calculated from the linear sloped region of Figure 5.12 (which occurs between about 2.7 and 3.1 V). This translates to a very high K_v of 1.08 GHz/V (though slightly lower than the K_v of 1.12 GHz/V predicted by SpectreRF simulations). In contrast, the "DC" C-V curve of the varactors predicts a much higher VCO gain of 1.57 GHz/V (see Figure 3.3). Thus, large-signal smoothing of the C-V curve effectively lowers the VCO gain [61]. The linear region of the measured tuning characteristic occurs at a higher voltage than in simulation because of the higher 3.3 V supply voltage used. As discussed in Chapter 3, such a high K_v makes this VCO undesirable for phase-locked loop applications, since very small changes in the control voltage (e.g., noise) can result in a dramatic change in frequency.

The phase noise was measured for various tank varactor control voltages using an

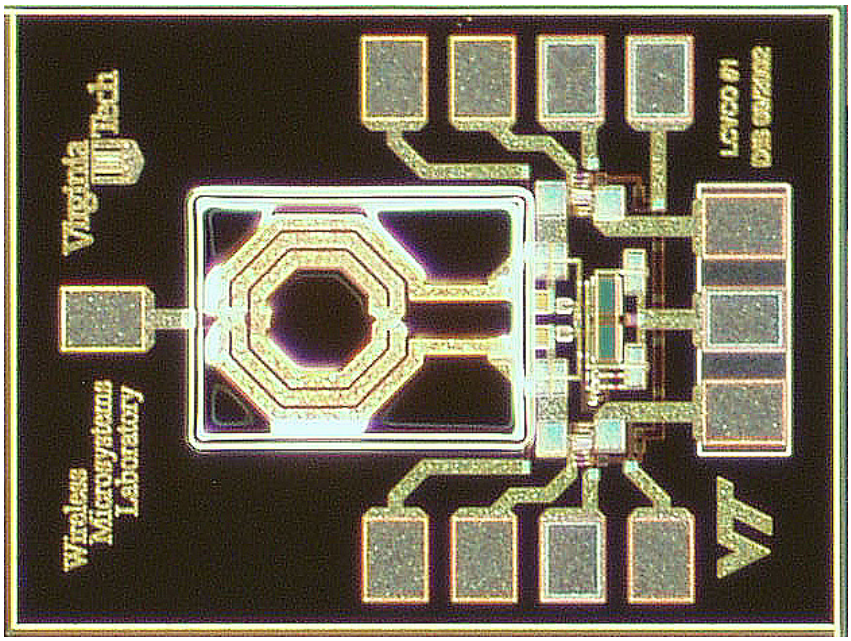

Figure 5.10: Die photo of the fabricated symmetric inductor VCO.

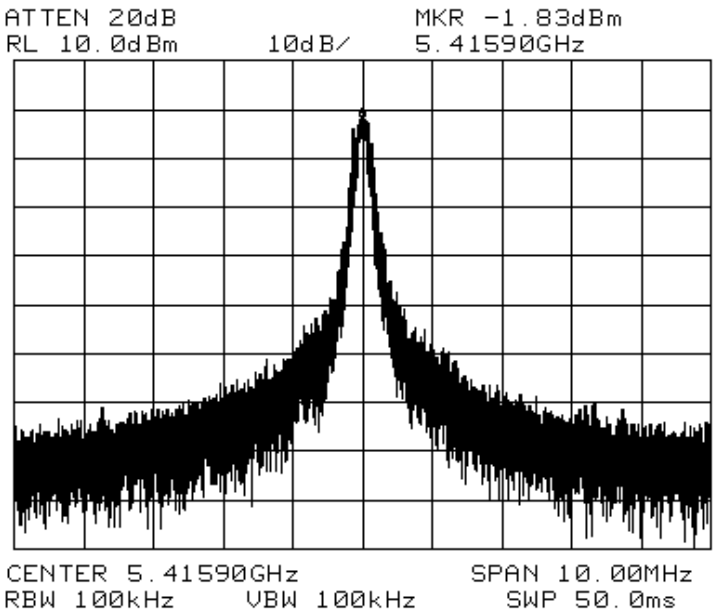

Figure 5.11: Measured single-ended output spectrum of the symmetric inductor VCO. The differential output power is 3 dB higher (1.17 dBm).

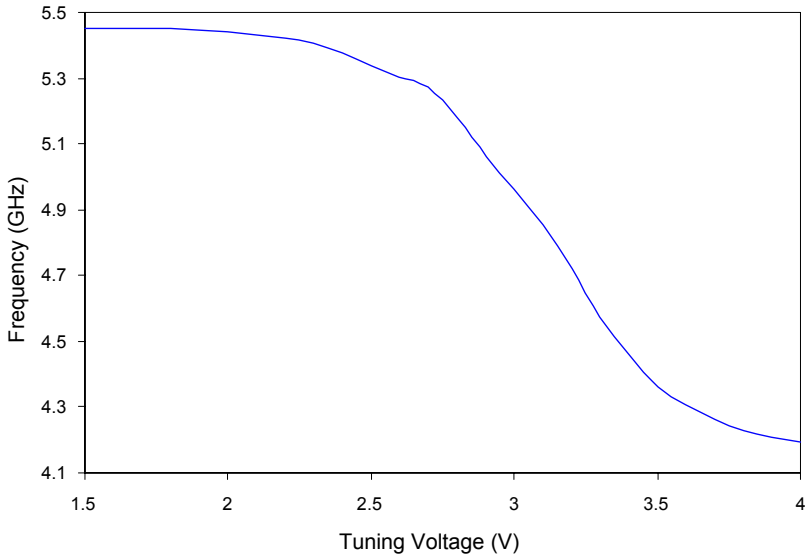

Figure 5.12: Measured frequency tuning characteristic of the symmetric inductor VCO.

Agilent E5500 phase noise measurement system. This phase noise system uses the delay line method to downconvert the signal to baseband and measure the sideband noise of the VCO [74]. Figure 5.13 shows the measured phase-noise spectrum of the symmetric inductor VCO for a tank varactor control voltage of 0 V. At a 1 MHz offset the measured phase noise is -112 dBc/Hz. This exceeds the -107 dBc/Hz at a 1 MHz offset specification for the IEEE 802.11a standard [20]. There appears to be a spur in all the phase noise measurements of the symmetric inductor VCO at about a 30 kHz offset, possibly from the measurement system or from an external interferer coupling into the VCO. It is not believed that this bend in the phase noise is inherent to the oscillator. Nevertheless, the results at a 1 MHz offset are not affected by this apparent spur, and are, therefore, believed to be accurate.

However, the phase noise varies with different varactor control voltages. The minimum phase noise of the symmetric inductor VCO (-115.5 dBc/Hz at a 1 MHz offset) occurs for a control voltage of 1.0 V (Figure 5.14). Figure 5.15 shows a plot of the measured phase noise at a 1 MHz offset for varactor control voltages from 0 to 3 V. In general, the phase noise increases when the tuning characteristic of the tank varactor is the sharpest. At this point the VCO has the highest tuning gain and is, therefore, more susceptible to noise in the control voltage.

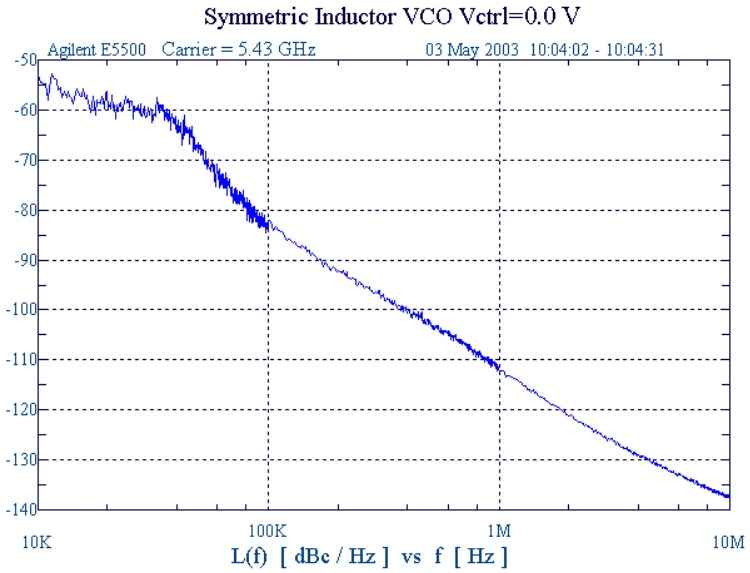

Figure 5.13: Measured phase noise spectrum of the symmetric inductor VCO with a tank control voltage of 0 V.

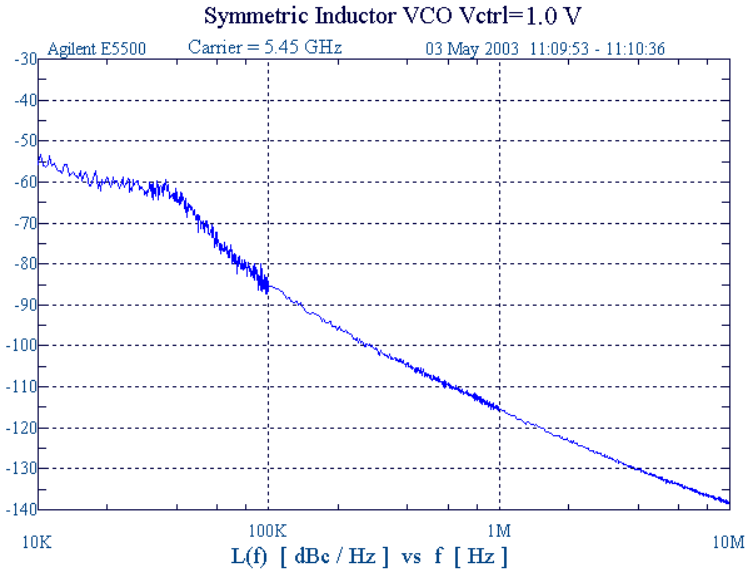

Figure 5.14: The best measured phase noise spectrum of the symmetric inductor VCO. The tank varactor control voltage is 1.0 V.

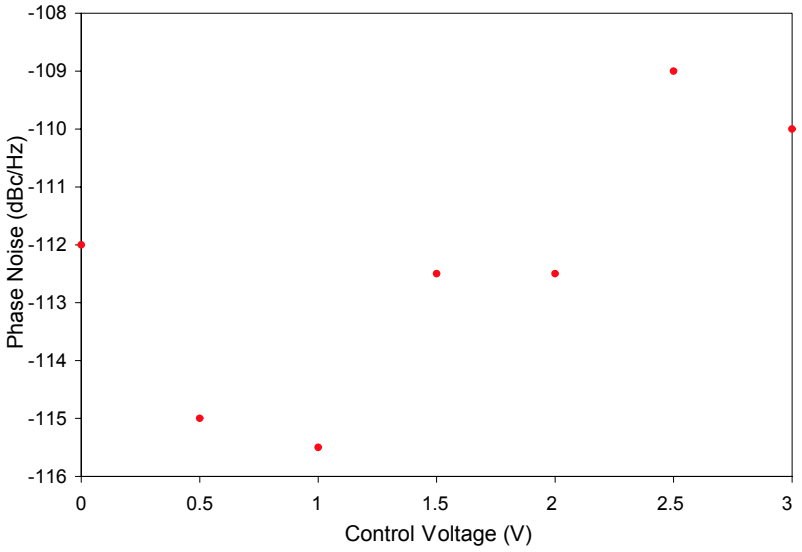

Figure 5.15: Measured phase noise at a 1 MHz offset versus control voltage for the symmetric inductor VCO.

5.3.2 Dual Inductor VCO

Figure 5.16 shows a die photo of the fabricated dual inductor VCO. The DC current consumption of the dual inductor VCO is 3.75 mA from a 3.3 V supply for the VCO and 13.3 mA from a 2.5 V supply for the buffer (45.6 mW total). Slightly increasing the supply voltage to match the currents in the symmetric inductor VCO resulted in an insignificant difference in the measured RF performance. Interestingly, the largest difference in the current consumption compared to the symmetric inductor VCO is in the output buffer; however, increasing this current to match that of the symmetric inductor VCO did not increase the output power. It should be noted that process variations are the likely cause for this VCO consuming less power than the symmetric inductor VCO; in a nominal circuit, the lower Q dual inductor in the tank circuit should result in *higher* power consumption.

As with the symmetric inductor VCO, the frequency tuning characteristic of the dual inductor VCO is shifted down (Figure 5.17). The output frequency of the fabricated dual inductor VCO ranges from 3.50 to 4.58 GHz, versus 4.6 to 5.96 GHz simulated. Using equation 1.15 in conjunction with the simulated and measured inductances of the dual inductor (3.1 nH and 2.6 nH, respectively), this change in

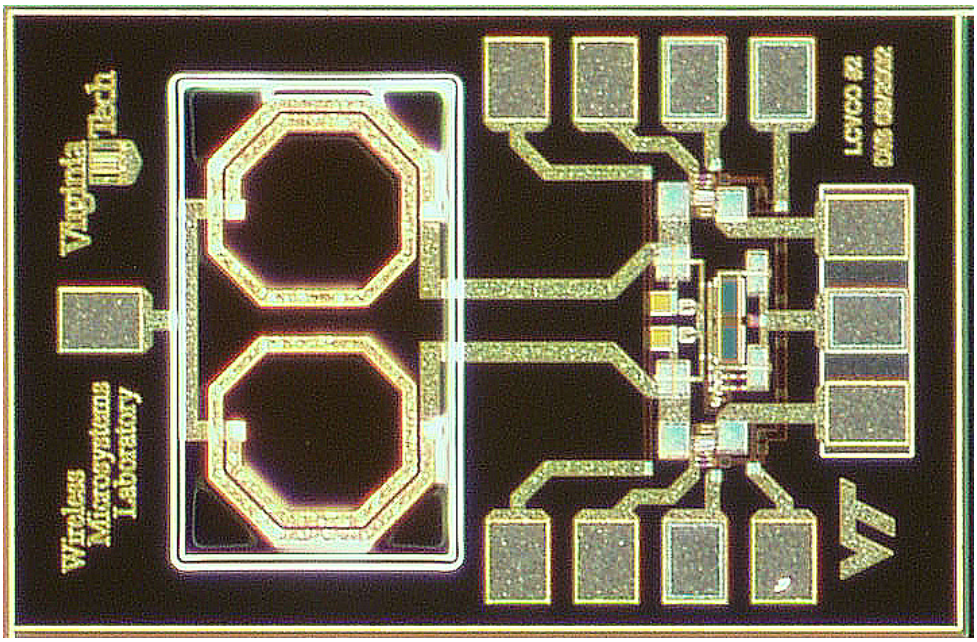

Figure 5.16: Die photo of the fabricated dual inductor VCO.

resonant frequency implies an additional equivalent parasitic capacitance of 234 fF in the fabricated circuit. As discussed previously, some additional capacitance was expected, since parasitic extraction was not performed on the layout during the design phase.

This VCO has a measured K_v of 1.09 GHz/V and a tuning range of 27%, in comparison to a K_v of 1.33 GHz/V and tuning range of 38% obtained from SpectreRF simulations. A larger difference between the measured and simulated K_v and tuning range for the dual inductor VCO than for the symmetric inductor VCO is a result of nearly twice the equivalent parasitic capacitance in the fabricated circuit (234 fF for the dual inductor VCO compared to 127 fF for the symmetric inductor VCO). The differential output power of the dual inductor is 1.0 dBm, in comparison to 1.17 dBm for the symmetric inductor VCO.

Figure 5.18 shows the measured phase noise of the dual inductor VCO for a tank varactor control voltage of 0 V. At a 1 MHz offset, the measured phase noise is -104 dBc/Hz. Due to limited time access to the E5500 system, extensive phase noise measurements versus control voltage were not taken for the dual inductor VCO. However, comparing the phase noise measurements at a control voltage of 0 V, it can

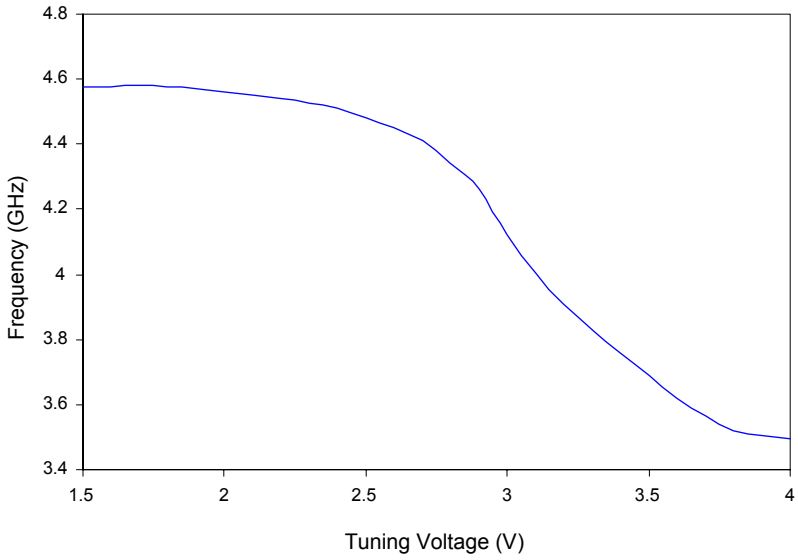

Figure 5.17: Measured frequency tuning characteristic of the dual inductor VCO.

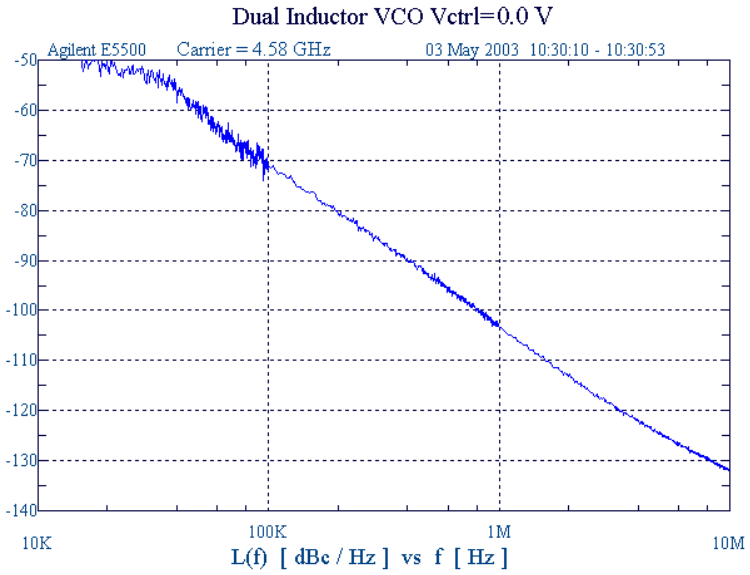

Figure 5.18: Measured phase noise spectrum of the dual inductor VCO with a control voltage of 0 V.

VCO	P_{OUT} (dBm)	I_{DC} (mA)	Phase Noise at 1 MHz (dBc/Hz)	Range (GHz)
Symmetric	1.17	3.81	-115.5	$4.19 - 5.45$
Dual	1.00	3.75	-104	$3.50 - 4.58$

Table 5.1: Measured characteristics of the symmetric and dual VCOs. The DC currents are for a supply of 3.3 V. The phase noise results are shown for tank varactor control voltages of 1.0 V for the symmetric inductor VCO and 0.0 V for the dual inductor VCO. The frequency tuning ranges are for tank varactor control voltages from 1.5 to 4.0 V.

be seen that the dual inductor VCO has 8 dBc/Hz higher phase noise at a 1 MHz offset then the symmetric inductor VCO (-112 dBc/Hz versus -104 dBc/Hz). The dual inductor VCO could potentially have a lower phase noise at higher control voltages (as much as 3 dB lower), since the minimum phase noise of the symmetric inductor VCO was measured at a control voltage of 1.0 V. Contrary to the SpectreRF PSS simulations (Section 3.3), the measured phase noise results clearly show the benefit of the higher Q tank circuit inductor in the symmetric inductor VCO. The measured results of both the symmetric and dual inductor VCOs are summarized in Table 5.1.

5.4 Tunable Polyphase Measurements

The objective of the fabricated stand-alone tunable polyphase filter is a proof-of-concept for the idea of using series output varactors to adjust the I/Q phase balance of the polyphase outputs. In Chapter 4, the I/Q phase balance was specified by taking the phase difference between neighboring curves in Figure 4.7. This results in four phase balance terms, as illustrated in Figure 5.19(a). The tunable output polyphase was introduced in Chapter 4 under the assumption that there was no *differential* phase imbalance — in other words $(I^-)-(Q^+) = (I^+)-(Q^-)$ and $(Q^-)-(I^-) = (Q^+)-(I^+)$. Since this is a valid assumption for the unbuffered tunable polyphase, Section 4.3.1 refers to the I/Q phase errors as simply I and Q. However, it was shown later in Chapter 4, that the input buffers introduce some differential phase imbalance to the polyphase [Figure 5.19(b)]. Therefore, differential phase imbalance also exists in the fabricated buffered polyphase. In this section, the four I/Q phase balance terms will be expressed as $(I^-) - (Q^+)$, $(I^+) - (Q^-)$, $(Q^-) - (I^-)$, and $(Q^+) - (I^+)$.

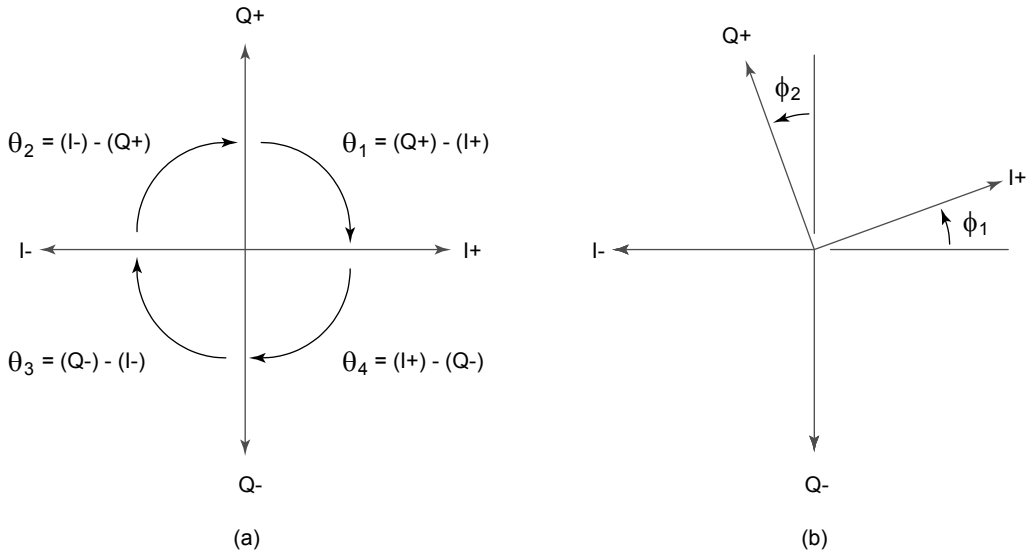

Figure 5.19: Definition of (a) the four I/Q phase error angles and (b) the two differential phase error angles.

During the design phase, the intended test setup for the polyphase incorporated a balun between port 1 of the vector network analyzer (VNA) and the differential input of the polyphase (Figure 5.20). Each of the outputs of the polyphase filter is then sequentially connected to port 2 of the VNA, while the other three outputs are terminated with DC blocks and 50 Ω loads. Thus, four separate S_{21} measurements are required with this test setup to find the relative phase versus frequency at each of the four polyphase outputs.

Unfortunately, the Anaren 30057 4-8 GHz balun used in this setup has an approximate 4° *differential* phase error over the 4.5 to 6.5 GHz bandwidth. This phase error combines with the differential phase error in the input buffers to skew the relative phase of the polyphase outputs. Without calibration, the effect of the differential phase error from the input buffers of the polyphase and that of the balun itself are indistinguishable.

The effect of the differential error at the input of the polyphase network on the output phase is significant. Simulations of an ideal three-pole unbuffered polyphase filter with a 0°-176° differential input signal (i.e., −4° differential phase error) result in the output phase imbalance shown in Figure 5.21. While a perfectly balanced differential input signal yields exact 0° I/Q phase error, the I/Q imbalance for a differential

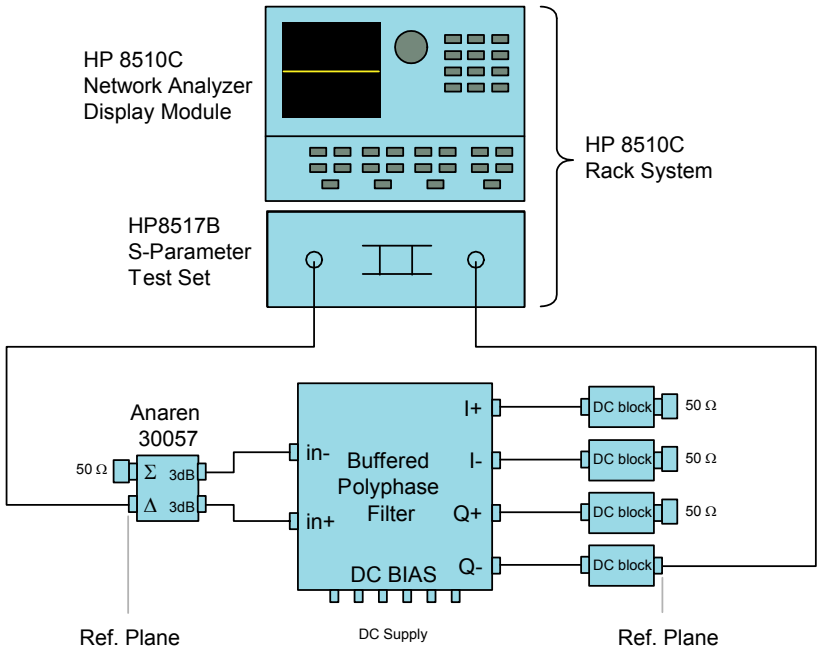

Figure 5.20: Initial test setup of the stand alone polyphase using a balun at the input of the polyphase.

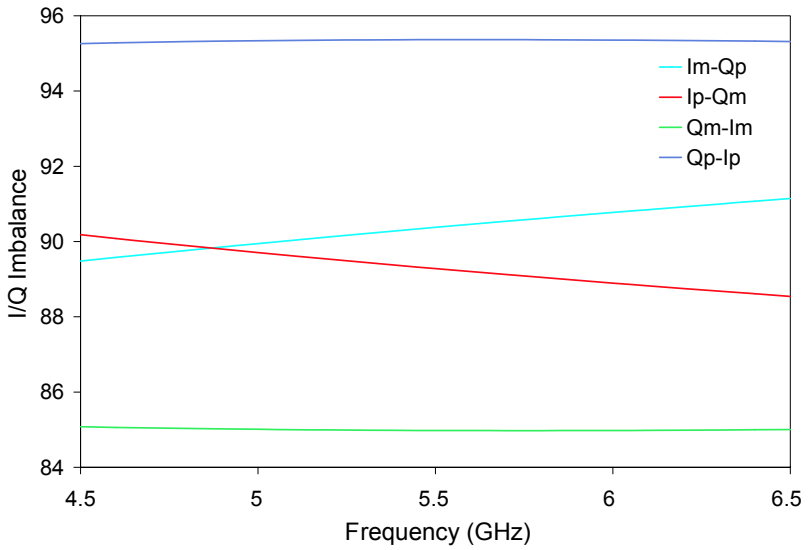

Figure 5.21: Simulated I/Q phase imbalance of an ideal polyphase filter driven with a 0°-176° differential signal (i.e., -4° differential phase error).

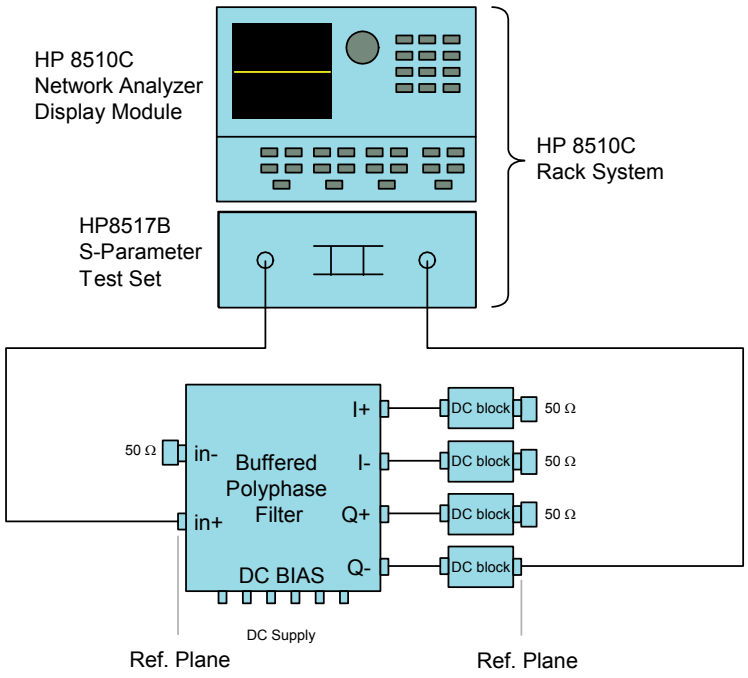

Figure 5.22: "Single-ended" test setup for measurements of the standalone polyphase filter circuit.

input phase error of 4° across the band from 4.5 to 6.5 GHz is approximately ±5°. Accurately deembedding input phase error from the measurements can be done with the measured S-parameter networks of the balun and polyphase filter. However, since the differential input polyphase filter is actually a six-port S-parameter network, deembedding the phase error from the test setup is far from trivial.

To avoid the problem with deembedding the phase error of the input balun, an alternate test setup was used (shown in Figure 5.22). This test setup allows the polyphase outputs to be effectively analyzed with a perfectly differential input signal. First, four "single-ended" measurements are made with port 1 of the VNA connected to the *positive* input of the polyphase and port 2 of the VNA connected to each one of the four outputs sequentially. The negative input and the outputs of the polyphase filter which are not connected to the VNA, are terminated with 50 Ω loads in order to present the same terminations as the ports of the VNA. These four measurements are repeated with port 1 of the VNA connected to the *negative* input of the polyphase filter, and the positive input terminated in 50 Ω. Using superposition, the effect of a perfectly differential signal is *mathematically* synthesized at the input of

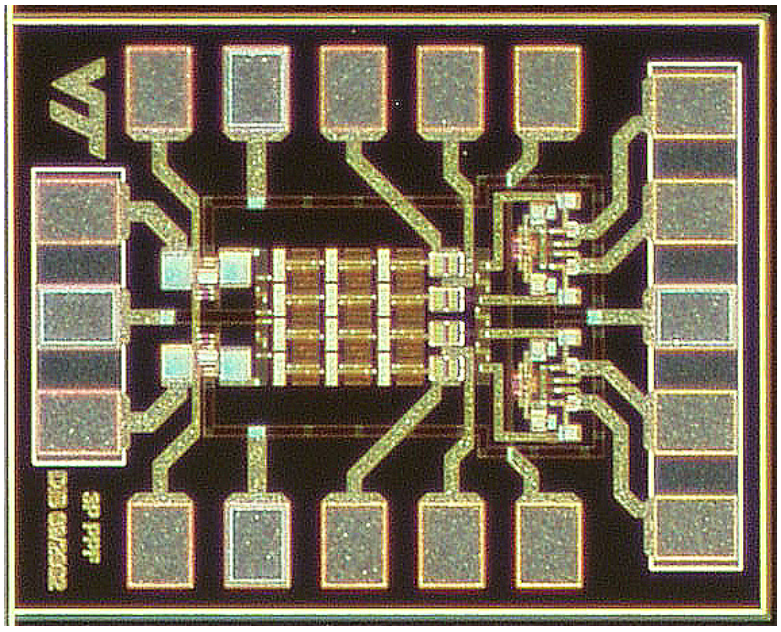

Figure 5.23: Die photo of the fabricated standalone polyphase.

the polyphase by subtracting the phasor S_{21} measurements with port 1 of the VNA connected to the negative input from the S_{21} measurements with port 1 of the VNA connected to the positive input. The relative phases are obtained from the combined S_{21} from these eight total measurements.

Figure 5.23 shows a die photo of the fabricated stand-alone polyphase. From a 2.5 V supply, the polyphase input buffer consumes 13.74 mA (same as for the VCO output buffers) and the output buffers consume 6.0 mA. The output buffers were designed for a 1 kΩ termination, so the 50 Ω test equipment prevents the actual output power of the polyphase from being measured correctly. However, the buffers prevent the test equipment from loading down the polyphase itself, so the output phase tunability can be accurately measured.

Measurements were taken for varactor control voltages ranging from 0 to 2.5 V. The phase tunability is obtained by fixing two of the polyphase output varactor control voltages (I or Q channel) while sweeping the other output varactor control voltages (Q or I channel). For example, several measurements were taken by fixing the V_{tune0} and $V_{tune180}$ at 0 V and sweeping the V_{tune90} and $V_{tune270}$ from 0 V to 2.5 V. The results from one point in this sweep ($V_{tune0} = V_{tune180} = 0$ V and $V_{tune90} = V_{tune270} = 2.5$ V)

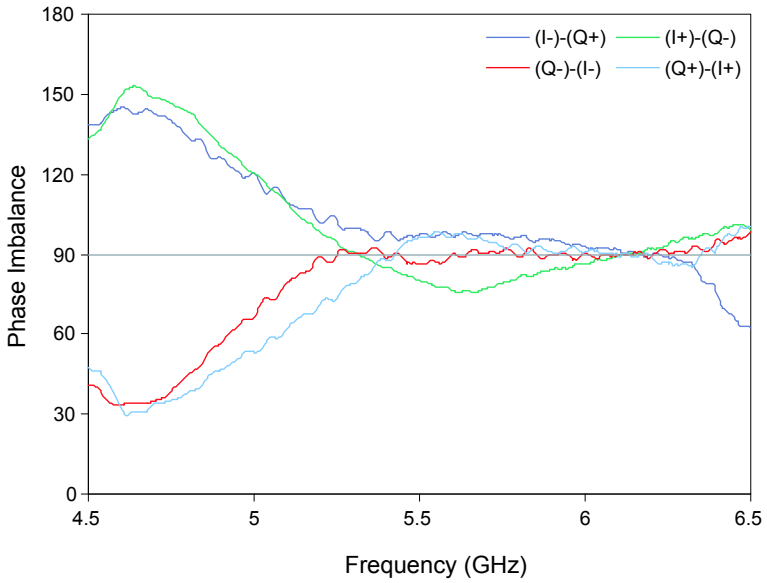

Figure 5.24: Measured I/Q imbalance of the tunable polyphase for the case $V_{tune0} = V_{tune180} = 0$ V and $V_{tune90} = V_{tune270} = 2.5$ V.

are plotted in Figure 5.24 versus frequency. Recall that the polyphase was originally designed to have poles at 5.15 GHz, 5.477 GHz, and 5.825 GHz. In the measurements of this sample, it appears that the poles have been somewhat shifted up in frequency, since the polyphase has a phase flatness from approximately 5.4 to 6.4 GHz, rather than from 5.15 to 5.825 GHz. The upward shift in the poles could come as a result of increased parasitic capacitance in the series combination of the output varactors and the DC blocking capacitors at the input of the buffers. Decreased capacitance due to series parasitics at the outputs could shift the pole frequencies upward. Process variation in the capacitor dimensions could also be the cause for the shift in the phase flatness bandwidth.

This sample of the stand-alone polyphase has an optimal measured $\pm 5^\circ$ phase flatness bandwidth of 315 MHz, centered at 6.14 GHz (Figure 5.24). In simulation, the $\pm 5^\circ$ phase flatness bandwidth is well over 2 GHz [Figure 4.10(b)]. However, a smaller measured bandwidth is expected since parasitic resistances and capacitances of the layout are not included in simulation. As previously shown in Figure 5.21, another source of the limited bandwidth of the polyphase is differential imbalance in the input buffers. It is likely that component mismatch in the input buffer introduces

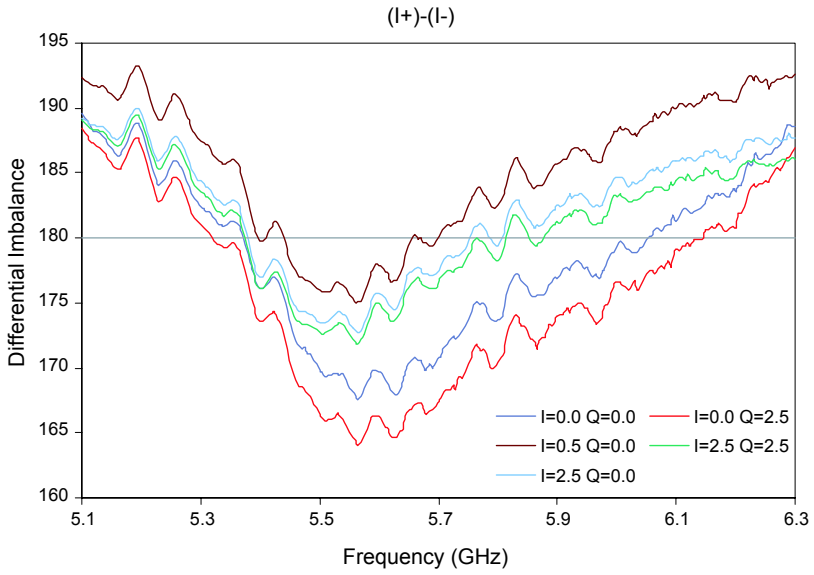

Figure 5.25: Measured differential phase error between the I^+ and I^- outputs of the tunable polyphase.

differential error at the input of the polyphase, since the CMOS class-B buffer design is not truly differential.

For the phase balance terms involving I^+, there is a severe "kink" in the tuning curves at approximately 5.65 GHz. The cause for this is seen by examining the *differential* error in the I channel (Figure 5.25). At 5.65 GHz the difference between the differential I^+ and I^- outputs has a similar kink. There are several potential causes for this differential imbalance. First, the input buffers may be introducing differential phase imbalance at the input of the polyphase that varies versus frequency. The class-B CMOS buffer used at the polyphase input is not truly differential, so it is more susceptible to component mismatch. However, one would not expect that differential error at the input of the buffer alone would introduce a kink in the phase in the I^+ channel and not in any of the other channels. Second, there could be a component mismatch or layout error within the polyphase filter itself that is only affecting the poles of the I^+ channel. Third, there could be a problem with the I^+ output bond wire, or other connections between the package and the network analyzer, that is responsible for the kink in the phase around 5.65 GHz.

The tunability of the polyphase can be plotted at a fixed frequency versus the swept

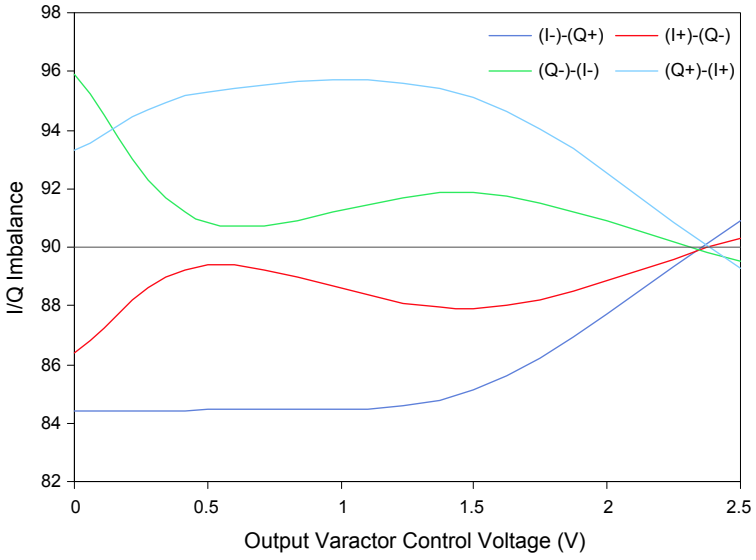

Figure 5.26: Measured I/Q imbalance at 6.14 GHz versus the output varactor control voltage of V_{tune90} and $V_{tune270}$. The V_{tune0} and $V_{tune180}$ output varactor control voltages are fixed at 0 V.

output varactor control voltage. In Figure 5.24 it can be seen that the I/Q imbalances all converge to 90° at approximately 6.14 GHz. I/Q imbalance data points at 6.14 GHz for a sweep of V_{tune90} and $V_{tune270}$ from 0 V to 2.5 V are plotted in Figure 5.26. At about 2.3 V, approximately 0° measured I/Q phase error for all four imbalance terms is achieved. This plot also shows that the I/Q phase tunability is related to the DC/small-signal C-V curve of the varactors.

A second sample of the stand-alone polyphase circuit was measured in order to investigate the cause for the kink in the I/Q phase angles and the frequency shift of the poles observed in the first sample. The four measured I/Q phase imbalance angles of the second sample are plotted at five distinct output varactor control voltage settings and are overlaid in Figure 5.27. This figure shows the tunability of the phase flatness bandwidth of the polyphase filter.

The kink at 5.65 GHz in the I/Q balance terms involving the I^+ output of the first sample does *not* occur within the bandwidth from 5.2 to 5.8 GHz for the second sample. In general, the curves for this sample are much flatter within the bandwidth specified by the design than the curves in Figure 5.24. The phase imbalance can be tuned across approximately 15° for varactor control voltage settings from 0 to

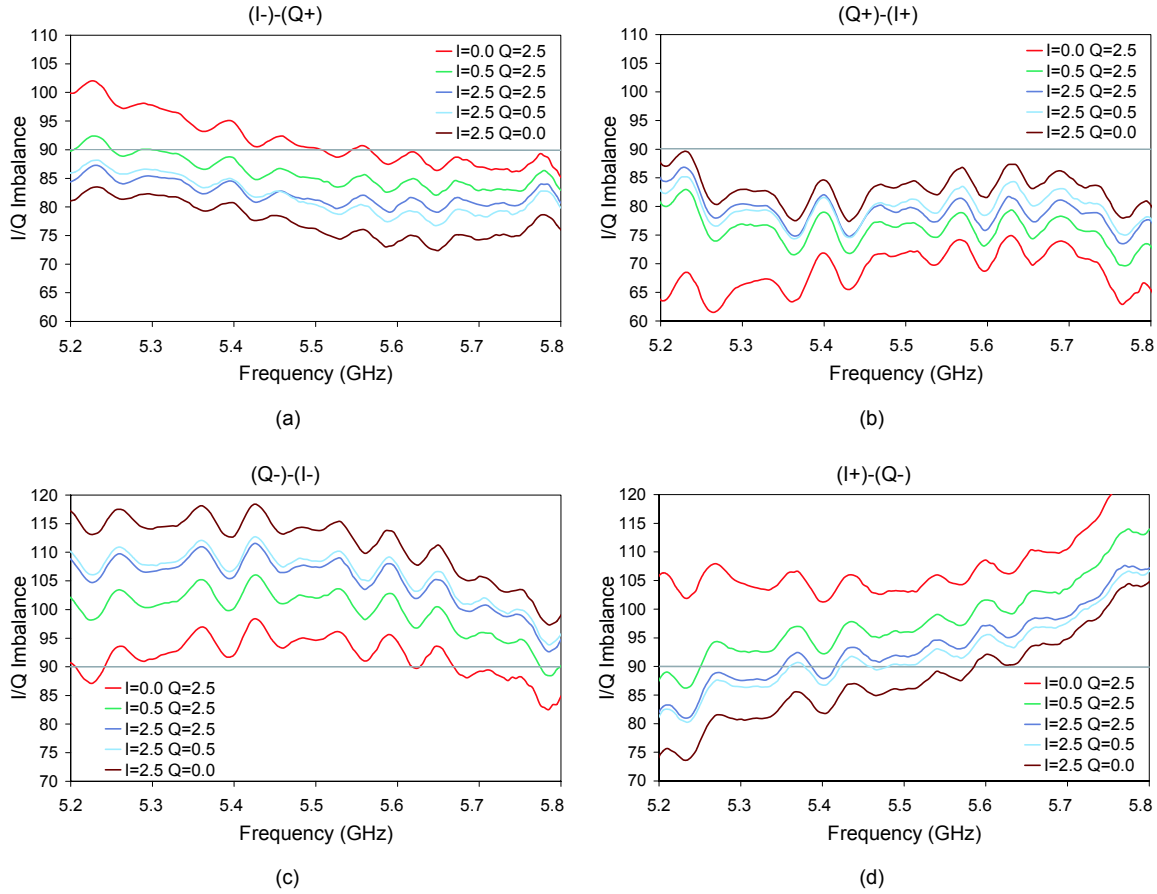

Figure 5.27: Measured I/Q imbalance of the four output signals versus frequency and various output varactor control voltages of a second polyphase circuit sample. The four I/Q phase imbalance terms are plotted separately: (a) $(I^-) - (Q^+)$; (b) $(Q^+) - (I^+)$; (c) $(Q^-) - (I^-)$; and $(I^+) - (Q^-)$.

2.5 V. Interestingly, the phase tunability in the fabricated circuit is nearly double that predicted in simulation (15° measured versus 8° simulated). The cause for this difference in measured and simulated data is still under investigation.

The upward frequency shift of the poles seen in Figure 5.24 is not present for this sample. This implies that the shift of the poles in the first polyphase sample is likely a result of a packaging error or smaller capacitor dimensions due to process variations, rather than series parasitic capacitance, which would affect all the samples in approximately the same way. However, a large ($\sim$20°), but relatively constant, differential error severely limits the $\pm$5° phase flatness bandwidth of this sample. To overcome this error, the four output varactor control voltages would need to be set to four unique voltages. Due to the number of measurements and post-processing mathematics required to determine I/Q phase balance, it would be very difficult to optimize voltages with the current test setup. However, because of the flatness of the curves, this sample offers the potential of having a $\pm$5° phase flatness bandwidth of approximately 700 MHz, covering all three of the U-NII bands (5.15 to 5.825 GHz) if the correct tuning voltages were found.

Extending the frequency range of Figure 5.27, a dramatic kink in the phase error angles is observed at approximately 5.9 GHz, similar to the kink in band in the first sample. Figure 5.28 shows this kink for the $(I^+) - (Q^-)$ phase error angle. A similar kink occurs in all the other I/Q phase error angles at 5.9 GHz, as opposed to just those involving the I^+ output as in the first sample. Therefore, the source of the kink in both samples is not likely to be an error in the design of the polyphase filter. Process and/or packaging variations appear to have a large effect on what frequency and range of phase error angles a kink may occur. Since the phase error introduced by the buffers at the input of the polyphase cannot be measured independently, the effect of phase imbalance in the buffers and shifted poles on the observed kink cannot be specifically validated.

5.5 Summary

This chapter has presented measured data for the fabricated stand-alone inductor test sites, symmetric inductor VCO, dual inductor VCO, and stand-alone tunable

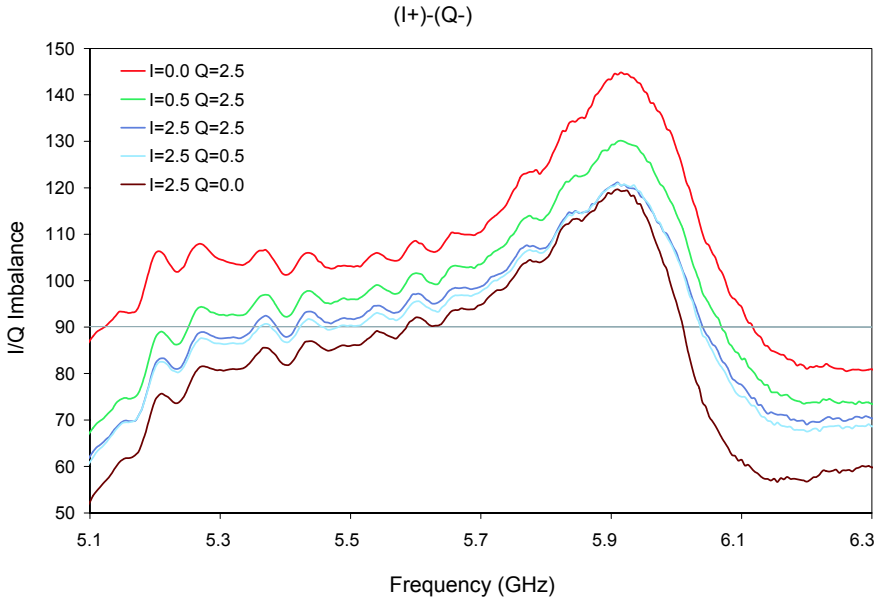

Figure 5.28: Measured $(\mathrm{I}^+)-(\mathrm{Q}^-)$ imbalance over an extended frequency range to 6.3 GHz.

polyphase circuit. The symmetric inductor VCO core consumes 12.6 mW from a 3.3 V supply. Including buffers with a 2.5 V supply, the symmetric inductor VCO consumes 47.8 mW, tunes from 4.19 to 5.45 GHz (K_v = 1.08 GHz/V in the linear tuning region), and provides an output power of 1.17 dBm. From a 3.3 V supply, the dual inductor VCO core consumes a comparable 12.4 mW. The buffered dual inductor VCO consumes 45.6 mW, tunes from 3.50 to 4.58 GHz (K_v = 1.09 GHz/V in the linear tuning region), and provides an output power of 1 dBm. For a tank varactor control voltage of 1.0 V, the symmetric inductor VCO has a measured phase noise of −115.5 dBc/Hz at a 1 MHz offset from the carrier. The dual inductor VCO has a phase noise of −104 dBc/Hz at a 1 MHz offset for a control voltage of 0.0 V.

The tunable polyphase consumes 13.74 mA in the input buffer and 6.29 mA in the two output buffers from a 2.5 V supply (50.1 mW) and offers the potential for a ±5° phase flatness bandwidth of approximately 700 MHz centered at 5.5 GHz, if the correct output phase control voltages were obtained. Tunable output varactor control voltages allow the fabricated circuit to tune through approximately 15° of I/Q phase imbalance.

The combined symmetric inductor VCO with tunable polyphase outputs was dam-

aged by the vendor in the packaging process and has not yet been tested. Efforts are underway to recover samples of this circuit from unsawed wafer sections. However, the independently verified functionality of the VCO and tunable polyphase circuits shows that the combined circuit would indeed result in a VCO with tunable polyphase outputs. Incorporating tunable I/Q phase balance, therefore, requires only an additional 6 mA (for the polyphase output buffers) over what is required for the buffered symmetric inductor VCO itself.

Chapter 6

Conclusions and Future Work

The primary objective of this work was to demonstrate the concept of a quadrature LO source with analog tunable I/Q balance, which could potentially be used to improve the bit-error-rate (BER) of an I/Q receiver or to improve the image rejection ratio (IRR) of a Weaver receiver architecture. The independent demonstrations of the symmetric inductor VCO and tunable polyphase presented in this thesis have verified the concept of a quadrature LO source with tunable I/Q phase balance. This analog method to correct I/Q phase imbalance is the major contribution of this work, and may have potential advantages in power consumption and speed compared to DSP based solutions. In the course of this research, knowledge was gained in the design, modeling, and characterization of differential monolithic inductors, VCOs, and polyphase circuits.

6.1 Conclusions

The I/Q balance tunability of a stand-alone polyphase filter was characterized in terms of phase flatness bandwidth, phase tuning range, and power consumption. First, the stand-alone polyphase offers the potential for a $\pm 5^{\circ}$ measured phase flatness bandwidth of 700 MHz versus a simulated bandwidth of over 2 GHz. The smaller measured phase flatness bandwidth realized in practice is mainly a result of the parasitic resistances and capacitances of the layout. These parasitics could not be reliably extracted, so they were not accounted for in the design phase of this work.

Another source of the limited bandwidth of the polyphase is differential imbalance in the input buffers, since the buffer design used was not truly differential. Any imbalance at the input of the polyphase network reduces the phase flatness bandwidth substantially. Also, the bandwidth of the fabricated polyphase is shifted upward in frequency from the simulated design. Process variation resulting in smaller pole capacitance or packaging variations in the stand-alone polyphase is the likely cause for an upward frequency shift of the poles in the fabricated circuit, since the shift was not consistently observed in every sample. Second, the measured phase tuning range of the polyphase is approximately 15°, though only 8° was predicted in simulation. Though this phase tunability would be sufficient to attain ±5° phase flatness across the 5.15 to 5.825 GHz bandwidth of the polyphase filter, the post-processing mathematics required to determine the I/Q phase balance make it very difficult to determine the appropriate output varactor control voltages. Finally, the phase tunability comes at the expense of only approximately 6 mA additional current consumption (due to the polyphase output buffers) over that consumed in the buffered VCO alone. The combined VCO and polyphase current consumption is potentially much less than what would be needed for I/Q phase correction using DSP-based techniques and possibly avoids latency issues.

Based on the measured results of the phase flatness bandwidth, phase tuning range, and power consumption for the fabricated circuit, the ability to tune I/Q balance at RF is quite feasible, particularly if corrections are made to improve the design of the polyphase network developed in this work. Efforts to improve differential phase balance in the input buffers would increase the phase flatness bandwidth and allow the tunable polyphase to correct for *or* introduce a greater range of I/Q phase imbalance. Moreover, the overall current consumption could be decreased by improving the output buffer of the VCO (input buffer of the polyphase).

Two differential inductors were designed and characterized in this work. The first is an electrically symmetric inductor and the second is the classical dual inductor structure. The inductors were measured with an on-wafer probe station to obtain the differential effective inductance and Q factor. At 5.25 GHz, the symmetric inductor has an effective inductance of 2.2 nH and Q factor of 15.4, whereas the dual inductor has an effective inductance of 2.6 nH and a Q factor of 10.4. Thus, the electrically symmetric inductor offers an approximate 48% improvement in Q factor over the dual

inductor structure at this frequency.

Several of the design goals for the symmetric inductor VCO obtained in simulation were met in practice. The phase noise for all varactor control voltages exceeds the phase noise specification for IEEE 802.11a of −107 dBc/Hz at a 1 MHz offset from the carrier. The best case phase noise measurement (−115.5 dBc/Hz at a 1 MHz offset) occurs for a tank varactor control voltage of 1.0 V. In addition, the 4.19 to 5.45 GHz tuning range covers the lower U-NII bands from 5.15 to 5.35 GHz, making the symmetric inductor VCO limitedly useful for direct conversion or low-IF receiver applications in this frequency regime. This VCO is not desirable for PLL applications due to a high K_v; however, the intended application of this VCO is to drive the tunable polyphase filter, which does not require low K_v. Another limitation of this VCO is that it does not cover the upper 100 MHz band from 5.725 to 5.825 GHz; however, this can be corrected by a revision which compensates for parasitics. The measured output power of the symmetric inductor VCO 1.17 dBm.

In comparison, the measured phase noise of the dual inductor VCO is −104 dBc/Hz at a 1 MHz offset (at a varactor control voltage of 0.0 V) — approximately 8 dBc/Hz worse than that of the symmetric inductor VCO at the same varactor control voltage (−112 dBc/Hz). A 48% lower measured Q factor for the tank inductor in this VCO compared to the symmetric inductor leads to the lower phase noise measurement. In addition, the highest output frequency of the dual inductor VCO is 650 MHz below the lower limit of the U-NII band (5.15 GHz). This makes the dual inductor VCO (as realized) unusable for direct conversion and low-IF receivers in the U-NII bands, though it provided a very useful comparison with the symmetric inductor VCO.

A widely accepted figure-of-merit (FOM) for VCOs is given by [75]:

$$FOM = L\left(\Delta\omega\right) - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log\left(\frac{P_{diss}}{1\text{ mW}}\right) \tag{6.1}$$

This FOM normalizes the phase noise at a given offset, the center frequency, and the power consumption in milliwatts. The FOM of the symmetric inductor VCO is −179.2 dBc/Hz, which compares well with the best reported VCO FOM in the 5 GHz frequency regime of −183.6 dBc/Hz [76]. Figure 6.1 plots the FOMs of several comparable 5 GHz VCOs over the past four years [77],[78],[79],[80],[81],[82],[83],[84],[85].

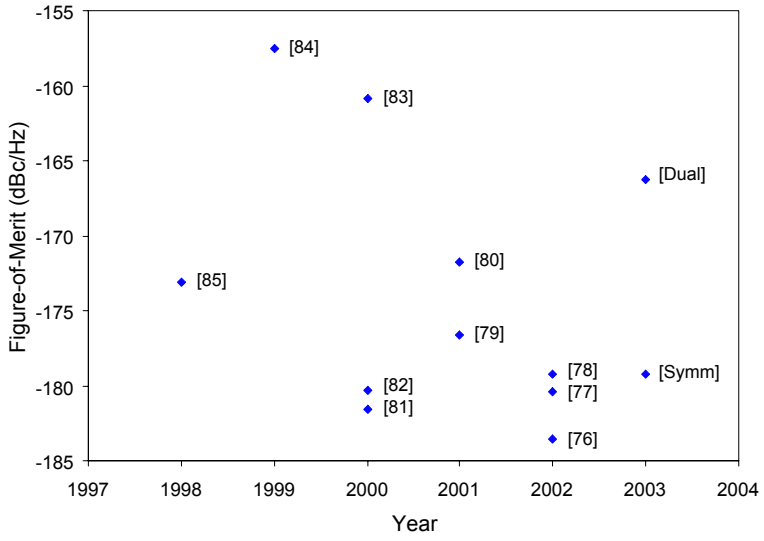

Figure 6.1: Comparison of the figure-of-merit from several VCOs over the past four years with the VCOs of this work.

The advantage of the higher Q symmetric inductor is quantified by comparing the FOM of the two VCO designs at the same varactor control voltage of 0 V. At this tuning voltage, the dual inductor VCO FOM is -166.3 dBc/Hz compared to -175.7 dBc/Hz for the symmetric inductor VCO — an improvement of about 10 dBc/Hz.

6.2 Improvements and Future Work

This section discusses several improvements that could be made in future revisions the circuits of this work as well as potential future work that could be done in the area of tunable I/Q LO sources.

- The inductor measurements could be improved by including open and short standards for the pads in any future revisions. It is expected that the measured data agrees more closely to the full-wave electromagnetic simulations performed than shown by the comparisons presented in Section 5.2, since simulated data was used to deembed the probe pad parasitics. More accurate deembedding standards would likely improve the correlation of measured Q factor with the electromagnetic simulations at higher frequencies.

- Future revisions of the VCOs would benefit from redesigning the tank circuit to account for parasitic capacitance so that the output frequency range would cover all three of the U-NII bands from 5.15 to 5.825 GHz. It should be noted that first pass success of an RFIC requires accurate and reliable parasitic extraction for the given process. A revised design could also include modifying the tank circuit with fixed switched capacitance and smaller varactors in order to lower the effective K_v of the VCOs. Both the VCO designs would benefit from lower K_v so that they could be integrated into phase locked loops (PLLs).

- The VCO design could be improved, as discussed in Chapter 3, by using a capacitive divider to attenuate the output of the VCO to avoid compressing a classical differential pair buffer at the output. This would not affect VCO phase noise, since the VCO core is allowed to operate with a high oscillation amplitude — the attenuation would primarily improve power consumption in the output buffers. However, if a differential pair were to be used, the input impedance of the polyphase would need to be increased to prevent loading down the output of the buffer and degrading the gain.

- Future work also includes testing the fabricated tunable polyphase VCO circuits that were damaged by the vendor in the packaging process. A die photo of this polyphase VCO is shown in Figure 6.2. Efforts are currently underway to package and test samples of this circuit from a previously unsawed wafer section. When the circuits are available for testing, a different test setup will be required than that used for the stand-alone polyphase filter. For example, the circuit could be tested by mixing down the quadrature phase outputs to a frequency that could be sampled by an oscilloscope in the time domain (e.g., less than 100 MHz) (see Figure 6.3). After downconversion, the output signals could be analyzed for various varactor control voltages as in Section 5.4. However, all the downconversion mixers would need to provide the same relative phase shift to each of the IF outputs to the oscilloscope for this test setup, unless the mixers were calibrated out of the measurements.

- The quadrature VCO with tunable polyphase outputs would benefit from a revision of the symmetric inductor VCO to increase its output frequency range. A similar revision is needed to reduce the differential error introduced to the

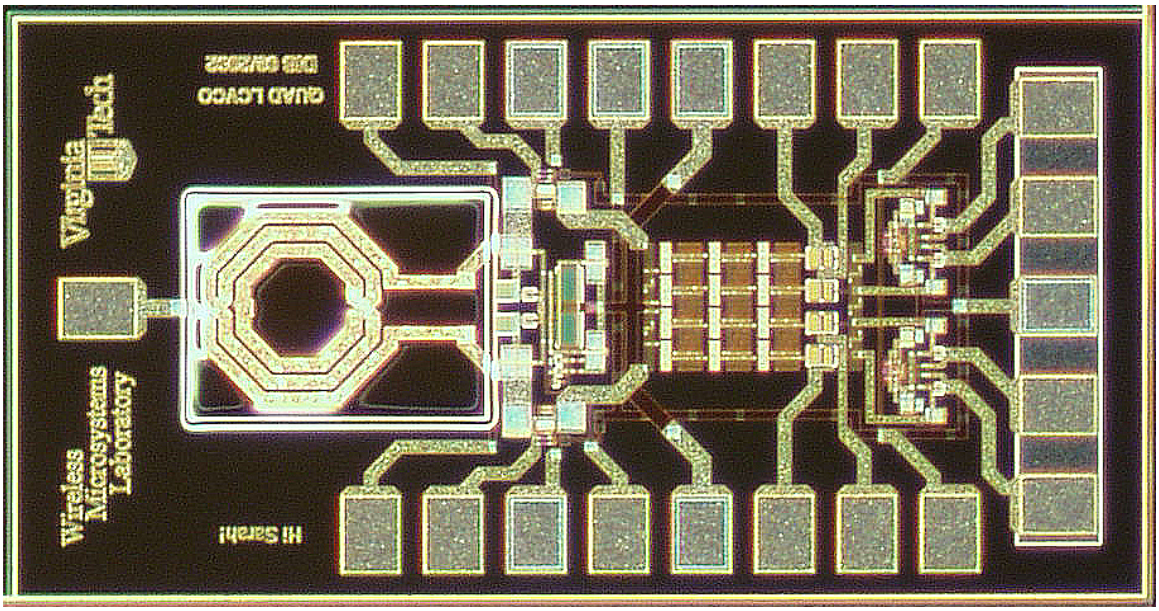

Figure 6.2: Die photo of the polyphase VCO with tunable I/Q phase balance.

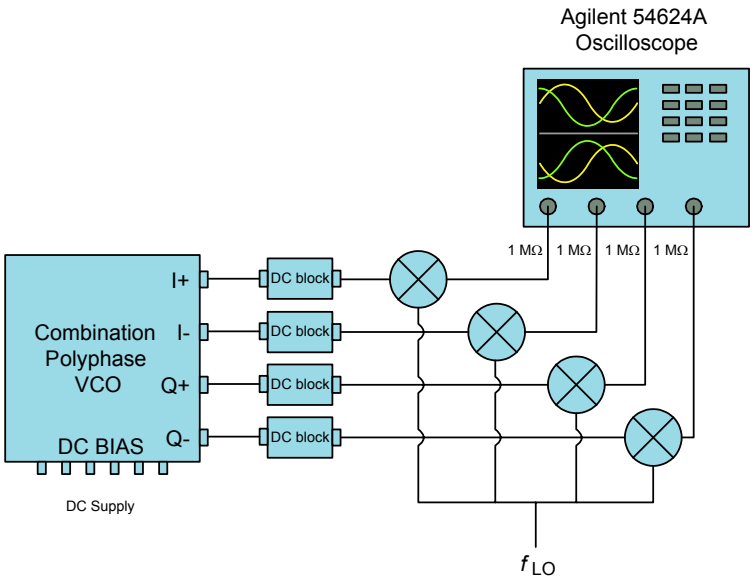

Figure 6.3: Potential test setup for the polyphase VCO circuit.

polyphase circuit by its input buffer (i.e., the VCO output buffer). Such a revision would need to increase the $\pm 5^{\circ}$ phase flatness bandwidth of the polyphase network and simplify tuning the polyphase output varactor control voltages for minimum phase error.

- Since the concept of a polyphase with tunable I/Q balance has been demonstrated, a method to sense the output I/Q imbalance and automatically adjust the output varactor control voltages is required in order to integrate a tunable I/Q LO source into a receiver. Using the tunable polyphase in a Weaver architecture would require sensing the required I/Q imbalance to *intentionally* introduce the phase compensation at the outputs to improve image rejection. To improve the BER of an I/Q receiver (e.g., direct conversion and low-IF receivers), a method to detect I/Q imbalance would be required. One potential solution is to use a variation of a phase-locked loop with multiple phase detectors to create control voltages for the polyphase output varactors. The feedback required for any automatic control of the phase tunability would introduce latency into the system, and this would need to be compared with the equivalent delay for competing DSP-based solutions.

Appendix A

Derivation of Inductor Parameters

As discussed in Chapter 2, a monolithic inductor on lossy Si substrates can be modeled by the lumped element network shown in Figure A.1. Furthermore, by assuming that $Y_{12} = Y_{21}$, the lumped elements can be combined into a π-equivalent circuit of admittance blocks (Figure A.2).

Single-ended excitation requires that port 2 of the inductor be grounded. Thus, the $Y_{22} + Y_{12}$ element of Figure A.2(a) is shorted out, reducing the input impedance to:

$$R + jX = \frac{1}{Y_{11} + Y_{12} - Y_{12}} = \frac{1}{Y_{11}} \tag{A.1}$$

Therefore, the single ended equivalent inductance and Q factor are given by:

$$L = \frac{X}{2\pi f} = \frac{1}{2\pi f} \cdot \mathrm{Im}\left(1/Y_{11}\right) \tag{A.2}$$

and

$$Q = \frac{X}{R} = \frac{\mathrm{Im}\left(1/Y_{11}\right)}{\mathrm{Re}\left(1/Y_{11}\right)}. \tag{A.3}$$

However, if the inductor is to be used differentially, the *floating* impedance between the two ports of the π-equivalent circuit in Figure A.2(b) must be used to calculate the equivalent inductance and Q factor. By inspection, this floating impedance is given as the parallel combination of the series admittance $(-Y_{12})$ and the sum of the two shunt elements ($Y_{11} + Y_{12}$ and $Y_{22} + Y_{12}$) [51]. This floating impedance can be

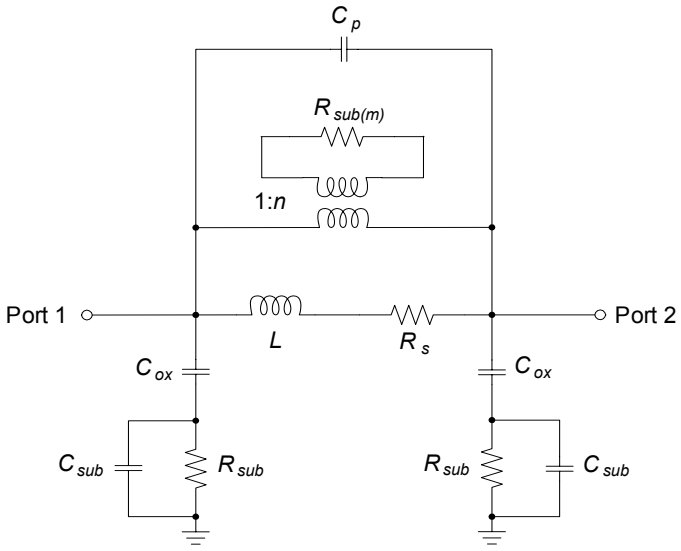

Figure A.1: A lumped element model for monolithic inductors on Si substrates (after [53]).

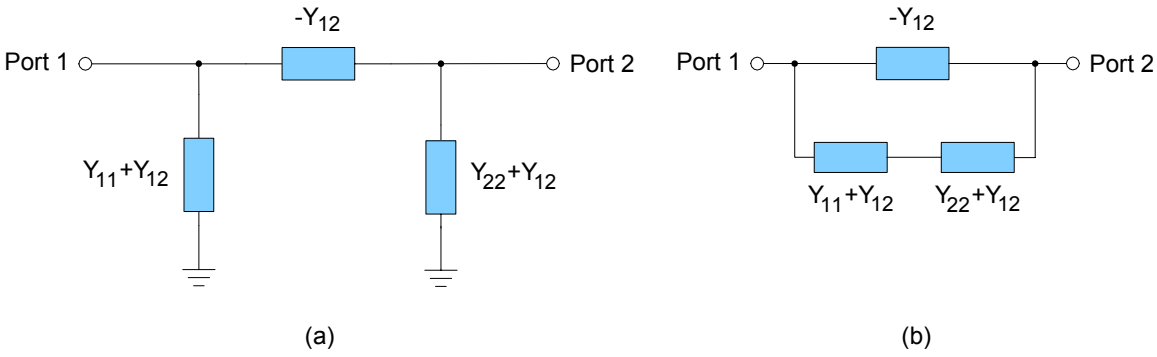

Figure A.2: (a) A π-eqivalent Y-parameter network of the lumped element model for monolithic inductors on Si substrates (see Figure A.1). (b) Simplification of the Y-parameter network for differential inductors.

simplified in several steps:

$$R + jX = \left(-\frac{1}{Y_{12}}\right) \| \left(\frac{1}{Y_{11}+Y_{12}} + \frac{1}{Y_{22}+Y_{12}}\right) \tag{A.4a}$$

$$= \frac{-\frac{1}{Y_{12}}\left(\frac{1}{Y_{11}+Y_{12}} + \frac{1}{Y_{22}+Y_{12}}\right)}{-\frac{1}{Y_{12}} + \frac{1}{Y_{11}+Y_{12}} + \frac{1}{Y_{22}+Y_{12}}} \tag{A.4b}$$

$$= \frac{\frac{Y_{22}+Y_{11}+2Y_{12}}{-Y_{12}(Y_{11}+Y_{12})(Y_{11}+Y_{12})}}{\frac{(Y_{11}+Y_{12})(Y_{22}+Y_{12})-Y_{12}(Y_{22}+Y_{12})-Y_{12}(Y_{11}+Y_{12})}{-Y_{12}(Y_{11}+Y_{12})(Y_{11}+Y_{12})}} \tag{A.4c}$$

$$= \frac{Y_{22}+Y_{11}+2Y_{12}}{(Y_{11}+Y_{12})(Y_{22}+Y_{12}) - Y_{12}(Y_{22}+Y_{12}) - Y_{12}(Y_{11}+Y_{12})} \tag{A.4d}$$

$$= \frac{Y_{22}+Y_{11}+2Y_{12}}{Y_{11}Y_{22}+Y_{11}Y_{12}+Y_{22}Y_{12}+Y_{12}^2 - Y_{12}Y_{22} - Y_{12}^2 - Y_{12}Y_{11} - Y_{12}^2} \tag{A.4e}$$

$$= \frac{Y_{22}+Y_{11}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}. \tag{A.4f}$$

This simplified equation can be used to calculate the differential equivalent inductance and Q factor:

$$L = \frac{X}{2\pi f} = \left(\frac{1}{2\pi f}\right)\left[\mathrm{Im}\left(\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right)\right] \tag{A.5}$$

and

$$Q = \frac{X}{R} = \frac{\left[\mathrm{Im}\left(\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right)\right]}{\left[\mathrm{Re}\left(\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}\right)\right]}. \tag{A.6}$$

Equations A.5 and A.6 were used in this work to characterize the differential inductors used in the symmetric and dual VCO tank circuits.

Appendix B

Derivation of the Polyphase Transfer Function

Figure B.1(a) shows a single-stage *RC-CR* network. Using the $V_{2,in}$ node as the reference, the $V_{1,in}$ to $V_{1,out}$ voltage transfer function is given by:

$$F_{11}(\omega) = \frac{V_{1,out}}{V_{1,in}} = \frac{1}{1 + j\omega RC} \tag{B.1}$$

and the $V_{1,in}$ to $V_{2,out}$ voltage transfer function is given by:

$$F_{21}(\omega) = \frac{V_{2,out}}{V_{1,in}} = \frac{-j\omega RC}{1 + j\omega RC}. \tag{B.2}$$

The phase angle of these two transfer functions are:

$$\angle F_{11}(\omega) = -\tan^{-1}(\omega RC) \tag{B.3}$$

$$\angle F_{21}(\omega) = 90^\circ - \tan^{-1}(\omega RC). \tag{B.4}$$

From these two equations, it follows that the two outputs always differ in phase by 90°. In particular, when $\omega = 1/RC$, the phase shift of $V_{1,out}$ is -45° and the phase shift of $V_{1,out}$ is $+45^\circ$.

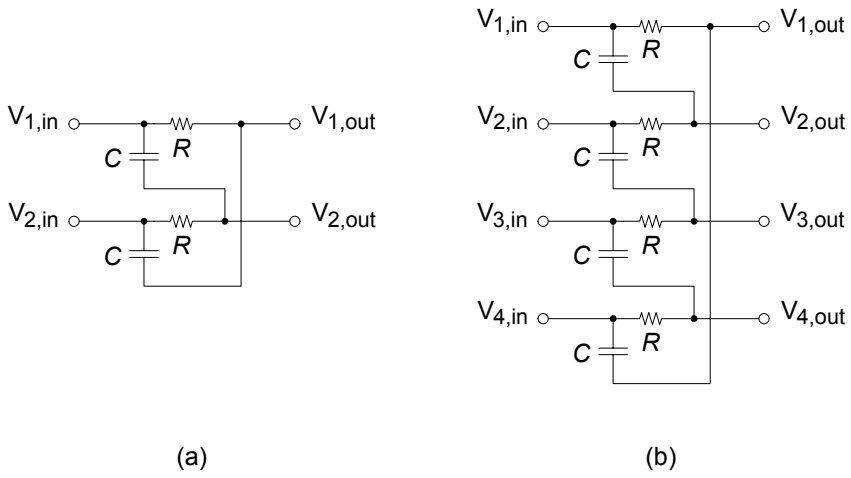

Figure B.1: Schematics of (a) a two-phase *RC-CR* network and (b) a four-phase *RC-CR* network.

Using equations B.1 and B.2, the transfer matrix of this network is given by:

$$\begin{bmatrix} V_{1,out} \\ V_{2,out} \end{bmatrix} = \frac{1}{1+j\omega RC} \begin{bmatrix} 1 & j\omega RC \\ -j\omega RC & 1 \end{bmatrix} \begin{bmatrix} V_{1,in} \\ V_{2,in} \end{bmatrix}. \tag{B.5}$$

The sign difference of the $j\omega RC$ elements of the matrix is necessary because the transfer equations depend on the polarity of the input signals with respect to the output signals. The transfer matrix is circulant and, therefore, the network can be classified as a Hilbert filter [86],[70],[87].

If a *positive* complex input signal is defined as $V_{in} = V_{1,in} + jV_{2,in}$ (i.e., a $+90^{\circ}$ phase difference as in equations B.3 and B.4), the open-circuit transfer function of the *RC-CR* circuit is given by:

$$G^{+}(\omega) = \frac{1}{2}F_{11}(\omega) + \frac{1}{2}F_{22}(\omega) - \frac{1}{2}jF_{12}(\omega) + \frac{1}{2}jF_{21}(\omega) = \frac{1+\omega RC}{1+j\omega RC} \tag{B.6}$$

where the complex number $(\pm j)$ included with $F_{12}(\omega)$ and $F_{21}(\omega)$ is necessary because of the polarity of the complex input signal. The factor of $1/2$ is necessary to account for the differential to single-ended conversion to find the transfer function. Similarly, the open-circuit transfer function of the *RC-CR* circuit when $V_{in} = V_{1,in} - jV_{2,in}$ (a

-90° phase difference or *negative* input sequence) is given by:

$$G^{-}(\omega) = \frac{1}{2}F_{11}(\omega) + \frac{1}{2}F_{22}(\omega) + \frac{1}{2}jF_{12}(\omega) - \frac{1}{2}jF_{21}(\omega) = \frac{1-\omega RC}{1+j\omega RC} \tag{B.7}$$

Therefore, the phase response of the complex output depends on the polarity of the input sequence, and is given by:

$$\angle G^{+}(\omega) = -\tan^{-1}(\omega RC) \tag{B.8}$$

$$\angle G^{-}(\omega) = -180^\circ - \tan^{-1}(\omega RC). \tag{B.9}$$

A relationship between the complex output phase and the individual output phases can be determined by comparing equations B.8 and B.9 with equations B.3 and B.4. First, the output phase of the differential $V_{1,out}$ signal can be found using equation B.8 or B.9, depending on the polarity of the input signal. Second, the output phase of the differential $V_{2,out}$ signal can be found by adding 90° to equation B.8 or B.9.

The differential input and output signals of the polyphase network shown in Figure B.1(b) can be defined as:

$$V_{I,in} = V_{1,in} - V_{3,in} \tag{B.10}$$

$$V_{Q,in} = V_{2,in} - V_{4,in} \tag{B.11}$$

$$V_{I,out} = V_{1,out} - V_{3,out} \tag{B.12}$$

$$V_{Q,out} = V_{2,out} - V_{4,out} \tag{B.13}$$

These differential signals allow the single stage polyphase network to be described using the same transfer matrix as the *RC-CR* network given in equation B.5:

$$\begin{bmatrix} V_{I,out} \\ V_{Q,out} \end{bmatrix} = \frac{1}{1+j\omega RC} \begin{bmatrix} 1 & j\omega RC \\ -j\omega RC & 1 \end{bmatrix} \begin{bmatrix} V_{I,in} \\ V_{Q,in} \end{bmatrix}. \tag{B.14}$$

As with the *RC-CR* network, for positive input sequences, the open-circuit transfer function of a single-stage polyphase network is given by:

$$G_1^{+}(\omega) = \frac{1+\omega RC}{1+j\omega RC}. \tag{B.15}$$

and for negative input sequences:

$$G_1^- (\omega) = \frac{1 - \omega RC}{1 + j\omega RC}. \tag{B.16}$$

Similarly, the output phase response for differential complex positive and negative sequences are again given by:

$$\angle G_1^+ (\omega) = -\tan^{-1} (\omega RC) \tag{B.17}$$

$$\angle G_1^- (\omega) = -180^\circ - \tan^{-1} (-\omega RC) . \tag{B.18}$$

However, for quadrature signal generation, the individual phases of the $V_{1,out}$, $V_{2,out}$, $V_{3,out}$, and $V_{4,out}$ nodes are of greater importance. Using equations B.3, B.4, and B.17, the phase angles of $V_{1,out}$ and $V_{2,out}$ are:

$$\angle V_{1,out} = -\tan^{-1} (\omega RC) \tag{B.19}$$

$$\angle V_{2,out} = 90^\circ - \tan^{-1} (\omega RC) . \tag{B.20}$$

From equations B.3, B.4, and B.18 the phase angles of $V_{3,out}$ and $V_{4,out}$ are:

$$\angle V_{3,out} = -180^\circ - \tan^{-1} (\omega RC) \tag{B.21}$$

$$\angle V_{4,out} = -90^\circ - \tan^{-1} (\omega RC) . \tag{B.22}$$

These four equations show the quadrature phase generation created by the polyphase network from a differential input signal.

The transfer function of multiple stage networks are found by simplifying a series connection of single-stage polyphase transfer functions (i.e., equation B.15). For example, the transfer function of a three-pole polyphase network is given by [86]:

$$G_3 (\omega) = G_{1,1}^+ (\omega) G_{1,2}^+ (\omega) G_{1,3}^+ (\omega) = \frac{N_3 (\omega)}{D_{3R} (\omega) + j D_{3I} (\omega)} \tag{B.23}$$

where

$$N_3 (\omega) = (1 + \omega R_1 C_1) (1 + \omega R_2 C_2) (1 + \omega R_3 C_3) \tag{B.24}$$

$$\begin{aligned} D_{3R}(\omega) &= 1-\omega^2[R_1C_1R_2C_2+R_2C_2R_3C_3+R_1C_1R_3C_3 \\ &\quad +2R_1C_3(R_2C_2+R_2C_1+R_3C_2)] \end{aligned} \tag{B.25}$$

$$\begin{aligned} D_{3I}(\omega) &= \omega[R_1C_1+R_2C_2+R_3C_3+2(R_1C_2+R_2C_3+R_1C_3)] \\ &\quad -\omega^3R_1C_1R_2C_2R_3C_3. \end{aligned} \tag{B.26}$$

The polyphase designed in this thesis has a transfer function represented by equation B.23. The gain and phase of this transfer function are given by [86]:

$$|G_3(\omega)| = \frac{|N_3(\omega)|}{\sqrt{[D_{3R}(\omega)]^2+[jD_{3I}(\omega)]^2}} \tag{B.27}$$

$$\angle G_3(\omega) = -\tan^{-1}\left(\frac{D_{3I}(\omega)}{D_{3R}(\omega)}\right) \tag{B.28}$$

Appendix C

Matlab Code for Calculating Differential Inductor Parameters

C.1 l_extract.m

```
function [f,Z,L,Q]=l_extract(sfile)
%l_extract imports the S-parameters from a real/imaginary touchstone
% formatted file, converts to Y-parameters and calculates the differential
% effective inductance and Quality (Q) factor.
% [f,Z,L,Q]=l_extract(sfile) where:
% sfile := the absolute or relative path to touchstone format input file
% f := a vector containing the frequency points
% Z := a vector of the impedance (complex numbers)
% L := a vector of the differential effective inductance (nH)
% Q := a vector of the differential Quality factor
%
% read all the data from comma separated ASCII files, real-imag format
[f,s11,s21,s12,s22]=readTouch(2,sfile);
% change units to GHz and nH
f=f/1e9;
%
fig=0;
```

```
%
% convert s-parameters to y-parameters
z0=50;
y0=z0^-1;
den=(1+s11).*(1+s22)-(s12.*s21);
y11=y0*(((1-s11).*(1+s22)+(s12.*s21))./den);
y22=y0*(((1+s11).*(1-s22)+(s12.*s21))./den);
y12=y0*((-2*s12)./den);
y21=y0*((-2*s21)./den);
%
% Calculate Inductor parameters
Z=(y11+y22+y12+y21)./(y11.*y22-y12.*y21);
L=imag((Z)./(2*pi*f));
L1=imag((1./-y12)./(2*pi*f));
Q=(imag(Z)./real(Z));
Q1=imag(1./-y12)./real(1./-y12);
%
% Plot Results
% Inductance
fig=fig+1;
figure(fig), plot(f,L,f,L1)
title('Differential Inductance');
ylabel('Inductance'), xlabel('frequency (Hz)')
% Quality Factor
fig=fig+1;
figure(fig), plot(f,Q,f,Q1)
title('Differential Quality Factor (Q)');
ylabel('Q'), xlabel('frequency (Hz)')
% Impedance
fig=fig+1;
figure(fig), plot(f,real(Z),f,imag(Z))
title('Floating Impedance');
ylabel('impedance (ohms)'), xlabel('frequency (Hz)')
legend('real','imaginary')
```

C.2 readTouch.m

```
function [f,s11,s21,s12,s22]=readTouch(portnum,file1)
%readTouch imports S-parameters from a touchstone formatted file
% and outputs the frequency and S-parameters in separate vectors.
% [f,s11,s21,s12,s22]=readTouch(portnum,file1) where:
% portnum := number of ports (1 or 2)
% file1 := the absolute or relative path to touchstone format input file
% f := a vector containing the frequency points
% s11 := a vector containing s11 (complex numbers)
% s21 := a vector containing s21 (complex numbers)
% s12 := a vector containing s12 (complex numbers)
% s22 := a vector containing s22 (complex numbers)
%
% Open input file
sdata = fopen(file1,'r'); % Open input file
% Ignore comment lines
n=0;
freqUnit=1e9; % set default frequency unit to GHz
while n==0
s = fgetl(sdata);
P = sscanf(s,'%s');
if P(1)=='!'
n=0;
elseif P(1)=='#'
% test for frequncy unit
if P(2)=='G' | P(2)=='g' % GHz
freqUnit=1e9;
elseif P(2)=='M' | P(2)=='m' % MHz
freqUnit=1e6;
elseif P(2)=='K' | P(2)=='k' % kHz
```

```
freqUnit=1e3;
else % Hz
freqUnit=1;
P(6)=P(5);
end
% test for complex number format
if P(6)=='M' | P(6)=='m'
n=1; % format is magnitude angle
else
n=2; % format is real imaginary
end
else
output=sprintf('\n"%s" is not in Touchstone format.\n',file1);
disp(output);
n=2;
end
end
if n==1 % Magnitude angle file
notEOF=feof(sdata);
n=1;
while notEOF==0
deg2rad=pi/180;
s = fgetl(sdata);
notEOF=feof(sdata);
if (portnum==1)
% Read 3 columns of the next row to vector P
P = sscanf(s,'%s')';
if P(1)~='!'
P = sscanf(s,'%g %g %g')';
f(n)=P(1)*freqUnit;
s11(n)=P(2)*cos(P(3)*deg2rad)+i*P(2)*sin(P(3)*deg2rad);
n=n+1;
end
elseif (portnum == 2)
```

```
% Read 9 columns of the next row to vector P
P = sscanf(s,'%s')';
if P(1)~='!'
P = sscanf(s,'%g %g %g %g %g %g %g %g %g')';
f(n)=P(1)*freqUnit;
s11(n)=P(2)*cos(P(3)*deg2rad)+i*P(2)*sin(P(3)*deg2rad);
s21(n)=P(4)*cos(P(5)*deg2rad)+i*P(4)*sin(P(5)*deg2rad);
s12(n)=P(6)*cos(P(7)*deg2rad)+i*P(6)*sin(P(7)*deg2rad);
s22(n)=P(8)*cos(P(9)*deg2rad)+i*P(8)*sin(P(9)*deg2rad);
n=n+1;
end
else
output=sprintf('\nOnly one or two port networks supported at this time.');
disp(output);
notEOF=2;
end % if portnum==1
end % while loop
end
if n==2 % Real Imaginary file
notEOF=feof(sdata);
n=1;
while notEOF==0
s = fgetl(sdata);
notEOF=feof(sdata);
if (portnum==1)
% Read 3 columns of the next row to vector P
P = sscanf(s,'%s')';
if P(1)~='!'
P = sscanf(s,'%g %g %g')';
f(n)=P(1)*freqUnit;
s11(n)=P(2)+i*P(3);
n=n+1;
end
elseif (portnum == 2)
```

```
% Read 9 columns of the next row to vector P
P = sscanf(s,'%s')';
if P(1)~='!'
P = sscanf(s,'%g %g %g %g %g %g %g %g %g')';
f(n)=P(1)*freqUnit;
s11(n)=P(2)+i*P(3);
s21(n)=P(4)+i*P(5);
s12(n)=P(6)+i*P(7);
s22(n)=P(8)+i*P(9);
n=n+1;
end
else
output=sprintf('\nOnly one or two port networks supported at this time.');
disp(output);
notEOF=2;
end % if portnum==1
end % end while
end
fclose(sdata);
```

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Vita

David Ivan Sanderson was born on August 18, 1976 in Heber City, Utah. After living in Colorado, Georgia, Indiana, and northern California, he moved to Bakersfield, California in 1989. He graduated in 1994 from Bakersfield High School and began his college studies at the University of California, Davis as a physics major. After one year of college he served a two-year, full-time mission for the Church of Jesus Christ of Latter-day Saints in Barcelona, Spain. After returning from Spain, he moved to Salt Lake City, Utah, where he attended the University of Utah, majoring in Electrical Engineering. He received his Bachelors of Science, Magna Cum Laude, in May 2001.

Two years of summer internships with Motorola, Wireless Infrastructure Systems Division, sparked David's interest in graduate research of wireless integrated circuits. The autumn after receiving his Bachelor's degree, he moved to Blacksburg, Virginia to pursue a Master's degree in Electrical Engineering at Virginia Tech.

David was married to his wife Tauna in 1998 in Salt Lake City, Utah. They have one daughter, Sarah, who was born in the spring of 2001.

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