# Frequency Locking Techniques Based on Envelope Detection for Injection-Locked Signal Sources

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## ABSTRACT

Signal generation at high frequency has become increasingly important in numerous wireline and wireless applications. In many gigahertz and millimeter-wave frequency ranges, conventional frequency generation techniques have encountered several design challenges in terms of frequency tuning range, phase noise, and power consumption. Recently, injection locking has been a popular technique to solve these design challenges for frequency generation. However, the narrow locking range of the injection locking techniques limits their use. Furthermore, they suffer from significant reference spur issues.

This dissertation presents novel frequency generation techniques based on envelope detection for low-phase-noise signal generation using injection-locked frequency multipliers (ILFMs). Several calibration techniques using envelope detection are introduced to solve conventional problems in injection locking. The proposed topologies are demonstrated with 0.13μm CMOS technology for the following injection-locked frequency generators.

First, a mixed-mode injection-frequency locked loop (IFLL) is presented for calibrating locking range and phase noise of an injection-locked oscillator (ILO). The IFLL autonomously tracks the injection frequency by processing the AM modulated envelope signal bearing a frequency difference between injection frequency and ILO free-running frequency in digital feedback.

Second, a quadrature injection-locked frequency tripler using third-harmonic phase shifters is proposed. Two capacitively-degenerated differential pairs are utilized for quadrature injection signals, thereby increasing injection-locking range and reducing phase error.

Next, an injection-locked clock multiplier using an envelope-based frequency tracking loop is presented for a low phase noise signal and low reference spur. In the proposed technique, an envelope detector constantly monitors the VCO's output waveform distortion caused by frequency difference between the VCO frequency and reference frequency. Therefore, the proposed techniques can compensate for frequency variation of the VCO due to PVT variations.

Finally, this dissertation presents a subharmonically injection-locked PLL (SILPLL), which is cascaded with a quadrature ILO. The proposed SILPLL adopts an envelope-detection based injection-timing calibration for synchronous reference pulse injection into a VCO. With one of the largest frequency division ratios (N=80) reported so far, the SILPLL can achieve low RMS jitter and reference spur.

# Frequency Locking Techniques Based on Envelope Detection for Injection-Locked Signal Sources

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## GENERAL AUDIENCE ABSTRACT

Signal generation at high frequency has become increasingly important in numerous wireline and wireless applications. In many gigahertz and millimeter-wave frequency ranges, conventional frequency generation techniques have encountered several design challenges in terms of frequency tuning range, phase noise, and power consumption. Recently, injection locking which synchronizes a signal frequency has been a popular technique to solve these design challenges for frequency generation. However, narrow operation ranges of the injection locking techniques limit their use. Furthermore, they suffer from significant noise degradation.

This dissertation presents studies of frequency generation techniques based on envelope detection (amplitude modulation) for low-phase-noise signal generation using injection-locked frequency multipliers. Several calibration techniques using envelope detection are introduced to solve conventional problems in injection locking.

First, a mixed-mode injection-frequency locked loop is presented for calibrating locking range and phase noise of an injection-locked oscillator. Second, a quadrature injection-locked frequency tripler using third-harmonic phase shifters is proposed to increase injection-locking range and reduce phase error. Third, an injection-locked frequency multiplier using an envelope-based frequency tracking loop is presented for a low phase noise signal and low noise degradation. Finally, this dissertation presents a subharmonically injection-locked PLL with a novel injection-

timing calibration circuit, which is connected to a quadrature frequency multiplier. The proposed designs are demonstrated with 0.13μm CMOS technology.

# DEDICATION

To

Soyoung Jung

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# Chapter 1.

# Introduction

## 1.1 Motivation

A phase-locked loop (PLL) is widely used in several wireline and wireless applications. In general, the PLL is used to generate a local signal which has low phase noise at a precise frequency. In the PLL, the output signal is synchronized to the phase of a low-frequency signal provided by a crystal oscillator. The design of the PLL considers several key performance specifications such as phase noise, power consumption, jitter, reference spur, and area. Typical RF transceivers require the PLL system for pure signal generation. Nowadays, they work optimally with full integration of the RF front-end on a single chip with CMOS technology for low cost and power consumption, compared to the more expensive bipolar technology. However, the unity current gain frequency, $f_t$, of the transistor in CMOS technology limits the operating frequencies in high frequency synthesizers. A voltage-controlled oscillator (VCO) and first-stage frequency divider which operate at the highest frequency are responsible for most power consumption in the high frequency synthesizer. In general, as the operating frequency increases in frequency synthesizers, the total power consumption normally increases to achieve a low phase noise signal. To alleviate this problem, currently, an injection-locked oscillator is a good alternative with low phase noise generation. Recently, many research works on injection locking aim to have a good figure of merit (FOM) between jitter and power consumption. Several sub-harmonically injection-locked frequency generators are proposed for very low-jitter integer-*N* frequency

generation based on either ring [1-1]–[1-3] or LC VCOs [1-4]–[1-9]. In this dissertation, the injection locking techniques based on LC VCOs are mainly analyzed and designed.

## 1.2 Overview of Injection Locking

The basic principle of injection locking is to synchronize an oscillatory system with an injection signal. If the frequency of the injection signal is very close to that of the oscillator frequency, the oscillator is locked by the injection frequency and the phase noise close to the output signal is shaped by the injection signal. This technique allows for circuit operation at high frequencies (such as millimeter waves) with low power consumption.

The injection-locked frequency generators are designed based on an injection-locked oscillator (ILO). The typical ILO is conceptually expressed as shown in Figure 1-1, which consists of an LC tank, an NMOS transistor, an inverter and a current source [1-10]. The resonance frequency without injection is $\omega_{out} = 1/(LC)^{1/2}$, where $L$ and $C$ are inductance and capacitance of the LC-tank. $I_{tank}$ through the LC tank equals $I_{osc}$ passing through the NMOS transistor. Hence, there is no phase shift in the LC-tank. When the injection current, $I_{inj}$, is injected into the oscillator, $I_{tank}$ equals the vector-sum of $I_{inj}$ and $I_{osc}$. Fig. 1.2(a) shows that $I_{inj}$ leads to the phase $\alpha$ between $I_{tank}$ and $I_{osc}$ in the LC-tank. As shown in Fig. 1-2(b), for injection locking, $\omega_{out}$ is shifted away from $\omega_0$ due to the phase shift of $\alpha$. If $\omega_{out}$ is not equal

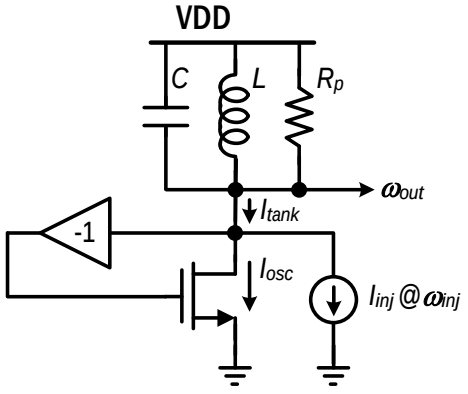
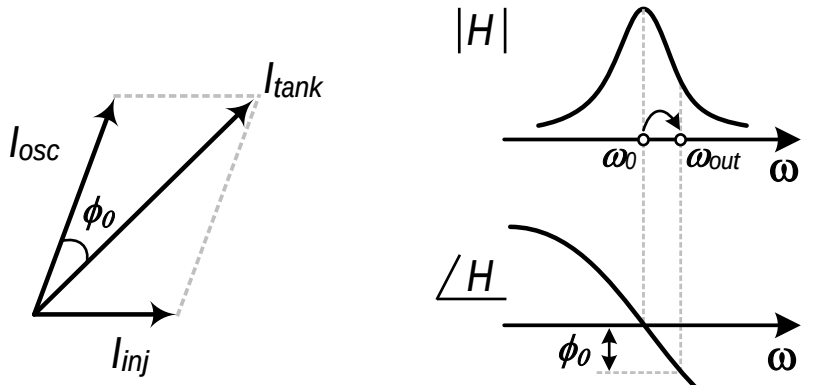



Fig. 1-1. Conceptual oscillator using injection locking.

to $\omega_{inj}$, the phase shift in the LC-tank is continuously changed to track $\omega_{inj}$. Finally, the ILO becomes stable when a specific phase shift of $\alpha$ is produced, which makes $\omega_{out}$ equal to $\omega_{inj}$.

In general, the oscillator is unlocked and distorted by the injection signal when the injection frequency deviates from the injection-locking range. It is called injection pulling. Injection pulling in an oscillator is usually undesirable in most of applications. For example Fig. 1-3 shows undesirable injection pulling in direct-conversion transmitters. Since the PA has very large output power, the local oscillator would be coupled to a fraction of the PA output. Recently, the system uses a $2\omega_{LO}$ local oscillator with a frequency divider to avoid the injection pulling at $\omega_{LO}$. In general, this occurs when the injection frequency is less than




(a) (b)

Fig. 1-2. (a) Phasor diagram and (b) open-loop characteristics.

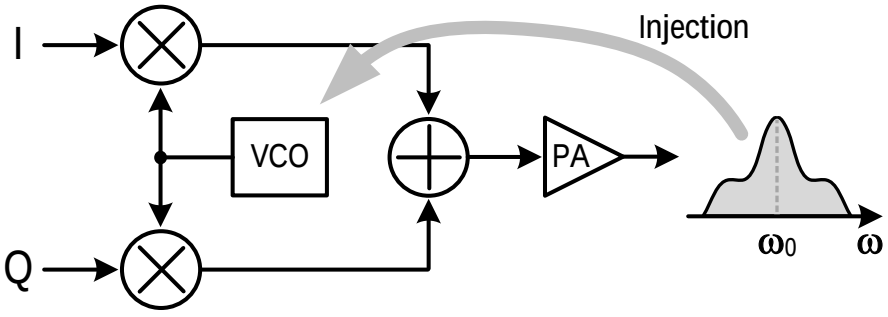
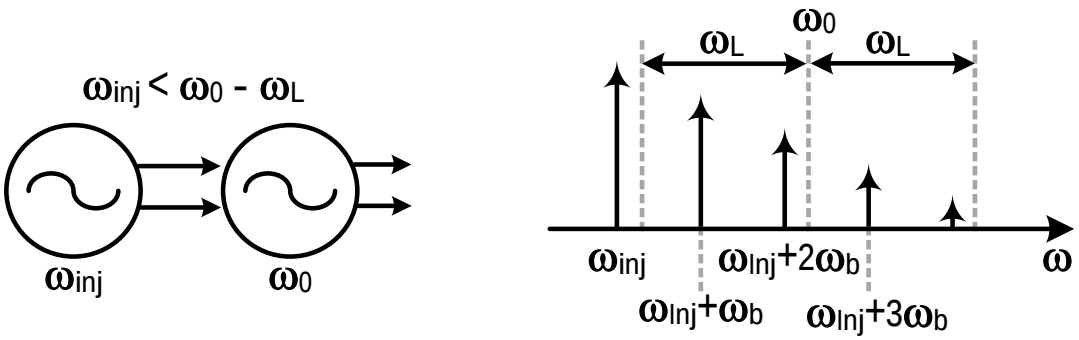



Fig. 1-3. Injection pulling example in a direct-conversion transmitter.




(a) (b)

Fig. 1-4. (a) Injection-pulled condition and (b) spectrum of an injection-pulled oscillator.

the frequency difference between free-running frequency of a slave oscillator and its injection locking range, $\omega_{L,}$ as shown in Fig. 1-4. Injection pulling causes frequency modulation of the slave oscillator where the modulation frequency is defined as $\omega_b \approx |\omega_{inj} - \omega_0|$ [1-10].

## 1.3 Use of Injection Locking

### 1.3.1 Multiphase Generation

Recently, multiphase signals play a key role in a variety of applications, such as image-reject receivers [1-11], half-rate clock-and-data recovery circuits [1-12] and phased arrays [1-13]. There are typical ways to generate multiphase signals: frequency divider [1-14], poly-phase filter [1-15] and multiphase ring oscillator. The frequency divider for multiphase signals has the advantage of easy design but several drawbacks of high phase noise, frequency limitation and poor phase accuracy. Likewise, the poly-phase filter suffers from poor phase accuracy due to device mismatch and process variation. Thus, the multiphase ring oscillator is more desirable for signal generation at millimeter waves.

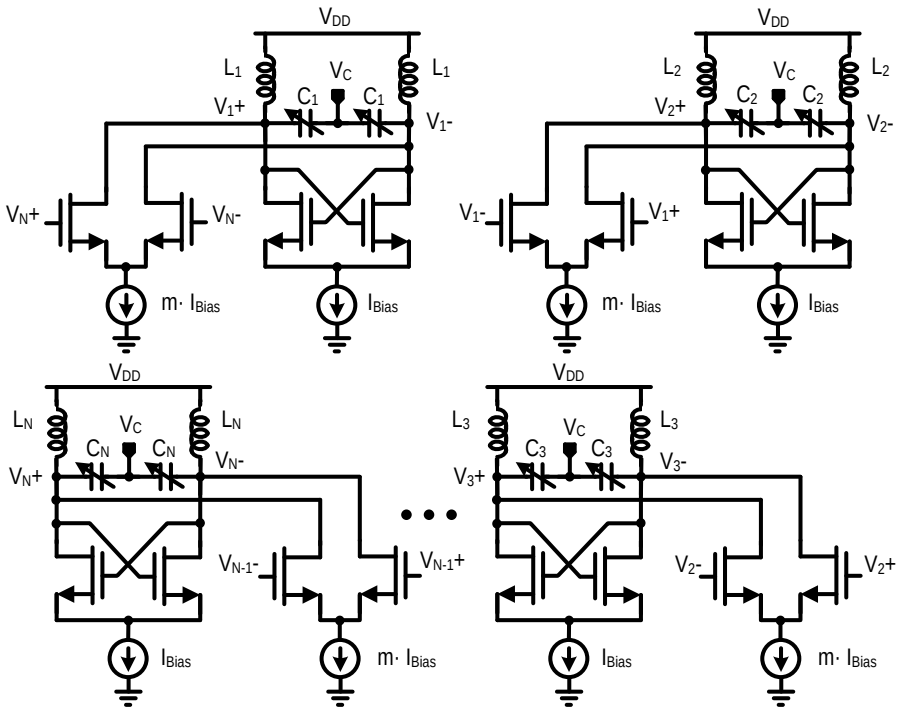
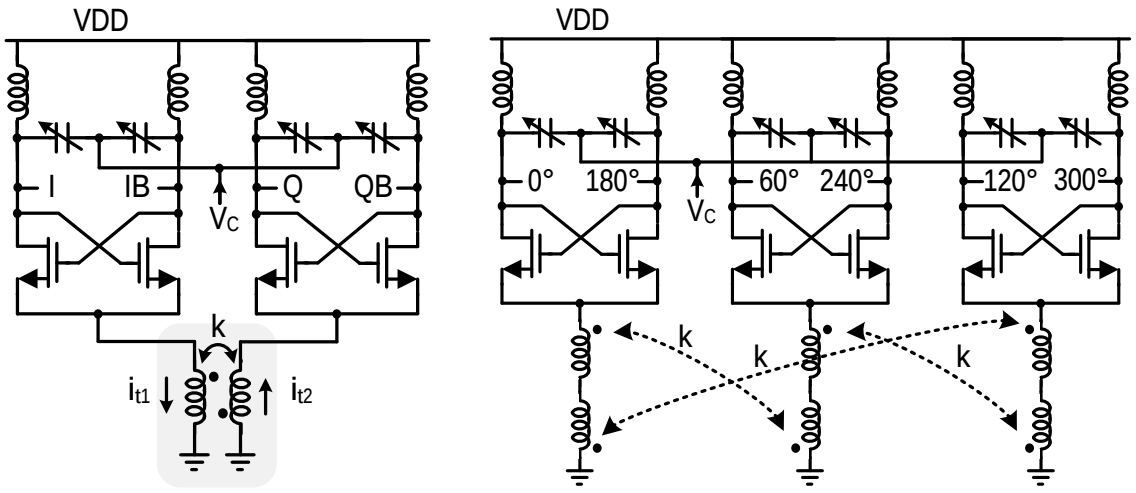



Fig. 1-5. Schematic of multiphase ring LC oscillator.

In general, a ring LC oscillator is widely used for multiphase signal generation at a high frequency. The injection locking concept is used to create phase relations between the multiphase signals. For example, Fig. 1-5 shows a schematic of a conventional *N* coupled LC oscillator. Each oscillator has an active transconductor to compensate for the parallel resistance of the LC tank. The *N*-stage LC tanks are connected in a ring topology by injecting an (*n*-1)th tank current into the *n*th tank. Therefore, the oscillators can generate *N*-phase signals. In general, a coupling differential pair is used to inject the adjacent phase into each LC tank. Since the coupled pair causes a phase shift of the LC tank, its effective quality factor (Q) is reduced. Therefore, the cross-coupled multiphase oscillator increases phase noise and is not efficient in both power consumption and phase noise performance, compared to a standalone oscillator.

To reduce an increase of phase noise due to the reduced Q, an in-phase coupling network is proposed for a quadrature VCO (QVCO) as shown in Fig. 1-6(a) [1-16]. The QVCO uses the $2^{nd}$-harmonic of the outputs to couple each oscillator by implementing an inductive



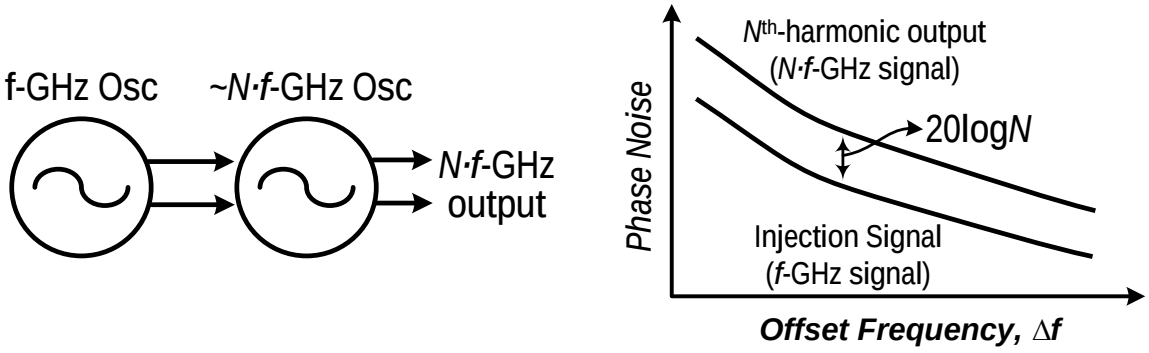

(a) (b)

Fig. 1-6. (a) Quadrature VCO and (b) six-phase VCO using super-harmonic coupling.

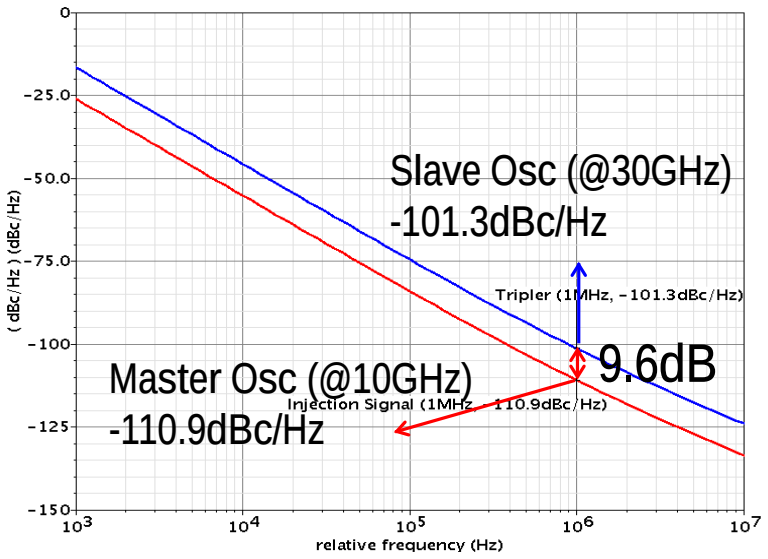
coupling network at two tail nodes. Two AC currents ($i_{t1}$ and $i_{t2}$) have opposite direction, which means in-phase coupling. Therefore, the QVCO achieves quadrature signal generation without any increase in phase noise and power consumption. Also, the inductive coupling network can be used to generate six-phase signals as shown in Fig. 1-6(b) [1-17]. In Appendix I, the six-phase VCO using super-harmonic coupling will be introduced.

### 1.3.2 Frequency Multiplication

A sub-harmonically injection-locked oscillator (ILO) is usually used to achieve a low phase noise signal at millimeter waves. It is very easy to implement the ILO. For example, let us assume that a master oscillator generates an $f_{inj}$ signal, and then the signal is injected into a slave oscillator which has the natural frequency of $f_0$ as shown in Fig. 1-2. If $f_0$ approximates $N$ times $f_{inj}$ and the slave oscillator is injection-locked, it will output an exact $N \cdot f_{inj}$ signal and its phase noise will increase only $20\log_{10}(N)$ than that of $f_{inj}$ as shown in Fig.



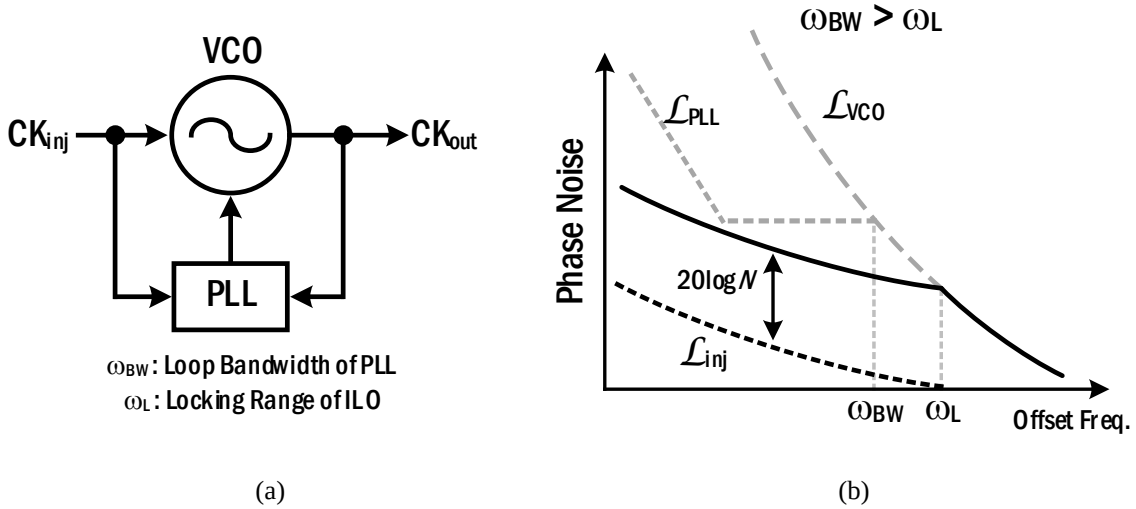

(a)




(b)

Fig. 1-7. (a) Injection-locked oscillator and (b) phase noise simulation.

1-7(a). There is an example of the phase noise simulation results in Fig. 1-7(b). The simulation results are performed with 0.13μm CMOS technology. The master oscillator generates a 10-GHz signal which is injected into the slave oscillator. After being injection-locked, the slave oscillator outputs a 30-GHz signal whose phase noise is -101.3 dBc/Hz at 1-MHz offset. The phase noise difference between the injection and output signals is 9.6 dB within all offset frequencies which is approximately $20\log_{10}(3)$.




(a) (b)

Fig. 1-8. (a) Block diagram of SILPLL and (b) its phase noise.

However, the operation of the sub-harmonic ILO depends on its injection locking range. In [1-10], the locking range, $\Delta\omega$, with weak injection is defined as

$$\Delta\omega = \frac{\omega_{osc}}{2Q}\frac{I_{inj}}{I_{osc}}\frac{1}{\sqrt{1-\left(I_{inj}/I_{osc}\right)^2}} \tag{1-1}$$

where $\omega_{osc}$ and $I_{osc}$ are the resonant frequency and current of the LC tank, respectively, $Q$ is the quality factor of the LC tank and $\omega_{inj}$ and $I_{inj}$ are the frequency and current of the injection signal, respectively. Although the locking range can increase with a decrease of $Q$ and $I_{osc}$, it causes a very small swing of the output. Also, enhancing the harmonic current for wide locking range is very limited. That is, it has difficulty in increasing the injection locking range by adjusting the parameters in (1-1).

In general, the sub-harmonic ILO has very narrow locking range. Therefore, it has difficulty in use for wide range applications. To solve this locking range issue, a frequency calibration circuit has been recently proposed in [1-18]. The calibration circuit corrects the free-running frequency of the ILO by detecting a phase difference between the free-running frequency and injection frequency. Also, another calibration circuit, an injection frequency-

locked loop is proposed in [1-19] to track injection frequency. In Chapter 2, the injection frequency-locked loop will be explained in detail.

A sub-harmonically injection-locked PLL (SILPLL) is a very popular choice to reduce in-band phase noise of PLL. Unlike a sub-harmonic ILO, the SILPLL does not suffer from the narrow injection locking range issue because the PLL already matched the $N^{th}$-harmonic of the injection signal with the VCO frequency (in Fig. 1-8(a)). However, the locking range affects phase noise shape of SILPLL output as shown in Fig. 1-8(b). When the locking range $\omega_L$ is greater than PLL loop bandwidth $\omega_{BW}$, in-band phase noise can be reduced as the reference phase noise plus $20\log_{10}(N)$. However, the SILPLL suffers from an injection timing issue [1-20]. If the injection pulse is not aligned with the optimal injection position, it may cause a significant reference spur and no phase noise reduction. Also, as the frequency ratio $N$ increases, the locking range rapidly decreases. Once the locking range is less than the PLL loop bandwidth, the SILPLL has the same phase noise shape as typical PLLs, without improving phase noise performance. Therefore, an injection timing aligner is required. In Chapter 4 and 5, two novel injection timing aligners are presented.

### 1.3.3 Frequency Division

When an ILO is locked by a super-harmonic input, it can act as a frequency divider which is known as an injection-locked frequency divider (ILFD). In general, static and current-mode logic (CML) frequency dividers are widely used as pre-scalars in frequency synthesizers. However, they have a speed limitation according to process technology and significant power consumption at high frequencies. The ILFD is very useful in millimeter-wave frequency synthesizers because the ILFD has inherent advantages in both speed and power dissipation compared to the static and CML dividers.

However, the ILFDs have disadvantages of a limited locking range and less flexible division ratios. Unlike static or CML frequency dividers, the ILFD can generate a frequency-divided signal only when the injection frequency is within the locking range. Furthermore, division ratio programming in the ILFD is obviously more difficult compared to its digital counterparts, which is partly due to its limited locking range for certain division ratios.

## 1.4 Challenges for Injection-Locked Frequency Generators

Sub-harmonically injection-locked frequency generators are widely used for low phase noise signal generation with easy frequency multiplication. However, they usually suffer from very limited locking range which causes unlocking without any phase noise reduction. In (1-1), the injection locking range can be increased as each parameter is maximized or minimized. However, their locking range is very limited with $N^{th}$-harmonic injection. Therefore, several frequency calibration circuits are presented in [1-2]-[1-6], [1-18]. In [1-18], the calibration circuit is very similar to PLL operation. However, it does not continuously track the frequency variation and has very large power consumption and area even through it provides exact frequency calibration. Also, in [1-5], the frequency tracking loops based on delay-locked loop are proposed. They can continuously track the frequency variation with slightly increased power consumption and area. However, the techniques cannot exactly correct phase error due to phase offset of their detectors at higher frequencies.

## 1.5 Dissertation Organization

The main objective of this dissertation is to study frequency locking techniques based on envelope detection for injection-locked signal sources in CMOS technology. As mentioned in Chapter 1.4, it is very difficult to utilize injection locking to frequency generators because of its very limited locking range. In order to solve the problem, three frequency locking techniques based on envelope detection are mainly presented in this dissertation. The techniques developed in this dissertation are designed and tested with 0.13-um CMOS technology at operating frequencies from 5 to 30 GHz. However, the architecture and techniques can be easily extended to any application where a low phase noise signal in frequency synthesizers is required.

In Chapter 2, a mixed-mode injection frequency-locked loop (IFLL) is presented for calibrating locking range and phase noise of an ILO. A brief understanding of the behavior of injection pulling is provided. The overall operation of the IFLL using envelope detection is explained. Also, the measurement results of the proposed IFLL are provided to prove its operation.

In Chapter 3, a quadrature injection-locked frequency tripler (ILFT) using third harmonic phase shifters is presented and analyzed. Characteristics of the proposed ILFT are compared to conventional quadrature ILFTs using single-phase differential injection. The mathematical models are provided to prove less injection loss of the proposed ILFT due to third harmonic phase shifters.

Chapter 4 presents a novel frequency tracking loop for a sub-harmonic ILO using envelope wave when a reference pulse is injected. First, the basic concept of the proposed phase detection is described, and the behavior of the VCO envelope wave with pulse injection is explained. Then, the overall operation of the proposed frequency tracking loop is presented in detail.

Chapter 5 presents an envelope detection-based reference pulse injection time control circuit for low VCO phase noise. Particularly, an envelope detector in an ILPLL is

introduced to constantly monitor waveform distortion of the VCO's output caused by the injection pulse timing mismatch. Also, an injection time calibration method that uses the information from the envelope detector is presented.

Finally, Chapter 6 concludes with a summary of this work and points to some future research directions.

Additionally, in Appendix I, a six-phase VCO using super-harmonic coupling is presented as an example of a multiphase oscillator based on injection locking. The detailed explanation of an inductive coupling network for six-phase signal generation is provided, and its electromagnetic (EM) simulation results are included. The proposed VCO is fabricated with a 32-nm SOI CMOS technology.

## 1.6 References


[1-1] C.-F. Liang and K.-J. Hsiao, “An injection-locked ring PLL with self-aligned injection window,” in *IEEE Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2011, pp. 90–92.

[1-2] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, “A compact, low-power and low-jitter dual-loop injection locked PLL using all-digital PVT calibration,” *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan. 2014.

[1-3] J.-C. Chien et al., “A pulse-position-modulation phase-noise-reduction technique for a 2-to-16 GHz injection-locked ring oscillator in 20 nm CMOS,” in *IEEE Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2014, pp. 52–53.

[1-4] B. M. Helal, C.-M. Hsu, K. Johnson, and M. H. Perrott, “A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop,” *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.

[1-5] Y.-C. Huang and S.-I. Liu, “A 2.4-GHz sub-harmonically injection-locked PLL with self-calibrated injection timing,” *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 417–428, Feb. 2013.

[1-6] I.-T. Lee, Y.-J. Chen, S.-I. Liu, C.-P. Jou, F.-L. Hsueh, and H.-H. Hsieh, “A divider-less sub-harmonically injection-locked PLL with self-adjusted injection timing,” in *IEEE Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 414–415.

[1-7] J. Lee and H. Wang, “Study of subharmonically injection-locked PLLs,” *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

[1-8] M. Elbadry, B. Sadhu, J. X. Qiu, and R. Harjani, “Dual-channel injection-locked quadrature LO generation for a 4-GHz instantaneous bandwidth receiver at 21-GHz center frequency,” *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 3, pp. 1186–1199, Mar. 2013.

[1-9] H.-Y. Chang, Y.-L. Yeh, Y.-C. Liu, M.-H. Li, and K. Chen, “A low-jitter low-phase-noise 10-GHz sub-harmonically injection-locked PLL with self-aligned DLL in 65-nm

CMOS technology,” *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 3, pp. 543–555, Mar. 2014.

[1-10] B. Razavi, “A study of injection locking and pulling in oscillators,” *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[1-11] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol.44, no.6, pp.428,435, Jun 1997.

[1-12] H. Noguchi, et al., "A 40-Gb/s CDR circuit with adaptive decision-point control based on eye-opening monitor feedback," *IEEE J. Solid-State Circuits*, vol.43, no.12, pp.2929,2938, Dec. 2008.

[1-13] H. Krishnaswamy, and H. Hashemi, "Effect of process mismatches on integrated CMOS phased arrays based on multiphase tuned ring oscillators," *IEEE Trans. Microw. Theory Techn.*, vol.56, no.6, pp.1305,1315, June 2008.

[1-14] C.-H. Park, O. Kim, and B. Kim, "A 1.8-GHz self-calibrated phase-locked loop with precise I/Q matching," *IEEE J. Solid-State Circuits*, vol.36, no.5, pp.777,783, May 2001.

[1-15] H.-S. Chen; L.-H. Lu, "An open-loop half-quadrature hybrid for multiphase signals generation," *IEEE Trans. Microw. Theory Techn.*, vol.60, no.1, pp.131,138, Jan. 2012.

[1-16] S. L. J. Gierkink, et al., “A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling,” *IEEE J. of Solid-State Circuits*, vol. 38, no. 7, pp. 1148-1154, July 2003.

[1-17] D. Shin, S. Raman, and K.-J. Koh, “A 0.6-V, 30-GHz six-phase VCO with superharmonic coupling in 32-nm SOI CMOS technology,” in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, 2015.

[1-18] W. Deng et al., “A sub-harmonic injection-locked quadrature frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers,” *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1710–1720, Jul. 2013.

[1-19] D. Shin, S. Raman, and K.-J. Koh, “A mixed-mode injection frequency-locked loop for self-calibration of injection locking range and phase noise in 0.13μm CMOS,” in *IEEE Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2016, pp. 50–52.

# Chapter 2.

# A Mixed-Mode Injection Frequency-Locked Loop for Self-Calibration of Injection Locking Range and Phase Noise in 0.13μm CMOS

## 2.1 Introduction

Recently, an nth-harmonic injection-locked oscillator (ILO) has been widely used in several millimeter-wave applications [2-1]-[2-2]. The conventional frequency synthesizer usually requires the implementation of the high-frequency divider like an injection-locked frequency divider [2-3] or Miller divider [2-4]. However, at high frequencies, multiple dividers may be required because their division ratio is very low. In addition, their narrowband characteristic demands higher injection power from the VCO. The extra buffer between the VCO and the divider is required to achieve a wider locking range for the divider. Thus, the power consumption would be increased. On the other hand, the *n*th-harmonic ILO has nothing with which to implement the high frequency divider since the VCO output, one-nth frequency of ILO output, can be directly connected to the CML or digital dividers with wide operating range and low power consumption.

In general, it is very difficult for a design of differential or quadrature VCO for a frequency synthesizer to attain a low phase noise performance. This is because the quality factor of varctors degrades as the desired frequency increases. On the other hand, an *n*th-

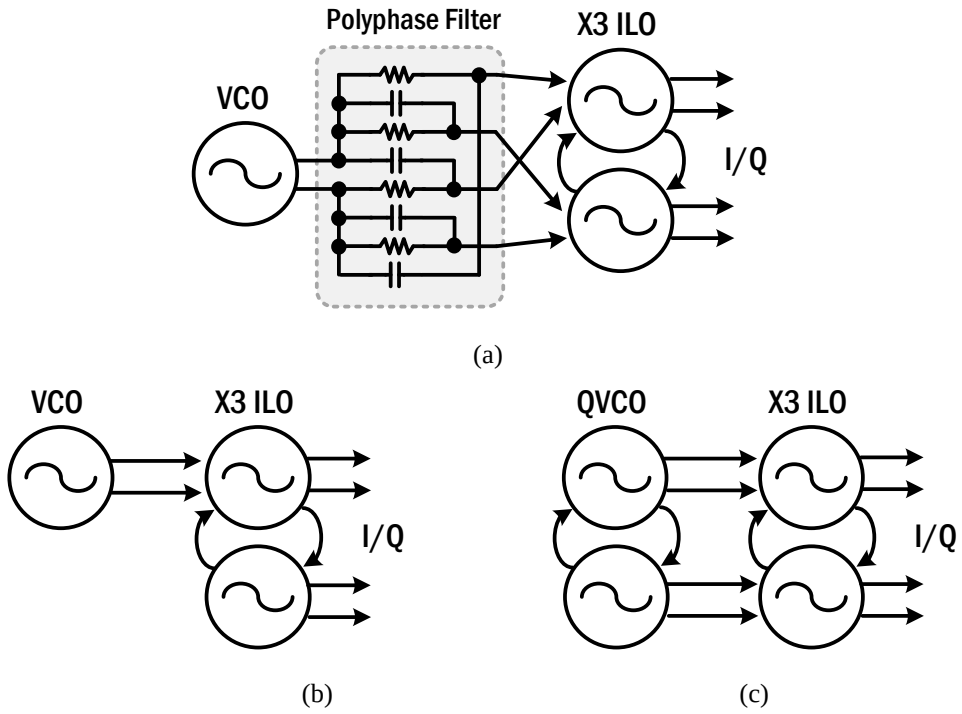



Fig. 2-1. Three approaches for QILO: (a) quadrature injection using PPF, (b) single-sided injection, and (c) quadrature injection using QVCO.

harmonic ILO can generate a low phase noise signal. In the frequency synthesizer using the ILO, a low frequency injection signal is generated by a differential or quadrature VCO having low phase noise with a high quality factor of its varactor. When the nth-harmonic of the injection signal is applied to the ILO and then it is locked, the ILO has the phase noise of the injection signal degraded by $20\log_{10}(n)$. In the case of quadrature ILO, it consists of injection transistors and two LC tanks that are cross-coupled each other. In general, the QILO has low phase noise following that of injection signal. However, it has very narrow locking range, and its phase accuracy depends on phase accuracy of injection signals. There are three typical approaches available when it comes to generating injection signals for QILO as shown in Fig. 2-1. The first approach would be to use an I/Q poly-phase filter (PPF), where a differential VCO is connected in Fig. 2-1(a). For example, in a 60-GHz third-harmonic QILO [2-5], the QILO adopts I/Q PPF to generate quadrature signals for injection locking. These signals are injected into each cell of the tripler. Hence, with 20-GHz injection

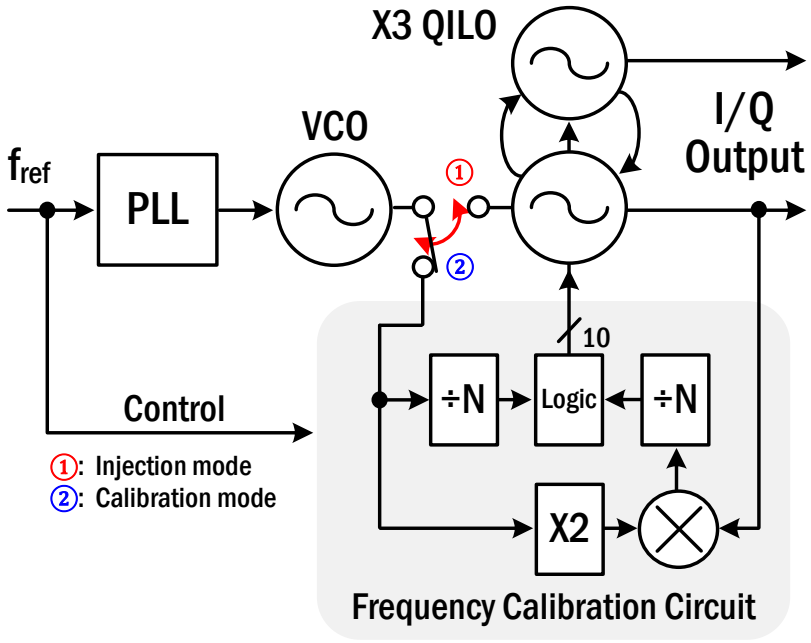



Fig. 2-2. Prior frequency calibration circuit for QILO.

signals, the QILO generates 60-GHz quadrature signals. Since the QILO uses quadrature injection signals, low quality factor of the tank and very low oscillation current for wide injection locking, it can achieve a wide locking range, from 56 to 65 GHz. However, the phase error between injection I/Q signals leads to serious phase error between I/Q signals of the tripler. Moreover, its small output power requires large conversion gain buffer.

In order to reduce phase error due to injection signals, another approach for the QILO is proposed in [2-6]. Differential outputs of VCO are injected into only one of the LC tanks in the QILO as shown in Fig. 2-1(b). The single injection could eliminate the drawbacks of QILO using the PPF. Generally, since the locking range of single injection becomes smaller than that of multiple signal injection, the QILO uses a dual injection scheme of the LC tank. However, even the dual injection scheme cannot achieve wider injection locking range than that of multiple signal injection. The last approach is to apply quadrature signals of a QVCO into a QILO. Although it may cause area and power consumption to increase, it may be the best way to have low phase noise and phase accuracy at the same time.

In spite of many efforts to improve the locking range of ILOs, their locking ranges are still very narrow. In order to achieve a wider locking range, an ILO frequency calibration circuit is proposed in [2-7]. The calibration circuit contains a frequency doubler, a mixer, two dividers, and a digital control circuit as shown in Fig 2-2. The doubler outputs a signal with twice the frequency of the injection signal. Then, it is mixed with a free-running signal of the ILO. The output of the mixer passed through a divider is compared to the injection signal divided by *N*. If a phase difference exists, the calibration circuit carries out an operation to match the free-running frequency of the ILO with three times the frequency of the injection signal. Hence, the ILO is injection-locked by tracking the injection frequency. However, the calibration circuit must have design complexity and large area to achieve a wide locking range. Furthermore, it requires an external control signal and long locking time to complete the calibration.

In order to achieve a wide locking range without the large burden of a conventional calibration circuit, this paper proposes a novel calibration technique. It carries out exact self-calibration without the extra control signals and time. With a simpler calibration method, it occupies a small area. In addition, in our work, a dual coupled QVCO is used to achieve low phase noise and phase accuracy. This contribution is organized as follows. Chapter 2.2 introduces overall architecture of the LO signal generator. Chapter 2.3 describes the proposed injection frequency-locked loop in detail. Lastly, Chapter 2.4 presents the experimental results.

## 2.2 Overall Architecture

Fig. 2-3 shows the block diagram of the proposed QVCO and QILO with injection frequency-locked loop (IFLL). The QVCO generates 8.8-10 GHz quadrature signals and injects them into the QILO which is third-harmonically locked and outputs 26.4-30 GHz quadrature signals. The QVCO generally generates low phase noise signal because the QILO follows the phase noise of the QVCO. The IFLL calibrates the injection-locking range of the QILO.

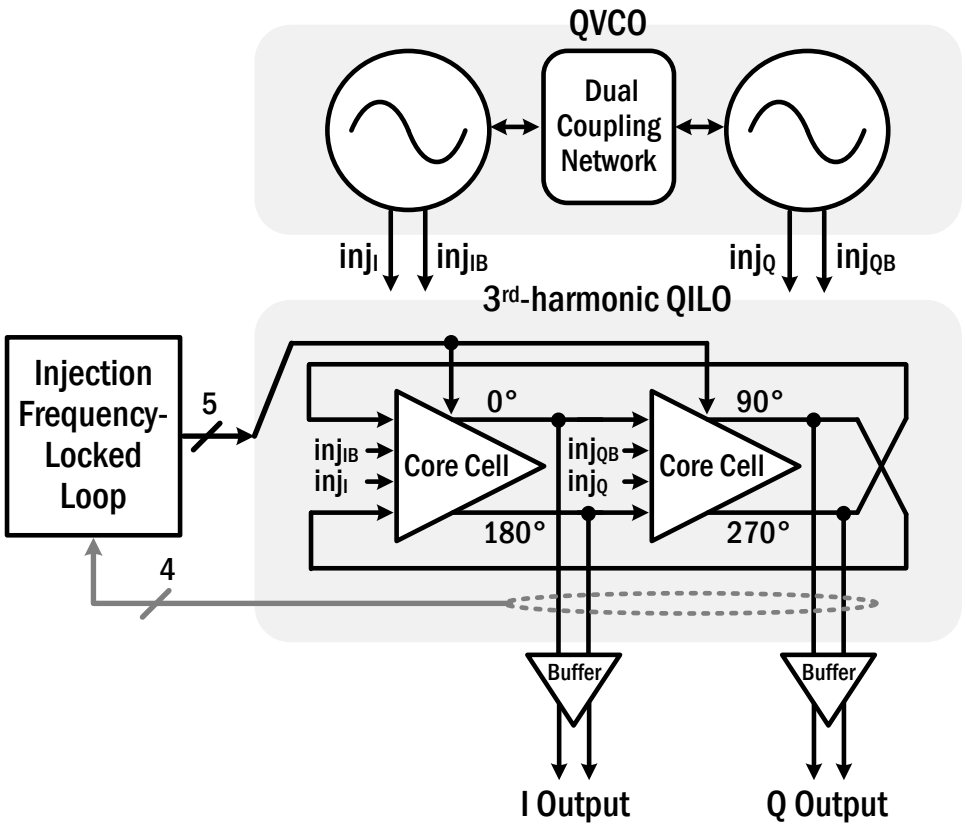



Fig. 2-3. Block diagram of the proposed QVCO and QILO with injection frequency-locked loop.

As shown in Fig. 2-4, the QILO employs two identical oscillators that consist of coupling transistors, 5-bit switched-C array, LC tank and injection transistors. Quadrature signals are utilized for injection locking to achieve wide injection-locking range compared to single-side injection. Therefore, the bit number of switched-C array can be optimized for wide frequency calibration and I/Q phase accuracy can be improved. The QILO utilizes the third-harmonic of the injection current to establish frequency locking with injection-locking range typically less than 3% due to a relatively small injection power of the third-harmonic compared with that of the fundamental. For calibration of the injection-locking range, the IFLL outputs the 5-bit control signals after locking status detection. These control signals are applied to the 5-bit switched-C array of each core cell in the QILO to adjust free-running frequency of the QILO. The current consumption of each core cell is 8 mA with a supply voltage of 1.3 V.

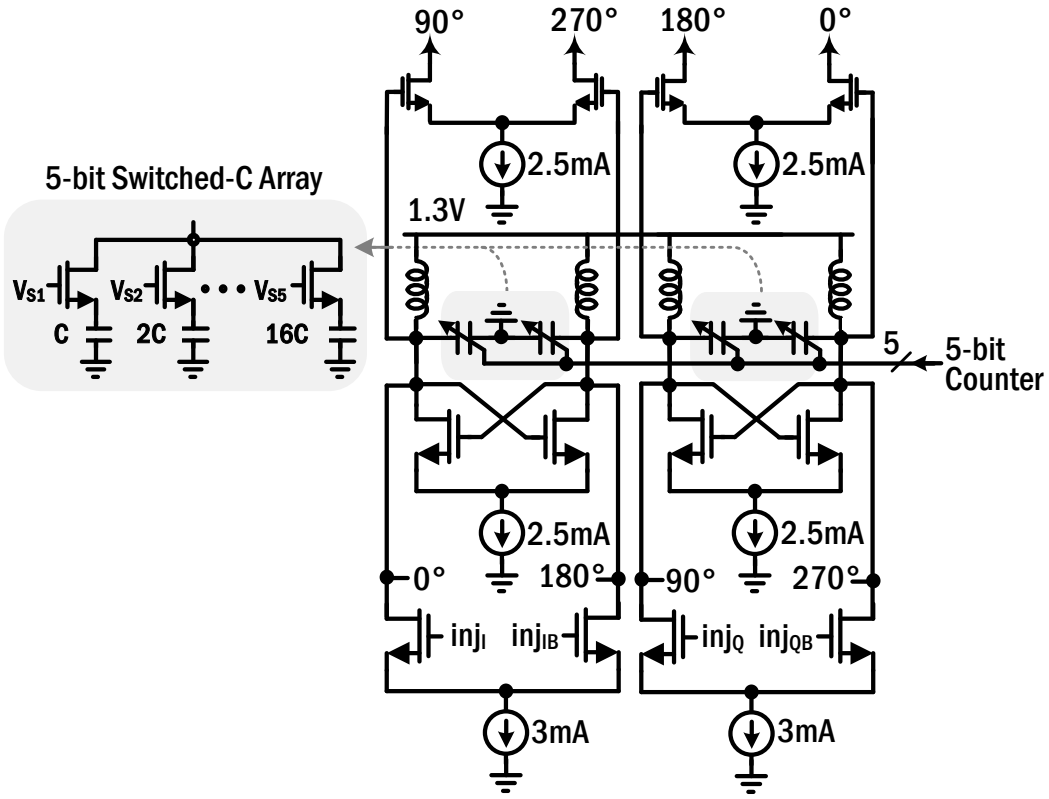
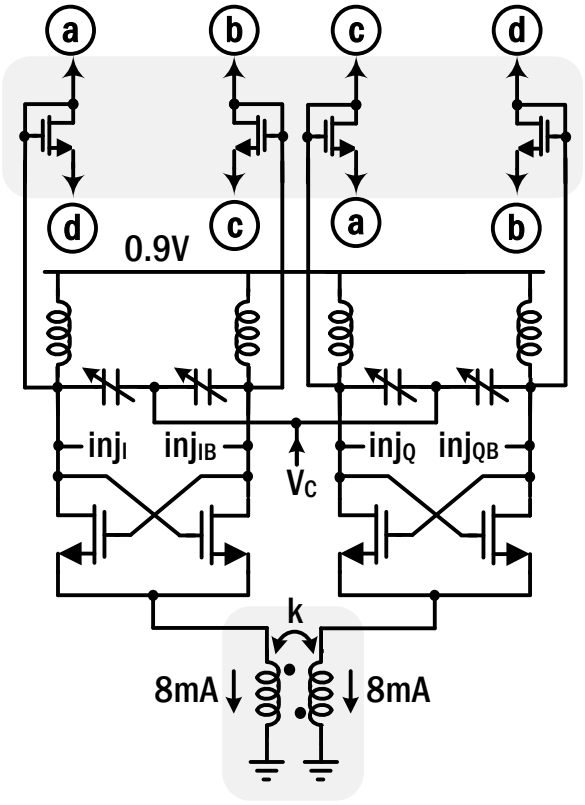
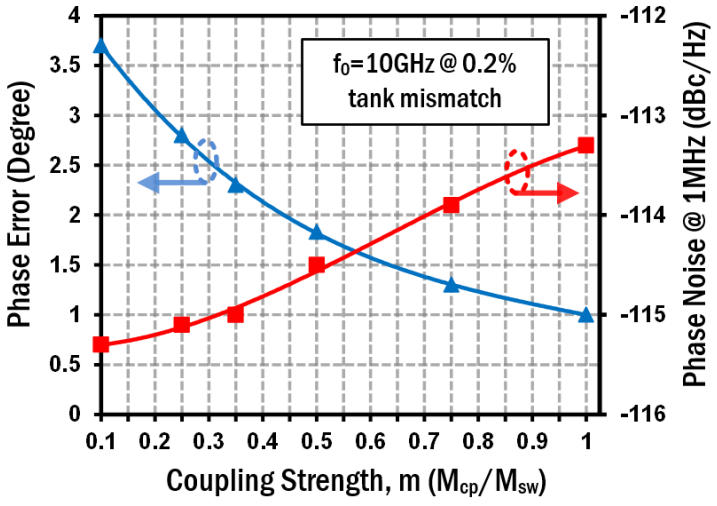



Fig. 2-4. Schematic of QILO.

For quadrature outputs of the QILO, the VCO in the frequency synthesizer usually provides quadrature injection signals to QILO. In this work, a dual coupled QVCO is adopted to provide lower phase noise with less I/Q phase error as shown in Fig. 2-5(a). The dual coupled QVCO employs a super-harmonic inductive coupling (SHC) [2-8] and symmetric in-phase injection-coupling (IPIC) [2-9]. Although the SHC requires additional area for the tail transformer, it can achieve low phase noise compared with other coupling types. However, it may have poor phase accuracy due to mismatch between two LC tanks. Moreover, it usually requires an auxiliary coupling network to provide directivity to the quadrature phase relations. The auxiliary network may cause the phase noise of the QVCO to be degraded. However, in the QILO, I/Q directivity of injection signals is very important for injection locking because uncertain I/Q directivity causes the QILO to fail to lock even at an injection frequency equal to the QILO free-running frequency. On the other hand, an IPIC has good phase accuracy, but there is a tradeoff between phase accuracy and phase




(a)




(b)

Fig. 2-5. QVCO: (a) schematic and (b) simulation results.

noise. Consequently, the use of a dual coupled QVCO maximizes the merits of both SHC- and IPIC- QVCOs. Fig. 2-5(b) shows the simulated phase noise and phase error of a dual

coupled QVCO with 0.2% tank mismatch according to coupling strength, m ($M_{cp}/M_{sw}$). Like the property of IPIC, as the coupling strength increases, the phase noise becomes worse, while the phase error decreases. Using an SHC, it has lower phase noise by approximately 2dB than when using a standalone IPIC-QVCO. In our design, the coupling strength is chosen as 0.35 to ensure lower phase noise and reasonable phase error. Each LC tank consumes 8 mA with a supply voltage of 0.9 V.

## 2.3 Proposed Injection Frequency-Locked Loop

In general, the output signal of an ILO incurs fluctuation of phase and amplitude of the output signals under injection-pulling. The proposed IFLL utilizes the amplitude fluctuation to detect injection-locking status. Then, it calibrates the free-running frequency of a QILO by extracting an envelope wave of unlocked signal due to the injection-pulling. Fig.2-6 shows an overall block diagram of the mixed-mode IFLL for the injection-locking range calibration of the QILO. The calibration of the locking range primarily relies on the frequency detection or FM-to-AM conversion capability of the QILO [2-10]: when the third-harmonic of the injection signal, $3f_{inj}$, deviates out of the intrinsic locking range from the free-running frequency of the QILO, the QILO starts to loose lock and produces an AM and PM modulated signal of which AM modulation frequency ($f_{AM}$) is proportional to [2-111]

$$\sqrt{\left( f_{osc} + 3 f_{inj} \right)^2 - \left( \frac{\Delta f_L}{2} \right)^2} \tag{2-1}$$

where $f_{osc}$ is the free-running frequency of the QILO and $\Delta f_L$ is the locking range of the QILO. In the IFLL, the AM modulated signal is demodulated using the envelope detector followed by rail-to-rail amplification through the five-stage feedback-inverter amplifier chain to generate a pulse signal.

The pulse signal is then fed to both the lock detector and update-controller to be processed further in a digital domain and to create a feedback signal that controls the amount of capacitance in the switched-C array such that the QILO can track the injection frequency,

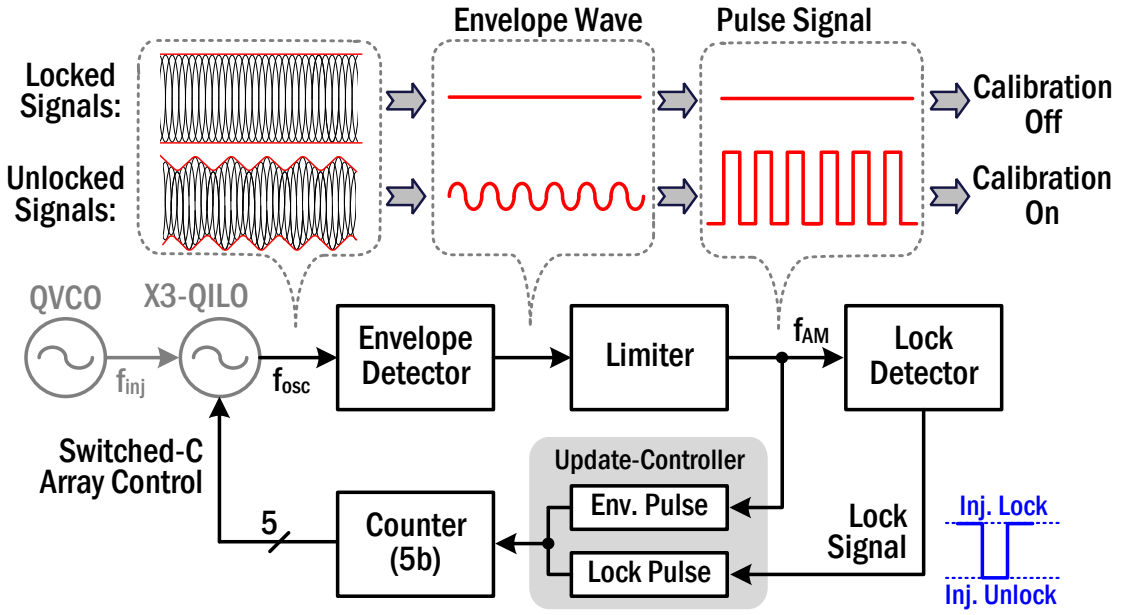



Fig. 2-6. Overall block diagram of mixed-mode IFLL.

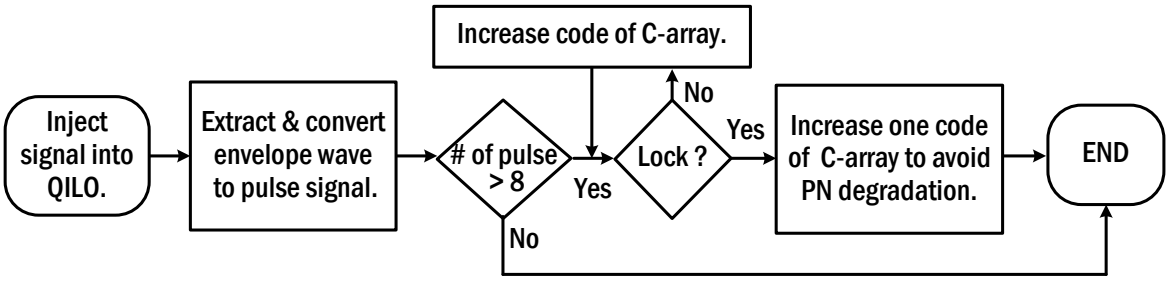



Fig. 2-7. Flowchart of overall calibration procedure.

calibrating locking range and therefore limiting the locking range only by the tuning range of the QILO. When unlocked, the lock detector after counting 8 consecutive pulses enables the upper path of the update-controller. Consequently, the 5-bit counter increases the LC tank capacitance by 1-LSB capacitance (ΔC) in the switched-C array, decreasing the free-running frequency of the QILO by Δf corresponding to the ΔC change. When locked, the lock detector outputs a lock signal which disables the update path. When locked at the edge

of the locking range, the phase noise degradation of QILO is significant. Thus, as a final step in the calibration, the lower path in the update-controller creates one more pulse to increase the LC tank capacitance by 1-LSB $\Delta C$ more, thereby preventing the phase noise degradation at the edge of the locking range. The flowchart of overall calibration procedure is shown in Fig. 2-7. By using the envelope wave of output signals as a control signal for the calibration circuit, the proposed calibration scheme does not require externally or internally generated signals to control its operation.

When the output of the QVCO, $f_{inj}$ is 9.43 GHz and initial free-running frequency of the QILO, $f_{osc}$ is 30.1 GHz, Fig. 2-8 shows typical transient simulation results at each designated node of the IFLL. The envelope magnitude is a nonlinear function of $f_{AM}$ and due to the far distance between $3f_{inj}$ and $f_{osc}$, the QILO is unlocked and output envelope magnitude is small (less than 50 $mV_{pp}$) at the beginning of the calibration, <20 ns in Fig. 2-9 ① and ②. However, the limiter produces rail-to-rail pulses due to a large gain, more than 60 dB at $f_{AM}$=1.8 GHz, in Fig. 2-8 ③ and initiates the frequency calibration, decreasing fosc to 28.3 GHz ($3f_{inj}$) progressively in a nonlinear fashion as the switched-C array code is being updated per every eight clock cycle of $f_{AM}$ in Fig. 2-8 ⑤. When $f_{osc}$ approaches toward the edge of the locking range (300 MHz) at around 130 ns, the AM-modulation effect in the QILO output becomes more prominent in the sub window in Fig. 2-8 ① and after eight pulses the feedback counter updates the switched-C array code to 01100, locking the QILO to the QVCO at the edge of the locking range. Subsequently, after locking the Q-pump starts to charge $C_I$ creating a lock signal which pushes one more LSB code up to 01101 at around 175 ns in Fig. 2-8 ④ and ⑤, pushing $f_{osc}$ closer to 28.3 GHz to calibrate phase noise in Fig. 2-8 ①. Note that the 8-bit SR acts as a pulse filter, requiring eight consecutive pulses to drive the Q-pump; for instance, due to a brief transient waveform uncertainty there are bursts of irregular pulses after locking, which are however ignored by the pulse filter.

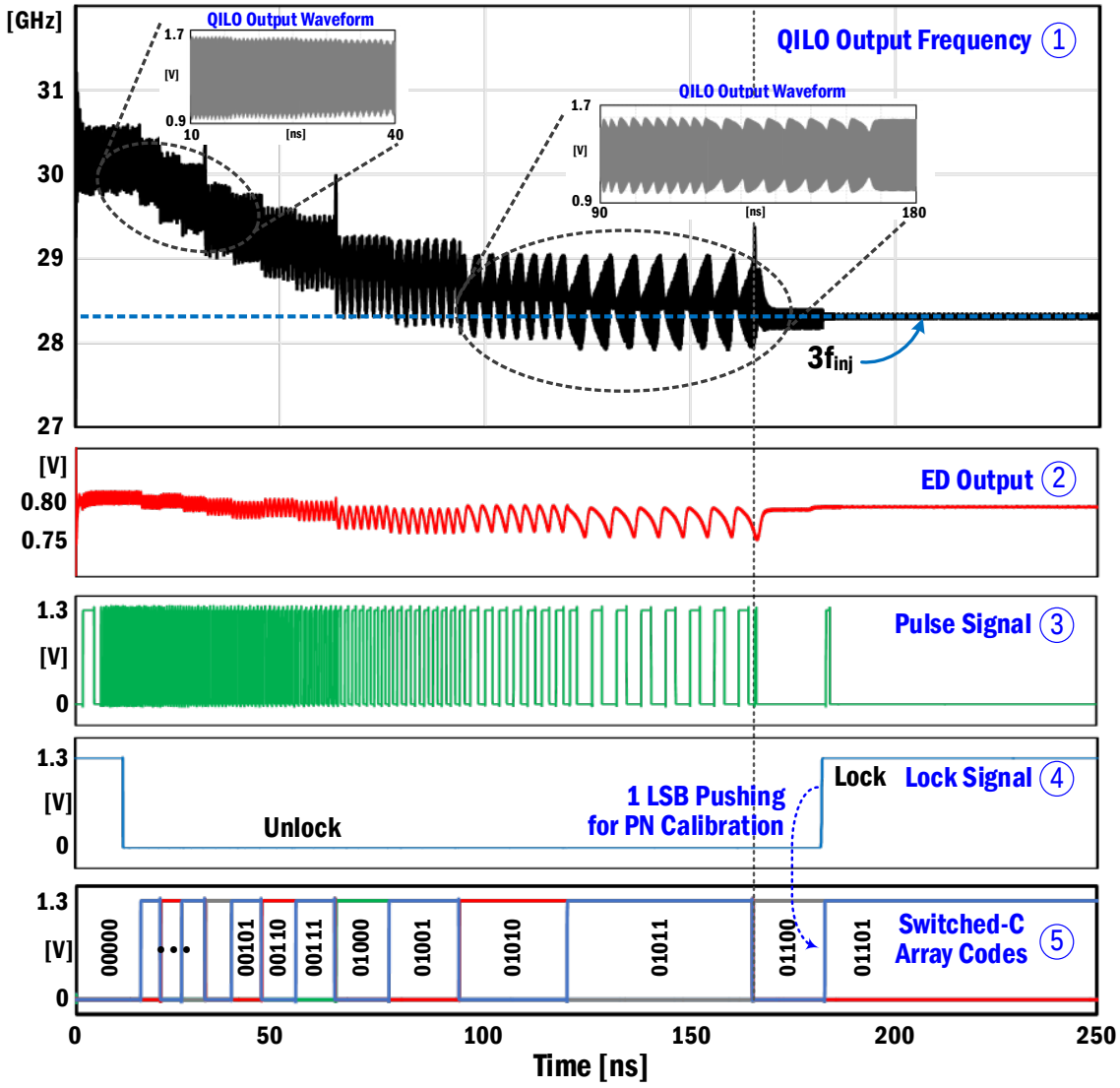



Fig. 2-8. Typical transient simulation results at each designated node of the IFLL.

### 2.3.1 Phase Noise Calibration

As mentioned earlier, a typical third-harmonic ILO should have phase noise more than 9.5 dB as much as that of injection signals. However, the phase noise at the edges of the locking range becomes more degraded because the phase noise from the self-oscillating signal of the ILO is dominant in total phase noise. Therefore, its effective locking range becomes narrow due to this degradation. Considering the trade-off between output swings and locking range of the ILO, the effective locking range is generally approximately 0.6 of the typical locking range as reported in [2-6]. In order to avoid the phase noise degradation at the edges, the proposed IFLL has utilized a control method that makes the free-running frequency of the ILO, $f_{osc}$, move into the center of the effective locking range. For example, let us assume that the QILO is unlocked and the injection-locking range, $\Delta f_L$, approximately equals to 3-LSB of the switched-C array as shown in Fig. 2-9(a). Starting the calibration circuit, $f_{osc}$ can be moved close to $3f_{inj}$ in the locking range due to a change of capacitance of the QILO. As shown in Fig. 2-9(b), in the worst case, the QILO may be locked at the edge of locking range, which has lots of degradation of phase noise so much more than 9.5dB when there is phase noise degradation within 40% of $\Delta f_L$. The maximum amount of the degradation in phase noise would be the same as the phase noise difference between $f_{inj}$ and $f_{osc}$. To avoid such degradation, that is, to lock within the effective locking range, the update controller carries out one more LSB update of the switched-C array after injection locking due to IFLL. Consequently, $f_{osc}$ can move into the effective $\Delta f_L$ and the QILO no longer incur the degradation of phase noise more than 9.5 dB as shown in Fig. 2-9(c). In order to utilize this method in our work, the relation between $\Delta f_L$ and 1-LSB ($\Delta f$) of the switched-C array should meet the following conditions. Fig. 2-10 shows two failure cases of phase noise calibration when the frequency resolution $\Delta f$ is smaller or larger than the requirement. In the case of $\Delta f < 0.2\Delta f_L + f_{AM,MIN}$, where $f_{AM,MIN}$ is the minimum detectable frequency of the envelope detector and limiter, the phase noise after frequency calibration is degraded more than 9.5 dB even though extra one $\Delta f$ is shifted to avoid the phase noise degradation at the

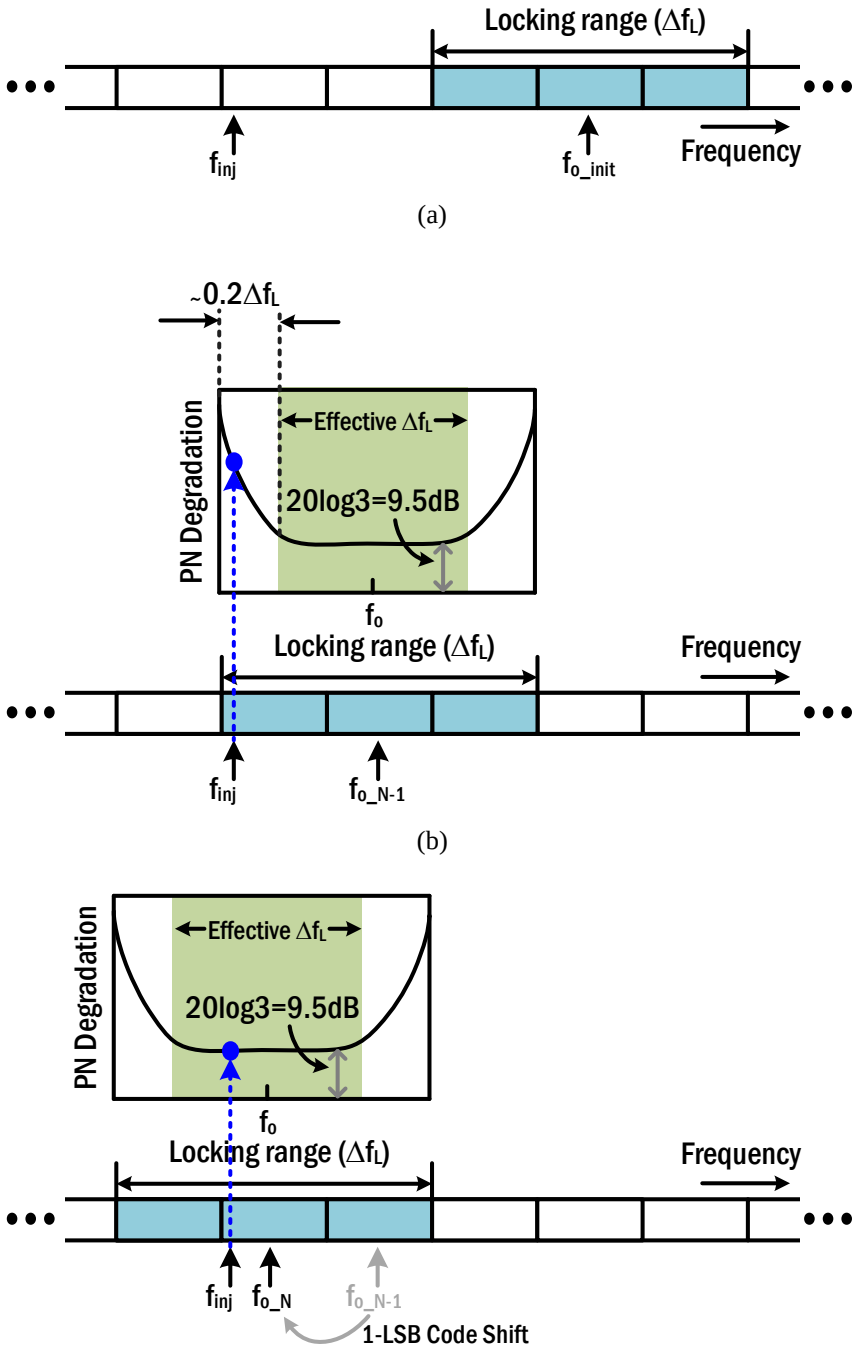



Fig. 2-9. Concept to avoid phase noise degradation at the edge of locking range: (a) before IFLL, (b) a case of phase noise degradation within locking range, and (c) after phase noise calibration.

edge of $\Delta f_L$ as shown in Fig. 2-10(a). Also, when $\Delta f > 0.5(0.8\Delta f_L + f_{AM,MIN})$ in Fig. 2-10(b),

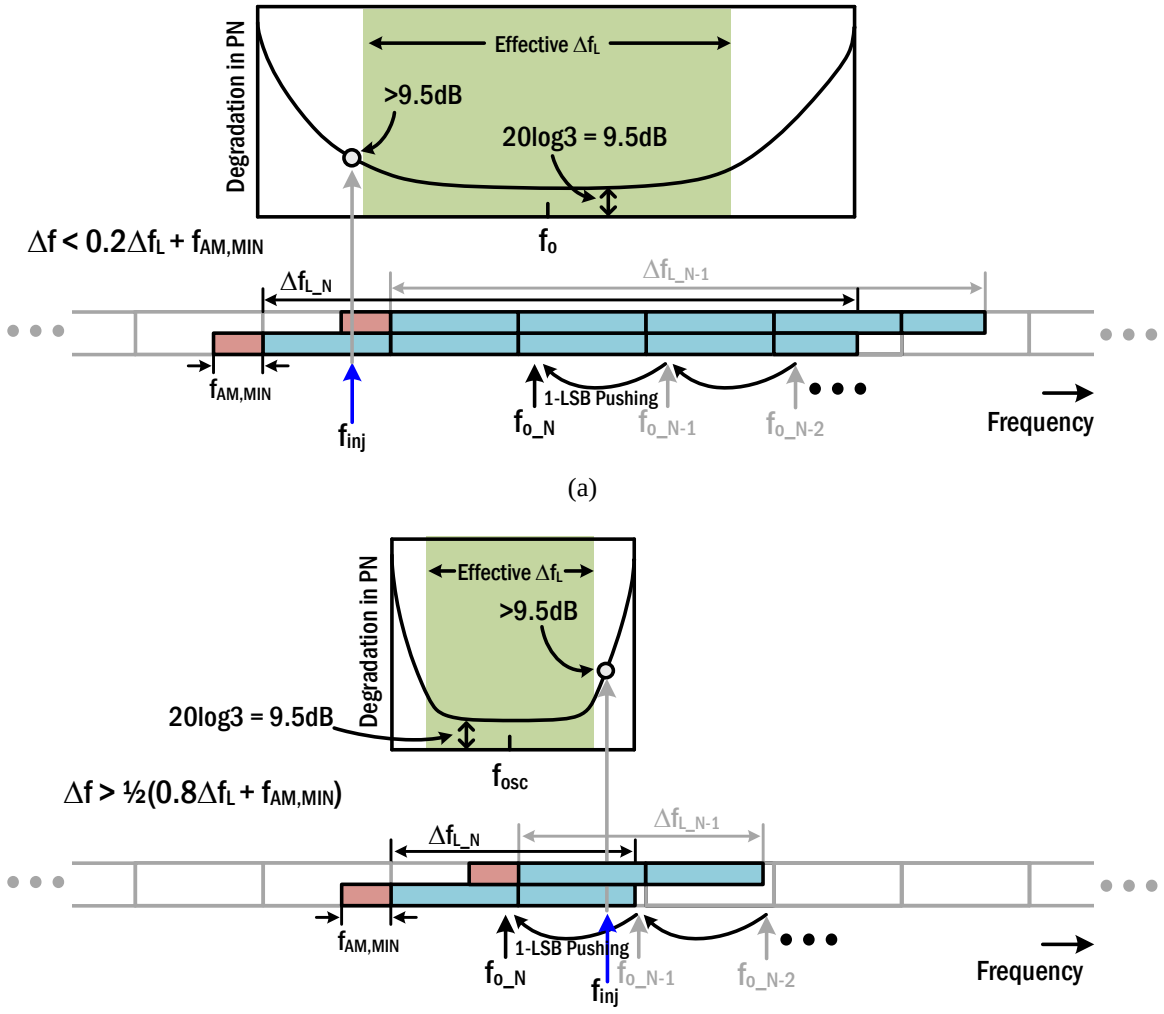



Fig. 2-10. Two failure cases of phase noise calibration when the frequency resolution Δf is (a) smaller and (b) larger than the requirement.

the phase noise degradation more than 9.5 dB would be incurred despite the additional one Δf pushing. Thus, based on two cases, the Δf of switched-C array can be expressed as

$$f_{AM,MIN} + 0.2 \cdot \Delta f_L \le \Delta f \le 0.5(f_{AM,MIN} + 0.8 \cdot \Delta f). \quad (2\text{-}2)$$

In this work, setting Δf with (2-2), the QILO is locked within the effective locking range (~$0.6 \cdot \Delta f_L$) despite its slight variation in natural frequency, process, temperature, etc.

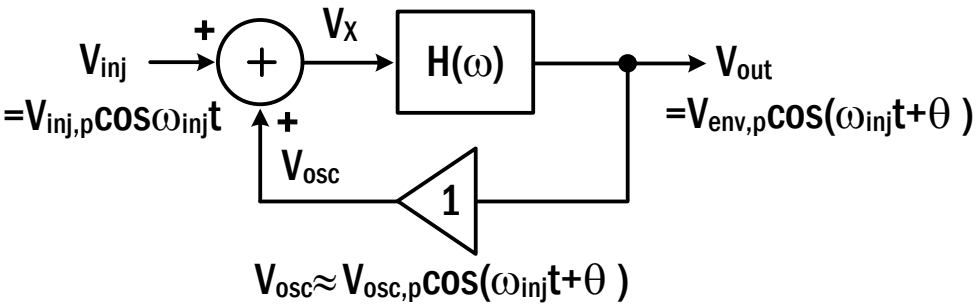



Fig. 2-11. LC oscillator under injection.

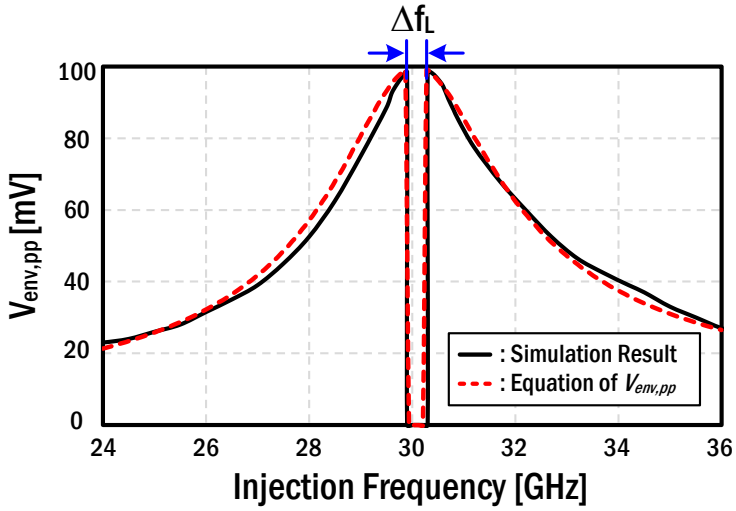



Fig. 2-12. Peak-to-peak amplitude of envelope wave according to injection frequency.

### 2.3.2 Envelope Wave under Injection Pulling

To determine the gain of the envelope detector and limiter, the envelope wave of the ILO output should be mathematically calculated. Referring to [2-11] for brief analysis, let us suppose that the oscillator is under injection and the envelope wave would be limited by feeding amplifier, as shown in Fig 2-11. First, a signal, $V_X$ can be written as

$$V_X = V_{inj,p}\cos\omega_{inj}t + V_{osc,p}\cos\left(\omega_{inj}t+\theta\right). \tag{2-3}$$

After passing through transfer function, $H(\omega)$, $V_{out}$ can be expressed as a cosine with a phase shift

$$\begin{aligned} V_{out} &= V_{inj,p} H(\omega_{inj}) \cos \omega_{inj} t + V_{osc,p} H(\omega_{inj} + \frac{d\theta}{dt}) \cos\left(\omega_{inj} t + \theta\right) \\ &= \frac{\beta V_{inj,p} + \alpha V_{osc,p} \cos\theta}{\cos\psi} \cos\left(\omega_{inj} t + \psi + \phi\right) \\ &= \sqrt{\alpha^2 V_{osc,p}^2 + \beta^2 V_{inj,p}^2 + 2\alpha\beta V_{inj,p} V_{osc,p} \cos\theta} \cos\left(\omega_{inj} t + \psi + \phi\right) \end{aligned} \tag{2-4}$$

where

$$\theta = \psi + \phi, \;\; \alpha = H(\omega_{inj} + \frac{d\theta}{dt}), \;\; \beta = H(\omega_{inj}),$$
$$\tan\psi = \frac{\alpha V_{osc,p} \sin\theta}{\beta V_{inj,p} + \alpha V_{osc,p} \cos\theta}.$$

In [2-11], $\theta$ is expressed as

$$\tan\frac{\theta}{2} = \frac{\omega_L}{\omega_{osc} - \omega_{inj}} + \frac{\omega_b}{\omega_{osc} - \omega_{inj}} \tan\frac{\omega_b t}{2} \tag{2-5}$$

where $\omega_L = 2\pi \cdot \Delta f_L / 2$ and $\omega_b = \sqrt{\left(\omega_{osc} - \omega_{inj}\right)^2 - \omega_L^2}$.

Considering the amplitude variation of $V_{out}$ due to $\theta$, the envelope wave can be calculated from (2-4). The peak amplitude of the output, $V_{env,p}$ can be written as

$$V_{env,p} = \sqrt{\alpha^2 V_{osc,p}^2 + \beta^2 V_{inj,p}^2 + 2\alpha\beta V_{inj,p} V_{osc,p} \cos\theta}\,. \tag{2-6}$$

If $\omega_{osc}$ is very close to $\omega_{inj}$ and $d\theta/dt$=0, the ILO will be locked and $V_{env,p}$ has constant value. On the other hand, if $\omega_{osc}$ is near $\omega_{inj}$ and $d\theta/dt \neq 0$, it will be unlocked (called quasi-lock) and $V_{env,p}$ will be affected by impedance variation of the LC tank. Therefore, $\alpha$ varies with the frequency variation from $\omega_{osc}+\omega_L$ to $\omega_{inj}$. Considering that the maximum and minimum impedance in [2-11] occur at approximately $\omega_{osc}$ and $\omega_{osc}+\omega_L$, respectively, a peak-to-peak amplitude of envelope wave from (2-6) can be approximated as

$$V_{env,pp} \approx (1-\alpha)\cdot V_{osc,p} + (1+\alpha)\cdot \beta V_{inj,p}\,. \tag{2-7}$$

On the other hand, as $\omega_{inj}$ deviates farther from $\omega_{osc}$, $\omega_b$ approximates $\omega_{osc}-\omega_{inj}$. Since the frequency of $V_{out}$ approximates free-running frequency, $\omega_{osc}$, the $V_{env,p}$ is mainly affected by $\theta$ which equals $\omega_b$. Therefore, from (2-6), minimum and maximum values of $V_{env,p}$ due to $\theta$. can be calculated. By subtracting minimum $V_{env,p}$ from maximum $V_{env,p}$, the peak-to-peak amplitude can be calculated and simply expressed as

$$V_{env,pp} \approx 2\beta V_{inj,p}\,. \tag{2-8}$$

The amplitudes of the envelope wave from simulation and equation are plotted in Fig. 2-12 when $Q$ = 10, $L$ = 100 pH, $C$ = 280 fF, and $\Delta f_L$ = 0.38 GHz.

### 2.3.3 Locking Time Analysis of IFLL

The previous calibration circuit in [2-7] requires several microseconds to complete the frequency calibration loop because loop update frequency is 2.4 MHz, that is, its update period is approximately 410 ns. Therefore, the additional time for frequency calibration should be allocated in the frequency synthesizer. On the other hand, the proposed IFLL requires less than 300 ns to complete the calibration. In this chapter, the locking time of the proposed scheme will be estimated by two loop models (transient and linear models).

Fig. 2-13 shows a loop model of the IFLL to estimate total locking time. The envelope detector outputs frequency modulation of the QILO due to injection-pulling. Based on the operational principle of the IFLL, the frequency of the envelope wave determines loop update period during the calibration. The frequency of $n$-th envelope wave, $f_{AM,n}$ is expressed as

$$f_{AM,n} = \sqrt{(f_{osc} - 3\cdot f_{inj} + (1-n)\cdot \Delta f)^2 - (0.5\cdot \Delta f_L)^2}\,. \tag{2-9}$$

One LSB of the switched-C array, $\Delta f$, is subtracted from the free-running frequency of QILO, $f_{osc}$, every $M$-times envelope period ($M/f_{AM,n}$) until the calibration finishes, where $M$ is a number of division to filter out some irregular pules (in this work, $M$ is set to 8). By

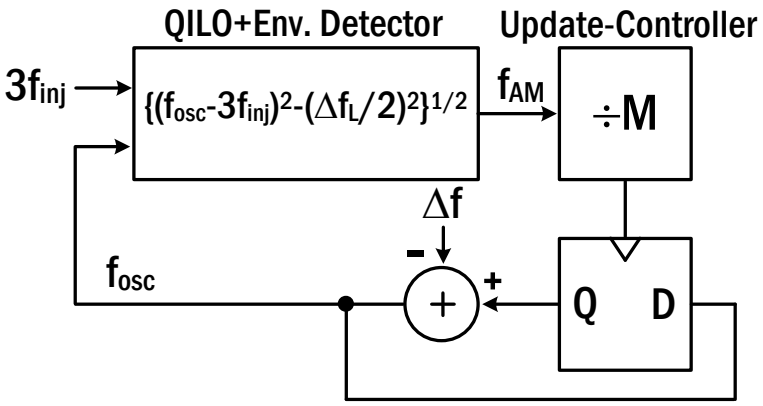



Fig. 2-13. Loop modelling of IFLL to estimate locking time.

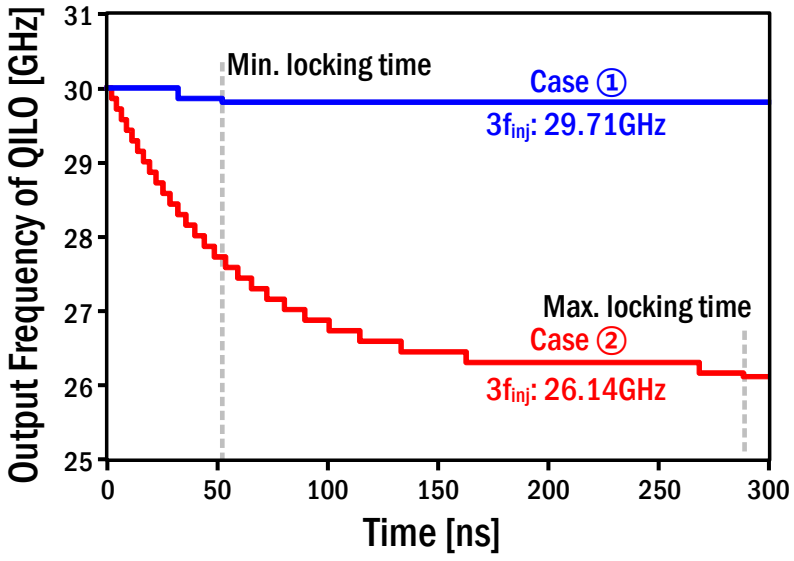



Fig. 2-14. Minimum and maximum locking time based on Fig. 2-13.

accumulating every *M*-times envelope period, the total locking time can be defined by the following equation:

$$t_{locking} = t_{disch} + \sum_{k=1}^{k=N} \frac{M}{\sqrt{(f_{osc} - 3\cdot f_{inj} + (1-k)\cdot \Delta f)^2 - (0.5\cdot \Delta f_L)^2}},$$

$$N = \left\lfloor \frac{f_{osc} - (3\cdot f_{inj} + 0.5\cdot \Delta f_L)}{\Delta f} \right\rfloor + 1 \qquad (2\text{-}10)$$

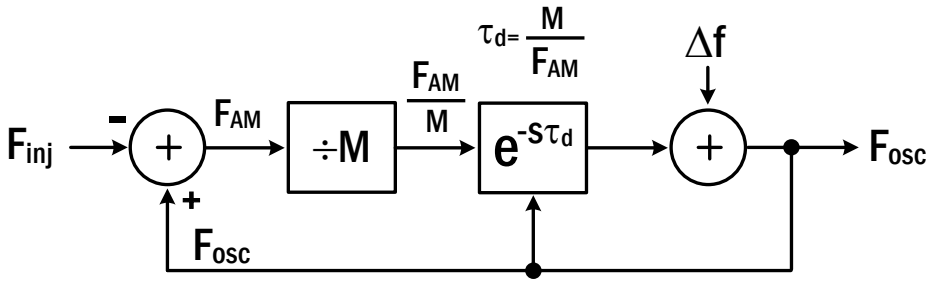
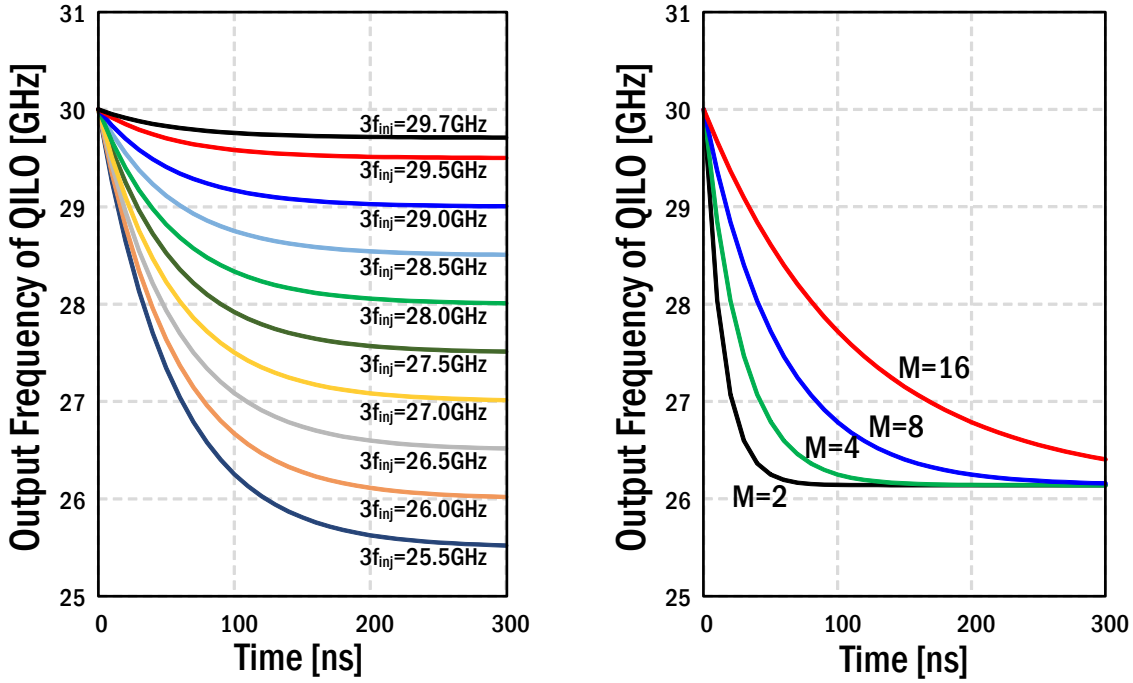



Fig. 2-15. Linear loop modelling of IFLL.




(a) (b)

Fig. 2-16. Locking time estimation according to (a) injection frequency and (b) M.

where $t_{disch}$ is a discharging time of the Q-pump due to the injection-unlocked signal and $N$ is a number of IFLL update. From (2-10), minimum and maximum locking time of the IFLL can be estimated as shown in Fig. 2-14. For minimum locking time, the IFLL should update only 1-LSB of the switched-C array from injection-pulling, where first $f_{AM}$ should be as high as possible, and then perform 1-LSB update more for phase noise calibration. When the initial $f_{osc}$ = 30 GHz, $t_{disch}$ =20 ns, $\Delta f_L$ = 300 MHz, $\Delta f$ = 142 MHz and $3f_{inj}$ = 29.71 GHz, the

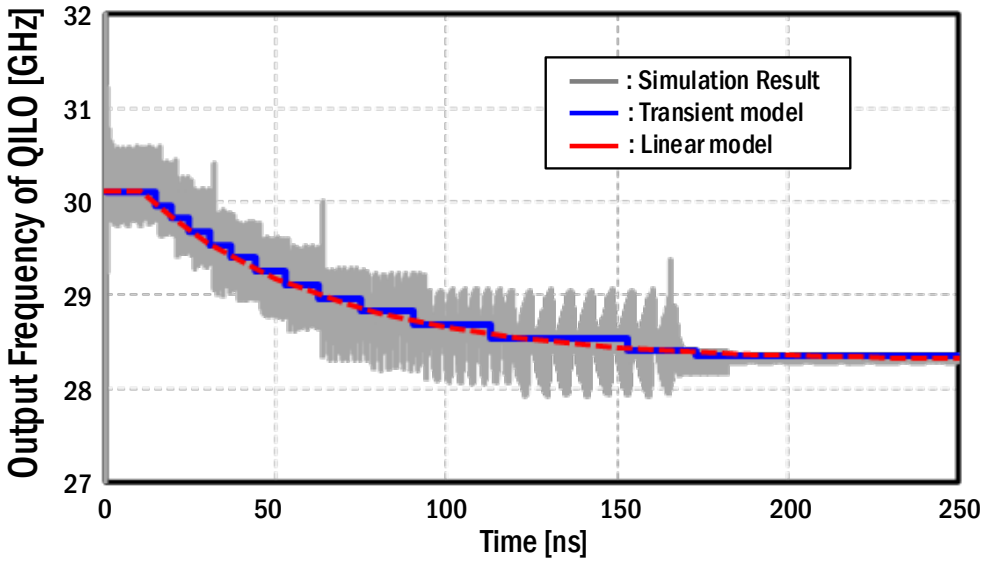



Fig. 2-17. Comparison of transient model analysis, linear model analysis, and SPECTRE simulation for injection-locking procedure.

estimated minimum locking time is 52 ns. For minimum locking time, the last $f_{AM}$ should be low as possible. On the other hand, when $3f_{inj}$ = 26.14 GHz, the estimated maximum locking time is 285 ns. As a result, the IFLL locking time from (2-10) absolutely depends on a period of $f_{AM}$ at the last step of the loop.

Also, the locking time can be calculated by analyzing another loop model of the IFLL for linearization as shown in Fig. 2-15. First, the step frequency Δf of the switched-C array can be expressed as

$$\Delta f = F_{osc} - e^{-s\tau_d} F_{osc} \tag{2-11}$$

where $\tau_d = M/F_{AM}$. Since $e^{-s\tau_d} \approx 1 - s\tau_d$, (2-11) can be linearized as

$$\Delta f = F_{osc}(1 - e^{-s\tau_d}) = F_{osc} \cdot s\frac{M}{F_{AM}}. \tag{2-12}$$

By substituting $F_{osc}$ - $F_{inj}$ into $F_{AM}$,

$$F_{osc} - F_{inj} = F_{osc} \cdot s\frac{M}{\Delta f}. \tag{2-13}$$

By rearranging (2-13), the transfer function between injection and free-running frequency is derived as

$$H(s) = \frac{F_{osc}}{F_{inj}} = \frac{1}{1 + s\frac{M}{\Delta f}} = \frac{1}{1 + s\tau_{IFLL}} \tag{2-14}$$

where $\tau_{IFLL}$ is $M/\Delta f$. Let us suppose that the injection signal, $f_{inj}$, has a unit step function to express turn-on/off of the IFLL. By solving (2-14) in time domain, the output frequency of the QILO can be expressed as

$$f_{osc}(t) = f_{osc,init} - (f_{osc,init} - 3f_{inj})(1 - e^{-\frac{t}{\tau_{IFLL}}}) \tag{2-15}$$

where $f_{osc,init}$ is the initial free-running frequency of the QILO. As a result, from (2-15) the division ratio of the update-controller and the step frequency of the switched-C array absolutely determine loop-locking time regardless of the difference between the initial free-running frequency and injection frequency. Fig. 2-16(a) shows that $\tau_{IFLL}$ determines the settling time regardless of the injection frequency. Also, as $M$ increases, the settling time increases as shown in Fig. 2-16(b). The results of transient model analysis, linear model analysis, and SPECTRE simulation for injection-locking procedure are shown in Fig. 2-17. When $f_{osc}$= 30.1 GHz, $3f_{inj}$ = 28.3 GHz, $M$ = 8, and $\Delta f$ = 142 MHz, every result shows a locking time of about 175ns. Therefore, the calculated equations (2-10), (2-15) are confirmed by the simulation result.

## 2.3.4 Building Blocks of IFLL

### 2.3.4.1 Envelope Detector & Limiter

Fig. 2-18 shows the schematic of an envelope detector and a limiter. The quadrature signals of the QILO are applied to an envelope detector, which consists of a source follower, load capacitor $C_{ED}$, and a current source. The envelope wave is held at the load capacitor where the discharge time constant depends on the impedance of the active load and bias

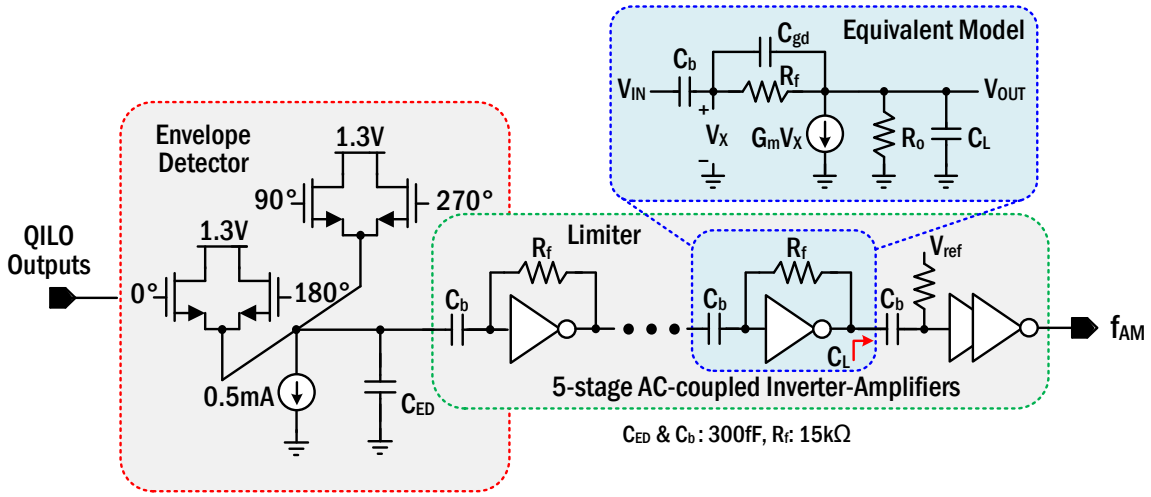



Fig. 2-18. Schematic of an envelope detector and a limiter.

circuit. The output signal of the envelope detector would be a constant DC value under injection-locked condition, while it would output a sinusoidal signal directly correlated with (1) when injection-unlocked. Since the envelope wave under unlocked condition has a very small swing (less than 50 mV), the limiter is implemented next to the envelope detector to convert the wave to rail-to-rail pulse. The limiter is composed of five AC-coupled CMOS inverters and fully swinging inverters. After amplifying the small envelope wave, the inverters generate rail-to-rail pulses with reference voltage, $V_{ref}$. To filter out very low frequency envelope waves when the envelope detector senses quasi-lock or prevent false pulses due to switching noise of the switched-C array, the overall gain response in the limiting amplifiers is band-pass shaped by leveraging node poles and zeroes created by transistor parasitics, $C_{ED}$, $C_b$ and $R_f$. The operation range of the IFLL is generally determined by that of the limiter which is controlled by its poles and zeros. As shown in Fig. 2-19, each AC-coupled inverter-amplifier can be expressed as the equivalent model. From the equivalent model, the transfer function, $H_{Limiter}(s)$, of the five-stage limiting amplifiers can be calculated as

$$H_{Limiter}(s) = \left( \frac{V_X}{V_{IN}} \cdot \frac{V_{OUT}}{V_X} \right)^5 \approx \left( \frac{s/f_{p1}}{1+s/f_{p1}} \cdot \frac{G_m R_o \cdot (1+s/f_z)}{1+s/f_{p2}} \right)^5 \qquad (2\text{-}16)$$

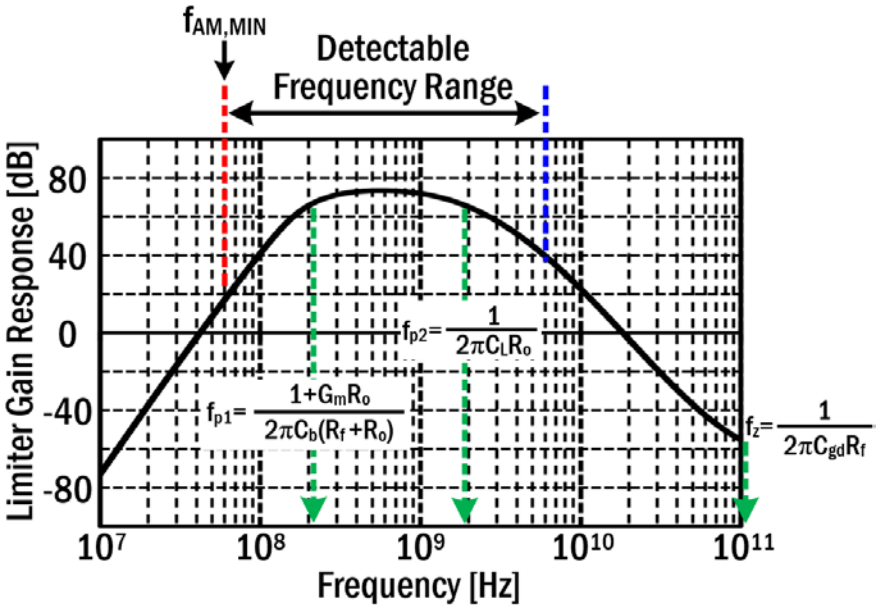



Fig. 2-19. Bandwidth of limiter.

where $f_{p1} = \dfrac{1+g_m R_o}{2\pi C_b (R_f + R_o)}$, $f_{p2} = \dfrac{1}{2\pi C_b R_o}$, $f_z = \dfrac{1}{2\pi C_{gd} R_f}$.

Fig 20 shows the gain response of the five-stage limiting amplifier chain in simulation. The first pole determines the minimum detectable frequency of the IFLL, while the maximum detectable frequency is restricted by the zero and second pole. Since the swing of the envelope wave becomes smaller as the frequency difference between $f_{osc}$ and $3f_{inj}$ increases, higher bands in the limiter require higher gain than low bands. In simulations, the minimum detectable frequency ($f_{AM,MIN}$) is around 60 MHz, about 20 dB gain crossing point in the gain response. On the other hand, the maximum detectable frequency requires more than 40 dB gain at 6 GHz to amplify a very small envelope wave ($2\beta V_{inj,p}$).

### 2.3.4.2 Lock Detector

The proposed IFLL performs phase noise calibration to avoid phase noise degradation at the edge of the locking range. For this operation, it requires a lock signal to judge lock status of the QILO. Fig. 2-20 shows the schematic and timing diagram of the lock detector. It consists of an 8-bit shift register and a *Q*-pump. When unlocked, pulses from the limiter are applied to the lock detector. The shift register and AND gate produce pulses after counting

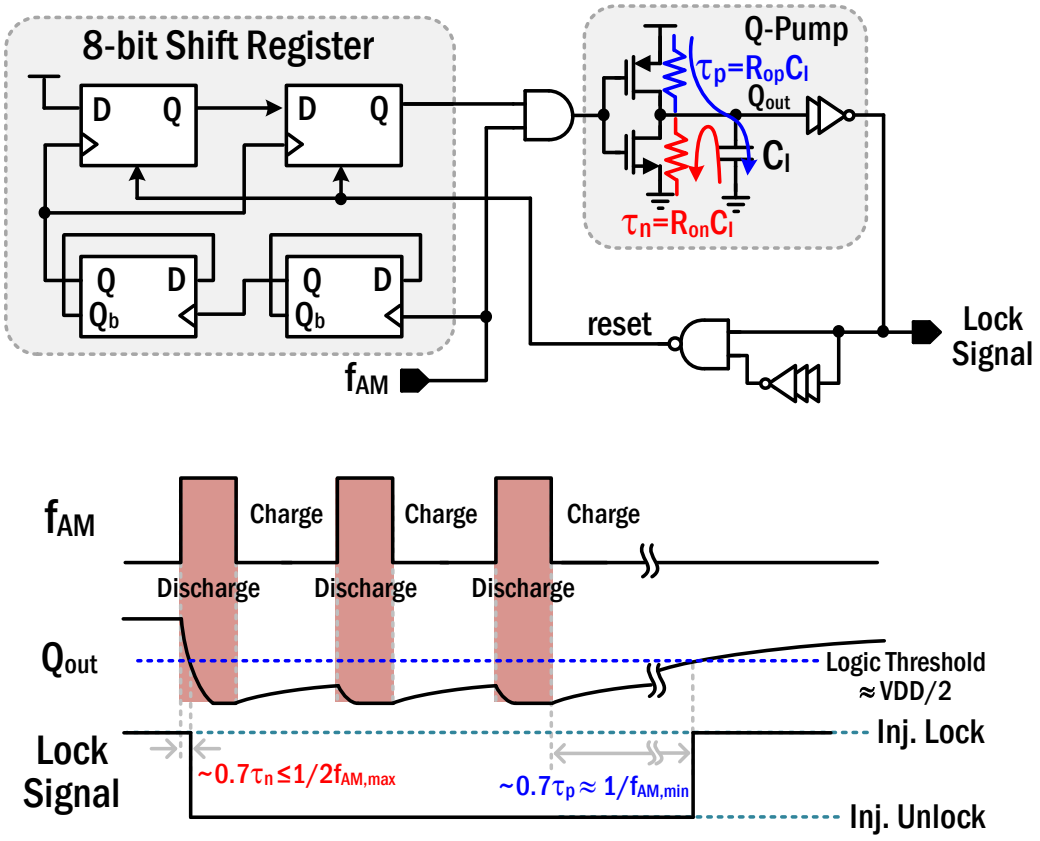



Fig. 2-20. Schematic and timing diagram of the lock detector.

eight consecutive pulses and drive the *Q*-pump that discharges the $C_I$ (2pF) progressively. Then, the lock signal becomes 'Low' and enables the envelope pulse path of the update-controller. Since the limiter may generate irregular pulses due to minute changes of small signals during settling time, the shift register prevents the operation of the IFLL until eight pulse signals are enabled. After calibration, there is no envelope signal and then the *Q*-pump charges the $C_I$. Hence the lock signal transits from 'Low' to 'High'. The lock signal is enabled in the update-controller for 1-LSB code shift after calibration. The charging and discharging totally depend on time constants, $\tau_p$ and $\tau_n$ due to the sizes of the NMOS and PMOS transistors in the *Q*-pump. To ensure the functioning of the *Q*-pump, $\tau_p$ and $\tau_n$ should meet the following conditions:

$$0.7\tau_n \le \frac{1}{2f_{AM,\max}}, \quad 0.7\tau_p \approx \frac{1}{f_{AM,\min}}. \tag{2-17}$$

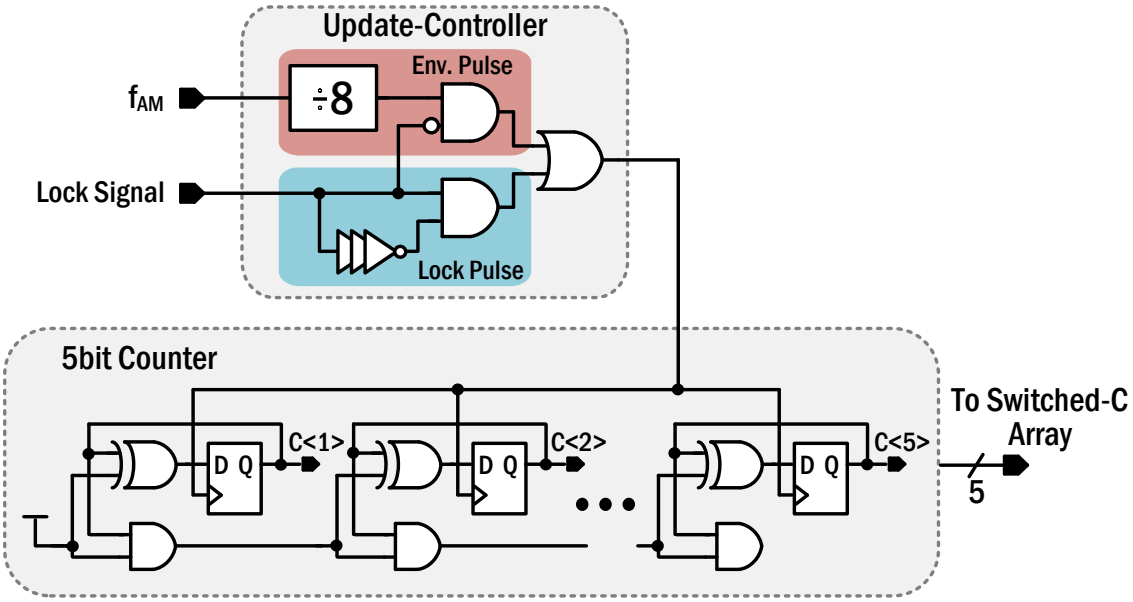



Fig. 2-21. Schematic of update-controller and 5-bit counter.

In this work, for an $f_{AM,min}$ of about 60 MHz, it requires about 17 ns to charge the $C_I$ as much as the logic threshold of the inverter. Also, less than 83 ps is required for discharging the time of $f_{AM,max}$ regardless of its duty cycle.

### 2.3.4.3 Update-Controller and Counter

Fig. 2-21 shows the update-controller and the 5-bit counter. When the lock signal is 'Low' under unlocked condition, the pulse signal, $f_{AM}$, passes through the envelope pulse path and then is divided by eight to filter out unwanted pulses when switching codes of the QILO. After that, it drives the 5-bit up-counter to update 1-LSB of the switched-C array in the QILO every eight-pulse signal. Once the lock signal goes to 'High' after completing frequency calibration, any pulse signal would not be applied to the counter and the update controller generates a short pulse signal by using the transition from 'Low' to 'High'. This additional pulse signal causes the free-running frequency of the QILO to move closer to the center of the effective range as shown in Fig. 2-9(c). Then, the operation of locking range calibration is completed.

## 2.4 Experimental Results

The chip photograph of the proposed IFLL with QVCO and QILO manufactured in a 0.13um CMOS process is shown in Fig. 2-22. The IFLL is characterized with on-wafer testing using GSSG probes for RF signal transition at the VCO outputs. Since all digital circuits are driven autonomously by the envelope pulse, no external control clock is required. After injection-locking with the IFLL, the output power spectrum of the QILO is shown in Fig. 2-23. The measured peak output power at third harmonic is -23 dBm at 26.5 GHz with some power loss from cable and probe. The injection signal of 8.85 GHz is suppressed by more than 40 dB below the third harmonic. The measured typical phase noise of the QVCO at 8.84 GHz is -117.2 dBc/Hz and -129.6 dBc/Hz at 1 MHz and 10 MHz offset, respectively, as shown in Fig. 2-24(a). When the QILO is third-harmonically locked by the QVCO, the phase noise degradation is consistently about 10.5 dB at both 20 dB-rolloff and flat regions, resulting in a phase noise of -106.8 dBc/Hz and -118.9 dBc/Hz at 1 MHz and 10 MHz offsets, respectively, at 26.54 GHz in Fig. 2-24(b). More comprehensive frequency measurement

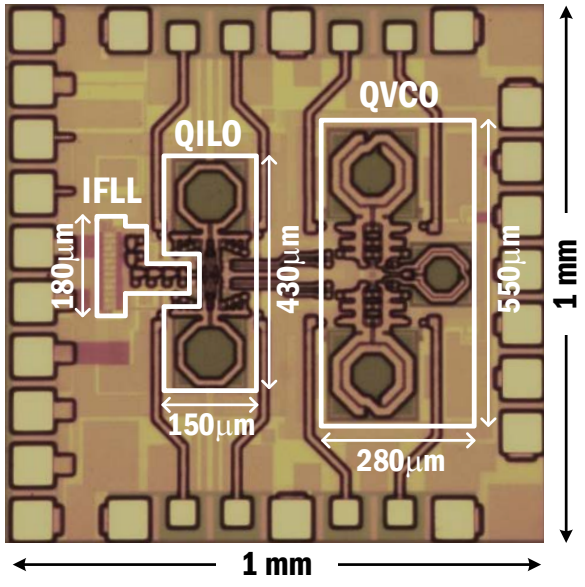



Fig. 2-22. Chip photograph.

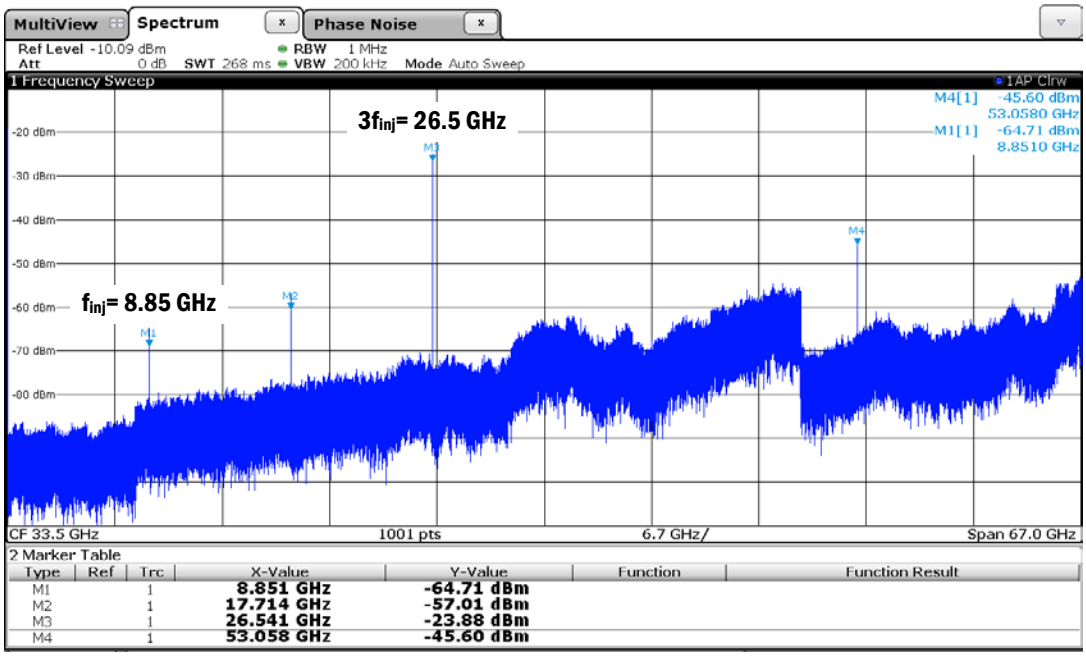
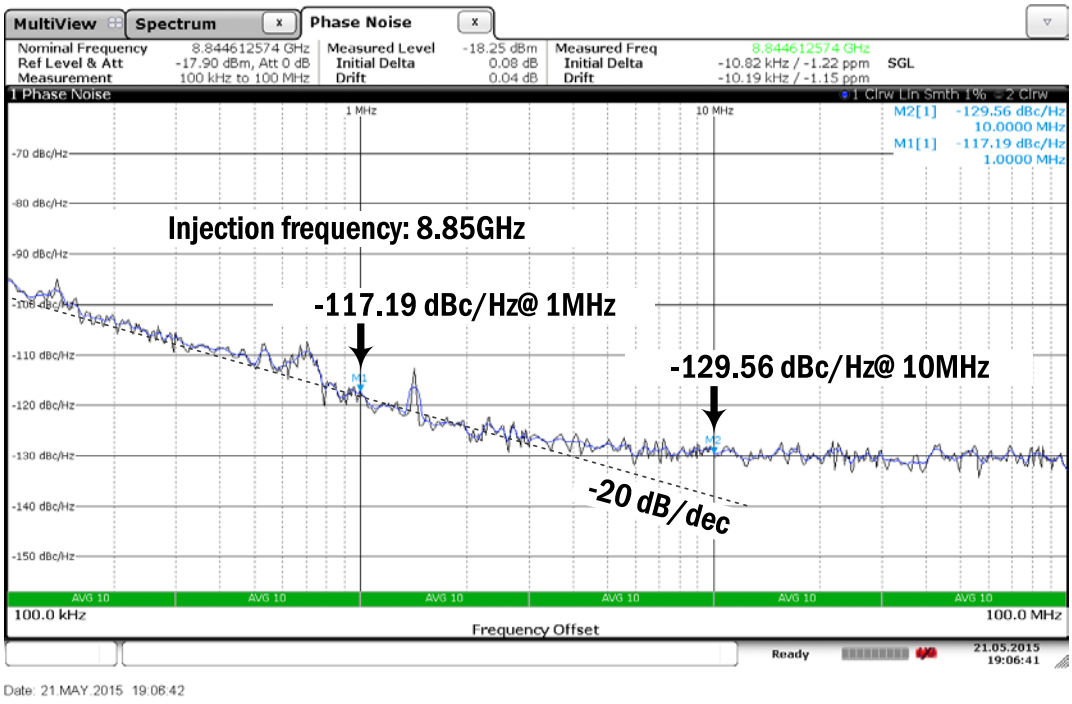
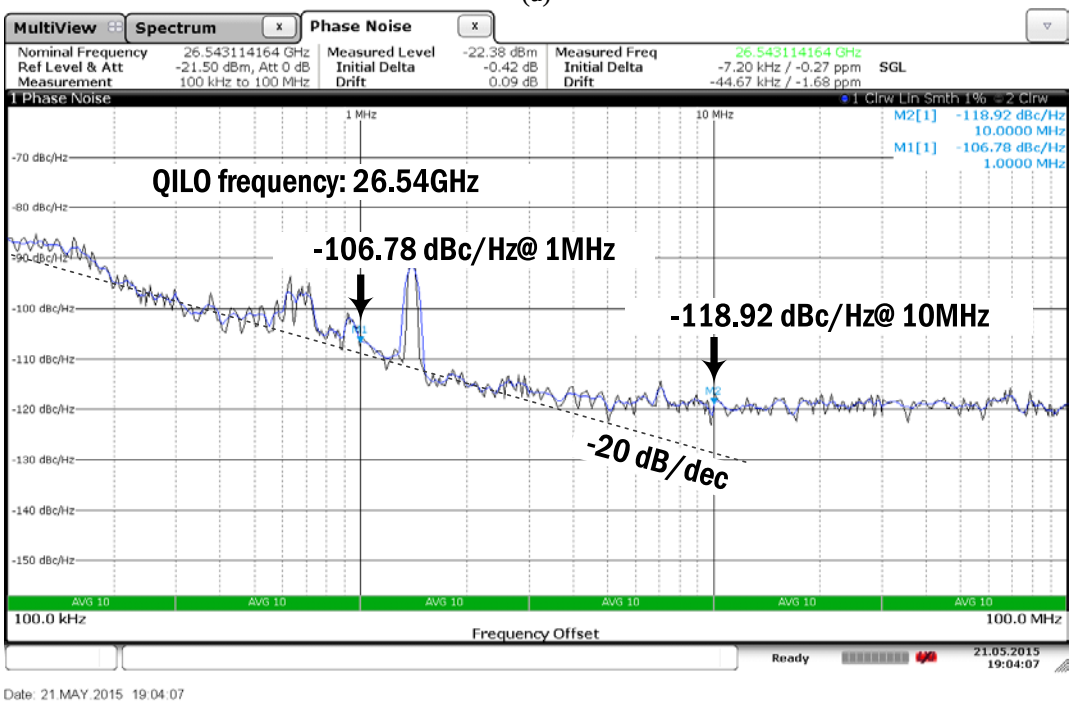



Fig. 2-23. Output power spectrum of the QILO after IFLL.

results are shown in Fig. 2-25. The measured QVCO phase noise at 5 MHz offset ranges from -130 dBc/Hz at 8.8 GHz to -115 dBc/Hz at 9.9 GHz as shown in Fig. 2-25 ①. With the IFLL disabled and by decreasing the QVCO $f_{inj}$ from 9.9 to 9.8 GHz, the QILO can maintain locking from 29.7 to 29.4 GHz ($\Delta f_L$= 300 MHz, QILO free-running $f_{osc}$= 29.55 GHz) but the phase noise degrades by 18-20.5 dB at the edges of the $\Delta f_L$ from the minimum of -107.5 dBc/Hz as shown in Fig. 2-25 ②. Thus, a more effective locking range claiming only 10-10.5 dB phase noise degradation from the QVCO phase noise is from 29.48 to 29.66 GHz (180 MHz), which is 60% of $\Delta f_L$ as shown in Fig. 2-25 ③ and ④. However, when the IFLL is enabled, the QILO can track the QVCO injection frequencies and exhibit consistent 9-10 dB phase noise degradation with ±1 dB error for the entire measurement range from 26.4 to 29.7 GHz as shown in Fig. 2-25 ③.




(a)




(b)

Fig. 2-24. Measured phase noise of (a) QVCO and (b) QILO after IFLL.

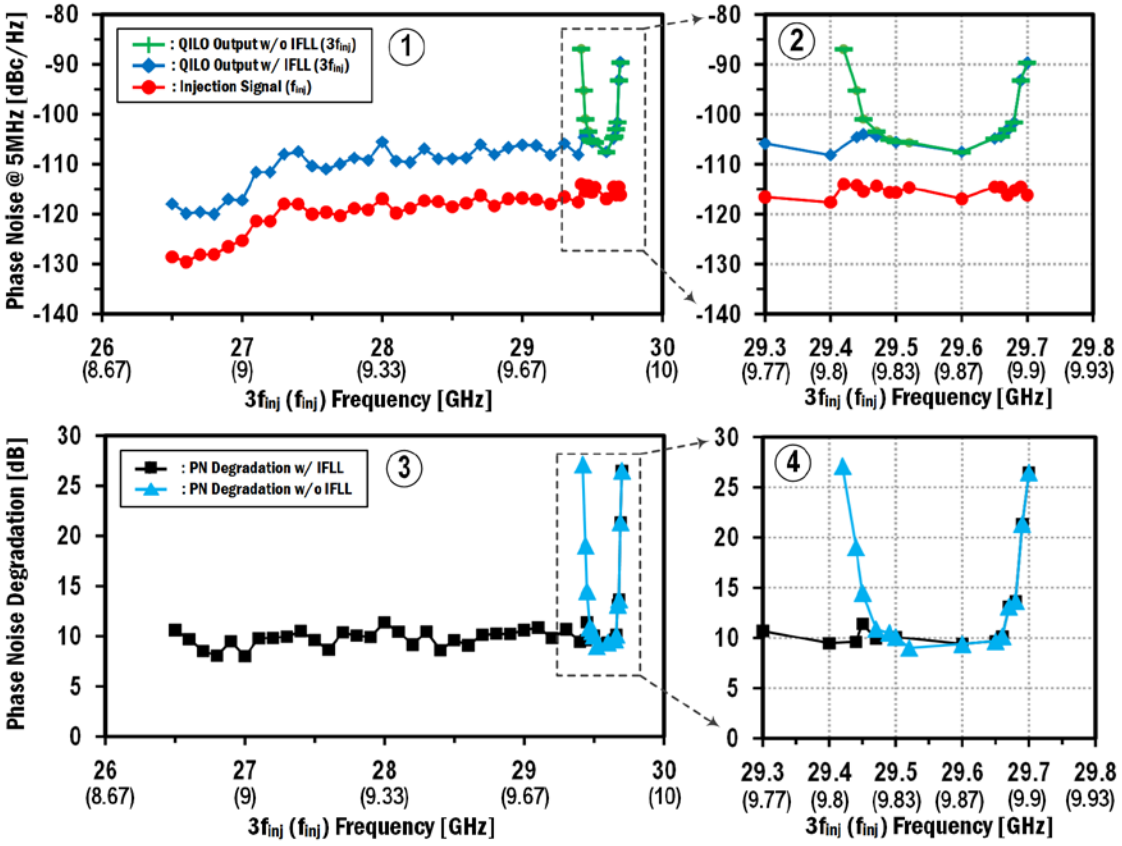
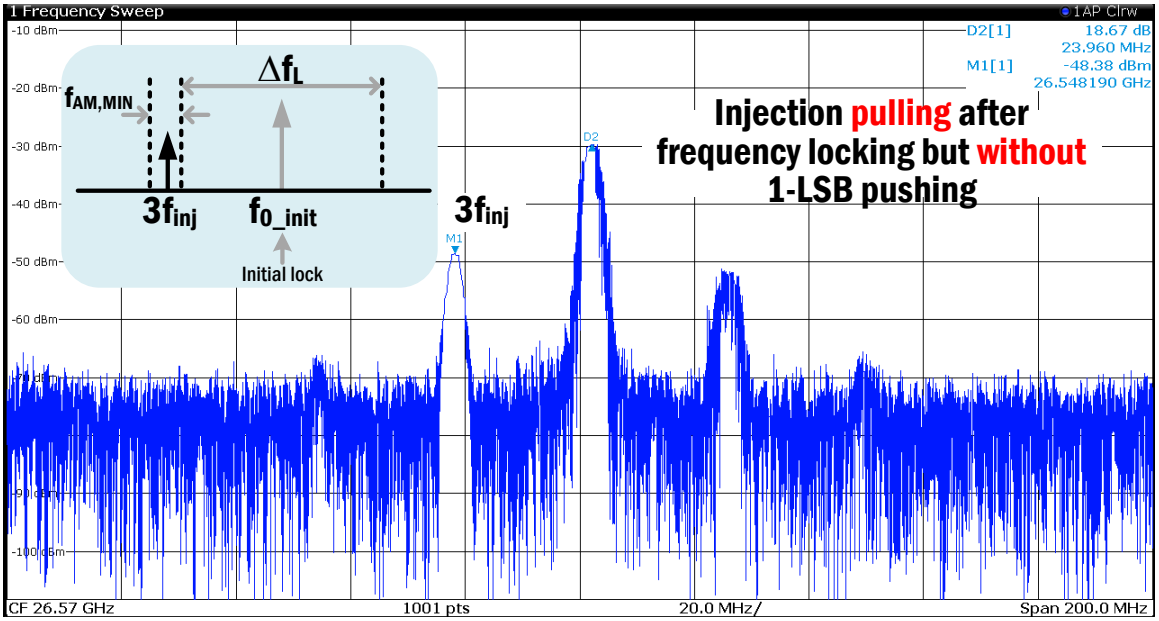


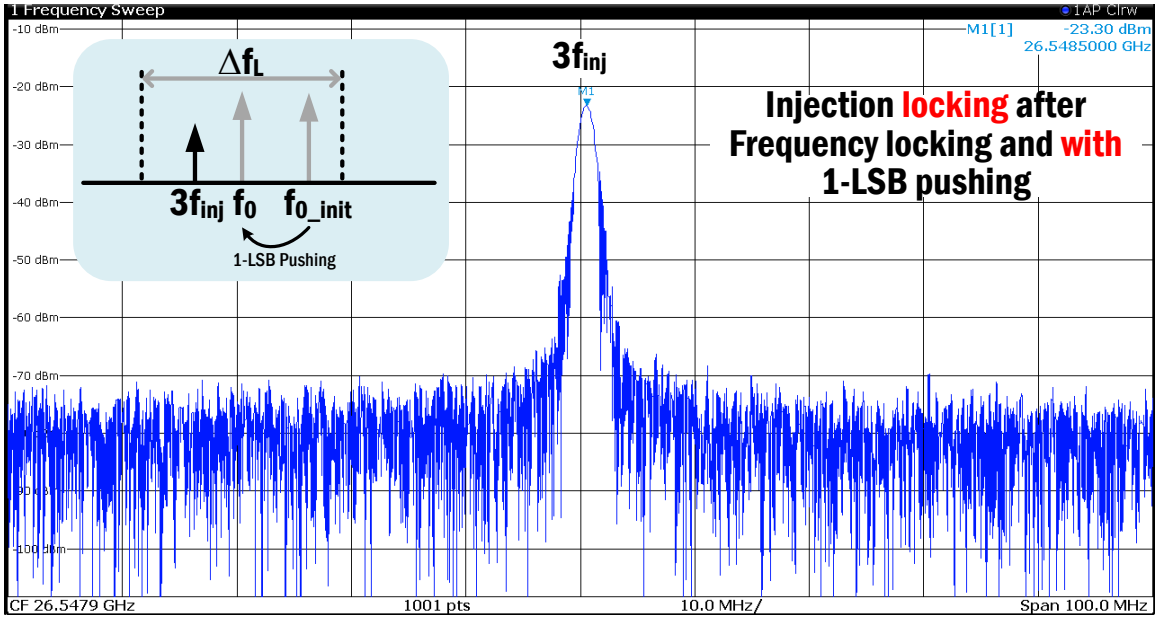

Fig. 2-25. More comprehensive frequency measurement results.

To verify the functional effect of phase noise calibration, its on/off modes were externally controlled. Fig. 2-26 shows output spectrum with and without 1-LSB pushing when quasi-locked out of locking range within $f_{AM,MIN}$. When $f_{osc}$ is 29.7 GHz and $3f_{inj}$ is 26.548 GHz, the QILO without phase noise calibration still suffers from injection-pulling in spite of the frequency calibration of the IFLL as shown in Fig. 2-26(a). The offset frequency from the edge of locking range can be approximated as the frequency difference between each spectrum tone. It shows 23.9MHz. On the other hand, when phase noise calibration is turned on, the QILO is injection-locked after 1-LSB pushing as shown in Fig. 2-26(b).

Fig. 2-27(a) shows the power consumption comparison of the proposed scheme. The QVCO and QILO, excluding the buffer stage, consume 14.4 mW and 20.8 mW at a supply voltage of 0.9 V and 1.3 V, respectively. The power consumption in the calibration circuits



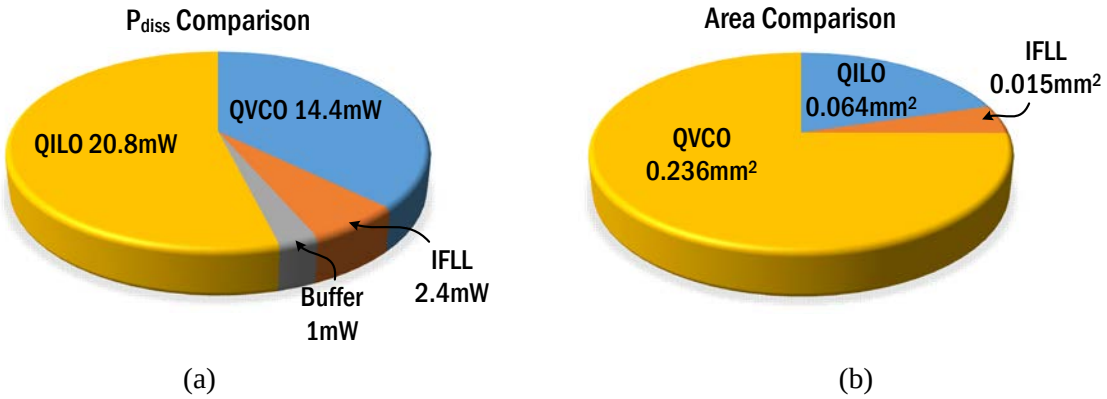

(a)




(b)

Fig. 2-26. Output spectrum (a) with and (b) without 1-LSB pushing when quasi-locked out of locking range within $f_{AM,MIN}$.

is 2.4 mW, where most of the power consumption comes from the static current of the envelope detector and the limiter. In terms of area, comparing the QVCO and QILO in the




(a) (b)

Fig. 2-27. (a) Power consumption and (b) area breakdown.

chip size of 1x1mm$^2$ including pads, the area penalty by the auxiliary calibration circuits is negligible as can be seen in Fig. 2-27(b).

Table 2.1 shows the performance summary of the proposed IFLL and comparison with prior works. The proposed calibration circuit implemented autonomous feedback calibration and simplified its structure by using an envelope detector and digital feedback circuit. Therefore, it achieved 27 times less power consumption, 63 times smaller area and 142 times faster locking time than previous work [2-7] while achieving equivalent locking range (11.4%). Also, the phase noise performance of this LO generator is on a par with other state-of-the-art designs when the frequency is scaled to similar range as shown in Table 2.2.

## 2.5 Summary

This work presents a mixed-mode injection-frequency locked loop (IFLL) for calibrating locking range and phase noise of an injection-locked oscillator (ILO). The IFLL autonomously tracks the injection frequency by processing the AM modulated envelope signal bearing the frequency difference between injection frequency and ILO free-running frequency using digital feedback. This self-calibration technique results in a compact, fast-locking and power-efficient IFLL, demonstrated in 130nm CMOS at 26.5-29.7GHz with less than 300ns locking time and 2.4mW power consumption in the calibration circuits.

TABLE 2.1. CALIBRATION CIRCUIT COMPARISON

| | Tech | Feature | Locking Range (%) (w/o Calibration) | VDD (V) | Power (mW) | Area ($mm^2$) | Locking Time | Operation |
|---|---|---|---|---|---|---|---|---|
| [2-7] | 65nm CMOS | PLL+Mixer +Doulber | 11.2 (0.5) | 1.2 | 65 | ~ 0.95* | < 42.7us | Externally Controlled |
| This Work | 130nm CMOS | Envelope Detector | 11.4 (1) | 1.3 | 2.4 | 0.015 | < **300ns | Autonomous |

*Estimation based on chip photograph. **Estimation based on simulations.

TABLE 2.2. COMPARISON WITH PRIOR STATE-OF-THE-ART WORKS

| | Tech | Phase | Freq. (GHz) | VDD (V) | Power (mW) | Phase Noise (dBc/Hz@1MHz offset) | Chip Area ($mm^2$) | Feature |
|---|---|---|---|---|---|---|---|---|
| [2-12] | 130nm SiGe | Diff. | 27.9-37.8 | 1.5 | 10 (VCO only) | -103.6 @32.9GHz | 1.93 | BiCMOS Cross-coupled Pair VCO |
| [2-6] | 65nm CMOS | Quad. | 67.2-67.7 | 1.2 | 68 | -95 @60GHz | 0.8 (QILO only) | PLL+QILO w/ Dual Injection |
| [2-7] | 65nm CMOS | Quad. | 58.1-65 | 1.2 | 137 | -96 @61.5GHz | 3.8 | PLL+QILO + Calibration Circuit |
| This Work | 130nm CMOS | Quad. | 26.5-29.7 | 1.3 | *38.6 (**49.7 ) | -106.8 @26.5GHz | 1 | QVCO+QILO + Calibration Circuit |

*Without VCO output buffers.
**With including VCO output buffers for measurement with 50-Ω instruments.

## 2.6 References


[2-1] L. Zhou, C.-C. Wang, Z. Chen, and P. Heydari, “A W-band CMOS receiver chipset for millimeter-wave radiometer systems,” *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 378–391, Feb. 2011.

[2-2] E. Monaco, M. Pozzoni, F. Svelto, and A. Mazzanti, “Injection-locked CMOS frequency doublers for μ-wave and mm-wave applications,” *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1565–1574, Aug. 2010.

[2-3] T.-N. Luo and Y.-J. E. Chen, “0.8-mW 55-GHz dual-injection-locked CMOS frequency divider,” *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 3, pp. 620–625, Mar. 2008.

[2-4] J. Lee and B. Razavi, “A 40-GHz frequency divider in 0.18-um CMOS technology,” *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 594–601, Apr. 2004.

[2-5] W. Chan and J. Long, “A 56–65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2739–2746, Dec. 2008.

[2-6] A. Musa, R. Murakami, T. Sato, W. Chaivipas, K. Okada, and A. Matsuzawa, "A low phase noise quadrature injection locked frequency synthesizer for mm-wave applications", *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2635-2649, Nov. 2011.

[2-7] W. Deng et al., “A sub-harmonic injection-locked quadrature frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers,” *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1710–1720, Jul. 2013.

[2-8] S. Gierkink, et al., “A Low-Phase-Noise 5-GHz CMOS quadrature VCO using superharmonic coupling,” *IEEE J. Solid-State Circuits*, pp. 1148–1154, July 2003.

[2-9] X. Yi, et al., “A 57.9-to-68.3 GHz 24.6 mW frequency synthesizer with in-phase injection-coupled QVCO in 65 nm CMOS technology,” *IEEE J. Solid-State Circuits*, pp. 347–359, Feb. 2014.

[2-10] J. Bae, et al., “A low energy injection-locked FSK transceiver with frequency-to-amplitude conversion for body sensor applications,” *IEEE J. Solid-State Circuits*, pp.928–937, April 2011.

[2-11] B. Razavi, “A study of injection locking and pulling in oscillators,” *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[2-12] Q. Wu, T. Quach, A. Mattamana, S. Elabd, S. R. Dooley, J. J. McCue, P. L. Orlando, G. L. Creech, and W. Khalil, “A 10mW 37.8GHz current-redistribution BiCMOS VCO with an average $FOM_T$ of -193.5dBc/Hz,” *in IEEE Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 150–151.

# Chapter 3.

# A 24-GHz Quadrature Injection-Locked Frequency Tripler Using Capacitively-Degenerated Differential Pairs for Quadrature Injection

## 3.1 Introduction

Recently, injection-locked frequency multipliers (ILFMs) are becoming widely used to generate local oscillator signals for millimeter-wave applications [3-1]-[3-5]. There are two main reasons why the ILFM is preferred over a typical standalone VCO in a millimeter-wave frequency synthesizer. Firstly, a conventional frequency synthesizer usually requires a high-frequency divider such as an injection-locked frequency divider [3-6]-[2-7] or Miller divider [3-8]-[3-9]. However, multiple stages of these dividers may be required because their division ratio is very low. In addition, their narrowband characteristic demands higher injection power from the VCO or a frequency calibration circuit [3-10]. Also, additional buffers are necessary to couple output signals from the VCO to the divider without any loss for a wider locking range of the divider. Hence, the overall power consumption of the frequency synthesizer can be quite high. On the other hand, the nth-harmonic ILFM does not require the high frequency divider since the output of the VCO, one-nth frequency of ILFM output, is directly connected to CML or digital dividers. Therefore, the injection-locked frequency synthesizer can optimize hardware complexity and achieve low power consumption. Secondly, a typical frequency synthesizer requires a low phase noise

differential or quadrature VCO. However, in the millimeter-wave band, it is very difficult to design the low phase noise VCO at the desired fundamental frequency because a quality factor of varactors degrades as tuning frequency increases.

The sub-harmonic ILFM is an alternative to achieve low phase noise VCO outputs at millimeter-wave frequencies [3-11]-[3-13]. Since high varactor quality factor can be attained at low frequency, in the injection-locked frequency synthesizer the low phase noise signal (injection signal) generated by a lower frequency VCO can be injected into a sub-harmonic ILFM. When the nth-harmonic of the injection signal is applied to the ILFM and it becomes locked, the ILFM has the phase noise of the injection signal degraded by $20\log_{10}(n)$. However, the phase noise degradation may be increased beyond $20\log_{10}(n)$ as the locked frequency moves closer to the edge of the locking range. Therefore, the most important design consideration for the ILFM is injection-locking range.

In general, the injection-locking range, $\Delta\omega$, has been defined by Razavi [3-14] as

$$\Delta\omega = \frac{\omega_{osc}}{2Q}\frac{I_{inj}}{I_{osc}}\frac{1}{\sqrt{1-\left(I_{inj}/I_{osc}\right)^2}} \tag{3-1}$$

where $\omega_{osc}$ and $I_{osc}$ are the resonant frequency and current of the LC tank, respectively, $Q$ is the quality factor of the LC tank and $\omega_{inj}$ and $I_{inj}$ are the frequency and current of the injection signal, respectively. (3-1) implies that for wide locking range, the $Q$ and $I_{osc}$ of the LC tank should be decreased and the $I_{inj}$ should be increased. However, lower $Q$ and $I_{osc}$ may cause start-up of an oscillator to fail. Moreover, increasing the $I_{inj}$ results in higher power consumption. In the case of a multiphase ILFM, the locking range can be widened when multiple signals are injected. However, a phase mismatch among multiple injection signals causes degradation of the locking range [3-15].

In this work, the characteristics of conventional quadrature injection-locked frequency triplers (ILFT) are analyzed, and are compared to the proposed quadrature ILFT using capacitively-degenerated differential pairs. This paper is organized as follows. Chapter 3.2 introduces previous and novel ways to design a quadrature ILFT with single-phase differential injection signal. In Chapter 3.3, the implementation of the proposed ILFT using

third harmonic phase shifter is described in detail. The experimental results are presented in Chapter 3.4. Finally, Chapter 3.5 provides a chapter summary.

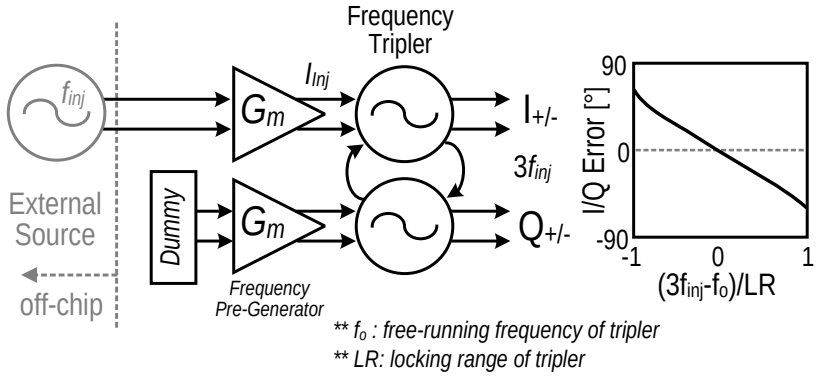
## 3.2 Quadrature Injection-Locked Frequency Triplers with Differential Injection

A typical quadrature ILFT consists of a frequency pre-generator for third harmonic generation and two LC tanks which self-oscillate near the third harmonic of the injection signal. Undesired harmonic frequencies from the frequency pre-generator are eliminated by the LC tanks. In general, the locking range of ILFT is proportional to the number of injection signals [3-15] under the assumption that there is no phase error between injection signals. Considering [3-15] and injection loss, $\alpha$ ($0 \leq \alpha \leq 1$), due to the pre-frequency generators, the locking range of (3-1) in weak multiple injection can be rewritten as

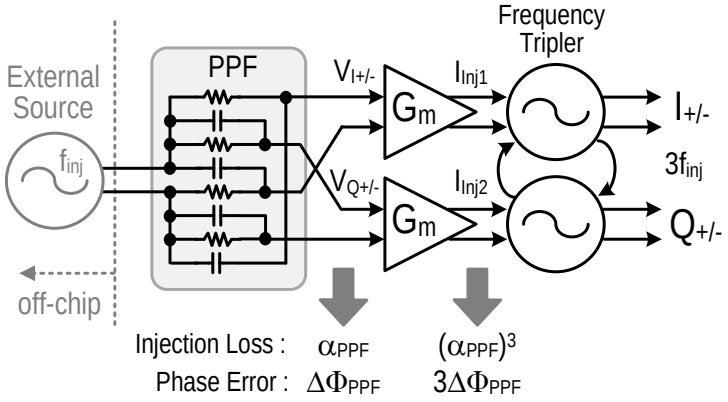
$$\Delta\omega = \alpha N \frac{\omega_{osc}}{2Q} \frac{I_{inj}}{I_{osc}} \tag{3-2}$$

where $N$ is the number of injection signals. In the case of quadrature ILFT, quadrature injection signals are required to maximize injection-locking range and achieve good phase accuracy. However, it is challenging to design an external quadrature signal generator and LO distribution system. Therefore, conventional quadrature ILFTs have tried to improve the injection-locking range and phase accuracy, using single-phase differential injection signals [3-16].

There are two conventional approaches for differential signal injection in ILFTs as shown in Fig. 3-1. The first approach is single-sided injection (SSI) as shown in Fig. 3-1(a). One core cell of the ILFT is injected directly with an external single-phase differential signal. Another core cell is connected to a dummy source impedance having the same value as the injection source to maintain symmetry. Although the SSI-ILFT can be easily implemented, it has very narrow locking range compared to quadrature injection and its phase error significantly increases as the injection frequency deviates from free-running frequency of




(a)




(b)

Fig. 3-1. Previous quadrature ILFTs: (a) single-sided injection type and (b) quadrate injection type using PPF.

the ILFT (within the injection-locking range). In order to improve the injection-locking range of SSI-ILFT, dual injection of one core cell was proposed in [3-16]. However, even this dual injection scheme could not achieve wider injection-locking range compared to quadrature injection. Also, a substantial I/Q error still exists within the injection-locking range. If the free-running frequency of the ILFT exactly matches with third harmonic of the injection signal, this drawback could be mitigated. To track third harmonic frequency, a frequency calibration circuit of the ILFT is implemented in [3-17]. However, the calibration circuit has significant design complexity and a large area.

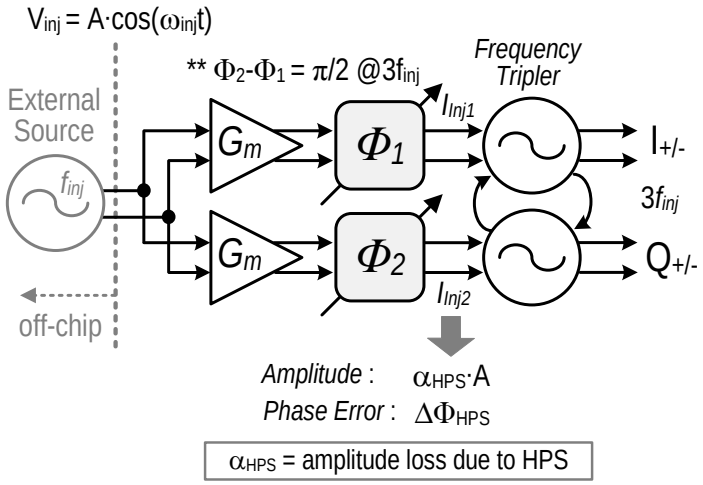



Fig. 3-2. Proposed ILFT using third-harmonic phase shifter.

A second typical approach is the use of a quadrature poly-phase filter (PPF) [3-18]-[3-19]. The external differential injection signals are applied to the PPF to generate quadrature signals for injection locking as shown in Fig. 3-1(b). The outputs of the PPF are directly injected into each core cell of the ILFT via a frequency pre-generator. Hence, the ILFT outputs 3X the injection frequency under the locked situation. As the quadrature signals are used for injection locking, this approach can achieve wider injection-locking range and better phase accuracy than the SSI-ILFT. However, typical PPFs entail injection loss and phase mismatch at the injection frequency due to frequency variation, loading effects and component mismatches. The injection signals due to the PPF suffer from a considerable amount of amplitude loss at third harmonic via the frequency pre-generator because the amplitude of the third harmonic is proportional to the cube of injection amplitude. Specifically, the injection loss is 3X in dB terms when injected to the ILFT. Likewise, an amplitude mismatch, $\Delta A$, between quadrature signals of the PPF would be amplified as much as $(\Delta A)^3$. In addition, the phase error, $\Delta\Phi_{PFF}$, would be 3X ($3\Delta\Phi_{PFF}$) via the frequency pre-generator [3-16]. The amplitude loss and phase mismatch may cause degradation of the injection-locking range.

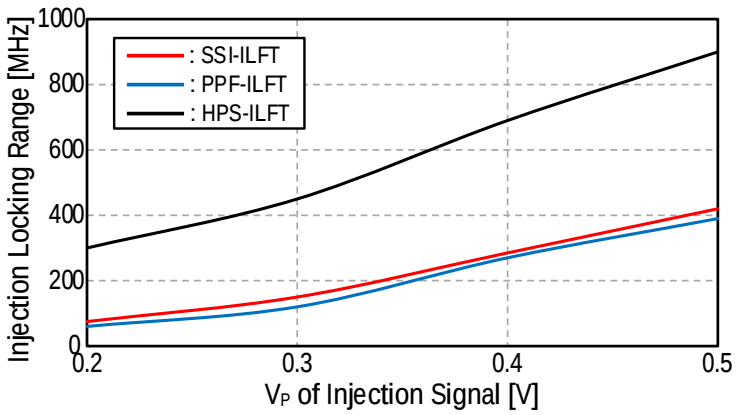



Fig. 3-3. Simulated injection locking ranges of SSI-, PPF-, and HPS- ILFTs.

TABLE 3.1. COMPARISON BETWEEN DIFFERENT QUADRATURE FREQUENCY TRIPERS

| | SSI-ILFT | PPF-ILFT | HPS-ILFT |
|---|---|---|---|
| I/Q Error | Poor (due to mismatch) | Moderate ($3\Delta\phi$) | Good ($\Delta\phi$) |
| Injection Loss | No | $(\alpha_{PPF})^3$ | $\alpha_{HPS}$ |
| Locking Range | $0.5\Delta\omega_i$ | $(\alpha_{PPF})^3 \cdot \Delta\omega_i$ | $\alpha_{HPS} \cdot \Delta\omega_i$ |
| Complexity | Good | Poor | Moderate |

* $\Delta\omega_i$= intrinsic locking range of ILO, ** $\alpha$ = 1- (Injection loss)

In order to optimize injection-locking range and reduce phase error between quadrature output signals, this paper proposes an ILFT using two third harmonic phase shifters as shown in Fig. 3-2. Conceptually, the phase shifters are located between a frequency pre-generator and a quadrature frequency tripler. Each generates a different phase shift, $\Phi_1$ and $\Phi_2$, respectively, at the third harmonic, such that the phase difference between $\Phi_1$ and $\Phi_2$ is 90° for quadrature injection. The proposed scheme can achieve lower injection loss and phase error than the PPF-ILFT since the injection loss and phase error are not amplified via the frequency pre-generator. In general, the injection loss, $\alpha_{HPS}$, and the phase error, $\Delta\Phi_{HPS}$, due to the third harmonic phase shift are approximately similar to $\alpha_{PPF}$ and $\Delta\Phi_{PPF}$, respectively

(further detailed analyses of $\alpha_{HPS}$ and $\Delta\Phi_{HPS}$ are given in Chapter 3.3.3). Table 3.1 briefly summarizes the merits and drawbacks of each ILFT approach in terms of I/Q error, injection-locking range, injection loss and complexity. It is expected that an ILFT using the third harmonic phase shifter (HPS-ILFT) would result in significantly better performance compared to previously considered injection types. The simulated injection locking ranges of injection types according to injection amplitude are presented in Fig. 3-3. Let us assume that three different quadrature ILFTs have the same $Q$, $I_{inj}/I_{osc}$, and $f_{osc}$ where $Q$ = 5, $I_{inj}/I_{osc}$ = 0.15, and $f_{osc}$ = 24 GHz. Also, let us assume the PPF has 6 dB fundamental loss and the HPS has 3 dB injection loss. The simulation results show that the HPS-ILFT has wider locking range than others as expected in Table 3.1. (Note that since the injection mismatch is not completely optimized, the SSI-ILFT has a considerable difference between simulated and calculated locking ranges.) However, the HPS-ILFT performance is critically dependent on the design of the third harmonic phase shifter. A detailed description of the design of the phase shifter for the quadrature ILFT is given in the following.

## 3.3 Proposed Frequency Tripler

Fig. 3-4 shows the block diagram of the proposed quadrature ILFT. Two identical core cells are connected in series to generate quadrature signals. External differential injection signals are applied to two phase shifters which comprise capacitively-degenerated differential pairs to create phase shifts of third harmonic. The two phase shifters have different source degeneration capacitance and resistance for two different phase shifts ($\Phi_1$, $\Phi_2$). The phase shifters provide differential injection signals to their corresponding core cell. The capacitively-degenerated differential pair suppresses the second harmonic of the injection signal and causes phase shift of the fundamental and third harmonic signals. The fundamental component is strongly filtered out by the core cell. The third harmonic is injected into the core cell, where the relative phase difference between the third harmonic signals should be 90° through selection of $R_1$, $R_2$, $C_1$ and $C_2$. The quadrature injection currents from two phase shifters are directly applied to the two core cells. If the free-running frequency of the coupled core cells is close to the third harmonic of injection signals ($\omega_{inj}$),

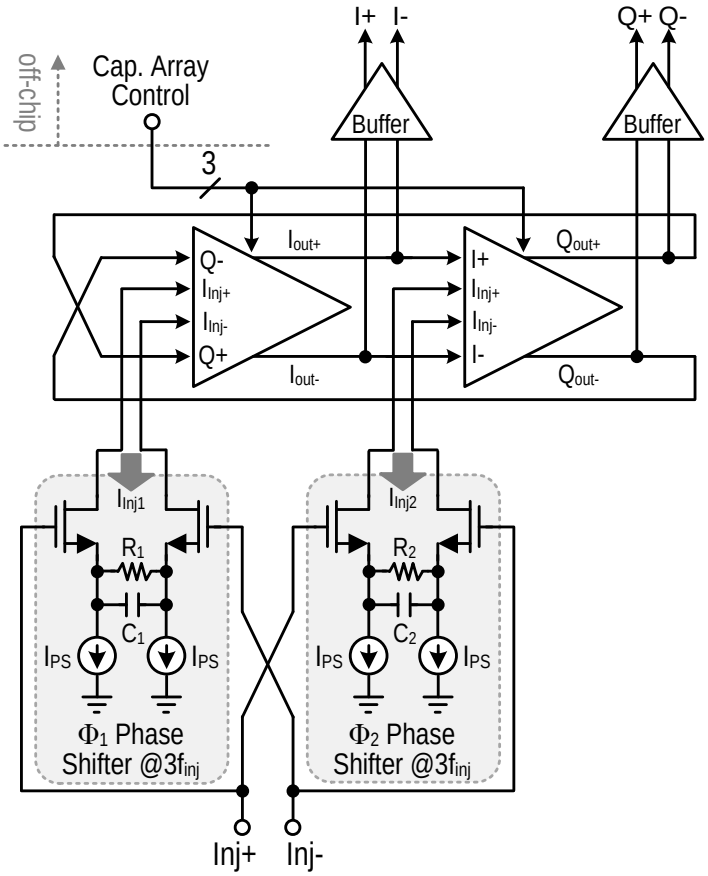



Fig. 3-4. Proposed frequency tripler using capacitive-degenerated differential pair.

the tripler is injection-locked and then outputs $3\omega_{inj}$ quadrature signals, where its phase noise would be degraded by $20\log_{10}(3)$ from that of the injection signal. The proposed ILFT is designed in 130-nm CMOS technology.

### 3.3.1 Core Cell of ILFT

The core cell of the ILFT is presented in Fig. 3-5. Each core cell consists of an LC tank, a 3-bit switched capacitor array, two coupling transistors and a negative resistance cell. The injection currents are directly connected with the output nodes of the core cell. The coupling

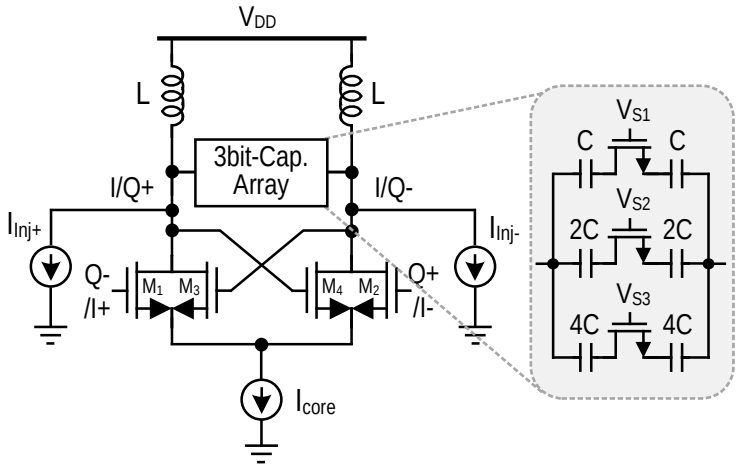



Fig. 3-5. Schematic of the core cell.

transistors (M1, M2) are placed in parallel with the cross-coupled transistors (M3, M4), thereby reducing phase and amplitude errors [3-20]. These transistors are designed with the same length and width. The tank inductance is 130 pH and the switched capacitance is determined by the desired resonance frequency (about 24 GHz), considering a phase shift due to quadrature coupling. By externally controlling the 3-bit capacitor array, the free-running frequency of each core cell can be changed from 22.9 GHz to 24.5 GHz. In order to avoid an unlocked situation of the ILFT, the LSB of the switched capacitor array should correspond to a frequency step less than the injection-locking range. The current consumption of the core cell is 2 mA with 1.3 V supply.

### 3.3.2 Capacitive-Degenerated Pair at Third Harmonic

The capacitively-degenerated pair has been widely used in QVCOs [3-21]-[3-22] to provide phase shift to coupling transistors, thereby reducing the quality factor degradation of the LC tank. However, in these cases the phase shift is considered at only the fundamental frequency. In the proposed ILFT, only the third harmonic is considered because the fundamental and other harmonics are filtered out by the LC tank. In this paper, a capacitively-degenerated differential pair is adopted to create the phase difference of 90°

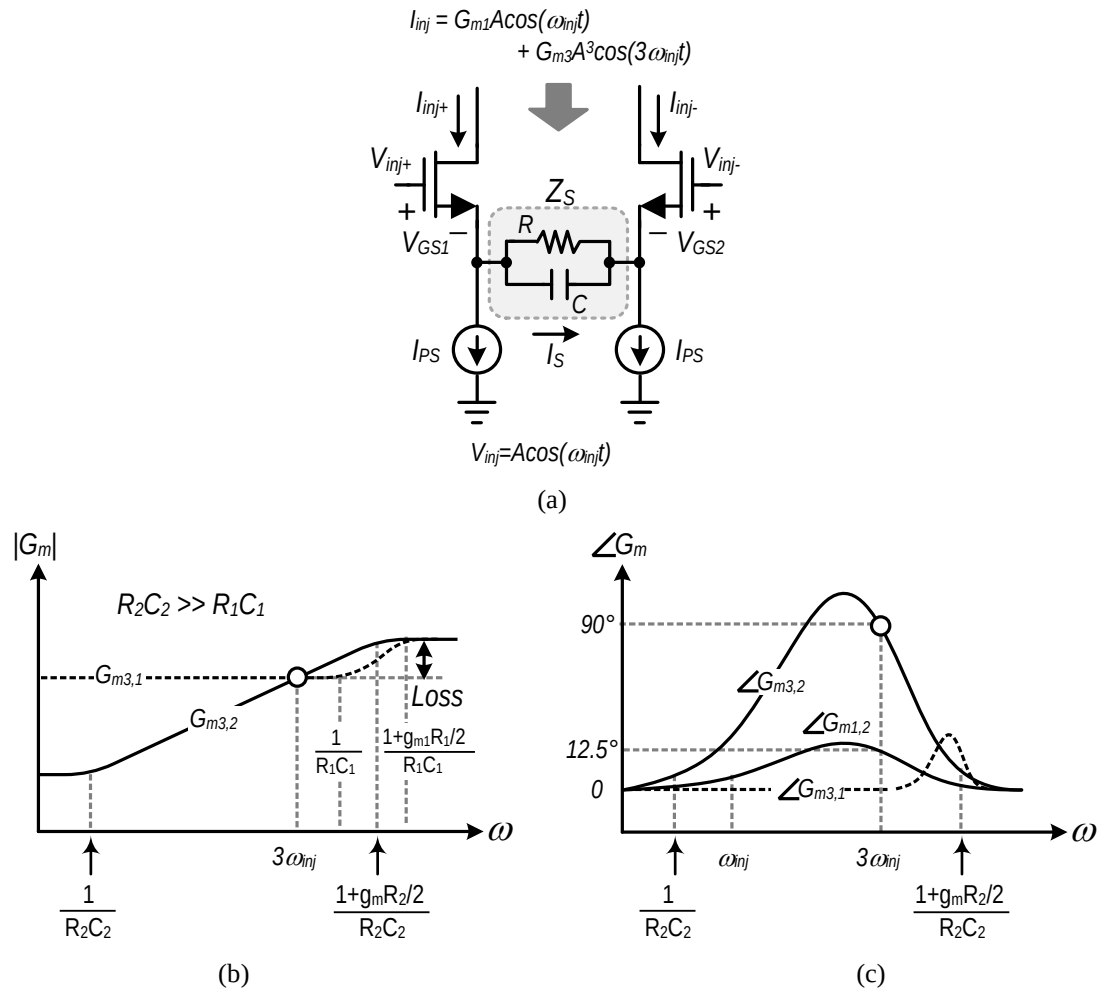



Fig. 3-6. Capacitive-degenerated differential pair for π/2 phase shift at third harmonic frequency: (a) schematic of frequency pre-generator, (b) gain response at third harmonic frequency and (c) its phase shift.

between the two differential injection signals. In this chapter, an amplitude and a phase shift of the harmonics due to the capacitive degeneration are analyzed.

Let us consider the simple schematic of the capacitively-degenerated pair as shown in Fig. 3-6. In general, the injection current has nonlinear characteristics due to the degenerated pair. Therefore, the injection current, $I_{inj}$, can be expressed as a polynomial such as

$$I_{inj} = a_0 + a_1 V_{inj} + a_2 V_{inj}^2 + a_3 V_{inj}^3 + \ldots \tag{3-3}$$

where an is the nth coefficient of the polynomial series. From the schematic in Fig. 3-6(a), the relation between the injection voltage and current can be written as

$$V_{inj+} - V_{GS1} - Z_S I_S = V_{inj-} - V_{GS2} \ . \tag{3-4}$$

With respect to injection current, (3-4) can be substituted with

$$V_{inj} - Z_S I_{inj+} + Z_S I_{PS} = \frac{1}{\sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}}\left(\sqrt{I_{inj+}} - \sqrt{I_{inj-}}\right) \tag{3-5}$$

where $I_S = I_{inj+} - I_{PS}$, $V_{inj} = V_{inj+} - V_{inj-}$ and $Z_S = (R||C)$. Each coefficient, $a_n$, of (3-3) can be calculated by differentiating (3-5) with respect to $V_{inj}$.

$$a_1 = \left.\frac{\partial I_{inj}}{\partial V_{inj}}\right|_{V_{inj}=0} = \frac{1}{Z_S + 2/g_m}, \qquad a_2 = \frac{1}{2}\left.\frac{\partial^2 I_{inj}}{\partial V_{inj}^2}\right|_{V_{inj}=0} = 0 \ ,$$

$$a_3 = \frac{1}{6}\left.\frac{\partial^3 I_{inj}}{\partial V_{inj}^3}\right|_{V_{inj}=0} = \frac{-1}{2\left(Z_S + 2/g_m\right)^4 g_m I_{PS}^2} \tag{3-6}$$

Using (3-6), when $V_{inj} = A\cos(\omega_{inj})$, the injection current of (3-3) through the phase shifter can be approximated as

$$I_{inj} \approx a_0 + G_{m1}A\cos(\omega_{inj}t) + G_{m3}A^3\cos(3\omega_{inj}t) \tag{3-7}$$

where $G_{m1} = (a_1 + 3a_3A^2/4)$ and $G_{m3} = a_3/4$. As indicated in (3-6), the second harmonic of the injection signal is suppressed by the differential pair. Since only the third harmonic is considered in the ILFT, the $G_{m1}$ would be neglected as well. The $G_{m3}$ would predominantly decide the amplitude and phase shift of third harmonic injection current. From $a_3$ of (3-6), Gm3 can be expressed as

$$G_{m3} = -\frac{1}{2^7 g_m I_{PS}^2}\cdot\left(\frac{g_m(RCs+1)}{RCs+1+g_mR/2}\right)^4 . \tag{3-8}$$

As shown in Fig. 3-6(b) and (c), the gain and the phase diagrams can be expressed in two

cases of

$$I_{inj1} = G_{m1,1} A\cos(\omega_{inj} t) + G_{m3,1} A^3 \cos(3\omega_{inj} t) \tag{3-9}$$

$$I_{inj2} = G_{m1,2} A\cos(\omega_{inj} t) + G_{m3,2} A^3 \cos(3\omega_{inj} t)$$

where $R_2C_2 >> R_1C_1$. In order to generate quadrature injection signals at the third harmonic, the phase difference between two phase shifters should be

$$\angle G_{m3,2} - \angle G_{m3,1}\Big|_{@3\omega_{inj}} = 90° \ . \tag{3-10}$$

Simply, to achieve 90° phase difference around the third harmonic, one of the two phase shifters creates approximately 90° phase shift due to $R_2$ and $C_2$ and the other then should not create any phase shift due to $R_1$ and $C_1$. This is the easiest way to create 90° phase shift at the third harmonic. However, the third harmonic phase shifter still entails some injection loss due to $R_2$. Therefore, $R_1$ of the second phase shifter should be selected to minimize injection mismatch among quadrature injection signals. From (3-8), the injection loss can be determined by calculating the ratio of $|G_{m3,1}|$ at $3\omega_{inj}$ to maximum $|G_{m3,1}|$:

$$Injection\ Loss = \frac{\left|G_{m3,1}\right|_{\omega=3\omega_{inj}}}{\left|G_{m3,1}\right|_{\omega=\max}} = \frac{1}{\left(1+g_{m1}R_1/2\right)^4} \tag{3-11}$$

where $1/(R_1C_1)$ should be determined greater than $3\omega_{inj}$ to have no phase shift at $3\omega_{inj}$. In other words, the injection loss can be only determined by $g_{m1}$ and $R_1$.

### 3.3.3 Implementation of 90° Phase Shifter

In practice, 90° phase shifter at third harmonic frequency (~24 GHz) can be implemented by determining each parameter of the capacitive-degenerated pair based on Table 3.2. $R_2$ and $C_2$ is set to generate 90° phase shift at third harmonic. Since there is amplitude loss due to $R_2$ and $C_2$, another phase shifter should be set to R1 and C1, thereby having no phase shift and the same amplitude loss as the 90° phase shifter. Based on these parameters, Fig. 3-7 shows the plots of amplitude loss (injection loss) and phase shift of third harmonic due to two different capacitive-degenerated pairs. As aforementioned, the

TABLE 3.2. DESIGN PARAMETERS OF THE PROPOSED THIRD HARMONIC PHASE SHIFTERS

| Parameter | $R_1$ | $C_1$ | $R_2$ | $C_2$ | $g_{m1}$ & $g_{m2}$ |
|---|---|---|---|---|---|
| Value | 10 Ω | 50 fF | 2 KΩ | 150 fF | 20 mS |

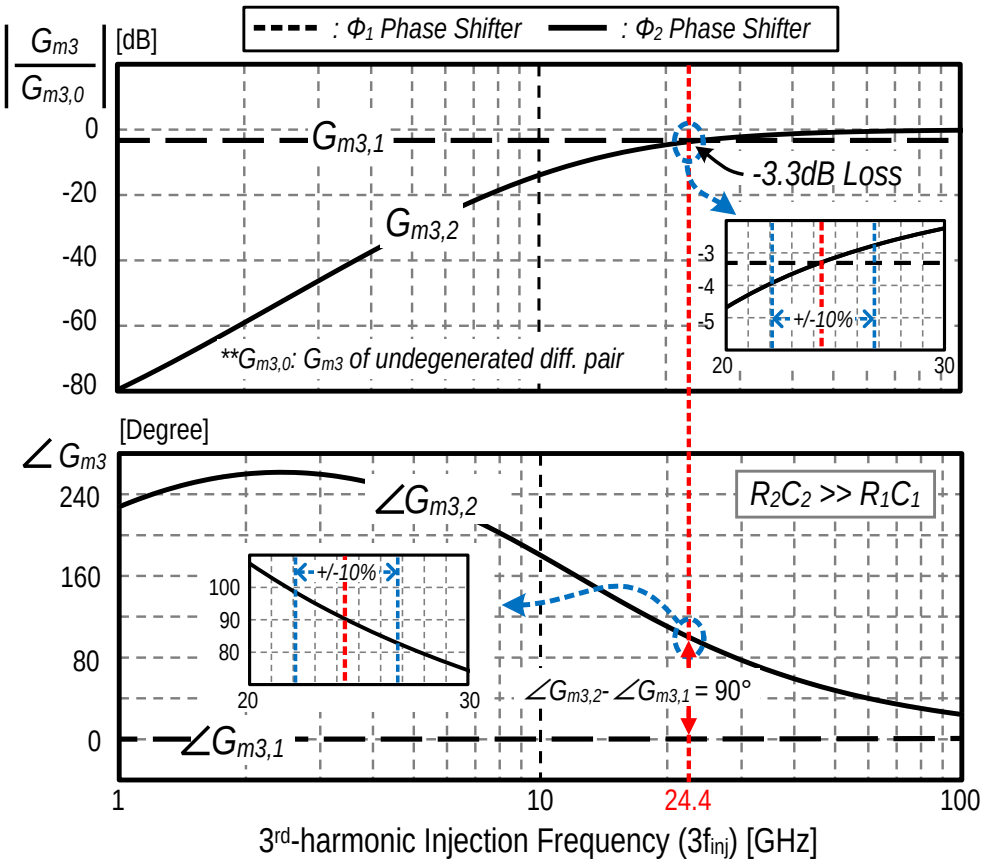
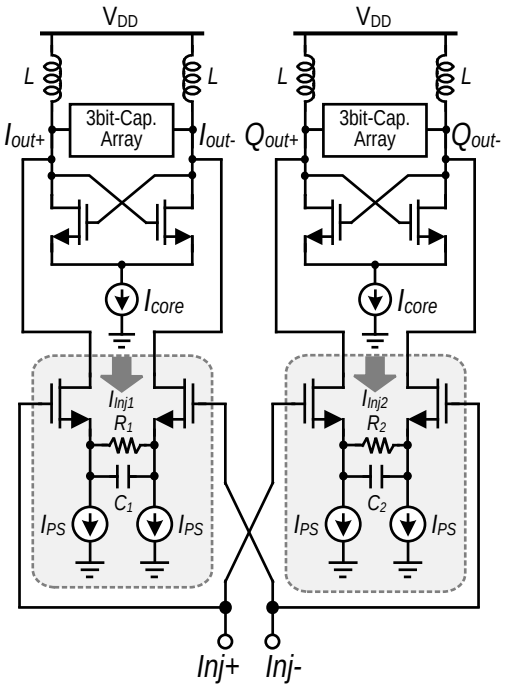
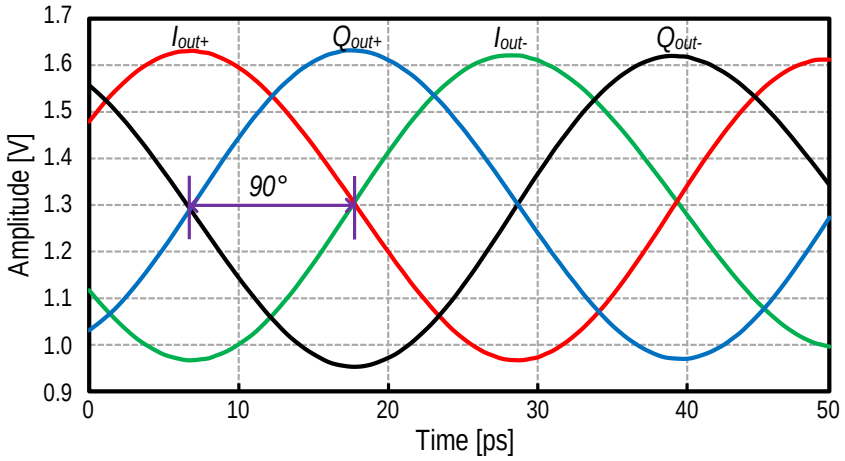



Fig. 3-7. Amplitude loss and phase shift due to two different capacitively-degenerated pairs.

proposed scheme has less injection loss and I/Q phase mismatch than the PPF-ILFT, which is indicated by the simulation results. Two phase shifts cause 90° phase difference with 3.3 dB injection loss at 24.4 GHz. Also, the phase error would be less than +/- 10° and the injection loss would approximately range from 2.8 dB to 4 dB when it comes to +/-10 % frequency variation. Fig. 3-8 shows the transient simulation result in the case of two standalone ILFTs without any quadrature coupling. As shown in the schematic, the




(a)




(b)

Fig. 3-8. Case of two standalone triplers without quadrature coupling: (a) schematic and (b) transient simulation results.

differential injection signal is individually injected into two ILFTs whose phase shifters result in different phase shifts ($\Phi_1$, $\Phi_2$). The simulated waveforms shows 90° phase difference among four signals with slight amplitude mismatch. Therefore, this simulation

result shows that two ILFTs can create quadrature output signals without quadrature coupling just by using two capacitive-degenerated pairs at third harmonic. Note that the quadrature coupling is usually used to minimize phase error and amplitude mismatch of ILFT outputs due to them of the injection signals.

## 3.4 Experimental Results

The proposed quadrature ILFT using capacitive degeneration has been implemented in a 130 nm CMOS process, and its chip photograph is shown in Fig. 3-9. The core chip area without the pads is 0.5 x 0.25 $mm^2$. The ILFT was characterized with on-wafer testing using GSSG probes for RF signal measurement. A signal generator (R&S SMF100A) and a spectrum analyzer (R&S FSW67) were used for the injection signal, and for the output spectrum and phase noise measurement, respectively.

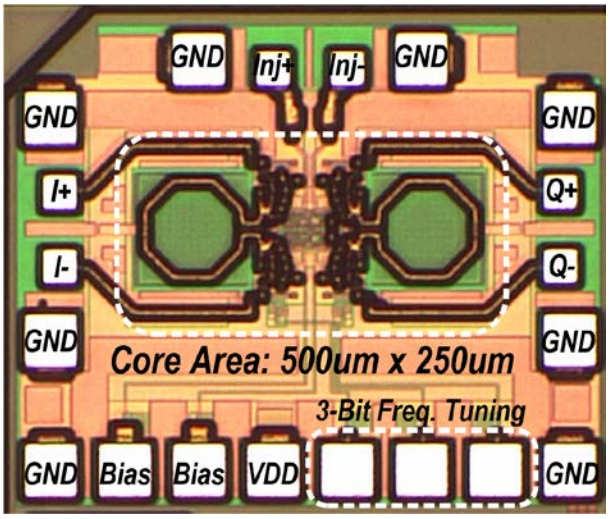
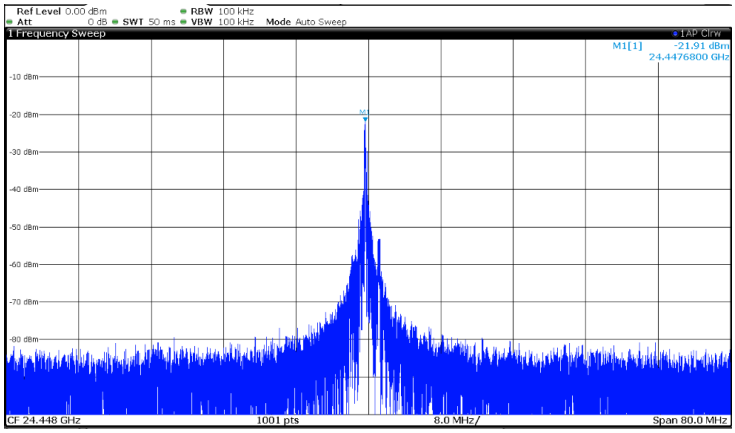
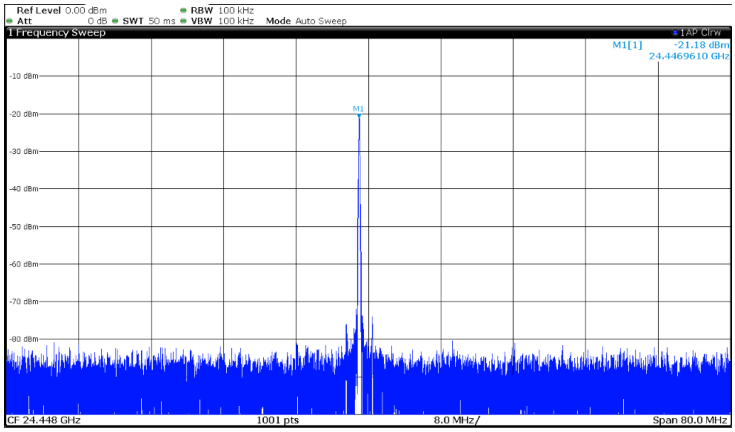


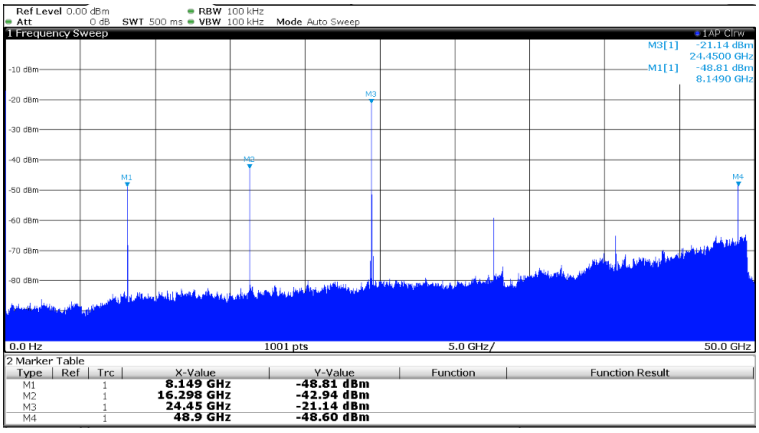

Fig. 3-9. Chip microphotograph of the proposed ILFT.




(a)




(b)




(c)

Fig. 3-10. Measured output spectra of the ILFT under (a) free-running, (b) injection-locked and (c) whole spectrum.

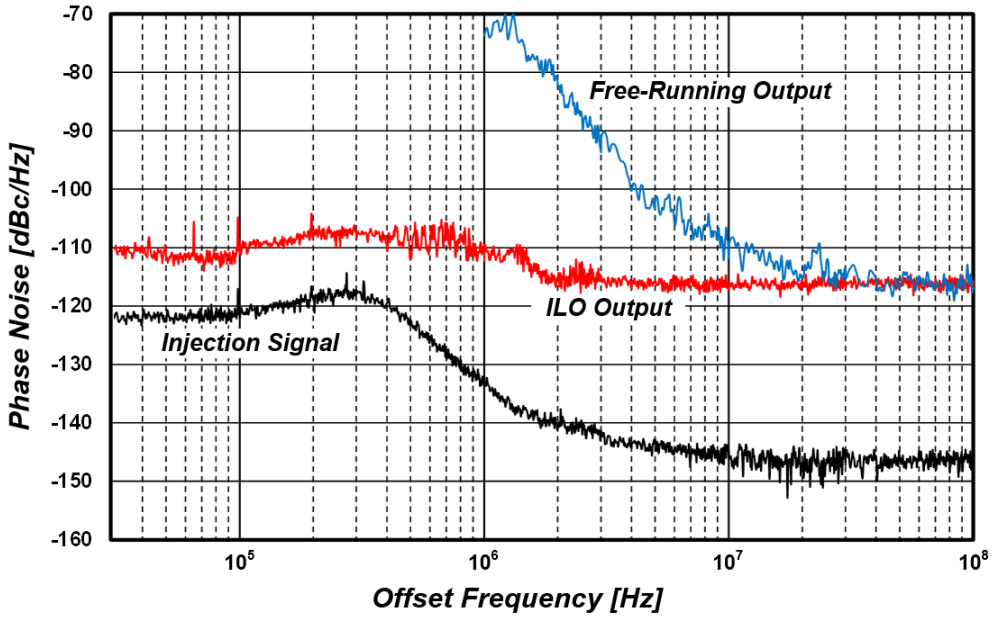



Fig. 3-11. Phase noise measurement of free-running output, injection signal and injection-locked tripler output.

The measured output spectra of the ILFT under free-running, injection-unlocked and whole spectrum by 8.149 GHz injection signal are shown in Fig. 3-10, excluding cable and probe loss calibration. Fig. 3-10(a) shows the free-running spectrum at 24.44 GHz with about -22 dBm output power. When injecting the signal of 8.149 GHz, which is one-third of free-running frequency, Fig. 3-10(b) shows that the output phase noise of the ILFT under injection-locking is appreciably improved compared to that under free-running condition. As shown in Fig. 3-10(c), the output power of the third harmonic is approximately -21 dBm, while the fundamental is suppressed by more than 27 dB with an input power of 0 dBm. The measured phase noise performance of the output signal, when the injection signal is 8.149 GHz and the ILFT is injection-locked to about 24.45 GHz, is shown in Fig. 3-11. The phase noise of output signal has -110 dBc/Hz at 100 kHz offset when that of the injection signal is -120 dBc/Hz. The phase noise difference is consistently about 10 dB below 300 kHz offset, which approximates to the expected theoretical value of $20\log_{10}(3)$. However, the output phase noise becomes degraded above 300 kHz offset because phase noise of the free-running frequency tripler dominates the output phase noise.

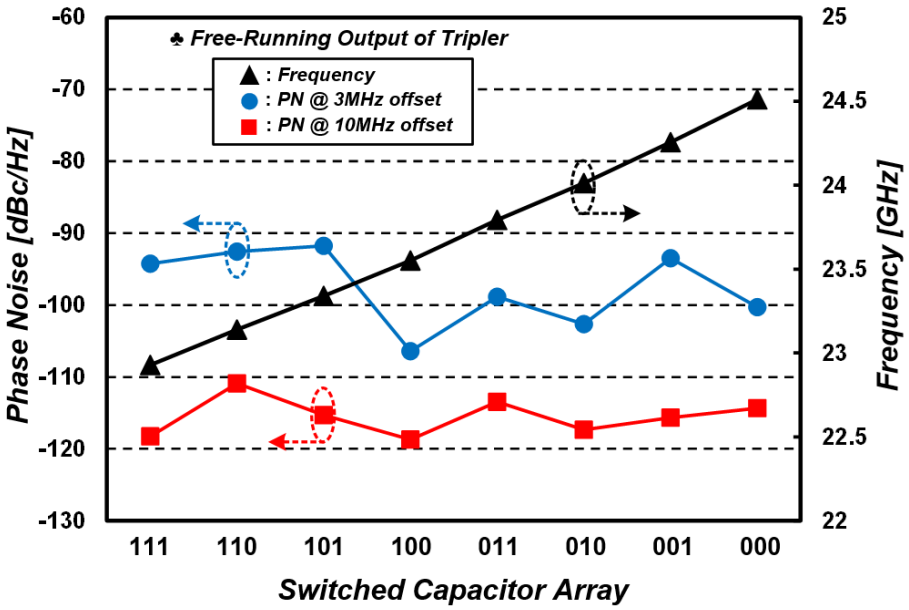



Fig. 3-12. Free-running frequencies of ILFT and their phase noise according to codes of switched capacitor array.

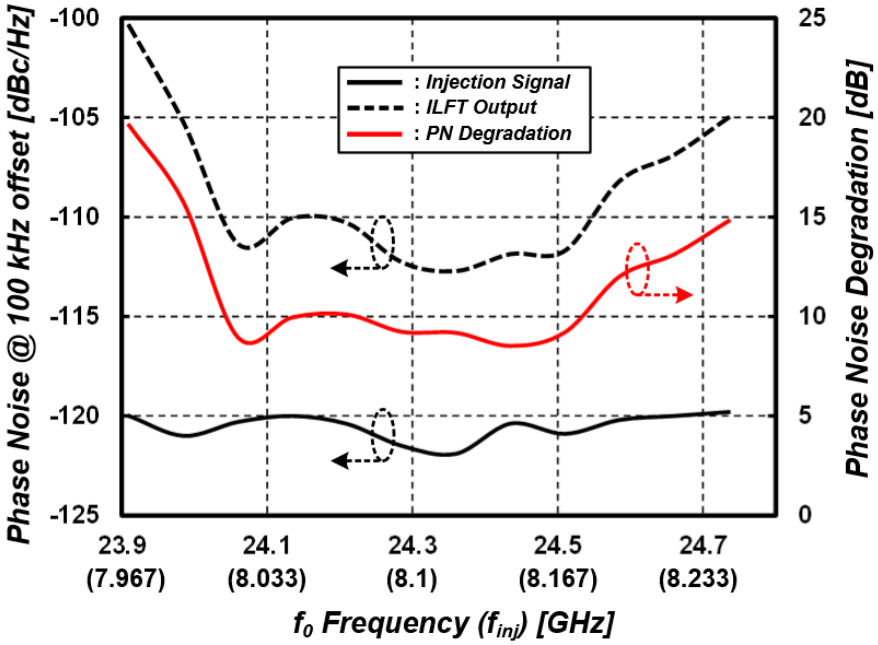



Fig. 3-13. Phase noise of injection signals and ILFT outputs and phase noise degradation within locking range.

The measured phase noise at free-running frequencies of the ILFT according to coarse tuning codes is shown in Fig. 3-12. The output signals range from 22.8 GHz to 24.4 GHz

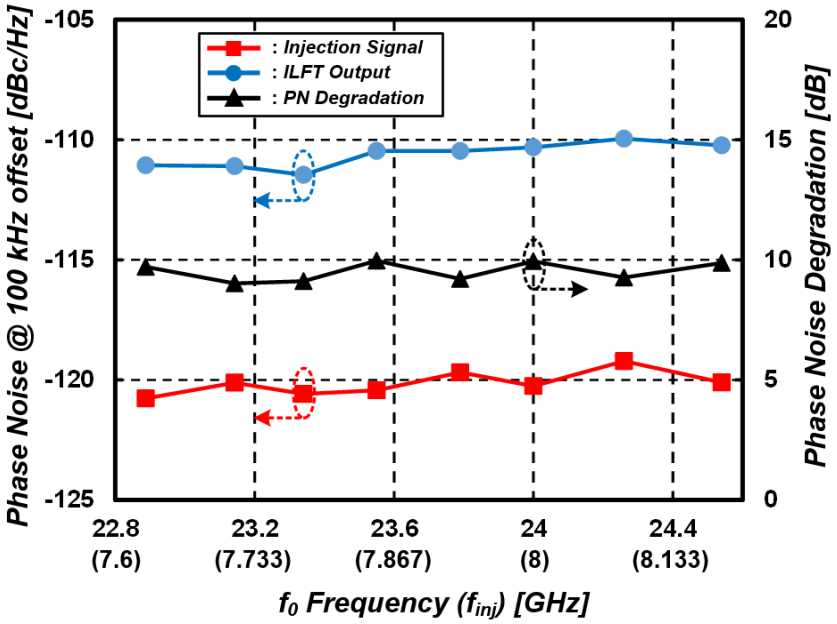



Fig. 3-14. Phase noise of injection signals and ILFT outputs and phase noise degradation within coarse tuning range.

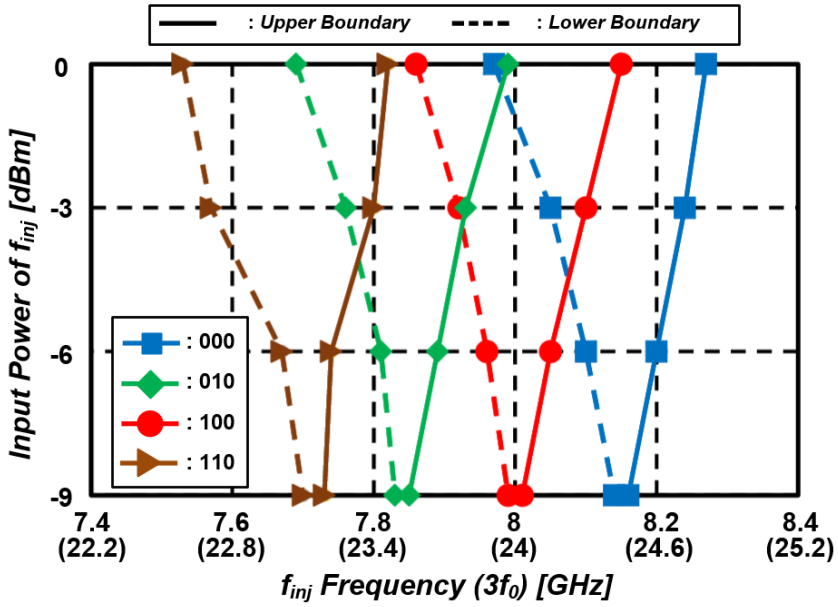



Fig. 3-15. Injection-locking range versus input injection power from -9 to 0 dBm.

according to 3-bit codes of the switched capacitor array. Their measured phase noise ranges from -90 dBc/Hz to -107 dBc/Hz and from -110 dBc/Hz to -120 dBc/Hz at 3 MHz and 10

TABLE 3.3. PERFORMANCE COMPARISON WITH PRIOR QUADRATURE ILFTS

| | [3-16] | [3-17] | [3-18] | [3-23] | [3-24] | This Work |
|---|---|---|---|---|---|---|
| **CMOS Process** | 65 nm | 65 nm | 90 nm | 130 nm | 40 nm | 130nm |
| **Injection Type** | SSI | SSI | PPF | QVCO | I/Q Inj. | HPS |
| **Frequency (GHz)** | 67.4 | 60 | 60 | 29.7 | 60 | 24 |
| **Locking Range (%)** | 0.7[1)] | 0.63 | 13.3 | 1[4)] | 3.5 | 3.3 |
| **Input Signal (dBm or V)** | 0 dBm | -2 dBm | 0 dBm | - | 650 $mV_{pp}$ | 0 dBm |
| **Output Power (dBm)** | -48 | -8[2)] | -27[3)] | -22 | -24 | -17 |
| **VDD (V)** | 1.2 | 1.2 | 1 | 1.3 | 1.3 | 1.3 |

[1)] Prelayout simulation result on [3-16] [2)] Calibrated output power
[3)] With about 20 dB gain of output buffer [4)] Without locking range calibration circuit

MHz offsets, respectively. When the injection signals, having phase noise at 100 kHz offset from -120 dBc/Hz to -122 at 8.1 GHz to 8.25 GHz, are applied to the ILFT, the measured phase noise of the ILFT ranges from -100 dBc/Hz to -112 dBc/Hz at 23.9 GHz to 24.74 GHz, as shown in Fig. 3-13. Since theoretical phase noise degradation is about 9.6 dB, the effective locking range of the ILFT is from 24.05 GHz to 24.6 GHz (about 550 MHz), which is 65.5 % of the injection-locking range. Fig. 3-14 shows the measured phase noise of injection signals and ILFT outputs and phase noise degradation within the coarse frequency tuning range. The ILFT outputs show consistent 9 to 10 dB phase noise degradation to that of the injection signals.

The measured locking ranges of the ILFT versus input injection power are shown in Fig. 3-15. The measured injection-locking ranges versus 2-bit LSB codes of the switched capacitor array are from 100 MHz to 850 MHz, while the input injection power varies from -9 to 0 dBm.

Table 3.3 compares the proposed quadrature ILFT with prior works according to injection types. Although the locking range can be widened by very small output power as in [3-18], the proposed injection type has maximized the locking range of 3.3% and output

power of -17 dBm. The locking range is on a par with the I/Q injection type presented in [3-24]. Also, the proposed scheme has improved locking range compared to SSI and QVCO approaches.

## 3.5 Summary

A quadrature ILFT using third harmonic phase shifters has been proposed and analyzed. Characteristics of the proposed ILFT have been compared to conventional quadrature ILFTs using single-phase differential injection. The proposed ILFT produces less injection loss due to third harmonic phase shifters, maximizing the injection-locking range. To verify performance of the proposed ILFT, a test chip was been designed and fabricated using 130 nm CMOS technology. The prototype ILFT can achieve the injection-locking range of 3.3% at 23.6 GHz with 0 dBm input injection power. The locking range of the proposed IFLT is on a par with that of conventional IFLTs using quadrature injection.

Although a quadrature ILFT using single-phase differential injection has a narrower injection-locking range than one of using quadrature injection, it is still an attractive solution because of the challenging design of a quadrature injection signal generator and quadrature LO distribution system in the conventional approaches. Therefore, the proposed ILFT provides great potential for low-phase noise quadrature signal generation in millimeter-wave frequency synthesizers.

## 3.6 References


[3-1] L. Zhou, C.-C. Wang, Z. Chen, and P. Heydari, "A W-band CMOS receiver chipset for millimeter-wave radiometer systems," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 378–391, Feb. 2011.

[3-2] Y.-L. Yeh and H.-Y. Chang, "A W-band wide locking range and low DC power injection-locked frequency tripler using transformer coupled technique," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 860–870, Feb. 2013.

[3-3] M.-C. Chen and C.-Y. Wu, "Design and analysis of CMOS subharmonic injection-locked frequency triplers," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 8, pp. 1869–1878, Aug. 2008.

[3-4] B. M. Helal, C.-M. Hsu, K. Johnson, and M. H. Perrott, "A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.

[3-5] E. Monaco, M. Pozzoni, F. Svelto, and A. Mazzanti, "Injection-locked CMOS frequency doublers for μ-wave and mm-wave applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1565–1574, Aug. 2010.

[3-6] T.-N. Luo and Y.-J. E. Chen, "0.8-mW 55-GHz dual-injection-locked CMOS frequency divider," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 3, pp. 620–625, Mar. 2008.

[3-7] Y.-L. Yeh and H.-Y. Chang, "Design and analysis of a W-band divideby-three injection-locked frequency divider using second harmonic enhancement technique," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1617–1625, Jun. 2012.

[3-8] J. Lee and B. Razavi, "A 40-GHz frequency divider in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 594–601, Apr. 2004.

[3-9] B. Razavi, “A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider,” *IEEE J. Solid-State Circui*ts, vol. 43, no. 2, pp. 477–485, Feb. 2008.

[3-10] Y.-H. Kuo, J.-H. Tsai, T.-W. Huang, and H. Wang, “Design and Analysis of Digital-Assisted Bandwidth-Enhanced Miller Divider in 0.18-mm CMOS Process,” *IEEE Trans. Microw. Theory Techn*., vol. 60, no. 5, pp. 1307–1320, May 2012.

[3-11] C. Wang, Z. Chen, and P. Heydari, “W-band silicon-based frequency synthesizers using injection-locked and harmonic triplers,” *IEEE Trans. Microw. Theory Techn*., vol. 60, no. 5, pp. 1307–1320, May 2012.

[3-12] P. K. Tsai and T. H. Huang, “Integration of current-reused VCO and frequency tripler for 24-GHz low-power phase-locked loop applications,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 4, pp. 199–203, Apr. 2012.

[3-13] S. Kang, J.-C. Chien, and A. Niknejad, “A W-band low-noise PLL with a fundamental VCO in SiGe for millimeter-wave applications,” *IEEE Trans. Microw. Theory Techn*., vol. 62, no. 10, pp. 2390–2404, Oct. 2014.

[3-14] B. Razavi, “A study of injection locking and pulling in oscillators,” *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[3-15] F. Yuan and Y. Zhou, “A phasor-domain study of lock range of harmonic oscillators with multiple injections,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, pp. 466–470 vol. 59, no. 8, Aug. 2012.

[3-16] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, “A compact, low-power and low-jitter dual-loop injection locked PLL using all-digital PVT calibration,” *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan. 2014.

[3-17] W. Deng et al., “A sub-harmonic injection-locked quadrature frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers,” *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1710–1720, Jul. 2013.

[3-18] W. Chan and J. Long, “A 56–65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2739–2746, Dec. 2008.

[3-19] S. Kalia, S. Patnaik, B. Sadhu, M. Sturm, M. Elbadry, and R. Harjani, “Multi-beam spatio-spectral beamforming receiver for wideband phased arrays,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 8, pp. 2018–2029, Aug. 2013.

[3-20] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, “A 900-MHz CMOS LC-oscillator with quadrature outputs,” in *IEEE Int. Solid-State Circuits Conf. Tech. Dig*., Feb. 1996, pp. 392–393.

[3-21] H. Tong, S. Cheng, Y.-C. Lo, A. Karsilayan, and J. Silva-Martinez, “An LC quadrature VCO using capacitive source degeneration coupling to eliminate bi-modal oscillation,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 9, pp. 1871–1879, Sep. 2012.

[3-22] J. Zhou, et.al., “A 0.4–6-GHz frequency synthesizer using dual-mode VCO for software-defined radio,” *IEEE Trans. Microw. Theory Techn*., vol. 61, no. 2, pp. 848-859, Feb. 2013.

[3-23] D. Shin, S. Raman, and K.-J. Koh, “A mixed-mode injection frequency-locked loop for self-calibration of injection locking range and phase noise in 0.13μm CMOS,” in *IEEE Int. Solid-State Circuits Conf. Tech. Dig*., pp. 50–51, Feb. 2016.

# Chapter 4.

# An Injection-Locked Clock Multiplier Using Envelope-Based Frequency Tracking Loop

## 4.1 Introduction

Recently, a sub-harmonically injection-locked clock multiplier (ILCM) has been an effective way of sup-pressing phase noise of an LC-VCO due to periodic injection locking of the VCO from a clean reference source. When injection locked, phase noise of the VCO becomes $20\log_{10}N$ more than that of the reference source, where $N$ is the number of frequency multiplication. However, in practice, a typical ILCM suffers from phase noise degradation and reference spur increase due to existing frequency mismatch between the VCO's free-running frequency and the target frequency. To minimize the frequency mismatch, several techniques are proposed. First, an injection-locked PLL (ILPLL) is a common approach to correcting the frequency mismatch as the PLL makes the free-running frequency of the VCO close to $N$-times reference frequency [4-1]. However, since the pulse injection almost completely resets the accumulated phase difference, the PLL under the injection has difficulty in detecting the frequency drift due to temperature and voltage variations. Also, the ILPLL requires an injection timing calibration circuit [4-2] to minimize the timing error between the injection pulse and the VCO zero-crossing point, which causes a significant reference spur.

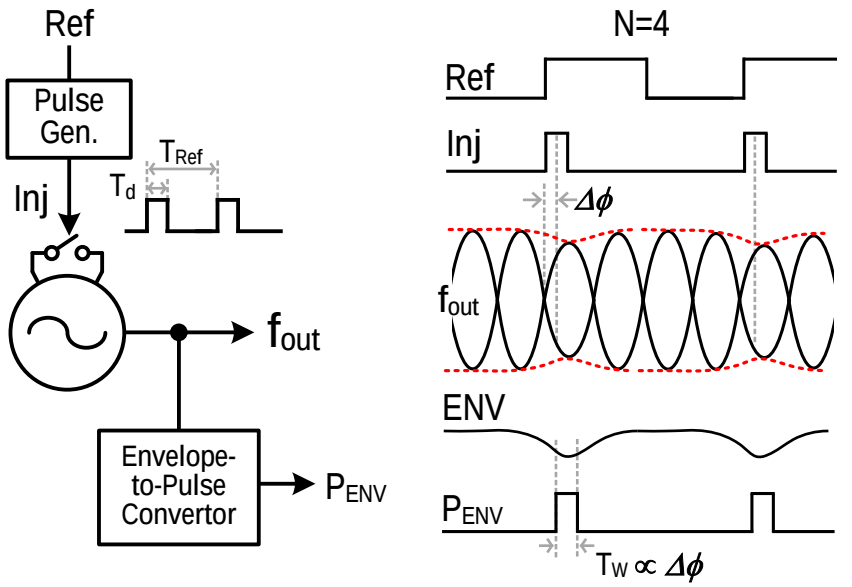
In the ILCM, use of a replica VCO can alleviate the drawbacks of ILPLL [4-3]. The ILCM uses two identical VCOs whose frequencies are controlled by the same control voltage. The main VCO is injection-locked by the reference pulse and the other VCO is controlled by a frequency-locked loop. Conceptually, the frequencies of two VCOs have to be the same under any process and temperature variations. However, a frequency difference between the two VCOs due to the inevitable mismatch in physical mismatch still results in performance degradation of the ILCM. Also, the two VCOs double both power and area. Another approach uses a pulse gating technique for a continuous FTL [4-4]. When the injection pulse is periodically disabled, the FTL detects and corrects the accumulated phase error. However, this technique still has some undetectable phase error due to finite width of the injection pulse.

In this work, we present a new continuous FTL for an ILCM. The proposed FTL is based on an envelope detector to continuously sense the frequency error. The envelope detection method can provide phase error detection under the injection. Therefore, it can minimize the phase error at PVT variation. This paper is organized as follows. Chapter 4.2 presents the proposed ILCM with the FTL. Then, experimental results are shown in Chapter 4.3 and the conclusions are given in Chapter 4.4.

## 4.2 Proposed ILCM with Envelope-Based FTL

### 4.2.1 Basic Concept of the Proposed Phase Detection

In general, pulse injection into an oscillator leads to perturbation of both amplitude and phase of the oscillator. Since the pulse injection causes difficulty in sensing an exact phase error, detecting the amplitude fluctuation can be considered as an optimal way to sense the phase error information previous to the pulse injection. As shown in Fig. 4-1, the proposed phase error detection method is based on an envelope detection technique. Due to the pulse injection, the envelope amplitude of the VCO output varies with the pulse position. An envelope-to-pulse convertor (EPC) is used to immediately detect and amplify the envelope



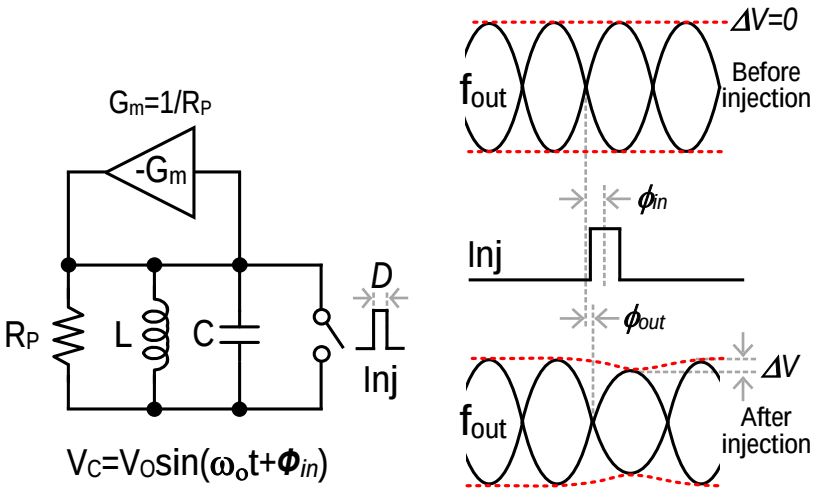

(a) (b)

Fig. 4-1. (a) Conceptual diagram of the proposed envelope-based phase detection. (b) Timing diagram.

wave for a rail-to-rail pulse signal. Then, the pulse signal (PENV) has a finite pulse width ($T_W$) which is proportional to the injection pulse width ($T_d$) and the absolute phase error ($\Delta\phi$) between the injection pulse and the crossing point of the VCO outputs. In order to utilize this pulse width for phase compensation, the phase directivity is required, which can be easily detected by a sub-sampling bang-bang phase detector (BBPD). Conceptually, the phase error can be cancelled out by applying the phase information to a charge pump like a typical CP-PLL. As a result, the free-running frequency of the LC-VCO is matched with *N*-times reference frequency. Furthermore, with the minimum allowable injection pulse width, reduction of the phase error can minimize the reference spur due to the pulse injection.

### 4.2.2 Envelope Wave of VCO with an Injection Pulse

When the reference pulse is injected into the LC-VCO, the initial phase error ($\phi in$) between the injection pulse and a crossing point of oscillator outputs is changed to the phase shift ($\phi out$) after the pulse injection as shown in Fig. 4-2. Also, the amplitude of the VCO outputs is distorted by the pulse injection. In order to mathematically calculate the initial




(a) (b)

Fig. 4-2. (a) Simplified half circuit of an LC-VCO with a pulse injection and (b) its phase relations before and after the injection.

phase error from the amplitude variation ($\Delta V$), a simplified half circuit of an LC-VCO with an injection transistor is used as shown in Fig. 4-2(b). The injection transistor is modeled in its on-resistance ($R_{on}$) state. Assume that RP is much greater than Ron, where RP is a parallel resistance of the LC tank. Initially, the voltage on the capacitor can be expressed as $V_O\sin(\omega_o t+\phi_{in})$, where $V_O$ is the amplitude of the LC tank and $\omega_o$ is the free-running frequency of the LC-VCO. After the pulse injection with a short pulse width of $D$, the capacitor voltage is degraded by a factor of

$$\gamma = 1 - e^{-(D/(R_{on}\cdot C))}. \tag{4-1}$$

Due to the pulse injection, the injection voltage (Vinj) on the LC tank can be expressed as

$$V_{Inj} = V\gamma\sin(\phi_{in}). \tag{4-2}$$

From the voltage phasor diagram in Fig. 4-3, the distorted amplitude ($V_O$) due to the pulse injection can be calculated by

$$V_O^2 = \left(V\cos(\phi_{in})\right)^2 + \left(V\left(1-\gamma\right)\sin(\phi_{in})\right)^2$$

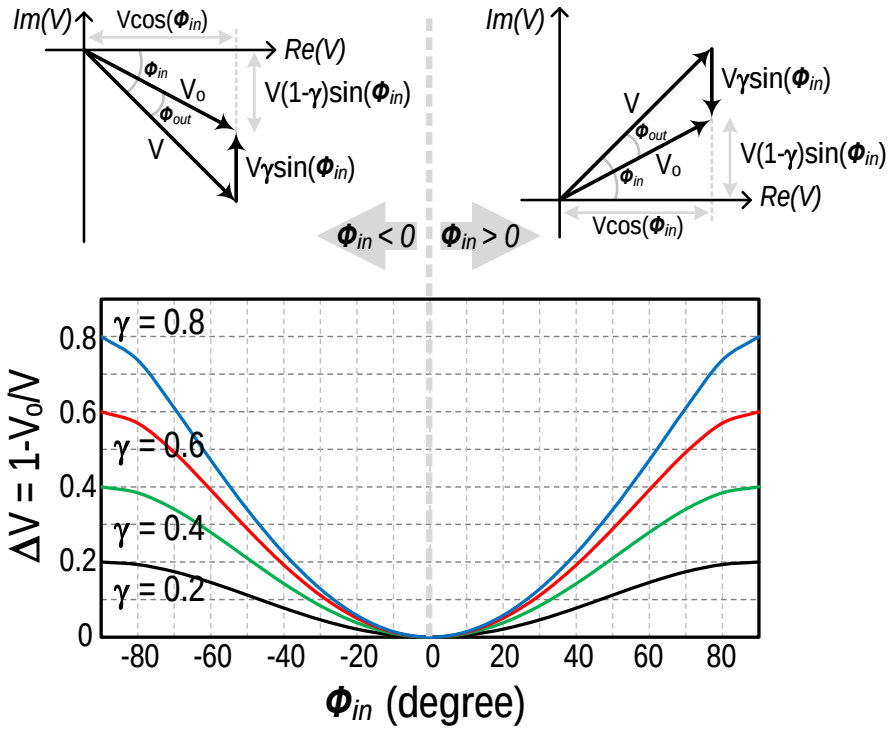



Fig. 4-3. Voltage phasor diagram over the input phase error and transfer curves of the amplitude variation and input phase error with γ = 0.2, 0.4, 0.6, and 0.8.

$$V_O = V\sqrt{\cos^2(\phi_{in}) + (1-\gamma)^2 \sin^2(\phi_{in})}\,. \tag{4-3}$$

Fig. 4-3 shows the transfer curve of the amplitude variation ($\Delta V$=1-$V_O/V$) using (4-3) when γ = 0.2, 0.4, 0.6, and 0.8. The curves in Fig. 4-3 indicate that $\Delta V$ increases as either γ or the absolute phase error increases. For example, when γ = 0.4, $\Delta V$ exponentially increases with the absolute phase error increase and then reaches 0.4 at $\phi_{in}$ = -π/2 and π/2. Also, as γ increases, a maximum $\Delta V$ follows a factor of γ. However, as mentioned before, for the phase error correction, the directivity of the phase error is required to apply this amplitude information.

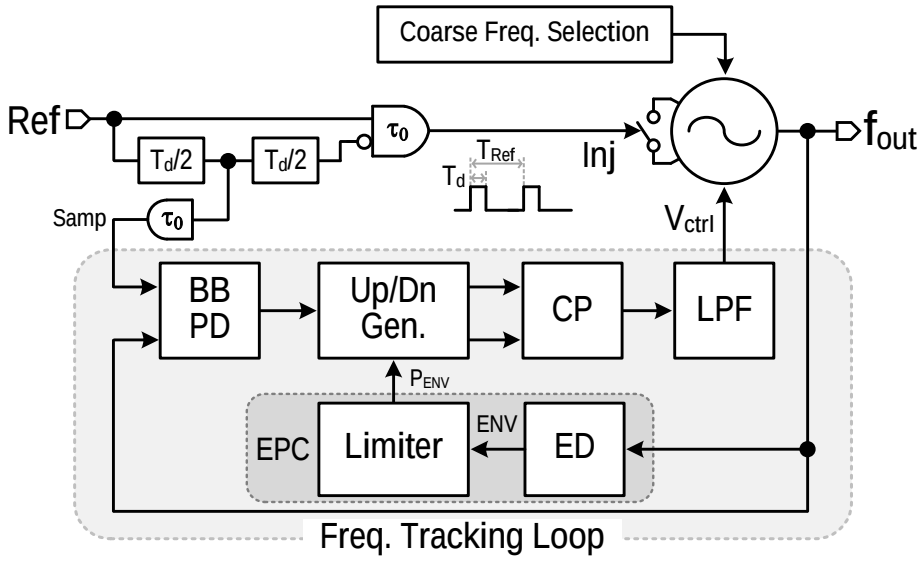



Fig. 4-4. Black diagram of the proposed ILCM.

### 4.2.3 Overall ILCM Structure

Fig. 4-4 shows the overall block diagram of the proposed ILCM. It consists of an injection pulse generator, FTL, and injection-locked LC-VCO. The LC-VCO is composed of a conventional cross-coupled oscillator, varactor, 3bit-switched capacitor, and injection transistor. The operation of the proposed scheme is the same as typical CP-PLLs. First, the coarse frequency tuning in the LC-VCO is performed to be close to *N* times the reference frequency and within the lock-in range by controlling the 3bit-switched capacitor. Although the pulse injection immediately corrects the phase error (or the frequency mismatch) due to the coarse frequency tuning, the remaining phase error causes the reference spur and phase noise degradation [4-4]. In order to minimize this phase error, the FTL continuously corrects it by using the envelope detection method. The EPC consists of an envelope detector and limiter as shown in Fig. 4-5 [4-5]. Once the reference pulse is injected into the LC-VCO, the envelope detector, which is a source follower type, extracts the envelope wave of the distorted VCO outputs due to the phase error. The envelope wave is converted into a pulse signal by the limiter to detect the phase error from its pulse width. The limiter is comprised

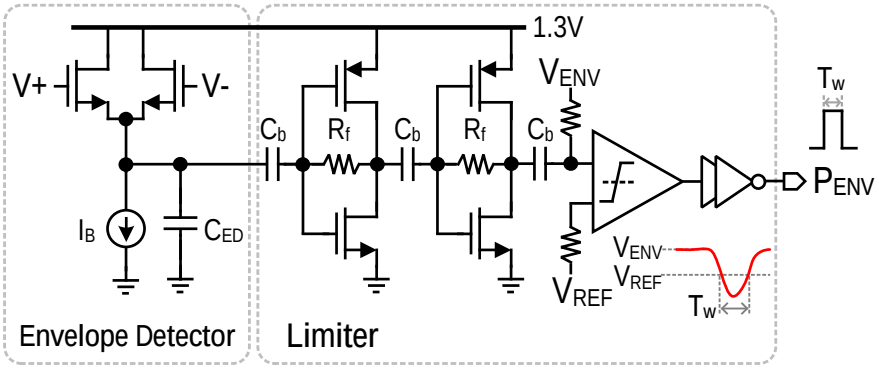
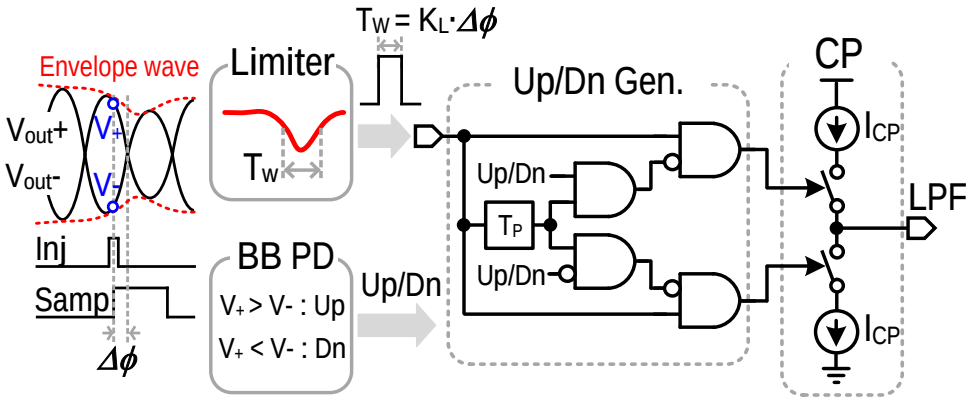


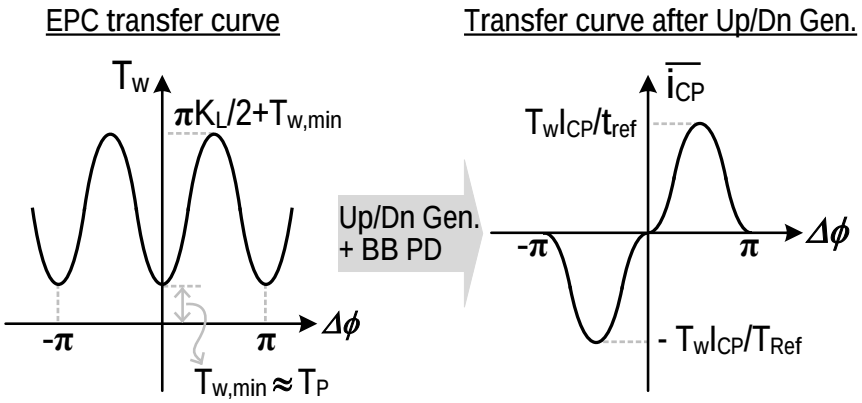

Fig. 4-5. Schematic of the envelope-to-phase convertor.

of two-stage AC-coupled CMOS inverter amplifiers and a comparator. The amplified envelope wave is compared with the reference voltage ($V_{REF}$) to determine the pulse width ($T_w$). Assume that a total conversion gain of the EPC is $K_L$. Therefore, $T_w$ is proportional to the absolute phase error by a factor of $K_L$.

In order to decide the directivity of calibration, a sub-sampling BBPD is required [4-6]. As shown in Fig. 4-6(a), the sampling signal (*Samp*) applied to the BBPD senses voltage difference between differential outputs of the LC-VCO, where the sampling signal is the reference injection clock delayed by $T_d/2$. When *V*+ is greater than *V*-, the BBPD outputs an up signal and when *V*- is greater than *V*+, it generates a down signal. Since the sampling signal is generated by extracting the signal at the middle of a delay line for the injection pulse width, its rising edge is always located at the center of the injection pulse, regardless of PVT variation. Fig. 4-6 (b) shows the transfer curves of the EPC and the up/dn convertor. The transfer curve of the EPC always has plus amounts of pulse width over plus and minus phase errors. It has the same curve as that of Fig. 4-3, which repeats every π period. Also, it has to have a minimum pulse width ($T_{w,min}$) which is caused by a finite injection pulse width (i.e. >30ps at 0.13μm CMOS technology). In the up/dn generator, $T_{w,min}$ can be cancelled out by adding a replica delay of $T_P$ to avoid the dead zone of the EPC like that of a typical PFD. The phase difference and its directivity are applied to the up/dn generator to generate up and down signals that then drive the charge pump to compensate for the phase




(a)




(b)

Fig. 4-6. (a) Control method for use of the envelope. (b) Transfer curves of the EPC before and after the up/dn generator and BBPD.

error by controlling $V_{ctrl}$ in the LC-VCO. As a result, the free-running frequency of the LC-VCO becomes $N$ times the reference frequency.

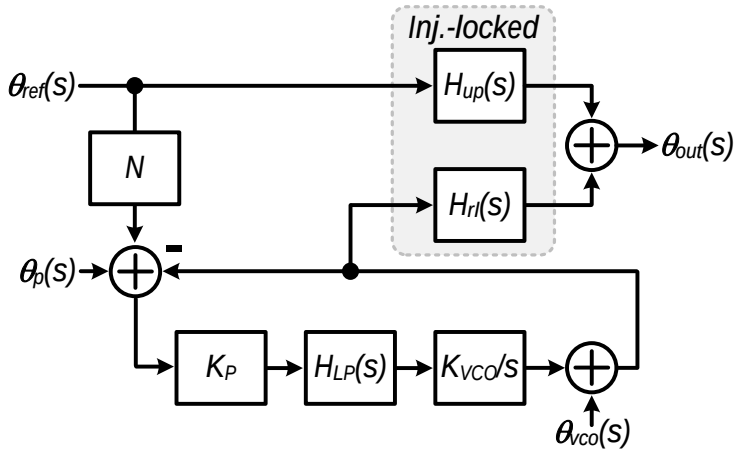



Fig. 4-7. Linear noise model of the proposed ILCM with FTL.

### 4.2.4 Phase Noise Analysis

Fig. 4-7 shows the linear noise model of the proposed ILCM with FTL, where $\theta_{ref}$ is the phase noise of the reference clock, $\theta_{vco}$ is that of the VCO, $\theta_p$ is that of the EPC and charge pump, and $\theta_{out}$ is that of the output. $H_{LP}(s)$ is a transfer function of the second-order passive loop filter, $K_{VCO}$ is the VCO gain, and $K_P$ is the gain of the EPC. $H_{up}(s)$ and $H_{rl}(s)$ represent the transfer function for the reference and VCO phase noise under pulse injection, respectively. From [4-7], $H_{up}(s)$ and $H_{rl}(s)$ can be expressed as

$$H_{up}(j\omega) = N \cdot \alpha(j\omega) \quad H_{rl}(j\omega) = 1 - \alpha(j\omega),$$

where

$$\alpha(j\omega) = \frac{\gamma}{1+(\gamma-1)e^{-j\omega T_{ref}}} e^{-j\omega\frac{T_{ref}}{2}} \operatorname{sinc}\left(\omega\frac{T_{ref}}{2}\right). \tag{4-4}$$

In (4-4), the output phase noise caused by the reference signal has the transfer function of a low-pass filter while that caused by the VCO has the transfer function of a high-pass filter, where 3-dB bandwidth is determined by γ.

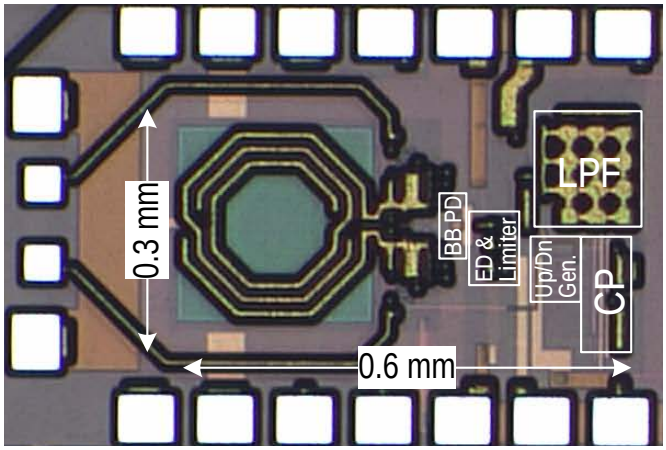



Fig. 4-8. Die photograph.

## 4.3 Measurement Results

The chip photograph of the proposed ILCM with FTL fabricated in 130 nm CMOS process is shown in Fig. 4-8. The active chip sizes of the ILCM and FTL are 0.3 x 0.6 $mm^2$. The total power consumption is 6 mW at a supply of 1.3 V. The ILCM is characterized with on-wafer testing using GSSG probes for RF signal transition at the VCO outputs.

The ILCM is locked to 5.15 GHz using a 5.15 MHz reference clock, with phase noise contributions shown in Fig. 4-9. The measured phase noise of the reference clock is around -156 dBc/Hz at 1 MHz offset. Once the reference clock is injected into the LC-VCO, the measured phase noise of the ILCM is -113 dBc/Hz at 1 MHz offset. It is observed that the phase noise degradation up to around 1 MHz offset is around 40 dB from the reference clock's phase noise level, consistent with the phase noise scaling by the frequency division factor of 100. The RMS jitter integrated from 1 kHz to 30 MHz is 201 fs. The measured output spectrum of ILCM with FTL at 5.15 GHz is shown in Fig. 4-10, where the measured reference spur magnitude is around -52 dBc.

Table 4.1 shows the performance summary of the proposed ILCM and comparison with prior injection-locked frequency multipliers. The proposed architecture achieves excellent jitter and spurious performance even with a large multiplication factor of 100. Compared to

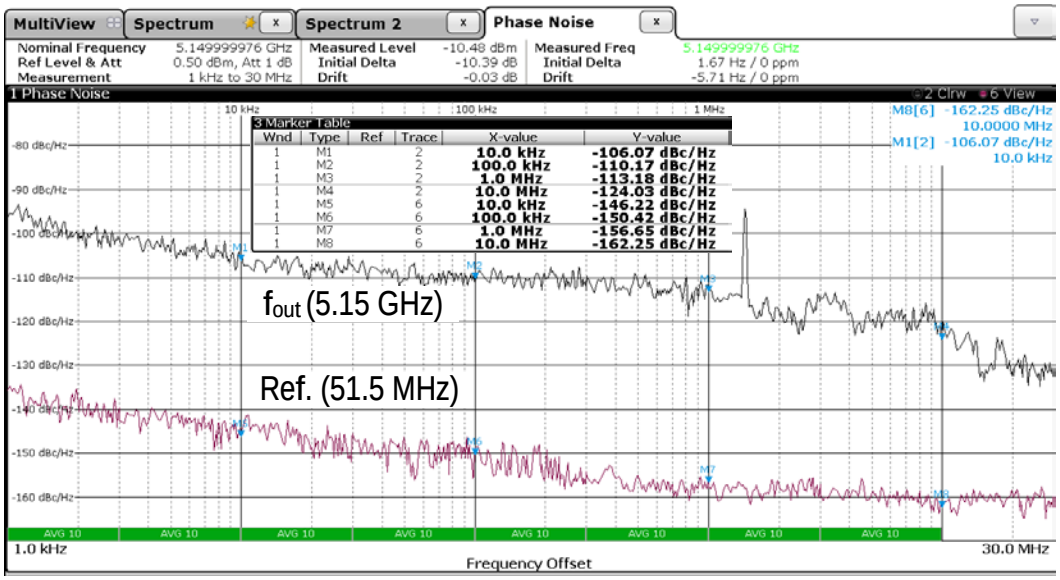



Fig. 4-9. Measured phase noise of the reference clock and the proposed ILFM.

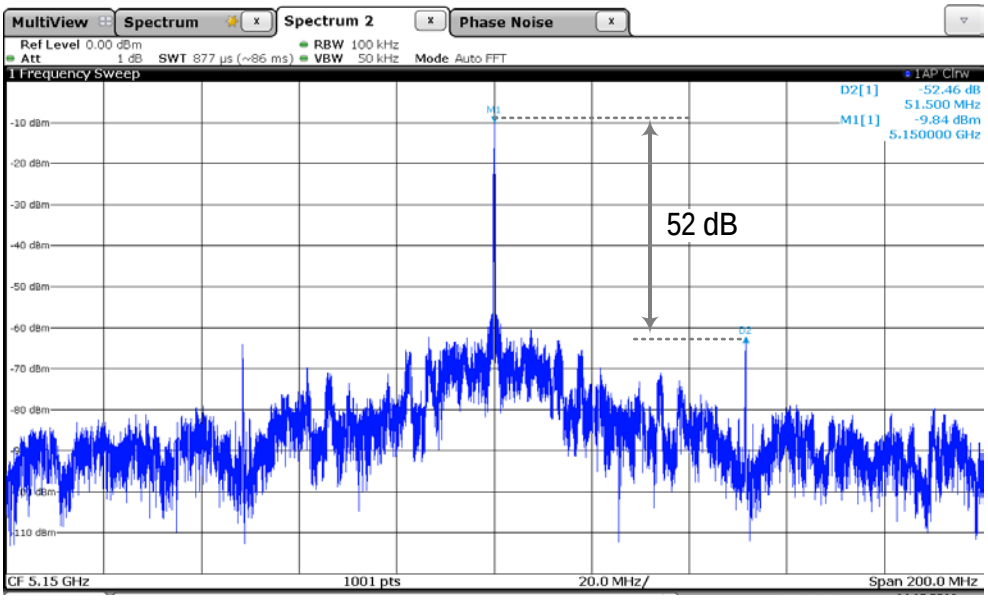



Fig. 4-10. Measured output spectrum of the proposed ILCM at 5.15GHz.

prior works, which rely on phase detection, the proposed FTL is based on a simple and accurate envelope detection technique that ensures robust operation across PVT variations.

TABLE 4.1. PERFORMANCE COMPARISON WITH PREVIOUS WORKS

| | Architecture | Detection Method | Tech (nm) | Freq. (GHz) | Div. Ratio (N) | Power (mW) | Ref. Spur (dBc) | PN @1MHz (dBc/Hz) | RMS Jitter ($\sigma_t$) | Chip Area ($mm^2$) | FOM (dB) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| [4-1] | LC-ILCM | Phase Detection | 90 CMOS | 20 | 20 | 38 | -46 | -113 | 110fs (50k~80MHz) | 0.455 | -243 |
| [4-2] | LC-ILPLL | Phase Detection | 180 CMOS | 2.4 | 16 | 12.6 | -39 | -129 | 145fs (1k~40MHz) | 0.64 | -246 |
| [4-5] | LC-ILPLL | Phase Detection | 65 CMOS | 2.4 | 16 | 5.2 | -49 | -126 | 188fs (1k~44MHz) | 0.25 | -247 |
| [4-6] | LC-ILCM | Phase Detection | 65 CMOS | 6.75-8.25 | 64 | 2.25 | -42 | -114.5 | 190fs (10k~100MHz) | 0.25 | -251 |
| This Work | LC-ILCM | Envelope Detection | 130 CMOS | 5.15 | 100 | 6 | -52 | -113 | 201fs (1k~30MHz) | 0.18 | -246 |

* FOM = $20\log(\sigma_t/1s) + 10\log(P_{dis}/1mW)$

## 4.4 Summary

This chapter presents an ILCM using envelope-based frequency tracking loop for a low phase noise signal. In the proposed technique, an envelope detector constantly monitors the VCO's output waveform distortion caused by frequency difference between the VCO frequency and reference frequency. Therefore, the proposed techniques can compensate for frequency variation of the VCO due to PVT variations.

## 4.5 References

[4-1] J. Lee and H. Wang, “Study of subharmonically injection-locked PLLs,” *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

[4-2] Y.-C. Huang and S.-I. Liu, “A 2.4-GHz subharmonically injection-locked PLL with self-calibrated injection timing,” *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 417–428, Feb. 2013.

[4-3] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, “A compact, low-power and low-jitter dual-loop injection locked PLL using all-digital PVT calibration,” *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan. 2014.

[4-4] A. Elkholy, M. Talegaonkar, T. Anand, and P. K. Hanumolu, “Design and analysis of low-power high-frequency robust sub-harmonic injection-locked clock multipliers,” *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3160–3174, Dec. 2015.

[4-5] D. Shin, S. Raman, and K.-J. Koh, “A mixed-mode injection frequency-locked loop for self-calibration of injection locking range and phase noise in 0.13μm CMOS,” in *IEEE Int. Solid-State Circuits Conf. Tech. Dig*., pp. 50–51, Feb. 2016.

[4-6] S.-Y. Cho et al., “A 5-GHz subharmonically injection-locked all-digital PLL with complementary switched injection,” in *Proc. Eur. Solid-State Circuit Conf.*, 2015, pp. 384–387.

[4-7] S. Ye, L. Jansson, and I. Galton, “AMultiple-crystal interface PLL with VCO realignment to reduce phase noise,” *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec. 2002.

# Chapter 5.

# A Sub-harmonically Injection-Locked PLL with 130 fs RMS Jitter at 24 GHz Using Synchronous Reference Pulse Injection from Nonlinear VCO Envelope Feedback

## 5.1 Introduction

Periodic injection locking of a VCO by a clean reference source in a sub-harmonically injection-locked PLL (SILPLL) is an effective way of suppressing the VCO phase noise. However, timing mismatch between the injection pulse and the VCO zero-crossing point can cause significant reference spurs. An open-loop injection timing alignment approach with a fixed delay in [5-1] is sensitive to PVT variations. The closed-loop technique in [5-2] detects the phase difference between reference clock and VCO-divided clock at the PFD input to generate an injection timing control signal, but poses a time offset ($T_{err}$) issue caused by the divider delay ($T_{div}$) plus finite injection pulse width ($T_d$) as shown in Fig. 5-1. $T_{err}$ is also sensitive to PVT variations and could be a significant fraction of the VCO half clock period, potentially generating a large spur, particularly at microwave and mm-wave frequencies. Fundamentally, the reference spur is the result of an amplitude modulation (AM) effect due to the time-mismatched reference pulse.

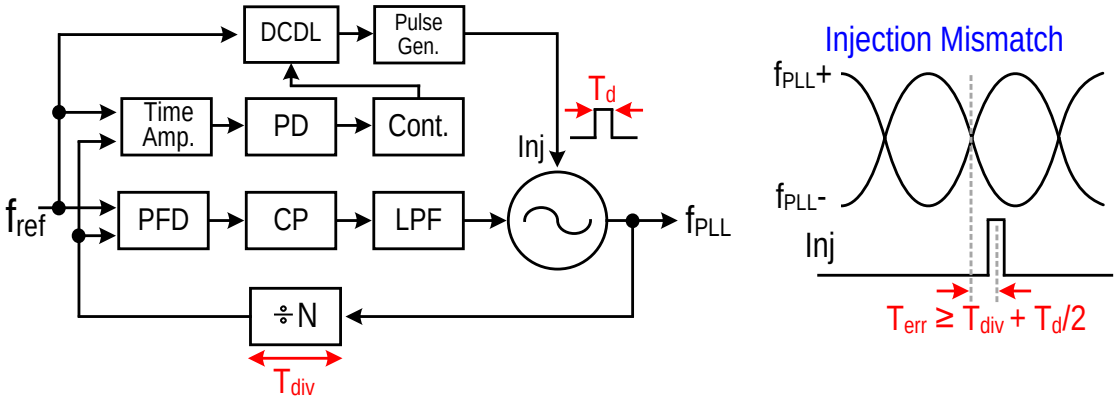



Fig. 5-1. Conventional SILPLL with injection timing calibration circuit.

In this work, a feedback injection-timing aligner as shown in Fig. 5-2 is proposed. An envelope detector (ED) similar to that in [5-3] is used here to detect optimal injection timing (in [5-3] the ED is used for injection-locking detection). The ED directly monitors VCO output envelope and senses the envelope's AM disturbance caused by injection pulse timing mismatch. Subsequently, the comparator following the ED output drives counters which control the amount of delay in a digitally controlled delay line (DCDL), controlling the pulse injection time in a closed-loop fashion at every rising and falling edge of the reference clock cycle. Therefore, the ED detects the optimal injection timing exactly regardless of the detection restrictions imposed by operation frequency, $T_{div}$, $T_d$, or any delays in digital control circuitry.

## 5.2 Proposed Frequency Multiplier

In Fig. 5-2, an integer-N PLL establishes frequency locking of the VCO to 8 GHz ($f_{PLL}$) using a 100-MHz reference clock (N=80). To generate 24-GHz quadrature outputs, the 8-GHz PLL output is directly fed to a third-harmonic quadrature injection-locked oscillator (QILO). The QILO employs RC phasing networks ($\Phi_1$ and $\Phi_2$) to set the phase difference of the 8 GHz PLL outputs to 30°, resulting in a 90° phase difference in the third-harmonic injection currents.

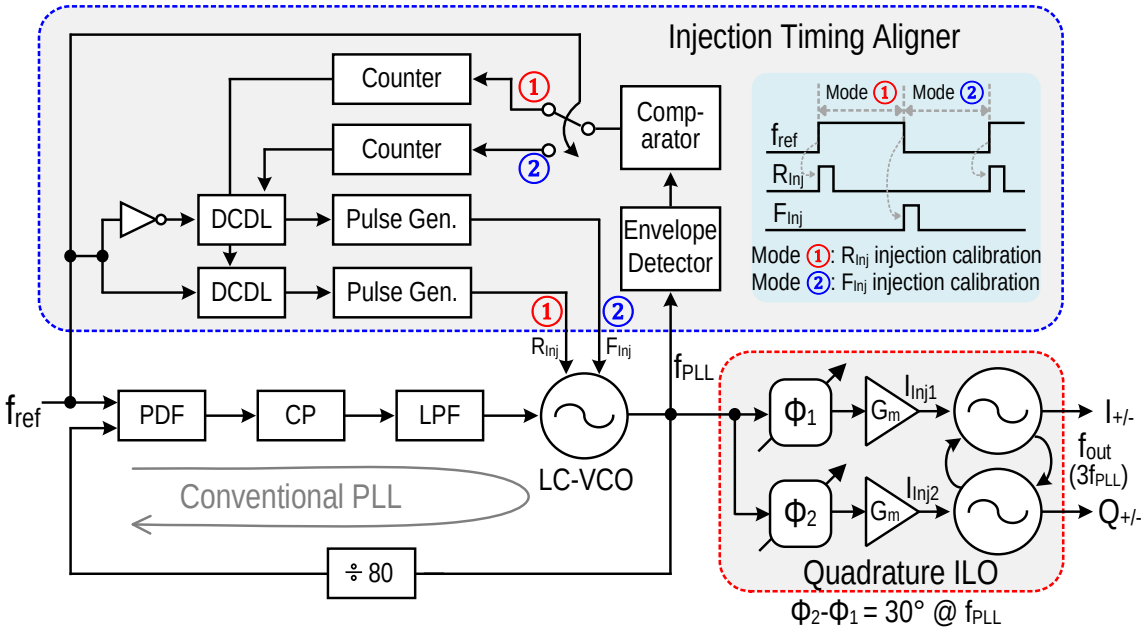



Fig. 5-2. Proposed envelope-detection based self-calibrated SILPLL with QILO.

### 5.2.1 Injection Timing Aligner

Fig. 5-3 shows the detailed schematic of the injection timing aligner. If an injection pulse is not optimally aligned with a zero-crossing point of the VCO outputs, it will instantly distort the VCO outputs and create an envelope variation whose amplitude is dependent on the injection time mismatch. The ED extracts the envelope distortion and amplifies it via a two-stage AC-coupled CMOS inverter amplifier. If the magnitude of the amplified AM signal ($V_{P,EW}$) is greater than the comparator's predetermined threshold point set by $\Delta V_{TR}=V_{ENV}-V_{REF}$, the comparator generates an enabling pulse which drives a 4-bit counter pair for every high and low level of the reference clock. Consequently, the counters increase the capacitance of the 4-bit DCDL by 1 LSB, equivalently delaying the injection pulses to the VCO by a corresponding 1 LSB time delay ($\Delta T$). The control loop completes the calibration when each injection pulse is located sufficiently closer to the zero-crossing of the VCO outputs so that $V_{P,EW}$ is smaller than $\Delta V_{TR}$, disabling the comparator.

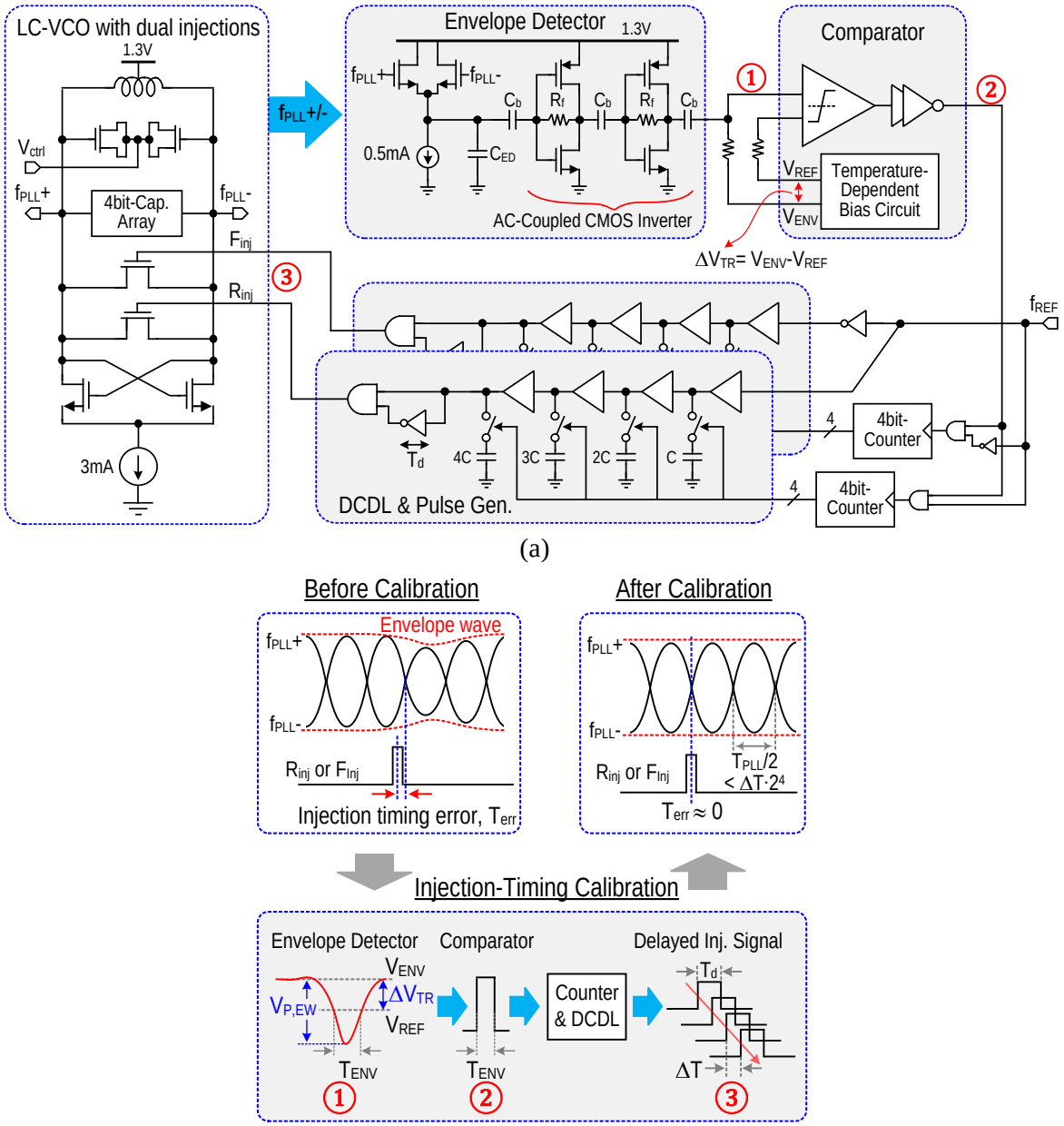



Fig. 5-3. (a) Schematic and (b) operation principle of the proposed injection timing aligner, which senses VCO envelope distortion caused by reference pulse injection timing mismatch.

## 5.2.2 Temperature Dependence of $V_{P,EW}$

In the envelope feedback aligner, the accuracy of the injection pulse position is dependent on the comparator threshold $\Delta V_{TR}$. Given the nonlinear nature of the envelope

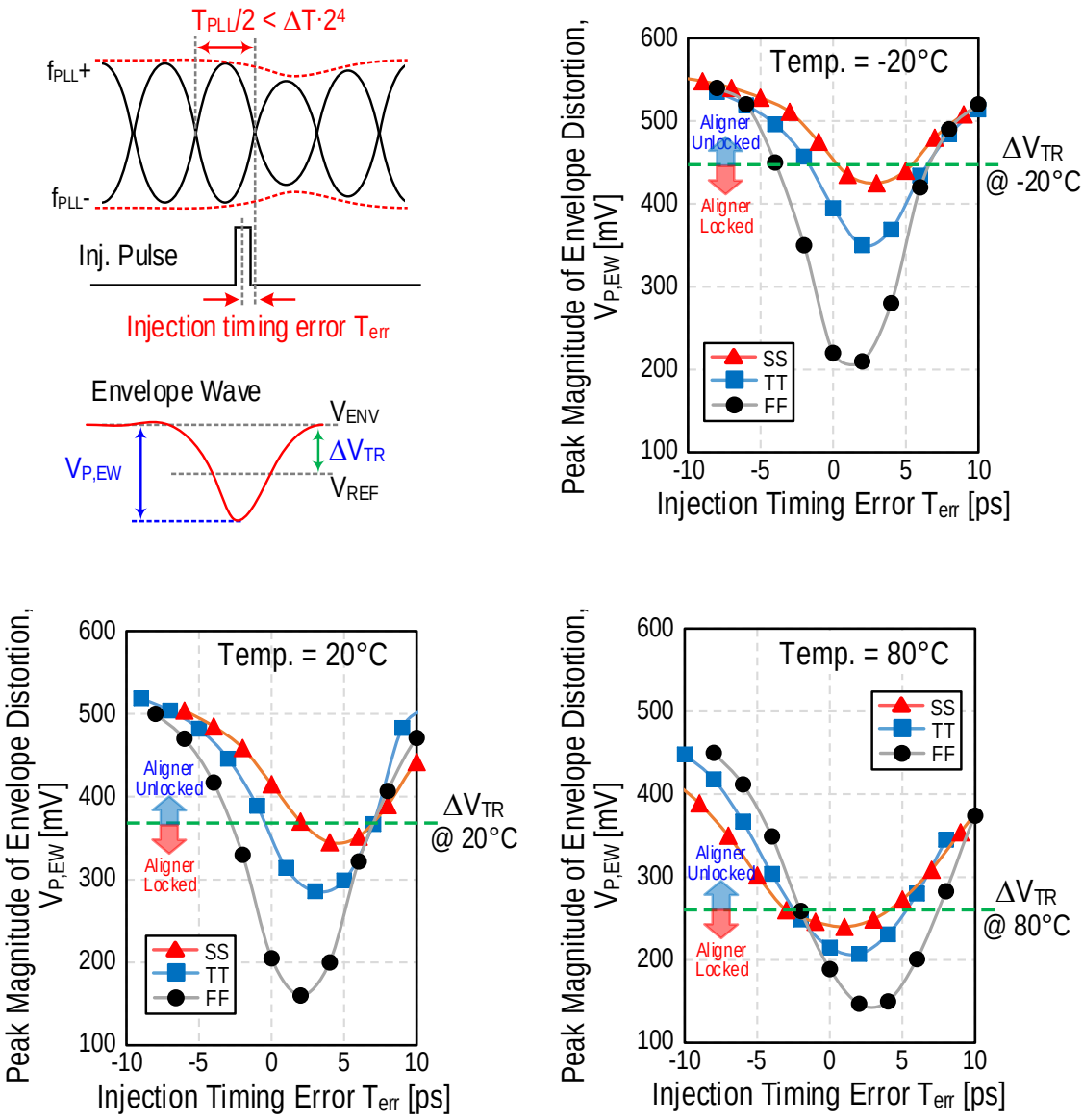



Fig. 5-4. Simulation results of peak magnitude of envelope distortion, $V_{P,EW}$ across process corners at T= -20/20/80°C.

distortion, the optimum $\Delta V_{TR}$ is obtained by a process corner-based analysis. $T_d$ of the injection pulse generator in Fig. 5-3 is ~40 ps, mainly limited by the inverter speed of the given 130 nm CMOS process. With the nominal gain setting of 20 dB for the 2-stage inverter-amplifier in the ED, the simulations over a full range of process variation reveal the minima of $V_{P,EW}$ spread over a $T_{err}$=0±5 ps span and vary by 150-to-420 mV over a -20-

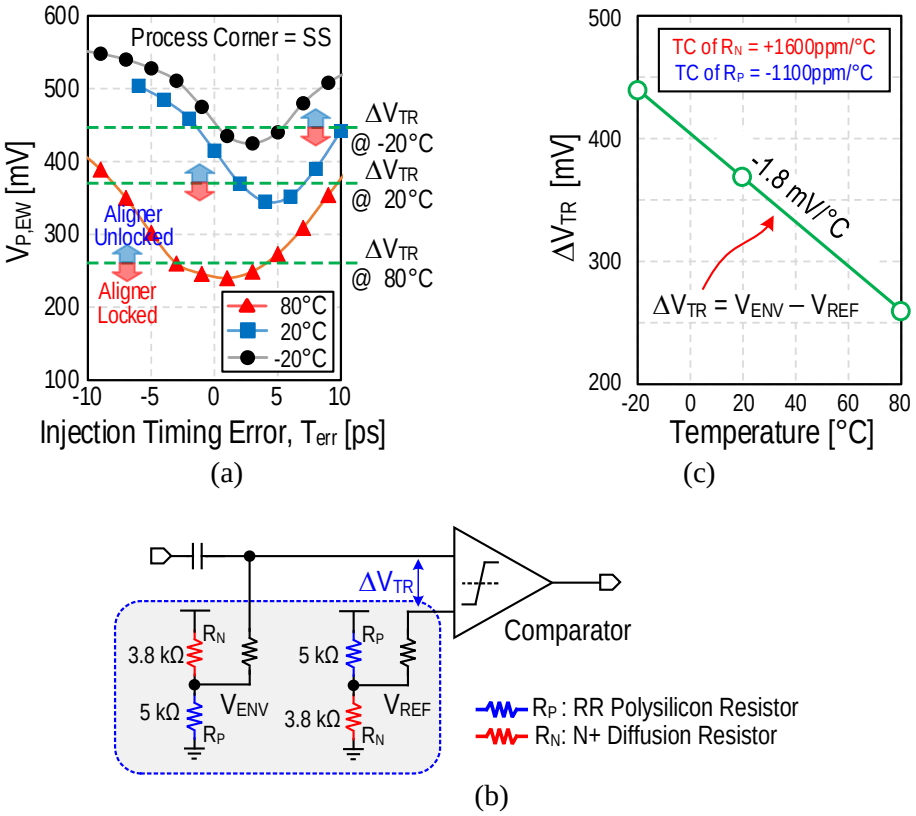



Fig. 5-5. Temperature-dependent $\Delta V_{TR}$ generation: (a) temperature dependency of $V_{P,EW}$ at SS process corner, (b) schematic of temperature-dependent bias circuit, (c) simulated temperature dependencies of $\Delta V_{TR}$ (solid) and $V_{P,EW}$ (circle).

to-80 °C temperature range as shown in Fig. 5-4. For a fixed temperature, the slow-slow (SS) corner exhibits the highest $V_{P,EW}$ over other corner models. Thus, $\Delta V_{TR}$ is set based on the SS corner and the simulation results are shown in Fig. 5-5(a). The minimum of $V_{P,EW}$ decreases progressively as temperature increases, from 420 mV at -20°C to 230 mV at 80°C. To track the $V_{P,EW}$ temperature dependency, $\Delta V_{TR}$ is generated using a temperature dependent bias circuit (as shown in Fig. 5-5(b)) leveraging an inverse temperature coefficient (TC) relation between a high-resistance polysilicon resistor ($R_P$) and an N+ diffusion resistor ($R_N$). In the given process, $R_P$ and $R_N$ have a negative and positive TCs, respectively, resulting in an overall negative TC of $\Delta V_{TR}=V_{DD}(R_P-R_N)/(R_P+R_N)$. Through temperature simulations, $R_P$ and $R_N$ are set to 5 kΩ and 3.8 kΩ, respectively, creating $\Delta V_{TR}$= 370 mV at

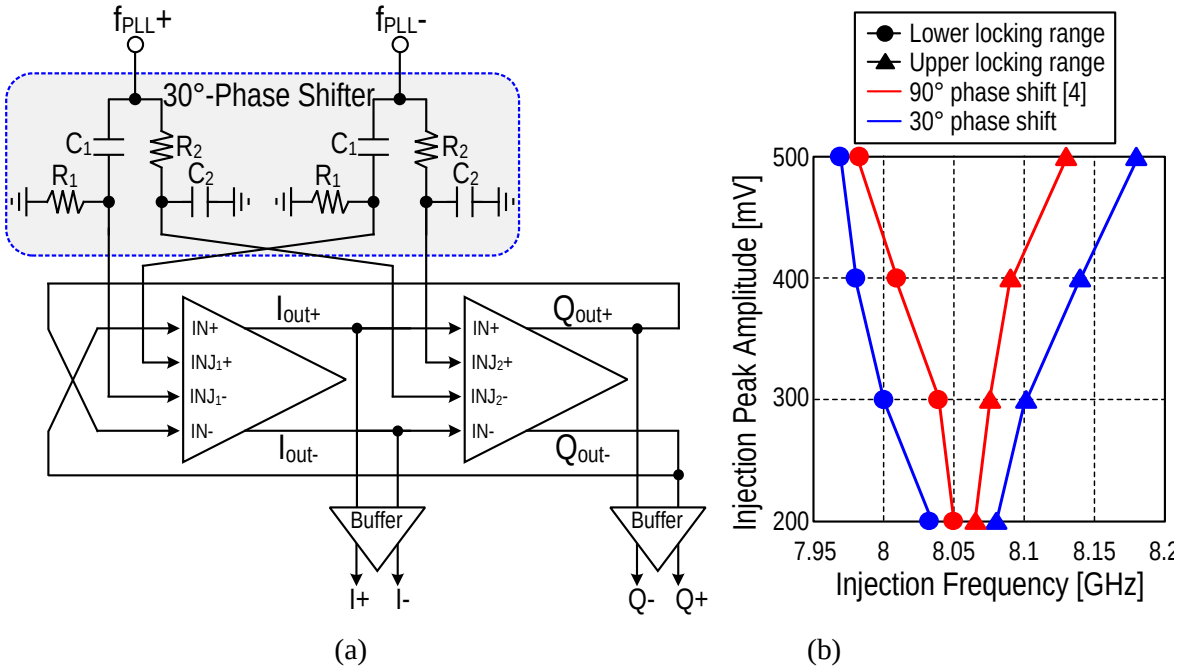



Fig. 5-6. (a) Schematic of QILO adopting 30° phase shifter, and (b) QILO locking range comparison.

T=20°C. The optimal comparator threshold gradient determined by $R_P$ and $R_N$ is $\partial\Delta V_{TR}/\Delta T$ $\approx$-1.8 mV/°C (line  in Fig. 5-5(c)) which tracks well with the $V_{P,EW}$ temperature dependency shown in Fig. 5 (a) at -20/20/80 °C (circles in Fig. 5-5(c)).

### 5.2.3 QILO with 30° Phase Shifter

In the RC-CR networks shown in Fig. 5-6(a), to achieve a maximum locking range by minimizing the voltage transfer loss, it is desirable to use a minimum time constant ($\tau_{RC}$) in the low-pass path since the loss increases as increasing $\tau_{RC}$. Consequently, the phase lag by the low-pass $R_2$-$C_2$ and the phase lead by the high-pass $C_1$-$R_1$ are set to -15° and +15°, respectively, at 8 GHz, resulting in

$$\frac{R_1C_1}{R_2C_2}=\frac{\tan 75^\circ}{\tan 15^\circ}\approx 14. \tag{5-1}$$

At the third-harmonic band, the amount of phase shift increases proportionally by the factor

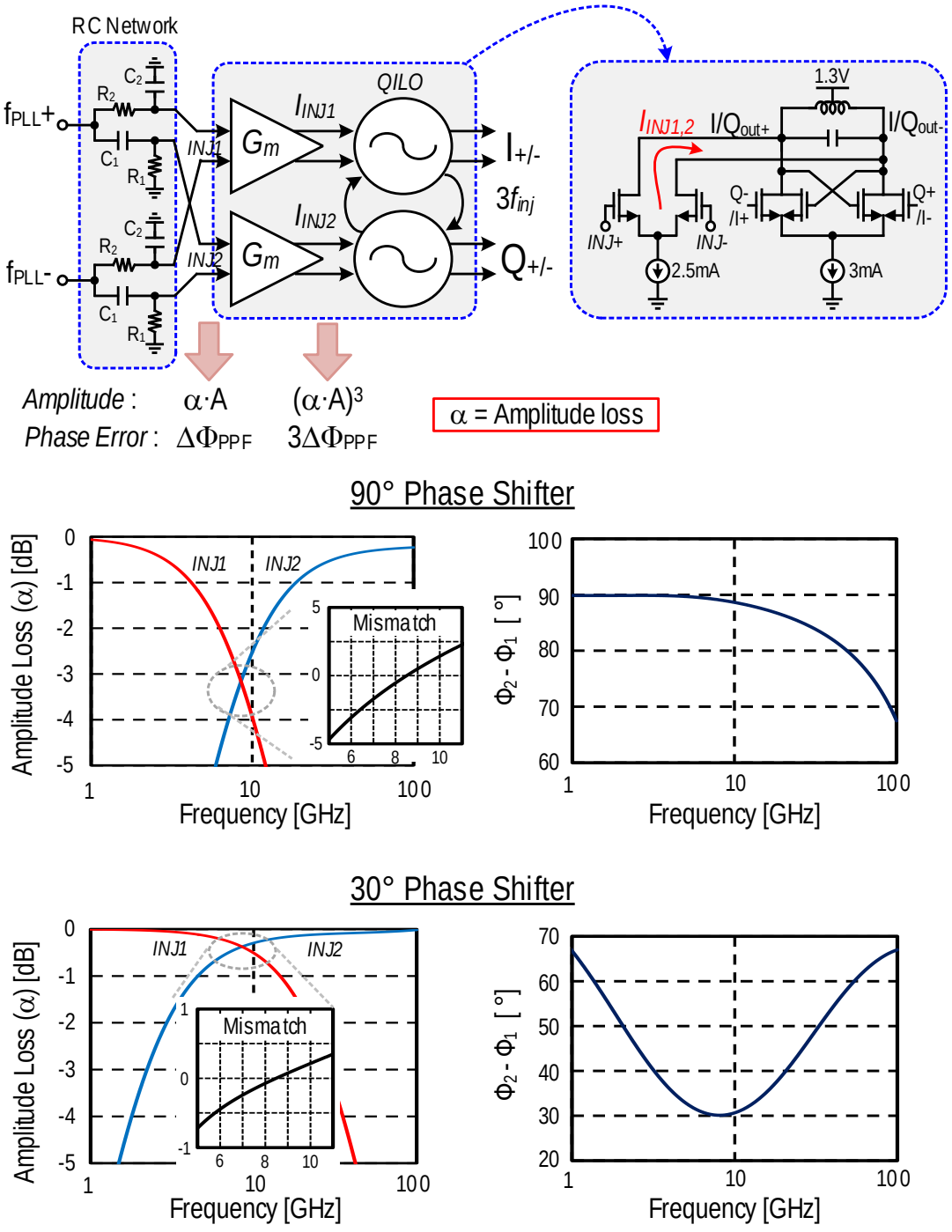



Fig. 5-7. Simulation results of QILOs using 30°- and 90°-phase shifters.

of the harmonic order, resulting in a quadrature phase difference at 24 GHz. Fig. 5-6(b)

compares the injection locking range between the proposed 30° and conventional 90° phase-shift [5-4] RC-CR networks. The excess phase delay by the 90° phasing circuit is 270° at 24 GHz, which narrows the locking range compared to the case with the minimum phase delay; i.e., the locking range of 30°-phase shifter is x1.5 to x2.5 wider than that of the 90°-phase shifter depending on the injection amplitude as shown in Fig. 5-6(b).

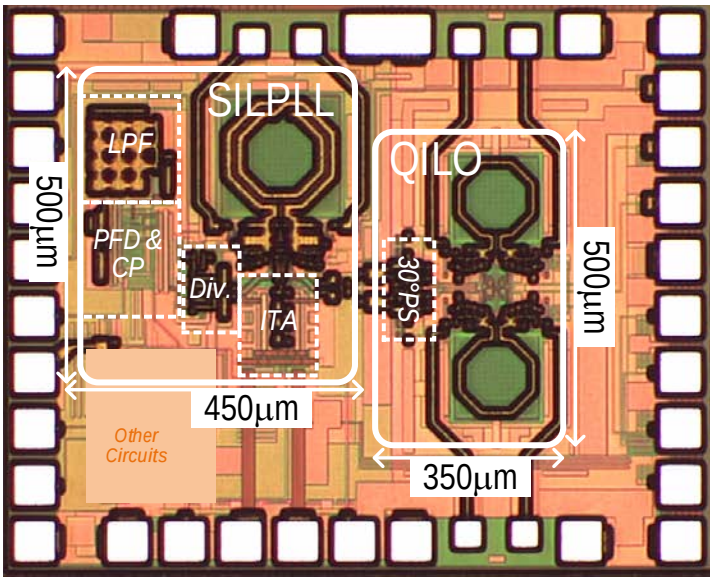



Fig. 5-8. Chip photograph of the SILPLL and QILO (chip size: 1x1.2 $mm^2$ including pads).

## 5.3 Measurement Result

The chip photograph of the proposed SILPLL with QILO fabricated in 130 nm CMOS process is shown in Fig. 5-8. The core chip sizes of the SILPLL and QILO are 0.5 x 0.45 $mm^2$ and 0.5 x 0.35 $mm^2$, respectively. The SILPLL is locked to 8.06 GHz with 300 kHz PLL BW using a 100.75 MHz reference clock, with phase noise contributions shown in Fig. 5-9. The measured phase noise of the reference clock is -160 dBc/Hz at 1 MHz offset. Once the reference clock is injected into the VCO, the measured phase noise of the SILPLL is -114 dBc/Hz at 1 MHz offset and its RMS jitter integrated from 1 kHz to 100 MHz is 124 fs.

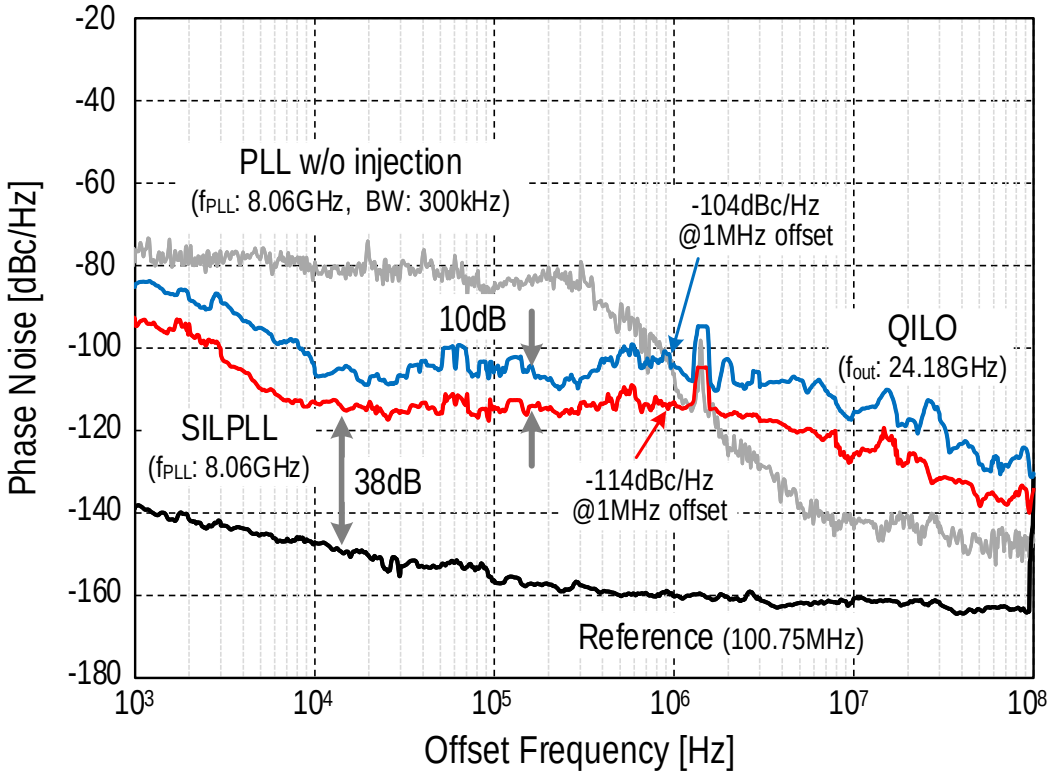



Fig. 5-9. Measured phase noise spectrum at fPLL= 8.06 GHz and fout= 24.18 GHz (fref= 100.75 MHz).

It is observed that the phase noise degradation around ~10's kHz offset is 38 dB from the reference clock's phase noise level, consistent with the phase noise scaling by the frequency division factor. The phase noise at the output of QILO increases by ~10 dB, resulting in -104 dBc/Hz at 24.18 GHz with 1 MHz offset, as shown in Fig. 5-9. The measured RMS jitter at the QILO output is 130 fs with 1 kHz-to-100 MHz phase noise integration interval. The measured reference spur magnitude when the LCVCO output is 8.06 GHz is -49.3 dBc as shown in Fig. 5-10. For a fixed switched-C in the VCO, the PLL lock-in range is limited to 120 MHz because of $K_{VCO} \approx 120$ MHz/V and 1-V headroom at the loop filter output. Therefore, the SILPLL's phase noise remains around -115±1 dBc/Hz from 8 GHz to 8.12 GHz at 1 MHz offset, as shown in Fig. 11. The SILPLL VCO holds a locked state due to the injected reference pulse in the vicinity of the lock-in range, and then gradually loses lock as the output frequency deviates further, increasing the phase noise. The effective locking range

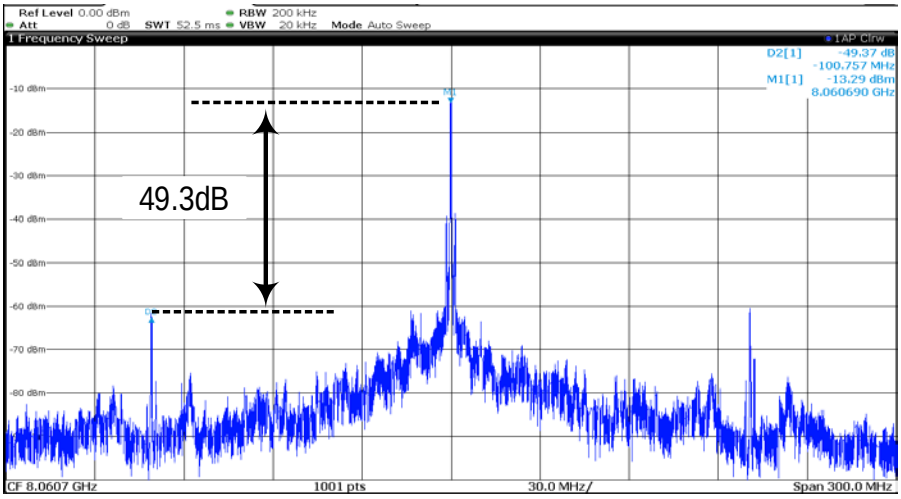



Fig. 5-10. Measured reference spur of the SILPLL.

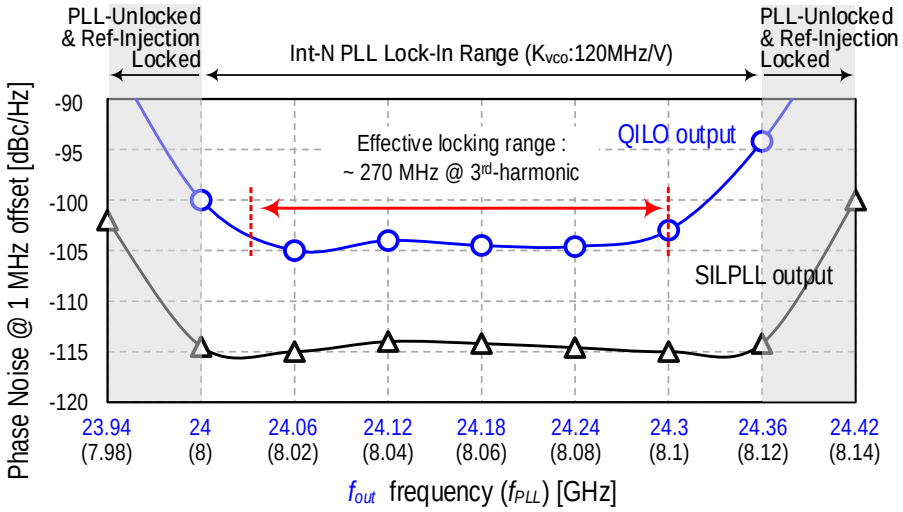



Fig. 5-11. Measured locking range of the QILO.

of the QILO is about 24.03-to-24.3 GHz (270 MHz, QILO free-running $f_{osc}$: 24.18 GHz) defined by where phase noise degrades by ~10 dB (Fig. 5-9). The SILPLL and QILO consume 23 mW and 14.3 mW, respectively. Compared with the prior published phase detection techniques in Table 5.1, the envelope-detection based timing calibration can regulate an optimal injection time, as evidenced by the low reference spur, with one of the largest frequency division factors, while achieving one of highest FOMs reported so far.

TABLE 5.1. PERFORMANCE COMPARISON WITH PREVIOUS WORKS

| | | Architecture | Detection Method | Tech (nm) | Freq. (GHz) | Div. Ratio (N) | Power (mW) | Ref. Spur (dBc) | PN @1MHz (dBc/Hz) | RMS Jitter ($\sigma_t$) | Chip Area ($mm^2$) | FOM (dB) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| [5-1] | | Two SILPLLs | N/A | 90 CMOS | 20 | 20 | 38 | -46 | -113 | 110fs (50k~80MHz) | 0.455 | -243 |
| [5-2] | | ITA | Phase Detection | 180 CMOS | 2.4 | 16 | 12.6 | -39 | -129 | 145fs (1k~40MHz) | 0.64 | -246 |
| [5-5] | | External ITA | Phase Detection | 130 CMOS | 3.2 | 64 | 28.6 | -63.9 | -127 | 130fs (0.1k~40MHz) | 0.4 | -243 |
| [5-6] | | ITA | Phase Detection | 55 CMOS | 0.432 | 16 | 6.9 | -70.7 | -123 | 2.4ps (1k~40MHz) | 0.03 | -224 |
| [5-7] | | Divider-less + ITA | Phase Detection | 65 CMOS | 2.4 | 16 | 5.2 | -49 | -126 | 188fs (1k~44MHz) | 0.25 | -247 |
| This Work | w/o QILO | ITA | Envelope Detection | 130 CMOS | 8 | 80 | 23 | -49.3 | -114 | 124fs (1k~100MHz) | 0.225 | -244.5 |
| | w/ QILO | ITA+QILO | Envelope Detection | 130 CMOS | 24 | 240 | 37.3 | - | -104 | 130fs (1k~100MHz) | 0.4 | -242 |

* ITA : injection timing aligner  **FOM = $20\log(\sigma_t/1s) + 10\log(P_{dis}/1mW)$

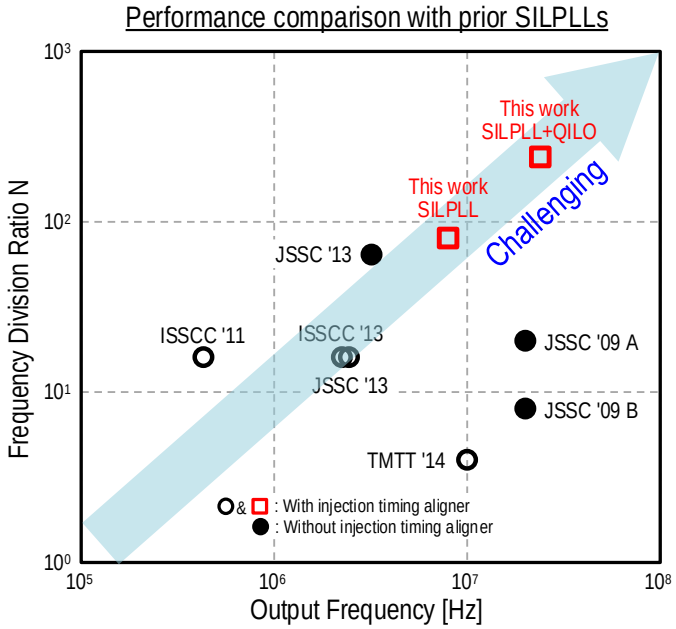



Fig. 5-12. Performance comparison.

## 5.4 Summary

This chapter presents an envelope detection-based reference pulse injection time control circuit for a low VCO phase noise. In the proposed technique, an envelope detector constantly monitors the VCO's output waveform distortion caused by the injection pulse timing mismatch and initiates the injection time calibration loop upon detection of the VCO waveform distortion. Since the control loop seamlessly corrects injection timing until the VCO exhibits a negligible AM distortion, the proposed technique can achieve an optimal injection time regardless of any delays in the digital control circuits.

## 5.5 References


[5-1] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp.1539–1553, May 2009.

[5-2] Y.-C. Huang and S.-I. Liu, "A 2.4 GHz sub-harmonically injection-locked PLL with self-calibrated injection timing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp.417–428, Feb. 2013.

[5-3] D. Shin, S. Raman, and K.-J. Koh, "A mixed-mode injection frequency-locked loop for self-calibration of injection locking range and phase noise in 0.13μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig*., pp. 50–51, Feb. 2016.

[5-4] W. Chan and J. Long, "A 56–65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2739–2746, Dec. 2008.

[5-5] B. M. Helal, C. M. Hsu, K. Johnson, and M. H. Perrott, "A low jitter programmable clockmultiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.

[5-6] C.-F. Liang, and K.-J. Hsiao, "An injection-locked ring PLL with self-aligned injection window," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig*., pp. 90–91, Feb. 2011.

[5-7] I-T. Lee et al., "A divider-less sub-harmonically injection-locked PLL with self-adjusted injection timing," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig*., pp. 414–415, Feb. 2013.

# Chapter 6.

# Conclusions and Future Work

## 6.1 Conclusions

In summary, this dissertation presented frequency locking techniques based on envelope detection. Each chapter introduced issues and solutions of several injection locking applications including a frequency multiplier, multiphase generator, and injection-locked PLL within 5-30 GHz frequency range.

In chapter 2, a mixed-mode injection-frequency locked loop (IFLL) was presented for calibrating locking range and phase noise of an injection-locked oscillator (ILO). The IFLL adjusts free-running frequency of ILO to track the injection frequency by processing the AM modulated envelope signal bearing the frequency difference between injection frequency and ILO free-running frequency using digital feedback. This self-calibration technique resulted in a compact, fast-locking and power-efficient IFLL, demonstrated in 130nm CMOS at 26.5-29.7GHz with less than 300ns locking time and 2.4mW power consumption in the calibration circuits.

Chapter 3 presented a quadrature injection-locked tripler using third-harmonic phase shifter. The capacitive-degenerated pair was utilized to implement the third-harmonic phase shifter which generates 90° phase shift at the third-harmonic. This injection technique resulted in maximizing injection locking range compared to prior injection schemes. It demonstrated in 130nm CMOS at 24GHz with 3.3% locking range and 10.4mW power consumption.

Chapter 4 presented an ILCM using envelope-based frequency tracking loop for a low phase noise signal. In the proposed technique, an envelope detector constantly monitors the VCO's output waveform distortion caused by frequency difference between the VCO frequency and reference frequency. Therefore, the proposed techniques can compensate for frequency variation of the VCO due to PVT variations. It was fabricated in a 0.13μm CMOS process. When the reference clock of 51.5 MHz was injected, the measured phase noise of the ILCM was -114 dBc/Hz at 1 MHz offset. The RMS jitter integrated from 1 KHz to 30 MHz was ~201 fs at 5.15 GHz.

In Chapter 5, the proposed frequency multiplier was presented using self-aligned SILPLL and wide locking range QILO. The injection timing aligner was based on envelope detector due to injection spur. Also, the QILO using 30° phase shifters was proposed to generate 24 GHz quadrature signals and achieve a wide locking range and good phase accuracy. It was fabricated in a 0.13μm CMOS process. When the reference clock of 100.75 MHz was injected into the VCO, the measured phase noise of the SILPLL at 8.06 GHz was -114 dBc/Hz at 1 MHz offset, and its rms jitter integrated from 1 kHz to 100 MHz was 124 fs. When the SILPLL output was third-harmonically locked by the QILO, its phase noise

increased by ~10 dB, resulting in -104 dBc/Hz at 1 MHz offset, at 24.18 GHz. The measured RMS jitter of the QILO output was 130fs.

Additionally, in Appendix I, a six-phase VCO was presented as one example of multiphase signal generators based on injection locking. In the six-phase VCO, three VCOs were coupled by an inductive network in their tail nodes to generate six-phase outputs. This network also served as a tail noise filter in each VCO. Therefore, the proposed six-phase VCO could achieve better phase noise performance than typical multiphase topologies. The proposed VCO was implemented in 32nm SOI CMOS process with core area of $0.6x0.5mm^2$. The VCO could be tuned from 29.24GHz to 31.56GHz, a frequency tuning range of 7.6% at 0.6V supply. With the power consumption of 4.56mW, the measured phase noise was -128dBc/Hz at 10 MHz offset when output frequency was 31.43GHz.

## 6.2 Future Work

The development of deep-submicron CMOS technology allows wireline and wireless applications to increase the operating frequency. However, conventional frequency generators may not be suitable for high frequency application. The proposed techniques can become a good alternative to injection-locked frequency generators at millimeter waves with less reference spur and phase noise, and low power consumption.

Another opportunity for future research is to develop the envelope detection technique in order to sense the frequency information for blocker (or interferer) frequency detection. As mentioned in Chapter 2, the envelope wave under injection unlocking has a frequency

which is the difference between the injection frequency and ILO's free-running frequency. Therefore, the proposed technique can be applied to a blocker detector by detecting the envelope frequency.

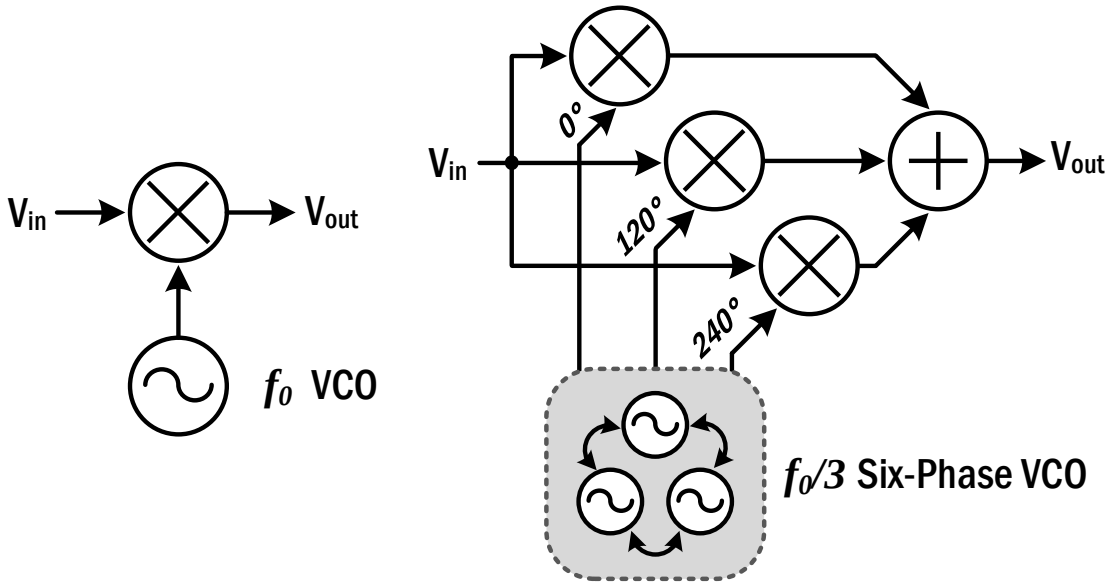
# Appendix.

## A 0.6-V, 30-GHz Six-Phase VCO with Superharmonic Coupling in 32-nm SOI CMOS Technology

### A.1. Introduction

Multi-phasing techniques have been widely used to improve system performance in a variety of applications, such as image-rejection receivers, multi-rate clock-and-data recovery circuits, phased arrays, and more recently N-path filters, to name a few. The phasing techniques are also useful in increasing carrier modulation speed in mixer arrays for millimeter-wave applications [A-1]. Fig. A-1 shows an example of mixer array that utilizes six phase differential signal to reduce a carrier frequency by a factor of three, which is particularly useful for far high end of millimeter-wave band (e.g. > ~100's GHz) where VCOs would exhibit very limited phase noise performance and output power capability because of inadequate active device speed combined with unacceptable level of device noise.

There are several ways to generate multiphase signals: frequency dividers [A-2], polyphase filters [A-3] and multiphase ring oscillators [A-4]. The frequency divider for multiphase signals has an advantage of simple design but suffers from frequency limitation not suitable for millimeter-wave systems. The polyphase filters are susceptible to phase inaccuracy due to device mismatches and process variations. Also, the multiphase ring type




(a) (b)

Fig. A-1. (a) Fundamental mixer with $f_0$ single VCO and (b) time-interleaved mixer array with $f_0/3$ six-phase VCOs [A-1].

oscillators have a phase noise penalty caused by signal coupling active devices that take extra DC power as well. In order to minimize the phase noise penalty with no extra power dissipation, a superharmonic coupling is adopted in this paper to create required phase shift for multiphase generation [A-5]. The proposed technique is basically pure passive and non-contact inductive 2nd-harmonic coupling technique, free from the noise penalty in the cascaded signal coupling to generate six-phase outputs. The coupled inductors at a 2nd harmonic frequency can be integrated compactly at millimeter-wave.

## A.2. Six-Phase VCO with Superharmonic Coupling

### A.2.1. Proposed Architecture

Fig. A-2 shows the schematic of the proposed six-phase VCO which uses a superharmonic coupling to generate six phases. The circuit consists of three separate VCOs and individual VCO's tail node ($V_{T1}$, $V_{T2}$, and $V_{T3}$) is dual-coupled with other VCOs through

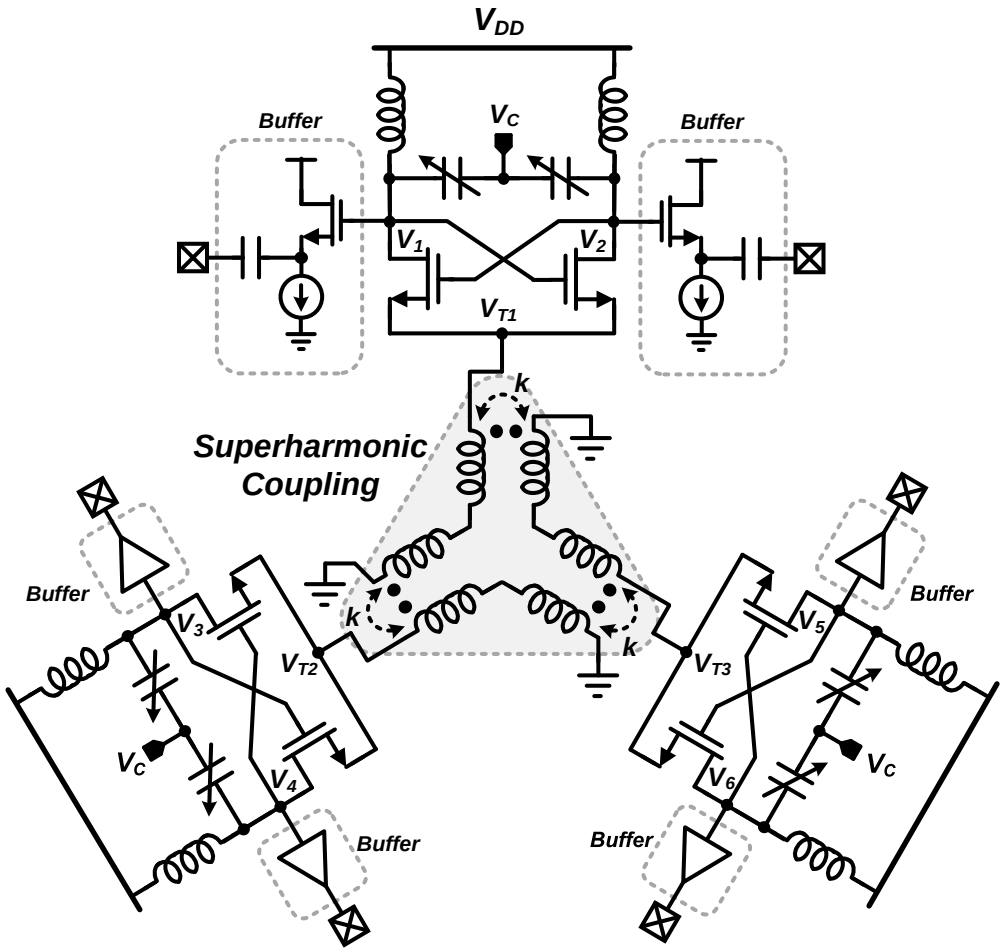



Fig. A-2. Proposed six-phase VCO with super-harmonic coupling.

a 2nd-harmonic coupling network. The coupling network is basically cascaded ring of three identical transformers which forces the three VCOs to be coupled tightly with an equal mutual coupling factor (k=0.8). DC and even harmonic currents of VCO will flow the VCO tail and dominant harmonic current will be the 2nd harmonic of the oscillation frequency ($\omega_0$). Because of the closed-loop ring structure, the phases of coupled signal will be equally distributed in the 2π phase space, resulting in 120 degree of relative phase difference among the 2nd harmonic voltages at individual VCO's tail node. This generates *equi-spaced* six differential phases at the VCOs outputs. The coupling network is designed to resonate parasitic capacitance at $2\omega_0$, forming a second harmonic resonant coupling. This will maximize the 2nd harmonic impedance at the tail node, improving the *$2\omega_0$-noise* filtering and

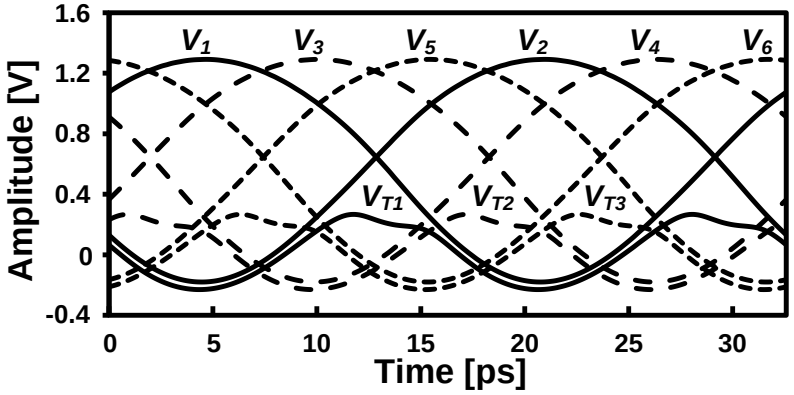
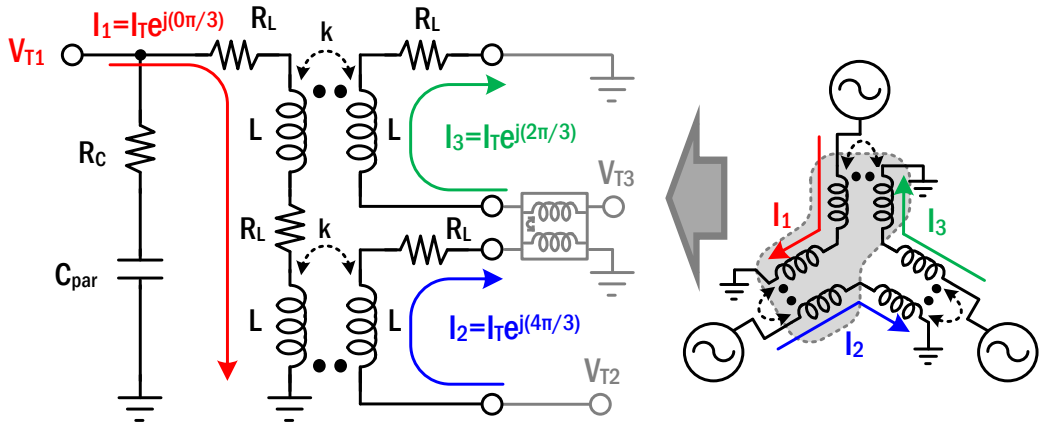



Fig. A-3. Simulated waveforms of the output voltages and the tail voltages at 0.6V supply voltage.

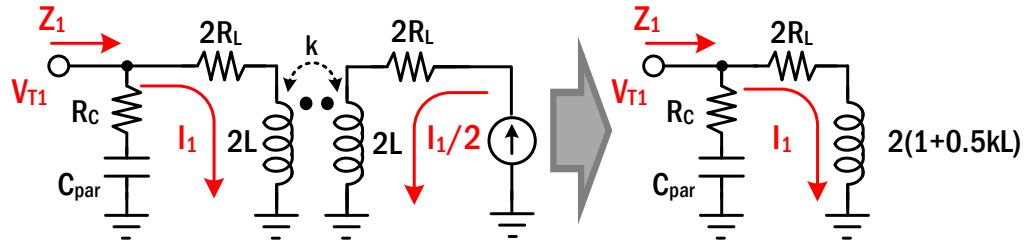
thereby achieving better phase noise performance. The high impedance at $2\omega_0$ also prevents the transistors in triode region from loading the resonator at large VCO output swing, preserving the LC tank quality factor over the entire VCO period. Fig. A-3 shows the simulated waveforms of six-phase output voltages ($V_1$~$V_6$) and three tail voltages ($V_{T1}$, $V_{T2}$, and $V_{T3}$). The tail voltages align well with the minima of each differential VCO outputs, telling that the second harmonic impedance at the tail node is optimally maximized. The simulated phase noise at 31 GHz is -109 dBc/Hz @1-MHz offset, which is about 5 dB improvement compared with the case without the second harmonic tail resonance in simulation.

## A.2.2. Analysis of Superharmonic Coupling Network

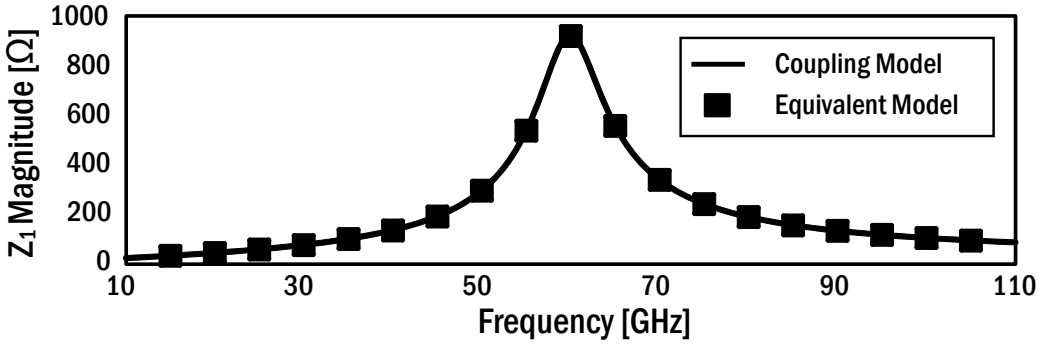
Fig. A.I-4 shows the general model of the coupling network from one VCO. Let us assume $I_1=I_T e^{j(0\pi/3)}$, $I_2=I_T e^{j(2\pi/3)}$ and $I_3=I_T e^{j(4\pi/3)}$ as the tail currents of the coupled VCOs and all coupled inductors have the same inductance, $L$, and coupling coefficient, $k$. A complete coupling model in the VCO is shown in Fig. A-4(a) where $C_{par}$ series with $R_C$ represents a parasitic capacitance with a finite Q at each tail node. Since the tail node in first VCO is coupled with two coils that are excited by $I_2$ and $I_3$, respectively, the tail voltage, $V_{T1}$, can be expressed as




(a)




(b)




(c)

Fig. A-4. Analysis of coupling network: (a) coupling model from first VCO, (b) its equivalent circuit, and (c) simulated results when $L$=107 pH, $C_{par}$=23.5 fF, $R_L$=6 Ω, $R_C$=2 Ω, and $k$=0.8.

$$V_{T1} = 2R_L I_1 + j\omega 2LI_1 - j\omega MI_2 - j\omega MI_3$$
$$= 2R_L I_1 + j\omega 2L(I_1 + k\frac{I_1}{2}) \quad \text{(A-1)}$$

where M=k·L and RL represents parasitic series resistance. From (A-1), the coupling network can be simplified to LC tank shown in Fig. A-4(b). Therefore, the resonance frequency of the coupling network can be approximated to

$$\omega_{res} = \frac{1}{\sqrt{2(1+0.5k)LC_{par}}} \quad \text{(A-2)}$$

Consequently, the inductance ($L$) of the coupled coils should be chosen such that the $\omega_{res}$ becomes twice the oscillation frequency of VCOs. Fig. A-4(c) shows simulation results of the tail impedance for two cases, complete coupled model in Fig. A-4(a) and its equivalent model in Fig. A-4(b), when $L$ is set to resonate at 60 GHz. Both are well matched, validating the equivalence of the models.

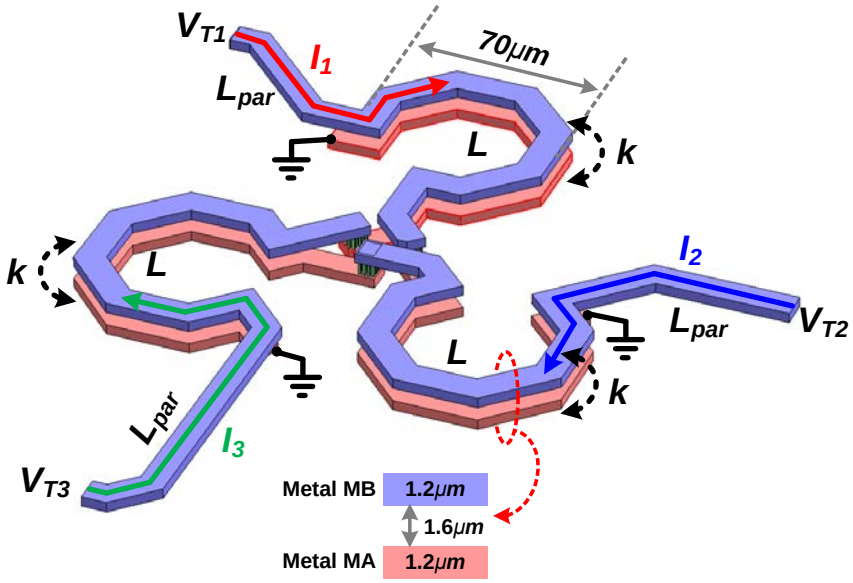
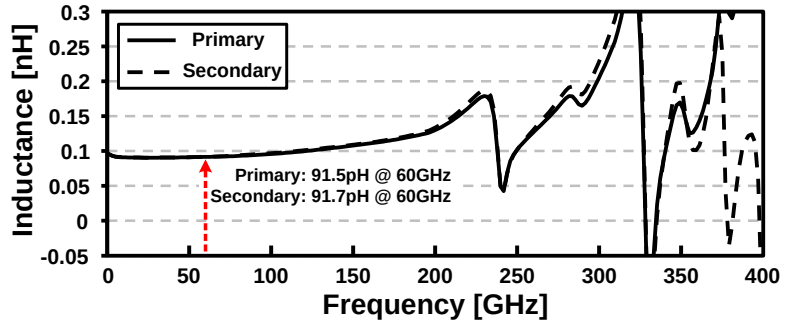


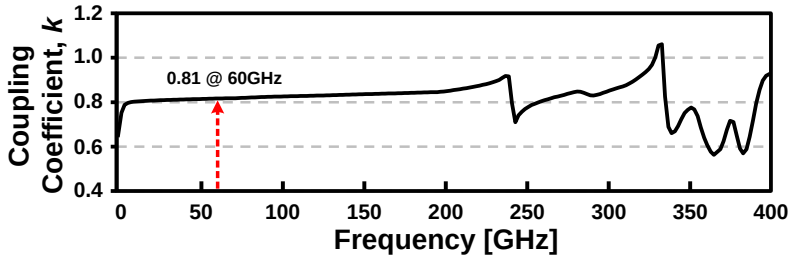

Fig. A-5. 3-D layout view of superharmonic coupling network.

## A.2.3. Implementation of Superharmonic Coupling Network

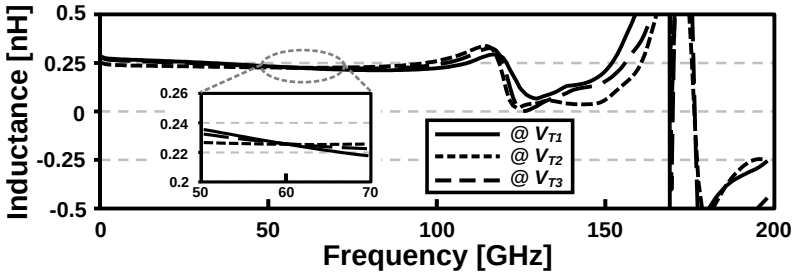
Fig. A-5 presents the layout of the superharmonic coupling network implemented in the 32SOI back-end. In order to maintain symmetry amongst the tail current paths, three identical inductors are used in the coupling network and they are cross-coupled with each other. Each stacked coupled inductors is implemented by using top two copper layers (MB and MA, thickness=1.2 μm). The outer diameter of the coupled coil is 70 μm with a line




(a)




(b)




(c)

Fig. A-6. Simulated coupling network: (a) self-inductance of each inductor, (b) coupling coefficient, *k*, of coupled inductor, and (c) equivalent self-inductance of cascade of two coupled-inductors at each tail branch, not including mutual inductance.

width of 6 μm. The self-inductance and coupling coefficient of the inductors are characterized with EM simulation including layout parasitics (Sonnet Software). The primary and secondary inductances of the transformer are about 91 pH with the self-resonant frequencies over 300 GHz (Fig. A-6(a)), and coupling coefficient, *k*, is 0.81 at 60 GHz (Fig. A-6(b)). When including layout routing inductance (~44 pH), equivalent net self-inductance in each tail branch becomes ~0.23 nH (Fig. A-6(c)). However, when taking mutual inductance by the coupling factor into account, the total inductance becomes ~0.3 nH that resonates ~23.5 fF of parasitic capacitance at 60 GHz ($2\omega_0$).

## A.3. Measurement Results

The proposed six-phase VCO was fabricated in IBM 32 nm SOI CMOS technology. The die photograph is shown in Fig. A-7. The VCO core area is about 0.6×0.5 mm2. Fig. A-8 shows the measured frequency tuning range versus varactor control voltage. The six-phase VCO can be tuned from 29.24 GHz to 31.56 GHz (frequency tuning range: 7.6%). The phase noise and the output spectrum were measured by using R&S FSU67 spectrum analyzer. Fig. A-9 shows that the measured phase noise is -107.55 dBc/Hz and -128 dBc/Hz at 1 MHz and

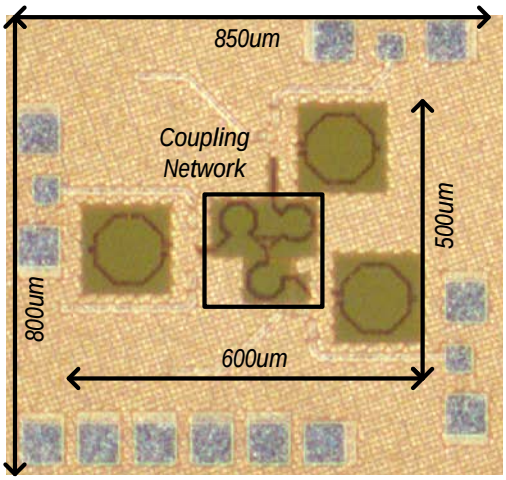



Fig. A-7. Chip photograph.

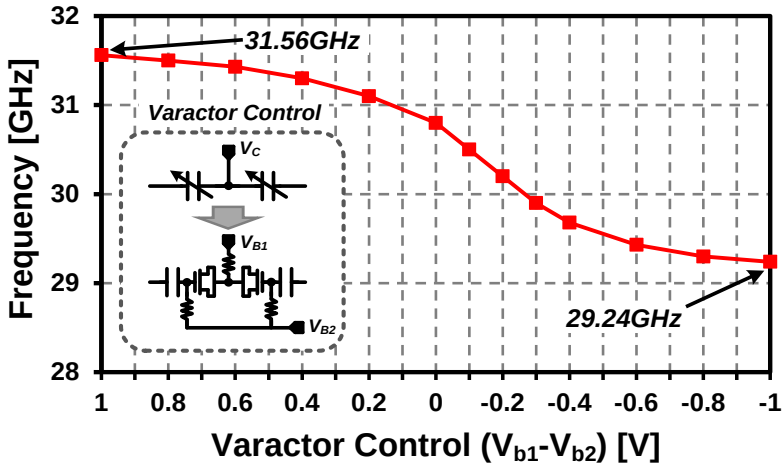



Fig. A-8. Measured frequency tuning range ($V_{DD}$=0.6V).

10MHz offset, respectively, when VCO output frequency is 31.43 GHz. The phase noise measurement is close to simulation result. With the power consumption of 4.56 mW from 0.6 V supply voltage, the figure-of-merit (FOM) and FOMT (FOM including tuning range) are -190.9 dBc/Hz and -188.5 dBc/Hz, respectively.

Table A.1 provides measured performance summary of the proposed six-phase VCO and comparison with recent state-of-the-art differential and quadrature VCOs in CMOS technology. In the proposed VCO, the required phase shifting to generate multiphase outputs can be obtained through a cascade of coupled inductors, a pure passive and non-contact approach that does not degrade phase noise performance with no extra power dissipation, compared with other ring type cascade structure using active transistors. This results in an exceptional low power dissipation of 1.52 mW/VCO with a good phase noise performance, achieving one of best FOMs. The size of the harmonic coupled inductors will be compact at millimeter-wave.

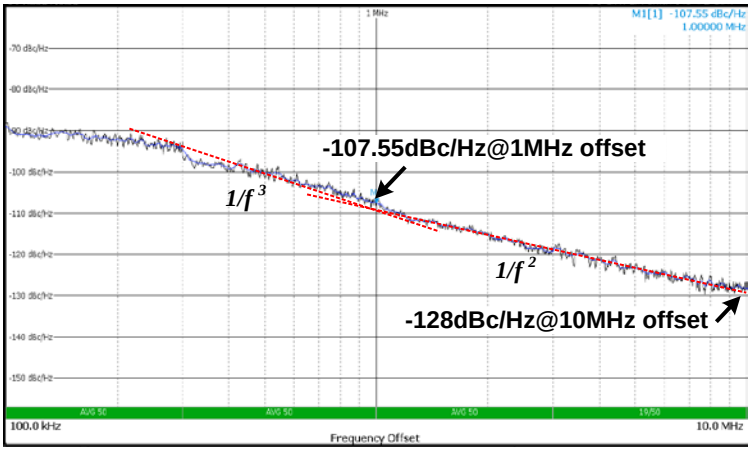



Fig. A-9. Measured phase noise at 31.43GHz oscillation frequency.

TABLE A.1. PERFORMANCE SUMMARY AND COMPARISON

| | JSSC 2013 | ESSCIRC 2012 | RFIC 2014 | CICC 2012 | **This Work** |
|---|---|---|---|---|---|
| Tech | 65nm CMOS | 65nm CMOS | 65nm CMOS | 32nm SOI | 32nm SOI |
| Phase | Diff. | Quad. | Diff. | Diff. | Six-Phase |
| Frequency (GHz) | 57.5<br>-90.1 | 48.8<br>-62.3 | 87.1<br>-91.7 | 20<br>-27 | 29.24<br>-31.56 |
| VDD (V) | 1.2 | 1.2 | 1 | 1.3 | 0.6 |
| Power (mW) | 8.4-10.8 | 15.6-30 | 11 | 24(2) | 4.56 |
| Phase Noise (dBc/Hz) | -105(1)<br>@10MHz | -90/-94<br>@1MHz | -108.3<br>@10MHz | -125.9(3)<br>@10MHz | -128<br>@10MHz |
| Area ($mm^2$) | 0.03 | 0.112 | 0.013 | 0.45(2) | 0.3 |
| FOM (dBc/Hz) | -172 | -173/-176 | -176.9 | N.A. | -190.9 |
| $FOM_T$ (dBc/Hz) | -184.2 | -181/-184 | -171.1 | N.A. | -188.5 |

(1): @ maximum frequency, (2): with PLL, (3): @23.4GHz

$$FOM = PN - 20\log\left(\frac{f_O}{\Delta f}\right) + 10\log\left(\frac{P_{dis}}{1mW}\right) \qquad FOM_T = PN - 20\log\left(\frac{f_O}{\Delta f}\cdot\frac{TR}{10\%}\right) + 10\log\left(\frac{P_{dis}}{1mW}\right)$$

## A.4. Summary

This chapter presented a six-phase VCO. In the proposed multiphase VCO, three individual VCOs are effective cascaded by a coupled inductors network that creates required phase shift of 120 degree amongst the unit VCOs. The chip is implemented in a 32 nm SOI CMOS process. With six-phase outputs, the VCO has 7.6% tuning range from 29.24 GHz to 31.56 GHz. The proposed phase shifting and phase coupling technique is pure passive approach, not incurring any extra power dissipation or phase noise penalty by the phase generation circuits. This results in a very low power dissipation, 1.52 mW per each VCO (4.56 mW total), with -128 dBc/Hz of phase noise at 10MHz offset, leading to one of highest FOMs of ~-191 dBc/Hz.

## A.5. References


[4-1] K.-J. Koh, et al., “Time Interleaved RF Carrier Modulations and Demodulations,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 573-586, Feb 2014.

[4-2] C.-H. Park, et al., "A 1.8-GHz Self-Calibrated Phase-Locked Loop with Precise I/Q Matching," *IEEE J. of Solid-State Circuits.*, vol.36, no.5, pp.777-783, May 2001.

[4-3] H.-S. Chen, and L.-H. Lu, "An Open-Loop Half-Quadrature Hybrid for Multiphase Signals Generation," *IEEE Trans. Microwave Theory and Techniques*, vol.60, no.1, pp.131-138, Jan. 2012.

[4-4] L. Romano, et al., "Multiphase LC oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.53, no.7, pp.1579-1588, July 2006.

[4-5] S. L. J. Gierkink, et al., “A Low-Phase-Noise 5-GHz CMOS Quadrature VCO Using Superharmonic Coupling,” *IEEE J. of Solid-State Circuits*, vol. 38, no. 7, pp. 1148-1154, July 2003.

[4-6] E. Hegazi et al., “A Filtering Technique to Lower LC Oscillator Phase Noise,” *IEEE J. of Solid-State Circuits*, vol. 36, no. 12, Dec. 2001.

[4-7] J. Yin, and H. C. Luong, “A 57.5–90.1-GHz Magnetically Tuned Multimode CMOS VCO,” *IEEE J. of Solid-State Circuits*, vol. 48, no. 8, pp. 1851-1861, Aug 2013.

[4-8] L. Wu, and H. C. Luong, “A 49-to-62GHz CMOS Quadrature VCO with Bimodal Enhanced Magnetic Tuning,” *IEEE ESSCIRC*, pp. 297-300, Sept 2012.

[4-9] T. Xi, et al., “Low-Phase-Noise 54GHz Quadrature VCO and 76GHz/90GHz VCOs in 65nm CMOS Process,” *IEEE RFIC*, pp. 257-260, June 2014.

[4-10] J. Plouchart, et al., “A 23.5GHz PLL with an adaptively biased VCO in 32nm SOI-CMOS,” *IEEE CICC*, pp. 1-4, Sept 2012.