Chapter 1. Introduction

Power electronics devices and modules are the key components in power systems for maneuvering the storage, conversion, and conditioning of massive electromagnetic energy. Marketing demands on manufacturing cost savings, functional integration and reliability are major driving forces on pushing packaging technologies to a higher level. Board-mounted discrete power packages are quickly marching toward a high silicon-to-footprint ratio and low die-free on-resistance. Figure 1.1 shows the package development roadmap from International Rectifier [1], one of the major power management product suppliers. From a mere 10% silicon-to-footprint ratio of the SOT-89 in 1985, this number has reached to 100% in today's chip-scale package, thanks to flip chip solder bumping technology.

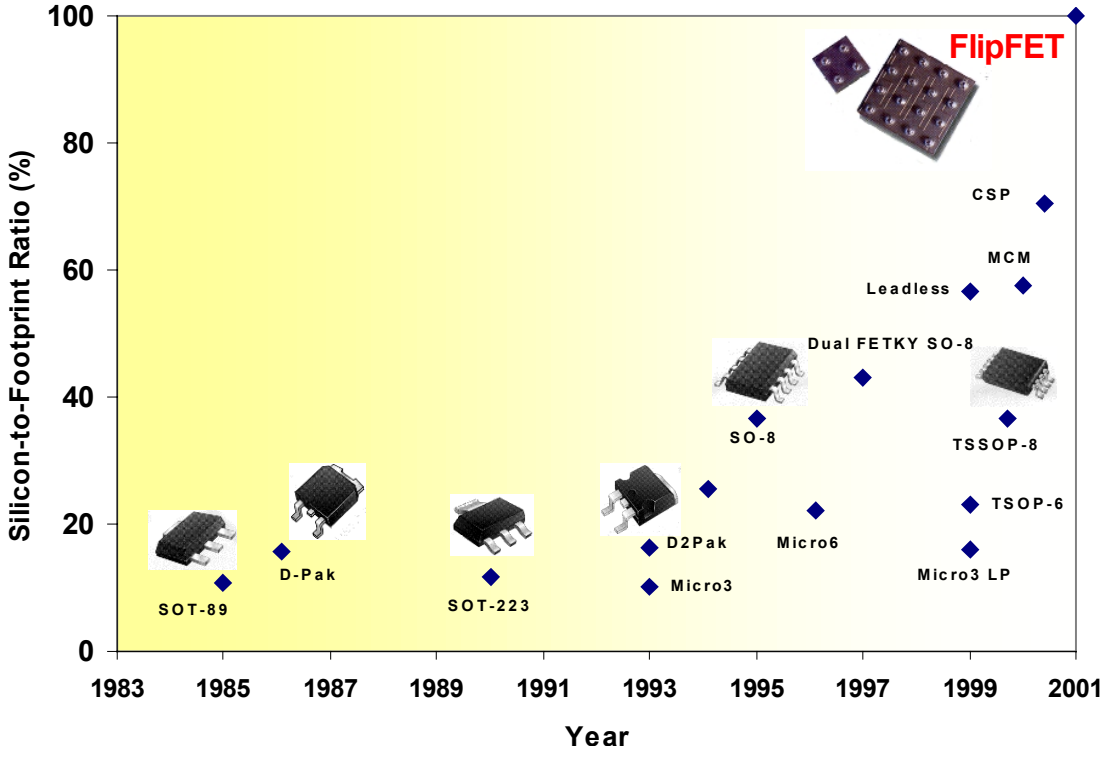


Figure 1.1 Technology roadmap of IR's board-level discrete power packages (courtesy of International Rectifier).

On the high-power single switch or multichip module end, progress is being made in materials and the bonding process for general reliability improvement [2]. For example,

a thin molybdenum plate is soldered on top of silicon as a strain-buffer layer. Aluminum wires are then bonded to the molybdenum plate, resulting a high lifetime under power cycling [3]. In another approach, polymer coating was used to support the bond foot and to reduce shear strains incurred during thermal cycling. A prolonged wire bond lifetime is observed using this method. Further approaches by ABB semiconductors, such as elimination of wire bonding to cut down stray inductance, elimination of the traditional copper base plate, omitting large area solder interfaces, and integrated temperature sensors for fault detection and lifetime monitoring [4], lead to substantial reliability enhancement.

This research presents the development of the Dimple Array interconnect (DAI) technique, an innovative area array solder interconnect structure for power electronics devices and modules with improved electrical, thermal and reliability performance.

1.1 Significance of first-level interconnections for power semiconductor devices and modules

Electronic packages provide protection (mechanical, chemical and electromagnetic), heat dissipation, and power and signal distribution for electrical components and their interconnections [5]. Hierarchically, the packaging begins at the interface of the semiconductor chip itself, which is considered the first-level packaging, to higher levels of packaging such as board-level and system-level packaging. First-level packaging deals with the attachment of one or more bare chips to a substrate, the interconnection from these chips to package leads and encapsulation. The first-level interconnection plays a vital role because it directly interfaces with the chips that contain millions of transistor circuits, not only electrically, but also thermally and mechanically.

In the specific application of power semiconductor devices and modules, the first-level interconnections must fulfill very different requirements compared to those for microelectronic Integrated Circuit (IC) chips. Performance-wise, first of all, the extent of

current and power handling capability per bond or joint increases by several orders of magnitude. This requires a larger cross-section area for these interconnections. Secondly, since these devices operate at high frequencies, in order to maintain a high level of circuit efficiency, parasitic noises must be reduced. Therefore, the conduction path must be minimized. Furthermore, the increased power density drives the first-level packaging to improve its role in heat dissipation [6]. A thermally superior interconnect design is thus desired because it reduces the temperature excursion and thus the thermal stresses as the chips are handling more power. And lastly, reliability of the first-level interconnections is vital in ensuring that the electronic assemblies have an extended lifetime.

1.2 Current interconnect technologies for packaging of power electronics devices and modules

1.2.1 Wire bonding

The most common chip-level interconnect technology in power electronics today is wire bonding. This is primarily due to the fact that this technology can easily accommodate changes in package design with the minimum modification of facilities and the lowest cost per connection. This flexibility and low cost combined with a continuous effort in process improvement and therefore much improved reliability [2] indicate that wire bonding will continue to be the predominant method for chip-level interconnection [5].

In a power discrete package such as a TO-247 metal oxide semiconductor field effect transistor (MOSFET), power semiconductor devices are solder-attached to a copper heat spreader or substrate, and source and gate terminals are connected from the aluminum chip bonding pad to nickel-plated copper leads. The top of the chip and wire bonds are encapsulated with molding compound for insulation, mechanical support and protection. Figure 1.2 shows a wire bond TO-247 package with the top molding hidden for clarity.

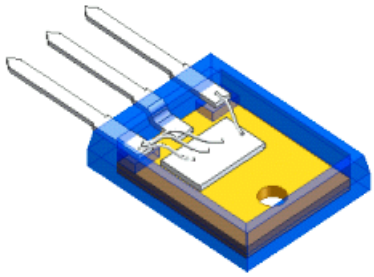
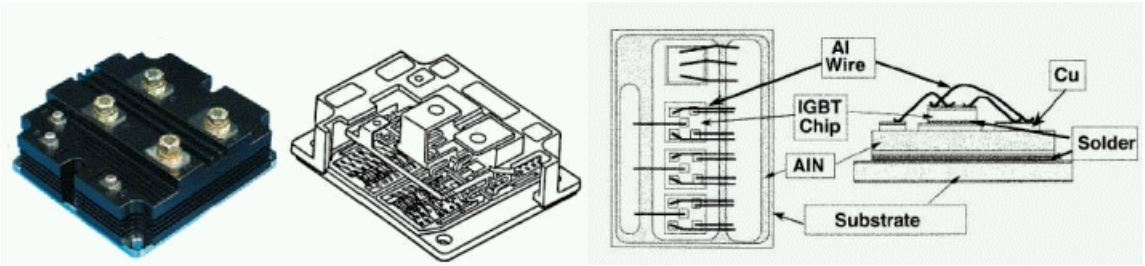


Figure 1.2 Opened-up view of a TO-247 MOSFET package.

In a typical power multichip module (MCM) packaged by wire bonding technology, a direct-bonded copper (DBC) substrate is commonly used as a base for the switching devices and free wheeling diodes. DBC provides excellent electrical insulation as well as good thermal conduction due to the direct bonding of copper on ceramic materials such as alumina and aluminum nitride. Joining materials for device attachment and DBC-to-base plate attachment are usually solder alloys. Aluminum (normally with less than 1 % silicon) wires ranging from 5 to 20 mils in diameter distribute electrical signals and power to the copper leads or traces on the periphery of the chips. Figure 3 (a) shows an EUPEC MCM package (6.5kV IGBT module) [7], Figure 1.3 (b) shows the inside of a power module [8], and Figure 3 (c) shows the schematic of power module components [9].



(a) (b) (c)

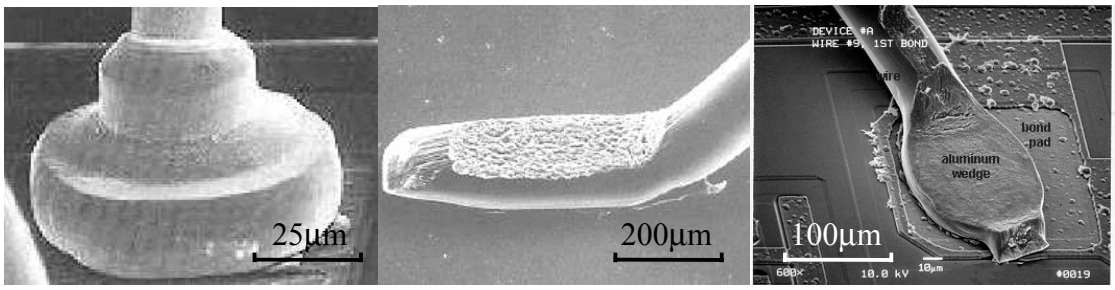
Figure 1.3 Wire bond power modules and schematic of interconnect hierarchy: (a) EUPEC MCM package (courtesy of EUPEC); (b) inside of a power module; and (c) power module components.

In IC industry, there are three major wire bond joining processes, as listed in Table 1.1 [10].

Table 1.1 Wire bonding processes.

Wire bonding	*Pressure*	*Temperature*	*Ultrasonic energy*	*Wire*	*Pad*
Thermocompression	High	300-500^{o}C	No	Au.	Al, Au
Ultrasonic	Low	25^{o}C	Yes	Au, Al	Al, Au
Thermosonic	Low	100-150^{o}C	Yes	Au	Al, Au

Ultrasonic bonding is the most commonly used wire bond joining process in the power semiconductor device application. This method joins aluminum wires to aluminum metallization on chip pads without the use of a heat source. An aluminum wire is first passed through a hole in a capillary. By applying a continuous downward force and ultrasonic horizontal rubbing (60k to 120kHz) of the wire to the bonding surfaces, the wire material plastically deforms and breaks the aluminum oxide layer on the chip to allow for pure aluminum-to-aluminum contact. After the first bond is formed, the bonding machine forms a second bond between the wires and the nickel-plated copper substrate to finish a bond cycle. This process produces wedge-shaped bonds. Figure 1.4 [11] shows SEM photographs of a ball bond (a) and typical ultrasonic wedge bonds (b) and (c). The bonding sequence for the aluminum wedge bond process is shown in Figure 1.5 [12].



(a) (b) (c)

Figure 1.4 Ball bond (a); and wedge bond (b) and (c) (magnifications were estimated).

1.2.2 Pressure pack

One of the bond wire-free technologies is the pressure pack (or press-pack) interconnect that was originally developed by Fuji, Toshiba and ABB [13]. This structure has been applied to high-power devices, such as diodes, thyristors, GTOs, etc., with a proven reliability record for applications that require extended thermal and power cycling

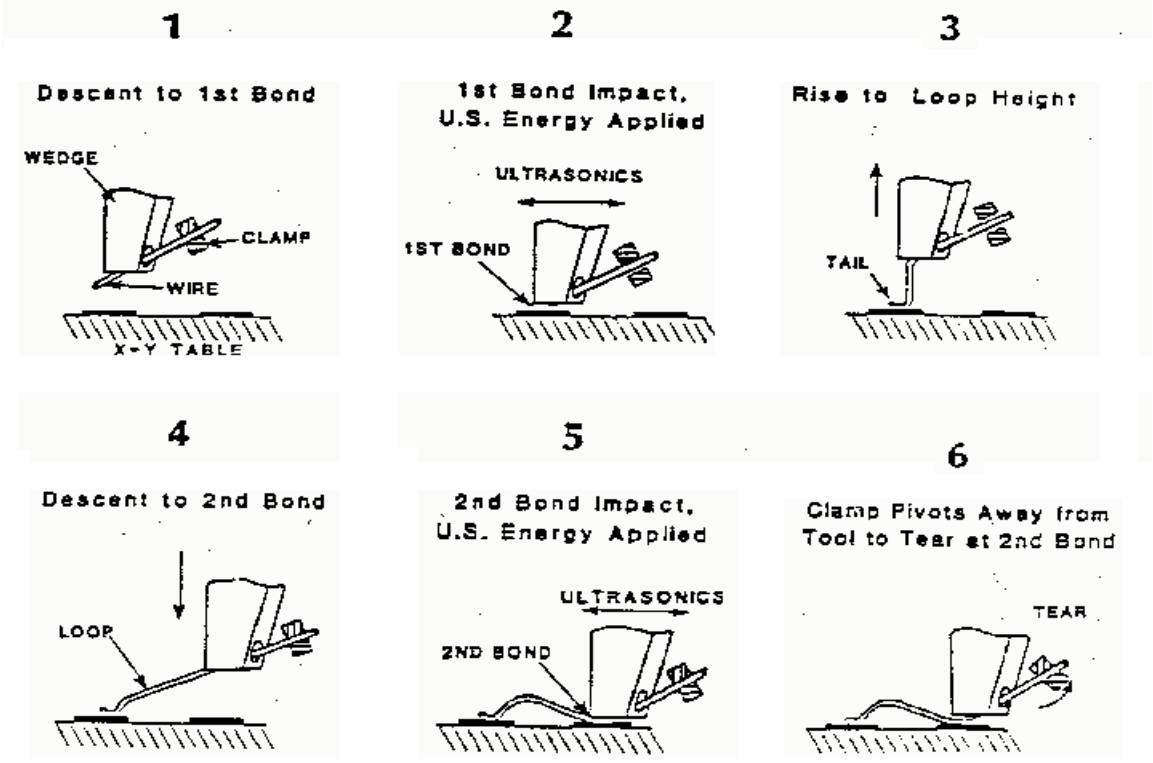


Figure 1.5 Aluminum wedge bonding machine step sequence (1-6) (reprinted with permission of Kluwer Academic Publishers).

reliability, such as transportation systems and motor drives [8]. With the increasing demand on long-term reliability as device area increases, high-power device assembly evolves from solder-attach to solder- or alloy-free [14,15,16,17], finally leading to the shape of today's pressure pack technology. Figure 1.6 shows this progress in high-power semiconductor device assembly [8].

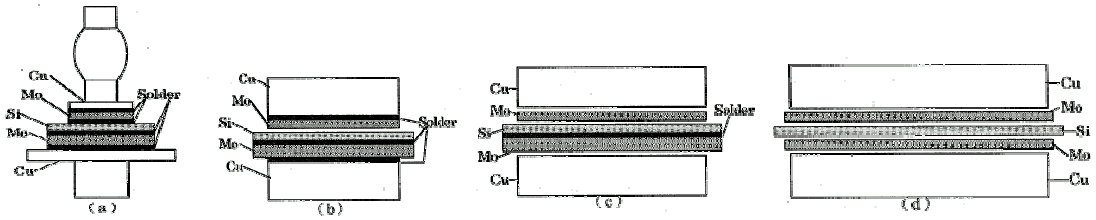
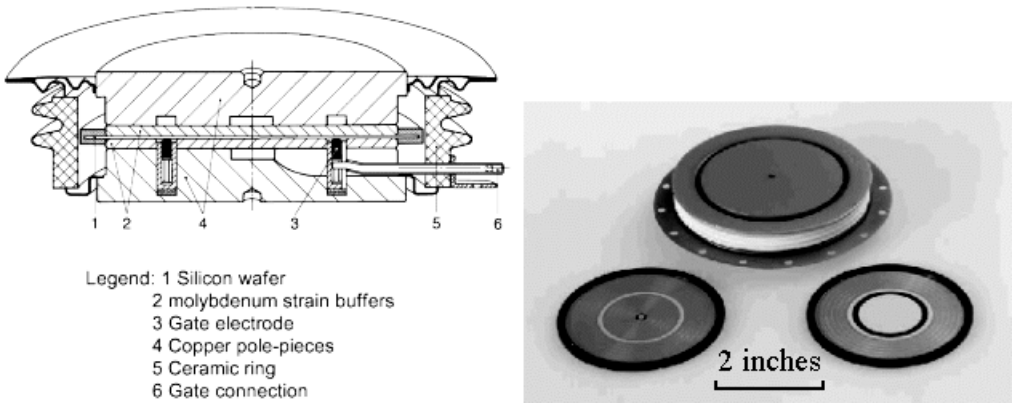


Figure 1.6 Evolution of pressure pack packaging.

The state-of-the-art pressure pack structure is constructed by pressing different device parts together. As shown in Figure 1.6, CTE-compatible (CTE stands for coefficient of thermal expansion) material such as molybdenum is used as the contact metal for the

silicon device. Figure 1.7 (a) is a schematic of the cross-section of a GTO device packaged using press-pack [18]. It is clearly shown that the components for forming a press-pack package include molybdenum strain buffers, gate connection and insulation, copper pole-pieces and a ceramic ring. In most cases the gate electrodes are annular. Figure 1.7 (b) shows a photograph of GTO housing and some wafers.



(a) (b)

Figure 1.7 Construction of a press-pack GTO (courtesy of ABB): (a) cross-section schematic of press-pack GTO; and (b) GTO housing and GTO devices.

A fully press-pack-packaged Integrated Gate-Commutated Thyristor (IGCT) with gate drive and control circuit is shown in Figure 1.8 [18].

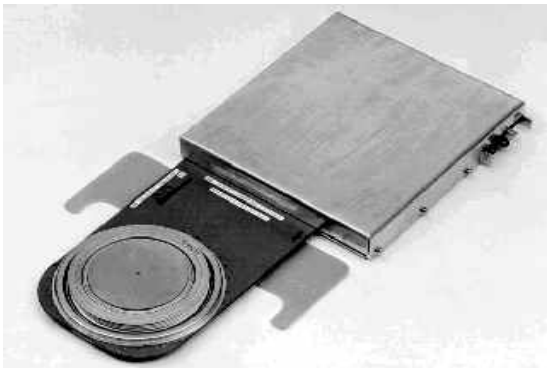


Figure 1.8 ABB IGCT (courtesy of ABB).

1.2.3 Deposited metallization

This is another first-level interconnect approach for packaging semiconductor devices without using bond wires. Device interconnects are constructed with metals (usually copper) and polymer layers that are formed directly on device electrodes. This metal

layer serves as power and signal planes linking power devices to the rest of the circuit, and is formed using chemical or physical deposition. Representative packaging schemes using the deposited metallization technology include General Electric's Power Overlay (POL) technology and the Embedded Power technology.

- GE Power Overlay

The POL technology by GE [19] eliminated wire bonding through the use of metallized Cu vias/polyimide to achieve power and control interconnection. As shown in Figure 1.9. POL takes a multilayer format with power semiconductor devices soldered to a direct-bonded copper (DBC) substrate from the backside, and deposited copper and polyimide dielectric layers on the topside. Differences in device thickness are compensated for by copper/moly shims.

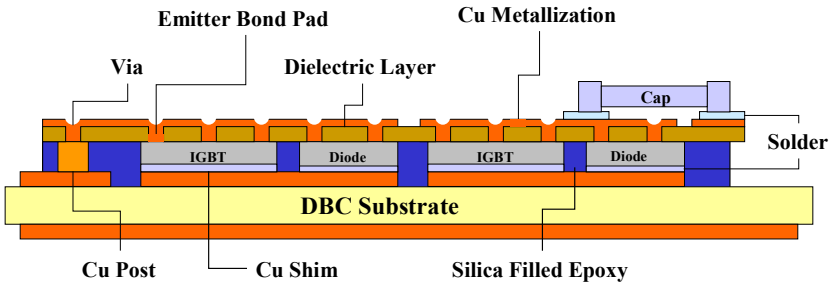


Figure 1.9 Cross-section view of GE POL module structure.

The fabrication process starts with laser-drilling of via holes on the polyimide sheet. Then, devices are attached to the polyimide sheet using special adhesives with device electrodes accurately aligned with via holes. In the next step, assemblies are metallized using sputtering and an electroplating process. Proper circuit patterns are then formed through wet etching in the metal layer. After cleaning, the devices along with the copper/dielectric layers are soldered to the DBC substrate. A final step of silicone gel-filling is needed to protect the devices from moisture. Figure 1.10 is a top view of a POL packaged converter module fabricated at the Center for Power Electronics Systems (CPES) at Virginia Tech. Due to its process compatibility with fine resolution photolithography, POL technology is capable of achieving a high density interconnect with a via diameter down to 0.25mm (10 mil) for power semiconductor devices.

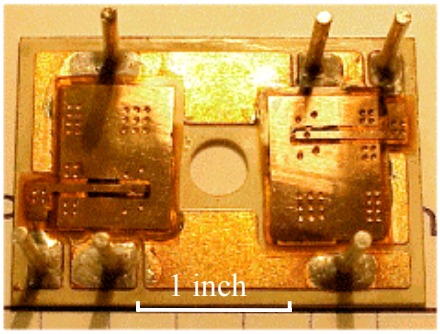


Figure 1.10 Photograph of a POL module fabricated at Virginia Tech.

- Embedded Power

Another deposited metallization interconnect scheme is termed as the Embedded Power [20], a multilayer structure that uses ceramic substrates, screen-printable dielectric materials and solder to enclose power devices. This approach is currently being pursued at CPES. There are three major parts in the structure—the embedded power stage, electronics circuitry and base substrate form a monolithic power module. Figure 1.11 shows a schematic of the cross-section of the Embedded Power module. The electronic components include gate drive, control and protection components. The base substrate provides electrical interconnection and a thermal path for the power chips. The core element in this structure is the embedded power stage that is comprised of the ceramic carrier, power chips (Si in the figure), isolation dielectrics and metallization circuit.

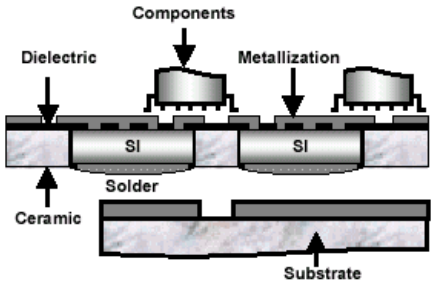


Figure 1.11 Cross-section schematic of the Embedded Power technology.

Figure 1.12 shows the process details of the embedded power stage. To accomplish the metallurgical interconnect, the under bump metallization (UBM) schemes widely used in ICs packaging are employed in this approach. These UBM schemes, such as Ti-Ni-Cu or Cr-Ni-Cu deposited layers, provide low film stress with good adhesive and

electrical/thermal conduction. In order to handle high current, a copper electroplating process is employed to thicken the Cu seed layer.

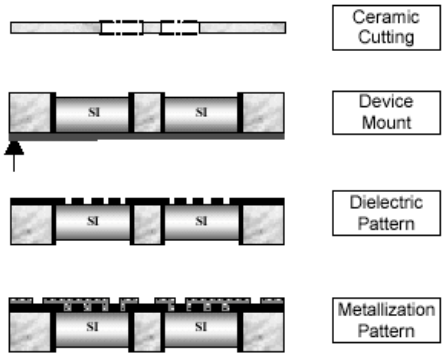


Figure 1.12 Processing flowchart of the embedded power stage.

The main features of the Embedded Power technology are the use of ceramic plate as a chip carrier, in which the power devices are buried and encapsulated with screen-printed dielectrics, and interconnected with deposited metallization to the external circuit. Another important aspect is that this is an all-low temperature (< 250^{o}C) hybrid processing technology. Figure 1.13 shows a finished integrated power electronics modules (IPEM) packaged by the Embedded Power technology.

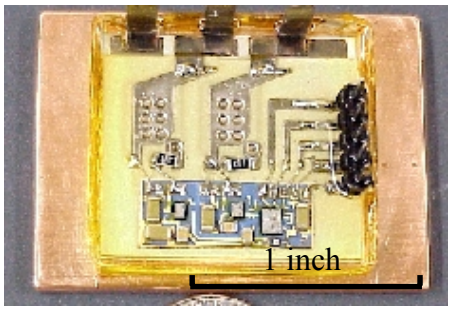


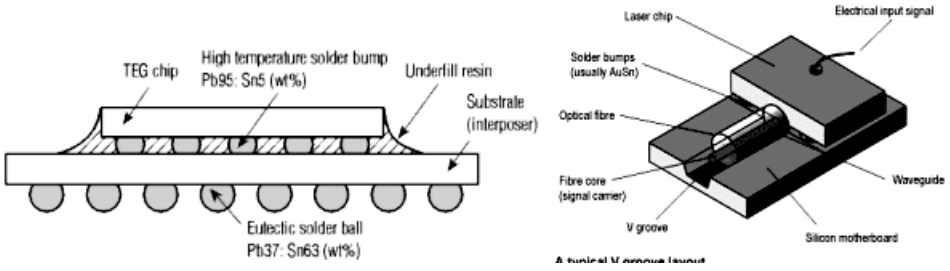
Figure 1.13 Embedded Power IPEM prototype.

1.2.4 Area array interconnect

Solder area array bumping uses area-populated metallurgical bumps or conductive polymer bumps to form permanent connections between device electrodes and the defined substrate metallization. The bumps also provide a heat dissipation path from the chip to the substrate. In addition, the bumps act as a mounting support for the chip as well as a buffer to relieve strain due to the CTE mismatch between chip and substrate.

The origin of area array bumping interconnection dates back to the early 1960s. First used in IBM's solid logic technology (SLT) hybrid modules of the System 360 in 1964, solder bumping technology was invented to replaced the expensive, unreliable manual wire bonding then used in those modules. The solder bumps not only served as electrical connections but also sealed the semiconductor electrodes that were left open by the glass protection coating. IBM's controlled collapse chip connection (C4) [21,22,23,24] developed a few years later used thick-film glass dams to prevent the solder bumps from collapsing, therefore preventing the solder from shorting the unpassivated silicon surfaces. Because the silicon chips are placed facedown when joining them to the alumina substrate, this type of packaging is named "flip chips." The state-of-the-art flip chip technology not only includes solder bumping, but also other metallurgy systems, such as gold or nickel-gold, as well as conductive adhesive bumps, as described later in this section.

Apart from the application of joining the chip to ceramic substrates, C4 technology has been successfully extended to chip carriers' attachment to boards [25] (Figure 1.14 (a)), in which it is called Ball Grid Arrays (BGAs), precision micro-alignment of GaAs waveguide in optoelectronics packaging (Figure 1.14 (b) [26]), and micro-electro-mechanical system (MEMS) devices. Currently, flip chip assembled packages are widely used in automotive electronics, portable communication devices, and high-speed microprocessors.



(a) (b)

Figure 1.14 Applications of flip chips: (a) flip chip BGA structure (courtesy of Oki Electric Industry Co. Ltd); and (b) V-groove fiber alignment using reflowed Au-Sn solder bumps (courtesy of Karl Suss).

The device package-level processing of area array bumping has two stages: the UBM deposition and the flip chip bumping process.

In order for the solder to join the chip, a metallization layer over the unsolderable aluminum pad of the chip is formed using either thin-film evaporation, sputtering, or an electroplating process. This layer is usually named the under-bump metallurgy (UBM). The UBM consists of several layers of metals that insures the adhesion of the bumps, prevents solder diffusion, and maintains good solderability.

The area array solder bumping process can be categorized into four types according to the way the solder is dispensed to the chip/wafer: screen printing, evaporation, electroless plating and electroplating. The solder bumps are then joined with the chips through solder reflow. Typically, a second reflow is needed for the chip to be mounted on printed circuit board (PCB) or substrates.

1.2.5 Flip chip in power packaging

There has been continuous progress in applying flip chip technologies to power electronics packaging in recent years. Among them are the MOSFET BGA and the Bottomless SO-8 (small-outline) packages from Fairchild Semiconductor [27,28] and FlipFET package from International Rectifier [29]. CPES also developed flip chip packages for power chips [30] used in the IPEMs. These area array packages are summarized in Table 1.2.

Common characteristics of these flip chip packages are:

- High packaging density,
- Better electrical and thermal performances due to a much shorter interconnect length, and
- Reduced package footprint and profile.

Table 1.2 Flip chip packaging in power electronics applications.

Developer	*Fairchild Semiconductor*	*International Rectifier*	*CPES*
Picture/photo			
Die size (mm x mm)	**5 x 5.5**	**1.5 x 1.5**	**7.2 x 9**
Bump height x pitch (mm x mm)	**0.30 x 0.75 (0.5mm ball diameter)**	**0.25 x 0.8**	**1 x 1.75**
Profile (mm)	**0.8**	**0.8**	**1.25**
$R_{DS(on)}$ (mΩ)	**5 @V_G=4.5V**	**42 @V_G=4.5V**	**NA**
Rating	**22A, 30V Power Trench MOSFET**	**20V, p-channel MOSFET**	**1200V 70A, IGBT**
Representative product	**FDZ5047N**	**IRF6100**	**Prototype**

- Fairchild MOSFET BGA

Fairchild Semiconductor [28] has transformed the solder bump technology in the microelectronics industry to power device application (Figure 1.15). Fairchild applied the flip chip process to MOSFET packaging using solder bumps for gate and source attachment. Package resistance and thermal impedance have been reduced and package current handling capability has been doubled.

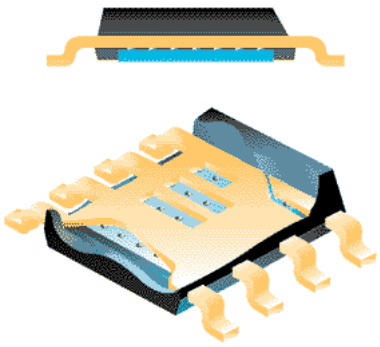


Figure 1.15 Fairchild's bottomless SO-8 package using solder bump technology (reprinted with permission of Power Electronics Technology).

Fairchild Semiconductor International's more aggressive move toward solder flip chip bumping and BGA packaging on power MOSFET and interface/logic applications [31] has led to the industry's first MSOFET BGA package (Figure 1.16), the 30V PowerTrench® MOSFET BGA. With an ultra-low $R_{DS(on)}$ of only 2.5mΩ, this package offers a low-profile of just 0.8mm and a package size of less than $28mm^2$. Using the MOSFET BGA, the efficiency and power density of the DC/DC converters in notebook computers and voltage regulation modules (VRMs) are dramatically improved [32].

Figure 1.16 Fairchild's MOSFET BGA (courtesy of Fairchild Semiconductor).

Advantages of Fairchild BGA packages include area savings on the PCB board and a large ball diameter (0.8mm pitch/0.5mm ball) for easy layout routing. The use of bismaleimide triazine (BT) resin substrate also facilitates package reliability due to a matched CTE.

- IR FlipFET™

FlipFET™ is a new generation of power MOSFET package from International Rectifier. FlipFET™ "combines the latest die design and wafer level packaging technology to give the smallest package footprint possible." [33] Since traditional power MOSFETs are vertical devices, in order to facilitate the standard flip chip bonding process, the gate, source and drain connections are all rearranged to be on the front face. Figure 1.17 shows an SEM photo of FlipFET™ device [33].

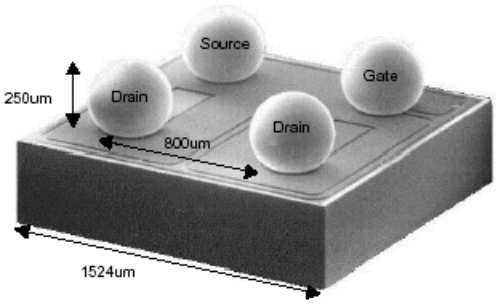
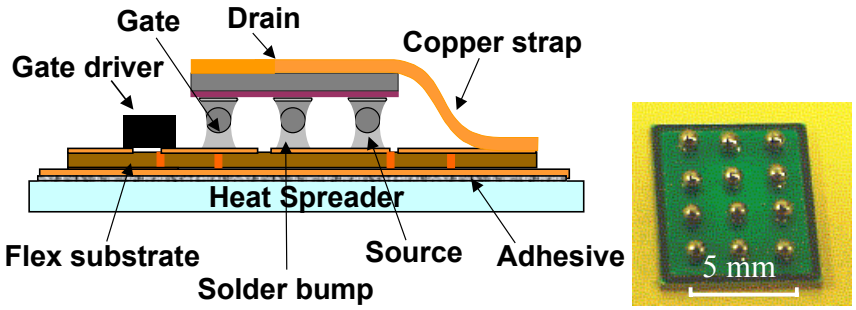


Figure 1.17 An SEM image of IR's FlipFET (courtesy of IR).

- CPES D²BGA [30]

Researchers at CPES developed a chip-scale power packaging structure called the Die-dimensional Ball Grid Array (D^2BGA). Figure 1.18 shows a schematic of this structure. Improvements in current handling capability, electrical characteristics, and package reliability were reported.



(a) (b)

Figure 1.18 Flip chip power packaging developed at CPES: (a) schematic of D^2BGA; and (b) chip scale power package.

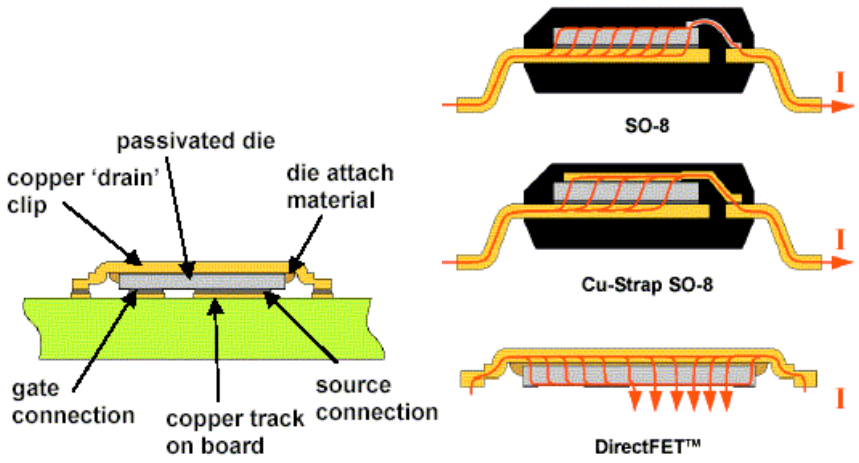
Flip chip area array solder bumping technology was invented to replace the expensive, unreliable manual wire bonding in IBM's solid logic technology (SLT) hybrid modules of the 1960s. Within a few decades, it has been extended to automotive electronics, portable communication devices, and high-speed microprocessors, due to its proven electrical, thermal and reliability performance. It was hoped that many advantages of this interconnect approach would also benefit power electronics. Currently, most commercial power devices packaged by flip chip solder bumping are in the low- and medium-power ranges. Requirements for the adoption of flip chip area array solder bumping into power electronics packaging are:

- New chip interconnect structure must have high current handling capability;
- Must offer better thermal management due to the high power density of the power semiconductor devices and modules;
- Must offer process compatibility;
- Must have good insulation due to high-voltage operation; and
- There must be a good understanding of the reliability of the solder bumping interconnect in the context of power applications.

- Other innovative power packaging approaches

Several other interconnect techniques are proposed. Again, the common characteristics of these techniques is their replacement of wire bonds with other interconnect approaches and the extension of power packaging into three-dimensional interconnect structures.

International Rectifier [34] developed a technique for packaging a low-power MOSFET by replacing wire bonds with a copper strap. Conductive epoxy has been used to attach the copper strap to the power chip pads. International Rectifier recently announced its DirectFET™ technology, as shown in Figure 1.19 [35].



(a) (b)

Figure 1.19 DirectFET™ package (courtesy of IR): (a) cross-section of DirectFET soldered to PCB; and (b) comparison of current conduction paths.

Aiming at reducing footprint size, package-related conduction losses, and making gains in thermal performance, DirectFET™ does not even use array solder bumping. This technology moves one step further from IR's Cu-strap structure to large-area soldering of a copper 'can' directly onto silicon devices. It combines a proprietary passivation system and a surface-mountable ultra-low-profile package with 20 times improvement in junction to PCB thermal resistance compared with wire bond SO-8. Also the improvement of die-free-package-resistance (DFPR) of the DirectFET is 86% over the wire bond SO-8.

The Silicon Power Corporation (SPCO) has developed ThinPak technology [36]. In this technology, a ceramic lid, with holes drilled in it and filled with solder, is attached to the chip by solder reflow (Figure 1.20). Specific routing can be made in the ceramic interposer to connect electrodes on the chip to circuits. This technique was claimed to increase power module yields to nearly 100%. The thin ceramic lid shrinks package volume and thermal resistance. It also serves as the base for integration of other circuit components.

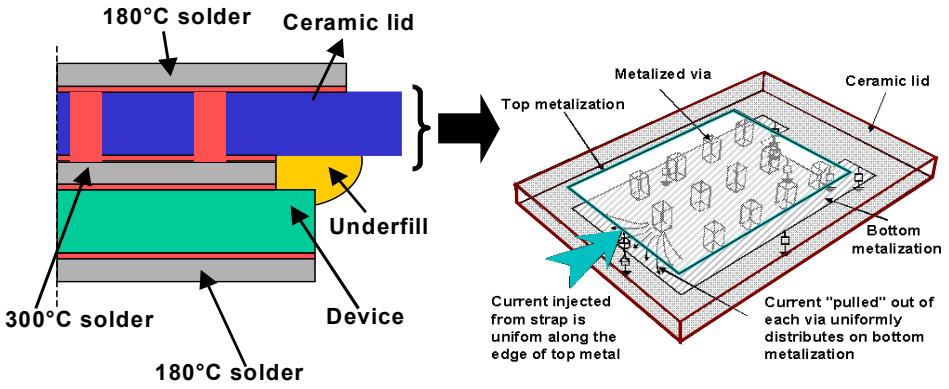


Figure 1.20 Schematics of ThinPak cross-section and three-dimensional view (courtesy of SPCO).

1.2.6 Performance of first-level interconnects

First-level interconnects are vital components that bridge miniaturized semiconductor devices with the system. The applications of these technologies cover a wide range including IC devices, MOSFETs, IGBTs and GTOs. Table 1.3 summarizes the advantages and disadvantages of different interconnect schemes for these systems.

Table 1.3 Pros and cons of various power packaging technologies

Technologies		*Advantages*	*Disadvantages/concerns*
Wire bond (IGBT, MOSFET)		High flexibility to adapt to various devices; No special requirement on wafer processing; Lowest cost per connection; Improved reliability.	Low throughput due to sequential bonding process; Large parasitic noises due to long interconnect path; Poor thermal management; Inapplicable to 3D integration.
Press pack (GTO, IGCT, IGBT)		Best reliability due to fatigue-free structure; Explosion-free; Low thermal impedance, double-sided cooling.	Special cooling scheme; Special insulation approach; Hermetic sealing; High cost packaging.
Deposited metallization (IGBT, MOSFET)	GE POL	Much better electrical performance than wire bond due to short interconnect path; 3D, multilayer integration applicable.	High parasitic capacitance; Lack of stress reliever between silicon and copper interconnect (high demand for structure cohesion); Processing complexity; High cost due to laser drilling, sputtering.
	Embedded Power	Compatible with hybrid thick-film processing; Much better electrical performance than wire bond due to short interconnect path; 3D, multilayer integration applicable.	High parasitic capacitance; Lack of stress reliever between silicon and copper interconnect (high demand for structure cohesion); Processing complexity; High cost due to laser drilling, sputtering.
ThinPak (MCT)		Good heat dissipation due to large-area soldering on both sides and the use of ceramic lid; Much better electrical performance than wire bond due to short interconnect path; 3D, multilayer integration applicable.	Reliability concern for large-area soldering.
Area array solder bumping (IGBT, MOSFET)		High packaging density; Much better electrical performance than wire bond due to short interconnect path; 3D, multilayer integration applicable; Lower cost than deposit metallization; ThinPak, or press pack; Good reliability.	Requires additional wafer processing; High cost for low-volume package; Fatigue of solder alloys.

1.3 Motivation for developing the Dimple Array interconnect

1.3.1 Issues with the wire bond interconnect

Although wire bond technology has been a mature and dominant technology for packaging of power semiconductor devices and modules and has gone through a continuous improvement in all aspects, there are a few bottlenecks preventing this technology from becoming the choice for the next generation integrated power modules and devices. These concerns are:

- Low power density and low silicon-to-footprint ratio result in insufficient use of limited PC board space for discrete power packages.

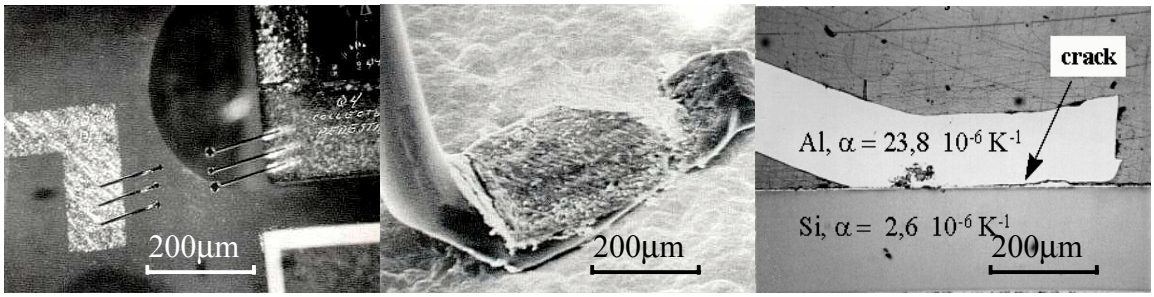
- Mutual coupling effects between adjacent wire bonds can lead to a change in the impedance of different bonding wires. Wires in the edge appear to be of low impedance, thus taking much higher current than those in the middle [37]. Also, the current crowding at each wire-to-chip joint causes hot spots [38]. Electrical overstressing may cause a fusing of wire bonds (Figure 1.21 (a)) due to its limited current handling capability [39]. All these will ultimately contribute to uneven thermal distribution.

- As a planar packaging technique, wire bonding technology interconnects devices using long wires. Parasitic noises related to these long wires and leads result in high switching energy loss and high device turn-off voltage spikes. The latter could cause the shoot-through failures [39].

- The fabrication of wire bond modules involves ultrasonic rubbing of bonding wires to an aluminum metallized silicon chip surface. Over-bonding or under-bonding of wires due to improper bonding parameter settings results in damage to the pad metallization, chip craters and wire bond lifts (Figure 1.21 (b) [39]). Fatigue failure at the heel and toe of the bond (Figure 1.21 (c) [40]) caused by shear forces due to mismatch in coefficients of thermal expansion [41,42] may be accentuated by these defects introduced during the manufacturing process.

- With the ever-increasing power density and heat dissipation, the conventional single-sided cooling scheme soon reaches its limit. Double-sided cooling [19, 35, 43] is becoming the technology trend for high-power integrated modules. It is impossible to attach additional heat sinking components on the top of the devices interconnected by wire bonds.

- Wire bond is simply not adaptable to the imminent 3D, integrated packaging for power devices and systems. The manufacturing of power modules is cost and labor-intensive, and the time-to-market delay for custom circuits is significant [44].



(a) (b) (c)

Figure 1.21 Wire bond failures: (a) photograph shows electrical overstress indicated by fusing of three parallel wirebonds of a power transistor (courtesy of Motorola); (b) wire bond heel crack, overbonded (courtesy of Motorola); and (c) wire bond fatigue crack (magnifications were estimated).

1.3.2 Issues with the conventional controlled collapse flip chip interconnection

The controlled collapse chip connection (C4) developed by IBM has been widely used in computer systems, portable devices, automobiles, and power management products. Excellent performance and reliability have been demonstrated in these packages throughout the past decades. In recent years, there is a growing trend toward using area array flip chip technology to package power semiconductor devices. Improvements in reducing on-resistance, current handling capability and package thermal dissipation are reported [6,27,28,30]. The area array solder bumping technology has become a promising

candidate for high-performance board-mountable discrete devices and shows competitiveness in high-power modules as well [30,45].

However, due to the need for a ball-defining mask on both the device surface and the copper flex substrate, as well as a second reflow of solder bumps, the fabrication process is time-consuming. Furthermore, conventional controlled collapse bonding (CCB) process results in barrel-shaped solder joints, in which highly localized stress/strain concentration is localized at the outer edge of the silicon/solder or substrate/solder interface. In low CTE mismatch applications, such as ceramic BGA or C4 interconnections, the reliability requirement can be fulfilled using underfill support. However, under the circumstance of a large CTE mismatch, such as that between copper and silicon in power modules, the barrel-shaped solder joints are prone to early fatigue crack at the solder/silicon interface. The stress/strain concentration-induced early fatigue failure is a major concern in power/thermal cycling conditions. Figure 1.22 shows the stress/strain concentration at the corner of CCB solder joints [46].

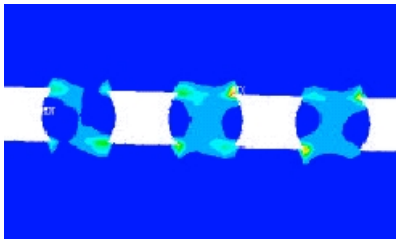
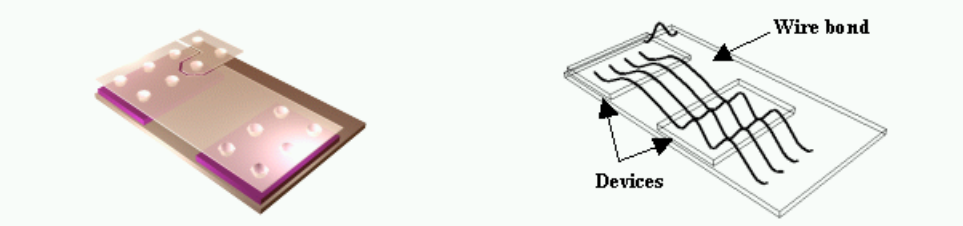


Figure 1.22 Stress/strain concentration at CCB solder joints.

1.3.3 Dimple Array interconnect — an alternative area array solder bumping technology

This research developed an innovative solder bumping interconnect technology that is capable of achieving lower switching loss, higher efficiency and better heat dissipation than the state-of-the-art wire bond technology. This technology is termed the Dimple Array interconnect (DAI) technique. The DAI not only facilitates integration of control components into 3D power electronics modules, but also demonstrates improved thermal and reliability performance over the conventional CCB flip chip power packaging methods.

The DAI technique establishes electrical connections onto power semiconductor devices by solder bumps formed between device electrodes and arrays of dimples pre-formed on a metal sheet. Figure 1.23 shows the schematics of both the DAI and the conventional wire bond interconnections. In the DAI structure, multiple wire bonds are replaced with a single metal sheet that connects to silicon devices through solder joints. Apparently, the DAI decreases the package footprint and offers a low-profile, planar interconnection that is favorable for multilayer integration with other circuit components.



(a) (b)

Figure 1.23 The Dimple Array interconnect (a); and the wire bond interconnections (b).

1.3.4 Advantages of the Dimple Array interconnect technique

First of all, the DAI is an alternative area array solder bumping technique. Therefore, it comes with most of the advantages of area array solder bumping. These advantages are:

- High packaging density, low-profile;
- Much better electrical performance than wire bonding due to short interconnect path;
- Better thermal management than wire bonding;
- 3D, multilayer integration applicability;
- Lower cost than deposit metallization, ThinPak, or press pack; and
- Wafer-level chip scale packaging.

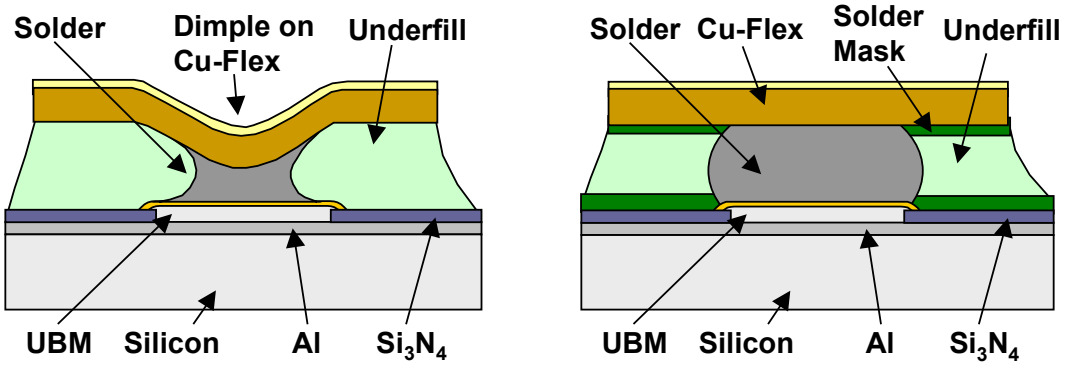
Table 1.4 compares wire bonding and area array flip chip bonding from the standpoint of processing and electrical performance [47,48]. It is clearly shown that the I/O count of the flip chip is substantially higher and the parasitic inductance and capacitance are lower.

Table 1.4 Comparison of wire bonding and flip chip bonding.

	Wire bonding		*Flip chip bonding*	
	Ball	Wedge		
Material	Au	Al	PbSn, AuSn, SnAg	Conductive polymer
Connection method	TS/TC	US	Soldering	Adhesive
Process temperature (°C)	100-150	RT	225-360	150
Typical pad pitch (μm)	150-200	50-200	200-250	100-200
Area ratio to die	1.5	1.5	1	1
Maximum I/O count	300-500	500-700	>1000	>1000
Resistance (mΩ)	122	142	1.2	5-10 (Au)
Lead capacitance (pF)	0.025	0.025	< 0.001	< 0.001
Lead inductance (nH)	2.6	2.6	< 0.2	< 0.1

- Better thermal management

Compared with the CCB, the DAI shows improved thermal management because of its reduced interconnect path. Figure 1.24 (a) shows the schematic of the cross-section of the DAI solder joint, and Figure 1.24 (b) shows a CCB solder joint. For the same land area (or footprint of solder) and the same distance between cu-flex to the chip (standoff height), the DAI package uses less solder mass, and thus has a shorter thermal path than the CCB package.



(a) (b)

Figure 1.24 Structures of (a) the Dimple Array interconnect; and (b) the controlled collapse bonding.

- Better reliability

The DAI structure has an hourglass shape similar to that of some specially processed flip chip interconnect. Satoh, et al. [49] has studied the effects of the shape of 95Pb/5Sn flip chip bumps on their fatigue mechanisms. It was concluded that the hourglass-shaped solder joint has a smaller maximum effective strain range than that of the barrel-shaped solder joints, and therefore has a longer thermal fatigue life. The DAI uses a dimpled solder-wettable metal sheet to form a solder fillet between the dimple and the chip. Improved reliability is expected due to the reduced strain/stress concentration.

- Better electrical performance

From an electrical standpoint, the concave dimple structure further reduces the interconnect length as compared to the CCB. This will result in a low parasitic inductance in the structure while maintaining a low parasitic capacitance. In developing technologies, such as the GE POL and Embedded Power, the parasitic capacitance is normally larger than that of the wire bond module due to the decreased distance between parallel conductor planes. High parasitic capacitance between midpoint and the ground could be detrimental. For example, if the module is attached to a heat sink, the high parasitic capacitance is the cause of common mode electromagnetic interference (EMI) [50]. The DAI approach can have a better control over the distance between emitter copper plate and the ground, and thus can minimize the parasitic capacitance as well.

- Simpler fabrication process

The CCB process requires ball-limiting masks (such as solder masks) on both the interconnect side and the device side to confine the liquid solder during reflow (Figure 1.24). The DAI structure eliminates solder collapse issues even without using the ball-limiting mask. This saves two clean-room steps and simplifies the fabrication process. Dimple stamping is the only step added to the original CCB solder bumping; this can be automated in the same way the IC packaging industry makes lead frames.

- Wide applications

Apart from improvements in electrical, thermal and mechanical performances, this technique offers package volume reduction and increased power density. The low-profile and the special dimple structure enable implementation of a multilayered package with control circuit and gate driver integration, which is the technology evolution trend in packaging a wide range of power electronics modules, including inverters for motor drives and converters for power transfer and conditioning. For some novel devices, such as the double-sided IGBT devices developed by the Naval Research Laboratory, DAI has been demonstrated to be a simple, unique, and effective packaging solution for the electrical burn-in test (see Chapter 5 of this thesis).

1.4 Objectives and outline of this thesis

The Dimple Array interconnect technique is a novel approach for interconnecting power devices and packaging high-performance power electronics modules. Therefore, it is imperative to perform a study of various design parameters such as interconnect geometry, material selection, electrical performance, thermal performance and thermomechanical reliability. Since solder alloys are employed as the joining material between power chips and the copper interconnect, their reliability performance is of particular importance. Based on the above reasons, the objectives of this research are:

1. To design and implement a high-performance Dimple Array interconnect technique for packaging power electronics modules; and
2. To analyze of the electrical, thermal and thermomechanical performance of the DAI interconnect technique with particular focus on its thermal fatigue reliability and physics of failure.

Study of the reliability and physics of failure of the DAI is approached from two perspectives: what numerical modeling predicts in terms of change of stress/strain distribution with time, and what the true failure is, according to the thermal/power

cycling experiment and failure analysis. Prototyping and reliability testing are the ultimate and most credible approaches for failure analysis. However, these do not provide insight into the continuous material responses to temperature variations. On the other hand, this well-established modeling approach can display convenient visualization of structure deformation and distribution of stress and strain. Unfortunately, modeling always makes assumptions in material behaviors, ignores interfacial interaction, and in no way incorporates microstructural evolution. Therefore, it is imperative to combine these two approaches for a more accurate physics-of-failure study.

The above research objectives have been divided into the following subtasks:

Chapter 2: Design and development of the Dimple Array interconnect

This chapter first presents previously patented applications of dimpled structures in microelectronics assemblies and processes. Then, the original DAI technique is introduced in its application to power semiconductor devices and modules. Design considerations of the DAI, including current handling capability, thermal management, parasitic inductance and capacitance, geometry, interconnect material, and solder alloy systems are discussed. Last, the development of the fabrication process is presented, and the DAI is demonstrated in a typical half-bridge power electronics module with much improved electrical characteristics.

Chapter 3: Thermomechanical reliability of the Dimple Array interconnect

This chapter examines the thermomechanical reliability of the DAI from an experimental approach. Common reliability evaluation techniques, such as thermal cycling, power cycling, and mechanical testing, are briefly introduced. Failure analysis methods such as acoustic scanning microscopy (SAM) and X-ray inspection for non-destructive inspection, metallographic sectioning, optical microscopy, and scanning electron microscopy (SEM) for destructive inspection, are introduced. After a review of documented approaches to improve solder joint reliability, the reliability design of the DAI is presented. The rest of this chapter describes in details on the experimental testing of the Dimple Array interconnected packages and the controlled collapse bonding flip

chip packages. Failure analysis of these packages is presented and discussed. A comparison is made between the DAI packages and the CCB packages, which shows that the DAI has improved thermal and power cycling capability over the flip chip packages.

Chapter 4: Numerical analysis using finite element simulation
This chapter presents a numerical analysis of the stress, strain and deformation history of the DAI and CCB structures during thermal/power cycling. The finite element method (FEM) is extensively used to simulate complex material responses in both the temperature field and the stress field. A correlation between the FEM results and the experimental testing results has been established. Parametric FEM modeling of the DAI structure illuminates the key parameters that lead to optimum design of the DAI.

Chapter 5: Future applications of the Dimple Array interconnect
In this chapter, packaging of discrete power devices such as a power MOSFET using the DAI technique has been proposed. A thermal evaluation of TO-247 packages interconnected by both the wire bond and the DAI is presented. Reduction of thermal resistance is seen in the DAI package. Then, packaging of the world's first high-power double-sided devices developed by the Naval Research Laboratory, the FTO devices, are achieved using the DAI technique.

1.5 Original contributions

This thesis offers the following original contributions:

1. Proposes an alternative first-level interconnect method, the DAI, for power semiconductor devices with improved electrical, thermal and reliability performance
2. Develops the process for fabrication of the DAI for packaging discrete devices such as the TO-247 package and multichip power electronics modules for converter/inverter applications.
3. Experimentally and numerically analyzes the reliability of the DAI and CCB area array bumping technologies under power cycling and temperature cycling conditions.

1.6 Publications and patents

- J. D. van Wyk, Simon Wen, Z. Liang, J. T. Strydom, S-Y. Lee, W. G. Odendaal and D.A. Huff, "The Development of Planar High Density Hybrid Integration Technologies for Power Electronics," EPE-PEMC 2002 Dubrovnik & Cavtat, Sept. 9-11, 2002.
- Simon Wen, Zhenxian Liang, Victor Liu, Shatil Haque and Guo-Quan Lu, "Power Device Interconnection Techniques Without Using Wire-bonds," the 4th International Symposium on Electronic Packaging Technology, Aug. 8-11, 2001, Beijing, China.
- Simon Wen, Daniel Huff and Guo-Quan Lu, "Enhancement of Thermal Fatigue Reliability of Power Semiconductor Interconnects Using Dimple-Array Solder Joints," the 32nd Power Electronics Specialists Conference (PESC'01), Vancouver, Canada, June 17-22, 2001
- Simon Wen, Daniel Huff and Guo-Quan Lu, "Dimple-Array Interconnect Technique for Packaging Power Semiconductor Devices and Modules," the 13th International Symposium on Power Semiconductor Devices & ICs (ISPSD'01), Osaka, Japan, June 4-7, 2001.
- Simon Wen, Dan Huff and Guo-Quan Lu, "Design and Thermomechanical Analysis of A Dimple-Array Interconnect Technique for Power Semiconductor Devices," the 51st Electronic Components and Technology Conference (ECTC'01), May 29-June 1, 2001, Lake Buena Vista, Florida, USA.
- Simon Wen and Guo-Quan Lu, "Finite-element Modeling of Thermal and Thermomechanical Behavior for Three-dimensional Packaging of Power Electronics Modules," Proceedings of the 7th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, Vol. II, May 23-26, 2000, Las Vegas, Nevada, USA, pp. 303-309.
- G-Q. Lu, J. Calata, S. Wen, S. Dutta, T. Tzeng, C. Stahl and P. Shu, "Packaging of Large-Area Individually Addressable Micro-Mirror Arrays for the Next Generation Space Telescope," to be published at the Symposium on Design, Test, Integration, and Packaging of MEMS/MOEMS, May 6-8, 2002, France.
- Simon S. Wen and Guo-Quan Lu, "Finite Element Modeling of Heat Transfer and Thermal Stresses for Three-dimensional Packaging of Power Electronics Modules,"

Proceedings of the 3rd International Power Electronics and Motion Control Conference, Beijing, China, Aug. 15-18, 2000, pp. 496-501.

- Simon S. Wen, D. Huff and G-Q Lu, "A Dimple-Array Interconnect Technique For Power Semiconductor Devices," MRS Proceedings, Volume 682E, Materials Research Society, San Francisco, CA, April 1-5, 2001.
- Simon Wen, Zhenxian Liang, Guo-Quan Lu and Fred C. Lee, "Thermal Performance of a Power Electronics Module Made by Thin-Film Planar Interconnection of Power Devices," Proceedings, the 8th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, Itherm'02, San Diego, CA, May 2002.

Patent:

A Dimple-Array Interconnect Technique for Semiconductor Devices
Simon Wen and Guo-Quan Lu
VTIP Disclosure No.: 00-012
Virginia Tech Intellectual Properties, Inc.
US Patent application No. **2002/0030276**