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Low temperature processed $0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$ thin films fabricated on multilayer electrode-barrier structure for high-density ferroelectric memories

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Thin films of solid-solution material $0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$ (0.7SBT–0.3BTT) were fabricated on n^+-polycrystalline (n^+-poly) Si substrates by a metalorganic solution deposition technique at a low processing temperature of 650 °C using a Pt–Rh/Pt–Rh–O_x electrode-barrier structure. The Pt–Rh/Pt–Rh–O_x structure was deposited using an *in situ* reactive radio frequency sputtering process. The electrodes had a smooth and fine-grained microstructure and were excellent diffusion barriers between the 0.7SBT–0.3BTT thin film and Si substrate. The ferroelectric (0.7SBT–0.3BTT) test capacitors using these electrode-barrier grown directly on Si showed good ferroelectric hysteresis properties, measured through n^+-poly Si substrate, with $2P_r$ and E_c values of 11.5 μC/cm^2 and 80 kV/cm, respectively, at an applied electric field of 200 kV/cm. The films exhibited good fatigue characteristics (<10% decay) under bipolar stressing up to 10^{11} switching cycles and the leakage current density was lower 10^{-7} A/cm^2 at an applied electric field of 200 kV/cm. The good ferroelectric properties of 0.7SBT–0.3BTT solid-solution thin films at a low processing temperature of 650 °C and excellent electrode-diffusion barrier properties of a Pt–Rh/Pt–Rh–O_x structure are encouraging for the realization of high-density nonvolatile ferroelectric random access memories on silicon substrates. © *1999 American Institute of Physics.* [S0003-6951(99)01240-1]

Layered perovskite materials are being intensively investigated for ferroelectric random access memory (FRAM) devices. Ferroelectric nonvolatile memories have the potential to replace current state-of-the-art nonvolatile memories such as floating and flash erasable programmable read only memories because of their low writing voltages, faster writing speeds, better endurance, and potentially fewer processing steps.[1] $SrBi_2Ta_2O_9$ (SBT), which is one of the bismuth layered-structure compounds, is the most promising candidate for FRAMs with high fatigue endurance and good memory retention. In terms of integration, a one transistor-one capacitor (1T–1C) memory cell structure has been suggested for the realization of high-density ferroelectric memory devices.[2] The basic structure of the 1T–1C cell requires the bottom electrode of the ferroelectric capacitor to be in direct electrical contact with the source/drain of the transistor. The interface reactions between ferroelectric oxide materials and silicon make it difficult to obtain a good ferroelectric/Si interface. For 1T/1C cell designs, electrode materials, such as TiN, which are compatible with both Si and the underlying capacitor electrode must be used. However, the realization of a commercially viable nonvolatile FRAM technology based on SBT has been hampered by problems related to a high processing temperature (>750 °C), low P_r, and low Curie temperature. The rapid oxidation of TiN, which is the industry standard diffusion barrier between metals and Si, results in large volume expansion and degradation of the electrical contacts and makes it unsuitable for ferroelectric materials which require processing temperatures greater than 500 °C. Several metal/metal oxide structures are being investigated to find a suitable electrode/diffusion barrier combination with low resistivity, good adhesion, excellent diffusion barrier properties, good thermal stability, and high chemical corrosion resistance.[1,3–6] However, these electrode or electrode/barrier materials are reported to be stable up to 700 °C which is lower than the commonly reported processing temperature of SBT (750–800 °C) and, for that reason, fewer studies have been focused on the effects of electrode/diffusion barrier materials on the properties of SBT thin films for the realization of high-density memories.[7]

In this letter, we report on the properties of a low temperature processed $0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$ (0.7SBT–0.3BTT) solid-solution thin films fabricated directly on n^+-polycrystalline (n^+-poly) Si substrates with Pt–Rh (10% Rh) and Pt–Rh–O_x as the electrode and diffusion barrier layers, respectively. Pt–Rh–O_x/Pt–Rh/Pt–Rh–O_x electrode-barrier structure was reported to show good electrical conductivity, high temperature stability, excellent diffusion barrier up to high processing temperatures (~ 700 °C), and good adhesion with the ferroelectric thin film and Si substrate.[8] Here, Pt–Rh is the electrode layer, the bottom Pt–Rh–O_x is

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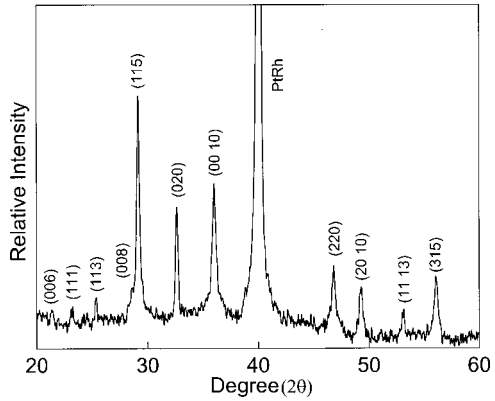

FIG. 1. XRD pattern of $0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$ thin films deposited on electrode-barrier/n^+-poly Si structure and annealed at 650 °C for 60 min.

the diffusion barrier layer, and the top Pt–Rh–O_x layer is the fatigue reduction layer. This electrode-barrier structure becomes even simpler for layered perovskite materials due to their excellent fatigue endurance characteristics. The electrode-diffusion barrier layers were deposited on n^+-poly Si substrates by an *in situ* reactive radio frequency (rf) sputtering process, details of which are described elsewhere.[8] The ferroelectric 0.7SBT–0.3BTT layer was deposited by a metalorganic solution deposition technique using carboxylate-alcoxide precursors.[9] Prior to the deposition of the electrode-barrier layers, the silicon substrates were cleaned by a room-temperature technique entitled spin etching[10] to remove the native silicon oxide and make the substrate surface hydrogen terminated. The post-deposition annealing of the films was carried out at 650 °C for 1 h in an oxygen atmosphere. The thickness of the films, as determined by spectroscopic ellipsometry, was about 2400 Å. The structure and surface morphology of the films were determined by x-ray diffraction (XRD) and atomic force microscopy (AFM). The electrical measurements were conducted on films in Pt–Rh/0.7SBT–0.3BTT/Pt–Rh [metal–ferroelectric–metal (MFM)] and Pt–Rh/0.7SBT–0.3BTT/Pt–Rh/Pt–RhO_x/n^+-poly Si [metal–ferroelectric–metal–oxide–silicon (MFMOS)] configurations. Top Pt–Rh electrodes (10% Rh), area$=3.0\times10^{-4}$ cm^2, were deposited through a shadow mask by rf sputtering. The films were annealed at 600 °C for 2 min after top electrode deposition to get good electrical contact. The bottom metal electrode of MFM capacitors was accessed by etching the 0.7SBT–0.3BTT thin films while a conducting silver adhesive paint was applied to the back surface of the silicon substrate after etching to make electrical contact on MFMOS capacitors.

The structure of the films was analyzed by XRD. The XRD patterns were recorded on a Scintag XDS 2000 diffractometer using Cu K_α radiation at 40 kV. Figure 1 shows the XRD pattern of a 0.7SBT–0.3BTT thin film annealed at 650 °C for 60 min. It was possible to obtain a well-crystallized perovskite phase at an annealing temperature of 650 °C. The intensity and sharpness of the peaks in the XRD pattern of present films was comparable to those deposited on Pt-coated Si wafers indicating a similar order of crystallization.[9] The surface morphology of the 0.7SBT–0.3BTT thin films on a Pt–Rh electrode was analyzed by Digital Instrument's Dimension 3000 AFM using the tapping mode with amplitude modulation. The films exhibited, as

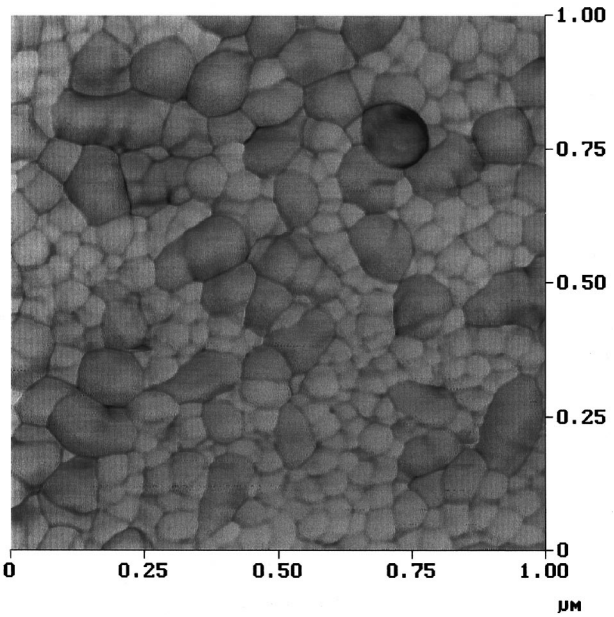

FIG. 2. AFM photograph of $0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$ thin film deposited on Pt–Rh/Pt–Ph–O_x/n^+-poly Si structure and annealed at 650 °C for 60 min.

shown in Fig. 2, a dense microstructure and fine grain size. The average surface roughness of the films was found to be less than 20 nm. The surface morphology of the films deposited on Pt–Rh electrodes showed more uniform grain growth as compared to films deposited on Pt-coated Si substrates where large elongated grains were observed along with small grains.[9] The average grain size was about 130 nm, which is comparable to average grain size observed for films deposited on Pt-coated Si wafers under similar annealing temperature conditions.

The dielectric properties of 0.7SBT–0.3BTT thin films were measured with a HP 4192A impedance analyzer at room temperature. The dielectric measurements were conducted on films in MFM and MFMOS configurations to analyze the diffusion barrier/n^+-poly Si interfacial characteristics. Figure 3 shows the dielectric constant, ϵ_r, and loss factor, tan δ, of MFM and MFMOS capacitors, processed at 650 °C, as a function of frequency. The measured small signal dielectric constant values for MFM and MFMOS capaci-

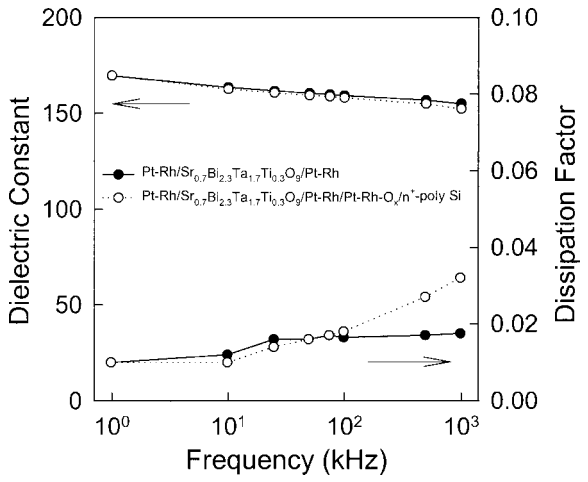

FIG. 3. Dielectric properties of (a) Pt–Rh/$0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$/Pt–Rh and (b) Pt–Rh/$0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$/Pt–Rh/Pt–Ph–O_x/n^+-poly Si capacitors.

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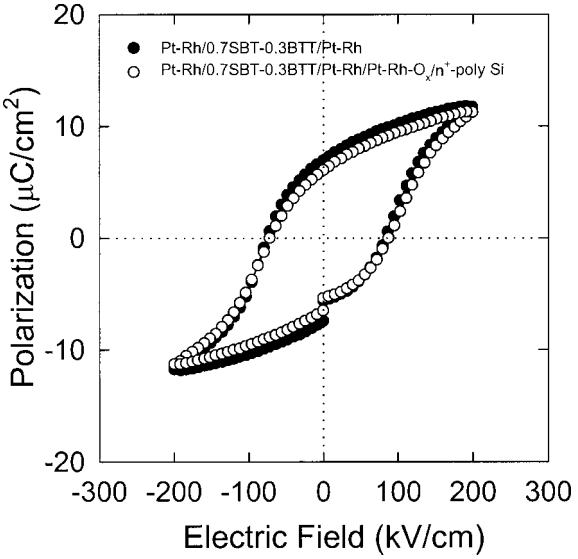

FIG. 4. Ferroelectric hysteresis properties of (a) Pt–Rh/$0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$/Pt–Rh and (b) Pt–Rh/$0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$/Pt–Rh/Pt–Ph–O_x/n^+-poly Si capacitors.

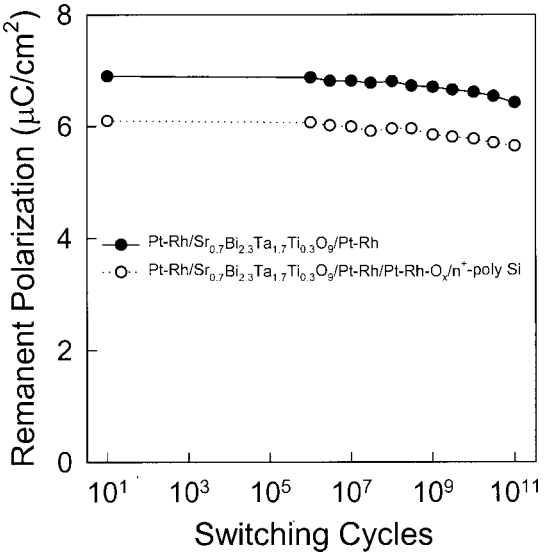

FIG. 5. Fatigue behavior of (a) Pt–Rh/$0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$/Pt–Rh and (b) Pt–Rh/$0.7SrBi_2Ta_2O_9$–$0.3Bi_3TaTiO_9$/Pt–Rh/Pt–Ph–O_x/n^+-poly Si capacitors.

tors were 159 and 158, respectively, at a frequency of 100 KHz. The dielectric constant was found to be slightly smaller for MFMOS capacitors indicating the presence of an oxide layer at the diffusion barrier/n^+-poly Si interface. However, the thickness of the oxide layer was found to be about 1.6 nm indicating that the combination of spin etching and the Pt–Rh–O_x diffusion barrier were effective in minimizing the oxide growth at the interface. Such a thin oxide layer should not screen the electrical response of the ferroelectric thin film through the n^+-poly Si substrate. The dissipation factor of both MFM and MFMOS capacitors was found to be about 1.7% at 100 kHz. However, the dielectric loss for the MFMOS capacitors was found to increase more rapidly with frequency than that of MFM capacitors at frequencies higher than 100 kHz indicating an increase in series resistance of the capacitors as a result of oxide growth at the interface.

Ferroelectric hysteresis measurements were conducted on 0.24-μm-thick 0.7SBT–0.3BTT films in both MFM and MFMOS configurations at room temperature using a standardized RT66A ferroelectric test system. Figure 4 shows typical hysteresis loops of films annealed at 650 °C. The measured remanent polarization ($2P_r$) values for MFM and MFMOS capacitors were 12.6 and 11.5 μC/cm^2, respectively, at an applied electric field of 200 kV/cm. The coercive field (E_c) values for both configurations were about 80 kV/cm. The high value of P_r on Pt–Rh/Pt–Rh–O_x electrode-barrier structure, comparable to the value obtained on Pt-coated Si substrates, indicated good film/electrode-barrier/n^+-poly Si interfacial characteristics.[9] The leakage current density of 0.7SBT–0.3BTT thin films was lower than 10^{-7} A/cm^2 at an applied electric field of 200 kV/cm, indicating good insulating characteristics. The polarization switching endurance tests were performed using an externally generated square wave with amplitude of $\pm$200 kV/cm and a frequency of 500 kHz. Figure 5 shows the decay of the remanent polarization as a function of polarization reversing switching cycles. Both MFM and MFMOS capacitors exhibited similar fatigue characteristics with less than 10% decay in remanent polarization after about 10^{11} switching cycles suggesting the suitability of 0.7SBT–0.3BTT thin films and Pt–Rh/Pt–Rh–O_x electrode-barrier for the fabrication of reliable high-density nonvolatile memories.

In conclusion, polycrystalline 0.7SBT–0.3BTT thin films were successfully produced on n^+-poly Si substrates at a low processing temperature of 650 °C by a metalorganic solution deposition technique using Pt–Rh/Pt–Rh–O_x electrode-barrier layers. The ferroelectric test capacitors showed excellent dielectric, insulating, and ferroelectric properties. The dielectric values did not show any appreciable dispersion with frequency up to about 1 MHz indicating good ferroelectric/electrode-barrier/n^+-Si interfacial characteristics. The typical measured $2P_r$ and E_c values were 11.5 μC/cm^2 and 80 kV/cm, respectively, at an applied electric field of 200 kV/cm. At this bias, the leakage current density was lower than 10^{-7} A/cm^2. The switching degradation of the polarization state was found to be less than 10% after about 10^{11} polarization reversing switching cycles. The low processing temperature of 650 °C and good structural, insulating, and ferroelectric properties of 0.7SBT–0.3BTT thin films, and excellent barrier properties of the multilayer electrode structure show promise for the integration of ferroelectric capacitors in the very large scale integrated nonvolatile random access memory cell structures.

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