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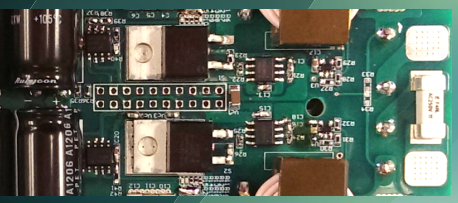
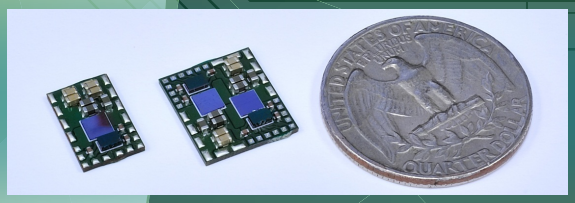
CPES

Center for Power Electronics Systems

2014 ANNUAL REPORT

VIRGINIA TECH · BLACKSBURG, VIRGINIA





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INTRODUCTION

The Center for Power Electronics Systems at Virginia Tech is a research center dedicated to improving electrical power processing and distribution that impact systems of all sizes – from battery – operated electronics to vehicles to regional and national electrical distribution systems.

Our mission is to provide leadership through global collaborative research and education for creating advanced electric power processing systems of the highest value to society.

CPES, with annual research expenditures of $5 million US dollars, has a worldwide reputation for its research advances, its work with industry, and its many talented graduates. From its background as an Engineering Research Center for the National Science Foundation during 1998 - 2008, CPES has continued to work towards making electric power processing more efficient and more exact in order to reduce energy consumption.

Power electronics is the "enabling infrastructure technology" that promotes the conversion of electrical power from its raw form to the form needed by machines, motors and electronic equipment. Advances in power electronics can reduce power conversion loss and in turn increase energy efficiency of equipment and processes using electrical power. This results in increased industrial productivity and product quality. With widespread use of power electronics technology, the United States would be able to cut electrical energy consumption by 33 percent. This energy savings in the United States alone is estimated to be the equivalent of output from 840 fossil fuel based generating plants. This savings would result in enormous economic, environmental and social benefits.

OVERVIEW

CPES INDUSTRY CONSORTIUM

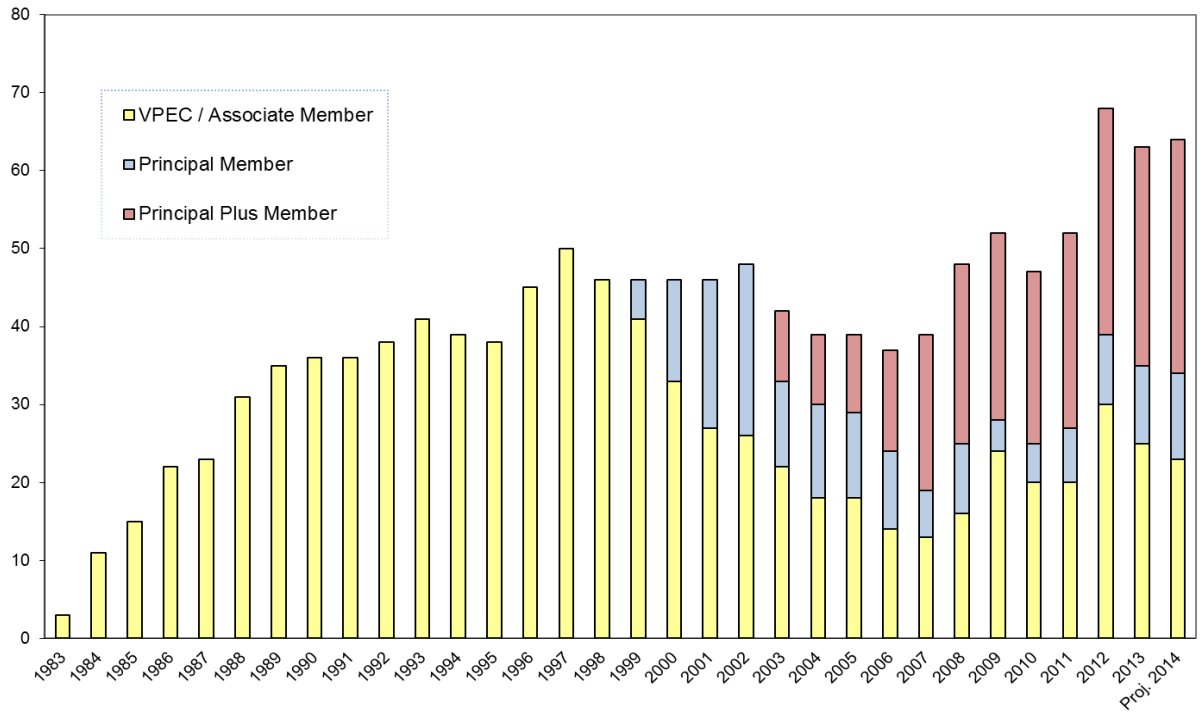
The CPES industrial consortium is designed to cultivate connectivity among researchers in academia and industry, as well as create synergy within the network of industry members. The CPES industrial consortium offers the best mechanism to stay abreast of technological developments in power electronics.

The CPES connection provides the competitive edge to industry members via:

- Access to state-of-the-art facilities, faculty expertise, top-notch students
- Leveraged research funding of over $5 million per year
- Industry influence via Industry Advisory Board and research champions
- Intellectual properties with early access for Principal Plus and Principal members via CPES IPPF (Intellectual Property Protection Fund)
- Technology transfer made possible via special access to the Center's multi-disciplinary team of researchers, and resulting publications, presentations and intellectual properties
- Continuing education opportunities via professional short courses offered at a significant discount
- Option to send engineers to work with CPES researchers on Campus via the Industry Residence Program.

The CPES industrial consortium offers the ideal forum for networking with leading-edge companies and top-notch researchers and provides the best mechanism to stay abreast of technological developments in power electronics.

CPES MEMBERSHIP COMPANY GROWTH



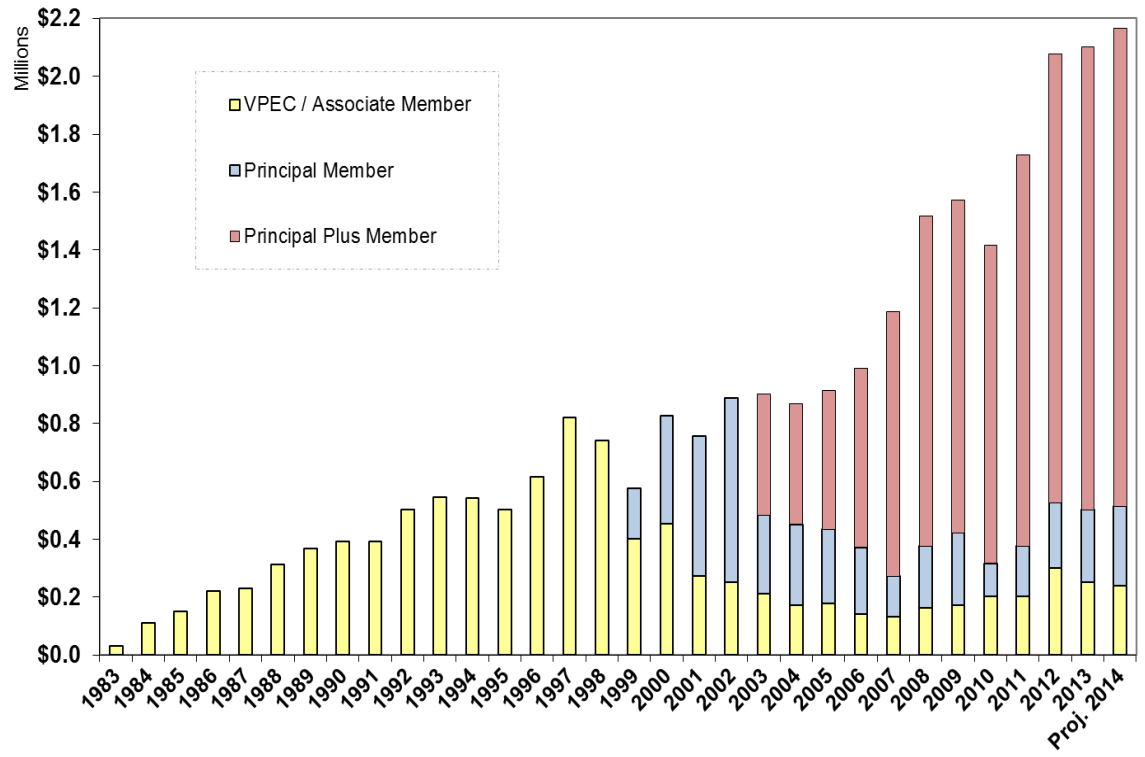
Principal Plus Members (annual contribution - $50,000) - gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research -- PMC (Power Management Consortium), HDI (High Density Integration), or REN (Renewable Energy and Nanogrids). Companies interested in more than one focused research areas may join another mini-consortium for an additional annual contribution of $50,000 each. In additiion to all the benefits offered to Principal and Associate Members, Principal Plus Members have easy access to cutting-edge IPs via CPES IPPF (Intellectual Property Protection Fund).

Principal Members (annual contribution - $25,000) - are well positioned to influence and guide CPES as Industry Advisory Board (IAB) members. Principal Members also have cutting-edge IP advantage via automatic IPPF (Intellectual Property Protection Fund), in addition to all the benefits offered to Associate Members.

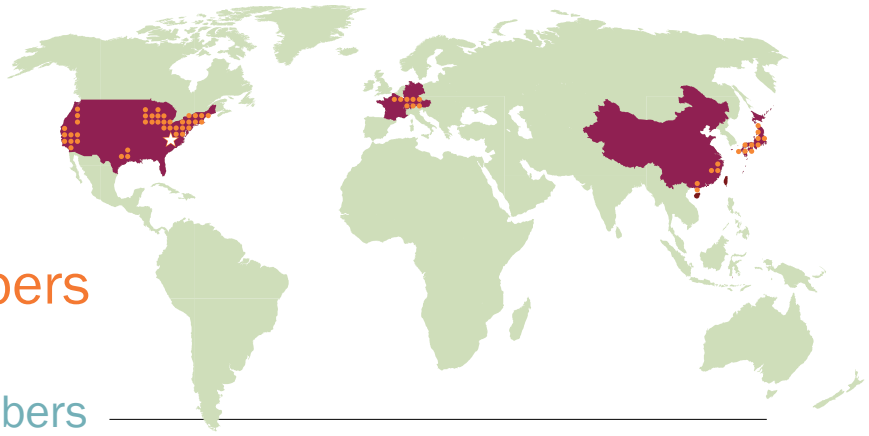
Associate Members (annual contribution - $10,000) - gain the competitive edge, not only through easy access to CPES research results, researchers, and state-of-the-art facilities, but also opportunities for technical exchanges via the Industry Residence Program and continuing education via CPES short course to stay abreast of new technologies. Companies participating in the Industry Residence Program must be actively engaged in collaborative research with the Center in technical areas that are of mutual interest, to be determined jointly with CPES faculty host.

Affiliate Members make in-kind hardware/software donations to CPES equivalent to $10,000 per year. Their contributions must be relevant to CPES research. Membership participation at this level requires Center Director approval.

INDUSTRY MEMBERSHIP FUNDING GROWTH



CPES



Industry members

Principal Plus Members

ABB, Inc.
Agilent Technologies
Alstom Transport
Chicony Power Technology Co., Ltd.
China Nat'l Electric Apparatus Res. Inst.
Crane Aerospace & Electronics
CSR Zhuzhou Institute Co., Ltd.
Delta Electronics, Inc.
GE Global Research
GE Power Conversion, Inc.
General Motors
Groupe SAFRAN
Huawei Technologies Co., Ltd.
Infineon Technologies
International Rectifier
Linear Technology
Macroblock, Inc.
Mitsubishi Electric Corporation
Murata Manufacturing Co., Ltd.
NEC TOKIN Corporation
Nissan Motor Co., Ltd.
NXP Semiconductors
Richtek Technology Corporation
Rolls-Royce
Samsung Electronics Co.
Siemens Corporate Research
Sumitomo Electric Industries, Ltd.
Texas Instruments
The Boeing Company
Toyota Motor Engineering & Manufacturing North America, Inc.
United Technologies Research Center
ZTE Corporation

Principal Members

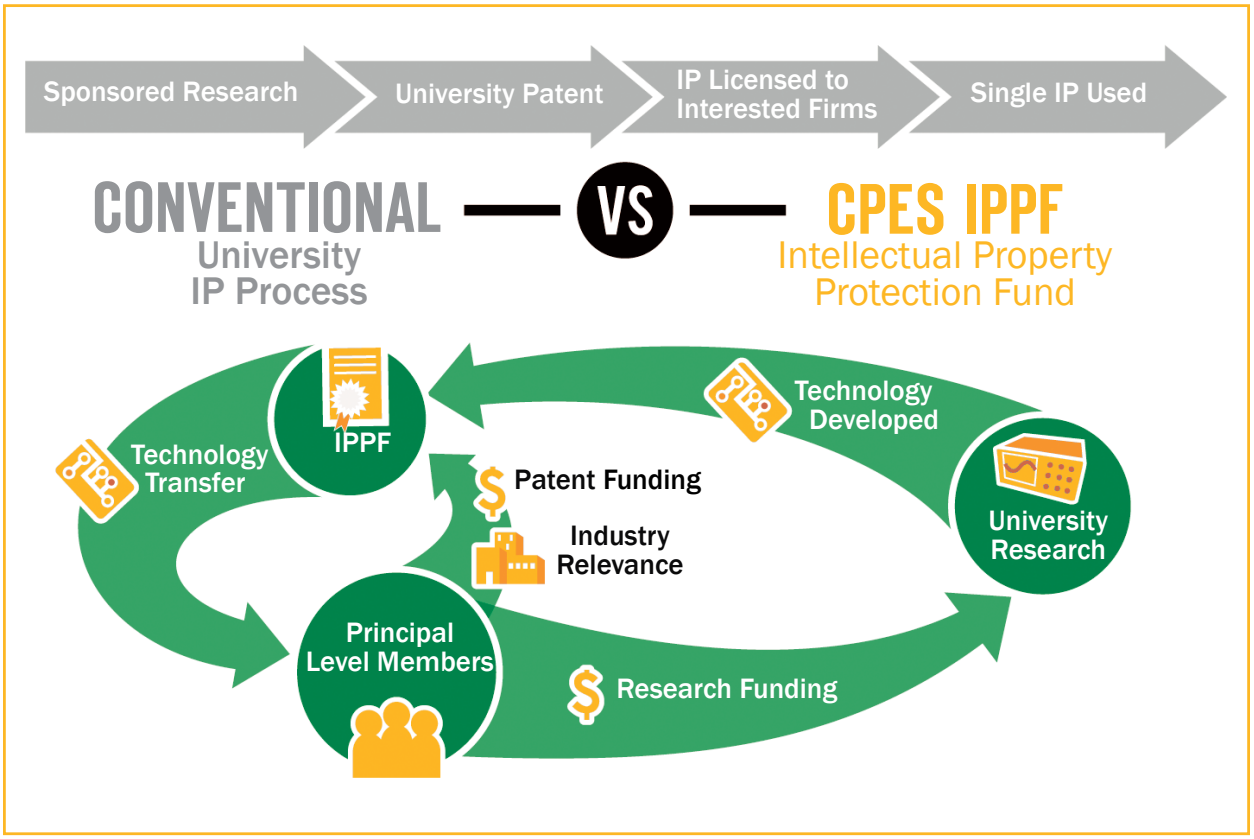
AcBel Polytech, Inc.
Altera - Enpirion Power
Analog Devices
Eltek
Emerson Network Power
Fairchild Semiconductor Corp.
Halliburton
Maxim Integrated Products
ON Semiconductor
Power Integrations

Associate Members

AVX Corporation
Calsonic Kansei Corporation
Crown International
Cummins, Inc.
Delphi Electronics & Safety
Dyson Technology Ltd.
Eaton Corporation, Innovation Center
Efficient Power Conversion
GHO Ventures, LLC
Hitachi Computer Peripherals Co., Ltd.
Hitachi, Ltd.
Inventronics (Hangzhou), Inc.
Johnson Controls, Inc.
Lexmark International
Lite-On Technology Corporation
LS Industrial Systems Co., Ltd.
Marvell International Ltd.
Metamagnetics, Inc.
Microsoft Corporation
Monolithic Power Systems
NetPower Technologies, Inc.
OSRAM Sylvania, Inc.
Panasonic Corporation
Schaffner EMV AG
Shindengen Electric Mfg. Co., Ltd.
Silergy Technology
TDK Lambda Corporation
Toyota Motor Corporation
Universal Lighting Technologies, Inc.

Affiliate Members

ANSYS, Inc.
ChiasTek, Inc.
CISSOID
Electronic Concepts
Plexim GmbH
Rohde & Schwarz
Simplis Technologies, Inc.
Synopsys, Inc.
Tektronix, Inc.
Transphorm, Inc.
Trendsetter Electronics
VPT, Inc.



Intellectual Property Protection Fund

IPPF is a unique IP access mechanism that provides extraordinary IP advantage to all Principal-level members. IPPF is available automatically, at no additional cost, to Principal Plus and Principal members. IPPF members meet quarterly with inventors to discuss invention disclosures and jointly decide which technologies to protect, with patenting costs covered by IPPF. Once a technology is protected, IPPF members are granted a royalty-free, non-exclusive, non-transferable license to use the technology. IPPF is applicable only to technologies developed by CPES-VT researchers under the CPES industry consortium.

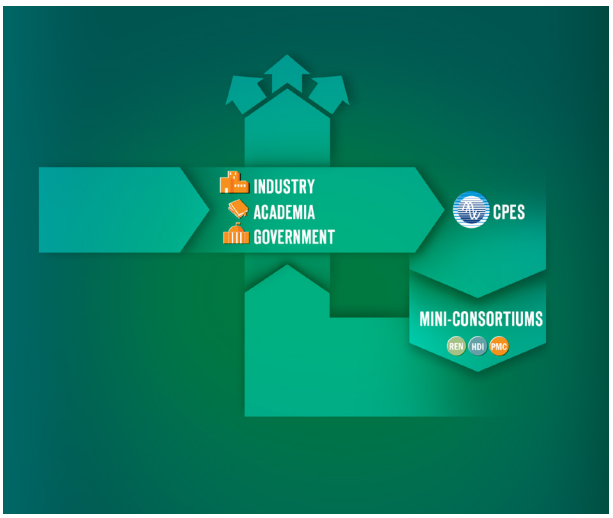
CPES Mini-Consortium Program

The CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The formation of the mini-consortium allows CPES to pool resources and focus on developing pre-competitive technologies to address common challenges, and sharing the research results among mini-consortium members.

Mini-consortium members are enrolled in CPES as Principal Plus Members, with annual contribution of $50,000. They gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research:

- PMC (Power Management Consortium)
- HDI (High Density Integration)
- REN (Renewable Energy and Nanogrids)

Companies interested in more than one focused research areas may join another mini-consortium for an additional annual contribution of $50,000 each.



Power Management Consortium (PMC)

In 1997, at the request of Intel, CPES established a mini-consortium to address the issue of power management for future generations of microprocessors, targeting at sub-1 volt and 100-200 amps current. As a result of this focused research, the CPES team has developed a multi-phased voltage regulator module. Instead of paralleling power semiconductor devices in order to meet the current demand and efficiency requirements, the research team proposed to parallel a number of mini-converters. By paralleling the mini-converters and phase-shifting the clock signal, not only were we able to cancel the significant part of the output current ripple, but also to increase the ripple frequency by N time, where N is the number of channels we parallel. This resulted in demonstrated improvement, specifically, 4 times improvement in transient response, 10 times reduction in output filter inductors, 6 times reduction in output capacitors, 6 times improvement in power density, and 3 times improvement in profile.

The new generation of Intel's microprocessor is operating at a much lower voltage and higher current, with a fast dynamic response in order to implement the sleep/power mode of operation. This particular mode of operation is necessary to conserve energy, as well as to extend the operation time for any battery-operated equipment. The challenge for the voltage regulator module in this case is to provide a precisely regulated output with fast dynamic response in order to transfer energy as fast as possible to the microprocessor.

Today, every Intel processor is powered by such multi-phased VRMs developed by CPES. CPES researchers are focused on developing pre-competitive technologies in the areas of power management for distributed power system architectures, EMI/EMC, power quality, high-frequency/high-density AC/DC and DC/DC converters, voltage regulator (VR) and POL converters in such applications as powering the microprocessor, tablet, notebook, desktop, server, networking products, telecom equipment, solid state lighting, battery system, PV system and other electronic applications.

Power Management Consortium (PMC)

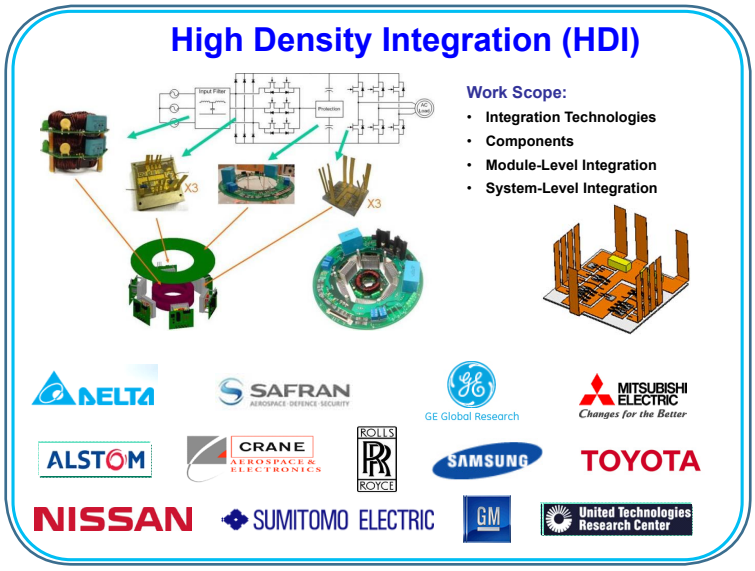
Chicony Power Technology
DELTA
HUAWEI
muRata
infineon
International Rectifier
NXP

NEC/TOKIN
Macroblock
CSR
Texas Instruments
ZTE中兴
LINEAR TECHNOLOGY
RICHTEK

WORK SCOPE:

- High-Performance VRM/POL Converters
- High-Frequency Magnetics Characterization and Design
- High-Frequency Modeling
- Digital Control
- High Efficiency Power Architectures for Laptops, Desktops and Servers
- EMI
- Solid State Lighting
- Power Management for PV System
- Power Management for Battery System

Mini-Consortium on High Density Integration (HDI)



Over the past two decades, CPES has secured research funding from major industries, such as GE, Rolls-Royce, Boeing, Alstom, ABB, Toyota, Nissan, Raytheon, and MKS, as well as from government agencies including the NSF, DOE, DARPA, ONR, U.S. Army, and the U.S. Air Force, in research pursuing high-density system design. CPES has developed unique high-temperature packaging technology critical to the future power-electronic industry.

In the HDI mini-consortium, the goal of high power density will be pursued following two coupled paths, both leveraging the availability of wide-bandgap power semiconductor, as well as high-temperature passive components and ancillary functions. The switching frequency will be pushed as high as component technologies, thermal management, and reliability permit. At the same time, the maximum component temperatures will be pushed as high as component technologies, thermal management, and reliability permit.

The emergence of wide-bandgap semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) makes it possible to realize power switches that operate at frequency beyond 5 MHz and temperature beyond 200° C. As the switching frequency increases, switching noise is shifted to higher frequency and can be filtered with small passive components, leading to improved power density. Higher operating temperatures enable increased power density and applications under harsh environments, such as military systems, transportation systems, and outdoor industrial and utility systems.

The HDI mini-consortium recognizes that the high-frequency, high-temperature switches need to be accompanied by high-frequency or high-temperature components and packages in the remainder of the power-electronic system. Thus, HDI has developed die-attach materials that can be processed at low temperature, yet are reliable at the temperature of the wide-band-gap junction. Processes have been developed to encapsulate ultra-thin planar packages with polymer having high glass-transition temperature and dielectric strength. Techniques to decouple the noise loops have been identified to enable high-dV/dt commutation. Magnetic powder with low core loss density has been synthesized from magnetic metals for 1–5 MHz operation. Inductors have been integrated into the converter package as a substrate to achieve power density approaching 1 kW/in^3. Design methodologies for high-temperature capacitors, power buses, protection, sensing, digital control, etc. have also been documented.

The current scope of work being conducted includes the following topics:

- **Integration technologies -**
  - Die-attachment on copper surface by sintering of nano-scale silver paste -
  - High-temperature encapsulants for power electronic modules – thermal stability of nano-composites -
  - Magnetic materials for high-frequency conversion and EMI containment
- **Components -**
  - Characterization and modeling of wide-bandgap semiconductor devices -
  - Low-profile magnetic substrate -
  - Magnetic structures with high energy density
- **Module-level integration -**
  - High-speed and high-temperature SiC power module for high-frequency motor drive systems -
  - High-temperature performance and reliability of planar power modules with double sided cooling capability and sintered joints
  - Integrated-passives module for resonant conversion and EMI containment
- **System-level integration -**
  - High-frequency converter packaging -
  - EMI and emission containment -
  - High-temperature converter packaging

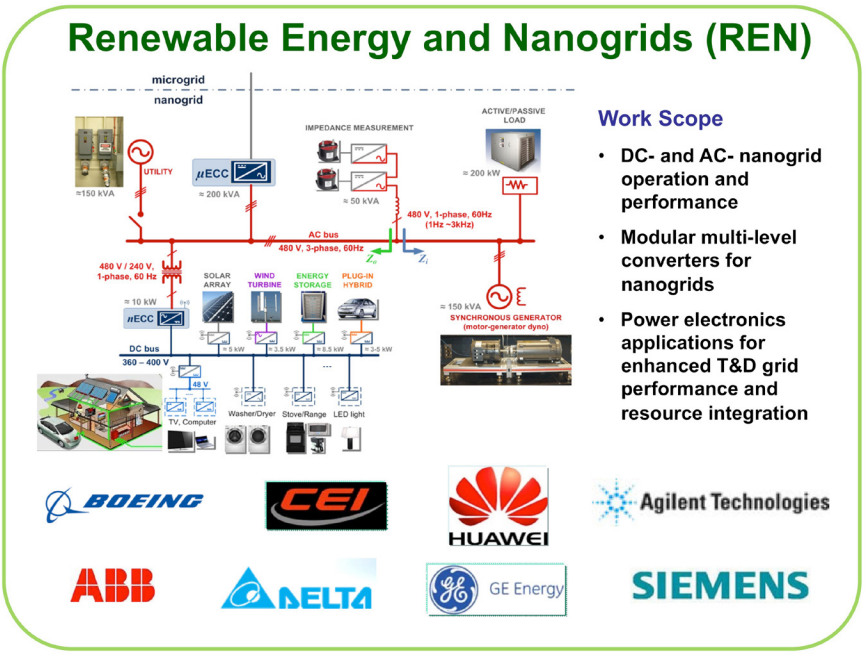
Mini-Consortium on Renewable Energy and Nanogrids (REN)

This CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The formation of the REN mini-consortium allows CPES to pool resources and focus on developing pre-competitive technologies to address common challenges, and sharing the research results among mini-consortium members. The main objective of the REN mini-consortium is to expand CPES' expertise in autonomous electric power systems (already established for transportation and IT), into the area of renewable energy and storage systems integration in the electric grid through power electronic converters, while providing competitive research and education in that area.

The current research directions of the REN mini-consortium comprise three different topics listed below with corresponding sub-topics. Additionally a REN system testbed structure is planned to be designed and built in the near future for the experimental validation purposes.

WORK SCOPE:

- **dc- Nanogrid Operation and Performance**
  - Nanogrid architectures and design (380 V dc bus, 48 V dc bus, and 480 V ac bus)
  - Bidirectional ac-dc nanogrid-interface converter – Energy Control Center
  - Battery-, PV- and wind- interface converters
  - Power management strategies and optimization of energy utilization (wind, PV and storage in nanogrids)
  - System stability, operation and performance
  - Hierarchical system modeling, analysis, and design
  - Dc outlets, ac and dc fault current limiting, system protection, prevention of arcing, etc.
- **Modular Multi-level Converters for Nanogrids**
  - 3-level bidirectional ac-dc nanogrid-interface converter
  - Harmonic/EMI filter design for interconnection of multi-level converters to nanogrids
  - Modeling, design and control of modular multi-level converters
  - Modular multi-level converter for impedance measurements in ac- and dc- nanogrids
- **Power Electronics Applications for Enhanced Grid Performance and Resource Integration**
  - Hierarchical network of dynamically-decoupled electronically-interconnected sub-networks (picogrid, nanogrid, microgrid, …intergrid)
  - Power sharing, dynamic interactions, and stability in grid-connected and islanded systems with power electronics converters
  - Use of power electronics converters at distribution and transmission levels for *P-f* and *Q-V* operation.

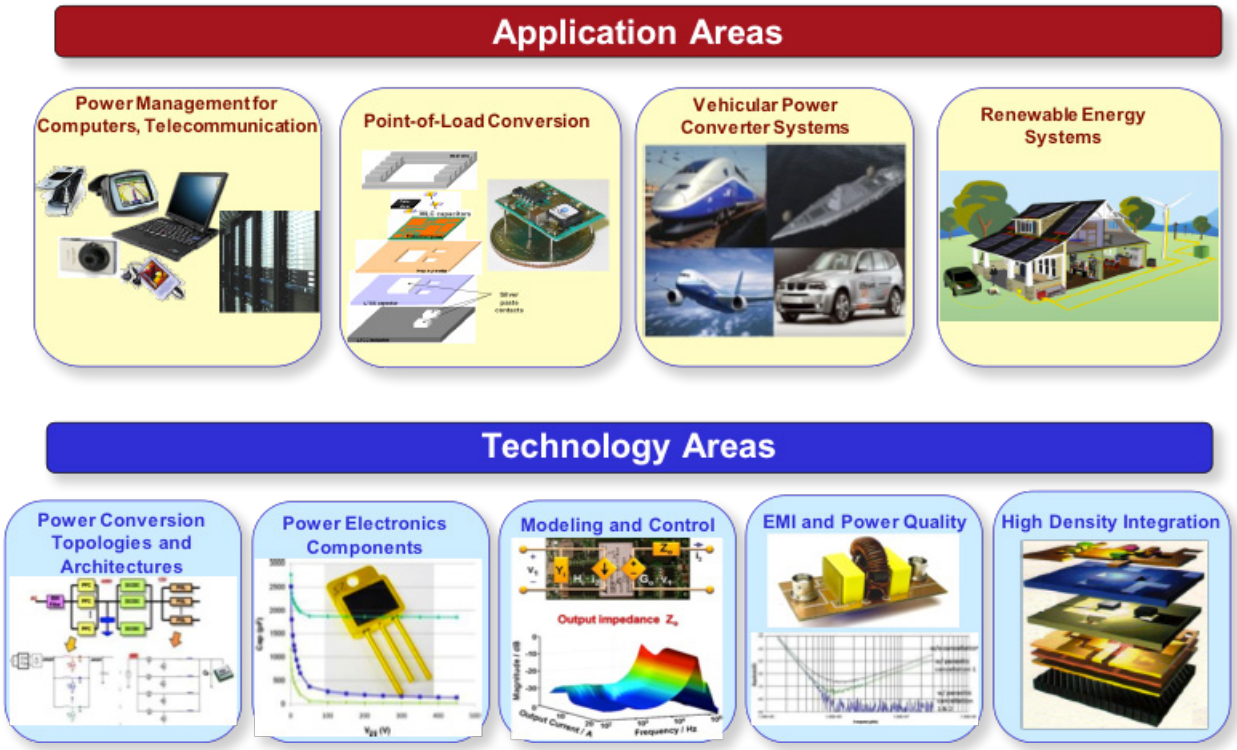


RESEARCH

In its efforts to develop power processing systems to take electricity to the next step, CPES has developed research expertise encompassing five technology areas: (1) power conversion technologies and architectures; (2) power electronics components; (3) modeling and control; (4) EMI and power quality; (5) high density integration.

These technology areas target applications that include: (1) Power management for information and communications technology; (2) Point-of-load conversion for power supplies; (3) Vehicular power conversion systems; (4) Renewable energy systems.

In 2014, CPES sponsored research totaled approximately $3 million. The following abstracts provide a quick insight to the current research efforts.



Sponsored Research

Power Supplies on a Chip (PSOC)

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency Energy, Agile Delivery of Electrical Power Technology)
Research collaborators: International Rectifier, University of Delaware, Enpirion
(September 1, 2010- March 31, 2014)

The first phase of the project aims to develop a proof of-concept prototype power supply on chip (PSOC) using-GaN devices operating at 5-l0MHz. The target was to achieve a power density greater than 1000W/in 3 with 88% efficiency. The proposed three-dimensional PSOC would be constructed using IR's GaN devices and Si-gate driver IC's assembled on top of a 1 mm magnetic substrate using a high frequency soft magnetic material. Such a level of integration has never been attempted with a current greater than 5A. The proposed prototypes will extend the current to 20- 40A at 12V input voltage, targeting such applications as computer, mobile electronics,and telecommunication. After successful completion of phase 1, a 5MHz, 12V to 1.2V, 20A, two-phase integrated POL converter with GaN transistors and coupled-inductor substrate is demonstrated with power density as high as 1000 W/in 3,which is a factor of 10 improvements compared to industry products at the same current level. In phase II, CPES is collaborating with Enpirion/Altera and focusing on commercializing this 3D integrated POL module. We are trying to transfer CPES's technologies, such as inductor substrate and 3 packaging design into Enpirion's products to develop silicon based 1-2MHz, 15-20A, 3D integrated POL module, which still can achieve power density as high as 900W/in 3. Currently both single phase and two phase modules have been fabricated. The performance of single phase module successfully meets the design targets. The evaluation of two phase module is undergoing. Furthermore, we will do research on design optimization of the two phase coupled inductor to improve its transient performance for whole load range.

A Study of Multi-Channel Constant Current Driver for Multiple Solid-State Light Sources on DC Distribution System

Sponsored by: Panasonic Electric Works
(April 1, 2011 - March 31, 2014)

Recently, many applications such as display backlighting, indoor lighting and street lighting, all prefer multi-channel LED drivers. In this project, a design methodology for MC3 LLC LED driver has been developed. The frequency controlled analog dimming solution has been verified by both simulation and experimentation. The circuit behavior under open and short failure is investigated as well. Moreover, in order to achieve lower dimming ratio and keep higher efficiency, the hybrid control approach combining with asymmetrical PWM control and frequency control is proposed. We are currently developing a two stage LED driver with multi-channel constant current resonant converter, which can drive multiple LED strings with uneven LED number.

Multi-Phase Auto-Tuning Self Compensating Power Supply Control Systems

Sponsored by: Energy Research Corporation
(September 1, 2012 – August 31, 2014)

The multi-phase voltage regulator (VR) has been widely used to power microprocessors. For multi-phase VR, a constant output impedance design is usually used to reduce the output capacitor bank. Conventionally, a fixed analog compensation network is chosen to compensate the worst-case component (such as inductor and output capacitor) variations on the plant, which will limit the converter bandwidth. Furthermore, since a microprocessor runs into sleep mode very frequently, several green-mode functions have been used to improve the light load efficiency such as phase shedding, discontinuous mode operation, and frequency changes. However, the plant characteristic will also change with these techniques under sleep mode, and will influence the stability and transient response during mode transitions. Therefore, it is very challenging and attractive to investigate multi-phase self tuning power supply control systems which can compensate the component variation and mode transition without suffering from the worst-case design compromises. In this project, a self-tuning power supply control system

will be developed to self-identify the plant characteristic change from component variation and operating mode transitions, and then adaptively adjust the compensation parameters to maintain stability and system performance. Therefore, external compensation circuitry and the output capacitor bank can be reduced to reduce total cost. We have already proposed several control methods with auto-tuning function to improve transient performance of voltage regulator. We are currently doing the prototype development.

Gallium Nitride Switch Technology for Bi-Directional Battery to Grid Charger Application

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency - Energy, Agile Delivery of Electrical Power Technology)
Sub – Awardee of: HRL
(October 1, 2010 – March 31, 2014)

The purpose of the project is to develop efficient, high power, and cost effective power converters with application to the automotive sector. More specifically, it will utilize high voltage Gallium Nitride (GaN) on low cost silicon substrate switches operating at megahertz frequencies. GaN semiconductors process electricity faster than the silicon semiconductors used in most conventional EV battery chargers. These high-speed semiconductors can be paired with lighter-weight electrical circuit components, which helps decrease the overall weight of the EV battery charger. The innovative design will result in a battery-to-grid bi-directional charger that enables efficient, cost effective power management focusing on grid-interactive distributed energy systems for the automotive sector.

High Density Motor Controller

Sponsored by: The Boeing Company
(August 1, 2005 – March 31, 2014)

In this project, a 10 kW high power density three-phase ac-dc-ac converter together with a high density PCB axial flux motor were developed and electrically evaluated. The converter consists of a Vienna-type rectifier front end and a two-level voltage source inverter (VSI). In order to reduce the switching loss and achieve a high operating junction temperature, SiC JFETs and SiC Schottky diodes are utilized. The design considerations for the phase-leg units, the gate driver, the input filter, the system protection and motor operation are investigated in detail. Experiments are carried out under different conditions, and the results verify the feasibility of the full system.

A second phase of the project has devoted its effort to the weight minimization of the inverter and EMI filters required by 100 kW motor controllers. To this end parallel converter configurations have been explored using symmetric and asymmetric interleaving PWM techniques, which have achieved harmonic cancellation at both the AC and DC terminals of power converters with a great impact on the EMI filter weight minimization. Additionally, multi-level power converter topologies have been investigated seeking further reduction of EMI emissions, higher power conversion efficiency, and superior power density.

System Stability and Analysis

Sponsored by: The Boeing Company
(October 22, 2004 – December 31, 2013)

CPES has developed design criteria and analysis tools for integrating ac and dc distributed power electronics conversion systems for the stable, safe and reliable operation of future aircraft electrical power systems. These power electronics systems combine numerous and different types of power converters, which when interconnected can easily interact with each other if no precautionary measures are taken. These interactions can easily lead to instabilities and system faults. Therefore, it is important to study the operation of the system carefully as part of its design process. As a demonstration testbed, CPES modeled a large electrical distribution system where it addressed the actual model implementation of the several components considered using the detailed switching models. CPES also evaluated the testbed correct operation by means of Lyapunov's indirect method—local assessment of large signal stability, studying as well the effect of faults in the system providing insight into the choice of models for the respective studies conducted. In addition, CPES developed ac-system small-signal stability criteria. For the verification of these stability analysis, CPES has developed an AC impedance tester to be capable of measuring the synchronous d-q frame impedance of ac networks and power converters for later use in stability studies. After delivering a first unit, CPES has developed an upgraded impedance tester unit capable of measuring in both shunt and series connection modes for improved accuracy.

In order to facilitate complex system-level simulation and analysis, CPES is developing enhanced average models that should be capable of capturing not just the fundamental frequency but also the mid-frequency range (up to half of switching frequency) large-signal behavior of power converters. The enhanced converter models will enable the simulation and study of phenomena otherwise neglected by conventional average models, including

distortion induced by dead-time, digital sampling, and other controller and power stage nonlinearities. To this end CPES has adopted an advanced modeling framework, namely validation, verification and uncertainty quantification (VV&UQ), which will empower the simulations conducted to fully estimate the level of uncertainty in the simulation predictions by taking into consideration all random (aleatory) uncertainty and lack-of- knowledge (epistemic) uncertainty in model inputs. In addition, it incorporates uncertainty due to the mathematical form of the model (relative to actual test data) and it provides a procedure for quantifying uncertainty due to numerical errors. The application of this modeling framework to a three-phase boost rectifier is presently underway.

Optimization of AC/AC Motor Controller Power Quality and EMI Filter Topology

Sponsored by: United Technologies Aerospace Systems
(January 1, 2012- December 31, 2014)

The objective of this work was the optimization of the combined power quality and EMI filters for motor controller comprising input power circuits fed by variable frequency power bus, and output power circuits that drive variable speed electric motors. The effect of the thermal and electrical characteristics associated with new materials with particular application on the EMI and PQ filters was thoroughly investigated demonstrating the advantages offered. From an EMI-filter weight minimization standpoint, interleaved two-level topologies, three-level topologies and 18-switch matrix converters were evaluated and compared face-to-face against the state-of-the-art two-level topology.

The second phase of this work has honed its efforts on the optimization of small local converters, each built on PCB cards addressing the combined power quality, EMI and thermal requirements and fed by variable frequency AC or higher voltage DC power bus and output power circuits that provide regulated 28 V DC power. The effect of the thermal and electrical characteristics associated with a number of power topologies and the trade off in their performance in terms of weight, size and perceived reliability was investigated. Addressing single-phase power conversion first, a novel three-level semi-bridgeless PFC topology was developed to achieve 99% efficiency. For three-phase power conversion, a dual channel Vienna-type three-level converter was developed and tested surpassing 99% efficiency too. The third phase of this project will address the efficient power conversion from 270 V DC to 28 V DC.

High-Temperature, High Power Density Power Converter for Embedded Generators

Sponsored by: Rolls Royce
(January 1, 2011 – September 30, 2013)

The objective of this project was to evaluate and demonstrate the feasibility of developing a complete high-power, high-temperature, high-power-density bidirectional three-phase ac-dc power converter unit required to operate embedded in generators at temperatures ranging from 200-250° C. In the Phase II of this program, the focus was on the development and validation of the critical system components at the rated power and temperature, and on the functional integration of the equivalent low-temperature subsystems at reduced power level.

The final phase of this project concentrated on the thermo-mechanical design, integration of all the system components and subsystems, and on the testing, characterization, evaluation, and demonstration of the complete system at full power and high ambient temperature. As a result a 50 kW three-phase power converter using 1.2 kV, 100 A SiC power modules designed and built at CPES and rated at 200° C was successfully built and demonstrated to operate in this high temperature environment.

Terminal Modeling of Noise Source in Switching Power Converters

Sponsored by: Hispano Suiza, SAFRAN
(October 1, 2010 -September 30, 2014)

The main objective of this research is to develop terminal models of noise sources in switching converters for easy EMI analysis. These models must be scalable for different load and source conditions. Conventional methods of EMI modeling use physics based models of semi-conductor devices and EMI coupling paths. Due to the complex nature of these models the simulations often fail to converge or lead to unusable results.

In its latest phase this project is exploring the use of terminal models for the development of EMI filter design procedure. Its main focus is the design of filters for parallel inverters using interleaved PWM techniques.

The efforts in this research are aimed at simplifying the simulations by using Thevenin or Norton models of these noise cells. Here "noise-cell" may refer to both device level (single device or a Phase-leg) and converter level abstraction. The afore method has been successfully demonstrated so far on an industrial low-voltage 10 kW motor drive, for which the unterminated EMI model of its 3-phase voltage source inverter (VSI) was built showing how it could predict the EMI behavior of the motor drive under varying conditions. The present effort in this topic is

the development of said EMI model for SiC-based power converters switching at 50–100 kHz, in order to assess the prediction capability for high switching frequency power converters.

A new research area recently opened in this project has been to explore the benefits and challenges from an EMI emission and filtering standpoint that multilevel power converters offer. These are increasingly replacing two-level converters in various applications due to their overall better performance; especially in what regards harmonic and EMI standards compliance.

Impedance Measurement Unit (IMU) for 4160V AC Networks

Sponsored by: Office of Naval Research

(November 1, 2012 – June 30, 2014)

In this project, CPES will design, construct, integrate and test a medium voltage (MV) impedance measurement unit (IMU) to assess the stability of electric power systems and components for future Navy electric ships. The IMU will be rated at 4160 V AC, 100 A, and uses 10 kV SiC semiconductor devices to demonstrate its operation at higher voltages and power level, as well as their exceedingly faster switching speeds enabling the IMU to characterize impedances from DC up to 1kHz. At the intermediate scale, the IMU will be capable of injecting 5% system current and 5% system voltage, performing all the data acquisition and necessary post processing. CPES will investigate the use of modular power converter topologies suitable for scaling the IMU towards higher MV networks, as well as single-phase injector solutions capable of measuring three-phase synchronous d-q frame impedances in an effort to reduce the overall complexity of the IMU.

The Next Generation Power Converter: Applications for Enhanced T&D Grid Performance and Resource Integration

Sponsored by: URS Energy and Construction/National Energy Technology Laboratory

(July 1, 2012 – November 14, 2013)

As a member of the NETL-RUA Grid Technologies Collaborative (GTC) group, CPES has been putting efforts on researching power electronics converter technology that can enable major improvements in performance, reliability, and maximal utilization of the renewable energy sources and energy storage systems that can be integrated into the electric power system. The main goal of the work in the first phase of the project was to explore functionality and performance of the bidirectional three-phase ac/dc (micro)grid-interface converter for the medium-voltage high-power applications (through functional average models), together with developing some specifications for the converter design that allow an on-demand active and reactive power delivery, as well as P-f control of the grid. The second phase of the project focused on analyzing the low-frequency dynamic interactions caused by power converters and synchronous generators, as well as exploring relationships and defining the physical/mathematical equivalency between them using both, analytical approach and simulation (average) models. In its latest phase this project is exploring the similarities between synchronous generators and power converters to investigate the potential advantages that the latter can offer over traditional power generation.

Reliability-Oriented Design of Modular MV and HV Power Converters

Sponsored by: ABB Corporate Research

(May 1, 2013 – April 30, 2014)

The critical nature of grid applications in power engineering demands the utmost levels of reliability of its apparatus, as well as high availability and low maintenance requirements.

The latter implies additionally a high lifetime of all components used. Power electronics, now a mature technology—it is currently employed in critical applications such as commercial aviation, is being increasingly introduced in grid applications to improve the controllability and efficiency of power flow within power grids. The design of power converters at medium voltage (MV) and high voltage (HV) levels nonetheless still represents an immense challenge in terms of reliability. To this end, this project proposes to develop a Reliability-Oriented Design (ROD) procedure for MV and HV power converters addressing reliability up-front in the design process. This will be done in three steps; first, the identification of critical system components; second, the assessment of reliability factors such as risk analysis, failure mode analysis, and fish bone diagrams; and third, the actual design, which is carried out by minimizing system complexity and stress, and by the use of the most reliable components, materials, structures, and converter configurations. Reliability models based on the latest release of MIL-HDBK-217F will be developed using existent knowledge and field data, and will be used to compare alternative modular MV and HV power converter configurations.

Isolated Converter with Integrated Passives And Low Material Stress

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency-Energy, Agile Delivery of Electrical Power Technology)
Research collaborators: University of Florida, University of Texas - Dallas
(September 1, 2010- November 30, 2013)

This project will develop a monolithic power converter to be used in efficient power adapters for mobile applications, such as netbooks. The chip converter will include the integration of a transformer, ultra-high-density capacitors, and a nano-magnetic material dispensable with high precision by low-cost inkjet printing. The magnetic structure, with a 3X improvement in energy storage, is introduced to keep the transformer volume at a minimum. The resulting highly efficient (>90%) converters with high power density will reduce the 15 terawatt- hours of energy consumed by notebooks and netbooks annually.

Dual Bi-Directional Silicon LGBTS Modules Enables Breakthrough PV Inverter Using Current-Modulation Topology

Sponsored by: ARPA-E, SunShot Program
Sub -Awardee of: Ideal Power
(January 1, 2012- January 29, 2015)

Ideal Power Converters is developing light-weight electronics to connect photovoltaic solar panels to the grid. Their technology explores innovative circuits using revolutionary transistor designs to develop solar panel electronics for commercial-scale buildings that are compact enough to be installed on walls or roof-tops. The project goal is to reduce the weight of these electronics by 98%, reducing the cost of materials, manufacturing, shipping and installation, and supporting the aggressive cost reduction goals of the Department of Energy's SunShot Initiative. Virginia Tech's role will be the development of a mechanically balanced dual chip module using proprietary wave joints to enable low inductances, low strain and passive heat extraction via two-sided cooling.

High-Temperature Packaging of Planar Power Modules by Low-Temperature Sintering of Nanoscale Silver Paste

Sponsored by: NBE Technologies/DOE-SBIR
(August 12, 2009 -August 31, 2013)

In present electric vehicles (PHEV/HEV/EV), an extra cooling loop is needed to lower the power-electronics coolant temperature below about 65° C from the radiator coolant temperature of 105° C. One way to reduce the cost of future EVs is to eliminate the extra cooling loop by developing reliable high-temperature power inverter modules that are sufficiently cooled by the radiator coolant. This calls for the development of power packaging technologies that can enable silicon and/or SiC power devices working at junction temperature in excess of 175°C. In the current phase of our power packaging research effort, we have focused on replacing the solder-reflow technique for die-attaching power chips by an emerging low-temperature joining technology (LTJT) which involves low-temperature sintering of silver powders. To reduce the process complexity of the conventional LTJT arising from the need of high pressure (30 to 40 MPa or 300 to 400 Kg-force per cm2, a nanosilver paste material was used to lower the dieattach temperature below 270°C with zero or less than 5 MPa pressure. This simplified LTJT is less likely to damage the chips and allows us to implement a planar packaging scheme for interconnecting both sides of the power devices without using wire bonds.

The planar power modules have low parasitic inductances thus less ringing noises from the device-switching action and can be cooled from both sides of the devices for improved thermal management. The electrical performance of the planar power module was tested and the results show that it can work properly under 175° C junction temperature.

Constant-Flux Magnetics for Power Conversion

Sponsored by: National Science Foundation
(November 15, 2012 – October 31, 2015)

At least 30% of the volume in commercial inductors store no or negligible energy. The "constant-flux" concept improves energy density by filling the available volume with as much magnetic (core) materials as practically feasible, then dispersing the windings to shape the distribution of magnetic flux, e.g., to distribute magnetic flux uniformly.

In this project, guiding principles will be developed from the structural and field standpoints to realize the constant-flux concept. Performance metrics, such as inductances, capacitances, and quality factor will be modeled, quantified, and compared with the corresponding benchmarks.

Linear Actuator with Permanent Magnets

Sponsored by: GE Appliances and Light (GEAL)
(October 1, 2012 – March 31, 2014)

In this project, CPES will work to improve the design procedure and performance of GEAL's Linear Actuator with Permanent Magnets (LAPM) by determining the proper materials to use, validating flux models, predicting force vs. position, and making an improved LAPM design to meet a cost function.

MHz Power Amplifier – Proof of Feasibility

Sponsored by: Halliburton Energy Sources, Inc.
(October 23, 2013 – October 24, 2014)

This project supports the development of a power amplifier for an inductive load. The amplifier is to employ simple, efficient, and reliable circuit topology. A boost output and a buck front end have been selected to achieve soft switching and envelope control. The amplifier is controlled to shape the amplitude and phase of the current in load to follow prescribed window functions. Silicon carbide switches are used to enable operation at high frequency and high temperature.

PowERazor: an Innovative Electronic Packaging Technique for Manufacturing High-Reliability Power Electronic Modules

Sponsored by: NBE/NSF SBIR Phase I
(October 1, 2013 – May 31, 2014)

This project was to demonstrate the feasibility of an innovative packaging technology or PowERazor for manufacturing a high-reliability, low-profile, double-side cooled power electronics module. A robust workflow was developed for successful and repeatable fabrication of power module packages. Basic electrical parameters were characterized for feedback throughout the manufacturing process. Electrical test beds were constructed to ascertain power module package quality using device self-heating. Thermal test beds were established to aid in quantifying the thermal management benefits of additional top side (double side) cooling. Reliability testing schemes were established and test beds were constructed for testing. Long term active and passive cycling schemes have been initiated.

MHz GaN Converter with Isolation

Sponsored by: Texas Instruments

This project starts with the design of the converter for zero-voltage switching over the full range of input voltage and output power to establish component requirements. Magnetic design of leakage inductance and harmonic losses in the coupled inductors with different winding structures are analyzed by finite-element simulation. The design of gate drive, loss analysis, effect of layout impedance, and other issues are addressed, leading to hardware verification with efficiency exceeding 85% at 5 MHz and 30 W output.

High-Density Integrated Inductor

Sponsored by: Texas Instruments

The "constant-flux" concept proposed recently is leveraged to distribute magnetic flux to improve energy density, lowering the profile of an inductor. The optimal flux distribution is identified mathematically, and verified by simulation. It is then applied to reduce the dc resistance of a commercial inductor by a factor of two, keeping the outer dimensions and inductance the same. Thermal-limited current rating is improved by 50%, whereas saturation-limited current rating is improved by 20% thanks to the suppression of flux crowding.

Design of Gapped Inductor under DC Bias

Sponsored by: Texas Instruments

Ferrite inductor with air gap is widely used because of low core loss and high inductance under dc bias. Conventional inductance formula for a gapped ferrite core assumes uniform or negligibly high permeability. When the core is designed to operate near saturation (to maximize core utilization) at rated current, such assumption is invalid owing to the appearance of regions with low, non-uniform permeabilities. Finite-element simulation uncovers a peak in the plot of inductance versus gap length that shifts with bias current, and that is not predicted by the conventional inductance formula. A reluctance model is formulated to explain the nonlinear behavior, and is verified experimentally.

New Projects approved and starting in the coming months:

Strategies for Wide-Bandgap, Inexpensive Transistors for Controlling High Efficiency Systems (Switches)

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency Energy, Agile Delivery of Electrical Power Technology)
Sub – Awardee of: HRL

High Power Solid State Circuits

Sponsored by: Office of Naval Research
Sub – Awardee of: ABB

Next Generation Power Electronics Manufacturing Innovation Institute (NGPEMII)

Sponsored by: Department of Energy
Sub – Awardee of: North Carolina State University

INTELLECTUAL PROPERTY

U.S. Patents Awarded

10.095
Multi-Channel Constant Current Source and Illumination Source
Shu Ji, Haoran Wu, Fred C. Lee
U.S. PATENT: 8,598,807
Issued: 12/03/13

10.094
Digital Hybrid V_2 Control for Buck Converters
Kuang-Yao (Brian) Cheng, Feng Yu, Paolo Mattavelli, Fred C. Lee
U.S. PATENT: 8,575,911
Issued: 11/05/13

10.003
Electrical Power System with High-Density Pulse-Width-Modulated (PWM) Rectifier
Ruxi Wang, Fred Wang, Dushan Boroyevich, Rolando Burgos, Kaushik Rajashekara
U.S. PATENT: US 8,570,774
Issued: 10/29/13

05.052
Method of Manufacture of a Variable Inductance Inductor (Divisional)
Michele H. Lim, J. Daan van Wyk
U.S. PATENT: 8,549,731
Issued: 10/8/2013

Invention Disclosures

14-097
2/24/2014
Two-Stage LED Driver with Multi-Channel Constant Current CLL Resonant Converter
Xuebing Chen, Daocheng Huang, Qiang Li, Fred C. Lee

14-091
2/10/2014
Coupled Inductor in Interleaved Multiphase Three-Level DC-DC Converters for High Power Applications
Sizhao Lu, Mingkai Mu, Yang Jiao, Fred C. Lee

14-075
1/6/2014
Magnetic Geometry with Programmed Field Distribution
Khai Ngo, Han Cui

14-066
11/18/2013
Hybrid Interleaving Structure with adaptive PLL Loop for Constant On-Time Switching Converter
Pei-Hsin Liu, Fred C. Lee, Qiang Li

14-065
11/18/2013
Avoiding Internal Switching Loss in Cascode Structure Device under Soft-Switching Condition
Xiucheng Huang, Weijing Du, Qiang Li, Fred C. Lee

14-053
10/16/2013
Switching-Cycle Control For The Modular Multi-Level Converter
Jun Wang, Rolando Burgos, Dushan Boroyevich, Bo Wen

13-171
6/27/2013
State-Trajectory Control of LLC Converter Implemented by Microcontroller
Chao Fei, Qiang Li, Fred C. Lee

13-170
6/27/2013
Fully Integrated SR Controller with Auto-Tuning Function for High-Frequency LLC Resonant Converters
Xin Ming, Fred C. Lee, Qiang Li

13-169
6/14/2013
High-Frequency Integrated Point-of-Load (POL) Module with PCB Embedded Inductor Substrate
Yipeng Su, Qiang Li, Fred C. Lee, Wenli Zhang

13-168
6/14/2013
Magnetic Loss Measurement Method with Partial Cancellation Concept
Dongbin Hou, Mingkai Mu, Fred C. Lee, Qiang Li

13-167
6/13/2013
System and Method for Impedance Measurement Using Chirp Signal Injection
Zhiyu Shen, Marko Jaksic, Paolo Mattavelli, Dushan Boroyevich, Jacob Verhulst, Mohamed Belkhayat

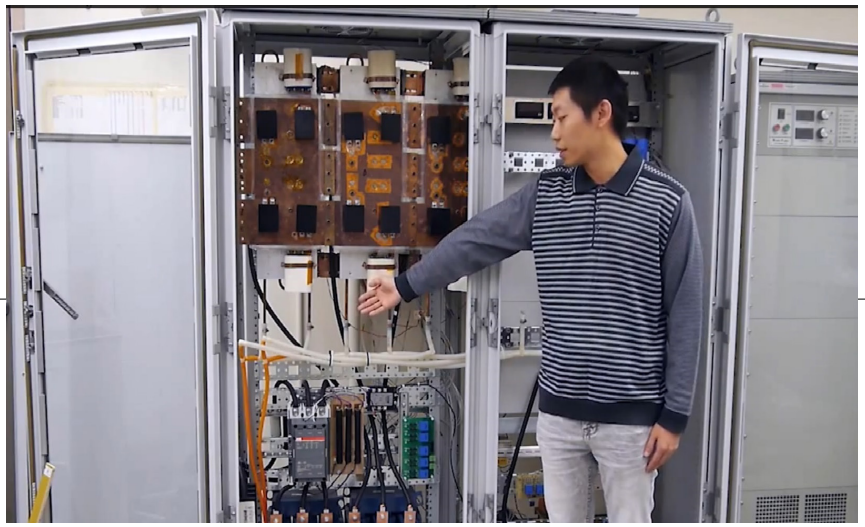
13-166
6/13/2013
System and Method for Impedance Measurement Using Series and Shunt Injection
Zhiyu Shen, Marko Jaksic, Paolo Mattavelli, Dushan Boroyevich, Jacob Verhulst, Mohamed Belkhayat

13-164
6/12/2013
System and Method for Self-compensating Time Constant Mismatch of Inductor DCR Current Sensing
Pei-Hsin Liu, Fred C. Lee, Qiang Li, Xin Ming

VIRGINIA TECH FACILITIES

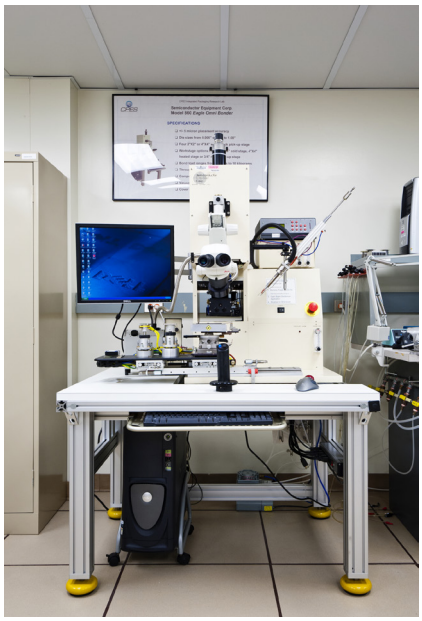
Introduction

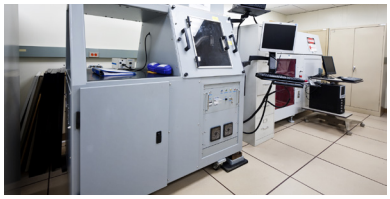
The Center headquarters is located at Virginia Tech, occupying office and lab facilities encompassing more than 19,000 sq ft of space in one building. Research space at CPES-VT includes an electrical research lab, an integrated packaging lab and computer lab. In addition to the headquarters labs and offices, a research library and a large conference room with voice and video conferencing capabilities supporting remote site course instruction as well as interaction among CPES collaborators is maintained. Interactive collaboration is routinely facilitated through conference calls, WebEx online conferencing, student and faculty exchanges, and face-to-face research project review meetings.



Electrical Research Laboratory

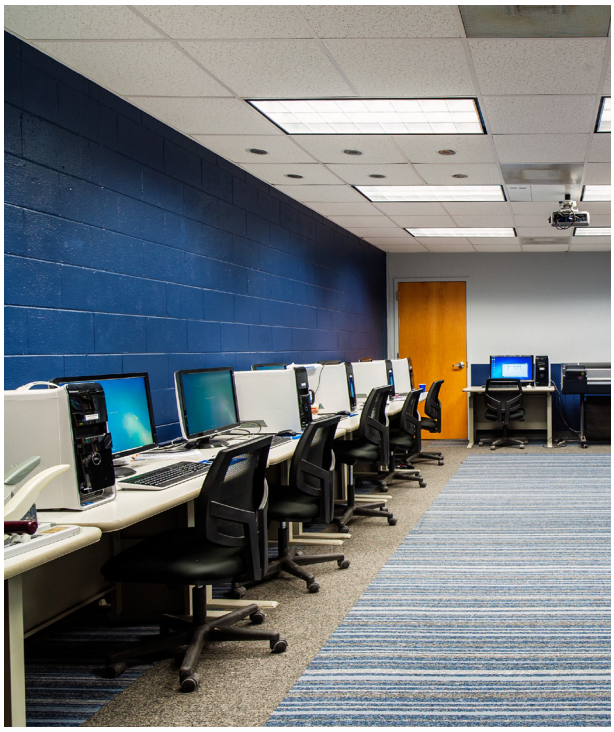
The electrical research laboratory is equipped with state-of-the-art power testing equipment, dynamometers, prototype PWB manufacturing equipment, an EMI chamber, a clean room, a mechanical shop. The Power Electronics Research Lab is equipped with state-of-the-art tools and instrumentation necessary for development of power electronic circuits and systems of all sizes from sub-volts, sub-watts to 6 kV, 1 MW. Each student bench is equipped with Dell Studio XPS computers with an i7 core processor and multiple GBs of RAM for running simulations. Standard instrumentation is comprised of GHz oscilloscopes, multi-channel function generators, electronic loads, network, spectrum, impedance, logic and power analyzers, thermal sensors and AC/DC bench supplies of all sizes. Specialized test room equipment includes: thermal imaging equipment, thermal cycling chambers, Hi-Pot tester, 3-D magnetic field scanner, EMI/EMC analyzer, large and small dynamometers, automatic circuit board routing equipment, programmable and variable loads, and liquid cooled heat-exchanger.





Integrated Packaging Lab

The Integrated Packaging (IP) Lab supports all CPES students, faculties, visiting scholars, and sponsors for their advanced needs in power electronics packaging research. The lab is established to create and evaluate alternative approaches to the design and manufacture of Integrated Power Electronics Modules (IPEMs) and provide the state-of-the-art electronic manufacturing and assembly equipment. The IP lab itself has installed a sealed ceiling and HEPA filtration to create over 1,600 square feet of class 10,000 clean room space, and the addition of a dark room for photolithography processing. It has the capability to produce FR4, DBC, and thick film hybrid substrates, perform metallization using RF sputtering thin film deposition and electro/electro-less plating, and develop substrate patterns by virtue of laser ablation machining, chemical metal etching, and screen printing. The IP lab also has the ability to mount bare dies and SMT components using high precision pick-n-place machine, solder reflow belt furnace, and convection reflow oven. The advanced vacuum solder reflow system provides another technical solution for die-attachment in a flux-less, void-less process. The wire bonding machines equipped in the IP lab provide interconnect options of heavy aluminum wire bonding, gold wire ball bonding, and aluminum/gold ribbon bonding for manufacturing IPEMs. For accurate and controlled dispensing of adhesives and encapuslants an automated precision dispensing system and a spin coater have been added in the lab. In addition, the IP lab has the full capability for low temperature co-fired ceramic (LTCC) processing from tape cutting, via drilling, screen printing, laminating, to co-firing. The Component- and module-level test and evaluation of electrical, thermal, and reliability performance for the assembled IPEMs are also available in the IP lab. Low and high power curve tracers, impedance analyzers, and precision multimeters can be used for electrical property measurements. Thermal performance evaluation can be made by the setup of thermocouples, optic-fiber sensors, IR imaging, and thermal diffusivity test system. Reliability analysis is performed using multi-purpose bond tester on as-made modules and the ones after certain numbers of temperature/humidity cycling. An array of cross-sectioning and grinding/polishing equipment has been used to better understand the microstructure of electronic packaging materials.



Library and Computer Lab

The Computer Lab supports all major software used in power electronics analysis and design including: SPICE, Saber, I-DEAS, Math Products – Matlab and Mathcad, Ansoft Products- Maxwell 2-D and 3-D finite-element analyzers, ePhysics, and Q3D, Mentor Graphics and Cadence circuit simulation software, SIMPLIS, PLECS, FLOTHERM circuit thermal analyzer software, and Inventor Professional.

High Power Lab

High power, high voltage power conversion technologies are attracting increasing attention in academia as well as industry in response to a need for more emerging power electronics applications, including alternative energy and power conversion such as wind power generations, fuel cells, hybrid electric vehicles and all-electric ships. Enabled by a 2002 award of $839,337 from the Defense University Research Instrumentation Program (DURIP) paired with CPES cost sharing of more than $250K for renovations, the electrical research lab area at VT has been renovated and upfit to accommodate medium voltage, megawatts power capability. The facility has two medium voltage 1 MVA reconfigurable transformers, corresponding reactors, capacitors, switchgears, and controllers. A 1 MW Innovation Series medium voltage IGBT drive donated by GE is installed as a programmable load. The complete set-up is capable of testing power converters in various active and reactive operation modes continuously at 1 MVA, 4160 V level. The unique installation distinguishes VT as one of a few select universities in the nation with this capability and enhances its position as a leader in power electronics research well beyond the NSF ERC life expectancy.

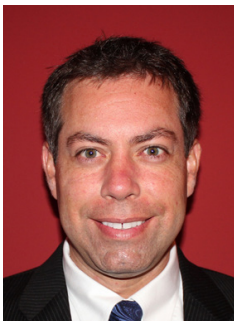
PEOPLE

FACULTY


Fred C. Lee


Dushan Boroyevich


Khai Ngo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Qiang Li

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Guo-Quan Lu

ADJUNCT FACULTY


Paolo Mattavelli

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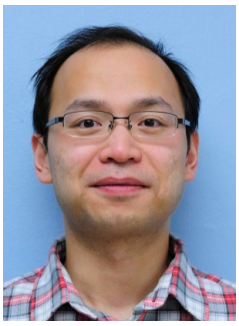
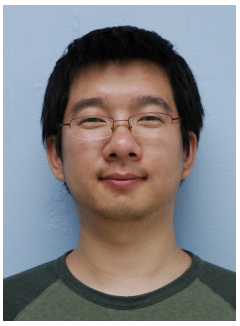
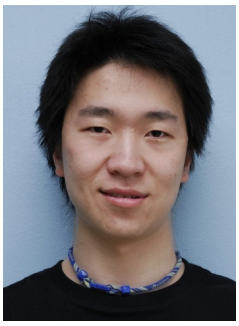
Wenli Zhang

RESEARCH SCIENTIST


Fang Luo


Mingkai Mu


Zhiyu Shen


Xuning Zhang

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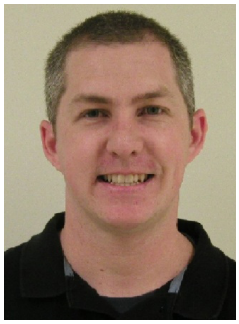
Igor Cvetkovic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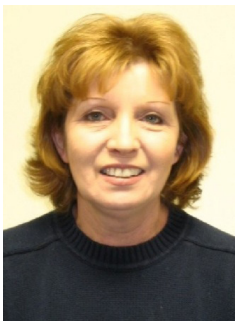
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Alonso, Marcos


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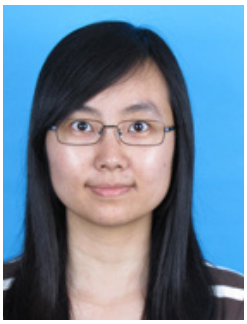
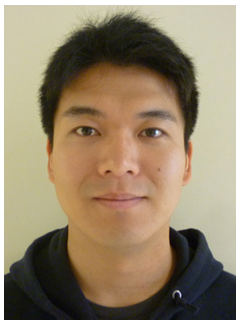

Du, Weijing


Farr, Ewan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Kanamoto, Kyozo

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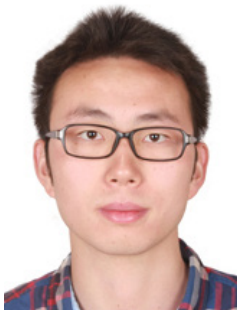
Konjedic, Tine

Leong, Kennith



Li, Kai

Lu, Sizhao

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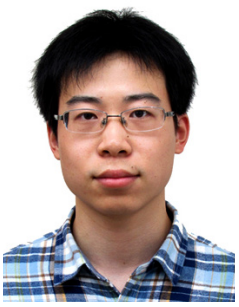
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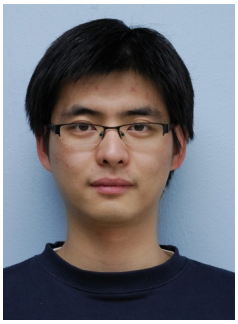
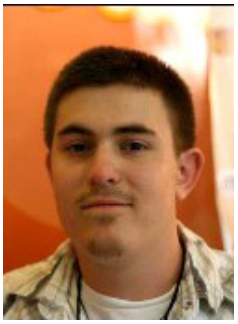
Chen, Xuebing


Chen, Zheng (Henry)


Cui, Han

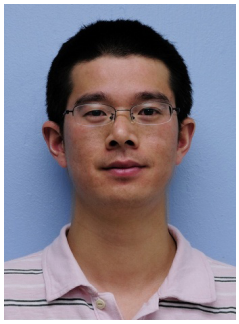

Cvetkovic, Igor


Dahlin, Nicholas


Danilovic, Milisav


DiMarino, Christina


Fei, Chao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Hou, Dongbin


Huang, Daocheng

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Jiao, Yang


Khatib, Mudassar


Kim, Woochan


Li, Bin


Li, Chen


Li, Chi


Li, Virginia

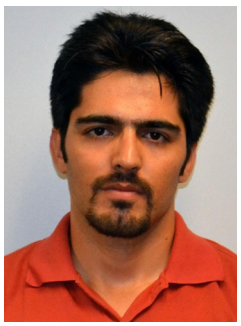

Liu, Pei-Hsin


Liu, Tao


Liu, Zhengyang


Lu, Ming


Mao, Yincan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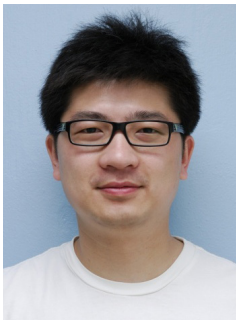
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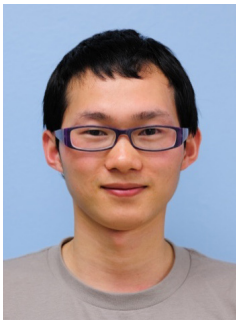
Sun, Bingyao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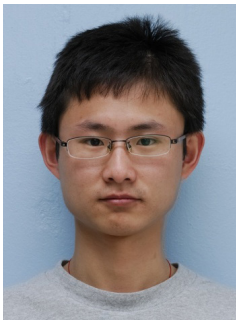
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Xue, Lingxiao


Yan, Yasmine


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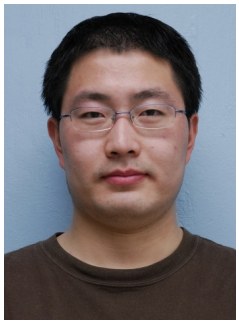
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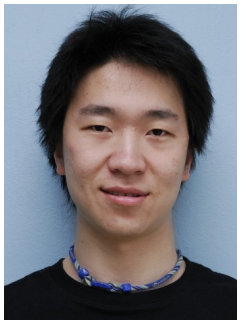
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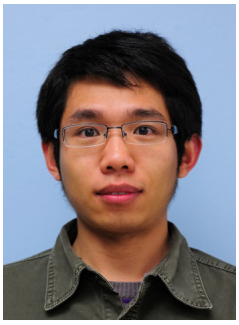
Zhang, Zhemin (Jimmy)


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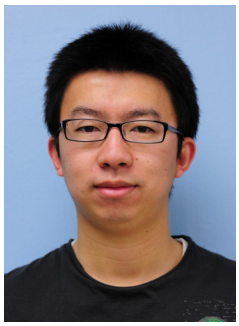
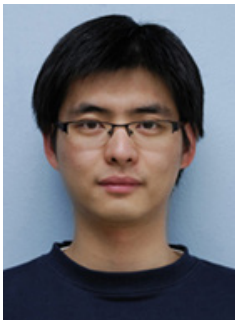

Zheng, Hanguang (Jason)

PEOPLE

GRADUATES


Bishnoi, Hemant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Bo Wen, Rolando Burgos, Xuning Zhang, Qiong Wang, Paolo Mattavelli, Dushan Boroyevich
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P. Acuna, I. Moran, Marco Rivera, Juan Dixon, Rolando Burgos
IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society, November 10-13, 2013, Vienna, Austria, pp. 8508-8513.

Theses & Dissertations

D-q Impedance Identification in Three Phase Systems Using Multi-Tone Perturbation
Bo Zhou
Thesis, January 30, 2013

Packaging of a High Power Density Point of Load Converter
David Joel Gilham
Thesis, March 8, 2013

State-Trajectory Analysis and Control of LLC Resonant Converters
Weiyi Feng
Dissertation, March 29, 2013

Constant-Flux Inductor with Enclosed-Winding Geometry for Improved Energy Density
Han (Helen) Cui
Thesis, June 28, 2013

Behavioral EMI Models of Switched Power Converters
Hemant Bishnoi
Dissertation, September 24, 2013

Electrical Integration of SiC Power Devices for High-Power-Density Applications
Zheng (Henry) Chen
Dissertation, September 26, 2013

Electrical and Thermal Characterizations of IGBT Module with Pressure-Free Large-Area Sintered Joints
Li Jiang
Thesis, September 26, 2013

Investigation of Topology and Integration for Multi-Element Resonant Converters
Daocheng Huang
Dissertation, December 6, 2013

Passive Component Weight Reduction for Three Phase Power Converters
Xuning Zhang
Dissertation, December 11, 2013

A 150 W/in^3 GaN Based ZVS Boost Converter for PFC Application in Hybrid Electric Vehicle
Kumar Gandharva
Thesis, December 17, 2013

Power Management Consortium Nuggets

New Core Loss Measurement Method with Partial Cancellation Concept

Planar Inductor Structure with Variable Flux Distribution – A Benefit or Impediment?

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High Frequency High Efficiency GaN Based Interleaved CRM Bi-directional Buck/Boost Converter with Coupled Inductor

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Evaluation of High-Voltage Cascode GaN HEMT in Different Packages

High-Frequency High Power Density 3-D Integrated Gallium-Nitride-Based Point of Load Module Design

High Frequency, High Density Point-of-Load (POL) Module with PCB Embedded Coupled Inductor Substrate for VR Application.

Characterization of Low Temperature Sintered Ferrite Laminates for High Frequency Point-of-Load Converters

Unified Equivalent Circuit Model of V^2 Control

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Modeling and Autotuning of AVP Control with Inductor DCR Current Sensing

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Comparison of Small Signal Characteristics in Current Mode Control Schemes for Point-of-Load Buck Converter Applications

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Analysis of Unified Output MPPT Control in Sub-Panel PV Converter System

State-trajectory Control of LLC Converter Implemented by Microcontroller

Distributed MPPT Method for Smart Converter PV System

Transient Performance Improvement for Constant On-time Control

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New Core Loss Measurement Method with Partial Cancellation Concept

In the existing core loss measurement method, the measurement accuracy is sensitive to the value of the cancellation component (either capacitor or inductor). Therefore, it is required to design and fine-tune the cancellation component for each testing sample at each testing condition (frequency, flux density, temperature, etc.). This is a very time-consuming process and makes the standardization of the measurement instrument almost impossible.

To overcome this drawback, a new measurement method with partial cancellation concept is proposed. The equivalent circuit is shown in Fig. 1. The capacitive cancellation version can be used for sinusoidal excitation only, and the inductive cancellation version can be used for arbitrary excitation. Taking the inductive cancellation version as an example, the core loss can be calculated by

$$P_{core} = \int v_2 \cdot \frac{v_R}{R_{ref}} - \frac{1}{k} \int v_L \cdot \frac{v_R}{R_{ref}}$$

where k is named as *cancellation factor*, which represents the percentage of cancelled reactive voltage to the total reactive voltage, and can be found by adding a phase perturbation into with the de-skew function of oscilloscope.

The core loss of iron powder material -52 from Micrometals, Inc. is measured at 0.5MHz, 10mT peak flux density under rectangular excitation with different duty cycle. The measurement result is shown in Fig. 2. It can be seen that using the proposed method, the accurate result can be acquired with different cancellation inductance value .

In summary, the proposed method enables an accurate measurement at high frequency without the fine-tuning of the cancellation component value, and is applicable to arbitrary wave excitation.

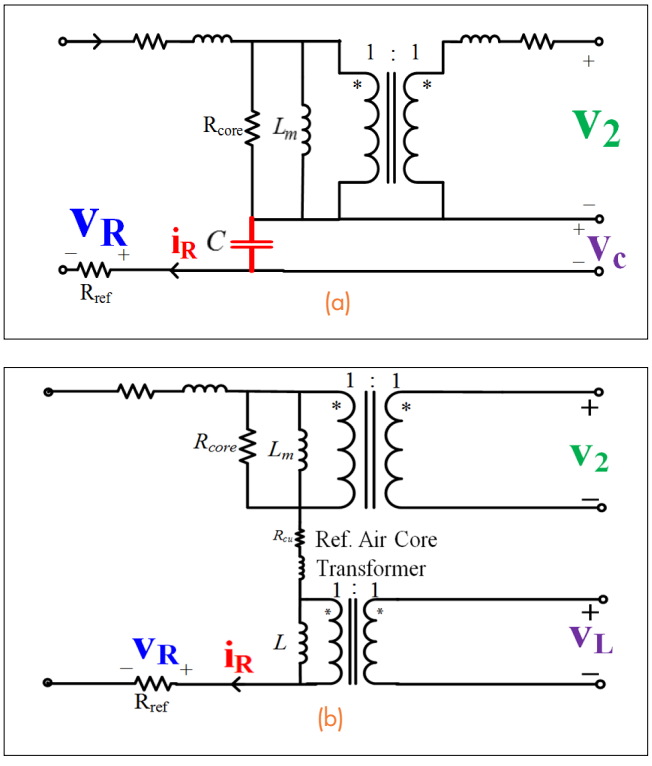


Figure 1. Equivalent circuit of proposed method: (a) capacitive cancellation and (b) inductive cancellation.

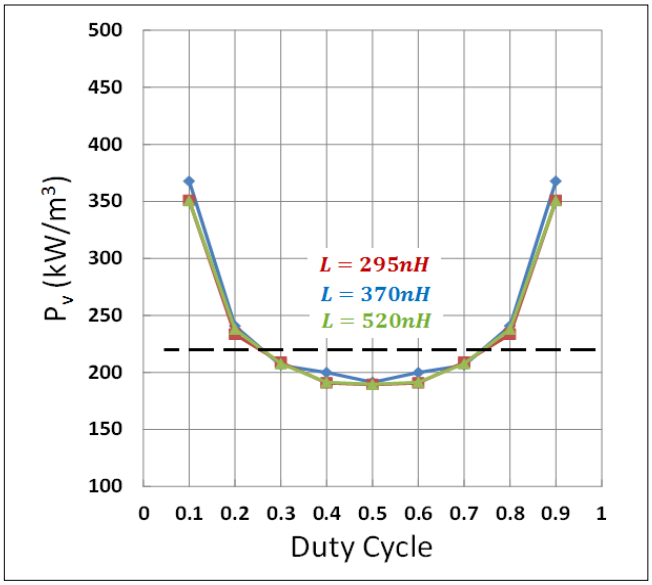


Figure 2. Summary of measurement result of -52 material (from Micrometals Inc.) for rectangular excitation with different duty cycle using proposed method. The dashed line indicates the result for sinusoidal excitation.

Planar Inductor Structure with Variable Flux Distribution – A Benefit or Impediment?

The lateral flux inductor structure has been widely used as the substrate in CPES high-current 3D integrated POL modules. Both an ultra-low profile and high power density can be achieved simultaneously with this structure. For our purposes, we can simplify and approximate the single-turn structure as two side-by-side circular disc cores.

Fig. 1 shows the top view of the DC flux distribution of the disc core with 20A DC current, from which it can be seen the disc core is excited in a large DC bias range. The inner core is almost saturated while the outer core is still running at a relatively low bias point. Because of the saturation, the permeability of the inner core is decreased to a very low value. Therefore, the AC flux avoids the inner core, where the magnetic reluctance is large. Fig. 2 illustrates the AC flux distribution of the disc core with 20A DC bias current and 6A peak-to-peak AC current ripple. It can be seen that the AC flux is automatically pushed to the outer core.

Due to the DC and AC flux counterbalance mechanism, the core loss density of the inner saturated core is limited. The peak Pv point is neither the maximum DC nor AC flux points.The operating points of the disc core are extended into saturated region, where there is better core utilization. The AC flux and core loss (i.e. the area of the minor loop of the BH curve shown in Fig. 4) is automatically reduced. The saturation is no longer detrimental in this special structure.

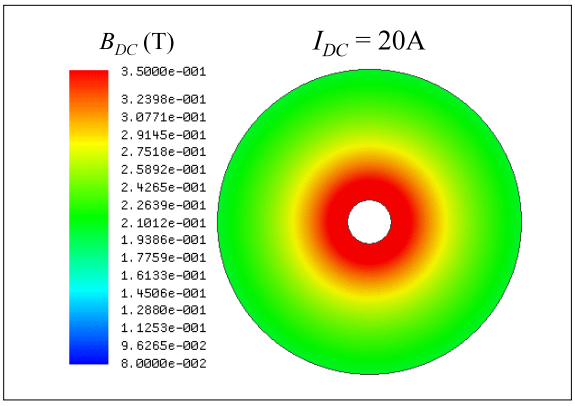


Fig. 1. DC flux distribution of planar disc core

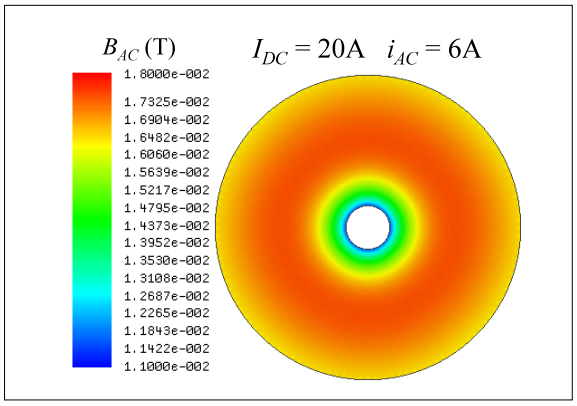


Fig. 2. AC flux distribution of planar disc core

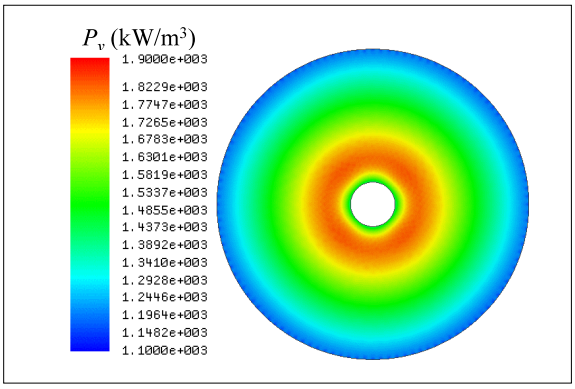


Fig. 3 Core loss density distribution of disc core

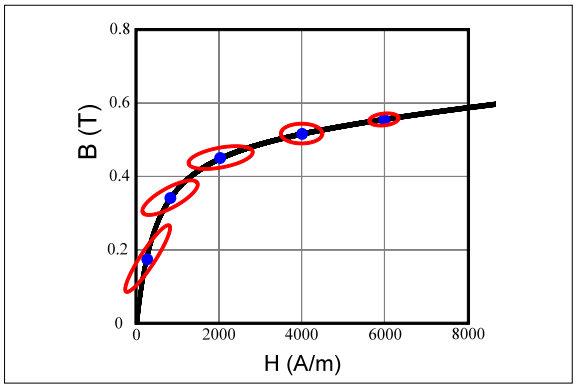


Fig. 4 Multiple operating points of the disc core

GaN-Based MHz Interleaved CRM PFC Converter

The critical conduction mode (CRM) boost power factor correction (PFC) converter is widely used in off-line power supplies due to its merits of zero-current switching (ZCS) turn-off of the diode and zero-voltage switching (ZVS), or valley switching, turn-on of the main switch. By interleaving two CRM boost PFC converters, the ripple of the input and output currents and the size of the input differential mode (DM) electromagnetic interference (EMI) filter can be reduced significantly, while the power rating can be extended to a higher level. Furthermore, a phase-shedding strategy can be used to improve the light-load efficiency.

With the advent of the 600V gallium nitride (GaN) high-electron-mobility transistor (HEMT), the converter's switching frequency can be pushed to several MHz. This is a dramatic improvement compared to the high-frequency capability of a silicon (Si) based power semiconductor devices. Previous research has demonstrated that the switching loss is the dominant loss in MHz frequency hard-switching conditions, and soft-switching is still critical to achieving high efficiency for the high-voltage GaN HEMT.

Combining the merits of the CRM PFC converter and the high-voltage GaN HEMT, a 1.2kW 1-3MHz GaN-based dual-phase interleaved CRM boost PFC converter is demonstrated to have 97.3% full-load efficiency and 120W/in$_3$ power density. By pushing the frequency above 1 MHz, the benefit for EMI filter design is significant. As the required corner frequency of the EMI filter reaches hundreds of kHz, dramatic size and weight reduction can be projected. Finally, the CRM boost PFC has the limitation that the rectifier conduction loss and non-ZVS switching loss are dominant, especially in the MHz frequency range. The totem-pole bridgeless PFC converter is a promising solution to further improve efficiency by full-line ZVS extension strategy.

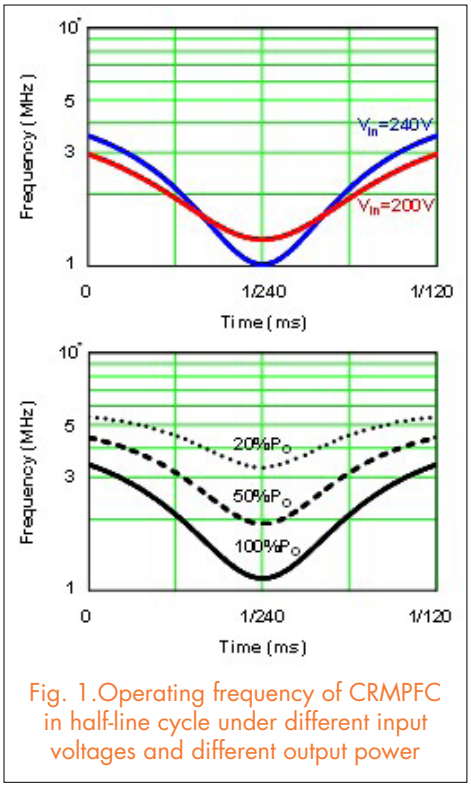


Fig. 1.Operating frequency of CRMPFC in half-line cycle under different input voltages and different output power

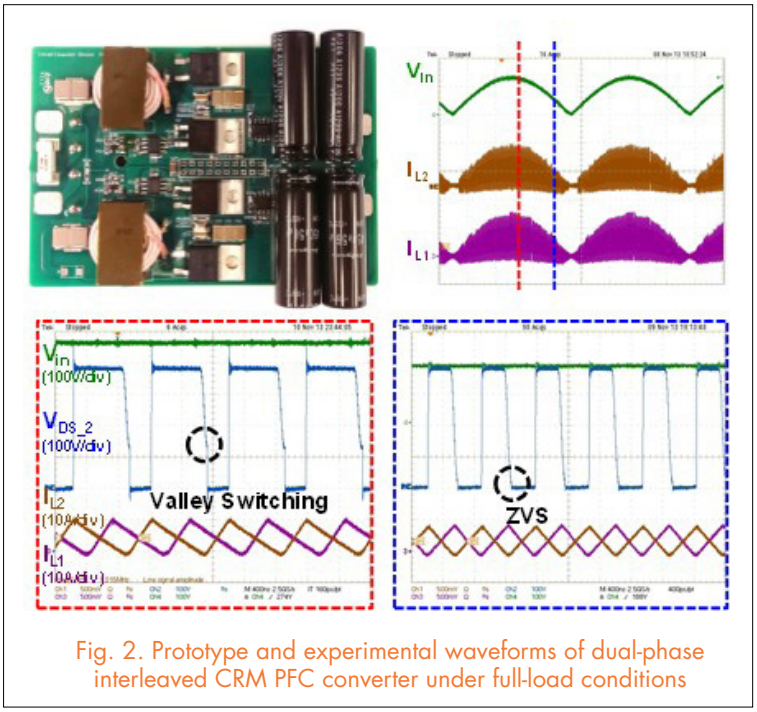


Fig. 2. Prototype and experimental waveforms of dual-phase interleaved CRM PFC converter under full-load conditions

High-Frequency, High-Efficiency GaN Based Interleaved CRM Bi-directional Buck/Boost Converter with Coupled Inductor

The bidirectional buck/boost converter is widely used in power electronics systems due to its simplicity and high efficiency. Some applications include on-board charger/dischargers for plug-in hybrid electric vehicles, and interfaced converters for energy storage in a dc-based nanogrid. Conventional silicon-based bidirectional buck/boost converters are usually intended to be operated in discontinuous current mode (DCM) in order to alleviate reverse-recovery issues and to be able to use a small inductor. However, the DCM operation greatly increases the turn-off loss because the main switch is turned off at least twice during the load current. As a result, the switching frequency can barely be pushed to the hundreds of kilohertz due to power loss.

In recent years, the GaN HEMT has emerged as a promising device for high-frequency, high-efficiency, and high-density power conversion due to its better figure of merit than comparable Si and SiC transistors. The switching frequency has been continuously pushed up to several MHz to both reduce passive component size and increase power density. Previous research concludes that the turn-on switching loss is dominant due to the reverse-recovery charge or the junction capacitor charge of the free-wheeling device under hard-switching conditions. On the other hand, the turn-off loss is negligible because of the intrinsic current-source driving mechanism in the cascode structure. These important switching characteristics indicate that zero-voltage-switching (ZVS) is still desired for GaN devices in high-frequency applications, while the turn-off current is no longer a big concern for cascode GaN devices.

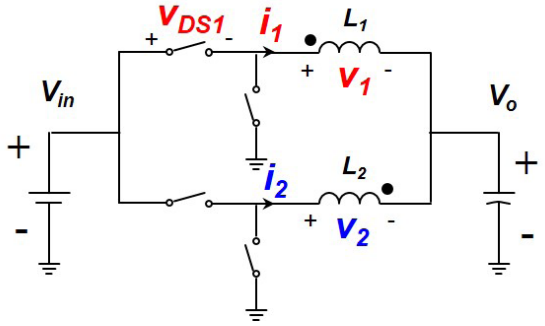


Fig. 1. Buck/boost converter with coupled inductor

The critical current mode (CRM) operation is the most simple and effective way to achieve ZVS and is widely used in medium-low power applications. Conventional CRM operation has some limitations in high frequencies and requires further improvement. The concept of a coupled inductor has been applied successfully in the interleaved voltage regulator modules to improve efficiency and transient response. A two-phase buck/boost converter with a coupled inductor is shown in Fig. 1, and the converter's key waveforms are shown in Fig. 2. The resonant period in CRM operation is less with the coupled inductor than with the non-coupled condition, which is beneficial for high-frequency operation. The soft-switching range and the circulating energy are both improved with the coupled inductor in CRM. The coupled inductor prototype efficiency is 98.5% at 1MHz, which is 0.5% higher than the efficiency of the non-coupled converter.

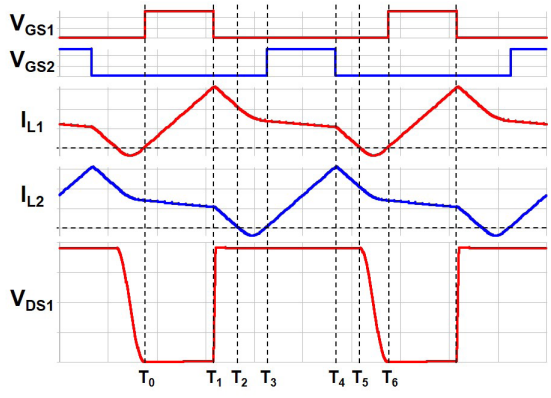


Fig. 2. Key waveforms

Avoiding Si MOSFET Avalanche in Cascode Device and Achieving Zero-Voltage-Switching for Cascode Device

High-performance active devices have consistently proven to be the first force to increase power density and meet the requirement of modern systems. Silicon (Si) devices have dominated power management since the late 1950s. However, after several decades of optimization and development in the production process, the Si device has approached its theoretical limits, and material properties have become the limiting factor. Based on the rapid development of research in recent years, high-voltage normally-on wide-band-gap devices have been proven to have better performance compared to the Si MOSFET. With high electron mobility, high breakdown voltage, low on-resistance, low input capacitance, and high thermal conductivity, the wide-band-gap device is more suitable for high-frequency, high-efficiency, and high-power-density applications.

The cascode structure shown in Fig. 1 is used to make the terminal a normally-off device. The Si MOSFET controls the on/off state of high-voltage normally-on devices. The interaction and parasitic capacitance of the two devices plays an important role in achieving high efficiency, especially under soft-switching conditions. The two devices should be well matched. Otherwise, the Si MOSFET may have an avalanche breakdown during the turn-off process. Although the avalanche voltage of Si protects the high-voltage normally-on device from the damage of over-voltage, avalanche is not recommended operation for the Si MOSFET, and it is a potential risk to the reliability of the device. The energy dissipated through the avalanche path brings additional loss. Moreover, the avalanche of an Si MOSFET will break the charge balance of the parasitic capacitors of the MOSFET and the high-voltage normally-on device, which will cause the device to lose its zero-voltage turn-on condition internally during the soft-switching turn-on process. This is undesirable, especially in applications that operates at MHz frequency.

After analyzing the voltage distribution process of the cascode device in detail, and quantifying the conditions under which Si will reach avalanche and the avalanche loss, we have devised a simple and effective solution which is paralleling an external capacitor with drain-source of Si MOSFET to compensate the junction capacitors charge mismatch and thus avoid Si reaching avalanche. This solution also achieves zero-voltage-switching for high-voltage, normally-on devices.

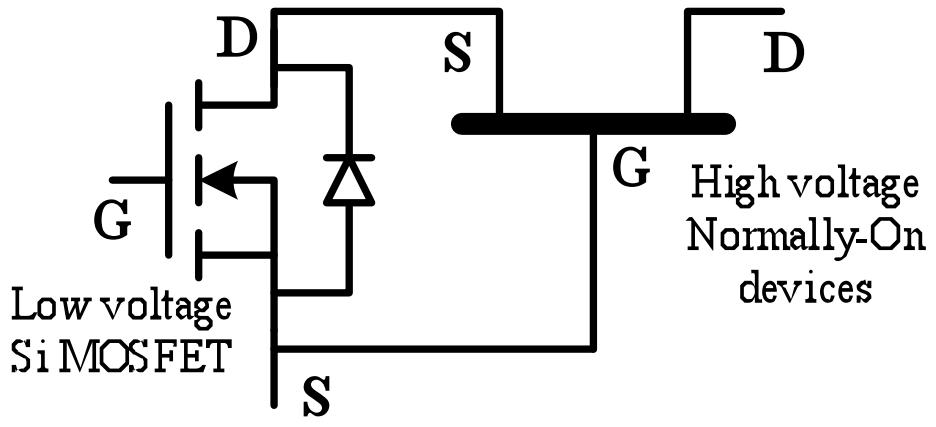


Fig. 1. Cascode structure for normally-on devices

Evaluation of High-Voltage Cascode GaN HEMT in Different Packages

Advanced power semiconductor devices have consistently proven to be a major force in pushing the progressive development of power conversion technology. The emerging gallium-nitride-based power semiconductor device is considered a promising candidate to achieve high-frequency, high-efficiency, and high-power-density power conversion because it has a faster switching speed and lower switching-related loss than previous devices. Accompanied by the fast switching speed, inevitably there is high dv/dt and di/dt introduced at the same time, which can barely be observed in the comparatively slow Si MOSFET. As a result, package design is critical to enabling the promising high performance of GaN devices.

The limitations of the traditional packaging for high-voltage cascode GaN HEMT includes significant turn-on loss during hard-switching turn-on, and significant internal parasitic ringing in hard-switching turn-off due to the impact of common-source inductors.

In order to improve the package design, we propose a stack-die package, with all common-source inductors eliminated. According to previously developed loss models, the stack-die package is predicted to have significant improvement compared to traditional packages. Experiments with a prototype of this stack-die package that was fabricated in the lab show that around 30% of the turn-on energy is reduced during hard-switching turn-on, and the internal parasitic ringing is almost eliminated in hard-switching turn-off.

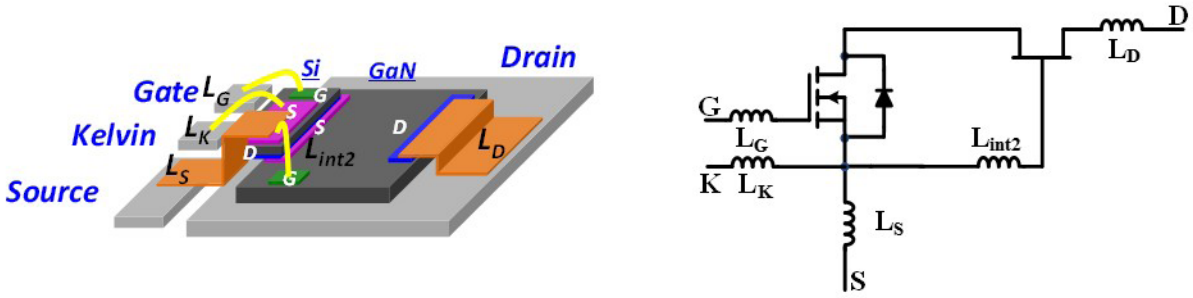


Fig. 1. Bonding diagram and schematic for cascode GaN HEMT in stack-die package

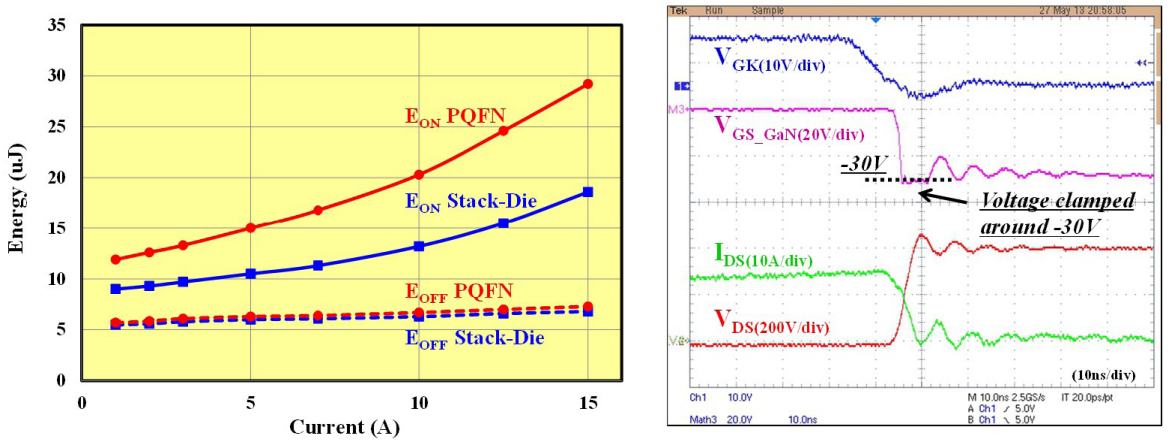


Fig. 2. Package impact in hard-switching turn-on and hard-switching turn-off

High-Frequency High Power Density 3-D Integrated Gallium-Nitride-Based Point-of-Load Module Design

We have created a design for a high-frequency, high-power-density 3-D integrated GaN-based POL module, and explore the enhancement mode and depletion mode GaN devices and their characteristics. The impact of parasitics on switching loss has been quantified by exploring the contributions of the common-source and high-frequency loop inductance on switching loss. With the reduced parasitic inductances introduced by the GaN device packaging, the design of the module becomes the major barrier to higher efficiencies and frequencies. Reduction of the high-frequency power loop can offer significant inductance improvements and provide a smaller design footprint. As power density is increased in the module, the thermal design becomes a critical aspect to consider, and is often the bottleneck in power handling capability. We use high-thermal conductive alumina DBC substrates to improve thermal performance with better heat distribution. The impact of switching from a traditional multilayer PCB to a two-layer DBC has major implications on the module design to achieve good electrical performance, and the impact of the shield plane on electrical performance has been considered. The proper shield plane design has been implemented on the DBC module.

The final demonstrations show that single-phase and two-phase modules can operate at up to 5 MHz. These modules can achieve three to five times the power density of the commercial modules, but with similar efficiency. Fig. 2 shows the power density map of the current products and research for similar applications.

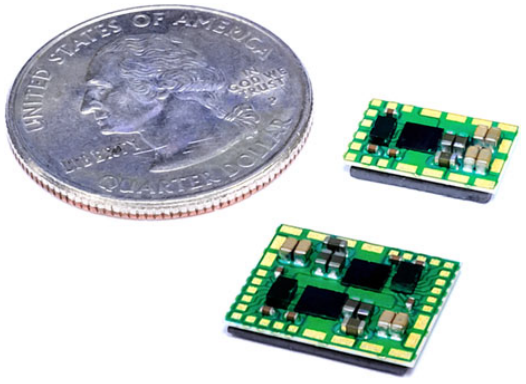


Fig. 1. Alumina design for single- and two-phase IR GaN modules

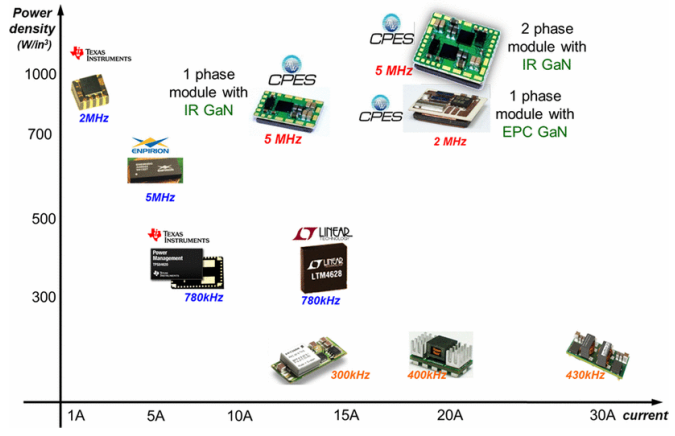


Fig. 2. Power density map of current high-density power modules

High Frequenty, High Density Point-of-Load (POL) Module with PCV Embedded Coupled Inductor Substrate for VR Application

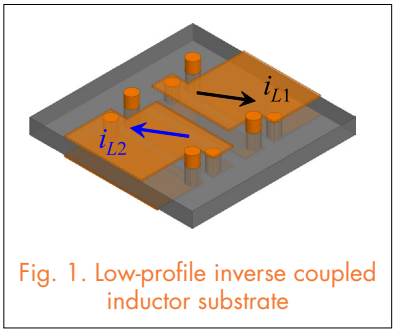
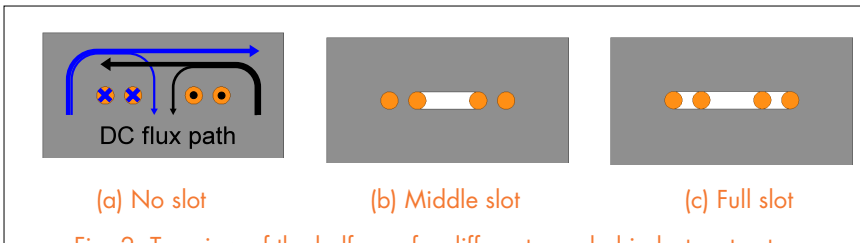


Fig. 1. Low-profile inverse coupled inductor substrate

The power density of the 3D integrated POL module can be improved by using two-phase inverse coupled inductors, as shown in Fig. 1. For this kind of coupled inductor, the steady-state inductance L_{ss} is very nonlinear, which means the value of L_{ss} increases greatly from heavy load to light load. The nonlinear $L_{ss}$is beneficial for light-load efficiency improvement. However, the nonlinearity of transient inductance L_{tr} is more prominent than that of L_{ss}, because the coupling becomes weaker at light load, as illustrated in Fig. 5. The huge Ltr at light load cause a severe under-shoot voltage spike during the load step-up transient. From the DC flux path shown in Fig. 2(a), it can be seen that the DC bias leakage flux path (i.e. the core between two windings) is sensitive to the load, as is the reluctance of the leakage flux path. This is the key reason that the coupling has a large variation when the load is changed. By adding an air slot into the leakage flux path, its reluctance becomes insensitive to the load, and the coupling can be maintained. The non-linearity of L_{ss} and L_{tr} also can be freely controlled by using a differently shaped slot. The middle slot exhibits moderate nonlinearity, while the full slot structure has almost linear inductance. The large voltage spike during the transient has been solved due to the significant reduction of the light-load L_{tr} value.



(a) No slot (b) Middle slot (c) Full slot

Fig. 2. Top view of the half-core for different coupled inductor structures

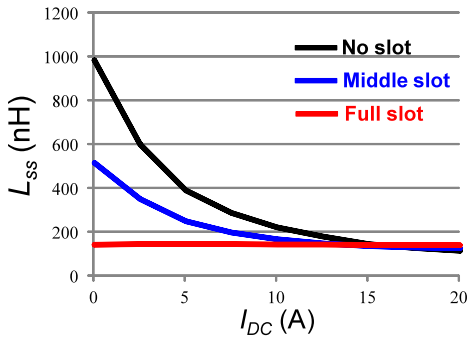


Fig. 3. L_{ss} for different coupled inductor structures

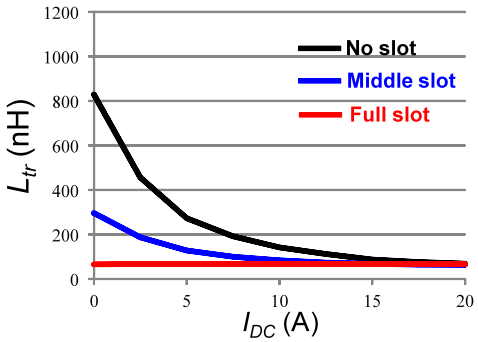


Fig. 4. L_{tr} for different coupled inductor structures

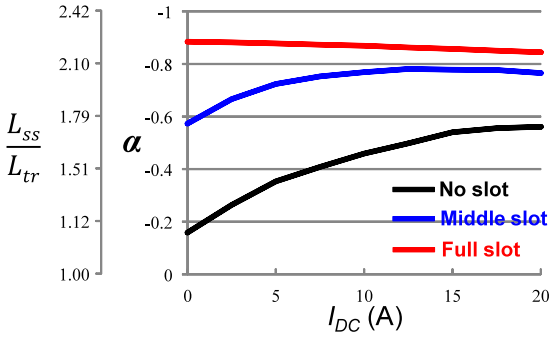


Fig. 5. Coupling coefficient, ration between L_{ss} and L_{tr} for different coupled inductor structures

Characterization of Low-Temperature Sintered Ferrite Laminates for High-Frequency Point-of-Load (POL) Converters

Low-profile magnetic components and their associated integration techniques are desirable for the design and fabrication of highly integrated point-of-load (POL) converters working at high frequencies. The multilayer low-fire ferrite inductors can be fabricated as the magnetic substrate in an integrated POL converter with the active components on top. The permeability and core loss density under high DC bias are of special interest, and were characterized on different low-fire ferrite laminates. The microstructures and chemical compositions of sintered multilayer ferrites were investigated in order to understand the difference in the magnetic properties among those samples.

Low-fire magnetic tapes ESL 40010, 40011, and 40012 are all Ni-Cu-Zn-based ferrite materials. Bi2O3 was added as a sintering aid to reduce the sintering temperature of the Ni-Cu-Zn ferrites to below 900° C. The analysis of permeability and core loss density under DC bias has been carried out to properly choose the low-fired ferrite materials for different applications. The ESL 40011 and 40012 tapes are good choices for transformers and low-frequency, low-current inductor applications because of their higher permeability at low DC current levels. The ESL 40010 tape, exhibiting higher permeability and lower core loss density under a high DC bias, is most suitable among the three commercially available low-fire ferrite tapes for high-frequency, high-current POL converter applications.

In this study, the mixed laminates 40010/40011, 40010/40012, and 40011/40012 in alternating layers in a 1:1 ratio were co-fired at 885° C under a prolonged sintering profile. All the resulting laminates illustrate uniform microstructures and homogeneous chemical compositions through elemental inter-diffusion and the assistance of the redistribution of Bi2O3-rich liquid during sintering. Compared to the 40010 material, higher permeability and lower core loss density are obtained in a mixed 40010/40012 laminate, where the DC bias is in the range of 0 to 4000 A/m.

The 40010/40012 ferrite laminate has been used for inductor fabrication and integrated into a POL module achieving high efficiency of 81% at 5 MHz. The developed low-profile ferrite inductors demonstrate a unique method for hybrid power electronics integration and realize a size reduction for high-frequency POL converters. Further investigation of these materials and associated techniques could potentially enable a system-in-package approach for power electronics applications.

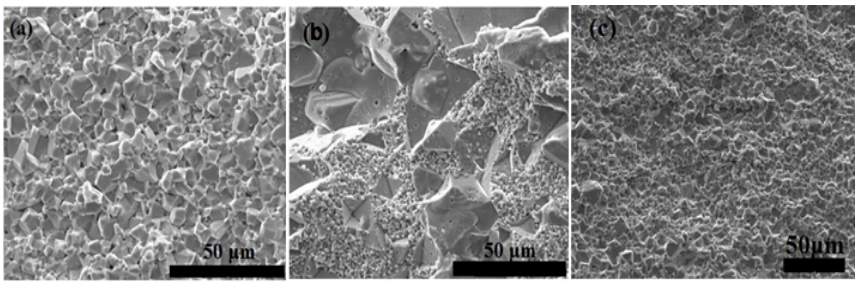


Fig. 1. SEM micrographs of ferrite samples (a) 40010, (b) 40012, and (C) mixed laminates 40010/40011 sintered at 885°C for 3

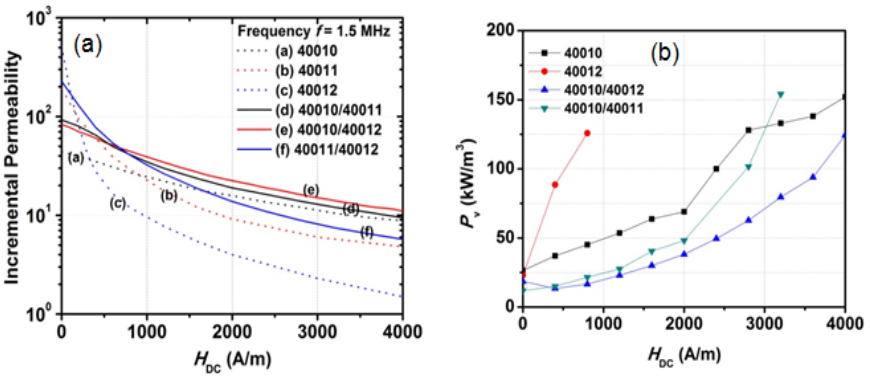


Fig.2. Variation of (a) permeability and (b) core loss density under DC bias for low-fire ferrite tapes and their mixed laminates

Unified Equivalent Circuit Model of V² Control

This nugget proposes a unified equivalent circuit model of V² control. The direct output voltage feedback in V² control contains inductor current, capacitor voltage and load current information, which can be separated into 3 feedback loops, as shown in Fig.1(a) (use constant on-time as an example). Fig.1(b) shows that for constant on time structure, the inductor current feedback turns the circuit into a controlled current source while the capacitor voltage feedback turns this controlled current source into a controlled voltage source, which will be realized by a current source in parallel with a resistor. Moreover, due to the sideband frequency in the capacitor voltage feedback, the voltage source is a non-ideal source, with the non-idealness shown by a R_{e2}-L_{e2} branch in Fig. 1(b), which forms a double pole at half of the switching frequency by resonating with the output capacitor. The damping of the double pole, which is shown as R_{damp} in Fig.1 (b), is related with the capacitor parameters and can be positive or negative. This explains why this structure is elegant when large ESR capacitors are employed (such as OSCON caps) while sub-harmonic oscillation occurs when low ESR capacitors are employed (such as ceramic caps). Fig. 2 shows a complete equivalent circuit model of V² control, which is applicable to all kinds of V² control. Generally speaking, the inductor current loop turns the circuit into a non-ideal current source, with the non-idealness shown by the R_e-C_e branch, which will form a double pole by resonating with the power state inductor. The capacitor voltage loop turns the non-ideal current source into a non-ideal voltage source, with the non-idealness shown by the R_{e2}-L_{e2} branch, which will form a double pole by resonating with power stage capacitor. The parameters of R_e, C_e, R_{e2} and L_{e2} are different between different modulation schemes. This equivalent circuit model can be used to examine all the transfer functions (control-to-output, output impedance, input impedance and audio susceptibility) and can be extended very easily to a multi-phase structure and V² control with a current ramp case.

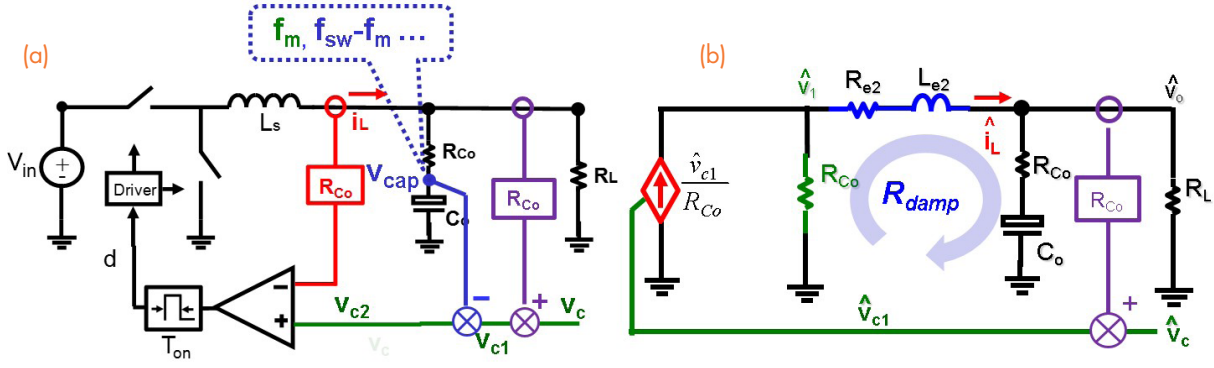


Fig. 1. V² Control with separated three feedback loop (a) and equivalent Circuit Model for control-port

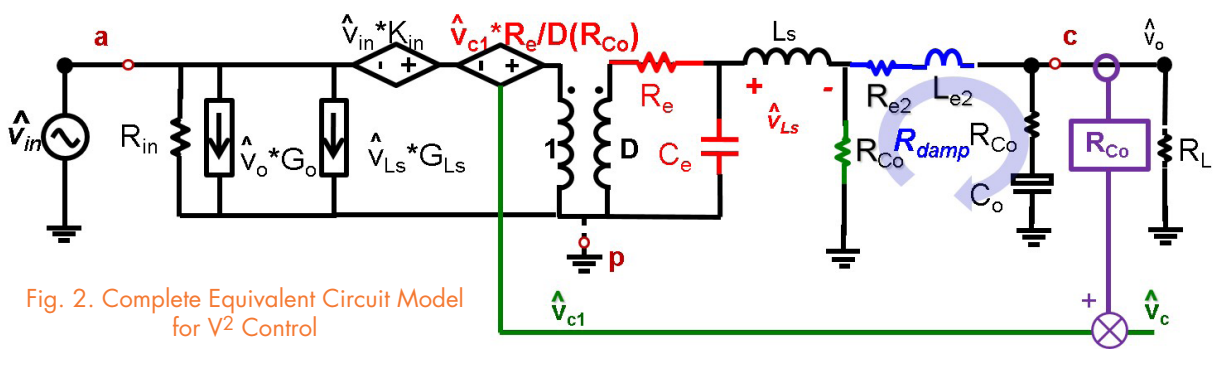


Fig. 2. Complete Equivalent Circuit Model for V² Control

Hybrid Interleaving Structure with Adaptive PLL Loop for Multiphase Constant On-time Switching Converter

Constant on-time control is widely used for better light-load efficiency, and faster transient response to save output capacitors. However, its nature of variable frequency control causes wide variation in switching frequency (f_{sw}) under input voltage (V_{in}) and/or output voltage (V_o) changes, which makes interleaving difficult. Phase manager and Phase Lock Loop (PLL) are two common solutions. The former is simpler, but is noise-sensitive by ripple cancellation effect and is unable to synchronize PWM signals among phases during transient. The latter is less noise-sensitive and allows overlapping PWM signals, but requires a PLL loop per phase. Also, the PLL loop has a stability issue, when the bandwidth (T_p) is designed too high or too low.

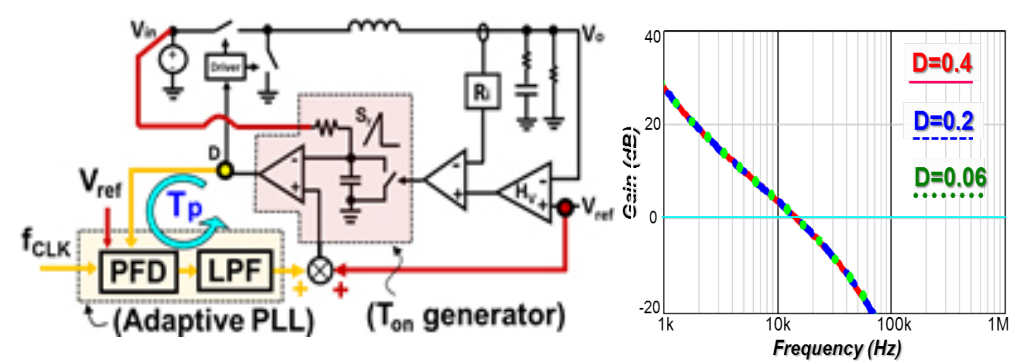


Fig. 1. Adaptive PLL loop (a) Block diagram, (b) Simulated T_p Loop gain

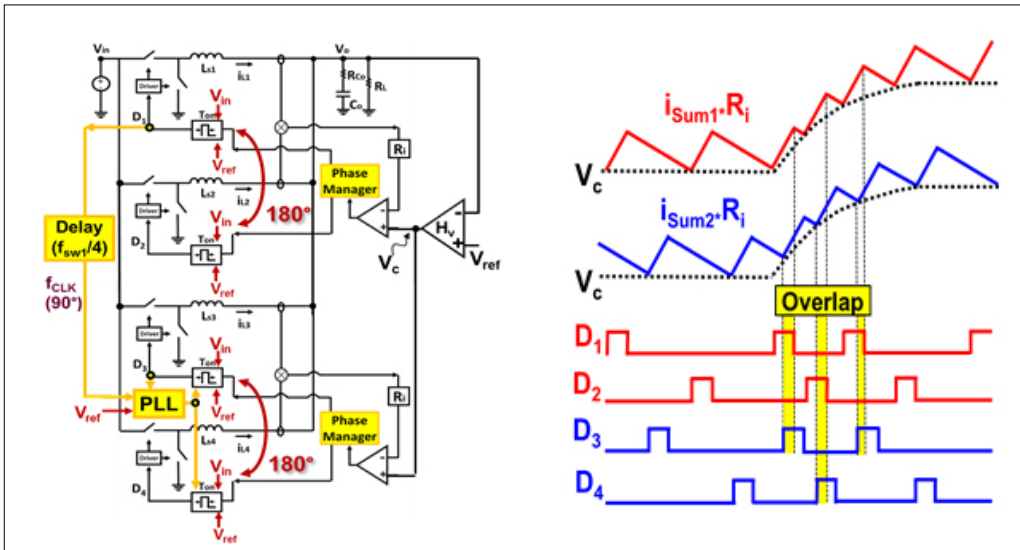


Fig. 2. 4-phase hybrid interleaving (a) Block diagram, (b) transient response

This paper first provides an accurate small-signal model to understand the dynamics of the PLL loop, and gives design guidelines for the Low Pass Filter (LPF) of PLL to avoid the stability problem. Then, an adaptive PLL loop is proposed to maintain a constant T_p bandwidth over a wide duty cycle range. Thus, the PLL loop design becomes simple and has fast tracking to f_{clk} without interfering with constant on-time control loop. As shown in Fig. 1, a proposed adaptive PLL loop maintains a constant gain by using V_{in} and V_o feedforward at on-time generator, and V_o feedforward at Phase Frequency Detector (PFD) of PLL. Secondly, a novel hybrid interleaving structure is developed with a comparable noise immunity and transient response as the PLL method, while the number of PLL loops is greatly reduced. For a 4-phase operation as shown in Fig. 2, it contains two phase managers that maintain a 180° phase difference for each of the two phases, and only one PLL locks 90° difference between D_1 and D_3. 3 PLL loops are saved when compared with the PLL method. Fig. 3 shows PWM overlapping during transient naturally. Finally, the simulation result based on the state-of-art filter model of the laptop VR demonstrates the constant output impedance design for an AVP over a wide duty cycle range.

Pulse-width Locked Loop (PWLL) for Automatic Resonant Frequency Tracking in LLC DC–DC Transformer (LLC-DCX)

In recently developed distributed power architecture, the LLC resonant converter has been widely used as a dc–dc transformer (DCX) to provide a semi-regulated or unregulated bus voltage. In order to achieve the highest efficiency, we propose a novel switching frequency control scheme for the LLC-DCX. First, the synchronous rectifier (SR) gate-driving signals are tuned by eliminating the body diode conduction. Then, the pulse-width locked loop (PWLL) is presented. By minimizing the pulse-width difference between the main switch and the well-tuned SR gate-driving signals, the LLC-DCX always runs at the f0 point to achieve the highest efficiency. For rapid prototyping purposes, the PWLL used to track f0 is realized in a Cyclone III field programmable gate array.

The proposed control strategy for LLC resonant converters, including well-tuned SR latch digital control with PWLL frequency tracking, is shown in Fig. 1. The new control strategy is easy to implement using commercially available FPGAs. Furthermore, key experimental waveforms, which verify operation of the proposed solution, are given in Fig. 2.

By setting the well-tuned SR gate-driving signal as the control reference and using the PWLL to minimize the pulse-width difference between the SR and the main switch-driving signals, the resonant frequency is always tracked (fs= f0).

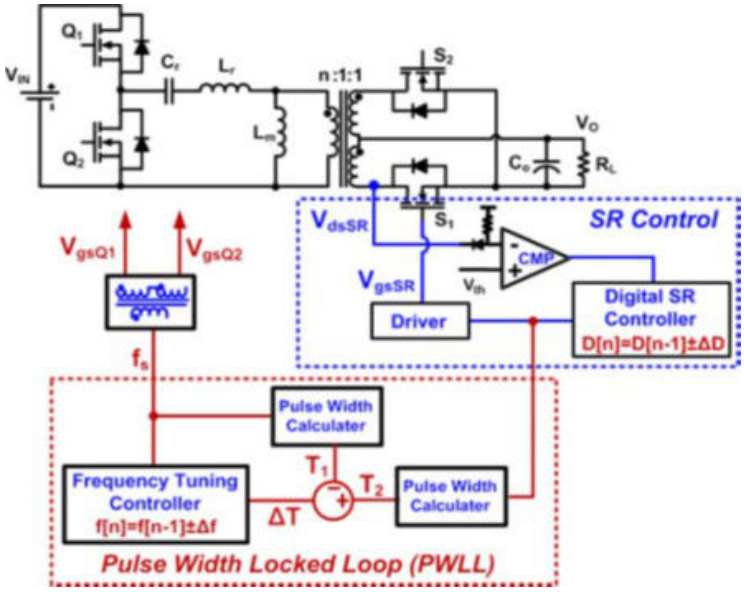


Fig. 1. Control blocks of the proposed universal adaptive SR driving scheme including frequency tracking

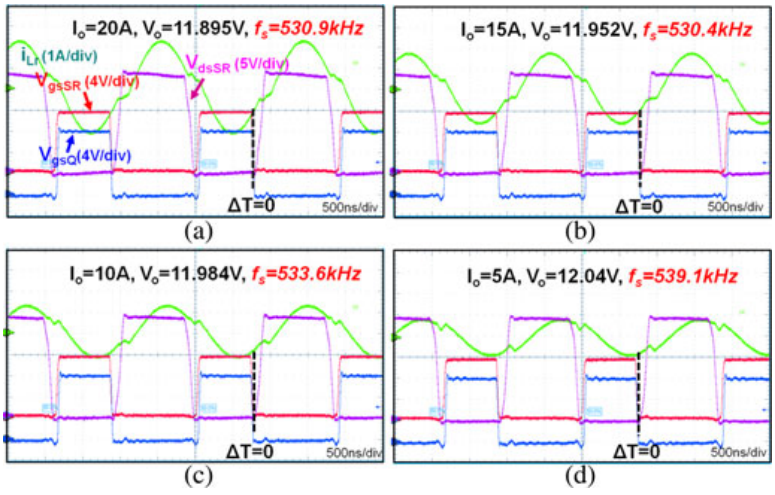


Fig. 2. Frequency tracking under different load conditions

Modeling and Autotuning of AVP Control with Inductor DCR Current Sensing

The inductor DCR sensing technique is widely used due to lossless sensing and simple implementation. However, mismatch between the time constant of the DCR sensor (τ_{Cs}) and the inductor (τ_{Ls}) increases the output voltage spike during load transient, but there is no analytical model to understand the dynamic. Although adding more output capacitors can avoid a transient spike, component cost and the area on motherboard also increase. The prior autotuning method solves the mismatch issue by adjusting -C_s close to -L_s such that the output capacitors can be reduced, but the implementation is too complex for monolithically integration.

This paper first presents a new equivalent circuit model to predict the small-signal characteristic of the current-mode control with DCR current sensing accurately. The model contains an $R_eL_sC_e$ resonant circuit and a current source to represent the mismatch effect at high frequency, while a R_sC_s low-pass filter loop represents the low-frequency effect. The model shows that the closed-loop output impedance (Z_{oc}) contains a pole-zero pair from the DCR sensor which makes Z_{oc} (move?) away from the desired load-line resistance (R_{LL}), so the transient response impairs.

Secondly, this paper develops a simple pole-zero compensation technique to maintain a constant output impedance and a fast transient under possible mismatch conditions, so the output capacitor can be minimized with a simpler autotuning circuit on the VR controller. The idea is adding a simple and easy-integrated compensator (H_{Com}) along the current feedback path to create an adjustable pole-zero pair to correct the output impedance close to R_{LL}.

$$Z_{oc} \approx (R_{LL}\frac{s\tau_{Ls}+1}{s\tau_{Cs}+1})H_{Com} = (R_{LL}\frac{s\tau_{Ls}+1}{s\tau_{Cs}+1})[\frac{s(A+1)RC+1}{sRC+1}] \approx R_{LL}$$

The proposed autotuning configuration in Fig. 2 contains Hcom with a high-pass filter (RC) and a variable gain amplifier (A), and a V_o slope detector. When a step-up load transient event is identified at V_i', H_{Com} is adjusted gradually based on sensed dV_o/dt, because Z_{oc} can be estimated by sensing dV_o/dt. When $Z_{oc}<R_{LL}$, the slow response makes $dV_o/dt<0$. When $Z_{oc}>R_{LL}$, $dV_o/dt>0$. The SIMPLIS simulation with the state-of-art output filter model of laptop VR and the experiment results on a commercial VR12 controller confirms the effectiveness of the proposed method.

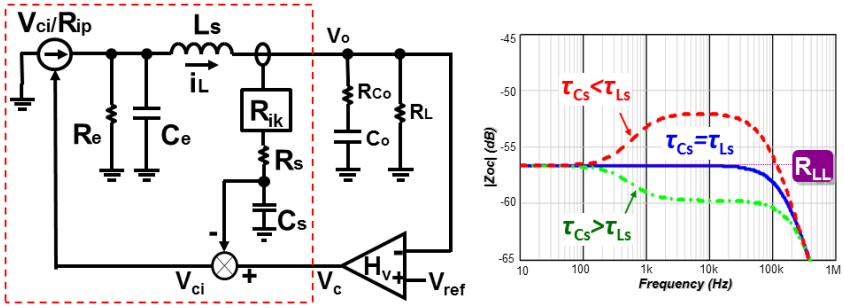


Fig. 1. Proposed Model (a) Block diagram, (b) Z_{oc} under mismatch

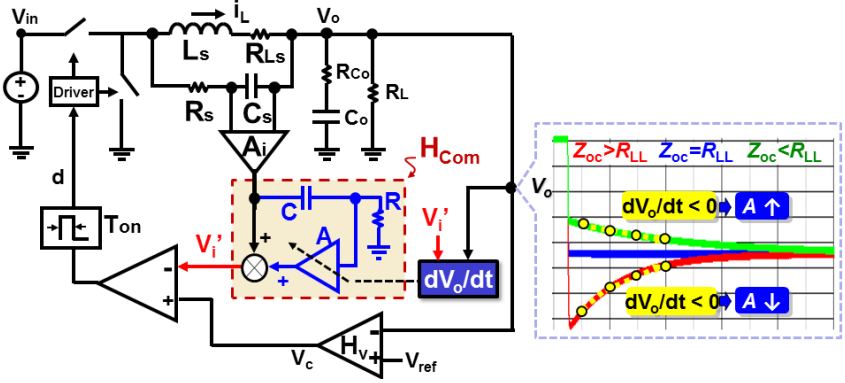


Fig. 2. Block diagram of proposed autotuning configuration

Equivalent Circuit Model and Design of Constant On-time Current Mode Control with External Ramp Compensation

This nugget proposes a three-terminal equivalent circuit model of Constant on-time current mode control with external ramp compensation. A multi-phase constant on-time current mode control based on pulse distribution structure is widely used in the Voltage Regulator application for a microprocessor. To minimize the ripple cancellation effect, an external ramp compensation is used in current solution as shown in Fig.1(a). However, an external ramp will introduce a dynamic to the system and the AVP requirement will be violated without considering the effect of the external ramp. For small D, The simplified control-to-output current transfer function with external ramp is shown as follows:

$$\frac{i_L(s)}{v_c(s)} \approx \frac{1}{R_i} \frac{1+\frac{T_{sw}}{2}s}{1+\left(\frac{s_e}{s_f}+\frac{1}{2}\right)T_{sw}s}$$

The external ramp will make the circuit behave as a non-ideal current source, as it will bring one moving pole, which is related to the magnitude of the external ramp, and one static zero, which is located at f_{sw}/π. The proposed equivalent circuit to represent this non-ideal current source is shown in Fig. 1(b). Where the R_{e2}-L_{e2} branch is utilized to resemble the non-idealness of this current source. R_{e2} and L_{e2} form a static zero while R_{e2}, L_{e2} and L_s form the moving pole. For a large duty cycle application, there is an additional double pole, which is shown by a R_e-C_e branch resonating with the power stage inductor. The three-terminal switch equivalent circuit model is shown in Fig. 2, where all the transfer functions (control-to-output, output impedance, input impedance and audio susceptibility) can be examined and extended very easily to multi-phase case. This equivalent circuit model is an extension of the original three-terminal current mode control by adding a R_{e2}-L_{e2} branch that resembles the effect of the external ramp in constant on time control.

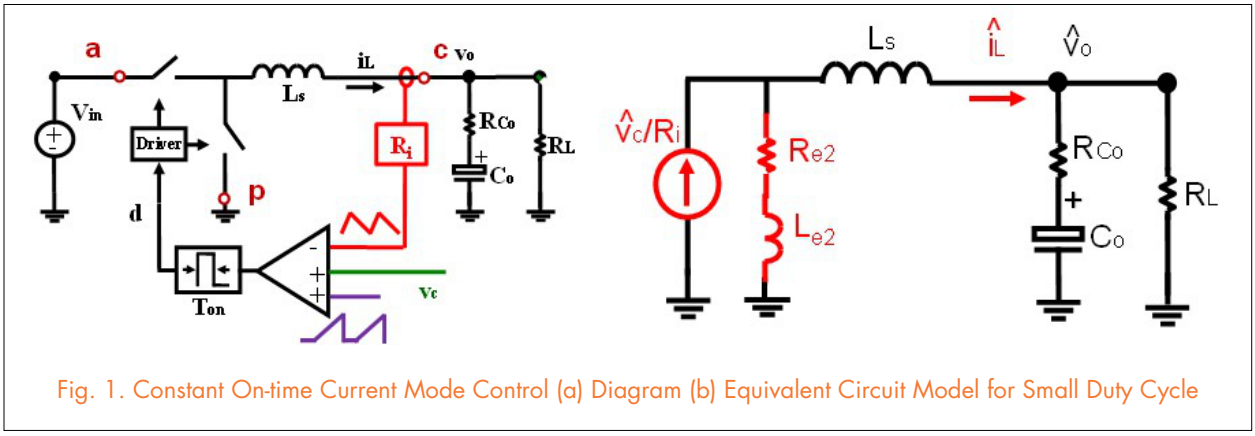


Fig. 1. Constant On-time Current Mode Control (a) Diagram (b) Equivalent Circuit Model for Small Duty Cycle

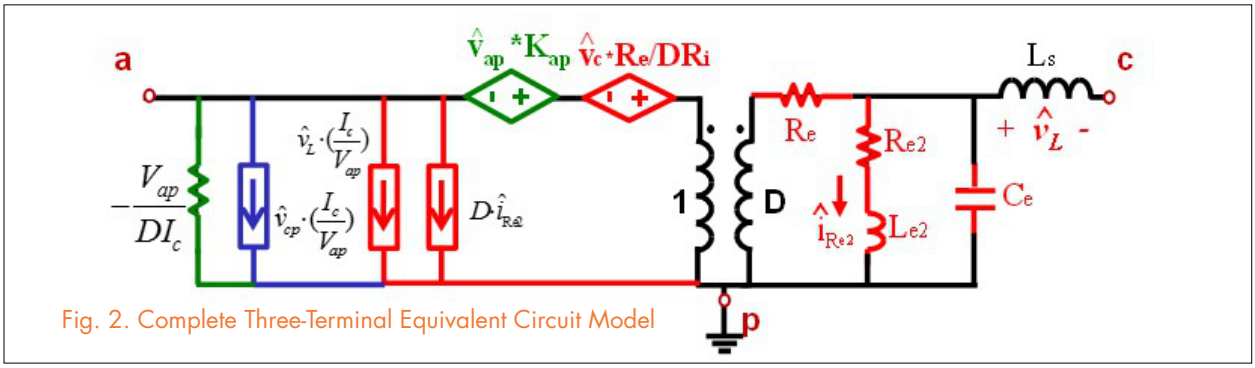


Fig. 2. Complete Three-Terminal Equivalent Circuit Model

V2 Control with Capacitor Current Ramp Compensation using Lossless Capacitor Current Sensing

V2 control is a popular control architecture in point-of-load buck converters due to its simplicity and fast transient response. Using V2 control with a ceramic capacitor is stable. We have reviewed the existing solutions and their limitations, and propose a solution that uses an output capacitor current ramp to stabilize the control loop. An analog capacitor current-sensing method based on impedance match is used in the implementation of lossless current sensing. A small-signal equivalent circuit is proposed for the analysis of the proposed control method. The proposed solution is superior to existing compensation methods because of its excellent transient response for a wide range of duty cycles. The effectiveness of the concept and implementation are verified by experimental results.

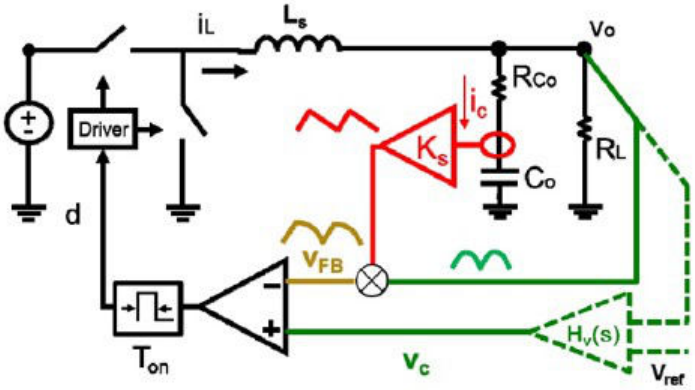
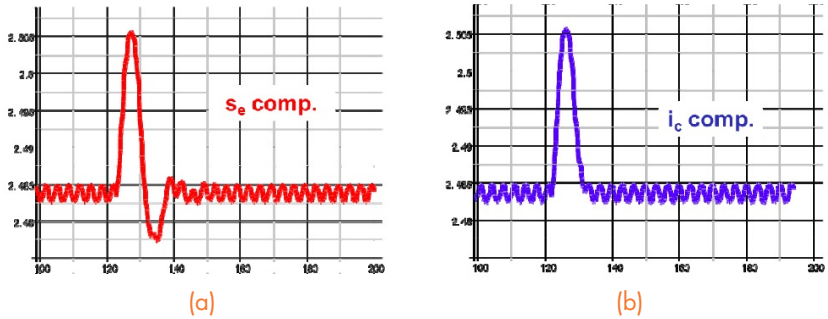


Fig. 1. Concept of V2 control with capacitor current ramp compensation



(a) (b)

Fig. 2. Output voltage waveforms (a) s_e compensation (b) i_c compensation

Fig. 1 shows the circuit schematic of the proposed control concept with capacitor current ramp compensation. Fig. 2. shows the input voltage transient response of this simulation circuit. As the gain of audio susceptibility is very low, the output voltage is tightly controlled, even without an outer loop.

V2 control is a popular control scheme in point-of-load buck converters and voltage regulators for microprocessors. V2 control using ceramic capacitors is unstable when the converter operates at hundreds of kHz. Moreover, jittering is a common concern in commercial products. Compensating the loop by an inductor current ramp increases the output impedance while compensating the loop by an external ramp, but cannot always achieve desirable damping. This research proposes capacitor current ramp compensation for V2 control, which can provide desirable damping to the loop while maintaining an ultra-fast load transient response. Meanwhile, the capacitor current ramp helps to reduce the jittering. The lossless sensing circuit is a simple R-C branch connected in parallel with output capacitors. When the R-C time constant of the sensing branch matches with the time constant of the output capacitor, the capacitor current is emulated by the voltage across the sensing resistor. The sensing scheme is very easy to implement in a control IC. The concept and implementation are applicable to V2 control with different PWM modulation schemes, including constant on-time V2, constant off-time V2, constant frequency V2 peak control and constant frequency V2 valley control.

Comparison of Small-Signal Characteristics in Current-Mode Control Schemes for Point-of-Load Buck Converter Applications

Different current-mode controls have been widely adopted in commercial pulse-width modulation controllers for point-of-load (POL) converter applications. To understand the unique properties of various current-mode control schemes, and to study the differences between them, we have investigated and compared four current-mode control schemes (peak-current control, valley-current control, constant on-time control, and constant off-time control) for POL power converters and voltage regulator applications. Performance attributes under investigation include high-bandwidth voltage loop design, adaptability to a converter with a wide input voltage range, adaptive voltage positioning design, and audio susceptibility. The pros and cons of these schemes are identified and explained by the unified small-signal equivalent circuit model. In terms of dynamic performance, this study provides a current-mode control scheme selection criteria and feedback design guidelines. The theoretical analyses are verified by both simulation and experimental results.

Four kinds of commonly used current-mode control schemes (peak-current control, valley-current control, constant on-time control, and constant off-time control) are compared for suitability for use in point-of-load buck converters. Selection guidelines have been created according to the small-signal characteristics of different implementations.

1. Compared with constant frequency control, constant on time/ off-time control can achieve wider T2 bandwidth in D<0.5 and D>0.5 applications. In constant frequency current-mode controls, PCM control does not need external ramp compensation for small duty cycles (e.g., D <0.3), so it is preferable to use PCM control for small-duty-cycle applications. Similarly, VCM control is preferable for large-duty-cycle applications.
2. Variable frequency control is preferable for the converter that must accept a wide input voltage range, because the high-frequency double poles are always on the left half-plane. No ramp compensation is needed, so the current control effect is never weakened by an external ramp. In contrast, PCM control and VCM control need an external ramp to keep the double poles on the left half-plane. Designing the external ramp based on the worst case (maximum duty cycle for PCM control and minimum dutycycle for VCM control) means overcompensation for other operating points.
3. To achieve AVP, constant on-time control simplifies the voltage loop finite-gain compensator.

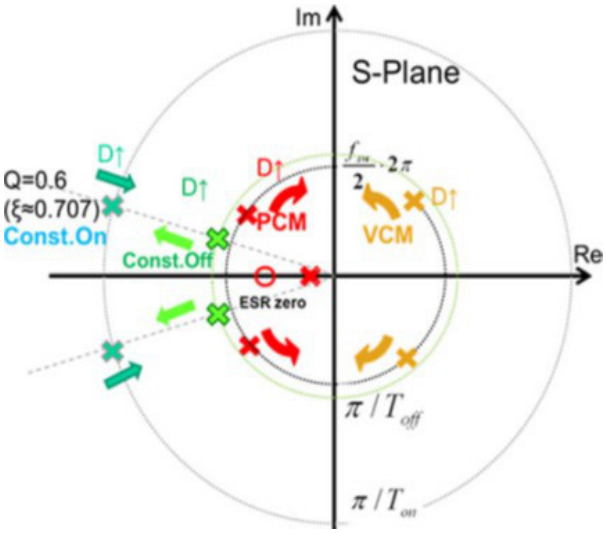


Fig. 1. Pole zero movement of different control strategies when duty cycle varies

Constant off-time control inherently has zero audio susceptibility at any operating point. It is suitable for applications requiring perfect line-transient performance. PCM control can also achieve zero audio susceptibility and proper double pole damping at around 0.2 < D < 0.4.VCM control, and constant on-time control cannot have this property. For VCM control and constant on-time control, the gain of audio susceptibility increases with duty cycle D.vv

Analysis and Optimization of Module Integrated MPPT Converter-Based Residential PV System

The power loss that results from mismatched power levels is critical to improving overall efficiency of the residential PV system. In general, a dedicated DC-DC converter with an extra distributed MPPT (maximum power point tracking) algorithm, used in a MIMC (module integrated MPPT converter), is connected to each panel to reduce the mismatch impact. However, even when using MIMCs, it is not always possible to guarantee all the panels work at their MPP (maximum power point) operation points. We have analyzed the characteristics of the MIMC-based residential PV, and derived the criteria for ensuring that all the MIMCs work at their MPPs. We propose an optimized MIMC system configuration to allow each of the PV panels to work at its individual MPP regardless of the mismatch case. Simulation and experimental results have validated the proposed system structure. The conventional NP balancing algorithms don't deal with switching loss reduction, because the redundant vector selection is based on a single objective. However, for high-power, high-frequency NPC power conversion systems, in addition to the NP balance, loss and noise reduction are also important goals. We have also developed a new SVM scheme based on the existing control algorithms, that can achieve multiple objectives at the same time.

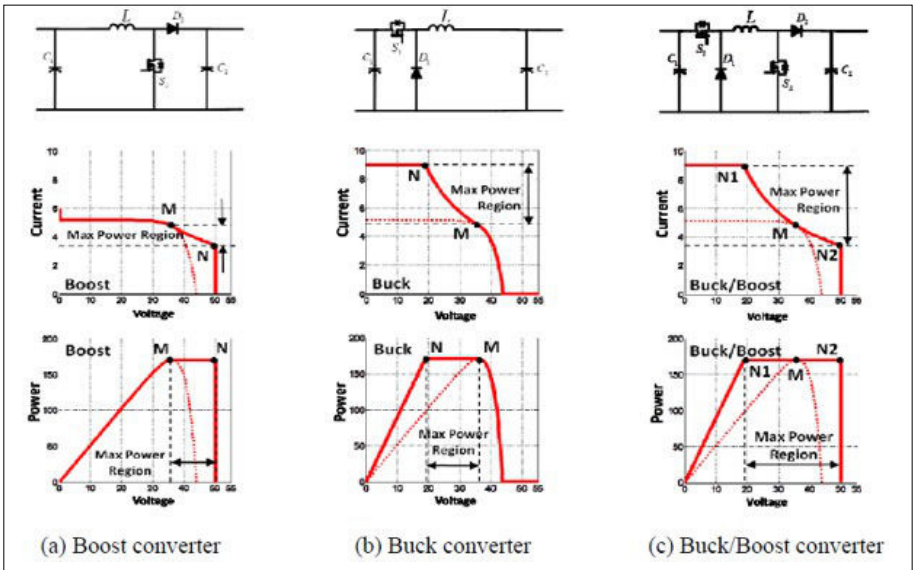


Fig. 1. Output characteristic curve of three topologies

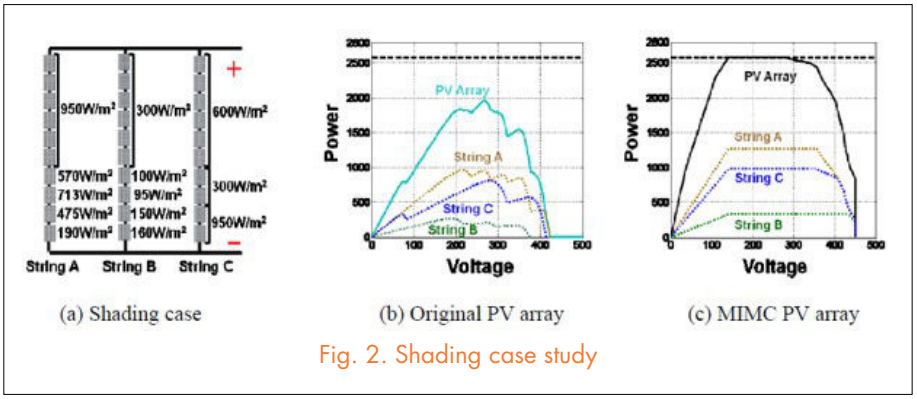


Fig. 2. Shading case study

High-Frequency Integrated Point-of-Load Converters: Overview

This overview paper focuses on state-of-the-art technologies and trends toward the integration of point-of-load (POL) converters. This paper encompasses an extended survey of literature, ranging from device technologies and magnetic materials to integration technologies and approaches. This paper is organized into three main sections.

1) Device technologies, including the trench MOSFET, lateral MOSFET, and gallium nitride (GaN) high electron mobility transistor, are discussed along with their intended applications. The critical role of device packaging to high-frequency integration is also assessed.

2) Magnetic materials: In recent years, a number of new magnetic materials have been explored to facilitate magnetic integration for high-frequency POL converters. These data are collected and organized to help select magnetic material for various frequency ranges.

3) Integration methods, which are defined with the focus on magnetic integration techniques and approaches. Two integration levels are classified; namely wafer level and package level. Detailed information is presented for each integration level to identify a suitable current scale and frequency range. Three-dimensional integration, which uses a magnetic component as a substrate, is one of the promising integration methods. By using an integrated GaN device and a low-profile, low-temperature co-fired ceramic inductor substrate, the power density of the latest 20-A 5-MHz 3-D integrated POL converter is demonstrated as high as 1100 W/in^3, which is an improvement of a factor of 10 compared to industry products at the same current level.

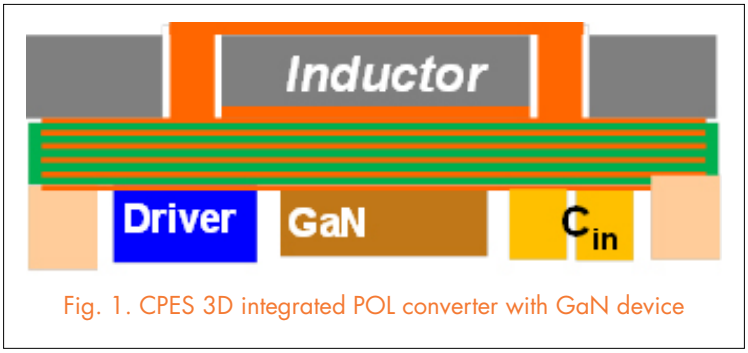


Fig. 1. CPES 3D integrated POL converter with GaN device

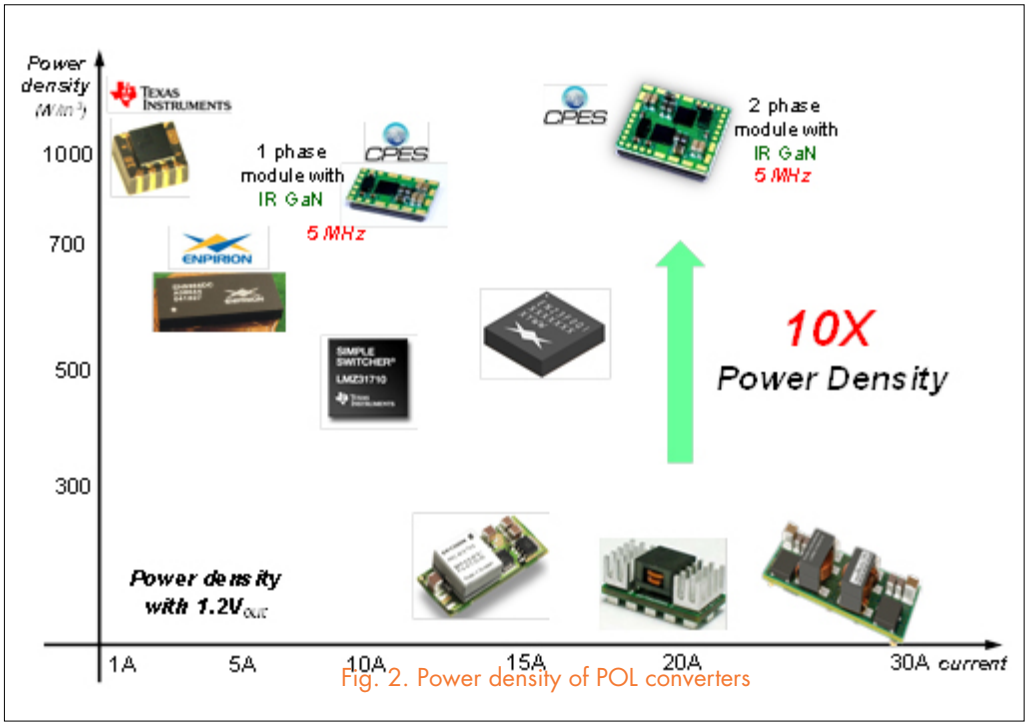


Fig. 2. Power density of POL converters

Analysis of Unified Output MPPT Control in Sub Panel PV Converter System

Photovoltaic (PV) systems frequently suffer disproportionate impacts on energy production due to mismatch cases. To remedy this, academia has proposed a distributed maximum power point tracking (MPPT) solution which has been implemented commercially. Taking the trend of the "distributed MPPT" concept a step further, this paper discusses and analyzes an MPPT converter that connects to each PV cell string, called a subpanel MPPT converter (SPMC), to better address the real-world mismatch issues. The SPMC system with a unified output MPPT control structure is also proposed in order to reduce the cost and simplify the distributed MPPT system. The proposal saves A/D units, current sensors and MPPT controllers on the premise of guaranteeing that all the PV cell strings work at their individual maximum power state regardless of the mismatch case. This is favorable for further integration and makes the whole SPMC system less expensive and easier to realize., The effectiveness of this proposal has been confirmed experimentally.

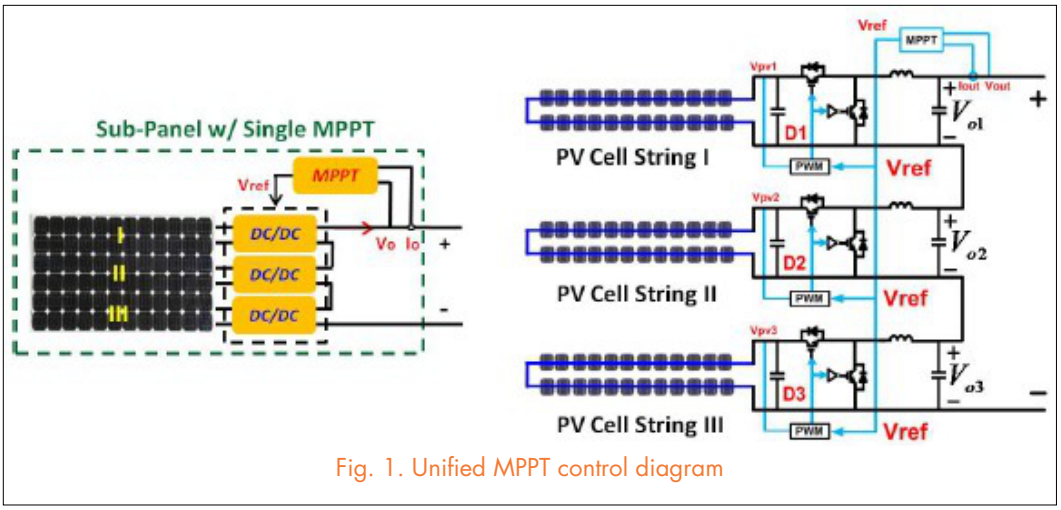


Fig. 1. Unified MPPT control diagram

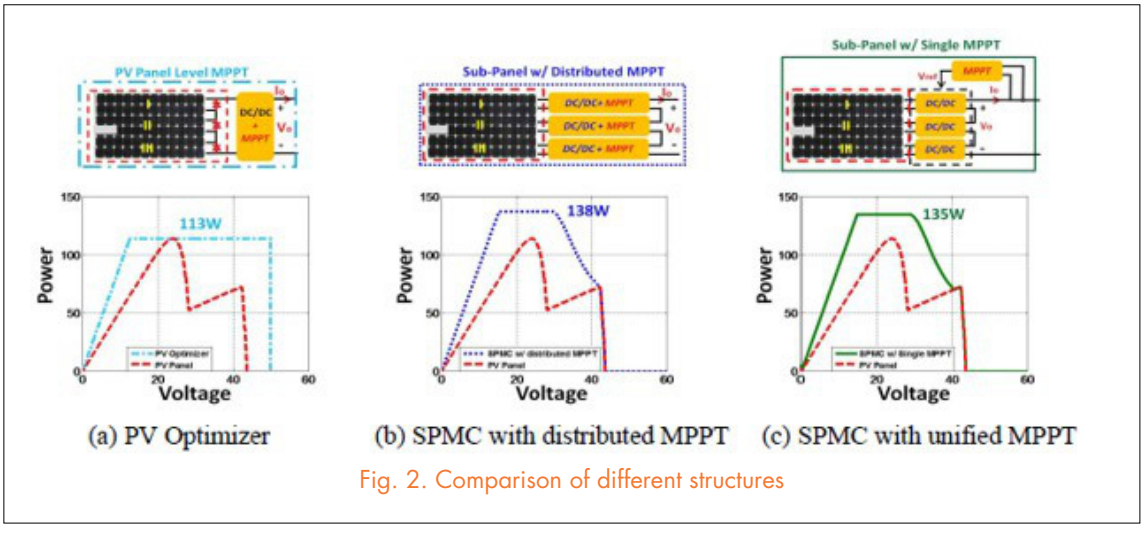


Fig. 2. Comparison of different structures

State-trajectory Control of LLC Converter Implemented by Microcontroller

This paper investigates how to integrate state-trajectory control functions of LLC resonant converters within a commercial low-cost microcontroller, including simplified optimal trajectory control (SOTC) for load transients, burst mode and soft start up.

State-trajectory control functions have been discussed and verified separately. However, in real applications, all these functions need to be realized in one single controller. Therefore, it is worthwhile to determine how to implement all state-trajectory control functions in one controller. There are mainly three challenges to achieve this goal: firstly, complex calculation in state-trajectory control requires a high-performance digital controller, such as a high-end FPGA and a very fast analog-to-digital converter; however, the cost-effective MCU is preferred in industrial applications; secondly, burst-mode control with constant burst-on time and optimal switch patterns can't be used directly when associated with normal operation, because there would be very large dynamic oscillation in both the resonant tank and output voltage during the transient processes between burst mode and normal operation; thirdly, for a given application, it is still unknown how to design the whole control system structure and then select a proper MCU.

To solve these problems, a simplified calculation process is proposed for the SOTC to minimize digital delay. The proposed guidelines to select a proper microcontroller limit calculation delay and ADC delay to within one switching cycle to ensure good transient performance. Optimized transient processes are proposed that eliminate large oscillation between burst mode and normal operation. Soft start-up is implemented by sensing the output voltage only.

After implementing each control function by MCU, all the control functions are integrated within one cost-effective MCU. The state transition diagram of the whole system is shown in Fig. 1. Experimental results are demonstrated on a platform, as shown in Fig. 2, which is a 130kHz 300W 380V/12V half-bridge LLC resonant converter with MCU TMS320F2808.

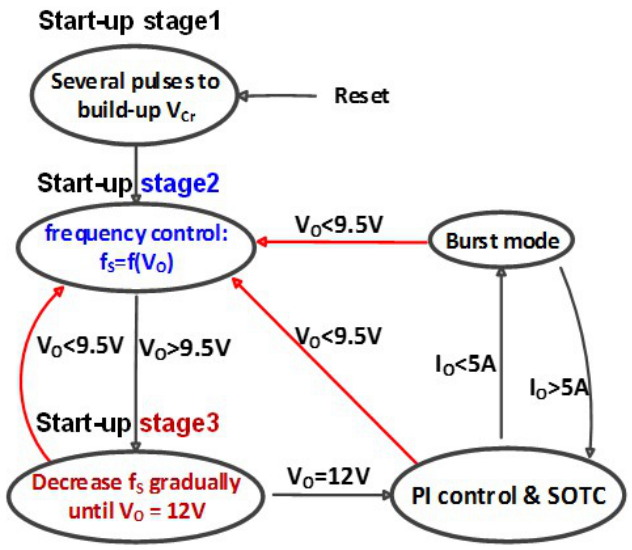


Fig. 1. State transition diagram of control system

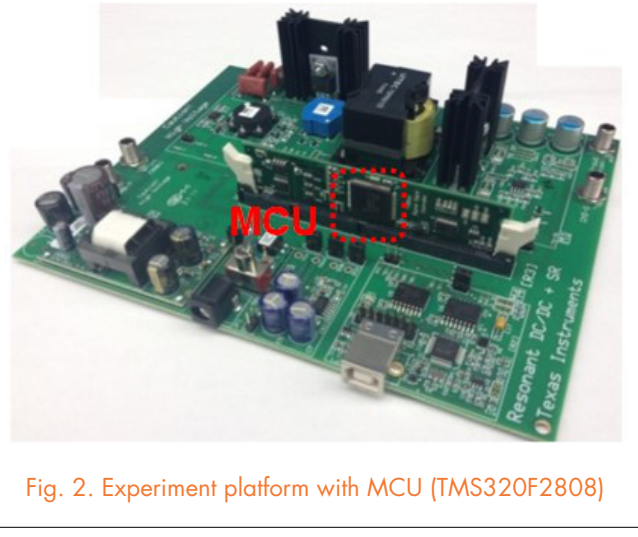
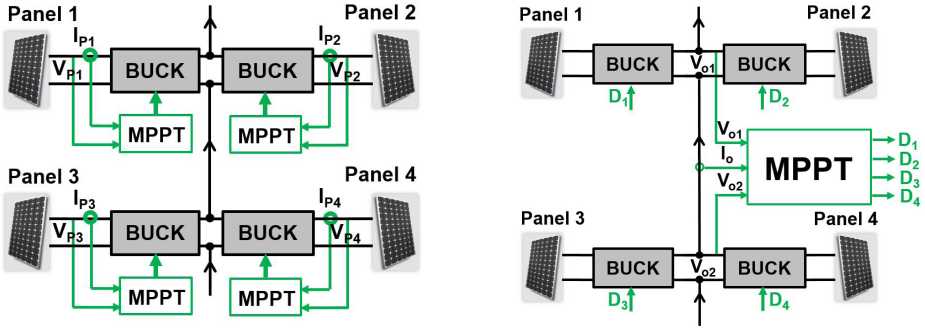


Fig. 2. Experiment platform with MCU (TMS320F2808)

Distributed MPPT Method for Smart Converter PV Systems

To improve PV system energy harvesting efficiency under mismatch conditions, a panel-level MPPT converter, or what we call a smart converter, has been developing very rapidly in recent years. In the smart converter PV system, each panel has a dedicated MPPT converter to improve energy production. In this dedicated converter, a voltage and current sensor are required to calculate the panel output power, and a MPPT controller is also needed for peak power tracking, as shown in Fig. 1(a). Although the dedicated converters can extract maximum power from the PV panels, the equipment cost is high. To reduce the cost and simplify MPPT control, a novel MPPT method with less sensor and controller is proposed, as shown in Fig. 1(b).

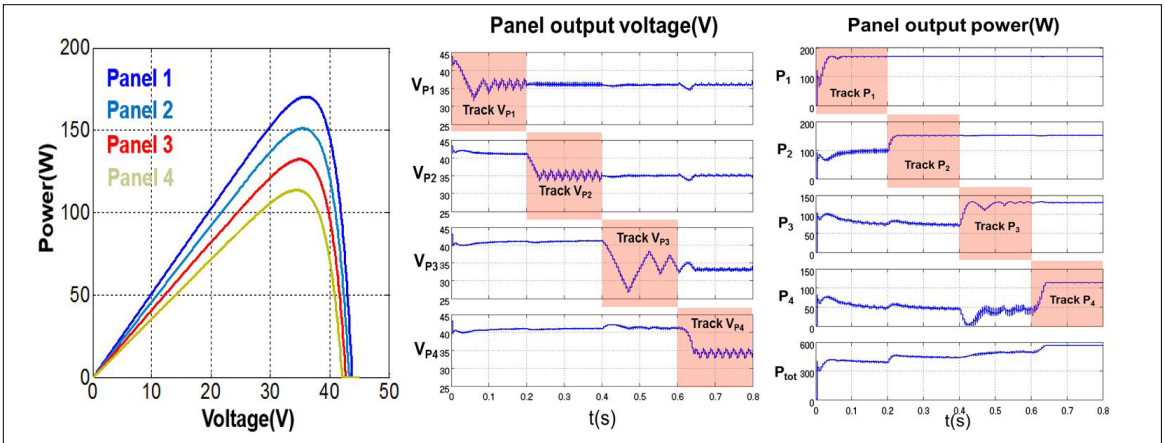


(a) Previous MPPT solution for smart converter

(b) Proposed MPPT solution for smart converter

Fig. 1. Existing and proposed distributed MPPT method for smart converter PV systems

To verify the proposed MPPT solution, a simulation is performed, the results of which are shown in Fig. 2. In this simulation, four panels have non-uniform irradiance, as shown in Fig. 2 (a). Firstly, the controller tracks the MPP for Panel 1, and fixes the output power of the other three panels, as shown in Fig. 2 (b). After finding the MPP for Panel 1, the controller tracks the MPP for Panel 2 and fixes the output power of the other three panels. Using the same method, the controller can track the MPP of the four panels one by one, as shown in Fig. 2 (c).



(a) P-V curve of four panels

(b) Start-up panel voltage

(c) Start-up panel power

Fig. 2. Simulation results for the proposed MPPT solution for a cascaded smart converter

Transient Performance Improvement for Constant On Time Control

For better light load efficiency and high bandwidth design capability constant on time (COT) control is widely used in the VR industry. However, COT control still has some limitations in load step up and load step down transient responses. In a large load step up, the inductor current might not be able to reach the target load very quickly because of minimum off time of the system after every pulse and output may experience undershoot. On the other hand, in the load step down case, for given power stage, overshoot can be very large if load release is occurred at the beginning of the gate turn on time (T_{on}) as inductor current will keep rising till fixed T_{on} expires.

This paper proposes a method called 'FastAOT' which increases or decreases the T_{on} in COT control immediately after load step up or load step down to reduce the undershoot or overshoot at aforementioned conditions. The Fig. 1 shows the concept of the proposed method, added in a conventional COT control, where the proposed circuit is inside the red box. In the proposed circuit, first a band pass filter is used to detect the undershoot or overshot at output (V_o) and to create a peak or valley accordingly and then a emitter follower is added so that only the peak in V_{FLT} created by V_o undershoot will pass through. Then follower output V_{FAOT} is used as the reference for the adaptive on time generator circuit inside the green box. In Fig. 2(a) and (b), we see the comparison of undershoot without and with the proposed 'FastAOT' method and found smaller undershoot in Fig 2(b) with proposed method than constant T_{on} in Fig. 2(a). In case of load step down, when the proposed 'FastAOT' method detects an overshoot at V_o, then output of the high pass filter, V_{FLT} goes down very quickly. Then this signal is compared with 80% of VID to generate logic V_{os} which eventually AN-Ded with T_{on} to expire T_{on} immediately after load step down and therefore, reduce overshoot at output. Comparing the Fig.3 (a) and (b), we can clearly see that in Fig.3 (b) the gate signal D expires right after load step down and hence produce smaller overshoot.

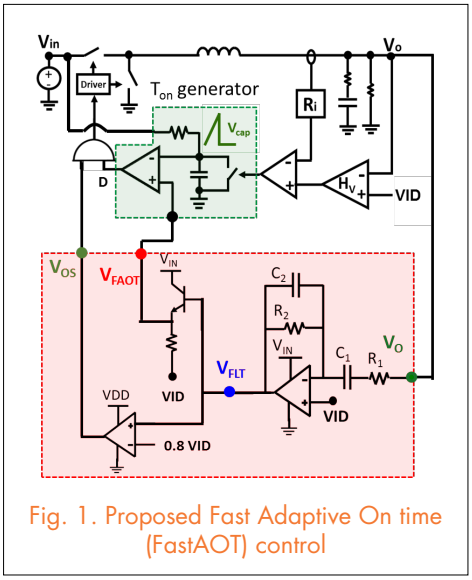


Fig. 1. Proposed Fast Adaptive On time (FastAOT) control

The main advantage of this proposed circuit is that it can reduce the undershoot and overshoot in COT control using the same simple circuit without affecting steady state condition. Another advantage of this method is that as the change of T_{on} is proportion to V_o change, chance of ring back problem is smaller which might exist in some cases where T_{on} increment is predefined. As the proposed circuit does not contain any negative voltage, it is easily implementable inside IC and also the magnitude of the T_{on} increment can also be adjusted by changing the filter gain easily.

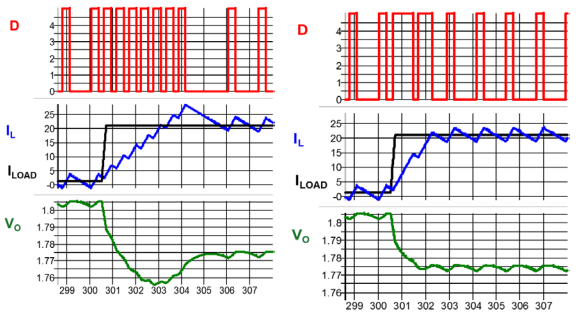


Fig. 2. Load step up response
(a) without FastAOT (b) with FastAOT

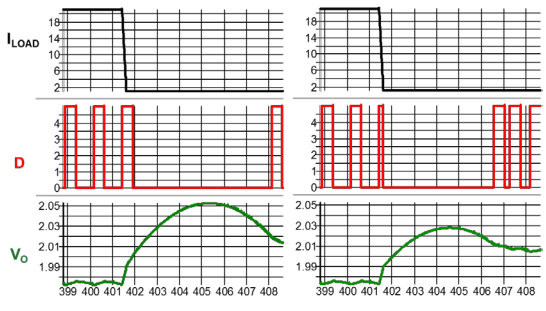


Fig. 3. Load step down response
(a) without FastAOT (b) with FastAOT

High Density Intergration Nuggets

Conducted EMI and Systems Integration

Design of Integrated Transformer and Inductor for High Frequency Dual Active Bridge GaN Charger for PHEV

Analysis and Reduction of Common Mode EMI Noise for Resonant Converters

Comparison of Coil Designs for Wireless Inductive Power Transfer

High-temperature Characterization and Comparison of 1.2 kV SiC Power Semiconductor Devices

High-temperature Characterization and Comparison of 1.2 kV SiC Power MOSFETs

Characterization and Comparison of 1.2 kV SiC Power Semiconductor Devices

A Thermally Enhanced High-Speed Switch Module: Fabrication and Application to Converter

Thermal Stability of Al_2O_3-Filled Silicone-Based Elastomers for Power Electronic Encapsulation

A Frequency-Domain Study on the Effect of DC-Link Decoupling Capacitors

High Frequency Integrated Point of Load (POL) Module with PCB Embedded Inductor Substrate

Chip-Bonding on Copper by Pressure-Less Sintering of Nanosilver Paste Under Controlled Atmosphere

Thermal Characterization of Planar High Temperature Power Module Packages with Sintered Nanosilver Interconnection

A Novel Hybrid Packaging Structure for High-Temperature SiC Power Modules

Comparison of Critical Conduction Mode, Triangular Conduction Mode and Fixed Frequency Modulation Schemes for Single Phase Hbridge Boost PFC

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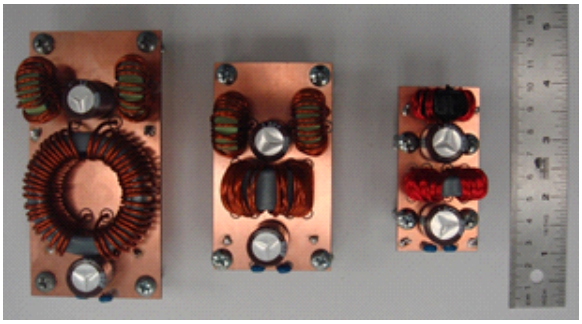
Conducted EMI and Systems Integration

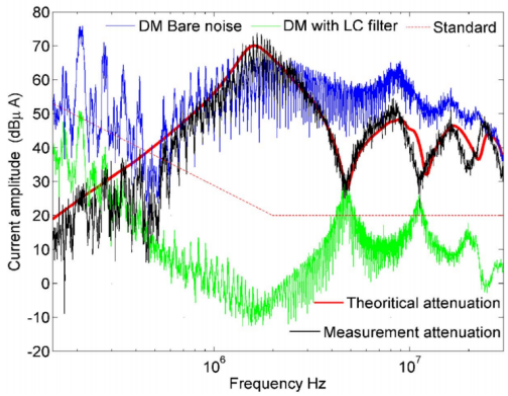
Electronic power processing technologies being developed now have the potential to revolutionize the way electricity is generated, distributed, and used. Over the past ten years, there has been increased incorporation of power electronics converters in "more electric" cars, ships, and airplanes to replace thermo-mechanical, mechanical, hydraulic, and pneumatic primary and secondary power systems. These converters have been introduced with the goals of reducing the size, weight, and maintenance and operational costs of these power systems, while increasing efficiency, safety, reliability, and optimizing mission-specific objectives. While energy efficiency is mostly being pursued through system-level power management and converter integration, power density increases are being addressed by the use of new materials, increased levels of integration, and innovative circuit designs. The recent increased availability of experimental active silicon carbide (SiC) and gallium nitride (GaN) devices has opened new opportunities for designing power converters that operate at increased switching frequencies with higher voltages and lower losses, which enables the reduction of the size and weight of the passive components for energy storage. However, switching devices introduce electromagnetic interference (EMI) problems into the system.

In order to avoid interference between different systems, the EMI noise emissions from the power converters need to be limited, and compliance with certain electromagnetic compatibility (EMC) standards is regularly required. EMI filters are inevitably made part of power electronics systems to provide attenuation for EMI noise, but the additional EMI filter weight may diminish the benefits power electronic converters have over traditional systems, and even make the total weight and size greater. Therefore, it is a big challenge for modern power electronic system design to integrate the power converter and EMI filter together to minimize total weight/size and thus improve system power density.

Minimizing conducted EMI noise to meet the standards often involves trial and error. Despite this prevalent tactic, there have been systematic EMI mitigation techniques and design procedures developed over the years. This paper summarizes some of the authors' research efforts towards improvements in system EMI noise reduction and EMI filter weight/size optimization. The paper addresses several issues and approaches to system EMI modelling, EMI filter design, and weight/size optimization and integration together with examples of the EMI noise measurement results. EMI noise attenuation methods are discussed in detail, and key issues in filter design optimization process are presented and illustrated with the EMI filter test results. Possible improvements in power density through compact filter design and filter integration are also shown. The results are presented in the form of "nuggets" that highlight the basic ideas and their possible impact, but do not provide great detail on the technical contributions – these details can be found in the referenced papers.



(a) EMI filter Size/Weight Reduction



(b) Prediction of EMI filter performance

Figure 1: Example issues in EMI filter design

Design of Integrated Transformer and Inductor for High Frequency Dual Active Bridge GaN Charger for PHEV

We propose a design of a high-power-density-transformer and inductor for a high-frequency dual active bridge (DAB) GaN charger. Because the charger operates at 500 kHz, the inductance needed to achieve ZVS for the DAB converter is reduced to as low as 3uH. As a result, it is possible to utilize the leakage inductor as the resonant inductor of the DAB converter. To create this amount of leakage inductance, a certain amount of space between the primary and secondary winding is allocated to store the leakage flux energy. The designed transformer is 99.2% efficient while delivering 3.3kW. Its volume is 40% smaller than the nearest published equivalent counterpart, and over 63% smaller than the lump transformer and inductor in a 50kHz Si charger.

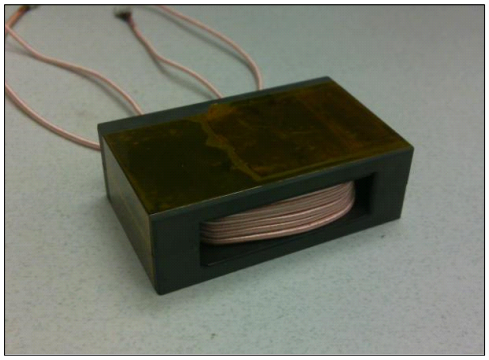


Fig. 1 Transformer and inductor in one component

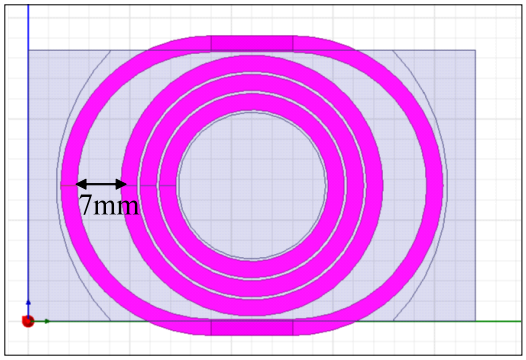


Fig. 2 Space between primary and secondary windings

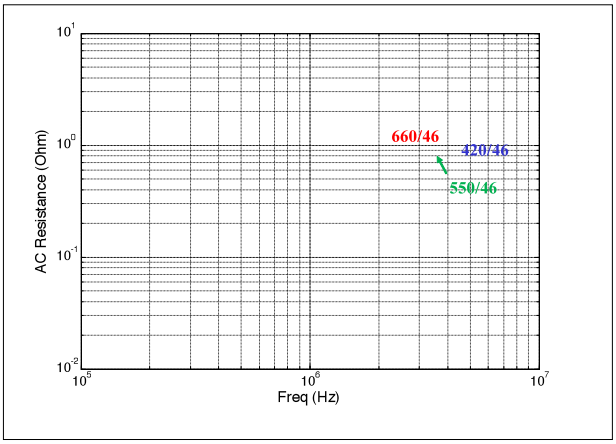


Fig. 3 Litz wire selection to reduce winding loss

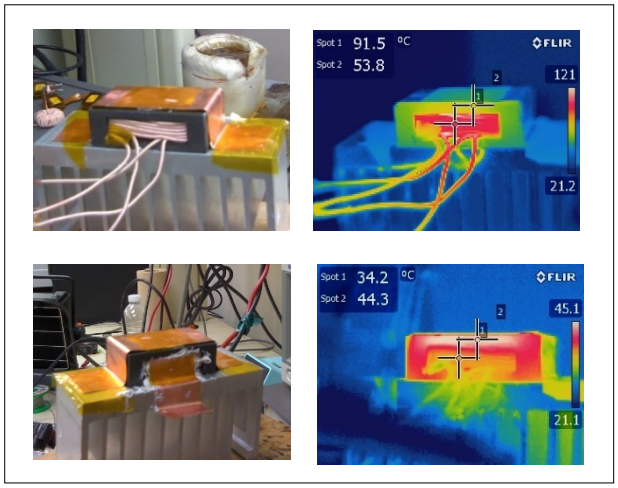


Fig. 4 Thermal management

Analysis and Reduction of Common Mode EMI Noise for Resonant Converters

There are many topologies of resonant converters. The topologies can be grouped according to the number of resonant elements. The simplest topology of resonant converter is the two-element resonant converter: the series resonant converter (SRC) and the parallel resonant converter (PRC). Unfortunately, these topologies cannot be applied widely due to their limitations. In practice, the three-element resonant converter is the most popular topology of resonant converter. In the three-element resonant converter group, there are a total of 36 different topologies. Among them, the most practical topologies are LLC, CLL and LCL resonant converters because of their LLC-like gain characteristic.

The source of CM noise is the voltage pulse (dv/dt) of the switching devices. The propagation path of CM noise is the parasitic capacitance, e.g. the inter-winding capacitance of the transformer, or the drain-to-ground capacitance of the switches. A high switching frequency not only brings the resonant converter high power density, but may also cause high dv/dt on the converter nodes, which may have resonant converters suffer from severe EMI issues. Different topologies of resonant converter have different dv/dt characteristics. After analyzing the dv/dt characteristic of three different topologies of resonant converter (LLC, CLL and LCL) and comparing their CM noise performance, we find that the LCL resonant converter has the best CM noise performance among three topologies, but it is not the most popular one in commercial products. The LLC resonant converter is the most widely used topology, however it has poor CM noise performance.

A 1 MHz 400/12V 1kW LLC converter with a matrix transformer is used as an example. The peak efficiency of this LLC converter is 95.4% and the power density is 710W/in$_3$. The typical commercial product has 98% efficiency and 60W/in$_3$ power density. However, the matrix transformer has very large inter-winding capacitance which leads to severe CM noise problems. Much research has been done to reduce the CM noise in LLC resonant converters. However, there is lack of study of CM noise reduction in matrix transformers. We have devised a novel shielding method to reduce the CM noise of LLC resonant converters. With shielding, the CM noise of LLC resonant converters is reduced significantly.

Loss analysis of the shielding is provided using the FEA tool. The experiment results show that the shielding introduces very little extra loss to the converter. Furthermore, a way to further reduces the loss and improve efficiency is introduced and verified by the FEA tool.

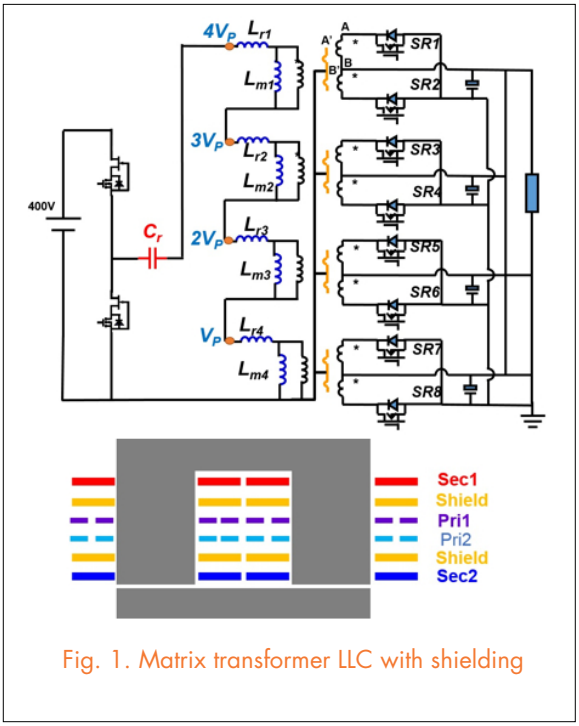


Fig. 1. Matrix transformer LLC with shielding

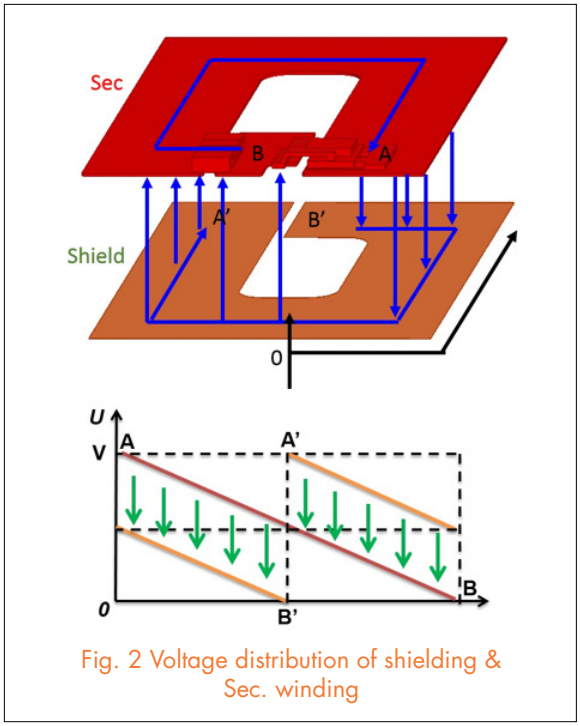


Fig. 2 Voltage distribution of shielding & Sec. winding

Comparison of Coil Designs for Wireless Inductive Power Transfer

The wireless inductive power transfer (WIPT) is an efficient method used to wirelessly charge objects such as biomedical devices, portable electronic devices, and electric vehicles. It transfers energy through a magnetic field between a transmitter and receiver coils. By placing resonant tanks with the same resonant frequencies on both the primary side and secondary side, the charging distance can reach up to tens of centimeters with 90% efficiency. The transfer efficiency of the WIPT is influenced by the resonant frequency, coupling coefficient, and quality factor of the coils. So to increase the transfer efficiency, coil design is very significant.

Four coil designs are surveyed and simulated using FEA software, including a circular pad, a DD-DDQ pad, a windings array, and a one-outer-loop coil. They are designed for different power levels and operating frequencies: the circular pad and DD-DDQ pad are designed for 2 kW and 20 kHz, while the windings array and one-outer-loop coil are designed for 10 W and 150 kHz. So the dimensions and percentage of materials for the coil designs are very different. To make a fair comparison normalized factors, such as power density, quality factor, and a coupling coefficient are used.

The coupling coefficient reflects the coupling between the transmitter and receiver. It will directly influence the transfer efficiency of the WIPT systems. The coupling coefficient of the four coil designs are compared with different gaps and misalignment. Fig.1 shows a coupling coefficient vs. a normalized gap. The circular pad and the DD-DDQ pad have larger coupling coefficients when the gap between the transmitter and the receiver is small. However, when the gap is increased, the windings array and the one-outer-loop coil have larger coupling coefficients. Which structure to choose in the design process depends on the gap specification of the application. Fig.2 shows a coupling coefficient vs. misalignment. The coupling coefficient of a circular pad drops fast with misalignment. Due to the function of a quadrature coil, the DD-DDQ pad has a coupling coefficient bigger than 0.1, but it fluctuates. The coupling coefficients of the windings array and the one-outer-loop coil are not sensitive to misalignment, because the transmitter size is bigger than the receiver. So the windings array and the one-outer-loop coil are better choices for applications where misalignment usually changes.

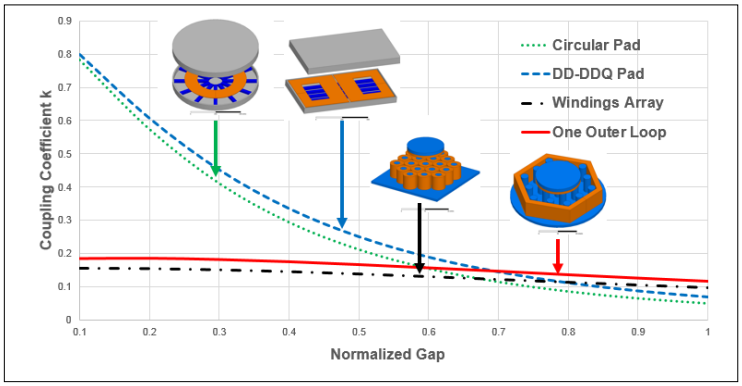


Fig. 1. Comparison of Coupling Coefficient vs. Gap

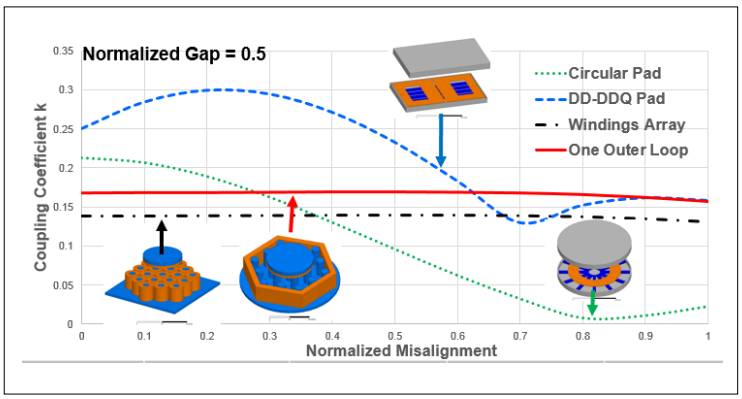


Fig. 2. Comparison of Coupling Coefficient vs. Misalignment

High-Temperature Characterization and Comparison of 1.2 kV SiC Power Semiconductor Devices

Although its high-temperature operation is one of the major advantages that Silicon Carbide (SiC) holds over silicon, few studies have assessed its full high-temperature (> 175° C) capabilities. This work seeks to provide insight into the high-temperature performances of state-of-the-art SiC power semiconductors by characterizing and comparing the latest generation of 1.2 kV SiC MOSFET, BJT, SJT, and normally-off (enhancement mode) JFET devices from the semiconductor industry's main players; namely Cree, Rohm, GE, Fairchild, and GeneSiC. To carry out this study, both static and dynamic characterization were performed from 25° C to 200° C.

The on-resistances of each device were measured using a curve tracer. It is important to look at the specific on-resistances of the devices since for a given breakdown voltage the smaller the die size the larger the resistance. In this case, this figure was obtained by multiplying the measured on-resistance values by their respective die area.

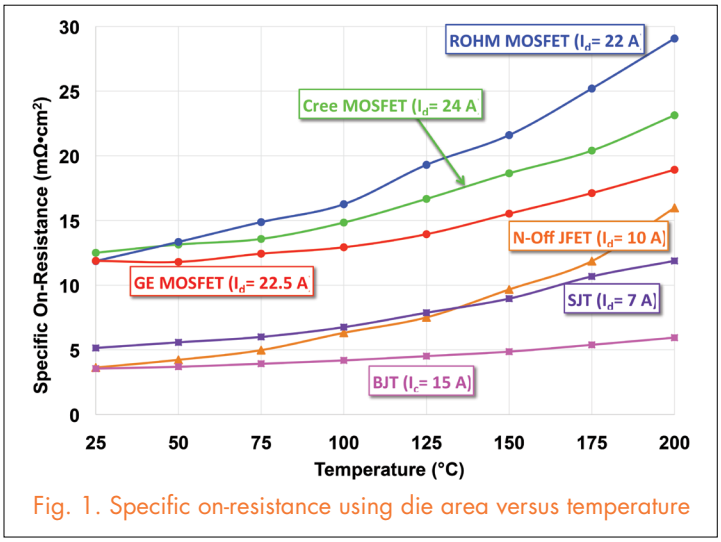


Fig. 1. Specific on-resistance using die area versus temperature

Fig. 1 shows the measured specific on-resistance versus temperature for each of the devices. As seen in this figure, the on-resistance of the SiC normally-off JFET was the most temperature-sensitive. This can be attributed to strong phonon scattering, which reduces the carrier mobility. Moreover, the SiC MOSFETs had the highest specific on-resistances while the BJT had the lowest. It can also be observed that the on-resistance of the BJT was the least temperature-dependent, which indicates constant conduction losses with varying temperature.

The DPTs conducted at high-temperature revealed that the SiC MOSFETs experienced a reduction in turn on energy, and an increase in turn off energy with increasing temperatures. The BJT and SJT, on the other hand, showed little change in the total switching loss with increasing temperature. Finally, the total switching loss of the normally-off JFET showed a small increase with temperature, which was accredited to the decreased dv/dt during turn-on.

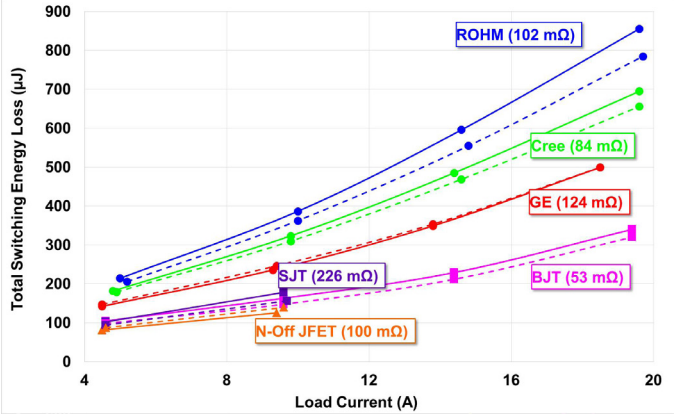


Fig. 2. Total switching energy loss versus load current at 25° C (solid) and 200° C (dashed)

High-Temperature Characterization and Comparison of 1.2 kV SiC Power MOSFETs

Wide bandgap semiconductors such as Silicon Carbide (SiC) make high-temperature, high-power-density converters feasible due to their high thermal conductivity, high breakdown field, and low intrinsic carrier concentration. This work thus fully characterizes a state-of-the-art 1.2 kV SiC MOSFETs from Cree, ROHM Semiconductor, and General Electric (GE). A complete static characterization from 25° C to 200° C is performed on each SiC MOSFET. This includes threshold voltage, specific on-resistance, leakage current, junction capacitances, and internal gate resistance. The dynamic performances are assessed through double-pulse tests (DPTs) from which the switching energy losses are calculated.

Fig. 1 shows the measured specific on-resistance versus temperature. The drain current used for the measurements is shown in parenthesis for each curve. The gate-source voltage used for the on-resistance measurement was 20 V since this is the voltage at which the MOSFETs will be driven. As seen in the figure, the GE MOSFET is the least temperature dependent, increasing by approximately 37% at 200° C with respect to its room-temperature resistance.

DPTs were performed on each SiC MOSFET with a DPT setup specifically designed to reduce the parasitic components that inhibit switching performance. The optimal driving condition for each SiC MOSFET was determined by performing multiple DPTs for several different external gate resistances RG, ext to account for the variation in internal gate resistance described above. The external gate resistance that yielded the lowest switching energy loss without causing significant ringing was selected. Due to the large internal gate resistance of the ROHM SCT2160KE MOSFET, even when no external gate resistance is used the total gate resistance is still nearly double that of the other devices. Consequently, although the ROHM SCT2160KE MOSFET proved to have low junction capacitances, the device can be expected to experience higher losses. Fig. 2 shows the total switching energy loss plotted against load current. DPTs revealed that the majority of the switching losses are experienced during turn on, thus soft switching could be applied in order to increase switching efficiency.

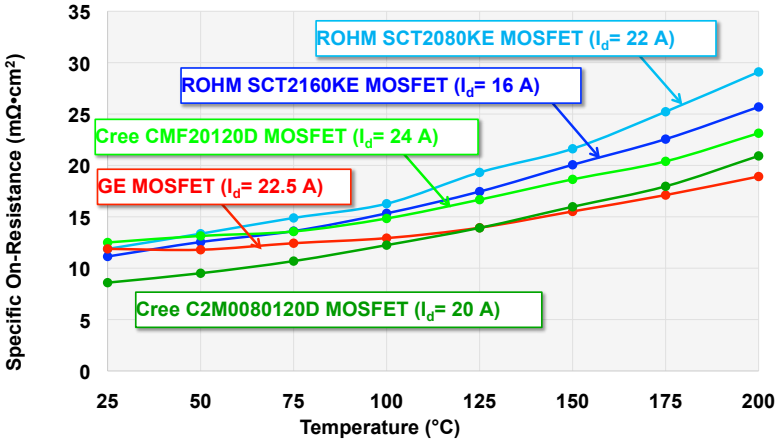


Fig. 1. Specific on-resistance using die area versus temperature

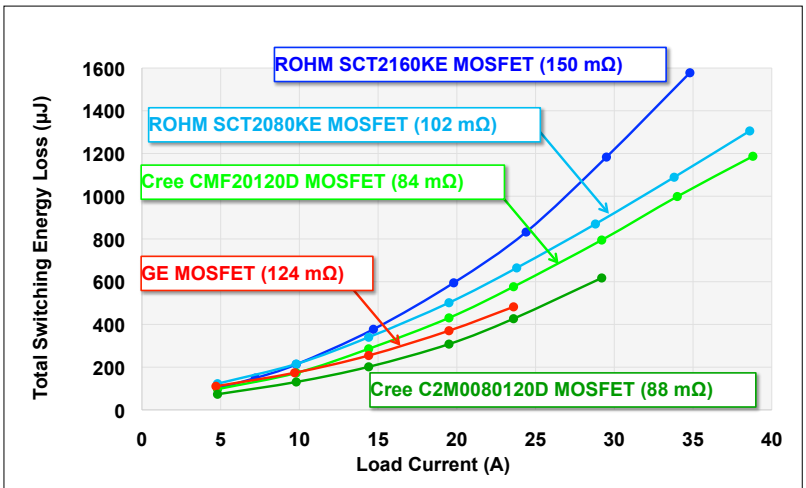


Fig. 2. Total switching energy loss versus load current

Characterization and Comparison of 1.2 kV SiC Power Semiconductor Devices

A significant effort has been devoted to characterizing the numerous Silicon Carbide (SiC) power semiconductor devices under development. Of these devices, the SiC MOSFET has received significant attention up to now given its maturity, relative ease of commercialization, and simple driving scheme. While recent studies have shown that the gate-oxide of the SiC MOSFETs is reliable beyond 200° C, which remained one of the major barriers of this device until now, oxide-free structures such as the BJT, and normally-on and normally-off JFETs have been pursued as well. Since high-temperature operation is one of the major advantages offered by SiC over Si, it is of great interest to evaluate the performance of these devices under extreme temperature conditions.

The on-resistances of each device were measured using a curve tracer. It is important to look at the specific on-resistances of the devices since for a given breakdown voltage the smaller the die size the larger the resistance. In this case, this figure was obtained by multiplying the measured on-resistance values by their respective die area.

Fig. 1 shows the measured specific on-resistance versus temperature for each of the devices. As shown by the figure, the ROHM SiC MOSFET and Infineon SiC normally-on JFET had the highest specific on-resistances (when calculating this figure based on the total die area), while the Fairchild SiC BJT experienced the lowest. The on-resistance of the BJT also proved to have the weakest temperature dependence.

Double-Pulse Tests (DPTs) were performed on each SiC transistor with a DPT setup specifically designed to reduce the parasitic components that inhibit switching performance. As shown Fig. 2, ROHM's SiC MOSFET has the highest total switching energy loss. SemiSouth's SiC normally-off JFET, on the other hand, showed the lowest total switching energy losses when plotted against load current. However, driving losses have not been taken into consideration. Depending on the application, the driver losses generated by the driving method used in this study for the normally-off JFET, BJT, and SJT, which are devices that consume notable gate currents in the on-state, could become sizable.

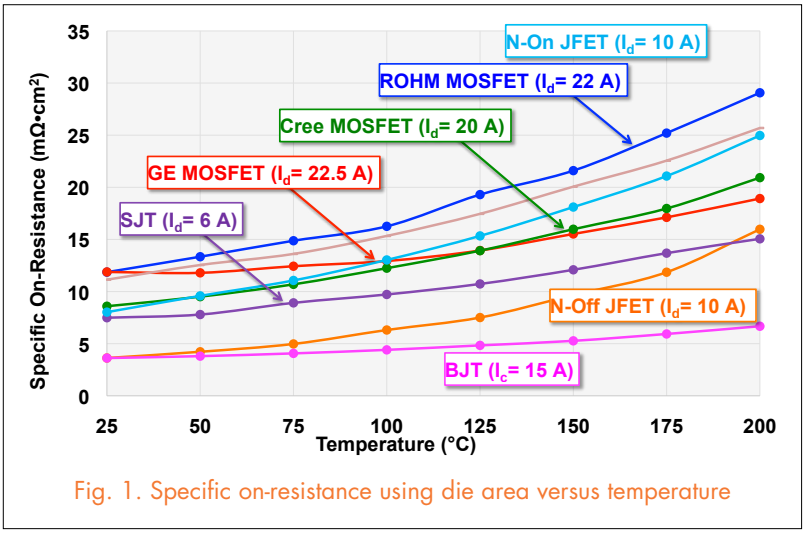


Fig. 1. Specific on-resistance using die area versus temperature

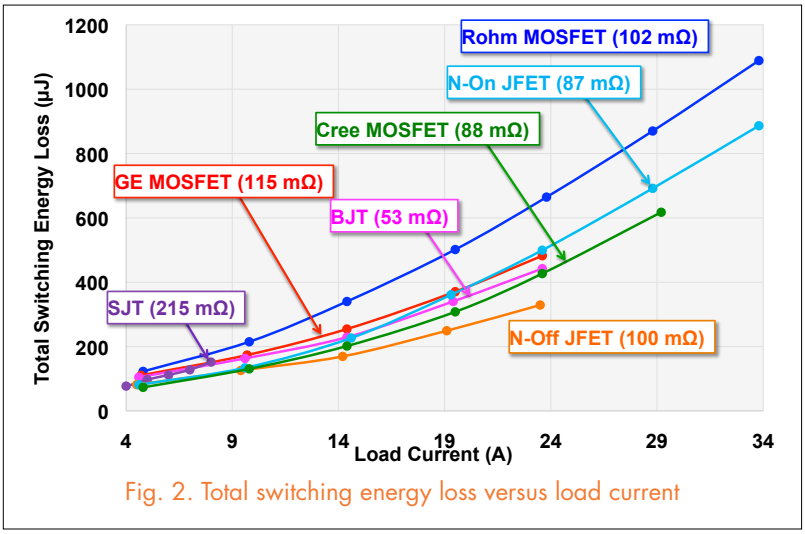


Fig. 2. Total switching energy loss versus load current

A Thermally Enhanced High-Speed Switch Module: Fabrication and Application to Converters

Vehicular power systems are characterized by their stringent requirements for reliability, efficiency, and power density. Along with high-frequency switching to decrease the size of passive components, efficient heat management is a key technique to obtaining high power density, as it can reduce the need for bulky cooling devices such as heat sinks, fans, and liquid coolants. We propose the construction and utilization of a thermally enhanced switching module to lower the system thermal resistance and achieve a compact power system. The proposed thermally enhanced module integrates the semiconductor devices, their drivers and heat sinks by using direct bond copper (DBC): on the top side the DBC is used to assemble the electric components (see Fig. 3(a)), and on the bottom side the heat sink is attached to the DBC (see Fig. 3(b)). The DBC provides a thermal path with low thermal resistance between the thermal source and the thermal sink; i.e., the semiconductor package and air.

A sample of the proposed module has verified that it suppresses the thermal resistance to 60% of that of its conventional printed circuit board (PCB) counterpart. The slopes of the blue and red curves in Fig. 1 indicate the thermal resistances of the proposed and conventional PCB. The proposed concept is applied to the 2-kW boost converter, of which a circuit diagram is shown in Fig. 2. Components in the dotted box in Fig. 2 are soldered on the DBC of the thermally enhanced module by a vacuum reflow process, as shown in Fig. 3(a), and the module is attached and wired by copper wires and ribbons, as shown in Fig. 3(b).

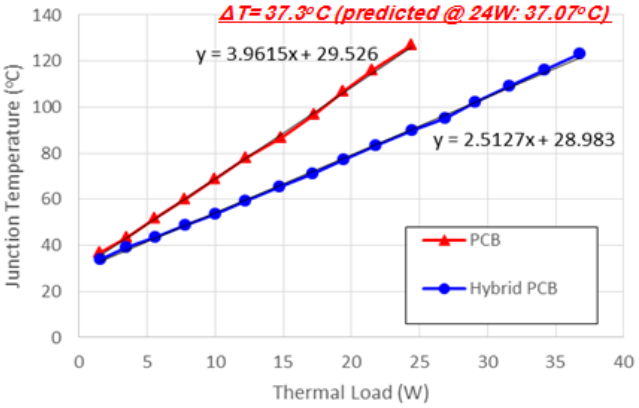


Fig. 1. Device temperature comparison between the PCB and proposed module

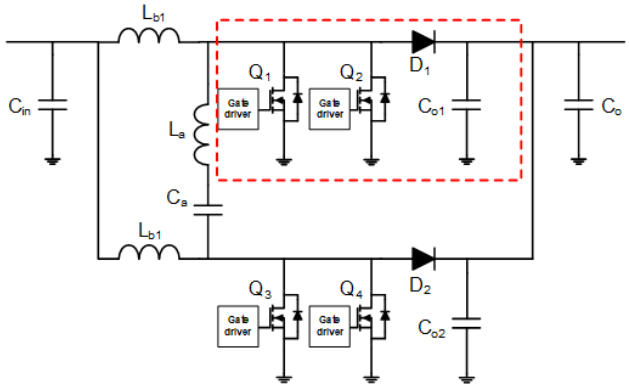
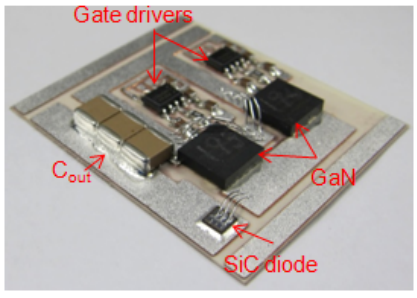
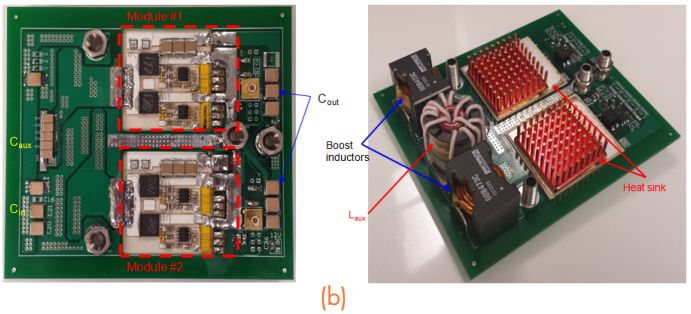


Fig.2. 2-kW boost converter configuration. Components in the box are on the DBC of the thermally enhanced module



(a)



(b)

Fig.3. (a) The proposed thermally enhanced switching module and (b) its attachment to PCB

Thermal Stability of Al_2O_3-Filled Silicone-Based Elastomers for Power Electronic Encapsulation

Silicones are widely used for encapsulating power electronic modules due to their high dielectric strength and thermal stability. However, silicones are found to be insufficiently stable at ≥250°C, which is the maximum junction temperature of commercial SiC devices. In this study, the thermal stability of pure silicone and its Al_2O_3 fiber-filled composites were investigated by thermogravimetric analysis (TGA) and isothermal (250°C) soak tests. Both tests revealed that Al_2O_3 fiber improved the thermal stability of silicone (Fig. 1). TGA results indicate that the temperature of degradation onset increased from 330°C to 379°C with a fiber loading of 30 wt%. In the isothermal soak test, pure and 30 wt%-filled silicones lost 10% of polymer weight in 700 and 1,800 hours, respectively. Improved thermal stability was explained by a restrained chain mobility caused by hydrogen bonds formed between the Al_2O_3 surface and the polymer matrix. Removal of hydrogen bonds impaired thermal stability, increasing the initial weight-loss rate from 0.025 to 0.036 wt%/hour.

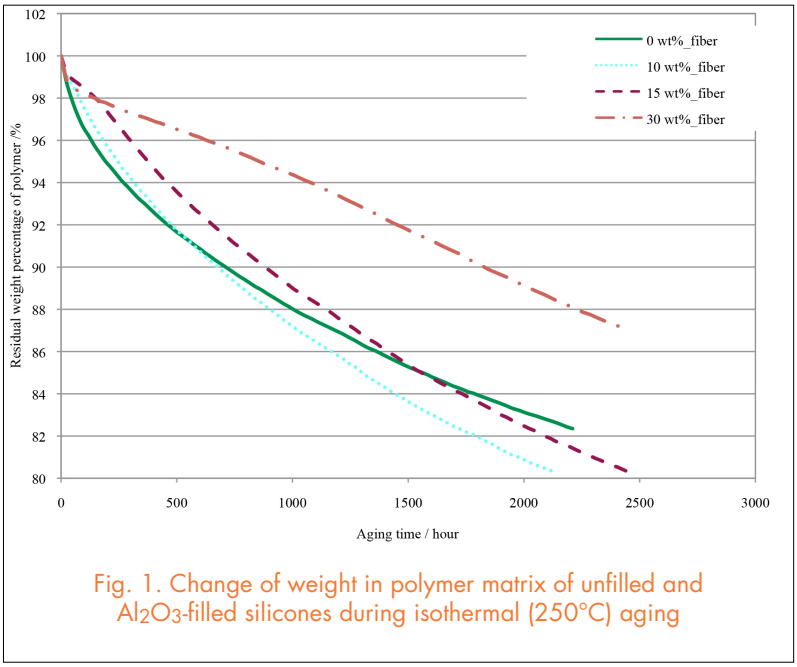


Fig. 1. Change of weight in polymer matrix of unfilled and Al_2O_3-filled silicones during isothermal (250°C) aging

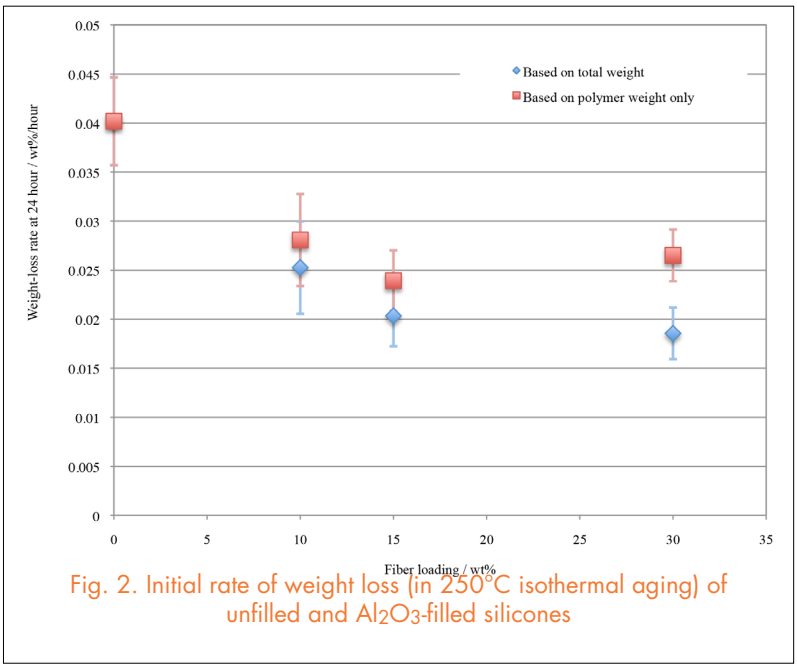


Fig. 2. Initial rate of weight loss (in 250°C isothermal aging) of unfilled and Al_2O_3-filled silicones

A Frequency-Domain Study on the Effect of DC-Link Decoupling Capacitors

DC-link decoupling capacitors are generally placed near the power switches in the converter to minimize the parasitic ringing and voltage overshoot on the devices. We have studied the influence of decoupling capacitors on the turn-off parasitic ringing of power MOSFETs in the frequency domain based on a small-signal modeling approach. This new angle helps explain the effect of these capacitors in a simpler and more straightforward way than the traditional time-domain analysis, and provides a deeper insight into the problem. A rule of thumb about the selection of effective decoupling capacitance value can also be derived from this study.

Fig. 1 shows the small-signal model with the decoupling capacitance. It is assumed that L_{DS} represents the minimum possible stray inductance associated with the device packages and the shortest necessary interconnections to access the decoupling capacitance C_{Dec}. The interconnection between the voltage source and the power stage, such as the DC bus bar, will then introduce an additional stray inductance L_1. Generally, C_{Dec} needs to be placed as near as possible to the power stage to minimize L_{DS}, and 50 to 100 times C_{OSS} is a sufficient value for C_{Dec} to achieve the decoupling effect. Further increasing C_{Dec} will not help improve the ringing caused by L_{DS} and C_{OSS}, which is determined by the packaging technology (e.g. the parasitics inside a power module) and the device characteristics. When fully decoupled, L_1 will not affect the high-frequency ringing, but will generate another resonant peak with C_{Dec} located at $1/\sqrt{(L_1 C_{Dec})}$ and cause low-frequency oscillation.

Fig. 2(a) shows the double-pulse circuit used to study the effects of parasitics. Fig. 2(b) shows the impedance measurement results at four discrete values of C_{Dec}, which is consistent with the turn-off waveforms of the MOSFET.

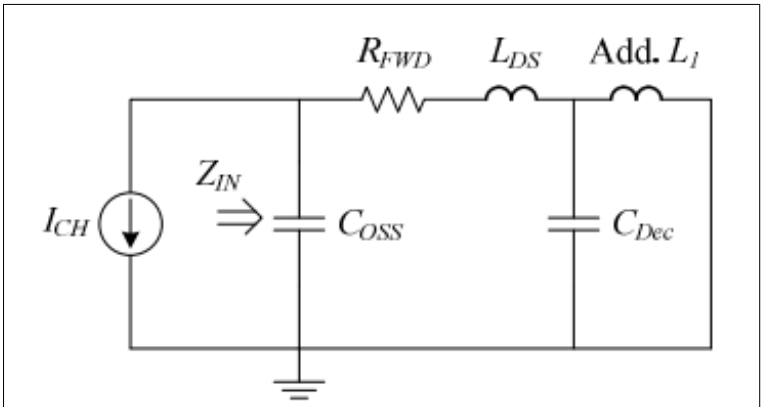


Fig. 1. Small-signal model with the decoupling capacitance

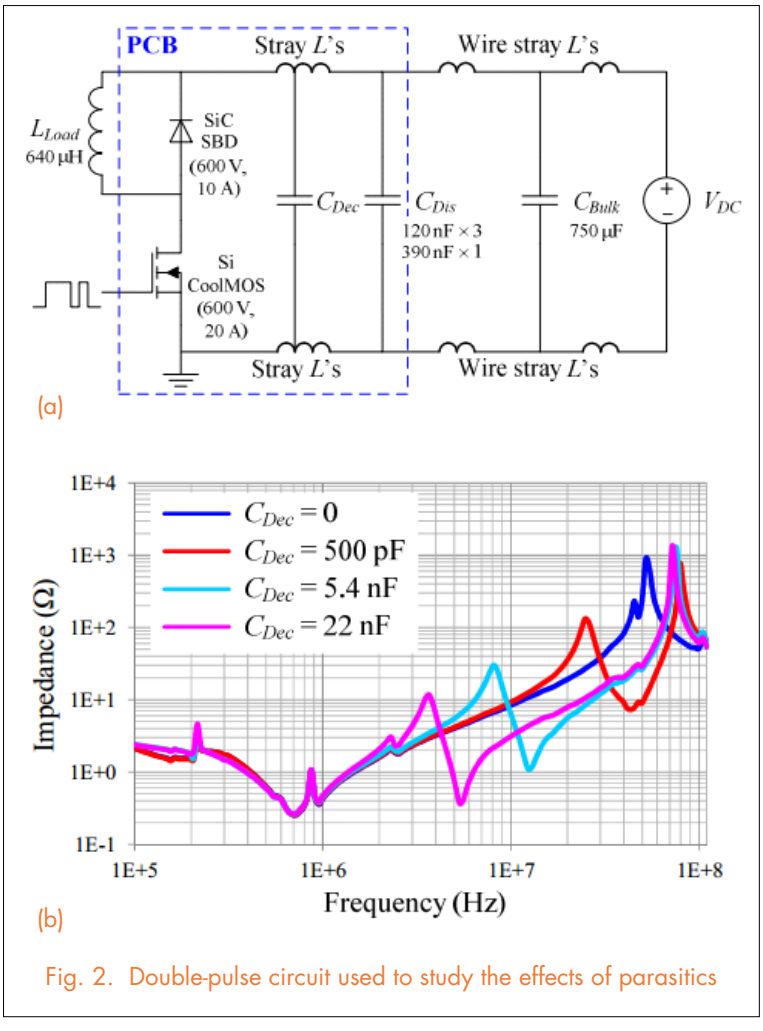
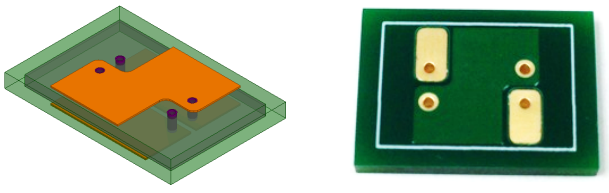


Fig. 2. Double-pulse circuit used to study the effects of parasitics

High-Frequency Integrated Point of Load (POL) Module with PCB Embedded Inductor Substrate

The large thickness of the conventional discrete magnetic component is often the bottleneck for the media and high current POL converter achieving high power density. The low-profile LTCC inductor can work as the substrate of the 3D integrated POL module to improve power density. However, the ceramic-based integration is not cost effective, because high-temperature sintering and complicated assembling processes are involved. This work justifies the feasibility of using SENFOLIAGE (SF) alloy flake composite for the high-frequency PCB integrated POL module. SENFOLIAGE is a composition of alloy flake and epoxy developed by NEC-Tokin. Compared with the traditional flake composite, the permeability and core loss of SENFOLIAGE are improved prominently by doing some lateral alignment of the flake and increasing the volume ratio of the alloy. The compatibility of the flake material with conventional PCB manufacturing technique has been studied, and the layer-wise magnetic core is sandwiched into the multi-layer PCB using the PCB laminating technique, after which the key properties of the SF flake core are kept almost the same. The winding of the inductor is built by the copper layers and conventional PCB vias. Fig. 1 illustrates the conceptual drawing and a prototype of a two-turn low-profile PCB embedded inductor substrate.

As a demonstration of system integration, a 20A, MHz integrated POL module is designed and fabricated based on a 4-layer PCB substrate with an embedded inductor, which achieves more than 85% efficiency and 600W/in$_3$ power density. The laminating structure is shown in Fig. 2. The bottom two layers of copper are used to build the winding of the inductor. The top layer of copper provides the connection between the other components of the converter. The second layer of copper is a shield, which alleviates EMI and minimize the parasitics of the active layer. Fig. 3 shows the PCB integrated POL module with and without mounted FETs and capacitors. The POL module survives after hundreds of thermal cycles, which validates the reliability and compatibility of the flake magnetic material with PCB integration. In addition, the application of the standard PCB process reduces the cost for manufacturing these integrated modules due to the easy automation and low-temperature process.



(a) Conceptual drawing (b) Prototype

Fig. 1. Low-profile inductor substrate based on 2-layer PCB

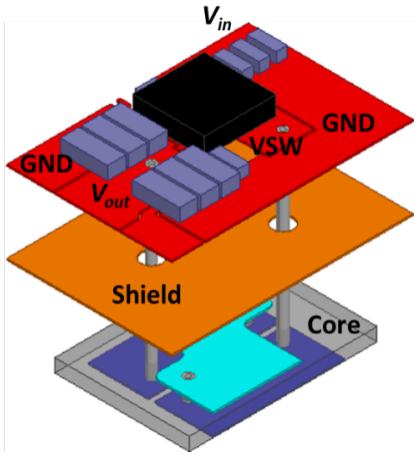


Fig. 2. Laminating structure of integrated POL module based on 4-layer PCB

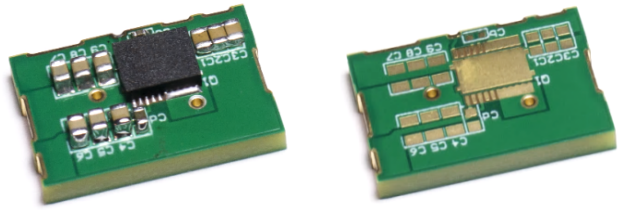


Fig. 3. 3D integrated POL module with PCB embedded inductor substrate

Chip-Bonding on Copper by Pressure-Less Sintering of Nanosilver Paste Under Controlled Atmosphere

POWER electronics devices have experienced significant increases in performance in the last decade. Silicon-based devices continue to improve, while wide-bandgap devices, such as silicon carbide (SiC) and gallium nitride (GaN), are becoming more available. The advances in device power density will ultimately lead to packaged devices, whose operating temperatures may exceed 200° C. Innovations in packaging materials and integration are required for meeting the demands of high temperature operations.

Nanosilver enabled Low temperature joining technique (LTJT) is a promising die-attach technique, which possesses much higher thermal and electrical conductivities, higher melting temperatures, and lower processing temperatures. It is the goal of this research to extend the nanosilver paste die attachment to bonding bare copper surfaces in an effort to lower manufacturing cost and time by removing the required metallization of substrates.

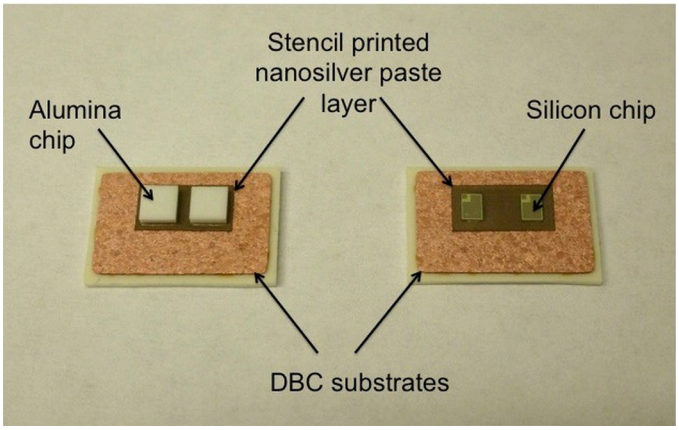


Fig. 1 Chip-paste-substrate assemblies before sintering.

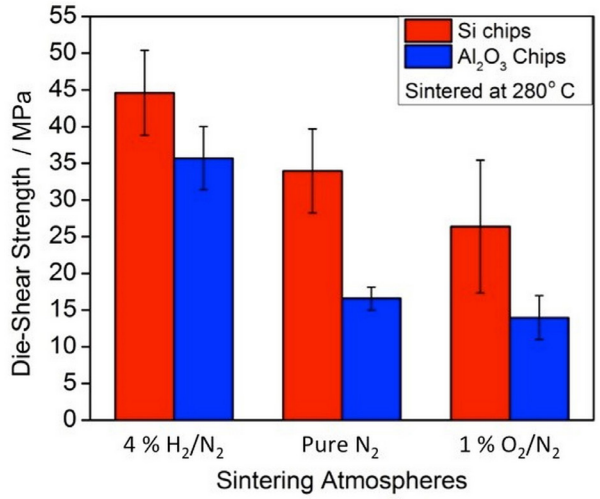


Fig. 2. Die-shear strength of joints sintered at 280° C

A bare copper surface oxidizes at the sintering temperature of nanosilver, i.e. 260° C. If a dense oxide layer forms on the copper surface before the sintering of nanosilver particles, the oxide can prevent adequate bonding between the copper and sintered silver, thus resulting in a very low bonding strength of the sintered joint (< 5 MPa). However, the organics in the nanosilver paste need to be removed during the process, usually by combustion with the oxygen in the air. Thus, oxygen plays conflicting roles during the sintering process. . In order to achieve a high bonding strength (> 30 MPa) by pressureless sintering at a temperature lower than 300° C, two strategies are presented: (1) The oxygen partial pressure (P_{O2}) was reduced to lower than 0.01 atm in order to suppress copper oxidation, while still providing sufficient oxygen for removing the binders in the paste; (2) apply an inert or reducing atmosphere – pure N_2 or pure N_2 with 4 vol% H_2, in an effort to completely avoid copper oxidation. Die-shear tests are performed on the samples sintered under both conditions. The failure surfaces from the die-shear test samples as well as the microstructures of the sintered silver under each atmosphere were characterized by optical and electronic microscopy.

Thermal Characterization of Planar High Temperature Power Module Packages with Sintered Nanosilver Interconnection

Many new innovations have emerged in the power electronics industry to aid in meeting the expanded market demand. Interest in high temperature and high power applications has fueled new developments in wide bandgap semiconductor devices, such as GaN and SiC, which are capable of operating above 200°C. However, silicon devices are still prevalent in the marketplace and offer significant power ratings at affordable prices. For this reason alone, silicon devices will continue to be a mainstay in high power electronics systems. The key to offering functional and reliable silicon packages that can endure higher temperatures is through innovative thermal management and packaging. Effective thermal management of packaged devices can be accomplished through materials selection, design or a combination of the two.

In this paper, we outline the fabrication of functional double sided power module switching unit utilizing LTJT sintered silver for each interface. This symmetrical structure replaces the low thermally conductive encapsulation, normally used above attached devices, with an additional substrate which should theoretically half the package thermal resistance. Thermal resistance measurements and techniques for single sided power module packages are well documented and used extensively by module manufacturers. However, a three dimensional structure which allows for heat transfer through both the top and bottom substrates presents a new challenge for characterization.

In this paper, the thermal characteristics of a functional double sided power module were measured in all possible cooling scenarios. These measurements utilized a dual interface thermal insulating material (TIM) technique developed by MentorGraphics. The resulting improvements in thermal resistance of the sintered silver power module package and constructed thermal simulation models will be discussed for each cooling configuration.

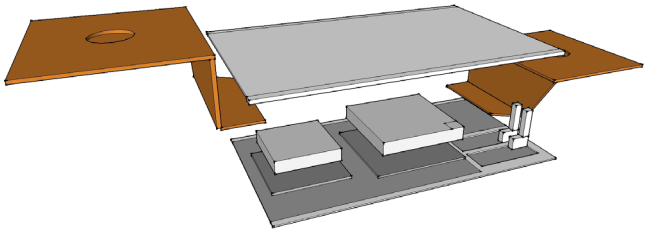


Figure 1: Double sided power module package design for use with sintered silver device attachment

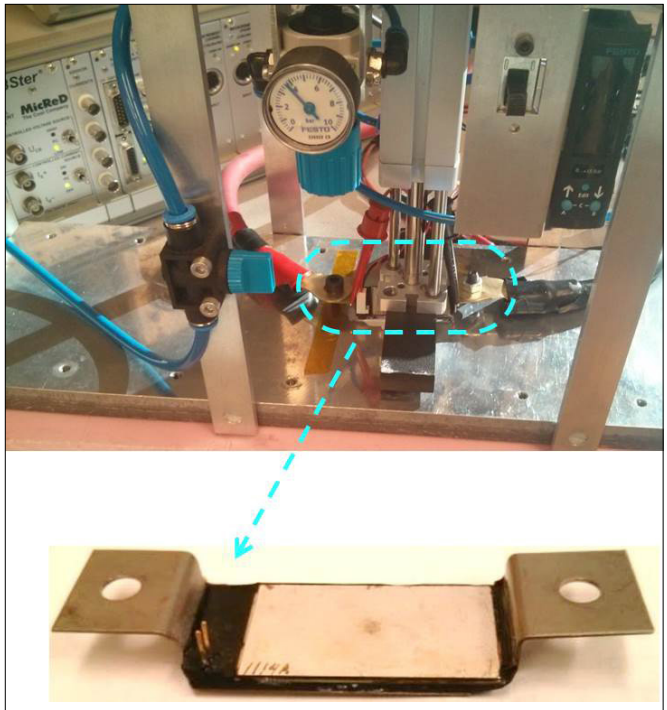


Figure 2: JEDEC JESD51-14 Test fixture for use with MentorGraphics T3Ster system.

A Novel Hybrid Packaging Structure for High-Temperature SiC Power Modules

We have developed a novel hybrid packaging structure for high-temperature SiC power modules that combines the benefits of both the wirebond structure and the planar structure. With the resulting hybrid structure, the power modules can achieve the same footprint and similar parasitics to regular planar structures, but with a much easier fabrication process and more reliable top-side interconnections. A three-phase multiple-chip prototype module has been built based on a SiC JFET, and tested with a 250 °C junction temperature. Detailed comparisons conducted between the hybrid, planar, and wirebond structures reveal better performance of the hybrid structure with smaller parasitics than the wirebond structure, and easier fabrication, more reliable top-side connection, and more flexible die-attachment material selection than the planar structure.

Fig. 1 shows the fabrication process with a single SiC JFET. The processing time is two hours less than that of the planar structure. In addition, the planar packaging structure employs a three-step sintering process, and each process temperature be at least 40°C lower than the previous one to prevent it from melting. This makes it difficult to select the die-attachment materials. However, since there is only one sintering process in the hybrid packaging structure, more flexible die-attach material selection is possible. The fabricated power module is shown in Fig. 2. There are three input power lead frames (A, B, and C), two output power lead frames (P and N), and two gate-drive lead frames (G and S). The lead frames are fabricated separately with a DBC substrate.

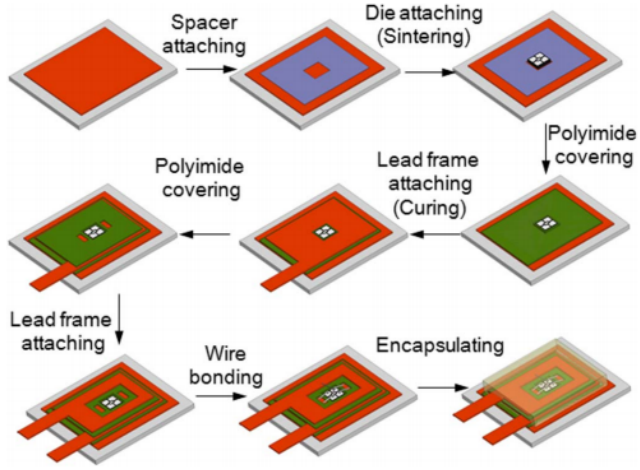


Fig. 1. Hybrid-structure packaging fabrication process

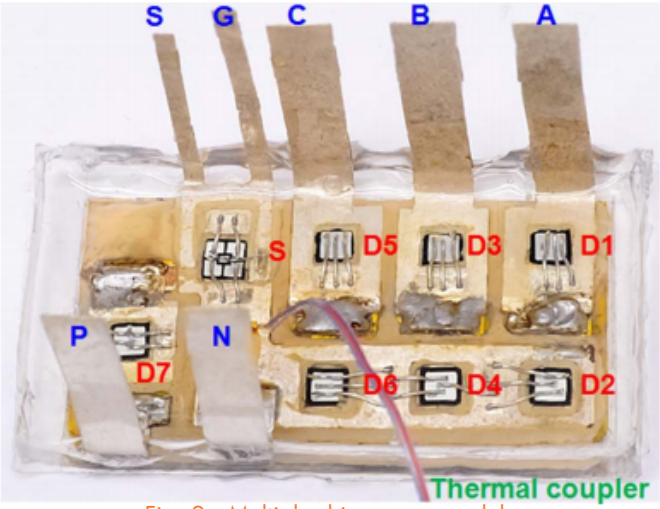


Fig. 2. Multiple-chip power module

Comparison of Critical Conduction Mode, Trianjular Conduction Mode and Fixed Frequenty Modulation Schemes for Single Phase H-Bridge Boost PFC

To implement a power conversion system (PCS) or energy control center (ECC) for medium-voltage, medium-power aerospace applications with a single phase H-bridge PFC, three control methods were implemented, and their efficiency was calculated based on the converter model with consideration of the common-source inductance. The most common modulation scheme used is the critical conduction mode (CRM), in which the on-time of the main switch is kept constant, the inductor current reaches a peak value, then the inductor current is brought back to zero and then the main switch is turned on again.

The structure of the H-Bridge PFC and its equivalent circuit when input voltage is positive is shown in Fig.1. The two switches of one leg operate at the mains frequency and the switches of the other leg operate at high frequency.

The current in the inductor is brought to zero, as shown in CRM in Fig. 2. However, this allows ZVS turn-on of the main switch only when vin<Vdc/2. While in triangular conduction mode (TCM), the current is brought to a negative value, which makes ZVS possible for the entire mains cycle, as shown in Figs. 2 and 3.

Thus TCM reduces the turn-on losses of the main switch, but it results in higher turn-off losses for the auxiliary switch. Both CRM and TCM have the drawback of variable switching frequency. However, TCM can be modified to obtain a fixed-frequency PWM switching by choosing a particular duty ratio.

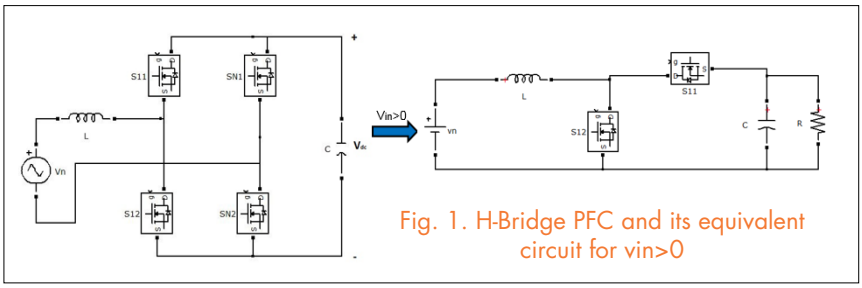


Fig. 1. H-Bridge PFC and its equivalent circuit for vin>0

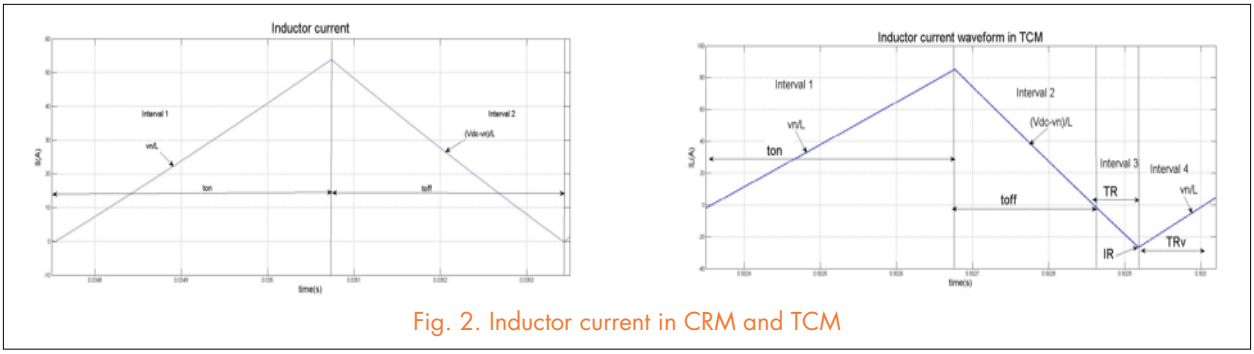


Fig. 2. Inductor current in CRM and TCM

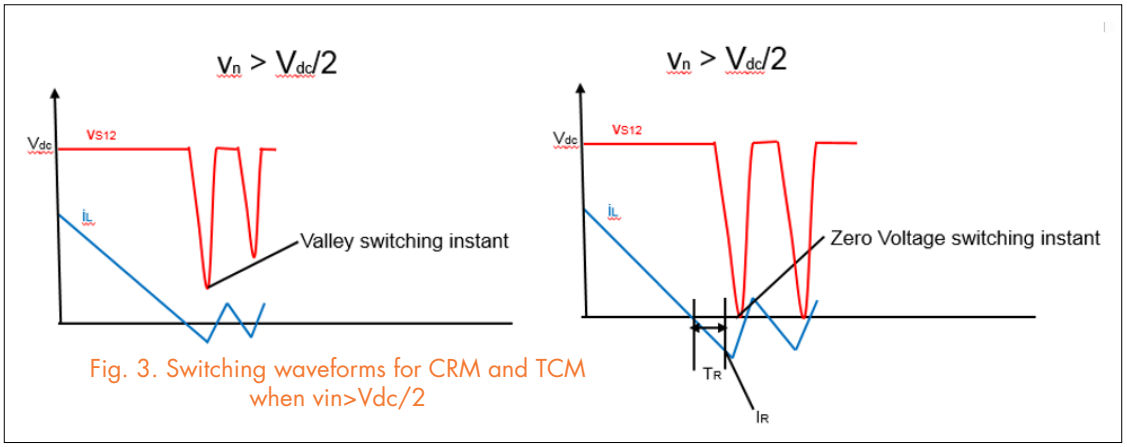


Fig. 3. Switching waveforms for CRM and TCM when vin>Vdc/2

Renewable Energy & Nanogrids Nuggets

Coupled Inductor in Interleaved Multiphase Three-level DC-DC Converters for High Power Energy Storage Applications

Energy Management System Control and Experiment for Future Home
Part 1 – 380V DC Testbed
Part 2 - System-Level Control and Experiment

Power-Cell Switching-Cycle Capacitor Voltage Control for Modular Multilevel Converters

Control Loop Design of a Two-stage Bidirectional AC/DC Converter for Renewable Energy Systems

Synchronous Generator-based Grid-interface Converter for Energy Storage Systems Integration

Analysis of Nonlinear Sideband Effects in Small-signal Input dq Admittance of Twelve-pulse Diode Rectifiers

Modeling the Output-Impedance Negative Incremental Resistance Behavior of Grid-Tied Inverters

Impedance-Based Analysis of Active Frequency Drift Islanding Detection Method for Grid-Tied Inverter System

Space Vector Modulation for 3-level NPC Converter with Neutral Voltage Balancing and Switching Loss/Noise Reduction

Investigation and Comparison of Cascaded H-bridge and Modular Multilevel Converter topologies for Medium Voltage Drive Applications

Evaluation and Control Design of Virtual-Synchronous-Machine-Based STATCOM for Grids with High Penetration of Renewable Energy

State-Space Switching Model of Modular Multilevel Converters

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Coupled Inductor in Interleaved Multiphase Three-Level DC-DC Converters for High Power Energy Storage Applications

A high efficiency and compact energy storage system is very important for renewable energy applications. This paper investigates and evaluates the coupled inductor in interleaved multiphase three-level DC-DC converters for high power energy storage applications.

An interleaved two phase three-level DC-DC converters circuit topology is shown in Fig.1. Two inverse-coupled inductors are employed as the interface between the phase legs and common output capacitors. If a non-coupled inductor is used to maintain the inductance of the inductor, the interleaving operation between the two phases will increase the inductor current ripple while the overall current ripple and Common Mode voltage will be reduced, which makes the input and output capacitors as well as CM filter smaller.

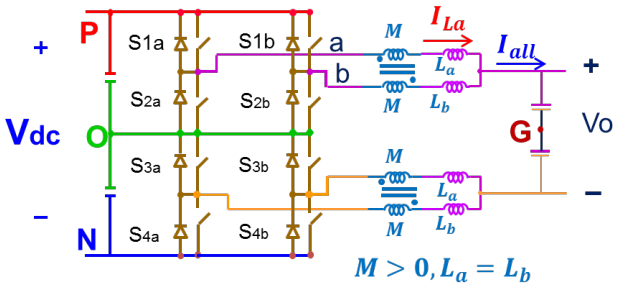


Fig. 1. A two phase paralleled three-level DC-DC converter

To reduce the inductor current ripple, a coupled inductor is employed to reduce the size of inductor. By adding a coupled inductor, an inductor current ripple can be reduced as shown in Fig.2. The maximal inductor current ripple can be much smaller than non-interleaving operation mode. By interleaving operation, output current ripple and CM voltage can also be reduced as shown in Fig.2. Therefore, by adding a coupled inductor and interleaving, it is possible to achieve a smaller inductor current ripple, smaller input and output capacitors, as well as a smaller CM filter simultaneously.

For interleaved multiphase three-level DC-DC converters, multiphase inverse-coupled inductors are needed, and overall current ripple and CM voltage will be further reduced when compared with the interleaved two phase case.

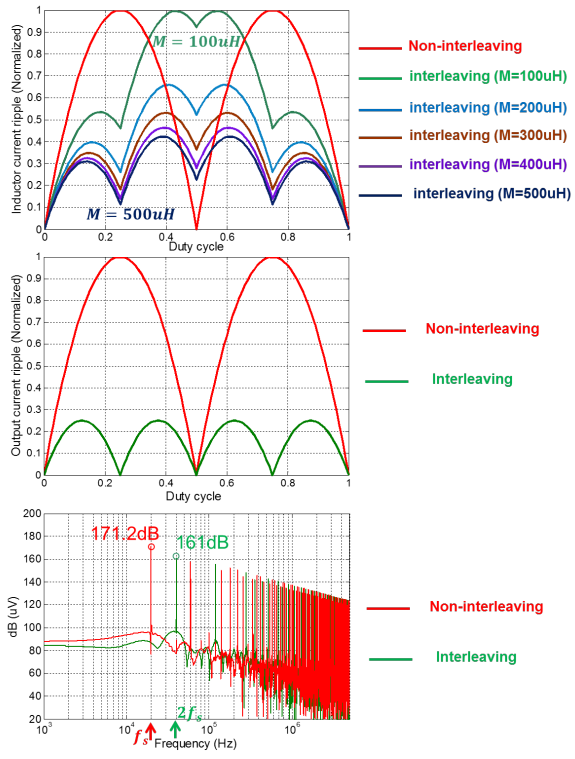
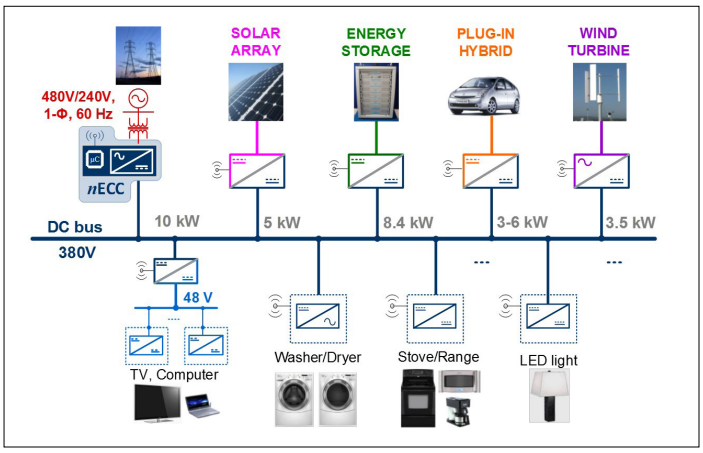
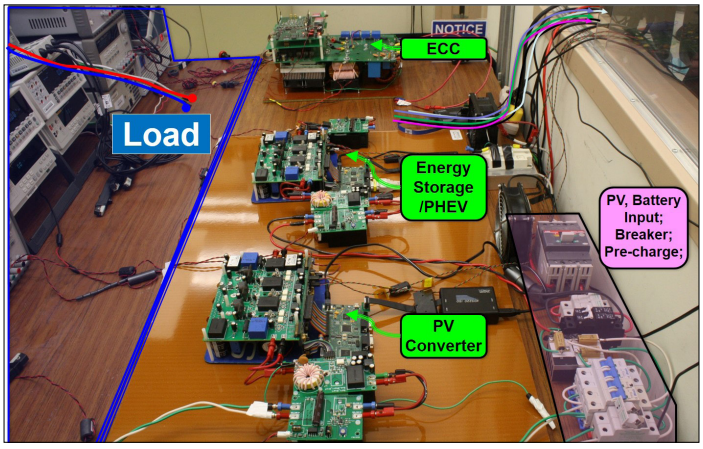


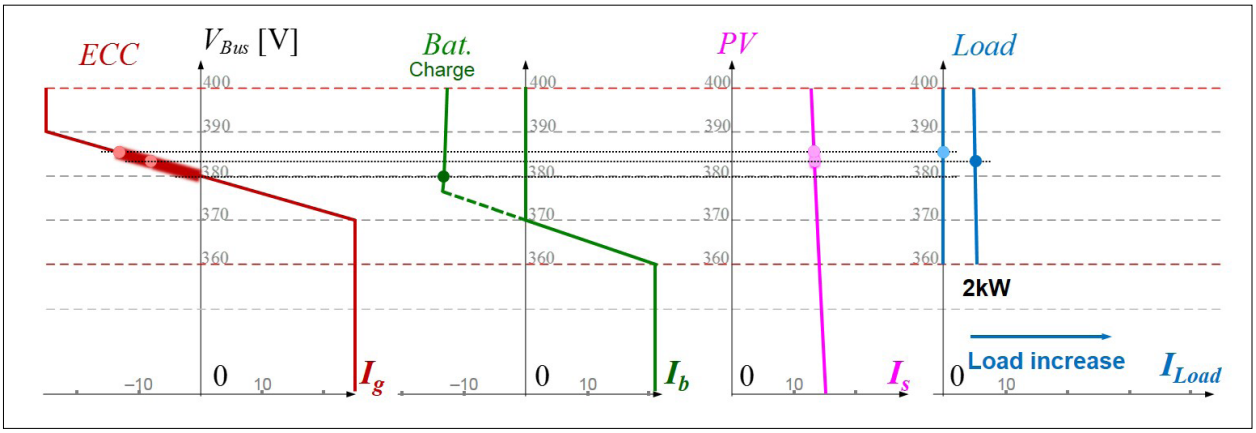
Fig. 2. Inductor current ripple, output current ripple and CM voltage spectrum

Energy Management System Control and Experiment for Future Home
Part 1 – 380V DC Testbed
Part 2 - System-level Control and Experiment

To enable zero net-energy consumption and optimal power management for future homes or buildings, the dc electric distribution systems (dc nano-grid) finds feasibility and simplicity for integrating multi-type renewable energy sources and energy storage elements. This paper introduces a 380V emulator testbed of 10~15kW, with integration of solar, wind, Li-ion energy storage, plug-in hybrid electric vehicles and smart appliance, to demonstrate the future home. Operation analysis and control laws for each source components are defined. Energy storage management and its control law in dc nano-rid is proposed. System level energy management control strategies in a day/24 hours are examined and discussed with considerations of residential load demand profile, local renewable energy source profile and schedules of electricity rate. Key scenarios of system level experiments are given for verification purposes.







Power-Cell Switching-Cycle Capacitor Voltage Control for Modular Multilevel Converters

The Modular Multilevel Converter (MMC), as shown in Fig. 1, has been increasingly considered for medium voltage and high voltage variable frequency applications due to its favorable features of high modularity and scalability. The conventional operation mode of the MMC requires the capacitors in power modules to absorb the power fluctuations at line frequency and second order harmonic frequency. This inherently results in a very large capacitance, in addition to the fact that the capacitor voltage ripple magnitude is inversely proportional to the phase current frequency and will become infinite at zero frequency (DC). This is a big issue when starting motors, for instance, since the phase current frequency is required to start from zero. In this paper the proposed SCC shifts the arm current towards the switching frequency to reduce the required capacitance value and to enable the converter operation at very low frequency and DC.

The SCC is described as shown in Fig. 1. In the case where the phase current is positive, the state ③ is applied right before state ① to control the lower arm current to an offset value such that in the time duration of the state ③ the average current flowing through the lower capacitor is controlled back to zero. Similarlty, the SCC arranges the state ④ right before state ② to control the upper arm current to an offset value such that in the time duration of the state ② the average current flowing through the upper capacitor is controlled toward zero. This method can be easily extended to the situation when the phase current is negative, which will be elaborated in the full paper.

The simulation waveforms of the single-module-per-arm are shown in Fig. 2, where a 13% p.u. capacitance and a 0.22% arm inductance are used to achieve a 2% capacitor voltage ripple with switching frequency at 1.98 kHz, compared to the implementation with the conventional control approach in which at least 100% p.u. capacitance and 22% arm inductance are required to achieve the same goal. The simulations with more module counts at variable line frequencies will be shown in the full paper, and the semiconductor loss will be estimated and compared to conventional control approaches as well.

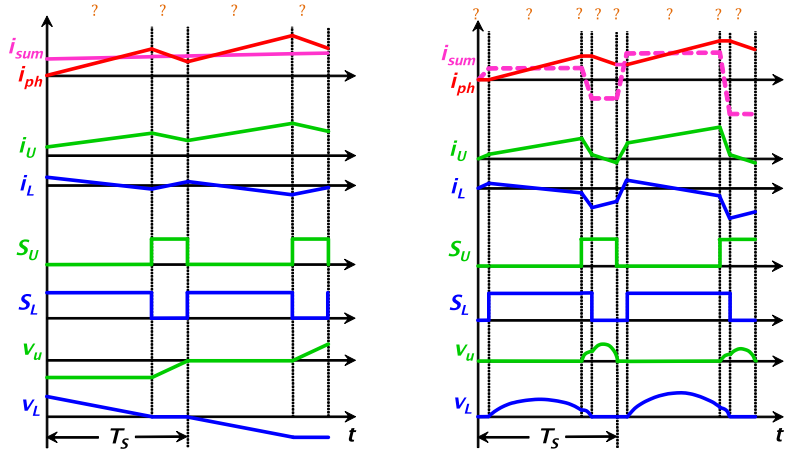


Fig. 1: Comparison between conventional control and SCC

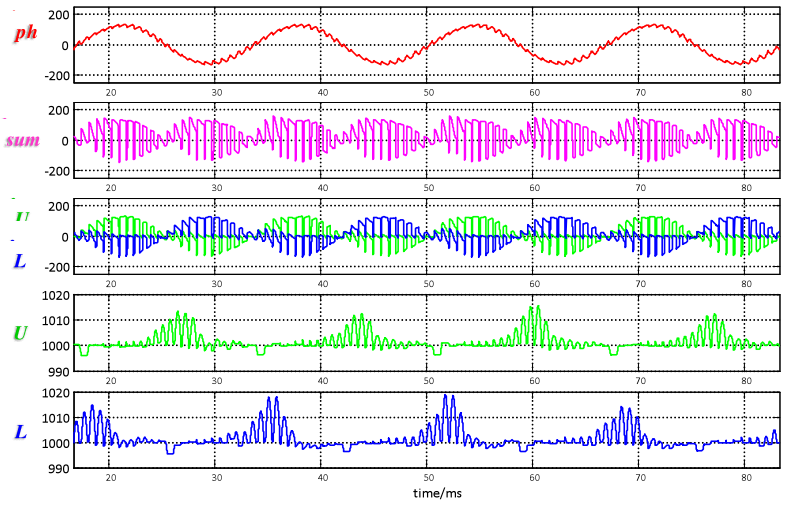


Fig. 2: Simulation waveform

Control Loop Design of a Two-Stage Bidirectional AC/DC Converter for Renewable Energy Systems

The full-bridge topology is widely used as a simple solution to transfer energy between the ac grid and the dc renewable energy system. However, it needs a large output capacitor and lacks the capability of short circuit protection. A two-stage topology consisting of an ac/dc stage and a dc/dc stage with a dc-link capacitor placed between them can reduce the dc-link capacitor dramatically and the dc/dc stage can limit the short circuit current if a proper topology is used.

In this paper, a unified control system is discussed for the two-stage converter to work in both rectifier and regenerative mode. Since the power stage consists of an ac/dc stage and a dc/dc stage with a dc-link capacitor placed between them, the corresponding controller design can be divided into two parts: the ac/dc stage controller and the dc/dc stage controller. The proposed bidirectional digital control system is shown in Fig. 1. Basically, the controller for the ac/dc stage is used to achieve a high power factor and loosely regulate the dc-link voltage at a high voltage (500 V). The controller for the dc/dc stage is used to regulate the dc output voltage with small ripple.

With the proposed controller, the converter can operate at these two modes and switch between them seamlessly. A 10 kW prototype is used to verify the performance. The output voltage is regulated accurately at 380 V with only 2.5 V peak to peak voltage ripple.

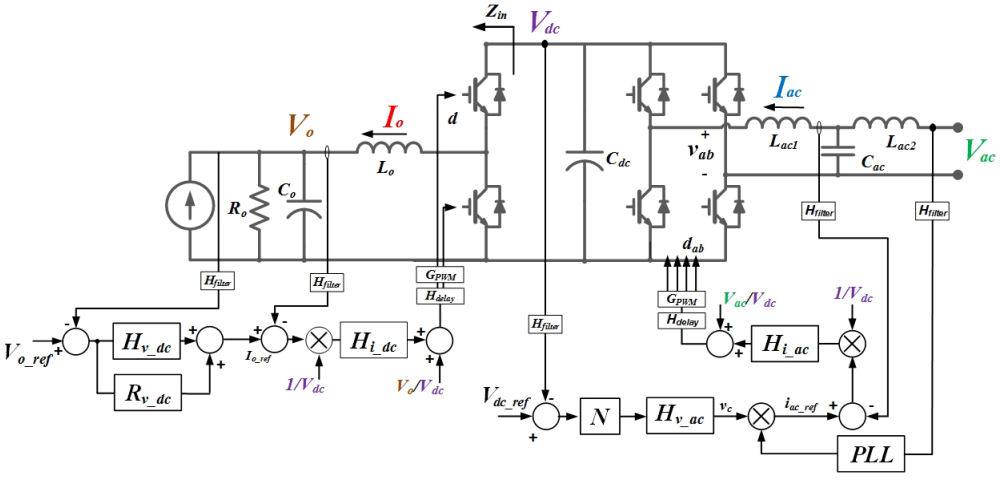


Figure 1: Bidirectional control structure.

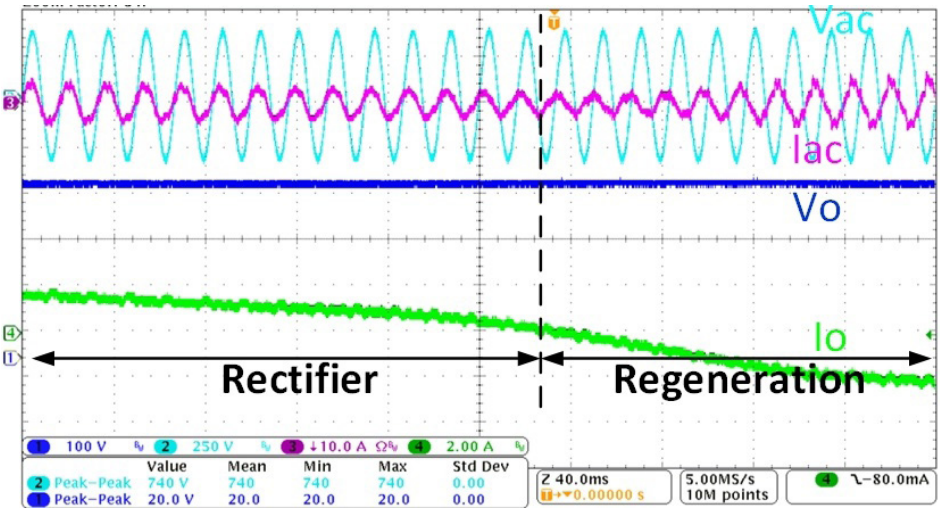


Figure 2: Mode transition test. Vac (light blue) [250V/DIV], Iac (purple) [10A/DIV], Vo (blue) [100V/DIV], Io (green) [2A/DIV].

Synchronous Generator-based Grid-interface Converter for Energy Storage Systems Integration

The common, and with some exceptions the only method to interconnect high power renewable energy sources and energy storage systems to the grid has been using power electronics converters that operate as current sources to the grid for the purpose of achieving the maximum primary-source power tracking. When the grid is not available, such sources would not be allowed to continue operating and will be shut-down after anti-islanded algorithms recognize the loss of the grid. Although existing standards and requirements still limit grid-interface converters to regulate voltage in the grid, this functionality will inevitably be the part of the power system operation in the future. This paper addresses physical and mathematical equivalency between power electronics converters and synchronous generators, and emphasizes how an inherent synchronization feature of the synchronous generators can be used to improve the performance of the grid-interface converters. It has also been shown that if operated as a voltage source, a grid-interface converter could have a significant stabilizing effect on the system dynamics due to the non-delayed power delivery.

Distributed generation was the rule rather than exception in the early days of electric energy production. Rapid commercialization of the renewable energy sources has resulted in an increased deployment of low, medium and high power distributed generation sources, as well as energy storage (ES) systems. Invariably, renewable DG and ES sources are interfaced to the grid with the assistance of power electronics converters. Fast, digitally controlled converters offer endless possibilities for the most optimal utilization of renewable resources. Moreover, power electronics-based DG can enhance power system controllability due to the fast dynamic response to the power system disturbances and deviations of the voltage and frequency. However, grid-interface converter's phase-locked loops can cause frequency instability in the case when grid output impedance becomes very high, or when there are multiple grid-interface converters connected on the same or adjacent bus with a "weak" link to the strong grid. On the other hand, thousands of synchronous generators work in parallel and share the power with much "milder" interactions in the sense of synchronizing to the grid and to each other. Thus, this paper addresses that issue by showing what features of the synchronous generators operation offer dynamic advantages that could be used in the future for the control of the next generation of grid-interface converters.

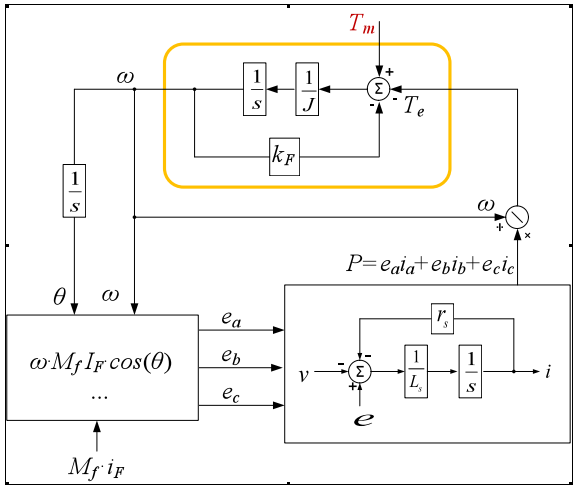


Fig. 1. Synchronous generator block-diagram model

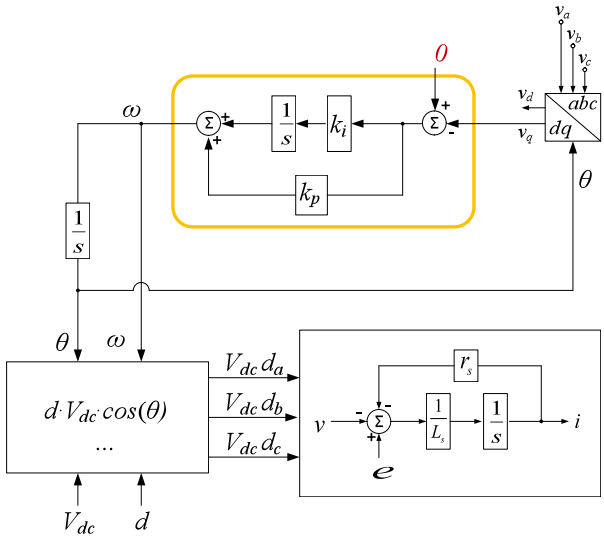


Fig. 2. . Block diagram model of the grid-interface converter

Analysis of Nonlinear Sideband Effects in Small-signal Input dq Admittance of Twelve-pulse Diode Rectifiers

This paper focuses on the modeling of small-signal input dq admittance of twelve-pulse diode rectifiers. It provides a comprehensive comparison of small-signal dq admittances between a well-known averaged value model (AVM), a switching simulation model and experimental measurements of a hardware set-up. Analytical AVM (AAVM) is used in the analysis since it has been commonly used to model diode rectifiers. In order to predict small-signal dq admittance accurately, the AAVM had to be modified. The modification describes injection properties in a more natural way by considering a d-channel perturbation as magnitude modulation and by considering a q-channel perturbation as phase modulation. Analytical expressions for a dq admittance of AAVM of twelve-pulse diode rectifier feeding a resistive load are derived and presented in the paper. Furthermore, it has been found that sideband admittances around multiples of switching frequency exist in the small-signal response due to the nonlinear behavior of the rectifier. The new phenomenon is analyzed theoretically, characterized in simulations with the extraction of small-signal response from the switching simulation model and captured experimentally by the hardware measurements.

Several conclusions can be drawn from the shown comparison. The first one is that AAVM predicts admittance Ydd(s) correctly in the whole measurement frequency range, even beyond the switching frequency. The other three admittances have additional dynamics in the response that is not predicted by the averaged model. Additional dynamics are especially noticeable in admittances Ydq(s) and Yqq(s), as they represent response to the q-channel injection, which is more nonlinear. The additional resonant points show-up left and right around multiples of switching frequencies (720 Hz, 1440 Hz, 2160 Hz etc) and there are additional resonant points in the response at odd multiples of 360 Hz (360 Hz, 1080 Hz, 1800Hz etc). Such responses are typical for nonlinear systems, where injection at one frequency point yields several responses that are strongly coupled each to the other. The described behavior is explained with the fact that the q-channel injection modulates phase, thus it modulates commutation angle and yields significant sideband response around multiples of the switching frequency.

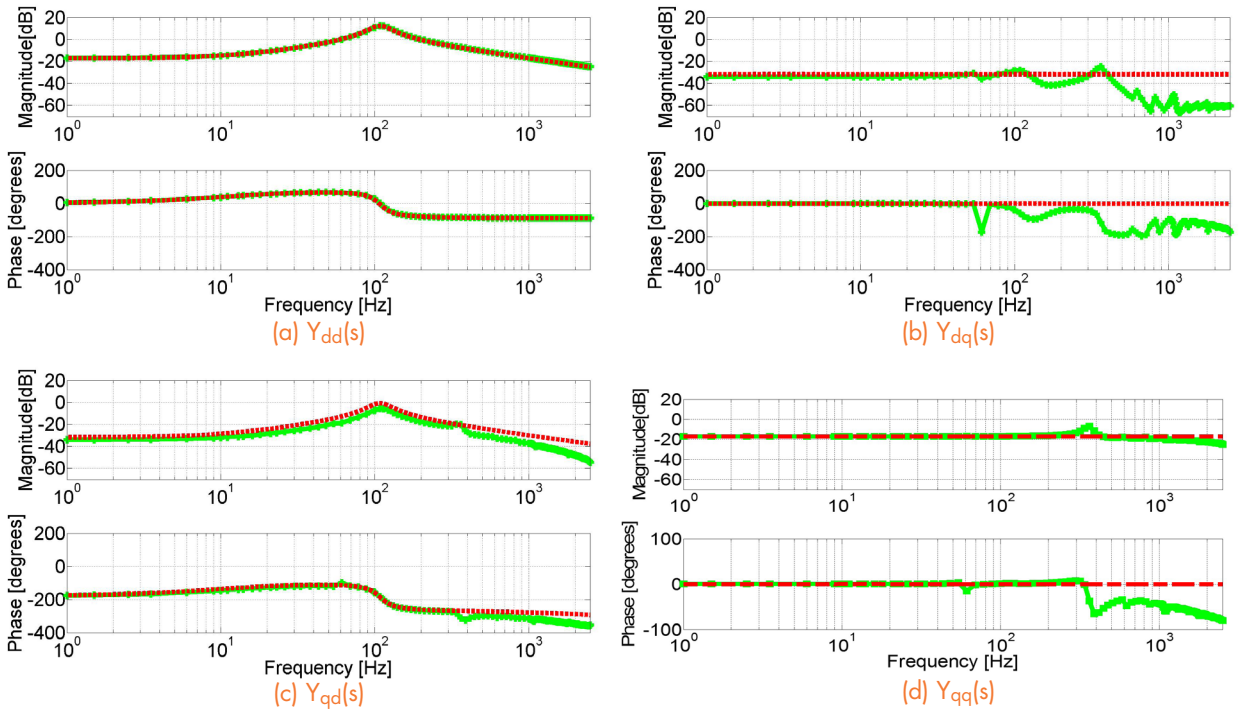


Figure 1. Small-signal input dq admittance of twelve-pulse diode rectifier: obtained from switching simulation model (green line with squares), analytical expression of modified AAVM (red dashed line)

Modeling the Output-Impedance Negative Incremental Resistance Behavior of Grid-Tied Inverters

Three-phase grid-tied inverters are widely installed in micro-grids to utilize renewable energy such as solar and wind energy. The stability issue caused by grid-tied inverters can be studied using an impedance based method. This paper models the output impedance of the grid-tied inverter shown in Fig. 1. The model shows that the output impedance of a grid-tied inverter in *dq* frame has a negative resistance feature in a *qq* channel. This is however, a result of the Phase-Locked Loop (PLL) influence on the converter dynamics, which function is to do grid synchronization. As shown in Fig. 1, perturbation from the grid voltage will propagate to the output angle of PLL, then to the duty cycle applied to the converter power stage, and finally to the output current of grid-tied inverter. PLL dynamic shapes Z_{qq} as a negative incremental resistance with in its bandwidth. Fig. 2 shows the comparison between model and measurement results. Both model and experimental results shows the negative resistance feature of Z_{qq}.

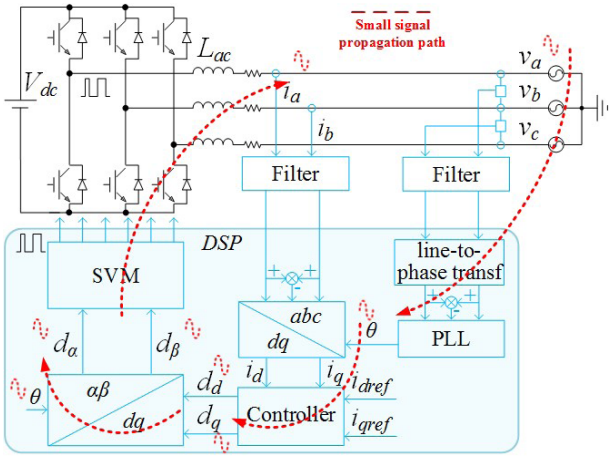


Fig. 1. Grid-tied inverter with current loop and PLL

Another interesting and important feature of Z_{qq} is that it has a right half plane (RHP) pole. The frequency of the RHP pole changes along with the PLL bandwidth and current rating of the inverter as shown in Fig. 3.

These features indicate that the grid-tied inverter is a source converter that has a negative incremental resistance. When the Nyquist stability criteria is applied and the grid-tied inverter is treated as a source converter, the number of encirclements of the critical point (-1, 0) should be equal to the number of RHP poles in the system. Alternatively, the inverse Nyquist criteria can be used since there is no right half plan zero in the system.

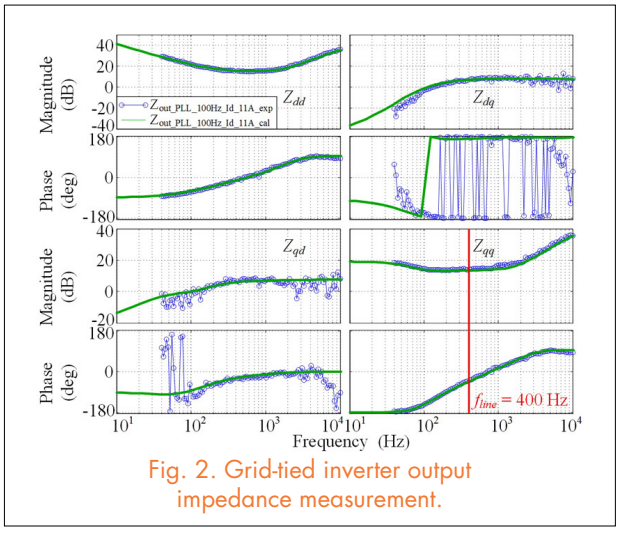


Fig. 2. Grid-tied inverter output impedance measurement.

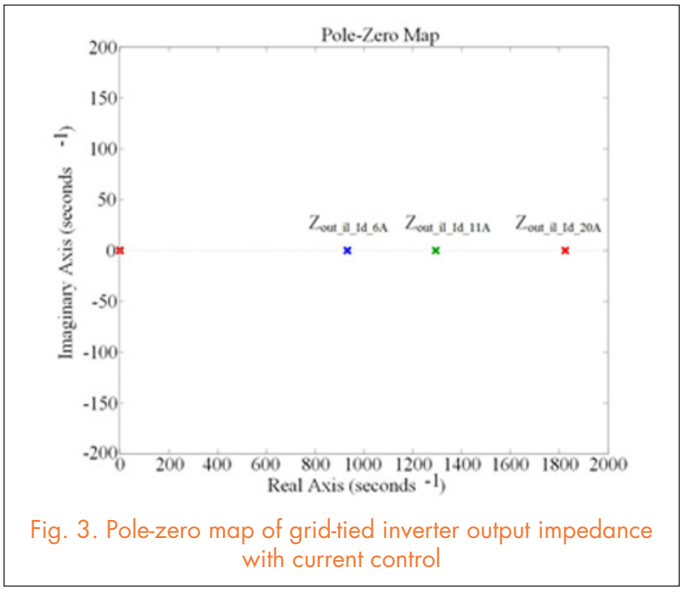


Fig. 3. Pole-zero map of grid-tied inverter output impedance with current control

Impedance-Based Analysis of Active Frequency Drift Islanding Detection Method for Grid-Tied Inverter System

Active frequency drift (AFD) methods are popular islanding detection methods, because of their simplicity, small non-detection zone, and low impact on system power quality. Most AFD methods generate a frequency positive feedback or feed forward which drives the converter system frequency away from the steady-state and detects the islanding event. Other methods are based on the analysis of PLL small-signal stability as shown in Fig. 1.

Differing from traditional analysis of the AFD method, this paper proposes an impedance-based analysis which unveils that frequency drift is the consequence of interaction between inverter output impedance and the impedance of local loads. As shown in Fig. 2, the dc impedance of the inverter is equal to the dc impedance of the local load. With feed forward gain N = 0, the phase difference is 180°; with N bigger than 0.015, the inverter output impedance drops below -180° and the system becomes unstable due to lack of phase margin. A three-phase voltage source inverter is used for experiments. Fig. 3 shows the islanding event with N = 0.015. It can be seen that the PLL output frequency starts to drift when an islanding event happens, the system is unstable.

Moreover, the impedance-based analysis also shows that the AFD method has the potential to destabilize the grid-connected inverter system when the grid is weak or the size of inverter is large. Because a grid-tied inverter features a negative incremental resistance in the *qq* channel, the AFD method makes the phase even below -180° which decreases the phase margin of the system.

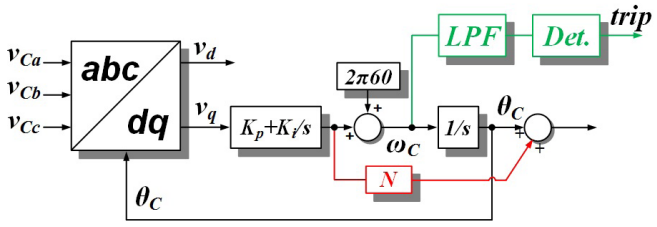


Fig. 1. PLL-based AFD islanding detection method.

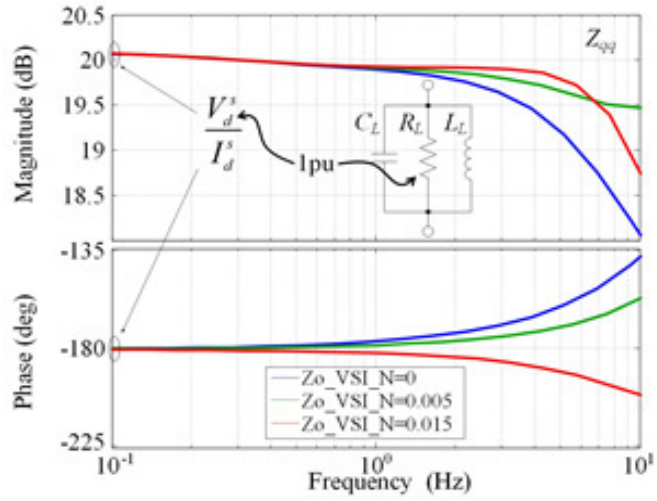


Fig. 2. Impedance interaction in qq channel between inverter and local load under islanding condition.

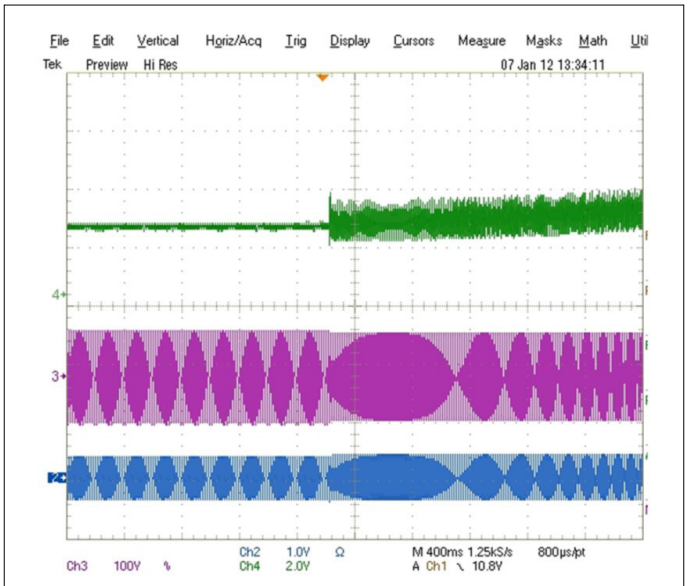


Fig. 3. PLL with feed forward gain N=0.015 when islanding event happens: terminal voltage (purple) [100 V/DIV], inverter current (blue) [20A/DIV], M (green) [5 Hz/DIV].

Space Vector Modulation for Three-level NPC Converter with Neutral Point Voltage Balance and Switching Loss Reduction

We have developed an improved space vector modulation (SVM) method to modulate the three-level, three-phase neutral point clamped (NPC) converter for renewable energy power conversion systems. The control objectives for the three-level NPC converter are loss reduction, neutral point (NP) balance and noise reduction of the SVM. A detailed loss model and simulation model are built to analyze quantitative loss and NP voltage ripple. An improved SVM method is proposed to simultaneously reduce the NP imbalance and the switching loss and noise.

The conventional NP balancing algorithms don't deal with the switching loss reduction because the redundant vector selection is based on a single objective. However, for high-power, high-frequency NPC power conversion systems, loss and noise reduction are important goals, in addition to the NP balance. Based on the existing control algorithms, a new SVM scheme is proposed to achieve multiple objectives at the same time.

The small vectors are selected so that both the NP charge and the pulse sequence are considered. As a result, minimized NP ripple and switching events are guaranteed within one switching cycle. The NP voltage is balanced, and the switching loss and noise are reduced. Moreover, the switching loss between switching cycles is also reduced by properly determining the pulse sequence order. This measure further reduces the total loss and, most importantly, makes symmetrical the phase leg loss distribution. The proposed SVM scheme maintains the same total loss and NP balance results under different power factors, and is verified by both simulation and experiment using the three-level NPC converter. The control result for NP balance and loss reduction are verified using a simulation model and an experimental prototype on 200 kVA three-level NPC converter hardware.

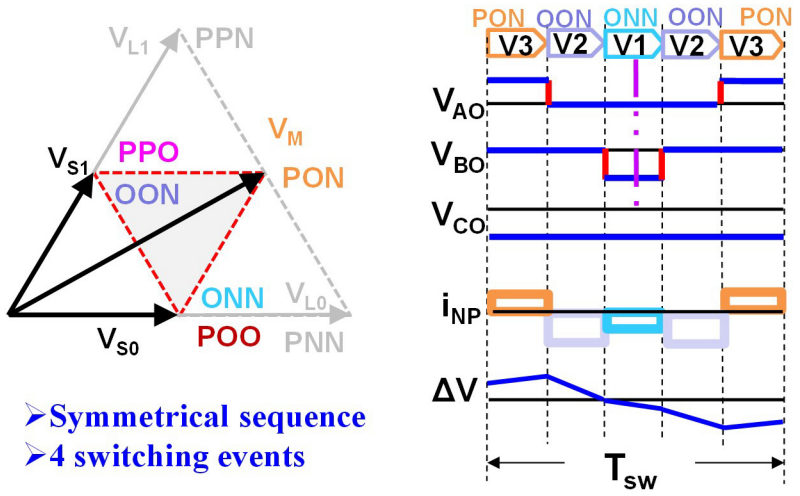


Fig. 1. Pulse sequence for the proposed SVM in one switching cycle

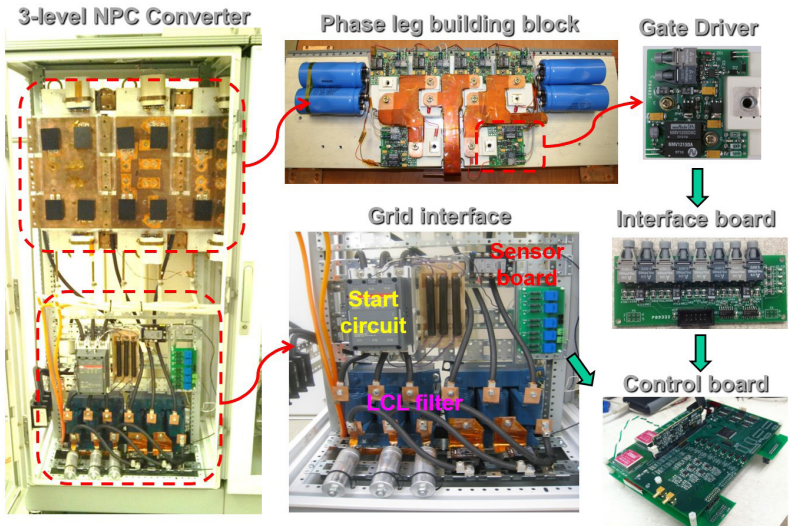


Fig. 2. System structure of the three-level, three-phase NPC power converter

Investigation and Comparison of Cascaded H-Bridge and Modular Multilevel Converter Topologies for Medium Voltage Drive Applications

In order to perform a comprehensive comparison between the cascaded H-bridge multilevel converter and the modular multilevel converter topologies an accurate and step-by-step design procedure for each converter is needed.

Fig.1 shows that the cascaded H-bridge converter (which is also known as Robicon converter) is composed of a multi-pulse transformer, 6-pulse diode front end rectifiers with a dc link filtering capacitor, and a cell-based inverter. The design procedure must include a specified procedure for determining the values and the selection of components for each of the mentioned parts.

In a similar way, the schematic of a modular multilevel converter (MMC) is brought out in Fig. 2, where the converter is composed of a series connected half-bridge modules and arm inductances. The dc links in the case of the MMC converter can be provided by an MMC rectifier or multi-pulse rectifiers.

The aim of providing design procedure is to design converters so we can compare the converters to each other from as many aspects as needed. Once we have both converters in hand, we may compare them from different points of view such as: number of parts (which affects reliability), individual component rating, energy storage, efficiency, power quality, controllability, modulation requirements, control requirements and maximum available output frequency.

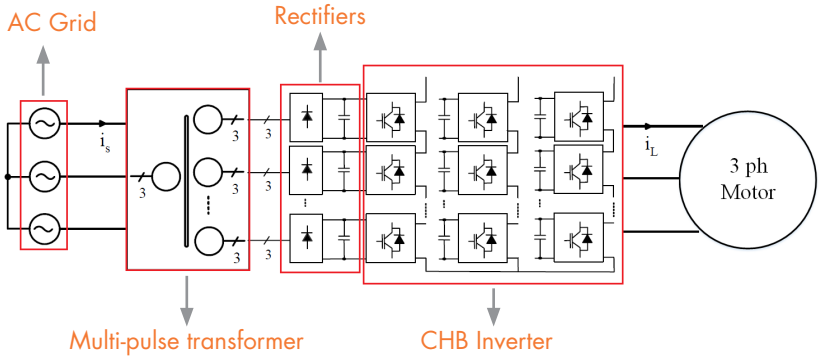


Fig. 1. Overall diagram of cascaded H-bridge converter (CHB)

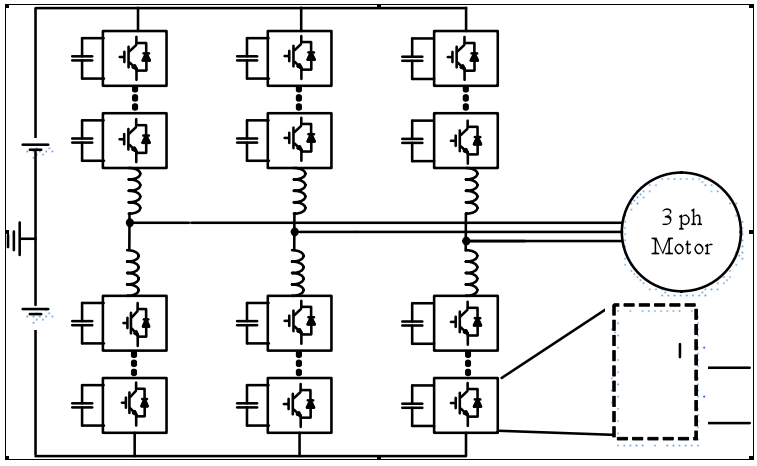


Fig. 2. Schematic diagram of modular multilevel converter (MMC)

Evaluation and Control Design of Virtual-Synchronous-Machine-Based STATCOM for Grids with High Penetration of Renewable Energy

Because renewable energy sources are environmentally friendly and inexhaustible, more and more renewable energy power plants have been integrated into power grids worldwide. To compensate for their inherent variability, STATCOMs are typically installed at the point of common coupling (PCC) to help their operation by regulating the PCC voltage. However under different contingencies, PCC voltage fluctuations in magnitude and frequency may impede the STATCOM from tracking the grid frequency correctly, hence worsening its overall compensation performance, and putting at risk the operation of the power plant. Furthermore, the virtual synchronous machine (VSM) concept has recently been introduced to control grid-connected inverters emulating the behavior of rotating synchronous machines in an effort to eliminate the shortcomings of conventional d-q frame phase-locked loops (PLL). The key advantage of VSM controllers over D-Q frame controllers is the way they synchronize; the VSM-type controller remains inherently in harmony with the electrical system, while the D-Q frame controller relies on the PLL to orient its control system and operation. The test bed is shown in Fig. 1.

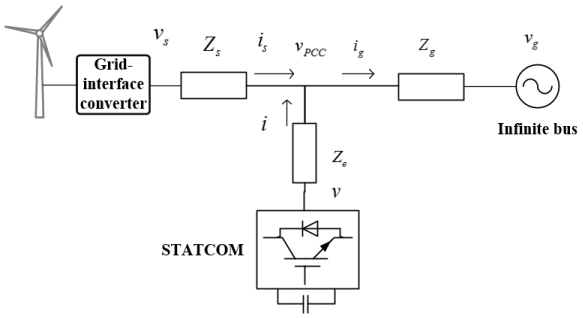


Fig. 1 Single-line diagram of the test bed

When a step change of the wind turbine input power is applied, the wind turbine frequency -s will increase or decrease at first, then come to a new steady state that is synchronized with the grid. During the transients, the STATCOM will synchronize with v_{PCC}, which will also suffer a change in frequency before returning to the nominal 50 Hz, where the VSM-based STATCOM will be less sensitive to the frequency change due to the virtual inertia applied, and stay closer to the nominal frequency than the D-Q frame controlled STATCOM. This is shown in Fig. 2. Thanks to the better synchronization performance plus virtual impedance, the PCC voltage regulation is also better, as shown in Fig. 3. Furthermore, the synchronization can be improved via virtual inertia, and the virtual impedance contributes voltage regulation and robustness to system disturbances.

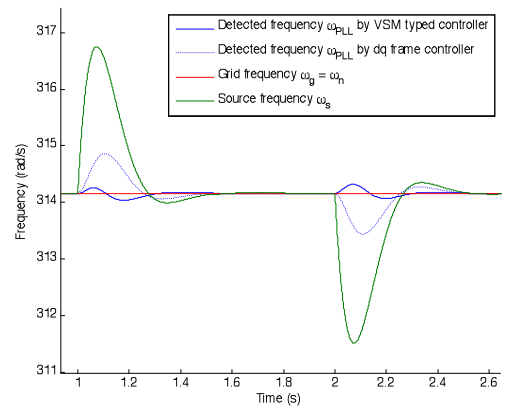


Fig. 2 Comparison of synchronization performance under power fluctuation

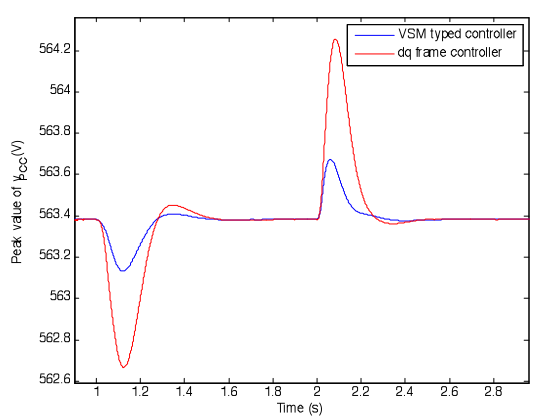


Fig. 3 Comparison of voltage regulation under power fluctuation

State-Space Switching Model of Modular Multilevel Converters

The modular multilevel converter (MMC) was originally developed for high-voltage DC (HVDC) transmission. However, it has been increasingly considered for medium- and high-voltage industrial and grid applications because it features high modularity, good voltage scalability, and the capability to operate in direct-to-line mode without a dedicated transformer.

The topology of the MMC has been modified since its invention. The original version was composed of half-bridge modules without inductors in the phase-leg arms. It was able to output sinusoidal voltage with low total harmonic distortion by using the appropriate control approach. However, the inrush currents in the arms were significant during the transient of switching the modules. To resolve this problem, additional inductors were put in series with the modules on each arm, which provided the MMC with the capability of limiting and controlling the arm currents.

Given the MMC's complex structure and operation, significant effort has been devoted to the development of appropriate controls for the MMC, and to the analysis of its circuit behavior, such as capacitor voltage imbalance and large circulating current. Prior to addressing these problems, it is necessary to determine the quantitative relationship between all state variables by building a faithful mathematical model of the MMC, which is of great importance and is indispensable in gaining real insight into the topology. The models of the MMC developed so far differ from each other in different degrees of assumptions and simplification. Most of these models are steady-state, whether sinusoidal or phasor-based, or assume that the module capacitors are DC sources (Fig. 1). Some models based on switching functions are transformed into average models, and thus the intrinsic nature of the, converter might not be fully understood, veiling possible operation modes. The other switching models that don't select appropriate state variables can offer very limited help to interpret the behaviors of the MMC. To this end, we propose a complete state-space switching model for MMCs that is derived mathematically without any of the assumptions made in other previous models, enabling the observation of circuit behaviors from a very fundamental point of view.

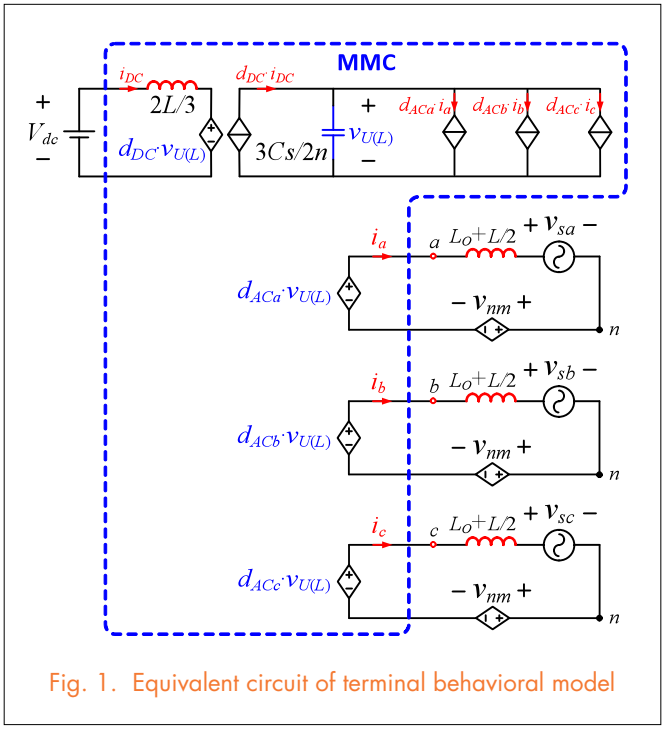


Fig. 1. Equivalent circuit of terminal behavioral model

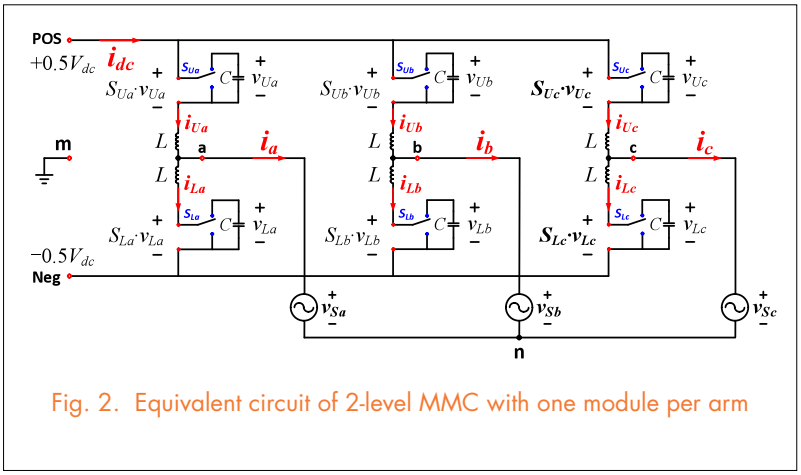


Fig. 2. Equivalent circuit of 2-level MMC with one module per arm

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Inductor Geometry with Improved Energy Density

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1200V Bi-Directional Si DMOS IGBT Fabricated with Fusion Wafer Bonding

Design and Integration of Interphase Inductors for Interleaved Three-Phase Voltage-Source-Inverters in DC-fed Motor Drive Systems

Adjustable-speed motor drives with a voltage-source pulse-width modulation inverter with long cables cause EMI issues. Usually EMI filters are made part of the system to meet EMI requirements, and these filters make up a big portion of the system weight. To improve system power density and reliability, paralleled and interleaved converter topology is commonly used. Fig. 1 shows the topology of an interleaved two-level dc-fed motor drive system. By phase-shifting the carrier waveform of individual converters with an appropriate angle, the voltage harmonics and EMI noise can be reduced, and the line inductor and EMI filter weight can also be reduced, as shown in Fig. 2.

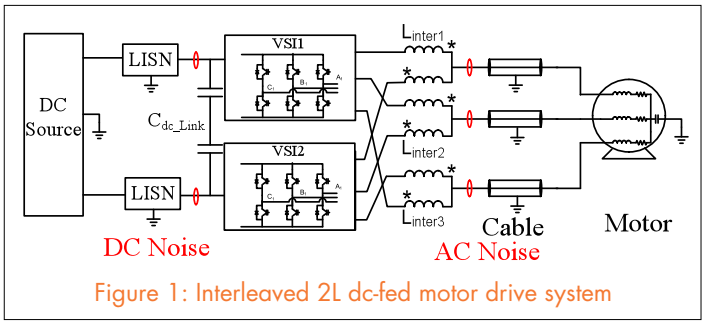
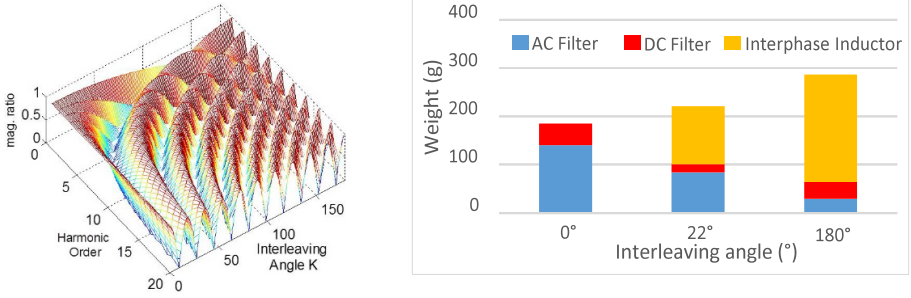


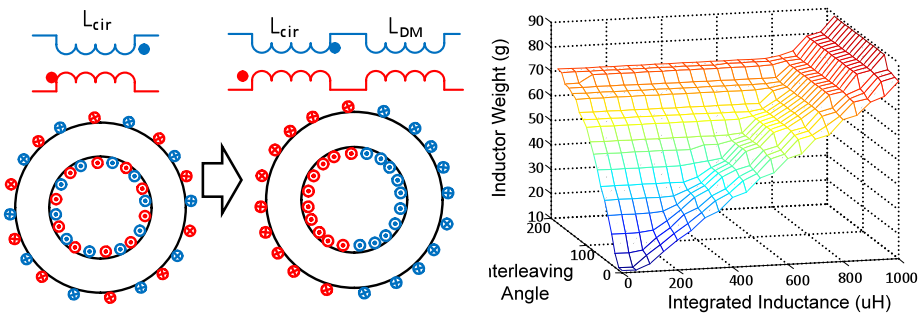
Figure 1: Interleaved 2L dc-fed motor drive system

However, interleaving also creates a voltage difference between the two converters, and requires interphase inductors to limit the circulating current. The additional weight of interphase inductors make the passive component heavier in the interleaving topology in motor drive applications. In order to reduce the total weight of passive components, an interphase inductor can be integrated with the load indcutor or DM inductors in the EMI filter with negligible increase in the weight, as shown in Fig. 3. The maximum integrated inductance is related to the interleaving angle and system operation conditions, which can be designed analytically.



(a) On-voltage harmonics b) Passive component weight reduction

Figure 2: Impact of Interleaving with different Interleaving angles

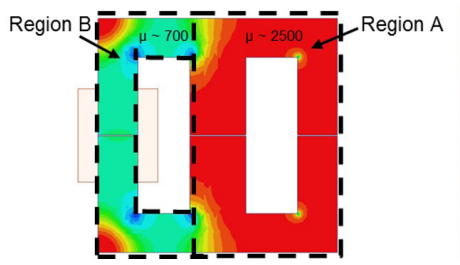


(a) Integration of interphase inductors (b) Integrated inductor design results

Figure 3: Integration and design results of interphase inductors

Gap Design for Ferrite Cores to Maximize Inductance in the Presence of NonUniform Saturation

Ferrite inductors with an air gap are widely used because of low core loss and high inductance under dc bias. The conventional inductance formula for a gapped ferrite core assumes uniform or negligibly high permeability. When the core is designed to operate near saturation (to maximize core utilization) at the rated current, such an assumption is invalid due to the appearance of regions with low, non-uniform permeabilities (Fig. 1). Finite-element simulation shows a peak in the plot of inductance versus gap length that shifts with bias current (Fig. 2(a)), and that is not predicted by the conventional inductance formula. A reluctance model is formulated to explain the nonlinear behavior, and is verified experimentally.



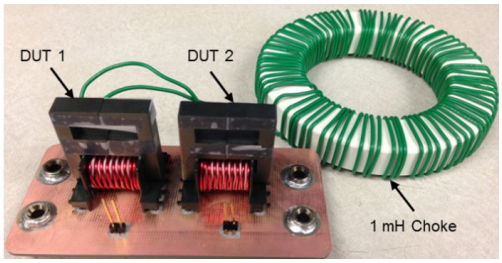
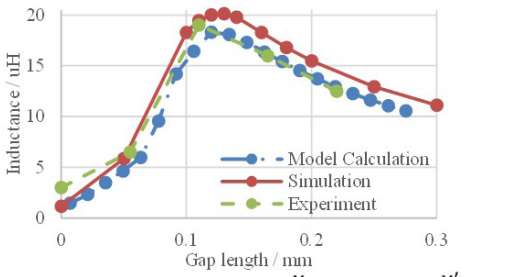


Fig. 1. Permeability map of gapped EE core and Inductance measurement setup

In order to assign the right permeability, the inductor should be divided into various cross-sections along the flux path. Dc operation point –φdc is then calculated using the first equation in Fig. 2(a). The total reluctance only depends on φdc if the μ-B curve of the core material is given. Maximum inductance can be derived when the first derivative of the reluctance formula equals zero. The peak position moves left with the decrease of dc current. The critical current where the peak position reaches zero is defined as the gapping current. This value can be used to determine whether a gap is necessary for an inductor. With a dc bias higher than the gapping current, the gapped core after optimization will have a larger inductance than an un-gapped core, and vice versa.

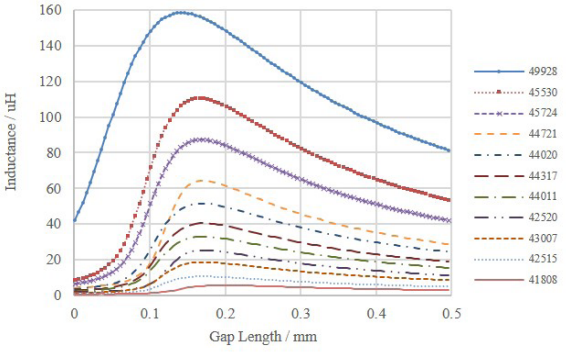
To construct an application with non-uniform permeability, the experiment of a gapped EE core with the winding around a smaller leg was carried out, as shown in Fig. 1. The calculation matches the experimental result, and the error for maximum inductance is less than 5%. Curves showing inductance versus gap length for different core dimensions were then generated to help choose a minimum-sized core to meet inductance requirement at a given dc current, as shown in Fig. 2(b).

Fig. 2.



$$NI = \sum_{i=1}^{M} f\left(\frac{\varphi_{dc}}{A_i}\right) l_i + \sum_{i=1}^{M'} \frac{\varphi_{dc} lg_i}{Ag_i \mu_0} \qquad R = \sum_{i=1}^{M} \frac{l_i}{\mu\left(\frac{\varphi_{dc}}{A_i}\right) A_i} + \sum_{i=1}^{M'} \frac{lg_i}{Ag_i \mu_0}$$

(a) Comparison of L-l_{gap} curves from three approaches;



(b) Calculated L-l_{gap} curves for different core sizes

Input and Output EMI Filter Design Procedure for Matrix Converters

The Matrix Converter (MC) is considered a main candidate for the next generation industrial motor drive, and more recently for "more electric aircraft" applications. EMI related phenomena are especially relevant in cases where its containment is of great concern—as in aircraft power systems, and as such they remain as the gap separating the MC from its actual deployment. Hence, the need for a comprehensive design procedure for EMI filters in MC applications is apparent. This comprises an appropriate model to predict the conducted EMI emissions of the MC, both in common-mode (CM) and in differential-mode (DM), and the actual filter design procedure. Further, if both input and output terminal EMI filters are required—as in the case under consideration, then the design procedure should address both filters simultaneously. This is as opposed to the dc-link based ac-to-ac power converters where typically input and output filters are designed assuming decoupled input and output noise. Lastly, to verify the power density of the filter designed, the weight and volume of the passive components should be carefully calculated too. The last step above allows the designer to verify the level of compactness achieved, a critical aspect since MCs are usually assumed to feature a higher power density than indirect power converters, an assumption which is based solely on the fact that the MC power stage lacks dc-link capacitors, without considering the impact of EMI filters. In this case, a comparison against alternative back-to-back converters ensures that the MC is indeed the best solution. In this paper specifically, two- and three-level voltage-source converters are used as possible alternatives for the design of the motor drive in question.

In this regard, this paper presents a detailed design procedure for the input and output EMI filters of an MC motor drive rated at 30 kW, driving a permanent magnet synchronous machine (PMSM). The procedure is based on frequency domain analysis of the EMI sources and conduction paths, where the input and output CM filters are designed simultaneously due to the coupling of the CM path.

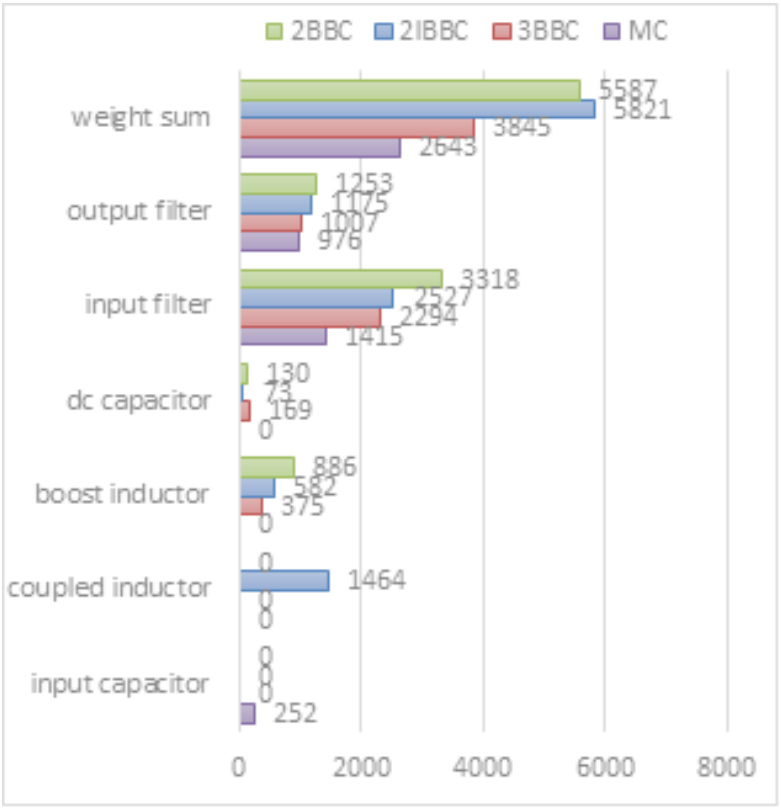


Fig. 1. Weight distribution of AC-AC converters

A comparison between the estimated EMI filter weight of the MC, and a two-level back-to-back converter (2BBC), two-level interleaved back-to-back converter (2IBBC), and three-level back-to-back converter (3BBC) is conducted using the proposed design procedure for all converters in question. This shows the advantage of the MC where high power density is desired.

Inductor Geometry with Improved Energy Density

The "constant-flux" concept is leveraged to achieve high magnetic-energy density, leading to inductor geometries with height significantly lower than that of conventional products. Techniques to shape the core and to distribute the winding turns to shape a desirable field profile have been devised for the two basic classes of magnetic geometries; those with the winding enclosed by the core and those with the core enclosed by the winding. A relatively constant flux distribution is advantageous not only in terms of density, but also in terms of thermal problems via the reduction of hot spots, and in terms of reliability via the suppression of flux crowding. In this study of the constant-flux inductor (CFI) with enclosed winding, the foci are the operating principle, dc analysis, and basic design procedure. Prototype cores and windings are routed from powder-iron disks and copper sheets, respectively. The design of the constant-flux inductor is validated by an assembled inductor prototype.

Based on the enclosed-winding geometry, the behavioral model of the constant-flux inductor can be constructed in such a way that it shapes the flux distribution and estimates the performance of the inductor. As shown in Fig. 1, an ideal constant-flux inductor with enclosed winding consists of a magnetic core with N_w winding windows carrying prescribed Ampere-turns AT_j. The objective is to synthesize the Ampere-turns to constrain the flux variation to a "uniformity factor α" ratio of the minimum flux density αB_{max} to the maximum flux density B_{max} allowed in the magnetic field around winding window j. "Constant" flux is achieved when α approaches unity. The model is modified to achieve a prescribed α, as well as the optimal design for a constant-flux inductor.

Fig. 2 gives an example of the relationships among the current rating, inductance, and dc resistance when the relative permeability changes from 20 to 30. Along each curve, the current rating is fixed while the relative permeability is swept from 20 to 30. Either a smaller permeability or a smaller current rating would increase the number of turns that each winding window represents in order to maintain the maximum flux density B_{max}. By selecting the optimal variables, the performance of the inductor can be significantly improved.

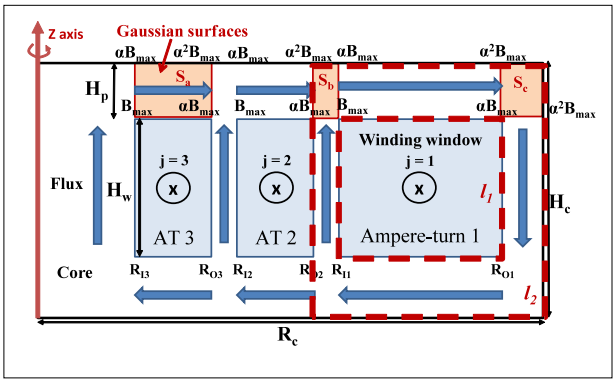


Fig. 1. Ideal constant-flux inductor geometry

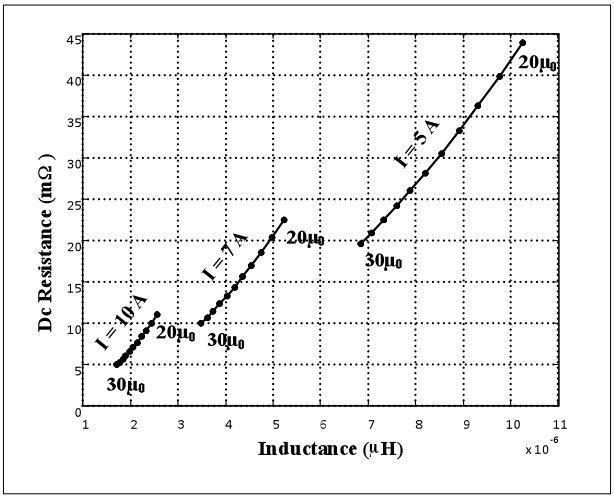


Fig.2. Relationship among inductance, dc resistance, permeability and current rating.

Assessment of Switching Frequency Impact on EMI Emissions of 10 kW SiC Power Converter Using Un-terminated Behavioral Models

High switching frequency operation contributes to the more complex inverter architectures, but also changes the EMI performance in a system. When the switching frequency of a three-phase inverter changes from 20kHz to 70kHz, the amplitude of the differential mode (DM) and common mode (CM) noise beyond the switching frequency will increase, especially above 1MHz. Fig. 1 and Fig. 2 show the DM and CM input/output current for a 3-phase SiC MOSFET power inverter at 20k and 70k switching frequency.

Un-terminated EMI behavioral modeling can describe the three-phase inverter with two noise sources and three inverter impedance parameters. The inverter model and EMI model are shown in Fig. 3. This model is accurate in predicting the DM and CM noise for most practical input and output conditions of an inverter. However due to the limitation of the measurement, it's difficult to have the amplitude of the frequency component above 10MHz during an experiment. Therefore the accuracy for the un-terminated model above 10MHz is uncertain. Pushing the switching frequency higher will help to provide high-frequency components of larger amplitude.

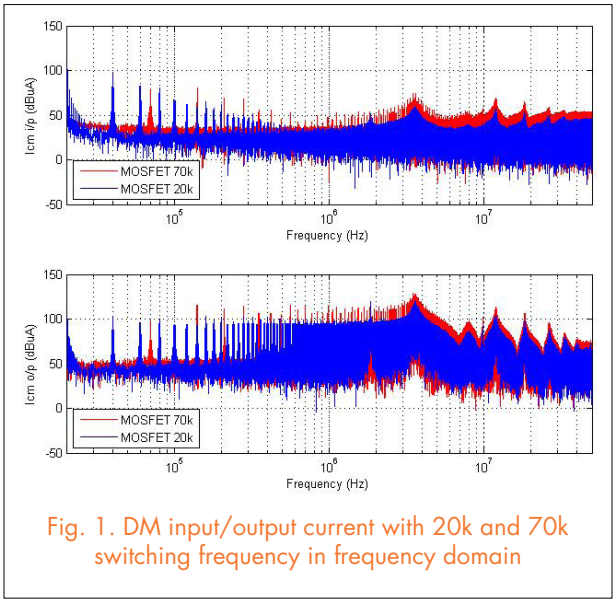


Fig. 1. DM input/output current with 20k and 70k switching frequency in frequency domain

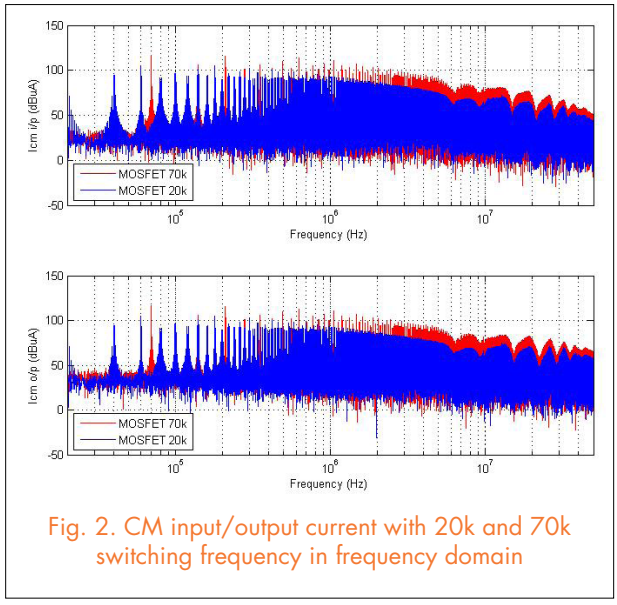


Fig. 2. CM input/output current with 20k and 70k switching frequency in frequency domain

In terms of the model, when the switching frequency goes high, the equivalent noise sources of the inverter will increase, as shown in Fig. 4, and the equivalent impedances are likely to remain unchanged, as shown in Fig. 5. This result will help understand the EMI analysis at the system level with different switching frequencies, and to design appropriate EMI filters. The model runs in the frequency domain and is validated with experiment on a SiC MOSFET inverter.

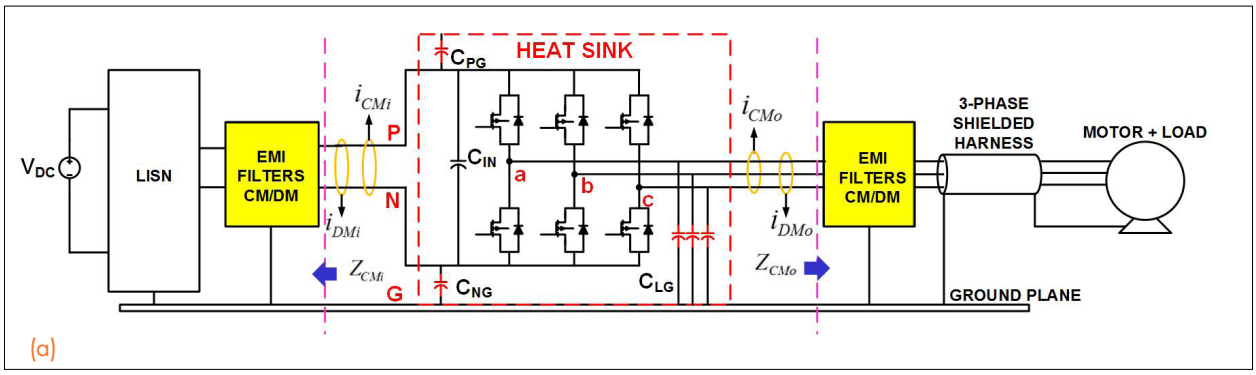
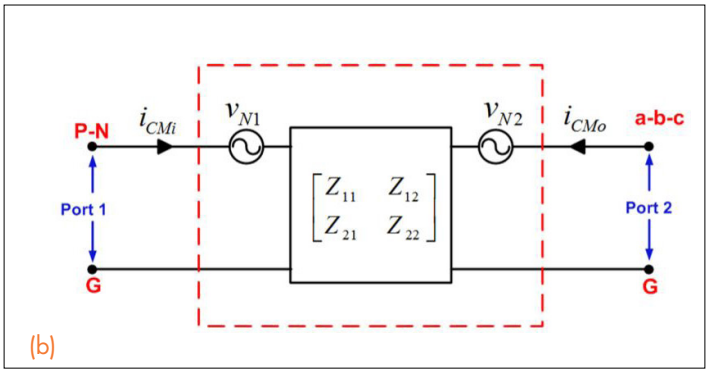


Fig. 3. Un-terminated CM EMI behavioral model: (a) The inverter modeled, (b) The extracted model



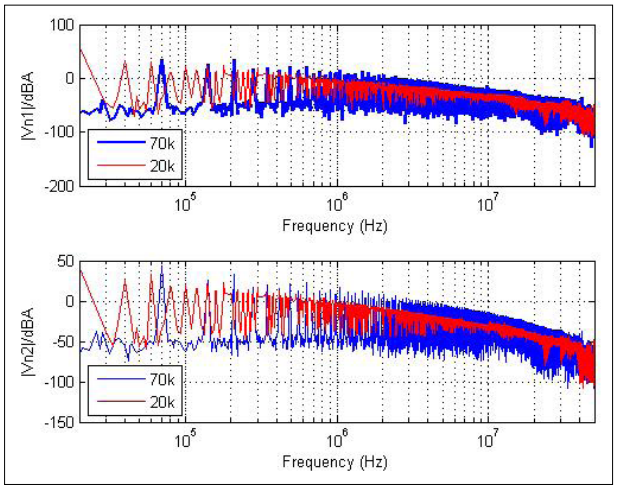


Fig. 4. The equivalent noise sources of the un-terminated behavioral inverter model

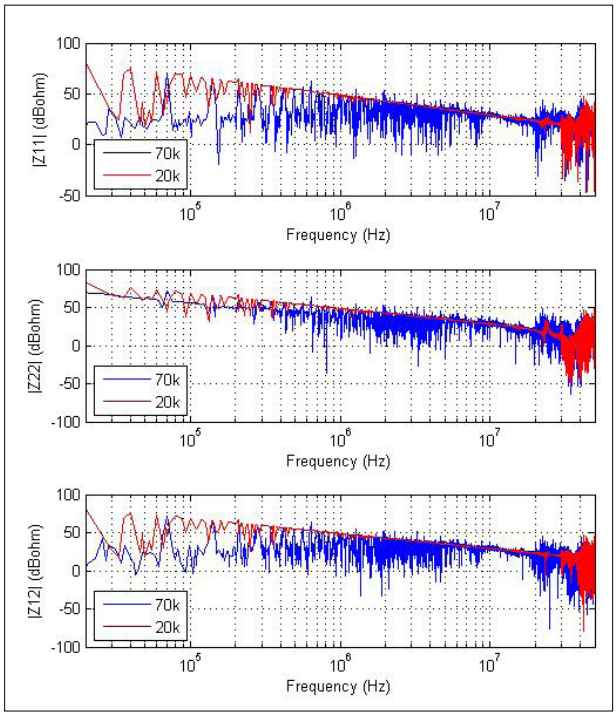


Fig. 5. The equivalent impedance matrix of the un-terminated behavioral inverter model

Bi-directional PHEV Battery Charger based on Normally-off GaN-on-Si Multi-Chip

Automobile manufacturers are intent to significantly reduce the weight and volume of the on-board charger for Lithium-Ion batteries in Plug-in Hybrid Electric Vehicle (PHEV). If the PHEV charger has enabled bi-directional power flow, can be used as part of the smart grid. With these two motivations, a high frequency, high efficiency bi-directional battery charger is built with high voltage normally-off GaN-on-Si HFETs. The battery charger topology consists of a 500 kHz Full Bridge (FB) AD/DC stage and a 500 kHz Dual Active Bridge (DAB) DC/DC stage, as shown in Fig. 1.

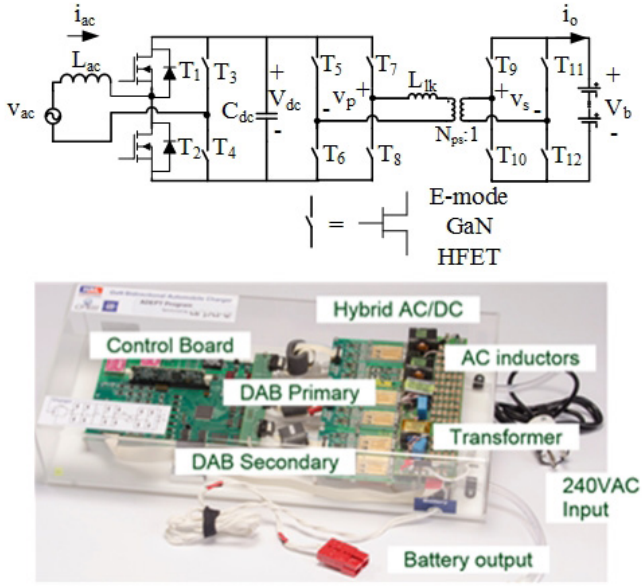


Fig. 1.GaN bi-directional battery charger topology and prototype

The full bridge topology is used for the bi-directional AC/DC stage. In the AC/DC stage modulation, one of the phase legs only flips the polarity of the midpoint every half line cycle. This enables the possibility to use a very large Si MOSFETs to optimize the conduction loss since the switching loss will be negligible due to 60Hz switching. DAB is one of the most widely researched bi-directional DC/DC topology because of the zero-voltage-switching and fixed frequency. Except for the 60Hz-commutation phase leg in the AC/DC stage, all the rest of the phase legs are built with an enhanced mode high voltage GaN HFETs from HRL Laboratories. The phase leg is packaged in a multi-chip-module with built-in gate driver and decoupling capacitors. The module realizes low parasitics, low switching overshoot and low switching energy.

The prototype shown in Fig. 1 consists of three building blocks of full bridge (designated as Hybrid AC/DC, DAB primary and DAB secondary), magnetics and the control board. High switching frequency leads to smaller magnetic size. The control board is for general purposes and can be reduced in the final implementation.

Experimental waveforms are shown in Fig.2. The test was conducted at 165Vrms AC input, 250V voltage at the battery and 1kW output power. By allowing the 120Hz ripple into the battery, the DC link capacitance can be significantly reduced so that only ceramic capacitors are used. The achieved system efficiency is 92.0%, and if doing DC charging, the efficiency is 94.2%.

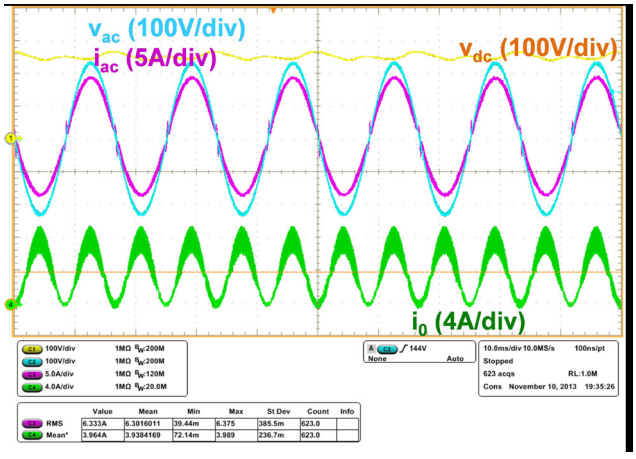


Fig. 2. Charging system waveforms at 1kW with sinusoidal charging. Conditions: Vac = 165V(rms), Vdc = 250V, Vb = 250V, Io(avg) = 4A.

A High-Temperature SiC Three-Phase AC–DC Converter Design for >100° C Ambient Temperature

High-temperature (HT) converters have gained importance in industrial applications where the converters operate in a harsh environment, such as in hybrid electrical vehicles, aviation,and deep-earth petroleum exploration. These environments require the converter to have not only HT semiconductor devices made of SiC or GaN, but also reliable HT packaging, HT gate drives, and HT control electronics. We have developed a detailed design process for an HT SiC three-phase PWM rectifier that can operate at ambient temperatures above 100° C. A SiC HT planar structure packaging is designed for the main semiconductor devices, and an edge-triggered HT gate drive is also proposed to drive the designed power module. The system is designed to make use of available HT components, including passive components, silicon-on-insulator chips, and auxiliary components.

Taking into consideration the material available, SiC diodes and JFETs are used as the main circuit devices and are packaged in a novel HT planar structure. Besides the HT SiC power module, an HT transformer-isolated gate drive circuit is also proposed. Other functions; such as the harmonic filter and the control system, including protection and sensor functions; are designed according to the available HT silicon-on-insulator (SOI) ICs and HT passive components. Because of both the simple topology and the simple control, a typical single-switch three-phase boost PFC circuit is used to demonstrate the concept of HT converter design. The structure and topology for the three-phase ac/dc rectifier are shown in Fig. 1. The power module is composed of seven SiC diodes and one normally ON SiC JFET. The first six diodes are utilized as a diode rectifier stage, and another diode and JFET make up the second boost stage. The input voltage is lower than 100V (rms/phase), and the output voltage is regulated to 270V. The system's power rating is 1.4kW.

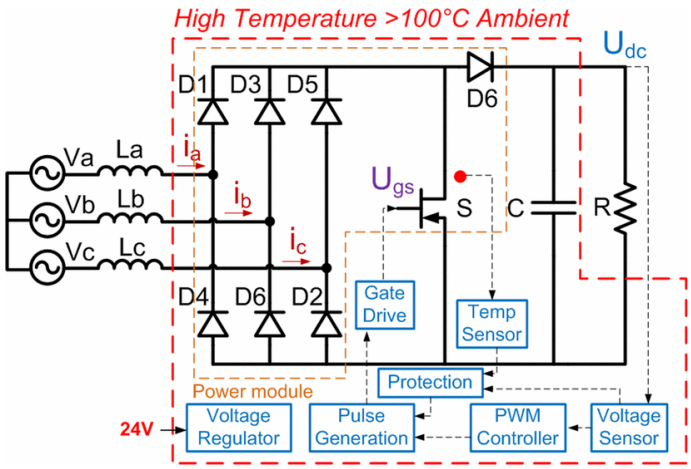


Fig. 1. System topology and configuration.

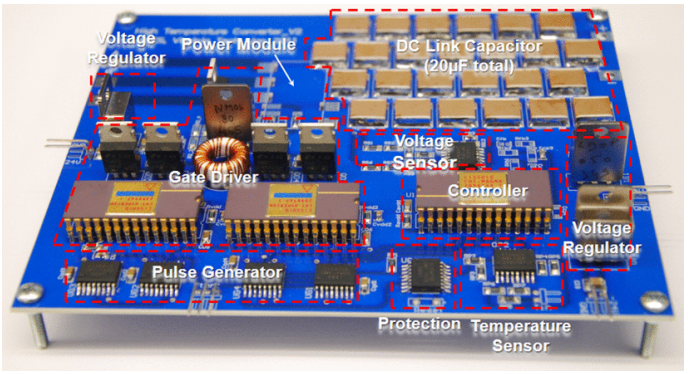


Fig. 2. System prototype.

30-W Flyback Converter Operating at 5 MHz

Thanks to the simplicity of the power stage, flyback converters have been widely adopted as cost-effective isolated power converters for low-power applications. While the flyback's coupled inductors provide a convenient means for isolation, their stored energy is responsible for the converter's low power density, and their leakage inductances are responsible for the high voltage stress on the semiconductor switches. Thus, attempting to reduce the size of the inductors by increasing the switching frequency will have limited success unless the switching frequency is increased significantly.

The baseline for this investigation is the class of converters with voltages of 36 -72 V down to 12 V at 0 - 30 W. Around 5 MHz would be a suitable switching frequency, considering the introduction of GaN transistors on the market in the last few years. To mitigate switching loss, the quasi-square-wave flyback converter with synchronous rectifier was selected, as shown in Fig. 1.

Nickel-zinc (NiZn) ferrite 4F1 with a relative permeability of 80 was selected as the magnetic material since it had low loss in the 5 - 10 MHz range. Fig. 2 shows the planar coupled inductors with 0.96 μH of magnetizing inductance and a size of ER 18×3.2×10 mm³, which were fabricated with a leakage inductance of 30 nH. In addition, the high dv/dt of 16 V/ns and high di/dt of 10 A/ns caused by the smaller output capacitance of GaN FETs necessitated negative 2 V between the gate and the source to prevent false turn-on of the switches.

The peak efficiency is 90.6% at a full load of 30 W, with ZVS achieved for both switches. The switching losses are the dominant losses (36.5%) of the total loss because of the large turn-off current for both switches; 35.3% of total losses are incurred in the coupled inductors; 66.1% of magnetic loss is the winding loss, due to the skin and proximity effects in the megahertz range. With the same power level and efficiency, the power density is 14% better than that of the commercial flyback converter.

The bulkiest component is the coupled inductor, and the flux density is the dominant parameter to determine the core size, which is constrained by the material properties. Future research will be focused on magnetic design to further decrease the winding loss and volume.

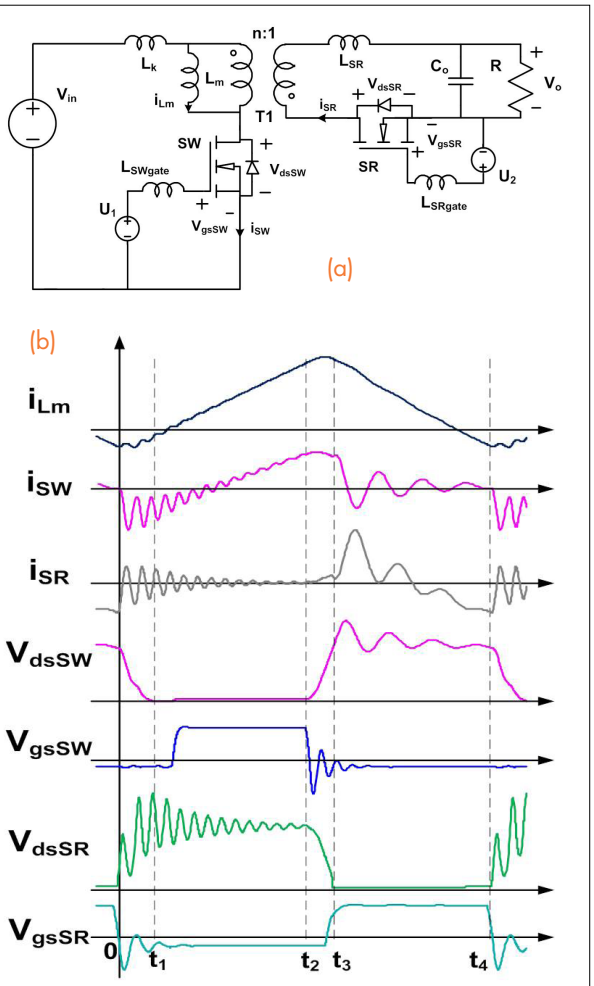


Fig. 1. (a) Schematic of quasi-square-wave flyback con-verter and (b) Steady-state waveforms

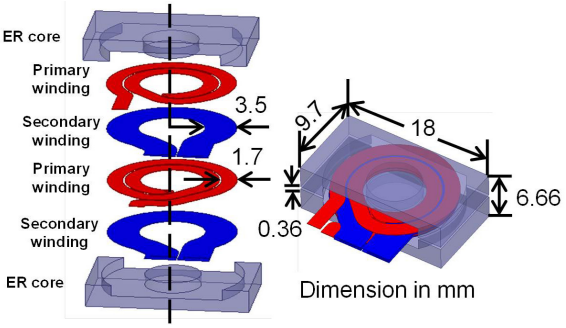


Fig. 2. Exploded view of planar coupled inductors

Design of a GaN Multichip Half-bridge Module for High-Frequency Power Converters

CPES has created a design of a multichip Gallium-Nitride (GaN) power module for high-frequency power conversion. The module is designed with the HRL 600 V Gallium-Nitride (GaN) enhancement-mode HEMT device. To exploit the capability of fast switching with low loss from high-voltage GaN devices, different layout structures have been analyzed to reduce power loop parasitic inductance and improve switching performance. The approach investigated is based on a multi-chip module where small-current-rated dies are placed in parallel to achieve higher current handling capability. Finite-element analysis (FEA) and switching circuit simulation show that the multi-layer powerloop design can effectively reduce the gate loop inductance and voltage overshoot on the devices. This multi-layer design also improves current sharing of the multi-chip module during switching operation.

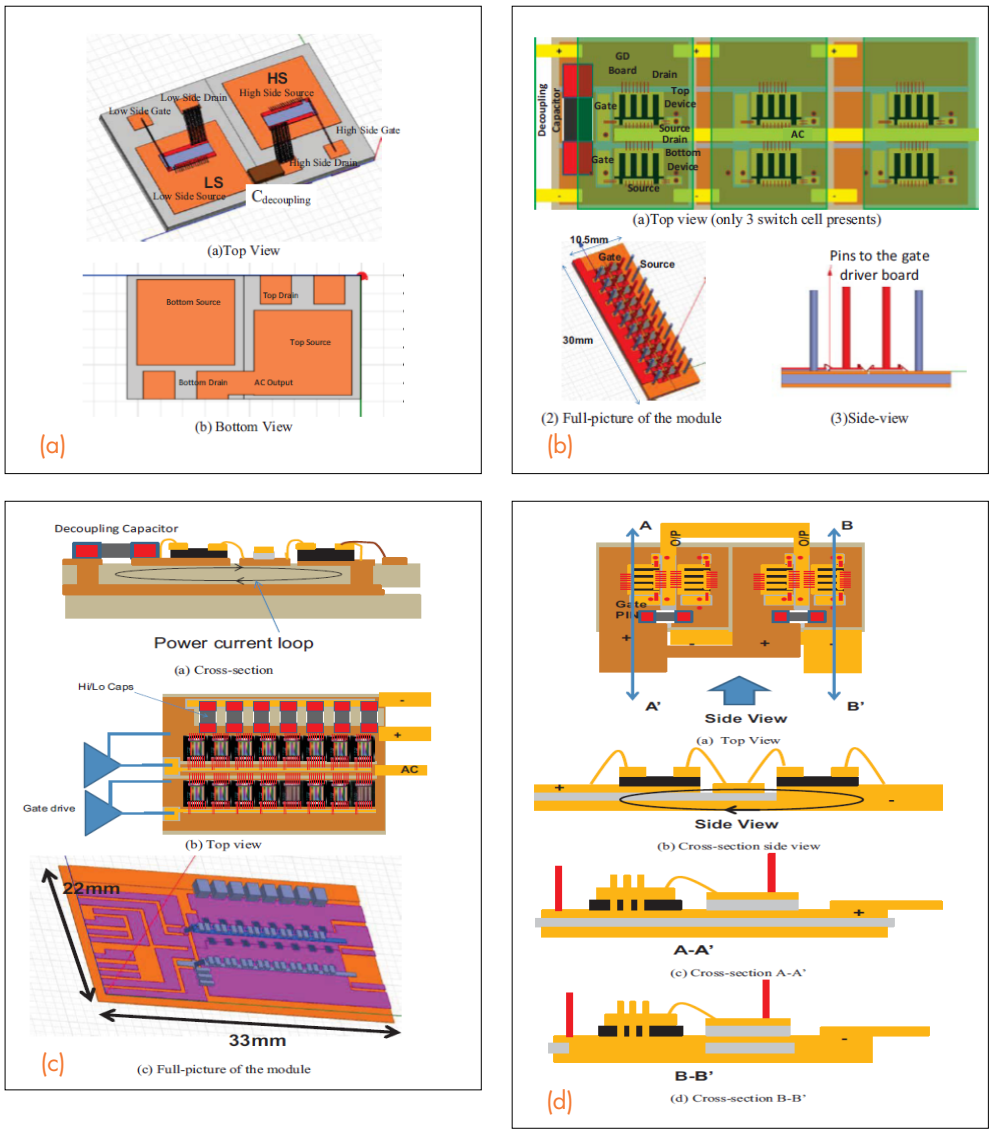


Fig. 1. (a) Half-bridge design using SMD devices; (b) Layout 1 - Cascade structure; (c) Layout 2 - Cascade multi-layer structure; (d) Layout 3 - Paralleled multi-layer structure

Multi-Level Single-Phase Shunt Current Injection Converter Used in Small-Signal dq Impedance Identification

This paper describes the detailed design of a single-phase multi-level single-phase shunt current injection converter based on cascaded H-bridge topology. The shunt current injection converter can inject an arbitrary current perturbation at three-phase power system interfaces, in order to identify small-signal dq impedances. Special attention is given toward the selection of inductors and capacitors, trying to optimize the selected component values. The proposed control is extensively treated and inner current and outer voltage loops are completely analyzed. Furthermore, voltage balancing is included into the control to assure dc voltage control for each H-bridge module. Analytical expressions, which describe the design procedure, are derived and verified to be accurate. The designed converter is simulated using a detailed switching simulation model and excellent agreement between theory and simulation results are obtained. The proposed multi-level single-phase converter is a natural solution for single-phase shunt current injection with the following properties: modular design, capacitor energy distribution, reactive element minimization, higher equivalent switching frequency, capability to inject higher frequency signals, suitable to perturb higher voltage power systems and capable of generating cleaner injection signals.

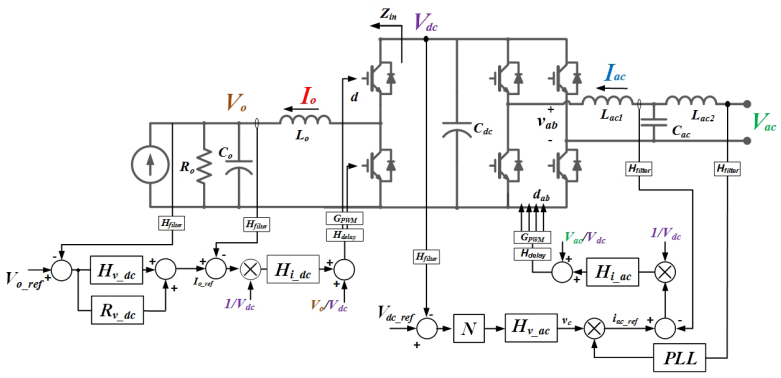


Figure 1.Multi-level single-phase shunt current injection converter based on cascaded H-bridge topology.

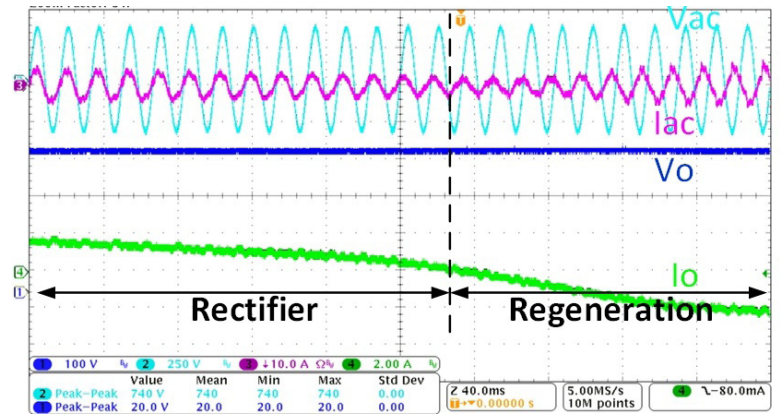


Figure 2: Simulation waveform signals for 50 Hz injection operating point (a) inductor current ilf and current reference iref (b) dc voltages vdc_1, vdc_2, vdc_3 (c) duty cycles d_1, d_2, d_3 (d) switching voltage.

The first simulated operating point investigates waveforms when low frequency (50 Hz) current is being injected into the grid, this operating point is equivalent to 10 Hz injection in dq coordinates. Thus, in this operating point a low frequency voltage ripple at 10 Hz is present in dc capacitor voltages. Another critical operating point is a high frequency injection of 30 A rms, 1 kHz current into the system. Figure 10 shows simulation waveforms that verify proper operation when the converter is injecting a 50 Hz sinusoidal signal. The dc voltages are balanced among themselves and a 10 Hz ripple is slightly below 60 V, which is accurately predicted by analytical expressions.

Efficiency Evaluation of Two-level and Three-level Bridgless PFC Boost Rectifiers

Increasing the efficiency has always been one of the most important topics in power electronics, besides power density increase and cost reduction. Recently, to improve the efficiency of the front-end PFC rectifiers for medium power applications such as telecom, the more-electric aircraft and the electric vehicle, industry has begun to look into bridgeless PFC rectifiers due to the efficiency increase brought by the absence of the diode bridge. In this paper, the efficiency of a two-level semi-bridgeless PFC boost rectifier (2LPFC) with clamping, a paralleled two-level semi-bridgeless PFC boost rectifier (P2LPFC) with clamping, an interleaved two-level semi-bridgeless PFC boost rectifier (I2LPFC) with clamping, a three-level bridgeless PFC boost rectifier (3LPFC), a three-level bridgeless PFC boost rectifier with AC switch (3LPFCAC), a paralleled three-level bridgeless PFC boost rectifier (P3LPFC) and an interleaved three-level bridgeless PFC boost rectifier (I3LPFC) are evaluated and compared. The topologies in question are shown in Fig. 1.

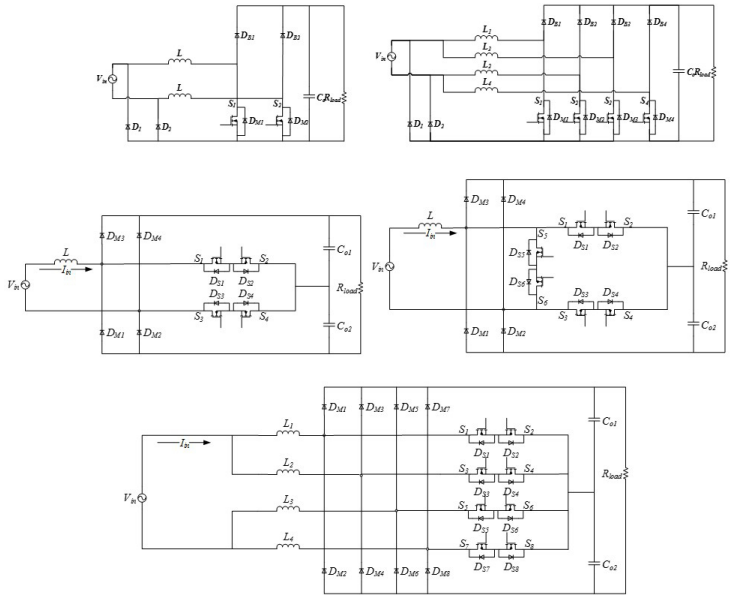


Fig. 1. (a) Semi-bridgeless PFC boost rectifier. (b) Paralleled or interleaved PFC boost rectifier. (c) Three-level bridgeless PFC boost rectifier. (d) Three-level bridgeless PFC boost rectifier with AC switch. (e) Paralleled or interleaved Three-level bridgeless PFC boost rectifier.

To estimate the efficiency of each converter, the operation of all the converters are first introduced and analyzed. Based on this, to make a fair comparison, an efficiency-oriented design optimization is conducted to all the converters. After that, the efficiency estimation is done by simulation and mathematical calculation. To be more specific, the conducting current at any time through any components can be obtained using simulation based on which the conduction loss can be calculated taking into consideration such factors as temperature. To estimate the switching loss of the switches, a piecewise linear model for MOSFET is applied. In this model, the gate charges of the MOSFET instead of the non-linear capacitance are used to calculate the turn-on and turn-off time due to the consistency of the charges in a wide voltage range. The loop inductors and the loss caused by charging the diode when turning on the switch is considered. Transition of the drain-to-source current and voltage are assumed to be linear. The efficiency comparison of the topologies is shown in Fig.2.

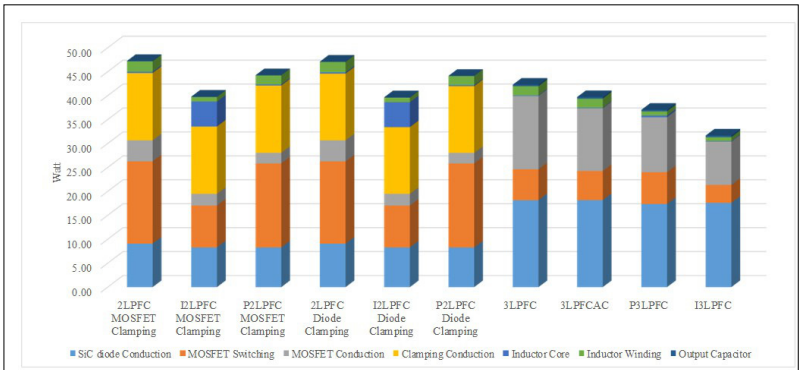


Fig. 2. Loss breakdowns of the compared topologies

Formal Procedure for Power Electronics Modeling Verification, Validation and Uncertainty Quantification (VV&UQ)

During the last two decades, a constructive approach has been developed to the concepts, terminology and methodology of Verification and Validation (V&V). Since this development is based on practical issues, not the philosophy of science, each community has tried to improve the existing terminology to one which is more comprehensible in their own field of study by building their own terminology and framework. All definitions follow the same concept, but they have been defined in a way that is applicable to the specific field of study. For this reason the Power Electronics Society also needs its own V&V definitions and framework that are applicable to power electronics systems. The main goal of the VV&UQ process is to assess the confidence in modeling and simulation. It should be noted that there is no validated model and the model can just be validated for intended use.

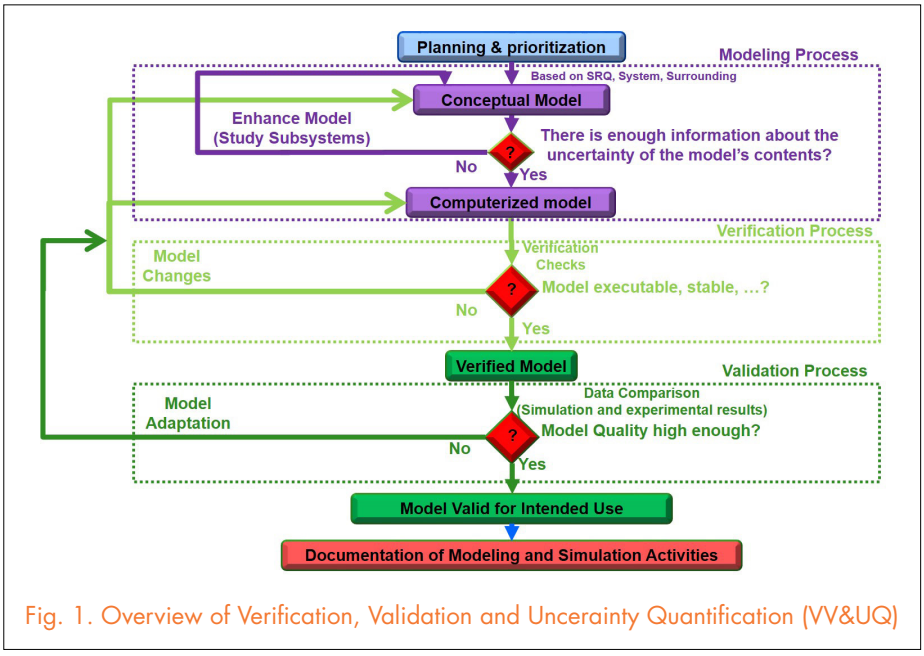


Fig. 1. Overview of Verification, Validation and Uncerainty Quantification (VV&UQ)

Fig. 1. represents the overview of the proposed VV&UQ formal procedure. The main steps to complete the VV&UQ process are: Planning and Prioritization (P&P), Modeling process, Verification process, Validation process and, at the end, documentation of modeling and simulation activities. Based on the validation metric chosen in this paper, the output of the VV&UQ process is the quantified uncertainty between the simulation and experimental results. The main feature of this procedure is the capability of improving the model until it is valid for intended use.

However, there is a tradeoff between the accuracy of the VV&UQ result and costs. Customers and development teams should decide about their desirable level of accuracy and the costs they are able to afford. These decisions are part of P&P activities. The Modeling Process provides a formulated procedure for building a conceptual model and computerizing it in order to have the most complete model for intended use before starting the V&V process. The verification process first checks the code verification requirements and then calculates the computational error to see whether the model is verified based on the requirements specified in the P&P step. Once the model is verified, the validation process gets started. The Validation Metric is the main part of the validation process, which is the methodology used to quantify the uncertainty between the computational and experimental results. The utilized metric in this paper is based on the Bayesian approach. This method is a statistics method which quantifies the difference between simulation and experimental results based on the intended level of confidence to complete the VV&UQ process. The last but most important is the documentation of the modeling and simulation activities in order to minimize the costs in future projects.

Discussion on the Compression of the Resistance Range in Two-port Networks

Load variations are a known problem for resonant conversion systems. With a wide range of variations, each requires a significant change in the switching frequency, complicating EMI compatibility design, and efficiency that would reduce especially in light load conditions. The load variation problem can be significantly reduced with use of dedicated circuitry that would "compress" the variation of the load resistance into a smaller range. Current effort in the scientific community examines a structure that utilizes a passive, lossless network with the combination of passive rectifiers. Although the structure (called resistance compression network) is simple and significant suppression of the load variations is possible, the structure is only applicable to DC-DC conversion systems, where the same effect could be achieved if the active solution had been pursued instead.

Thus, this work examines the existence and practicality of the resistance compression networks for resonant power conversion. The investigation has been carried out generalizing a compression network as the Linear, Time-Invariant, lossless two-port network (Fig. 1). ABCD parameters have been used in the analysis. After some mathematical derivations, it was found that such a range in a compression circuit cannot be synthetized. Fig. 2 summarizes the issue. Although the compression can be achieved when looking at the real part of the input impedance (range [10 Ω, 100 Ω] compressed to [1 Ω, 6 Ω]), it is not possible to keep the imaginary part of the impedance small. The solution has to be found as a time-variant circuit and one such practical topology will be presented in the full paper, namely a resistive point-compressor, where a range of resistance is compressed to a single point only.

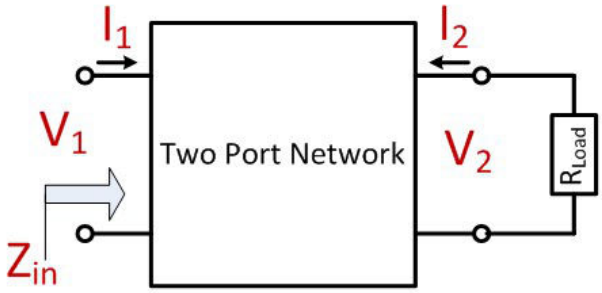


Fig. 1. LTI lossless two port network

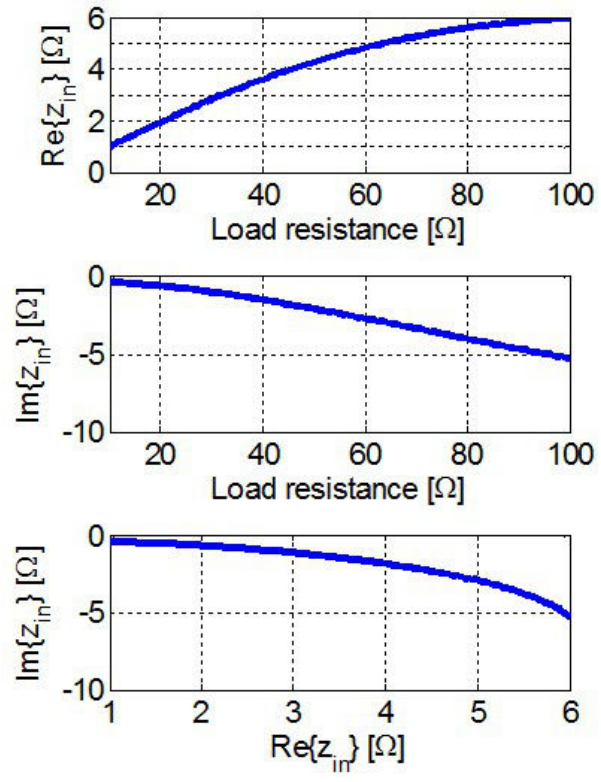


Fig. 2. Parasitic inductance with different switching loops

Resistive point-compression – Theory of Operation in Resonant Power Transfer

Resonant converters have been the favored principle of power transfer among vehicular, medical and consumer electronics due to high efficiency, high operating frequency and compact size/weight. High performance is typically achieved when a resonant converter operates near the designed "sweet spot". However, when circuit parameters and loads are changed the efficiency, transferred power, or power density can worsen. Often, to regulate a resonant converter it is required to change the switching frequency, complicating EMI and thermal designs. A resistive point-compression has been conceived to tackle circuit parametric variations. The primary operation of the resistive point-compressor is to compress wide variations of the load resistance into a single resistance value. The adaptive approach also gives the possibility of accommodating other changing parameters in the circuit. Having the capability to control parametric variations, the system can be optimized for efficiency and power transfer, switching at the constant switching frequency. In addition, multiple-output systems are easily feasible, with the capability to regulate power sharing.

Fig. 1 shows the principle of the operation for the resistive point-compressor. It is actually an adaptive matching circuit, where equivalent inductance L_{ew} and equivalent capacitance C_{eq} can be controlled. Controllable reactances are implemented very similarly to the phase-controlled switched inductor/capacitor. By controlling L_{eq} and c_{eq} it is possible to operate the adaptable matching circuit that $Z_{in} = R_{ing} = R_{opt}$, where the R_{opt} is the desired value of the input resistance of the resistive point-compressor. Fig. 2 gives an example where R_{in} controlled to the value of 50 Ohms.

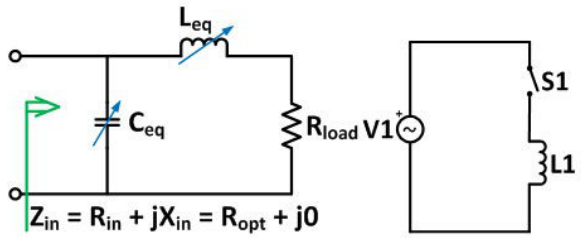


Fig. 1. Left: Resistive Point-Compressor; Right: Implementation of variable inductance.

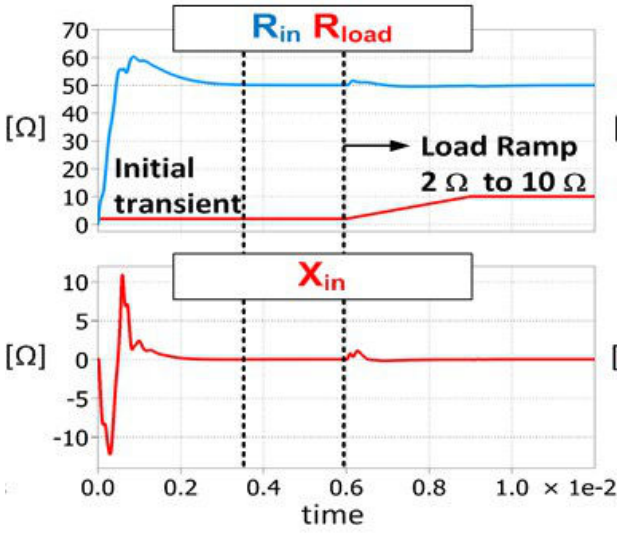


Fig. 2. Time response of resistive point-compressor.

Energy Harvesting from a Generator with Time-Dependent Output Inductance

The output current of a generator with time-dependent output inductance is distorted because of non-linear inductance. The distortion reduces the harvested power from the generator. Reducing the distortion in the output current of the generator enhances the power output of the generator.

The conditions to maximize power obtained from a generator with time-dependent output inductance are derived mathematically in this paper. These conditions are realized using a converter behaving as variable impedance compensator. A hardware prototype of the converter is developed. The generator with time-dependent output inductance is designed and constructed in the lab using two discrete air-core inductors. An example of a generator with time-dependent output inductance is a magnetostrictive generator. The two inductance values for the designed generator are calculated to match the terminal behavior of the magnetostrictive generator. A picture of the developed generator is shown in Fig. 1. The output current (Fig. 2) for the 320-W generator shows a 29% THD (Total Harmonic Distortion). Reducing the distortion to 4 % improves the power in the load to 465 W. Thus, even after accounting for the losses in the converter, there is 45% improvement in the harvested power from the generator. The experimental hardware of the variable impedance compensator is shown in Fig. 3, and the output current waveforms of the generator, on connecting the compensator are shown in Fig. 4.

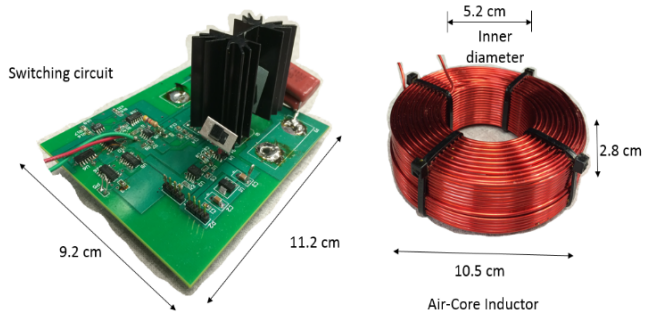


Fig. 1. Hardware prototype of switching circuit of the generator and air-core inductor (together constitute the generator).

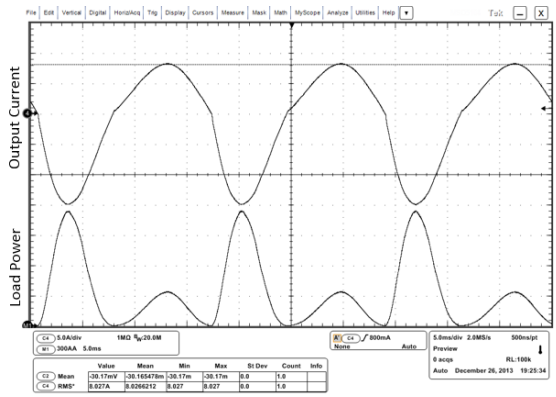


Fig. 2. Distorted output-current (5 A/div) from the generator and power (300 W/div) dissipated in the load without variable impedance compensator.

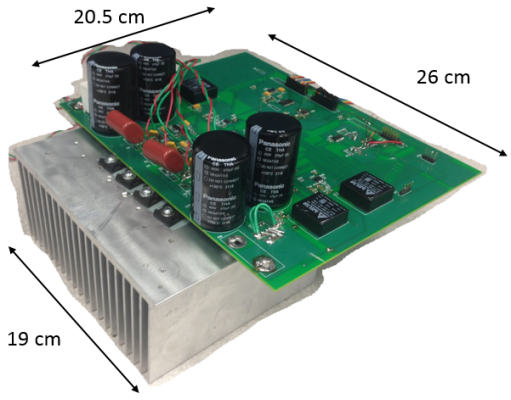


Fig. 3. Hardware prototype of the variable impedance compensator.

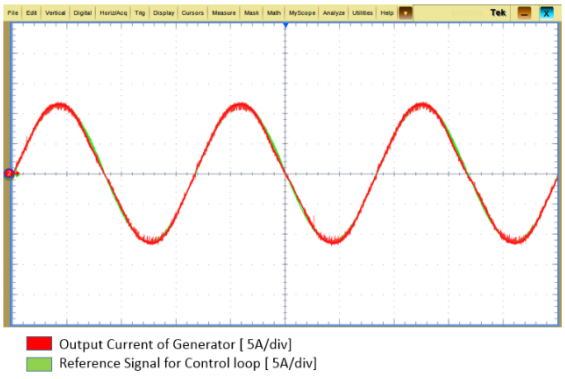


Fig. 4. Output current (5 A/div) of the generator with the variable impedance compensator.

Two-Stage Multi-Channel LED Driver with CLL Resonant Converter

The CLL resonant converter is a variant of the LLC resonant converter, as shown in Fig. 1. The resonant tank of the CLL converter is composed of C_r, L_{r1} and L_{e2}. In normal operation, C_r will resonate with L_{r1} and L_{e2}. Its operation principles are very similar to the LLC's. However, for CLL, the magnetizing inductance of the transformer can be very large, because the magnetizing current of the transformer does not play an important role in achieving ZVS during dead time. In contrast, the current flowing through the external inductance L_{r1} is very critical for achieving ZVS. For simplicity, the impact of a small magnetizing current can be ignored in practice, so $i_{Cr} \approx i_{Lr1}$ during dead time. Therefore, L_{r1} could be designed properly to meet the ZVS requirement.

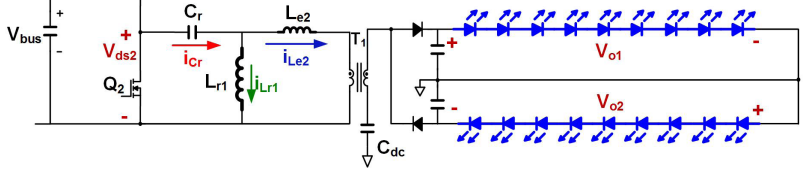


Fig. 1. Basic CLL resonant converter for LED Driving

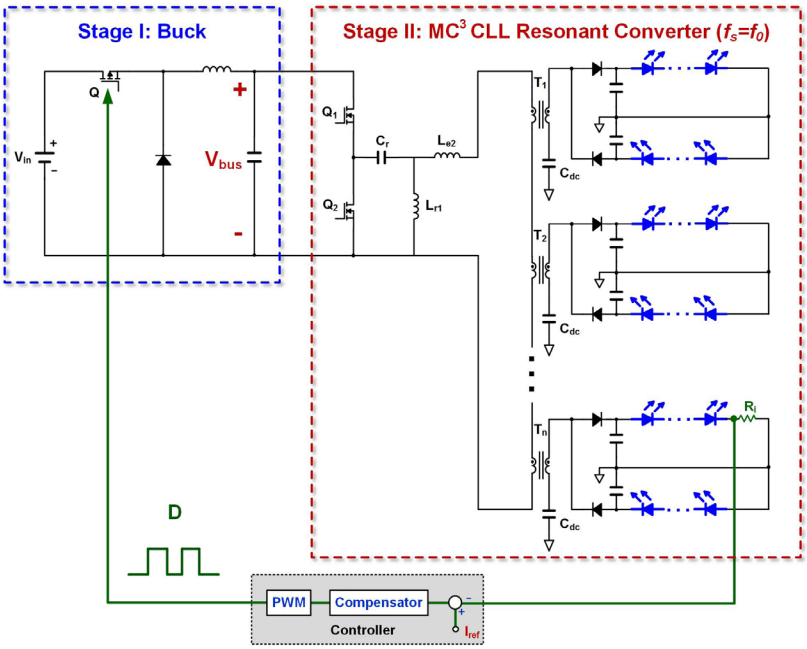


Fig. 2. Two-stage LED driver with MC³ CLL resonant converter

The CLL resonant converter is a good candidate for LED driving. Because its magnetizing inductance could be very large, excellent current-sharing capability can be achieved even under unbalanced loads. Furthermore, ZVS of the primary-side switches can be achieved by optimizing L_{r1}. In addition, the leakage inductance of the transformer can be absorbed as a part of L_{e2}. Therefore, a two-stage LED driver is proposed, which consists of a buck converter as the first stage and a MC³ CLL resonant converter as the second stage, as Fig. 2 presents.

The control strategy for this two-stage LED driver is as follows. The forward current of one specific LED string is sensed for feedback control to tune the duty cycle of the buck converter. Therefore, V_{bus}, which is also the input voltage of MC³ LLC, is adjusted according to the output requirement. In addition, the MC³ LLC resonant converter is always working at the resonant frequency point, so the second stage is unregulated and it works like a DCX. Under this working condition, ZVS of the primary-side switches and the ZCS of the secondary-side rectifiers can be achieved. Therefore, the CLL can attain higher efficiency with a wide load variation.

High Reliability Capacitor Bank Design for Modular Multilevel Converters in MV Applications

Modular multilevel converters are a new topology that has gained high interest from amongst the other multilevel converters. The reasons for this interest are the modular structure and the high-quality output voltage and current, which doesn't require an output filter. One of the main disadvantage of the MMC is the high second harmonic circulating current, which causes a high-voltage ripple over the capacitor of each module.

In Fig. 1 A and B, the modular multilevel converter is shown along with each module for each of its three arms, respectively. The DC-link capacitor for the power converters can be described using equations (1), (2) and (3), in which $VCPerArm$ is the voltage of the capacitors per arm, $CPerArmMin$ is minimum total capacitor value of the arm, and $tVmax$ is the time interval of the voltage ripple.

Considering reliability and life time based on (2), the practical floating DC-Link capacitor bank is designed. Because of the design of the DC-link capacitor, usually two types of capacitor are used: aluminum electrolytic capacitors and film capacitors. Three design examples for the floating DC link capacitor are carried out to investigate the practical design issues of the capacitor bank using aluminum electrolytic and film capacitors. These three design examples are simulated, as shown in Fig. 2. The values of the capacitance in each case, which are greater than the minimum required capacitor value for the specific ripple, are shown in Table 1. For each case, three design examples are created using Cornell Dubilier aluminum electrolytic capacitors, Cornell Dubilier film capacitors, and Electronicon film capacitors.

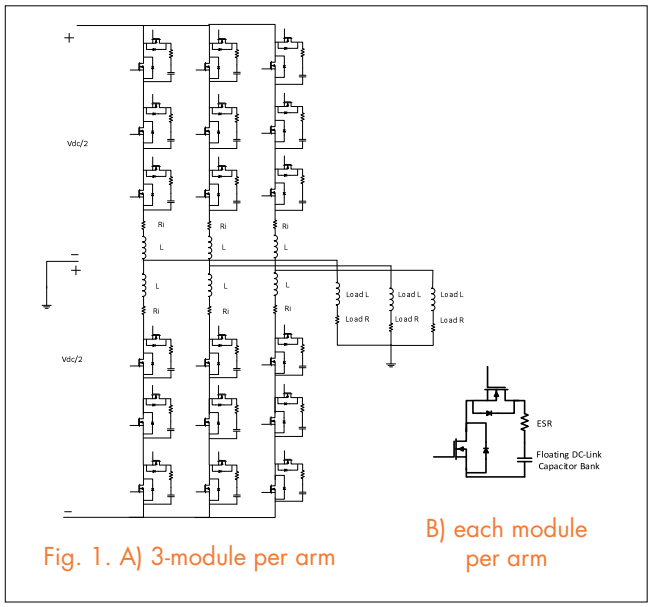


Fig. 1. A) 3-module per arm B) each module per arm

The reliability equation of the each design example in each cases are obtained and shown in Fig. 3. The failure rate of each capacitor is calculated based on the datasheets, which are provided by the manufacturer.

The result shows that in each case the design based on the film capacitor has a longer life and higher reliability than the design based on the aluminum electrolytic capacitor.

In order to increase the reliability of the aluminum electrolytic capacitor, we present the novel idea of the adding the film capacitor to the aluminum electrolytic capacitor to enhance the life time and reliability of the capacitor bank.

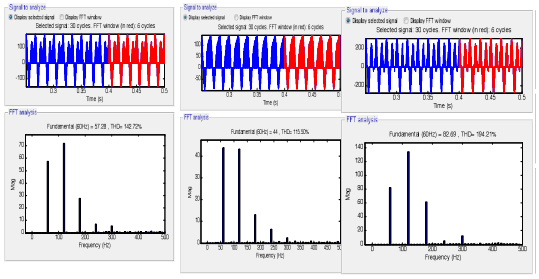
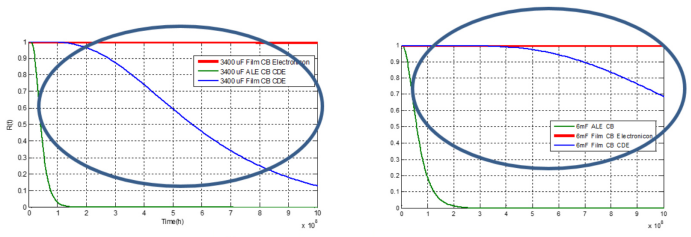


Fig. 2. Simulation for each of the three cases

Table1

CASE 1	C=3400UF
CASE 2	C=6MF
CASE 3	C=2500UF

Three-Design Case Studies



$$W = \int_0^{tVmax} P_o.dt = \frac{1}{2}C_{PerArm}(V_{CPerArm} + \Delta V_C)^2 - \frac{1}{2}C_{PerArm}V_{CperArm}^2 \quad (1)$$

$$C_{PerArmMin} \geq \frac{P_O(t_{Vmax})}{\left(V_{CPerArm}\Delta V_C + \frac{1}{2}V_{CperArm}^2\right)} \quad (2)$$

$$C_M = \frac{C_{PerArmMin}}{n} \quad (3)$$

Fig. 3. Reliability function comparison among three different

Performance Projection of Vertical High-Voltage GaN power MOSFETs and Comparison to SiC power MOSFETs

In this paper, we quantitatively evaluate the dc and switching performance characteristics of GaN vertical DMOSFETs at different BV ratings (1.2 kV, 3.3 kV, 5 kV and 10 kV) using device simulation. The performance of GaN MOSFETs is then compared to reported results on 4H-SiC MOSFETs and the findings show that GaN devices offer significant improvement over SiC devices because the GaN has a higher critical electric field (3.75 MV/cm) when compared to the 4H-SiC (2 MV/cm).

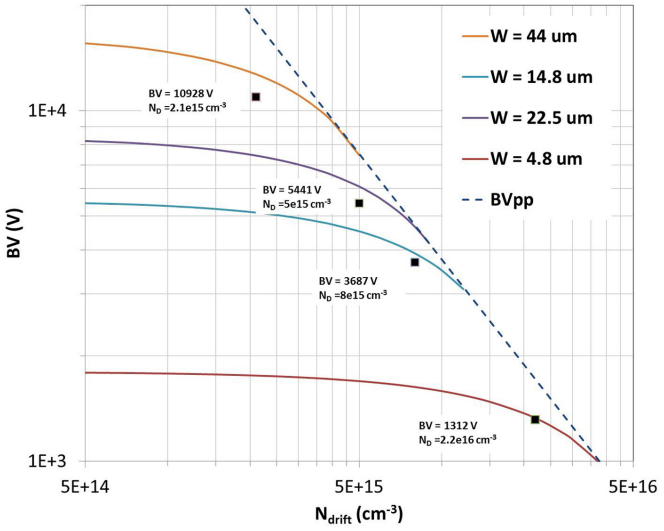


Fig. 1. Calculated punch-through breakdown for GaN as a function of drift layer doping. Solid lines correspond to the drift layer thickness used in 1.2 kV, 3.3 kV, 5 kV and 10 kV MOSFETs.

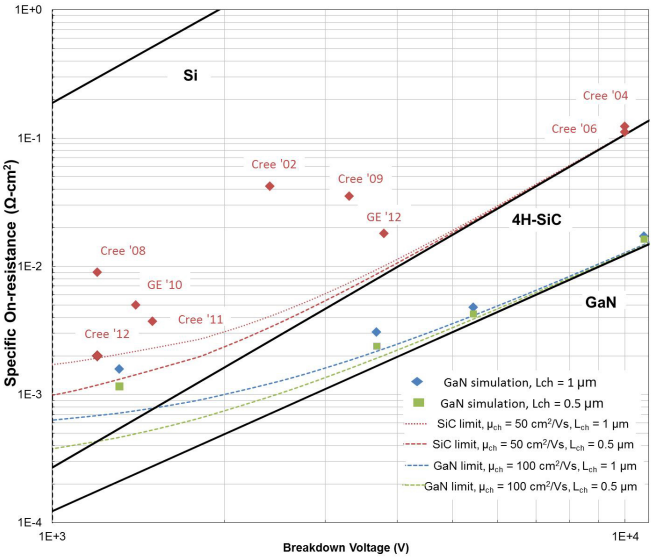


Fig. 2. $R_{on,sp}$ of simulated GaN MOSFETs and reported 4H-SiC MOSFETs as a function of BV. Solid lines represent the theoretical limits of Si, 4H-SiC and GaN.

Fig. 1 shows the calculated punch-through breakdown voltage curves for GaN at different drift layer thicknesses corresponding to the drift layer thickness used at different voltage ratings. The drift region doping and thickness is optimized to obtain the lowest drift region resistance for a given blocking voltage (highlighted by markers in Figure 1). Channel length values of 1 µm and 0.5 µm are simulated. Channel mobility of 100 $cm^2/V.s$ and an oxide thickness of 50 nm is used. Fig. 2 shows the extracted specific on resistance of the devices as a function of blocking voltage compared with the reported values for the 4H-SiC MOSFETs. A resistive switching simulation is performed with J_{on} = 100 A/cm^2, V_{DD} = rated BV. The extracted performance metrics of the GaN MOSFETs are listed in the table below. The GaN MOSFETs give a much lower on-resistance than commercially available 4H-SiC MOSFETs at all BV ratings. These simulations quantify the significant performance benefits that can be achieved by vertical GaN power devices for high frequency applications as compared to 4H-SiC power devices.

BV (V)	$R_{on,sp}$ (mΩ. cm^2)		Gate charge (nC/cm^2)			FOM ($R_{on,sp}$ x $Q_{GD,sp}$) (mΩ .nC)	FOM for 4H-SiC (mΩ.nC)
	L_{ch} = 1 µm	L_{ch} = 0.5 µm	Q_{GS}	Q_{GD}	Q_G		
1312	1.51	0.95	104	767	1410	1154	3440[3]
3687	2.99	2.37	104	704	1360	2105	
5441	4.78	4.23	104	696	1340	3326	
10928	17.1	16.3	104	680	1300	11628	9313[4]

Characteristics of Monolithically Integrated LED/Power MOS Channel HEMT Pair in GaN with Selective Epi Removal

We report the first demonstration of monolithically integrated LEDs and power MOS Channel-HEMTs (MOSC-HEMTs) in GaN. Monolithic integration of GaN-based LEDs and GaN power switching transistors, such as MOSFETs, HEMTs, and MOSC-HEMTs, can reduce the cost and the size of solid-state lighting systems, improve system reliability, and serve as a technology platform for light-emitting power ICs (LEPICs) in smart lighting applications.

The GaN LED and GaN MOSC-HEMT are monolithically integrated using the selective epi removal (SER) process approach. The starting HEMT epi is on a sapphire substrate, and an LED epi is grown in-house on top. The integrated LED and MOSC-HEMT structure is fabricated by first removing selected regions of the LED structure to expose the HEMT epi using ICP-RIE. Subsequent fabrication processes of the LED and MOSC-HEMT are carried out with multiple shared steps. Finally the interconnection metal connects the LED cathode to the MOSC-HEMT drain, forming a series configuration, as shown in Fig. 1.

Detailed electrical and optical characteristics of the integrated GaN LED/HEMT pair are measured at 25° and up to 225°. The GaN LED emits a bright blue light, which is directly driven by the integrated MOSC-HEMT. The room-temperature (25°) LED current and light output intensity are measured as a function of the supply voltage and the HEMT gate voltage, showing that the light output has been successfully modulated by the gate voltage of the MOSC-HEMT with good linearity (Fig. 2). With the temperature rising, the light output power at the same driving current of the LED/HEMT pair shows an obvious decrease. The results demonstrate the compatibility of III-nitride LED and HEMT processes. The high-temperature performance of the integrated GaN LED is comparable to that of discrete GaN LEDs. The integrated GaN LED emission spectrum is dependent on current and temperature. A dominant wavelength of 459 nm has been extracted, with a FWHM as small as 22 nm.

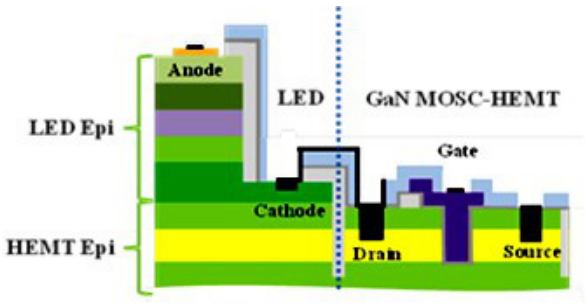


Fig. 1. Cross-section view of the monolithically integrated GaN LED and GaN MOSC-HEMT

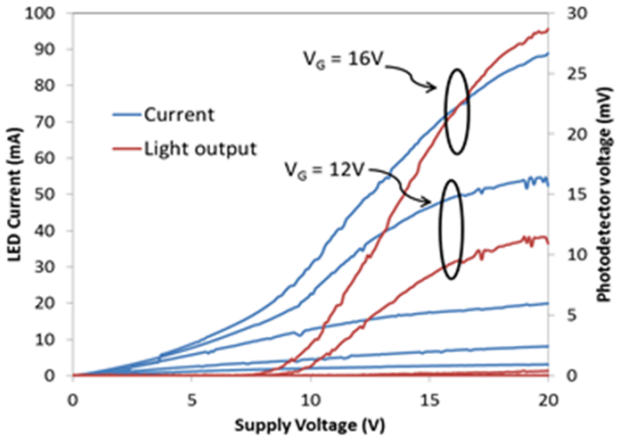


Fig. 2. Room temperature (25° C) current and LED light output intensity of the LED/HEMT pair

1200V Bi-Directional Si DMOS IGBT Fabricated with Fusion Wafer Bonding

A promising application in the fabrication of two-sided, bi-directional power semiconductor devices is the bonding of silicon wafers. With proper process technologies, bipolar devices such as IGBTs, which require an optimum level of minority carrier transport across the bonded interface, can be realized. Figure 1 demonstrates a 3300V, bi-directional functional IGBT, which is achieved by bonding two front-side processed, thinned wafers back-to-back. Previous researchers have used a custom mechanical apparatus to align wafers in vacuum. Applying this wafer bonding approach to lower BD IGBTs becomes increasingly difficult due to the decreasing wafer thickness and the increasing likelihood of wafer breakage during wafer handling, cleaning and bonding steps. In addition, the bonding temperature must be constrained up to the maximum sintering temperature (typically 400-450° C) to ensure metal contact reliability while the two wafers or dice must not delaminate (even partially) at any step after wafer bonding.

In this paper, we report results demonstrating that a flat and clean surface is the key requirement for a hydrophobic bonding process producing an electrically transparent junction. Wafers can receive final polish and scrub clean after being thinned down to a thickness of 150□m by mounting them onto glass carriers using a benzocyclobutene based resin (BCB). After diffusion groove fabrication, surface cleaning, and dilute HF treatment, the wafers are aligned back to back and then bonded with a slow ramp rate to 400° C. They must stay at 400° C for 24 hours under atmospheric vacuum and mechanical pressure. After bonding, the glass carriers delaminate from the bonded pair, since the BCB between silicon device wafers and the glass carrier wafers is degraded during the 400° C silicon bonding process.

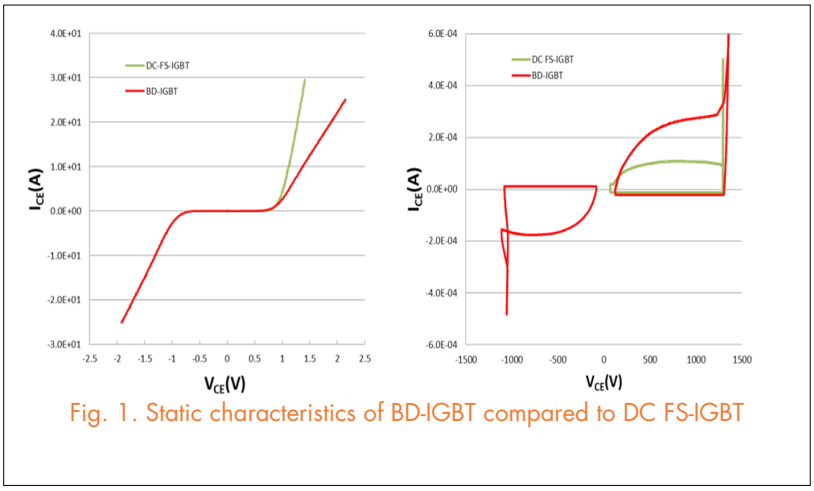


Fig. 1. Static characteristics of BD-IGBT compared to DC FS-IGBT

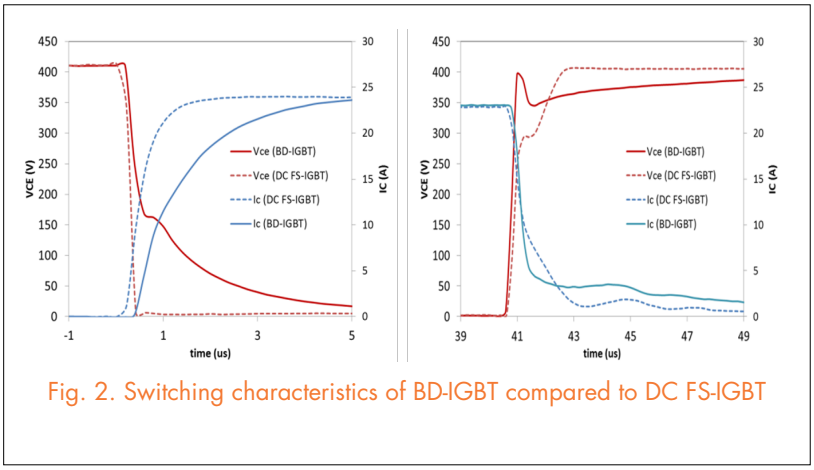


Fig. 2. Switching characteristics of BD-IGBT compared to DC FS-IGBT

Static and dynamic measurement was performed using a Tektronix 371A curve tracer. The forward conduction and breakdown characteristics are shown in Figure 1. The forward voltage drop was measured at 2.2 V in the first quadrant and 1.9 V in the third quadrant at a current of 25 A, while the breakdown voltages were measured at 1400 V in the first quadrant and 1050 V in the third quadrant at a current of 500μA. The testing result implies that a good electrically transparent bonding interface is achieved. For switching performance, the turn-on and turn off characteristics at a current of 15 A are illustrated in Figure 2.

In summary, the bi-directional IGBT has been successfully fabricated and characterized. The electrical results demonstrate the feasibility of low temperature hydrophobic wafer bonding to achieve good static and dynamic performance.

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