A Reliable CMOS Receiver for Power Line Communications in Integrated Circuits

Jebreel Mohamed Muftah Salem

Thesis submitted to the faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

Dong S. Ha, Chair
Kwang-Jin Koh
Majid Manteghi

December 11, 2012
Blacksburg, VA

Keywords: Power Line Communications, PLC Receiver, ASK Modulation, Voltage Supply Variations

A Reliable CMOS Receiver for Power Line Communications in Integrated Circuits

Jebreel Mohamed Muftah Salem

(ABSTRACT)

Power line communications (PLC) in integrated circuits (ICs) was proposed by Dr. Dong S. Ha' group in 2005. Their goal was to utilize the power distribution network for data communications as well as delivery of power, so that the routing overhead can be avoided and the number of pins in the chip can be reduced. Dr. Ha's group demonstrated through measurements the existence of pass-bands in the power distribution networks and the feasibility of power line communications in ICs. Several PLC receivers were developed to recover data superimposed on the power lines of an IC. This thesis research investigated a new PLC receiver to improve shortcomings of previous PLC receivers, specifically to improve the reliability while reducing power dissipation.

The proposed PLC system adopts an amplitude shift keying (ASK) modulation to transmit and detect data through power distribution networks. The proposed PLC receiver consists of three main sub-blocks. The first sub-block is a level shifter, which lowers the offset voltage of the supply voltage to approximately $0.5V_{DD}$. The second sub-block is a signal extractor, which detects a data signal superimposed on the power line. The signal extractor is a differential amplifier, in which one input is connected through an RC low-pass filter. The DC voltage of the data signal varies in accordance with the supply voltage fluctuations and droop. The low-pass filter intends to pass only the DC term of the data signal. Since the DC voltage is common for both inputs of the differential amplifier, it is removed from the data signal through the common mode rejection of the differential amplifier. Therefore, the signal extractor can mitigate supply voltage fluctuations and droops. The last sub-block is the logic restorer, which converts the differential signal to a logic value based on a Schmitt trigger. The hysteresis of the Schmitt trigger improves the noise immunity of the receiver.

The proposed PLC receiver is designed and fabricated in CMOS 0.18 μm technology under the supply voltage of 1.8 V. Measurement results of the three sub-blocks and the entire PLC receiver are presented and compared with simulation results. The data rate for the measurements is set to 10.0 Mbps, and the ASK modulation scheme adopts V_{DD} (= 1.8 V) for logic 0 and 90 mV above V_{DD} for logic 1. The measurements show that the PLC receiver can tolerate the supply voltage drop by 0.423 V or 23.0%. The power dissipation for the receiver is 3.2 mW under 1.8 V supply. The core area of the receiver is 72.2 μm x 74.9 μm.

To my parents, sisters and brothers

Acknowledgements

First and foremost I would like to offer my sincerest gratitude and appreciation to my advisor, Dr. Dong S. Ha, who has guided me throughout my thesis with his invaluable patience, advices, and knowledge. I would like to thank him for being an excellent advisor, and I am also looking forward to working with him toward my PhD study. One simply could not wish for a more tolerant and friendlier supervisor. I would like to thank Dr. Kwang-Jin Koh and Dr. Majid Manteghi for being part of my advisory committee and providing me with valuable advice and feedback.

I would like to thank the Canadian Bureau for International Education (CBIE) for supervising my scholarship. Especially, I am thankful to my direct advisor Ms. Sarah Levinson for her effort in facilitating my scholarship. In addition, I would like to thank Texas Instruments for providing the fabrication services for the test-chips.

Also, I would like to thank my colleagues, Carlos Quemada, Ji-Hoon Jeong, Jeong Ki Kim, Jinsik Yun, John Turner, Maruf Newaz Ahmed, Na Kong, and Travis Cochran. It was a great pleasure working with them for the past two years. Also, many thanks go to my colleagues with the MICS group for their support and encouragement and for making the stay at MICS more enjoyable. I am also grateful for Yumi Lim for her help and support during my study. Also, I would like to thank Virginia Tech staff, Dr. Leslie Pendleton, Ms. Cynthia Hopkins, Mr. John Harries, and Mr. Randall Nealy for their great help throughout my Master's study. I am grateful to all the professors and mentors who have helped me throughout my career, both in Libya and the United States.

Special thanks go to my best friend, Hesham Elmkharram, for his support and help. Thanks to my roommates Ibraheem Rasoul and Mahmoud Elhassan for their invaluable friendship. Thanks to all my friends at Virginia Tech. Life at Virginia Tech was lively and enjoyable with you guys around!!

Finally, I am also extremely grateful to my parents, sisters and brothers for their unconditional support, love and patience. Without their encouragement and endurance, this work would not have been possible.

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

Advancement of silicon processing technologies pushes the limit of integration for today's integrated circuits (ICs). For example, an Intel Itanium® processor in 32 nm CMOS with nine copper metal layers contains 3.1 billion transistors [1]. A major constraint for a high level of integration stems from the package due to limiting factors such as I/O pin count, provision of stable power supply with large power consumption, and thermal heat removal. A limited number of I/O pins for IC packages such as those for microprocessors poses a major challenge to IC designers, who push to integrate an ever increasing number of functions in a single chip.

As the integration level of an IC increases, the number of sensors to monitor internal state of the chip such as the temperature and the supply voltage also increases. The increased need to monitor the internal state is mainly due to two factors, increasing system complexity and decreasing reliability in deep sub-micron silicon technologies. The increased system complexity simply has more nodes to monitor. The decreased reliability due to PVT (Process Voltage Temperature) variations makes the operation status of blocks and circuits less predictable, which requires deployment of more sensors. Control of those individual sensors requires dedicated pins and routings. Dedicated pins are expensive for packages with complex ICs, and routings cost expensive design hours.

A power distribution network (PDN) is ubiquitous to internal nodes of a chip. In other words, a power pin reaches any internal node through a PDN. Thus, a dual use of power pins and the PDN for data communications as well as delivery of power is highly attractive. It saves pins, and routing of the data signals to the internal nodes. It is particularly attractive to control a large number of sensor nodes, which does not require a high data rate. Further, it provides the

flexibility on placements of sensor nodes without careful preplanning due to no need for routing. The ability to communicate with internal nodes without routing data paths also opens up a possibility for fault diagnosis, monitoring transient logic values during built-in self-test and for on-line/off-line testing.

1.2 Power Line Communication Systems in VLSI Circuits

Power line communication (PLC) in VLSI circuits was proposed by Dr. Dong Ha's group to control internal nodes of an IC [2]-[6]. A PLC system achieves communications between an external control module and one or multiple internal nodes of an IC through the power distribution network. The goal of the proposed research is to reduce the cost of complex ICs through reduction of the number of pins required to control internal nodes. The external transmitter of our PLC system superimposes the data on the power supply and sends the data through a power pin(s) and the power distribution network of the IC to an internal node(s) without affecting the performance of the chip. The PLC receiver at an intended node extracts the data from the power distribution network. Each receiving node has a pre-assigned unique identification code, which enables the data to be delivered to the intended node(s).

Figure 1.1 shows a PLC system in a VLSI circuit environment. The Test/Control module sends data superimposed on a power line of the system board. The signal travels through a power pin(s), power planes of a package, and the power distribution network and reaches at the intended node(s). The channel characteristics of the power distribution network of a target IC are important to select proper frequency bands, and measured results on channel characteristics of Intel processors are available in [6].

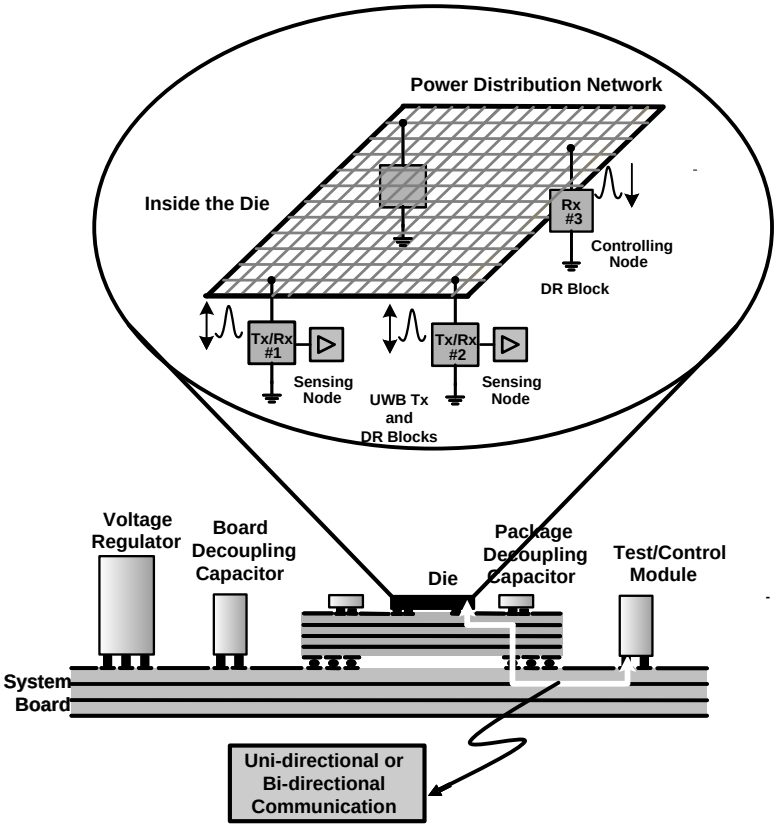


Figure 1.1: Power line communication system in a VLSI circuit

1.3 Review of PLC Receivers in Integrated Circuits

The proposed topic of the thesis research is to develop a PLC receiver in CMOS technology. A few of PLC receivers in CMOS were developed by Dr. Dong S. Ha's team [8]-[10]. The PLC receivers demonstrate feasibility of power line communications in ICs. The PLC receiver proposed by Thirugnanam et al. in [8] is composed of a sensing circuit, a differential amplifier with an offset cancellation, and a positive feedback latch. The offset cancellation, which removes the DC voltage of the signal, is based on a fixed bias voltage, and is sensitive to supply voltage fluctuations. The PLC receiver was designed in CMOS 0.18 um technology. The PLC receiver proposed by Chawla et al. in [9] adopts a coherent detection for ultra wideband (UWB) data signals. It achieves a higher sensitivity than its predecessor owing to the coherent detection, but dissipates more power due to higher circuit complexity. Like its predecessor, the PLC receiver also relies on a fixed bias voltage to remove the DC voltage from the signal and

hence suffers from the same shortcoming. The PLC receiver was designed in CMOS 0.18 μm technology initially, and was also developed in 0.13 μm CMOS technology later [10].

1.4 Technical Contributions of the Proposed Research

The research work of this thesis was to improve previous PLC receivers developed by Dr. Ha's group and to design and fabricate a test chip. The three major design objectives of the PLC receiver are to mitigate supply voltage fluctuations and droops, to improve the noise immunity, and reduce power dissipation. The main research contributions of this thesis work are as follows.

First, we designed a PLC receiver, which can mitigate supply voltage fluctuations and droops. A differential amplifier with a low-pass filter on one input is adopted for our PLC receiver, which improves resilience to low frequency voltage fluctuations and is effective for voltage droops.

Second, a Schmitt trigger with hysteresis is adopted to increase the noise immunity. The switching voltages of the Schmitt trigger are in synchronous with the clock, which changes the two threshold voltages to further improve the noise immunity.

Third, a non-coherent is adopted for the PLC receiver, which reduces the circuit complexity to lower power dissipation.

Fourth, the proposed PLC receiver was fabricated in CMOS 0.18 μm technology, and measurement results on a test chip are reported in this thesis.

1.5 Organization of the Thesis

The organization of the thesis is as follows. Chapter 2 provides background and preliminaries for the proposed research work. The requirements for PLC receivers in ICs are discussed, and two PLC receivers in ICs designed by Dr. Ha's former students are briefly reviewed. Binary amplitude shift keying (ASK) modulation, which is adopted for our PLC system, and its probability of symbol error and energy per bit noise ratio are covered. Finally

operation of two building blocks of the proposed PLC receiver is discussed. Chapter 3 presents the proposed PLC receiver consisting of three building blocks, a level shifter, a signal extractor, and a logic restorer. Design of the three blocks in CMOS 0.18 μm is described and simulation results to verify the operation of the logic restorer are presented. Chapter 4 presents post-layout simulation and measurement results of a test chip. Measurements were performed with three individual building blocks first followed the entire receiver, and the results on individual blocks as well as the entire chip are presented. The performance of the receiver at different operating conditions and power consumption of individual blocks are also reported. Lastly, Chapter 5 draws a conclusion on the proposed PLC receiver design and suggests a few areas to improve as future research.

Chapter 2

Preliminaries

This chapter provides preliminary topics and the previous research activities that are necessary to understand the proposed Power line communication (PLC) receiver and the contributions of this thesis research. Section 2.1 provides the characteristics of power supply voltage at ICs and gives a set of typical target requirements as a reference for the proposed PLC receiver. Section 2.3 reviews the previous PLC receivers. Section 2.3 describes amplitude shift keying (ASK) modulation scheme adopted for the proposed PLC. Section 2.4 briefly describes a Schmitt trigger circuit, which is a major building block of our PLC receiver. Section 2.5 explains the power supply rejection ratio (PSRR) of amplifiers, and the property of PSRR is exploited for our design. Section 2.6 summarizes the chapter.

2.1 Requirements

The supply voltage of an IC varies spatially across the IC as well as in time. Supply voltage may vary because of the non-ideal voltage regulator, IR drop, Ldi/dt noise, and varying power consumption of blocks connected to the same power line. Figure 2.1 shows a supply voltage map indicating the worst case voltage droop on a chip [11]. The map indicates that the supply voltage droop ranges from 3 to 15% of V_{DD} across the chip area. The problem could be worsened for devices powered by batteries as the battery voltage drops over the operating period. Therefore, supply voltage fluctuation is critical issue for IC design.

Superposition of the data signal on power lines should not affect the integrity of the supply voltage, and variation of the supply voltage for ICs should remain less than ±10% of the voltage supply [12]. Like any communication system, the bit-error-rate is an important parameter

for the proposed receiver. A low bit-error-rate (BER), desirably less than 10^{-6}, would be necessary to apply our receiver for testing and diagnosis purpose of ICs, and adoption of an error coding scheme may be necessary in addition to a high performance PLC receiver. The above requirement combined with a high level of noise on power lines in ICs makes a PLC receiver design challenging.

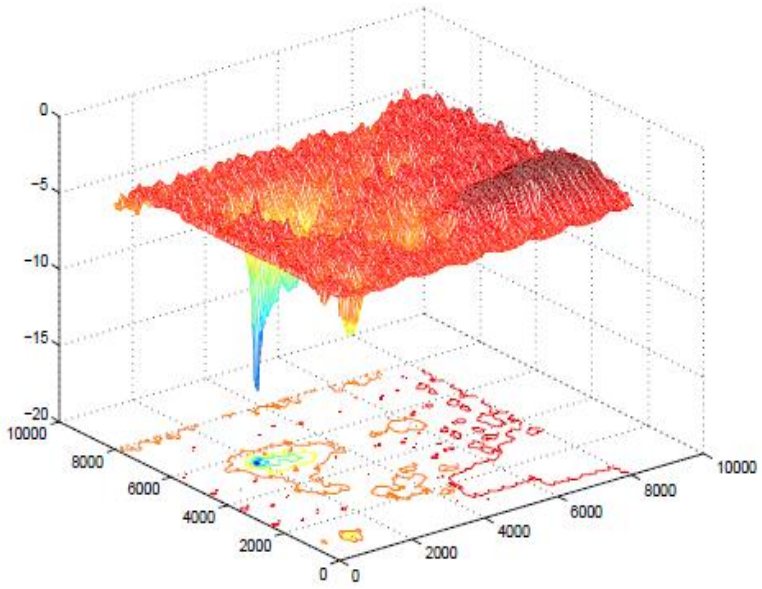


Figure 2.1: A power supply voltage map, H. Su, F. Liu, A. Devgan, E. Acar, and S. R. Nassif, ‘‘Full Chip Leakage Estimation Considering Power Supply and Temperature Variations,’’ Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED), 2003, pp. 78–83. Used under fair use, 2012.

2.2 Previous PLC Receivers in ICs

Measurement results in the frequency response of power distribution networks performed by Dr. Ha’s group show the existence of pass-bands for Intel processors [6]. A couple of PLC receivers were proposed by Dr. Ha’s former students, Rajesh Thirugnanam and Vipul Chawla, and their designs are reviewed in the this section [6]-[7].

2.2.1 Thirugnanam PLC Receiver

The PLC receiver proposed by R. Thirugnanam in [6] is shown in Figure 2.2. It consists of a sensing circuit, a differential amplifier, and a latch. The sensing circuit, which is simply a common source with diode connected load, detects the transmitted signal in the power line and shifts the DC level of the signal down. The output of the sensing circuit, which is single ended, is applied to a differential amplifier. One input of the differential amplifier is connected to a constant reference voltage, and the other input to the drains of M_3 and M_4 whose gates are connected to the clock signal. When the clock signal is low, the output of the sensing circuit is connected to the input of the differential amplifier, and the amplifier amplifies the sensed signal and compares it with the reference signal. When the clock is high, M_3 is off and M_4 is on. The amplifier is disconnected from the sensing circuit, and the M_5 acts as diode with resistance $1/g_m$. The output of the differential amplifier is connected a latch, consisting of back-to back inverters. The latch converts the output of the differential amplifier to the supply rails, i.e., logic values. The transistor M_9 enables the latch to sample at the falling edge.

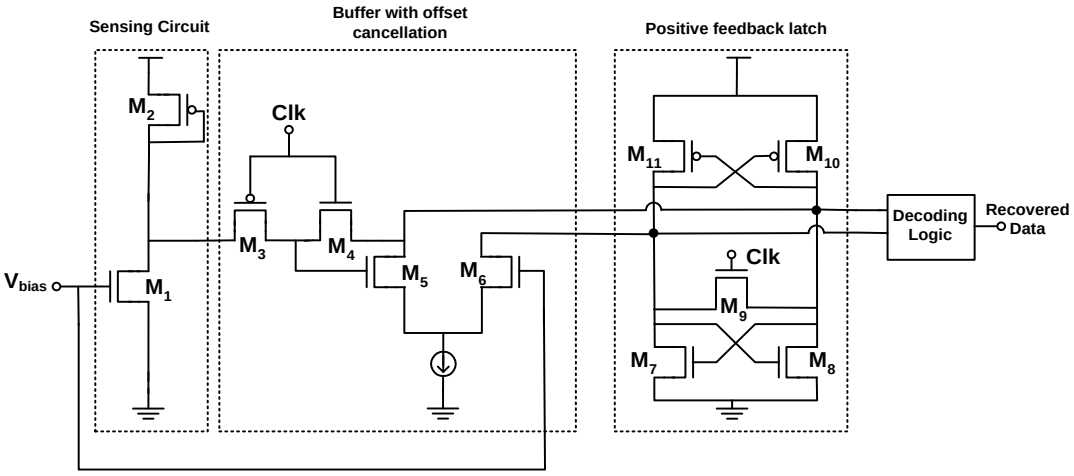


Figure 2.2: PLC receiver proposed by R. Thirugnanam, "The dual use of power distribution networks for data communications in high speed integrated circuits," Ph.D. dissertation, Department of Electrical and Computer Engineering, Virginia Tech, 2006. Used under fair use, 2012.

A shortcoming of the PLC receiver is that the offset voltage at the output of a differential amplifier is directly affected by the fluctuation of the supply voltage. The offset voltage may pull up or down the latch according the fluctuation of the supply voltage to disrupt the operation.

Also, the turn-on resistance associated with M_3 weakens the strength of the output signal to reduce the sensitivity of the receiver.

2.2.2 Chawla PLC Receiver

The block diagram of V. Chawla's receiver is shown in Figure 2.3. The receiver consists of a sensing and amplifying circuit, a merged mixer integrator, and a comparator. The sensing circuit senses and amplifies impulse data on the power line, while shifting down its DC level. A merged mixer-integrated circuit correlates the received signal with a template signal generated by a template generator. The output of the merged mixer-integrator is applied to a comparator, which translates the sensed pulses to logic values.

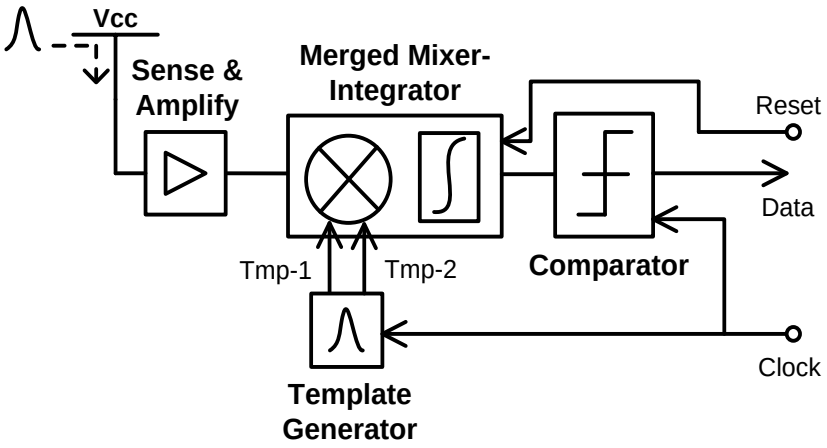


Figure 2.3: PLC receiver proposed by V. Chawla, "power line communications in microprocessors - system level study and circuit design," M.S. thesis, Department of Electrical and Computer Engineering, Virginia Tech, 2009. Used under fair use, 2012.

The sensing and amplifying circuit is shown in Figure 2.4. It is simply a cascaded two stage of the differential amplifier. One of the inputs of the first amplifier is connected to the supply voltage, and the other one connected to a RC filter tied to the supply voltage. The filter extracts the DC voltage of the impulse signals superimposed on the power line.

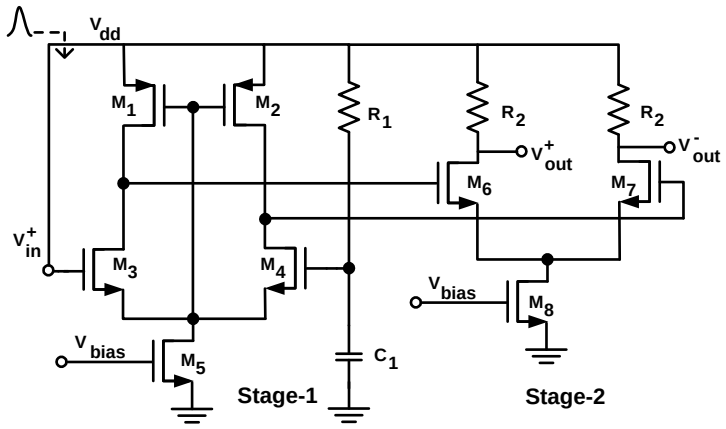


Figure 2.4: Sensing and amplifying circuit proposed by V. Chawla, "power line communications in microprocessors - system level study and circuit design," M.S. thesis, Department of Electrical and Computer Engineering, Virginia Tech, 2009. Used under fair use, 2012.

The merged mixer-integrator circuit is shown in Figure 2.5. The lower portion of the circuit consists of two single-balanced mixers with cross-coupled outputs. The mixer outputs are loaded with capacitors C1 and C2. The transconductors (M_{15} and M_{16}) at the bottom of the two single-balanced mixers are driven by two similar, but time separated, template signals. The template signals are digital impulses generated by Template Generator.

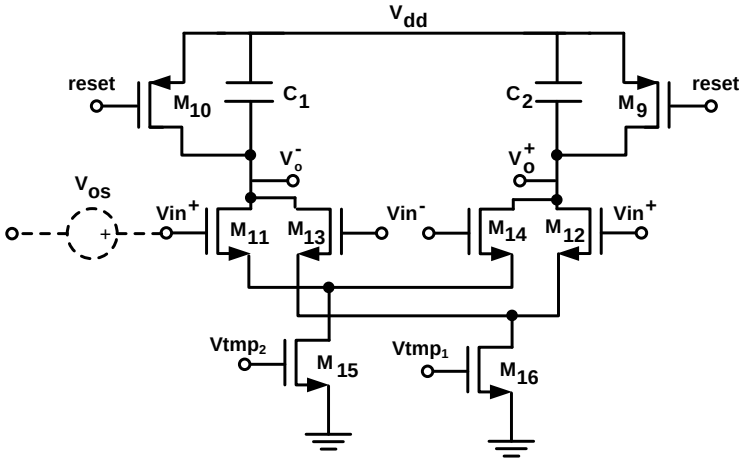
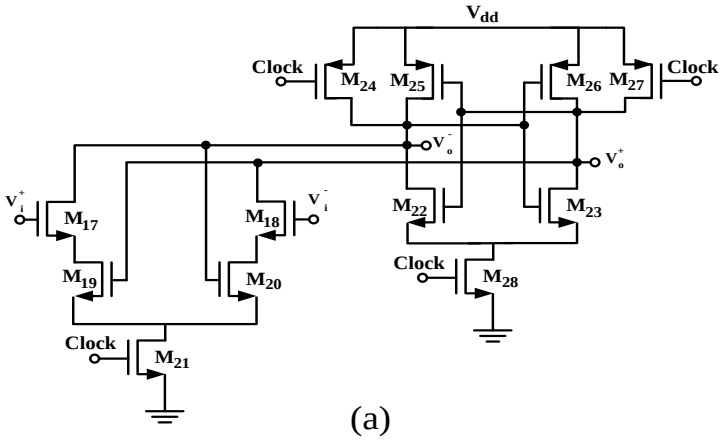
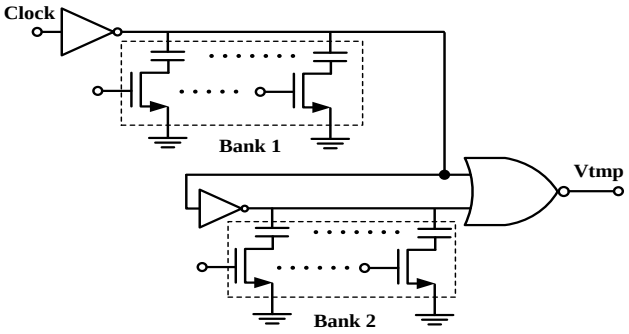


Figure 2.5: A merged mixer- integrator circuit proposed by V. Chawla, "power line communications in microprocessors - system level study and circuit design," M.S. thesis, Department of Electrical and Computer Engineering, Virginia Tech, 2009. Used under fair use, 2012.

The comparator circuit shown in Figure 2.6 (a) converts the impulses into digital. It has an input gain stage and a regenerative latch stage. The input stage consists of $M_{17} - M_{21}$, where M_{17} and M_{18} are input transistors and M_{19} and M_{20} are included to minimize static current of the input stage. A regenerative latch is back-to-back inverter pairs. The template generator circuit diagram is illustrated in Figure 2.6 (b). One of the inputs to the NOR gate is inverted with respect to the other by introducing an inverter. Every time the input switches from V_{dd} to 0, a glitch is generated at the output (V_{tmp}), which serves as the template waveform for the correlation. The glitch duration is adjusted by controlling the delay between the two inputs of the NOR gate with the aid of switched capacitor bank 2. A template is generated at every clock transition from 0 to V_{dd}. The switched capacitor bank 1 synchronizes the template waveform with the received impulse by controlling the delay.



(a)



(b)

Figure 2.6: (a) A comparator circuit and (b) A template generator circuit proposed by V. Chawla, "power line communications in microprocessors - system level study and circuit design," M.S. thesis, Department of Electrical and Computer Engineering, Virginia Tech, 2009. Used under fair use, 2012.

The main advantage of the PLC receiver is that it can mitigate the voltage fluctuation effectively. However, the receiver is complex to consume large power, notably use of two differential amplifiers for the sensing stage and the merged mixer-integrated in the second stage. Also, the large number of transistor for the PLC contributes more noise on the input of the comparator, which is rather sensitive to the noise due to adoption of one threshold voltage.

2.3 ASK Modulation

Binary amplitude shift keying (ASK) modulation is adopted for our PLC receiver. Binary ASK is attractive for low data rate systems due to simple modulation and demodulation schemes, which lead to low power consumption. Figure 2.7 shows the relationship between probability of symbol error and energy per bit to noise ratio (E_b/N_o). To achieve the bit error rate of 10^{-6}, the binary ASK (in which M=2) requires more than 11.0 dB of E_b/N_o . Note that the symbol rate is equal to the bit rate for binary ASK. At the same time, the data signal should not be excessive to maintain the integrity of power supply. Adoption of an error correction scheme is a solution to meet the both requirements.

An ASK demodulator consists of three stages, an envelope detector, an average detector, and a comparator. ASK demodulator circuits can be classified into voltage-mode, current-mode, and mixed-mode, and three different types of circuits are illustrated in Figure 2.8. The data for a voltage-mode ASK demodulator is represented as the nodal voltage and is shown in Figure 2.8 2.8 (a) [14] An inverting amplifier amplifies the voltage of the received signal, and the modulated signal is reconstructed by the OR gate. The low-pass filter removes the noise and extracts the envelope from the carrier, and the comparator recovers the digital data based on the threshold voltage. A voltage-mode ASK demodulator has a lower circuit complexity compared with the other two modes as it does not require a conversion between voltage and current. The data is represented as the branch current for a current-mode ASK demodulator and is illustrated in Figure 2.8 (b) [15]. The modulated signal is rectified by the current mode squarer with a small impedance, and the carrier signal is eliminated using a 3^{rd}-order G_m-C lowpass filter. A level detector extracts the digital data from the envelope information. The data for a mixed-mode ASK

demodulator is represented in both nodal voltage and branch current, which intends to benefit the advantages of both modes. An example of mixed-mode demodulator is shown in Figure 2.8 (c) [16]. The operational transconductance amplifier (OTA) converts the input voltage into current, and the current mode envelope detector. The current level detector translates the current into digital values.

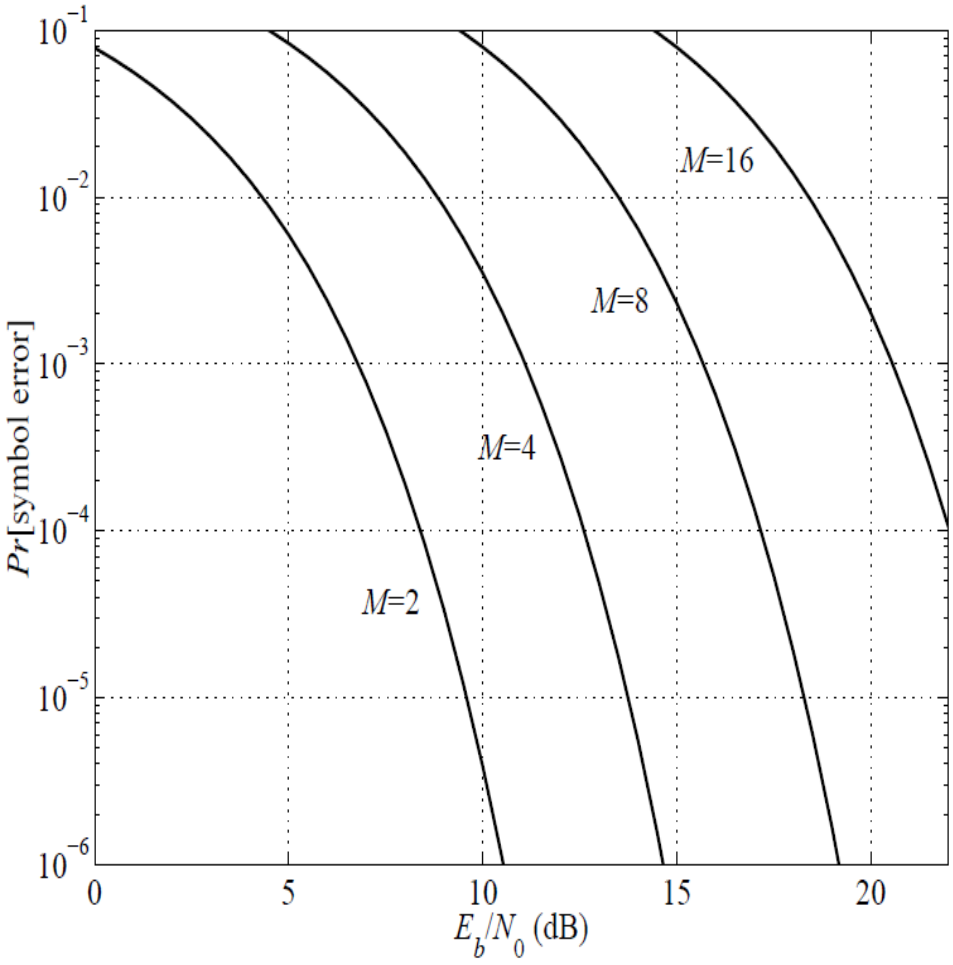


Figure 2.7: Probability of symbol error for M-ASK modulation, H. Nguyen and E. Shwedyk, A First Course in Digital Communications. Cambridge University Press, 2009.. Used under fair use, 2012.

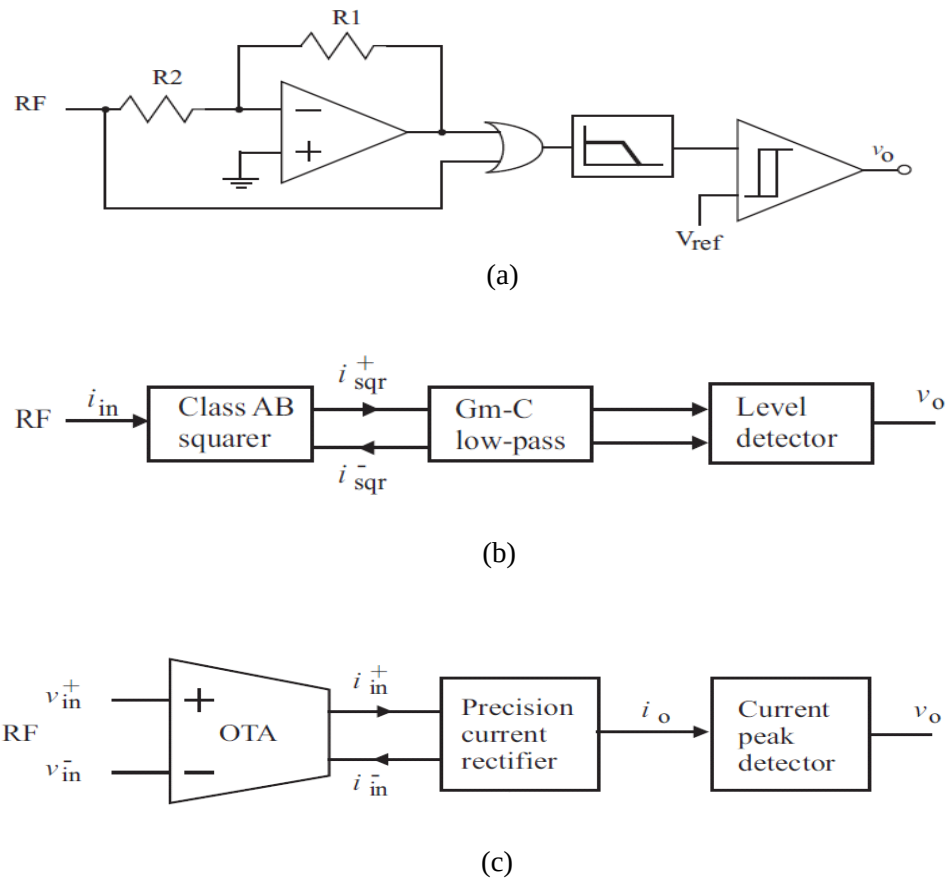


Figure 2.8: Three different types of ASK demodulator, (a) A voltage-mode ASK demodulator (b) A current-mode ASK demodulator (c) A mix-mode demodulator.

A voltage-mode demodulator is chosen for our PLC receiver due to its simplicity to have a smaller die area. It is suitable to our application since the transmitted signal is a voltage signal. Our PLC receiver adopts a Schmitt trigger with two threshold voltages instead of a comparator with one threshold voltage, which increase the noise immunity.

2.4 Schmitt Trigger

A Schmitt trigger generates a bi-stable state with two different threshold values or triggering voltages and is widely used to enhance the immunity to noise and disturbances. A Schmitt trigger determines the level of the signal instead of a comparator. A comparator has one threshold

voltage to switch from one rail to the other, and its threshold voltage is determined by

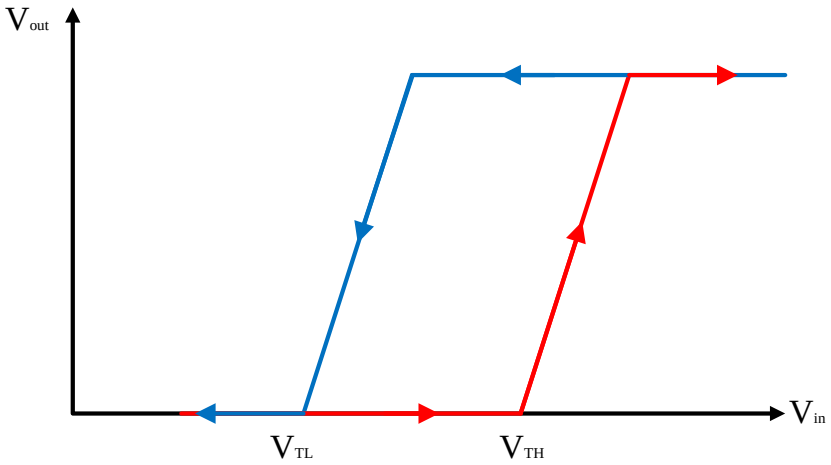


Figure 2.9: An example of hysteresis of a Schmitt trigger

the reference voltage. Unlike comparators, Schmitt triggers have hysteresis which has two threshold voltages to switch from rail to the other. The lower threshold voltage, V_{TL}, at which the Schmitt trigger switch from high to low, and the higher threshold voltage, V_{TH}, at which the output of the Schmitt trigger switch from low to high. Figure 2.9 shows an example of a Schmitt trigger hysteresis. The main advantage of having two threshold voltages is circuit becomes immune to noise variation, and this is what makes a Schmitt trigger superior to a comparator.

The advantage of hysteresis in noise environment is demonstrated in Figure 2.10. In this figure, the comparator output change as soon as the input exceeds or falls behind the threshold voltage (the blue line). On the other hand, the output of the Schmitt trigger changes from low to high when the inputs exceeds the higher threshold voltage, and change from high to low when the input falls behind the lower threshold voltage which is well below the high threshold voltage.

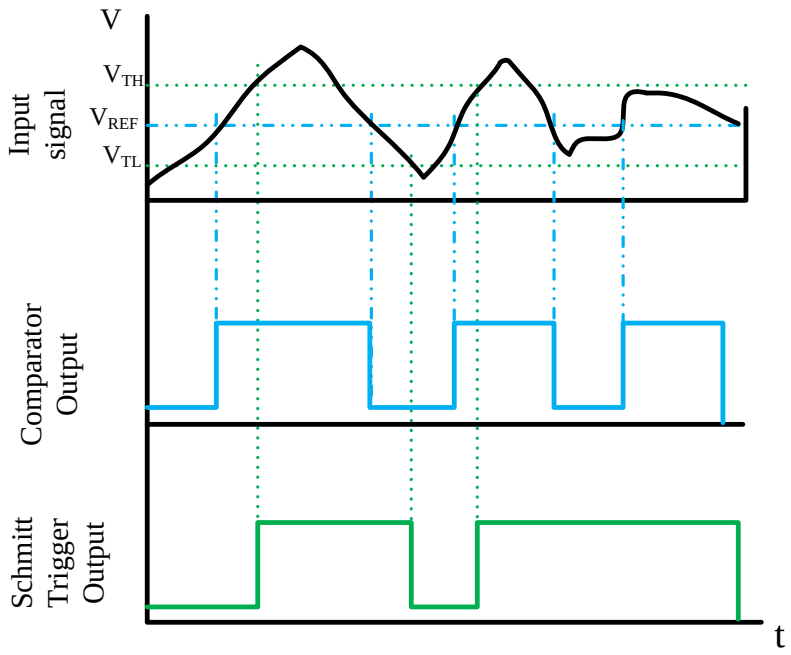


Figure 2.10: A comparison between a comparator and a Schmitt trigger output

Our PLC adopts a differential Schmitt trigger with tunable hysteresis presented in [17] and is shown in Figure 2.11. Transistors M_1 and M_2 convert input voltages v_{in+} and v_{in-} to currents I_1 and I_2, respectively. The hysteresis of the Schmitt trigger is generated using regenerative feedback which established by a cross-coupled inverter pair, $M_7 – M_{10}$, and adjusted by the load control voltage V_{tune}. M_5 and M_6 are voltage-controlled current sources. The width of M_3 and M_4 is set to be much smaller than that of M_5 and M_6, so that current of M_5 and M_6 is much greater than M_3 and M_4. M_{12} and M_{13} pull the node output of the Schmitt trigger up to V_{DD} or down to ground depending on the state of node A.

The operation of the differential Schmitt trigger is explained as follows [17]. M_1, M_2, and M_{11} with two load transistors, M_3 and M_4, form a differential amplifier (DA). Let voltage V_{in-} be fixed to V_{ref} throughout the entire operation and V_{tune} is connected to a bias voltage so that M_5 and M_6 are in saturation. Suppose the inverter pair M_7-M_{10} is inactive. The switching voltage of the DA is $V_{in+} = V_{in-} = V_{ref}$ and the currents I_{D1}, I_{D2}, I_{D5}, and I_{D6} are the same when current I_3 and I_4 are ignored. Now, suppose $V_{in+} < V_{ref}$ and the inverter pair is active with voltage V_A high and V_B low. In this case, M_7 and M_{10} are turned on. Two current sources, M_6 and $M_{10,}$ pull up the node A to high voltage while M_1 and M_7 sink the current I_5 and pull down the node B to low

voltage. $I_1 = I_5 + I_9$ and $I_2 = I_6 - I_8$. When voltage v_{in+} increase more current will be sunk through M_2 and the voltage at node A starts to decrease. Simultaneously, voltage at node B starts to increase. When the voltage v_{in+} becomes equal to V_{ref}, M_{10} is on and trying to pull up the node A and M_7 trying to pull down node B. In this case there will not be a transition at V_{ref} because M_7 and M_{10} are still on. When v_{in+} increases far above V_{ref} ($V_{ref}+\Delta V$), most of the current, I_{11}, goes through M_1 lowering the voltage at node A further which in turns switches the M_8 and M_9 on and M_7 and M_{10} off. In this case, V_A is low, and V_B is high. The output voltage, v_{out} switches from low to high. The same scenario happens when the voltage v_{in+} decreases back. The transition occurs when v_{in+} well below V_{ref} ($V_{ref}-\Delta V$).

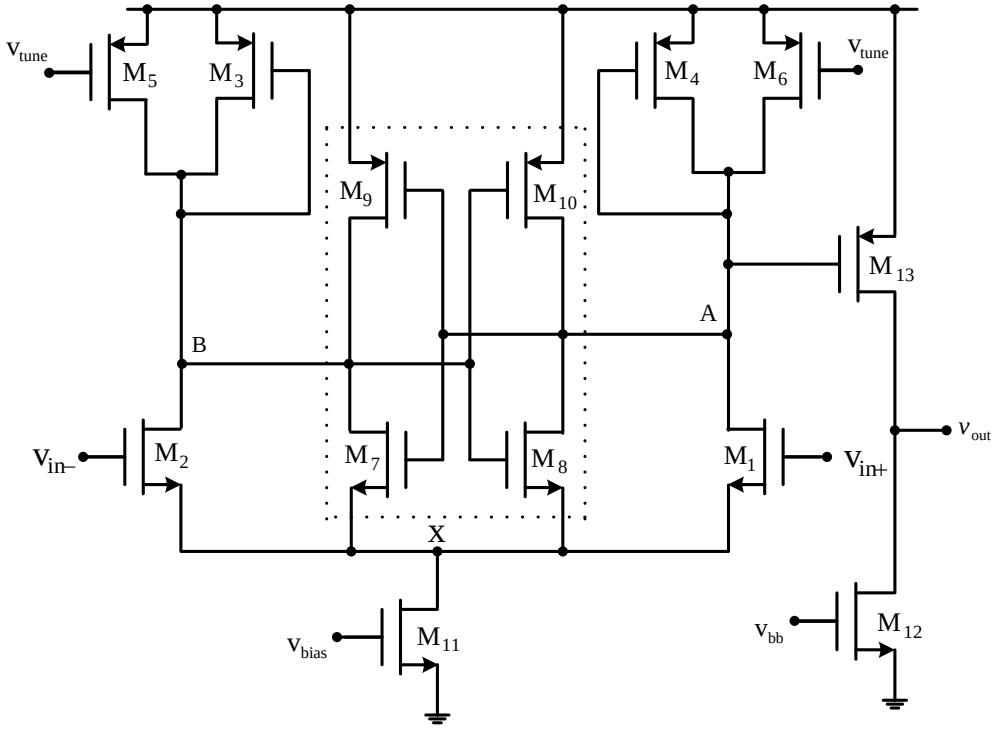


Figure 2.11: A differential Schmitt trigger with the tunable hysteresis, F. Yuan, "Differential CMOS Schmitt Trigger with Tunable Hysteresis," Analog Integrated Circuits and Signal Processing (Springer). Vol.62, No.2, pp.245 - 248, Feb. 2010. Used in fair use, 2012.

To quantify the switching voltages of the circuit at state transitions with $V_{in+} > V_{in-}$, it is noticed that when the V_A is at low voltage and V_B is at high voltage switching, transistor M_1, M_2, M_7, and M_{10} are in saturation. Since M_8 and M_9 will switch off at the end of state transition, they can be represented by open switches. To simplify the analysis, M_5, M_6, M_7, and M_{10} are

represented by ideal current sources I_5, I_6, I_7 and I_{10}, respectively, and neglect the impedances of M_3 and M_4. When the inverter pair is inactive, the input voltages can be written as:

$$V_{in+} = (V_x + V_{th}) + \sqrt{\frac{I_6}{K_1}} \tag{2.1}$$

$$V_{in-} = (V_x + V_{th}) + \sqrt{\frac{I_5}{K_2}} \tag{2.2}$$

Where V_x is the voltage at node x, V_{th} is the threshold voltage for the transistor which all are the same.

$$K = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)$$

Subtract (2.1) from (2.2), we get:

$$V_{in+} = V_{in-} + \left(\sqrt{\frac{I_6}{K_1}} - \sqrt{\frac{I_5}{K_2}}\right) \tag{2.3}$$

It can be seen from (2.3) that if the $I_6 = I_5$, and $K_1 = K_2$, then $V_{in+} = V_{in-}$, which means that the transition occurs when both inputs are equal.

Now, suppose the case when the inverter pair is active. The input voltages can be derived as:

$$I_6 = I_1 + I_8$$

$$I_6 = K_1(V_{in+} - V_x - V_{th})^2 + I_8$$

$$V_{in+} = \sqrt{\frac{I_6}{K_1}}\sqrt{1 - \frac{I_8}{I_6}} + (V_x + V_{th}) \tag{2.4}$$

Assume that the current generated by M_8 is much smaller the current generated by M_6, and

$$\frac{I_8}{I_6} << 1$$

Therefore, the following approximation can be used:

$$\sqrt{1+x} \approx 1+\frac{1}{2}x-\frac{1}{8}x^2 \ldots \approx 1+\frac{1}{2}x \text{ with } |x| << 1.$$

Equation 2.4 can be written as:

$$V_{in+} = \sqrt{\frac{I_6}{K_1}}\left(1-\frac{1}{2}\frac{I_8}{I_6}\right)+(V_x+V_{th}) \tag{2.5}$$

The similarly for the second input:

$$I_2 = I_5 + I_9$$

$$K_2(V_{in-}-V_x-V_{th})^2 = I_5 + I_9$$

$$V_{in-} = \sqrt{\frac{I_5}{K_2}}\sqrt{1-\frac{I_9}{I_6}}+(V_x+V_{th})$$

$$V_{in-} = \sqrt{\frac{I_5}{K_2}}\left(1-\frac{1}{2}\frac{I_9}{I_5}\right)+(V_x+V_{th}) \tag{2.6}$$

Now, subtract (2.5) from (2.6):

$$V_{in+} = \left(V_{in-}+\sqrt{\frac{I_6}{K_1}}-\sqrt{\frac{I_5}{K_2}}\right)-\frac{1}{2}\left(\frac{I_9}{I_5}\sqrt{\frac{I_5}{K_2}}+\frac{I_8}{I_6}\sqrt{\frac{I_6}{K_1}}\right) \tag{2.7}$$

By comparing 2.7 with 2.3, it can be seen that the second term in 2.7 is the shift in switching voltage when the inverter pair is activated. Therefore:

$$\Delta V = \frac{1}{2}\left(\frac{I_9}{I_5}\sqrt{\frac{I_5}{K_2}}+\frac{I_8}{I_6}\sqrt{\frac{I_6}{K_1}}\right)$$

2.5 Power Supply Rejection Ratio

The PSRR is defined as the ratio of the output gain from the input to the output gain from the supply voltage [18]. Consider a common source amplifier with a diode-connected load shown in Figure 2.12.

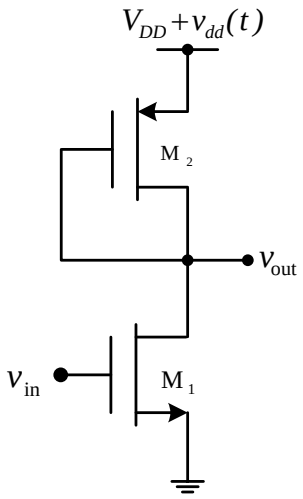


Figure 2.12: A common source amplifier

A design objective of a typical analog circuit is to isolate the circuit output from supply voltage variations, which is represented as power supply rejection ratio (PSRR), and a large PSRR is desired for typical circuits. The PSRR of an amplifier is defined as [18]:

$$\text{PSRR} = \frac{A_V}{A_{Vdd}} \tag{2.8}$$

where A_v the small-signal is gain from the input to the output, and $A_{v_{dd}}$ is the small-signal gain from the power supply to the output. The PSRR of a common source amplifier is expressed as below.

$$\text{PSRR} = -\frac{g_{m1}}{g_{m2}} \tag{2.9}$$

where g_{m_1} and g_{m_2} are the transconductance of M_1 and M_2 respectively. The transconductance of a MOS transistor is :

$$g_m = \mu C_{ox}\left(\frac{W}{L}\right)\left(V_{GS} - V_{th}\right) \tag{2.10}$$

By substituting the equation (2.10) into equation (2.9), the PSRR becomes:

$$\text{PSRR} = -\frac{\mu_n (W/L)_1 (V_{GS} - V_{th})_1}{\mu_p (W/L)_2 (V_{GS} - V_{th})_2} \tag{2.11}$$

The common source amplifier in Figure 2.12 is used for our PLC to propagate the data superimposed on the power line to the output. Hence, the supply voltage variations should appear at the output. Therefore, the PSRR of the amplifier should be degraded. It can be seen from equation (2.11), the PSRR can be lowered if the size and overdrive voltage of transistor M_1 are chosen to be small and the size of the transistor M_2 is chosen to be large.

2.6 Chapter summary

In this chapter, several topics related to the proposed work were reviewed. Firstly, an overview of a power line communication system in VLSI circuits was presented. Then, the requirements and the challenges were discussed. It was discussed that the voltage fluctuation, signal integrity and noise effects are the major challenges of the receiver. This chapter also reviewed the previous PLC receivers, specifically those by Thirugnanam and Chawla. Binary amplitude shift keying (ASK) modulation and the relationship between probability of symbol error and energy per bit to noise ratio were described. Circuit configurations of ASK demodulators were also discussed. Finally, two circuits, a Schmitt trigger and a common source amplifier, which are adopted for the proposed PLC receiver, were covered. A Schmitt trigger in terms of its operation and a common source amplifier with respect to power supply rejection ratio were described.

Chapter 3

Proposed PLC Receiver

The proposed PLC receiver intends to control internal logic values of ICs for applications such as testing and diagnosis. Therefore, a high data rate is not a design concern. Rather, a reliable operation under supply voltage fluctuations, droops, and noise, along with low power dissipation, are the primary design objectives. The chapter describes circuit design of the proposed PLC receiver, specifically three building blocks, a level shifter, a signal extractor, and a logic restorer. The proposed PLC receiver is designed and fabricated in CMOS 0.18 μm technology under 1.8 V supply.

3.1 Block Diagram

The proposed PLC receiver adopts the binary amplitude shift keying (ASK), in which a signal level higher than $V_{DD} + V_{TH}$ represents logic 1 and a signal level lower than $V_{DD} + V_{TL}$ represents logic (0), where V_{TH} and V_{TL} are preset high and low threshold voltages, respectively. A block diagram of the proposed PLC receiver is shown in Figure 3.1.

The PLC receiver mainly consists of three different blocks. The first block is a level shifter, which lowers the DC level of the signal superimposed on the supply voltage, so that the level-shifted signal can be processed by the following signal extractor. The subsequent block, a signal extractor, amplifies the signal and converts it to a differential signal. The logic restorer, which is a Schmitt trigger, recovers logic values from the analog signal. The logic restorer has a differential input and translates the sensed analog signal into a logic value based on the threshold of its hysteresis.

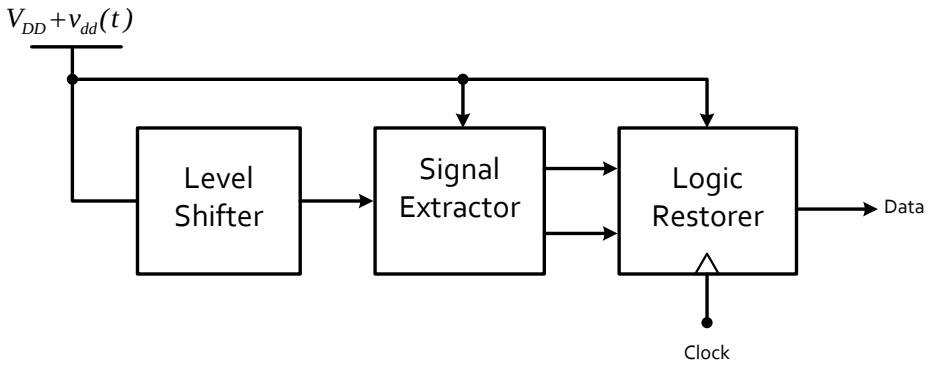


Figure 3.1: Block diagram of the proposed PLC receiver

3.2 Level Shifter

The level shifter adopts the common source amplifier with a diode-connected load as shown in Figure 3.2, in which V_{in} is a fixed bias voltage. The level shifter propagates the data signal v_{dd}(t) imposed on the supply voltage V_{DD} to the output, while lowering the DC voltage level of the signal v_{dd}(t) to one half of V_{DD}.

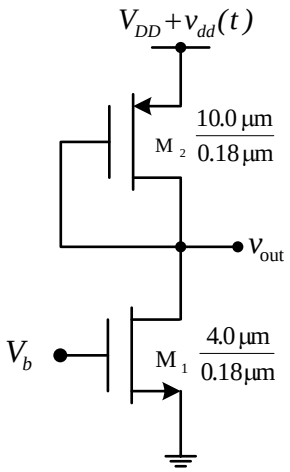


Figure 3.2: Level shifter

To propagate the data signal superimposed on the power line to the output, the output should be sensitive to power supply variations. In other words, contrary to typical amplifier design, the PSRR of the level shifter should be set to small. The PSRR of the level shifter given in (2.5) is shown again below.

$$PSRR = -\frac{g_{m1}}{g_{m2}} = -\frac{\mu_n (W/L)_1 (V_{GS} - V_{th})_1}{\mu_p (W/L)_2 (V_{GS} - V_{th})_2} \quad (3.1)$$

Equation (3.1) shows that the PSRR can be lowered through a small W/L and a small overdrive voltage of M_1 and a large (W/L) and a large overdrive voltage of M_2. As the desired DC voltage level at the output of the sensing circuit is fixed at $0.5V_{DD}$, which in turn fixes the overdrive voltage of M_2. Also, the W/L ratio for M_2 is compromise between the minimum current I_D and a low PSRR. The bias voltage and the W/L ratio of the M_1 are calculated to ensure that M_1 remains in saturation. The overdrive voltage (V_{GS} -V_{TH}) for the level shifter is set to a near minimal (= 0.08 V), $(W/L)_{M1}$ relatively small (=22.2), and $(W/L)_{M2}$ relatively large (=55.6). The level shifter is designed in CMOS 0.18 μm technology under 1.8 V supply. The parameter values of M_1 are, V_{GS} = 0.622 V, and V_{th} = 0.537 V , which result in g_{m1} of 1.002 mS. The parameter values for M_2 are $|V_{GS}|$= = 0.723 V, and $|V_{th}|$= 0.556V to result in g_{m2} of 0.794 mS. The PSRR for the level shifter is obtained as 1.3 (or 2.27 dB), which is small compared to a typical value ranging from 65.0 dB to 80.0 dB for analog IC [19].

The layout of the level shifter is shown in Figure 3.3, and its size is 4.875 × 13.26 μm^2.

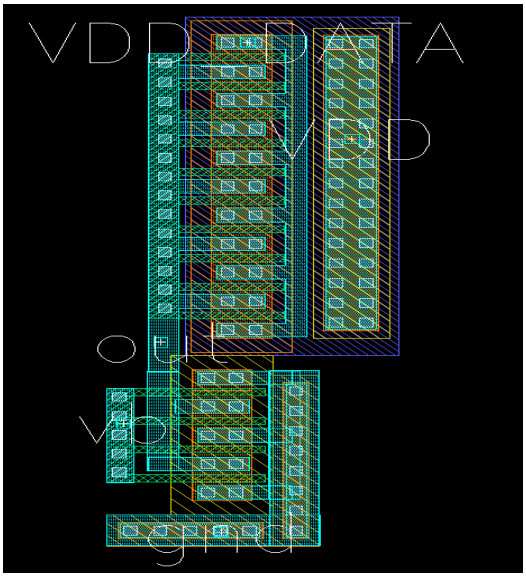


Figure 3.3: Layout of the level shifter

3.3 Signal Extractor

The output of the level shifter is the data signal with a DC value of $0.5V_{DD}$. The following signal extractor amplifiers and extracts the signal, while removing the DC voltage of the signal. The signal extractor shown in Figure 3.4 is a differential amplifier, in which one input has a RC low-pass filter. The low-pass filter extracts the DC value of the signal, which can possibly vary or fluctuate, while removing the signal ideally. The differential amplifier removes the DC value, which is common for both inputs. The differential amplifier also converts a single-ended input into a differential output.

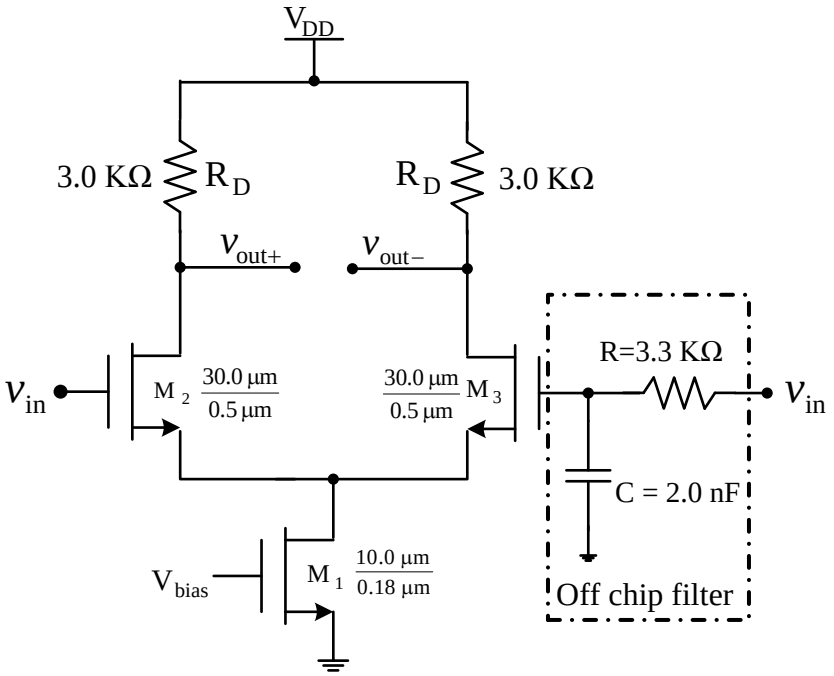


Figure 3.4: Signal extractor

The voltage gain of the differential amplifier is expressed as below.

$$A_v = -g_{m2/3}R_D \tag{3.2}$$

where $g_{m2} = g_{m3}$ and can be expressed as $g_m = \mu_n C_{ox}(W/L)(V_{GS} - V_{th})$. It can be seen from (3.2) that the gain increases by increasing the transconductance, which in turns increases by increasing W/L or by increasing R_D. However, a large device size leads to increased device

parasitic capacitances and a die size, and a higher R_D leads to a higher voltage drop to limit the maximum voltage swings. Thus, a trade-off has to be made between parasitic capacitances and the maximum voltage swing. In our design the size of the transistor is chosen to be reasonably large to avoid an excessively large R_D, which reduces the die size. The gain of the differential amplifier is 10.0 dB, which is large enough to amplify the sensed signal to the required level. Also, a large transistor size and a large resistor are desirable to minimize the DC offset voltage at the input side of the amplifier due to mismatching between devices. The DC offset voltage resulting from mismatching is expressed as [20]:

$$V_{OS,in} = \left(\frac{V_{GS} - V_{th}}{2} \right) \sqrt{\left(\frac{\Delta R_D}{R_D} \right)^2 + \left(\frac{\Delta (W/L)}{(W/L)} \right)^2 + \Delta V_{th}^2} \tag{3.3}$$

(3.3) shows that a large the transistor size and a resistor reduce the DC offset voltage.

The RC filter passes the DC and low frequency terms, while removing the signal ideally. So that only the data signal appears at the differential output. The filter is off-chip for our test chip, but can be implemented on chip in the final design. The resistor R of the filter is set to 3.0 KΩ , and the capacitor 5.0 pF for our experiments. The -3 dB cutoff frequency of the RC filter is 10.6 KHz, which is considerably low.

The layout of the differential amplifier signal extractor is shown in Figure 3.5, and its size is $20.175 \times 26.27\ \mu m^2$. Most of the area is occupied by the transistors M_2 and M_3. The space between the drains and the load resistors is used to route a global metal wire.

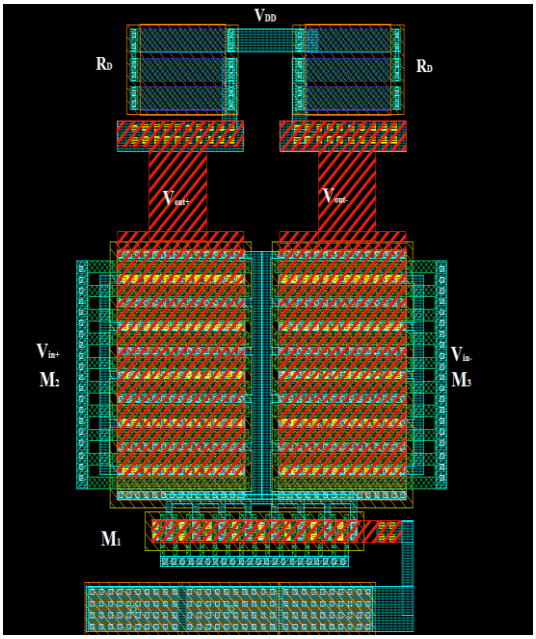


Figure 3.5: Layout of the differential amplifier signal extractor

3.4 Logic Restorer

The logic restorer translates the data in analog differential signal form into logic values. It is based on the Schmitt trigger described in Section 2.5. The logic restorer and its transistor sizes are shown in Figure 3.6. A key aspect of the Schmitt trigger is the hysteresis through the regenerative feedback circuit, which is a cross-coupled inverter pair. The transistor size of the inverter pair, specifically M_7, and M_8, are smaller compared with M_1 and M_2, so that transistors M_1 and M_2 have more influence on the current.

When a new date signal is applied to the logic restorer, the clock is turned to high to turn off M_5 and M_6 (which are voltage controlled current sources). The cross-coupled inverter pair settles to a high or low state and the output of the logic restorer is interpreted as a logic value according. Then, the clock signal becomes low, M_5 and M_6 are turned on. The gap between the high and the low switching voltages of the Schmitt trigger becomes wider due to the additional current supplied by the two transistors. Hence, it requires a larger differential voltage to change the state of the inverter pair, which increases the immunity to noise and disturbances. It should be noted that the sizes of all the transistors were determined through simulations.

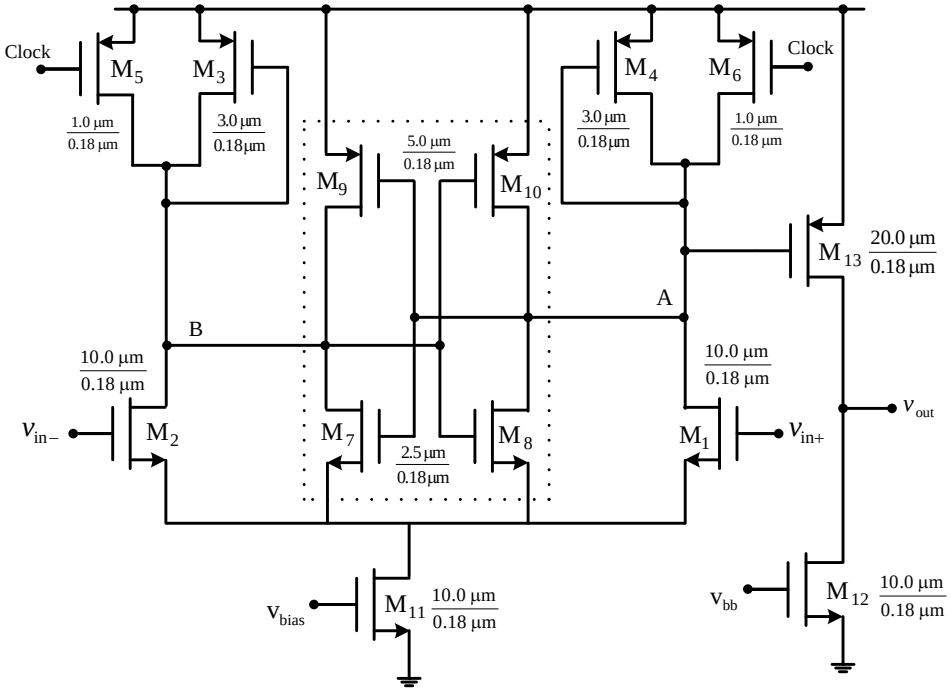


Figure 3.6: A differential Schmitt trigger with the tunable hysteresis

We verified operation of the logic restorer through simulations. We fixed V_{in-} to a certain reference voltage called V_{ref} for our simulations. Let the cross-coupled inverter pair be deactivated. If V_{in+} is equal to V_{ref}, then V_A is equal to V_B. The voltage transfer characteristic for the circuit under V_{ref} = 1.1V is shown in Figure 3.7. Note that the switching voltage is V_{in+} is equal to V_{ref} = V_{in-} = 1.1 V. Suppose that the inverter pair becomes active at the moment. The inverter pair can take a state arbitrarily, and hence the output can be either value 1 or 0. So V_{ref} is indeed the switching voltage. We set V_{ref} to 1.1 V for our all simulations described below.

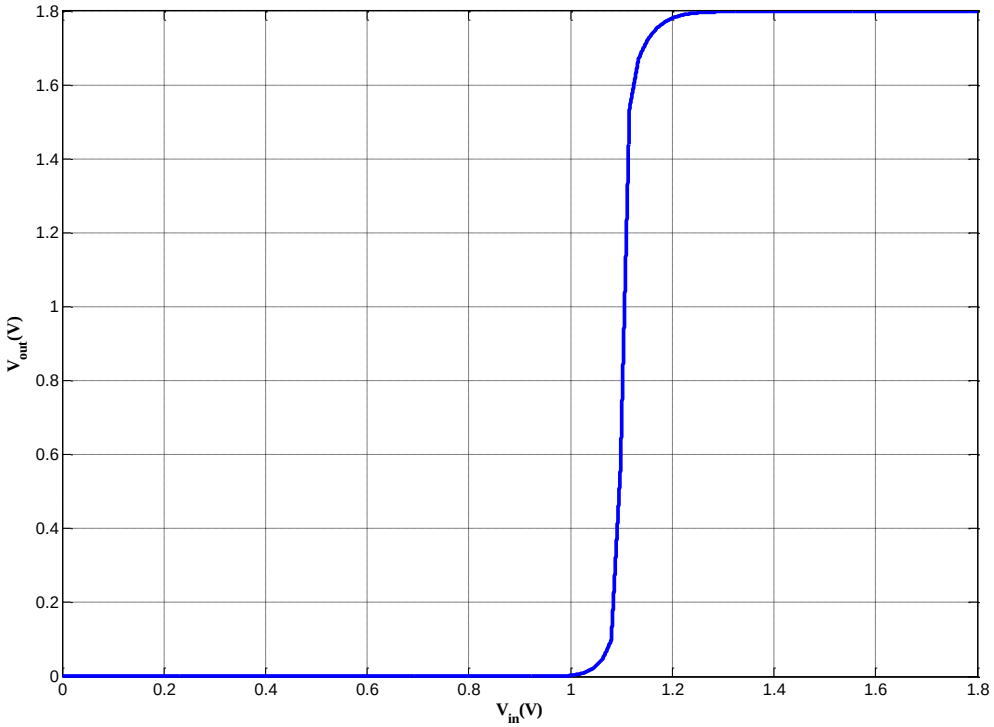


Figure 3.7: DC response for the Schmitt trigger with the inverter pair being inactive

Suppose that V_{in+} is 0 V, while V_{in-} is set to V_{ref} = 1.1 V and the clock to 1.8 V. Then, V_A is at a high voltage and V_B at a low voltage, which turns on M_7 and M_{10} and turns off M_8 and M_9. Figure 3.8 shows the situation, where turned-off transistors are shown in dashed lines. The output voltage V_{out} of the Schmitt trigger is low. As V_{in+} increases from 0 V, M_1 gradually turns on to decreases V_A, and M_2 gradually turns off to increase V_B. When V_{in+} becomes V_{in+}= V_{ref}, the node voltage V_A is still higher than V_B due to M_7 and M_{10}. So the switching does not occur at the point. When V_{in-} exceeds V_{ref}, V_A becomes equal to V_B eventually and a switching occurs. M_7 and M_{10} turn off and M_8 and M_9 turn on. In this case, the switching from high to low occurs. A simulation result in Figure 3.9 shows that the switching occurs at V_{in} = 1.18V. Note that it is higher than V_{ref} = 1.1V.

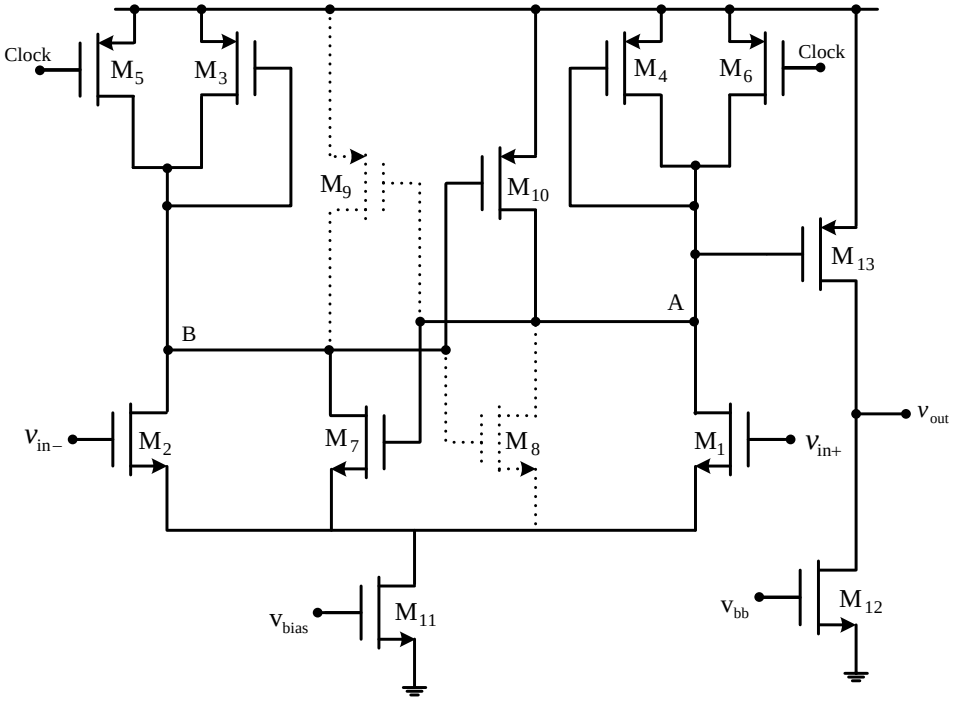


Figure 3.8: A Schmitt trigger with V_{in+} =0 V and V_{in-} = 1.1V

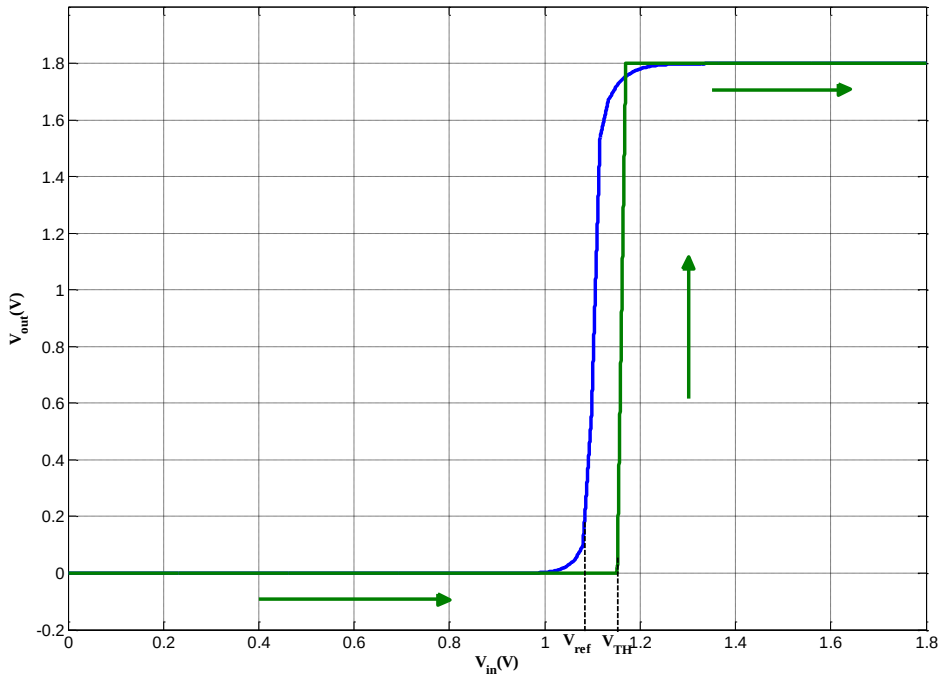


Figure 3.9: V_{in+} changes from 0 V to 1.8 V with V_{in-} = 1.1 V

Next, we simulated the opposite case. V_{in+} decreases from 1.8 V to 0 V, while V_{in-} is set to the same 1.1V and the clock to 1.8 V. Initially, M_8 and M_9 are turned on, and M_7 and M_{10} are turned off. A simulation result in Figure 3.10 shows that the switching occurs at V_{in-} = 0.98V. Note that the switching occurs at 1.18 V for the previous case, and the switching voltage is lower than V_{ref} = 1.1 V.

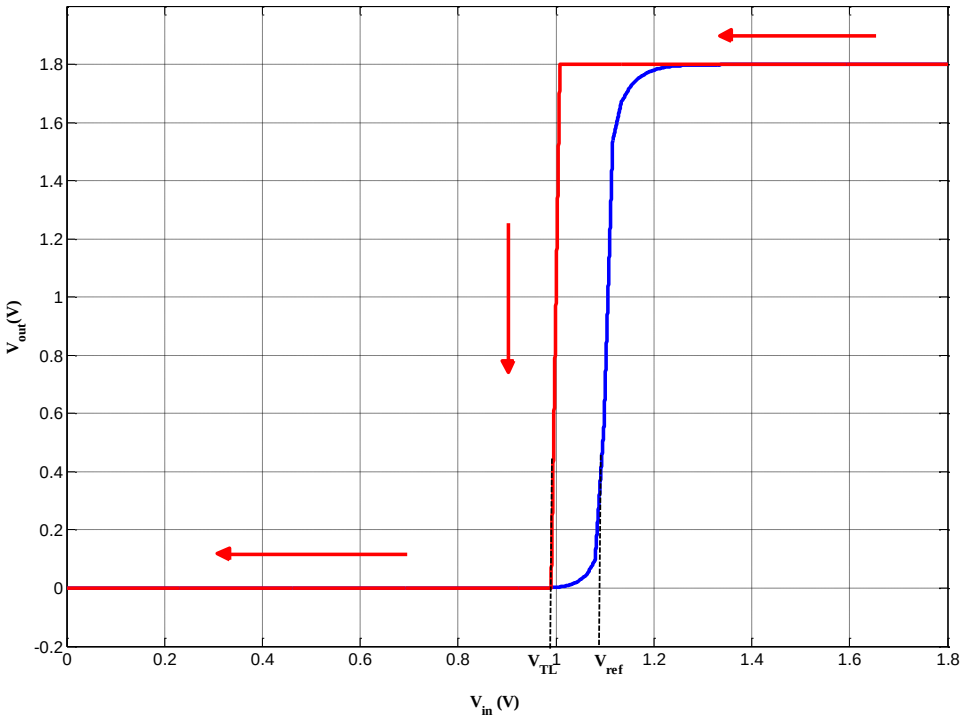


Figure 3.10: V_{in+} changes from 1.8 V to 0 V with V_{in-} = 1.1 V

Figure 3.11 shows a composition of the two simulations shown in Figure 3.7 and Figure 3.8. When V_{in+} changes from low to high, the switching voltage V_{TH} is 1.18. When V_{in} changes from high to low, the switching voltage V_{TL} is 0.98. The difference in the two switching voltages is a hysteresis, which is V_{TH}-V_{TL} = 200 mV.

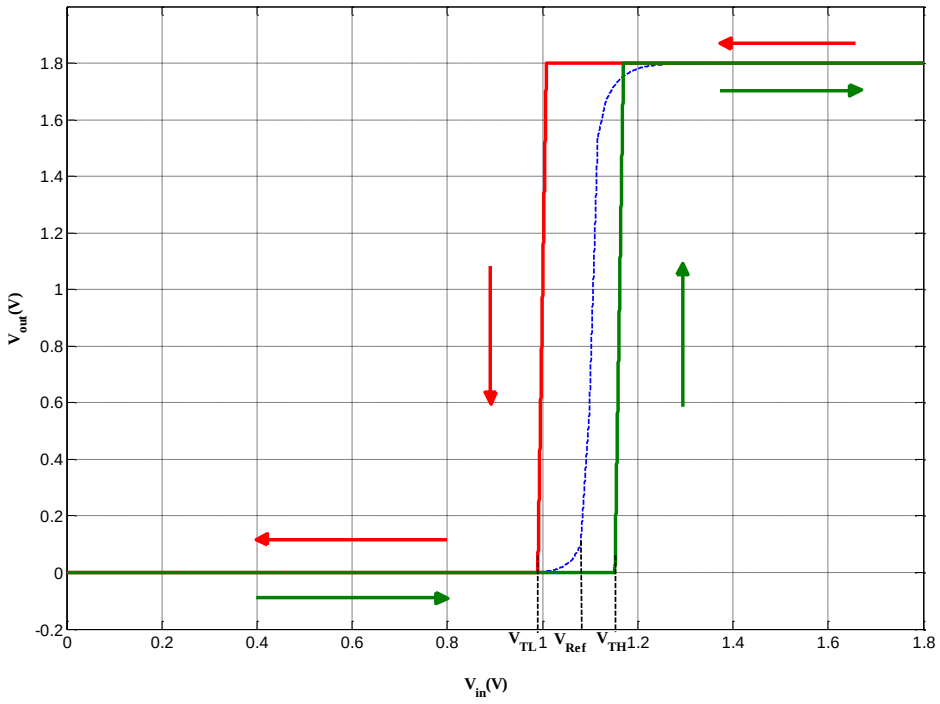


Figure 3.11: Hysteresis obtained from the two simulations in Figure 3.7 and Figure 3.8

We simulated the impact of the two transistors, M_5 and M_6, to the switching voltages. The above simulations in Figure 3.11 are the case under the clock signal of 1.8 V, i.e., when both voltages controlled current sources, M_5 and M_6, are turned off. When the clock signal is 0 V, M_5 and M_6, are turned on to supply more current to M_1 and M_2. Larger current on M_1 and M_2 further skew the switching voltages to widen the gap between V_{TH} and V_{TL}. The simulation results for the case as well as the previous case are summarized in Table 3.1. When the clock signal changes from 1.8 V to 0 V, the $V_{TH} - V_{TL}$ increases from 200.0 mV to 318.0 mV as shown in the table.

Table 3-1: Switching Voltages of the logic restorer

	V_{TL}	V_{TH}	Difference (V_{TH}- V_{TL})
Clock = 0 V	0.88 V	1.198 V	318.0mV
Clock = 1.8 V	0.98 V	1.18 V	200.0 mV

The layout of the signal extractor is shown in Figure 3.12, and its size is 26.22×35.9 μm^2. We noticed that seven large transistors (M_1, M_2, M_{11}, M_{12}, and M_{13}) take most area. Substrate and Nwell contacts are distributed around the layout to ensure their connection to the ground and V_{DD}, respectively.

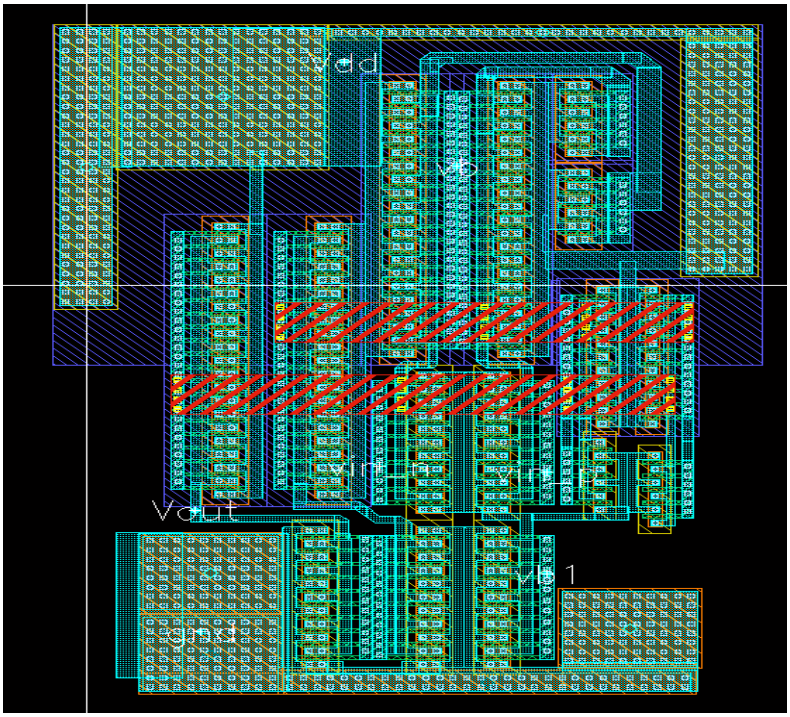


Figure 3.12: The layout of the logic restorer

3.5 Chapter Summary

The chapter describes implementation of three major building blocks, the level shifter, the signal extractor, and the logic restorer, of the proposed PLC receiver in CMOS 0.18 μm process. It explains sizing of key transistors for each block and gives the layouts of the three blocks. It finally gives simulation results of the logic restorer to verify the hysteresis operation of the Schmitt trigger, which is a major function.

Chapter 4

Simulation and Measurement Results

This chapter describes the simulation environment for the proposed PLC receiver and a measurement setup to test chips first. Next, post-layout simulation and measurement results for each sub-block, specifically the level shifter, the signal extractor, and the logic restorer, are presented and then the results for the entire PLC receiver are presented. The chip layouts and die photos of the PLC receiver are given. The performance of the proposed PLC receiver is compared with previous PLC receivers developed by Dr. Ha's group.

4.1 Simulation Environment

The proposed PLC receiver was designed and laid out in CMOS 0.18 μm technology under the supply voltage of 1.8 V and fabricated through Texas Instruments. The signal level for logic 0 is the same as the supply voltage, and that for logic 1 is 90 mV above the supply voltage or 5% of the supply voltage. Note the signal level for logic 1 lies well below the tolerable range of ±10% of the supply voltage. The entire design of the PLC receiver including circuit level simulations, layouts, and post-layout simulations was performed with Cadence design tools.

To measure the performance of individual sub-blocks (such that the level shifter, the signal extractor, and the logic restorer) of the receiver, all the three sub-blocks are designed to be separate. Specifically, all the inputs and outputs of each block are accessible through I/O pins of the receiver.

4.2 Measurement Setup

Chips fabricated through Texas Instruments were mounted on adapter boards for easy access of the pins. Measurements were performed for individual blocks first to verify their correct operations. The performance of each block was measured in terms of maximum data rate and the power consumption. Then the three blocks were connected, and the performance of the entire chip was measured in terms of the maximum data rate, voltage droop, and the power consumption.

Figure 4.1 shows the test setup for a chip under test. A dual-channel function generator (Tektronix AFG 3252) applies the data superimposed on the power line and the clock to the test chip, and a four-channel oscilloscope (Agilent Technologies) observes the waveforms. The blocks were tested at a relatively data rate of 10.0 Mbps, at which the PLC receiver achieves good performance on voltage fluctuations and droops.

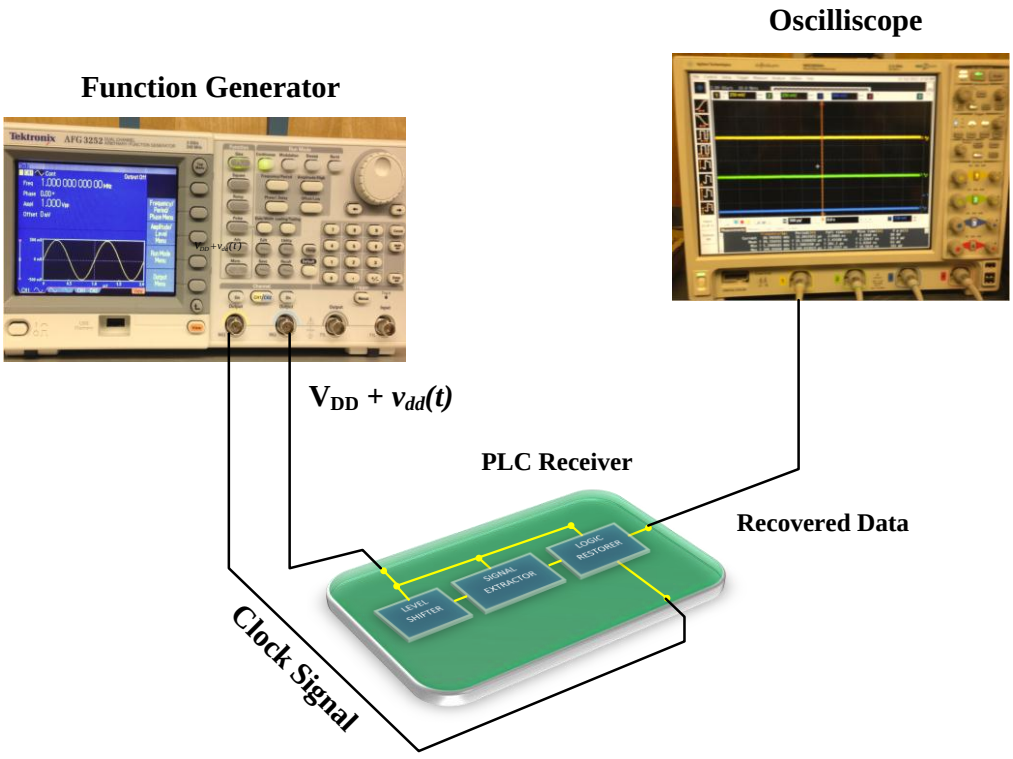


Figure 4.1: Test setup for measurements

4.3 Post-layout Simulation and Measurement Results

4.3.1 Level Shifter

4.3.1.1 Post-layout Simulations

The level shifter is a common source amplifier whose input is fixed to a bias voltage. Figure 4.2 shows the post-layout simulation of the level shifter. The data rate is set to 10.0 Mbps, and the ASK has 1.89 V for logic 1 and 1.8 V for logic 0. The simulation results show that the DC level of the output is shifted down to 0.94 V, approximately a half of the V_{DD}. The simulated power consumption for this sub-block was 157.2 µW.

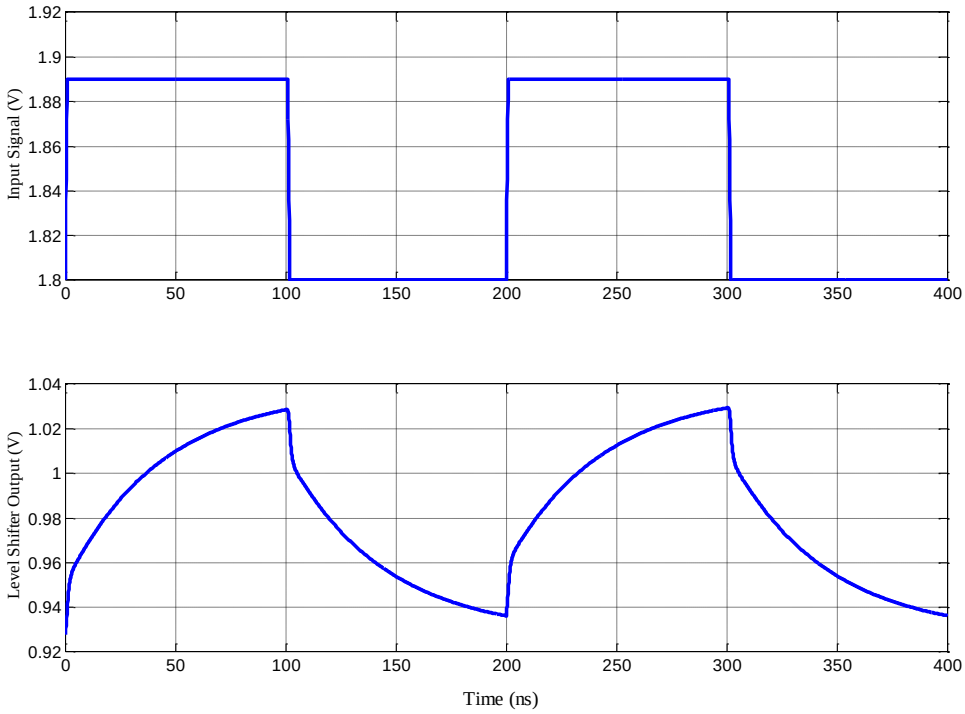


Figure 4.2: Simulation results of Level Shifter when the offset of the input signal is 1.8V

Next, the supply voltage is reduced to 1.5 V, and the ASK modulation has 1.59 V for logic 1 and 1.5 V for logic 0. Figure 4.3 shows the post-layout simulation result. The DC level of the output is shifted down to 0.58 V, more than a half of the supply voltage.

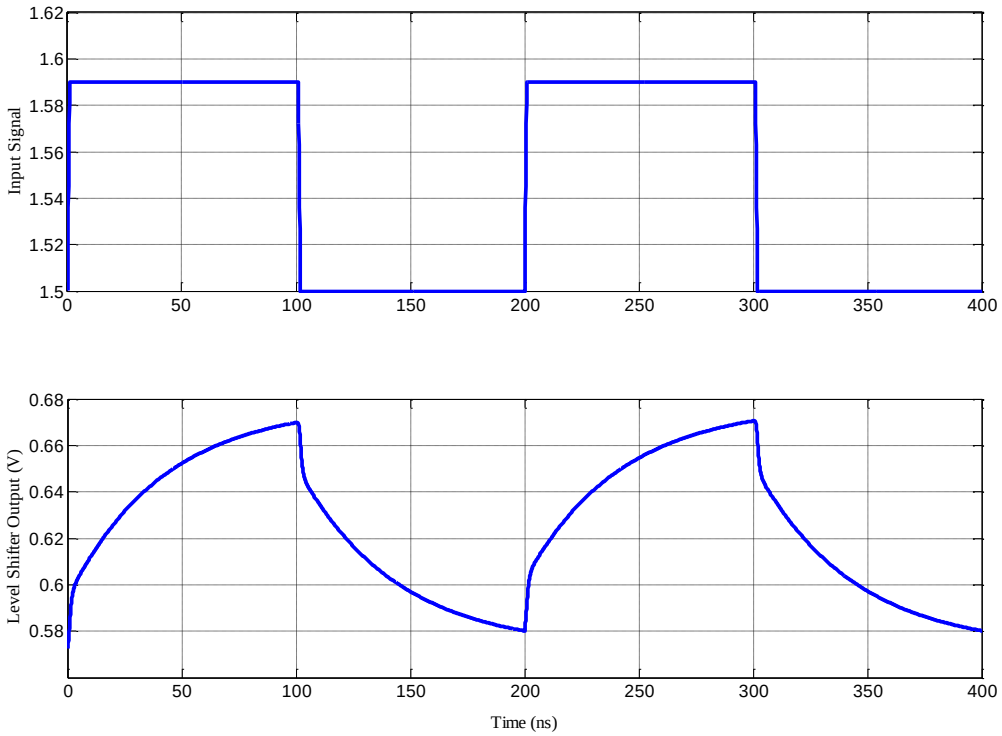


Figure 4.3: Simulation results of Level Shifter when the offset of the input signal is 1.5V

4.3.1.2 Measurements

Figure 4.4 shows the input and measured outputs of the level shifter with the data rate of 10.0 Mbps. The top signal in yellow color is the input signal of the level shifter, in which the level 1.89 V represents logic 1 and 1.8 V logic 0. The bottom signal in green color is the output of the level shifter. The measured DC level of the level shifter is 1.01 V, which is higher than the simulation result by 70 mV. Note that the DC level for the post-layout simulation is 0.94 V. The level shifter draws 220.7 µA under the supply voltage of 1.8 V and dissipates 397.2 µW.

Figure 4.5 shows the measured results for the supply voltage of 1.5 V. The applied input signal has 1.59 V for logic 1 and 1.5 V for logic 0. The simulation results show that the DC level of the output is shifted down to 0.74 V, which is higher than the simulation result by 160 mV. Note that the DC level for the post-layout simulation is 0.58 V

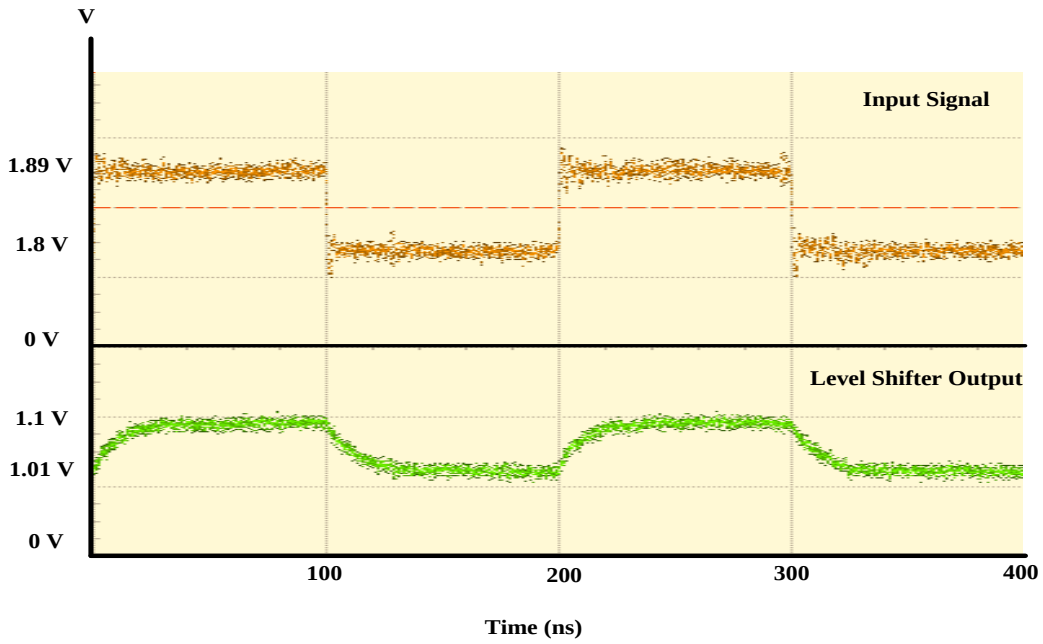


Figure 4.4: Measured results for the level shifter under the supply voltage of 1.8V

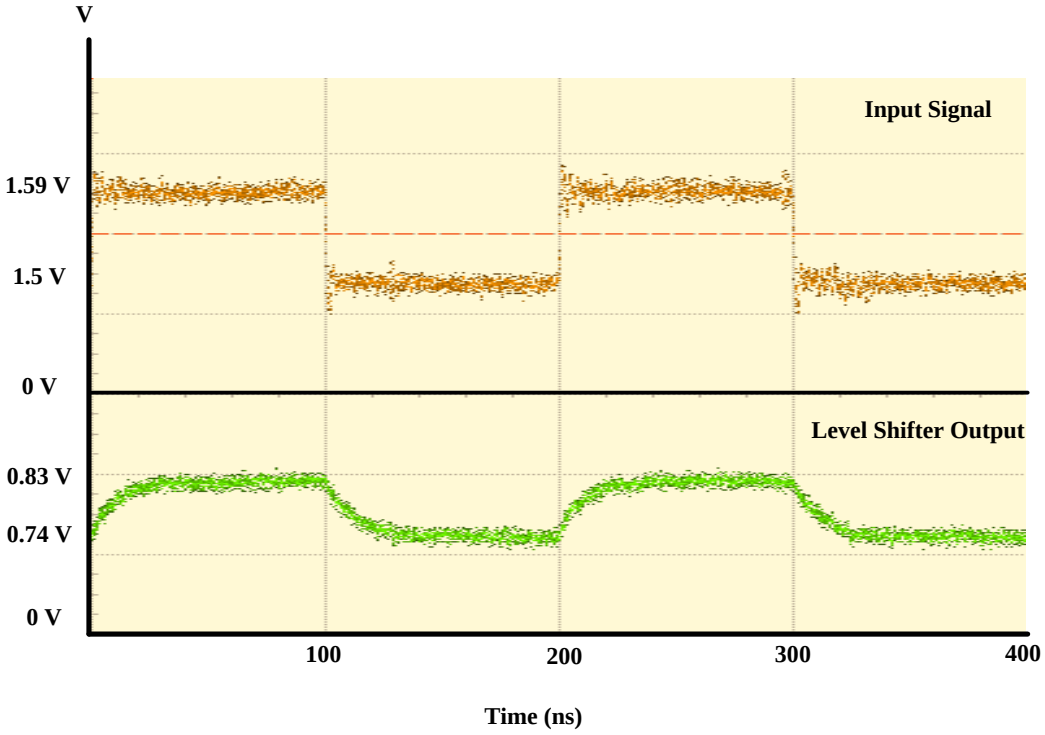


Figure 4.5: Measured results for the level shifter under the supply voltage of 1.5V

4.3.2 Signal Extractor

The signal extractor is a differential amplifier, in which one of the inputs is connected to an RC low-pass filter. The input of the filter and the other input of the differential amplifier are connected together, i.e., one signal is applied to the signal extractor. The two differential outputs are observed for measurements and simulations.

4.3.2.1 Post-layout Simulations

Figure 4.6 shows simulation results for the signal extractor. The topmost signal in blue is the input signal varying between 0.9 V and 0.99 V. The second waveform in red is the output of RC filter, which is almost constant at 0.9 V. The third waveform shows both the positive output V_{out+} in blue and negative out V_{out-} in red. V_{out+} varies between 1.112 V and 1.259V, while V_{out-} varies between 1.254 V and 1.385 V. The bottommost waveform is the differential output, V_{out+} - V_{out-}. The amplitude is 272.2 mV with 0 V offset to result in the voltage gain of the amplifier 3.1 (9.6 dB).

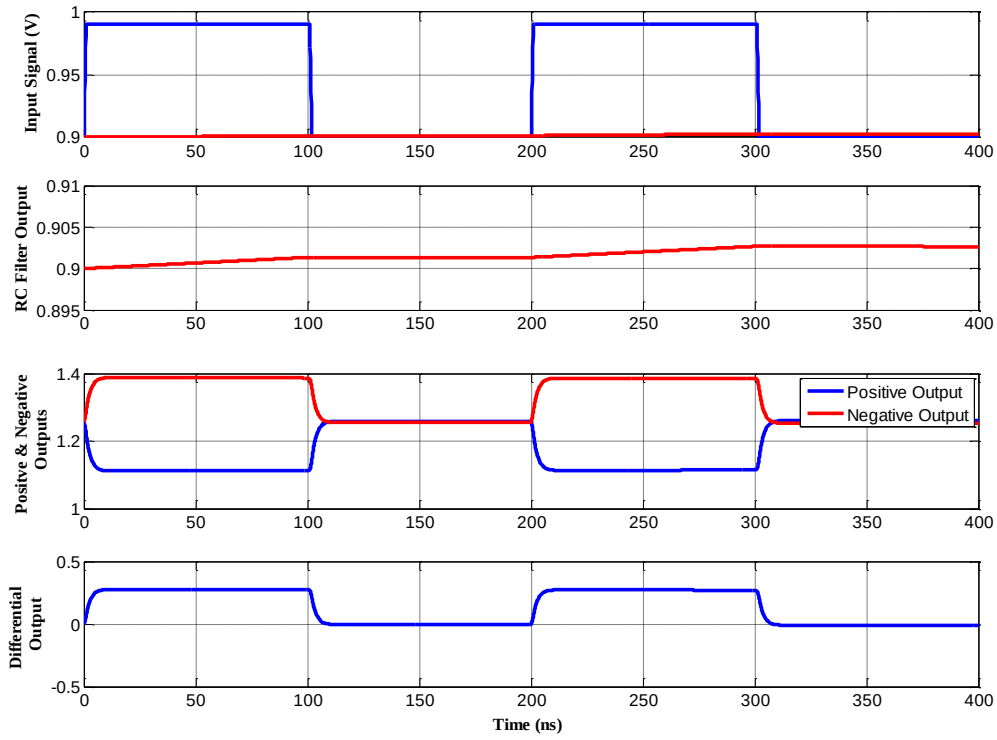


Figure 4.6: Simulation results for the signal extractor

Figure 4.7 shows simulation results for the case when the level shifter and the signal extractor are connected together. Also, in this simulation, 50 mV of white noise is added to to the data signal to examine the performance of the two blocks. The topmost waveform in blue is the applied signal, which varies between 1.8 V and 1.89 V. The second waveform in blue is the output of the level shifter, in which the noise is apparent due to its Y-axis scale. The red ones in the second and third waveforms are the output of the RC filter. The RC filter output is nearly constant at 0.93 V. The forth waveform shows both the positive (V_{out+}) and negative (V_{out-}) differential output voltages. V_{out+} in blue varies between 1.154 V and 1.252V, and V_{out-} in red varies between 1.245 V and 1.352 V. The last waveform is the differential output whose amplitude is 236.2 mV and the DC offset is 0 V.

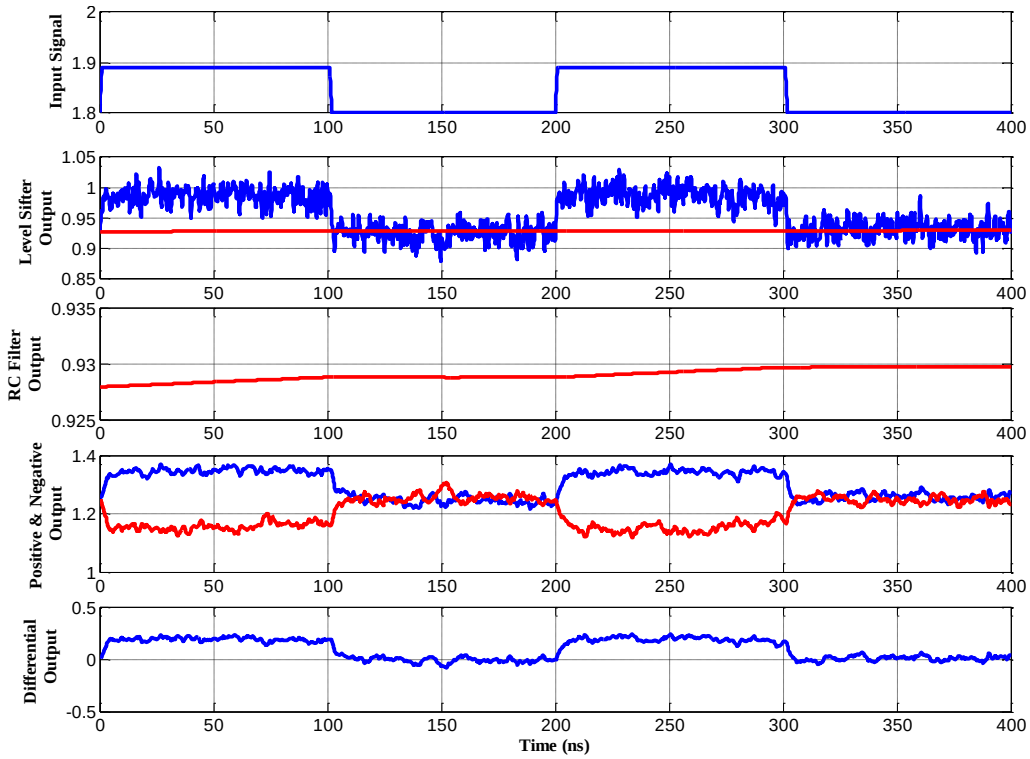


Figure 4.7: Simulation results when the level shifter and the signal extractor are connected together

4.3.2.2 Measurements

Figure 4.8 shows the measured results for the signal extractor. The topmost waveform is the input signal without any noise, which varies between 0.9 V and 1.0 V. The second waveform shows the output of the RC low-pass filter, which changes slowly . The third waveform shows the positive output (V_{out+}), which it varies between 1.1V and 1.25V. The last one is the negative output voltage (V_{out-}) varying between 1.2V and 1.35V. This signal extractor draws 256.0 µA under the supply voltage of 1.8 V and dissipates 460.8 µW.

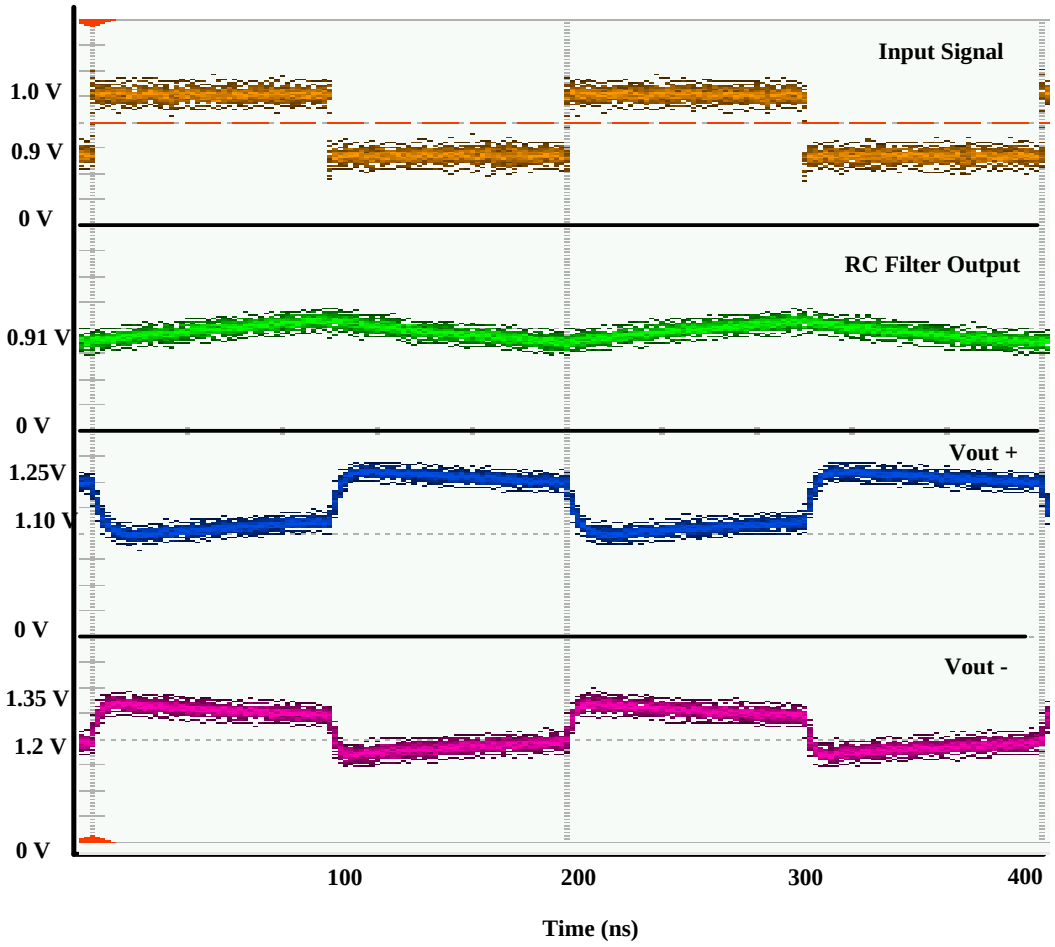


Figure 4.8: The measured results of the signal extractor

4.3.3 Logic Restorer

4.3.3.1 Post-layout Simulations

A ramp signal with 1.8V peak-to-peak is applied to the positive input V_{in+} of the Schmitt

trigger, while the negative input V_{in-} is fixed at 1.0 V and the clock signal fixed at 1.8 V. Figure 4.9 shows the simulation results on of the logic restorer. The output switches at 1.08 V when the input rises and switches at 0.86 V when the input falls, which exhibits the hysteresis.

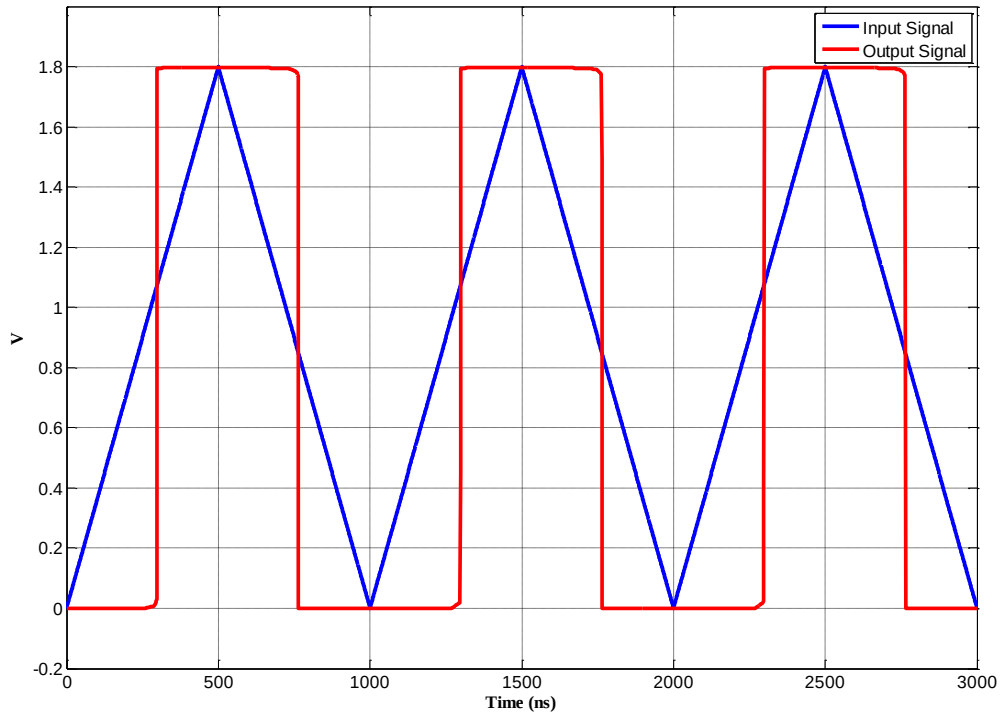


Figure 4.9: Simulation results the logic restorer under the clock signal voltage of 1.8 V

Figure 4.10 shows simulation results of the logic restorer with an rail-to-rail clock signal of 10 MHz. As in the previous case, the negative input V_{in-} is fixed to 1.0 V and a sequence of data 1010 is applied to the positive input V_{in+}. The topmost waveform is the clock signal which varies between 0 V and 1.8 V. The second waveform is the input data signal 1010 with 1.0 V to represent logic 1 and 0.8 V for logic 0. The bottommost waveform shows the output of the logic restorer. When the clock is high, the input data is captured and processed by the logic restorer, and the output data can be obtained at the falling edge of the clock. The power consumption of the logic restorer is 2.1 mW in simulation, which is the largest among the three sub-blocks.

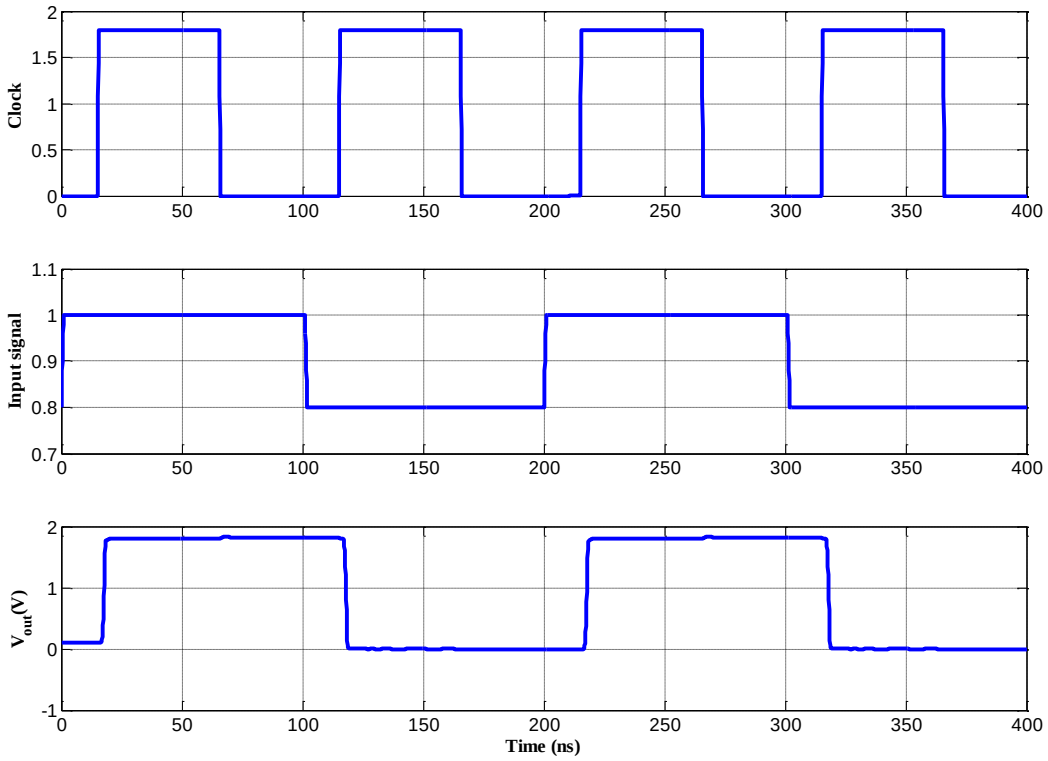


Figure 4.10: Simulation results of the logic restorer with an active clock signal

4.3.3.2 Measurements

The measurement set up for the logic restorer is the same as the above simulation environment. First, a ramp signal is applied to the positive input V_{in+}, while the other input is connected to a fixed voltage of 1.0 V. Figure 4.11 shows the measured waveforms. The measured low threshold voltage V_{TL} is approximately 0.78 V and the high threshold voltage V_{TH} approximately 1.1 V. In comparison with the simulation result, the measured results showed that the hysteresis is wider than the simulated hysteresis with V_{TL} = 1.08 V and V_{TH} = 0.86 V.

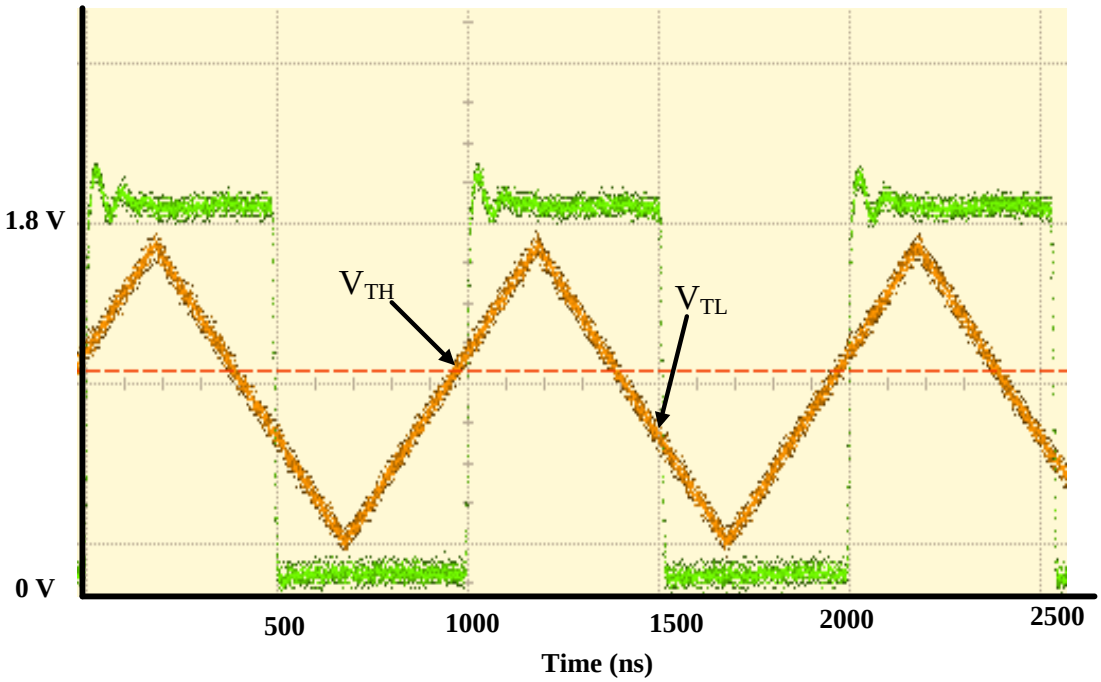


Figure 4.11: The applied input and measured output of the logic restorer

Figure 4.12 shows measurement results active clock. The top waveform is the clock signal with the rail-to-rail at 10.0 MHz. The middle waveform shows the applied input signal to represent 1.15 V for logic 1 and 0.95 V for logic 0. The bottom wave is the output of the logic restorer, which shows a successful recovery of the input data signal. A ripple of 100 mv for logic 1 signal is due to the clock signal. The logic restorer draws 1.34 mA under the supply voltage of 1.8 V and dissipates 2.41 mW.

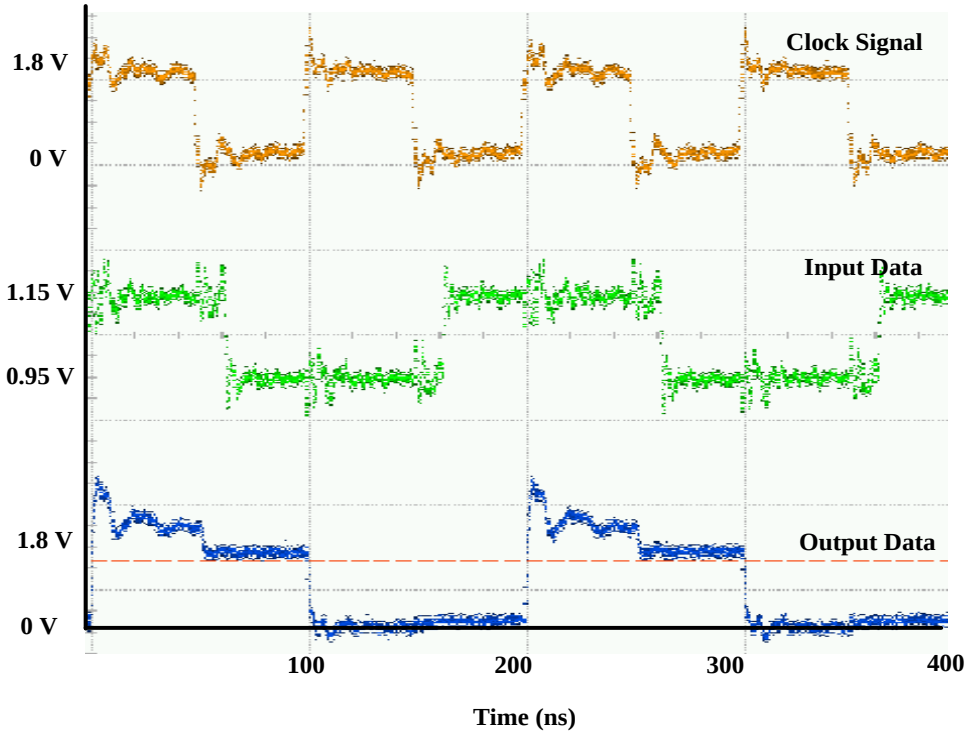


Figure 4.12: The measurement results for the logic restorer with clock signal being connected

4.3.4 PLC Receiver

4.3.4.1 Post-layout Simulations

Now, all the three sub-blocks are connected together, and the entire PLC receiver is simulated for the data rate of 10.0 Mbps. The power line channel is modeled as a cascade of two low-pass filters with the -3dB cutoff frequency of 20.0 MHz. White Gaussian noise voltage of 25.0 mV is added to the data signal to model power line noise [21].

Figure 4.13 shows waveforms of the proposed PLC receiver under 1.8 V supply voltage. The topmost is the clock, and the second waveform is the transmitted data sequence “1010” imposed on the supply voltage. The third noisy waveform in blue is the output of the level shifter (equally input to the signal extractor) and the almost DC waveform in red is the output of the RC low-pass filter. The level shifter lowers the DC level of the data signal to around 0.9 V, and the low-pass filter extracts the DC term of the signal while removing the noise term and the data. The fourth waveform shows the outputs of the signal extractor. The waveform in red at the

positive output varies between 1.05 V and 1.30 V, and the waveform in blue at the negative output varies between 0.8 V and 1.02 V. The last waveform is the PLC output, which shows a successful recovery of the data at the falling edge of the clock. The PLC receiver consumes 2.48 mW of power in simulation.

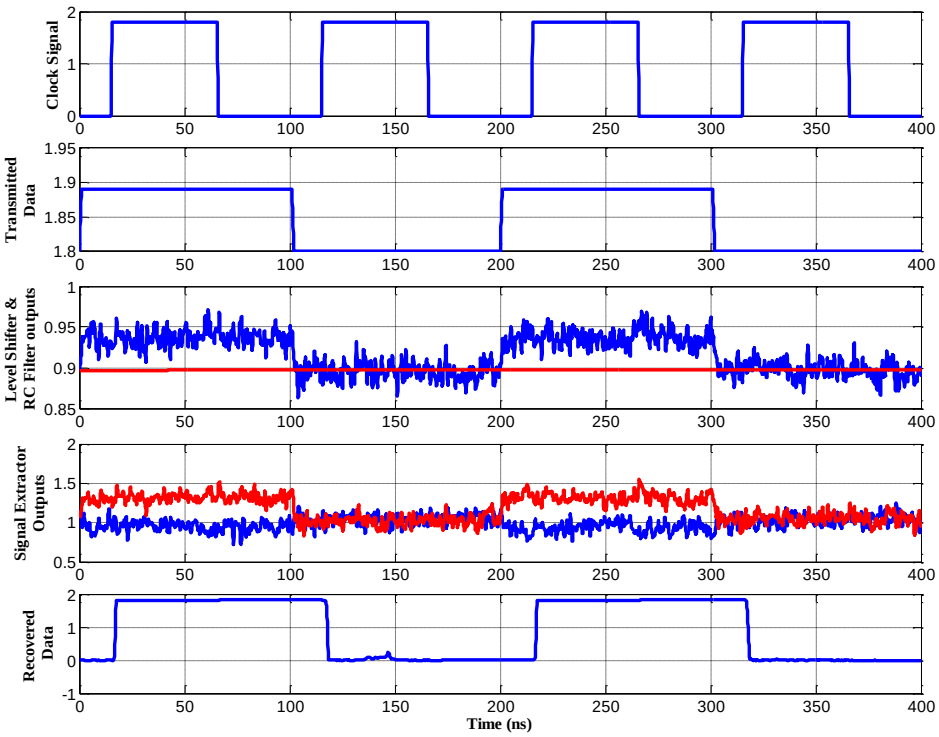


Figure 4.13: Waveforms of the receiver under 1.8 V voltage supply

Next, it was observed that the lowest supply voltage, at which the PLC still could function correctly, was identified as 1.5 V through simulation. The simulation result for 1.5 V supply is shown in Figure 4.14. Note that the rest of the simulation conditions remain the same including the signal level for logic 1, which is 90 mV above the supply voltage. The waveforms under the supply voltage of 1.5 V are essentially the same as that for 1.8 V except the DC level of the level shifter output is reduced to around 0.54 V. It demonstrates that the proposed PLC can tolerate a supply voltage droop by 0.3 V or 17.0%.

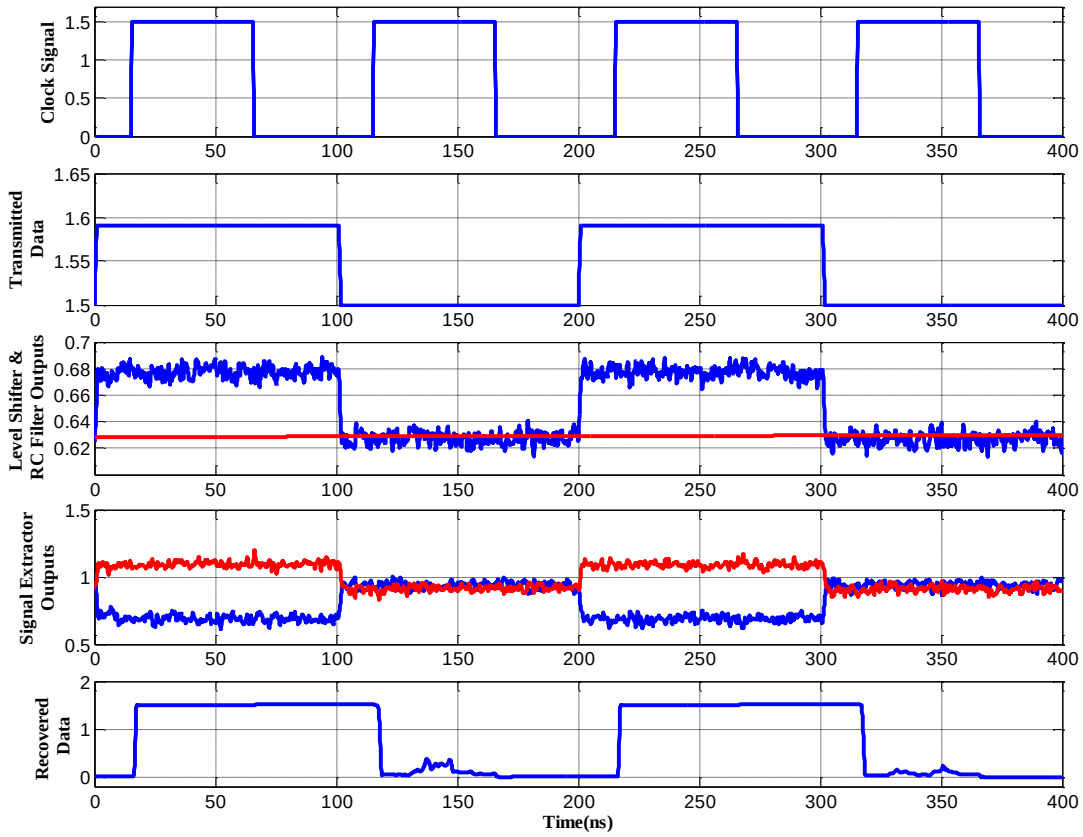


Figure 4.14: Waveforms of the receiver under the supply voltage of 1.5 V

4.3.4.2 Measurements

The operation of the PLC receiver was measured in the same environment as that of the above simulations. Figure 4.15 shows the measurement result of the PLC receiver. The top waveform is the clock signal at 10 MHz. The second waveform is the output of the PLC receiver, which correctly produces a data sequence of "1010" at the falling edges of the clock. The bottom waveform is the input data sequence "1010" superimposed on the supply voltage of 1.8 V. The PLC receiver draws 1.81 mA under the supply voltage of 1.8 V and dissipates 3.2 mW.

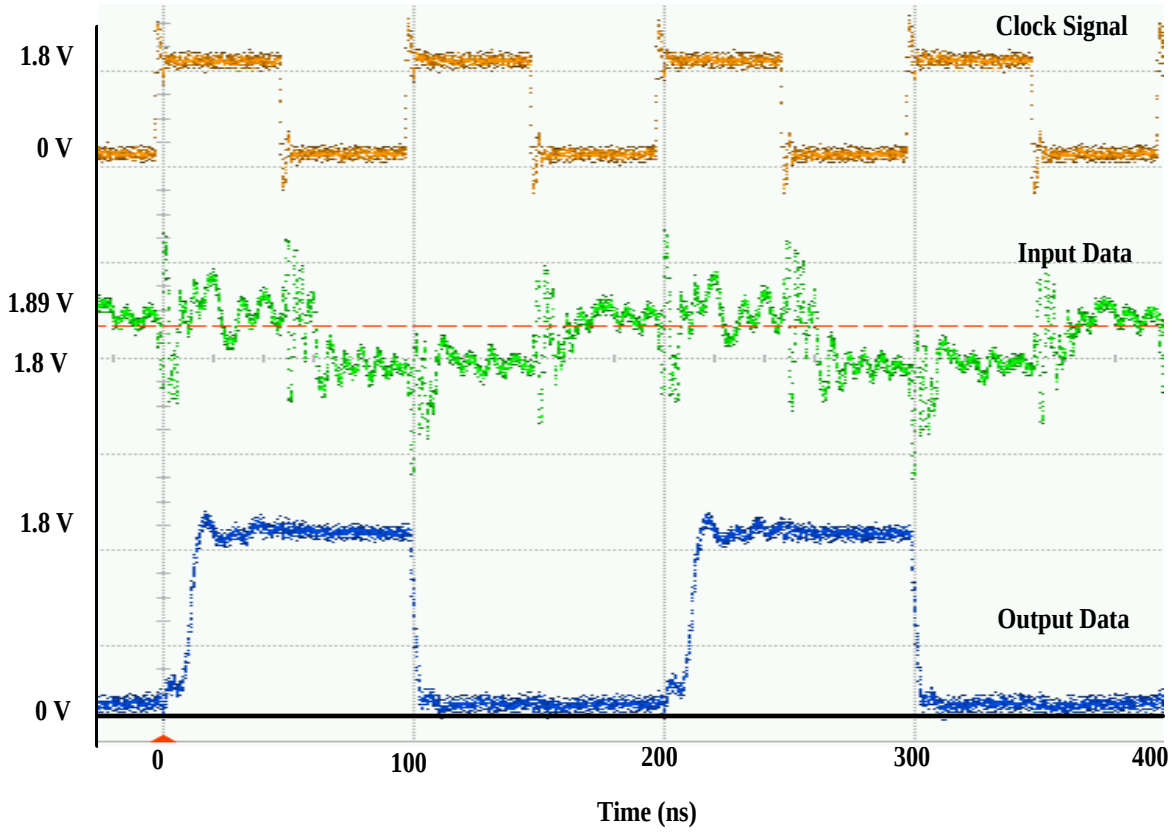


Figure 4.15: Measured waveforms of the receiver under 1.8 V voltage supply

To measure the maximum allowable supply voltage droop, the supply voltage was reduced until the PLC receiver fails to function correctly. The lowest supply voltage, at which the PLC still could function correctly, was observed as 1.377 V. Therefore, the proposed PLC can tolerate a supply voltage droop by 0.423 V or 23.5%, which is slightly larger than the predicted value of 0.3 V through simulation. Figure 4.16 shows the measured results for 1.5 V supply. It demonstrates that the proposed PLC can tolerate a supply voltage droop by 0.423 V or 23.5%. The noise is more dominant for the input data sequence, but the PLC produces the correct output data sequence of "1010".

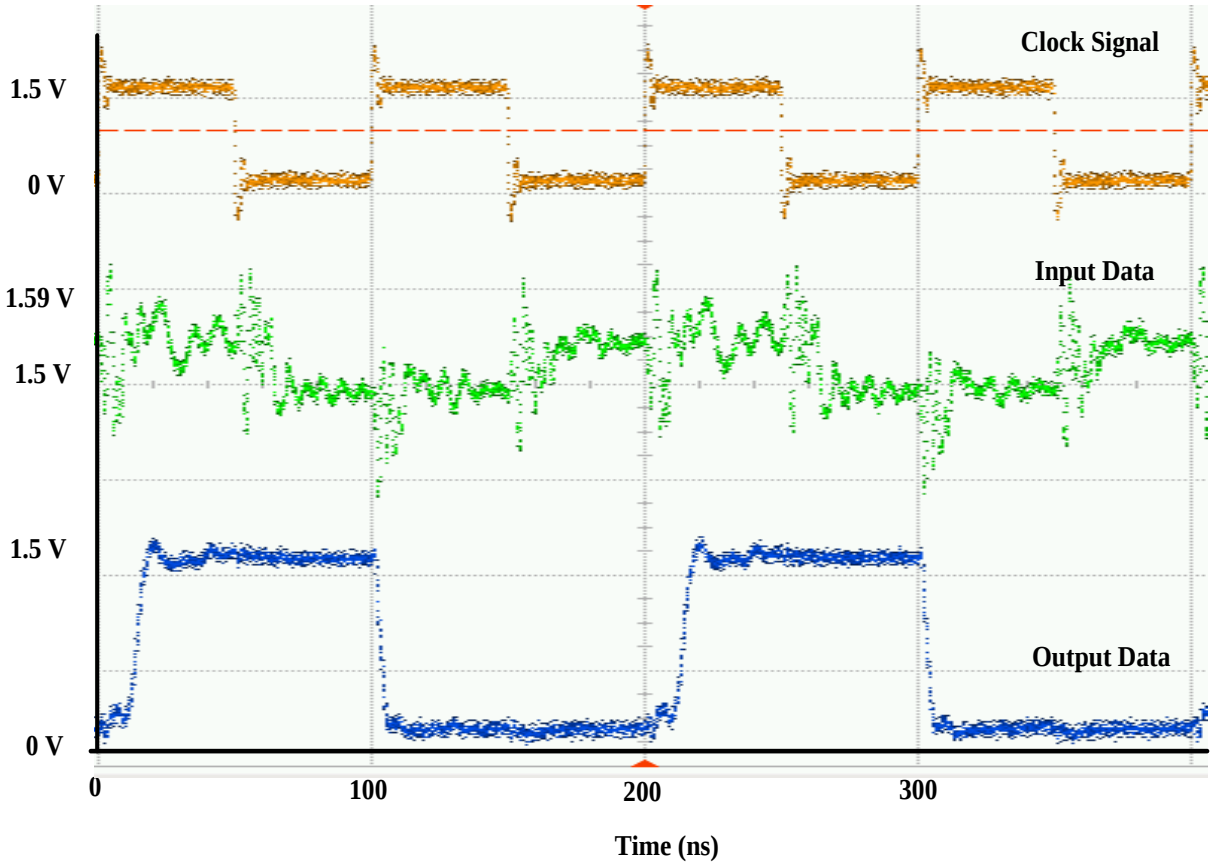


Figure 4.16: The measured waveforms of the receiver under 1.5 V supply voltage

4.4 Layouts and Die Photos

The layout of the entire chip with pin diagrams is shown in Figure 4.17, and the core layout with annotated sub-blocks is shown in Figure 4.18. The die size of the chip is 1.225 mm x 1.223 mm, while the core size is 72.2 µm x 74.9 µm. Figure 4.19 exhibits a die photo of the PLC receiver, and Figure 20 gives a close up die photo of the chip.

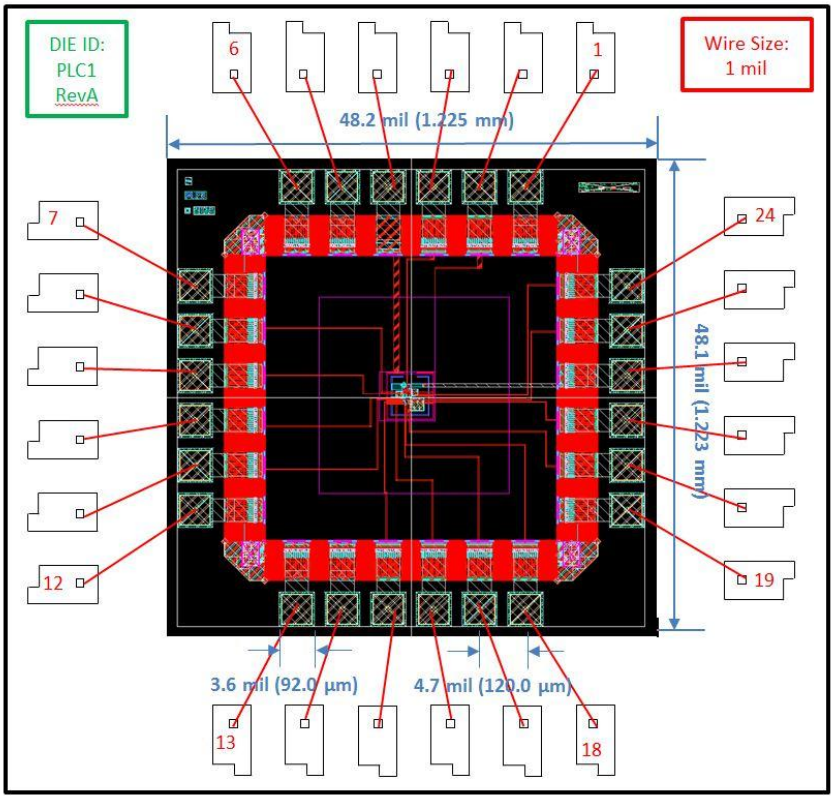


Figure 4.17: Layout with a pin diagram of the PLC receiver

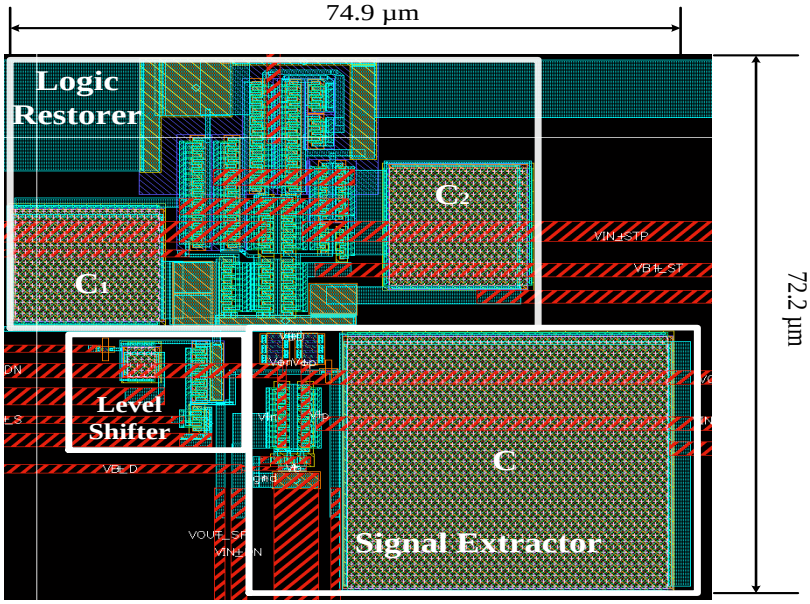


Figure 4.18: Core layout of the PLC receiver

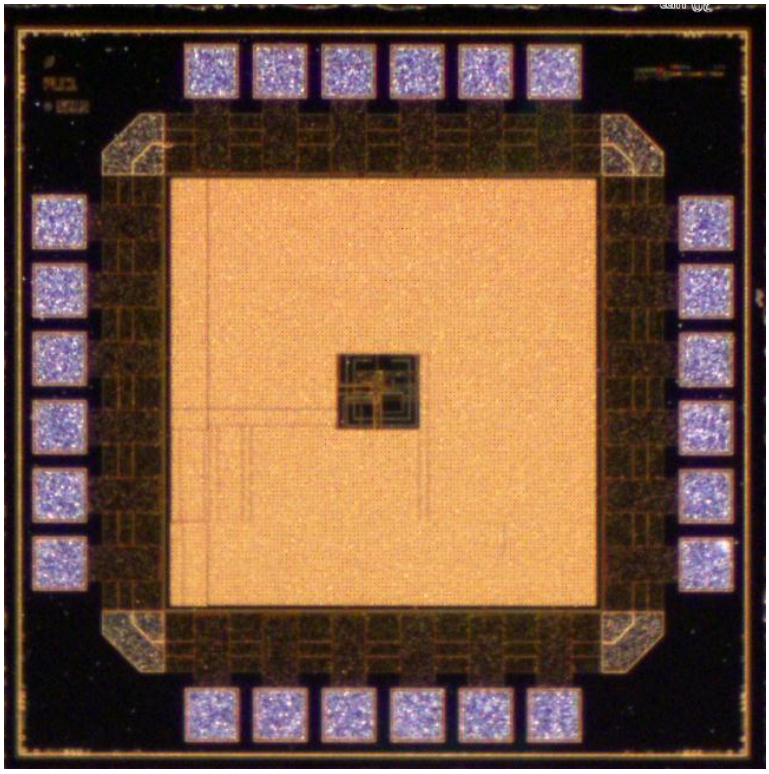


Figure 4.19: Die photo of the PLC receiver

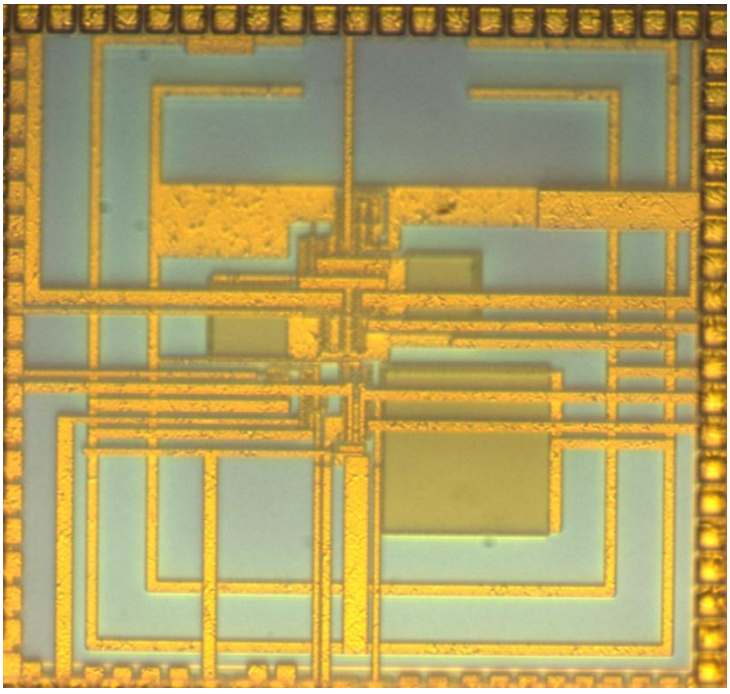


Figure 4.20: Close up die photo of the PLC receiver

4.5 Performance Comparison

Table 4.1 shows a comparison of the proposed receiver with earlier PLC receivers developed by Dr. Ha's group. Although a fair comparison is difficult due to different technologies used and design objectives and constraints, the proposed receiver has the lowest power dissipation among all the PLC receivers. Although not compared directly, we believe that the proposed one can tolerate a far larger voltage droop than previous ones. It should be noted that proposed design has a much lower data rate than its predecessors, and the above advantages of the proposed design may attribute to the low data rate.

Table 4-1: Comparison of Performance with PLC Receivers for ICs

	This work	**[8]**	**[9]**	**[10]**
Technology	0.18 µm	0.18 µm	0.18 µm	0.13 µm
Supply Voltage	1.8 V	1.8 V	1.8 V	1.2 V
Pulse amplitude	90.0 mV	90.0 mV	20.0 mV	10.0 mV
Pulse duration	8 ns	300 ps	200 ps	1.2 ns
Power consumption	2.4 mW	2.8 mW	4.42 mW	3.58 mW
Data Rate	250.0 Mbps	1.0 Gbps	200.0 Mbps	100.0 Mbps

4.6 Chapter Summary

Post-layout simulations and measurements were performed for sub-blocks and the entire PLC receiver for the clock speed of 10 MHz under the supply voltage of 1.8 V. Post-layout and measurements results of sub-blocks and the entire PLC receiver match very well. The measurement results show that the proposed PLC receiver performs well for the data rate of 10 Mbps and can tolerate the supply voltage drop by 0.423 V or 23.5%. The chip dissipates 3.2 mW under the supply voltage of 1.8 V.

Chapter 5

Conclusion

The use of the power distribution networks of ICs for data communications as well as delivery of power was firstly introduced by Dr. Dong S. Ha' group in 2005 [2]. Follow up research works by his group verified existence of pass-bands in power distribution networks and the feasibility of power line communications in ICs. Later, a few PLC receivers in CMOS were developed for PLC in ICs. This thesis research intends to improve previous PLC receivers with three major design objectives, mitigation of the supply voltage fluctuations and droops, improving the noise immunity, and reducing power dissipation.

Design of a robust PLC receiver in a CMOS 0.18 μm technology was investigated in this thesis. The proposed PLC system adopts an ASK modulation scheme, and the PLC receiver consists of three sub-blocks. The first sub-block is a level shifter, which lowers the offset voltage of the supply voltage to approximately $0.5V_{DD}$. The second sub-block is a signal extractor, which detects a data signal superimposed on the power line. The signal extractor is a differential amplifier, in which one input is connected through an RC low-pass filter. The DC voltage of the data signal varies in accordance with the supply voltage fluctuations and droop. The low-pass filter intends to pass only the DC term of the data signal. Since the DC voltage is common for both inputs of the differential amplifier, it is removed from the data signal through the common mode rejection of the differential amplifier. Therefore, the signal extractor can mitigate supply voltage fluctuations and droops. The last sub-block is the logic restorer, which converts the differential signal to a logic value based on a Schmitt trigger. The hysteresis of the Schmitt trigger improves the noise immunity of the receiver.

The proposed PLC receiver was designed and fabricated in CMOS 0.18 μm technology. Measurement results of the three sub-blocks and the entire PLC receiver were presented and

compared with the simulation results. The data rate is set to 10.0 Mbps (the maximum simulated data rate can reach as high as 250.0 Mbps), and the ASK modulation scheme adopts V_{DD} (= 1.8 V) for logic 0 and 90 mV above V_{DD} for logic 1. The measurements show that the PLC receiver can tolerate the supply voltage drop by 0.423 V or 23.0%. The power dissipation for the receiver is 3.2 mW under 1.8 V supply. The core area of the receiver is 72.2 μm x 74.9 μm. Although a fair comparison is difficult due to different technologies used and design objectives and constraints, the proposed receiver has lower power dissipation compared with previous PLC receivers. Although not compared directly, we believe that the proposed one can tolerate a far larger voltage droop than previous ones.

The measurement results show reasonably good performance of the proposed PLC receiver, and a few future research areas to improve the PLC receiver and to make the PLC in ICs feasible are suggested below.

- The most power hungry block of the proposed PLC receiver is the logic restorer or a Schmitt trigger. Design of a power efficient Schmitt trigger is suggested to reduce the overall power dissipation of the receiver.
- The proposed PLC can tolerate supply voltage droop by 0.423 V or 24% under supply voltage of 1.8 V. It would be possible to increase the tolerance level of the voltage droop through careful redesign of sub-blocks.
- Although a high data rate is not the goal of the proposed PLC receiver, the data rate of the PLC can be increased relatively easily through resizing and matching of transistors.
- The current PLC system is intended to control internal nodes, and hence an instrument can be used as a transmitter. To monitor internal nodes, a PLC transmitter should be designed, and the feasibility of PLC from an internal node to an external pin should be investigated.

The above items are left for future research in PLC receiver design as well as system level investigations of PLC systems in ICs.

Bibliography

[1] R. J. Riedlinger et al., “A 32nm 3.1 billion transistor 12-wide-issue Itanium; processor for mission-critical servers,” in ISSCC ’11, Feb. 2011,pp. 84 –86.

[2] W. C. Chung, D. S. Ha, and H. J. Lee, “Dual use of power lines for data communications in a system-on-chip environment,” Proceedings of IEEE International Symposium on Circuits and Systems, Vol. 4, pp. 3355-3358, May 2005.

[3] W. C. Chung, and D. S. Ha, “A new approach for massive parallel scan design,” Proceedings of IEEE International Test Conference, pp. 497-506, November 2005.

[4] R. Thirugnanam, D.S. Ha, and T. M. Mak, “On Channel Modeling for Impulse-Based Communications over a Microprocessor's Power Distribution Network,” International Symposium on Power Line Communications, pp. 355-359, March 2007.

[5] V. Chawla and D. S. Ha, "On feasibility study for power line communications in microprocessors", TBD journal, manuscript submitted on xxxx date.

[6] R. Thirugnanam, “The dual use of power distribution networks for data communications in high speed integrated circuits,” Ph.D. dissertation, Department of Electrical and Computer Engineering, Virginia Tech, 2006.

[7] V. Chawla, “power line communications in microprocessors - system level study and circuit design,” M.S. thesis, Department of Electrical and Computer Engineering, Virginia Tech, 2009.

[8] R. Thirugnanam, D.S. Ha, and T. M. Mak, "Data Recovery Block Design for Impulse Modulated Power Line Communications in a Microprocessor," IEEE Computer Society Annual Symposium on VLSI, pp. 153 - 158, May 2007.

[9] V. Chawla, R. Thirugnanam, D.S. Ha, and T.M. Mak, "Design of a Data Recovery Block for Communications over Power Distribution Networks of Microprocessors,” International Conference on Circuits & Systems for Communications, 5 pages, May 2008.

[10] V. Chawla and D.S. Ha, "Dual Use of Power Lines for Data Communications in

Microprocessors" IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems, pp. 23-28, April 2011.

[11] H. Su, F. Liu, A. Devgan, E. Acar, and S. R. Nassif, ‘‘Full Chip Leakage Estimation Considering Power Supply and Temperature Variations,’’ Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED), 2003, pp. 78–83.

[12] N. Weste and D. Harris, CMOS VLSI design: A circuit and systems perspective. 4th ed. Addison-Wesley, 2011.

[13] H. H. Nguyen and E. Shwedyk, A First Course in Digital Communications. Cambridge University Press, 2009.

[14] S. Lee and S. Lee. “An implantable wireless bidirectional communication microstimulator for neuromuscular stimulation”. IEEE Trans. on Circuits and Systems I.,52(12):2526–2538, December 2005.

[15] G. Gudnason. “A lowpower ASK demodulator for inductively coupled implantable electronics”. In Proc. European Solid State Circuits Conf., pages 385–388, September 2000.

[16] J. Alegre, S. Celma, B. Calvo, and J. Pozo. “Design of a novel envelope detector for fastsettling circuits ”. IEEE Trans. on Instrumentation and Measurement, 57(1):4–9, January 2008.

[17] F. Yuan, "Differential CMOS Schmitt Trigger with Tunable Hysteresis," Analog Integrated Circuits and Signal Processing (Springer). Vol.62, No.2, pp.245 - 248, Feb. 2010.

[18] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed. New York, NY: Wiley, 2001.

[19] Phillip E Allen, Douglas R Holberg. CMOS Analog Circuit Design, 2nd Edition. Oxford:Oxford University Press, 2002.

[20] B. Razavi, Design of Analog CMOS Integrated Circuits. New York: McGraw-Hill, 2001.

[21] E. Alon, V. Stojanovic´, and M. A. Horowitz, “Circuits and techniques for high-

resolution measurement of on-chip power supply noise," IEEE J. Solid-State Circuits, vol. 40, no. 4, pp. 820–828, Apr. 2005.