Implementation of a 100kW Soft-Switched DC Bus Regulator Based on Power Electronics Building Block Concept

Jia Wu

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

In

Electrical and Computer Engineering

Dr. Fred C. Lee, Chair

Dr. Dusan Borojevic

Dr. Jason Lai

Keywords: Power Electronics Building Blocks (PEBB), Power Factor Correction (PFC), Rectifier, Space Vector Modulation (SVM), Zero Current Transition (ZCT) Soft Switching, DC Bus Regulator

May 3, 2000
Blacksburg, Virginia

Implementation of a 100 kW Soft-Switched DC Bus Regulator Based on Power Electronics Building Block Concept

By

Jia Wu

ABSTRACT

Power electronics building blocks (PEBBs) are standardized building blocks used to integrate power electronics systems. The PEBB approach can achieve low cost, high redundancy, high reliability, high flexibility and easy maintenance for large-scale power electronics systems. This thesis presents the implementation of a 100kW PEBB-based soft-switched bus regulator for an 800V DC distributed power system. The zero current transition (ZCT) soft-switching technique is used to improve the performance of the bus regulator by minimizing switching loss and improving overall efficiency.

PEBB modules and a digital control building block are the subsystems of the DC bus regulator. This thesis addresses the design issues at subsystem and system levels. These include: operational principles and design of ZCT PEBB modules; design and implementation of the digital control block, based on DSP and EPLD; and modeling and control design of the DC bus regulator.

There are several considerations when using the ZCT soft-switching technique in three-phase applications: the timing of the auxiliary switch gate signals must be arranged differently; there are low-frequency harmonics caused by the pulse width limits; and there is high thermal stress on the resonant capacitors. These issues are resolved by

utilizing the sensed phase current information and the design freedom in the PWM modulator. A PWM modulation technique is proposed that can considerably reduce the switching events and further remove the associated loss while keeping THD low. Reduced switching events alleviate the thermal issue of the resonant capacitors. The same modulation technique can avoid the low-frequency harmonics caused by the pulse width limits and double the sampling frequency. The phase current information is used to deal with the control timing issue of the auxiliary switches and to control the three-phase soft-switching operation in order to achieve better efficiency. Additionally, the phase current information is used to implement dead time compensation to reduce THD.

The soft-switched DC bus regulator has been tested up to a 100kW power level with 20kHz switching frequency. Experimental results demonstrate that high performance of the DC bus regulator is accomplished in terms of high efficiency, wide control bandwidth, low THD, unity power factor and high power density.

Acknowledgments

I would like to express my gratitude to my advisor, Dr. Fred C. Lee, for his support and guidance during my graduate studies at Virginia Tech. His broad vision, profound knowledge, and creative thinking have been the source of inspiration through the course of this research.

I am grateful to my professors, Dr. Dusan Borojevic, Dr. Jason Lai, Dr. Dan Chen and Dr. Alex Huang for their valuable guidance and advice in my research and graduate studies.

I would also like to thank all of the members in the CPES (previously VPEC) with whom I shared the last three years. I cherish the experience to work with these students and visiting scholars. Among them are Mr. Dengming Peng, Dr. Kun Xing, Dr. Richard Zhang, Dr. Kunrong Wang, Dr. Xiaogang Feng, Mr. Kelvin Motto, Mr. Jae-Young Choi, Mr. Zhihong Ye, Ms. Ivana Milosavljevic, Mr. Nikola Celanovic, Mr. Ivan Celanovic, Mr. Jianwen Shao, Mr. Liming Ye, Mr. Heping Dai, Mr. Yuqing Tang, Mr. Fengfeng Tao, Mr. Qun Zhao, Mr. Huibin Zhu, Mr. Yuxin Li, Mr. Dongyu Wang, Mr. Rengang Chen, Mr. Jia Wei, and Dr. Xiaorong Xia. Also I wish to thank Ms. Teresa Shaw, Mr. Jeffery Batson, Ms. Teresa Rose and many other people for their countless help. I wish to thank all the PEBB and MURI team members for the valuable discussions. Thank you for all your friendship and help.

Finally, I would like to thank my family, for their love and support. Especially, I would like to thank my wife, Wenhua, for her love, care and encouragement.

Table of Contents

List of Illustrations

Chapter 1 Introduction

1.1 Power Electronics Building Blocks and DC Distributed Power System

Power electronics building blocks (PEBBs), a concept proposed by the Office of Naval Research (ONR) [1], essentially involves the integration of large-scale power electronics systems using standardized building blocks. PEBBs are not limited to being solely the building blocks of the converter power stage, which here and hereafter are called PEBB modules. A PEBB can be a standard control building block or even a standard converter. How to partition power electronics systems into hierarchical systems that consist of several kinds of PEBBs is still an interesting research topic and will be discussed later in this section.

The major advantage of the PEBB approach is the reduced cost of power electronics products, especially for the high volume products and those with low volume but high power level. The PEBB approach is particularly suitable for the development of large-scale power electronics systems, such as DC distributed power systems and utility power conditioning systems. Since all the converters in a large-scale power electronics system can be constructed based on one or several standard PEBBs, the development cycle of each converter will be significantly reduced. The costs and developing time for the whole system can be driven down considerably.

Other major benefits of the PEBB approach include but are not limited to increased redundancy, reliability, flexibility and easy maintenance. One distinct feature of the PEBBs is that they have a certain level of intelligence and communication capability. This feature enables the fault diagnosis and system reconfiguration for a power electronics system, which is extremely important to both the military and crucial industry applications. Actually, one objective of developing PEBBs is to investigate a PEBB-based DC distributed power system for the next generation of naval ships. Besides, if the PEBB approach is adopted by the power electronics industry, the competitiveness of products will be strengthened, similar to what happened in the computer industry.

To implement the PEBB concept, the first major step is to exploit the commonality of power electronics systems. For the power stage, large-scale power electronics systems can be partitioned into individual PEBB modules by identifying one or more basic topologies among available practical converter topologies. Meanwhile, controllers of various power electronics systems can be standardized based on their applications. In other words, controller building blocks are not related to specific hardware configurations; they are application-oriented. All the building blocks have standard interfaces such that they can be easily interconnected to construct large systems. In literature [2], PEBB modules are defined based on the power level of a converter. For a power level between 50kW and one megawatt, a half-bridge power module is identified as the basic element of a PEBB module. A PEBB module is basically an assembly of power semiconductor devices and associated circuitry such as gate drive, sensors and standard communication interface.

As previously mentioned, the PEBB approach is suitable for system integration. It provides low cost, high reliability and feasible control architecture to large-scale power electronics systems. To explore the issues of PEBBs in power electronics systems as well as the system issues in DC distributed power systems, a 100kW testbed has been built to. The frame of the system structure of this testbed is shown in Figure 1.1. In this testbed, an 800V DC distributed bus is used to connect the power source and various DC loads. A 100kW three-phase PEBB-based power factor corrected (PFC) pulse width modulated (PWM) boost rectifier is used as the DC bus regulator due to its notable features: sinusoidal input current, adjustable input displacement factor and high efficiency [3,4]. The parallel issues of the PFC PWM rectifiers are investigated in a different system [2]. The main load is a four-leg utility inverter that feeds various AC loads. A DC bus conditioner is used to stabilize the DC distributed power system by decoupling the low- and medium-frequency interactions between loads and sources when the utility inverter or other load is under unbalanced and/or nonlinear load conditions.

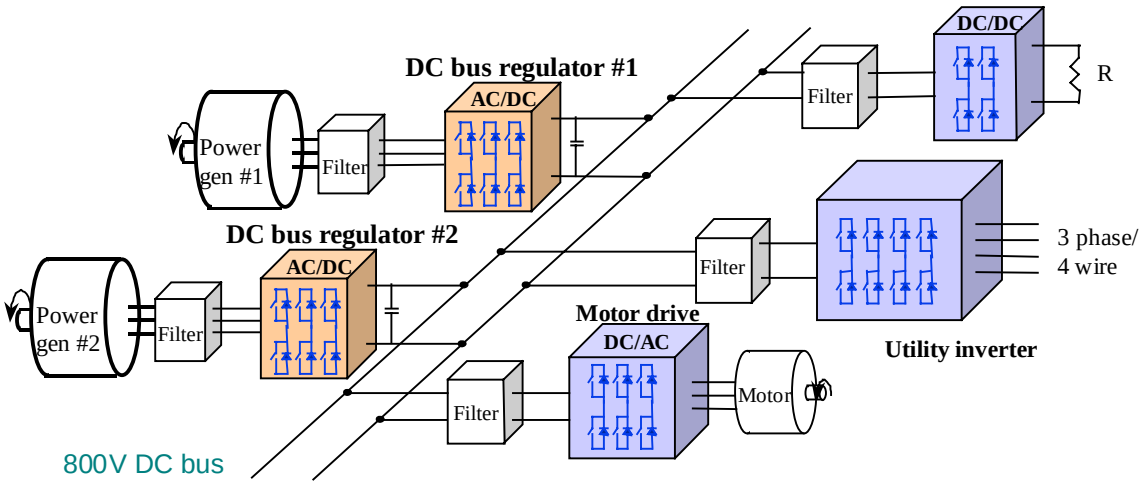


Figure 1.1 Overview of the 100 kW DC distributed power system testbed

High switching frequency is a factor crucial for the PEBB-based DC bus regulator to achieve high performance for the distributed power system and to reduce the size of passive components. As in commercially available power modules, semiconductor devices used as the switching elements of PEBB modules determine the switching performance. Despite the continuous improvements in the design and manufacturing of power semiconductor devices, hard-switching PWM converters with high power level still suffer from high switching loss and severe EMI due to high dv/dt and di/dt. An effective approach dealing with these issues is using soft-switching techniques, which can shape the rising and falling edges of switch current and voltage waveforms of the conventional PWM. Meanwhile, switches and diodes can be turned on under zero voltage and/or turned off under zero current, which means minimal switching loss. Zero voltage transition (ZVT) and zero current transition (ZCT) are two classes of the most practical soft-switching techniques available for PWM converters. In the past several years, various ZVT and ZCT techniques have been proposed [5-10].

Better performance is expected from a PEBB module that incorporates a soft-switching network. An important requirement is decoupling of any possible interference among PEBB modules. The interference is mostly caused by the switching actions that occur due to the non-ideal switching characteristics of the semiconductor devices. Although soft-switching techniques are good for devices, some may not be good for PEBB applications. Several practical soft-switching techniques have been investigated [11]. The ZCT soft-switching technique is shown to be better for PEBB applications because it is less sensitive to system layout. Thus, this kind of PEBB module is better for system integration.

1.2 Thesis Outline

The 100 kW DC bus regulator basically consists of three ZCT PEBB modules and a digital control block, which are called subsystems. Chapter 2 discusses these subsystem design issues. Circuit topology of the ZCT PEBB module is described as well as its physical structure. Operational principle of the adopted ZCT soft-switching technique is analyzed in detail to show its ability to significantly reduce diode reverse recovery and IGBT switching loss in PEBB modules. Designing the resonant tank in order to achieve effective soft switching is also discussed. The IGBT gate drive is a key issue in PEBB module design. Appropriate tradeoffs need to be made to achieve favorable switching performance of the PEBB modules. A circuit schematic of the IGBT gate drive boards and on-board protection mechanisms are presented. Switching frequency of the PEBB module is determined by several factors at PEBB module level. Due to the considerable gate capacitance of the high-power IGBT switches, the switching frequency can be limited by the gate drive power. It is found that the power consumption of the gate drive is proportional to the switching frequency. An issue associated with high switching frequency is the thermal stress on the soft-switching circuitry. Because of the poor thermal management ability of the passive components, passive components especially the resonant capacitors (more vulnerable to thermal stress than the resonant inductors) are subject to high thermal stress. Testing also finds the thermal ability of the heatsink for the IGBT switches to be inadequate. Solutions are proposed.

The digital control block serves as a command subsystem. It is composed of a digital signal processor (DSP) and erasable programmable logic device (EPLD) based digital controller, an A/D D/A board and an optic fiber interface board. The DSP

performs control algorithms and the EPLD implements the peripheral digital circuit of the DSP. The DSP code is illustrated by a flow chart, while the EPLD design is represented with functional blocks. The digital controller, combined with the DSP and EPLD, is very flexible. An example is that the digital controller is modified to control a butterfly valve with the same hardware setup. A PWM space vector modulator is used to convert the duty cycle command from the current compensator to PWM gate switching signals. The flexibility of the three-phase modulator enables a space vector modulation (SVM) scheme that has the least circulating energy, low total harmonic distortions (THD), low switching loss and small digital delay.

Chapter 3 deals with the system-level design issues and their solutions in the DC bus regulator. Since the DC bus regulator is a multi-input and multi-output system, a classic cascaded control scheme is used to simplify the control design process. The inner loop is the inductor current feedback loop to achieve sinusoidal input current as well as PFC. The outer loop is the DC bus voltage loop that targets a stiff DC bus. Control design of the DC bus regulator is based on the large-signal average model in rotating d-q coordinates. The d-axis is aligned with the three-phase line voltage. Thus, the three-phase inductor current can be easily decoupled. Besides, active power and reactive power can be controlled independently. The designed control parameters are verified by the switching model built in the SABER simulation environment.

There are several issues in the implementation of the ZCT soft-switching technique for three-phase applications. One issue is how to control the ZCT PEBB module in a three-phase system. If the auxiliary switch gate signals are generated based only upon the main IGBT gate signals, there will be an overlap between the two auxiliary switch gate

signals in the same phase leg due to the complementary operation of the main switches. To avoid the shoot-through in the auxiliary switch branch, it is necessary to disable the auxiliary switch, the corresponding main switch of which is not carrying current.

Another important issue is the low-frequency harmonics in input phase current. Strong low-frequency harmonics will cause instability and significantly degrade the system performance. The causes of the low-frequency harmonics in this bus regulator are identified as pulse width limits (required by the ZCT soft switching), improper SVM schemes and dead time.

For the adopted soft-switching technique, the same resonant circuit functions for a time span at both turn-on and turn-off of the main switches. The consecutive soft-switching operations should not overlap. In other words, pulse width limits have to be applied. Otherwise, high spikes as twice as DC bus voltage will occur across the switches and destroy the switches. Unfortunately, the pulse width limits also can cause inaccurate duty cycle, which leads to severe waveform distortion and even instability in the bus regulator. It is found that different modulation schemes can have different outcomes under the same duty cycle limits. One continuous scheme is identified to be suitable for medium- and low-modulation indices. A discontinuous scheme is suitable for medium- and relatively high-modulation indices, which occur in the DC bus regulator. The 60°-clamping SVM scheme can significantly reduce switching loss. The second cause of low-frequency harmonics is use of improper SVM schemes. An asymmetrical SVM scheme is found to be the cause of the current spike at zero-crossings of the phase current waveform. The current waveform is distorted due to the sequence arrangement of the switching vectors. The inductor ripple current doubles at zero-crossings when the zero

vectors and output sequences change. The symmetrical scheme can eliminate this phenomenon. The third cause of the low-frequency harmonics is the dead time inserted into the gate signals of the two complementary switches in the same phase leg. A compensation scheme is provided to eliminate the low-frequency distortions due to the dead time. The adopted SVM scheme also alleviates the thermal stress in IGBT switches and resonant tanks.

Noises are always an important system-level issue in a high-power, high-voltage and high switching frequency PWM converter. Several practical approaches of the noise reduction in the DC bus regulator are briefly addressed.

Chapter 4 presents experimental results for both the ZCT PEBB modules and the digital control block. Critical protections are tested to verify that the DC bus regulator can handle extreme fault conditions. System-level operation tests of the bus regulator in the inverter mode and the rectifier mode are also given. Wide-range power tests from light load to full load are conducted with 20kHz switching frequency. Total harmonic distortion and efficiency curves are plotted to show how well the DC bus regulator performs.

Chapter 2 Subsystem Design

2.1 System Overview

Since this 100kW bus regulator is the front-end power source for the DC distributed power system, high performance (in terms of fast voltage control loop, unity power factor, high efficiency and high power density) is desirable. To achieve wide control bandwidth, high switching frequency and low THD are required. All these factors should be taken into consideration in system and subsystem design. Among them, minimizing switching loss (and thus increasing switching frequency) is the radical foundation necessary to achieve high performance because wide control bandwidth, high power density (due to the reduced passive component size) and low THD are based on high switching frequency. This is the reason an effective soft-switching technique is used in the bus regulator. The general specifications of this DC bus regulator are as follows:

- AC Input Voltage: 3Ø 60Hz 380~480V (Line to Line)
- DC Output Voltage: 800V
- Output Power: 100kW
- Switching Frequency: 20kHz
- THD under rated power level: <5%

The topology of this soft-switched DC bus regulator is shown in Figure 2.1. The main switches are S1 through S6, S1x through S6x and L-C branches comprise the auxiliary circuit. This bus regulator is basically a three-phase PWM voltage source converter with AC-side commutated soft-switching circuitry. The bus regulator converts three-phase AC power into DC power. This process is a boost operation due to the existence of the inductors at the input side of the switching network. This converter also can be run as an inverter with the reversed power flow, which is called inverter mode. If the AC side of the converter is connected to a three-phase utility power system, DC power also can be fed back to the utility in the inverter mode.

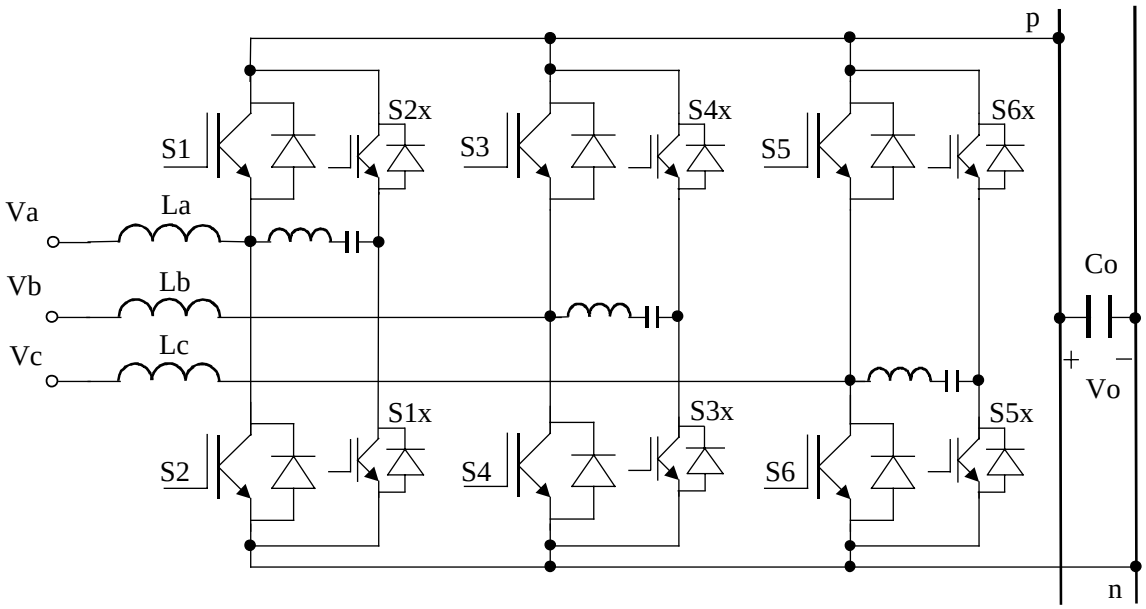


Figure 2.1 Circuit topology of the soft-switched DC bus regulator

The block diagram of the ZCT PEBB-based DC bus regulator is shown in Figure 2.2. It can be divided into two basic functional blocks: the power stage and the digital control block. The power stage mainly consists of three ZCT PEBB modules. From the

system perspective, these functional blocks are considered as subsystems. The design and implementation of each subsystem will be described in this chapter.

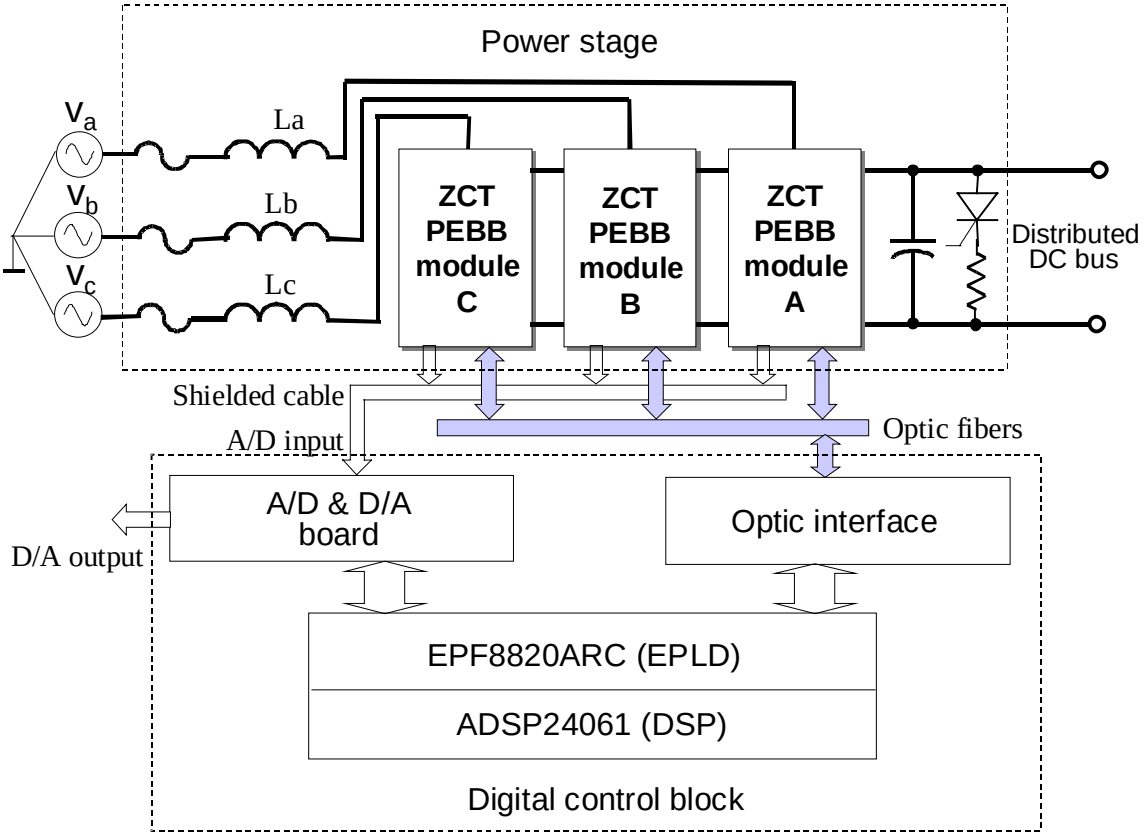


Figure 2.2 Overall system structure of the DC bus regulator

The power stage includes three ZCT PEBB modules, three boost inductors and a capacitor bank. A laminated bus is used as the distributed DC bus. The input boost inductors use amorphous magnetic core AMCC-630 due to the high switching frequency and high current. The inductance for the boost inductors is about 350μH. The capacitor bank has eight 360μF film capacitors with 450V rating each. Every two capacitors are connected in series to support 800V bus voltage. Resistors paralleled with the series capacitors are used to balance the capacitors' midpoint voltage level.

Plastic optic fibers connect ZCT PEBB modules to the digital control block. Using optic fibers effectively reduces common-mode noise sensitivity of the digital controller. This can also be regarded as an effort to decouple the high-frequency interference from PEBB modules to the control block under high voltage and high power level. Another potential benefit brought by the optic fibers is that they can minimize the number of wires between the digital control block and PEBB modules if a high-speed communication protocol is applied [12].

A picture of the four-layer DC bus regulator cabinet is shown in Figure 2.3. The digital controller, the A/D D/A board, the optic interface board and associated power supplies are on the highest layer. The second layer is the main part of the power stage, on which are three ZCT PEBB modules, a water-cooled heat sink, the laminated bus and the DC capacitor bank. On the third layer are the three boost inductors and a crowbar. AC and DC power connectors and input fuses are on the lowest layer.

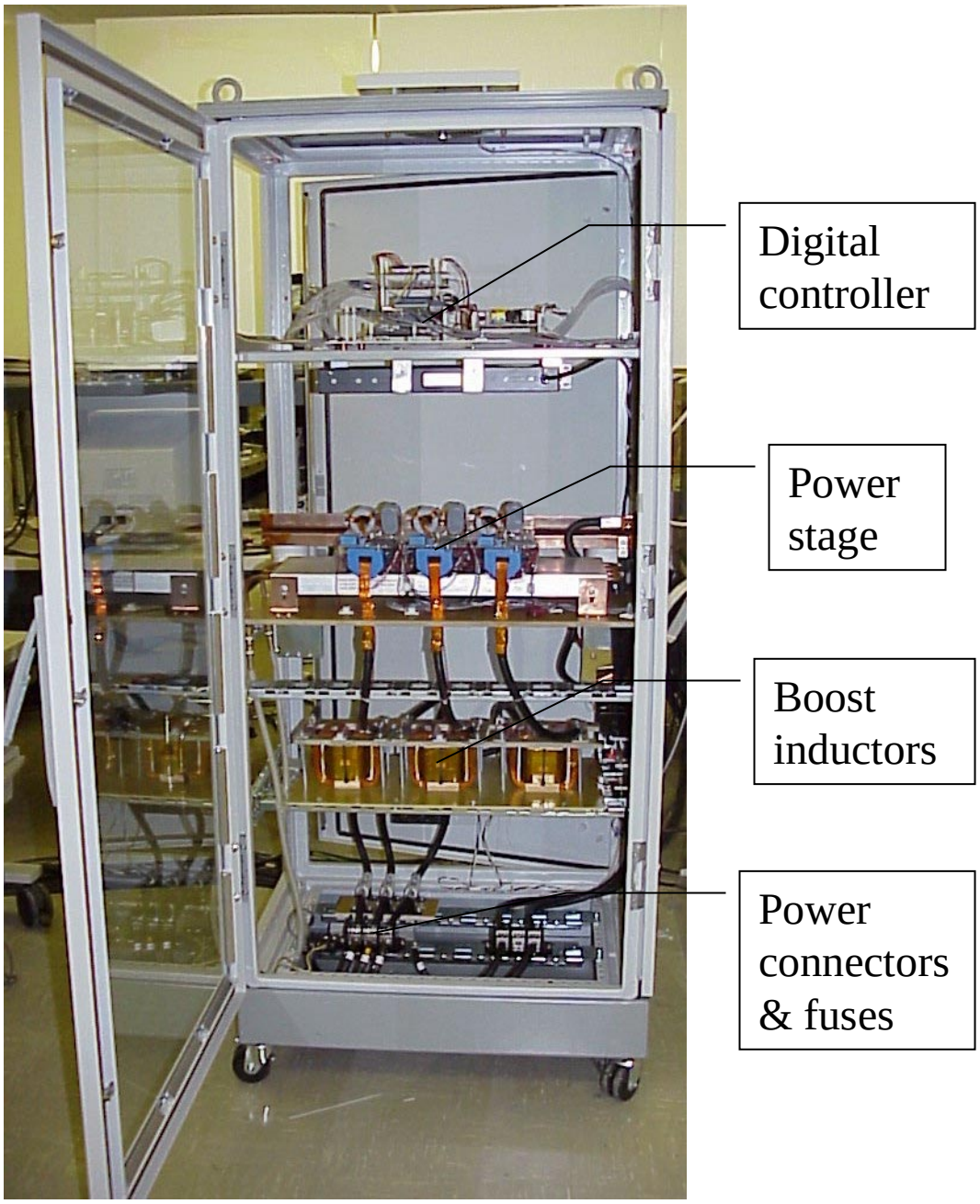


Figure 2.3 Picture of the 100kW DC bus regulator

2.2 ZCT PEBB Module

ZCT PEBB modules are the building blocks of the power stage. They are connected to the laminated DC distributed bus, as shown in Figure 2.4. The capacitor bank is mounted directly under the laminated bus. Three ZCT PEBB modules have identical interface in terms of power, signal and thermal connection. They are interchangeable. One ZCT PEBB module is a phase leg of the bus regulator.

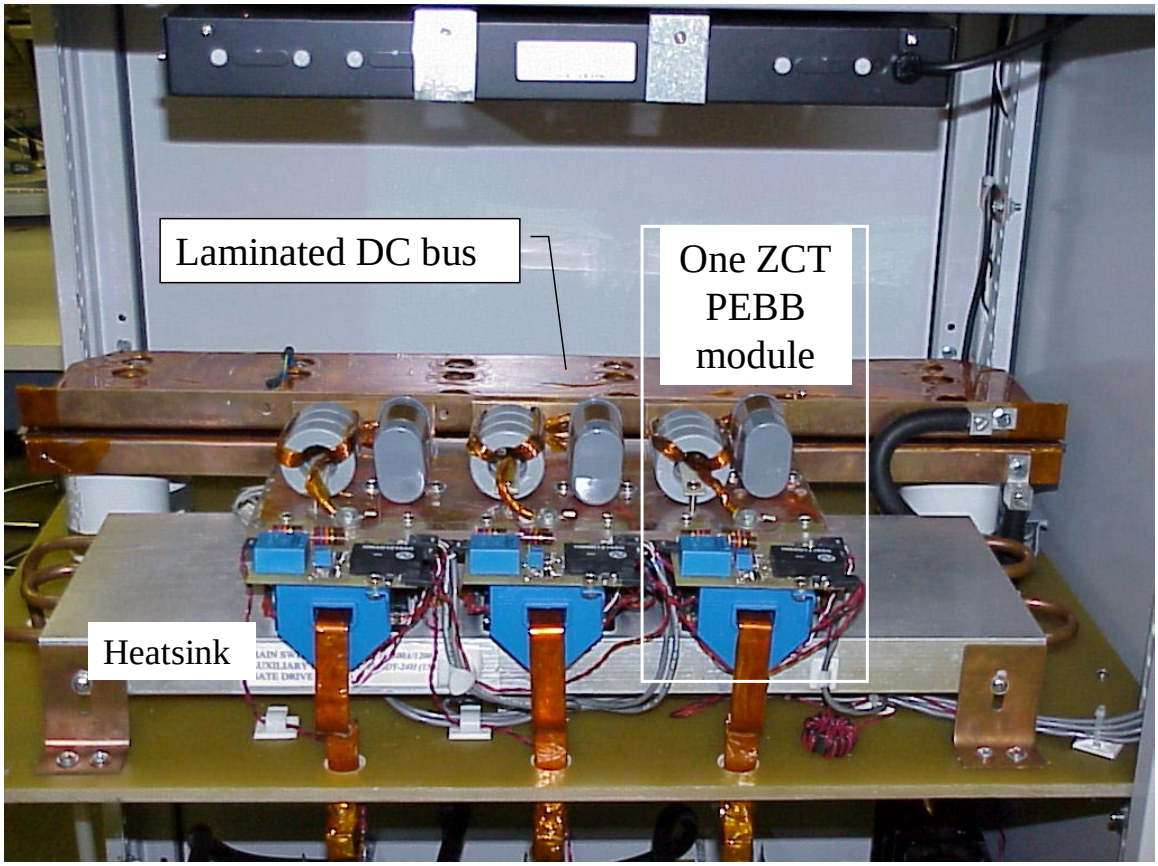


Figure 2.4 Picture of the power stage

2.2.1 Physical Structure of a ZCT PEBB Module

A ZCT PEBB module includes a main IGBT module, an auxiliary IGBT module, IGBT gate drive boards, a sensor board and a resonant tank. The structure of one ZCT PEBB module is illustrated in Figure 2.5. Stray inductance of a PEBB module is minimized by careful layout and the use of a laminated bus. The main and auxiliary IGBT switches are beneath the laminated bus. Gate drive boards are mounted around the IGBT modules (as shown in Figure 2.6) to make the PEBB module compact. In the future, a PEBB module may be integrated in one package. Better performance and much smaller size are expected.

Sensors are used to measure voltage and current of the PEBB module. In this converter, they are used to measure three-phase AC currents and voltages or DC bus voltage.

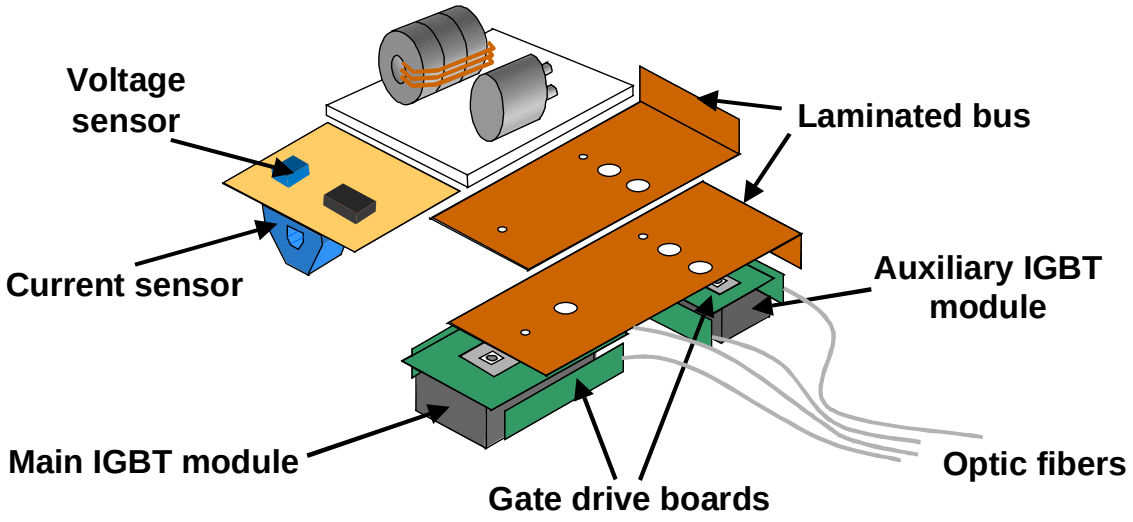


Figure 2.5 Structure of one ZCT PEBB module

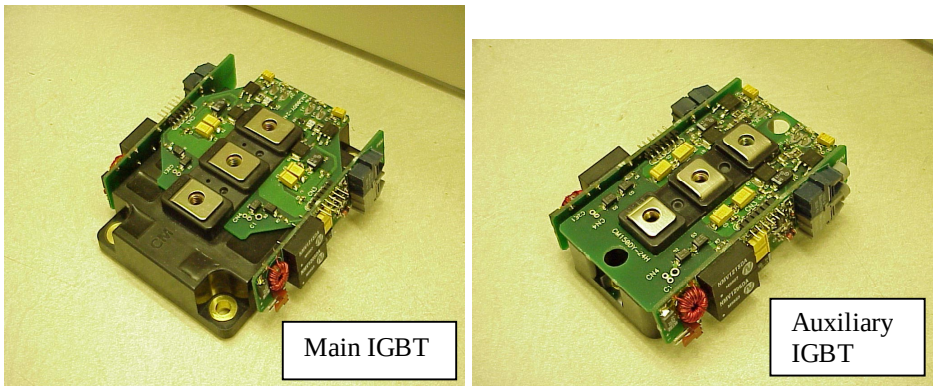


Figure 2.6 Main and auxiliary IGBTs and associated gate drive boards

2.2.2 ZCT Soft-Switching Topology and Operation Principle

Since all the PEBB modules in the bus regulator have the same structure, for the purpose of simplification, phase A PEBB module is used as an example for the soft-switching operation analysis. As shown in Figure 2.7, the topology of a ZCT PEBB module is similar to that of a full-bridge DC-DC converter, but the operation is different. Auxiliary switches and the resonant tank are activated only during the switching transitions of the corresponding main switches. The relationship between the main switch and its corresponding auxiliary switch in the PEBB module topology is diagonal. This means the control timing of S1x is related to S1, and S2x is related to S2.

From the operating perspective, a ZCT PEBB module can be regarded as the combination of two soft-switching cells. One of the switching cells is shown within the shaded area of Figure 2.7. Due to the symmetry of the two soft-switching cells in the same PEBB module, the analysis of ZCT soft-switching operation in a PEBB module can be confined to the operation in a switching cell.

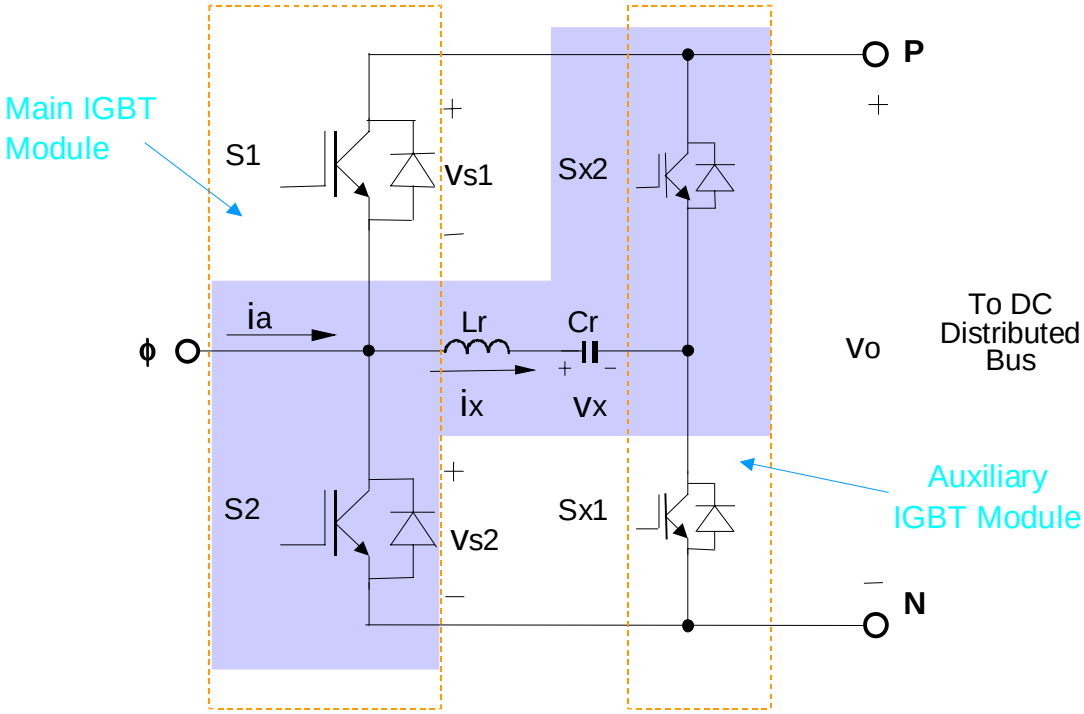


Figure 2.7 Topology of one ZCT PEBB module

A switching cycle is enough for the soft-switching operation analysis in this DC bus regulator. Assume the positive amplitude of phase C current is the largest. Only phase A and phase B are switching. The gate signals for S2, S4, S6 and S2x are shown in Figure 2.8. There are 11 operating stages for a complete soft-switching cycle. The key waveforms and control timings are shown in Figure 2.8. Figure 2.9 shows five sub-topologies for soft-switching operation during the turn-on transition of S2, while Figure 2.10 shows six sub-topologies for the turn-off transition of S2.

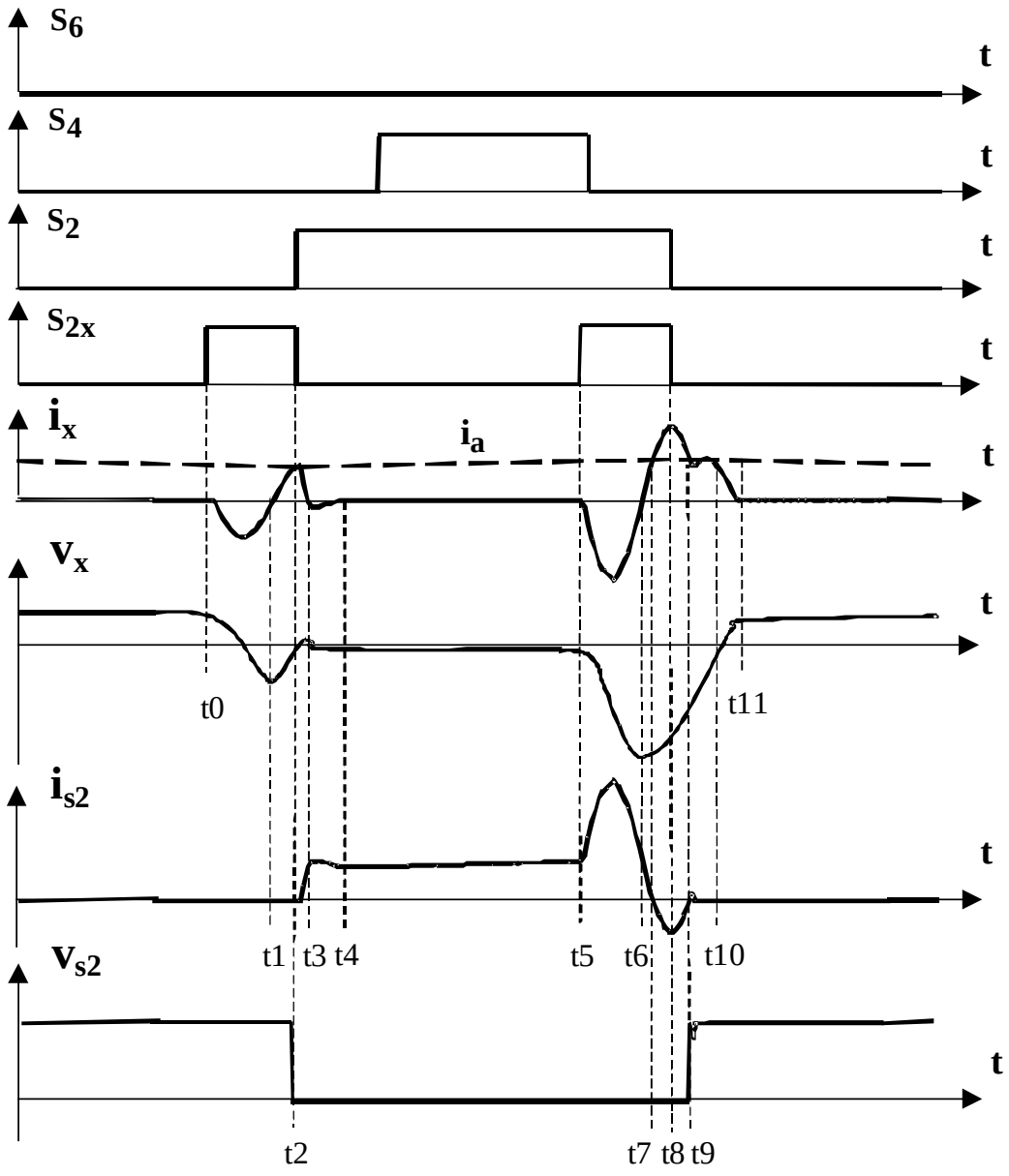


Figure 2.8 ZCT soft-switching waveforms for a switching cycle

Assume the boost inductor current i_a and output capacitor voltage V_o are constant due to their large inductance and capacitance. The initial conditions before the turn-on transition are as follows: voltage across the resonant capacitor C_r is positive; current in resonant inductor L_r is zero; current in the boost inductor is positive. All the reference directions are denoted in Figure 2.7.

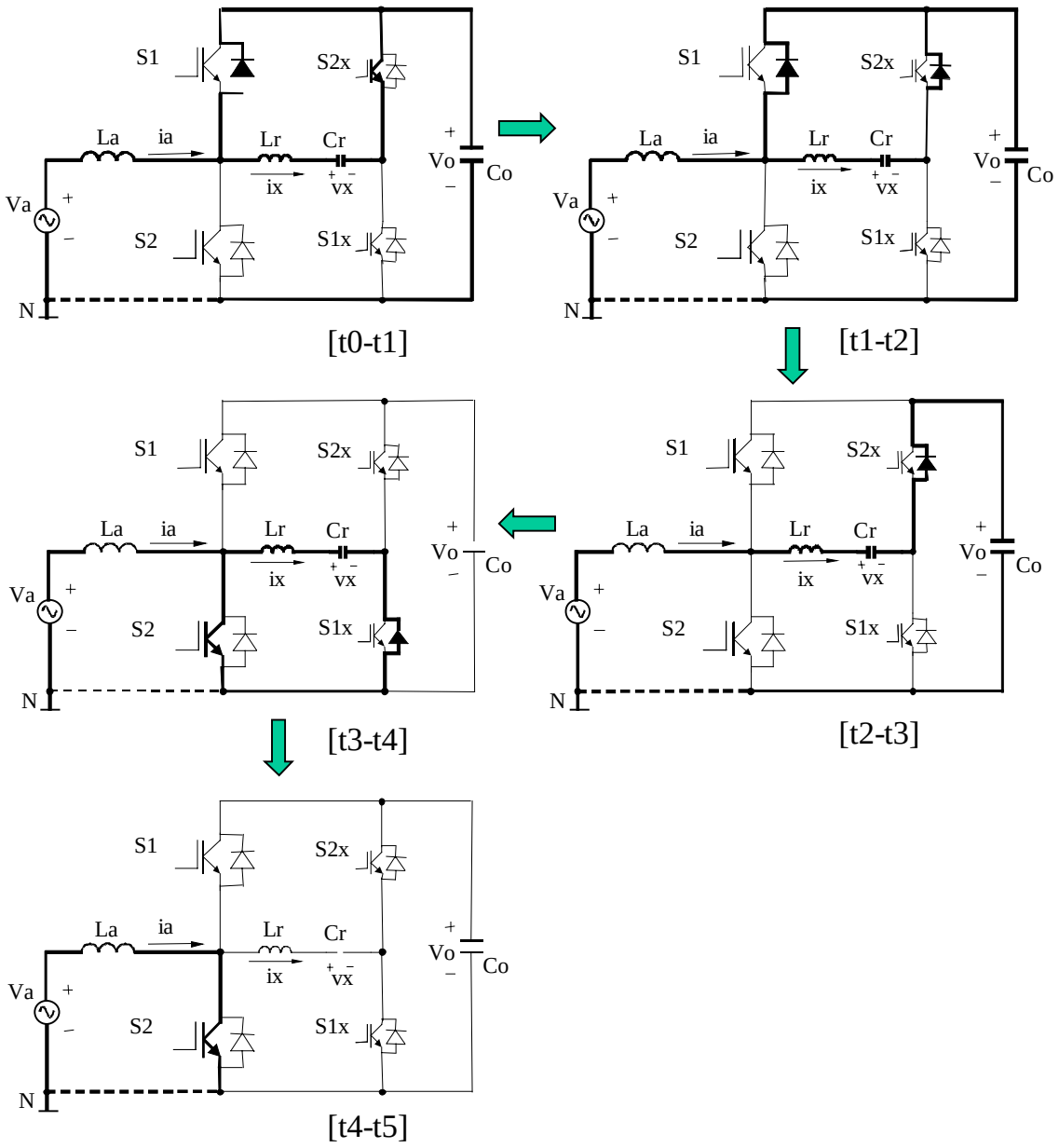


Figure 2.9 Operation stages for turn-on transition of the main switch S2

Period [t0 – t4] is the turn-on transition. At t0, S2x is turned on. The auxiliary resonant tank begins to resonate. Resonant tank current ix reaches zero at t1 and then changes direction. The anti-parallel diode of S2x conducts when ix is negative. Almost all the current in the freewheeling diode of main switch S1 can be diverted into the

resonant tank at t2. Diode reverse recovery is almost eliminated. At that time, the main switch S2 is turned on under zero current. The gate signal of S1 is removed at the same instant because the current is being conducted by its anti-parallel diode. After t2, ix falls rapidly because S2 introduces high output voltage V_o in the resonant path. The di/dt of the main switch current is controlled by the resonant inductor. Therefore, di/dt is less than in a hard switching scenario. At t3, ix reaches zero again. After t3, ix is commutated to the anti-parallel diode of S1x, and the diode is naturally turned off at t4. The auxiliary circuit stops resonating at t4.

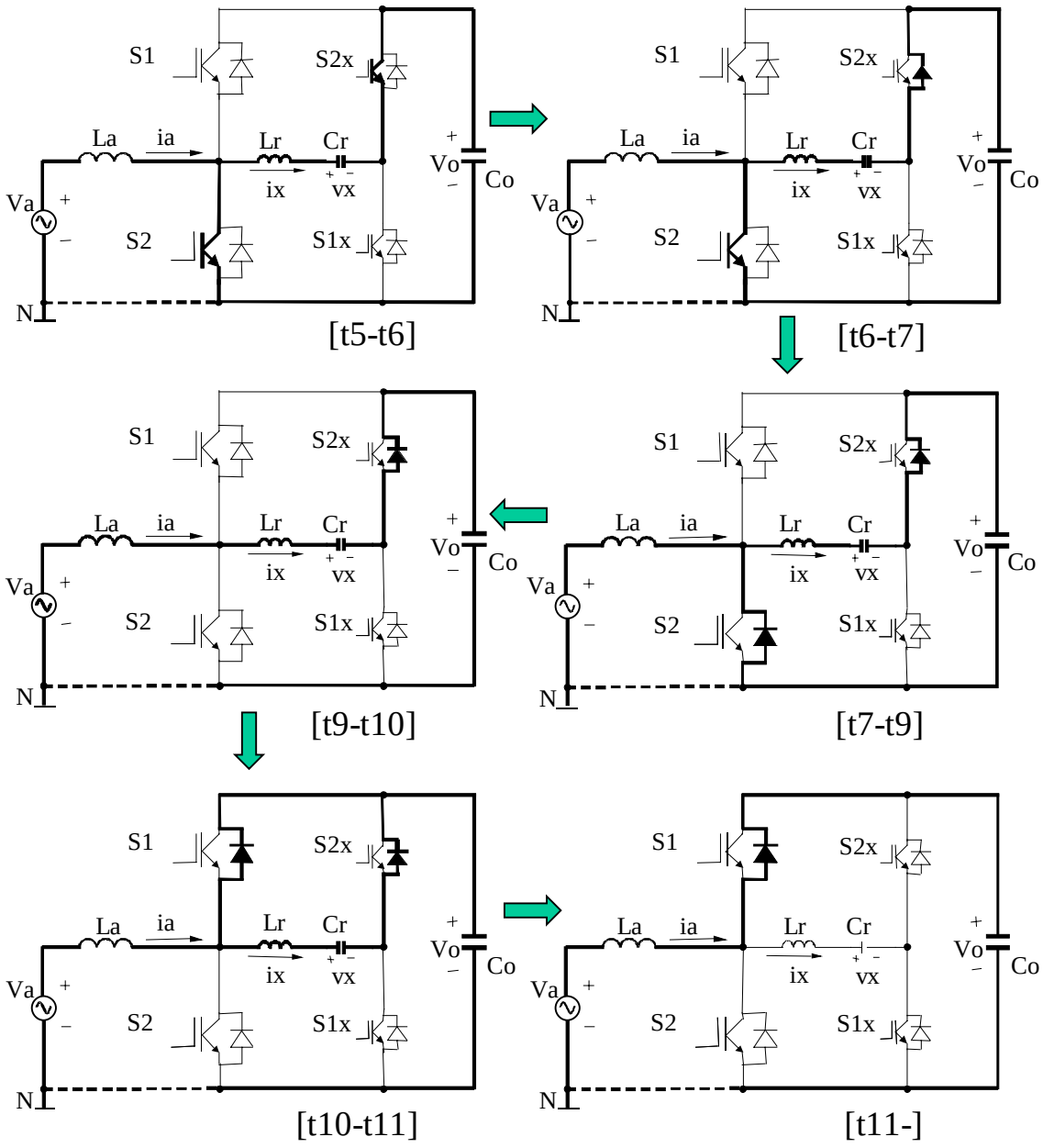


Figure 2.10 Operation stages for turn-off transition of the main switch S2

Turn-off transition begins at t5 and ends at t11. At t5, S_{2x} is turned on again. The resonant tank starts to resonate. Resonant tank current ix changes direction at t6. At t7, ix is the same as input current i_a. That means all the input current is commutated into the auxiliary circuit. At t8, ix reaches its maximum amplitude. Main switch S_2 and auxiliary switch S_{2x} are turned off simultaneously at t8 without causing any turn-off loss. Since

neither the main nor the auxiliary switches are carrying any current during the time period between t8 and t9, it is desirable for the minority carriers to recombine in the main IGBT switch S_2. At t10 ix decreases to i_a and Vx is discharged to zero. The anti-parallel diode of main switch S_1 begins to conduct after t10. At t11 ix resonates to zero. The di/dt in the main circuit diode is also determined by the resonant inductor. The auxiliary circuit is disconnected from the main circuit after t11. Vx is charged to positive, and is then ready for the next turn-on transition.

Figure 2.8 shows that both leading and trailing edges of the main switch PWM signal occur at exactly the same instant as the falling edge of the auxiliary switch gate signal. This kind of timing arrangement facilitates the real implementation.

2.2.3 Resonant Tank Design

The resonant tank is designed to make the resonant tank peak current i_{pk} exceed the instantaneous maximum input current to be commutated and allow a time span for minority carriers to recombine. A tradeoff is made when choosing the resonant period T_o. If T_o is too long, the duty cycle loss will be high. If T_o is too short, it will have a negative effect on switching loss reduction and also make the control timing implementation difficult. Resonant inductor L_r and resonant capacitor C_r can be selected based on the rated input phase current (120A RMS) and Equations 2-1–2-3. V_o is the DC bus voltage (800V) in Equation 2-3.

$$T_o = 2\pi\sqrt{L_r C_r} \qquad (2\text{-}1)$$

$$Z_o = \sqrt{L_r / C_r} \tag{2-2}$$

$$I_{pk} \approx V_o / Z_o \tag{2-3}$$

A pair of resonant tank parameters is selected, L_r=2.0μH and C_r=0.25μF. Toroid core 55440A2 is used for the resonant inductor to avoid fringing effects. The resonant period T_o is about 4μs. The calculated I_{pk} is about 280A. However, the measured resonant peak current is less than 240A due to the existing ESR in the resonant tank.

2.2.4 IGBT Gate Drive Circuit Design

IGBT gate drive boards are directly mounted around IGBT modules. The schematic of the IGBT gate drive board is shown in Figure 2.11. The driver IC is the MC33153 from Motorola. This eight-pin surface-mounted chip incorporates several protection functions with the gate drive. One protection is the under-voltage lockout, which disable the gate drive signal when the power supply voltage for the gate drive is below 11V. Another protection is the desaturation/programmable blanking time protection, which turns off the IGBT switch when short circuit occurs.

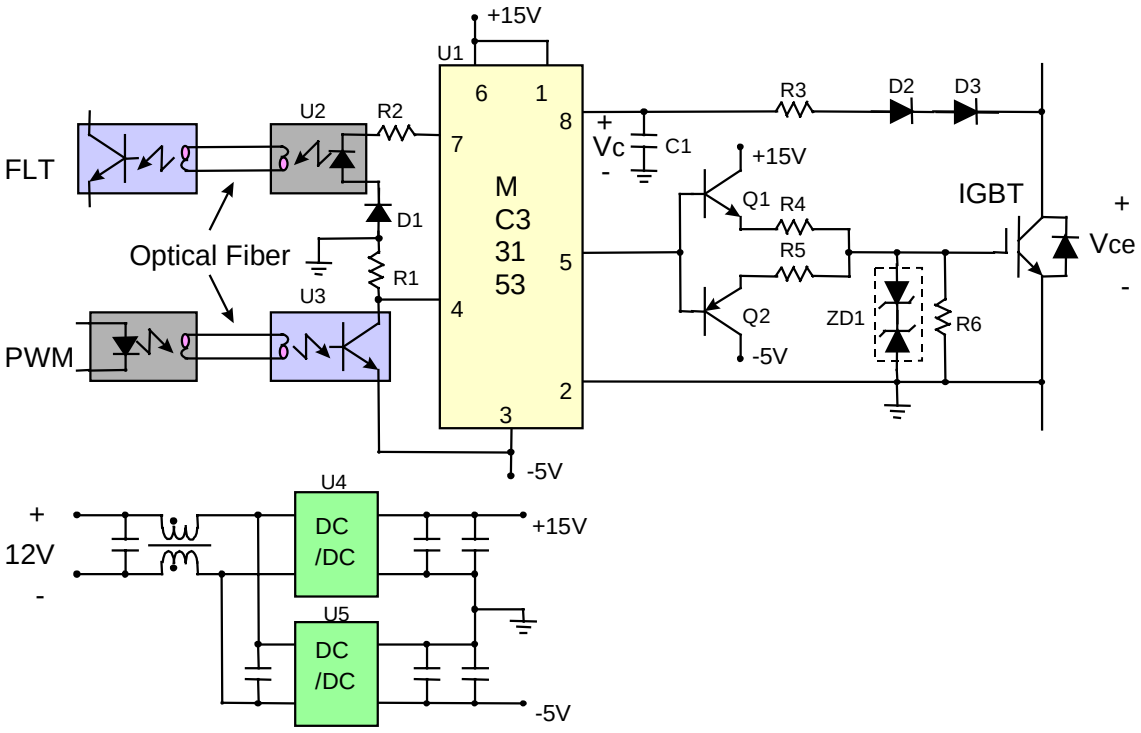


Figure 2.11 IGBT gate drive schematic

There is a built-in constant current source (I_s=270μA) charging the capacitor C1 after the gate drive signal goes high. When the threshold voltage V_{th}=6.5V, the charging time Tc is given by the following equation:

$$T_c \approx C_1 \cdot V_{th} / I_s . \qquad (2\text{-}4)$$

In this gate drive design, C1 is 270pF to achieve 6.5μs blank time. This time span is used to blank parasitic ringing following the IGBT turn-on. To set the threshold for desaturation protection, a resistor R3 is inserted between D2 and C1. When the IGBT switch is on, the current flowing in the IGBT will cause voltage drop Vce. The current source in the MC33153 charges the capacitor C1 and causes forward bias in diodes D2 and D3. The voltage across the capacitor C1 is Vc. Vc is given by Equation 2-5. The

threshold for Vc is 6.5V. When Vc exceeds this threshold, the gate signal will be disabled.

$$V_c = V_{R3} + V_{d2} + V_{d3} + V_{ce} \ , \qquad (2\text{-}5)$$

where $V_{R3} = I_s \cdot R_3$.

Assume the voltage drop across each of the two diodes is Vd_1=Vd_2=0.7V. Since Vce increases with the switch current, by choosing a resistance value for R3, the desaturation protection threshold is set. As is discussed further in the Chapter 4, the resistor R3 for main switches is 6.9kΩ, and the corresponding protection IGBT switch current is 450A. The threshold for auxiliary switches is 290A when R3 is equal to 5.7kΩ. Based on this information, the voltage drop for the main IGBT switch at 450A is about 3.3V. The voltage drop for the main IGBT switch at 290A is about 3.6V. And vice versa, the resistance of R3 can be calculated based on the corresponding voltage drop under the intended protection switch current, which is given by the data sheet of the IGBT switch.

A push-pull transistor pair is used to amplify the gate drive signal from MC33153. R_4 is the turn-on gate resistor that controls the turn on di/dt of the IGBT switch. It is necessary to make the tradeoff between turn-on speed and associated switching loss. The smaller R4 is, the more quickly the IGBT is turned on, and the more severe the diode reverse recovery is caused. If R4 is too large, associated turn-on loss increases (because the overlap of the switch current and voltage increase). The turn-off gate resistor R5 should be chosen much smaller than the turn-on resistor R4 in order to keep the IGBT off under the switching transitions of the complementary switches. Too-small turn-off

resistance will cause large turn-off voltage overshoot, but this is not an issue with the properly designed ZCT soft-switching network.

For main IGBT switches, 6.5Ω resistors are used for gate turn-on and 1.4Ω for gate turn-off. For auxiliary IGBTs, R4 is 5Ω and R5 is 1Ω. The component lists for the common part of the main and auxiliary IGBT switches are shown in Table 2-1. Decoupling capacitors for gate drive power supply are not listed.

Table 2-1 Component list for the IGBT gate drive boards

Item	REF	Name	Type	Description
1	U1	Gate Driver IC	MC33153	
2	U2	Optic Fiber Transducer	HFBR-1521	
3	U3	Optic Fiber Receiver	HFBR-2521	
4	U4	DC-DC Power Supply	NMV1215DA	3 kV DC Isolated 1 W 15 V Output
5	U5	DC-DC Power Supply	NMV1205DA	3 kV DC Isolated 1 W 5 V Output
6	R1	Resistor	1.8kΩ	
7	R2	Resistor	220Ω	
8	C1	Capacitor	270pF	
9	D1	Diode	1N4148	
10	D2, D3	Fast Recovery Diode	FR107	
11	ZD1	Zener Diode	MMBZ15VALT1	
12	Q1	NPN Transistor	MDJ200	
13	Q2	PNP Transistor	MDJ210	

2.2.5 Switching Frequency

The power capability of the IGBT gate drive circuit is associated with the switching frequency. The higher the switching frequency, the more gate power is required.

Switching frequency tests on the IGBT gate drive circuit are conducted. Four different levels of gate resistance (from 2.2Ω to 11Ω) are used to investigate the input power dissipation versus the switching frequency. As shown in Figure 2.12, the gate resistance basically does not affect the gate drive power dissipation for the investigated frequency range. The rated output power of the two DC-DC power supplies on one IGBT gate drive board are 1W each. Considering uneven power consumption in the positive and negative power supplies, the total capability of the two power supplies is estimated as 1.5W. Therefore, a reasonable switching frequency limit for the designed gate drive is 35 kHz from the curve plots in Figure 2.12.

Switching frequency is also limited by soft-switching techniques due to the associated duty cycle loss. As will be analyzed in Chapter 3, the minimal pulse width limit is about 6μs. That is a 12% duty cycle loss at 20kHz switching frequency. Further increasing the switching frequency may lead to severe low-frequency harmonics.

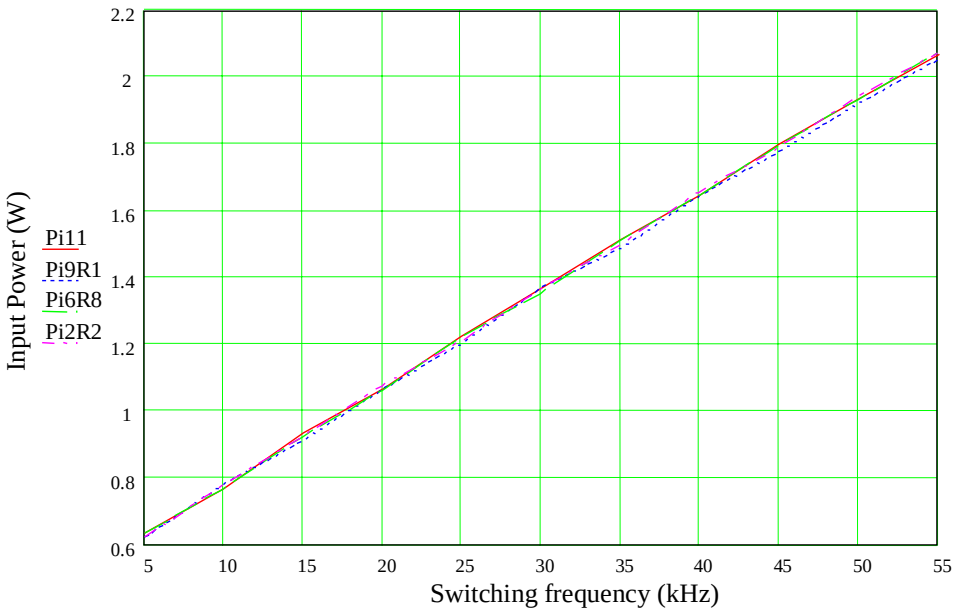


Figure 2.12. Input power of gate drive board vs. switching frequency with different gate (turn-on) resistors

2.3 Thermal Issues on Power Stage

Although the ZCT soft-switching technique can significantly reduce the switching loss of the PEBB modules, both active switches and passive components of the power stage are still subject to high electrical and thermal stress because of the high power and high operating switching frequency. The resonant circuit operates with doubled frequency because the ZCT soft switching circuitry functions at both turn-on and turn-off transitions. In fact, part of the switching loss reduction is dissipated in the form of conduction loss in the resonant tank and main and auxiliary switches. Since passive components normally have poor thermal transfer capability (compared with active switches/diodes), thermal issues very likely exist for passive components, too. A test setup (shown in Figure 2.13) is used to investigate the thermal issues on the power stage.

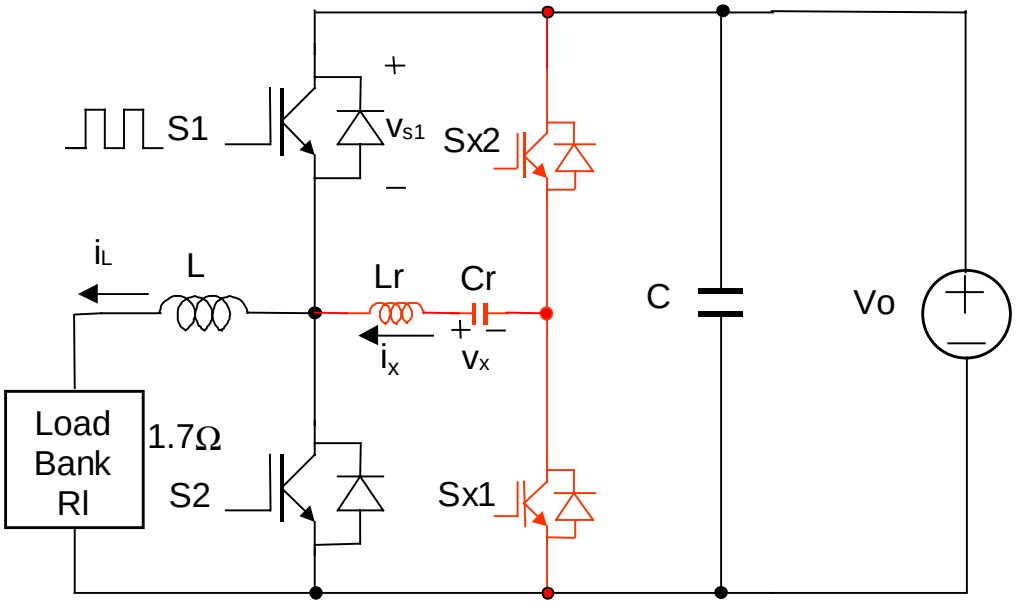


Figure 2.13 Test setup for thermal investigation

The temperature of the resonant capacitor Cr versus DC bus voltage Vo is shown in Figure 2.14. The room temperature is 24°C. Each test point is obtained after 30 minutes of operation. Both current and voltage of the resonant capacitor increase proportionally to the DC bus voltage. Obviously, the steady-state temperature of the resonant capacitor exceeds its rating (80°C) before the DC bus reaches 800V. The 800V DC bus test is done in a relatively short time before the resonant capacitor temperature goes too high.

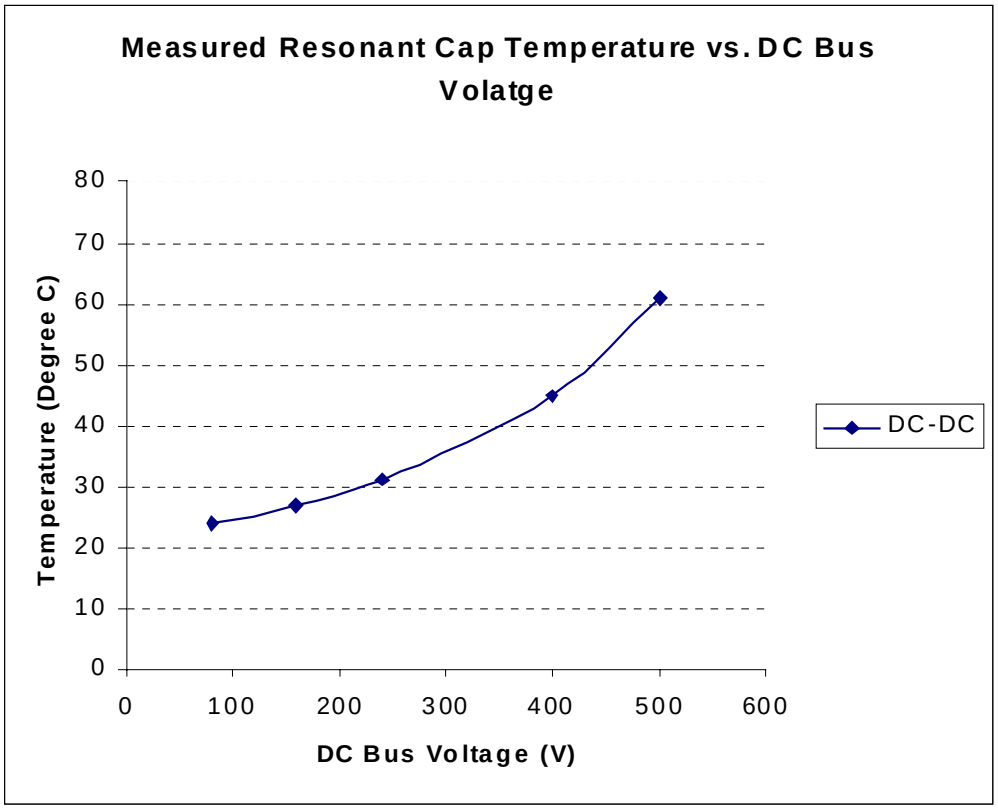


Figure 2.14. Measured resonant capacitor temperature

It is evident that the existing thermal issue in the resonant capacitor may prohibit high switching frequency operation of PEBB modules. The measured RMS current of the resonant tank (47A) almost reaches the current rating of the resonant capacitor (50A RMS) under 800V with 20kHz switching frequency. Resonant capacitors with higher

current and better thermal capability have to be chosen. However, it is difficult to find resonant capacitors that can withstand high peak voltage, higher RMS current, that have low profile that can be accommodated in the ZCT PEBB module. This issue is solved by 60°-clamping SVM scheme, which will be addressed later in this chapter. The RMS current is reduced by 10A under 800V because the effective switching events per phase are reduced one third. Adding triple cooling fans can further reduce the temperature rise. The temperature measurement with these solutions is shown in Figure 2.15 as PFC (three-phase operation) compared with the previous case as DC-DC (operation). From the curve plot, there is no problem for the DC bus regulator to operate with the 800V DC bus.

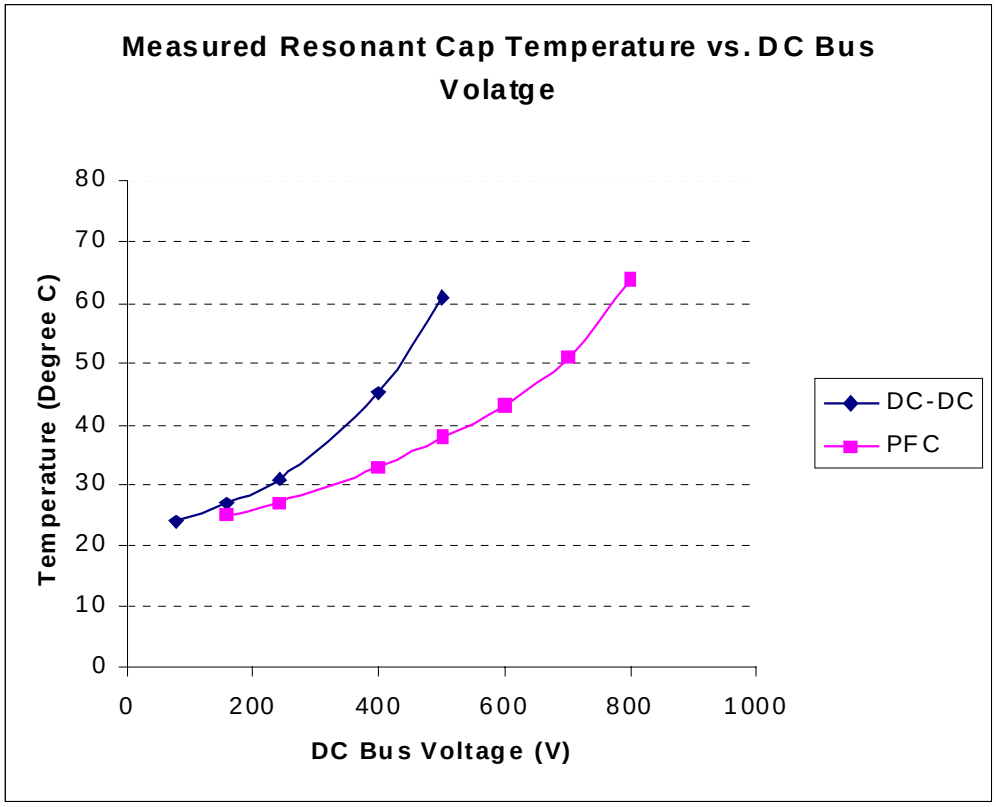


Figure 2.15 Comparison between DC-DC and PFC with the reduced thermal issue

Another thermal issue is the thermal capability of the heatsink for the PEBB modules. Figure 2.16 shows the temperature rise of the heatsink and plastic case of the main IGBT switch at different power levels. The switching frequency is set to 10kHz to avoid the thermal issue in the resonant capacitor (as discussed above). The environment temperature is 24°C. The heatsink is cooled by 21°C unregulated flowing water. All the test data are recorded after 30 minutes of steady-state operation, except the data under 18kW. Since tests are conducted on one of the two switching cells in a PEBB module, 18kW on a switching cell is equivalent to 100kW for three PEBB modules. The plastic case temperature of the main IGBT reaches 64°C and continues rising when input power reaches 18kW. Due to the large thermal impedance between the plastic case and the junction of the IGBT switch, the junction temperature is extremely high. IGBT failure occurs at this test point.

As 18kW power for one switching cell in a PEBB module is equivalent to 100kW for six switching cells, it is impossible for the DC bus regulator to run at 100kW power level without improving the thermal management. Actually, the situation at 100kW is worse for three reasons: first, if one switch in the three-phase operation is assumed to have the same loss as in DC-DC operation when handling the same amount of power, the power loss for six switching cells is six times that of one switching cell. But the power dissipation capability of the heat sink under the same cooling condition is fixed. The heatsink will have much higher temperature rise for the 100kW DC bus regulator. Second, power loss doubles in one PEBB module because two switching cells are working alternatively. The doubled power loss will also result in higher case temperature rise due to the fixed thermal impedance of a IGBT module package. Third, the average

switching frequency of each phase is 13.3kHz in three-phase operation (higher than 10kHz in DC-DC operation).

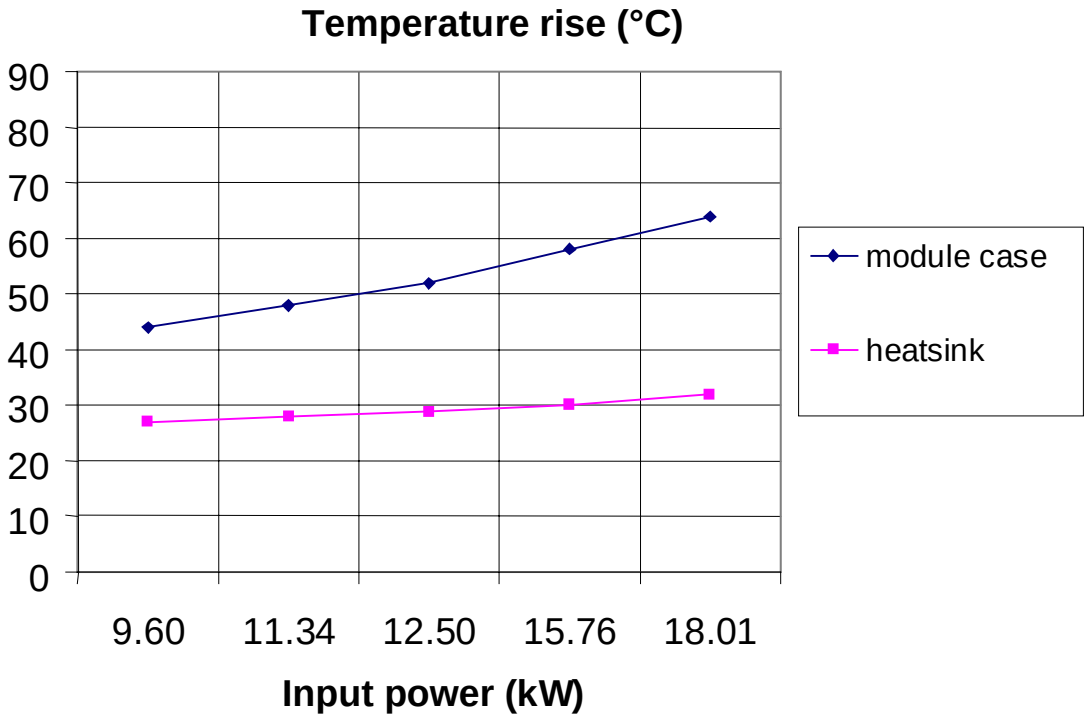


Figure 2.16. Temperature rise for heatsink and IGBT plastic case

The solution is using fast flowing cooling water with regulated temperature (e.g. 10°C). The measured heatsink temperature is about 29°C under 100kW with the improved thermal management.

2.4 Digital Control Block

As shown in the overall system structure (Figure 2.2), the digital control block consists of a DSP, an EPLD, an A/D D/A board and fiber optic interface. Figure 2.17 shows the digital controller used in the setup. The SHARC DSP is a 32-bit 33MHz processor with floating point calculation capability from ANALOG DEVICE. The EPLD used here is an EPF8820ARC from ALTERA Company, which is fast enough to be compatible with the SHARC DSP. In this digital control block, the DSP performs control algorithms (e.g. current loop and voltage loop compensators, coordinate transformation and line voltage synchronization). The EPLD implements the peripheral digital circuit of the DSP and the time critical functions, such as the PWM space vector synthesis and fault protection.

Both the DSP and the EPLD are flexible for programming. Different versions of DSP and EPLD codes for this DC bus regulator in inverter and rectifier mode, with or without ZCT soft switching, have been developed. The implementation of the DSP program and the EPLD design will be discussed later in this chapter.

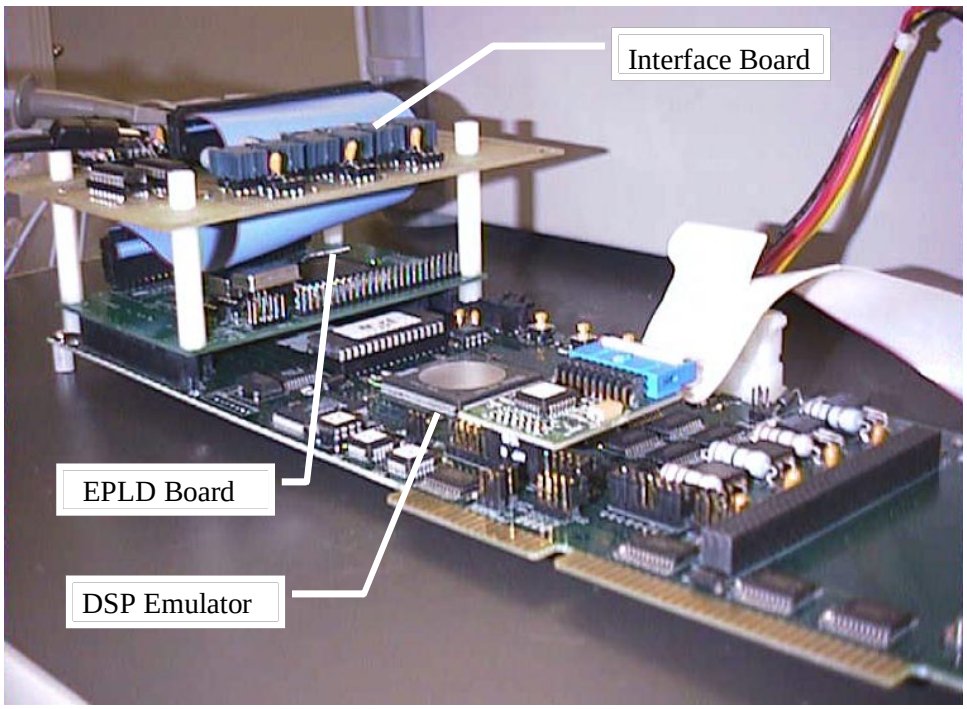


Figure 2.17 Picture of the digital controller

The A/D D/A board is used to convert the sensed signals from the PEBB modules to the DSP and send digital signals from the DSP to the output test pins. The test pins can be used to debug the DSP controller or to measure the loop gain of the DC bus regulator. There are 4X4 10-bit A/D channels with 20MSPS sampling speed on the A/D D/A board.

The interface board acts as a relay for distributing PWM signals from the EPLD to the PEBB modules and collecting fault signals from PEBB modules via optic fibers. The transmitter and receiver circuit for the optic fibers is shown in Figure 2.18.

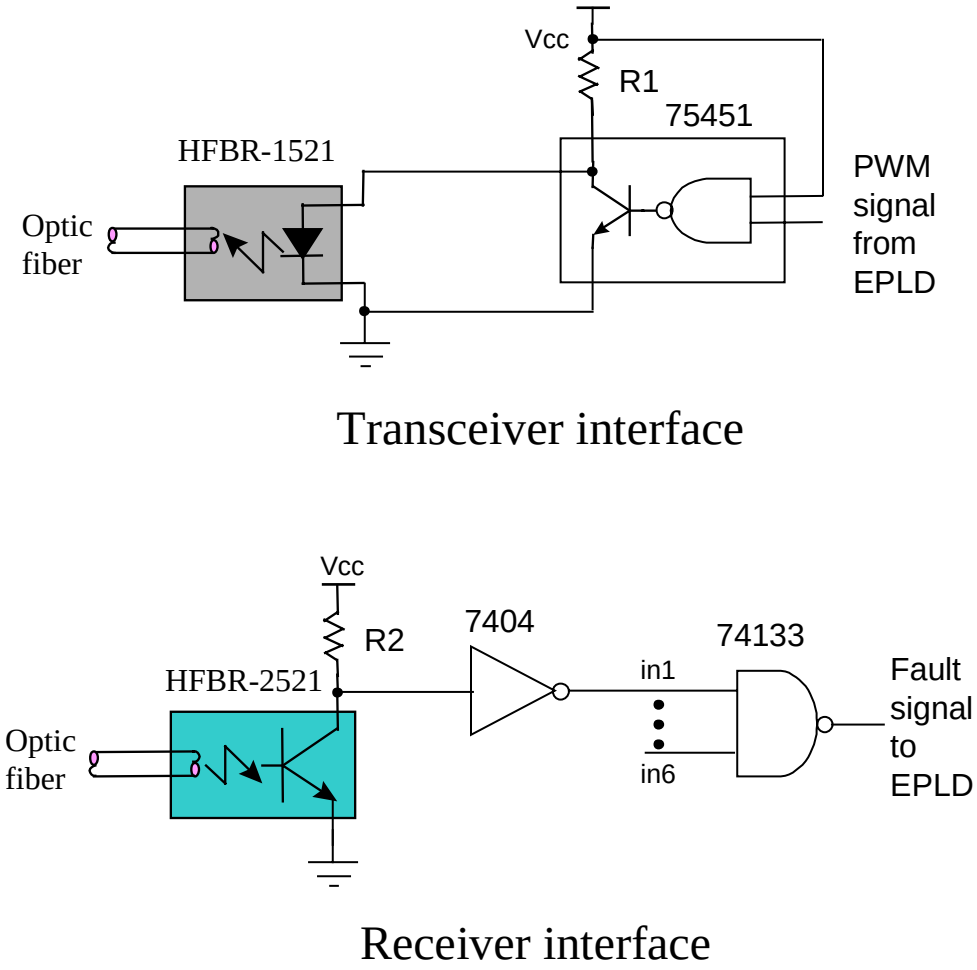


Figure 2.18 Interface circuit for optic fibers

2.4.1 PWM Space Vector Modulator

The control functional block diagram of the bus regulator is shown in Figure 2.19. The voltage and current loop compensators are designed (as will be discussed in chapter 3) based on the small-signal analysis in the d-q coordinates. The output of the voltage regulator is the reference for the d-channel current compensator. The output of the current regulator is the duty cycle information dd and dq. The control effect of the duty cycle is to generate the three-phase sinusoidal PWM voltage at the input side of the switching

network. The PWM space vector modulator is used to generate the gate signals for the main IGBT switches based on the duty cycle information. The soft-switching pulses for auxiliary switches are generated according to the main switch gate signals.

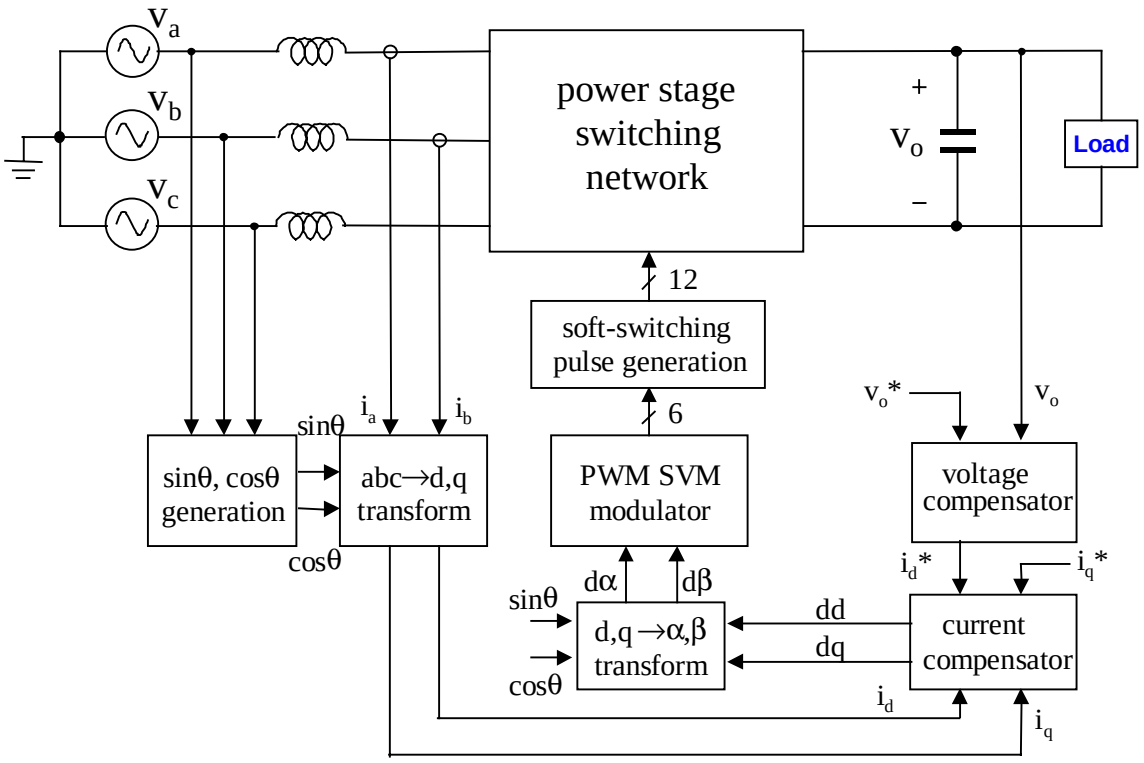


Figure 2.19 Functional block diagram of the soft-switched bus regulator

As stated in Chapter 3, voltage vector $\vec{V}_m$ represents the three-phase voltage at the input side of the switching network, which is generated by PWM switching the DC link voltage. There are eight valid switching combinations (called space vectors) available in the switching network. The eight vectors, shown in Figure 2.20, are named V0 thru V7. Among them, V0 and V7 are called zero vectors. The other six vectors are called nonzero vectors. The relationships between the vectors and the switching combinations are listed

in Table 2-2, where "p" denotes that the corresponding phase is connected to the positive DC rail, while "n" denotes that the phase is connected to the negative DC rail.

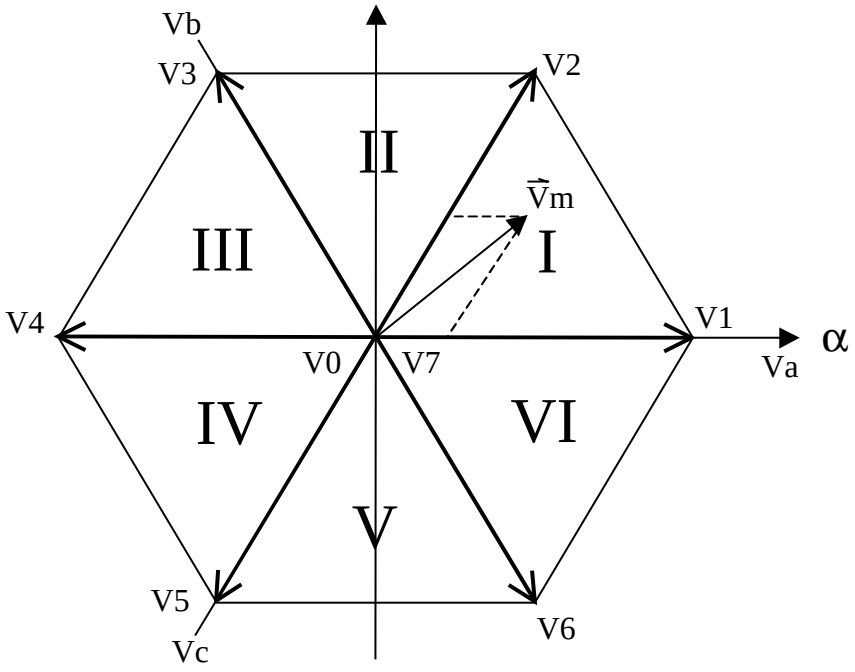


Figure 2.20 Space vector hexagon

Table 2-2 Relationships between the vectors and switching combinations

Vector	V0	V1	V2	V3	V4	V5	V6	V7
Switching combination (in the order of A, B, C)	nnn	pnn	ppn	npn	npp	nnp	pnp	ppp

For the same $\vec{V}_m$, there is more than one solution. The way to synthesize the voltage vector by the eight space vectors is called the space vector modulation (SVM) scheme. An enormous number of SVM schemes have been proposed during the past

several decades. Different SVM schemes can cause different switching losses and THD. A scheme that has less switching loss normally has more THD, and vice versa.

For this high-power application, it is very important to minimize the switching loss, as long as the THD is not consequently made too large. Three steps facilitate this process. First, adjacent nonzero vectors are selected to synthesize the reference voltage vector to minimize the circulating energy. For the reference vector shown in Figure 2.20, nonzero vectors V1 and V2 are chosen. Second, via a properly selected zero vector, the phase carrying the highest current does not switch at all. This method can save one-third of the switching events in every switching cycle, compared with the conventional scheme (as shown in Figure 2.21), which has six commutations in one switching cycle. This method can also reduce the peak switching current more than 13% below the conventional one. The total effective switching loss reduction for a line cycle is about 50%. Additionally, reduced peak switched current also leads to the reduction of the designed peak resonant tank current. Third, the sequencing of the vectors is chosen to minimize the switching actions. Such a scheme (shown in Figure 2.22) is called 60°-clamping SVM [17] because the phase with the highest current is clamped by the diode for a 60° period.

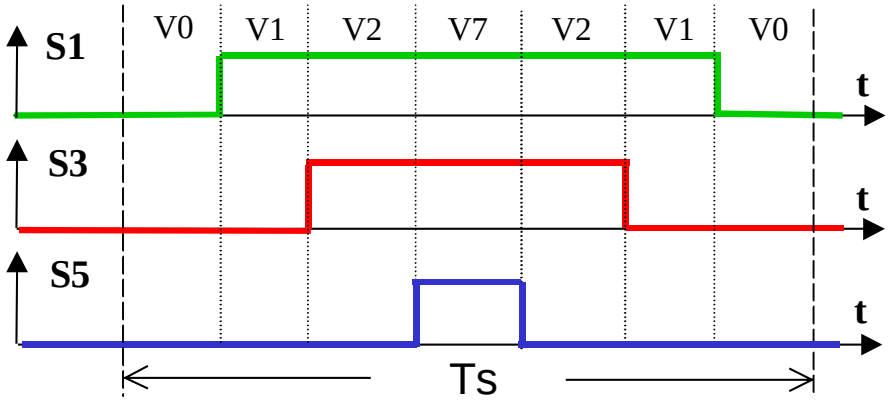


Figure 2.21 Conventional SVM scheme

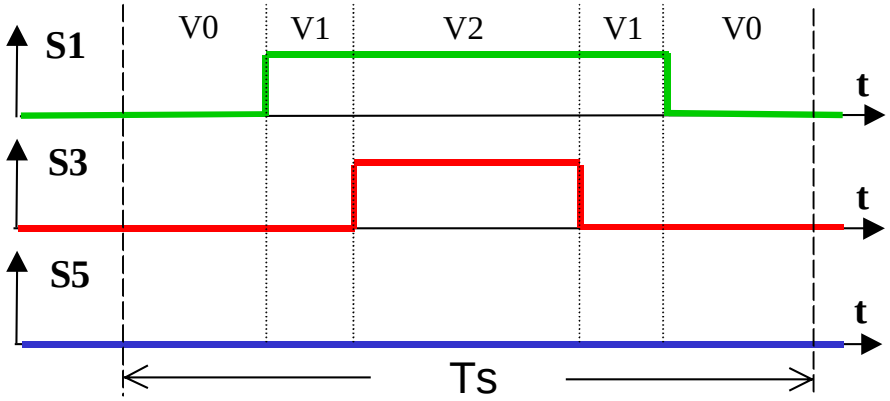


Figure 2.22 The 60°-clamping SVM

Due to the small voltage drop across the boost inductors of the DC bus regulator, the input current vector $\vec{i}_s$ is almost in phase with the reference vector $\vec{V}_m$. This means that when the phase voltage is the highest, its phase current is also the highest. The simple implementation of the 60°-clamping SVM is shown in Figure 2.23. For each 60° interval in the shaded area, zero vector V0 is applied. For the other intervals, zero vector V7 is selected. Therefore, for each 60° sector, denoted as I, II, … VI, the nonzero vectors are identical. Two zero vectors are applied for a 30° interval respectively in each sector.

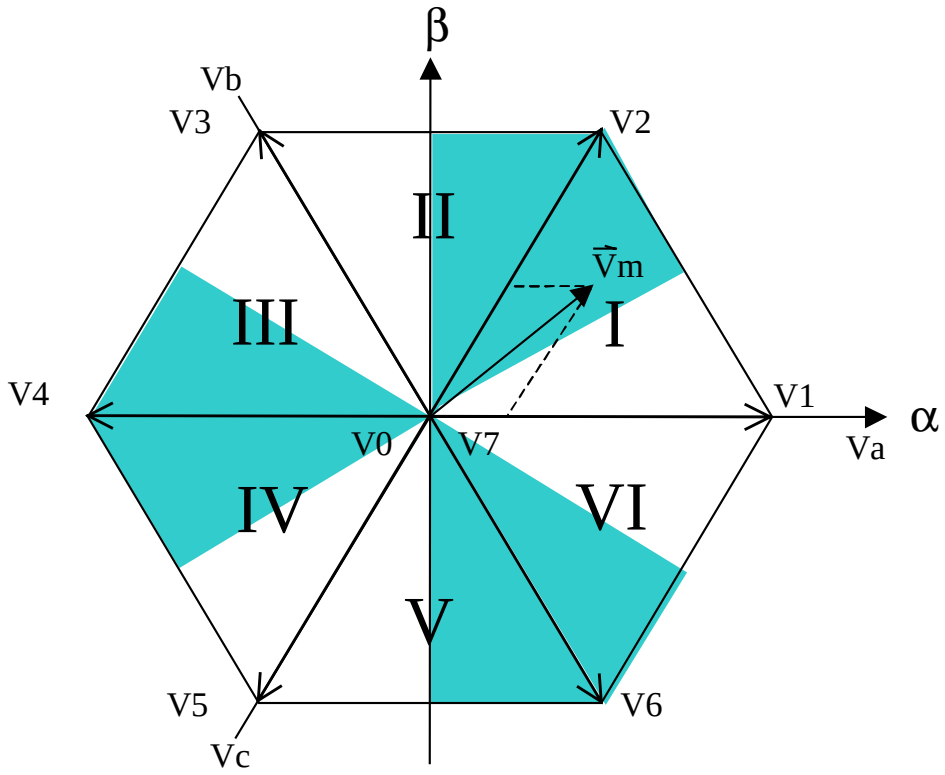


Figure 2.23 Illustration of simple implementation of 60°-clamping SVM scheme

The simulated phase current and corresponding gate signal waveforms are shown in Figure 2.24. The phase current does not switch when the phase current is the highest.

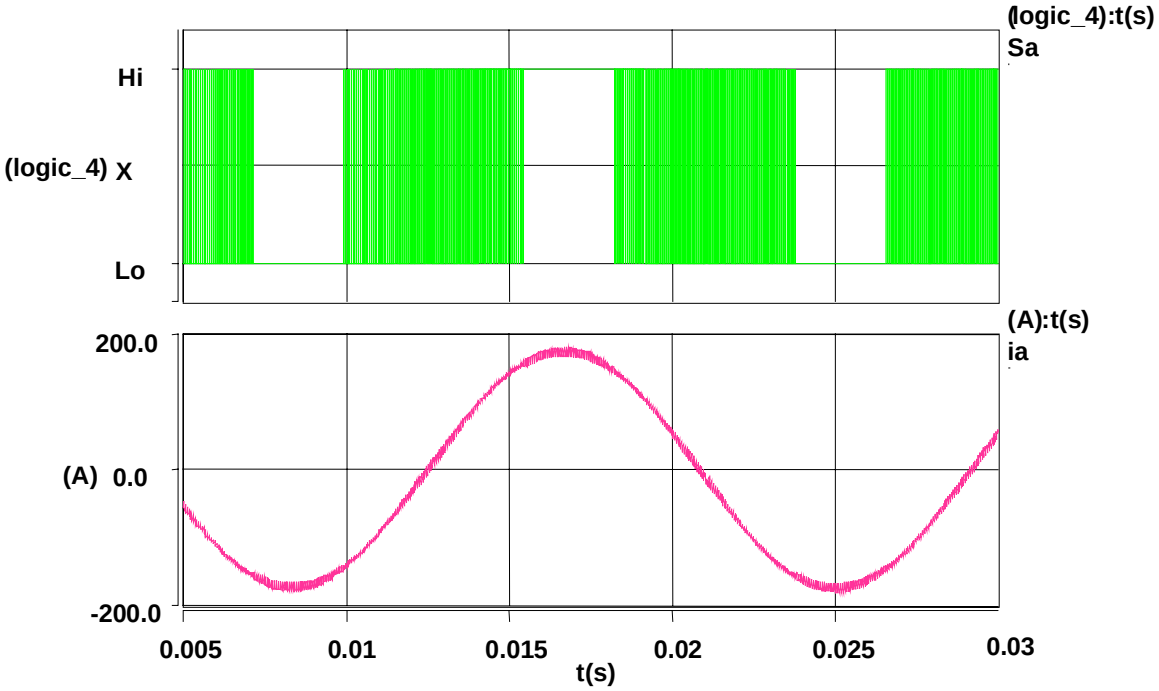


Figure 2.24 Simulated phase current and associated main switch gate signal

A general algorithm to assure the 60°-clamping scheme by comparing three-phase current is shown in Figure 2.25. As long as the phase shift between $\vec{V}_m$ and $\vec{i}_s$ does not exceed 30°, the highest phase current is guaranteed to not be switched. This algorithm can be directly applied to the PWM inverter applications.

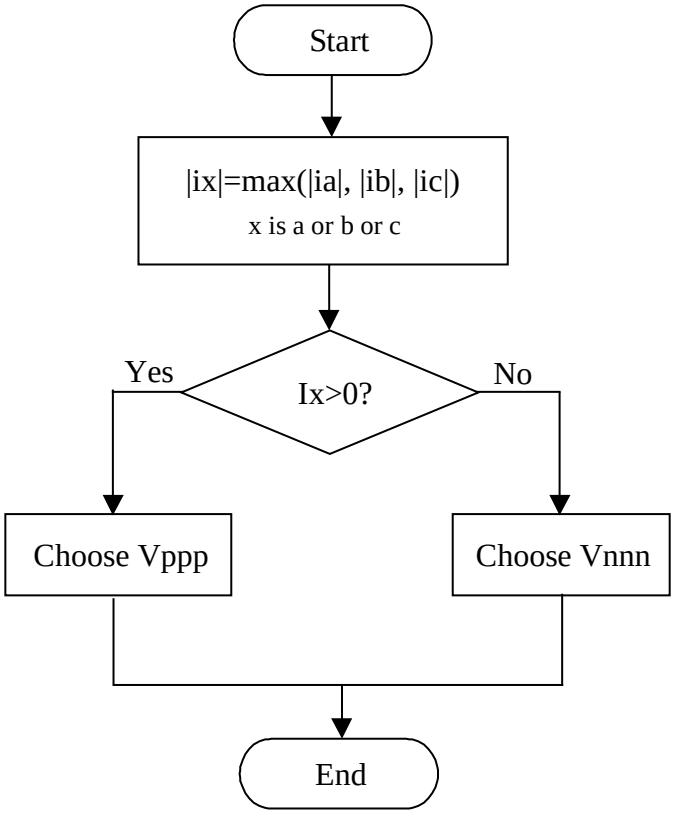


Figure 2.25 An algorithm to implement 60°-clamping SVM scheme

2.4.2 DSP Controller Implementation

All the control algorithms in the digital control block are performed by the DSP. The main program is used for initialization and start-up progress. The core of the DSP program is the periodical interrupt routine that fulfills sampling data control. The flowcharts of the DSP programs are shown in Figure 2.26. For the DC bus regulator, an important function is the line voltage synchronization.

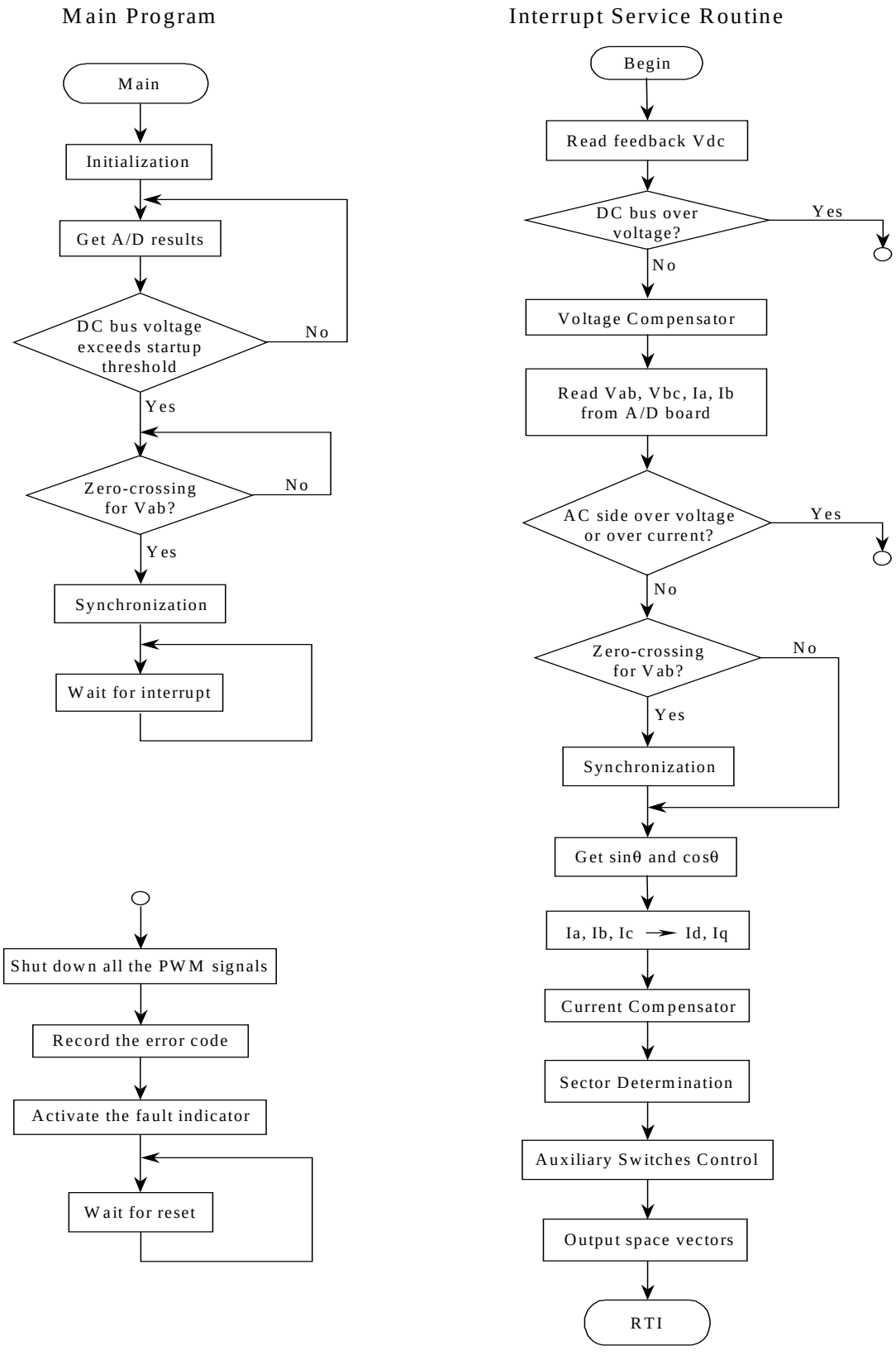


Figure 2.26 Flowcharts of the DSP program

2.4.3 EPLD Design

PWM space vector synthesis is implemented in the EPLD. The logic design for PWM signal generation is simplified, as shown in Figure 2.27. Using a timer, a comparator and a multiplexer, it is very clear and easy to synthesize any digitalized SVM scheme. Auxiliary switch signals are generated automatically based on main switch signals. This does not change the SVM synthesis. Thus, the soft-switching pulse generation circuit can be designed as a piggyback system, which is enabled and disabled according to the phase current direction.

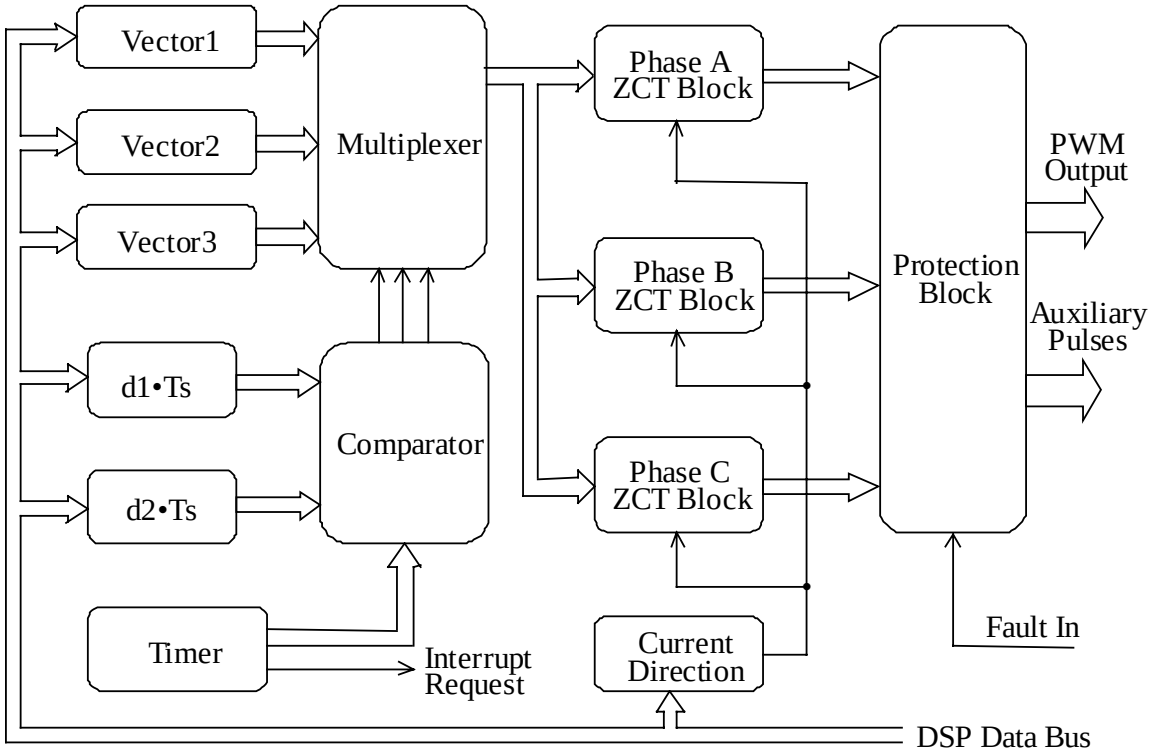


Figure 2.27 Block diagram of the EPLD design

To simplify the implementation of the SVM modulator, three vector registers and two duty cycle timers are used. Therefore, only the simple edge-aligned SVM scheme can be directly used, as shown in Figure 2.28.

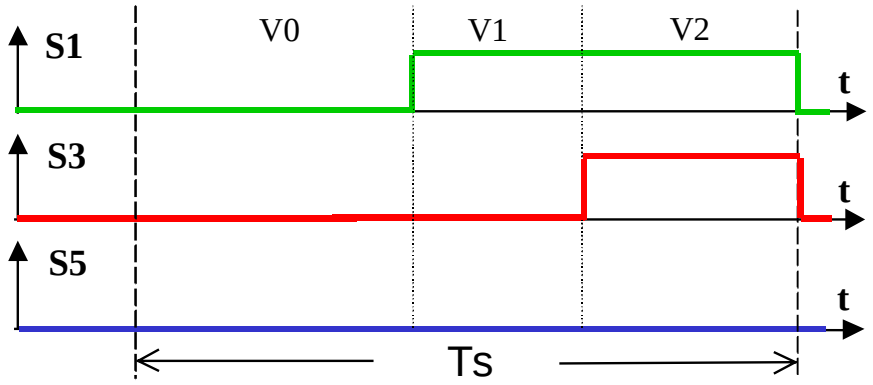


Figure 2.28 A simple edge-aligned SVM scheme

For this ZCT soft-switching scheme, auxiliary switch pulses are generated based on both edges of the corresponding main switch gate signal. The pulse width of the main switch gate signal should be larger than that of the auxiliary switch gate signal to avoid the interference between the turn-on and turn-off transitions. The pulse width of the auxiliary switch signals should be 3·To/4 to align the switching instant with the maximal resonant peak current (To=4μs). The minimal main switch pulse width should be no less than 6μs. It is necessary to either extend the narrow pulse to 6μs or just eliminate the narrow pulse. To minimize the distortion introduced by the inaccurate pulse width, the implementation extends any narrow pulse larger than 3μs to 6μs and eliminates any pulse smaller than 3μs. Both positive and negative parts of the PWM signals are adjusted. Duty cycle loss is inevitable in soft-switching implementation.

2.4.4 DSP Control Program for Valve Control

Plug and play (PnP) is a concept based on PEBB but takes a step further. Power electronics systems built with the PnP concept allow interchange among different PEBB modules, which means the PEBB modules can have different topologies (such as different soft-switching topologies) as long as the PEBB modules can fulfill the same functionality required by the system. Each PEBB module has standard hardware and software interface. A low-level controller is integrated into each PEBB module. This controller is called a hardware manager (HWM). The PnP concept is also applied to the control block of the converter. In other words, the control building blocks are also interchangeable. Every PnP controller is developed for a specific application, which is called an application manager. Therefore, a conventional converter is divided into two parts, one part is one or more PEBB modules with a HWM, and another part is the application manager. The control information is transferred between these separate parts by optical fibers. The wide bandwidth of the fiber optic cables enables the high-speed communication between the separate parts. The application managers can be controlled by a system-level controller via high-speed data link. A preliminary demonstration system that consists of two PnP controllers with the same PEBB module-based power stage is shown in Figure 2.29. One of the PnP controllers is for the DC distributed power systems, the other one is for the butterfly valve control. This feature also demonstrates the flexibility of the digital control block.

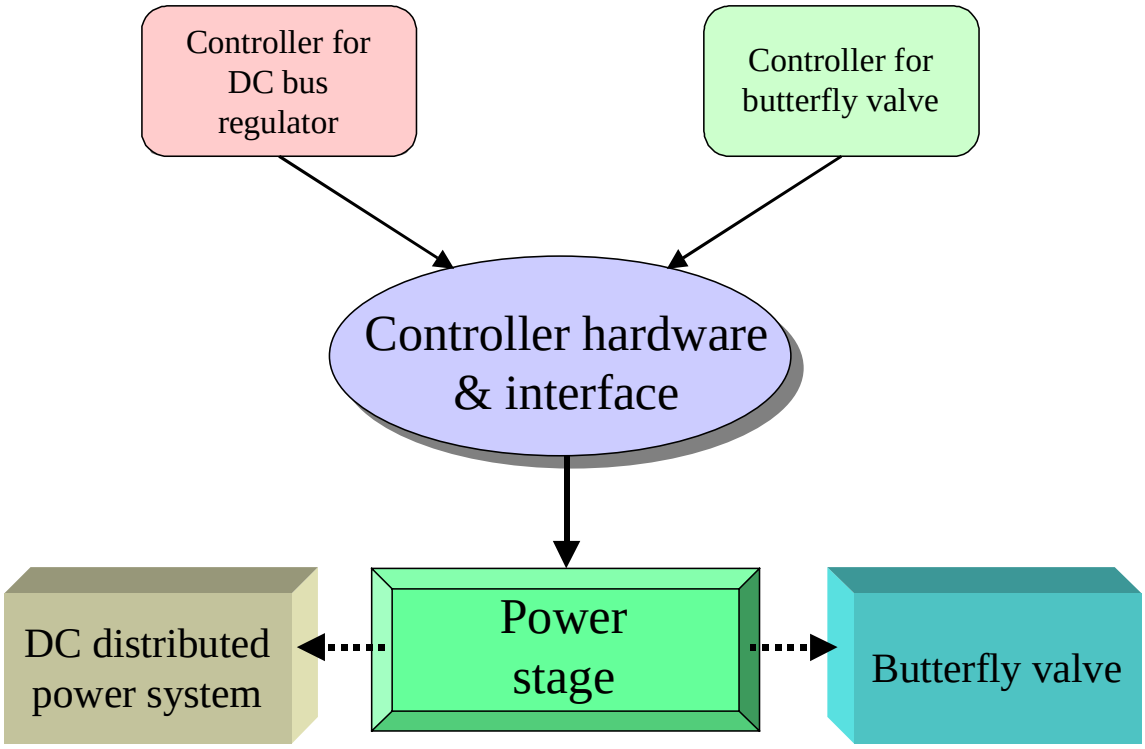


Figure 2.29. A plug and play demonstration system

With the PnP concept, a three-phase converter can be configured as a voltage source inverter for the valve control or as a bus regulator for a DC distributed power system. A DSP program for a butterfly valve (driven by a built-in induction motor) control is developed. For the butterfly valve, the information about the limit switches being open or closed is sensed by the digital control block. The digital controller controls the direction of rotation and the start-up/stop of the motor built in the valve. Soft-start and variable-speed operation of the butterfly valve is implemented to achieve better performance. The simplified main DSP routine for the butterfly valve control is shown in Figure 2.30.

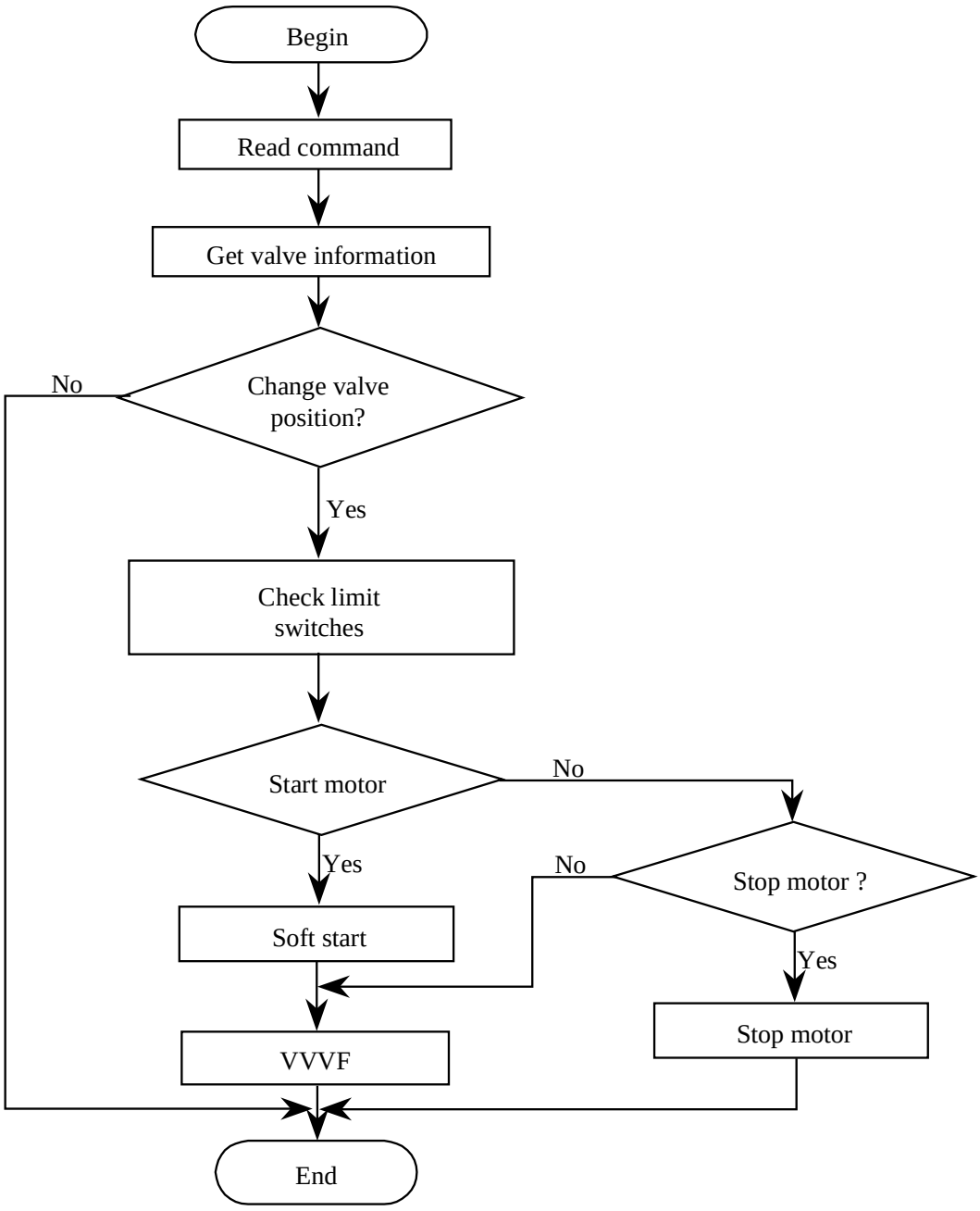


Figure 2.30. Flow chart of the DSP program for butterfly valve control

Chapter 3 System Design Issues and Solutions

3.1 Modeling and Control of the DC Bus Regulator

The simplified power stage of the DC bus regulator is shown in Figure 3.1. The first control objective of this PWM converter is to achieve three-phase sinusoidal input current in phase with the input phase voltage. In order to do that, the switching network (seen from the input side in Figure 3.1), should convert the DC bus voltage into three-phase sinusoidal (carried by PWM) voltages V_A, V_B and V_C, which are so called reflected DC bus voltage.

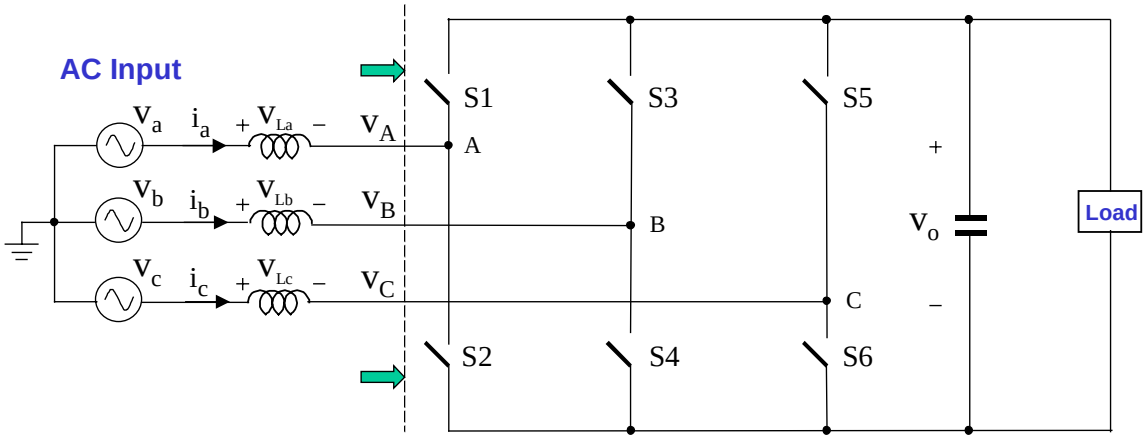
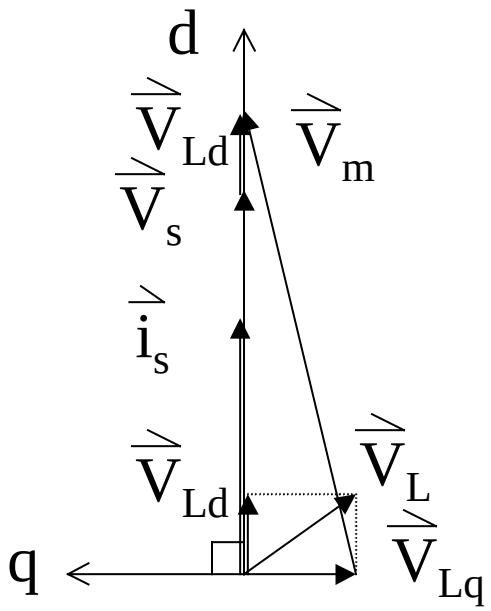


Figure 3.1 Simplified power stage of the DC bus regulator

Since three-phase variables can be regarded as a vector in the d-q coordinates, with rotating angular speed equal to the line frequency, the relationship of the input voltage, current and reflected DC bus voltage in the d-q coordinate is shown in Figure 3.2. The d-axis is aligned with the vector $\vec{V}_s$, which represents the three-phase input voltages. Three-phase input currents and inductor voltages are represented by $\vec{i}_s$ and $\vec{V}_L$ respectively. $\vec{V}_m$

is the reflected DC bus voltage. Obviously, the amplitude of $\vec{V}_m$ is larger than the amplitude of $\vec{V}_s$. That is why this type of PWM converter is called three-phase boost converter.



$V_d=V_s+V_{Ld}$,
$V_q=0$,
$V_{Lq}=\omega \cdot V_{Ld}$,
$i_d=i_s$,
$i_q=0$.

Figure 3.2 Vector diagram of the DC bus regulator

PWM converters behave in a nonlinear, discrete manner due to the switching operations. To simplify the control design, a large-signal average model is normally used to get around the discrete behaviors in the frequency range lower than half of the PWM switching frequency. Based on the average model, PWM converters can be linearized at the operating point by perturbing the control variables. The linearized outcome is the small signal model of the PWM converters. The loop transfer functions can be obtained and thus the feedback compensator can be designed by using the small signal model.

Since the adopted ZCT soft-switching technique is only used to help the transitions of the IGBT switches, it does not affect the control design of the bus regulator in the

average sense. The DC bus regulator operates according to the low-frequency average of the PWM control rather than the switching transition itself. As a result, the control design for this soft-switched DC bus regulator is exactly the same as its hard-switching counterpart.

The d-q average large signal model [3] for the DC bus regulator is shown in Figure 3.3. Vd and Vq are the projection of $\vec{V}_s$ on d and q axes; id and iq are the d and q components for $\vec{i}_s$. The product of Vo and dd is the projection of $\vec{V}_m$ on the d-axis, while $dq \cdot V_o$ is its component on the q-axis.

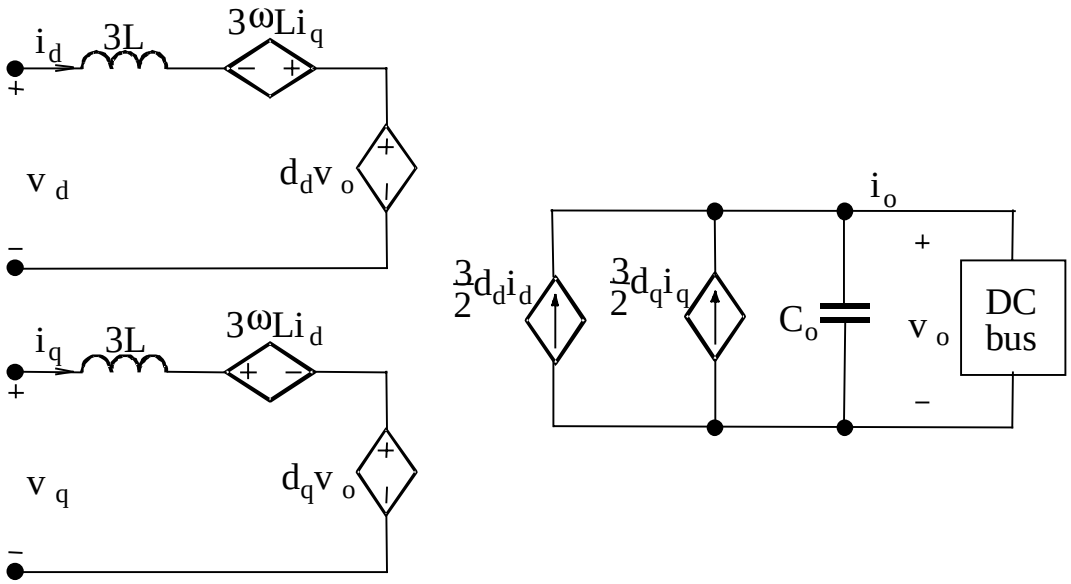


Figure 3.3 Average large signal model of PWM boost rectifier

Equations 2-6 and 2-7 show the average model of the DC bus regulator in the d-q coordinates:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{3L}\begin{bmatrix} V_d \\ 0 \end{bmatrix} - \frac{1}{3L}\begin{bmatrix} d_d \\ d_q \end{bmatrix} Vo + \omega \begin{bmatrix} i_q \\ i_d \end{bmatrix} \quad , \tag{2-6}$$

$$\frac{d}{dt} Vo = \frac{3}{2}\frac{1}{C}\begin{bmatrix} d_d & d_q \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} - \frac{1}{C} i_o \quad , \tag{2-7}$$

where i_o is the load current.

A two-loop cascade control scheme is used in implementing the controller. The inner loop is a current loop with wide bandwidth needed to achieve unity power factor. The outer loop is a voltage loop in order to tightly regulate the DC bus voltage. The control block diagram is shown in Figure 3.4. The reference value for i_q is zero if there is no input EMI filter. If there is an EMI filter at the AC-side of the bus regulator, i_q needs to be set to a nonzero value to counteract the introduced phase shift.

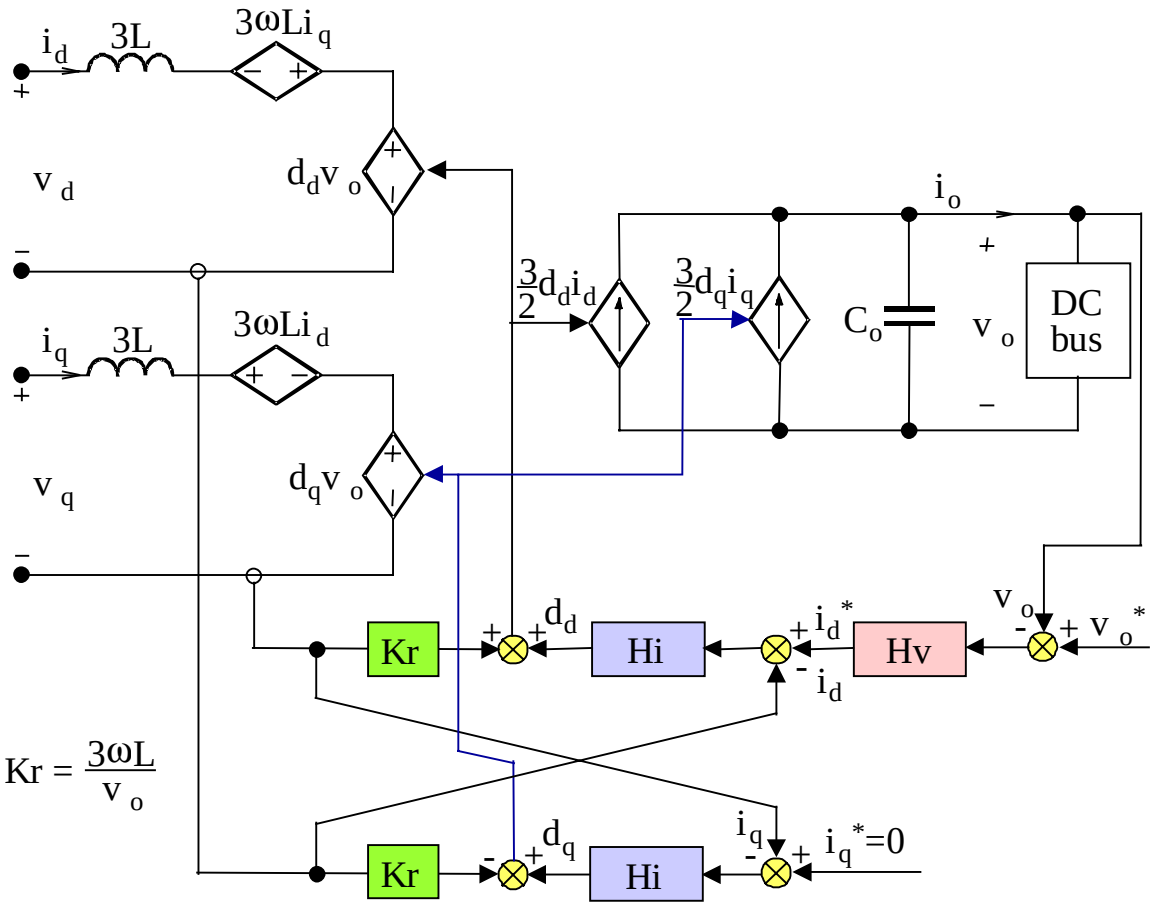


Figure 3.4 Control block diagram with PWM rectifier average model
(Kr: Decoupling coefficient; Hv: Voltage compensator; Hi: Current compensator)

The small-signal control-to-current transfer function id/dd and iq/dq for three different power levels are plotted in Figure 3.5 and Figure 3.6. In Figure 3.5, the Bode plots for different power levels are almost the same at the high-frequency region, while the low-frequency gain increases as the power level increases. The resonant peaking is also damped more for higher power due to the smaller load resistance. Since the current loop is normally closed at high-frequency region to achieve high performance, the current feedback loop design is based upon the loop transfer function at the full power load.

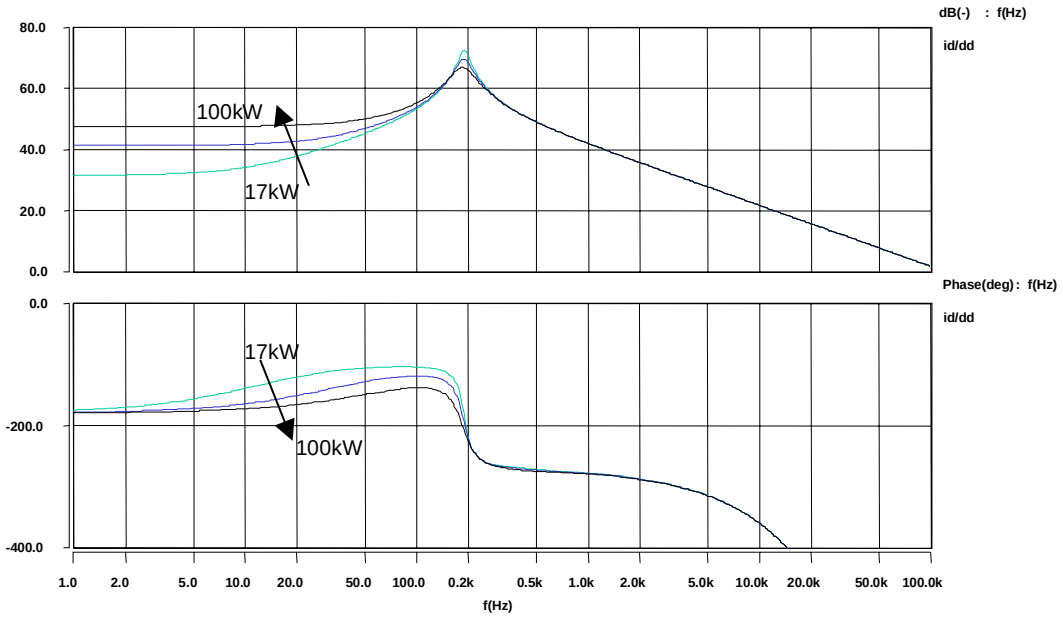


Figure 3.5 The d-channel control-to-current transfer function at different power levels (17kW, 50kW, 100kW)

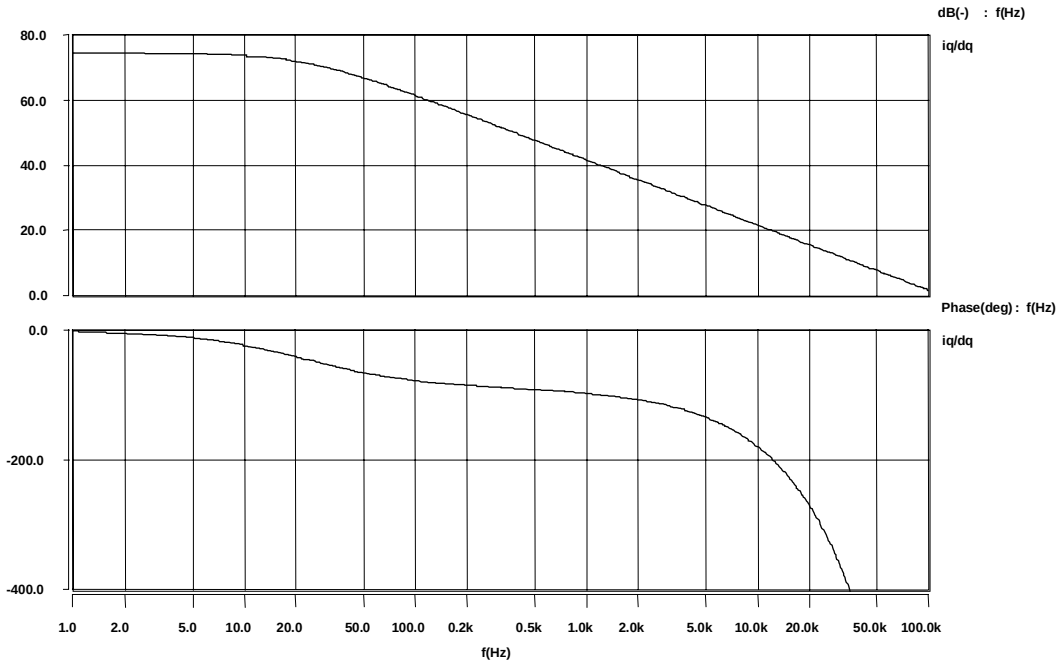


Figure 3.6 The q-channel control-to-current transfer function at different power levels (17kW, 50kW, 100kW)

The q-channel control-to-current transfer function is independent of the power level after the decoupling between d and q channels. This is because the q-channel is only related to the reactive power while the d-channel controls the active power. The q-channel has almost the same high-frequency characteristics as the d-channel. Therefore, the feedback control design based on the d-channel transfer function is used for both d and q channels.

A PI regulator is used as the current loop compensator. A pole is put at the zero frequency and a zero is put right before the resonant peak of the open-loop transfer function. By changing the gain of the PI regulator, the corner frequency can be adjusted. In this design, Kp=0.025 and Ki=24.75. The current loop gain for the d-channel is shown in Figure 3.7. The corner frequency is 3kHz. The phase margin is about 60°. Due to the digital delay, after 5kHz, the phase angle of the current loop drops quickly. Using the same feedback compensator for the q-channel as shown in Figure 3.8, the corner frequency is the same as that of the d-channel. The phase margin is also about 60°.

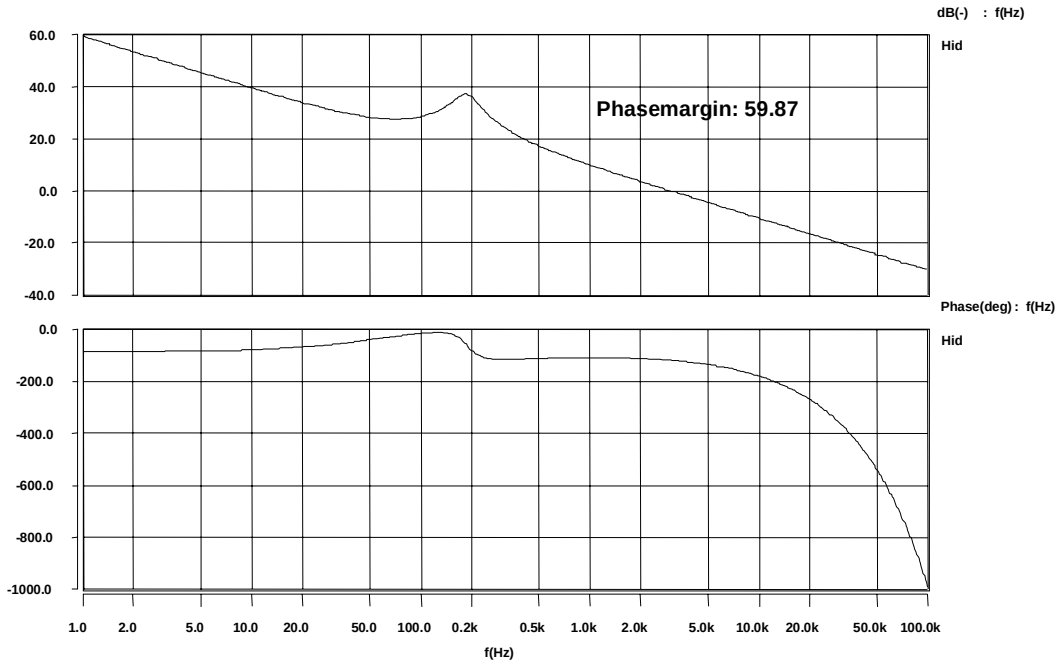


Figure 3.7 The d-channel current loop gain Hid at 100kW

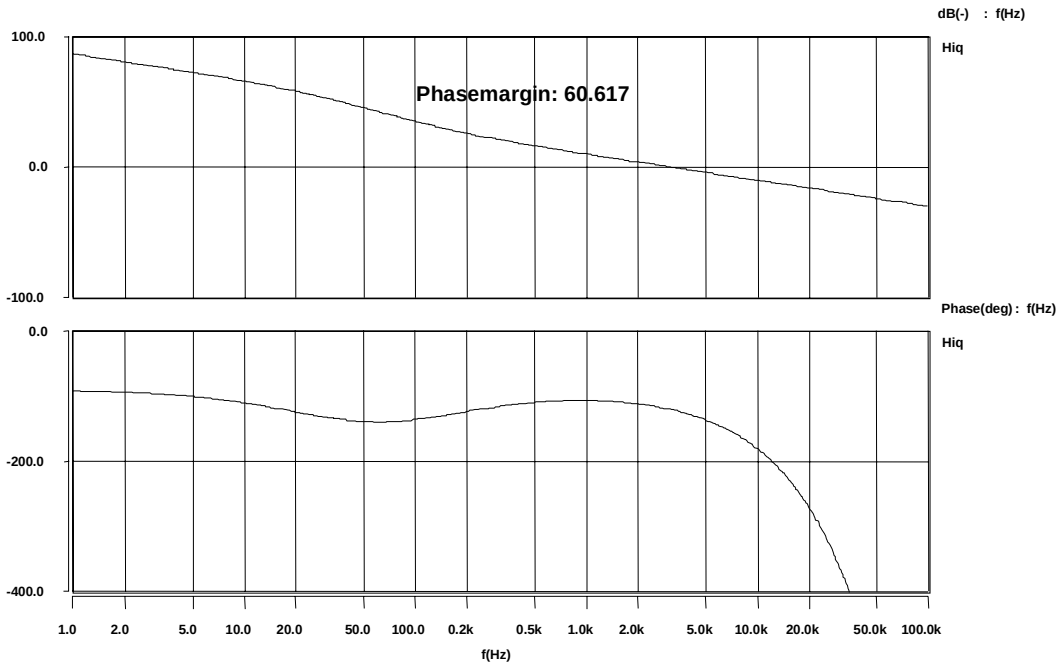


Figure 3.8 The q-channel current loop gain Hiq

In the average model of the DC bus regulator, the d-channel and q-channel currents are coupled. That is why a decoupling coefficient Kr is used in Figure 3.4. To compare the decoupling effects, the q-channel current-to-d channel current transfer function id/iq* and d channel current-to-q channel current transfer function iq/id* without decoupling are shown in Figure 3.9. The same transfer functions with decoupling are shown in Figure 3.10. Apparently, the coupling between the d-channel and q-channel currents is greatly attenuated, up to the corner frequency with decoupling coefficient. The attenuation at low frequency is more than 100dB.

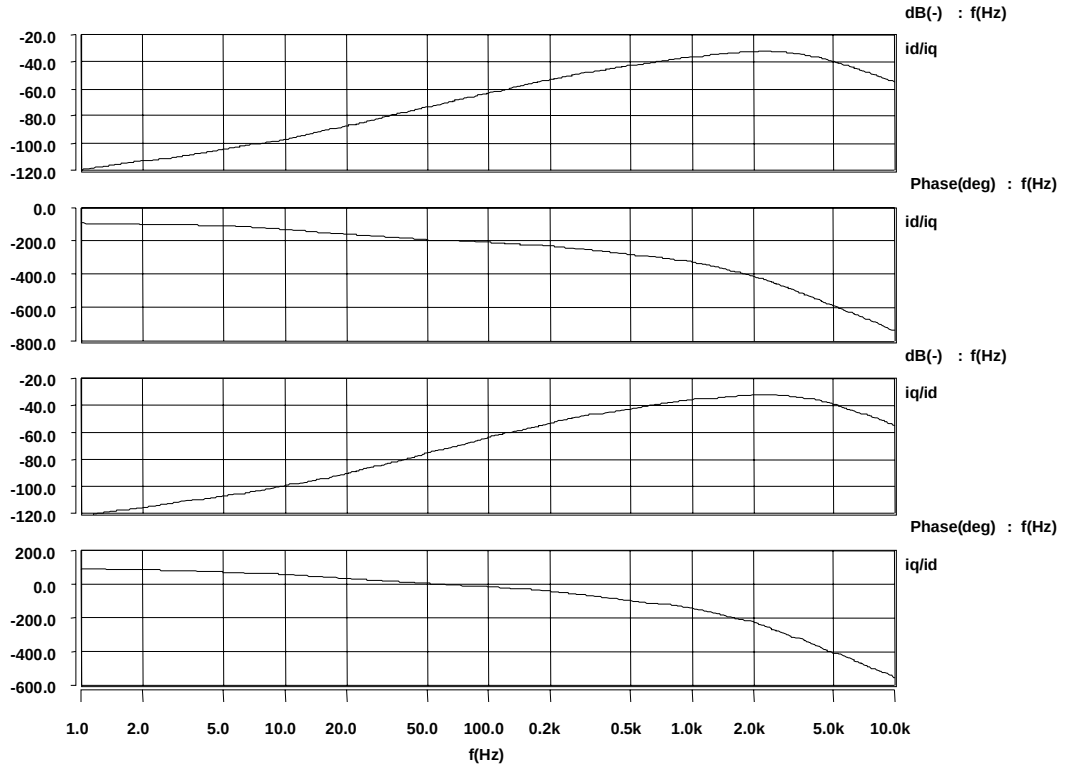


Figure 3.9 Transfer functions id/iq* and iq/id* without decoupling

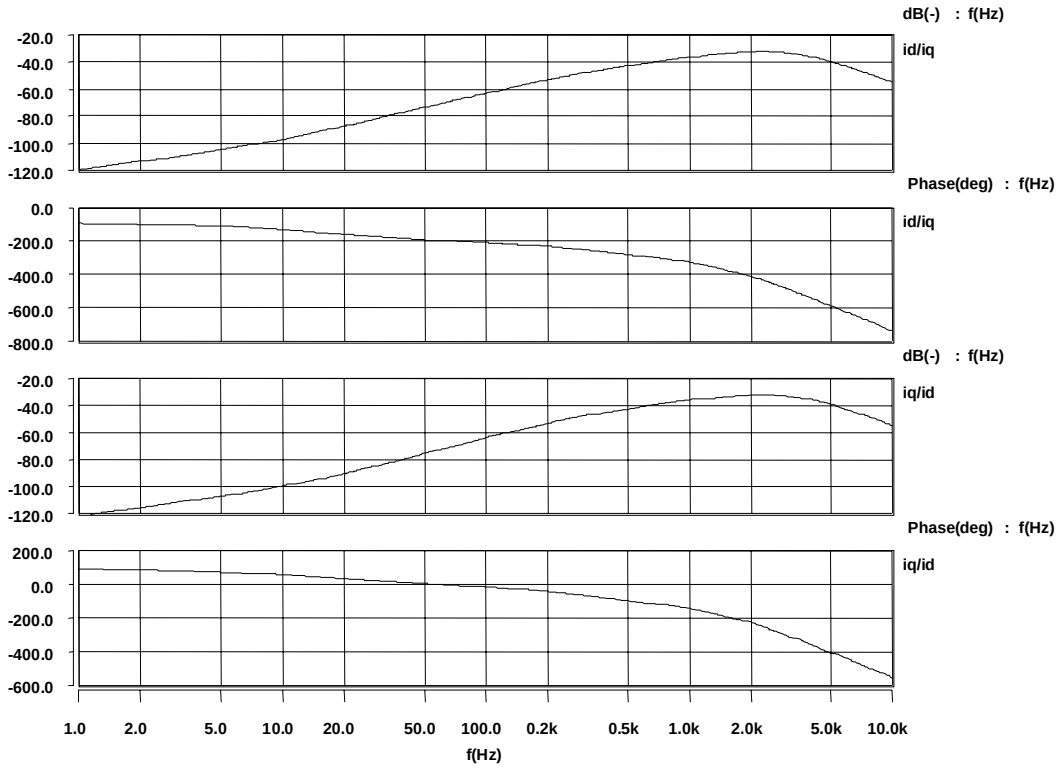


Figure 3.10 Transfer functions id/iq* and iq/id* with decoupling

The voltage compensator design is based on the plant with the current loop closed. The d-channel current reference-to-output voltage transfer function at different power levels is shown in Figure 3.11. From the Bode plots, the open-loop voltage transfer function at different power levels has a crossover point near 300Hz, which means both gain and phase are the same for this particular frequency. Below this frequency, the low-frequency gain is lower for higher power level, while beyond this frequency the phase shift is larger. Due to the linearity of the small-signal model, superposition can be applied to the compensator design, which means the closed-loop transfer function will also have the lowest low-frequency gain as well as the least phase margin under the highest power. Therefore, the 100kW power scenario is used to design the feedback voltage loop. Again

a PI regulator is used: Ki=500 and Kp=1.59. The voltage loop gain is shown in Figure 3.12. The corner frequency is 500Hz and the phase margin is about 59°.

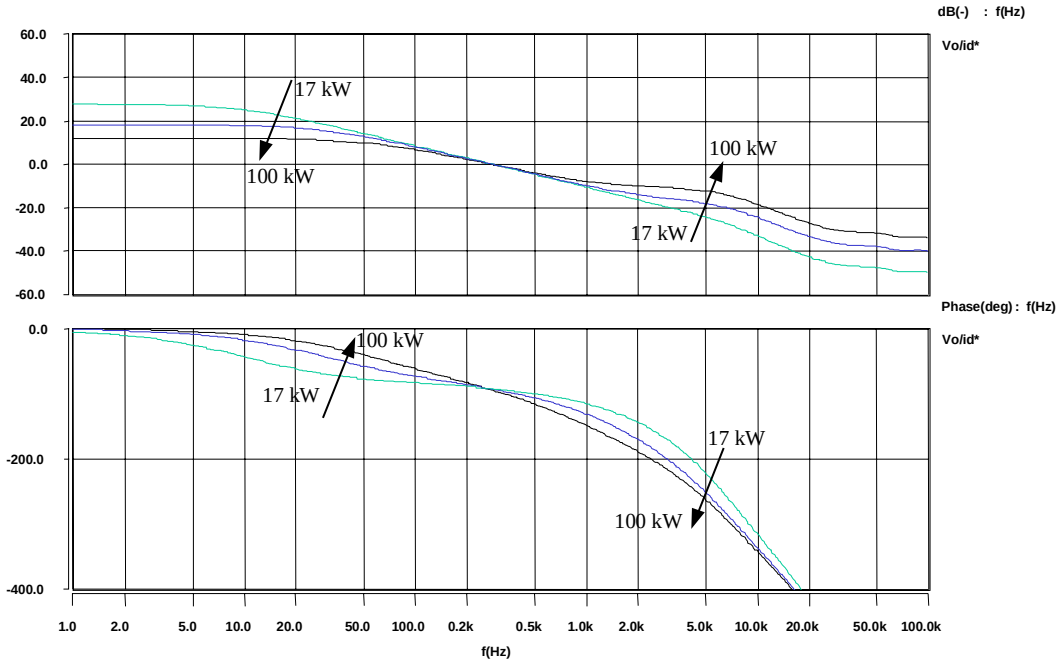


Figure 3.11 Open loop DC bus voltage transfer function

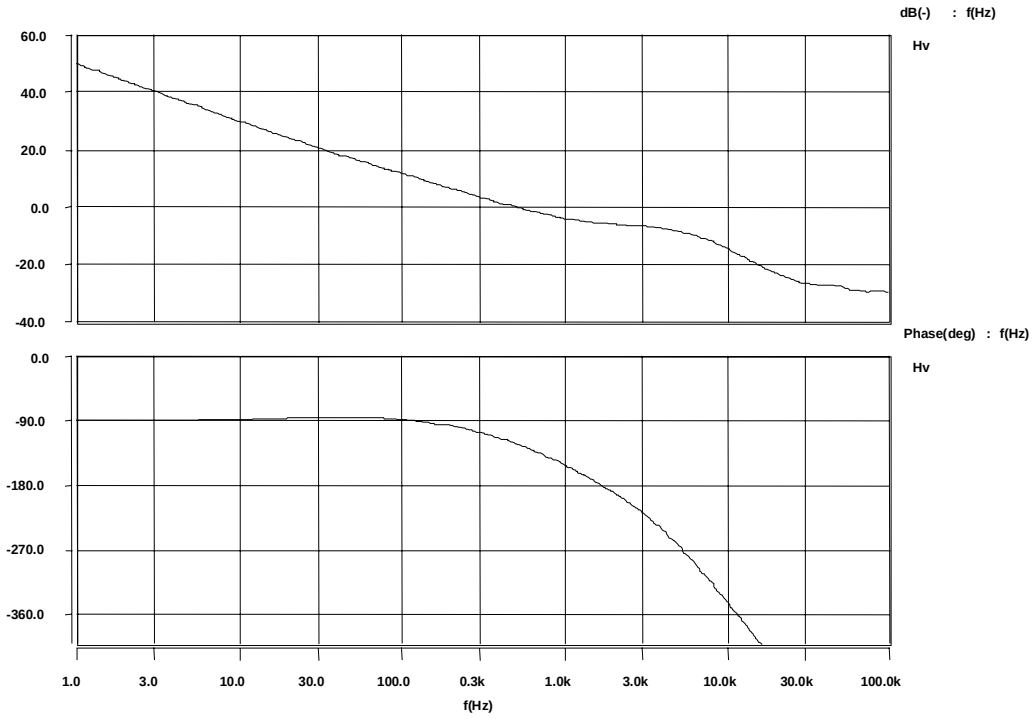


Figure 3.12 Voltage loop gain at 100kW

Small-signal output impedance of the bus regulator for different power levels is plotted in Figure 3.13. The output impedance is very important for this front-end power supply because it determines the system-level interactions between the bus regulator and various loads connected to the distributed DC bus. The favorable output impedance of the source converter is as low as possible to avoid the possible interactions. Figure 3.13 shows that the output impedance is relative high and flat at the medium-frequency range, especially under full power load.

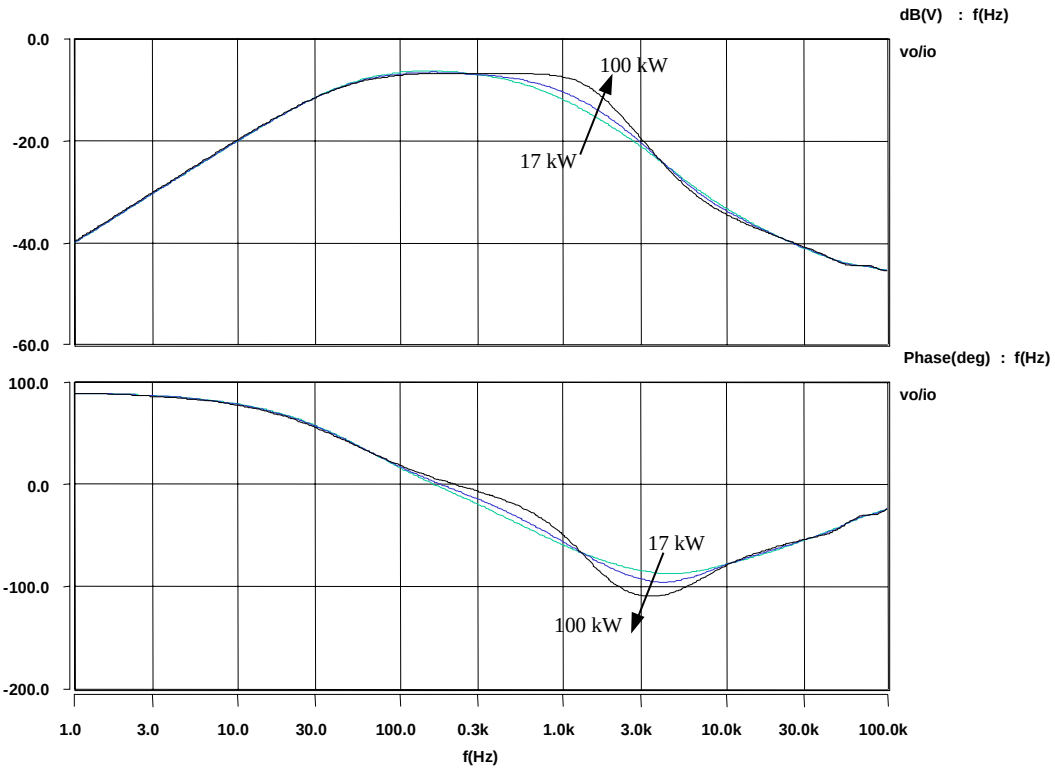


Figure 3.13 Small-signal output impedance of the DC bus regulator at different power levels (17kW, 50kW and 100kW)

The step-load change is an important approach verifying the converter's (large-signal) stability as well as dynamic performance. Figure 3.14 and Figure 3.15 show how the DC bus regulator reacts to the step-load change. Vo is the DC bus voltage, and ia, ib

and ic are the three phase currents. The response time is about 10ms. Voltage overshoot is about 30V. The phase current transitions are smooth.

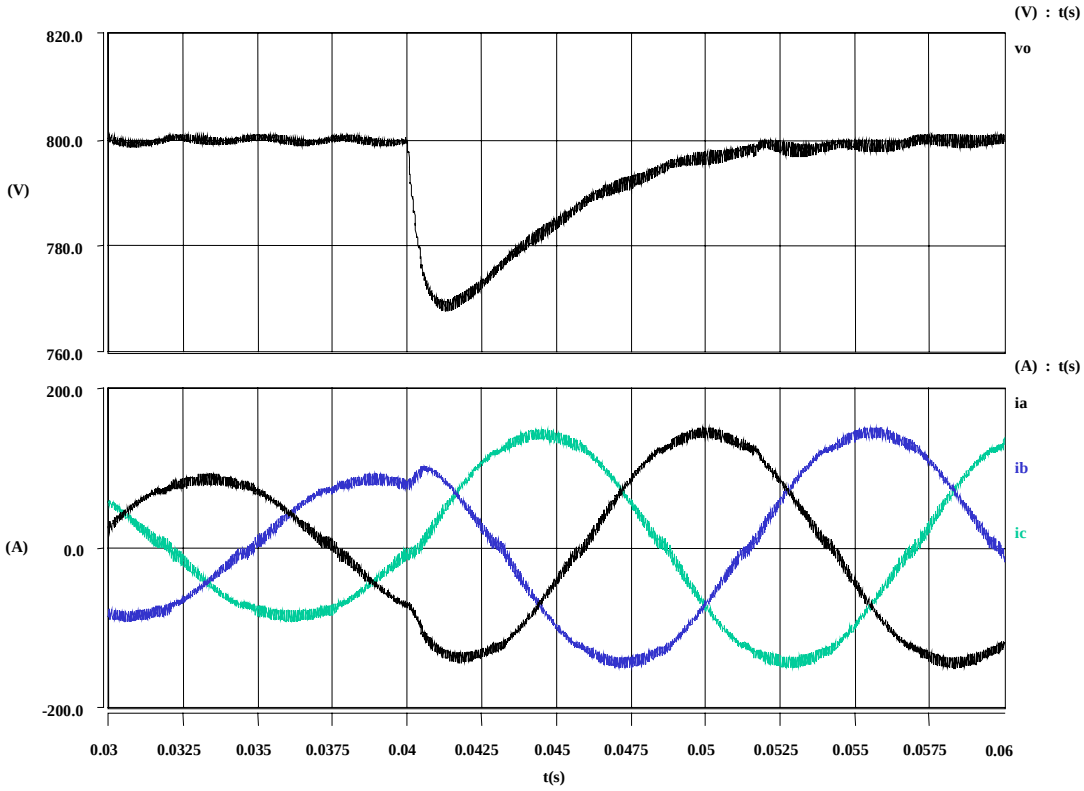


Figure 3.14 Simulated step-load change from 50kW to 83kW

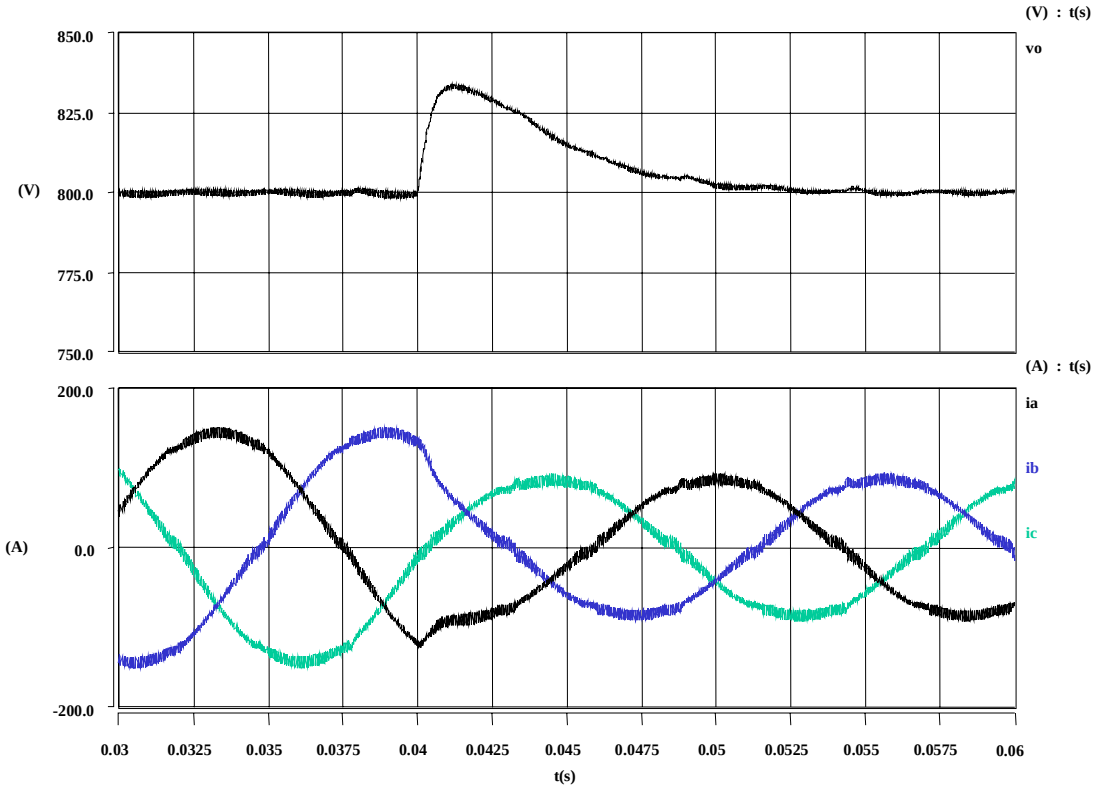


Figure 3.15 Simulated step-load change from 83kW to 50kW

3.2 ZCT Soft-Switching Technique in Three-Phase PWM Converters: Control Issue and Its Solution

Although the operation principle of each ZCT PEBB module in the DC bus regulator is the same as that in a DC-DC PWM converter, there is one distinctive trait in the DC bus regulator: the operation of the two main IGBT switches in the same phase leg is complementary. There is only a short period of dead time between the turn-on gate signals of the two IGBT switches. If the auxiliary IGBT switch gate signal is applied only based on the gate signal of the main IGBT switch (as is done in a DC-DC converter), then shoot-through occurs in the auxiliary switch leg. This is because the dead time is much less than the pulse width of the auxiliary switch gate signals, as shown in Figure 3.16. The shaded areas are the overlaps between the top and the bottom auxiliary IGBT switch gate signals. Shoot-through occurs in the auxiliary switch leg during this period of time.

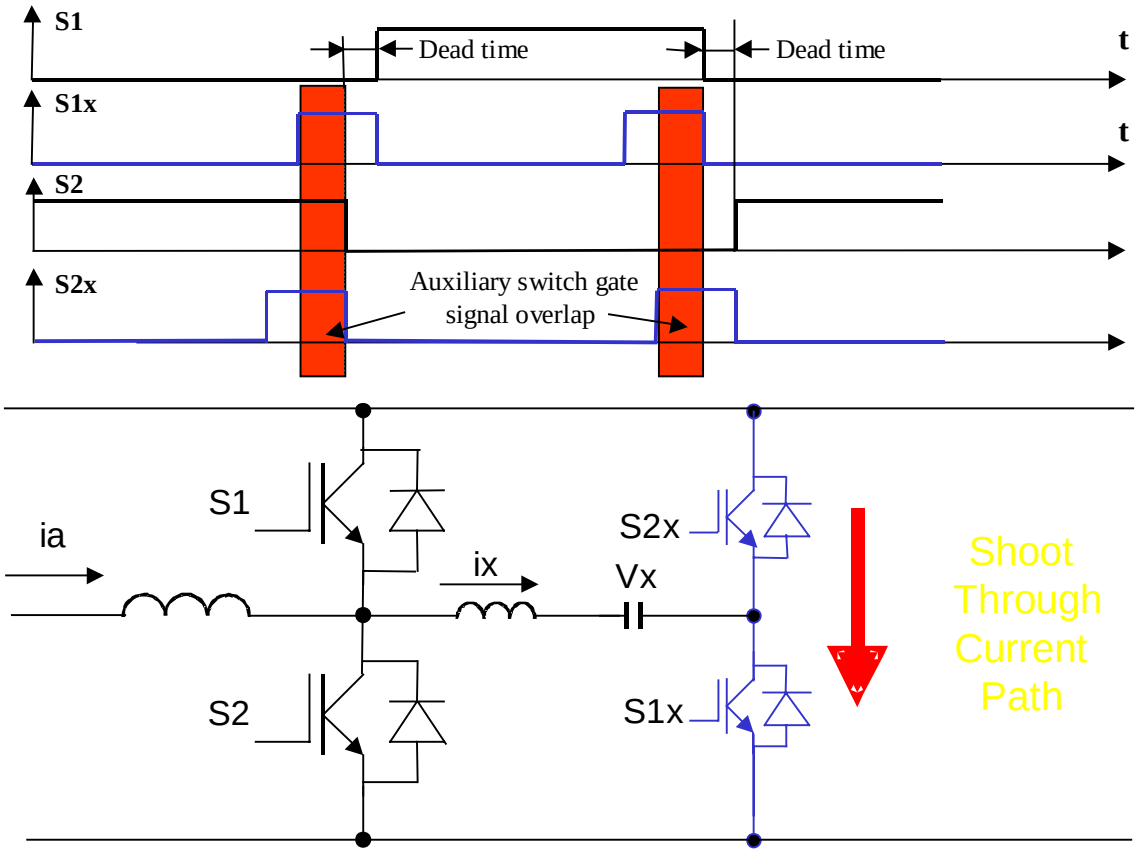


Figure 3.16 Shoot-through in the auxiliary switch leg

If we greatly increase the period of dead time in order to avoid shoot-through, the initial condition of the resonant tank will be disturbed. Simulation results illustrating this consequence are given in Figure 3.17. Compared with normal operation, conduction loss increases due to the extra conduction and resonance of the auxiliary circuit. Another disadvantage of increasing the dead time is the waveform distortion of the input current, which will be discussed in the next section.

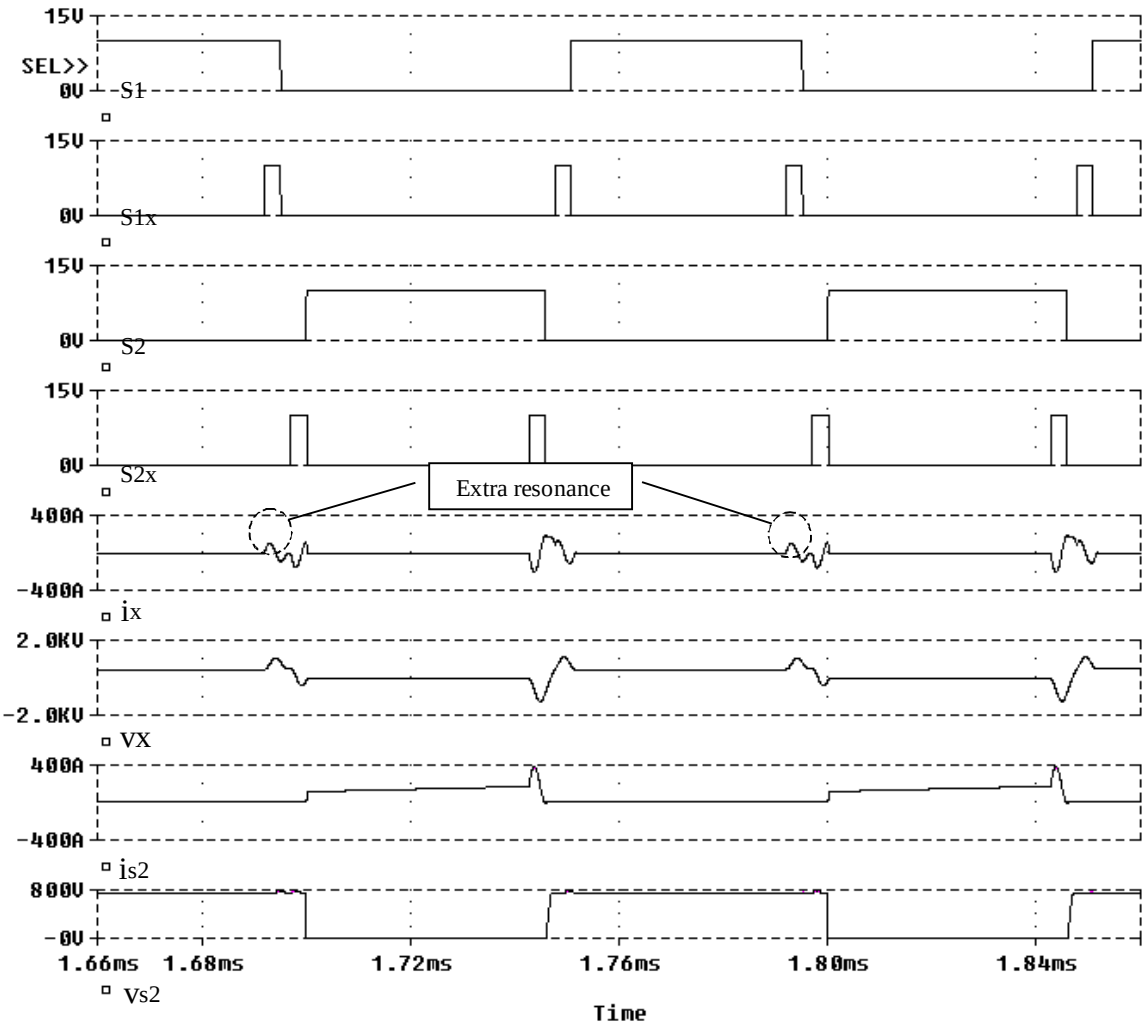


Figure 3.17 Simulation results with extending dead time

The solution is to enable the gate signals of either the auxiliary switch that is associated with the main switch or the anti-parallel diode that is carrying current. This can be done by detecting the direction of each phase current, as shown in Figure 3.18. In this DC bus regulator, the phase current information is required by the current feedback control. Thus, the phase current direction information is used to enable and disable the auxiliary switch signal to assure the correct operation without adding any extra hardware. Additionally, the phase current amplitude information can be used to enable and disable

soft-switching operation in order to optimize the total efficiency of the converter. This is meaningful for three-phase operation due to the time-varying input current and voltage. Since the ZCT soft-switching technique does not offer many benefits when the phase current is small, it is disabled under this circumstance.

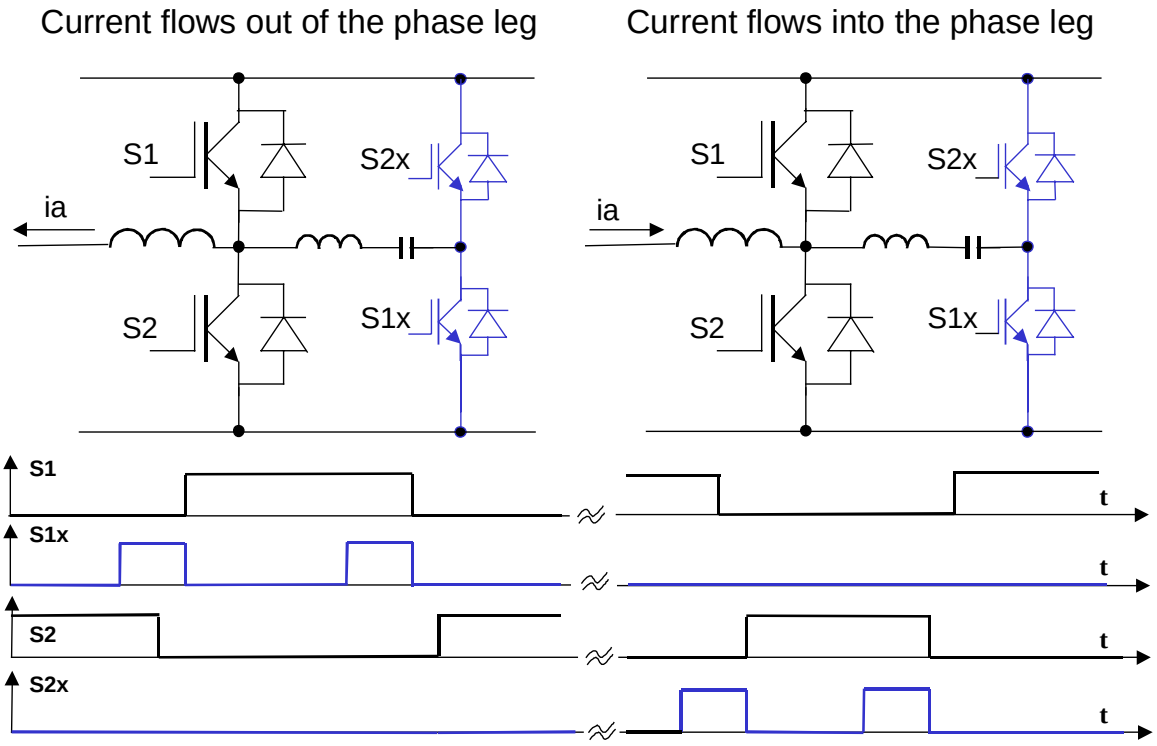


Figure 3.18 Control timing for a ZCT PEBB module in the DC bus regulator

3.3 Low-Frequency Harmonics and Their Elimination

Although the operation of the AC-side commutated soft-switching technique adopted in this DC bus regulator should have a negligible effect on the operation in terms of low frequency, significant low-frequency harmonics are observed in both test and simulation results. Figure 3.19 shows the simulated input phase current of this DC bus regulator with an ideal balanced three-phase AC power source and an ideal resistive load.

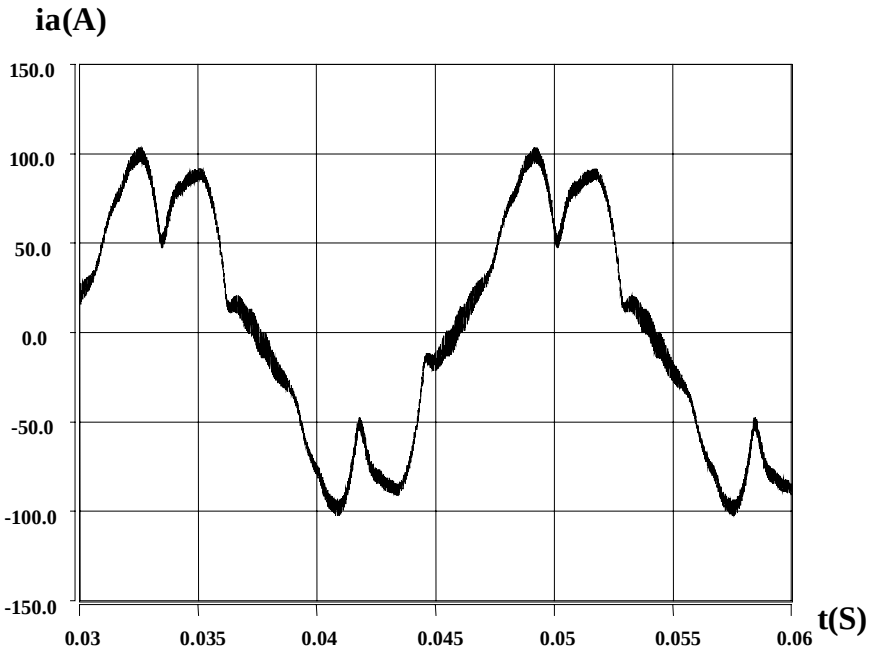


Figure 3.19. Phase A input current waveform of the soft-switched bus regulator

The harmonic spectrum of the input phase current is shown in Figure 3.20. The low-order harmonics are comparable to the fundamental frequency component. The THD, mainly low-frequency harmonics, is about 21.4%. Low-frequency harmonics generated by the bus regulator appear at the DC output side in the form of low-frequency DC voltage ripples, as shown in Figure 3.21.

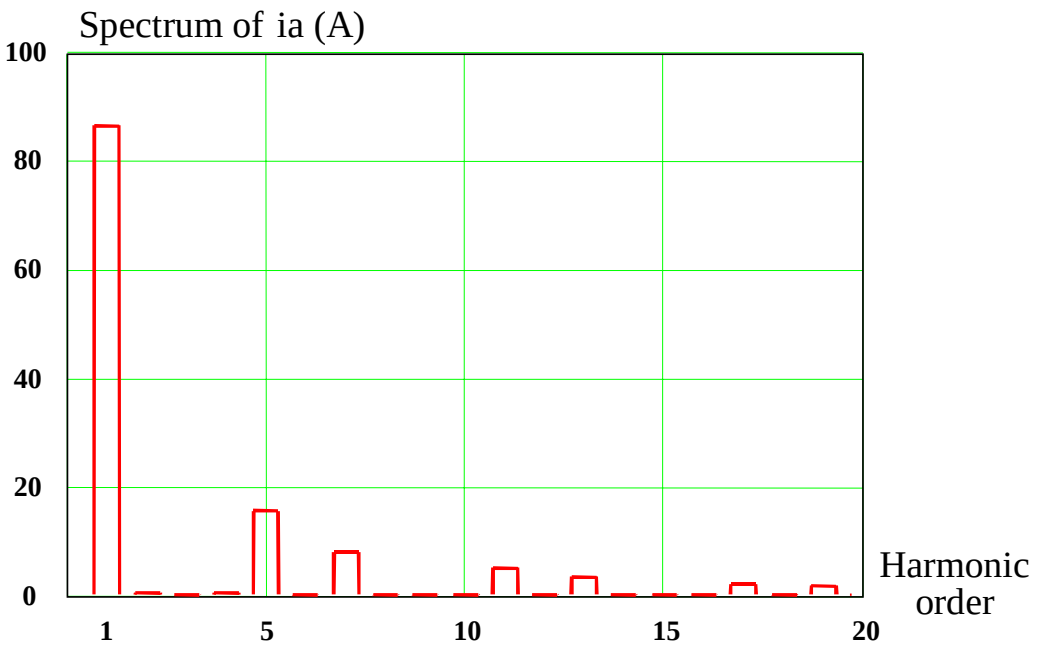


Figure 3.20. Spectrum of the phase A input current

The issue of low-frequency harmonics is very important in power conversion and power quality areas. Apart from their harmful effects on the AC source (such as generator sets or utility power systems), strong low-frequency harmonics can limit the control bandwidth of the bus regulator such that the bus regulator cannot tightly regulate the DC bus. On the other hand, low-frequency DC voltage ripple may cause oscillation of the whole DC distributed power system. Besides, low-frequency harmonics are more difficult to mitigate than high-frequency ones. In order to filter out the low-frequency harmonics, bulky low-pass filters have to be added at both input and output sides of the bus regulator. As a result, the volume and cost of the DC bus regulator will increase significantly. Therefore, it is extremely important to investigate how these low-frequency harmonics are generated and find practical ways to remove them.

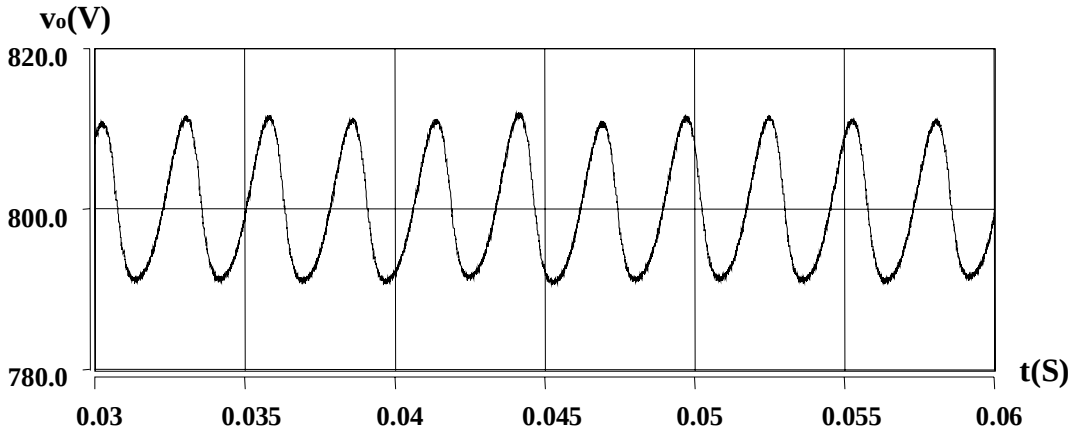


Figure 3.21. DC voltage ripple at the bus regulator output

Three major causes have been identified for low-frequency harmonics: pulse width limits, an improper SVM scheme and dead time. The first cause is only related to soft-switching techniques, while the other two causes may also exist in three-phase hard-switching PWM converters. These causes will be illustrated in the following sections. Solutions and correction techniques are provided accordingly to achieve clean AC input current.

3.3.1 Pulse Width Limits in Soft-Switched PWM Converters

Pulse width limits have to be set for soft-switched PWM converters. Soft-switching techniques utilize high-frequency resonance to achieve favorable switching transitions for power switches and/or diodes in PWM converters. The whole resonant process is normally much longer than the switching transition itself. In order to avoid malfunction of the resonant tank (due to the overlap between consecutive resonant cycles), pulse width limits must be set for the main switch gate signals.

In this soft-switched bus regulator, the same resonant tank operates twice for every switching cycle. As illustrated in Figure 3.22, the pulse width T_w of the main switch gate signals has to be limited by Equation 3-1.

$$T_{lmt} \le T_w \le T_s - T_{lmt}\,, \tag{3-1}$$

where T_s is the switching period, and the minimal pulse width limit $T_{lmt} = \max(t_1 + t_4, t_2 + t_3)$.

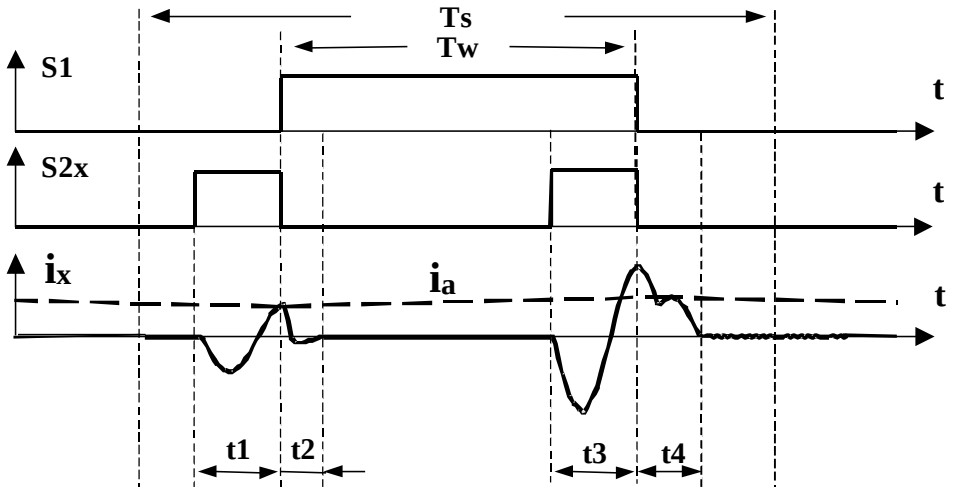


Figure 3.22. ZCT soft-switching operation waveforms.

Equation 3-1 is not applied when the duty cycle equals 0 or 1 because the soft-switching operation is not activated under these circumstances. In this DC bus regulator, the switching frequency is 20kHz. To obtain satisfactory soft-switching operation, the resonant period is about 4μs. The minimal pulse width limit T_{lmt} for the main switch gate signals is 6μs, and the maximal pulse width limit is 44μs. Therefore, the effective switch duty cycle ranges from 12% to 88%. In this bus regulator, the switch duty cycle is the same as the phase duty cycle. The term phase duty cycle will be used in the following discussion.

The impact of the phase duty cycle loss on the steady-state operation of three-phase PWM converters is not as straightforward as on their DC-DC counterparts. First, the duty cycle for each phase in a three-phase PWM converter changes in a line cycle. Second, the phase duty cycle depends on modulation strategies even under the same operating point (same modulation index). Here, a method of choosing zero and non-zero vectors is called a modulation strategy. An SVM scheme refers to a modulation strategy with a determined output vector sequence. To investigate the impact of the duty cycle loss on the PWM rectifier, the modulation index is computed for the given operating point using:

$$M = \sqrt{\tfrac{3}{2}} \cdot V_{ll\_rms} / V_o , \qquad (3\text{-}2)$$

where V_o is the DC bus voltage, and V_{ll_rms} is the RMS value of the input line-to-line voltage.

For this bus regulator, the modulation index at the operating point is 0.734 from Equation 3-2 with 480V line-to-line input and 800V output. For the sake of simplification, a conventional modulation strategy with the two zero vectors applied evenly will be analyzed as an example. The phase duty cycle d_a for this modulation strategy is shown in Figure 3.23. The pulse width limits, in the form of the phase duty cycle, are indicated by the dashed line $D_{\max}$ and $D_{\min}$ in Figure 3.23. The areas beyond the two dashed lines are where the phase duty cycle command is limited. Even if we only use one SVM scheme, which has the least high-frequency harmonics due to the symmetrical arrangement of the vectors [13-15], the duty cycle limits still lead to the heavily distorted input current waveform, as shown in Figure 3.19. The maximal modulation index M (maximum without causing distortion for this modulation strategy) is given by

$$M \le \sqrt{3}/2 \cdot (1 - 2 \cdot T_{lmt}) . \quad (3\text{-}3)$$

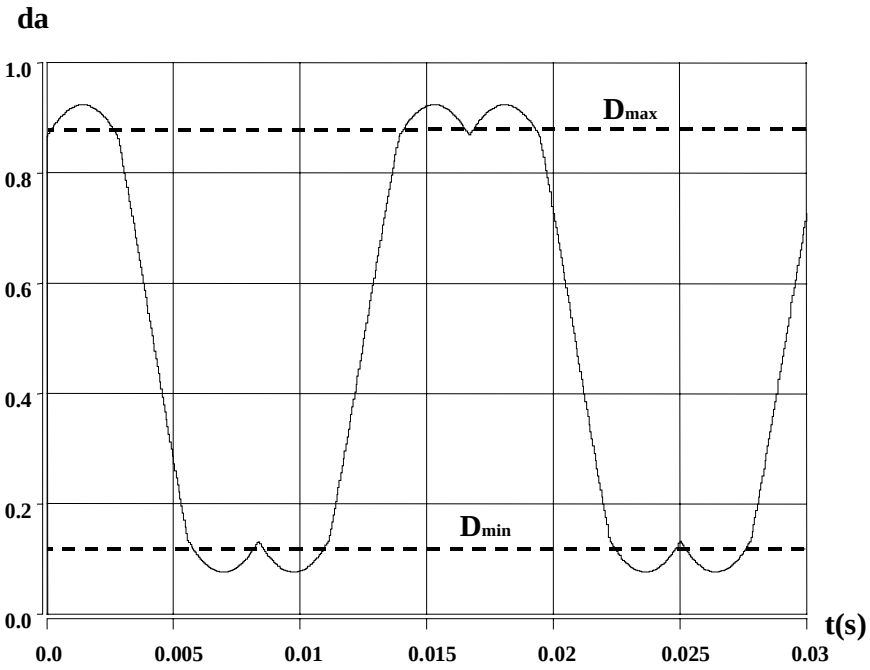


Figure 3.23. Continuous phase duty cycle pattern

From Equation 3-3, the maximum M not affected by the pulse width limits is 0.658. This means the command phase duty cycle is affected by the pulse width limits under the given operating point. To compare, the continuous phase duty cycle pattern with low modulation index (M=0.5) is shown in Figure 3.24. It is evident that the pulse width limits do not affect the phase duty cycle for M=0.5. Therefore, this modulation strategy is only suitable for the soft-switched PWM converters with low or medium modulation index.

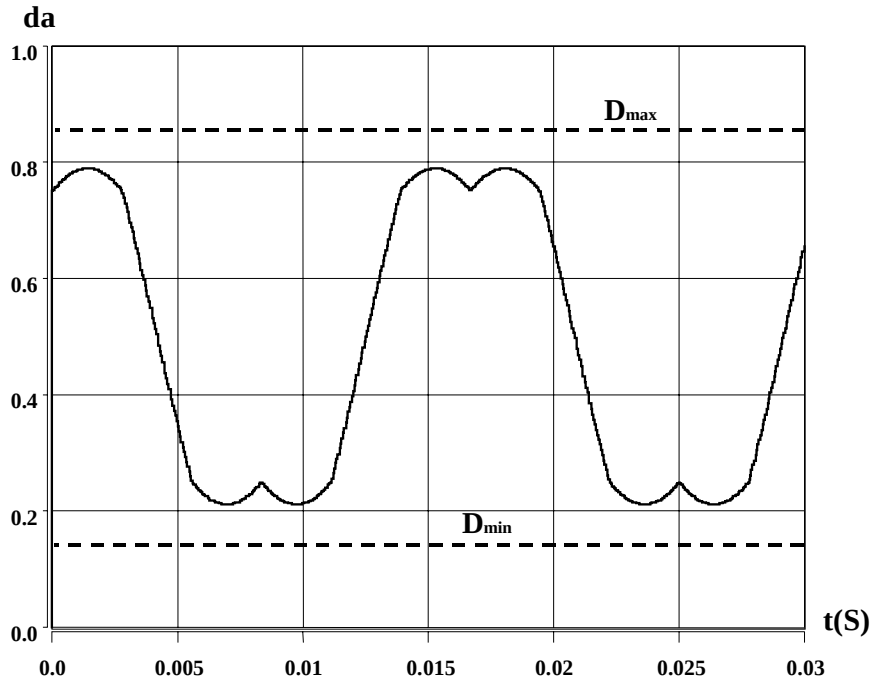


Figure 3.24 Continuous phase duty cycle pattern with low modulation index M=0.5

For this DC bus regulator, the modulation index is high (M=0.734). It is necessary to find a modulation strategy suitable for high modulation index applications.

The proposed solution utilizes the freedom of selecting zero vectors to shape the phase duty cycle pattern. By properly choosing zero vectors, the phase duty cycle pattern for the same operating point is changed to that is shown in Figure 3.25. Here, all the vertical lines perpendicular to the dashed lines are the discontinuous parts of the new duty cycle pattern. It is evident that this discontinuous modulation strategy avoids the pulse width limits in the DC bus regulator. This discontinuous modulation strategy turns out to be the 60°-clamping SVM that can reduce the switching loss by 50% under the unity power factor [16], as mentioned in Chapter 2. The modulation index range (without any distortion for this modulation strategy) is determined by

$$\sqrt{3} \cdot T_{lmt} / T_s \le M \le \sqrt{3} / 2 \cdot (1 - T_{lmt} / T_s) . \quad (3\text{-}4)$$

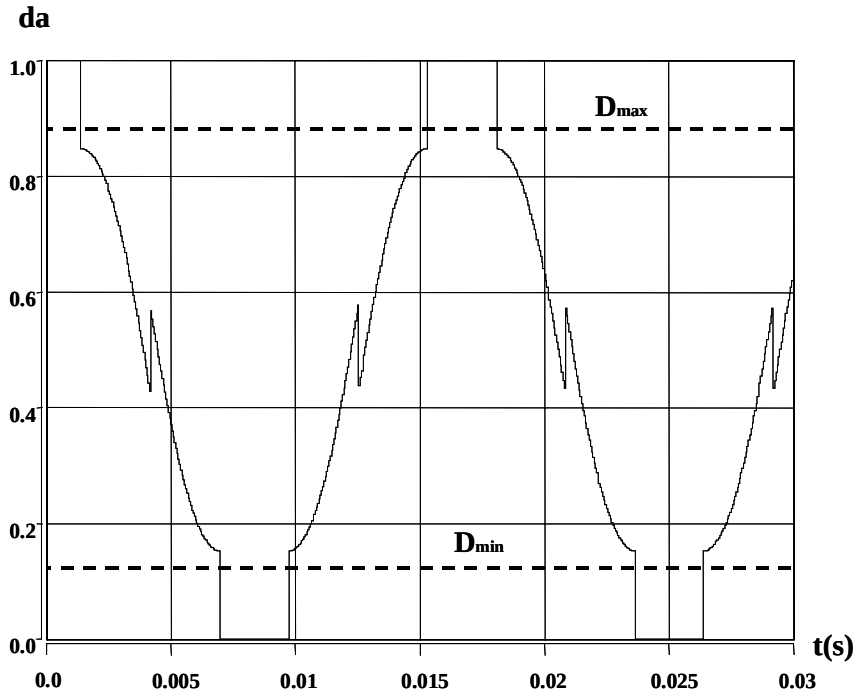


Figure 3.25. Discontinuous phase duty cycle pattern

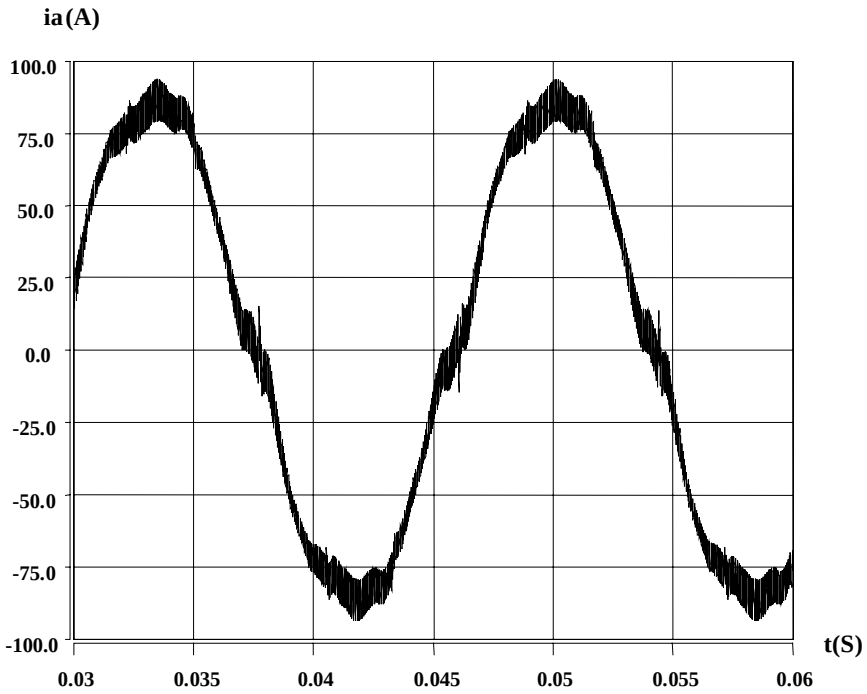


Figure 3.26. Simulated phase A input current without the effect of pulse width limits

Equation 3-4 gives M_{min}= 0.207 and M_{max}= 0.762. Therefore, the modulation index at the specified operating point is not affected by the pulse width limits. As shown in Figure 3.26, the input phase current waveform is significantly improved by the discontinuous modulation strategy. The distortion left in the input current waveform of Figure 3.26 is due to improper SVM scheme and dead time.

Figure 3.27 shows the discontinuous phase duty cycle pattern with low modulation index *M*=0.5. Obviously, a very low modulation index will be affected by the pulse width limits. Therefore, this modulation strategy is suitable only for the soft-switched PWM converters with medium and high modulation indices.

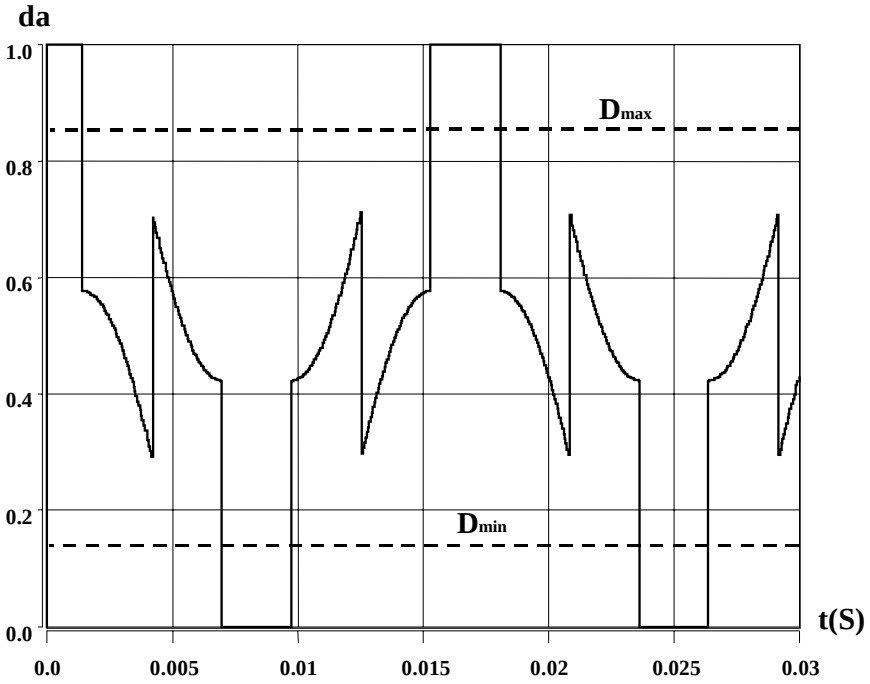
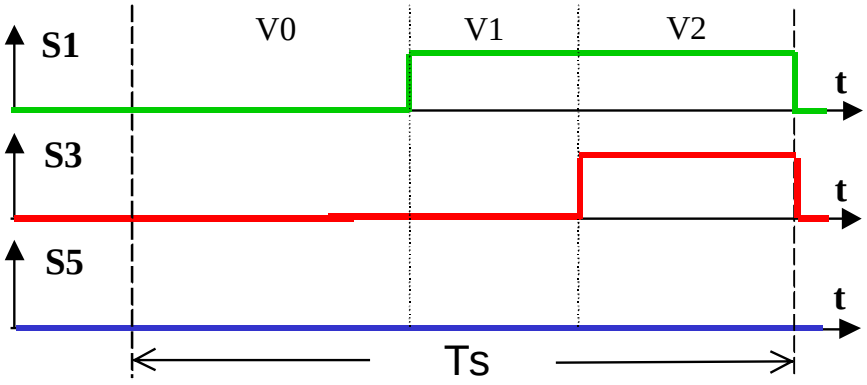


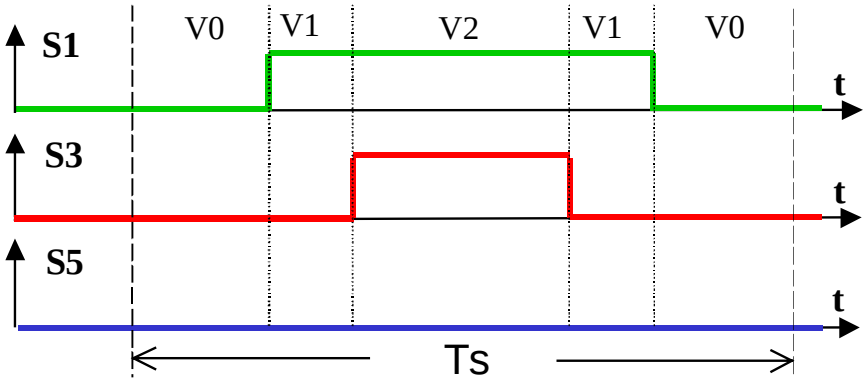
Figure 3.27 Discontinuous phase duty cycle pattern with low modulation index *M*=0.5

3.3.2 An Improper Space Vector Modulation Scheme and its Correction

An improper SVM scheme is identified as another cause of low-frequency harmonics in the DC bus regulator. SVM is a prevailing technique in controlling three-phase PWM converters. There are numerous SVM schemes, which can be classified as either symmetrical or asymmetrical. An asymmetrical scheme is shown in Figure 3.28a. V1 and V2 are the two non-zero vectors selected to synthesize the reference vector. V0 is one of the two zero vectors. A symmetrical scheme is shown in Figure 3.28b. As described in the literature [13-15], different SVM schemes can have different high-frequency harmonics. The asymmetrical schemes are easy to implement but have more high-frequency harmonics. High-frequency harmonics are relatively easy to mitigate by adding a small EMI filter, while low-frequency harmonics are much more difficult to suppress.



(a)



(b)

Figure 3.28. SVM scheme examples: (a) an asymmetrical scheme; and (b) a symmetrical scheme

Nevertheless, it is found in this research that an improper SVM scheme can cause pronounced low-frequency harmonics. The improper SVM scheme is shown in Figure 3.29. V0 and V7 are the two zero vectors available in a three-phase PWM converter. In order not to switch the phase with the highest current, the two zero vectors are applied alternatively. The sequence of the vectors is arranged in such a way as to minimize switching loss. However, the low-frequency harmonics still occur, as shown in Figure 3.30.

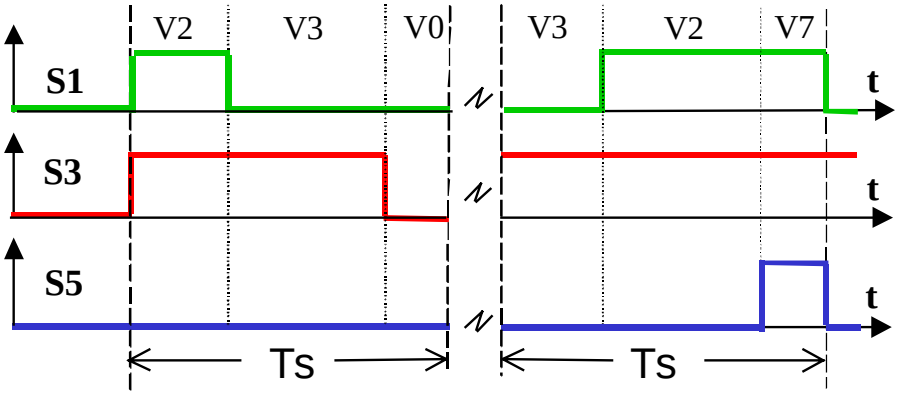


Figure 3.29. An improper SVM scheme

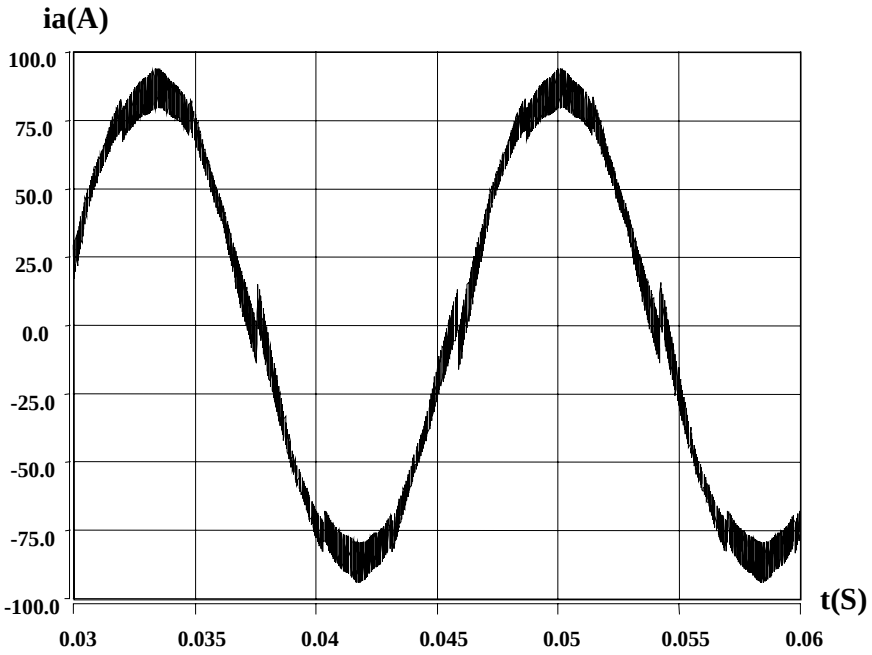


Figure 3.30. Distorted input phase current due to improper SVM scheme

The reason for the low-frequency harmonics can be illustrated by the extended view of the phase current waveform at the zero crossing where the distortion occurs, as shown in Figure 3.31. The sequence of the nonzero vectors changes at the zero crossing to

minimize the switching events. This change leads the average phase current of a switching cycle to shift by the magnitude of the input inductor current ripple.

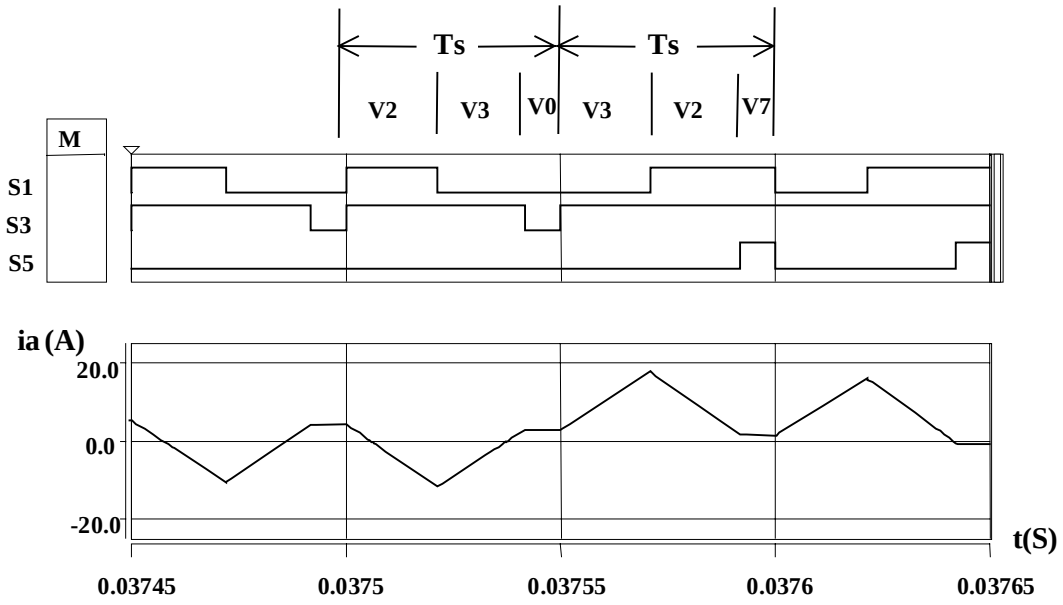


Figure 3.31. Detail of phase current at zero-crossing and associated main switch gate signals

The solution is to rearrange the sequence of the vectors, as shown in Figure 3.32. This scheme is referred to as a quasi-symmetrical 60°-clamping SVM. In every two consecutive switching cycles, the sequence of the vectors flips. Each PEBB module has only one switching cycle in every two sampling cycles.

The detail of the phase current waveform at the zero crossing with the corrected scheme is shown in Figure 3.33. Since the average current in every switching cycle is roughly equal to zero, smooth transition is achieved at the zero crossing points. After this problem is solved, the input current waveform is changed to the one in Figure 3.34. The remaining distortion is due to dead time.

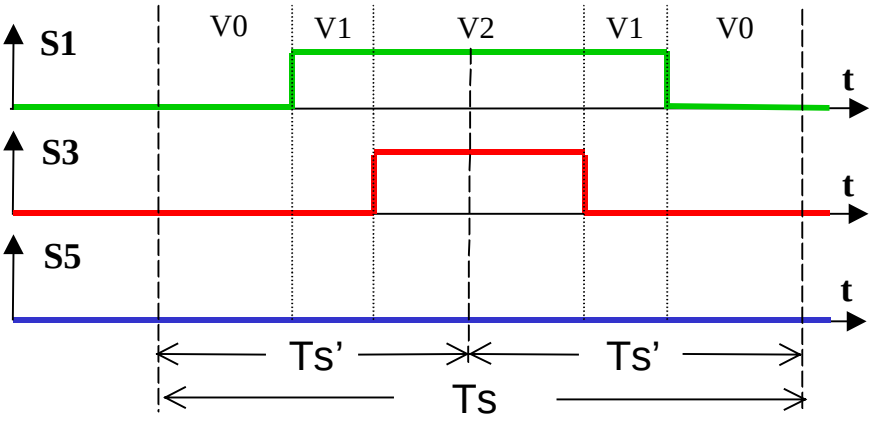


Figure 3.32 Quasi-symmetrical 60°-clamped SVM

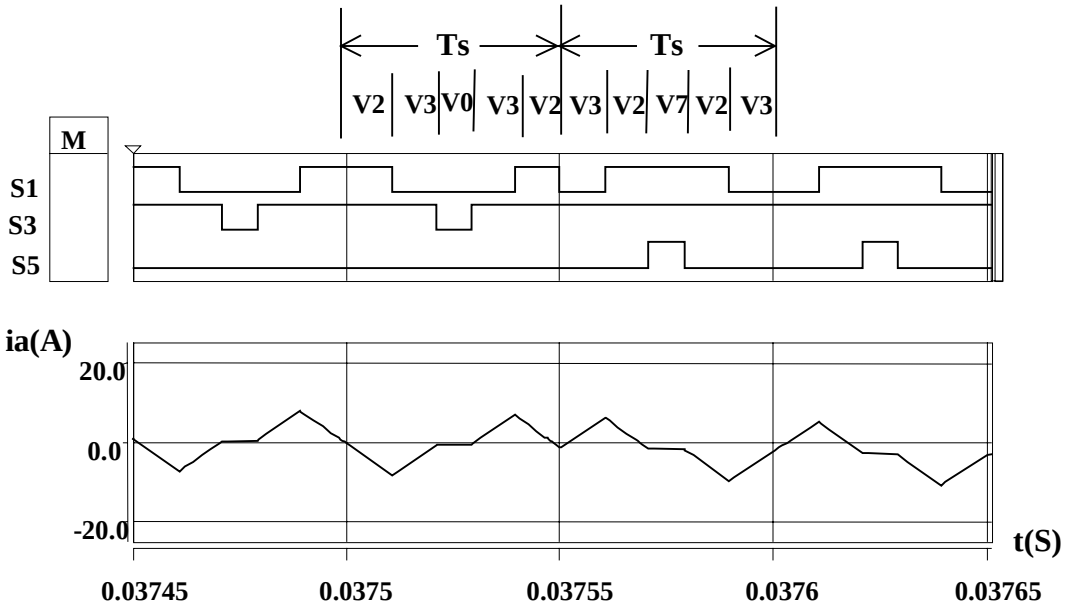


Figure 3.33. Corrected input phase current at the zero-crossing

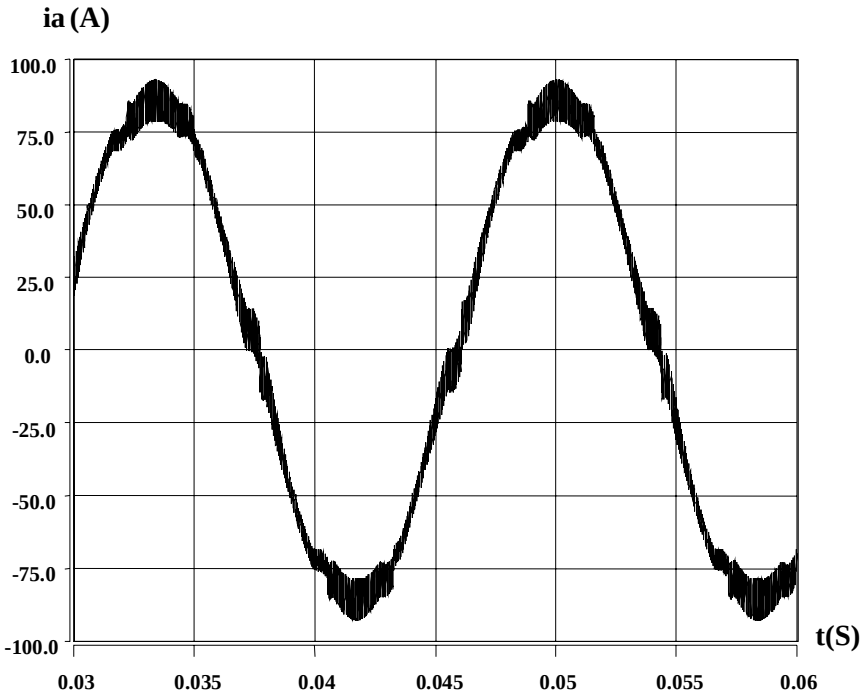


Figure 3.34. Phase current waveform with dead time

Another benefit of this SVM scheme is that the pulse width of each phase is almost doubled. This is helpful in minimizing the duty cycle loss introduced by soft switching. Additionally, the duty cycle does not change much in the consecutive switching cycles, especially in steady state. The symmetry of the PWM signals means less THD.

Due to the fast computation ability of the DSP, the sampling frequency of the DC bus regulator is set to 40kHz while keeping the switching frequency at 20kHz. This minimizes the maximum digital control delay from 100μs to 50μs.

For this high-power application, wide control bandwidth and high performance are especially desired. Thus, an SVM with high sampling frequency, low switching loss and minimal circulating energy is desirable. The evolution diagram of the proposed SVM scheme from the conventional low switching loss SVM scheme is shown in Figure 3.35.

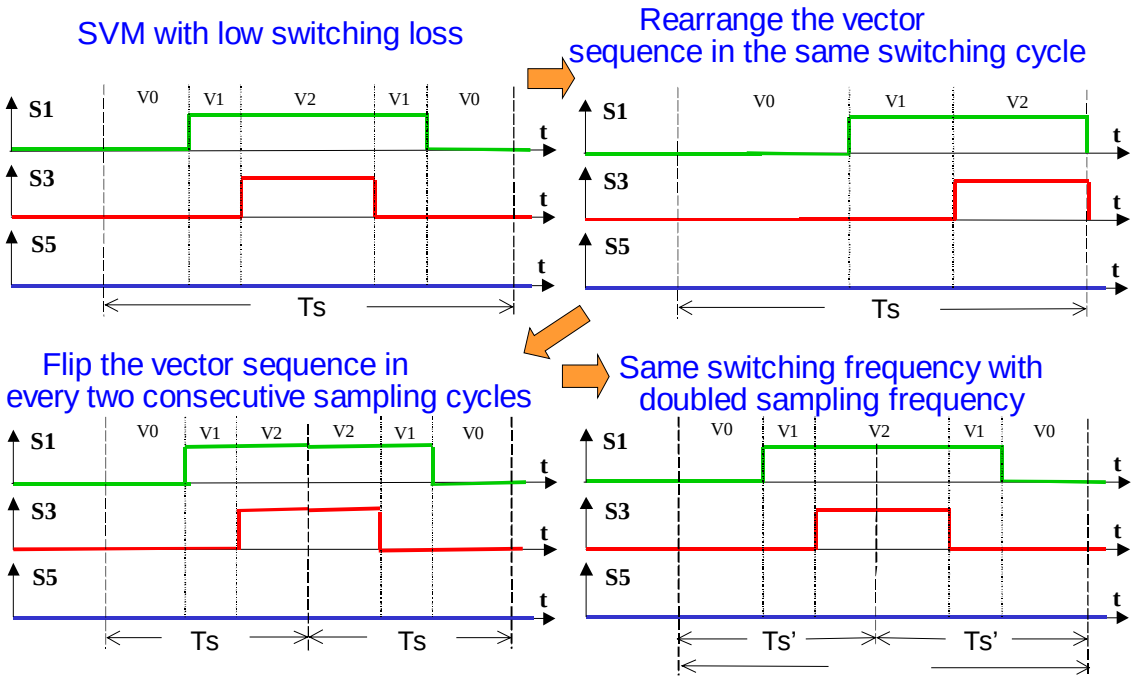


Figure 3.35. Evolution diagram of the proposed SVM scheme

3.3.3 Dead time and its compensation

The third major cause for the low-frequency harmonics is identified as the dead time. The dead time is inserted into the gate signals of the complementary main switches to prevent a short circuit of the DC bus. The dead time is 2μs for the DC bus regulator.

Dead time compensation methods are widely investigated for voltage-source PWM inverters [18-20]. Most of the compensation techniques fall into two categories. One is based on an average value theory [18]. The lost volt-seconds are averaged over an entire cycle and added to the voltage command. In the second category, dead time compensation is realized for each PWM switching cycle [19,20]. This solution can achieve better performance because the compensation has much less phase lag. The key factor in obtaining good compensation is accurate polarity information for each phase current.

Since this DC bus regulator can be treated as a voltage-source PWM inverter with reversed power flow, the compensation techniques proposed for inverters can be applied to the bus regulator. Moreover, the DC bus regulator senses the input phase current for feedback control. It is feasible to obtain accurate phase current information here. Dead time compensation can be conducted in every switching cycle.

The suggested compensation method involves extending the pulse width of the main switches that carry current by the amount of the dead time, as shown in Figure 3.36. Sa* is the command gate signal for phase A. Here, the top switch S1 and the anti-parallel diode of S2 are assumed to carry current. Thus, the gate signal for the bottom switch S2

is not important at this moment. Sad* is extended by the length of the dead time so that S1 has the accurate pulse width after the dead time processing circuit. The actual gate signal for phase A is shown as Sa, which does not have any pulse width loss except that a dead time delay is added.

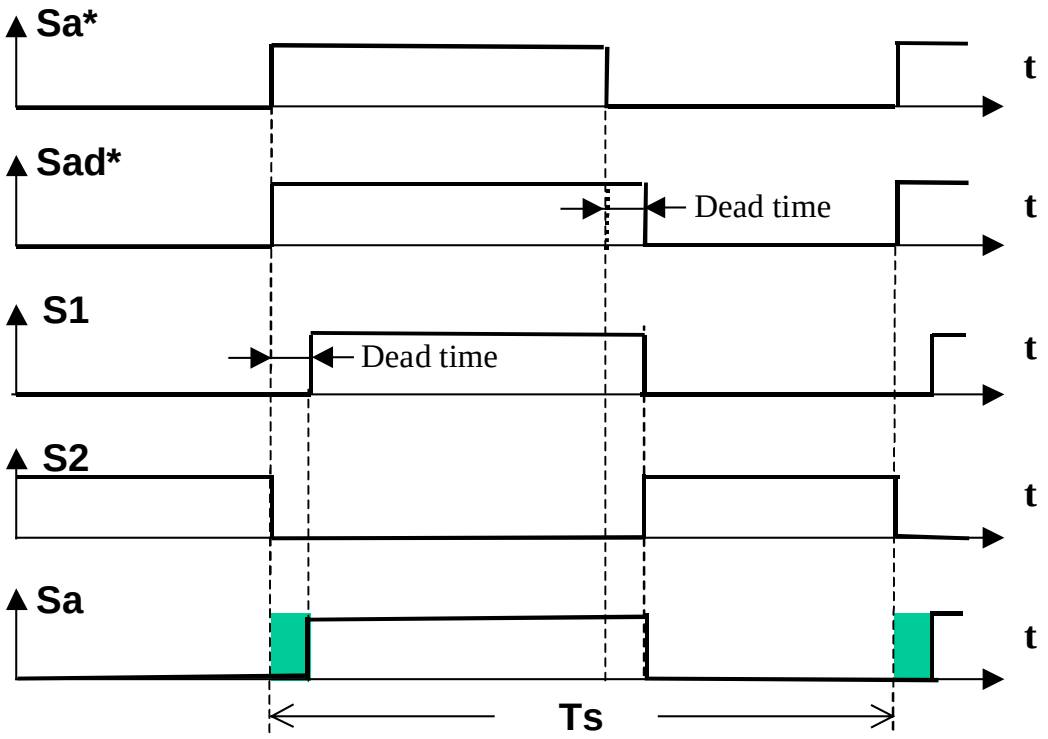


Figure 3.36. Dead time compensation scheme

Phase A current waveform with dead time compensation is shown in Figure 3.37. Clean input phase current waveforms are achieved after correction of the problems associated with PWM techniques. The spectrum of the low-frequency harmonics in the phase current is shown in Figure 3.38. Apparently, the low-frequency harmonics are almost eliminated. The THD for this waveform is about 0.4%.

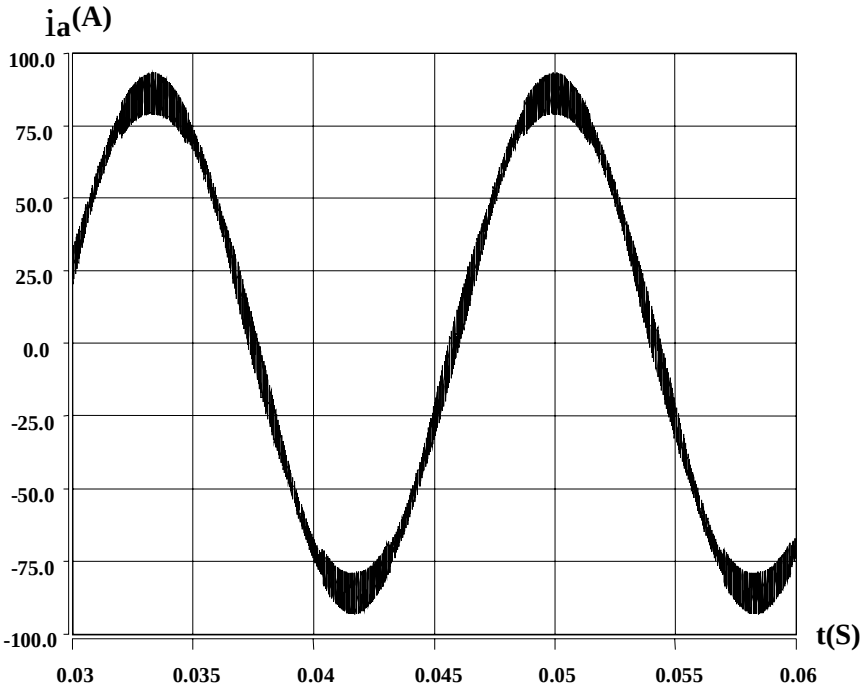


Figure 3.37. Phase current waveform without dead time

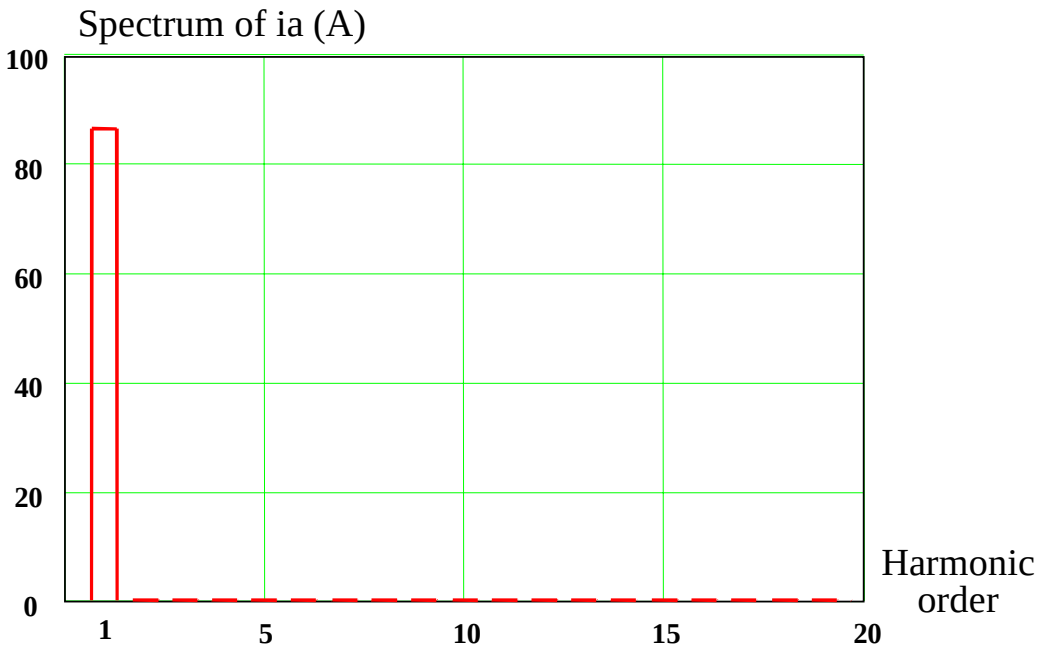


Figure 3.38. Spectrum of the phase current after the compensation

3.4 Noise

Noise is a very important and sometime complex issue, which deserve some discussion in this section.

Appropriate grounding and shielding are always necessary. Optical fibers, isolated DC-DC power supplies and common-mode chokes are used to reduce common-mode noise in this DC bus regulator. Instead of voltage signals, current signals are used to improve the noise immunity of the feedback channels between the PEBB modules and the digital control block.

However, a noise issue still emerges under high voltage. When the DC bus voltage reaches 700V in three-phase PWM operation, the fault signals from PEBB modules often erroneously trigger the protection of the digital controller. The noise occurs in the form of narrow pulses associated with the PWM switching actions. Since the noise pulses are different from the real protection signals, a digital filter is added in the EPLD design to eliminate narrow pulses of less than 500ns. The digital filter resolves the noise issue.

Chapter 4 Experimental Results

4.1 High-Power DC-DC Tests on Individual ZCT PEBB Modules

Each ZCT PEBB module is tested under its rated power and 800V DC bus voltage. The tests assure the proper design and implementation of each PEBB module before it is used to construct the DC bus regulator.

4.1.1 Test Setup for a ZCT PEBB Module

As described in Chapter 2, the ZCT soft-switching PEBB module can be regarded as a combination of two soft-switching cells, as shown in Figure 4.1. The shaded area is the lower of the two soft-switching cells. Due to the symmetry of the two cells, a PEBB module test is further divided into two soft-switching cell tests.

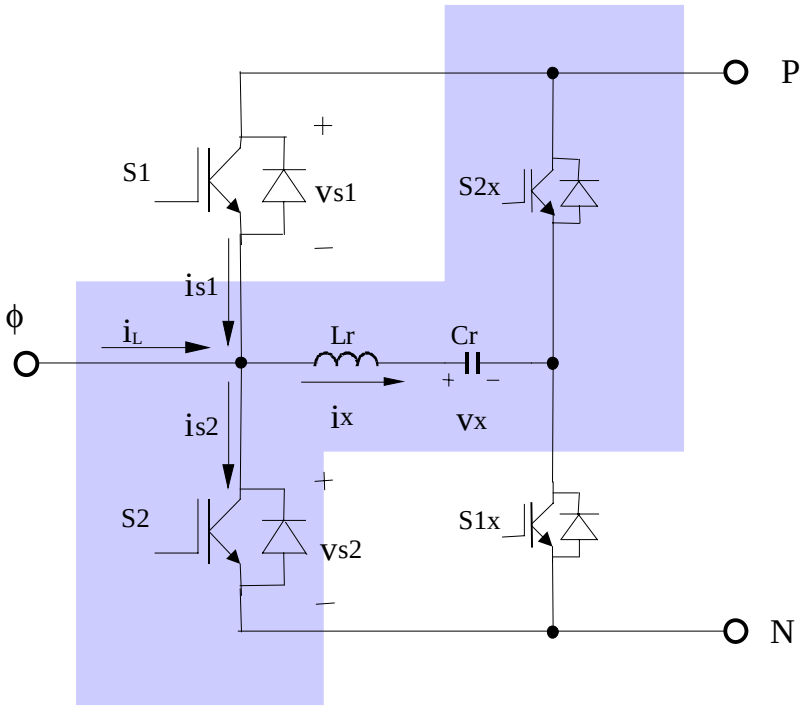


Figure 4.1. Topology of a ZCT PEBB module

Each soft-switching cell can be configured as a boost, buck or other type of DC-DC converter. The objective is to test each soft-switching cell up to its rated power level (18kW) as it works in the DC bus regulator. Since the available resistance of the load bank for high-power tests is very low, each soft-switching cell is configured as a buck converter. The test setup for a phase A top soft-switching cell is shown in Figure 4.2. Control signals are sent to S1 and S1x while S2 and S2x remain turned off. The effective duty cycle for the main IGBT switch S1 is 22%.

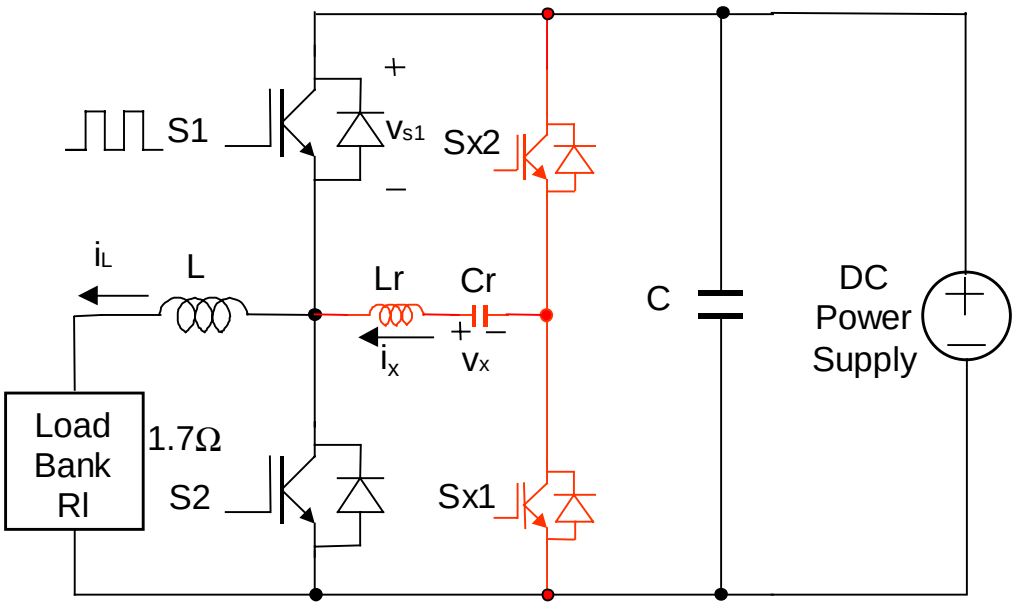


Figure 4.2. Test setup for a single ZCT soft-switching cell

4.1.2 ZCT PEBB Module Test Waveforms

The operating switching frequency is 20kHz (with the ZCT soft switching enabled). The input voltage from the DC power supply is 800V. The output power is adjusted to 18.3kW to emulate the processing power of one ZCT soft-switching cell in the 100kW DC bus regulator. Test waveforms are shown in Figure 4.3. Channel 2 is the voltage across the main IGBT switch. The switch voltage waveform is clean at the turn-off due to the effective ZCT soft-switching operation. Channel 1 is the resonant capacitor voltage Vx. Channels 3 and 4 are resonant inductor current and load current, respectively. It can be found that the main switch is turned off under zero current because the resonant tank sinks more current than that flowing in the inductor L. The auxiliary switch current is zero before it is turned off. This is because the current flows in its anti-parallel diode at that instant. Since the slew rate of the current in the main and auxiliary switches during

the turn-on transition is controlled by the resonant inductor, the rising edge is not as steep as it is in the hard-switching case.

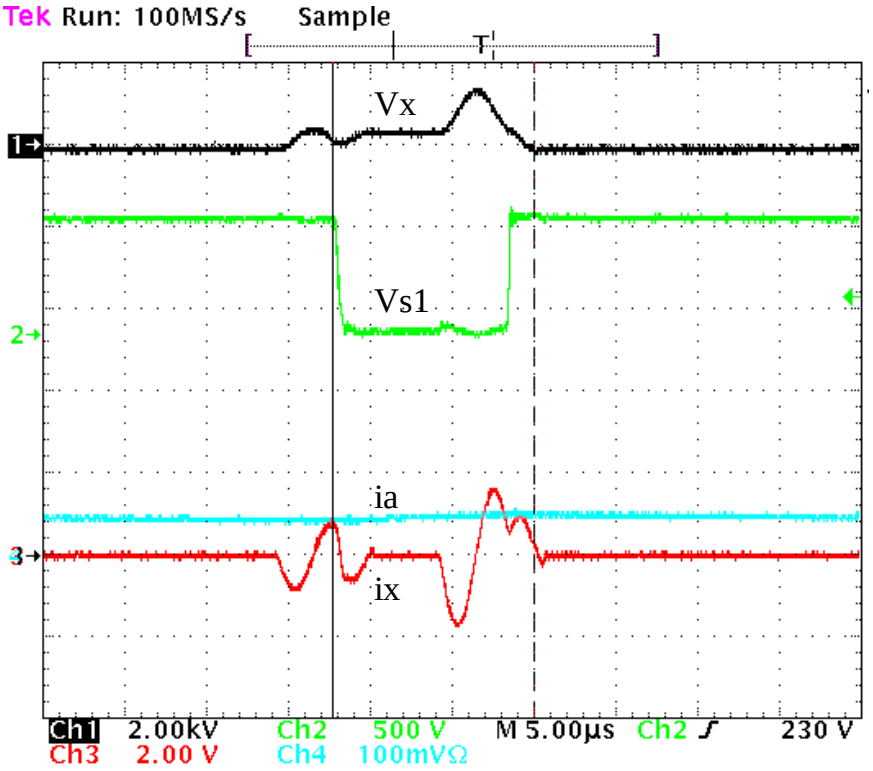


Figure 4.3. Test waveforms of a ZCT soft-switching cell

4.2 Tests on the Digital Control Block

Some of the tests performed on the digital control block are presented in this section. Among these tests, main and auxiliary IGBT switch gate signals for three-phase PWM operation indicate the proper implementation of the SVM PWM modulator and soft-switching pulse generation circuitry. Comparison tests with and without soft-start are conducted to show the necessity of the soft-start function in the digital control block. The computation time of the DSP for a sampling cycle is also tested; based on these results, the sampling frequency is determined.

Figure 4.4 shows two of the three-phase control timings for the main IGBT switches and their corresponding auxiliary IGBT switches. Channels 1 and 3 are the main IGBT gate signals. Channels 2 and 4 are their corresponding auxiliary switch gate signals. The PWM switching frequency is 20kHz. Auxiliary pulse width is 3μs.

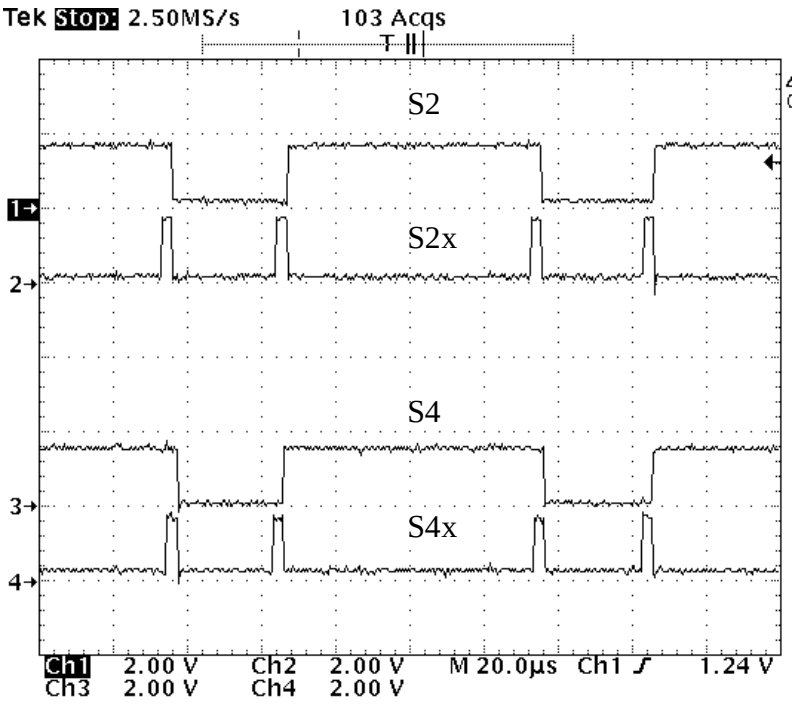


Figure 4.4 Gate drive signals for main and auxiliary IGBT switches

The computation of the DSP for a sampling cycle is measured. The sampling cycle is about 20μs when both the voltage loop and current loop are closed. Leaving some margin for the sampling cycle, 25μs is enough time for the DSP to complete all the computations. Therefore, 40kHz sampling frequency is used to minimize the digital delay for the controller.

During the start-up process, the current loop regulator may not limit the input phase current due to the large transient. Since the rated input current of the DC bus regulator is 120A RMS, without any current limit method, high inrush current may occur during the start-up transition and trigger the over-current protection. The comparison tests are shown in Figure 4.5 and Figure 4.6. Without the soft-start function, the peak input current in Figure 4.5 triggers the protection threshold set at 60A, while the actual start-up phase

current can be limited to 30A with the soft-start function in Figure 4.6. The input current reference is 33A. The start-up current command is 5A.

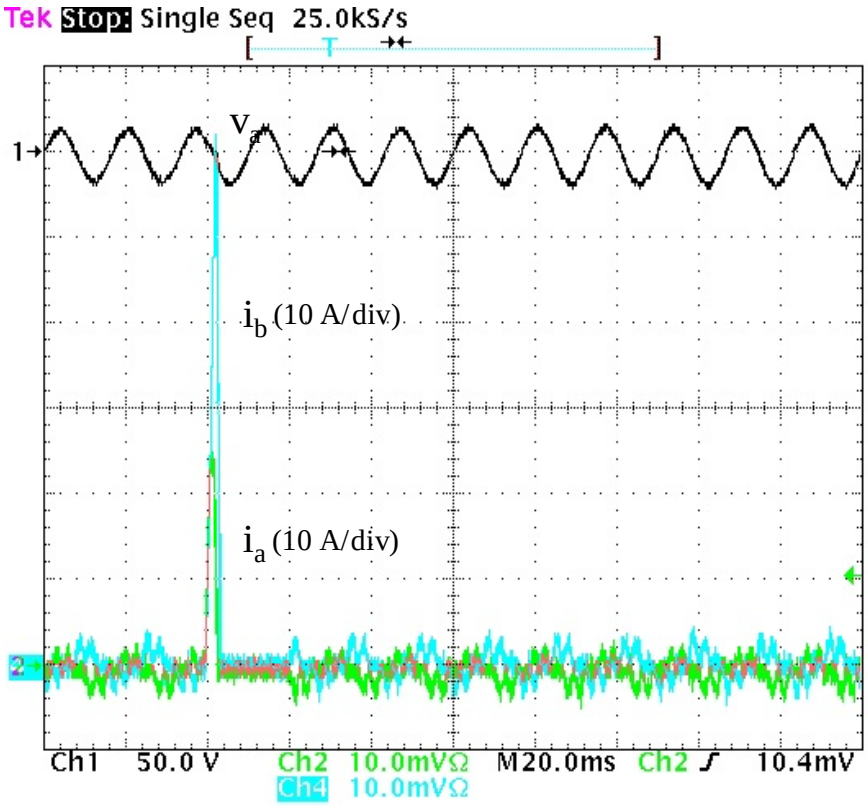


Figure 4.5 Start-up of the DC bus regulator without the soft-start function

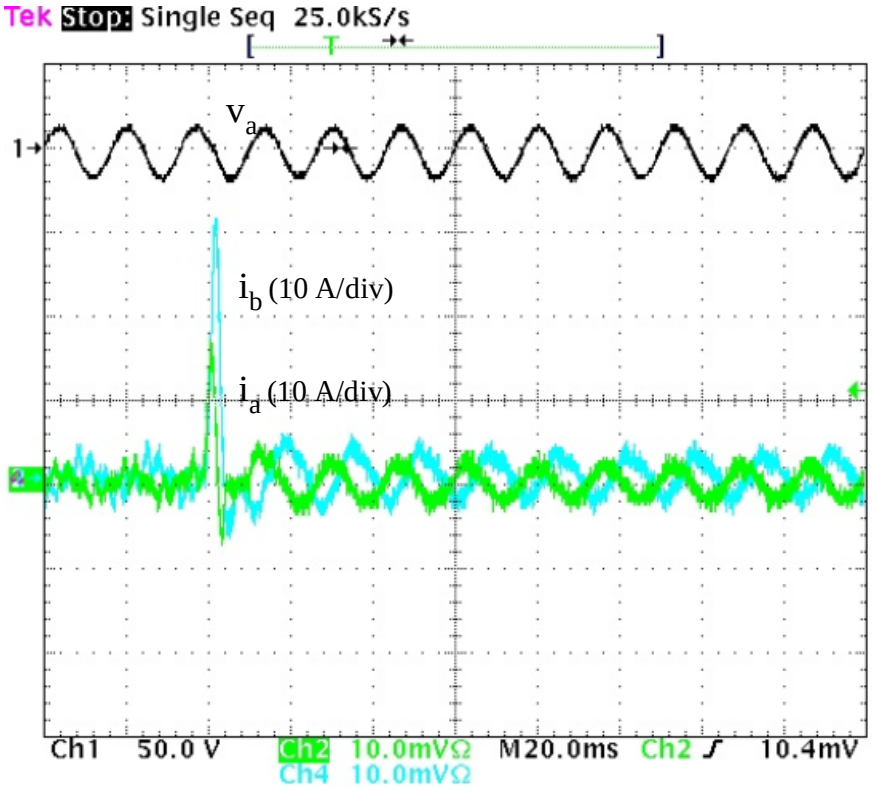


Figure 4.6 Start-up of the DC bus regulator with the soft-start function

4.3 Tests on Critical Protections of the DC Bus Regulator

To ensure safe operation of the DC bus regulator, a multilevel protection scheme is implemented. At PEBB module level, the gate drive circuit incorporates the desaturation protection, which protects the IGBT switch from short-circuit current. At the system level, three-phase AC voltage, current and DC bus voltage information sensed for feedback control is used to protect the DC bus regulator from abnormal operation conditions. Generally speaking, these protection functions cover most of the fault conditions as long as the control building block works properly. However, the DSP controller may malfunction as a result of strong external interference. Under this circumstance, the DSP may end up with improper operation that leads to over-current at the AC side and/or over-voltage at DC side, and it will not try to shut down the bus regulator. One method to deal with this situation is to implement a "watchdog" in the digital control block. This is basically an independent timer that requires a reset signal from the DSP controller periodically. When something is wrong with the DSP controller, the "watchdog" cannot get the reset signal from the controller. It will deactivate the control signals to the PEBB modules and reset the DSP controller, in other words, it shuts down the DC bus regulator. The "watchdog" can be implemented in the EPLD. In this DC bus regulator, extra hardware is added instead. For the AC side over current, semiconductor fuses are used. At the DC side, a crowbar is designed and installed to prevent the over-voltage across the DC bus. Hardware methods are reliable and can prevent further damage under fault conditions.

4.3.1 Tests on the Desaturation Protection of IGBT Switches

The desaturation protection is a built-in function in the driver IC MC33153. As shown in Figure 4.7, the voltage drop of an IGBT switch during turn-on is introduced by the fast recovery diodes D2 and D3. When short circuit occurs, the fast recovery diodes are anti-biased. The capacitor C1 is charged by the current source in the MC33153. When the capacitor voltage Vc exceeds the threshold, the driver IC will soft turn off the IGBT switch and send fault a signal to the digital control block via optic fibers.

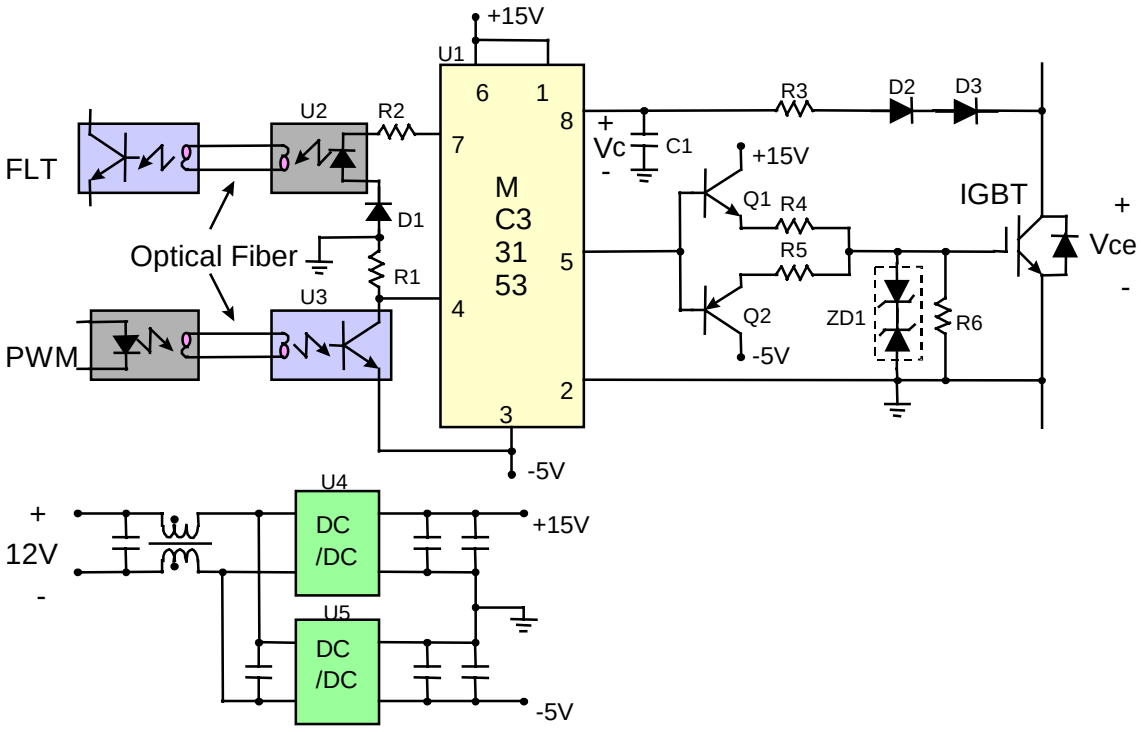


Figure 4.7 Desaturation protection of the IGBT gate drive

The protection mechanism of the IGBT gate drive is tested using the circuit configuration shown in Figure 4.8.

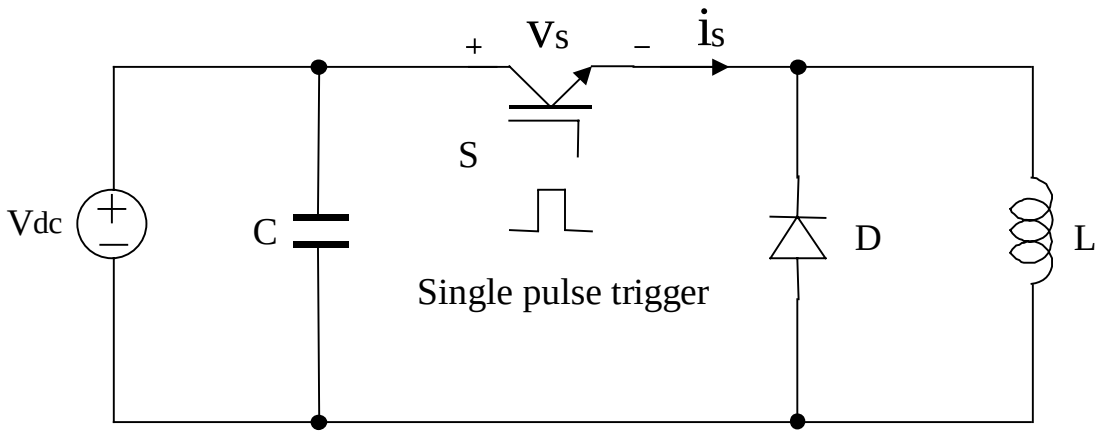


Figure 4.8 Test circuit for the IGBT gate drive protection

In this DC bus regulator, the maximum current in the main IGBT switches is about 400A due to the soft switching. Thus, the protection threshold for the main IGBT switches was set to 450A. The burst mode of the function generator (HPE3631A) is used as a single pulse trigger. The pulse width of the gate signal and DC bus voltage are adjusted to charge the inductor current to exceed the protection threshold. Test waveforms are shown in Figure 4.9.

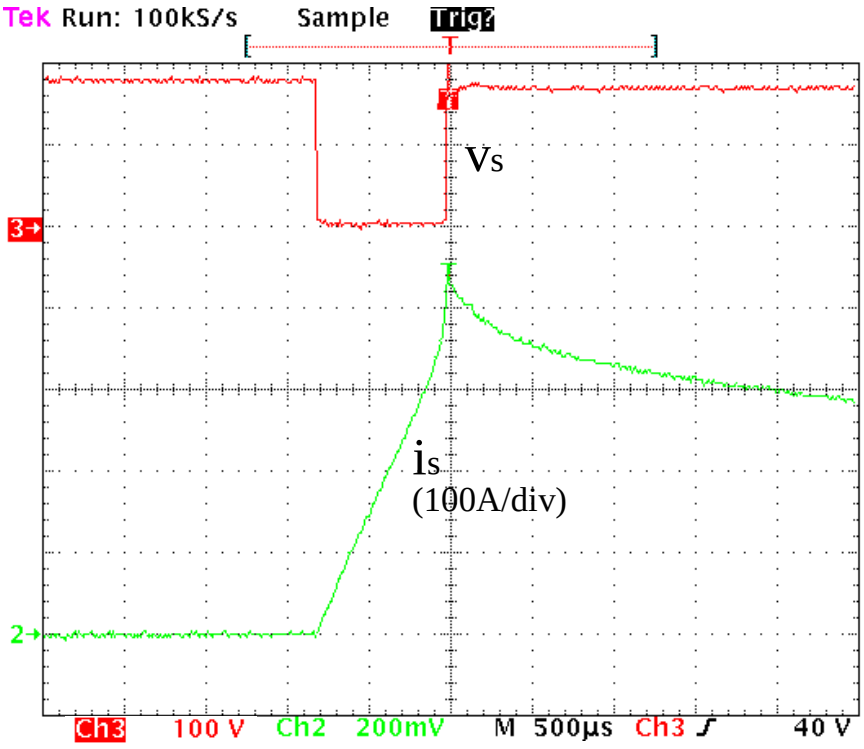


Figure 4.9. Test waveforms of IGBT gate drive desaturation protection

In Figure 4.9, channel 2 is the IGBT switch current waveform (100A/div). Channel 3 is the voltage across the IGBT switch. From the switch current waveform, the magnetic core of the inductor becomes saturated at about 360A. After the saturation, the switch current increases sharply. This is similar to what happens during short-circuit. The IGBT switch is turned off when the current reaches 450A. For the auxiliary switch, the desaturation threshold is set to 290A to enable the peak resonant current.

4.3.2 Tests on the Over-Voltage Protection of the DC Bus

Since over voltage can destroy the switches and capacitors connected to the DC bus, it is extremely important to prevent the DC bus voltage from reaching a dangerous

level. To prevent catastrophic DC bus voltage, a crowbar is installed across the DC bus as shown in Figure 4.10.

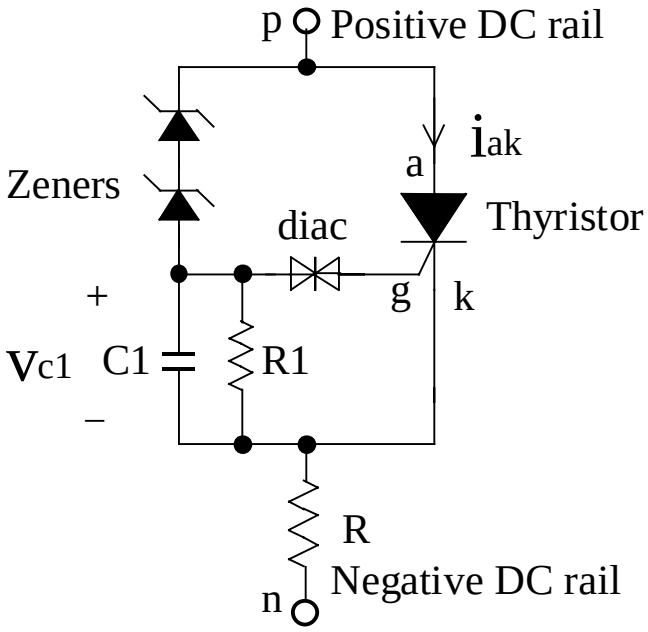


Figure 4.10 Crowbar circuit

In Figure 4.10, the threshold is set to 1070V by the zener diodes. When the DC bus voltage exceeds this threshold, the diac will trigger the thyristor. After the thyristor is turned on, the DC bus capacitor will be discharged by the crowbar. The series resistor R limits the discharge current through the thyristor. If the crowbar takes action, the semiconductor fuses will be blown out and the input power will be cut off. The test waveforms in Figure 4.11 show that the thyristor is triggered when the bus voltage reaches 1070V.

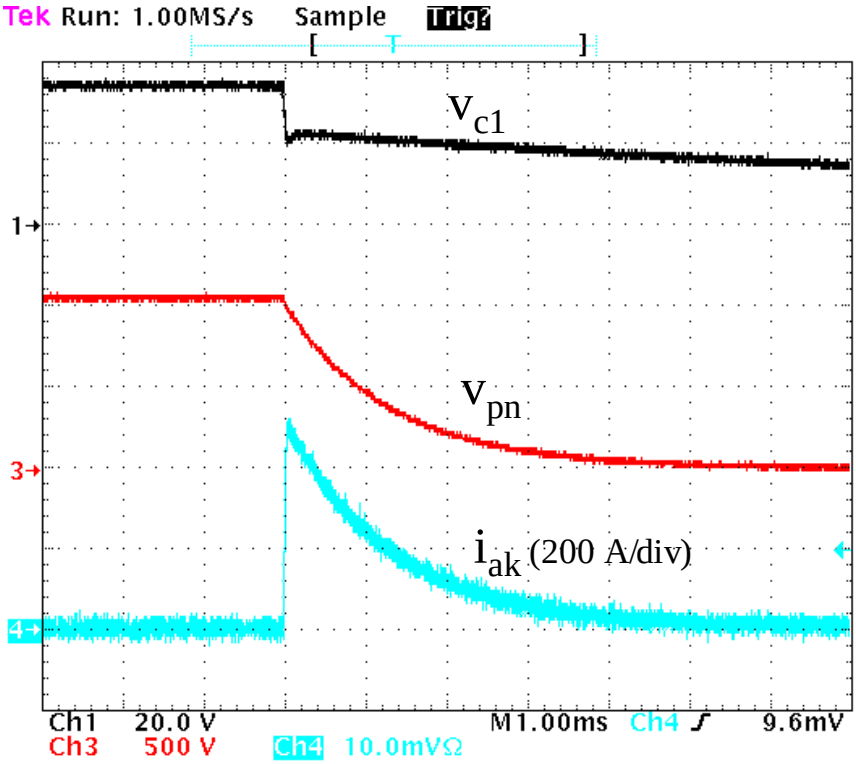


Figure 4.11. Test waveforms for the crowbar

In Figure 4.11, channel 1 is the voltage across capacitor C1. Channel 3 is the DC bus voltage, and channel 4 is the current flowing into the crowbar i_{ak}. The measured peak current in the crowbar is 520A.

4.4 DC Bus Regulator Tests in Inverter Mode

The inverter mode test is necessary for this DC bus regulator. The main difference between the inverter mode and the rectifier mode is that the direction of the power flow is different. This makes the inverter mode similar to a buck converter, and the rectifier mode similar to a boost converter. High-power tests in inverter mode can assure that the ZCT PEBB modules can work well in three-phase PWM operation.

From the control aspect, the rectifier mode has to use closed-loop control to achieve unity power factor and tightly regulated output DC voltage, while the open-loop control is sufficient for the inverter mode. The PWM modulator and other parts of the digital control block are almost the same for the two different operation modes. Therefore, the inverter mode greatly facilitates the debugging of the digital control block for the bus regulator.

4.4.1 Inverter-Mode Test Setup

The inverter-mode test scheme is shown in Figure 4.12. A three-phase R-L load is used in the tests. The DC bus is connected to an 800V power supply. The AC output voltage is set to 480V (line-to-line). By adjusting the load resistance, the output power is set.

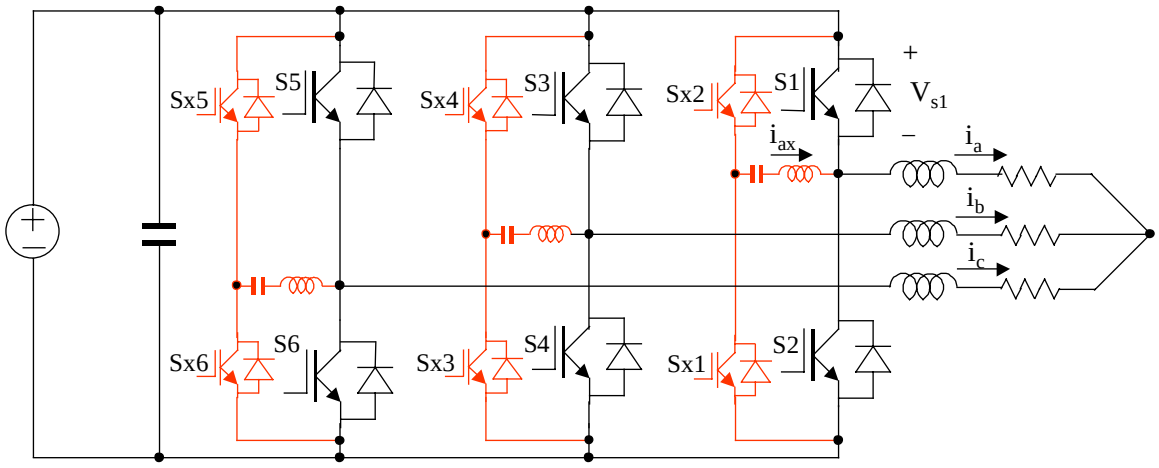


Figure 4.12. Inverter mode test scheme

4.4.2 High Power Test Results in Inverter Mode

The bus regulator in the inverter mode is tested up to 70kW with 800V DC bus voltage, which is the maximum power available from the DC power supply. The test waveforms are shown in Figure 4.13. Channels 2 and 4 are output phase current ia and ib, respectively. Channel 1 is the voltage across the main IGBT switch S1 Vs1. Channel 3 is the resonant tank current iax, which indicates the soft-switching operation. The soft-switching operation is only activated when the main IGBT switches are switching.

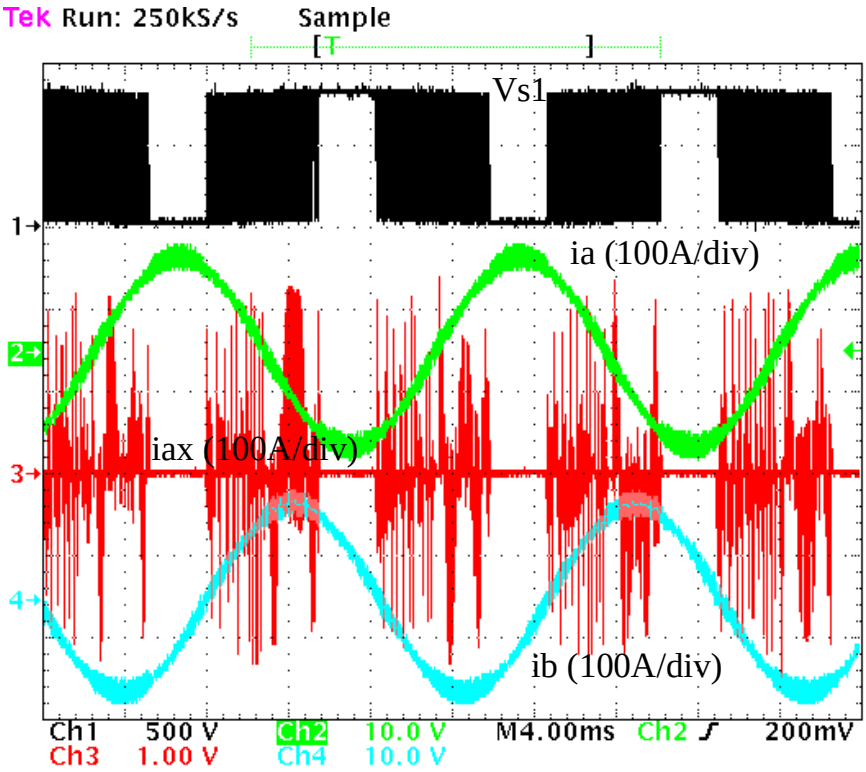


Figure 4.13. Inverter test waveforms at 70kW with ZCT soft switching

The reliability of the power stage and basic functions of the digital control block are proven in the inverter mode tests.

4.5 DC Bus Regulator Tests in Rectifier Mode

4.5.1 Test Setup For Rectifier-Mode Operation

The test circuit configuration for the DC bus regulator in rectifier mode is shown in Figure 4.14. A three-phase AC power supply is connected at the input of the DC bus regulator. The output of the DC bus regulator is connected to the load bank.

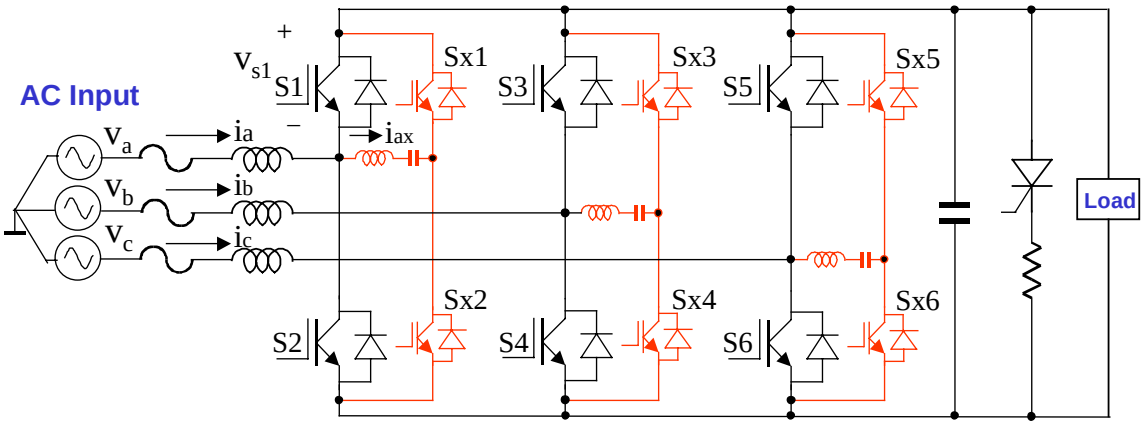


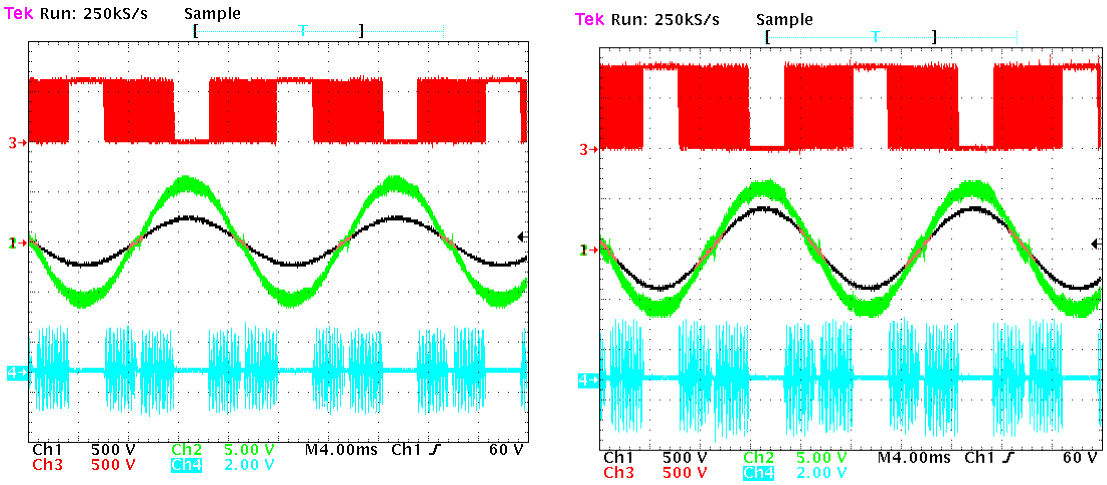
Figure 4.14. Circuit configuration for the rectifier mode tests

4.5.2 Test results of the DC Bus Regulator in Rectifier Mode

In rectifier mode tests, 20kHz switching frequency is applied. The control bandwidth for the current loop is set at 1.5kHz. The corner frequency of the voltage loop is set to 300Hz. Wide loop bandwidth ensures a tightly regulated DC bus.

The experimental waveforms with current loop closed under different DC bus voltages are shown in Figure 4.15. Channel 1 is the input phase voltage. Channel 2 is the

input phase current (50A/div). Channel 3 is the IGBT switch voltage. Channel 4 is the corresponding resonant tank current. The same reference current is used. However, the phase current ripple is larger for Figure 4.15b due to the higher DC bus. And it is evident that there are distortions at the zero-crossings due to the improper SVM scheme discussed in Chapter 3. But the zero-crossing distortions are eliminated for all the other waveforms shown in this section because the correction technique is applied.



(a) (b)

Figure 4.15. Experimental waveforms for rectifier mode under different DC bus voltages: (a) 600V; and (b) 800V.

Figure 4.16 shows the test waveforms at 800V DC voltage output with both current and voltage loops closed. The output power is 83kW. Va is the phase A input voltage, and ia is the input phase A current. ia is the phase A resonant tank current. It indicates the soft-switching operation of the PEBB module in a three-phase converter. Vs1 is the IGBT switch waveform, which shows the 60°- clamping SVM PWM pattern.

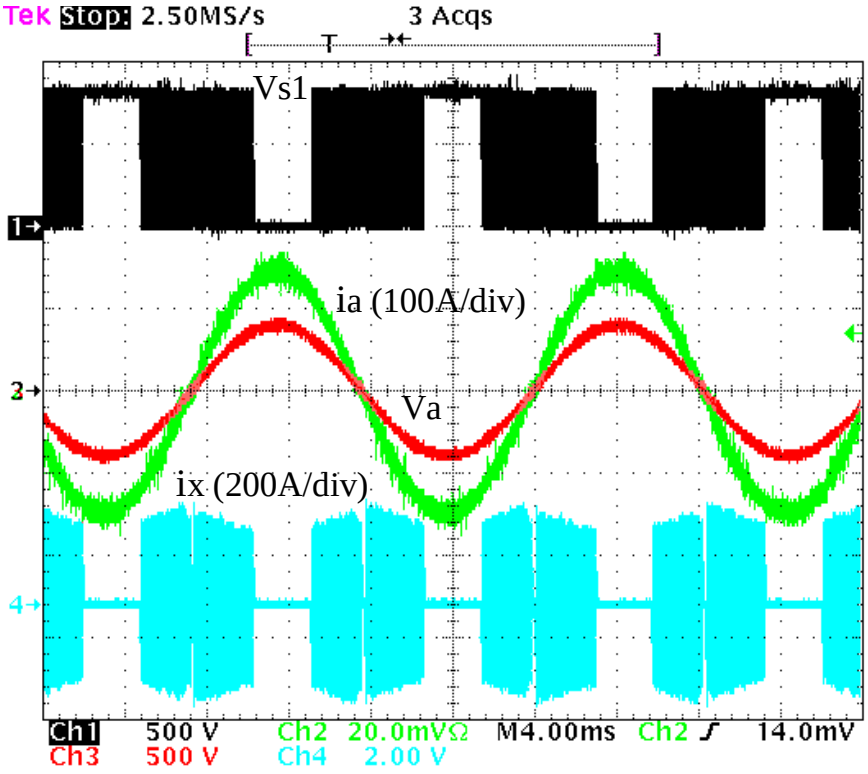


Figure 4.16. Experimental waveforms with two loops closed under 800V

The test waveforms under a wide range of the load conditions are shown in Figure 4.17 through Figure 4.21. Unity power factor is achieved for all these load conditions based on the measurements.

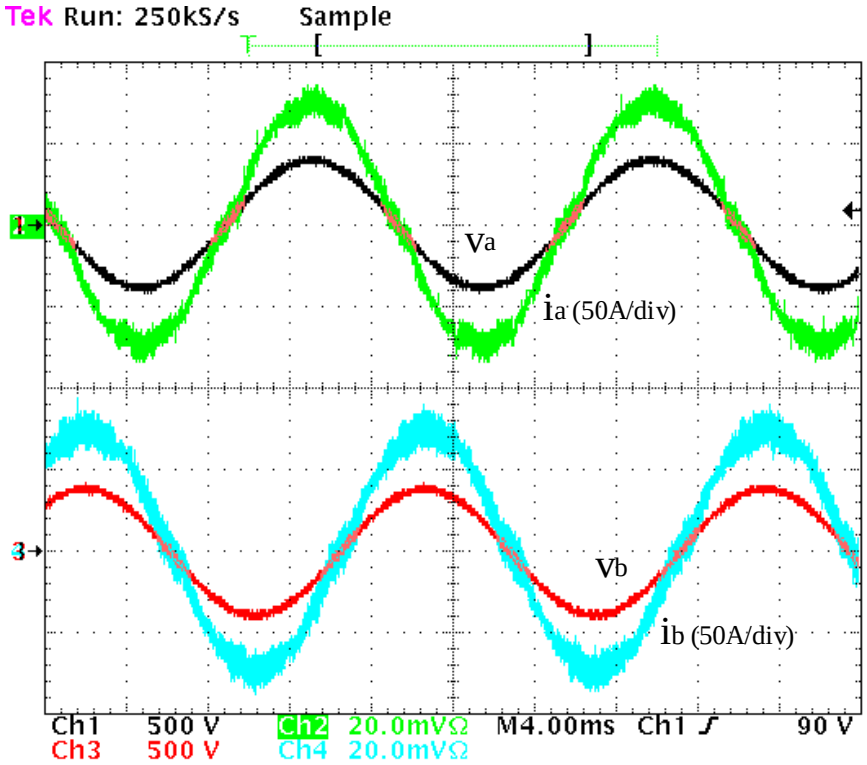


Figure 4.17 Input phase voltage and current waveforms at 34kW

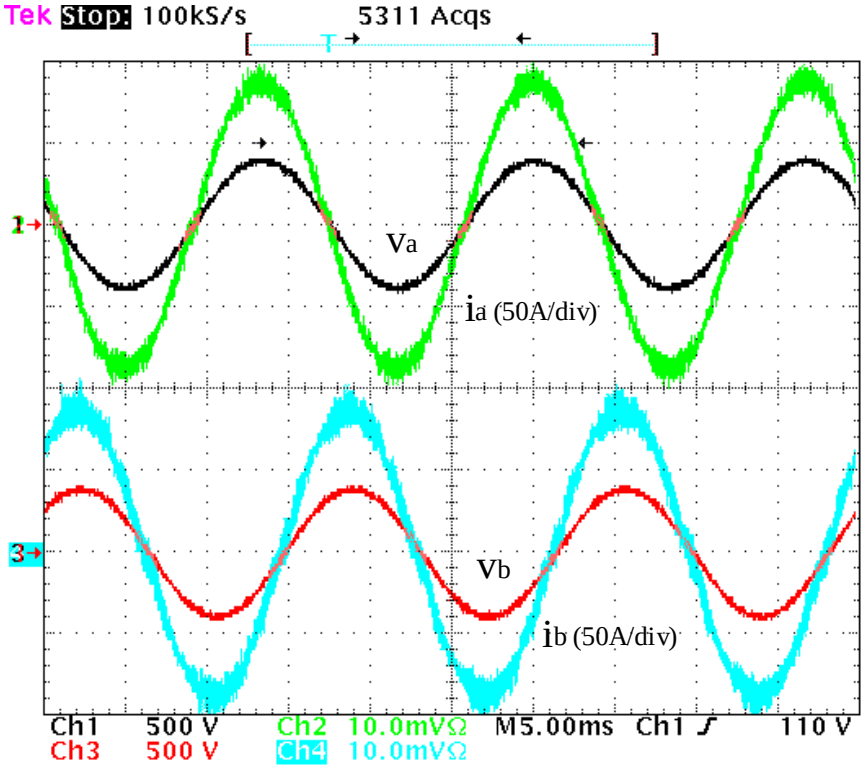


Figure 4.18 Input phase voltage and current waveforms at 50kW

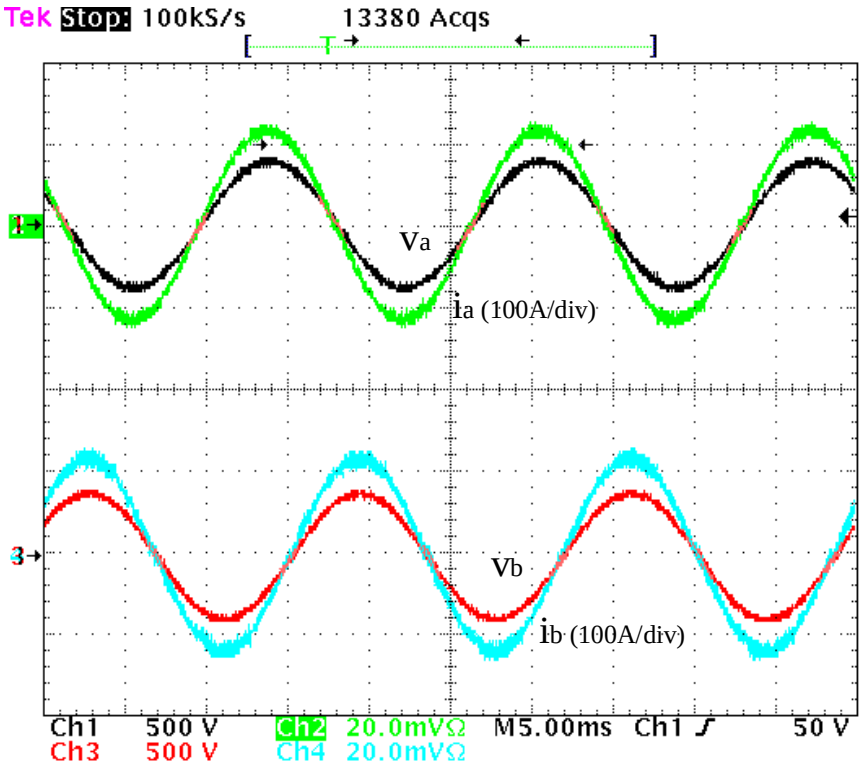


Figure 4.19 Input phase voltage and current waveforms at 67kW

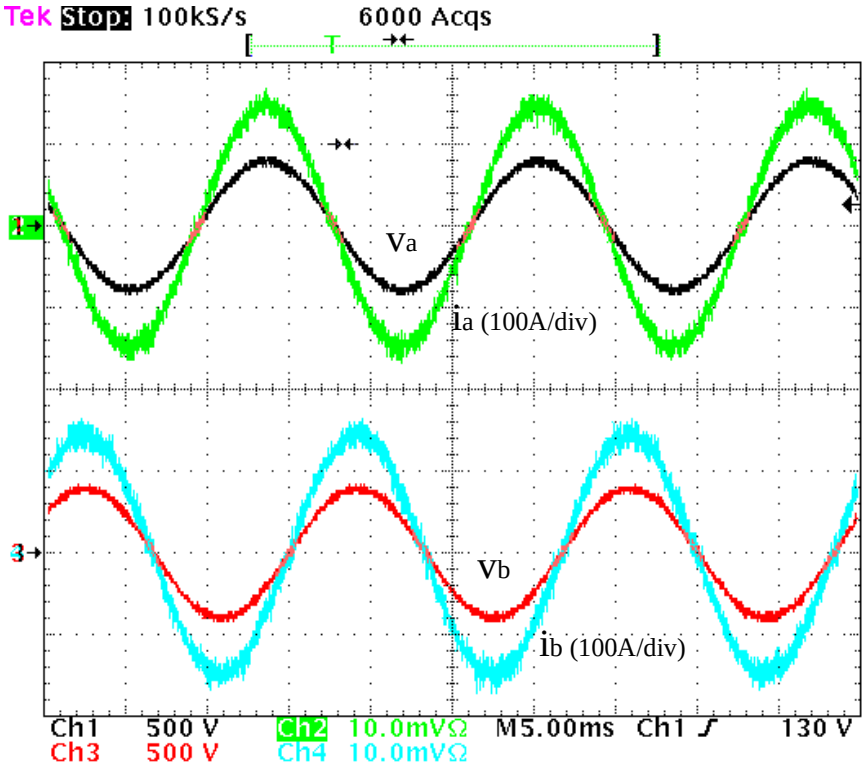


Figure 4.20 Input phase voltage and current waveforms at 83kW

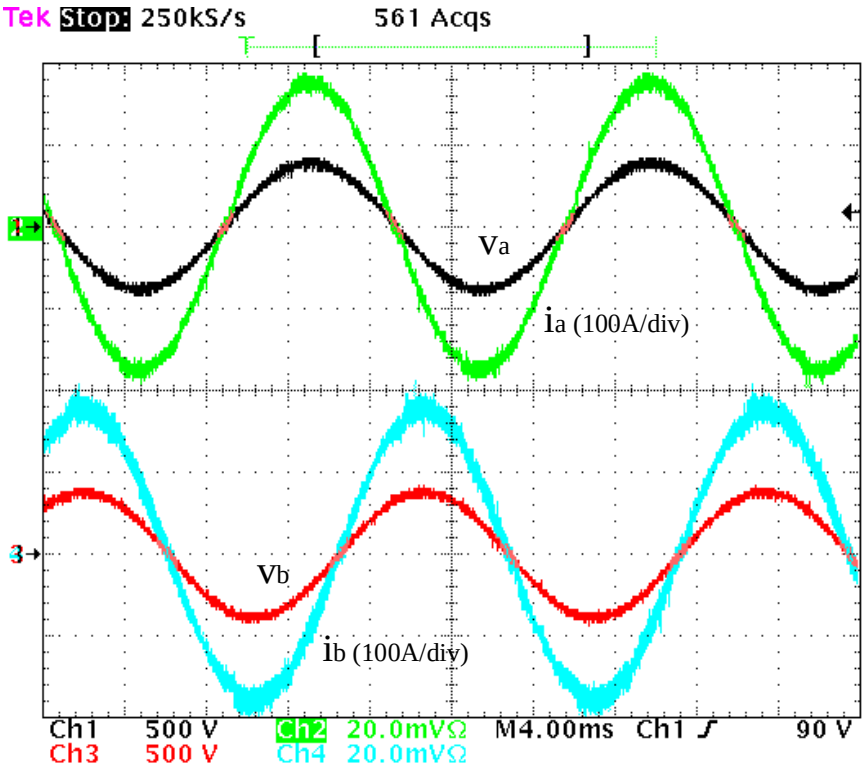


Figure 4.21 Input phase voltage and current waveforms at 100kW output power

Measured efficiency under different power levels is plotted in Figure 4.22. As shown by the efficiency curve, high efficiency has been achieved over a wide power range. More than 97% efficiency is reached for the load conditions higher than 75% of the full load.

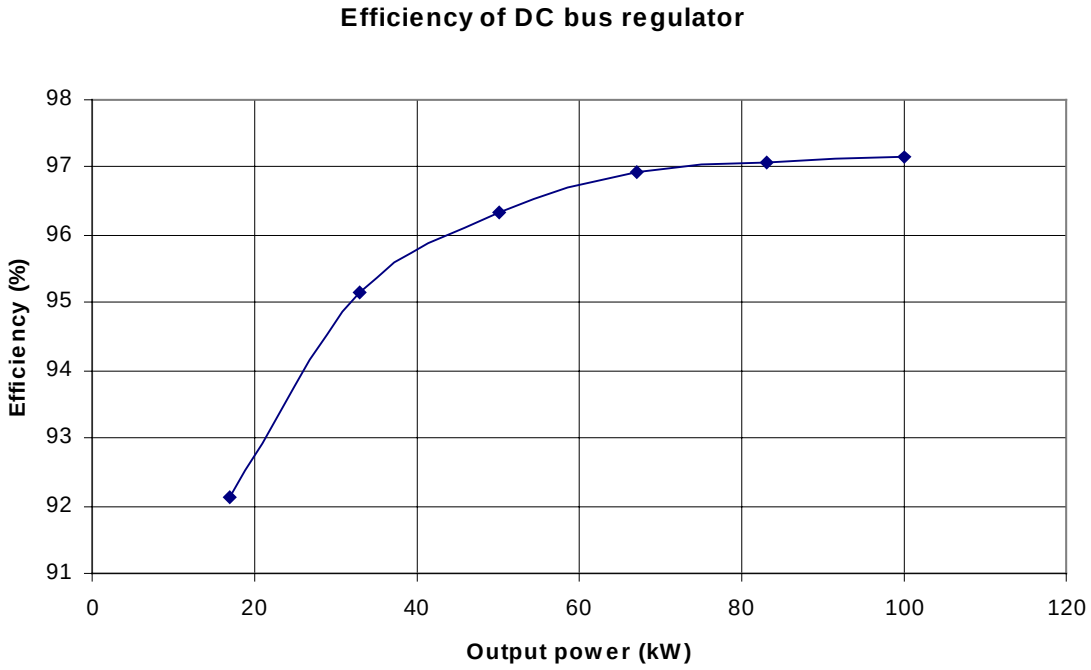


Figure 4.22 Efficiency curve of the DC bus regulator

Measured THD for the input current is shown in Figure 4.23. The THD decreases with the power level. At full power level, the THD is about 2.3%, which is much lower than the specified goal.

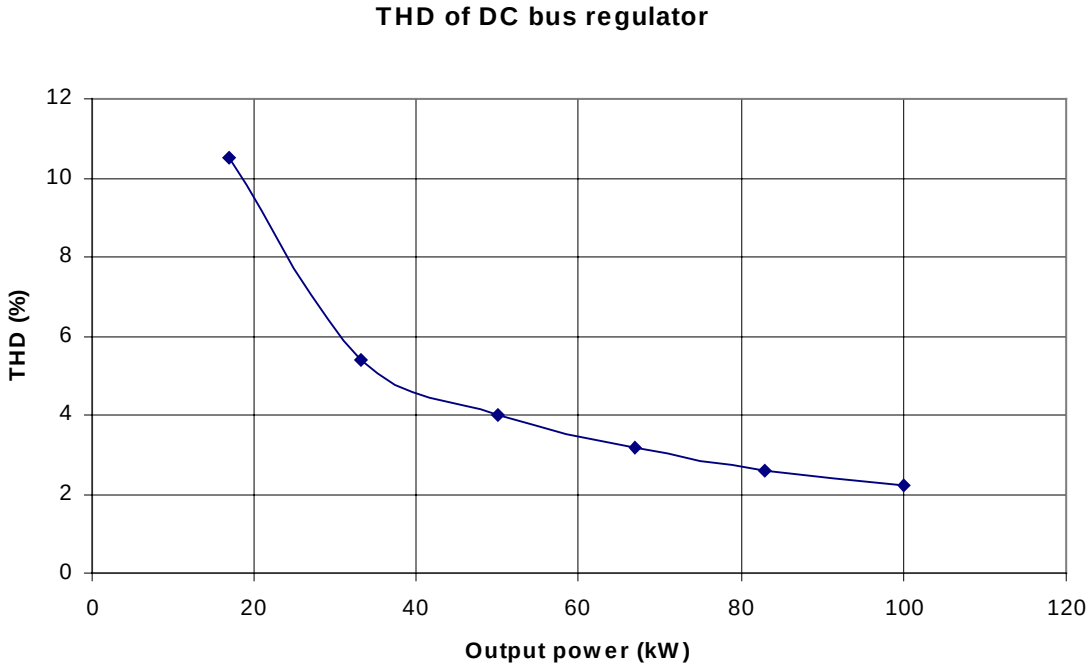


Figure 4.23 Measured THD under different power levels

In summary, high efficiency, low THD, unity power factor, wide control bandwidth and high power density are all achieved.

Chapter 5 Conclusions and Future Work

5.1 Conclusions

PEBBs have many advantages as elements in power electronics systems. Based on the PEBB concept, large-scale power electronics systems are much easier to implement. The PEBB approach not only reduces cost, but also leads to high redundancy, high reliability, high flexibility and easy maintenance.

ZCT soft-switching techniques are favorable for the PEBB system because they can absorb the parasitic inductance along the distributed DC bus. The adopted ZCT technique can achieve zero current switching for all of the main and auxiliary IGBT switches and their anti-parallel diodes. Turn-off loss can be basically eliminated. Diode reverse recovery and IGBT turn-on loss also can be greatly reduced. In summary, this ZCT soft-switching technique substantially drives down switching loss and improves overall efficiency.

The ZCT soft-switching technique has several potential issues in three-phase applications: (1) control timing of the auxiliary switch gate signals, (2) low-frequency harmonics caused by the pulse width limits, and (3) thermal stress on resonant capacitors. These issues are resolved by utilizing the freedom of the PWM modulator and the sensed phase current information. By properly designing a PWM modulator, the switching events and associated loss are significantly reduced while keeping low THD. Reduced switching events also alleviate the thermal issue of the resonant capacitors. The same modulation technique can double the sampling frequency and avoid the low-frequency harmonics caused by the pulse width limits. The phase current information is used to

solve the control timing issue of the auxiliary switches by disabling the ones that are unnecessary. It is also used to control three-phase soft-switching operation to achieve better overall efficiency. In addition, the phase current information is used to implement dead time compensation in order to reduce THD.

The soft-switched DC bus regulator built based on the PEBB concept has been tested up to the 100kW power level with 20kHz switching frequency. The ZCT soft-switching technique is proved to be an effective approach to achieve high performance for the DC bus regulator. The switching frequency of the bus regulator is four times as high as its hard-switching counterparts used in industry (5kHz switching frequency) with the same rated IGBT modules.

The experimental results demonstrate that high performance is accomplished for the DC bus regulator in terms of wide control bandwidth, low THD, unity power factor, high efficiency and high power density.

5.2 Future Work

One of the future working directions is the optimization of the ZCT soft-switching operation to achieve higher overall efficiency. Although the adopted ZCT soft-switching technique can significantly reduce the switching loss, the increased conduction loss in the main switches and auxiliary circuit is not negligible. Therefore, minimizing the circulating energy due to the soft-switching operation will improve overall efficiency.

Another issue for future study is minimizing the duty cycle loss required by the soft-switching operation.

The EMI issue is also worthy of exploration. How to utilize the soft switching to effectively minimize the EMI is another topic of the future work.

References

[1] Chester Petry, “Shipboard Electrical Power Architecture, “ Control Technology Workshop: The Regulation and Distribution of Power in Large Systems, 1995, pp. 102-131.

[2] Kun Xing, Modelling, Analysis, and Design of Distributed Power Electronics System Based on Building Block Concept, Dissertation, Viginia Tech, 1999.

[3] S. Hiti, D. Boroyevich, R. Ambatipudi, R. Zhang and Y. Jiang, “Average Current Control of Three-Phase PWM Boost Rectifier,” VPEC’95 Proc., pp. 85-92, 1996.

[4] G. Carli, “Elimination of Input Harmonic Currents in 3 Phase AC to DC Converters: A Practical Approach,” INTELEC’93 Proc., pp. 399-406, 1993.

[5] G. Hua, E. Yang, Y. Jiang, and F. C. Lee, “Novel Zero-Current-Transition PWM Converters,” IEEE-PESC, 1993, pp. 538-544.

[6] R. W. De Doncker and J. P. Lyons, “The Auxiliary Resonant Commutated Pole Converters,” IEEE-IAS Annu. Meet., 1990, pp. 1228-1235.

[7] G. Hua, C. Leu, and F. C. Lee, “Novel Zero-Voltage Transition PWM Converter,” IEEE-PESC, 1992, pp. 55-61.

[8] C. Cuadros, D. Boroyevich, S. Gataric, V. Vlatkovic, H. Mao, and F. C. Lee, “Space Vector Modulated, Zero-Voltage Transition Three- Phase to DC Bidirectional Converter,” IEEE-PESC, 1994, pp. 16-23.

[9] K. Taniguchi, T. Morizane, N. Kimura, “High-Performance Soft-Switched Three-Phase Converter with Sinusoidal Input Current and Unity Power Factor,” IEEE-APEC, 1997, pp. 672-678.

[10] H. Mao, F. C. Lee, X. Zhou, and D. Boroyevich, “ Improved Zero-Current Transition Converters for High Power Application,” IEEE-IAS Annu. Meet., 1996, pp. 1145-1152.

[11] H. Dai, K. Xing and F. C. Lee, “Investigation Of Soft-Switching Techniques For Power Electronics Building Blocks (PEBB),” IEEE-APEC, 1998, pp. 633-639.

[12] I. Milosavljevic, D. Boroyevich, “ Modularized Control Architecture for Power Converters,” VPEC ’98 Seminar Proceedings, September 1998.

[13] H. van der Broeck, “ Analysis of the Harmonics in Voltage Fed Inverter Drives Caused by PWM Schemes with Discontinuous Switching Operation,” EPE’91 Proc., pp. 3/261-3/266, 1991.

[14] D.G. Holmes, “ The Significance of Zero Space Vector Placement for Carrier Based PWM Schemes,” IEEE-IAS Annu. Meet., 1995, pp. 2451-2458.

[15] H. Prasad, D. Boroyevich and S. Dubovsky, “Comparison of High Frequency PWM Algorithms for Voltage Source Inverters,” VPEC’96 Proc., pp. 115-122, 1996.

[16] J. Wu et al, “Implementation of a 100KW Three-Phase PFC Rectifier with ZCT Soft-Switching Technique,” PESC’99 Proc., pp. 647-652, 1999.

[17] K. Xing et al, “Interleaved PWM with Discontinuous Space Vector Modulation”, IEEE Trans. on PE, Vol. 14, No. 5, pp. 906-917, 1999.

[18] T. Sukegawa et al, “Fully Digital, Vector-Controlled PWM VSI Fed AC Drives with an Inverter Dead Time Compensation Strategy,” IEEE Trans. on IA, Vol. 27, No. 3, pp. 552-559, 1991.

[19] Munoz-Garcia, A. and T. A. Lipo, “On-Line Dead Time Compensation Technique for Open-Loop PWM-VSI Drives,” IEEE APEC’98, Anaheim, CA, Feb.15-19, pp. 95-100, 1998.

[20] D. Leggate and R. Kerkman, “Pulse Based Time Compensator for PWM Voltage Inverters,” IEEE Trans. on IE, vol. 44, No.2, pp. 191-197, 1997.

[21] J. Wu, F. C. Lee and D. Borojevic, “Elimination of Low-Frequency Harmonics Caused by PWM in a Three-Phase Soft-Switched Boost Rectifier for PWM Voltage Inverters,” to be published at IEEE IAS’2000.

Vita

The author received the B.S. degree in 1993 and the M.Eng. degree in 1996, both from the Department of Electrical Engineering in Tsinghua University, Beijing, China.

He was employed as a development engineer in Tsinghua Unisplendor Co., Beijing, China from 1996 to 1997.

In the summer of 1997, he was enrolled in the Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University as a research assistant. His research interests are modeling and control of power electronics system, DC distributed power system and embedded system design.