Surge-energy and Overvoltage Robustness of Cascode GaN Power Transistors

Qihao Song

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

Yuhao Zhang, Chair
Yang (Cindy) Yi
Qiang Li

May 9th, 2022
Blacksburg, Virginia

Keywords: Wide-bandgap, Power Electronics, Power Device, Gallium Nitride,
Robustness, Unclamped Inductive Switching

Surge-energy and Overvoltage Robustness of Cascode GaN Power Transistors

Qihao Song

ABSTRACT

Surge-energy robustness is essential for power devices in many applications such as automotive powertrains and electricity grids. While Si and SiC MOSFETs can dissipate surge energy via avalanche, the GaN high-electron-mobility transistor (HEMT) has no avalanche capability and withstands surge energy by its overvoltage capability. However, a comprehensive study into the surge-energy robustness of the cascode GaN HEMT, a composite device made of a GaN HEMT and a Si metal-oxide-semiconductor field-effect-transistor (MOSFET), is still lacking. This work fills this gap by investigating the failure and degradation of 650-V-rated cascode GaN HEMTs in single-event and repetitive unclamped inductive switching (UIS) tests. The cascode was found to withstand surge energy by the overvoltage capability of the GaN HEMT, accompanied by an avalanche in the Si MOSFET. In single-event UIS tests, the cascode failed in the GaN HEMT at a peak overvoltage of 1.4~1.7 kV, statistically lower than the device's static breakdown voltage (1.8~2.2 kV). In repetitive UIS tests, the device failure boundary was found to be frequency-dependent. At 100 kHz, the failure boundary (~1.3 kV) was even lower than the single-event UIS boundary. After 1 million cycles of 1.25-kV UIS stresses, devices showed significant but recoverable parametric shifts.

Physics-based device simulation and modeling were then performed to understand the circuit test results. The electron trapping in the buffer layer of the GaN HEMT can explain all the failure and degradation behaviors in the GaN HEMT and the resulted change in its dynamic breakdown voltage. Moreover, the GaN buffer trapping is believed to be assisted by the Si MOSFET avalanche. An analytical model was also developed to extract the charges and losses produced in the Si avalanche in a UIS cycle. These results provide new insights into the surge-energy and overvoltage robustness of cascode GaN HEMTs.

Surge-energy and Overvoltage Robustness of Cascode GaN Power Transistors

Qihao Song

GENERAL AUDIENCE ABSTRACT

Power conversion technologies are now inseparable in industrial and commercial applications with widespread solar panels, laptops, data centers, and electric vehicles. Power devices are the critical components of power conversion systems. Since the introduction of Si power metal-oxide-semiconductor field-effect-transistor (MOSFET) in the mid-1970s, it has become the go-to device for efficient and reliable power conversion. After decades of practice on Si MOSFET, the device performance has reached the theoretical limit of the Si material. The recent introduction of wide-bandgap (WBG) power transistors, represented by silicon carbide (SiC) and gallium nitride (GaN) devices with superior figures of merits, opens the door for faster and more efficient power systems. To exploit the benefits of WBG devices, researchers need to evaluate the reliability and robustness of these devices comprehensively.

The work presented here studies the robustness of one mainstream GaN power transistor – the cascode GaN high-electron-mobility transistor (HEMT). This robustness test replicates the surge events in power electronics systems and exams their impact on power devices. Over the years, people have thoroughly investigated the surge-energy robustness of Si MOSFETs and concluded that Si MOSFETs are robust against these surge events thanks to the avalanche mechanism. However, GaN HEMTs lack p-n junction structures between the two major electrodes, leading to the lack of avalanche ability. Instead, GaN HEMTs rely on the overvoltage capability to sustain the surge energy. For the first time, this work evaluates the surge-energy and overvoltage ruggedness of cascode GaN HEMTs, a major player in the GaN power device market. By analyzing the device failure mechanism and degradation behaviors, this research provides insight into these devices' weaknesses for both device designers and application engineers.

Acknowledgments

First and foremost, I would like to extend my deepest gratitude to my advisor, Dr. Yuhao Zhang. I still vividly remember talking with Dr. Zhang in his office and listening to him introduce his group and research. As a rookie, I didn't know what to do for my graduate research. He explained everything to me so patiently. I was surprised and ecstatic when he decided to adopt me into the group with trust. Over the years, Dr. Zhang has supported me in and out of the laboratory. He has motivated me with brilliant ideas and unique solutions to various problems. He was also tolerant and helpful when I encountered difficulties, leading me through the barriers with immense knowledge and insightful suggestions.

I would also like to thank Dr. Khai Ngo, Dr. Guo-Quan Lu, Dr. Qiang Li, and Dr. Christina DiMarino for the valuable suggestions on my research. Additionally, I am thankful to Dr. Yang Yi and Dr. Dong Dong for agreeing to be my committee members.

I also must thank all CPES staff for always providing timely support for my research. Many thanks to Ms. Trish Rose, Mr. David Gilham, Ms. Audri Cunningham, Ms. Brandy Grim, Ms. Ling, Li, Mr. Dennis Grove, Ms. Na Ren, Mr. Matthew Scanland, and Ms. Yan Sun.

Furthermore, I am also grateful to my colleagues and friends in CPES: Mr. Xingyu Chen, Mr. Bo Li, Mr. Yuliang Cao, Mr. Xingchen Zhao, Mr. Jian Liu, Mr. Shuo Wang, Mr. Tianlong Yuan, Mr. Feiyang Zhu, Ms. Tianyu Zhao, Mr. Ahmed Nabih, Mr. Zheqing Li, Mr. Feng Jin, Dr. Slavko Mocevic, Mr. Cong Tu, Mr. Che-wei Chang, Mr. Xipei Yu, Mr. Gibong Son; and the co-workers in our group: Mr. Ruizhe Zhang, Dr. Jingcun Liu, Dr. Joseph Kozak, Mr. Boyan Wang, Mr. Yunwei Ma, Dr. Ming Xiao, Mr. Yifan Wang.

Special thanks to Mr. Haisong Deng, Ms. Xiaozhan Zhang, Mr. Xinran Li, Ms. Yulu Mao, Mr. Haowen Min, Mr. Yanbo Shi, Ms. Wansu Fang, Mr. Yijie Bai, Mr. Xiyuan Li, Mr. Jinhua Wang, and Ms. Yasang Shi for the enjoyment during my undergraduate and graduate years. They helped me through the tough days.

Finally, words cannot express my gratitude to my family for their love and support. They work hard and sacrifice a lot for me, paving the way for my life journey. They mean the world to me, but I don’t tell you enough.

Table of Contents

List of Figures

Chapter 1: Introduction to Cascode GaN HEMTs

1.1 Wide Bandgap Power Devices

In the past few decades, silicon technologies have enabled efficient power electronics in industrial and commercial applications, e.g., power grids, solar energy conversion, data centers, and consumer electronics. The innovation of silicon power metal-oxide-semiconductor field-effect transistors (Si MOSFET) in 1976 has stimulated the rapid development of power conversion systems. Being optimized for decades, Si MOSFETs have become the most popular candidates for power switches in various circuit topologies. Having approached the theoretical limits in recent years, Si power devices show their limit for further advancement of power electronics systems. With a prominent figure of merit, wide-bandgap (WBG) power devices were recently introduced, which are represented by silicon carbide (SiC) and gallium nitride (GaN) transistors. These WBG devices outperform Si devices and open the door for more efficient power conversion circuits. Fig. 1 compares the five vital electrical properties of Si and WBG materials, in which WBG materials show superior benefits. These features make WBG devices the next-generation power devices that

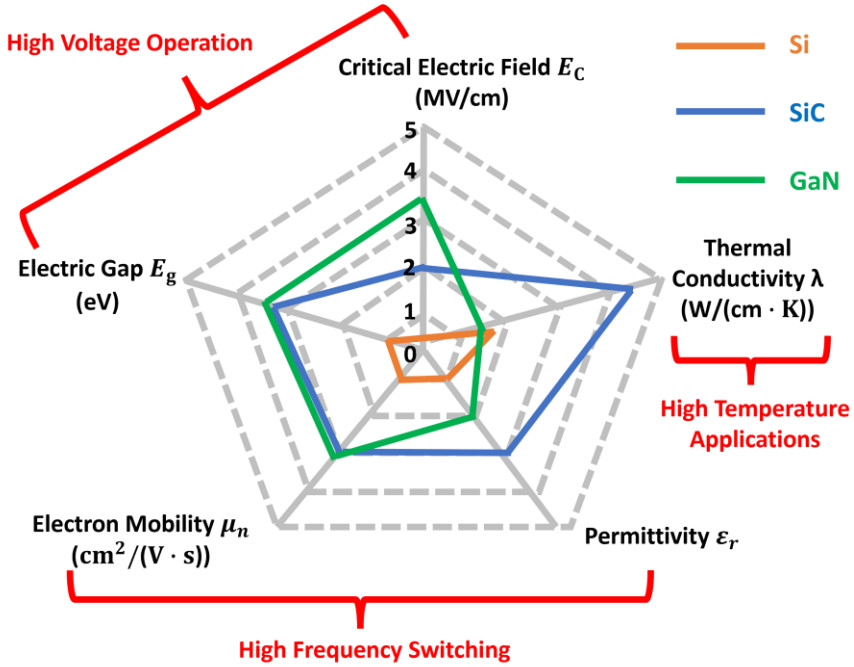

Figure 1. Capacity comparison of Si and WBG materials

enable high-voltage, high-frequency, and high-temperature power conversion [1]–[3], which will be reviewed in the following paragraphs.

The band gap (E_g) is the minimum amount of energy an electron needs to obtain to enter into a free state. A higher E_g usually means a lower density of intrinsic carrier density, allowing for a low leakage current and high operating temperatures. These also result in a higher critical electrical field (E_C) needed to initiate a device breakdown. Formula (1) estimates the breakdown voltage (BV) of a semiconductor layer (drift layer) based on the non-punch-through design [4]:

$$BV = 1/2 \cdot W_{drift} \cdot E_C \tag{1}$$

where W_{drift} is the width of the drift region. For WBG devices, the drift region can be ten times thinner than silicon devices for the same BV while accommodating a higher carrier density. Based on the non-punch-through design, the drift region is just fully depleted when the peak electric field (E-field) reaches E_C. In an N-type semiconductor, formula (2) calculates the doping concentration (N_D) for this design:

$$q \cdot N_D = \varepsilon_0 \cdot \varepsilon_r \cdot E_C \,/\, W_{drift} \tag{2}$$

The total charge, i.e., the product of the charge of the electron ($q = 1.6 \times 10^{-19}$coulombs) and the total number of donors (N_D) in the volume is dependent on E_C. ε_r represent the relative permittivity of material with respect to the vacuum permittivity (ε_0).

Formula (3) calculates the specific on-resistance $R_{DS(ON)}$ (resistance per unit area in $\Omega \cdot \mathrm{mm}^2$) in unipolar device:

$$R_{DS(ON)} = W_{drift}/(q \cdot \mu_D \cdot N_D) \tag{3}$$

where μ_D is the electron mobility. Then formula (4) [4], [5] builds upon a relationship between BV and $R_{DS(ON)}$, which are the two most vital design metrics for a power device:

$$R_{DS(ON)} = (4 \cdot BV^2)/(\varepsilon_0 \cdot \varepsilon_r \cdot \mu_D \cdot E_C^3) \tag{4}$$

Fig. 2 illustrates this relationship for Si, SiC, and GaN, showing that WBG devices have a higher theoretical limit than Si devices. Ideally, a power device with infinite BV and zero $R_{DS(ON)}$ is desirable. However, the real semiconductors are not ideal, and intrinsic material properties, i.e., ε_r, μ_D and E_C determine the ratio between BV and $R_{DS(ON)}$ limits. WBG devices can enable a

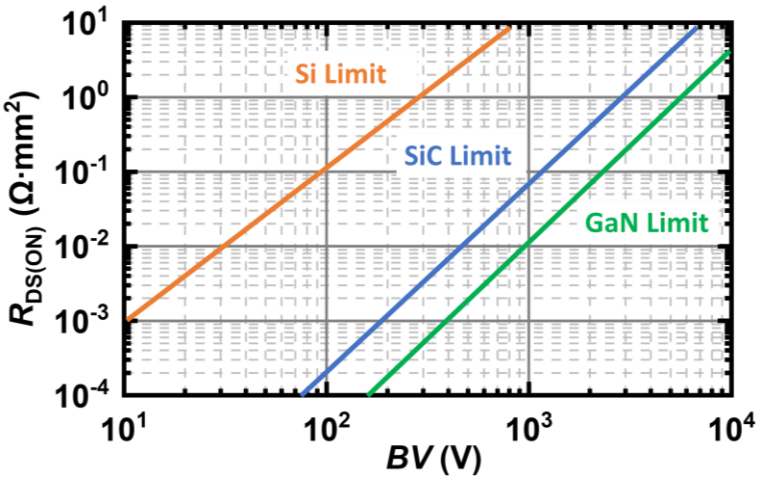

Figure 2. *BV* vs. specific $R_{DS(ON)}$ limits for Si and WBG-based power semiconductor devices

smaller specific $R_{DS(ON)}$ than Si devices. Hence, for the same $R_{DS(ON)}$ and current ratings, WBG devices allow for smaller chip sizes, smaller capacitances and charges, and smaller power losses. These device benefits can lead to higher efficiency and higher operating frequency in power electronics systems.

1.2 GaN HEMTs

When the aluminum gallium nitride layer (AlGaN) is grown on the GaN layer, an AlGaN/GaN heterojunction forms, with a strongly pronounced polarization property due to the wurtzite crystal structures. Two sources of polarization contribute to the total polarization in the AlGaN/GaN heterostructures: spontaneous polarization (P_{SP}) and piezoelectric polarization (P_{PE}). P_{SP} refers to the built-in polarization field in an unstrained field, while P_{SE} refers to the polarization field resulting from crystal lattice distortions. Since the polarization charges generated in the AlGaN are much higher than that in GaN, net positive charges accumulate in the interface, which produces 2DEG (Fig. 3) [6]–[8].

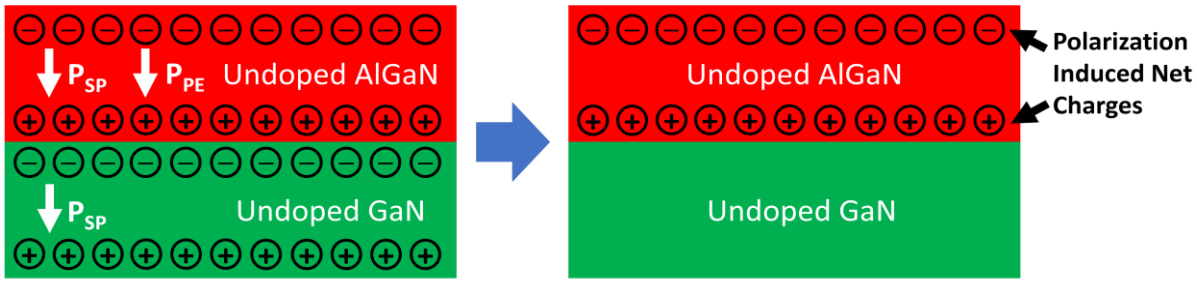

Figure 3. Formation of the 2DEG channel due to the polarization charges in AlGaN/GaN heterostructures

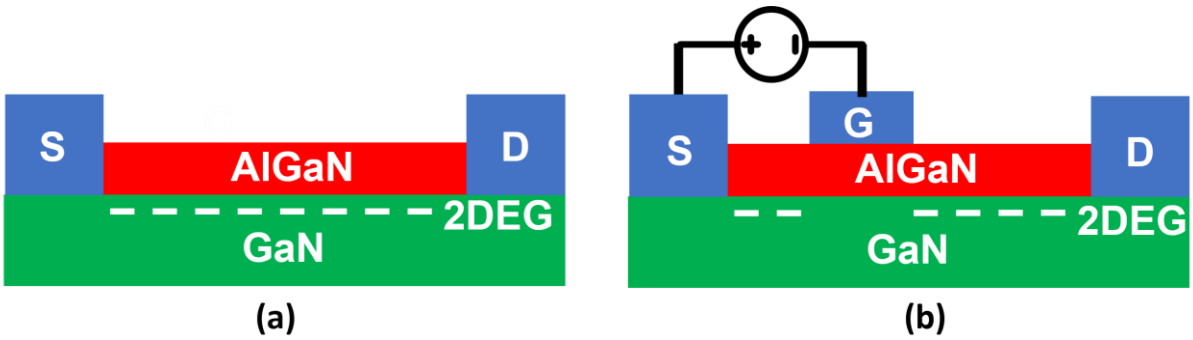

Figure 4. A basic structure of a D-mode GaN HEMT

The 2DEG can accommodate electrons to flow fast and efficiently when a lateral E-field is applied between source and drain. At the interface, electrons are confined in a quantum well, which increases the mobility of electrons up to 1500 – 2000 $cm^2/(V \cdot s)$, as shown in Fig. 4(a). Then, by adding a gate electrode on the top of the AlGaN, a GaN HEMT forms Fig. 4(b). Due to the nature of 2DEG, GaN HEMT is normally-on, which usually refers to a depletion-mode (D-mode) device. However, a normally-off device, which refers to an enhancement-mode (E-mode) device, is more preferred in applications from safety considerations. Several popular architectures have been adopted to realize E-mode operation based on a D-mode GaN HEMT, falling into two categories: composite and standalone [9], [10].

Standalone E-mode GaN HEMTs can achieve the E-mode operation by engineering the gate structures. For example, the recessed gate structure is made by thinning the AlGaN layer underneath the gate metal, leading to reduced polarization charges and piezoelectric E-field. 2DEG density decreases accordingly, inducing a higher threshold voltage (V_{th}) larger than zero, thus enabling the E-mode operation [11], [12]. Commercially-available E-mode GaN HEMTs adopt p-GaN gated structures. As shown in Fig. 5(a), a P-gate GaN HEMT is made by adding a P-type GaN layer under the gate electrode. The p-GaN gate can deplete the 2DEG below the gate, leading to a normally-off operation. In some p-gate GaN HEMTs, e.g., a mixed-drain gate-injection transistor (GIT), as shown in Fig. 5(b), another P-GaN can also be connected to the drain, acting as a hole injector to de-trap the electron trapping in the buffer region. This could improve the reliability of the P-gate GaN HEMT [15].

Connecting a low-voltage E-mode Si MOSFET with a D-mode GaN HEMT in series, a composite E-mode GaN HEMT can also ensure the normally-off safety. For instance, in a "cascode" GaN HEMT, a low-voltage E-mode Si MOSFET chip controls the gate-to-source

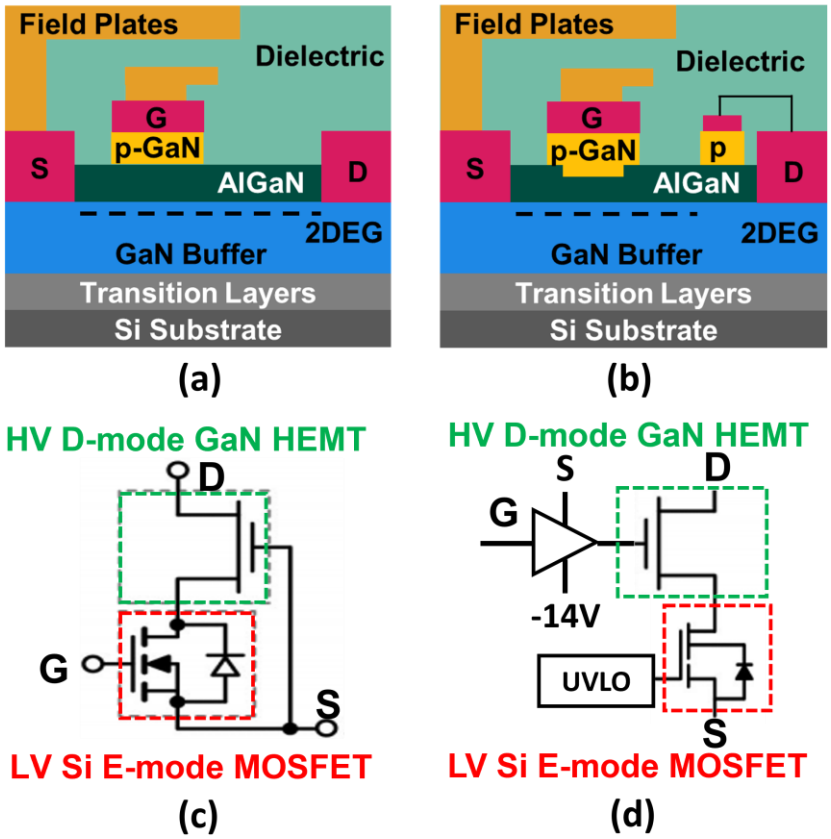

Figure 5. Various structures of commercially available GaN HEMTs.

voltage (V_{GS}) of the D-mode GaN HEMT (Fig. 5(c)) [14]. The entire cascode GaN HEMT can switch by controlling the gate of the Si device: when a positive voltage bias applies to the Si device gate, the V_{GS} of the D-mode GaN HEMT goes to zero and turns on. Current flows through the series-connected D-mode GaN HEMT and Si MOSFET; if the gate bias on the Si MOSFET gate is removed, a negative V_{GS} builds upon the D-mode GaN HEMT, turning the entire cascode GaN HEMT off. With an idea similar to the cascode structure, "direct-drive" devices have also been commercialized recently (Fig. 5(d)), which also consists of a low-voltage E-mode Si MOSFET and a high-voltage D-mode GaN HEMT. Instead of controlling the gate of the Si device, the gate of the GaN HEMT is directly driven by an integrated gate driver. The Si MOSFET ensures the normally-off operation but always turns on during the switching events. The gate driver generates zero/negative voltage bias to turn the D-mode GaN HEMT on/off [15].

1.3 Cascode GaN HEMT

As mentioned in section 1.2, a cascode GaN HEMT is a composite GaN device containing a low-voltage E-mode Si MOSFET and a high-voltage D-mode GaN HEMT (Fig. 5(c)). Besides normally-off operation, a cascode structure brings several benefits. First, the gate is possibly more robust than the p-gate, as the gate of a cascode GaN HEMT is the gate of the Si MOSFET, which has been heavily studied and verified. The Si MOS gate can sustain a much broader voltage switching, e.g., -20 V to 20V [16], while the p-gate can usually only accommodate -10 V to +7 V [17]. Also, the MOS gate usually has a higher threshold voltage (V_{th}) than the p-gate GaN HEMT, e.g., 4 V versus 1.7 V [16], [17]. Therefore, regular Si gate drivers can drive cascode GaN HEMTs, and the potential false turn-on issues on the p-gate GaN HEMT can be eliminated.

However, the complexity of the cascode structure brings several challenges and undesired features. For example, the co-packaging of the Si and GaN chips needs to be optimized to achieve stable operation by minimizing the parasitics between the two chips [18]. Unlike other standalone GaN HEMTs, due to the Si MOSFET, the reverse recovery occurs in a cascode GaN HEMT. Also, the slew rate of cascode GaN HEMT is not adjustable, given that the GaN HEMT is connected to the MOSFET source. The total output capacitance of the device is higher than the standalone GaN HEMT due to the multiple devices [15].

Besides these intrinsic drawbacks brought the cascode structure, some other unique reliability issues have been reported in cascode GaN HEMTs caused by the crosstalk and interconnections between the Si and GaN devices. For example, under other switching conditions, the internal switching loss [19], divergent oscillation [20], false turn-on [21], and short-circuit oscillation [22] are threatening the safety operation of the cascode GaN HEMTs. Therefore, it requires more studies to improve the reliability and robustness of the cascode GaN HEMT devices.

In this chapter, an overview of commercial GaN HEMTs is presented. It is also worth noting that many emerging GaN devices are being actively developed to expand the application space of GaN power device technologies. Many of these GaN device technologies are recently reviewed in [10]. For example, 3-D FinFET and tri-gate architectures are being adopted in GaN transistors [23], [24]. Various 1.2 kV class vertical GaN devices have been demonstrated on GaN and foreign substrates [25], [26] by academia and industry, with the state-of-the-art performance surpassing 1.2 kV SiC MOSFETs [27]–[29]. Remarkably, some vertical GaN diodes and transistors have

demonstrated excellent avalanche [30]–[34] and short-circuit [34]–[36] robustness. On the horizon, lateral GaN devices can also be developed on a multi-channel structure with vertically-stacked AlGaN/GaN heterostructures. This multi-channel platform allows for a much smaller specific on-resistance and is suitable for high-voltage devices. Multi-channel lateral GaN Schottky rectifiers have been demonstrated with the performance surpassing the 1-D SiC limit at the voltage class of 3.3 kV [37], 5 kV [38], and up to 10 kV [39]. 10-kV class E-mode GaN HEMTs were also demonstrated recently on the multi-channel platform with a specific $R_{ds(on)}$ 2.5-fold lower than 10 kV SiC MOSFETs [12]. This progress of emerging GaN devices shows GaN power technology's great promise.

Chapter 2: Introduction to Surge-energy and Overvoltage Robustness

2.1 Surge Energy in Power Electronics Systems

Power electronics systems are affected by environment and equipment-related abnormal events that cause transient surge events [40]. Power semiconductor devices are connected in series with an inductive load or stray inductance in the circuits. The abrupt change of the current in inductors may deliver surge energy to the devices. Therefore, good surge-energy robustness of power devices, through which the device can absorb, dissipate or withstand the surge energy, is highly desirable in many power applications, such as motor drives, electricity grids, and powertrains [41]. The traditional evaluation of surge-energy robustness is based upon the avalanche capability, as many Si and SiC devices have the avalanche capability to absorb and dissipate the surge energy. However, GaN HEMTs have no or very limited avalanche capability. Thus, the surge robustness of GaN HEMTs remains a critical knowledge gap, which will be probed in this work.

2.2 Unclamped Inductive Switching (UIS) Test

The surge-energy test is typically characterized by the unclamped inductive switching (UIS) test. Fig. 6 shows the schematic of a UIS circuit. A power supply (V_{DD}) is in serial connection with a load inductor (L_{load}) and the device under test (DUT). A bus capacitor C is used to stabilize the voltage supplied by V_{DD}. The L_{load} resembles the component that stores surge energy in power converters. The test contains two stages: first, the DUT is turned on, and the V_{DD} charges the L_{load}; Then, the DUT is turned off when the inductor current reaches the desired value, and the surge energy stored in L_{load} will be forced to go through the off-state DUT. The UIS has become a widely-

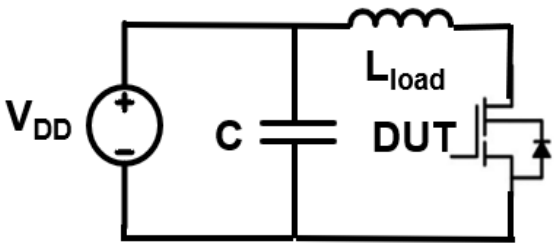

Figure 6. Scematic of a UIS circuit.

used, standard test method for Si and SiC devices to evaluate their avalanche capability. It is also referred to as the avalanche test in many contexts.

2.3 Withstanding Mechanism of Si and GaN Devices

GaN HEMTs have different withstanding mechanisms from the Si MOSFET [42]. Fig. 7 illustrates the UIS waveforms of Si MOSFET and GaN HEMT. For Si MOSFET, the drain-to-source voltage (V_{DS}) quickly ramps up to the avalanche breakdown voltage (BV_{AVA}) and clamps at BV_{AVA}. The drain-to-source current (I_{DS}) gradually shrinks to zero, along with the device's resistive dissipation of surge energy. The avalanche energy (E_{AVA}), as illustrated by the grey area in Fig. 7(a), is the integral of the product of V_{DS} and I_{DS} through the avalanche period (t_{AVA}). E_{AVA} is an essential parameter for Si MOSFET, representing the device's intrinsic capability to withstand the surge energy safely. The E_{AVA} is usually thermally limited for Si and SiC devices [43]. The ruggedness of Si MOSFET under repetitive UIS stresses has been extensively reported in [44].

In contrast, owing to the lack of p-n junctions between source and drain, GaN HEMTs have no avalanche capabilities and were recently found to withstand the surge energy through capacitive charging [42], [45]–[50]. As shown in Fig. 7(b), resonance occurs between the device output capacitance and load inductance with minimal energy dissipation in the GaN HEMT [42], [45]. After a half cycle of resonance, the device turns on reversely. During the resonant withstanding process, the GaN HEMT fails when the peak resonant V_{DS} reaches the device's dynamic breakdown voltage [42], [45]. In two types of p-gate GaN HEMTs, this dynamic BV was found to depend on

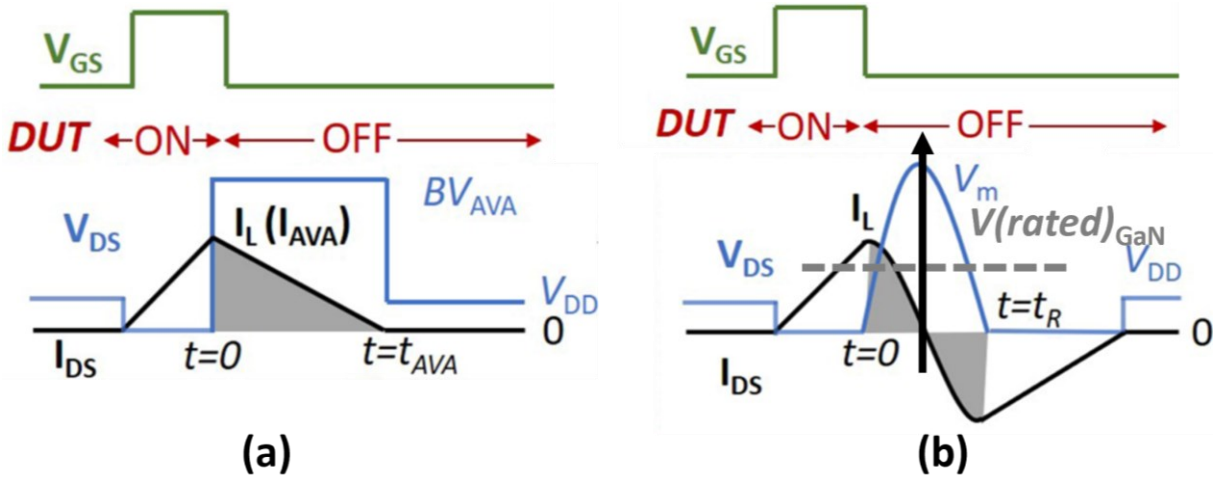

Figure 7. Illustration of UIS waveforms of (a) Si and (b) GaN devices

the resonance duration [46], and generally higher than the device static BV measured on a curve tracer [46]–[49]. [42] has concluded that the p-gate GaN HEMTs rely on their overvoltage capability to withstand the surge energy. As demonstrated in Fig. 7(b), the BV of the p-gate GaN HEMTs is always designed to be much higher than the devices' rated voltage to ensure surge-energy robustness, even in high-frequency converters at MHz [51]. [47], [48] has illustrated that the p-gate GaN HEMTs are robust under repetitive overvoltage events below the devices' BV. With the peak V_{DS} of 1050 V (90% of the destruction limit), 600-V, 31-A rated GIT shows no failure or permanent degradations after 1-million overvoltage events at different periods or elevated temperatures [48]. Also, similarly-rated Schottky-type p-gate GaN HEMT exhibits recoverable parametric shifts after 1-million overvoltage pulses. With the peak V_{DS} of 1330 V (95% of the dynamic BV), the p-gate GaN HEMT shows small V_{th} and $R_{DS(ON)}$ reductions. For GIT and Schottky-type p-gate HEMT, these shifts show saturation and are attributable to the trapping of holes produced in impact ionization (I. I.). The GIT shows a faster natural recovery than the Schottky-type HEMT, which benefits from the efficient hole removal through the Ohmic gate. The hole-detrapping in the Schottky-type p-gate HEMT can be modeled by the Poole-Frenkel emission, allowing for accelerated recoveries at negative V_{GS} and high temperatures [52].

[53], [54] have studied the overvoltage robustness of a metal-insulator-semiconductor HEMT (MIS-HEMT), the D-mode GaN HEMT in the composite GaN devices, e.g., cascode and direct-drive. Similar to the p-gate GaN HEMTs, MIS-HEMT is robust under overvoltage stresses close to BV. Switched at V_{DS} of 90% BV, the device shows recoverable shifts in V_{th}, $R_{DS(ON)}$, and saturation current ($I_{DS(SAT)}$). Unlike p-gate GaN HEMTs, the MIS-HEMT can hardly fully recover naturally, e.g., at room temperature with no voltage bias, believable due to the MIS gate structure. The I. I. generated holes can be removed through the p-gate, while the MIS gate structure blocks the hole-removal path. A positive V_{GS} and substrate bias can efficiently recover the device by facilitating the hole recombination in the 2DEG channel [53].

However, the surge-energy/overvoltage robustness of the composite GaN power device, represented by the cascode GaN HEMT, has not been comprehensively studied. Implemented in a cascode structure, the MIS-HEMT may show different behavior under overvoltage stresses due to the composite structure, e.g., the parasitics brought by the interconnections [18], [21] and Si avalanche issue [19]. Recently, the authors reported the first study into the single-event and repetitive UIS withstanding process and failure mechanisms of the cascode GaN HEMT [55], [56],

which were quite distinct from those of p-gate GaN HEMTs. This study is an extension of [55] and [56], trying to investigate 1) single-event UIS studies at elevated temperatures, 2) the correlation between the device failure under single-event and repetitive UIS stresses, 3) physics-based simulation and an analytical model regarding the UIS withstand process and failure mechanisms. These unknowns serve as the motivation for this work.

Chapter 3: Single-event Robustness of Cascode GaN HEMTs

3.1 Test Setup

The DUT in this work is commercial 650-V, 50-mΩ rated cascode GaN HEMTs in a TO-247 package [16]. Fig. 8(a) shows a photo of a decapsulated device and its cross-sectional schematic. A vertical Si MOSFET stacks onto a lateral GaN HEMT. The drain pad of the Si MOSFET is electrically connected to the source pad of the GaN HEMT. The BV_{AVA} of the Si MOSFET was measured to be 35 V, and the V_{th} of the GaN HEMT was -17 V.

Fig. 8(b) shows the schematic of the UIS test circuit for the cascode GaN HEMT. A 30-V power supply (V_{DD}) was in series with a load inductor and the DUT. A series of bus capacitors were connected in parallel with V_{DD} to stabilize the supply voltage. Three load inductors of

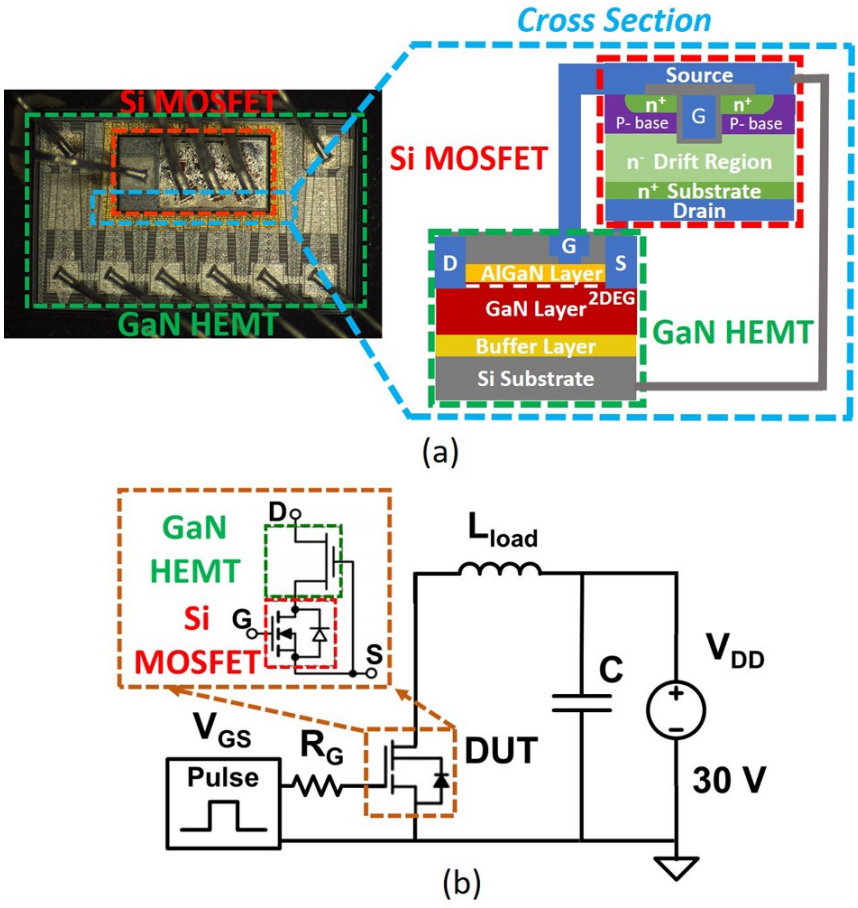

Figure 8. (a) Photo of a decapsulated cascode GaN HEMT and its structure. (b) schematics of the DUT and the UIS test setup.

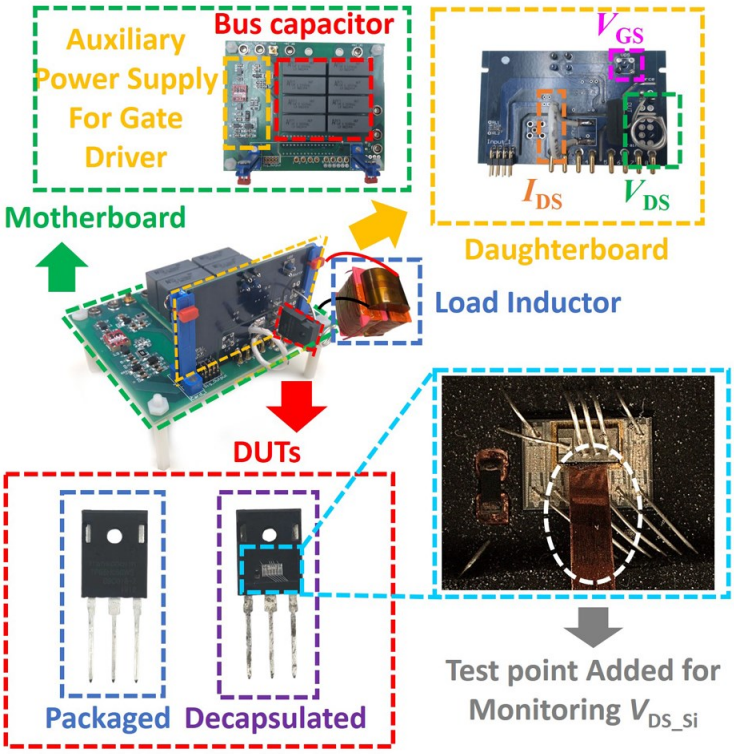

Figure 9. Photo of the UIS test setup

different inductance, i.e., 20 μH, 100 μH, and 1 mH, were used in the UIS tests. Over 30 DUTs were tested in the single-event UIS tests at 25 °C and 150 °C, and another 40 DUTs in the repetitive UIS tests. Fig. 9 shows the photo of the experimental UIS test setup. Similar to [42], the setup comprises a motherboard and a daughterboard. The motherboard contains the main power loop, bus capacitors, and input signals. The daughterboard contains the DUT and test points.

The waveforms of V_{GS}, V_{DS}, and I_{DS} of the DUT are monitored on the daughterboard. To fully understand the behaviors of Si MOSFET and GaN HEMT in the UIS test, the fresh packaged devices and the decapsulated devices with an extra test point were tested in the UIS circuit. As shown in Fig. 9, in the decapsulated DUT, an extra test point was added onto the drain pad of the Si MOSFET (also the source pad of the GaN HEMT). This decapsulated DUT was fabricated by immersing the packaged device in a mixture of hot fuming nitric acid and sulfuric acid (HNO_3:H_2SO4 = 1:2). Then hydrochloric (HCl) was applied to dissolve the original interconnection between the Si MOSFET and GaN HEMT. A thin piece of the copper band was finally placed between these two devices by reflow soldering. This test point enables monitoring

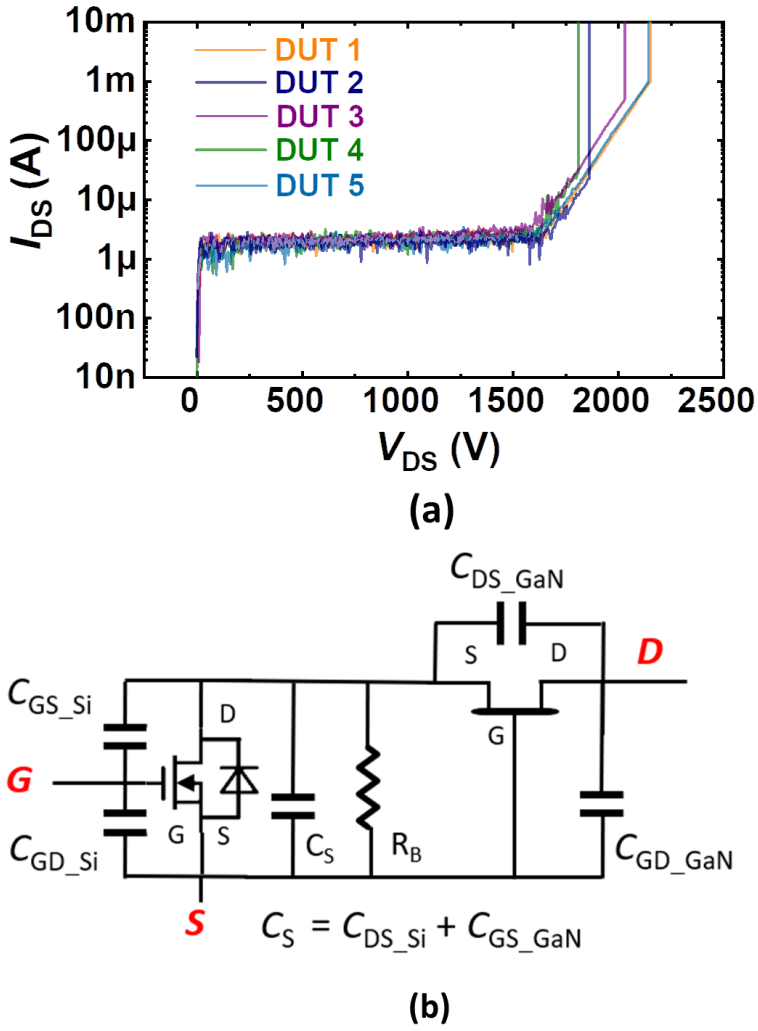

Figure 10. (a) OFF-state *I-V* characteristics of 5 DUTs on a curve tracer. (b) Equivalent circuit model of the DUT.

of the Si MOSFET's V_{DS} in the UIS test, which provides direct information regarding the Si avalanche.

3.2 Static Breakdown Voltage

Fig. 10(a) shows the OFF-state I-V characteristics of 5 DUTs measured on a curve tracer (Keysight B1505 Semiconductor Analyzer) at 25 °C. The DUTs show a destructive BV ranging from 1820 V to 2200 V. At V_{DS} < 1.6 kV, the OFF-state leakage current (I_{DSS}) was clamped at 2.2 µA. According to [57], a ~10-MΩ resistor (R_B) is in parallel with the Si MOSFET to balance the leakage current between the Si MOSFET and GaN HEMT (Fig. 10(b)). Assuming most of 2.2 µA goes through R_B, the maximum V_{DS} of the Si MOSFET is ~22 V, which is smaller than the BV_{AVA}

of the Si MOSFET. At V_{DS} > 1.6 kV, the increased leakage current in the GaN HEMT requires additional leakage current from the Si MOSFET to balance, which will drive the V_{DS} of the Si MOSFET to approach its BV_{AVA}.

Note that, under the DC voltage blocking conditions (e.g., curve tracer measurements), the voltage distribution between the Si MOSFET and GaN HEMT is governed by the leakage current matching. By contrast, under switching conditions, the voltage distribution is governed by the output capacitance of the two devices, which may lead to the Si avalanche at a much lower V_{DS}. This will be illustrated in the next section. According to [57], R_B can be ignored in switching operations, as the time constant associated with R_B is too large to come into play.

3.3 Single-event UIS Tests

3.3.1 *Safe-withstanding*

Fig. 11(a) shows a typical DUT safe-withstanding waveform in the UIS test with a 100-μH load inductor. Six distinct phases have been identified in the waveform:

(a) *Phase I*: The DUT is in ON-state, and V_{DD} charges the inductor until the inductor current reaches the desired value.

(b) *Phase II*: The Si MOSFET is turned OFF. V_{DS} of the Si MOSFET builds up until reaching the GaN HEMT's $|V_{TH}|$.

(c) *Phase III*: A L-C resonance occurs between the load inductance (L_{load}) and the DUT's equivalent output capacitance (C_{OSS}). As shown in Fig. 11(b), the DUT's C_{OSS} during this phase (C_{OSS_1}) can be written as

$$C_{OSS\_1} = \frac{C_{DS\_GaN} \times (C_{GS\_Si} + C_{DS\_Si} + C_{GD\_Si})}{C_{DS\_GaN} + C_{GS\_Si} + C_{DS\_Si} + C_{GD\_Si}} + C_{GD\_GaN} \quad (5)$$

(d) *Phase IV*: When the DUT's V_{DS} exceeds ~200 V, the Si MOSFET avalanches and its V_{DS} clamps at BV_{AVA} (~35 V). This results in a change in the resonance period due to the increase in the DUT's C_{OSS}. In this phase, the resonance is no longer lossless; it is accompanied by the resistive energy loss in the Si MOSFET avalanche. The DUT's C_{OSS} in this phase (C_{OSS_2}) equals to the GaN HEMT's C_{OSS} (Fig. 11(c)).

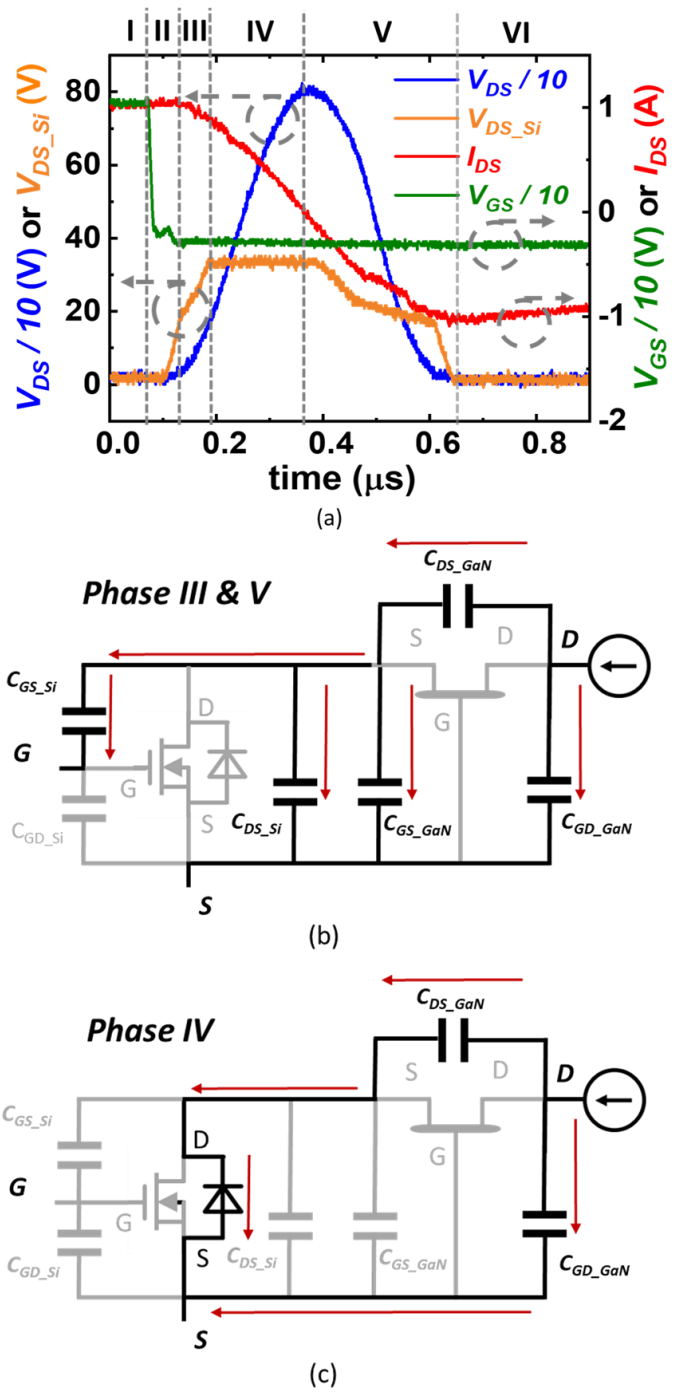

Figure 11. (a) Safe-withstanding waveforms of Cascode GaN HEMT in UIS test. Equivalent circuit model in (b) phase III and V and (c) phase IV.

$$C_{OSS\_2} = C_{OSS\_GaN} = C_{DS\_GaN} + C_{GD\_GaN} \tag{6}$$

(e) *Phase V*: The avalanche stops when I_{DS} reduces to zero. The circuit returns to the lossless *L-C* resonance, and I_{DS} is purely capacitive. The DUT's C_{OSS} returns to C_{OSS_1}.

(f) *Phase VI*: Most of the energy has transferred from the DUT's C_{OSS} to the load inductor. Soon after V_{DS} changes its polarity, the DUT turns on reversely, and the load inductor is discharged by V_{DD}.

3.3.2 *Failure Mode I*

Fig. 12(a) shows a typical DUT failure waveform with a 20 μH load inductor. The current-voltage (I-V) measurements between the DUT pins reveal a short connection between the cascode drain and source (~1 Ω resistance), implying a short between the HEMT gate and drain. This is consistent with the failure after the device static breakdown measured on the curve tracer and the reports by the device vendor [58].

The source and gate of the Si MOSFET were measured to be open, indicating an intact MOS gate. As shown in Fig. 12(b), a test circuit was designed to evaluate the health condition of the Si MOSFET. In the circuit schematic, the HEMT gate-to-drain path is represented by a short resistance (R_{short}) of 1 Ω. A 3-Ω power resistor (R_{series}) was connected in series with the failed DUT and a power supply that outputs 10-V DC voltage. A function generator controls the gate of the failed DUT. If the Si MOSFET failed, I_{DS} should show no dependence on the gate signal applied to the Si MOSFET. Otherwise, when the Si MOSFET turns ON, R_{short} is expected to be bypassed by the $R_{DS(ON)}$ of the Si MOSFET, as $R_{DS(ON)}$ is much smaller than 1 Ω. As a result, different I_{DS} are expected when the Si MOSFET is ON and OFF, which are given by

$$I_{DS-ON} = \frac{V_{DD}}{R_{series}+R_{DS\,(on)\_Si}} \cong 3.3\ A \tag{7}$$

$$I_{DS-OFF} = \frac{V_{DD}}{R_{series}+R_{short}} \cong 2.5\ A \tag{8}$$

Fig. 12(c) shows the testing waveform of the failed cascode device, revealing an over 0.3-A difference when the Si MOSFET is ON and OFF. This current difference is smaller than the expected value due to the unstable $R_{DS(ON)}$ of the failed HEMT. Nevertheless, the difference in I_{DS-ON} and I_{DS-OFF} suggests the intact Si MOSFET and confirms the drain-to-gate short failure in the GaN HEMT.

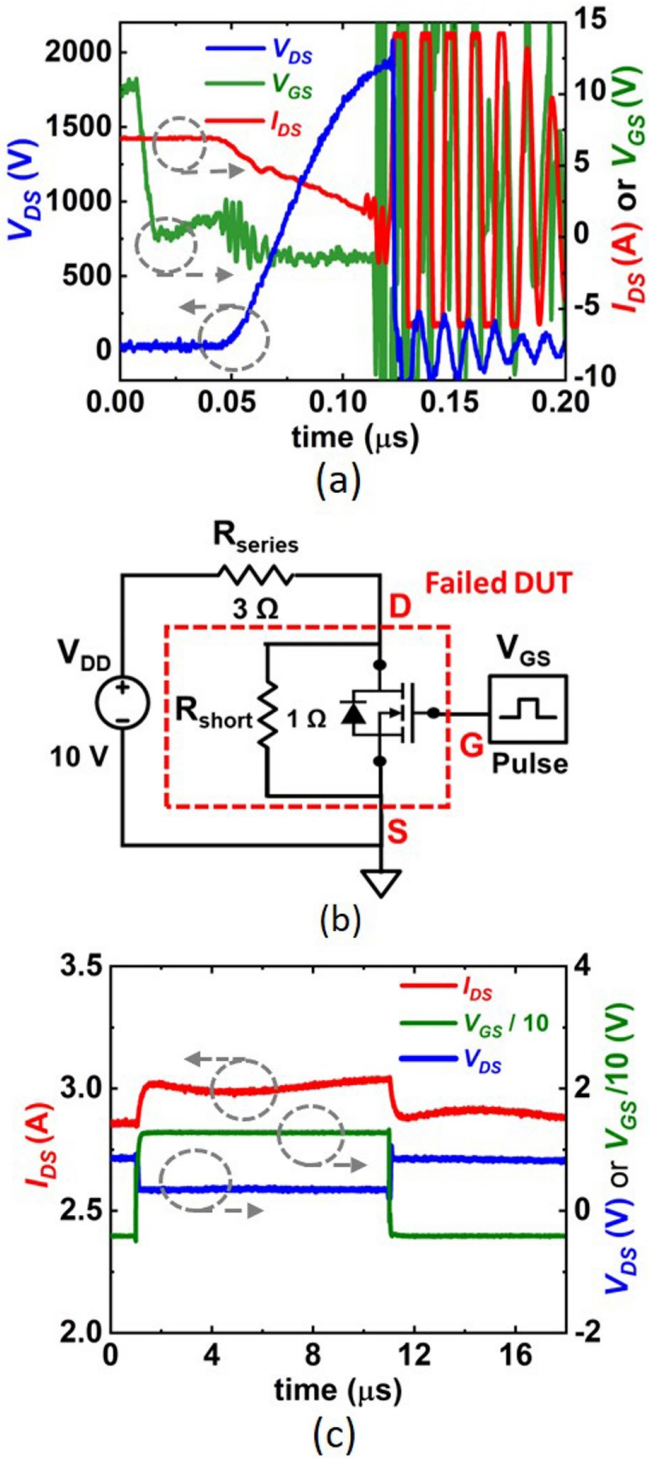

Figure 12. (a) The waveform of failure mode I (b) Test circuit for the failed DUT. (c) Test waveform of the failed DUT.

3.3.3 *Failure Mode II*

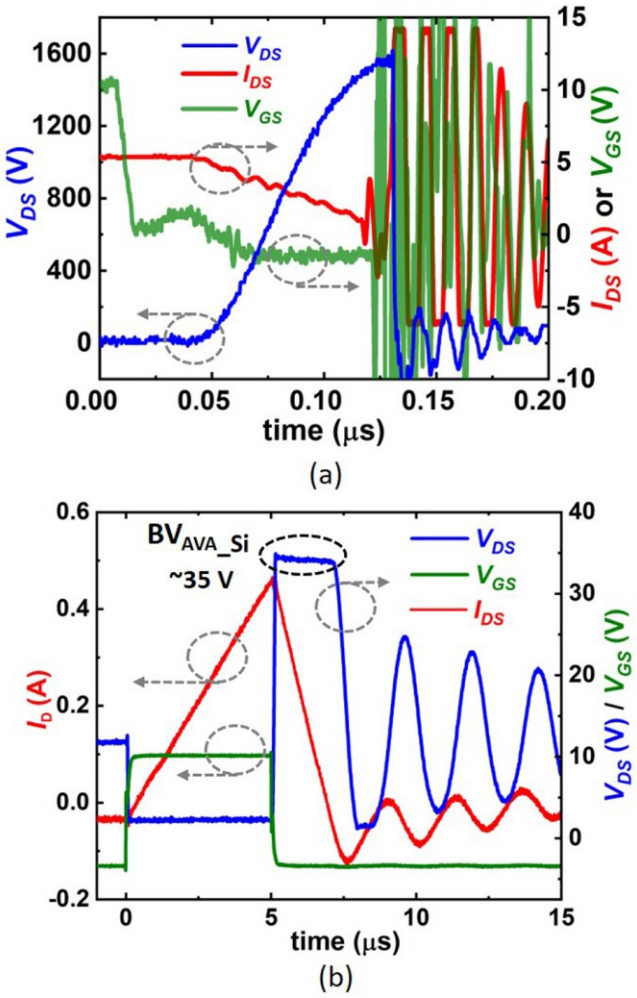

Figure 13. (a) The waveform of failure mode II. (b) The UIS waveform of the failed DUT.

Under the same load inductance (20 μH), some DUTs were found to fail with a different failure mode. Fig. 13(a) shows a typical DUT failure waveform in which the DUT fails at 1618 V, a voltage much lower than the DUT's static *BV*. In addition to exhibiting lower failure voltages, the DUTs that failed in mode II were found to function as a standalone Si MOSFET with avalanche capability. Fig. 13(b) shows the UIS test of the failed DUT, revealing a BV_{AVA} of 35 V, i.e., the Si MOSFET's BV_{AVA}. This suggests a short between the GaN HEMT's drain and source while its gate and drain remain open.

3.3.4 *Dependence on Load Inductance and Temperatures*

30 DUTs were tested for failure under three different load inductances and at 25 °C and 150 °C. Note that the *L*-*C* resonance period increases with a larger load inductance and the inductor

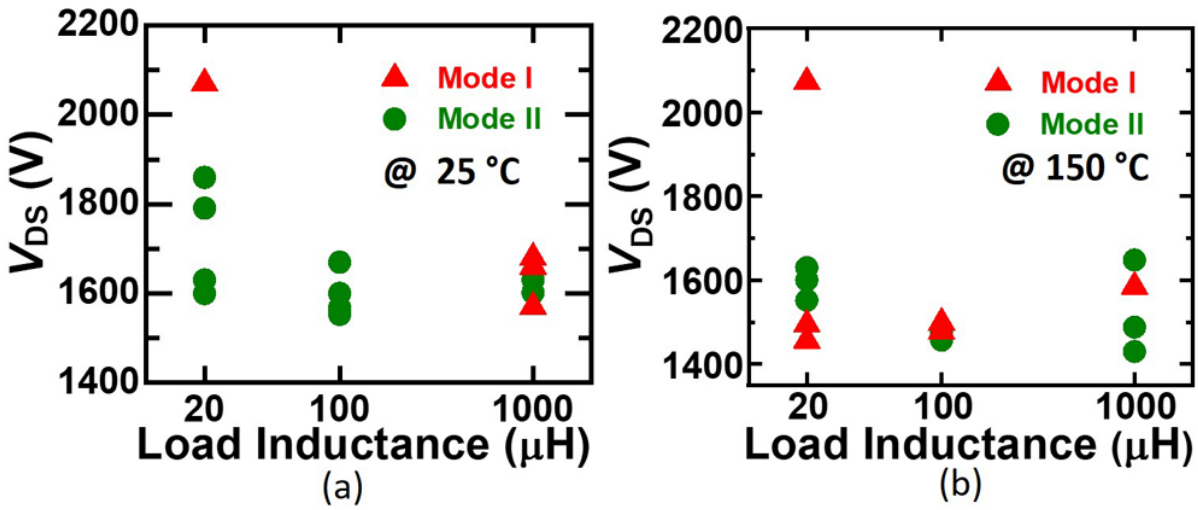

Figure 14. The DUT's breakdown voltage in the UIS tests under different load inductances and at two temperatures.

turn-off current (I_{OFF}) that drives the DUT into failure decreases [42]. Fig. 14(a) and (b) summarize the failure modes and failure voltages of 30 DUTs tested at 25 °C and 150 °C, respectively. Here the failure modes are determined by the blocking voltage of the failed DUT (i.e., 35 V or 0 V).

Three findings can be deduced from the statistical results: (a) the failure voltage of most DUTs (1400~1650 V) is lower than the DUT's static *BV* (1800~2200 V); (b) mode II generally dominates; (c) the failure voltages in both modes show a relatively large spread; they exhibit no statistically significant dependence on the load inductance but are statistically lower at 150 °C than at 25 °C. For example, the lower bound of the DUTs' failure voltages is ~1.5 kV at 25 °C and ~1.4 kV at 150 °C.

3.3.5 *Failure Analysis*

Two DUTs were decapsulated: one failed at 2080 V in mode I and the other at ~1500 V in mode II. The optical microscopic inspection and the Optical Beam Induced Resistance Change (OBIRCH) were used to locate the failure spots, followed by the cross-sectional microscopic imaging using the Scanning Electron Microscopy (SEM) and Focused Ion Beam (FIB).

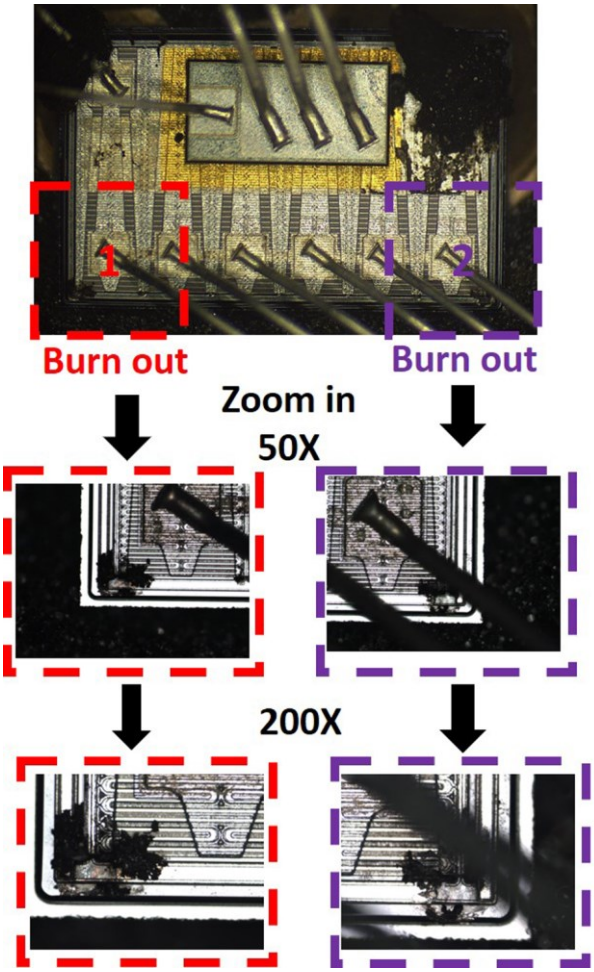

Figure 15. Microscopic images of the decapsulated DUT failed at 2080 V with failure mode I, revealing a failure at HEMT edge termination region.

Fig. 15 shows the microscopic image of the decapped DUT failed in mode I at 2080 V. The failure locations are in the edge-termination region of the GaN HEMT, consolidating a failure mechanism similar to that of the static breakdown due to high voltage and high E-field.

Fig. 16(a) shows the microscopic image of the decapped DUT failed in mode II at ~1500 V, showing no burning traces or noticeable destruction on the exposed surface of the Si and GaN chips. The OBIRCH was then used, in which the optical beam scanned the decapped DUT, and the induced optoelectrical current was mapped across the sample. As a secondary effect, the beam-induced local heating magnified the local resistivity changes at the destructive spot.

Fig. 16(b) shows the identified emission site on the decapped DUT, suggesting that the failure spot is in the region where the Si chip stacks on the GaN HEMT chip. Since no destruction traces are present on the surface, the Si chip was spalled from the GaN chip by the HCl acid, which only dissolved the metal pad but incurred no damage to GaN. After spalling, clear destruction spots were observed on the surface of the GaN chip in the scanning electron microscope (SEM) characterization. No destruction spots were observed in the Si chip. A FIB cut was performed to obtain the cross-sectional SEM at the failure spot of the GaN HEMT, as shown in Fig. 16(c). Local burning traces are present at the drain, and cracks are shown in the field plate dielectric, extending into the GaN buffer layers and reaching the transition layers above the Si substrate.

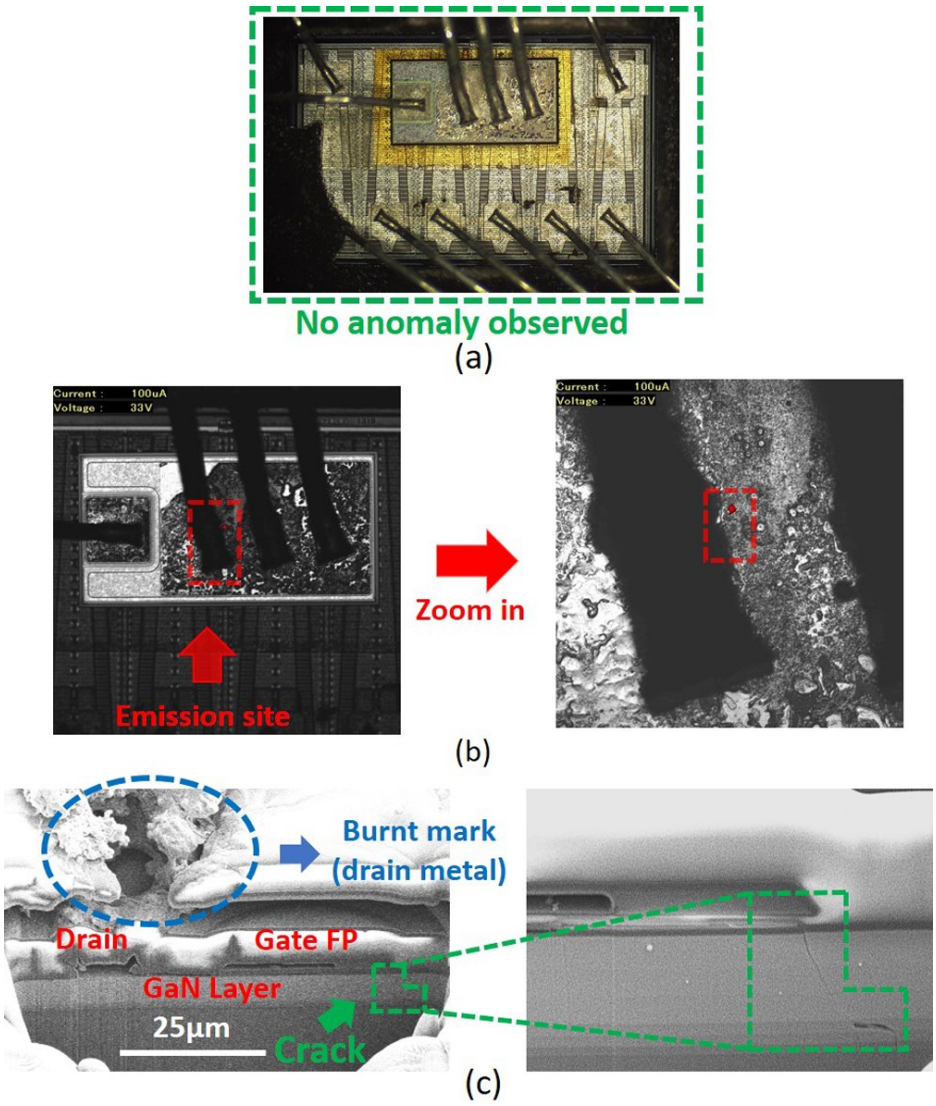

Figure 16. (a) Microscopic images of the decapsulated DUT that failed at ~1500 V with failure mode II. (b) OBIRCH image showing an emission site buried below the Si MOSFET. (c) Cross-sectional SEM image of the HEMT channel region at the failure spot.

Chapter 4: Physical Explanation and Simulation

4.1 Physical Explanation

Recently, it was found that the filled acceptor-like traps in the buffer region of a GaN HEMT can re-shape the electrical field (E-field) distribution and increase the peak E-filed in GaN at the same V_{DS}. As a result, the GaN HEMT's BV decreases with the increased buffer trapping, i.e., the dynamic BV phenomenon [46]. The cascode's much lower failure voltages in mode II than its static BV could be explained by the increased buffer trapping in the GaN HEMT.

In a standalone GaN HEMT, the dynamic BV in a short UIS pulse is usually higher than the static BV due to the reduced buffer trapping in a short pulse [46]. By contrast, increased buffer

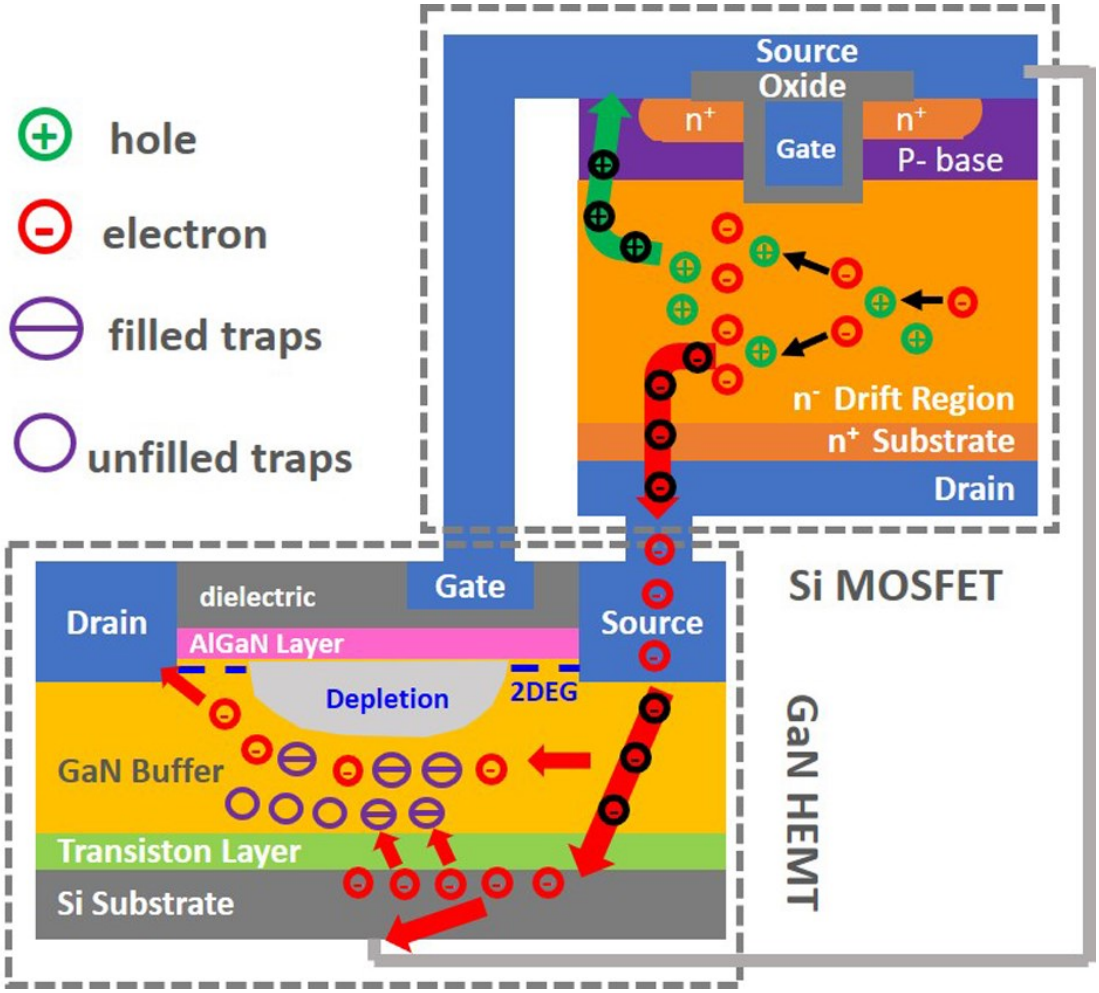

Figure 17. Illustration of the electron and hole dynamics during the capacitive voltage sharing process.

trapping is believed to occur in the cascode GaN HEMT during the short UIS pulse compared to the trapping during the static I-V sweep. This discrepancy could be correlated to the Si MOSFET avalanche, i.e., the phase IV, as shown in Fig. 11(a). It is the major difference between the UIS withstanding process of a cascode HEMT and that of a p-gate GaN HEMT.

As illustrated in Fig. 17, the holes produced during the Si avalanche leave the Si MOSFET via its source. The electrons produced in the avalanche are pumped to the drain of Si MOSFET by the V_{DS} of the Si MOSFET. As the Si chip stacks on the GaN HEMT chip and no external wires are connected to the drain of the Si MOSFET, the majority of these avalanche-produced electrons are expected to be injected into the source of the GaN HEMT and subsequently pushed towards the Si substrate. Some of these electrons will recombine in the p^+-doped Si substrate, and some finally flow back to the source of the Si MOSFET through external interconnects in the packaging to

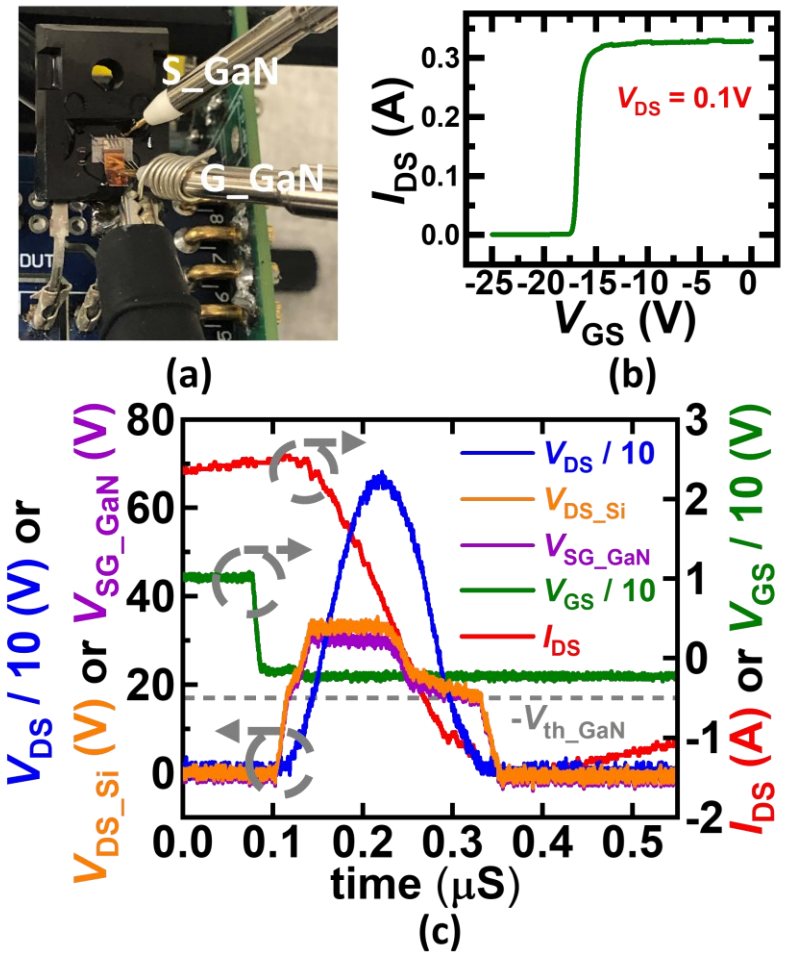

Figure 18. (a) Photo of the measurement setup of the GaN HEMT's V_{GS}. (b) Transfer characteristics of the D-mode GaN HEMT. (c) UIS waveforms of the cascode V_{DS}, V_{GS}, and I_{DS}, the Si MOSFET's V_{DS}, and the GaN HEMT's V_{SG}.

annihilate with holes. Note that some industrial papers have explicitly shown the common connection of the GaN HEMT substrate to the cascode's source [59].

When these avalanche-generated electrons travel through the GaN buffer and transitional layers, some may be pushed into the GaN buffer by the high V_{DS} of the GaN HEMT. When they reach the p-type Si substrate, some may aggregate and laterally transport along with the interface between the Si substrate and transitional layers and be further injected into the GaN buffer [46], [60], [61]. These two paths both favor the GaN buffer trapping.

Another possible explanation for the Si-avalanche-assisted GaN trapping could be the GaN HEMT's false turn-on. Recent studies reported the oscillation at the nodes connecting the Si MOSFET and GaN HEMT due to parasitic components [21], [22]. In the UIS test, this oscillation may turn ON the HEMT and supply the electrons for buffer trapping.

Additional UIS tests were performed with the HEMT V_{GS} monitored to explore this possibility. The test setup is similar to the one in Fig. 9. Two passive probes (Tektronix TPP 1000) with a bandwidth of 1 GHz were tapped on the extra test point (labeled as S_GaN) and the gate wire bond of the HEMT (labeled as G_GaN), respectively (Fig. 18(a)). Both probes were grounded to the source lead of the cascode GaN HEMT, and their voltage difference was extracted to be the source-gate voltage of GaN HEMT (V_{SG_GaN}). The transfer characteristics of the D-mode GaN HEMT shows a threshold voltage (V_{th_GaN}) of -17 V (at V_{DS} = 0.1 V and I_{DS} = 0.1 A) (Fig. 18(b)). The UIS waveform of this decapped cascode GaN HEMT is shown in Fig. 18(c), revealing small oscillations in V_{SG_GaN} and the drain-source voltage of the Si MOSFET (V_{DS_Si}). In addition, both V_{SG_GaN} and V_{DS_Si} are much higher than the absolute value of V_{th_GaN} during the Si avalanche, confirming the absence of GaN HEMT false turn-on. Hence, the HEMT false turn-on is not the cause for the Si-avalanche-assisted GaN trapping.

4.2 TCAD Simulations and Discussions

Physics-based Technology Computer-Aided Design (TCAD) device simulations were performed in Silvaco Atlas to confirm the correlation between the buffer trapping and the dynamic BV. The simulated GaN HEMT structure was determined from the microscopic images of the decapsulated DUTs. The simulation models are similar to those reported in [62], [63].

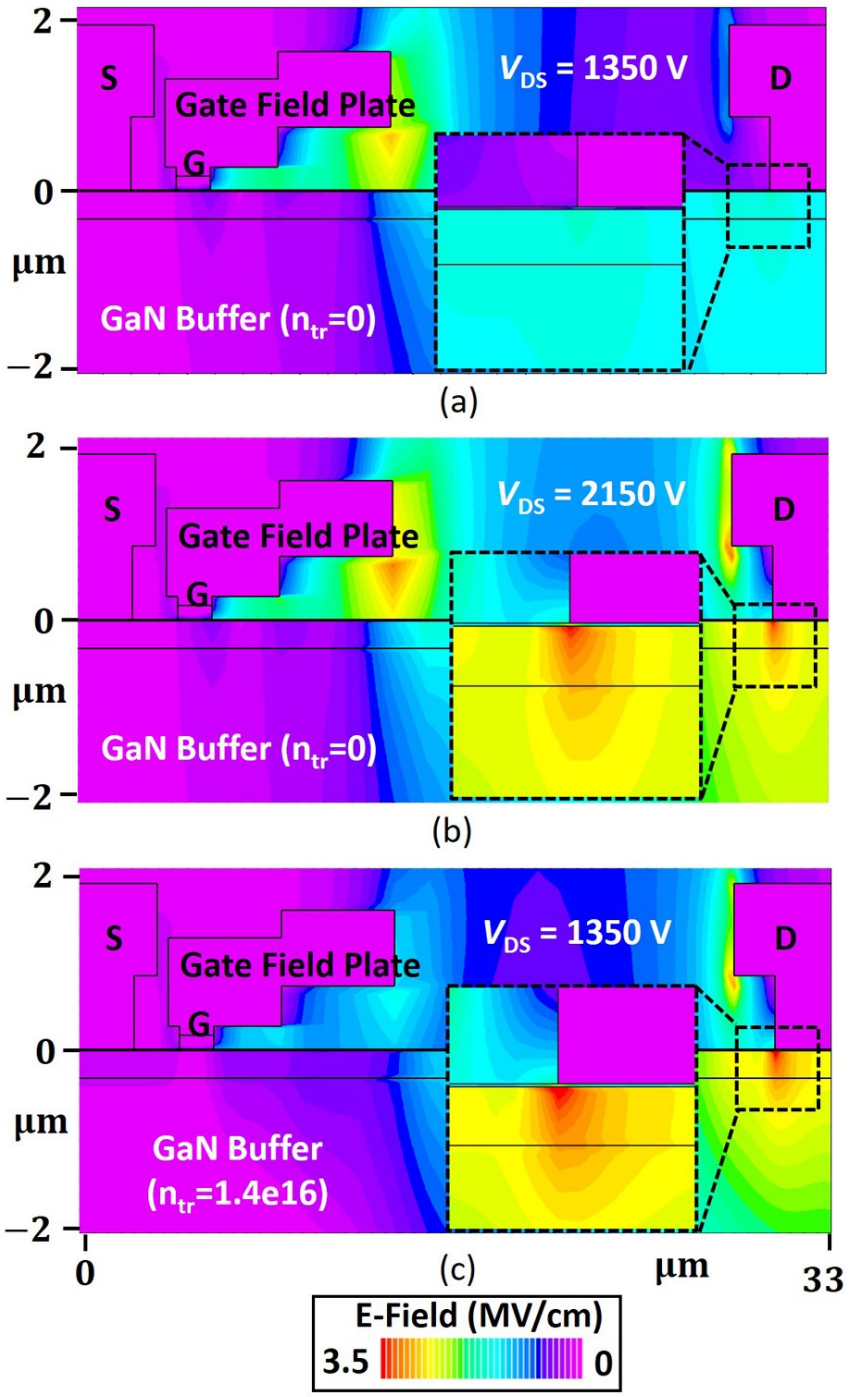

Figure 19. Simulated E-field distribution in the GaN HEMT (a) at V_{DS} = 1350 V without buffer traps, (b) at V_{DS} = 2150 V without buffer traps, and (c) at V_{DS} = 1350 with buffer traps with a density of 1.4×10^{16} cm-3.

The E-field distribution was simulated at V_{DS} of 2150 V and 1350 V with and without adding the buffer traps in the GaN buffer layer, as shown in Fig. 19. At V_{DS} = 2150 V, the peak E-field in GaN locates near the drain side (similar to other commercial GaN HEMTs [42], [45]), and it reaches the critical E-field of GaN (Fig. 19(a)). This is consistent with the highest static *BV*

measured on the curve tracer. At V_{DS} = 1350 V, the peak E-field in GaN is significantly lower than the critical E-field of GaN if no buffer trapping is considered (Fig. 19(b)). However, it reaches the critical E-field of GaN when ~1.4×10^{16} cm^{-3} filled acceptor-like traps are added to the buffer region (Fig. 19(c)). This trap density is consistent with many other reports [46], [64].

From the TCAD simulations, the DUT's failure analysis results in Fig. 16 can be well interpreted. In a GaN HEMT, the high E-field near the drain usually induces a time-dependent device failure featured by a percolation process [64], generating localized shunt paths between the drain and substrate [64]. The concurrence of high E-field and high percolation current may further induce the local thermal runaway, explaining the burning traces near the drain in Fig. 16. This local heating could also result in a large temperature gradient, which facilitates the crack formation in sharp edges of diverse material interfaces [33] due to the significant mismatch in the coefficient of thermal expansion of various semiconductor, dielectric, and metal materials. This explains the observed crack formation in the field plate extending into GaN layers. Note that, in p-gate GaN HEMTs failed in the UIS tests, a similar crack formation was also reported, which was initially induced by the electrical failure at the drain [42], [46].

It should be noted that the trapping effect, the percolation-based electrical breakdown, and the crack formation are all sensitive to the material non-uniformity, i.e., the localized micro-defects from imperfect epitaxy and device processing. This could explain the relatively large variations in the failure voltages, as shown in Fig. 14. In addition, the crack may also extend laterally in the passivation dielectrics to short the gate and drain of the HEMT, resulting in the cascode failing in mode I. This explains some mode I failures at 1400~1600 V, as shown in Fig. 14. Regardless of failure modes, in the UIS test, most DUTs fail at a voltage much lower than the static *BV*, statistically confirming a lower dynamic *BV*.

4.3 Analytical Model

The previous discussions in section 4.2 show that electrons produced in the Si avalanche provide a key source for the GaN buffer trapping in the UIS. A positive correlation between the total number of avalanche-generated charges and the GaN buffer trapping (thereby the device's dynamic *BV*) would be naturally expected. In this section, an analytical model was developed to calculate the Si-avalanche-produced charges and energy loss in a UIS event, which cannot be well

captured by the existing models of the GaN cascode HEMT (e.g., the manufacturer's SPICE model or the models reported in [21], [65]–[67]).

As shown in Fig. 11(a), the model describes a safe-withstanding UIS waveform. Before the DUT is turned OFF (*phase I*), the load inductor with an inductance L is charged by V_{DD}, with a charging time of t_c and the final inductor current I_L.

$$I_L = V_{DD}/L \cdot t_c \tag{9}$$

The total inductor energy E_L is given by:

$$E_L = 0.5 \cdot L \cdot I_L^2 \tag{10}$$

After the DUT is turned OFF, in *phases II* and *III*, a lossless resonance occurs between the load inductance and the DUT's C_{OSS_1} described by Eqn. (5). The voltage across the cascode device (i.e., between the Si MOSFET source and GaN HEMT drain), $V_{DS}(t)$, can be derived from resonance relations:

$$V_{DS}(t) = L\sqrt{I_L/C_{OSS\_1}} \cdot \sin\left(t/\sqrt{L \cdot C_{OSS\_1}}\right) + V_{DD} \tag{11}$$

Based on the equivalent circuit model shown in Fig. 11(b), the V_{DS} of the Si MOSFET, $V_{DS\_Si}(t)$, can be written as

$$V_{DS\_Si}(t) = \frac{C_{DS\_GaN} \cdot V_{DS}(t)}{C_{DS\_GaN}+C_{GD\_Si}+C_{DS\_Si}+C_{GS\_GaN}} \tag{12}$$

When $V_{DS\_Si}(t)$ reaches the BV_{AVA} of the Si MOSFET, BV_{AVA}^{Si}, the *L*-*C* resonance starts to be accompanied by a resistive loss in Si avalanche (*phase IV*), and the new circuit model is shown in Fig. 11(c). From resonance relations, $V_{DS}(t)$ can be depicted by (11) with C_{OSS_1} replaced by the C_{OSS_2} given by (6). However, due to avalanche losses, the inductor current, iL(t), would deviate from the ideal resonant current. From the energy point of view, the time derivative of the total energy in L and C_{OSS_2} equals to the avalanche power loss:

$$0.5 \cdot d[L \cdot i_L(t)^2 + C_{OSS\_2} \cdot V_{DS}(t)^2\,]/dt = -(BV_{AVA}^{Si} - V_{DD}) \cdot i_{Si}(t) \tag{13}$$

where $i_{Si}(t)$ is the avalanche current of the Si MOSFET:

$$i_{Si}(t) = i_L(t) \cdot C_{DS\_GaN}/C_{OSS\_2} \tag{14}$$

The total charge generated in the Si avalanche, Q_{AVA}, can be calculated by integrating $i_{Si}(t)$ until it drops to zero:

$$Q_{AVA} = \int i_{Si}(t)dt \tag{15}$$

The total energy loss in the Si MOSFET avalanche is:

$$E_{AVA} = \int i_{Si}(t) \cdot BV_{AVA}^{Si}\, dt = Q_{AVA} \cdot BV_{AVA}^{Si} \tag{16}$$

After $i_{Si}(t)$ drops to zero, the Si avalanche stops, and the resonance becomes lossless again (*phase V*), which can be well depicted by (11) and (12). After V_{DS} resonances to negative values and exceed the reverse turn-on voltage, the resonance ends, and the inductor is discharged by V_{DD} (*phase VI*).

Using the device parameters in the datasheet and the vendor's SPICE model, the UIS waveforms of a cascode GaN HEMT can be calculated from Eqns. (5)-(6) and (9)-(14). Fig. 20 shows a set of calculated UIS waveforms, which agrees well with the experimental waveforms.

Fig. 21 shows the calculated Q_{AVA} and E_{AVA} as a function of the peak V_{DS} in the UIS withstanding process, V_{m}, and the load inductance. At the increased V_{m}, Q_{AVA} builds up, suggesting more electrons flow through the GaN HEMT structure, thereby increasing buffer trapping and

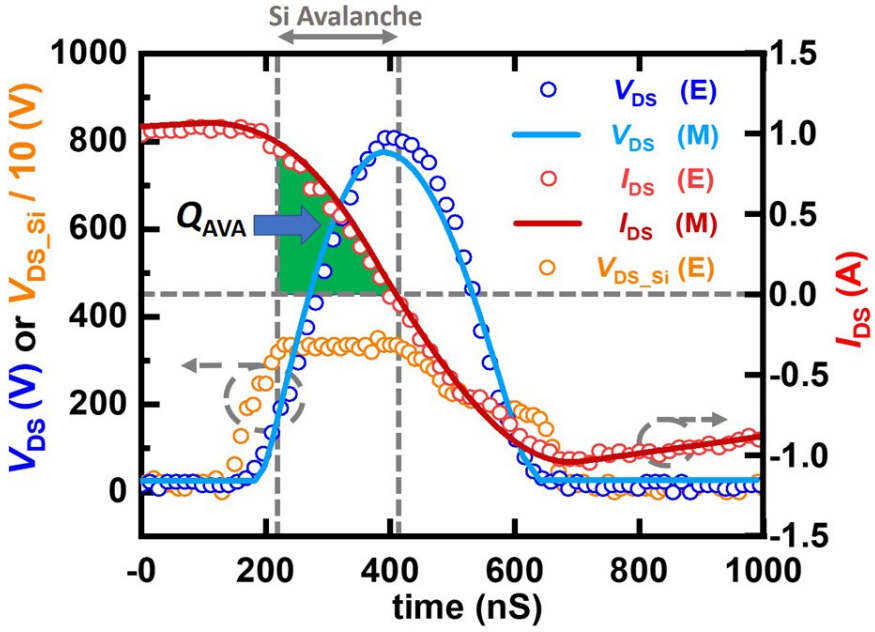

Figure 20. Comparison between a typical UIS waveform calculated by the analytical model and that measured experimentally. "E" stands for the experiment, and "M" stands for the model.

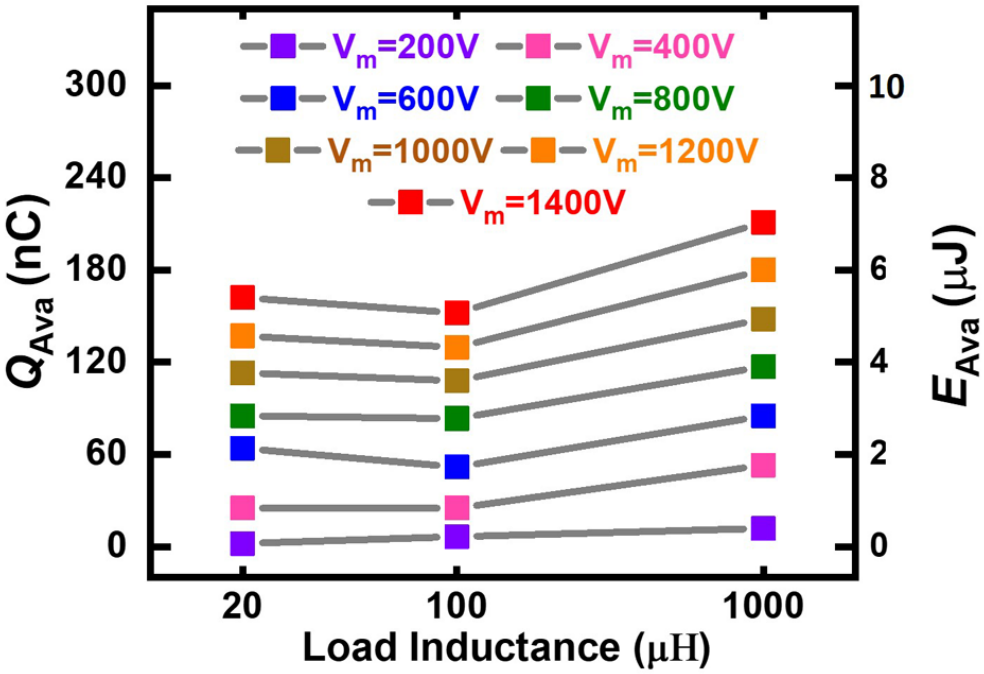

Figure 21. Total charge and energy loss produced in Si avalanche in a UIS cycle under different load inductance.

reducing dynamic BV. This implies a more severe GaN trapping assisted by the Si avalanche during higher overvoltage stress for the cascode GaN HEMT.

As shown in Fig. 21, the calculated Q_{AVA} shows a relatively weak dependence on L, supporting the statistically insignificant correlation between the DUT's failure voltage and L [see Fig. 14]. The calculated Q_{AVA} at 1 mH is slightly higher, which may explain the generally lower failure voltages observed at 1 mH in the UIS experiments.

Finally, the calculated E_{AVA} in Si MOSFET is 6~7 μJ in a UIS event with a V_{m} of 1400 V, which is much smaller than the critical avalanche energy of the Si MOSFET (typically > 50 mJ) [57]. This explains the fact that almost no cascode devices were found to fail in the Si MOSFET in the UIS tests; the heat and junction temperature increase in the Si MOSFET are expected to be far from the Si failure limits. The impact of Si avalanche on the cascode failure is not directly thermal-related but through the trapping effects that are more related to electrical failure.

Chapter 5: Repetitive Robustness of Cascode GaN HEMTs

The DUT failure in the single-event UIS is related to charge trapping. Therefore, studying the cumulative stress effects is essential, i.e., the DUT failure and degradation under repetitive UIS tests. This is because: (a) in repetitive tests, if the trapped carriers cannot be fully de-trapped within the pulse width, they are likely to accumulate in the GaN buffer, which may lead to a lower dynamic *BV*, i.e., a lower failure voltage boundary; (b) for actual device operations in power electronic systems, it is crucial to identify suitable precursors of failure, which can be used to design the monitoring and intervening systems; (c) the DUT's failure and degradation behaviors

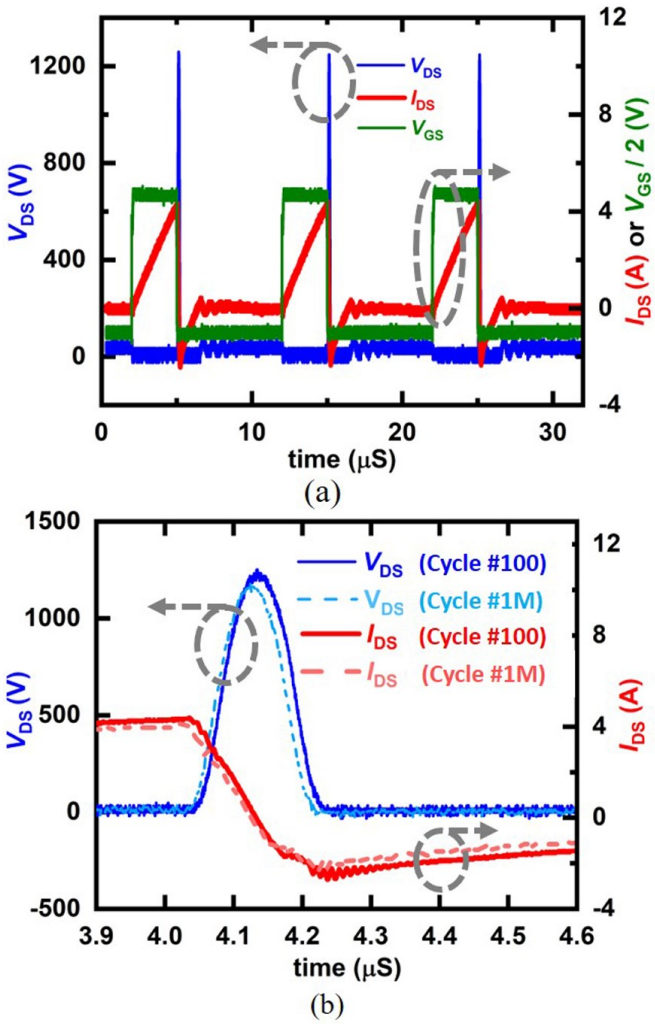

Figure 22. (a) The DUT waveforms under the repetitive UIS stresses at 100 kHz. (b) Comparison of the UIS waveforms during the repetitive tests at the starting and ending stages.

under repetitive UIS tests can in return validate our theories accounting for the DUT failure in the single-event UIS tests.

As the DUT failure is trapping-related, the frequency of repetitive UIS tests is critical in determining the de-trapping time in each pulse. In this work, two frequencies were selected, i.e., 1 kHz and 100 kHz. A load inductance of 20 μH was used in all repetitive UIS tests. The peak V_{DS} was modulated by the inductor charging time, and the same charging time was applied to all pulses in each repetitive UIS test. The charging time was within the 2-3 μs range in different repetitive tests. Due to this short charging time and small avalanche loss in each UIS pulse (as calculated in Section 4.3), the DUT's junction temperature is expected to see a slight rise. The thermal camera measurements revealed that the DUT's temperature rise was within a few degrees in the 100 kHz repetitive UIS tests. Each repetitive trial was stopped after 1 million pulses or the DUT failure.

Fig. 22(a) shows the DUT waveforms in a 100-kHz repetitive UIS test with a peak V_{DS} of 1.25 kV. Fig. 22(b) shows the UIS waveform at the initial state (cycle #100) and the final stage (cycle #1,000,000). The two UIS waveforms show a discrepancy, suggesting parametric shifts in the DUT. The decreased magnitudes of both V_{DS} and I_{DS} indicate an increase in the device's $R_{DS(ON)}$, which induces smaller inductor energy during the charging period. The DUT's parametric shifts will be discussed in detail later in this section.

5.1 Failure Boundry

To explore the failure boundary in repetitive UIS tests, 40 DUTs were tested at 100 kHz and 1 kHz at 25 ^{o}C. At each frequency, the peak V_{DS} in a UIS pulse was increased from 1.2 kV (80% of the single-event UIS failure boundary) to 1.4 kV with a step of 50 V. In the 1-kHz tests, all DUTs survived the 1-million-cycle UIS stresses with V_{DS} up to 1.4 kV.

In the 100-kHz tests, only the DUTs tested under the 1.2 kV, 1.25 kV, and 1.3 kV UIS stresses survived the 1-million-cycle stress. As the peak V_{DS} exceeds 1.35 kV, all DUTs failed mid-test, and all the failure was in the capacitive charging phase of a UIS pulse. As shown in Fig. 23, the cycles that the DUTs survived show a statistically inverse correlation with the peak V_{DS}. The DUTs were found to survive tens of thousand cycles at 1.4 kV peak V_{DS} and hundreds of thousand cycles at 1.35 kV peak V_{DS}. To confirm the safe-withstanding boundary further, a DUT was tested in 1.3

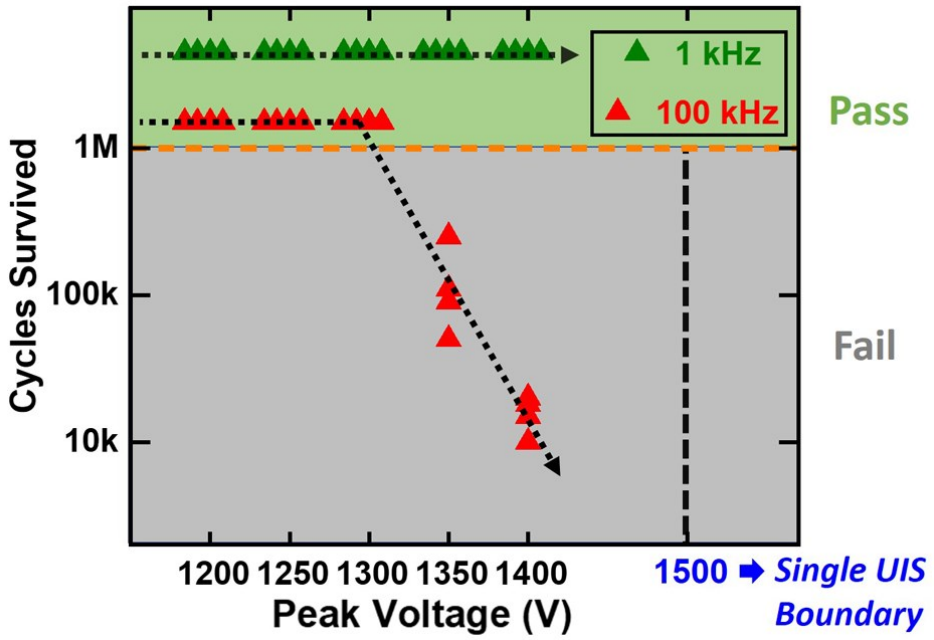

Figure 23. Cycles that the DUTs survived as a function of peak V_{DS} in the UIS stress, for 20 DUTs tested to failure or up to 1 million cycles at 1 kHz and 100 kHz.

kV UIS stresses up to 10 million cycles and showed no failure. This ~1.3 kV boundary is lower than the single-event UIS boundary (~1.5 kV) at 25 ºC.

These experimental results can be explained by the dynamic buffer trapping/de-trapping and the resulted change in DUT's dynamic *BV*. Fig. 24 shows a schematic of the filled buffer traps in the GaN HEMT during the repetitive UIS tests. In each cycle, the UIS pulse results in buffer trapping, the magnitude of which is positively correlated with the peak V_{DS}. These filled traps are de-trapped in the remaining cycle period. At a low frequency (e.g., 1 kHz), the de-trapping time in each cycle is long, and there is no accumulation effect of the buffer trapping. As a result, the DUT's failure boundary, i.e., dynamic *BV*, was experimentally observed to be the same as in the single-event UIS test.

At a high frequency (e.g., 100 kHz), the de-trapping time in each cycle is limited. The filled traps in each UIS pulse may not be fully de-trapped by the end of each cycle. The filled traps keep accumulating until a saturation effect in filling all available traps occurs. The increased trap filling leads to a continuous reduction in the DUT's dynamic *BV* until the buffer trapping saturates. The DUT would fail when the dynamic *BV* drops below the peak V_{DS}. The trap accumulation and dynamic *BV* drop are faster at a higher V_{DS} (e.g., 1.4 kV). This explains the fewer survived cycles

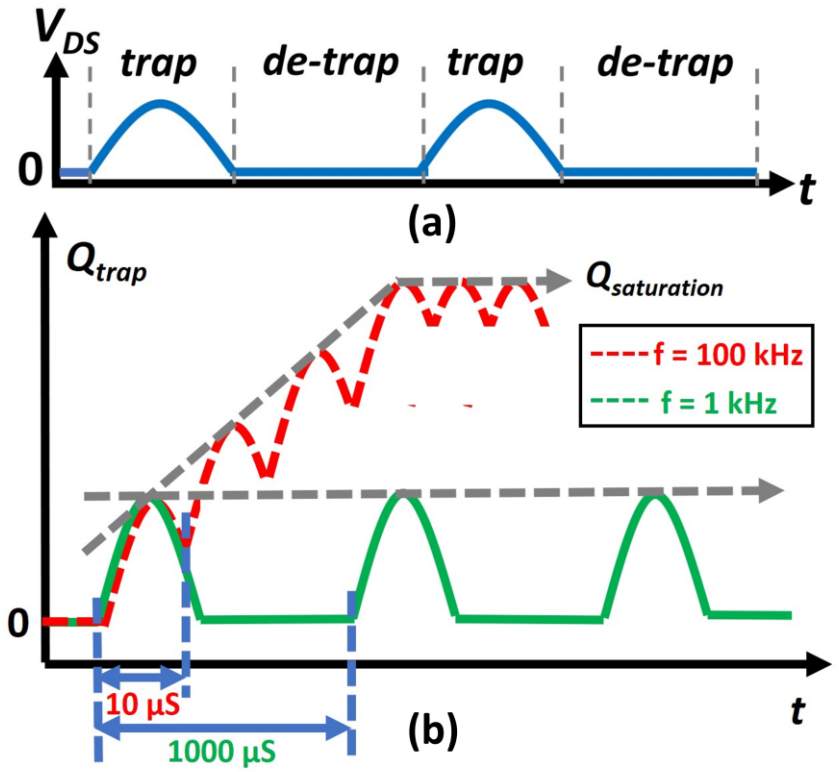

Figure 24. Illustration of (a) device trapping and de-trapping during two UIS periods and (b) the evolution of the filled GaN buffer traps in the repetitive UIS tests with two frequencies.

in the 1.4-kV repetitive UIS tests than in the 1.35-kV tests. All DUTs survived when V_{DS} is lower than ~1.3 kV, suggesting that when the buffer trapping saturates, the corresponding dynamic BV is ~1.3 kV.

5.2 Parametric Shifts and Degradation Precursors

After identifying the failure boundary under repetitive UIS stresses, 10 DUTs were comprehensively characterized before and after the 1-million-cycle UIS stress with 1.25 kV peak V_{DS} at 100 kHz. These DUTs show consistent behaviors, and a representative DUT is reported here.

Fig. 25 shows the DUT's output I-V, transfer, third-quadrant, I_{DSS}, and drain-to-source capacitance (C_{DS}) characteristics measured before and after (5 minutes, 30 minutes, and 60 minutes after) the 1-million-cycle UIS stress. The DUT's threshold voltage shows no shift, suggesting no degradation in the Si MOSFET. $R_{DS(ON)}$ increased by ~100% in both forward and reversed conductions after the UIS stress, a reduction in I_{DSS}, and a negative shift of C_{DS}. After 60 minutes,

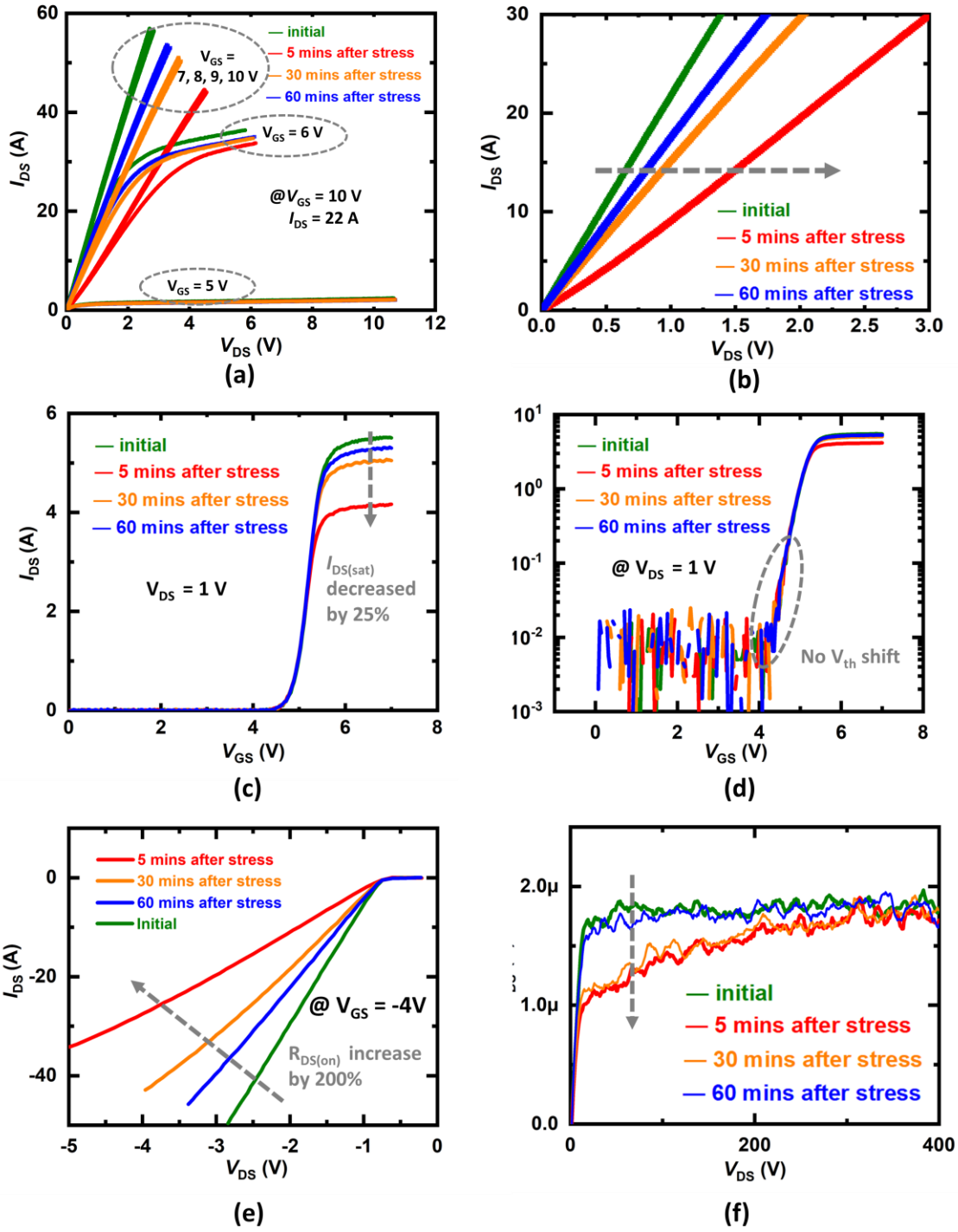

Figure 25. (a) Output characteristics, (b) $R_{DS(ON)}$ measurement at V_{GS} = 10 V, (c) transfer characteristics, (d) third-quadrant I-V characteristics, (e) off-state leakage current, and (f) drain-to-source capacitance (C_{DS}) of the DUT measured before the 1-million-cycle UIS stress with a peak V_{DS} of 1.25 kV, and measured 5 minutes, 30 minutes and 60 minutes after the stress. The dashed arrows indicate the parametric shifts, and the dotted arrows show their recovery.

most of these parametric shifts show considerable recovery, e.g., $R_{DS(ON)}$ recovered to 1.1-fold the

original value. After a few days, most parametric shifts are fully recovered, suggesting that none of these parametric shifts represent permanent device degradation. On the other hand, these results illustrate that $R_{DS(ON)}$, I_{DSS}, and C_{DS} can be the candidate degradation precursors for the cascode GaN HEMT under repetitive overvoltage and surge-energy stresses.

The buffer trapping can well explain these parametric shifts in GaN HEMTs. The filled traps in the buffer deplete the two-dimensional-electron gas (2DEG), increasing $R_{DS(ON)}$. These filled traps will also increase the potential barrier of the depletion region and lead to a reduced I_{DSS} [68]. The buffer trapping will also expand the depletion region, explaining the decreased C_{DS} [47], [69]. After the stress, the de-trapping of buffer traps explains the recovery of the above parametric shifts.

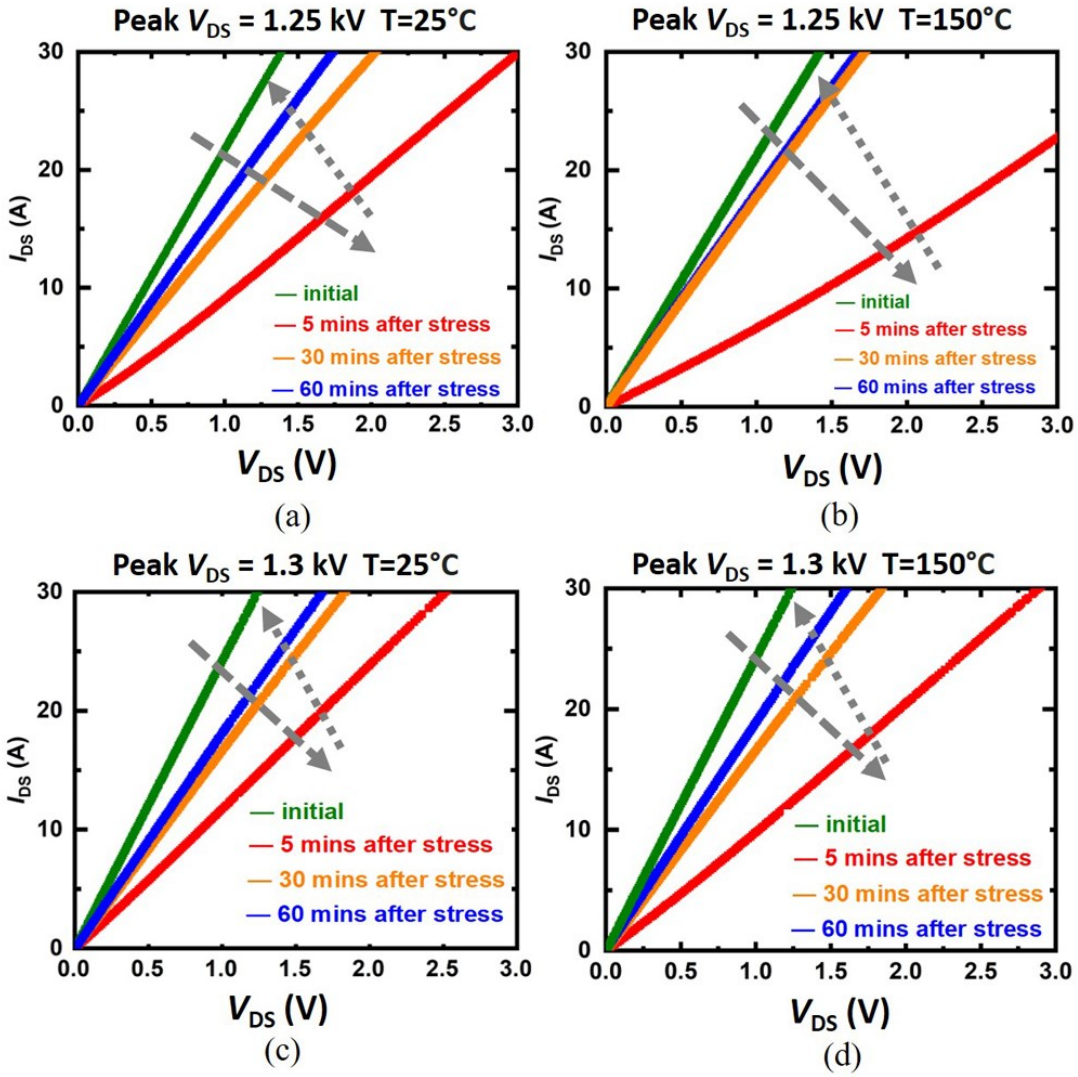

Figure 26. Similar I_{DS}-V_{DS} evolutions of the DUTs with (a) 1.25-kV peak voltage at 25 °C, (b) 1.25-kV peak voltage at 150 °C, (c) 1.3-kV peak voltage at 25 °C, and (d) 1.3-kV overvoltage stress at 150 °C.

The relatively long de-trapping time up to ~1 hour suggests the deep energy levels of the UIS-induced buffer trapping in GaN HEMTs.

To further investigate the impacts of the peak V_{DS} and temperature on the DUT's degradation, 4 DUTs were tested under the 100-kHz, 1-million-cycle UIS stresses with a peak voltage of 1.25 kV and 1.3 kV and a temperature of 25 ºC and 150 °C. All electrical parameters were measured for the 4 DUTs before and after the repetitive UIS stresses. All 4 DUTs showed very similar degradation and recovery behaviors. For example, Fig. 26 shows the I_{DS}-V_{DS} curve evolutions of the 4 DUTs measured at V_{GS} of 10 V, before and after 1-million cycles of UIS stresses, revealing a similar magnitude in $R_{DS(ON)}$ shift and recovery. Additional DUTs have been tested under these four conditions, confirming almost no statistically significant correlation between DUT degradation behaviors and the peak UIS V_{DS} or the temperature.

The above phenomena further supported the saturation effect of the buffer trapping. Under different V_{DS} and temperatures, although the filled traps in each UIS pulse could be different, the trap filling can be all saturated after a million pulses, leading to the consistent shifts in DUT's electrical parameters.

Chapter 6: Conclusions

This work presents comprehensive investigations into the failure and degradation of 650-V-rated cascode GaN HEMTs in single-event and repetitive UIS tests. The cascode device was found to withstand surge energy by a resonant charging of the GaN HEMT's C_{OSS}, accompanied by an avalanche in the Si MOSFET. Two failure modes were observed in the single-event UIS test, occurring in the GaN HEMT. The failure boundaries (~1.5 kV at 25 ºC and ~1.4 kV at 150 ºC) are lower than the device's static *BV* (1.8~2.2 kV). The failure boundary could be lower in repetitive UIS tests, particularly at high frequencies. At 100 kHz, the failure boundary was identified to be ~1.3 kV. After 1 million cycles of 1.25~1.3-kV UIS stresses at 25 ºC and 150 ºC, the DUTs show a significant increase in $R_{DS(ON)}$ and considerable decreases in I_{DSS} and $C_{DS;}$ these parametric shifts are recoverable.

The buffer trapping can explain all these failure and degradation behaviors in the GaN HEMT. In particular, the electrons produced in the Si avalanche flow through the GaN HEMT, facilitating the GaN buffer trapping. The resulting reduction in dynamic *BV* explains the lower UIS failure voltage than the static *BV*. The buffer trapping accumulation in high-frequency repetitive UIS tests accounts for the even lower failure boundary, corresponding to the saturated buffer trapping. The parametric shifts in repetitive tests are also the consequences of GaN buffer trapping.

The results in this work imply that the cascode GaN HEMT cannot fully exploit its static *BV* to withstand surge energy and overvoltage stresses in power converters, as the repetitive failure boundary is merely 60~70% of its static *BV*. By contrast, the repetitive failure boundary (and dynamic *BV*) of p-gate GaN HEMTs were found to be higher than their static *BV* [46]–[48]. The fundamental root cause of this discrepancy is the internal Si avalanche issue uniquely present in the cascode GaN HEMT, which facilitates the GaN buffer trapping. Hence, for power applications requiring device surge-energy and overvoltage robustness, an extra *BV* margin needs to be designed for the cascode GaN HEMT, which may compromise chip size, capacitances, and switching speed.

Bibliography

[1] A. Lidow, M. de Rooij, J. Strydom, D. Reusch, and J. Glaser, *GaN Transistors for Efficient Power Conversion*. John Wiley & Sons, 2019.

[2] A. Q. Huang, "Power Semiconductor Devices for Smart Grid and Renewable Energy Systems," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2019–2047, Nov. 2017, doi: 10.1109/JPROC.2017.2687701.

[3] H. Amano *et al.*, "The 2018 GaN power electronics roadmap," *J. Phys. D: Appl. Phys.*, vol. 51, no. 16, p. 163001, 2018, doi: 10.1088/1361-6463/aaaf9d.

[4] B. J. Baliga, "Semiconductors for high-voltage, vertical channel field-effect transistors," *Journal of Applied Physics*, vol. 53, no. 3, pp. 1759–1764, Mar. 1982, doi: 10.1063/1.331646.

[5] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum semiconductors for high-power electronics," *IEEE Transactions on Electron Devices*, vol. 36, no. 9, pp. 1811–1823, Sep. 1989, doi: 10.1109/16.34247.

[6] M. Asif Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, "High electron mobility transistor based on a GaN-AlxGa1−xN heterojunction," *Appl. Phys. Lett.*, vol. 63, no. 9, pp. 1214–1215, Aug. 1993, doi: 10.1063/1.109775.

[7] A. Bykhovski, B. Gelmont, and M. Shur, "The influence of the strain-induced electric field on the charge distribution in GaN-AlN-GaN structure," *Journal of Applied Physics*, vol. 74, no. 11, pp. 6734–6739, Dec. 1993, doi: 10.1063/1.355070.

[8] P. Asbeck, E. Yu, S. Lau, G. Sullivan, J. Hove, and J. Redwing, "Piezoelectric charge densities in AlGaN/GaN HFETs," 1997, doi: 10.1049/EL:19970843.

[9] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, Sep. 2016, doi: 10.1109/JESTPE.2016.2582685.

[10] K. Hoo Teo *et al.*, "Emerging GaN technologies for power, RF, digital, and quantum computing applications: Recent advances and prospects," *Journal of Applied Physics*, vol. 130, no. 16, p. 160902, Oct. 2021, doi: 10.1063/5.0061555.

[11] W. B. Lanford, T. Tanaka, Y. Otoki, and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," *Electronics Letters*, vol. 41, no. 7, pp. 449–450, Mar. 2005, doi: 10.1049/el:20050161.

[12] M. Xiao *et al.*, "Multi-Channel Monolithic-Cascode HEMT (MC2-HEMT): A New GaN Power Switch up to 10 kV," in *2021 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2021, p. 5.5.1-5.5.4. doi: 10.1109/IEDM19574.2021.9720714.

[13] S. Kaneko *et al.*, "Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 41–44. doi: 10.1109/ISPSD.2015.7123384.

[14] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and Application of 600 V GaN HEMT in Cascode Structure," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2453–2461, May 2014, doi: 10.1109/TPEL.2013.2276127.

[15] P. L. Brohlin, Y. K. Ramadass, and C. Kaya, "Direct-drive configuration for GaN devices," p. 7, 2018.

[16] "TP65H050WS 650V Cascode GaN FET," *Transphorm*. https://www.transphormusa.com/en/product/tp65h050ws-2/ (accessed Jan. 16, 2021).
[17] "GS66508T-DS-Rev-180424.pdf." Accessed: May 24, 2022. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS66508T-DS-Rev-180424.pdf
[18] W. Zhang *et al.*, "A New Package of High-Voltage Cascode Gallium Nitride Device for Megahertz Operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1344–1353, Feb. 2016, doi: 10.1109/TPEL.2015.2418572.
[19] X. Huang, W. Du, F. C. Lee, Q. Li, and Z. Liu, "Avoiding Si MOSFET Avalanche and Achieving Zero-Voltage Switching for Cascode GaN Devices," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 593–600, Jan. 2016, doi: 10.1109/TPEL.2015.2398856.
[20] X. Huang, W. Du, F. C. Lee, Q. Li, and W. Zhang, "Avoiding Divergent Oscillation of a Cascode GaN Device Under High-Current Turn-Off Condition," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 593–601, Jan. 2017, doi: 10.1109/TPEL.2016.2532799.
[21] T. Zhu, F. Zhuo, F. Zhao, F. Wang, and T. Zhao, "Quantitative Model-Based False Turn-on Evaluation and Suppression for Cascode GaN Devices in Half-Bridge Applications," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 10166–10179, Oct. 2019, doi: 10.1109/TPEL.2018.2890680.
[22] P. Xue, L. Maresca, M. Riccio, G. Breglio, and A. Irace, "Investigation on the Short-Circuit Oscillation of Cascode GaN HEMTs," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6292–6300, Jun. 2020, doi: 10.1109/TPEL.2019.2947274.
[23] Y. Zhang *et al.*, "GaN FinFETs and trigate devices for power and RF applications: review and perspective," *Semicond. Sci. Technol.*, vol. 36, no. 5, p. 054001, Mar. 2021, doi: 10.1088/1361-6641/abde17.
[24] Y. Zhang and T. Palacios, "(Ultra)Wide-Bandgap Vertical Power FinFETs," *IEEE Transactions on Electron Devices*, vol. 67, no. 10, pp. 3960–3971, Oct. 2020, doi: 10.1109/TED.2020.3002880.
[25] Y. Zhang, A. Dadgar, and T. Palacios, "Gallium nitride vertical power devices on foreign substrates: a review and outlook," *J. Phys. D: Appl. Phys.*, vol. 51, no. 27, p. 273001, 2018, doi: 10.1088/1361-6463/aac8aa.
[26] J. Hu, Y. Zhang, M. Sun, D. Piedra, N. Chowdhury, and T. Palacios, "Materials and processing issues in vertical GaN power electronics," *Materials Science in Semiconductor Processing*, Dec. 2017, doi: 10.1016/j.mssp.2017.09.033.
[27] Y. Zhang *et al.*, "Large-Area 1.2-kV GaN Vertical Power FinFETs With a Record Switching Figure of Merit," *IEEE Electron Device Letters*, vol. 40, no. 1, pp. 75–78, Jan. 2019, doi: 10.1109/LED.2018.2880306.
[28] J. Liu *et al.*, "1.2 kV Vertical GaN Fin JFETs with Robust Avalanche and Fast Switching Capabilities," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, p. 23.2.1-23.2.4. doi: 10.1109/IEDM13553.2020.9372048.
[29] J. Liu *et al.*, "1.2-kV Vertical GaN Fin-JFETs: High-Temperature Characteristics and Avalanche Capability," *IEEE Transactions on Electron Devices*, vol. 68, no. 4, pp. 2025–2032, Apr. 2021, doi: 10.1109/TED.2021.3059192.
[30] J. Liu *et al.*, "Trap-Mediated Avalanche in Large-Area 1.2 kV Vertical GaN p-n Diodes," *IEEE Electron Device Letters*, vol. 41, no. 9, pp. 1328–1331, Sep. 2020, doi: 10.1109/LED.2020.3010784.

[31] J. Liu *et al.*, "Surge Current and Avalanche Ruggedness of 1.2-kV Vertical GaN p-n Diodes," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 10959–10964, Oct. 2021, doi: 10.1109/TPEL.2021.3067019.
[32] J. Liu *et al.*, "Tuning Avalanche Path in Vertical GaN JFETs By Gate Driver Design," *IEEE Transactions on Power Electronics*, vol. 37, no. 5, pp. 5433–5443, May 2022, doi: 10.1109/TPEL.2021.3132906.
[33] R. Zhang *et al.*, "Robust Through-Fin Avalanche in Vertical GaN Fin-JFET With Soft Failure Mode," *IEEE Electron Device Letters*, vol. 43, no. 3, pp. 366–369, Mar. 2022, doi: 10.1109/LED.2022.3144698.
[34] Y. Zhang, R. Zhang, Q. Song, Q. Li, and J. Liu, "(Invited) Breakthrough Avalanche and Short Circuit Robustness in Vertical GaN Power Devices," *ECS Trans.*, vol. 108, no. 6, pp. 11–20, May 2022, doi: 10.1149/10806.0011ecst.
[35] R. Zhang *et al.*, "Breakthrough Short Circuit Robustness Demonstrated in Vertical GaN Fin JFET," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6253–6258, Jun. 2022, doi: 10.1109/TPEL.2021.3138451.
[36] R. Zhang *et al.*, "Vertical GaN Fin JFET: A Power Device with Short Circuit Robustness at Avalanche Breakdown Voltage," in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, pp. 1–8. doi: 10.1109/IRPS48227.2022.9764569.
[37] M. Xiao *et al.*, "3.3 kV Multi-Channel AlGaN/GaN Schottky Barrier Diodes With P-GaN Termination," *IEEE Electron Device Letters*, vol. 41, no. 8, pp. 1177–1180, Aug. 2020, doi: 10.1109/LED.2020.3005934.
[38] M. Xiao *et al.*, "5 kV Multi-Channel AlGaN/GaN Power Schottky Barrier Diodes with Junction-Fin-Anode," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, p. 5.4.1-5.4.4. doi: 10.1109/IEDM13553.2020.9372025.
[39] M. Xiao, Y. Ma, K. Liu, K. Cheng, and Y. Zhang, "10 kV, 39 mΩ·cm2 Multi-Channel AlGaN/GaN Schottky Barrier Diodes," *IEEE Electron Device Letters*, vol. 42, no. 6, pp. 808–811, Jun. 2021, doi: 10.1109/LED.2021.3076802.
[40] S. R. Bahl and P. Brohlin, "A New Approach to Validate GaN FET Reliability to Power-Line Surges Under Use-Conditions," in *2019 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2019, pp. 1–4. doi: 10.1109/IRPS.2019.8720479.
[41] J. Wang and X. Jiang, "Review and analysis of SiC MOSFETs' ruggedness and reliability," *IET Power Electronics*, vol. 13, no. 3, pp. 445–455, 2020, doi: 10.1049/iet-pel.2019.0587.
[42] R. Zhang, J. P. Kozak, M. Xiao, J. Liu, and Y. Zhang, "Surge-Energy and Overvoltage Ruggedness of P-Gate GaN HEMTs," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13409–13419, Dec. 2020, doi: 10.1109/TPEL.2020.2993982.
[43] "ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD: | JEDEC." https://www.jedec.org/standards-documents/docs/jesd-24-5 (accessed May 06, 2021).
[44] O. Alatise *et al.*, "The Impact of Repetitive Unclamped Inductive Switching on the Electrical Parameters of Low-Voltage Trench Power nMOSFETs," *IEEE Transactions on Electron Devices*, vol. 57, no. 7, pp. 1651–1658, Jul. 2010, doi: 10.1109/TED.2010.2049062.
[45] R. Zhang, J. P. Kozak, J. Liu, M. Xiao, and Y. Zhang, "Surge Energy Robustness of GaN Gate Injection Transistors," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2020, pp. 1–7. doi: 10.1109/IRPS45951.2020.9129324.

[46] R. Zhang, J. P. Kozak, Q. Song, M. Xiao, J. Liu, and Y. Zhang, "Dynamic Breakdown Voltage of GaN Power HEMTs," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, p. 23.3.1-23.3.4. doi: 10.1109/IEDM13553.2020.9371904.
[47] J. P. Kozak, R. Zhang, Q. Song, J. Liu, W. Saito, and Y. Zhang, "True Breakdown Voltage and Overvoltage Margin of GaN Power HEMTs in Hard Switching," *IEEE Electron Device Letters*, vol. 42, no. 4, pp. 505–508, Apr. 2021, doi: 10.1109/LED.2021.3063360.
[48] J. P. Kozak, Q. Song, R. Zhang, J. Liu, and Y. Zhang, "Robustness of GaN Gate Injection Transistors under Repetitive Surge Energy and Overvoltage," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2021, pp. 1–5. doi: 10.1109/IRPS46558.2021.9405173.
[49] J. P. Kozak, R. Zhang, J. Liu, Q. Song, M. Xiao, and Y. Zhang, "Hard-Switched Overvoltage Robustness of p-Gate GaN HEMTs at Increasing Temperatures," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2020, pp. 677–682. doi: 10.1109/ECCE44975.2020.9235461.
[50] W. Saito and T. Naka, "Relation between UIS withstanding capability and I-V characteristics in high-voltage GaN-HEMTs," *Microelectronics Reliability*, vol. 76–77, pp. 309–313, Sep. 2017, doi: 10.1016/j.microrel.2017.07.009.
[51] R. Zhang, Q. Song, Q. Li, and Y. Zhang, "Overvoltage Ruggedness and Dynamic Breakdown Voltage of P-Gate GaN HEMTs in High-Frequency Switching up to Megahertz," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2022, pp. 175–180. doi: 10.1109/APEC43599.2022.9773713.
[52] J. P. Kozak *et al.*, "Accelerating the Recovery of p-Gate GaN HEMTs after Overvoltage Stresses," in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, pp. P22-1-P22-5. doi: 10.1109/IRPS48227.2022.9764463.
[53] Q. Song *et al.*, "GaN MIS-HEMTs in Repetitive Overvoltage Switching: Parametric Shift and Recovery," in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, p. 10B.4-1-10B.4–7. doi: 10.1109/IRPS48227.2022.9764548.
[54] Q. Song *et al.*, "Evaluation of 650V, 100A Direct-Drive GaN Power Switch for Electric Vehicle Powertrain Applications," in *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov. 2021, pp. 28–33. doi: 10.1109/WiPDA49284.2021.9645143.
[55] Q. Song, R. Zhang, J. P. Kozak, J. Liu, Q. Li, and Y. Zhang, "Failure Mechanisms of Cascode GaN HEMTs Under Overvoltage and Surge Energy Events," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2021, pp. 1–7. doi: 10.1109/IRPS46558.2021.9405208.
[56] Q. Song, R. Zhang, J. P. Kozak, J. Liu, Q. Li, and Y. Zhang, "Robustness of Cascode GaN HEMTs under Repetitive Overvoltage and Surge Energy Stresses," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Jun. 2021, pp. 363–369. doi: 10.1109/APEC42165.2021.9487252.
[57] Y. Wu and Y. Lai, "Reliability Performance Related to Internal Avalanche of GaN Cascode Devices," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2018, pp. 94–97. doi: 10.1109/WiPDA.2018.8569055.
[58] S. R. Bahl and M. D. Seeman, "New electrical overstress and energy loss mechanisms in GaN cascodes," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2015, pp. 1262–1265. doi: 10.1109/APEC.2015.7104509.

[59] M. Tack, P. Moens, C. Liu, and F. Bauwens, “An Industrial 650V GaN DHEMT Cascode Technology,” *ECS Trans.*, vol. 64, no. 7, p. 171, Aug. 2014, doi: 10.1149/06407.0171ecst.
[60] M. Meneghini *et al.*, “Temperature-Dependent Dynamic R_{ON} in GaN-Based MIS-HEMTs: Role of Surface Traps and Buffer Leakage,” *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 782–787, Mar. 2015, doi: 10.1109/TED.2014.2386391.
[61] P. Moens *et al.*, “On the impact of carbon-doping on the dynamic Ron and off-state leakage current of 650V GaN power devices,” in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC’s (ISPSD)*, May 2015, pp. 37–40. doi: 10.1109/ISPSD.2015.7123383.
[62] M. Xiao, R. Zhang, D. Dong, H. Wang, and Y. Zhang, “Design and Simulation of GaN Superjunction Transistors With 2-DEG Channels and Fin Channels,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1475–1484, Sep. 2019, doi: 10.1109/JESTPE.2019.2912978.
[63] Y. Zhang *et al.*, “Electrothermal Simulation and Thermal Performance Study of GaN Vertical and Lateral Power Transistors,” *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2224–2230, Jul. 2013, doi: 10.1109/TED.2013.2261072.
[64] M. Borga *et al.*, “Evidence of Time-Dependent Vertical Breakdown in GaN-on-Si HEMTs,” *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3616–3621, Sep. 2017, doi: 10.1109/TED.2017.2726440.
[65] X. Huang, Q. Li, Z. Liu, and F. C. Lee, “Analytical Loss Model of High Voltage GaN HEMT in Cascode Configuration,” *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2208–2219, May 2014, doi: 10.1109/TPEL.2013.2267804.
[66] H. Li *et al.*, “Evaluation of high voltage cascode GaN HEMTs in parallel operation,” in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 990–995. doi: 10.1109/APEC.2016.7467991.
[67] Z. Liu, X. Huang, F. C. Lee, and Q. Li, “Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT,” *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014, doi: 10.1109/TPEL.2013.2264941.
[68] Y. Wang *et al.*, “Dynamic OFF-State Current (Dynamic I_{OFF}) in *p* -GaN Gate HEMTs With an Ohmic Gate Contact,” *IEEE Electron Device Letters*, vol. 39, no. 9, pp. 1366–1369, Sep. 2018, doi: 10.1109/LED.2018.2852699.
[69] J. Chen *et al.*, “OFF-State Drain-Voltage-Stress-Induced VTH Instability in Schottky-Type p-GaN Gate HEMTs,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 3, pp. 3686–3694, Jun. 2021, doi: 10.1109/JESTPE.2020.3010408.