# Chapter Two

# Topology Improvement for Multiphase VRMs

Today's multiphase VRMs are almost universally based on the buck topology. With higher input voltage and lower output voltage, multiphase buck converter has a very small duty cycle, which compromises the steady-state and dynamic performances.

To improve the efficiency without compromising the transient, this chapter proposes to use multi-winding coupled inductors in multiphase converters in order to extend their duty cycles. The simplest topology employing this concept is the multiphase tapped-inductor buck converter. Unfortunately, the leakage inductance between the coupled windings causes severe voltage spikes across the MOSFETs and impairs efficiency.

In order to solve the voltage spike problem, this chapter also presents the use of multi-winding coupled inductors to form an active clamping circuit between interleaving channels. A novel topology, named the multiphase coupled-buck converter, is proposed to enable the use of a large duty cycle with recovered leakage energy and clamped device voltages. The multiphase coupled-buck converter has an efficiency that is significantly better than the multiphase buck converter.

The concept proposed for the multiphase coupled-buck converter can be extended to other applications. The isolated counterpart of the multiphase coupled-buck converter is the push-pull forward converter with the current-doubler rectifier. Compared to the push-pull converter that is the isolated counterpart of the multiphase buck converter, the push-pull forward converter has clamped device voltage and recovery leakage, and therefore it can offer a better efficiency.

## 2.1. MULTIPHASE BUCK CONVERTER

Figure 2.1 shows the multiphase buck converter (two-phase as an example), which is the most common of today's VRM topologies.

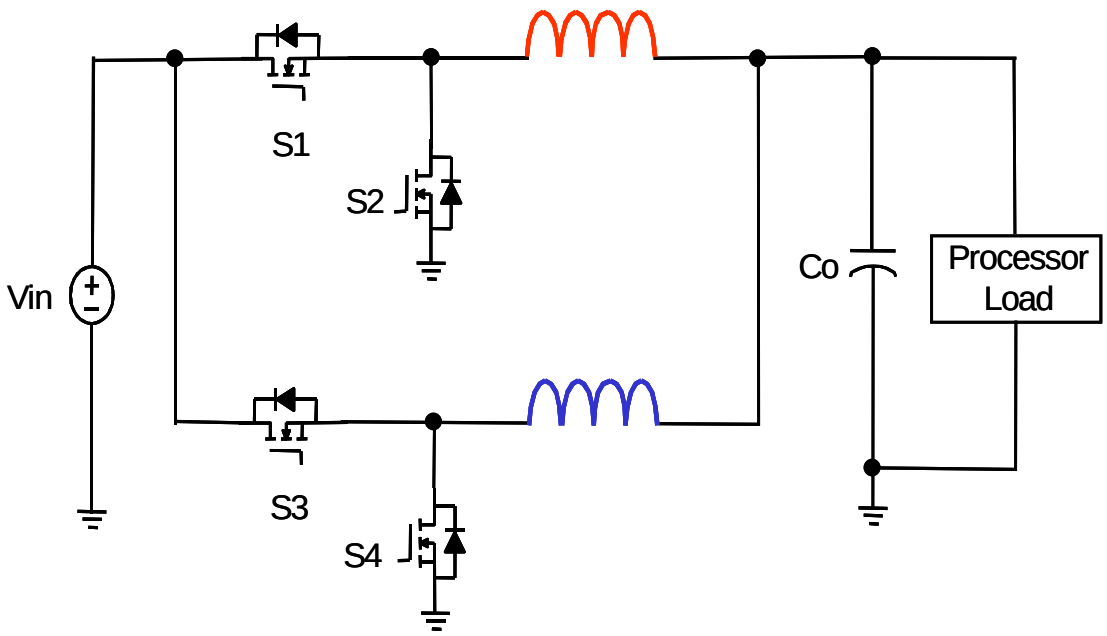



Figure 2.1. Multiphase buck converter (two-phase as an example).

### 2.1.1. Small Duty Cycle Limitation

In the multiphase buck converter, duty cycle D is the ratio of the output voltage $V_O$ and input voltage $V_{IN}$. The earlier VRMs use 5 V as the input; the synchronous buck topology works very well. The latest processors for desktop computers, workstations and low-end servers require VRMs to work with 12V input. In laptop computers, VRMs directly step from the battery charger voltage of 16-24 V down to the processor voltage of 1.5 V. For future processors, the supply voltage is expected to decrease to below 1 V in order to reduce power dissipation. For these applications, the multiphase buck converter is required to operate at a very small duty cycle.

Figure 2.2 shows test waveforms corresponding to a four-phase buck converter ($V_{IN}$=12 V, $V_O$=1.5 V and $F_S$=300 kHz), which is designed according to the VRM 9.0 specification for the latest Pentium ®4 processors. Its duty cycle D is only about 0.12.

The small duty cycle will be a big challenge for future VRMs, if the buck topology is adopted. As predicted at the Intel Technology Symposium 2001, by the year 2005 VRMs will be required to run at about 3 MHz with output voltages of less than 1 V. With the duty cycle less than 10%, the conduction time for the top switches will be less than 30 ns. This makes the use of the synchronous buck topology very difficult, even with much better devices.

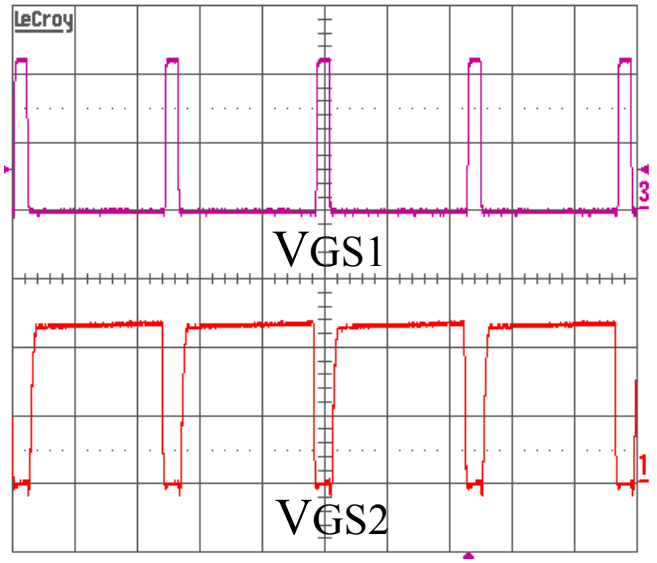



Figure 2.2. Small duty cycle of multiphase buck converter.

### 2.1.2. Influence of Duty Cycle on Ripple Cancellation

The main benefit of multiphase technology is the ripple cancellation effect, which enables the use of the small inductance to both improve transient responses and minimize output capacitance.

Due to the tight voltage tolerance during the load transients, VRMs must use small inductances so that energy can be quickly transferred from the input to the output. Unfortunately, this small inductance results in large inductor current ripples in steady-state conditions. Equation 2.1 shows the relationship between the magnitude of inductor current ripples $\Delta I_{LCH}$ and the inductance value $L_{CH}$. For single-phase converters, large inductor ripple currents flow into the output capacitors and generate large output voltage

ripples. These output voltage ripples can be so large that they are comparable to transient voltage spikes. It is impractical for single-phase converters to work this way.

$$\Delta I_{LCH} = \frac{V_O \cdot (1 - D)}{L_{CH} \cdot F_S}, \tag{2.1}$$

where $F_S$ is the switching frequency.

Multiphase converters interleave the inductor currents in individual channels, and therefore greatly reduce the total current ripples flowing into the output capacitors. With the current ripple reduction, the output voltage ripples are also greatly reduced, which enables the use of very small inductances to improve the transient response, and therefore a small output capacitance can be used to meet the transient requirements. The reduced output ripple voltage also allows more room for voltage variations during the load transient because the ripple voltage will consume a smaller portion of the total voltage tolerance budget. Consequently, multiphasing helps to improve the load transient performance and minimize the output capacitance.

In multiphase converters, the current ripple cancellation effect $K_I$ can be defined as the ratio of the magnitudes of output current ripple $\Delta I_L$ and inductor current ripple $\Delta I_{LCH}$. For N-phase buck converters, the current ripple cancellation effect $K_I$ can be qualified as:

$$K_I = \frac{\Delta I_L}{\Delta I_{LCH}} = \frac{N \cdot (D - \frac{m}{N}) \cdot (\frac{m+1}{N} - D)}{D \cdot (1 - D)}, \tag{2.2}$$

where $m = \text{floor}(N \cdot D)$ is the maximum integer that does not exceed the $N \cdot D$.

The current ripple cancellation is poor when a very small duty cycle is present. The small duty cycles further increase the output current ripples by increasing the individual inductor current ripples, as can be seen from Equation 2.1. Substituting Equation 2.1 into Equation 2.2, the magnitude of the output current ripples for multiphase buck converters can be easily derived, as follows:

$$\Delta I_L = \Delta I_{LCH} \cdot K_I = \frac{V_O \cdot (1 - D)}{L_{CH} \cdot F_S} \cdot \frac{N \cdot (D - \frac{m}{N}) \cdot (\frac{m+1}{N} - D)}{D \cdot (1 - D)} \quad . \tag{2.3}$$

The first term in Equation 2.3 represents the inductor current ripple, and the second term represents the current ripple cancellation effect. These two terms together generate much larger current ripples that flow into the output capacitors.

Figure 2.3 demonstrates the influence of duty cycle on the output current ripple for multiphase buck converters. The output current ripple is normalized against the inductor current ripple at zero duty cycle ( $\Delta I_{LN} = \frac{V_O}{L_{CH} \cdot F_S}$ ).

In summary, multiphase converters reduce the current ripple that flows into the output capacitors, and this enables the use of small inductances to improve the transient response. However, in multiphase buck converters with very small duty cycles, the current ripple reduction is very little, and therefore the benefits of multiphasing, as far as improving the transient response, are compromised. A larger duty cycle is required in order to take full advantage of multiphase technology.

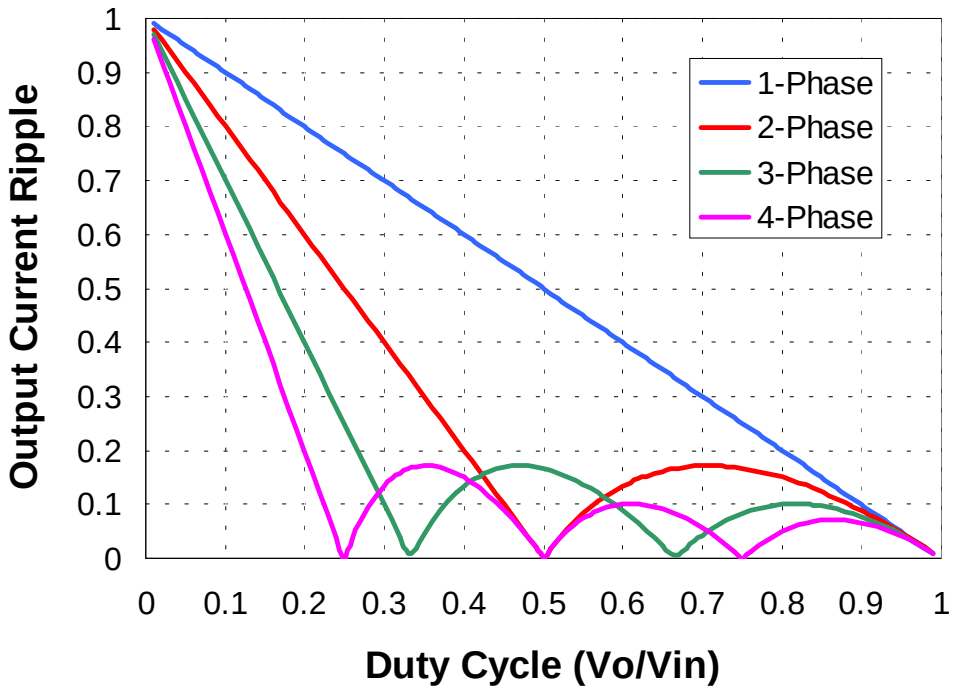



Figure 2.3. Normalized output current ripple vs. duty cycle, $\Delta I_{LN} = \frac{V_O}{L_{CH} \cdot F_S}$.

### 2.1.3. Influence of Duty Cycle on Efficiency

Another disadvantage of the small duty cycle in multiphase buck converters is that inductor current ripples become larger. Large current ripples not only increase the conduction losses but also increase the switching losses of the MOSFETs. The large current ripples in the inductors also increase the losses in the inductors.

In order to investigate the influence of duty cycle on efficiency, the major losses in multiphase buck converters are analyzed and quantified, including the losses in MOSFETs, inductors, input capacitors and output capacitors.

The top MOSFET operates at hard-switching conditions. Its losses $P_{Q1}$ consist of conduction loss $P_{ON}$, switching loss $P_{SW}$, and gate driving loss $P_{DR}$. They can be approximated and derived as follows:

$$P_{Q1} = P_{ON} + P_{SW} + P_{DR}$$

$$P_{ON} = I_D^2 \cdot R_{DS} = (I_{LCH}^2 + \frac{\Delta I_{LCH}^2}{12}) \cdot D \cdot R_{DS}$$

$$P_{SW} = V_{IN} \cdot I_{LV} \cdot T_{ON} \cdot F_S + V_{IN} \cdot I_{LP} \cdot T_{OFF} \cdot F_S \quad , \tag{2.4}$$

$$T_{ON} = \frac{Q_{TH}}{V_{TH}} \cdot R_G \cdot \ln(\frac{V_{DR} - V_{GS1}}{V_{DR} - V_{TH}}) + \frac{Q_{GD} \cdot R_G}{V_{DR} - V_{GS1}}$$

$$T_{OFF} = \frac{Q_{TH}}{V_{TH}} \cdot R_G \cdot \ln(\frac{V_{GS2}}{V_{TH}}) + \frac{Q_{GD} \cdot R_G}{V_{GS2}}$$

$$P_{DR} = Q_G \cdot V_{DR} \cdot F_S$$

where $I_{LCH}$, $\Delta I_{LCH}$, $I_{LV}$ and $I_{LP}$ are the channel inductor average current, peak-to-peak ripple current, valley current and peak current, respectively. $R_{DS}$ is the on-resistance of the top MOSFET. $Q_{TH}$, $Q_{GS1}$ and $Q_{GS2}$ are the gate-source charges at $v_{GS}$=$V_{TH}$, $V_{GS1}$ and $V_{GS2}$, respectively. Here, $V_{GS1}$ and $V_{GS2}$ are the gate-source voltages required to support the load currents $i_{LV}$ and $i_{LP}$, respectively, as read from the MOSFET transconductance characteristics ($i_D$ vs. $V_{GS}$ curves). $Q_{GD}$ and $Q_G$ are the gate-drain charge and total gate

charge, respectively. $V_{DR}$ is the gate supply voltage. $R_G$ is the gate resistance, including the MOSFET internal gate resistance.

The bottom MOSFET operates at synchronous rectification with zero-voltage switching. Its losses $P_{Q2}$ consist of conduction loss $P_{ON}$, body diode loss $P_{DB}$, and gate driving loss $P_{DR}$. They can be approximated and derived as follows:

$$P_{Q2} = P_{ON} + P_{DB} + P_{DR}$$

$$P_{ON} = I_Q^2 \cdot R_{DS} = (I_{LCH}^2 + \frac{\Delta I_{LCH}^2}{12}) \cdot (1 - D) \cdot R_{DS}$$

$$P_{DB} = P_{ON} + P_{RR} = (V_F \cdot I_{LV} \cdot T_{DEAD1} \cdot F_S + V_F \cdot I_{LP} \cdot T_{DEAD2} \cdot F_S) + Q_{RR} \cdot V_{IN} \cdot F_S \quad , (2.5)$$

$$P_{DR} = Q_G \cdot V_{DR} \cdot F_S$$

where $I_{LCH}$, $\Delta I_{LCH}$, $I_{LV}$ and $I_{LP}$ are the channel inductor average current, peak-to-peak ripple current, valley current and peak current, respectively. RDS is the on-resistance of the top MOSFET. $T_{DEAD1}$ and $T_{DEAD2}$ are the dead times introduced by the gate drives and MOSFETs, which cause the body diode conduction loss. $Q_{RR}$ is the reverse-recovery charge of the body diode. $Q_G$ is the total gate charge. $V_{DR}$ is the gate supply voltage.

The inductor losses $P_{LO}$ consist of winding loss $P_{WIND}$ and core loss $P_{CORE}$. They are based on finite element simulations and empirical formulas derived as follows:

$$P_{LO} = P_{WIND} + P_{CORE}$$

$$P_{WIND} = [I_{DC}^2 + \gamma \cdot (I_{RMS}^2 - I_{DC}^2)] \cdot R_{DC} = (I_{LCH}^2 + \gamma \cdot \frac{\Delta I_{LCH}^2}{12}) \cdot R_{DC}, \quad (2.6)$$

$$P_{CORE} = \sum_i C \cdot F_S^{\alpha} \cdot \Delta B_i^{\beta} \cdot V_{COREi}$$

where $I_{LCH}$ and $\Delta I_{LCH}$ are the channel inductor average current and peak-to-peak ripple current, respectively. $R_{DC}$ is the DC resistance of the windings. $\gamma$ is the ratio of the AC resistance and DC resistance of the windings. C, $\alpha$ and $\beta$ are the empirical parameters for core loss, given by the manufacturer of the core material. $\Delta B_i$ and $V_{COREi}$ are the flux density and the corresponding core volume for different core regions, as read from finite element simulations.

The loss in output capacitors $P_{CO}$ is caused by the RMS current on the equivalent series resistance (ESR) of the output capacitors, and can be derived as follows:

$$P_{CO} = I_{RMS}^2 \cdot ESR = \frac{1}{12} \Delta I_L^2 \cdot ESR$$
$$\Delta I_L = \frac{V_O \cdot (1 - D)}{L_{CH} \cdot F_S} \cdot \frac{N \cdot (D - \frac{m}{N}) \cdot (\frac{m+1}{N} - D)}{D \cdot (1 - D)} \quad (2.7)$$

where $\Delta I_L$ is the peak-to-peak ripple current of the output capacitors. $m = \text{floor}(N \cdot D)$ is the maximum integer that does not exceed the $N \cdot D$. Lch is the channel inductance value.

Similarly, the loss in input capacitors $P_{CIN}$ can be derived as follows:

$$P_{CIN} = I_{RMS}^2 \cdot ESR$$

$$I_{RMS} = I_O \sqrt{(D - \frac{m}{N})(\frac{m+1}{N} - D) + \frac{N}{12}(\frac{\Delta I_{LCH}}{D \cdot I_O})^2 [(m+1)^2 (D - \frac{m}{N})^3 + m^2 (\frac{m+1}{N} - D)^3]} \quad , \tag{2.8}$$

where $I_O$ and $\Delta I_{LCH}$ are the load current and the channel peak-to-peak inductor current, respectively. $m = \text{floor}(N \cdot D)$ is the maximum integer that does not exceed the $N \cdot D$.

Based on the preceding loss analysis, the loss contributions of the major components are given for a typical four-phase synchronous buck VRM, which is designed according to the VRM 9.0 specification for the latest Pentium ®4 processors. Hardware is also built in order to demonstrate the influence of duty cycle on efficiency.

The circuit operation condition is $F_S$=300 kHz, $V_O$=1.5 V and $I_O$=50 A. The circuit is designed under two input voltage conditions: $V_{IN}$=5 V and $V_{IN}$=12 V. Consequently, the duty cycle is about 0.3 with 5V input, and 0.125 with 12V input.

Each top and bottom switch uses one SO-8 package MOSFET, so there are eight MOSFETs in four channels. The top switches use Siliconix's Si4884DY and the bottom switches use Siliconix's Si4874DY. The output capacitors consist of six Sanyo 4V, 820μF OSCON capacitors, and the input capacitors consist of three Sanyo 16V, 270μF OSCON capacitors.

Two pairs of E-I cores are used in the four-phase buck VRM. The two channels with phase shifts of $0^o$ and $180^o$ share a pair of cores, while the other two channels with phase

shifts of $90^o$ and $270^o$ share another pair. The cores used are E18/4/10 and PLT 18/10/2 cores from Philips. The materials for all the cores are 3F3. Each inductor has two turns of winding. The windings are built on the two sides of the printed circuit board (PCB). The two outer legs of the E core are milled to generate the air gaps and give about 320nH inductance for each channel.

Figure 2.4 shows the loss contributions of the major components in the tested four-phase synchronous buck VRM with two different input voltages: $V_{IN}$=5 V and 12 V.

Using the different input voltages, 5 V and 12 V, the gate drive losses for both top and bottom switches are the same. With the increase of input voltage from 5 V to 12 V, the duty cycle is decreased from about 0.3 to 0.125, which reduces the conduction loss of the top switches but increases the conduction loss of the bottom switches. The overall conduction losses for both top and bottom switches are almost the same. With the reduction of duty cycle, the losses in the input capacitors, both the inductor windings and cores, and in the body diodes of the bottom switches are all increased very little. As the duty cycle is reduced, the major increase in loss comes from the switching of the top switches. As can be seen from Figure 2.5, the switching loss of the top switches is increased by about 5 W, which corresponds to more than 5% efficiency at full load.

Figure 2.5 shows the measured efficiency comparison under input voltages $V_{IN}$=12 V (D=0.125) and $V_{IN}$=5 V (D=0.3). The measured efficiency data include the power losses in the power stage, but exclude the control and gate drive losses.

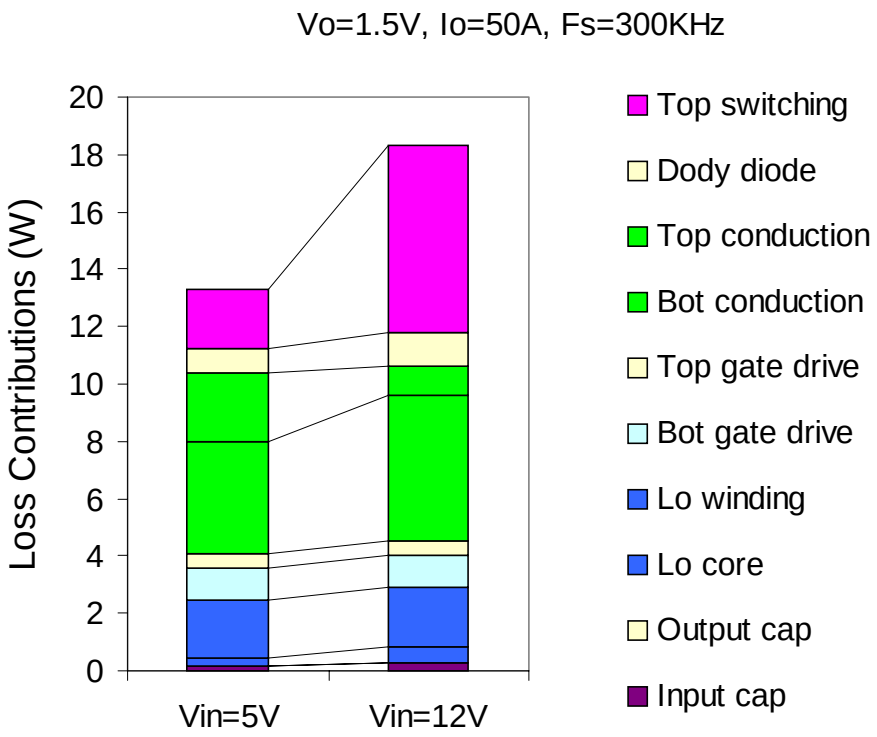



Figure 2.4. Loss contributions in four-phase buck VRM with $V_{IN}$=5 V and 12 V.

As can be seen from Figure 2.5, the 5V-input VRM can achieve 87% efficiency at full load and 91% as the highest efficiency, while the 12V-input VRM can only reach 81% efficiency at full load and 84.5% as the highest efficiency. The increase of the duty cycle from 0.125 to 0.3 improves the efficiency by about 6% at full load and about 7% at the point of highest efficiency. As can be seen from the loss contributions shown in Figure 2.5, the efficiency improvement is mainly caused by the reduced switching loss of the top switches.

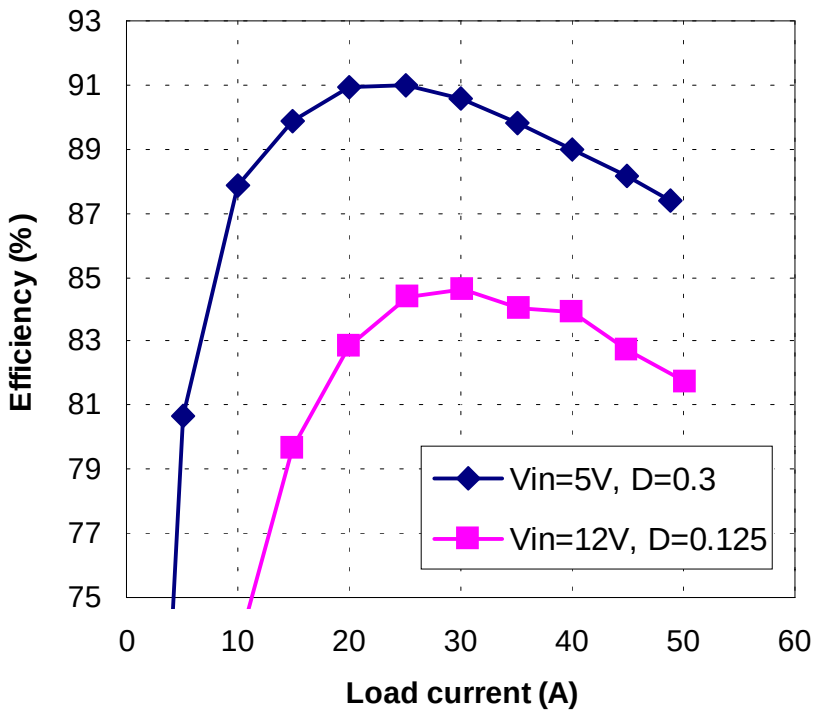



Figure 2.5. Measured efficiency of four-phase buck VRM under $V_{IN}$=5 V and 12 V.

In summary, with a higher input voltage and a lower output voltage, the duty cycle for multiphase synchronous buck converters is very small, which significantly increases the switching loss of the top switches and greatly impairs the overall converter efficiency.

The following sections will explore topologies other than the multiphase buck converter that can achieve high levels of efficiency by having larger duty cycles.

## 2.2. MULTIPHASE TAPPED-INDUCTOR BUCK CONVERTER

Several methods exist for extending the duty cycle of the conventional buck converter. Some examples are the cascade buck topologies [A42, A45], Middlebrook's transformerless converter [A43], and the topologies that employ transformers or coupled inductors [A44, A46]. Among them, the tapped-inductor buck converter is one of the simplest topologies with an extended duty cycle. The biggest advantage of the tapped-inductor buck converter over other proposed topologies is the fact that it only involves a slight modification of the original buck converter.

Figure 2.6 shows a multiphase tapped-inductor buck converter (two-phase as an example). The turns ratio of the tapped inductor is defined as the turns number of the winding in series with the top switch over that of the winding in series with the bottom switch, as shown in Figure 2.6.

### 2.2.1. Design Considerations for Turns Ratio and Duty Cycle

In multiphase tapped-inductor buck converters, the DC voltage gain is a function of both the duty cycle D and the turns ratio of the tapped inductor, n, and can be derived as follows:

$$\frac{V_O}{V_{IN}} = \frac{D}{D + n \cdot (1 - D)}. \tag{2.9}$$

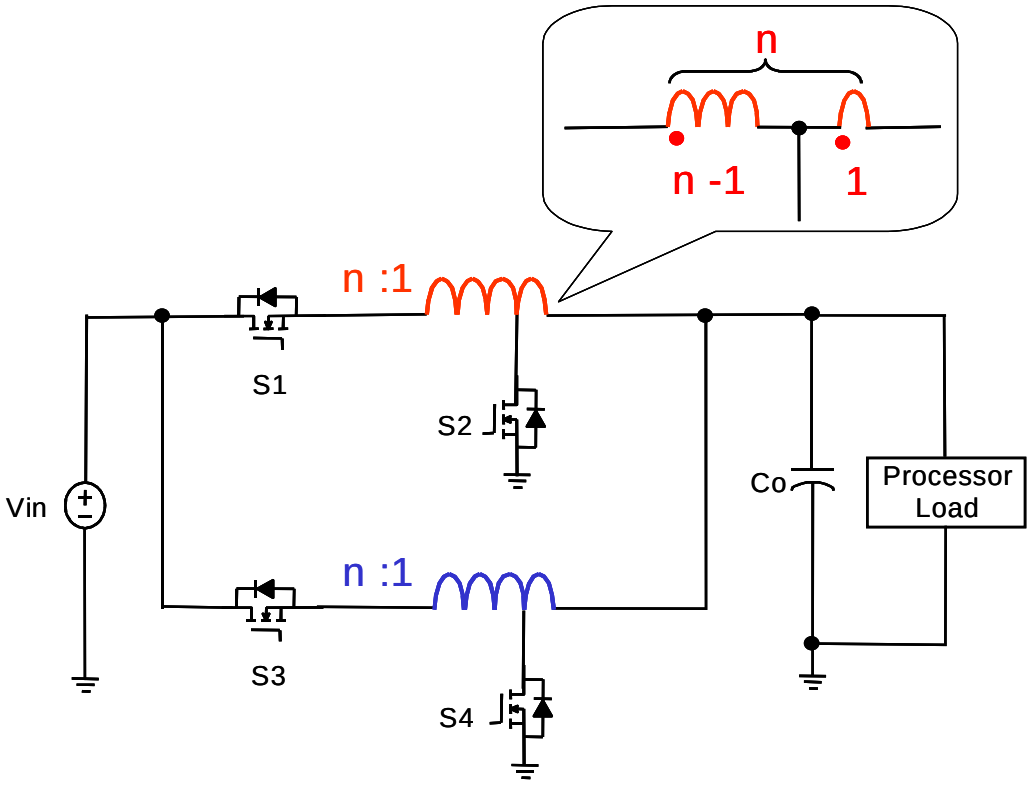



Figure 2.6. Multiphase tapped-inductor buck converter (two-phase as an example).

Figure 2.7 shows the DC voltage gain of the multiphase tapped-inductor buck converter as a function of the duty cycle D and the turns ratio n. The DC voltage gain of the multiphase buck converter is also included for comparison. For the multiphase tapped-inductor buck converter, the higher the turns ratio, the larger the resultant duty cycle. For a VRM stepping down from 12 V to 1.5 V, the multiphase tapped-inductor buck converter operates at a duty cycle of 0.225 with the turns ratio n=2, while the duty cycle of the multiphase buck converter is only 0.125.

For the multiphase tapped-inductor buck converter, the desirable turns ratio is determined by transient responses.

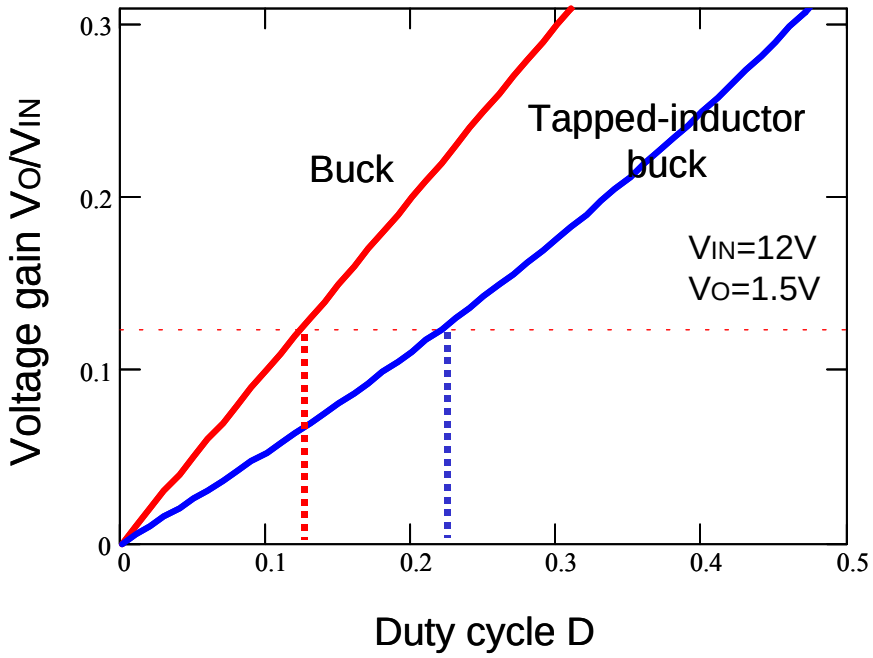



Figure 2.7. DC voltage gain of tapped-inductor buck converter as a function of the duty cycle D and the turns ratio n.

The transient response is mainly determined by the output inductance and the control bandwidth. The control bandwidth needs to be pushed as high as possible in order to achieve fast transient response. With the highest control bandwidth, the fastest transient response can then be achieved if the critical inductance value is chosen as the output inductance. The critical inductance is the largest inductance that gives the fastest transient response.

For the VRM designed according to the critical inductance, the duty cycle would barely become saturated during the transient responses. That is, the duty cycle D=1 for the step-up transient, and the duty cycle D=0 for the step-down transient.

Figure 2.8 shows equivalent circuits of the tapped-inductor buck converter during step-up and step-down transients. The output inductance is assumed to be designed according to the critical inductance in order to achieve the fastest transient response.

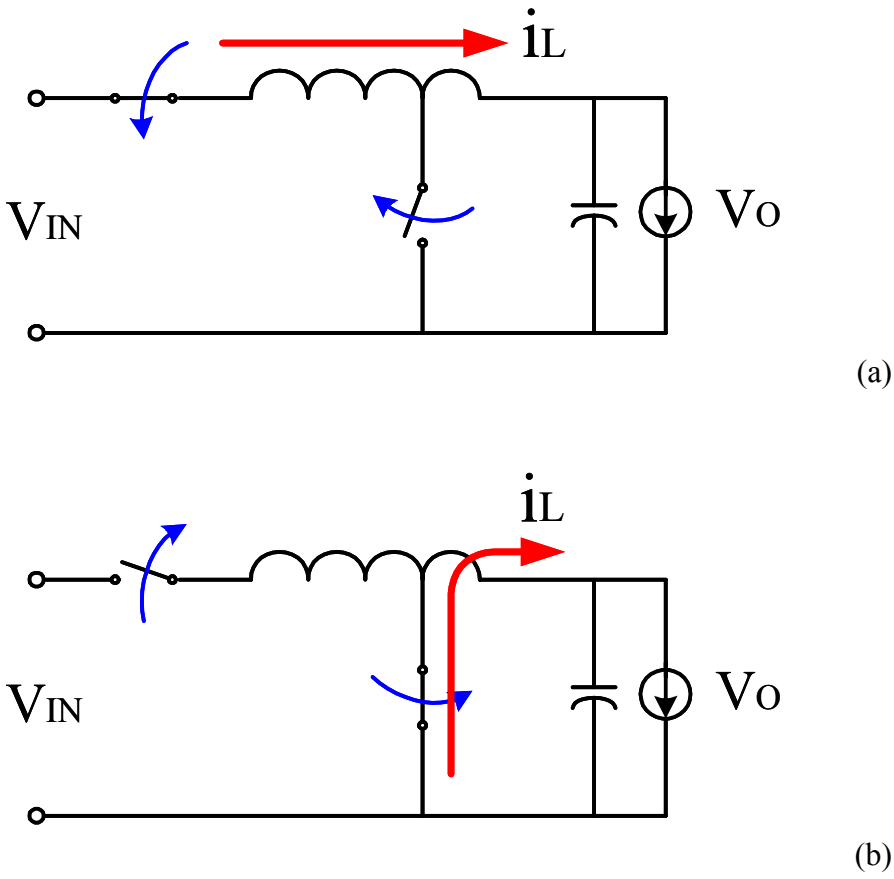



Figure 2.8. Equivalent circuits of tapped-inductor buck converter during transients: (a) step up, and (b) step down.

During a step-up transient, the top switch is on and the bottom switch is off. The inductor slew rate during the step-up transient can be expressed as follows:

$$\frac{di_L}{dt} = \frac{V_{IN} - V_O}{n^2 \cdot L_O}, \tag{2.10}$$

where $L_O$ is the inductance value of the tapped inductor reflected to the low-turns winding.

Similarly, during a step-down transient, the bottom switch is on and the top switch is off, and the inductor slew rate can be expressed as follows:

$$\frac{di_L}{dt} = -\frac{V_O}{L_O}. \tag{2.11}$$

The difference between the load current and the inductor current causes the unbalanced charge that must be provided by the output capacitors. The smaller the unbalanced charge area, the faster the transient responses will be. From the efficiency standpoint, it is desirable to choose a high turns ratio in order to achieve a larger duty cycle. However, from the transient standpoint, with the increase of the turns ratio the step-up transient becomes slower than the step-down transient, which impairs the overall transient performance. Therefore, the optimum turns ratio is chosen to achieve the same transient inductor slew rates for both step-up and step-down transients.

Equalizing Equations 2.10 and 2.11, the optimum turns ratio can be obtained as follows:

$$n = \sqrt{\frac{V_{IN}}{V_O} - 1}. \tag{2.12}$$

As can be seen from Equation 2.12, the optimum turns ratio is related only to the ratio between the input and output voltages. The value calculated from Equation 2.12 is often non-integral, so the turns ratio is chosen as the integer closest to that value.

Figure 2.9 shows the transient inductor slew rates as a function of the turns ratio for a VRM stepping down from 12 V to 1.5 V. The optimum turns ratio is 2:1, and the tapped inductor has a very simple winding structure: The entire tapped winding has two turns, each side having one turn only.

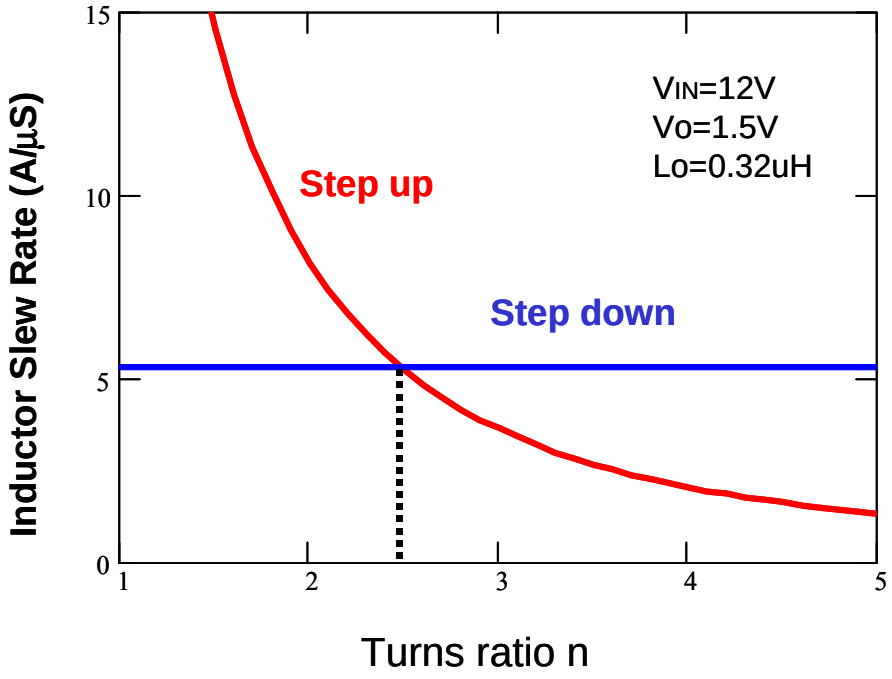



Figure 2.9. Inductor slew rates during step-up and step-down transients for tapped-inductor buck converter as a function of the turns ratio n.

### 2.2.2. Limitation of Voltage Spike Problem

Even with the simplest winding structure that has only one turn for each side, leakage inductance still exists between the two parts of the tapped winding. The leakage inductance causes a severe voltage spike across the switching devices, especially for the top switches. The energy trapped in the leakage inductance is also dissipated in each switching cycle and generates great amounts of power loss.

A four-phase tapped-inductor buck VRM prototype is built to investigate the influence of the leakage inductance on converter performance. For a fair comparison, the four-phase tapped-inductor buck VRM has the same operation conditions: $F_S$=300 kHz, $V_{IN}$=12 V, $V_O$=1.5 V and $I_O$=50 A, and the same MOSFETs, input capacitors and output capacitors as the four-phase buck VRM described in Section 2.1.3. The top switches are Siliconix's Si4884DY and the bottom switches are Siliconix's Si4874DY. The output capacitors consist of six Sanyo's 4V, 820μF OSCON capacitors, and the input capacitors consist of three Sanyo 16V, 270μF OSCON capacitors.

The implementation of inductors is also similar to that in the four-phase buck VRM. Two pairs of E-I cores are used. The two channels with phase shifts of $0^o$ and $180^o$ share a pair of cores, while the other two channels with phase shifts of $90^o$ and $270^o$ share another pair of cores. The same E18/4/10 and PLT 18/10/2 cores are used and the same 3F3 material is used for all cores. Each inductor also has two turns of winding and the windings are built on the two sides of the PCB. The two outer legs of the E core are milled to generate the air gaps.

Compared to the inductor design in the four-phase buck VRM, one difference is that the drain of the bottom switch is connected to the middle point of the two-turns winding instead of to the starting point. Another difference is the length of the air gaps. In order to design both VRMs to have the same transient response for a fair comparison, the worst inductor slew rates are designed to be the same. Consequently, the air gaps of the four-phase tapped-inductor buck VRM are milled to give about 320 nH for one turn of tapped inductor, while in the four-phase buck VRM, the two-turns inductor has 320 nH.

Figure 2.10 shows the measures efficiency for the four-phase tapped-inductor buck VRM. The efficiency of the four-phase buck VRM is also plotted for comparison.

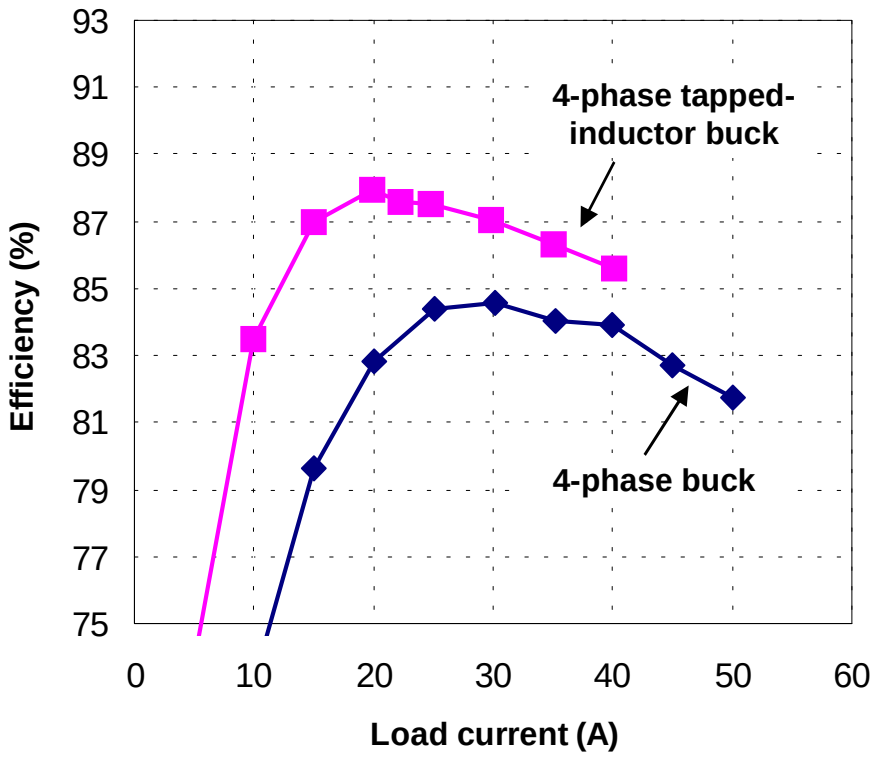



Figure 2.10. Measured efficiency of four-phase tapped-inductor buck VRM.

As can be seen from Figure 2.10, the efficiency of the multiphase tapped-inductor buck converter is higher than that of multiphase buck converter. However, the four-phase tapped-inductor buck VRM blew up when the load current was increased beyond 40 A. Figure 2.11 shows the measured switching waveforms at the moment when the circuit blew up. A huge voltage spike is observed across the top switch; the spike voltage is higher than 30 V and causes the failure of the top switch, which uses the best-available 30 V MOSFET.

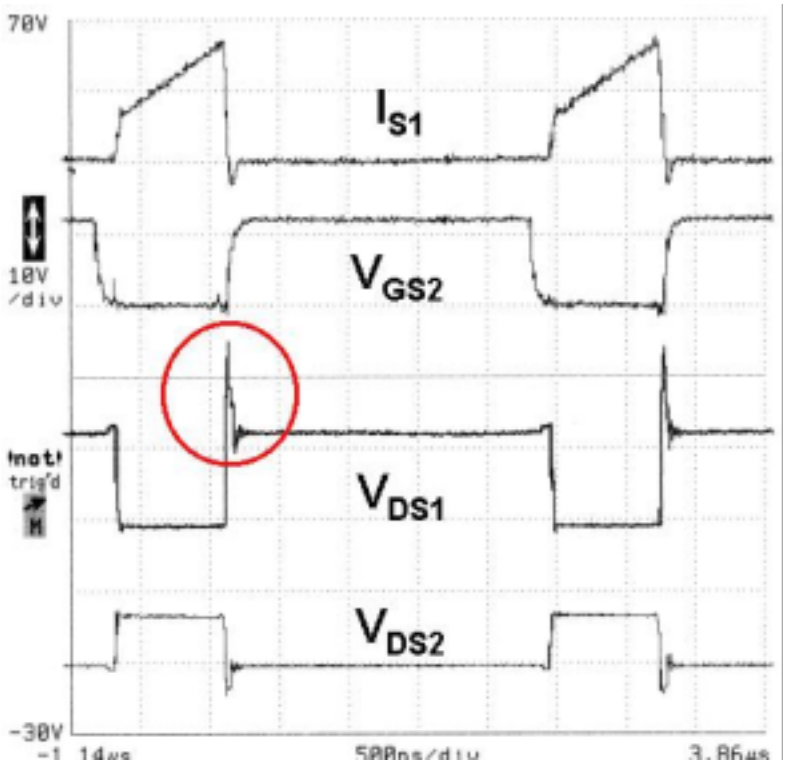



Figure 2.11. Measured waveform shows a huge voltage spike across the top switch in the four-phase tapped-inductor buck VRM.

The huge voltage spike is caused by the leakage inductance and the output capacitance of the top switch; this can be explained in the equivalent circuit of the tapped-inductor buck converter when the top switch turns off, as shown in Figure 2.12.

After the top switch turns off, the bottom switch turns on, and the leakage inductor current is equal to the output inductor current. The leakage inductor and the output capacitor of the top MOSFET form a resonant circuit. The energy trapped in the leakage inductor transfers to the output capacitor of the top MOSFET, which causes a huge voltage spike across the top switch. The spike voltage can be estimated as follows:

$$\Delta V_{DS} = I_{LP} \cdot \sqrt{\frac{L_K}{C_{DS}}} \tag{2.13}$$

where $L_K$ is the leakage inductance of the tapped inductor, $C_{DS}$ is the output capacitance of the top MOSFET, and $I_{LP}$ is the peak value of the output inductor current.

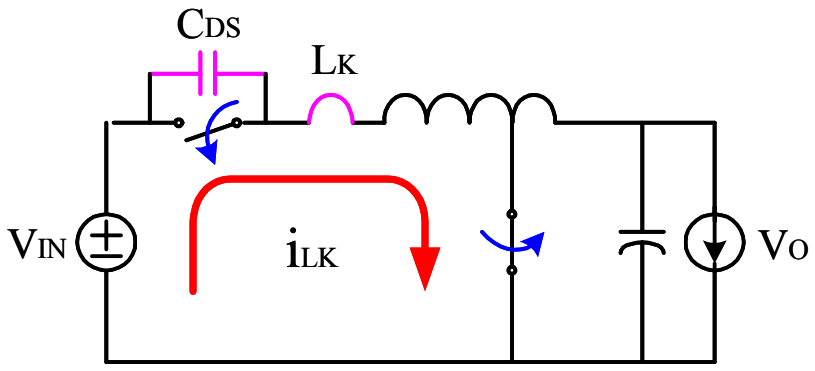



Figure 2.12. Voltage spike across the top switch is caused by the leakage inductance of the tapped inductor and the output capacitance of the top switch.

## 2.3. MULTIPHASE COUPLED-BUCK CONVERTER

Clamping or snubber circuits can be used to solve the voltage spike problem of the tapped-inductor buck converter. However, these require many additional components for each channel. For multiphase topologies, this solution would impose great increases in both the cost and complexity of the circuit.

This section proposes the use of multi-winding coupled inductors to form an active clamping circuit between the interleaving channels to solve the voltage spike problem. By sharing some components between interleaving channels, the leakage energy is recovered and the voltage spike across the top switches is clamped.

### 2.3.1. Concept of Multiphase Coupled-Buck Converter

The idea for the multiphase coupled-buck converter is derived from the multiphase tapped-inductor buck converter with an active clamping circuit for each channel being used to solve the voltage spike problem, as shown in Figure 2.13.

Each channel has an active clamping circuit formed by a capacitor and a MOSFET. The capacitor has a constant voltage, which serves as a voltage source in steady-state operation. The MOSFETs S1a and S2a have the same control timings as bottom switches S2 and S4, respectively. After top switch S1 or S3 turns off, the current trapped in the leakage inductance forces the body diode of S1a or S2a to conduct. Consequently, the drain-source voltage of top switch S1 or S3 is clamped by the input voltage source and

the clamping capacitor. The leakage energy is stored in the clamping capacitors C1 or C2 and is then recovered to the load.

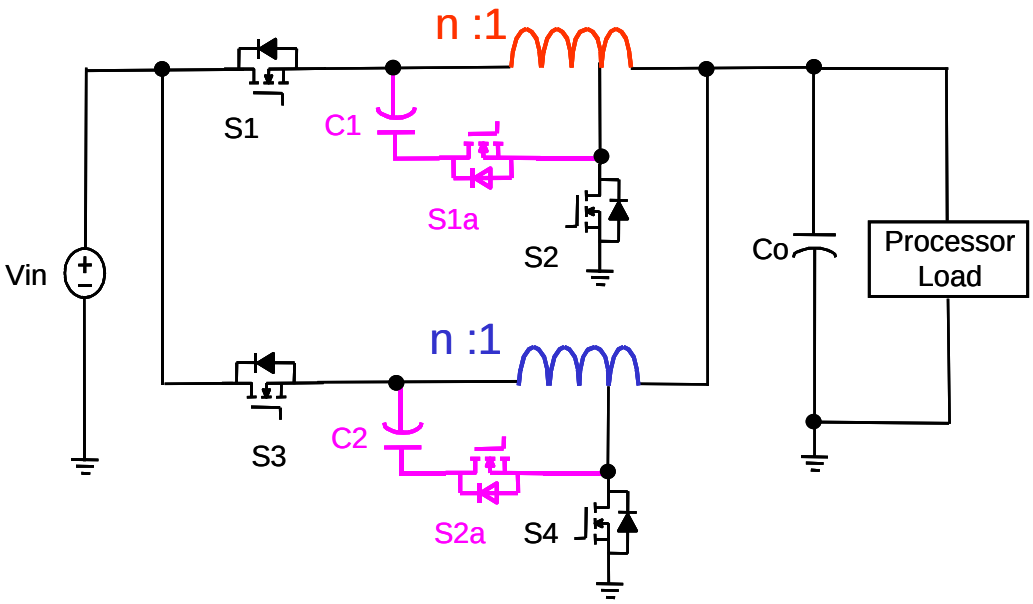



Figure 2.13. Multiphase tapped-inductor buck converter with an additional active clamping circuit for each channel.

Although the solution shown in Figure 2.13 can effectively solve the leakage problem for the multiphase tapped-inductor buck converter, this kind of method requires many additional components, greatly increasing the cost and complexity of the circuit.

Since multiphase topologies already have many switches, the idea is that neighbor channels can probably be rearranged so that the existing switches can incorporate the function of the additional switches shown in Figure 2.13. Figure 2.14 shows a resulting configuration. The topology is very simple. Top switches S1 and S2 have two functions: they serve as the control switches for their own channels, and meanwhile, also serve as

the active clamping switches for neighbor channels. In order to realize this active clamping concept, the capacitor Cc has to appear as a constant voltage, as shown in Figure 2.14. However, further investigation reveals that this capacitor does not have a constant voltage. The reasons are that switches S1 and S3 do not switch complementarily, and the two top windings in the neighbor channels have different voltages across them.

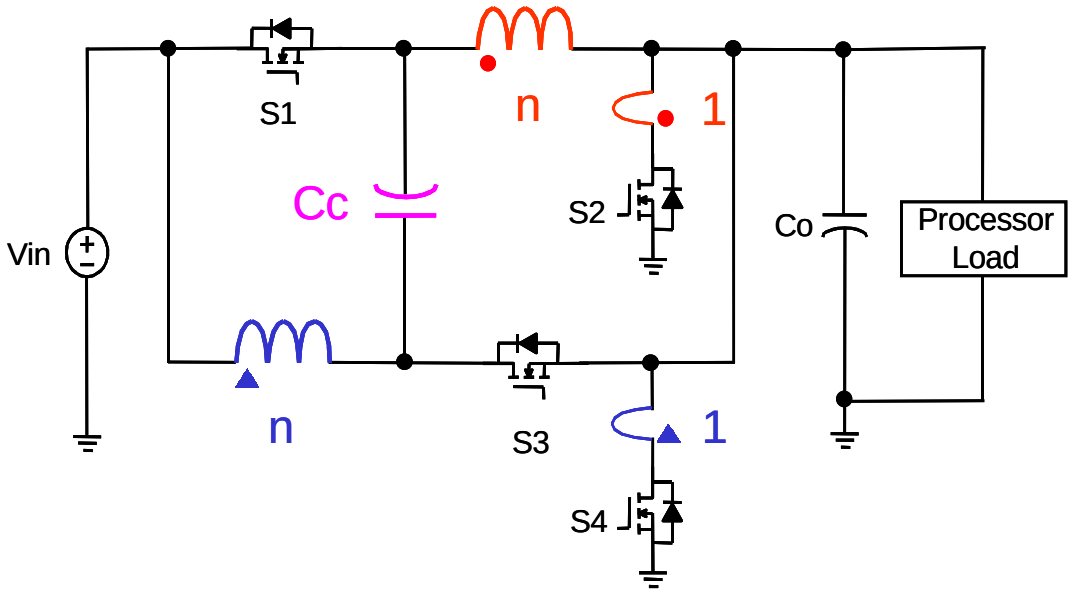



Figure 2.14. Active clamping circuits are formed between neighbor channels; however, the capacitor voltage is variable.

A modification is made in order to allow the clamping capacitor to have a constant voltage. The resulting topology, called the multiphase coupled-buck converter, is shown in Figure 2.15.

As shown in Figure 2.15, a third winding is coupled with the output inductor of the neighbor channel and is placed in series with the existing top winding. The voltage

induced in the third winding compensates the voltage of the existing top winding in the neighbor channel, and therefore, the clamping capacitor appears as a constant voltage, which equals the input voltage minus the output voltage. The detailed operation principle will be given in Section 3.3.2.

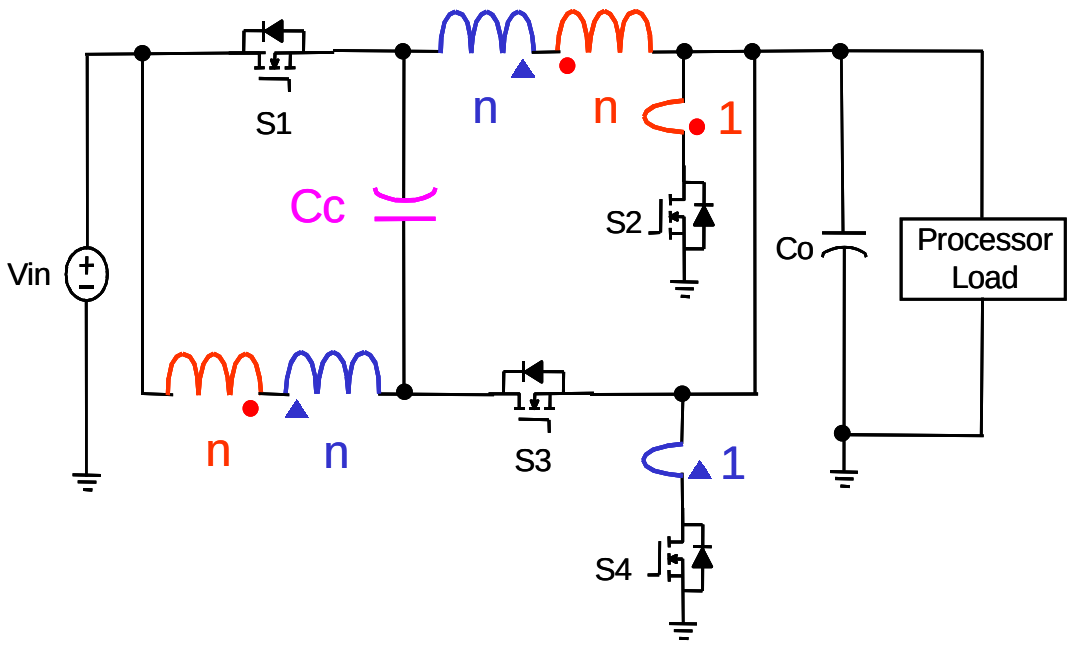



Figure 2.15. Proposed multiphase coupled buck converter.

### 2.3.2. Principle of Operation

Figure 2.16 shows the simplified circuit used for steady-state analysis. The clamping capacitor is assumed to have a large capacitance enough to be treated as a voltage source. The coupled output inductors have three windings, and are modeled as a three-winding transformer paralleled with a discrete inductor. All the semiconductor devices are treated as ideal switches.

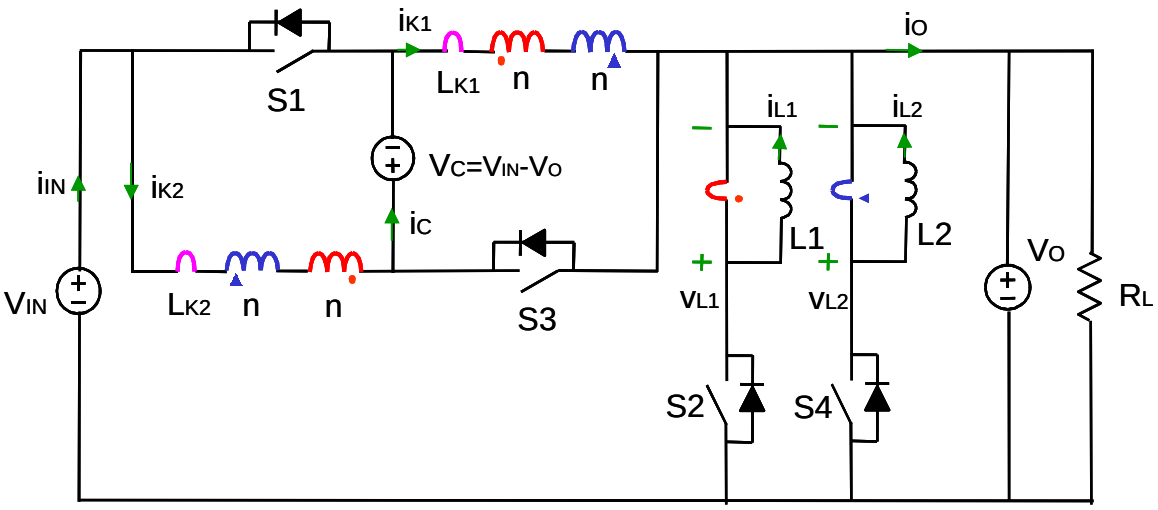



Figure 2.16. Simplfied multiphase coupled-buck converter for steady-state analysis.

Figure 2.17 shows the key operation waveforms. The four operation stages in a half switching cycle correspond to the buck mode, the leakage energy recovery mode, the freewheeling mode, and the leakage current reset mode. The other half switching cycle has the same operation stages.

As can be seen from Figure 2.17, the proposed multiphase coupled buck converter is immune to the leakage inductance. The drain-source voltages of the top switches are clamped to two times the level of the input voltage minus the output voltage. For 12-input VRMs, the best-available 30V MOSFETs have sufficient safety margins to be used as the top switches.

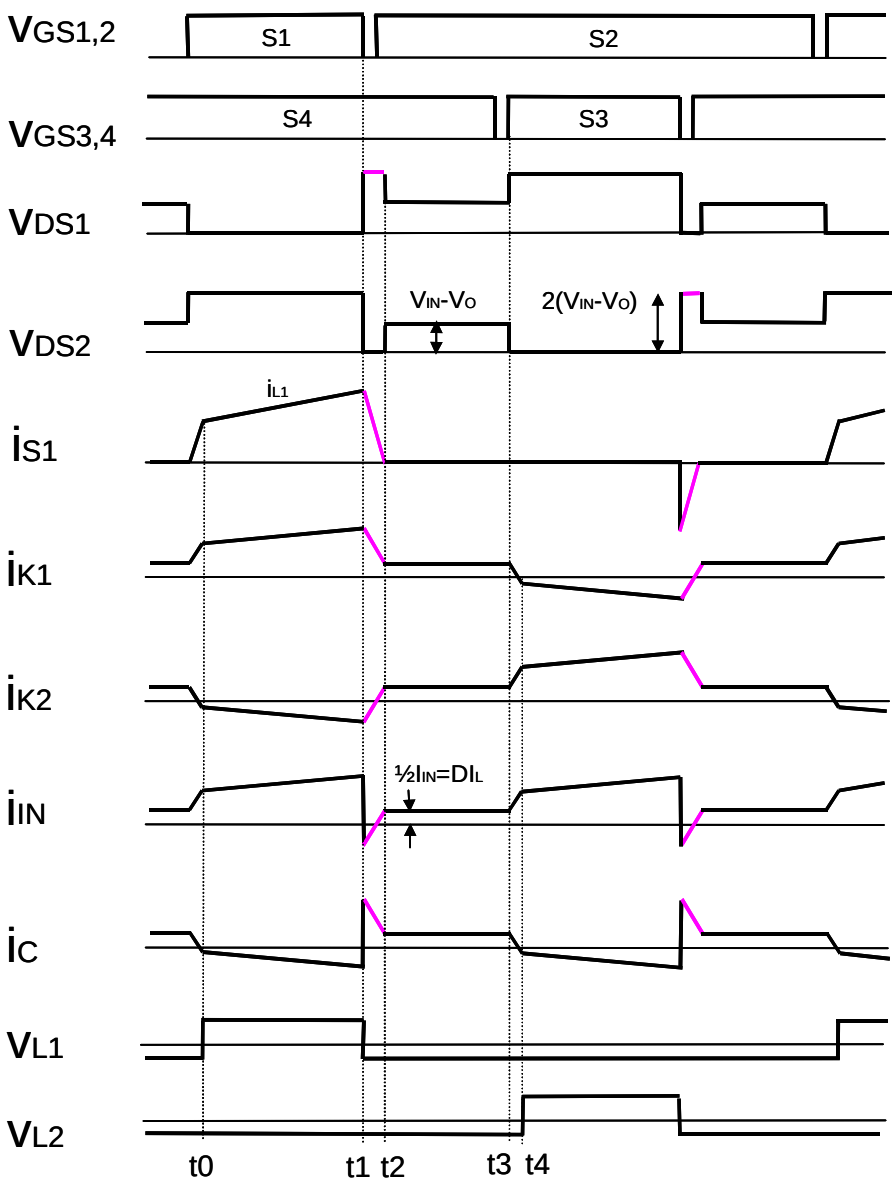



Figure 2.17. Key operation waveforms of the multiphase coupled-buck converter.

Figure 2.18 shows the equivalent circuits for the different stages. The operation during these stages can be briefly described as follows.

Stage I (t0-t1) corresponds to the buck mode. As shown in Figure 2.18(a), S1 is on, S2 is off, S3 is off, and S4 is on. The input source and the clamping capacitor feed energy to the output through output inductor L1. Inductor L2 is freewheeling. The stage ends when the control signals turn S1 off and S2 on.

Stage II (t1-t2) corresponds to the leakage energy recovery mode. As shown in Figure 2.18(b), S1 is off, S2 is on, the body diode of S3 is on, and S4 is on. The drain-source voltage of S1 is clamped to the sum of the clamping voltage and the input voltage. The leakage energy is recovered to the clamping capacitors. Inductors L1 and L2 are both freewheeling. The stage ends when the body diode of S3 turns off.

Stage III (t2-t3) corresponds to the freewheeling mode. As shown in Figure 2.18(c), S1 is off, S2 is on, S3 is off, and S4 is on. Inductors L1 and L2 are both freewheeling. The input voltage feeds energy to the clamping capacitor in order to maintain the balance of the charge in the clamping capacitor. The stage ends when a control turns S3 on.

Stage IV (t3-t4) corresponds to the leakage current reset mode. As shown in Figure 2.18(d), S1 is off, S2 is on, S3 is on, and S4 is on. Inductors L1 and L2 are both freewheeling. The current in S3 increases. The stage ends when the current in S3 reaches the level of the output inductor current. Then, Stage I begins again.

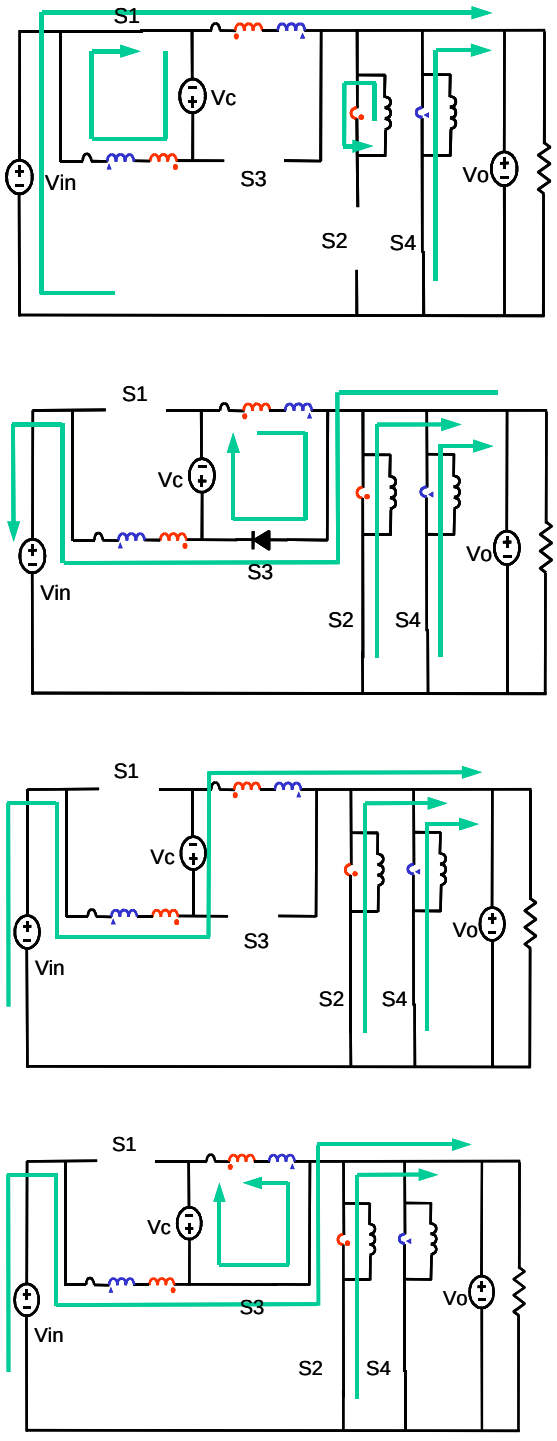



Figure 2.18. Equivalent circuits of the multiphase coupled-buck converter: (a) Stage I, (b) Stage II, (c) Stage III and (d) Stage IV.

### 2.3.3. Design Considerations for Turns Ratio and Duty Cycle

According to the steady-state operation waveforms shown in the previous section, the DC voltage gain of the multiphase coupled-buck converter can be obtained as follows:

$$\frac{V_O}{V_{IN}} = \frac{D}{D+n}. \tag{2.14}$$

Figure 2.19 shows the DC voltage gain of the multiphase coupled-buck converter as a function of the duty cycle D and the turns ratio n. The DC voltage gain of the multiphase buck converter is also included for comparison. For a VRM stepping down from 12 V to 1.5 V, the multiphase coupled-buck converter operates at a duty cycle of 0.286 with the turns ratio n=2, while the duty cycle of the multiphase buck converter is only 0.125.

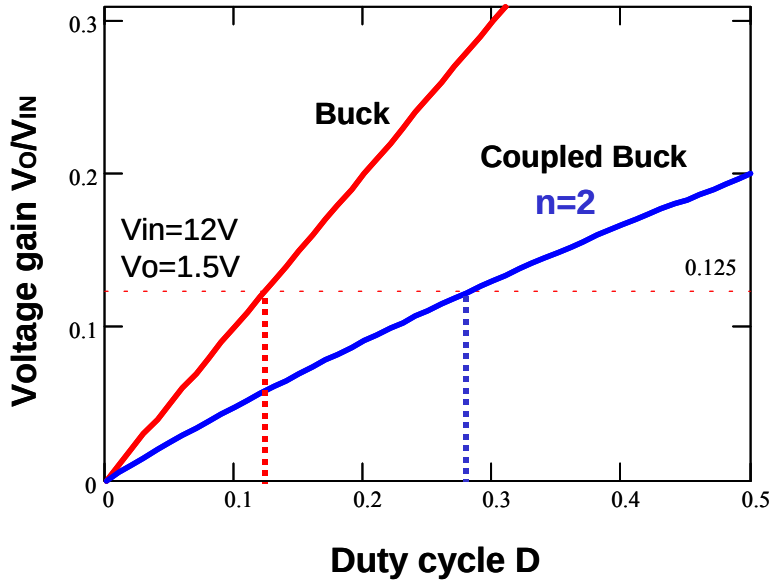



Figure 2.19. DC voltage gain of multiphase coupled buck converter as a function of the duty cycle D and the turns ratio n.

The design of the turns ratio in the multiphase coupled-buck converter is the same as that in the multiphase tapped-inductor buck converter. The desirable turns ratio is related to the transient reponses. As discussed in Section 2.2.1, from the efficiency standpoint, it is desirable to choose a high turns ratio in order to achieve a larger duty cycle. However, from the transient standpoint, with the increase of the turns ratio the step-up transient becomes slower than the step-down transient, which impairs the overall transient performance. Therefore, the optimum turns ratio is chosen to achieve the same transient inductor slew rates for both step-up and step-down transients.

Assume that the output inductance is designed according to the critical inductance in order to achieve the fastest transient response; the duty cycle would barely become saturated during transient responses.

The inductor slew rate during the step-up transient can be derived as follows:

$$\frac{di_L}{dt} = \frac{V_{IN} - (2n+1)\cdot V_O}{2n\cdot(1 - V_{IN}/V_O)\cdot L_O}, \tag{2.14}$$

where $L_O$ is the inductance value of the coupled inductor reflected to the low-turns winding.

The inductor slew rate during the step-down transient can be derived as follows:

$$\frac{di_L}{dt} = -\frac{V_O}{L_O}. \tag{2.15}$$

Equalizing Equations 2.14 and 2.15, the optimum turns ratio for the multiphase coupled-buck converter can be obtained as follows:

$$n = \frac{1 - V_O / V_{IN}}{2 \cdot V_O / V_{IN} \cdot (2 - V_O / V_{IN})}. \tag{2.16}$$

As can be seen from Equation 2.16, the optimum turns ratio is related only to the ratio between the input and output voltages.

Figure 2.20 shows the transient inductor slew rates as a function of the turns ratio n. For a VRM stepping down from 12 V to 1.5 V, the optimum turns ratio is 2:1.

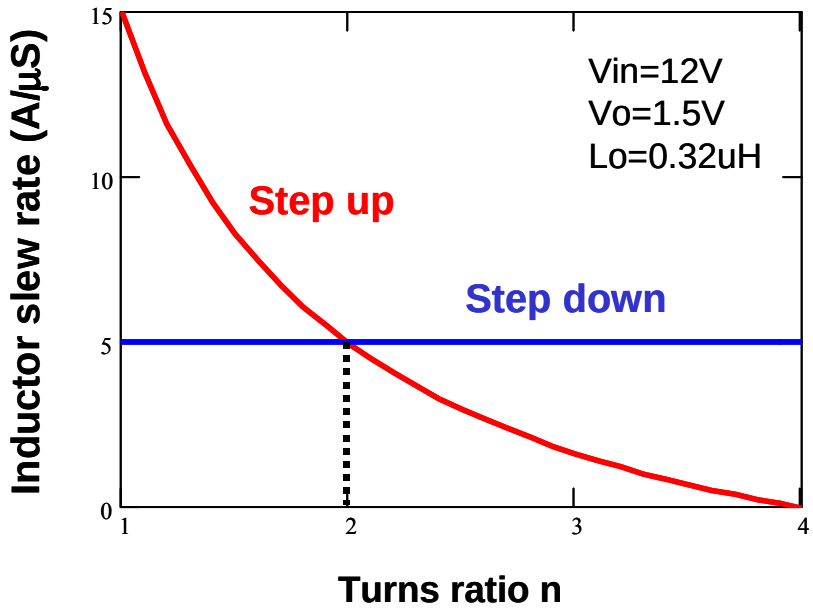



Figure 2.20. Inductor slew rates (during step-up and step-down transients for the multiphase coupled-buck converter) as a function of the turns ratio n.

### 2.3.4. Efficiency Evaluation and Experimental Results

With extended duty cycle, the multiphase coupled-buck converter is expected to have a higher efficiency than the multiphase buck converter. In order to illustrate this efficiency improvement, the major losses from MOSFETs, inductors, input capacitors, clamping capacitors and output capacitors are analyzed and quantified. The loss formulas for multiphase coupled-buck converter are similar to those for the multiphase buck converter in Section 2.1.3, except for the different magnitudes of some voltages and currents.

The top MOSFET operates under hard-switching conditions. Its losses $P_{Q1}$ consist of conduction loss $P_{ON}$, switching loss $P_{SW}$, and gate driving loss $P_{DR}$. They can be approximated and derived as follows:

$$P_{Q1} = P_{ON} + P_{SW} + P_{DR}$$

$$P_{ON} = I_D^2 \cdot R_{DS} = \frac{1}{n^2}\left(I_{LCH}^2 + \frac{\Delta I_{LCH}^2}{12}\right) \cdot D \cdot R_{DS}$$

$$P_{SW} = V_{DS1} \cdot \frac{I_{LV}}{n} \cdot T_{ON} \cdot F_S + V_{DS1} \cdot \frac{I_{LP}}{n} \cdot T_{OFF} \cdot F_S \,, \qquad (2.17)$$

$$T_{ON} = \frac{Q_{TH}}{V_{TH}} \cdot R_G \cdot \ln\left(\frac{V_{DR} - V_{GS1}}{V_{DR} - V_{TH}}\right) + \frac{Q_{GD} \cdot R_G}{V_{DR} - V_{GS1}}$$

$$T_{OFF} = \frac{Q_{TH}}{V_{TH}} \cdot R_G \cdot \ln\left(\frac{V_{GS2}}{V_{TH}}\right) + \frac{Q_{GD} \cdot R_G}{V_{GS2}}$$

$$P_{DR} = Q_G \cdot V_{DR} \cdot F_S$$

where $I_{LCH}$, $\Delta I_{LCH}$, $I_{LV}$ and $I_{LP}$ are the channel inductor average current, peak-to-peak ripple current, valley current and peak current, respectively. n is the turns ratio of the coupled inductors, which is defined in Figure 2.15. $V_{DS1}$ is the turn-off voltage of the top MOSFET, which is equal to $V_{IN}-V_O$. $R_{DS}$ is the on-resistance of the top MOSFET. $Q_{TH}$, $Q_{GS1}$ and $Q_{GS2}$ are the gate-source charges at $v_{GS}=V_{TH}$, $V_{GS1}$ and $V_{GS2}$, respectively. Here, $V_{GS1}$ and $V_{GS2}$ are the gate-source voltages required to support the load currents $i_{LV}$ and $i_{LP}$, respectively, as read from the MOSFET transconductance characteristics ($i_D$ vs. $V_{GS}$ curves). $Q_{GD}$ and $Q_G$ are the gate-drain charge and total gate charge, respectively. $V_{DR}$ is the gate supply voltage. $R_G$ is the gate resistance, including the MOSFET internal gate resistance.

The bottom MOSFET operates at synchronous rectification with zero-voltage switching. Its losses $P_{Q2}$ consist of conduction loss $P_{ON}$, body diode loss $P_{DB}$, and gate driving loss $P_{DR}$. They can be approximated and derived as follows:

$$P_{Q2} = P_{ON} + P_{DB} + P_{DR}$$

$$P_{ON} = I_Q^2 \cdot R_{DS} = \left(I_{LCH}^2 + \frac{\Delta I_{LCH}^2}{12}\right) \cdot (1 - D) \cdot R_{DS}$$

$$P_{DB} = P_{ON} + P_{RR} = (V_F \cdot I_{LV} \cdot T_{DEAD1} \cdot F_S + V_F \cdot I_{LP} \cdot T_{DEAD2} \cdot F_S) + Q_{RR} \cdot V_{DS2} \cdot F_S \quad ,(2.18)$$

$$P_{DR} = Q_G \cdot V_{DR} \cdot F_S$$

where $I_{LCH}$, $\Delta I_{LCH}$, $I_{LV}$ and $I_{LP}$ are the channel inductor average current, peak-to-peak ripple current, valley current and peak current, respectively. $V_{DS2}$ is the turn-off voltage

of the bottom MOSFET, which is equal to $(V_{IN}–V_O)/n$. $R_{DS}$ is the on-resistance of the top MOSFET. $T_{DEAD1}$ and $T_{DEAD2}$ are the dead times introduced by the gate drives and MOSFETs, which cause the body diode conduction loss. $Q_{RR}$ is the reverse-recovery charge of the body diode. $Q_G$ is the total gate charge. $V_{DR}$ is the gate supply voltage.

The inductor losses $P_{LO}$ consist of winding loss $P_{WIND}$ and core loss $P_{CORE}$. They are based on finite element simulations and empirical formulas derived as follows:

$$P_{LO} = P_{WIND} + P_{CORE}$$

$$P_{WIND} = \sum_i [I_{DCi}^2 + \gamma_i \cdot (I_{RMSi}^2 - I_{DCi}^2)] \cdot R_{DCi}\,, \tag{2.19}$$

$$P_{CORE} = \sum_i C \cdot F_S^{\alpha} \cdot \Delta B_i^{\beta} \cdot V_{COREi}$$

where $I_{DCi}$ and $I_{RMSi}$ are individual winding DC current and RMS current, respectively. $R_{DCi}$ is the DC resistance of windings. $\gamma_i$ is the ratio of the AC resistance and DC resistance of the windings. C, $\alpha$ and $\beta$ are the empirical parameters for core loss, given by the manufacturer of the core material. $\Delta B_i$ and $V_{COREi}$ are the flux density and the corresponding core volume for different core regions, as read from finite element simulations.

The loss in output capacitors $P_{CO}$ is caused by the RMS current on the ESR of the output capacitors, and can be derived as follows:

$$P_{CO} = I_{RMS}^2 \cdot ESR\,, \tag{2.20}$$

where $I_{RMS}$ is the RMS current going through the output capacitors.

The loss formulas for input capacitors and clamping capacitors are the same, because both have the same current waveforms. Their loss, $P_{CIN}$, can be derived as follows:

$$P_{CIN} = I_{RMS}^2 \cdot ESR$$

$$I_{RMS} = \frac{I_O}{2}\sqrt{(D-\frac{m}{N})(\frac{m+1}{N}-D)+\frac{N}{12}(\frac{\Delta I_{LCH}}{D\cdot I_O})^2[(m+1)^2(D-\frac{m}{N})^3+m^2(\frac{m+1}{N}-D)^3]}\,, \tag{2.21}$$

where $I_O$ and $\Delta I_{LCH}$ are the load current and the channel peak-to-peak inductor current, respectively. $m = \text{floor}(N \cdot D)$ is the maximum integer that does not exceed the $N \cdot D$.

Based on the preceding loss analysis, the loss contributions of the major components are given for a typical four-phase coupled buck VRM. Hardware is also built in order to demonstrate the efficiency improvement. For a fair comparison, the four-phase coupled-buck VRM is designed with the same MOSFETs, input capacitors and output capacitors, and operates at the same conditions as the four-phase buck VRM described in Section 2.1.3. The switching frequency is 300 KHz. The input voltage is 12 V, and the output voltage and current are 1.5 V and 50 A, respectively. The top and bottom switches use Si4884DY and Si4874DY, respectively, both of which are from Siliconix. The output capacitors consist of six Sanyo 4V, 820μF OSCON capacitors, and the input capacitors consist of three Sanyo 16V, 270μF OSCON capacitors.

Figure 2.21 shows the loss contributions at full load for the four-phase coupled buck VRM and the four-phase buck VRM. The main loss differences are due to the switching loss of the top switches and the conduction loss of the bottom switches. The losses from the other components are almost the same. The coupled-buck VRM has 1 W more conduction loss from the bottom switches than the buck VRM, but 5 W lower switching loss from its top switches. Compared to the buck VRM, the overall loss reduction for the coupled-buck VRM is 4 W, which corresponds to a 4 % efficiency improvement.

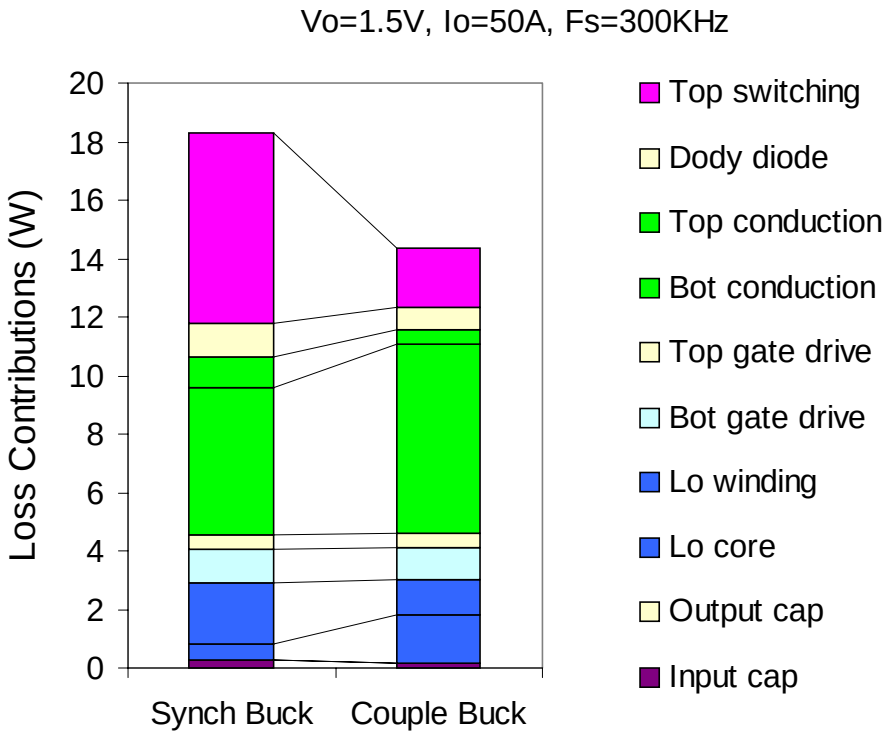
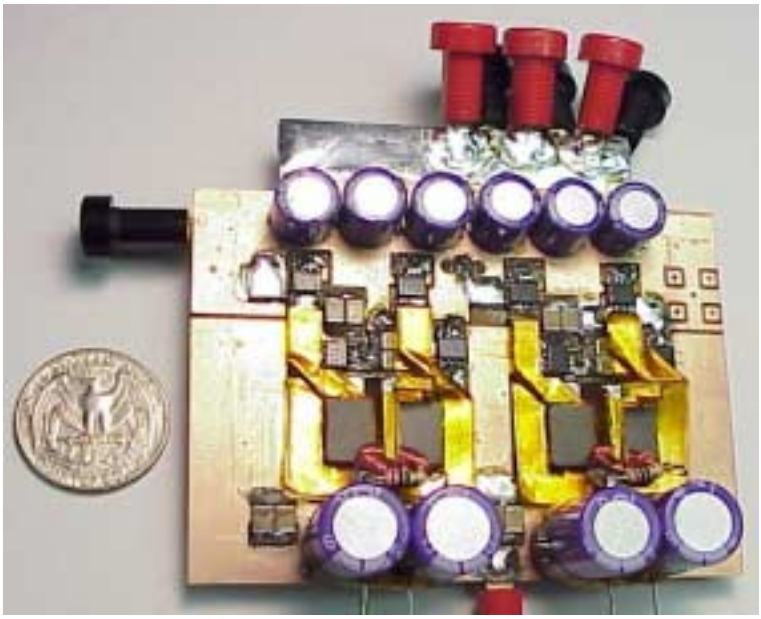
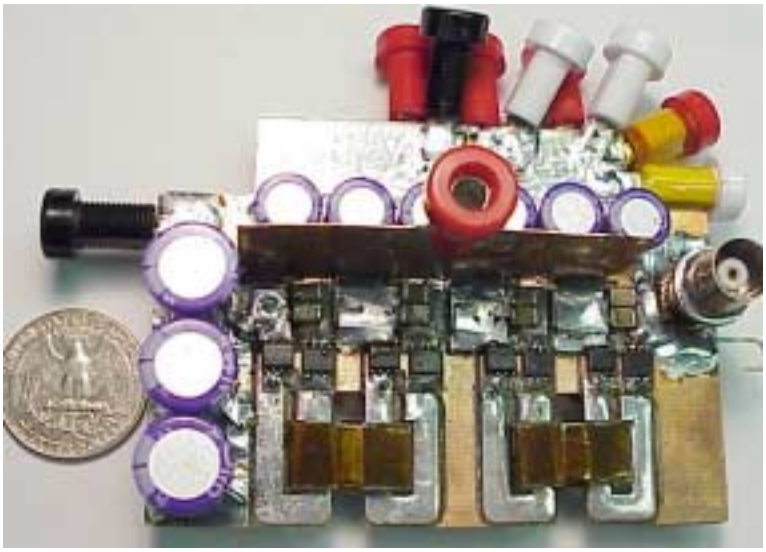



Figure 2.21. Loss contributions at full load for four-phase coupled-buck VRM and four-phase buck VRM.

Figure 2.22 shows the hardware pictures of the four-phase coupled-buck VRM and the four-phase buck VRM.



(a)



(b)

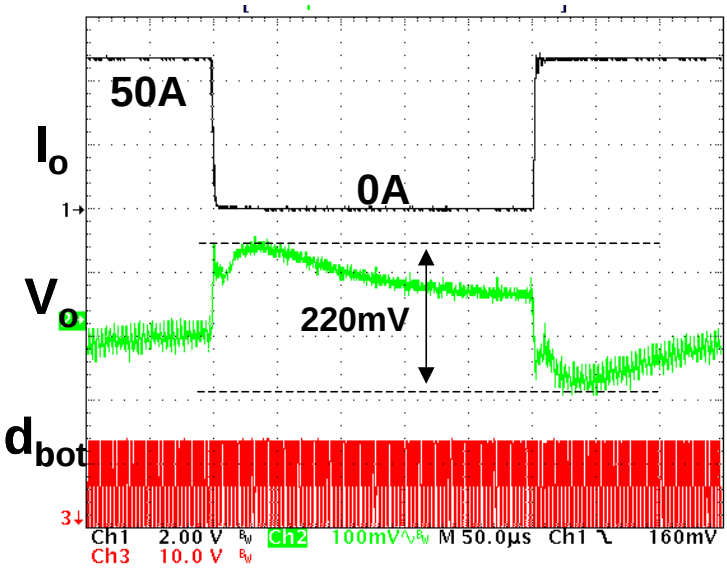
Figure 2.22. Hardware pictures: (a) the four-phase coupled-buck VRM, and (b) the four-phase buck VRM.

In order to make the efficiency comparison between the multiphase coupled-buck converter and the multiphase buck converter meaningful, the design of the inductors is based on the same transient.

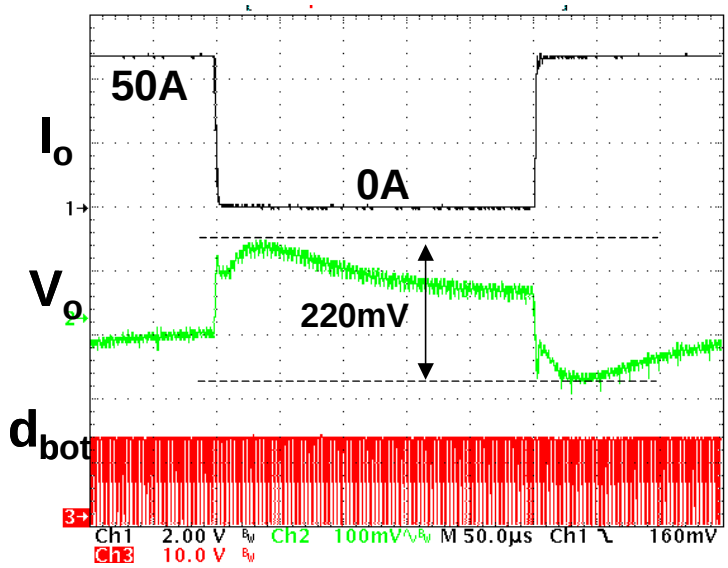
In order to design the four-phase coupled-buck VRM so that it has the same transient response as the four-phase buck VRM, the inductance value reflected to the bottom winding in the four-phase coupled-buck VRM is designed to be 320 nH, which is the same as the output inductance of the four-phase buck VRM.

The implementation of inductors in the four-phase buck VRM is similar to that in the four-phase buck VRM. Two pairs of the same E18/4/10 and PLT 18/10/2 cores are used with the same 3F3 core material. The two channels with phase shifts of $0^o$ and $180^o$ share a pair of cores, while the other two channels with phase shifts of $90^o$ and $270^o$ share another pair of cores. The two outer legs of the E core are milled to generate the air gaps, and no air gap exists in the center leg. The turns ratio of the coupled inductors is 2:1 as discussed in the previous section. Each coupled inductor has three windings. Both top windings have two turns, and the bottom winding has only one turn. Two top windings are built on each side of the double-sided PCB. The bottom winding is made of two layers of paralleled copper foils, each of which is placed on top of the two-turns windings.

Figure 2.23 shows the transient responses of the four-phase coupled-buck VRM and the four-phase buck VRM. The two VRMs have the same transient waveforms, as expected.




(a)




(b)

Figure 2.23. The same transient response is found in (a) the four-phase coupled buck VRM and (b) the four-phase buck VRM.

Figure 2.24 shows the measured efficiency of the four-phase coupled-buck VRM and the four-phase buck VRM.

As can be seen from Figure 2.24, for the four-phase coupled-buck VRM, the full-load efficiency is more than 85%, and the highest efficiency is 89%. Compared to the four-phase buck VRM, the four-phase coupled-buck VRM has an efficiency improvement of about 3.5% at full load and 4.5% at the highest point of efficiency.

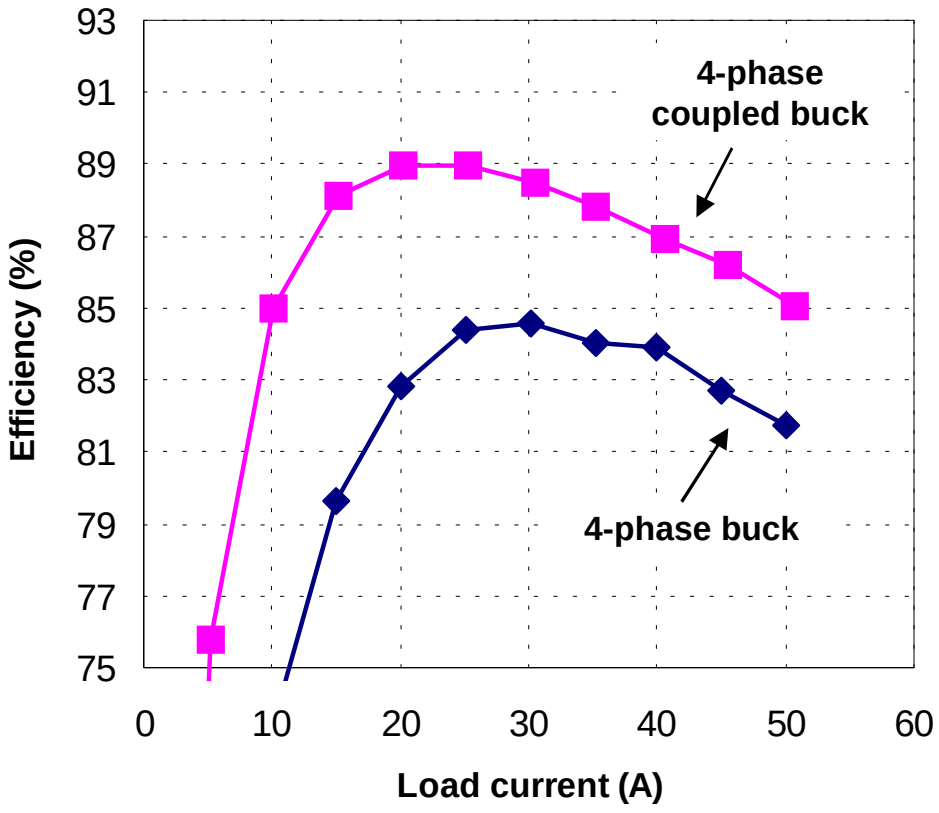



Figure 2.24. The four-phase coupled-buck VRM has a higher efficiency than the four-phase buck VRM.

## 2.4. CONCEPT EXTENSION FOR OTHER APPLICATIONS

For higher-power server-type applications, microprocessors are often driven by VRMs with 48V input. Without the isolation requirement, the proposed multiphase coupled-buck converter can be applied with a suitable turns ratio. However, isolation is often required for 48V VRMs that are used in distributed power systems. For such applications, isolation topologies are needed.

The isolated counterpart of the multiphase buck converter is the push-pull converter with the current-doubler rectifier. As shown in Figure 2.25, a transformer can be placed in the two-phase buck converter, and the resulting topology is the conventional push-pull converter with the current-doubler secondary side.

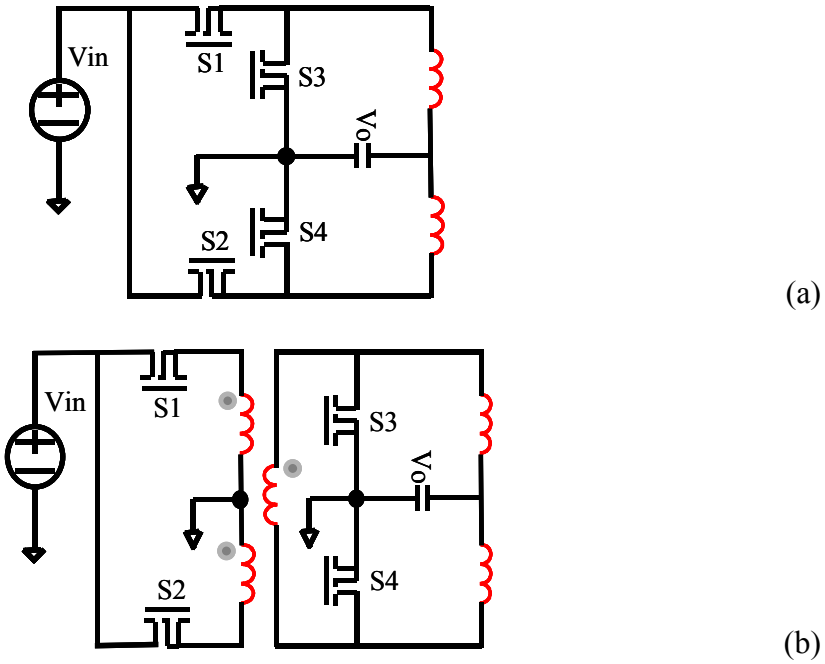



Figure 2.25. (a) The two-phase buck converter, and (b) its isolated counterpart – the push-pull converter with the current-doubler rectifier.

Correspondingly, the isolated counterpart exists for the multiphase coupled-buck converter, and it can be derived as follows.

First, the proposed multiphase coupled-buck converter can be redrawn with labeled winding terminals, as shown in Figure 2.26. Each channel has a three-winding coupled inductor.

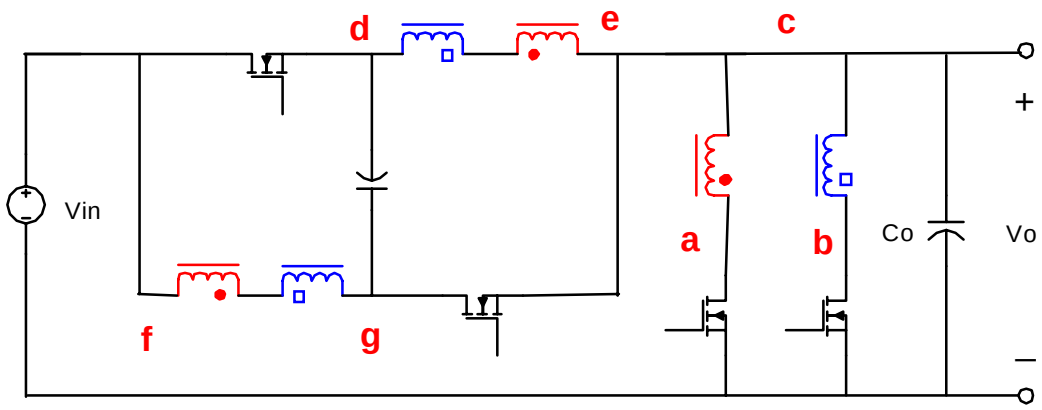



Figure 2.26. Multiphase coupled-buck converter with labeled winding terminals.

In the multiphase coupled-buck converter, the configuration of coupled inductors can be extracted and drawn as shown in the left side of Figure 2.27. Since the coupled inductor can be modeled as a transformer paralleled with an inductor, the configuration of coupled inductors is equivalently interchangeable with the configuration shown in the right side of Figure 2.27, which uses discrete transformers and inductors instead of coupled inductors.

The two configurations shown in Figure 2.27 are interchangeable. The left side shows the configuration of coupled inductors. The red windings correspond to one coupled

inductor, and the blue windings correspond to the other coupled inductor. The right side shows the equivalent configuration using transformers and inductors. The pink windings correspond to a three-winding transformer. The red and blue windings represent two discrete inductors. The configuration shown in the right side is composed of one transformer and two inductors, which actually is the popular current-doubler structure.

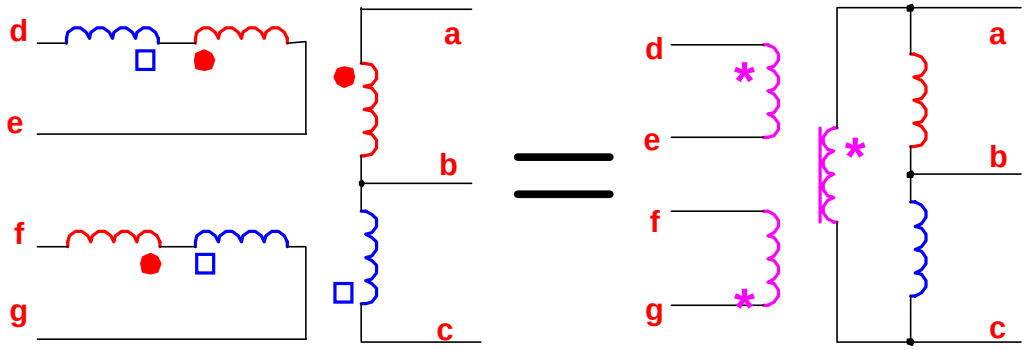



Figure 2.27. Interchangeable configuration using discrete transformers and inductors instead of coupled inductors.

Replacing the configuration using discrete transformers and inductors into Figure 2.26, one variation of the multiphase coupled-buck converter can be derived, as shown in Figure 2.28(a).

In Figure 2.28(a), if node "e" is connected to "GND" instead of "OUTPUT," the modified topology (as shown in Figure 2.28(b)) becomes the push-pull forward converter with the current-doubler rectifier. Figure 2.29 shows the more familiar drawing for the push-pull forward topology with the current-doubler secondary.

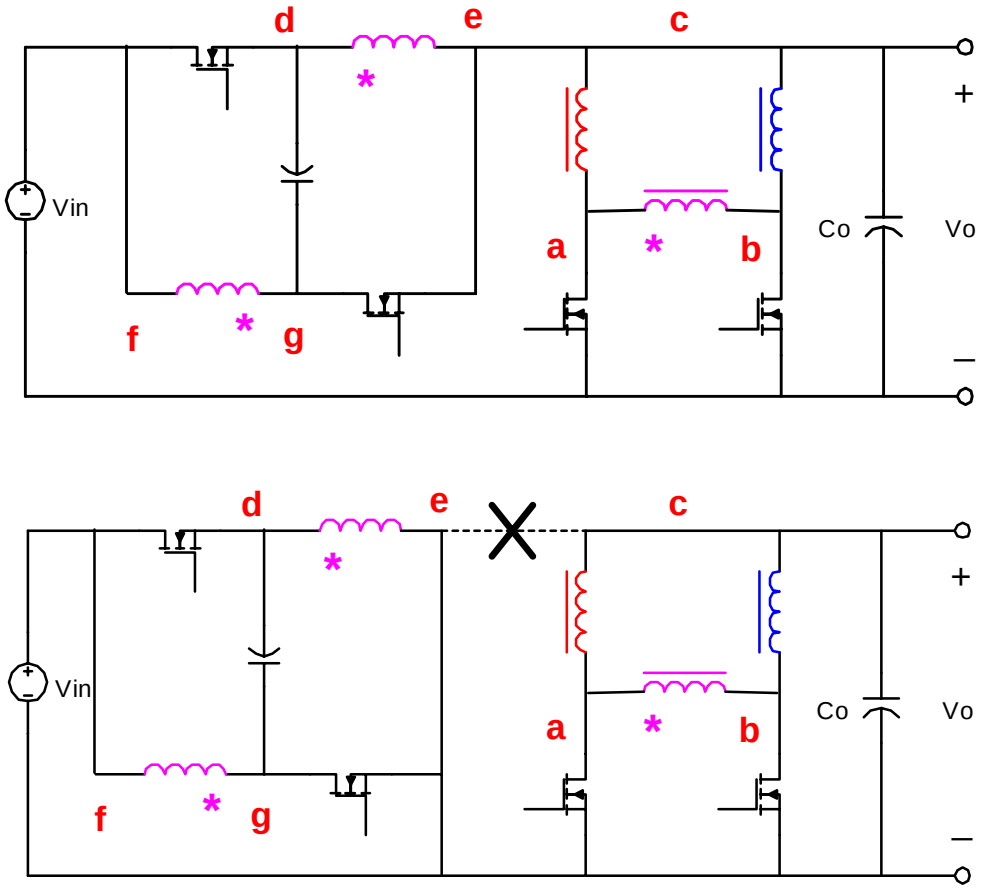



Figure 2.28. (a) Two-phase coupled-buck converter, and (b) its isolated counterpart – the push-pull forward converter with the current-doubler rectifier.

The active-clamping concept in the proposed multiphase coupled-buck converter can be extended to the push-pull forward converter. As shown in Figure 2.29, after Q1 turns off, the current in the leakage inductance forces the body diode of Q2 to conduct. The drain-source voltage of Q1 is clamped to the input voltage plus the clamping capacitor voltage, and the leakage energy is transferred to the clamping capacitors Cs. The energy stored in the clamping capacitors is released to the load when Q2 turns on in the following switching cycle.

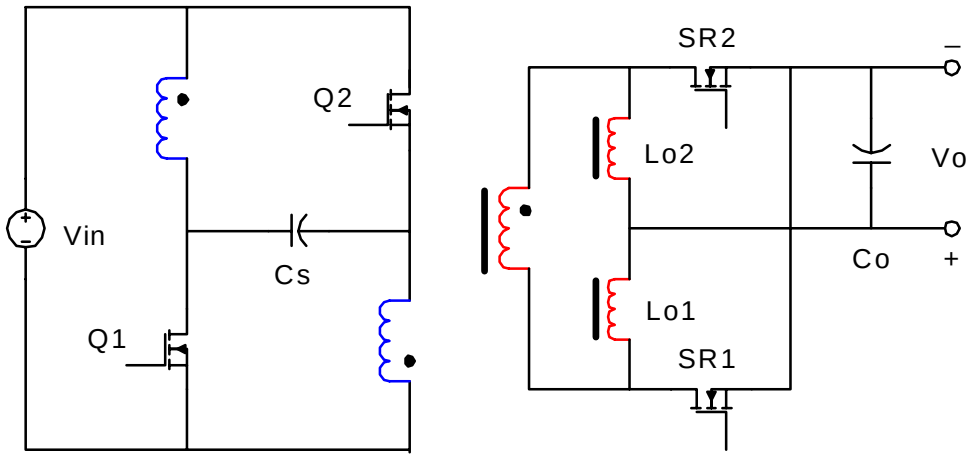



Figure 2.29. Push-pull forward converter with the current-doubler rectifier.

The advantages of the multiphase coupled-buck converter over the multiphase buck converter can also be extended to their isolated counterparts. Compared with the push-pull converter, the push-pull forward converter has clamped device voltages and recovered leakage energy. The efficiency of the push-pull forward converter is expected to be higher than that of the push-pull converter.

Hardware is built for both the push-pull converter and the push-pull forward converter in order to demonstrate these advantages. Both test conditions are $V_{IN}$ = 48 V, $V_O$ = 1.2 V, $I_O$ = 70A, and $F_S$ = 100kHz. For a fair comparison, both are designed with the same power MOSFETs and output inductance. Each of the two primary switches uses PSMN035-150B (150 V, 35 mΩ) from Philips Semiconductor, and each of the two secondary switches uses 2 X STV160NF03L (30 V, 3 mΩ) from ST Microelectronics. The output inductance is 360 nH.

Figure 2.30 shows the measured power-stage efficiency. The push-pull forward converter can achieves a 90.5% ceiling efficiency and an 85% full-load efficiency. Compared to the push-pull converter, the push-pull forward converter has more than 3% efficiency improvement.

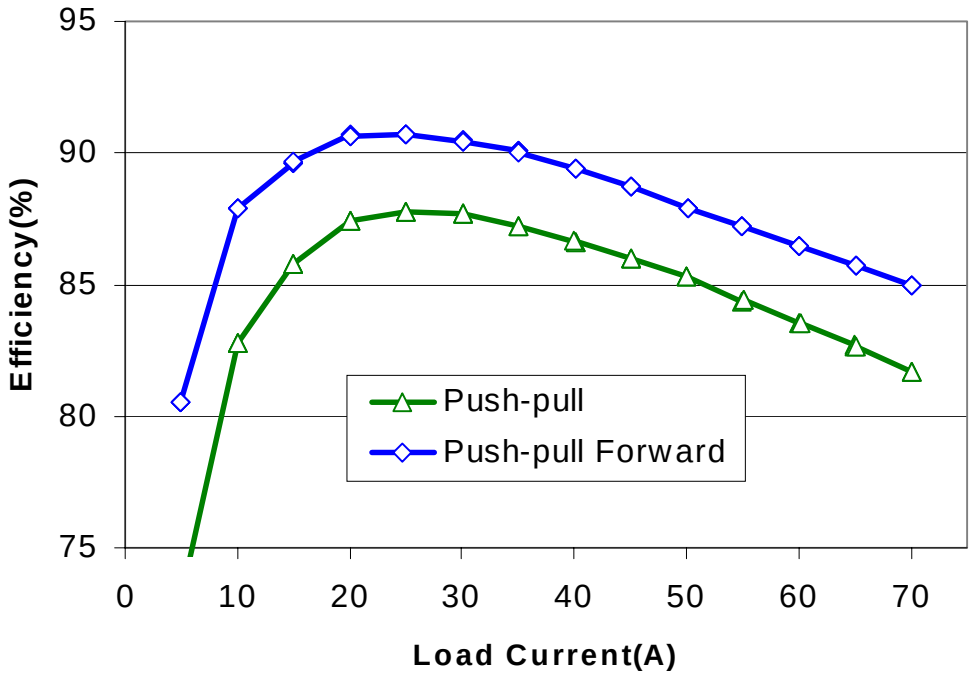



Figure 2.30. Measured power-stage efficiency for both the push-pull and the push-pull forward VRMs.

## 2.5. SUMMARY

Today's multiphase VRMs are almost universally based on the buck topology. With increased voltage and decreased output voltage, the multiphase buck converter suffers from a extremely small duty cycle. It is very difficult for multiphase buck converter to achieve a desirable efficiency while providing a fast transient response. Loss analysis indicates that the efficiency drop is mainly caused by the switching loss of the top switches when the duty cycle is reduced.

In order to improve the efficiency without compromising the transient performance, the multiphase tapped-inductor buck converter has been explored, which employs multi-winding coupled inductors to extend the duty cycle. Under the same transients, the multiphase tapped-inductor converter has a much larger steady-state duty cycle, and consequently, it has a higher efficiency than does the multiphase buck converter. However, the multiphase tapped-inductor buck converter suffers from a voltage spike problem caused by the leakage inductance between the coupled windings.

An improved topology, named the multiphase coupled-buck converter, has been proposed. This innovative topology enables the use of a larger duty cycle with a clamped and coupled structure. Therefore, the leakage energy can be recovered and the voltage spike across the device can be clamped. With the extended duty cycle, the multiphase coupled-buck converter has a significantly lower switching loss for the top switches than does the multiphase buck converter. Both analyses and experiments have proved that

under the same transients, the multiphase coupled-buck converter has an efficiency that is significantly better than that of the multiphase buck converter.

The concept proposed for the multiphase coupled-buck converter can be extended to isolation applications. Correspondingly, the benefits of the multiphase coupled-buck converter can also be extended to its isolated counterpart, which is the push-pull forward converter with the current-doubler rectifier. Compared to the isolated counterpart of the multiphase buck converter - the push-pull converter, the push-pull forward converter has clamped device voltage and recovered leakage, and therefore a higher efficiency.