CVR College of Engineering Faculty Development Program

Wide Bandgap Power Electronics Impacts and Challenges to EV and PV Technologies

February 27, 2021
Hyderabad, India

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Outline

- Background
- WBG Devices and Their Figure of Merits
- Applications and Challenging Issues
  - EV Motor Drive Inverters
  - PV Converters
  - Dead-Time Issues
- Discussion and Conclusion

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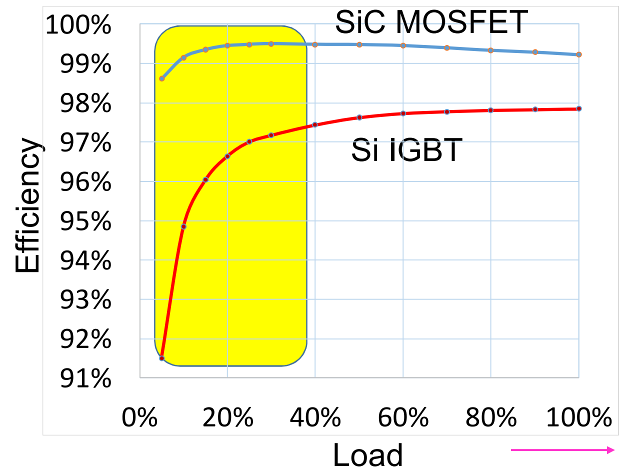
A Commercial Product Using SiC Device



- An example commercial product using WBG device – SiC MOSFET based EV inverter has demonstrated significant motor drive efficiency.
- Especially at light loads, the loss is reduced by >80% ➔ a big gain on urban driving cycle

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A Commercial Product Using GaN Device

PC charger with Si devices – 120W
Weight: 340 g

PC charger with Si devices – 65W
Weight: 170 g

Universal charger with GaN devices – 65W
Weight: 50 g

- The example GaN based universal charger has demonstrated >70% size and weight reduction over the Si based PC chargers
- As GaN is still in its infant stage while Si is >65-year old, Future GaN performance is practically unimaginable

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Key Properties of Wide Band Gap (WBG) Semiconductors

Material	A. Band gap (eV)	B. Breakdown electric field (10^6·V/cm)	C. Electron mobility (cm^2/V·s)	D. Dielectric constant
Si	1.12	0.3	1350	11.8
SiC-4H	**3.26**	**3.0**	650	10.0
GaN	**3.4**	**3.3**	**2000**	9.5
β-Ga_2O_3	**4.5**	**7.0**	300	10
Diamond	**5.45**	**5.6**	1900	5.5
AlN	**6.1**	**11.7**	1100	8.7

- There are many factors for WBG materials to be superior to Si.
- Bandgap and breakdown e-field are the key factors. In fact these two are related.

Sources: 1. F. Ren and J.C. Zolper, *Wide Energy Bandgap Electronic Devices*, World Scientific, 2003
2. T. Igawa, "Unleashing the Potential of α-Ga_2O_3," IEEE CMPT Symposium, Japan, 2019.

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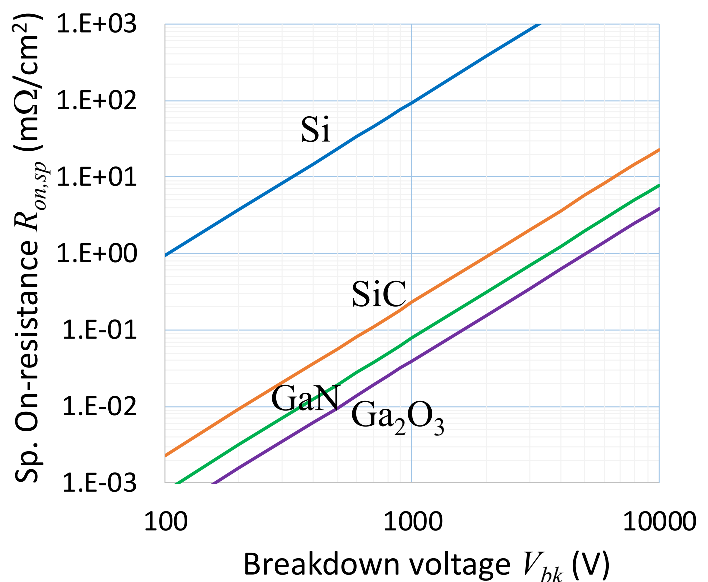
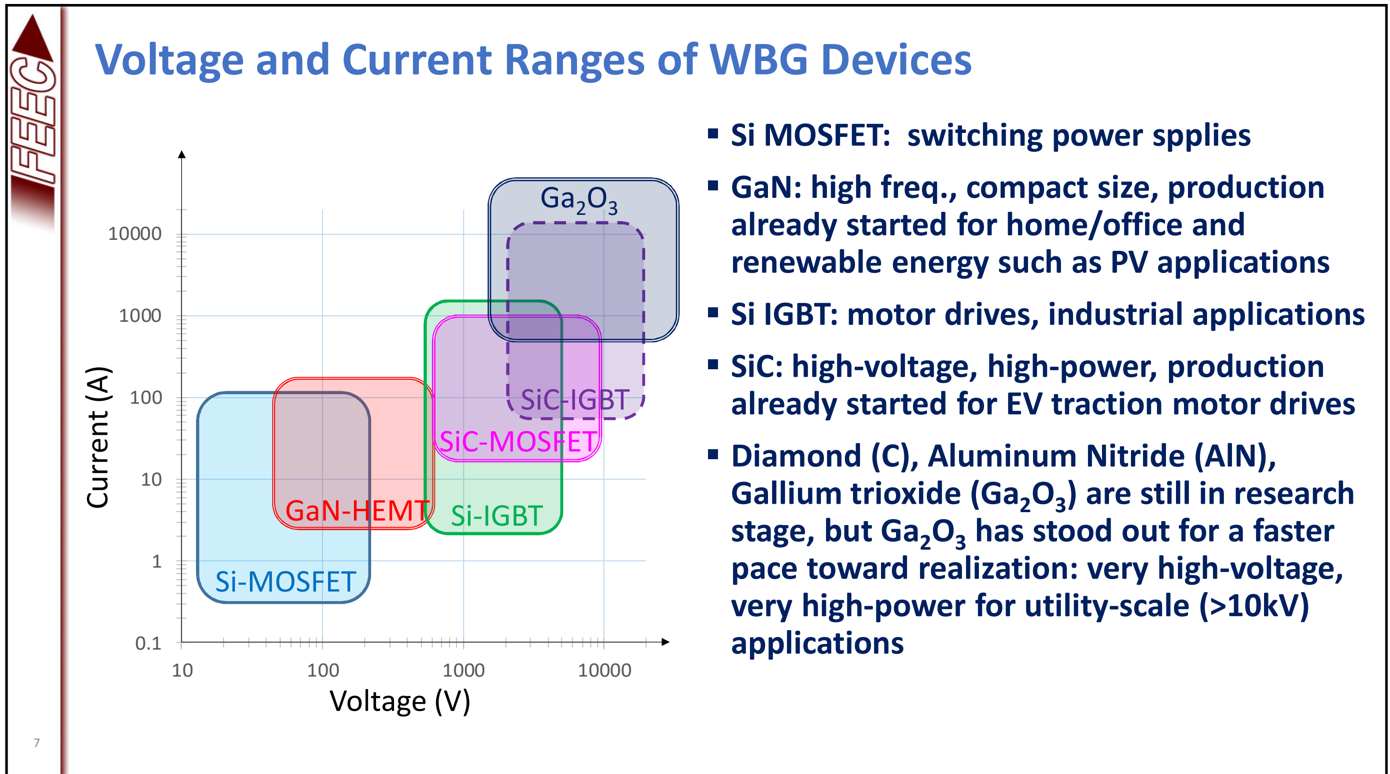
Power Figure of Merit (FOM) Based on Conduction Loss

$$\text{BFOM} = \varepsilon \cdot \mu \cdot E_C^3$$

$$R_{on,sp} = \frac{4V_{bk}^2}{\varepsilon \cdot \mu \cdot E_C^3}$$ ← BFOM

- **For a given breakdown voltage V_{bk}, lower on-drop resistance, better figure of merit (FOM)**
- **Without considering switching losses, power FOM can be compared with $R_{on,sp}$**
- **All WBG devices are showing orders of magnitude better than the Si device**





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Voltage and Current Ranges of WBG Devices
Current (A)
Voltage (V)
10000
1000
100
10
1
0.1
10
100
1000
10000
Ga_2O_3
SiC-IGBT
SiC-MOSFET
GaN-HEMT
Si-IGBT
Si-MOSFET
Si MOSFET: switching power spplies
GaN: high freq., compact size, production already started for home/office and renewable energy such as PV applications
Si IGBT: motor drives, industrial applications
SiC: high-voltage, high-power, production already started for EV traction motor drives
Diamond (C), Aluminum Nitride (AlN), Gallium trioxide (Ga_2O_3) are still in research stage, but Ga_2O_3 has stood out for a faster pace toward realization: very high-voltage, very high-power for utility-scale (>10kV) applications
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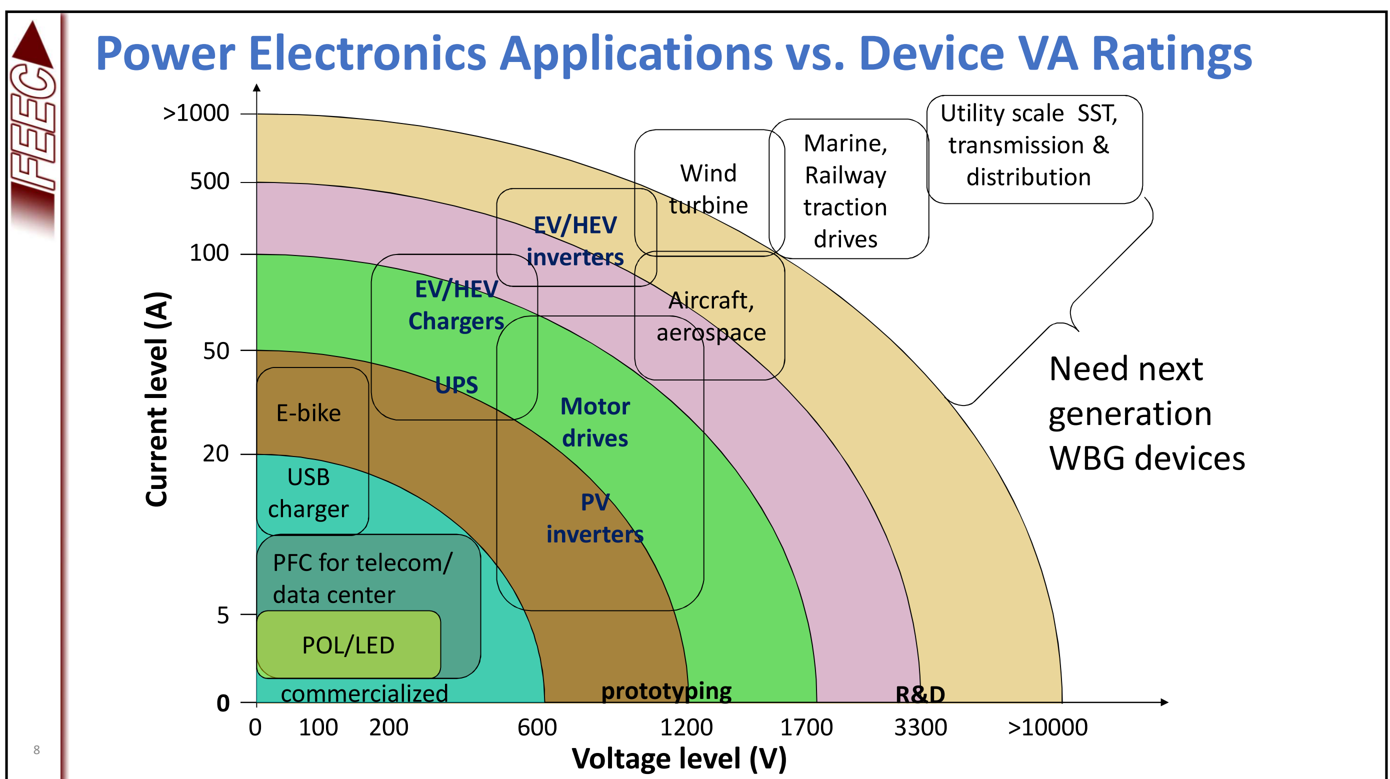

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Power Electronics Applications vs. Device VA Ratings
Current level (A)
Voltage level (V)
>1000
500
100
50
20
5
0
0
100
200
600
1200
1700
3300
>10000
Utility scale SST, transmission & distribution
Marine, Railway traction drives
Wind turbine
EV/HEV inverters
EV/HEV Chargers
Aircraft, aerospace
UPS
Motor drives
PV inverters
E-bike
USB charger
PFC for telecom/ data center
POL/LED
commercialized
prototyping
R&D
Need next generation WBG devices
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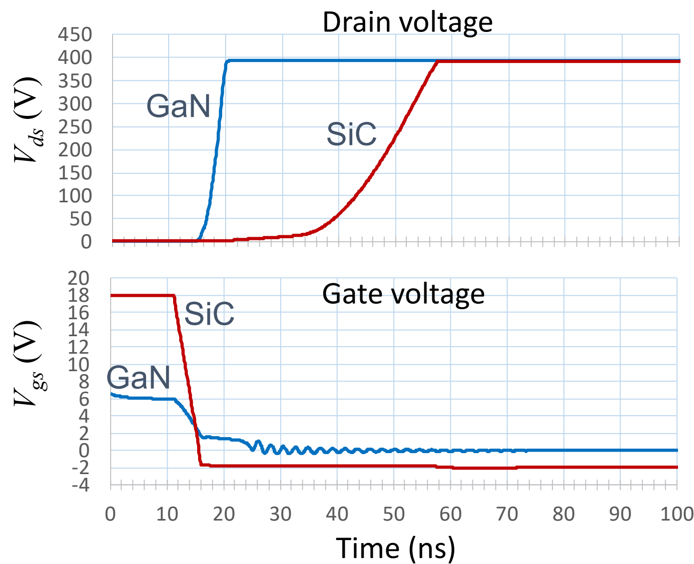
A Challenging Issue for Motor Drives – High dv/dt



- Dv/dt is related to the junction capacitance C_{oss}.
- As WBG device requires a smaller chip size for the same power rating, C_{oss} of WBG devices tends to be much lower as compared to Si devices.
- Simulation study shows dv/dt of SiC is about 20 V/ns and GaN is higher than 100 V/ns

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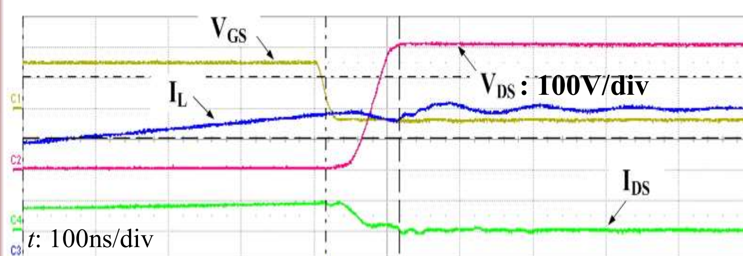
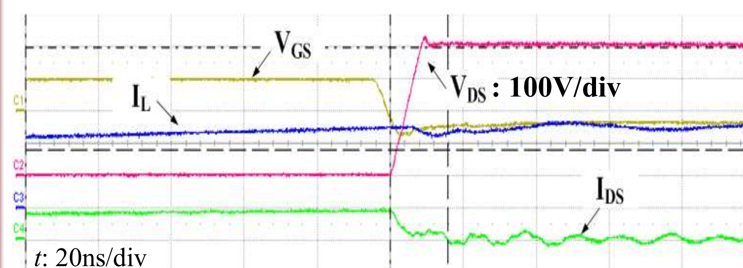
Experimental Verification of WBG Device Switching dv/dt

SiC MOSFET: SCT2120AF



GaN HEMT: TPS3002



- Experimental results show dv/dt of SiC is about 15 V/ns and GaN is about 90 V/ns. They are slightly slower due to parasitic inductance in the loop.
- As compared to Si IGBT typically at <10 V/ns, dv/dt caused by WBG devices will worsen
  - Voltages spikes induced by long cable transmission lines,
  - bearing circulating current,
  - capacitive coupled current,
  - EMI, etc.

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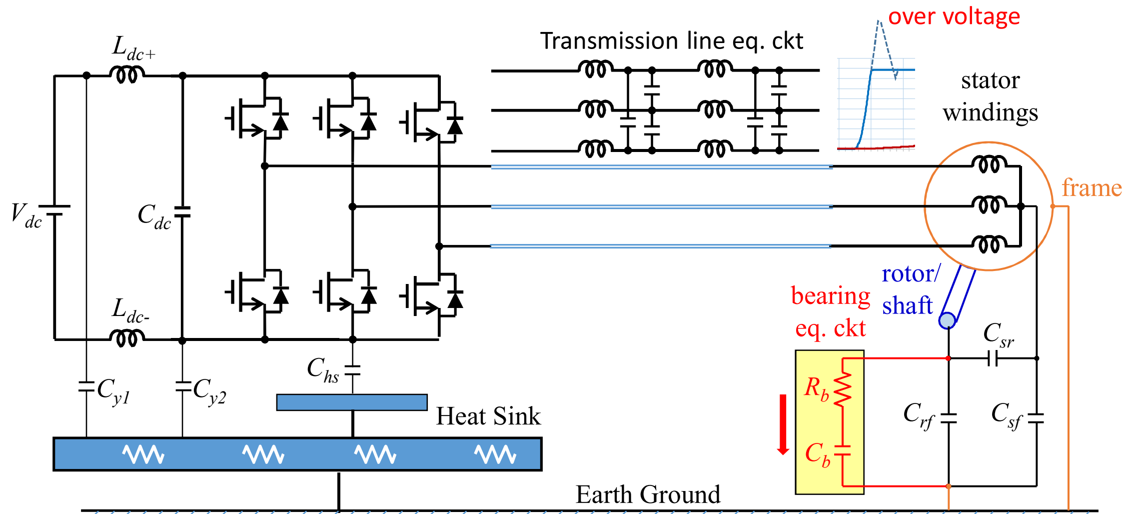
A Typical Motor Drive with a Long Cable Between Inverter and Motor

Some dv/dt related issues

1. Motor terminal over-voltage ➔ due to the long cable transmission line effect
2. Bearing parasitic capacitance induced circulating current (C·dv/dt)



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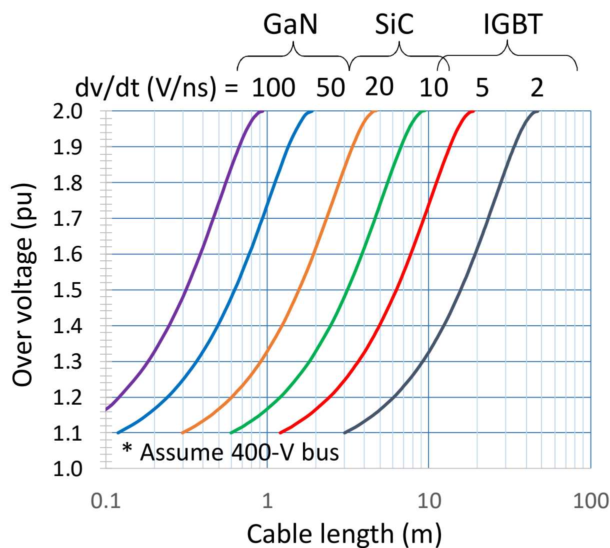
Voltage Overshoot vs. Cable Length under Different dv/dt Conditions



- **The transmission line effect due to the long cable between inverter and motor is a well-known phenomenon for the Si-IGBT drives.**
- **The motor terminal sees twice voltage typically between 10 and 100 meters with conventional IGBT drives, resulting motor insulation breakdown.**
- **For the SiC based drives, the voltage can double within 10 meters easily**
- **For the GaN based drives, under 100 and 50 V/ns conditions, the voltage doubles at 1 and 2 m, respectively**

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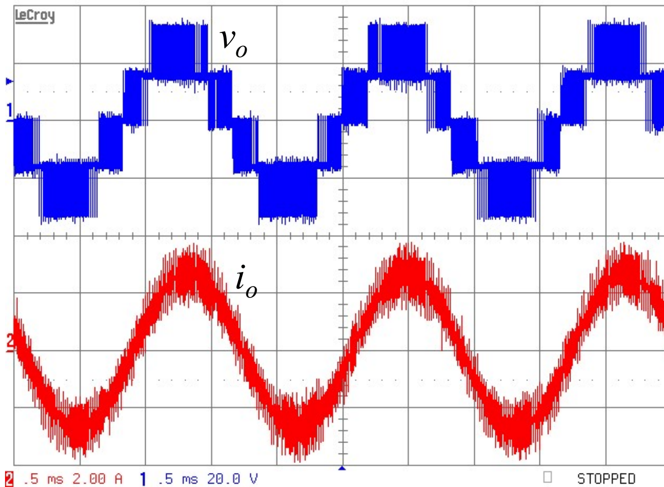
GaN Based Multilevel Inverter Output



- Even with the multilevel output voltage, dv/dt of GaN inverters still causes severe capacitive coupled current.
- Should we slow down the switching to ease the issue?

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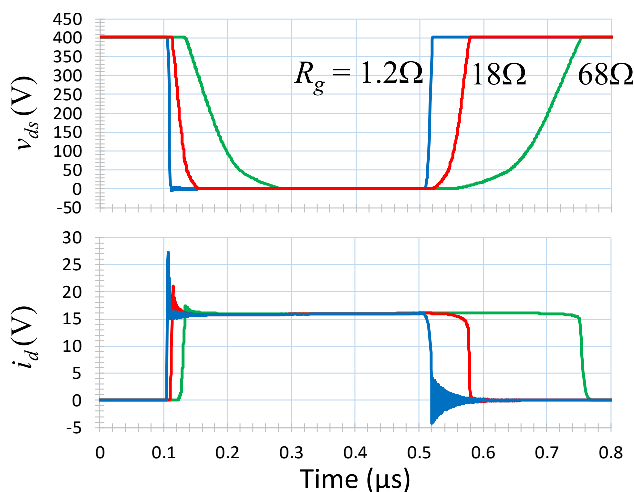
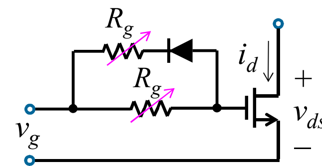
Switching Energy under Different Slew Rates





Turn-on

dv/dt (V/ns)	E_{on} (nJ)
100	30
40	82
4	320

Turn-off

dv/dt (V/ns)	E_{off} (nJ)
133	18
13.3	112
4	1050

- Adjusting gate drive resistance allows the control of slew rates
- Reducing turn-on slew rate by 25X, loss is increased by ≈10X
- Reducing turn-off slew rate by 33X, loss is increased by ≈60X
- We have a good reason to keep high dv/dt, but what about the noises and capacitive coupling?

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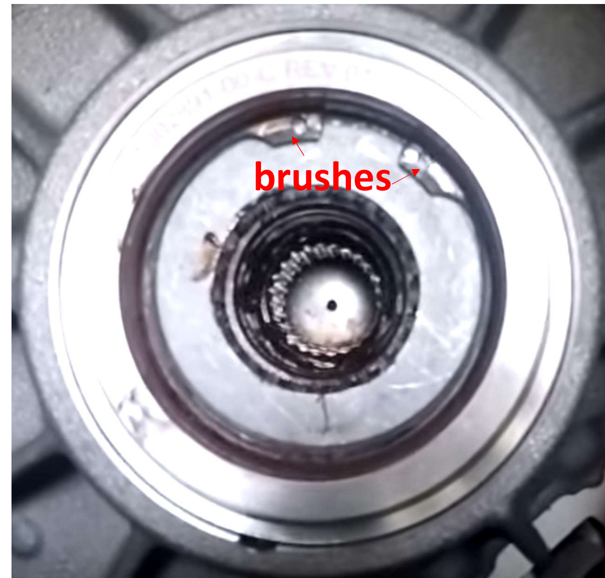
Tesla EV Motor Drive Solution to the C·dv/dt Current Issue!

- Slowing down switching is not preferred as it increases loss substantially. Therefore, EV motor drives tend to keep fast switching that results in a significant current caused by C·dv/dt or common mode (CM) current
- The CM current can circulate through bearing and damage the bearing balls
- The remedial solution by Tesla EV is to add brushes to bypass such a CM current through the shaft to ground
- Not elegant, but a tradeoff !!!



Photograph from Tesla Model S

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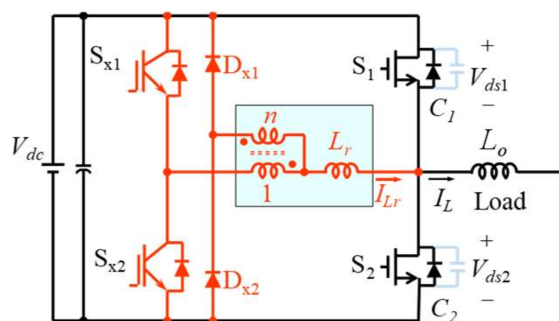
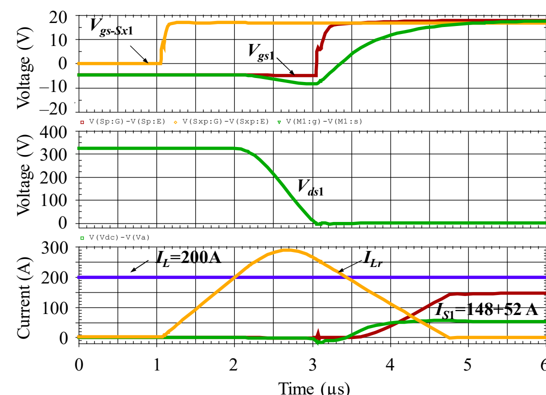
VT-FEEC Solution to C·dv/dt Problem – Soft Switching

- Apply an auxiliary resonant circuit to create zero-voltage before the device turns on ➔ V_{ds1} drops to zero before V_{gs1} turns on
- Lossless snubber capacitors C_1 and C_2 reduce dv/dt to <2 V/ns (50X reduction), completely solving the dv/dt related issue





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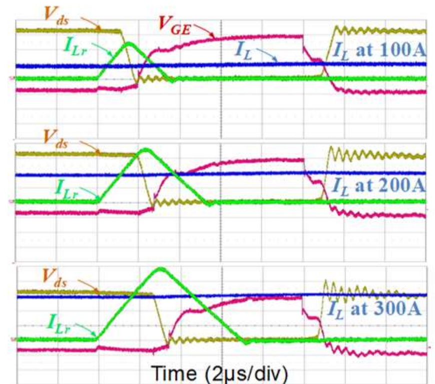
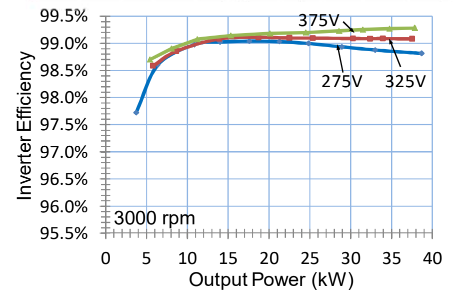
VT-FEEC Soft-Switching Inverter for In-Vehicle Experiment

- Soft turn-on and turn-off under all voltage and current conditions have been verified with experiments
- Improve the efficiency to >99% by eliminating switching losses
- Implemented for in-vehicle testing and test drives with a modified Citivan





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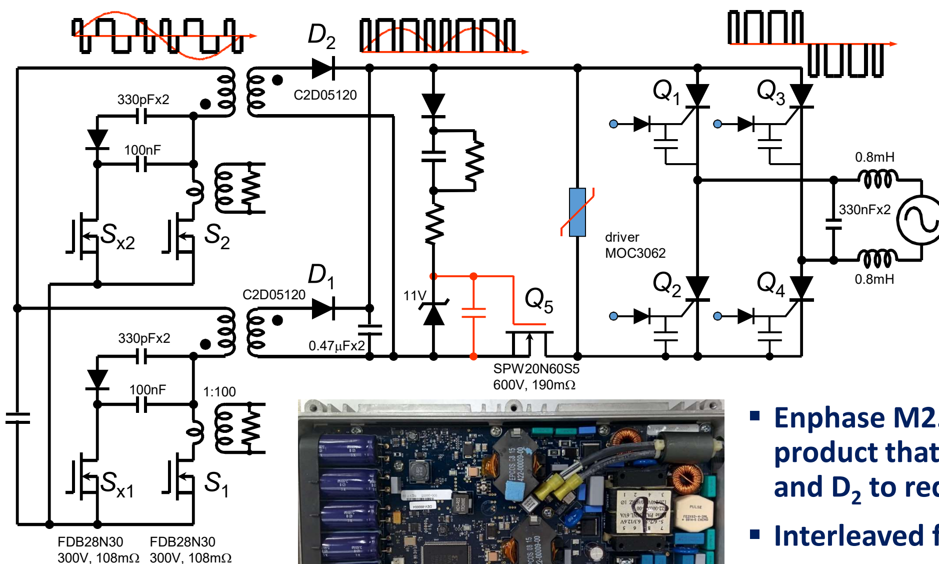
First Commercial Product to Adopt WBG Devices –PV Microinverter



- Enphase M250 – The first commercial product that adopts SiC diodes, D_1 and D_2 to reduce switching losses
- Interleaved flyback + unfolding
- Large capacitor bank for ripple reduction

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Two-Stage Design to Eliminate Electrolytic Capacitors

- DCDC control
  - ✓ MPPT
  - ✓ PV voltage control with double-line ripple rejection
- Inverter control
  - ✓ DC bus regulation with grid-current distortion reduction
  - ✓ Grid current control

- Design of two-stage dc-dc + dc-ac allows the ripple current to be suppressed in the middle dc link capacitor C_b
- Implementation with proportional + resonant controller further eliminates the double line frequency ripple

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Use of GaN Devices for DC-DC and DC-AC with MHz Switching to Reduce Size and Soft-Switching to Improve Efficiency

- The commercial 300-W product:
  - Dimension: 200 x 140 x 31 mm, or 0.868 liter
  - Efficiency: 95.5%
- VT's 400-W PV Microinverter prototype containing four stages: DC-DC, DC-AC and EMI filters
  - Dimension: 178 x 70 x 16 mm, or 0.2 liter, 23% of commercial 300-W product
  - Efficiency: 98%

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A Challenging Issue in Soft-Switching Converter – PCB Layout

Circuit diagram

PCB layout

Positive-half cycle

Negative-half cycle

Q3D Simulated ACL	L_{PCB}
Positive half cycle L_{PCB+}	9.26 nH
Negative half cycle L_{PCB-}	19.72 nH

➔ **Parasitic loop inductances are highly unbalanced**

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Re-Layout to Balance Positive and Negative Cycles

Move one leg to bottom side

Top view | Bottom view

Positive Half Cycle $S_1 - S_4$

Negative Half Cycle $S_2 - S_3$

Q3D Simulation Results	Positive Half Cycle	Negative Half Cycle
DCR, DCL (mOhms, nH)	2.36 mOhms, 28.408 nH	2.21 mOhms, 25.757 nH
ACR, ACL @1MHz (mOhms, nH)	7.80 mOhms, **16.47 nH**	8.67 mOhms, **15.69 nH**

- Positive and negative loop PCB parasitic inductances are nearly balanced.
- The difference accounts less than **3%** of the resonant inductance L_r.

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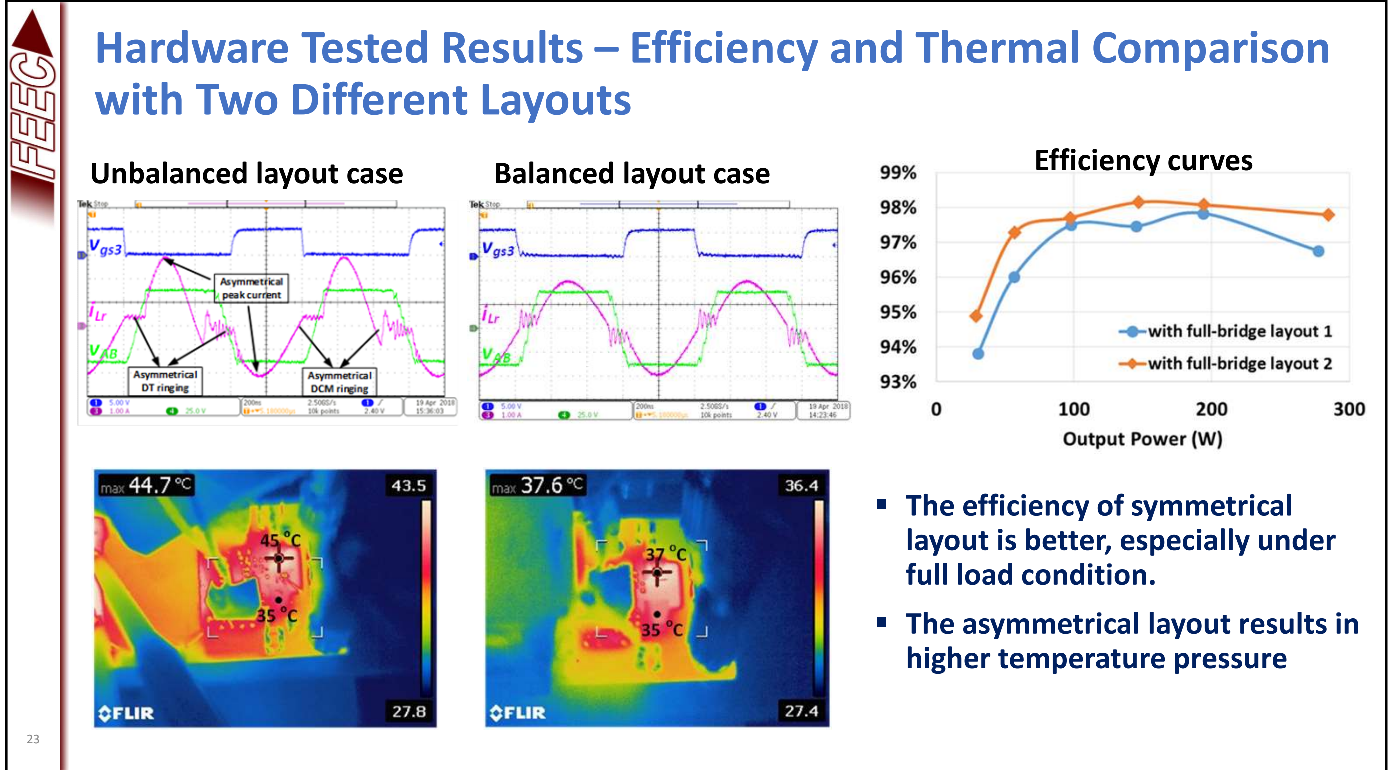
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Hardware Tested Results – Efficiency and Thermal Comparison with Two Different Layouts
Unbalanced layout case
Balanced layout case
Efficiency curves
Asymmetrical peak current
Asymmetrical DT ringing
Asymmetrical DCM ringing
99%
98%
97%
96%
95%
94%
93%
0
100
200
300
Output Power (W)
with full-bridge layout 1
with full-bridge layout 2
max 44.7 °C
43.5
45 °C
35 °C
27.8
FLIR
max 37.6 °C
36.4
37 °C
35 °C
27.4
FLIR
The efficiency of symmetrical layout is better, especially under full load condition.
The asymmetrical layout results in higher temperature pressure
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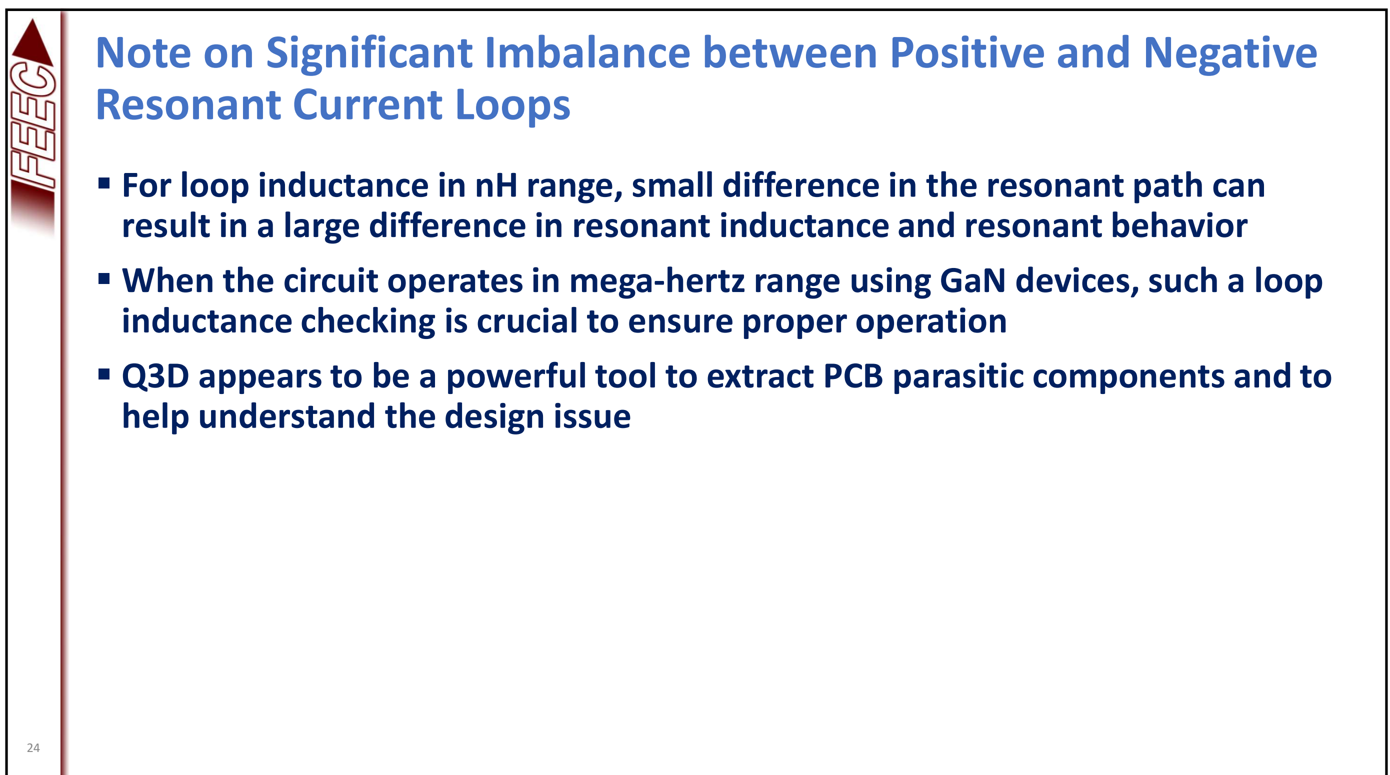
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Note on Significant Imbalance between Positive and Negative Resonant Current Loops
For loop inductance in nH range, small difference in the resonant path can result in a large difference in resonant inductance and resonant behavior
When the circuit operates in mega-hertz range using GaN devices, such a loop inductance checking is crucial to ensure proper operation
Q3D appears to be a powerful tool to extract PCB parasitic components and to help understand the design issue
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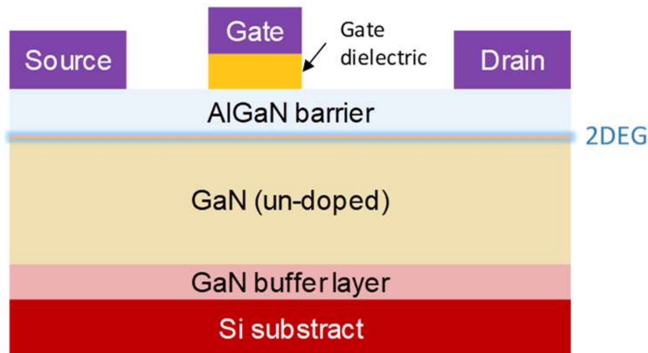
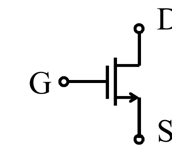
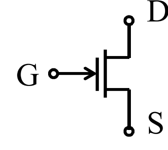
A Challenging Issue with GaN HEMT Reverse Current Flow





e-Mode HEMT



d-Mode HEMT

- **Picture shows a typical GaN high-electron-mobility transistor (HEMT) structure**
- **Both e-mode and d-mode HEMT do not have body diode between source and drain**
- **Question is "do we manually add an external Schottky diode or not"**

The answer is normally negative because it will add junction capacitance that will slow down the switching, same situation found in SiC case.

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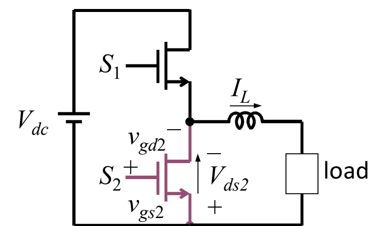
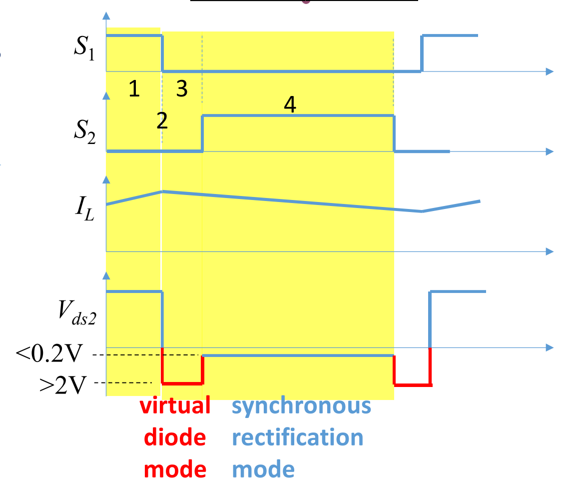
Circuit Operation of GaN "Virtual Diode"

1. **Initially S_1 on and S_2 off, $v_{gs2} = 0$.**
2. **When S_1 turns off, I_L is freewheeling from S_2 source to S_2 drain, thus $v_{d2} < v_{s2}$ or $v_{d2} < v_{g2}$.**
3. **In this case, S_2 drain becomes a "virtual source" with $v_{gd2} > 0$ and the gate voltage against drift region is positive, thus a reverse current can flow, but with non-optimized gate-source voltage, voltage drop v_{sd2} is quite high (typically >2V for LV devices and >5V for HV devices) ➔ a "virtual diode" is naturally formed.**
4. **If v_{gs2} turns back on under freewheeling and S_1 turn-off condition, then S_2 will be reverse conducting under synchronous rectification mode, which will reduces the voltage drop v_{sd2} substantially (typically <0.2V).**





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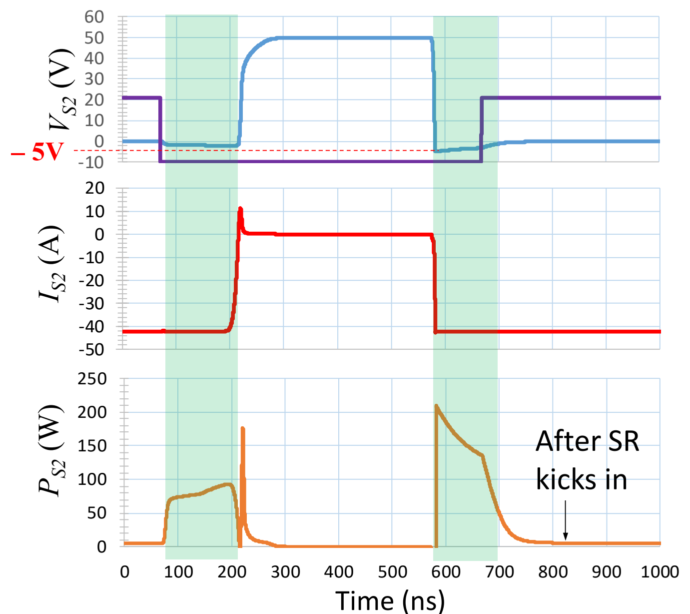
Significant Power Loss with Non-Optimized Dead Time

- GaN converters are normally designed for high-frequency operation, such as mega-hertz switching for passive size reduction
- Example here shows 100-ns dead time for a 1-MHz switching low-voltage converter. Before SR kicks in, the "Virtual Diode" voltage is as high as –5V, and the peak power loss reaches 200 W with *I* = 40 A.
- A dead time of higher than 100 ns is quite common in Si devices, but for GaN, this number needs to go down to single nano-second digit.



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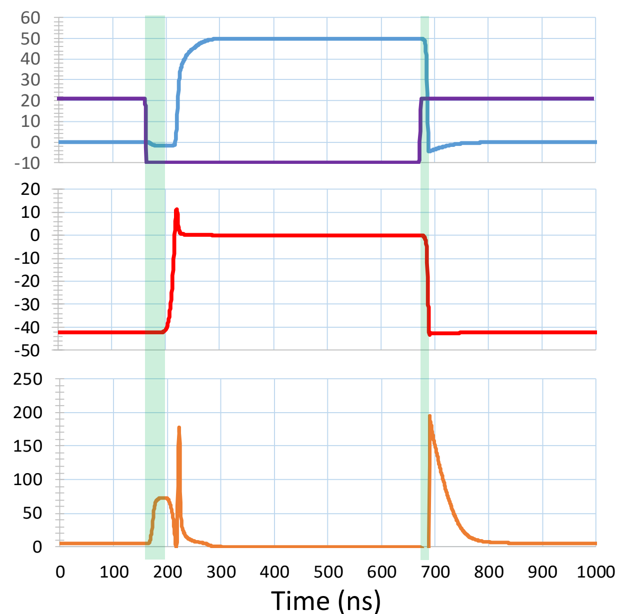
Operation with Single-Digit Nano-Second Dead Time

- After reducing dead time to 5ns, the dead-time loss is significantly reduced
- With single nano-second digit dead time, the conventional dead-time compensation technique could be obsolete
- Even ZVS detection will face the challenge with the conventional logic and DSP delay.
- Future adaptive SR needs an integrated design at the gate drive chip level



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Discussion and Conclusion

- WBG devices are "revolutionizing" the EV and PV industries and in fact the entire transportation and energy/power area.
- Performances of WBG devices are very impressive – low conduction drop, fast switching, low loss, etc. However, there are many challenging issues such as dv/dt, parasitic asymmetry, reverse diode conducting, etc.
- Novel solutions to the fast slew rate induced issues need to be explored.
- Some old school topics are becoming obsolete or need a new angle to look at, such as dead-time compensation, ZVS detection, etc.
- A whole new set of knowledge is needed to deal with WBG devices such as PCB layout, parasitic extraction, EMI, thermal management (not discussed as this talk is mainly focusing on electrical side), etc.

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Questions

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