Characterization, Reliability and Packaging for 300 °C MOSFET

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(ABSTRACT)

Silicon carbide (SiC) is a wide bandgap material capable of higher voltage and higher temperature operation compared to its silicon (Si) counterparts due to its higher critical electric field (E-field) and higher thermal conductivity. Using SiC, MOSFETs with a theoretical high temperature operation and reliability is achievable. However, current bottlenecks in high temperature SiC MOSFETs lie within the limitations of standard packaging. Additionally, there are reliability issues relating to the gate oxide region of the MOSFET, which is exacerbated through high temperature conditions. In this thesis, high temperature effects on current-generation SiC MOSFETs are studied and analyzed. To achieve this, a high temperature package is created to achieve reliable operation of a SiC MOSFET at junction temperatures of 300 ^{0}C. The custom, high temperature package feasibility is verified through studying trends in SiC MOSFET behavior with increasing temperature up to 300 ^{0}C by static characterization. Additionally, the reliability of SiC MOSFETs at 300 ^{0}C is tested with accelerated lifetime bias tests.

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(GENERAL AUDIENCE ABSTRACT)

Electrical devices that are rated for high temperature applications demand a use of a material that is stable and reliable at the elevated temperatures. Silicon carbide (SiC) is such a material. Devices made from SiC are able to switch faster, have a superior efficiency, and are capable of operating at extreme temperatures much better than the currently widely used silicon (Si) devices. There are limitations on SiC certain structures of SiC devices, such as the metal oxide semiconductor field effect transistor (MOSFET), have inherent reliability issues related to the fabrication of the device. These reliability issues can get worse over higher temperature ranges. Therefore, studies must be made to determine the feasibility of SiC MOSFETs in high temperature applications. To do so, industry standard tests are conducted on newer generation SiC MOSFETs to ascertain their use for said conditions.

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Chapter 1 Introduction

1.1 General Application

Aerospace applications focus in the effort to research and design products related to flying in earth's atmosphere. Electronics for aerospace applications have many stringent requirements in reliability, power density, and efficiency due to the high cost, safety focused nature of the field. Integration of electronics is becoming more popular as replacing mechanical components with electronics improves fuel efficiency of aerospace vehicles not only due to the superior efficiency of said applications, but also through the weight reduction of having small, integrated circuits over bulky analog components.

As more systems within aerospace applications are replaced with electronics, improving the power density and efficiency of power electronics converters becomes more of an interest as they have a significant impact on the fuel efficiency and total weight capacity of aerospace vehicles. Improving the power density and efficiency in power electronics often involves increasing the operating frequency and thermal management efficiency. Increasing operating frequency will reduce the size of inductive components, while increasing thermal management efficiency will reduce the size of heat relief components such as heatsinks and fans.

Components in elevated temperature environments, such as electronics close to the engine compartment, require a much higher base temperature operation and thermal management efficiency than circuits in other parts of the vehicle. These environments can reach up to 250 °C ambient temperature—temperatures which require a highly specialized design to realize electronic circuit integration. The commonly utilized silicon (Si) for power switches typically has a

temperature limitation of 150 ^{0}C due to functionalities as a switch, such as turn-on and blocking capability, quickly degrading at temperatures beyond this point.

To its conclusion, power devices with a superior material limitation compared to Si devices are desired for aerospace applications to reduce component size, increase efficiency, and operate in extreme temperature environments that Si devices are incapable of reaching. The wide bandgap material silicon carbide (SiC) is a promising alternative to Si devices.

1.2 Motivation

With the emergence of SiC devices, high temperature applications of electronic devices can be taken to a new due to SiC's excellent thermal conductivity and material stability at higher temperatures. SiC, when compared to its popular counterparts for power devices such as gallium nitride (GaN) and Si, has approximately 3x higher thermal conductivity. This allows thermal management systems to extract heat more efficiently, allowing for a smaller system size and lower equilibrium temperatures.

Additionally, SiC devices support a high voltage due to their high electric breakdown field. High voltage silicon carbide devices are also able to switch faster than their competitors in high voltage applications, namely Si IGBTs, due to SiC's high electron mobility. The wide bandgap nature of SiC (3.3 eV) also allows for lower leakage currents at higher temperatures [2]. A comparison of material characteristics for SiC compared to GaN and Si is shown in Figure 1.

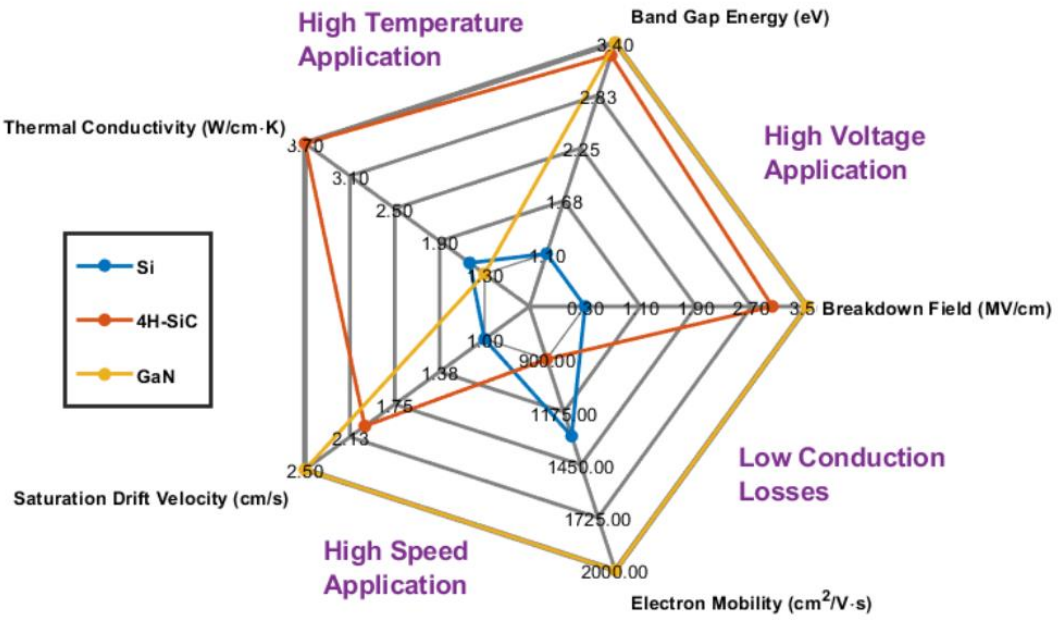


Figure 1. Summary of significant material properties of SiC, GaN, and Si [1]

[4-5] have studied SiC power devices such as the BJT and JFET over temperatures beyond 250 °C. However, devices such as the BJT and JFET are either current driven or have a normally on operation. Current driven switches are not desirable from a drive circuitry standpoint due to increased power demands to operate it, while normally on switches are not desirable from a circuit design standpoint due to failure mode management. To elaborate on the latter point, a failure in the power device drive circuitry for normally on, or depletion mode switches could result in a short-circuit event.

The MOSFET has an advantage of being both a voltage driven and normally off device. However, there is a lack of literature that provide insight into the operation and reliability of SiC MOSFETs at temperature at or greater than 250 °C.

Due to advancements in manufacturing capabilities of SiC devices, studies incorporating SiC devices into power electronic circuits are currently a hot topic. However, the full thermal range

of SiC devices are difficult to access for commercial production due to limitations in packaging. While SiC devices and power modules are commercially produced by manufacturers such as Cree and Rohm, a large part of their marketed advantage is high voltage, high speed applications—the common maximum junction temperature listed in datasheets is 150-175 ^{0}C. The breakdown for common materials used in TO-247 packaging for a typical 3-terminal device is shown below in Figure 2.

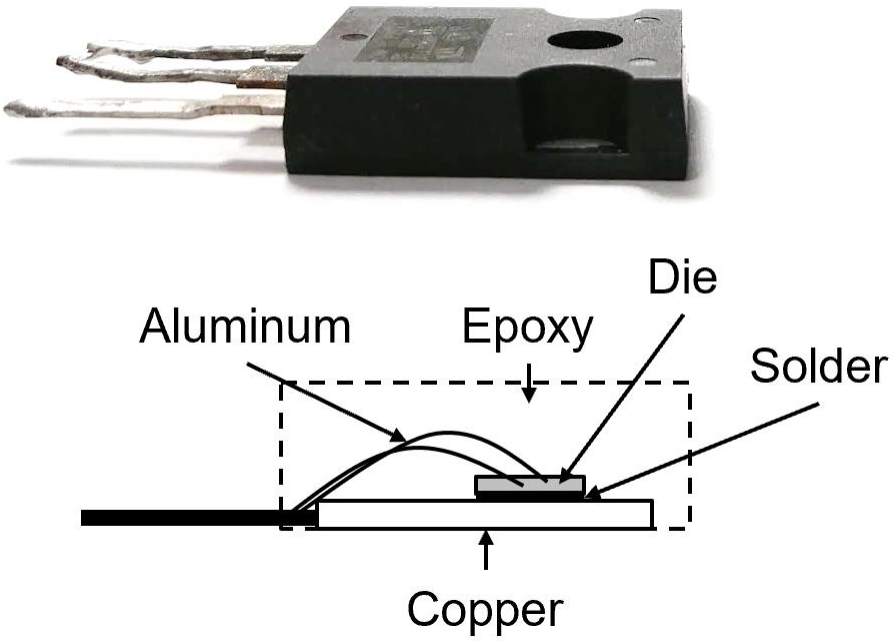


Figure 2. TO-247 package breakdown

The encapsulant, typically made from a epoxy molding compound, is rated for relatively low temperatures and is not able to sustain temperatures greater than 175 ^{0}C without quickly breaking down. The die attach, typically made from solder, has a wide range of melting point depending on the composition. Tin-lead (SnPb) alloys, which are a common solder material, have a melting point of 188 ^{0}C.

To explore the extreme thermal limits of SiC transistors, a package must be developed that can withstand the extreme temperature ranges that these devices are theoretically capable of achieving. If a package that can withstand extreme temperatures can be developed, SiC devices have the potential to establish a new limitation for high temperature applications for power electronics.

1.3 Thesis Objective and Outline

The purpose of this thesis is to inform the reader of the performance and limitations in current generation SiC MOSFETs as a high temperature power device for aerospace applications. This is achieved through analyzing the operation and reliability of SiC MOSFETs at temperatures at and above 250 °C. To realize such a study, a high temperature package is developed and tested for a discrete die.

Chapter 2 discusses the methodology for building a high temperature package for a power device. Package development and analysis for incorporating a SiC MOSFET is presented.

Chapter 3 tests the feasibility of the high temperature package developed in Chapter 2 while also performing a preliminary survey of SiC MOSFET operation at high temperatures. SiC MOSFET static characteristics are monitored as temperature is increased. The trends in characteristics are compared to theoretical expectations. Dynamic testing is also tested and compared between 25 °C and 300 °C.

Chapter 4 describes reliability testing for SiC MOSFETs. Industry standards for MOSFET reliability testing are reviewed. Common breakdown mechanisms for relevant reliability testing are reviewed. Results from reliability testing are discussed.

Chapter 5 reviews work conducted for this thesis, summarizes the main conclusions, and discusses possible future work.

Chapter 2 Packaging for High Temperature

2.1 Introduction

Commercially available packages are typically encapsulated in a plastic epoxy molding compound. These devices are limited to at most 175 ^{0}C in their datasheets due to the materials limitations for the packaging. In other words, the SiC devices inside are theoretically able to operate at a much higher temperature; a package rated at a higher temperature will enable such capabilities. A custom package is developed to test these devices at 300 °C.

A package for a transistor typically involves the following as shown in Figure 3:

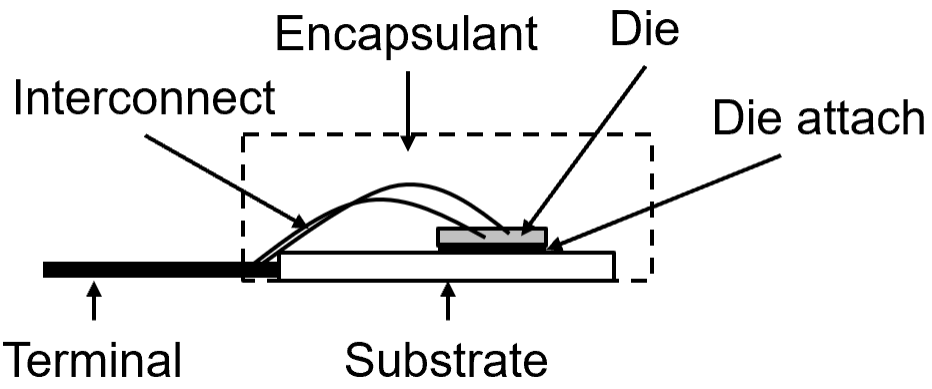


Figure 3. Package part breakdown

The package begins with a substrate, or a base plate to support all the other connections of the package. It typically has an insulating layer and a conducting layer; the insulating layer is the core layer of the substrate, whereas the conducting layer is etched away to a specific pattern necessary for connections from the die to other parts of the package. Typical substrate insulating materials include Al_2O_3 (Alumina) and aluminum nitride (AlN). Other alternatives include laminate substrates, which can vary from FR4 to polyimide.

The die is bonded to the substrate through a form of die attach. The most common die attach method is solder. There are many combinations of solder alloys, which range in temperature depending on elements used. Another form of die attach is sintering. Sintering is a process that solidifies a material through heat and pressure without bringing the material to a liquidous state. For metal sintering, such as silver sinter, the metal is typically in a powder form with a bonding agent to make the material a spreadable paste. Once a uniform paste is layered on the substrate, the die is placed on top of the sinter paste and cured over a high temperature with pressure added.

Once the device is attached to the substrate, interconnects must be made to connect the die to other parts of the package. Other parts of the package can include the lead terminals or other devices attached to the substrate. In the case of a singular device packaging, the interconnects connect to the lead terminals. Typical interconnect materials consist of aluminum, copper, gold, and silver. The thickness of the interconnect depends on the current it needs to support.

Terminals are the connections from the package to other, external parts of the circuit. A common form of terminals are leads as seen in most through hole discrete device components. Other forms of terminals include ball grid arrays (BGA) for solder mount components and pin grid arrays (PGA).

Encapsulation is the housing that protects the device and other fragile components of the package, such as the interconnects, from physical damage. Encapsulation also often serves as electrical insulation to prevent breakdown or partial discharge for high voltage devices and power modules. Common encapsulation materials include epoxy and silicone. However, there are other niche alternatives for high temperature applications, such as lead glass and polyimide.

Ideally, each component listed above would have minimum thermal resistance to facilitate heat generated from the die to the external environment. Additionally, the materials' coefficient of thermal expansion (CTE) would be minimal to prevent mechanical stress as each component expands or contracts in response to an increased temperature.

2.2 Package Fabrication

Table 1 shows the materials list for this work's packaging.

Table 1. List of Materials for High Temperature Packaging

Package Part	Material	Part Number/Manufacturer
Die	SiC MOSFET	CPM3-1000-0065B, Cree
Substrate	Silver-plated Alumina DBC	Stellar Industries
Interconnect	Aluminum Wire Bond	N/A
Lead Terminal	Silver strips	N/A
Buffer Layer	Polyimide	PI2611, HD Microsystems
Encapsulation	Lead glass	24927, 3M

A 1 kV SiC Wolfspeed CPM3-1000-0065B MOSFET die is selected. A third generation SiC MOSFET was selected as it was the most recent revision available in the market. In addition, the die was readily available for distribution; other manufacturers' dies were difficult to obtain for reliability purposes.

The die is sintered to a silver-plated direct bonded copper (DBC) ceramic alumina (Al_2O_3) substrate using pressure-less silver sintering. The interconnects are made of aluminum wire bonds. A polyimide layer coats the die as a buffer layer. The encapsulation used is a lead glass, which is poured into a mold and cured to room temperature. A summary of the package's materials with relevant material thicknesses are shown in Tables 2.

Table 2. Material Thicknesses

Material	Thickness (mm)
Alumina	0.6
Cu	0.6
Polyimide	0.022
Glass	3.5
Wire Bond	0.254

Each material was selected for their high temperature capability. The lead glass, being a novel encapsulant, was studied for its capabilities at high temperature [6]. Alumina DBC is a material stable at temperatures up to 1750 ^{0}C. Aluminum is temperature stable up to 660 ^{0}C.

A summary of the process to build the high temperature package is shown in Figure 4.

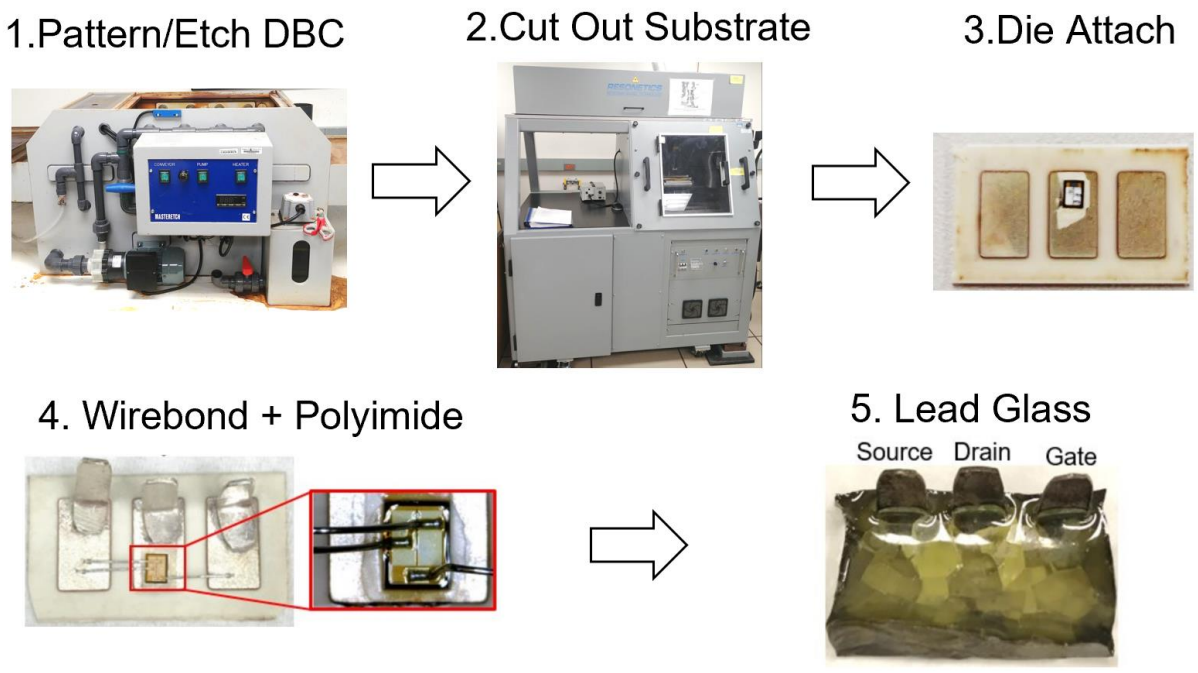


Figure 4. Package building process

First, a blank substrate is lasered a pattern to etch out. This pattern is the finalized pad shape for gate, drain and source. The dimensions for the pattern are shown in Figure 5.

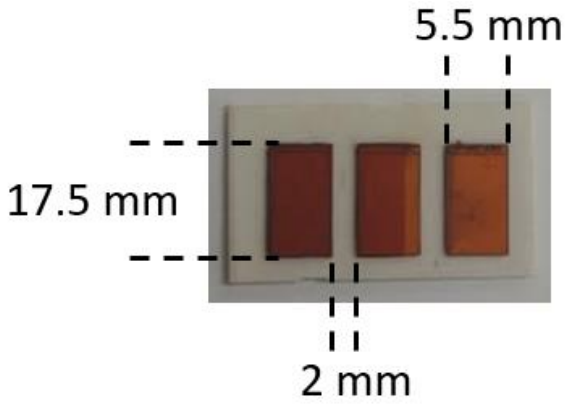


Figure 5. Pad dimensions for substrate

A layer of Kapton is used as an etcher-resist. Once the pattern is set on the substrate, the etching machine sprays ferric chloride to corrode away the copper, leaving the relevant pads protected by the Kapton. A laser machine is then used to cut the substrate into equal pieces, which serves as the substrate for each individual package. The relevant laser focus settings are shown in Table 3. Some of these values are unitless as they are calibrated to the laser settings and hold a scaled value to actual measurements in the software of the laser machine.

Table 3. Laser Settings for Cutting 0.381 mm Ceramic

Laser Setting	Value
Focus	4.2
Speed	0.1
On-Time	400 uS
Firing Distance	0.0001

Using the correct laser power and turn-on length is crucial in cutting the ceramic. We found that the most effective cut was made by making a single pass through the ceramic. Multiple passes at low power resulted in the ceramic shattering. Additionally, setting the laser power too high made the ceramic shatter as well. Additional steps were taken to ensure that the ceramic is less susceptible to shattering from cutting through the pattern, as illustrated in Figure 6.

Figure 6. To reduce ceramic cracking during cutting, traces were left between sample cutouts (right) and a backplane was added to the back of each sample (left)

A backplane was added to the back of the samples to reinforce the ceramic within each sample pattern. Copper traces were also left in between the sample patterns to further reinforce the ceramic. Figure 7 shows a successful ceramic cut compared to an unsuccessful sample.

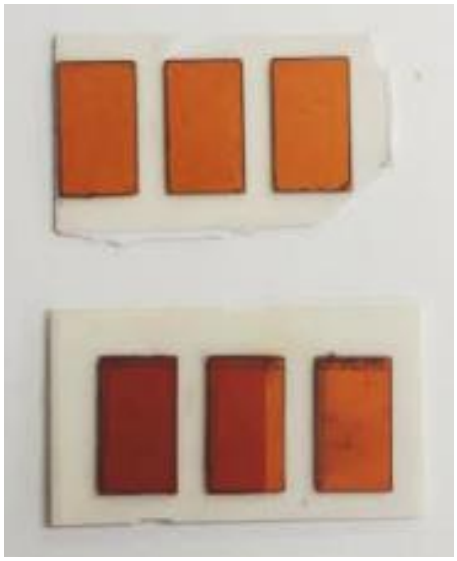


Figure 7. Unsuccessful ceramic cut (top) versus successful ceramic cut (bottom)

Pressure-less silver sinter is used to attach the die. The sinter is layered 0.05 mm thick onto the substrate. The thickness is controlled by laying down Kapton tape of the same thickness near the

area where the sinter is applied. A metal squeegee is used to ensure the silver sinter is spread to the same thickness as the Kapton tape.

The material is then cured in the oven for 215 ^{0}C for 90 minutes. Silver leads are also shaped and sintered onto the substrate. These leads are flattened from an 11 mm x 2 mm x 0.5 mm strip of silver. We found a successful sinter for leads were from flatness and contact surface area to the silver sinter paste.

Once the die is attached, aluminum wire bonds are bonded to each relevant pad using the TPT HB30 wire bonder using an ultrasonic wedge bonding technique. The settings used to bond the wires onto the die is shown in Table 4.

Table 4. Wire Bond settings for SiC MOSFET

Wire Bond Setting	Value
US	500
Time	300 mS
Force	100 cN

On testing with various bond settings, we found that having a high bond strength and time damaged the die. Therefore, it is crucial to keep the order of the bond (die to substrate) consistent while bonding with the given settings.

A polyimide coating is then cured over the die. The polyimide used was PI2611 from Hitachi DuPont Microsystems. An adhesion promoter, VM-652, is first applied over the die at a rate of 3500 RPM for 30 seconds. The polyimide is spin-coated at the manufacturer specified rate of 3000 RPM for 30 seconds. It is soft baked at first with the temperature profile shown in Figure 8. A total of 3 coatings of polyimide is applied using the polyimide spin-coating and soft baking process.

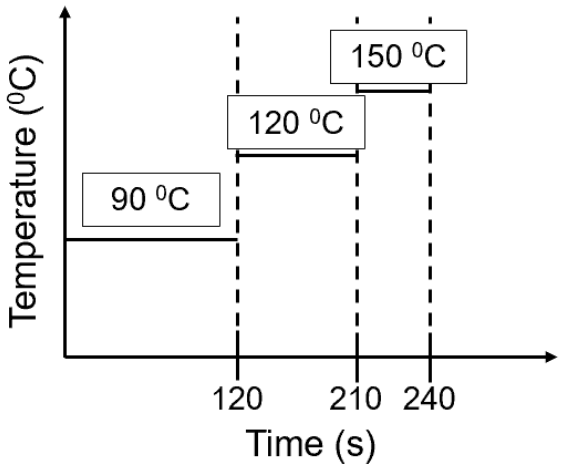
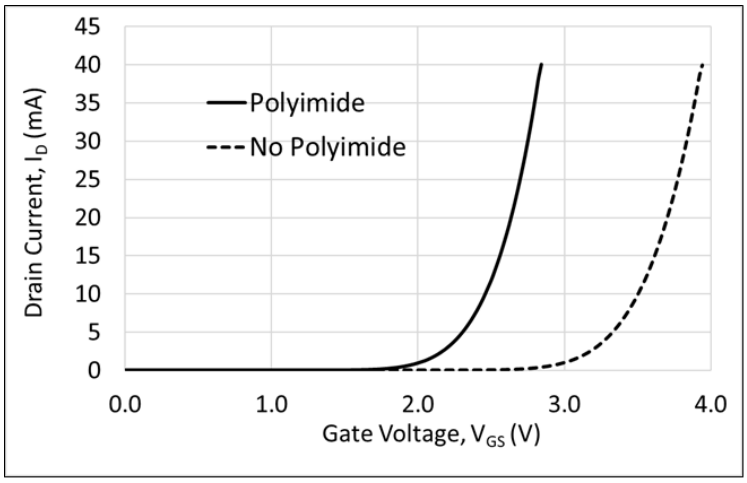


Figure 8. Soft baking profile for polyimide layer

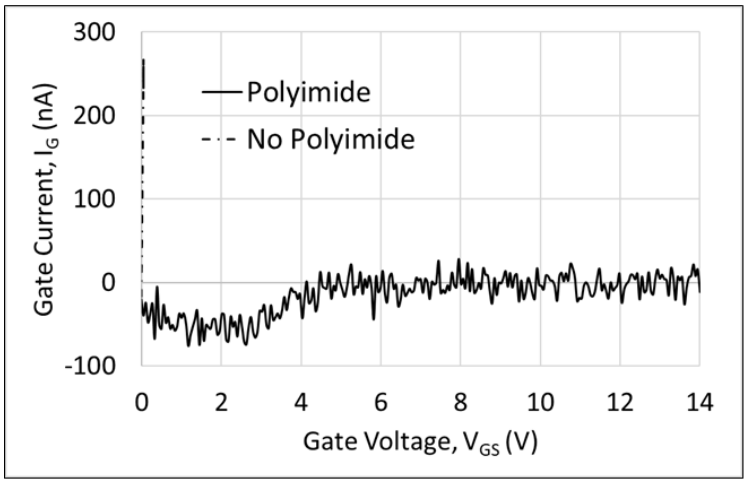
After soft baking, the polyimide is then cured in a nitrogen chamber at 400 ^{0}C for 4 hours. The cooling rate is not controlled after the curing period; the device is left to cool at room temperature.

The polyimide coating is necessary to prevent mechanical stress to the die as the glass cures over it. Without the polyimide layer, the die is not functional after encapsulation. This is likely due to CTE mismatch between the die and the glass as the glass cured to room temperature. As the polyimide has a low Young's modulus of 8.5 GPa, it serves as a mechanical buffer layer while the glass cures over the package.

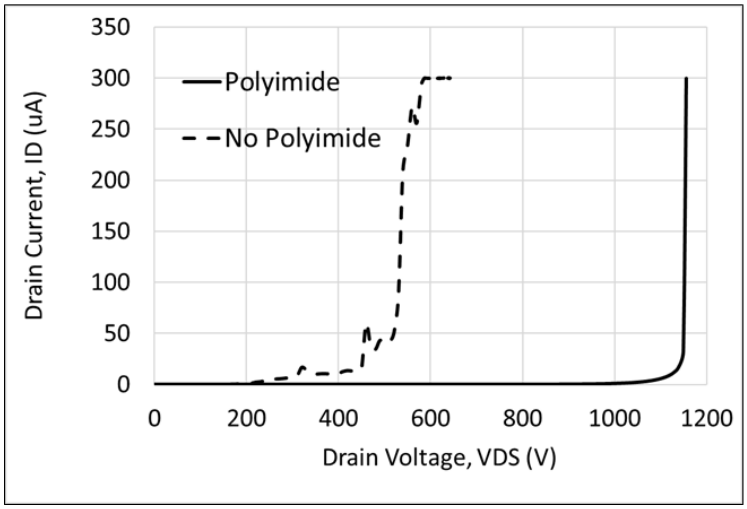
Figure 9 compares relevant static characterizations made to the die with and without polyimide layer, after glass encapsulation.



(a) Threshold voltage measurement



(b) Gate leakage current measurement



(c) Avalanche breakdown measurement

Figure 9. Static characterization difference between polyimide coated and non-polyimide coated glass encapsulated samples

After polyimide coating, the glass is prepared for pouring onto the substrate. As it comes in a powdered glass form, the glass is first melted and cured at 500 ^{0}C for 4 hours at atmospheric pressure. This ensures that the trapped bubbles resultant from melted powder is not present in liquidous form. The glass is then poured onto the substrate, which is surrounded by an aluminum foil mold. A summary of the preparation for glass is shown in Figure 10. The cooling temperature profile for the glass is shown below in Figure 11.

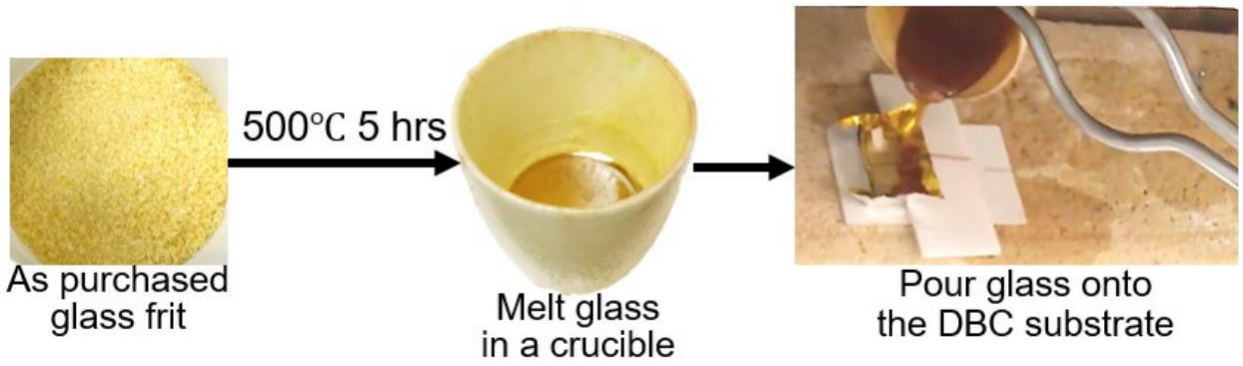


Figure 10. Glass pouring process [6]

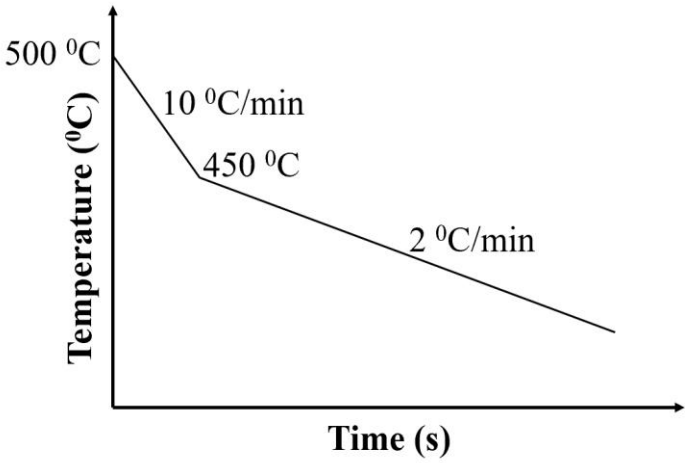


Figure 11. Glass curing temperature profile

The resultant sample with the glass encapsulant is shown in Figure 12.

Figure 12. Glass encapsulated sample

The sample shown shows some cracking in the glass. These cracks are potential voltage breakdown weak-points and are an issue that needs to be addressed. Using COMSOL simulation software, the electric field intensity was simulated for the substrate and leads that are attached. As shown in Figure 5, the distance between each pad is set to 2 mm. The simulation results are shown in Figure 13.

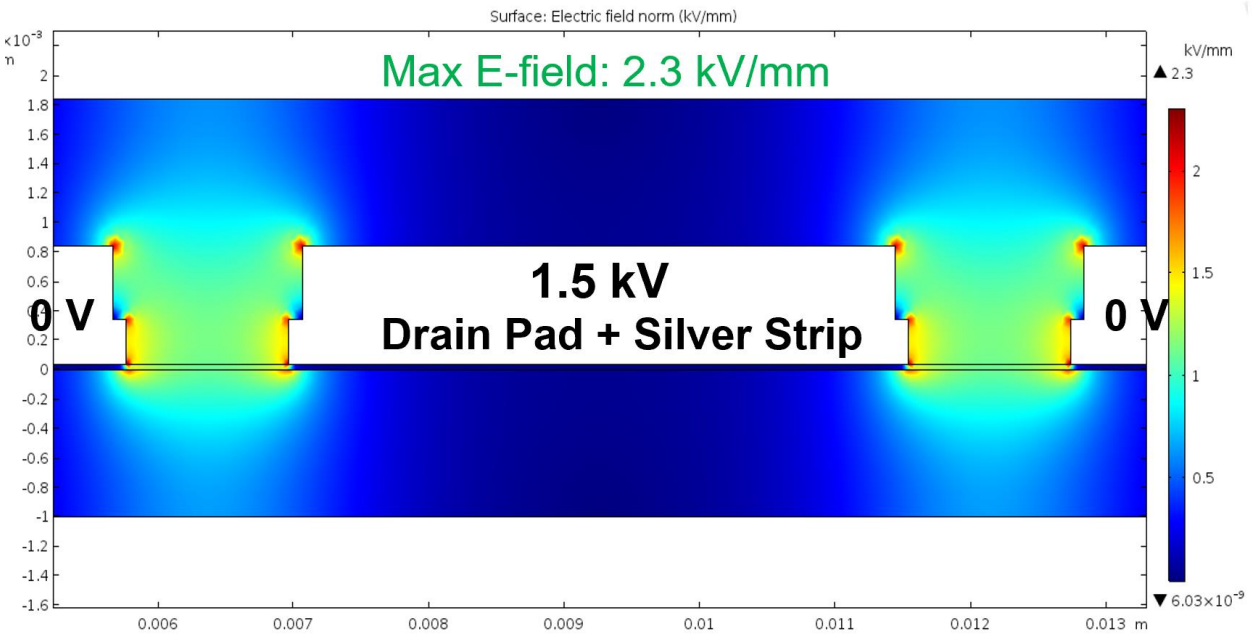


Figure 13. Electric field intensity simulation for package layout

The SiC MOSFET that is being used is a 1 kV device, with its avalanche breakdown voltage ranging from 1.1 kV to 1.2 kV. With a generous estimate of 1.5 kV at the drain pad of the die in simulation, the maximum electric field intensity present in the package was 2.3 kV/mm. As air breakdown voltage is at 3 kV/mm, it was concluded that the cracks in the glass are unlikely to have breakdown present under normal device operating conditions, even up to the avalanche breakdown voltage.

This cracking in the glass after curing is not yet resolved, but using this encapsulation is still a feasible idea for the high temperature tests involved. Glass exists to prevent widespread oxidation on the surface of the substrate during high temperature testing.

Chapter 3 Characterization

3.1 Static Characterization Background

Once the high temperature package was fabricated around the SiC MOSFET, its feasibility was verified through static characterizations. To make static characterizations, an Agilent B1505A Curve Tracer is used. Threshold voltage, on-resistance, output characteristic, transfer characteristic, gate leakage current, drain leakage current, and avalanche breakdown voltage were monitored through the curve tracer.

The threshold voltage for a power MOSFET can be defined as (1).

$$V_{TH} = \frac{\sqrt{4\epsilon_s kTN_A \ln\left(\frac{N_A}{n_i}\right)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{OX}}{C_{OX}} \quad (1)$$

Where permittivity (ϵ_s), Boltzmann constant (kT), doping concentration (N_A), oxide capacitance (C_{OX}), charge of an electron (q), and total oxide charge (Q_{OX}) are invariant to temperature compared to the intrinsic carrier concentration, n_i. Intrinsic carrier concentration increases exponentially with temperature as elevated temperatures excites more carriers for conduction [7]. As such, threshold voltage can be seen to have a negative temperature coefficient.

The on-resistance of a vertical power MOSFET can be described by 3 dominating resistances: the channel resistance, R_{CH}, the JFET region resistance, R_{JFET}, and the drift layer resistance, R_D [7]. As R_{CH} is proportionally dependent on the threshold voltage, as temperature increases, R_{CH} decreases. This will initially cause a drop in on-resistance, until R_{JFET} and R_D start to dominate due to decreased drift region mobility and inversion layer mobility [7]. Thus, with increasing temperature, the on-resistance will first drop before increasing.

The avalanche breakdown voltage can be described by:

$$\int_0^W \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p)\right]dx]dx = 1 \quad (2)$$

Where α_n and α_p are impact ionization coefficients for electrons and holes, respectively. According to Chynoweth's Law [7], impact ionization coefficient for 4H-SiC material is given as:

$$\alpha_n = a_p = 6.46E16 - 1.07E4 * T \quad (3)$$

Where temperature, T, has an inversely proportional relationship. As such, avalanche breakdown voltage increases with increasing temperature for SiC MOSFETs.

The output characteristic is a sweep of the drain voltage at a fixed gate voltage. The drain current is measured as the response. This characterization can be used to observe the MOSFET current saturation behavior at various gate voltages.

The transfer characteristic is a sweep of the MOSFET gate voltage while measuring the drain current. This characterization can be used to observe the current carrying capacity of the MOSFET at different levels of gate voltage.

3.2 Static Characterization Results

Figure 14 shows the test setup to realize the MOSFET static characterization comparison between 25 °C versus 300 °C junction temperature.

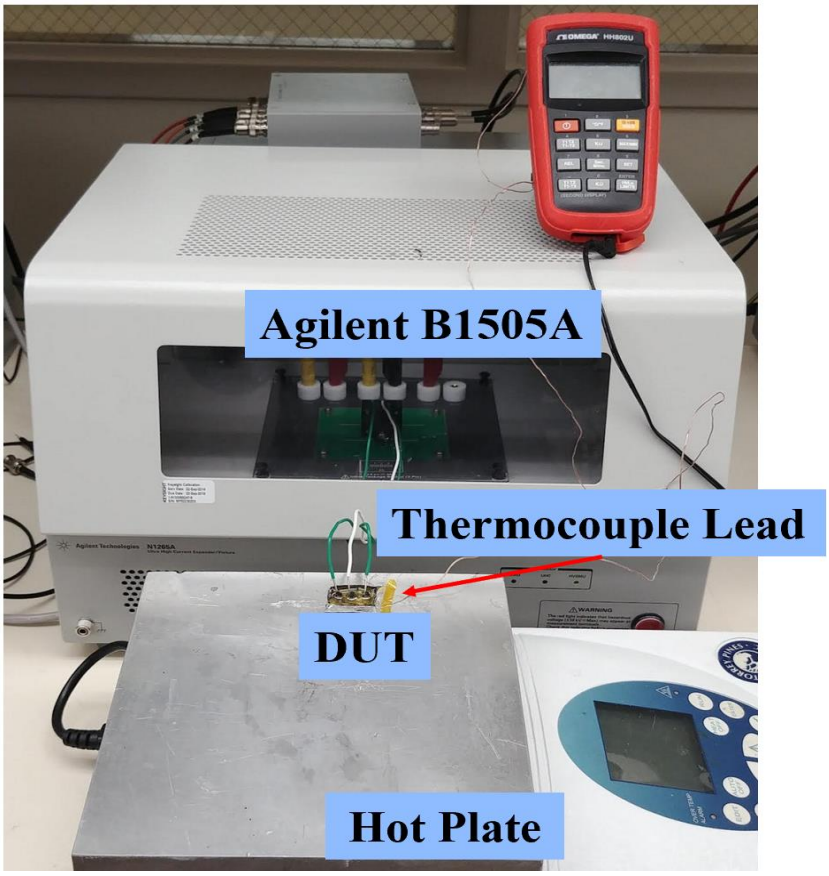


Figure 14. Physical test setup for 25 °C vs 300 °C static characterization

It is worth noting the temperature measurement technique for this test setup. Although it is not feasible to extract the real temperature of the die within the TO-247 packaged MOSFET, calculations for thermal resistances of the MOSFET from the hotplate to the die is possible. Through the thermal resistance calculations, it is possible to assume the calculated die temperature while knowing the hot plate temperature, which can be directly measured with the thermocouple. A thermocouple is necessary because despite the hotplate's readout for its temperature, measuring with the thermocouple reveals that only the center area's temperature is accurate with the hotplate reading, and the outer edges remain the coolest. Therefore, a secondary temperature confirmation is crucial to maintaining accurate measurements. For this test setup, the thermocouple leads were placed as close as possible to the device on the hotplate. In this case, since the only tests being

performed are short static characterizations, device switching loss, or self-heating, is not taken into consideration.

Another point worth noting are the long leads required to make the connections from the 3-terminal socket within the curve tracer to the hot plate. Although this adds a significant amount of resistance and inductance to the package's total parasitic values, the purpose of this test is comparative between room temperature and high temperature; as long as the added parasitic values are kept constant, the observed changes should only be affected from the temperature.

Figure 15 and Table 5 show the experimental results of a static characterization performed on a SiC MOSFET at 25 °C versus 300 °C junction temperature, T_j.

Table 5. V_{TH}, I_{GLEAK}, I_{DLEAK}, and V_{AV} for 25 °C vs 300 °C

	25 °C	300 °C	Test Conditions
V_{TH}	2.43 V	1.73 V	$V_{DS} = V_{GS}$, I_D = 5mA
I_{GLEAK}	15 nA	25 nA	V_{GS} = 10 V, V_{DS} = 0 V
I_{DLEAK}	30 nA	980 nA	V_{DS} = 800 V, V_{GS} = 0
V_{AV}	1.1 kV	1.16 kV	I_D = 100 uA, V_{GS} = 0

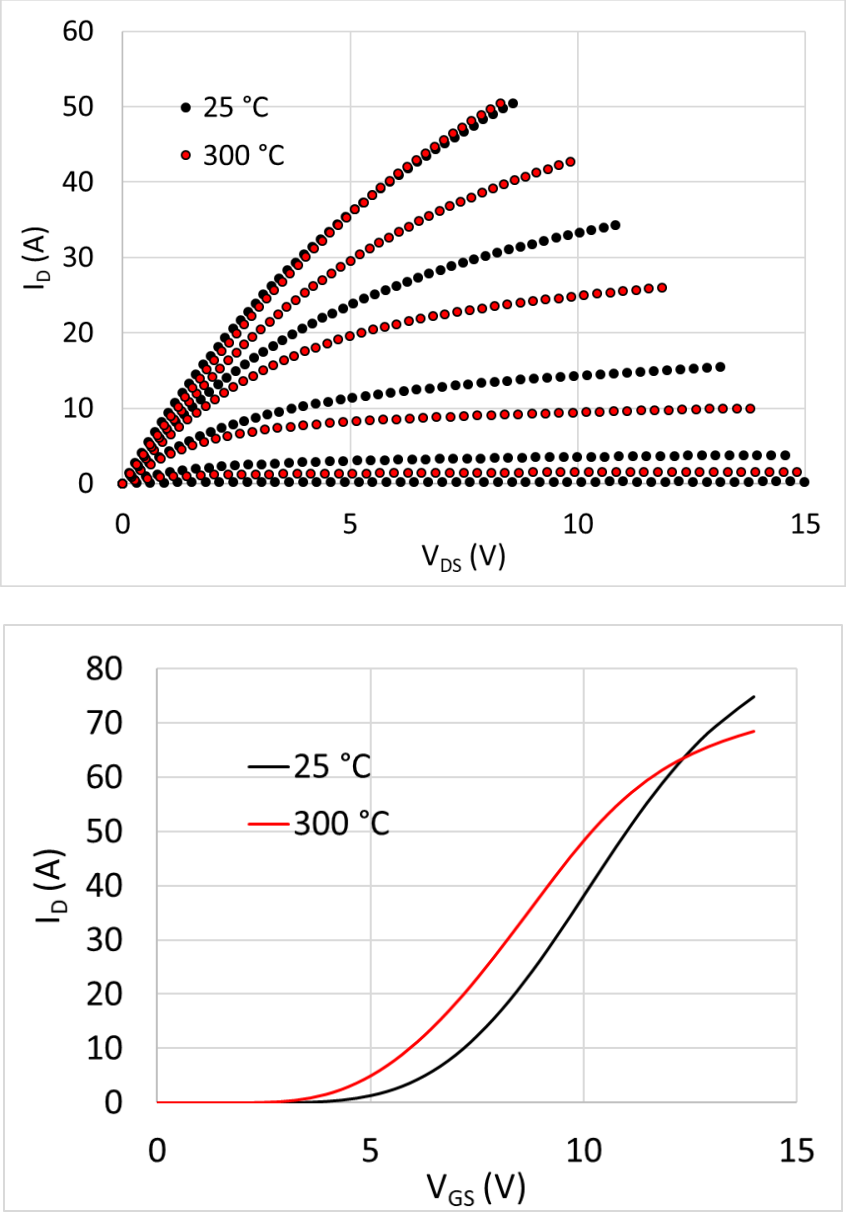


Figure 15. Output characteristic (top) versus transfer characteristic (bottom) of 25 °C vs 300 °C

This work assists in understanding the trends in characteristics when a SiC MOSFET is taken to a higher temperature.

3.3 Dynamic Characterization Background

Dynamic performance of a MOSFET is important to gauge for its use as a power switching device. Through studying the MOSFET switching performance under specified load conditions, its losses

under realistic applications can be predicted. A common dynamic test to study the switching losses of a device is the double pulse test (DPT). In this test, the MOSFET is switched with an inductive load. The MOSFET is switched under high current conditions established by the inductor, and the resultant switching waveforms are analyzed.

Circuit POV:

Figure 16 shows the generic schematic for a DPT setup.

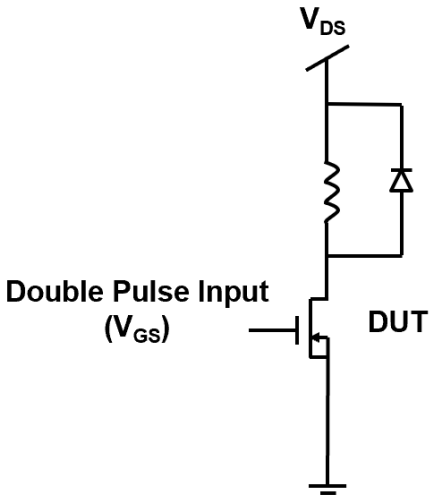


Figure 16. DPT generic schematic

During the first pulse of the DPT, the inductor current rises at a rate of

$$V_L = L\frac{di}{dt} \tag{4}$$

The desired switching current is established during this stage. At this point, the device under test (DUT) is switched off, and the resultant transients are recorded.

Observing the turn-on switching conditions of the device at high currents requires the inductor to 'hold' the current while the device turn-off transients settle. During this time, the inductor current is circulated, or freewheeled, through D1, the diode in Figure 16. In a half bridge configuration,

the top-side switch's body diode is commonly used as the freewheeling diode. The energy dissipated during this time is dictated by the parasitic resistance of the loop.

After ensuring the device turn-off transients are settled, the DUT is turned back on. The inductor current, which ideally suffered minimal loss during the deadtime, continues to circulate through the freewheeling diode until its reverse recovery charge is depleted. The device is then switched on under high current conditions, and the resultant transients are recorded.

Device POV:

(A) Turn-On:

According to [7], the MOSFET switching during turn-on transient can be delineated into 4 stages, as shown in Figure 17.

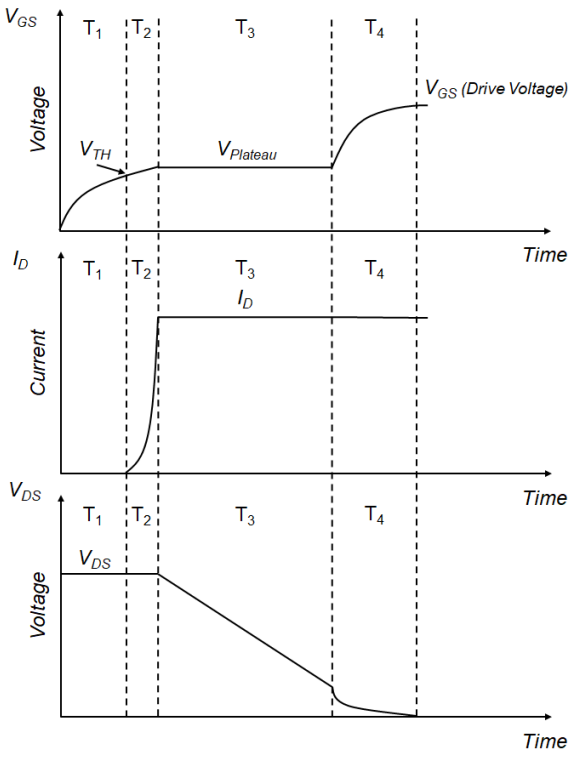


Figure 17. MOSFET switching transient waveforms during turn-on

During Phase T_1, the MOSFET gate voltage rises as dictated by:

$$T_1 = R_G\left(C_{GS} + C_{GD}(V_{DS})\right)\ln\left(\frac{V_{GS}}{V_{GS}-V_{TH}}\right) \quad (5)$$

Once V_{TH} is achieved, the MOSFET is able to conduct current and I_D increases during T_2. The gate voltage during T_3 remains constant at the Miller plateau voltage, $V_{Plateau}$, dictated by:

$$V_{Plateau} = \frac{I_D}{g_m} + V_{TH} \quad (6)$$

Where g_m is defined to be the transconductance, or the slope of the transfer characteristic. $V_{Plateau}$ persists the Miller capacitance, C_{GD}, is charged. The gate current during this time is defined as:

$$I_G = \frac{V_{GS}-V_{Plateau}}{R_G} \quad (7)$$

Here, V_{DS} drops at a constant rate defined by:

$$\frac{dV_{DS}}{dt} = \frac{dV_{Plateau}}{dt} = -\frac{V_{GS}-V_{Plateau}}{R_G C_{GD} V_{DS}} \quad (8)$$

Once G_{GD} is charged, the drain voltage drops to a value of the product between I_D and on-resistance. Gate voltage increases to the voltage provided by the drive circuitry.

(B) Turn-off

Figure 18 shows the turn-off waveform transient breakdown.

During turn-off, the gate voltage initially decreases as dictated by:

$$V_{GS}(t) = V_{GS(ON)}e^{-t/R_G(C_{GS}+C_{GD})} \quad (9)$$

T_1 of turn-off can be determined by:

$$T_1 = R_G(C_{GS} + C_{GD})\ln\left(\frac{V_{GS(ON)}}{V_{Plateau}}\right) \quad (10)$$

At the beginning of T_3 of turn-off, C_{GD} is discharged and gate voltage is held at $V_{Plateau}$.

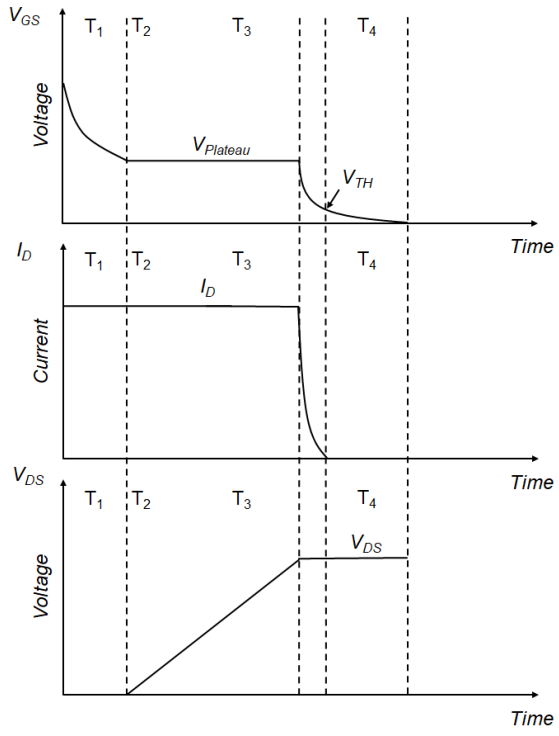


Figure 18. MOSFET switching transient waveforms during turn-off

Gate current during this time is defined by:

$$I_G = \frac{V_{Plateau}}{R_G} \tag{11}$$

The drain voltage rises at a constant rate given by:

$$\frac{dV_{DS}}{dt} = \frac{dV_{Plateau}}{dt} = \frac{I_G}{C_{GD}V_{DS}} \tag{12}$$

This period lasts for a time defined by:

$$T_3 = R_G C_{GS(Average)} \left(\frac{V_{DS}+V_{Diode}-I_D R_{ON}}{V_{GP}}\right) \tag{13}$$

During T_4, V_{DS} is established and I_D is able to transfer from the MOSFET channel to the freewheeling diode.

From the trends observed during high temperature static characterization, the dynamic performance change due to an increased temperature can be predicted. As shown from Table 5, as temperature increases, the threshold voltage is lowered. In addition, the transconductance, as shown by the slope of the transfer characteristics in Figure 15, increases as temperature increases. As shown by (6), the Miller plateau voltage is proportional to threshold voltage and inversely proportional to transconductance. Therefore, the Miller plateau voltage decreases with increasing temperature. As such, the MOSFET is able to turn on faster, and has a faster turn-on current, or *di/dt* for drain current. Additionally, the lower Miller plateau voltage will result in a higher gate current as shown by (7). This will lead to a faster turn-off as the junction capacitance C_{DS}, or the Miller capacitance. In conclusion, the turn-on energy loss for a SiC MOSFET will be lowered in response to an increasing temperature since I_D has an increased *di/dt* and V_{DS} has a faster start to decreasing. The opposite effect occurs during turn-off as temperature increases, therefore increasing turn-off energy loss.

3.4 Dynamic Characterization Results

Figure 19 schematic for the double pulse test along with the relevant values listed.

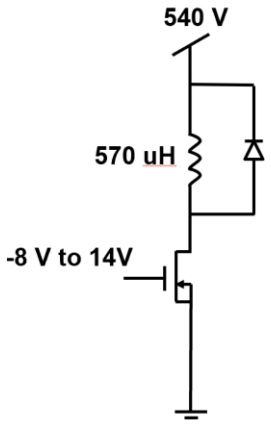


Figure 19. DPT schematic with test values

Figure 20 shows the physical test setup for the dynamic characterization. A hot plate heats up the device while a thermocouple located close to the device monitors the temperature. At temperature increments of 100 ^{0}C, the device is soaked for 15 minutes at each temperature before being pulsed with the double pulse waveform.

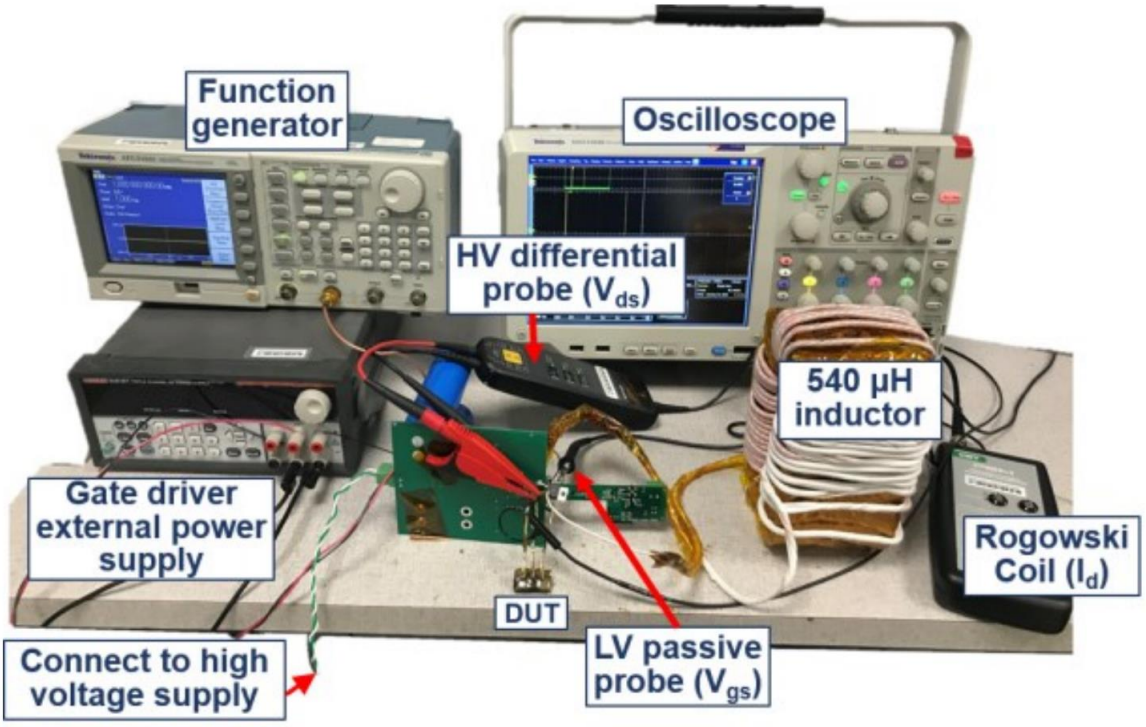


Figure 20. DPT physical test setup

Not pictured in Figure 20 is the hot plate, which is set up to the device in the same way as the static characterization performed in Chapter 3.

Relevant DPT waveforms are shown in Figure 21 below.

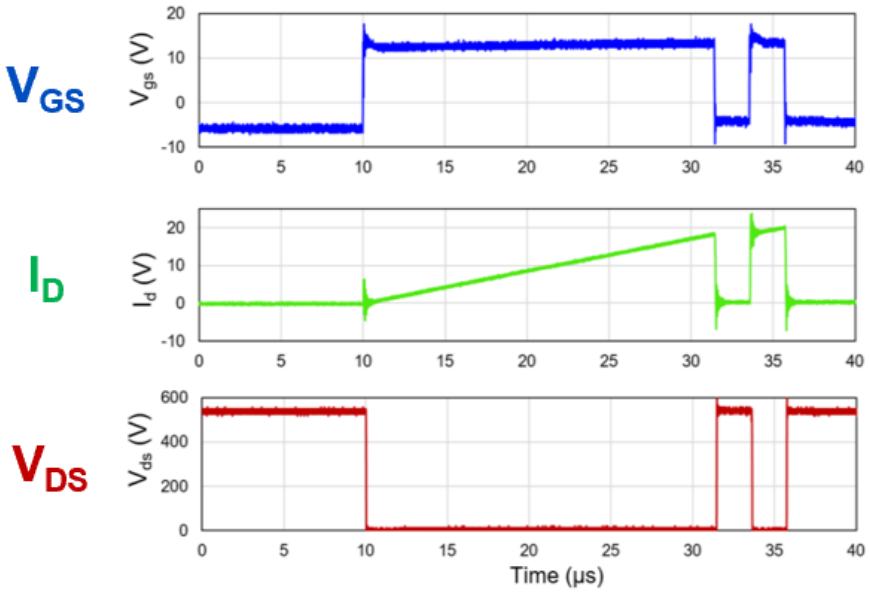


Figure 21. DPT waveform overview

The switching energy loss is calculated and shown in Table 6. Energy loss was calculated to be the absolute value integral multiplication between I_D and V_{DS} during switching transient.

Table 6. Switching Loss Measurement

	Temperature	Turn-On (mJ)	Turn-Off (mJ)	Total (mJ)
Sample 1	25 °C	.193	.97	.290
Sample 1	300 °C	.170	.106	.276
Sample 2	25 °C	.173	.98	.271
Sample 2	300 °C	.165	.101	.266

The energy loss during the switching transient between room temperature and high temperature is relatively close. As expected from theory, the turn-on energy decreases with increasing temperature while the turn-off energy decreases. This trend can be observed for both samples tested. Although the table shows a decreasing trend for total energy loss, the values are so close that any noise could skew the loss values to the opposite trend. Therefore, the conclusion is that

increasing the temperature did a significant impact in the dynamic switching losses given the testing conditions.

Chapter 4 High Temperature Reliability Testing

4.1 Introduction

Silicon carbide (SiC) is a high temperature stable material. When utilized in power switching devices, it shows superior performance over silicon (Si) devices due to its higher electric breakdown field and higher maximum current density [11-12]. It is therefore able to support higher voltages and have a faster switching speed, respectively. SiC power devices such as JFETs were proven to be reliable at high temperatures up to 500 ^{0}C [3]. Although SiC material and other power device structures are proven to be stable at temperatures beyond 300 °C, there is a lack of research in pushing the boundaries of SiC operation and reliability above 200 ^{0}C.

Previous literature shows that reliability of the MOSFET gate oxide layer becomes an issue, especially at elevated temperatures [8]. This is due to the traps present in the gate oxide, which are introduced due the mismatch between the SiC/SiO_2 layer. This mismatch, present from manufacturing processes, is a widely prevalent issue for SiC MOSFET reliability. The effects of this mismatch lead to threshold voltage drifts and are exacerbated by elevated temperatures [8].

For this reason, it is important to study the reliability of the SiC MOSFET at temperatures of 300 °C. To utilize the SiC MOSFET in a power module capable of 300 °C, the selected device must be reliable at high temperatures. There are common industry standards to testing SiC MOSFET reliability; these are observed in selecting the relevant tests to study the reliability of the chosen SiC MOSFETs for the tests.

In this chapter, the mechanism behind SiC MOSFET reliability issues is further explored. Common industry tests for reliability testing is surveyed. Reliability tests are chosen and carried out on third

generation, Wolfspeed SiC MOSFETs that were selected in Chapter 2. The test results are revealed and discussed.

4.2 Mechanisms of Reliability Testing

Typically, power devices such as the SiC MOSFET are designed to last for significant periods of time when operating within their recommended conditions. Testing the lifetime of these devices under nominal conditions could possibly take thousands of hours. To make the testing more feasible in terms of time, the MOSFET can be placed under stress beyond their recommended conditions to accelerate the degradation. Thus, the actual lifetime can be extracted from how severe the stress was. These tests are called accelerated lifetime bias tests (ALBT).

Several industry standards exist for ALBT for MOSFETs. Through these tests, the blocking capability, the turn-on characteristic, and other aspects of a power switch can be tested for lifetime during normal use. Some include specific conditions necessary for operation, such as high humidity or low pressure.

A survey literature that worked with ALBTs shows that high temperature gate bias (HTGB), high temperature gate switching (HTGS), high temperature reverse bias (HTRB), temperature cycling (TC), and power cycling (PC) are common tests for determining the reliability of MOSFETs [14-64]. Other reliability tests included high humidity environment ALBTs, short circuit testing, avalanche ruggedness, and body diode reliability. A distribution of the occurrence of each test in all papers surveyed is shown in Figure 22.

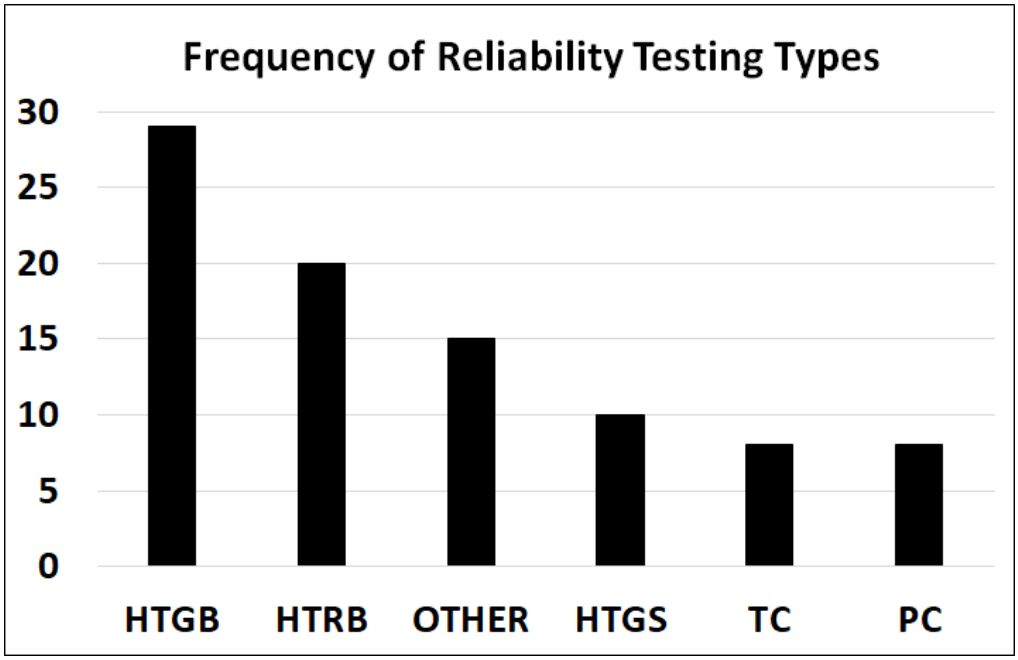


Figure 22. Frequency of different types of ALBTs over a review of literatures

Types of tests selected were based on how commonly each test was chosen across the surveyed literature. The tests selected for determining the selected SiC MOSFETs in the high temperature packaging were HTGB and HTRB. Although HTGS was also commonly mentioned during each test, it was not chosen because the results from HTGS show a that threshold voltage does not drift in a significant manner as compared to HTGB testing [3]. Effectively, HTGB can be considered as the worst-case scenario of HTGS as HTGB provides a constant, unchanging bias across the gate to source terminal of the MOSFET. An electric field that is changing in polarity or reducing in intensity periodically will not stress the device as effectively. [3] compares the threshold voltage shift following an HTGS compared to an HTGB.

HTGB and HTRB tests stress the turn-on capability and the blocking capability of the MOSFET, respectively. HTGB is a gate stress, which provides a static bias across the gate to source terminals.

Figure 23 shows the cross-sectional structure of a vertical power MOSFET. A MOSFET requires a SiC/SiO_2 in the gate interface to fabricate the gate metallization. This layer, extensively studied for Si MOSFETs [9], introduces defects that affect the device reliability and performance. The origin of these defects is suspected to be from the incompatibility in geometry of the SiC layer with the oxide layer [10].

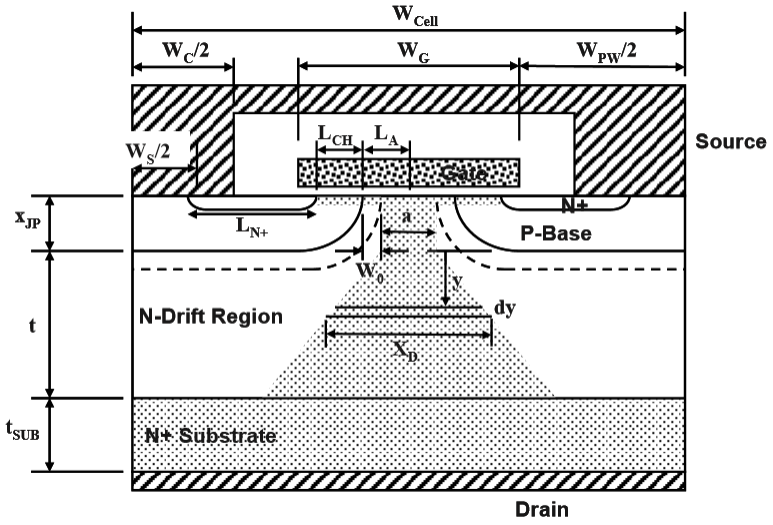


Figure 23. Vertical power MOSFET structure [7]

Studies on Si MOSFETs show these defects can include oxide traps and interface traps, which are localized within the interface region of the SiC/SiO_2 layer and SiO_2 layer, respectively. These traps can be visualized as leaks in the wall that is the insulating layer, or the oxide layer. As electrons are trapped, there are less available for free movement required to form a conducting channel. This effect is known to be exacerbated by elevated temperatures when the MOSFET is under an electric field bias, or an applied voltage at the gate. Elevated temperatures are suspected to activate, or energize, more traps [8].

Other gate bias breakdown mechanisms at high temperatures include gate oxide material breakdown and intermetal dielectric breakdown [11]. Precursors for degradation at the gate include a shift in threshold voltage and an increased gate leakage current [11].

For HTRB, possible breakdown mechanisms include edge termination breakdown, gate oxide breakdown, and SiC breakdown. Edge termination breakdown could occur due to the high electric field intensity between the top of the die metallization, which is the gate/source, and the bottom of the die, which is the drain. As the edge termination needs to hold the voltage potential between the terminals, a high electric field over this region for long periods of time could result in degradation of the insulation capability. SiC breakdown is related to electron and hole tunneling in defects within the SiC layer [9]. Gate oxide breakdown could occur due to HTRB due to a presence of high electric field within the gate oxide even when there is only a voltage bias applied at the drain to source terminal. Although during HTRB conditions, the gate is tied to the source at ground potential, simulations for a 1 kV, SiC MOSFET with 0 V at the gate show that there exists a significant electric field within the gate oxide region, as illustrated in Figure 24.

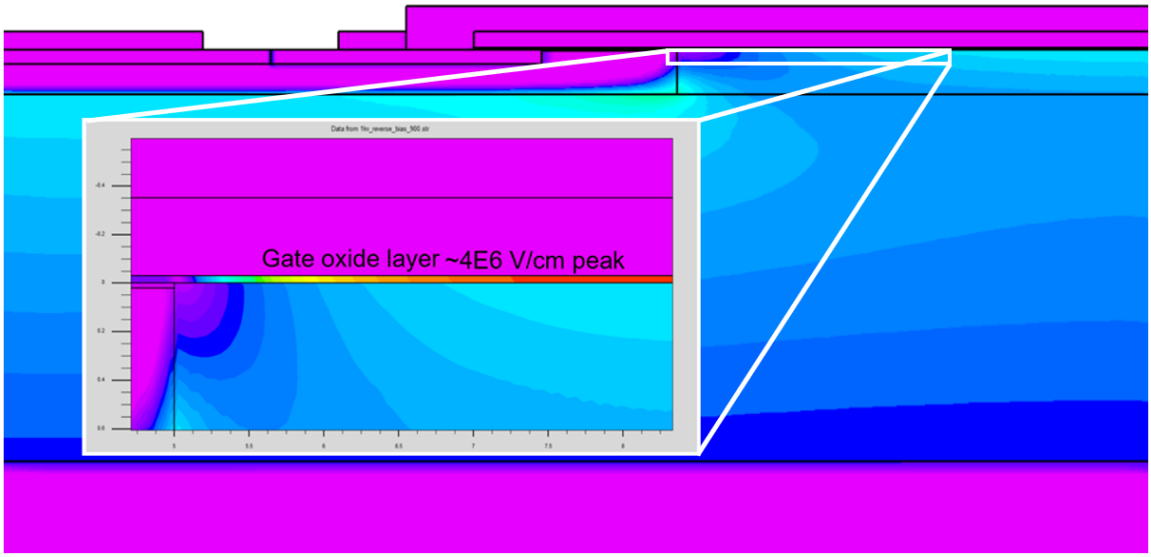


Figure 24. Electric field intensity simulation for 1kV SiC MOSFET

Precursors for degradation for HTRB can include an increased drain leakage current, a shift in avalanche breakdown voltage, and an increased gate leakage current [11].

4.3 Reliability Testing Results

HTGB and HTRB testing conditions were determined using industry guidelines. JEDEC's 22A108F and AEC's AECQ101 were used as references [12-13]. The HTGB had a 12 V bias at the gate, which was 80% of the maximum datasheet value (15 V). The HTRB had an 800 V bias at the drain, or 80% of the maximum datasheet value (1000 V). For the HTGB test, drain was tied to source, which was connected to ground. For the HTRB test, gate was tied to source, which was connected to ground.

The test setup of the HTGB and HTRB tests is shown in Figure 25. 16 samples are spread out on a hotplate, with 8 samples connected in an HTGB bias and the other 8 connected in an HTRB bias. These devices are heated to 300 °C; with the hotplate temperature monitored through a thermocouple. Every 100 hours, device characteristics were monitored on the Agilent B1505A curve tracer. Characteristics monitored included gate threshold voltage, gate leakage current, avalanche breakdown voltage, and drain leakage current. To measure on the curve tracer, the devices were first cooled down to room temperature and measured at room temperature. After measurement, devices were placed back under their respective ALBT stresses and heated up to 300 °C again until the next 100-hour increment. The tests were planned for 1000 hours or until all the samples failed. Failure was defined to be when the devices catastrophically failed with a gate-short or a drain-short.

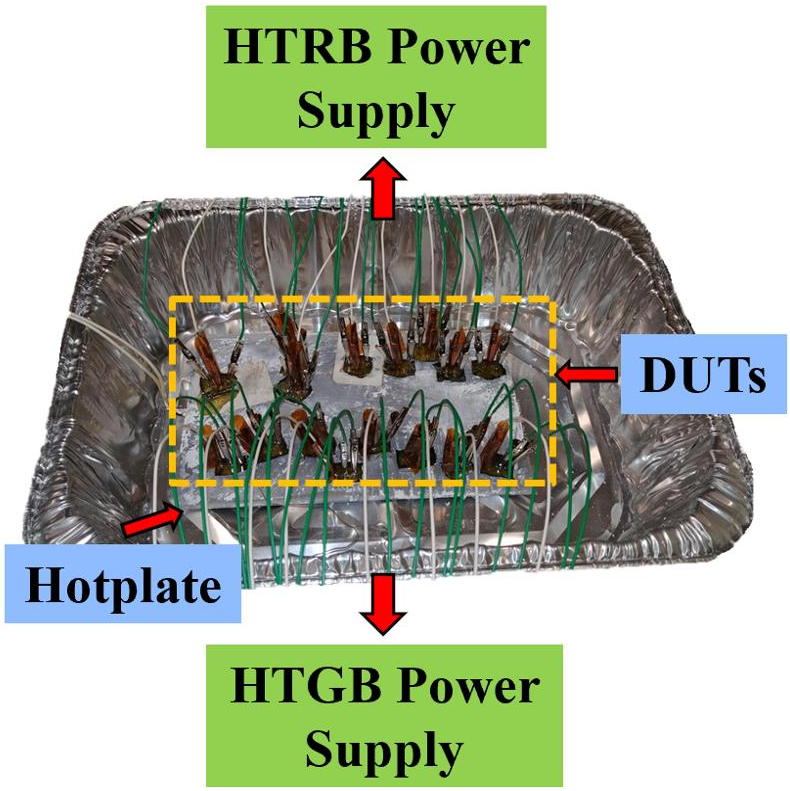


Figure 25. HTGB and HTRB setup

Figure 26 shows the test results for the HTGB and HTRB tests. As shown, 6/8 samples for HTRB failed within the first 100 hours. Although 2/6 samples failed for the HTGB within the same amount of time, most of the samples failed within the next 100 hours (200-hour mark). All the samples failed within 300 hours. Given that the electrical biases for these test conditions were within datasheet nominal values, we can assume that at 300 °C, these devices are not reliable within 300 hours.

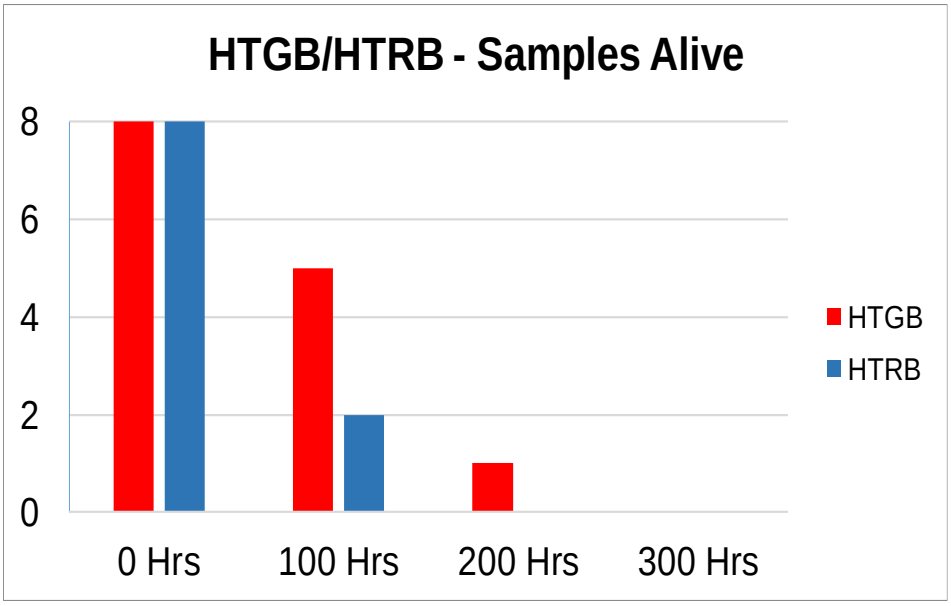


Figure 26. HTGB and HTRB test results over 300 hours

All the devices were past the datasheet nominal value for threshold voltage for HTGB within the first 100 hours. These extreme shifts in threshold voltage could potentially cause issues when considering precise turn-on and turn-off timing, switch paralleling, and other applications.

As the devices failed rapidly at 300 °C, temperature was modulated during further testing to determine the threshold temperature at which the MOSFETs fail rapidly. Here, the goal of making further samples and testing under ALBT conditions was to explore the relationship between elevated temperature and reduced lifetime of MOSFETs.

To achieve this, more samples were created to place under HTRB bias. HTRB bias was chosen as the method for further testing due to its higher percentage of failure within 100 hours compared to HTGB bias. As we were concerned with the Boolean condition of whether the device was reliable or not, any sort of failure was a condition that fulfilled the defined criteria.

Figure 27 shows the package used for further HTRB testing. Here, the encapsulation was changed to a commercial epoxy, Durapot 863. This encapsulant, rated for temperatures up to 343 ^{0}C, served

as replacement for the lead glass encapsulant that was previously used. This encapsulant was chosen due to limited availability of the glass.

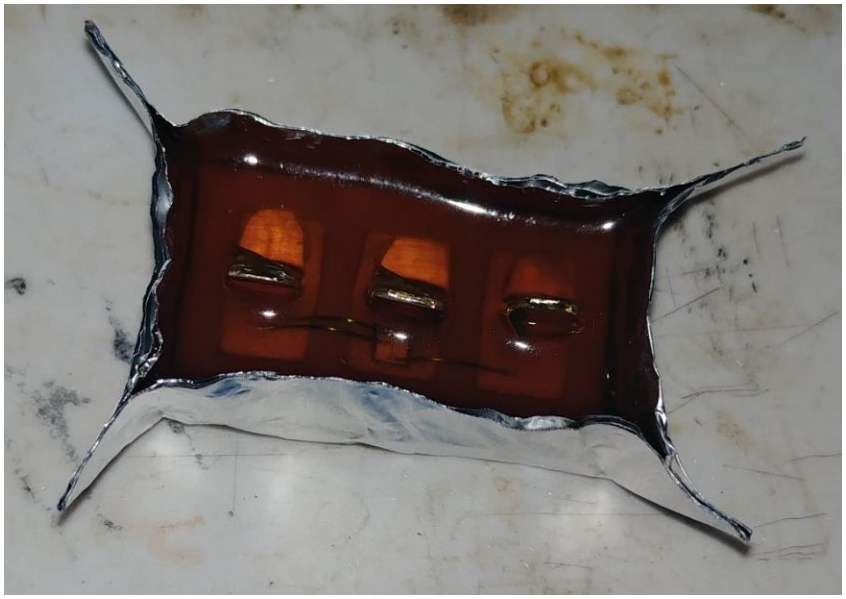


Figure 27. Durapot 863 encapsulated SiC MOSFET sample

The relatively low temperature curing compared to lead glass made the fabrication process easier to control. The oven was also not required to be open for long periods of time while glass was poured over the samples, eliminating a temperature variability during the beginning stages of the curing profile. Additionally, this material did not damage the die during while hardening, eliminating the need for the polyimide buffer layer between the die and the encapsulant. Overall, the new encapsulant provided benefit of tighter control of the curing profile as well a simplified fabrication process over the lead glass.

Initially, a benchmark sample was tested at 150 ^{0}C, with 3 samples tested under HTRB bias and 1 sample with no electrical connections. These samples were used to verify the package and MOSFET feasibility when the device was under nominal datasheet conditions. For this purpose,

the MOSFET was the bottleneck with a datasheet temperature limitation of 150 ^{0}C. After 240 hours, no characteristics monitored showed a markedly different value.

Using the new method of packaging, an exploratory sample was created. This exploratory sample served as an initial survey of the temperature range at which the SiC MOSFET would fail. Previous literature has SiC MOSFET reliability tests at temperatures up to 200 ^{0}C—therefore, the temperature range we are interested in studying is between 200 ^{0}C to 300 °C. As this is a large temperature range to test multiple samples for each increment, the exploratory sample was used to narrow down the range of temperature.

Table 7 shows the planned testing profile for the exploratory sample. Temperature ranges from 150 ^{0}C to 200 ^{0}C 48 hours of stress time compared to the 100-hour stress time for higher temperatures as previous literature for SiC MOSFETs already tested up to 200 ^{0}C for reliability testing.

Table 7. Testing times for exploratory sample

Temperature (^{0}C)	Time Stressed
150	48 Hours
175	48 Hours
200	48 Hours
225	100 Hours
250	100 Hours
275	100 Hours
300	100 Hours

This exploratory sample failed at 250 °C, with a short between the drain and source. Consequently, 8 more samples were created and tested under HTRB bias at 250 °C.

These 8 samples were tested thus: the devices were heated to 250 °C. Every 12 hours, the device characteristics were measured through the Agilent B1505A curve tracer. Characteristics monitored included threshold voltage, gate leakage current, drain leakage current, and avalanche breakdown voltage. The devices were cooled to room temperature before making the curve tracer measurements. After making the measurements, they were placed under HTRB bias and heated back up to their testing condition. These devices were tested until a short was observed between the drain and source of the device.

Figure 28 shows the results of the 250 °C HTRB tests.

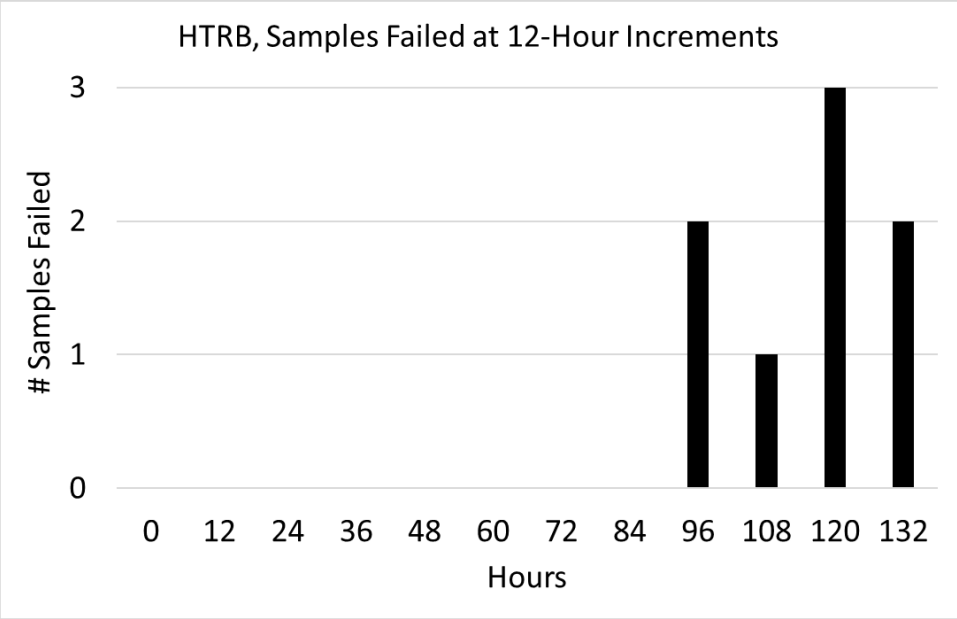


Figure 28. HTRB testing results

As shown, all 8 samples failed within 132 hours.

4.4 Conclusions on Reliability Testing

This chapter explores the concept of third generation SiC MOSFETs being used for a high temperature power module. Although SiC power devices such as the JFET are already

experimentally verified to be reliable at temperatures above 300 °C, there is a motivation to study the reliability of the MOSFET due to its advantageous voltage driven, normally off operation. To determine the reliability, two common tests for reliability are chosen—HTGB and HTRB. These tests stress the gate reliability and blocking reliability, respectively.

When stressed through industry standard based reliability testing, the SiC MOSFETs lasted less than 200 hours at 250 °C. It can be concluded that SiC MOSFETs are not reliable at temperatures at or greater than 250 °C. To realize a high temperature capable power module, alternative choices should be selected, such as the SiC BJT and JFET.

Chapter 5 Conclusions and Future Work

1.1 Summary

In this thesis, the concept of a silicon carbide (SiC) MOSFET as a device in a high temperature power module for aerospace applications was explored. To achieve this study, a high temperature package was fabricated for the SiC MOSFET. The device, with the high temperature package, was tested for operation and reliability at 250 °C and above.

1.2 Conclusions

As wide bandgap devices, SiC MOSFETs have the advantage of a higher critical electric field (E-field) and thermal conductivity, making them a suitable choice for high voltage, high temperature applications. Other SiC transistors, such as BJTs and JFETs, have proven to be reliable and operational at high temperatures exceeding 250 °C, thus providing evidence that SiC transistors can far exceed the standards for Si temperature limits [4-5]. Though significant progress has been made in the semiconductor industry for SiC MOSFET fabrication, there remains a lack of research in pushing the high temperature operation and reliability beyond 250 °C for the newest generation of SiC MOSFETs available.

Incorporating the SiC MOSFETs into a high temperature capable package was an overall success. Static characterization showed that the packaging process did not have any immediate damage to the die; dynamic characterization provided further experimental evidence of the SiC MOSFET functioning within normal parameters.

Experimental results from show that current generation SiC MOSFETs are not reliable at temperatures of 250 °C, and quickly break down over a period of 140 hours when stressed with

accelerated lifetime bias tests (ALBT). Static characterization at 300 °C supports the idea that short term operation of SiC MOSFETs at high temperatures is possible.

1.3 Future Work

Understanding the failure mechanisms related to the ALBTs performed on the SiC MOSFETs is important in selecting a device that is suitable for a high temperature capable power module. To analyze the failed packages, imaging techniques such as scanning electron microscope and focused ion beam imaging could be performed on the die. Encapsulation would have to be broken down to reveal the bare die—techniques such as corroding the encapsulation with hydrochloric acid could be applied.

Expected results from imaging the die could reveal the breakdown mechanisms discussed in Chapter 4 in the form of physical damage to the die. To clarify, the damage to the die would be localized to the point where damage occurred—for example, gate oxide breakdown would show a damaged gate oxide layer and edge termination breakdown would show a damaged edge termination.

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