**Time Domain Device Modeling of**

**High Frequency Power MOSFETs**

**by**

**Richard W. Hoagland**

**Thesis submitted to the Faculty of the**

**Virginia Polytechnic Institute and State University**

**in partial fulfillment of the requirements for the degree of**

**Master of Science**

**in**

**Electrical Engineering**

**Approved:**

Aicha Elshabini-Riad

A. Elshabini-Riad, Chairman

D. J. Moore

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**December, 1993**

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(Abstract)

The development of the High Frequency Power MOSFET has brought about a need for accurate models. Now that the frequency range of these MOSFETs is in domains where typically scattering parameter measurements are used, a broad band device model can prove to be extremely useful. This thesis summarizes the research performed towards the development of a wideband Gate model for the Motorola MRF162 High Frequency Power Transistor. The device theory for typical MOSFETs will be explained. This theory will lead into the development of the Power MOSFET and its associated frequency limitations. The benefits of Time Domain Techniques will be explained and how a wideband model is achieved from this technique. The result from the analysis of the measurements and the device theory is a wideband Gate model developed for the frequency range from 100MHz to 400MHz. Verification is achieved by curve matching the measured Time Domain Reflected waveforms with the simulated waveforms generated using a proprietary program Modified Transient Analysis Program (MTCAP) and by comparison of expected and simulated parasitic values.

# Acknowledgment

I offer each committee member my sincere thanks. A true appreciation goes out to Dr. Elshabini-Riad for her friendship, support, and time. I also thank Dr. Moore and Dr. Riad for their friendship and commitment. The assistance with the TDR measurements from Dr. Su is deeply appreciated

I thank family, friends, and especially Mary for making me explain my thesis to them **several** times while they actually pretended to understand. Most of all I would like to express my gratitude to my family who has made graduate school possible.

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# Chapter I. Introduction

## 1.0 Introduction

Power Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) became an integral part of microwave design during the past decade. It has been sixty years since the concept of the first FET was conceived by Lilenfeld and Hiel [1]. It has only been within the past Thirty years that the first working MOSFET has been developed. By the mid seventies power MOSFETs were available for switching applications. With the introduction of gallium arsenide (GaAs) Technology MOSFETs began to overtake applications typically reserved for high frequency Bipolar-Junction Transistors (BJTs). With new developments in geometry, MOSFETs have been able to reach microwave frequencies and also handle power on the order of tens of watts.

There are several reasons why power MOSFETs frequency response lags far behind the low power MOSFETs. The limiting factor for high speed switching is the parasitics and the circuits used [Grant]. The power FETs use a different geometry in order to maximize current carrying ability and to effectively use the substrate. The problem here is that while gaining power handling capability, the FET looses its high frequency ability due to an increase in parasitic capacitance and inductance.

A low power MOSFET uses a lateral design in which the Gate, the Drain, and the Source are on the top surface. In contrast, the power FET uses a vertical design in which

the Drain is located on the bottom side of the substrate and the Source and the Gate remain on the top. The advantage of the vertical design is that it improves current flow within the device, but also makes it very easy to connect the devices in parallel. This geometry increases the power handling capability by increasing the amount of current that can pass through the linked devices.

The critical factors in a power MOSFET are very high input impedance, high current capability, low On-resistance, and a high breakdown voltage. As in most cases, there are trade-offs for obtaining one or the other. For instance, the current handling capability will decrease as the breakdown voltage increases.

High Frequency Power MOSFETs require special modeling techniques. The present low frequency models will not accurately represent the device in the higher frequency ranges. Traditionally, frequency domain techniques have been used model devices that operate in the range above a few hundred megahertz. Time Domain Reflectometry (TDR) Techniques offer a wideband model with only one measurement. This is vastly more simple then the many frequency measurements necessary to obtain scattering parameter model. TDR techniques also provide physical insight to device characteristics.

## 1.1 Objective

The objective of the research is to develop a wideband Gate model of a High Frequency Power MOSFET using Time Domain Reflectometry (TDR) Techniques. These

techniques will provide a wideband model not previously obtainable using Frequency domain methods. In this development, the MOSFET device theory will be covered as well as its predecessor the Power MOSFET. This theory development is important since both physical insight and knowledge are in required to properly develop a device model using Time Domain Techniques.

## 1.2 Overview

The two types of microwave modeling and characterization measurements are frequency domain and time domain techniques. Chapter 2 introduces the two techniques and provides a background on the these techniques are used to model devices. Particular attention is given to Time Domain Techniques in this thesis work. The Time Domain Reflectometry (TDR) device modeling program MTCAP is introduced.

Basic MOSFET theory is developed in Chapter 3. The modes of operation, the electrical characteristics and the physical device characteristics are covered in this chapter. The developments in this chapter will lead into the Power MOSFET theory provided in Chapter 4.

Chapter 4 contains the analysis and the physical characteristics of the Power MOSFET as well as the principle frequency limiting aspects. Parasitic capacitances, terminal and On-resistances are covered. Finally, Power MOSFET device modeling is evaluated.

Chapter 5 explains the experimental procedures that were taken to develop the wideband model. The wideband MOSFET Gate model is presented and the lumped values are explained in this chapter.

Finally, Chapter 6 offers concluding remarks as well as topics for future research investigation.

# Chapter II. Microwave Circuit Analysis

## 2.0 Introduction

An accurate device model is essential to all network synthesis techniques. Computer process power has progressed to the point where computerized simulation is an expected step in the development of networks of different complexity. Accurate device modeling allows iterative simulations to accurately describe the expected response from the network. Now that electronics has reached ranges well into the microwave region, accurate simulation is an essential requirement; otherwise, needless time could be spent building physical circuits that do not function well due to inaccurate or insubstantial calculations.

Active devices that operate in the microwave range provide a particular challenge in the development of device models. The voltage and current must be treated as waves at these high frequencies. Transmission line theory and scattering parameters must be considered to accurately describe the device performance. The two types of microwave modeling and characterization measurements are frequency domain and time domain techniques.

Frequency domain measurement techniques accurately describe linear device characteristics. On the other hand, time domain waveforms also contain the nonlinear information portion. The second advantage of time domain techniques is that only one

waveform is needed to determine the device characteristics over a wide range of frequencies.

In this Chapter, a time domain characterization technique is presented for the modeling of High Frequency Power Transistors. A description will be given on frequency and time domain approaches. The work will illustrate how the resultant time domain waveforms can be used to obtain device models through mathematical techniques and by using computer analysis programs such as the Modified Transient Circuit Analysis Program (MTCAP).

## 2.1 Transmission Lines and Scattering Parameters

Microwave device modeling cannot be explained without first understanding the basics of transmission lines and scattering parameters theories. The following descriptions are aimed at providing a brief review of both theories.

The Device Under Test (DUT) requires a simple setup in order to measure the scattering parameters (Fig. 2.1.1). The configuration shown is for a two port device with a transmission line at the junction of each port. The transmission lines can take on four configurations: coaxial line, microstripline, stripline, coplanar line. The elements that make up the equivalent model (Fig. 2.1.2) are,

R ~ series resistance

L ~ series inductance

G ~ shunt conductance

C ~ shunt capacitance

$\Delta X$ ~ transmission line distributed length

The scattering parameters play an important role in device modeling. It is through the S-parameters that the DUT can be accurately modeled. Figure 2.1.3 shows the signal flow graph for a two port 'black box' network.

$a_1$ & $b_1$ represent the incident and reflected waves on port 1, respectively.

and

$b_2$ & $a_2$ represent the transmitted and reflected waves on port 2, respectively.

The output waveforms are of the form:

$$b_1=S_{11}a_1 + S_{12}a_2$$

and

$$b_2=S_{21}a_1 + S_{22}a_2$$

Therefore, the individual coefficients are:

$$S_{11} = \frac{b_1}{a_1}, \quad a_2 = 0$$

$$S_{21} = \frac{b_2}{a_1}, \quad a_2 = 0$$

$$S_{12} = \frac{b_1}{a_2}, \quad a_1 = 0$$

$$S_{22} = \frac{b_2}{a_2}, \quad a_1 = 0$$

The understanding of these fundamentals is essential to the understanding of wideband device modeling.

## 2.2 Frequency and Time Domain Techniques

A review of literature reveals that the majority of device modeling has been achieved in the frequency domain under small signal conditions [19,20]. The frequency domain technique involves mounting the device under test (DUT) on or at the end of a transmission line. The scattering parameters are then measured. It is from these S-parameter measurements that lumped elements can be extracted using network synthesis methods; therefore, modeling the DUT.

To obtain a frequency domain measurement, it is necessary to find the S-parameters under different bias conditions. Also, for each bias condition, it is necessary to sweep each frequency in the range of interest. The measurements must be derived this

way because the values of the lumped elements will change under different biasing conditions. This measurement can be automated using the HP8510 Network Analyzer. Even with the automated measuring equipment, the frequency domain model does not account for the nonlinearities encountered in the lumped elements. This type of modeling illustrates the performance under specific conditions with out any justification [19,20].

Time domain measurement, in contrast, only requires one S-parameter measurement, a transient response or a step waveform. Both the reflected and transmitted responses to the test waveform can be analyzed using the appropriate Fourier Techniques and the resulting reflection coefficient will hold for a wide range of frequencies. Under a few special conditions, it is possible to obtain a characterization of just the DUT and avoid the stray characteristics of the connectors or port mismatches. Nicolson [21] shows that by scanning the portion of the waveform that represents the transient response of the DUT, the spectrum of the Fourier transform will not contain errors due to these mismatches [21]. It is important, using this technique that any mismatches do not have long transient responses that could possibly overlap the DUT's response. These mismatches cause errors when the Fourier transform is performed; and thus, the resulting model will not be accurate.

## 2.3 Time Domain Reflectometry Technique (TDR)

The experimental setup for Time Domain Reflectometry (TDR) measurement consists of a fast pulse generator, a feed through sampler, a sampling oscilloscope, a

computer for data storage, and a transmission line with a device mounted on it (Fig. 2.3.1a) [22,23]. The equivalent model for HP components is shown in Figure 2.3.1b. The TDR measurement involves launching a pulse down a transmission line through the feed through sampler and then along the 50Ω transmission line in which the DUT is mounted. The reflected signal then travels in the opposite direction, where the computer can record the reflected waveform as a function of time. Before the reflected waveform is measured, the reference waveform should be measured by connecting a short in place of the DUT. This step is used to compensate for the unwanted effects of the connecting cables and connectors [19,23]. Both the reference and the response waveforms are stored in order to conduct further analysis and signal processing.

Active devices, such as transistors, must be properly biased and isolated using a bias-tee arrangement (Fig. 2.3.2). Improper isolation can cause damage to the transistor as well as the pulse generator. If just the TDR measurement is to be taken, the output of the transistor should be properly terminated with a matching load.

Once the two waveforms have been recorded, the type of modeling method must be determined. Two such modeling methods are iterative improvement and single discontinuity. The technique of single discontinuity relies on simple resistive, inductive and capacitive discontinuity relationships. This method becomes difficult to use because as the test pulse encounters each discontinuity, it becomes degraded and will not give the same ideal result for the next discontinuity down the line. The discontinuity method becomes more of a problem when the discontinuities are closely spaced and/or they

contain composite elements in nature. There are techniques to help overcome these problems; such as, the deconvolution of the reflected signal, thus removing the dependence of the test signal. Deconvolution may help the problem of multiple elements by exposing various element contributions, but it cannot cure the problems due to discontinuities and overlapping time windows. Homomorphic deconvolution can help separate the overlapping contribution, but this technique has its limitations [24]. The two signals should have substantially different frequency content for the method to work effectively [25].

The iterative improvement method avoids the problems of closely spaced and composite discontinuities that plague the single discontinuity method. For this method, an initial model is derived from the TDR information [26], the devices differential equations [19], or the previously obtained linear device model [20]. A computer simulation is performed on the model and the results are compared to the results of the measured reflected waveform. Adjustments can then be made on the model to help improve the match. The adjusted model is then simulated again and the results are compared. The process is repeated until an acceptable match is acquired [27].

For the cases of iterative improvement, TDR information and previous linear device model, it is necessary to have a program that will perform the transient analysis of the device model. PSPICE can simulate a transient analysis but the incident waveform must be approximated to an ideal case. In contrast, a program such as MTCAP can use the actual data recorded from the TDR measurement. For the case where differential

equations are used, the program required must solve the equations given the input and reflected waveforms.

## 2.4 Modified Transient Circuit Analysis Package (MTCAP)

MTCAP is an in-house developed program and is specifically designed to use transient analysis to simulate microwave device models. The models developed through this program use standard elements, such as, resistors, linear and nonlinear capacitors, inductors, lossless transmission lines, and other elements. The excitation waveform data is provided by the user; this would be the data collected from the measurement of the reference waveform. The object of running multiple computer simulations is to match the simulated output with the measured reflected response. The modeling process begins by trying to match the first discontinuity (the one closest to the launching end). For this reason, it is required to have some knowledge of the responses different discontinuity configurations are likely to give. An element is selected that will give the same type of discontinuity configuration as the first discontinuity displayed in the measured response waveform. A suitable value is assigned to this element and the circuit is simulated. The simulated response is compared to the measured waveform and the appropriate adjustments are made to the element value in order to match the two responses. The process is repeated until a close match is obtained on the first discontinuity. Once the element is correctly adjusted, it is considered fixed and subsequent elements added to model later discontinuities will not effect the previous waveform matching since the work

proceeds in the time domain [28]. The next element is added to the model and the iteration process is repeated. Once all the discontinuities have been accounted for, the model is complete and it should accurately describe the microwave characteristics of the device under test. The result of this technique will not provide a unique model . TDR techniques are dependent on the individual modeler and the accuracy of the matched waveforms [22].

## 2.5 Conclusion

This chapter explored the steps and techniques necessary to develop a wideband model of a device such as a transistor using time domain techniques. A review on scattering parameters and transmission lines was provided in the first part of the chapter, then frequency and time domain measurements were briefly discussed. The second half of the chapter discussed how the measurements are converted to discrete elements (resistors, capacitors, and transmission lines), representing the device performance (electrical network model). Finally, specific reference was given to the program MTCAP with an explanation on how the program helps develop an accurate device model.

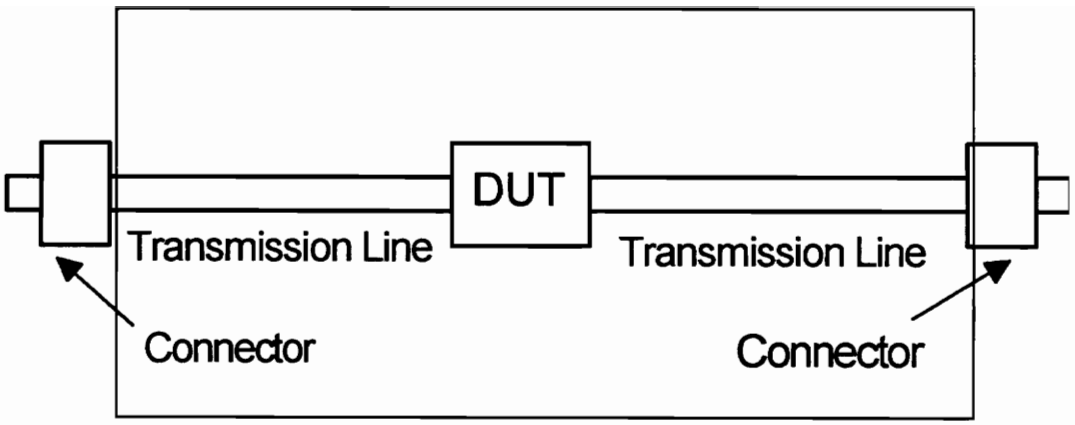



**Figure 2.1.1 Mounted device**

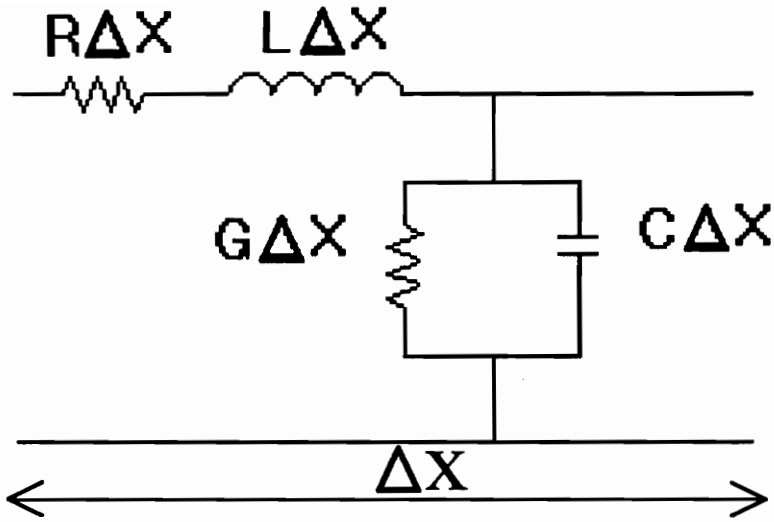



**Figure 2.1.2 Equivalent circuit model for transmission line increment**

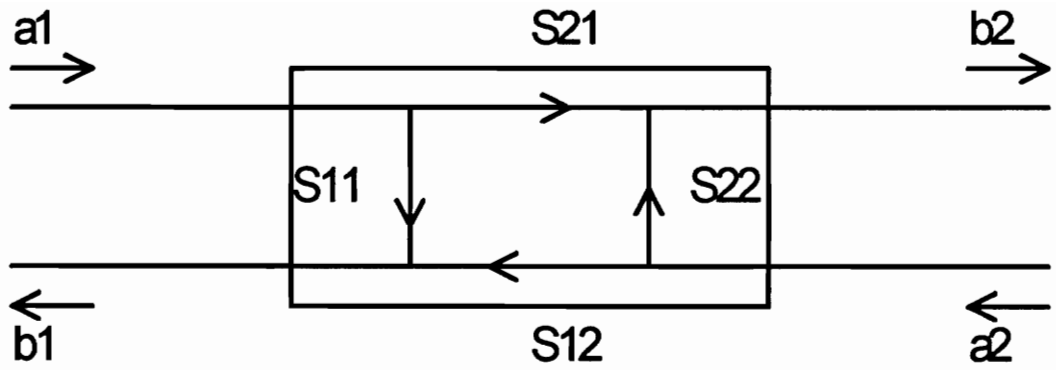



**Figure 2.1.3 Two port S-Parameter signal flow graph**

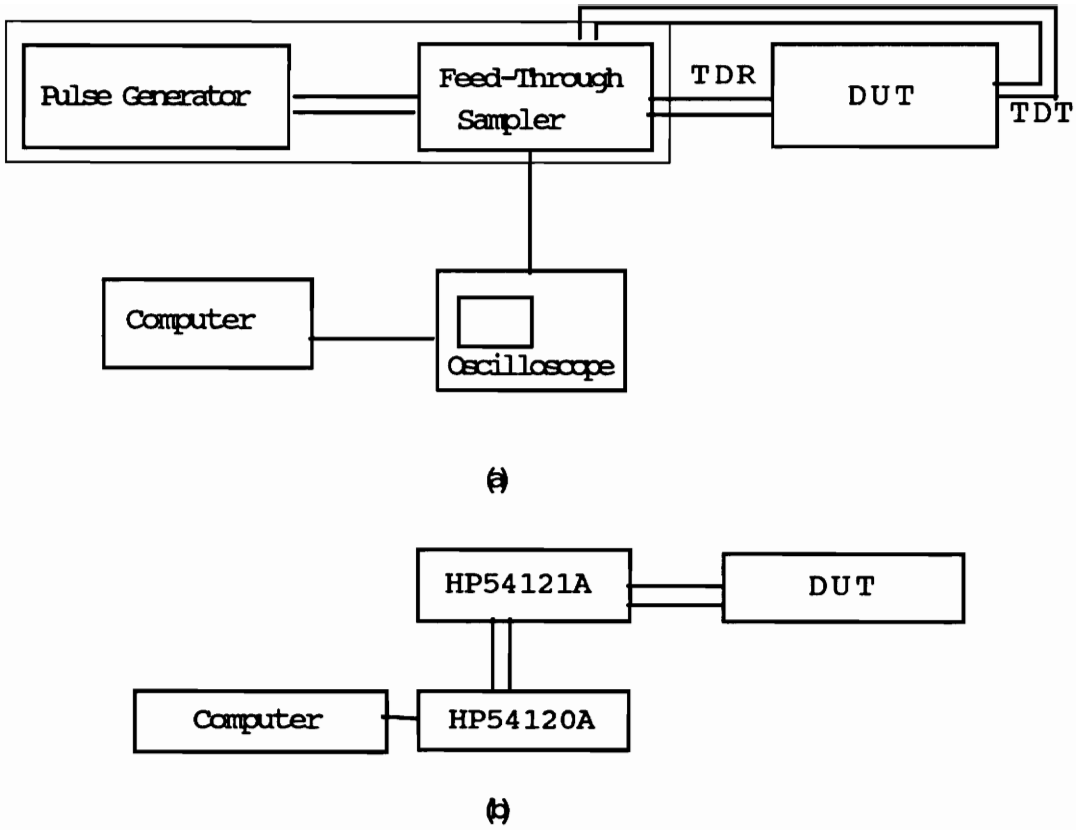



**Figure 2.3.1 Measurement device configuration**

**(a) General Setup**

**(b) Actual Hewlett Packard Setup**

**TDR: Time Domain Reflectometry line**
**TDT: Time Domain Transmission line**

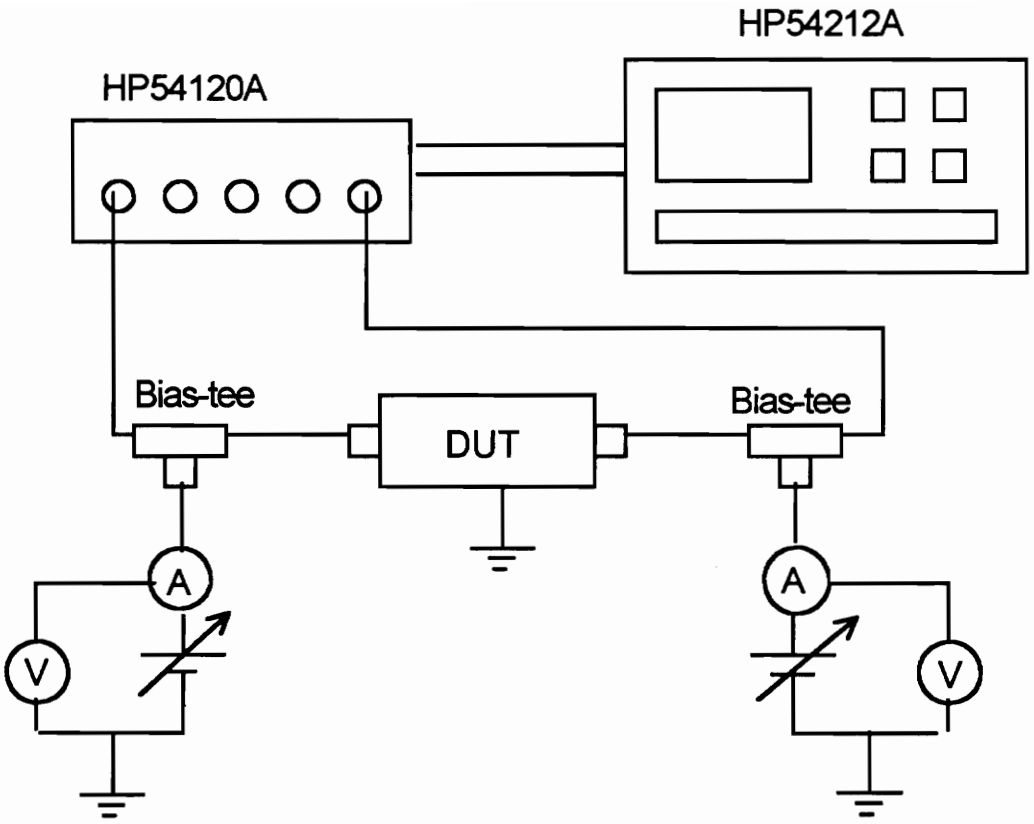



**Figure 2.3.2 Time Domain Measurement Setup**

# Chapter III. The Basic Theory of MOSFETs

## 3.0 Introduction [1,2]

The original Metal-Oxide-Semiconductor Field Effect Transistor, MOSFET, proposed by Clienfeld and Heil [1] in 1903 is a low power surface field-effect transistor. The concept has evolved finally to a design developed by Kahnj and Aptyalia in 1960 [1]. This chapter will explain the basic planar surface geometry of MOSFET devices and the corresponding analysis of a typical low power MOSFET. This development and understanding of the basic MOSFET structure will lead into the development of the power MOSFET in Chapter 4.

## 3.1 Basic Kinds of MOSFETs [1,2,3,6]

The MOSFET is distinguished from other transistors because first, its current transport is conducted primarily by majority carriers. Second, the control current is isolated from the main flow of current; and last, the MOSFET is a voltage controlled device as opposed to a current controlled Bipolar Junction Transistor (BJT) or thyristor.

The MOSFET is a four terminal device. The Gate controls the switching action of the transistor. The Source and Drain are the entrance and exit points for the majority current flow and the substrate acts to balance leakage effects.

The fabrication of a MOSFET can take on many forms and each manufacturer will have its own form. Although each process is uniquely different, the underlying transistor development remains the same. The process involves starting with a lightly doped P-type or N-type substrate, a high resistivity material. A thick layer of silicon-dioxide ($SiO_2$), also known as field oxide, is grown on the substrate surface. A photoresist is then deposited on the field oxide. Portions of the photoresist are developed through a mask that is used to define the areas that will contain transistors. The exposed areas are then etched, thus removing the field oxide in the selected areas. The photoresist is removed and a thin layer of $SiO_2$, known as Gate oxide is grown over the entire structure. Polysilicon is deposited on the Gate oxide, and a mask alignment and an etch process leave a region that will become the Gate of the transistor. The area not covered by the polysilicon is etched away to expose two regions of the substrate. These two regions are ion implanted (a method of injecting charged particles into a substrate to change its electrical properties), forming the Source and the Drain of the MOSFET. A final layer of field oxide is grown on the surface. The final mask and etch processes provide the necessary metalization contact holes. This fabrication process is known as the self aligned Gate transistor.

The MOSFET can be categorized into two categories: the enhancement mode device and the depletion mode device. Both of these categories can have either electrons as the majority carriers (N-channel) or holes as the majority carriers (P-channel). The N-channel MOSFET starts with a P-type substrate, in which two highly doped n+ areas are diffused with a separation by a length L. Similarly, the P-channel uses two highly

doped p+ areas in a N-type substrate. For either case, the geometry is basically the same. The basic structure of the long N-channel MOSFET device is shown in Figure 3.1.1.

The physical dimensions consist of:

d is the Gate oxide thickness

l is the length of the channel between the Source and Drain

x is the depth from semiconductor-oxide interface down into substrate

z is the width of the channel

rj is the Drain diffusion depth

## 3.2 Electrical Characteristics of a Typical MOSFET Device

The operating mechanism behind the MOSFET is the MOS capacitor. It is the influence of the MOS capacitor, Figure 3.2.1, that provides the gateing action for the MOSFET.

The point of interest in the correlation of the MOS capacitor and the MOSFET is the inversion characteristic. Inversion is a characteristic property when the minority carrier concentration at the surface of the metal-SiO2 interface exceeds the bulk majority carrier concentration. In a P-type Si, an inversion may be accomplished by grounding the Si substrate and applying a positive voltage to the metal contact. Figure 3.2.2 shows the band diagram representation of the inverted MOS capacitor. For inversion to occur, the condition $\Phi_{su}=2\Phi_F$ needs to be satisfied. Figure 3.2.3 shows how an inversion layer is

formed on the surface layer of the metal-SiO2 interface. It is the inversion region that is the conducting channel in the MOS transistor. By applying a voltage to the Gate of a MOSFET, a conducting channel is formed between the Drain and the Source.

Unlike the MOS capacitor where the minority carriers must be thermally generated, the Source and Drain contacts provide most of the carriers of the inversion layer in the MOSFET. When a Gate voltage is applied, an inversion layer is formed and the conducting channel is formed. The voltage necessary to cause inversion is called the threshold voltage. When the Gate voltage exceeds the threshold voltage (Vt), the inversion occurs and the conducting channel is formed, thus the transistor turns on. This type of device is referred to as an enhancement type device. A depletion mode device normally has a conducting channel formed by a doped region under the Gate through an extra diffusion process. When a Gate voltage is applied to the MOSFET, the channel is depleted of carriers and the conducting channel is eliminated. Table 3.2.1 gives a summary of the operation of these two types.

As the importance of the inversion layer has been clarified, the characteristics that govern the typical transfer characteristics as seen in Figure 3.2.4 will be covered in more detail. To simplify the explanation, the substrate and the Source are assumed to be grounded and the Gate and the Drain voltages are in reference to ground. All arguments will be given for a N-channel MOSFET, and these arguments will hold for the P-channel by observing the proper doping parameters and reversing voltage polarities.

In the analysis of the MOSFET, we will first start where $V_d$ is equal to $V_t$, where $V_d$ and $V_t$ refer to the Drain voltage and the threshold voltage, respectively. As seen in Figure 3.2.5, the channel under the Gate is formed and a depletion region is formed around both the reverse biased Drain, the Source regions and also along the inverted channel. As the Gate voltage increases, the channel will build up more charge. As the build up of charge increases, the resistance of the channel decreases. By modulating the Gate voltage, the resistance of the channel can be varied.

As the Drain voltage increases slowly, leaving Vg > Vt so inversion persists, the remaining characteristics can be explained. For small increases in the Drain voltage, the current begins to flow through the channel. At this point, the current-voltage (I-V) characteristics are linear, as the channel acts as a simple resistor. The reverse bias current also contributes to the Drain current, but in modern devices this component is small and usually neglected.

Further up the I-V curve, the linear portion slowly begins to disappear. The increase in Drain voltage causes the depletion region around the Drain to increase. The channel starts to close at the Drain as the carriers are being swept away.

The Drain voltage will eventually reach a point that completely closes off the channel. This point is known as "pinch off". For long channel devices ($\Delta L << L$), the slope of the I-V curve essentially becomes zero. For short channel devices, the slope does not reach zero but does start to become constant.

From the point where the Drain voltage is increased beyond "pinch off", the channel length widens from a point to $\Delta L$. The current remains constant with increasing Drain voltage because the voltage drop in excess of the Drain saturation voltage appears across the region represented by $\Delta L$. When $\Delta L \ll L$, the length of the channel essentially remains uncharged. When $\Delta L \approx L$, then the current will not remain constant because there is an equal voltage drop across $\Delta L$ and L portion of the channel, thus causing an increase in the Drain current with further increase in Drain voltage.

## 3.3 Physical Parameters of a MOSFET Device

There are several important physical parameters that are commonly used to describe a MOSFET.

| | |
|---|---|
| $C_o$ | $C_o=\varepsilon_i/d$ insulator capacitance per unit area ($F/cm^2$) |
| $D_n$ | is the electron diffusion constant ($cm^2/sec$) |
| $D_p$ | is the hole diffusion constant ($cm^2/sec$) |
| $\bar{E}$ | is the electric field (V/cm) |
| $E_F$ | is the Fermi level energy (eV) |

| | |
|---|---|
| $E_i$ | is the intrinsic Fermi level energy (eV) |
| $I_D$ | is the Drain current (A) |
| J | is the total current density ($A/cm^2$) |
| $J_n$ | is the electron current density ($A/cm^2$) |
| $J_p$ | is the hole current density ($A/cm^2$) |
| $K_o$ | is the dielectric constant of free space |
| $K_s$ | is the semiconductor dielectric constant |
| L | is the channel length (cm) |
| $N_a$ | is the acceptor concentration (sites\$cm^3$) |
| $N_d$ | is the donor concentration (sites\$cm^3$) |
| n | is the electron carrier concentration (# electrons/$cm^3$) |
| p | is the hole carrier concentration (# holes/$cm^3$) |

| | |
|---|---|
| $Q_G$ | is the Gate charge per unit area (charge/cm$^2$) |
| $Q_n$ | is the total channel charge per unit area (charge/cm$^2$) |
| $Q_{os}$ | is the oxide-semiconductor interface charge per unit area (charge/cm$^2$) |
| q | is the magnitude of electric charge (Coul) |
| $U_F$ | is the semiconductor doping parameter |
| $U_s$ | is the normalized surface potential |
| $V_D$ | is the Drain voltage (V) |
| $V_G$ | is the Gate voltage (V) |
| $V_{ox}$ | is the electronic potential voltage in the oxide (V) |
| W | is the depletion width (cm) |
| $W_T$ | is the depletion width at inversion-depletion transition point (cm) |
| $x_c$ | is the depth of channel (cm) |

$\chi_{ox}$ is the oxide electron affinity which is defined as the energy required to remove an electron to the bottom of the vacuum level (V)

$\chi_s$ is the silicon electron affinity which is defined as the energy required to remove an electron to the bottom of the vacuum level (V)

$\Delta L$ is the decrease in channel length under pinchoff conditions (cm)

$\varepsilon_i$ is the insulator permittivity (farad/cm)

$\varepsilon_s$ is the semiconductor permittivity (farad/cm)

$\phi_F$ is $(KT/q)U_F$

$\phi_m$ is the metal work function which is defined as the energy required to remove an electron from the Fermi level to the vacuum level (eV)

$\phi_s$ is the semiconductor workfunction which is defined as the energy required to remove an electron from the Fermi level to the vacuum level (eV)

$\mu_n$ is the electron mobility ($cm^2$/V-sec)

$\bar{\mu}_n$ is the average electron mobility resulting from lattice scattering and ionized impurity scattering ($cm^2$/V-sec)

$\Psi_b$ $\Psi_b=(E_i-E_F)/q$ potential difference between the Fermi level and the intrinsic Fermi level

These parameters will be used in the following MOSFET analysis.

## 3.4 Analysis of a MOSFET Device [1,2]

An accurate description of MOSFET operation requires an understanding of carrier mobility, MOS inversion characteristics, and semiconductor bulk charge theory. Through the analysis of these three areas, mathematical relations will be obtained to describe the I-V transistor characteristics.

The current that passes through a MOSFET is of direct consequence of the carrier mobility. The bulk mobilities are well documented for various semiconductor materials, doping, and temperatures but for the MOSFET an effective mobility must be obtained because the carrier motion occurs in the inversion layer. The inversion layer will cause carriers to accelerate toward the surface and the result will cause carrier interaction with the semiconductor-oxide interface. Also, the electric field produced by the Gate voltage will accelerate the carriers toward the Si-$SiO_2$ interface. The depth into the semiconductor will be defined by x, the length along the channel, starting at the Source is y and $x_c(y)$ is the channel depth. The effective mobility then is given by

$$\bar{\mu}_n = \frac{\int_0^{x(y)} \mu_n(x, y) n(x, y) dx}{\int_0^{x(y)} n(x, y) dx} \tag{3.4.1}$$

The charge along the channel is of the form,

$$Q_n(y) = -q \int_0^{x_c(y)} n(x, y) dx \tag{3.4.2}$$

therefore, combining Eq. 3.4.1 and 3.4.2 we obtain,

$$\bar{\mu}_n = -\frac{q}{Q_n(y)} \int_0^{x_c(y)} \mu_n(x, y) n(x, y) dx \tag{3.4.3}$$

Equation 3.4.3 is the effective carrier mobility in the MOSFET inversion layer. For small Drain voltages, the mobility in the inversion layer will be almost constant for the length of the channel. It is necessary to assume that the mobility is constant even for larger Drain voltages in order to continue towards a closed form analysis.

An accurate analysis of a MOSFET is through bulk charge theory. The bulk charge analysis accounts for changes in the depletion width along the channel caused by changes in total electric charge and changes in depletion layer charge. The IV characteristics for transistor operation in the linear region, $V_G > V_T$ and $0 \leq V_D \leq V_{Dsat}$, will be derived first . The general formula for electron current density is given by,

$$J_n = q\mu_n n\bar{E} + qD_n \nabla n \tag{3.4.4}$$

The first term refers to the drift component due to an applied electric field and the second term refers to the diffusion component caused by carrier migration from highly concentrated areas to lower concentrated areas. The diffusion component becomes negligible because $n \approx N_D$. Also, current is assumed to flow only parallel to the channel . The current along the channel length is given by,

$$J_n = J_{ny} = q\mu_n n\bar{E}_y = -q\mu_n n\frac{dv}{dy} \tag{3.4.5}$$

Since the channel is narrow, the voltage can be assumed independent of the channel depth. Then a cross sectional area of the channel reveals the Drain current to be found as follows:

$$I_D = -\iint J_{ny}dxdz = -z\int_0^{x_c(y)} J_{ny}dx \tag{3.4.6}$$

$$I_D = \left(-z\frac{dv}{dy}\right)\left(-q\int_0^{x_c(y)} \mu_n(x, y)n(x, y)dx\right) \tag{3.4.7}$$

$$I_D = \left(-z\frac{dv}{dy}\right)(\bar{\mu}_n Q_n) \tag{3.4.8}$$

$$I_D = -z\bar{\mu}_n Q_n\frac{dV}{dy} \tag{3.4.9}$$

$$\int_0^L I_D dy = I_D L = -z\bar{\mu}_n\int_0^{V_D} Q_n dV \tag{3.4.10}$$

$$\boxed{I_D = -\frac{z\bar{\mu}_n}{L}\int_0^{V_D} Q_n dV} \qquad (3.4.11)$$

The above equation assumes that $\bar{\mu}_n$ and $I_D$ are independent along the length of the channel.

The change in Drain current due to changes in the depletion width of the channel can be explained by looking at the charge theory below.

$$Q_G(y)|_{V_G \geq V_T} - Q_G|_{V_G = V_T} = -Q_n(y) + qN_a w(y) - qN_a w_T \qquad (3.4.12)$$

$$Q_G(y)|_{V_G \geq V_T} - Q_G|_{V_G = V_T} \approx C_0\left(V_G - V - \frac{KT}{q}2U_F\right) - C_0\left(V_T - \frac{KT}{q}2U_F\right) \qquad (3.4.13)$$

$$Q_G(y) = -C_0(V_G - V_T - V) + qN_a w_T\left[\frac{w(y)}{w_T} - 1\right] \qquad (3.4.14)$$

An expression is now needed for the depletion width W(y). It must be assumed that the inversion layer resides in a narrow region right on the semiconductor-oxide interface. The depletion width of the channel will increase substantially upon an increase in bias, but once inversion occurs, $U_S=2U_F$, the increase in the depletion width increase is negligible. Once the inversion layer is formed, it provides a shield to the interior of the semiconductor from further charge placed on the Gate. Before the onset of inversion, the width of the depletion region may be determined using normal depletion approximations. At the onset of inversion, the carrier build up approximates a delta distribution; therefore,

w,r,E,and V remain constant for any further charge applied to the Gate. If an expression can be found for the depletion region and then the restriction caused by the onset of inversion is applied, $U_S=2U_F$, the constant channel width can be derived.

For the depletion region n«$N_a$ and p«$N_d$; therefore, for $0\leq x\leq w$ the charge density is of the form,

$$\rho = q(N_d - N_a) \tag{3.4.15}$$

also

$$\frac{d\bar{E}}{dx} = \frac{-d^2V}{dx^2} = \frac{q(N_d - N_a)}{K_s\varepsilon_o} \tag{3.4.16}$$

Through an integration process (the electric field and voltage are zero at x=w)

$$\bar{E}(x) = \frac{q(N_a - N_d)}{K_s\varepsilon_o}(w - x) \tag{3.4.17}$$

$$V(x) = \frac{q(N_a - N_d)}{K_s\varepsilon_o}(w - x)^2 \tag{3.4.18}$$

Using the boundary condition $V=\left(\frac{KT}{q}\right)U_s;\ \ at\ \ x=0$ the simplified expression is obtained.

$$\frac{KT}{q}U_s = \frac{q(N_a - N_d)}{2K_s\varepsilon_o}w^2 \tag{3.4.20}$$

$$w=\left[\frac{2K_s\varepsilon_o}{q(N_a - N_d)}\frac{KT}{q}U_s\right]^{\frac{1}{2}} \tag{3.4.21}$$

Or rewritten as a function of the channel length,

$$w(y) = \left[ \frac{2K_s\varepsilon_o}{q(N_a - N_d)} \frac{KT}{q} 2U_F + V \right]^{\frac{1}{2}} \tag{3.4.22}$$

Finally, substituting the inversion restrictions, a transition depletion width is obtained.

$$w_T = \left[ \frac{2K_s\varepsilon_o}{q(N_a - N_d)} \frac{KT}{q} 2U_F \right]^{\frac{1}{2}} \tag{3.4.23}$$

It is now possible to simplify the equation 3.4.14. By defining two terms, $V_w = \frac{qN_a w_T}{C_o}$ and $\phi_F \equiv \frac{KT}{q} U_F$, and using equations 3.4.22 and 3.4.23, the simplification becomes,

$$Q_n(y) = -C_o \left[ V_G - V_T - V - V_w \left( \sqrt{1 + \frac{V}{2\phi_F}} - 1 \right) \right] \tag{3.4.24}$$

Combining Equations 3.4.24 and 3.4.11 and integrating produce the linear region Drain current ($0 \le V_D \le V_{Dsat}$ and $V_T \le V_G$).

$$\boxed{I_D = \frac{z\bar{\mu}_n C_o}{L} \left[ (V_G - V_T)V_D - \frac{V_D^2}{2} - \frac{4}{3} V_w \phi_F \left[ \left( 1 + \frac{V_D}{2\phi_F} \right)^{\frac{3}{2}} - \left( 1 + \frac{3V_D}{4\phi_F} \right) \right] \right]} \tag{3.4.25}$$

Ignoring the depletion width modulation, the Drain current can be approximated by,

$$I_D \approx \frac{z\overline{\mu}_n C_o}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \qquad (3.4.26)$$

From the equation above (3.4.26), the gain factor, b, is given as,

$$\beta = \frac{z\overline{\mu}_n C_o}{L} \qquad (3.4.27)$$

The current in the saturation region can be found by setting $V_D$=$V_{Dsat}$. This current is then considered fairly constant over the saturation range.

$$I_{D_{sat}} \approx \frac{z\overline{\mu}_n C_o}{L}\left[(V_G - V_T)V_{D_{sat}} - \frac{V_{D_{sat}}^2}{2}\right] \qquad (3.4.28)$$

To complete the analysis, it is necessary to find a reasonable value for $V_{Dsat}$ and the threshold voltage $V_T$. The saturation voltage is found by realizing that the bulk charge (equation 3.4.24) approaches zero when y=L and V approaches $V_{Dsat}$.

$$V_{D_{sat}} = V_G - V_T - V_w\left[\left[\frac{V_G - V_T}{2\phi_F} + \left(1 + \frac{V_w}{4\phi_F}\right)^2\right]^{\frac{1}{2}} - \left(1 + \frac{V_w}{4\phi_F}\right)\right] \qquad (3.4.29)$$

By neglecting the depletion with modulation, an approximation can be made.

$$V_{D_{sat}} \approx V_G - V_T \qquad (3.4.30)$$

An approximation for the saturation Drain current is achieved by combining equations 3.4.30 and 3.4.26.

$$I_{D_{sat}} \approx \frac{z\overline{\mu}_n C_o}{L}(V_G - V_T)^2 \qquad (3.4.31)$$

The final value needed is the threshold voltage. The prime symbol will represent values for an ideal structure. The Gate voltage appears across the semiconductor as well as the oxide.

$$V'_G = \Delta V_{semi} + \Delta V_{ox} \qquad (3.4.32)$$

For the ideal insulator $\frac{d\overline{E}_{ox}}{dx} = 0$ and $\overline{E}_{ox} = -\frac{dV_{ox}}{dx} = const$ ; therefore, the voltage drop across the oxide can be written as

$$\Delta V_{ox} = \int_{-x_o}^{0} \overline{E}_{ox} dx = x_o \overline{E}_{ox} \qquad (3.4.33)$$

The boundary conditions require that

$$Q_{os} = \left(\varepsilon \overline{E}_{semi} - \varepsilon \overline{E}_{ox}\right)\Big|_{os\ \ interface} = 0 \qquad (3.4.34)$$

So

$$\overline{E}_{ox} = \frac{K_s}{K_o}\overline{E}_s \tag{3.4.35}$$

$$x'_o = \frac{K_s x_o}{K_o} \tag{3.4.36}$$

$$\Delta V_{ox} = \frac{K_{ox} x_o}{K_o}\overline{E}_s = x'_o \overline{E}_s \tag{3.4.37}$$

Combining equations 3.4.37,3.4.32 and the drop across the semiconductor

$$\Delta V_{semi} = \frac{KT}{q} U_s \tag{3.4.38}$$

the ideal Gate voltage relation is obtained.

$$V'_G = \frac{KT}{q} U_s + x'_o \overline{E}_s \tag{3.4.39}$$

From equation 3.4.17 limiting to just the thin delta inversion region

$$\overline{E}_s = \frac{q(N_a - N_d)}{K_s \varepsilon_o} W \tag{3.4.40}$$

We know that when $U_s = 2U_F$ then $V'_G = V'_T$. Substituting equation 3.4.40 and 3.4.21 into 3.4.39, the ideal threshold voltage is obtained.

$$V'_T = \frac{KT}{q} 2U_F + \frac{q(N_a - N_D)}{K_s \varepsilon_o} x'_o \left[ \frac{2K_s \varepsilon_o}{q(N_a - N_D)} \frac{KT}{q} 2U_F \right]^{\frac{1}{2}} \tag{3.4.41}$$

$$V_T' = \begin{cases} 2\phi_F + \frac{1}{C_o}\sqrt{4qN_aK_s\varepsilon_o\phi_F} & N-channel \\ 2\phi_F - \frac{1}{C_o}\sqrt{4qN_dK_s\varepsilon_o(-\phi_F)} & P-channel \end{cases} \quad (3.4.42)$$

Carrier mobility, MOS inversion characteristics, and semiconductor bulk charge theory were used to obtain $I_D$ and $V_D$ which allow for IV characteristic modeling.

## 3.5 Conclusion

MOSFETs have become an important circuit element in today's integrated electronics. With circuit operating frequencies reaching into the gigahertz, it is important to understand the basic structure and characteristics of each device used. The limiting factors to speed and power can only be explored on a micro device physics level. Chapter 3 has attempted to give insight to the operation and the device physics of the typical linear MOSFET. Special attention was given to the MOS inversion characteristic. Variation of Gate voltage modulates the channel through inversion carrier buildup. I-V characteristics were derived through determination of the Drain current and the Drain voltage. This development and understanding of the basic MOSFET structure will lead into the development of the power MOSFET in the next chapter of this thesis.

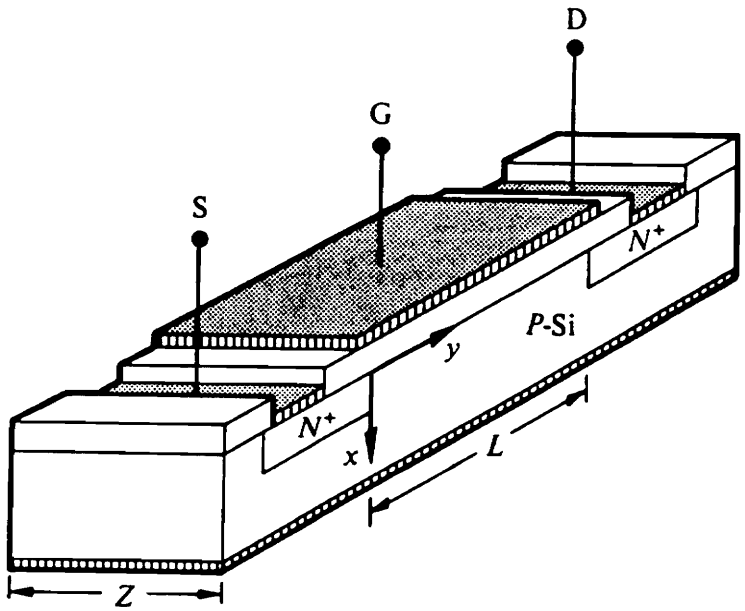



**Figure 3.1.1 MOSFET device structure [2]**

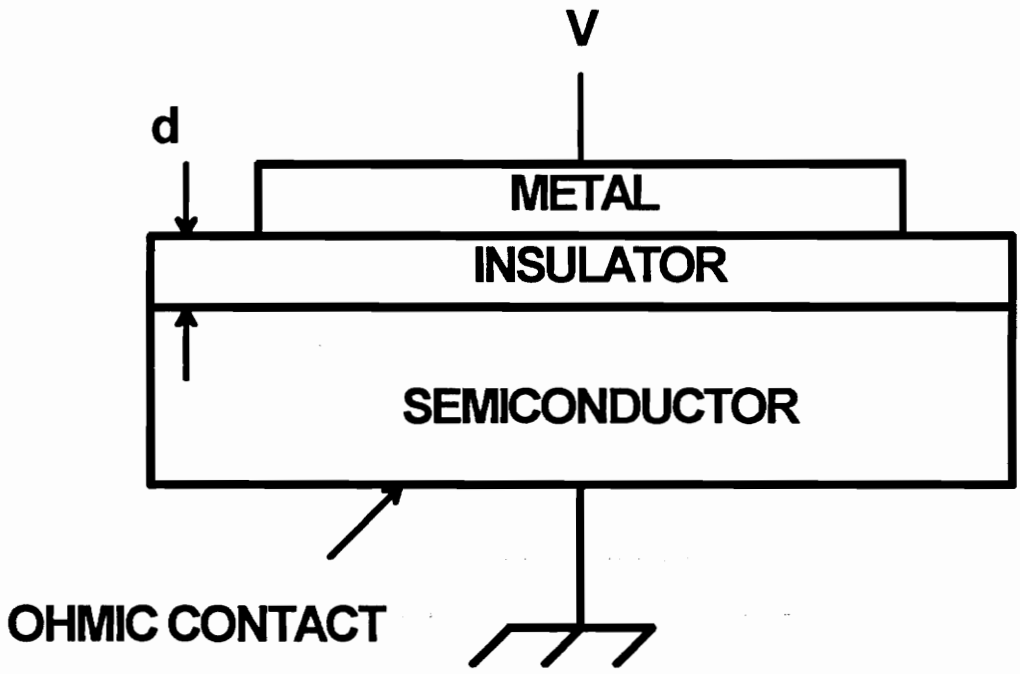



**Figure 3.2.1 Two-Dimensional MOS device structure**

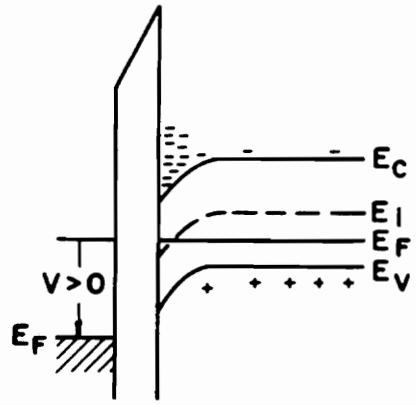



**Figure 3.2.2 MOS band diagram [2]**

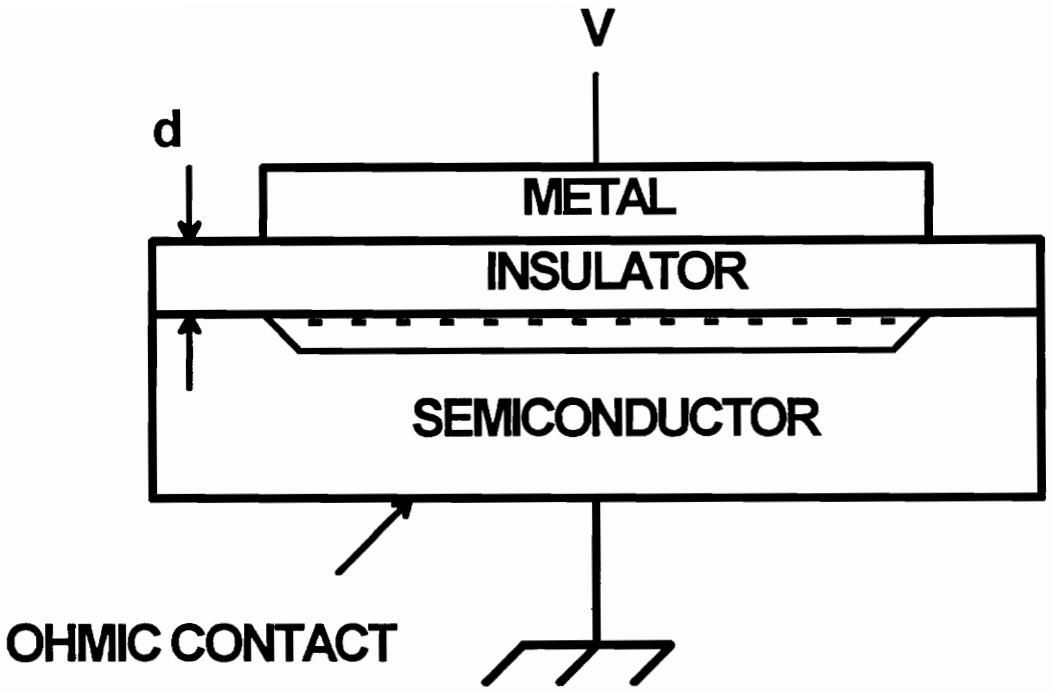
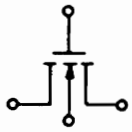
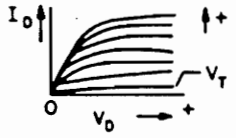
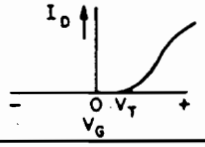
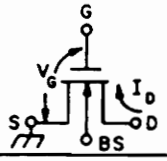
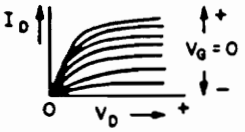
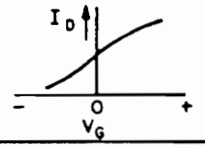
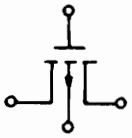
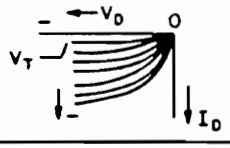
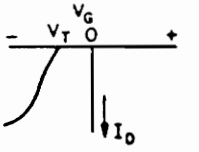
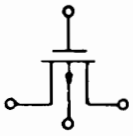
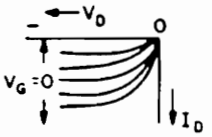
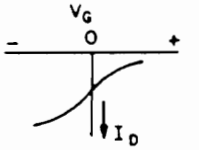



**Figure 3.2.3 MOS capacitor with inversion layer**

**Table 3.2.1 MOSFET modes and characteristics [1]**

| TYPE | ELECTRICAL SYMBOL | OUTPUT CHARACTERISTIC | TRANSFER CHARACTERISTIC |
|---|---|---|---|
| N-CHANNEL ENHANCEMENT (NORMALLY OFF) |  |  |  |
| N-CHANNEL DEPLETION (NORMALLY ON) |  |  |  |
| P-CHANNEL ENHANCEMENT (NORMALLY OFF) |  |  |  |
| P-CHANNEL DEPLETION (NORMALLY ON) |  |  |  |

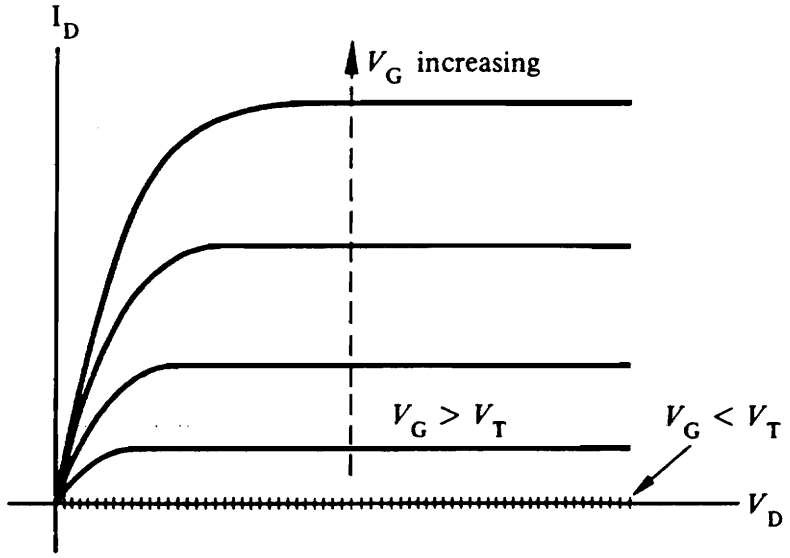



**Figure 3.2.4 MOSFET I-V curve [2]**

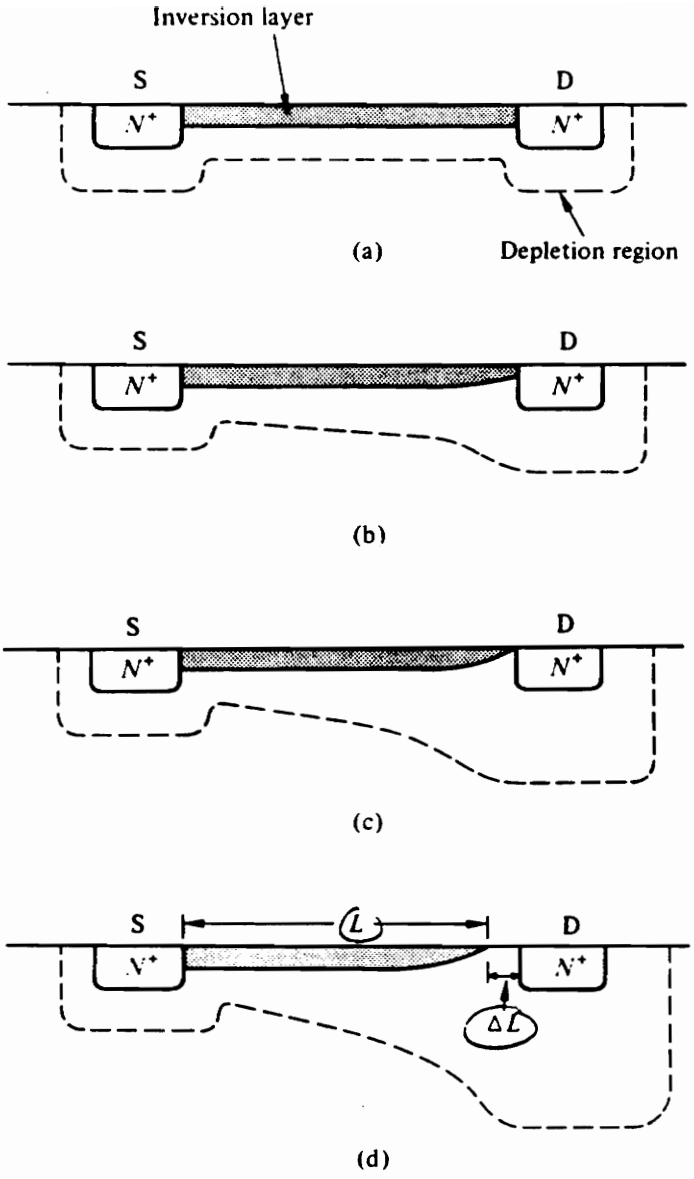



**Figure 3.2.5 Channel Characteristics [2]**

# Chapter IV. The Basic Theory of High Frequency Power MOSFETs

## 4.0 Introduction

Power MOSFETs have become an integral part of high frequency power electronics. Formerly, power and frequency ranges reserved primarily for Bipolar Junction Transistors (BJT) and vacuum tubes have been replaced by power MOSFETs because of improved device parameters and falling production costs due to mass production. The power MOSFET device has distinct advantages over the corresponding BJT device. In contrast to the BJT, the MOSFET is a voltage controlled device, it can withstand inductive loads, current can be passed in both directions, and it requires less drive and stability circuitry.

This chapter will investigate the intricacies of the High Frequency Power MOSFET. Several different MOSFET structures will be discussed: DMOS, VMOS, HEXFET, TMOS. Important design parameters will be covered, such as, On-resistance, frequency limit, and breakdown voltage. Finally, a summary of the power MOSFET device modeling will be discussed.

## 4.1 Power MOSFET Overview

The power MOSFET is a direct descendant from the low power MOSFET. The operation, the limiting power and the limiting frequency are almost exactly the same. For

the power device, channel length and input capacitance are crucial to the power handling capabilities of the device. With this in mind, the low power MOSFET was transformed to conform to the low On-resistance and small Gate capacitance critical for power and speed.

The process that was developed to fabricate a short channel device is double diffusion. This process uses two diffused regions, one on top of the other, to form the channel region. Figure 4.1.1 shows the double diffused structure for the MOSFET device. The P-base and the $n^+$ Source contacts are diffused through the same window formed by the edge of the Gate. The first diffusion, P-base, is allowed to penetrate deeper and wider. The second diffusion, $n^+$ region, is overlaid into the P-base region (Figure 4.1.2). The difference in the two edges will form the length of the channel. A small channel length can be achieved by a careful diffusion process, 2μ to 0.5μ long. Even with different geometries, the double diffusion process is used [9].

In the double diffused device, the On-resistance is defined by the length of the channel as well as the length drift region. The drift region is important since it gives the power MOSFET its high voltage blocking capacity. We can already see one trade off that must be made; the On-resistance at high voltage operation is primarily determined by the drift region that increases by a power of 2.5 of the blocking capacity [9]. Careful consideration must be taken with the trade off between the blocking voltage and the desired On-resistance.

Once a breakdown voltage is determined, the current capability of the device must be developed. Examining Chapter 3, the Drain current is seen to be a factor of channel

width over channel length. At this point, one might ask, "Since the channel length is made as small as possible, why not make the width large?" The problem is that there are two conflicting parameters. As the width of the channel is increased, the capacitance of the Gate also greatly increases. Since the MOSFET is a majority carrier device, the Gate capacitance becomes one of the largest limiting factors in the switching speed of the MOSFET.

In a power device, the ratio of the heat dissipation to the total resistance determines the maximum current capacity [11]. As the breakdown voltage increases, the drift region must increase, therefore increasing the heat dissipation problem. Different power MOSFET geometries help spread the current out within the drift region, helping to dissipate the heat. Also, by the development of the vertical structure, the transistors can be connected in parallel. By making the channel width relatively small in each individual device, connection of MOSFETs in parallel effectively gives wide channel widths while dissipating heat. One must remember that the trade off is width for Gate capacitance; in other words, current capacity for speed [11].

## 4.2 Basic Structures of Power MOSFETs

The same concepts that govern the low power MOSFET hold for the power MOSFET. A voltage is applied to the Gate, thus forming a conduction channel allowing current to flow between the Source and the Drain. The major difference between the low power device and the high power device is that the low power device is fabricated for

lateral current flow while the majority of power MOSFETs use vertical current flow. Although vertical fabrication retards VLSI integration, it does allow the device to be connected in parallel, thus increasing the device power handling capability.

There are several structures of power MOSFETs: V-shaped MOS (VMOS), U-shaped MOS (UMOS), Hexagonal MOSFET (HEXFET), T-shaped Gate MOSFET (TMOS), Double-diffused MOS (DMOS). The development of each of these devices brought along a corresponding solution to electrical enhancements through new fabrication techniques and new geometries.

### *4.2.1 Lateral Diffused MOSFET (DMOS)*

The lateral DMOS allows channel widths to be decreased through a double diffusion process. These smaller channel lengths can be achieved without the usual technological advancements in photolithography. The result reduces the on-channel resistance and lowers the parasitic capacitances [11]. At high voltages, the channel length must be made reasonably long to insure blocking capability in the "off" state. The vertical DMOS allows utilization of the otherwise unused substrate; therefore, large blocking voltages can be achieved in small areas and easy paralleling of the transistors is possible, thus, making the vertical DMOS competitive with the BJT. Both the lateral and vertical DMOS are presented in Figure 4.2.1.

### *4.2.2 VMOS and UMOS*

The VMOS and UMOS use etching to form transistors capable of handling large amounts of current. The device is oriented on the <100> plane and a Gate surface is etched along the intersection <100> and <111> planes, 57.7 degrees to the surface. This unique Gate structure allows current to pass along both sides of the sloped Gate down through the substrate. Figure 4.2.2 shows the VMOS and the UMOS structures, respectively. For further fabrication processes, refer to [1,11,12].

### *4.2.3 HEXFET*

The HEXFET uses a unique geometry to obtain high packing density resulting in large current handling ability. The HEXFET is a part of the DMOS family in that it shares the same type of doping profiles but with different photolithographic geometries. Figure 4.2.3 shows the structure for the HEXFET. For further information, see references [1,12].

## 4.3 Parameters of a Power MOSFET Device

There are several important parameters that are commonly used to describe a Power MOSFET. The parameters are BV, L', $L_G$, M, $\rho$, $\rho_{N+}$, $R_a$, $R_{ch}$, $R_d$, $R_{dv}$, $R_j$, $R_N$, $X_a$, and $\alpha$, where

| | |
|---|---|
| BV | is the breakdown voltage |
| L' | is the effective length of the epitaxial resistor |
| $L_G$ | is the length of Gate electrode between adjacent cells |
| M | is the 1/2 of the diffusion window width |
| $\rho$ | is the drift region resistivity |
| $\rho_{N+}$ | is the sheet resistance of the N+ diffusion |
| $R_a$ | is the accumulation layer resistance |
| $R_{ch}$ | is the resistance of the conducting channel |
| $R_d$ | is the drift region-resistance |
| $R_{dv}$ | is the drift region at the point of the VMOS structure |
| $R_j$ | is the drift region-resistance between P-base regions |
| $R_N$ | is the resistance of the N+ region |

$X_a$ is the JFET region depth

$\alpha$ is the angle factor

## 4.4 Power MOSFET On-resistance

The On-resistance is the total resistance from the Source to the Drain when the transistor is in the conducting ("On") state. The On-resistance is important because it is what limits the amount of current the device can handle. This resistance is determined by the channel resistance, the drift region-resistance, the spreading effects, and the device geometry. Figure 4.4.1 shows the multitude of elemental resistances that are found in a simple power MOSFET. Drain and Source diffusion ($R_{N+}$), channel ($R_{ch}$), accumulation layer ($R_a$ & $R_j$), and substrate ($R_s$) resistances all contribute to the total On-resistance of a power MOSFET [12]. Depending on the geometry, some of these resistances may become negligible.

It is true for power MOSFETs that, bulk resistance is the dominating factor of the On-resistance for high voltage transistors (above 50V). It can also be shown that at high voltage operation, the On-resistance is approximately the same for the geometries LDMOS, DMOS and VMOS [36].

### DMOS

The physical representation of the DMOS and the important dimensional representations are shown in Figure 4.4.2 The equivalent resistive model, as proposed by

Sun and Plumer [36], is shown in Figure 4.4.3a. The substrate resistance ($R_s$) is a function of the wafer used for fabrication. The complete development of the resistances can be found in either [12] or [36]. The results are stated below.

$$R_{N+} = \frac{1}{2}\rho_{N+} L_E (L_G + 2M) \tag{4.4.1}$$

$$R_E \equiv R_{ch} = \frac{1}{2}\frac{L(L_G + 2M)}{\mu_{ns} C_{ox}(V_G - V_T)} \tag{4.4.2}$$

$$R_D \equiv R_A = \frac{3(L_G - 2X_p)(L_G + 2M)}{\mu_{na} C_{ox}(V_G - V_T)} \tag{4.4.3}$$

$$R_{JFET} \equiv R_J = 2\rho_D (L_G + 2M)\left[\frac{1}{\sqrt{1-(2X_p/L_G)^2}}\tan^{-1}(0.414)\sqrt{\frac{(L_G+2X_p)}{(L_G-2Xp)}} - \frac{\pi}{8}\right] \tag{4.4.4}$$

$$R_4 \equiv R_D = \rho_D \frac{(L_G + 2M)}{\tan(\alpha)} \ln\left[1 + 2\frac{h}{a}\tan(\alpha)\right] \tag{4.4.5}$$

$$\alpha = \begin{cases} 28^\circ - \frac{h}{a} & h \geq a \\ 28^\circ + \frac{h}{a} & h < a \end{cases} \tag{4.4.6}$$

Where $\alpha$ is the spreading angle. The final result for the On-resistance of the DMOS is,

$$R_{on} = R_E + R_D + R_{JFET} + R_4 \tag{4.4.7}$$

## LDMOS

The total resistance, as modeled by [36] and shown in Figure 4.4.3a, is more complicated then firsts appears. Some approximations must be made to simplify the result. The contribution of the depletion-mode device is neglected; therefore, the equation deviates for low voltage devices. The development incorporates the resistance r1 into r2 and is given as,

$$R_2 = \frac{\rho(L_G + 2M)}{\pi}\left[\ln\left(\frac{L' - r1}{r1}\right) + \ln\left(\frac{L' - r2}{r2}\right)\right] \qquad (4.4.7)$$

r1 is the effective radius of the current Source at the end of the channel and r2 is the current sink radius at the N+ contact. The total On-resistance for the LDMOS at high voltages is given as,

$$R_{on} = R_E + R_2 \qquad (4.4.8)$$

This model does not account for current crowding at low Gate voltages and it also does not account for a non-uniform channel doping.

## VMOS

The On-resistance for the VMOS, Figure 4.4.4 and Figure 4.4.3c, consists of values already determined for the DMOS and the Lateral MOS, and a new resistance R3 that is the bulk resistance at the point of the V-structure.

$$R_{D1} \equiv R_3 = (0.477)\rho_D(L_G + 2M) \qquad (4.4.9)$$

Therefore, the VMOS On-resistance is,

$$R_{on} = R_E + R_D + R_3 + R_4 \qquad (4.4.10)$$

The three cases given above only start to begin to explain the complex relation for On-resistance. When high frequency operation applies, the length of each section will become of more importance, as will the carrier mobility of each section. Particularly, the long drift region will inhibit rapid carrier transport at very high frequencies. The above formulas give a good indication of DC and low frequency performance.

## 4.5 Frequency Limitations

The limiting factors to high frequency operation are attributed to the rate of change of the Gate capacitance and by the transient time across the drift region. The transient time can be shown to be a function of breakdown voltage and thus, dependent on the length of the drift region and the length of the channel. The Gate capacitance is attributed to several factors: Gate-Source capacitance, Gate-Drain capacitance, and other capacitances. Also, the time required to charge the Gate is heavily dependent on the Gate input resistance. Once these parasitic components are understood, then the frequency of operation limitations will be apparent.

The frequency of operation should not be confused with the switching speed of the device. Switching speeds imply that, the device will normally be in the completely On state or completely off state, thus allowing time for switching transients to decay. The frequency of operation merits imply that the device is continuously switching from the On state to the off state or operating in the region in between.

There are three parasitic capacitances that are associated with the power MOSFET. $C_{iss}$ is the input capacitance measured when the Drain and Source are shorted together. $C_{oss}$ is the output capacitance with the Gate and Source shorted together. Finally, $C_{rss}$ is the Gate to Drain capacitance, also known as the Miller capacitance.

The Miller effect is a result of the input signal of the gain stage being 180 degrees out of phase with the output signal. The feedback causes a reduction in the amplitude of the incoming signal. The result is the input of the MOSFET sees a larger effective capacitance then exists physically. Simply put, the input capacitance as effected by the Miller effect is,

$$C_{in} = C_{GS} + (1 + g_m R_L) C_{GD} \tag{4.5.1}$$

Also, the components that make up the three parasitic capacitances are,

$$C_{iss} = C_{GS} + C_{Gn} + C_{GD} \tag{4.5.2}$$

$$C_{oss} = C_{GD} + C_{DS} \tag{4.5.3}$$

$$C_{rss} = C_{GD} \tag{4.5.4}$$

Figure 4.5.1 shows how these capacitances are arrived at in the power MOSFET. It is very important to reduce the effects of the Miller capacitance $C_{GD}$. If not compensated for during fabrication, the Miller capacitance can ruin high frequency operation.

The measurement of $C_{GS}$, $C_{DS}$, and $C_{GD}$ may not be given in the data sheets, but they can be experimentally determined. The small signal capacitive equivalent circuit is shown in Figure 4.5.2. The following measurement technique is from Sevens [37]. The capacitance measurements are taken by shorting two terminals and then measuring,

$$C_{iss} \equiv C_{GS} + C_{GD} \qquad C_{DS} = short \qquad (4.5.5)$$

$$C_{oss} \equiv C_{DS} + \frac{C_{GS}C_{GD}}{C_{GS} + C_{GD}} \approx C_{DS} + C_{GD} \qquad C_{GS} = short \qquad (4.5.6)$$

$$C_{rss} = C_{GD} \qquad (4.5.7)$$

Measuring the resulting parallel capacitance at 1MHz,

$$C_1 = C_{GS} + C_{GD} \qquad (4.5.8)$$

$$C_2 = C_{GD} + C_{DS} \qquad (4.5.9)$$

$$C_3 = C_{DS} + C_{GS} \qquad (4.5.10)$$

Then $C_{iss}$, $C_{oss}$, and $C_{rss}$ can be determined.

$$C_{iss} = C_1 \tag{4.5.11}$$

$$C_{oss} = C_2 \tag{4.5.12}$$

$$C_{rss} = \frac{C_1 + C_2 - C_3}{2} \tag{4.5.13}$$

These can then be simply manipulated to give the final values.

$$C_{GS} = \frac{C_1 - C_2 + C_3}{2} \tag{4.5.14}$$

$$C_{DS} = \frac{-C_1 + C_2 + C_3}{2} \tag{4.5.15}$$

$$C_{GD} = \frac{C_1 + C_2 - C_3}{2} \tag{4.5.16}$$

For a complete derivation of these results see [37].

The drift region transient time turns out to be,

$$F_T = \frac{6.11X10^{11}}{(1 + \frac{L}{d})(BV)^{\frac{7}{6}}} \tag{4.5.17}$$

Where d is the length of the drift region, L is the channel length, and BV is the breakdown voltage. It is important to make the channel length small, but at the expense of breakdown voltage. It is also evident for high voltage devices that frequency response suffers.

## 4.6 Parasitic Elements, Secondary Breakdown, and dv/dt capability [8,11,12]

There are a few other power MOSFET characteristics that are introduced into some models. Unwanted turn on (dv/dt effects), a parasitic diode, and a parasitic BJT may be included in the device model depending on the application of the device. All these effects are always present, but under certain situations the can be neglected. For instance, the integral diode only needs to be considered if the Drain and Source become reverse biased, as in the fly back current generated in an inductive load due to back EMF. Compensating for the dv/dt effects can prevent accidental device turn on of the transistor.

The parasitic BJT is formed by the $N^+$ Source contact, the P body, and the N drift region. The P base region and the $N^+$ emitter region are shorted together to keep the BJT inactive for all of the power MOSFETs operating conditions. The effect of the body Drain diode remains. If the BJT is not properly shorted, forward biasing of the emitter-base junction can start minority carrier transport. The activation of the parasitic BJT will slow down the switching behavior of the MOSFET, but can also cause secondary breakdown.

The parasitic diode will conduct when the MOSFET if reverse biased. This can be a desirable parasitic effect, especially for inductive loads. To effectively use the diode, it is helpful to know its characteristics. The current capability, recovery speed, and voltage drop are important to know if the parasitic diode is elemental to circuit operation. It is important to realize that when switching a power MOSFET , the diode must have time to recover; otherwise, there will be a low resistive path that effectively shorts the transistor. This phenomenon is known as the dv/dt characteristic [8]. There are circuit solutions to dv/dt effects and they can be implicated if the power MOSFET is going to be operated in manner that requires the use of the body diode [38].

## 4.7 Device Model

There are three commonly used modeling techniques. First , one of the most basic and well used models is a standard component model. This type of model uses simple and often ideal components, such as resistors, capacitors, inductors, and diodes. This circuit oriented model attempts to express device characteristics through a network of components; the result, visually intuitive operation can be seen from the model. The second type of model is the physical equation model. This second model attempts to describe the device through mathematical relations. These equations describe basic operating characteristics of the device, such as input/output resistances and capacitances, transconductance, and operating currents and voltages. Although this type of modeling can be highly accurate, an intuitive sense of device operation may not be immediately

evident. The last common device modeling technique is experimental curve fitting. Measurements from a typical device are accurately measured , then either equations or components are configured so the model output closely matches the measured data. These type of models are good for developing nonlinear and high frequency models where the complexity of mathematical models quickly becomes cumbersome.

One device may have several different models. Each model will be accurate for a limited range of operation. For instance, models differ for high and low frequency operations and they differ for small and large signals. In the case of the Power MOSFET, there is a difference between switching and amplification models. The model that represents a switching transistor has to be accurate for the static characteristics. These characteristics include parameters such as Gate leakage current, DC parameters, breakdown voltage, On-resistance, and zero bias Drain current. In the case of amplification, the disapative dynamic losses must be emphasized. The dynamic characteristics include forward transconductance, capacitance, and frequency limitations.

Combining the elements discussed in the previous sections, a typical Power MOSFET model is shown in Figure 4.7.1. The origin of the elements and parasitics are shown in Figure 4.7.2. Another typical model , this time for the VMOS, is shown in Figure 4.7.3. Again, the origin of these elements is shown in Figure 4.7.4. It should be obvious that these models are derived using ideal components by investigation of physical and doping geometries.

Chapter 5 will investigate the modeling of the power MOSFETs through time domain techniques. The methods and results will be discussed. By using the previous chapters mathematical, physical and operational characteristics in combination with time domain measurements , the nonlinearities in the device model should become more apparent.

## 4.8 Conclusion

Now that technological advances have brought power MOSFET's operating frequencies to near microwave operation, broad band, non linear models are important for circuit simulation. The development of the power MOSFET dynamic and static characteristics developed in this chapter, along with the basics of device modeling techniques, will provide a starting point for the time domain device modeling that will proceed in Chapter 5.

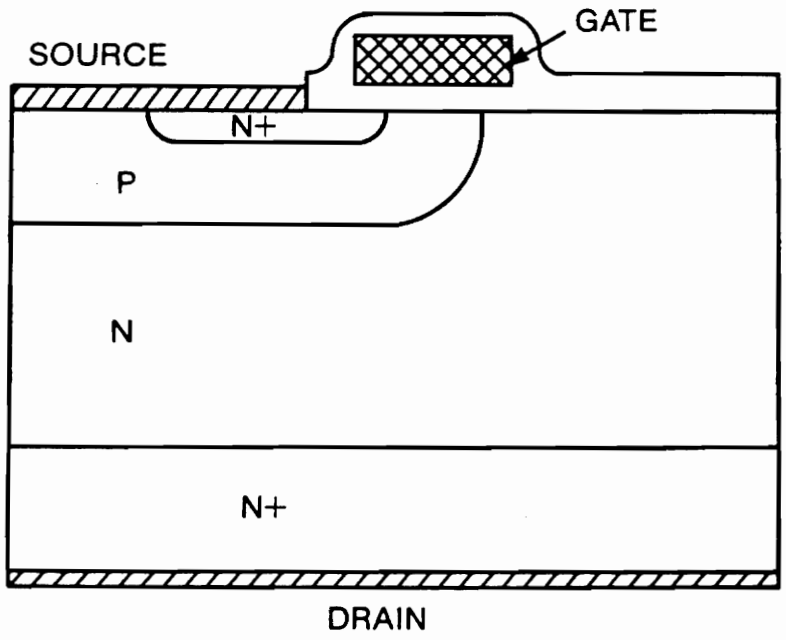



**Figure 4.1.1 Double diffused MOSFET [12]**

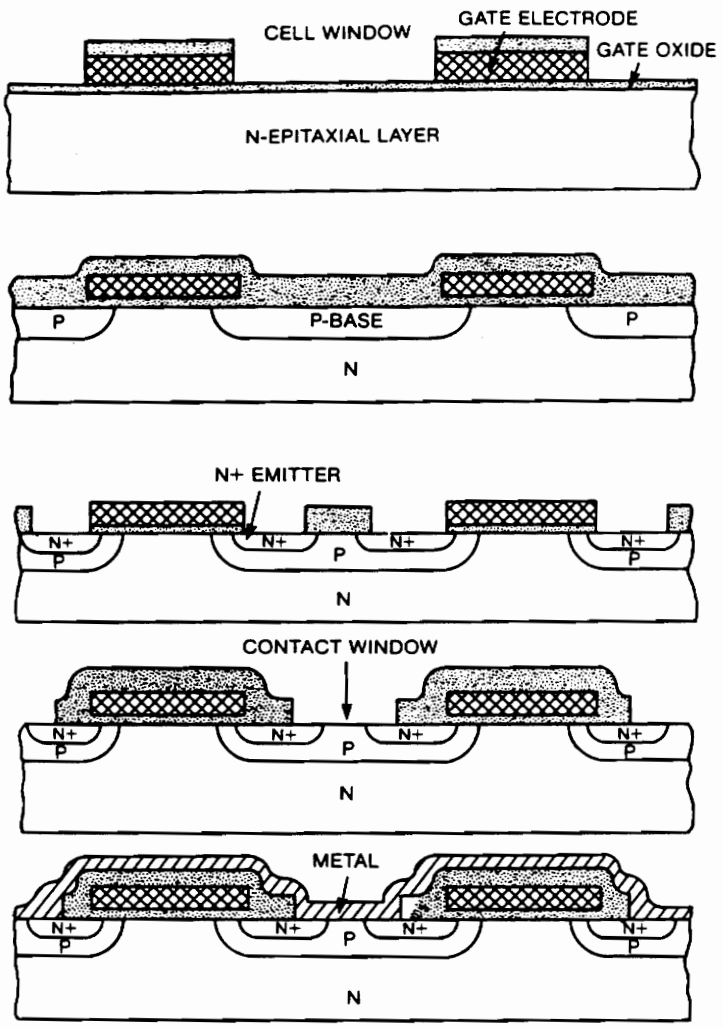



**Figure 4.1.2 Double diffused process**

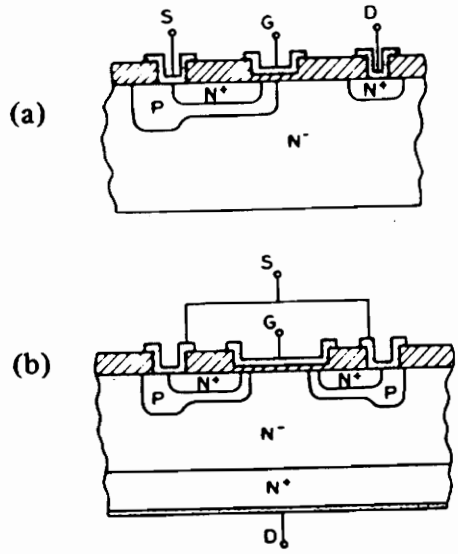



**Figure 4.2.1 Lateral and Vertical DMOS [36]**

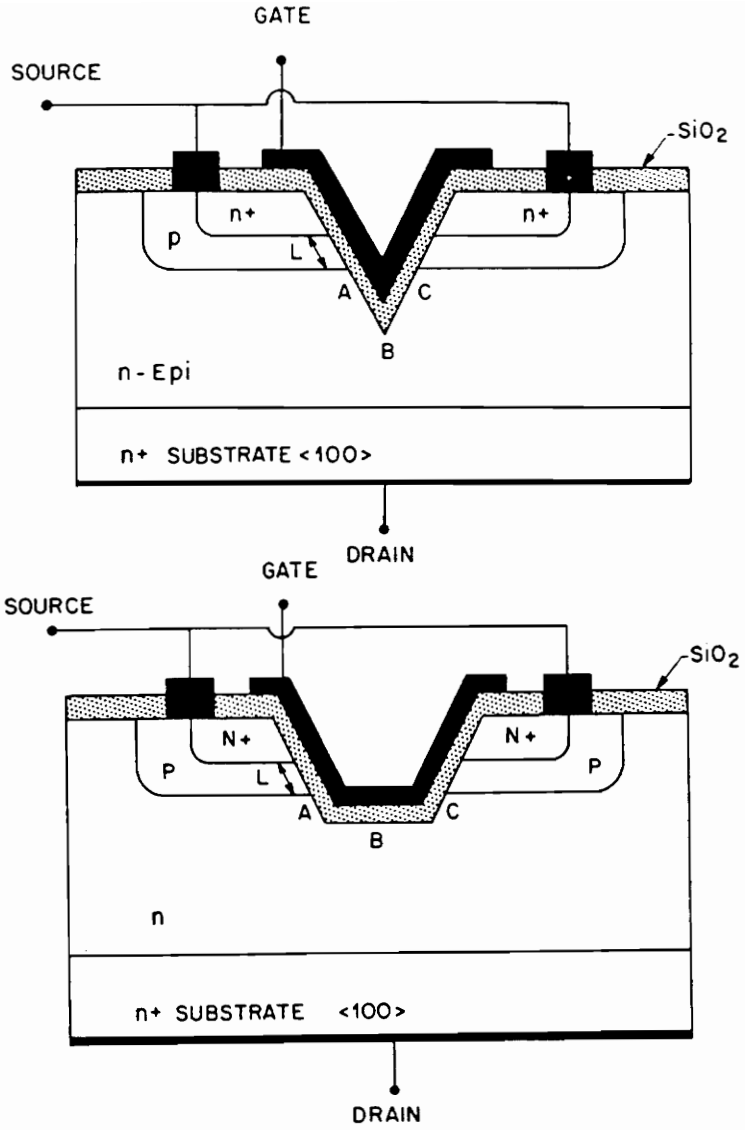



**Figure 4.2.2 VMOS and UMOS structures [1]**

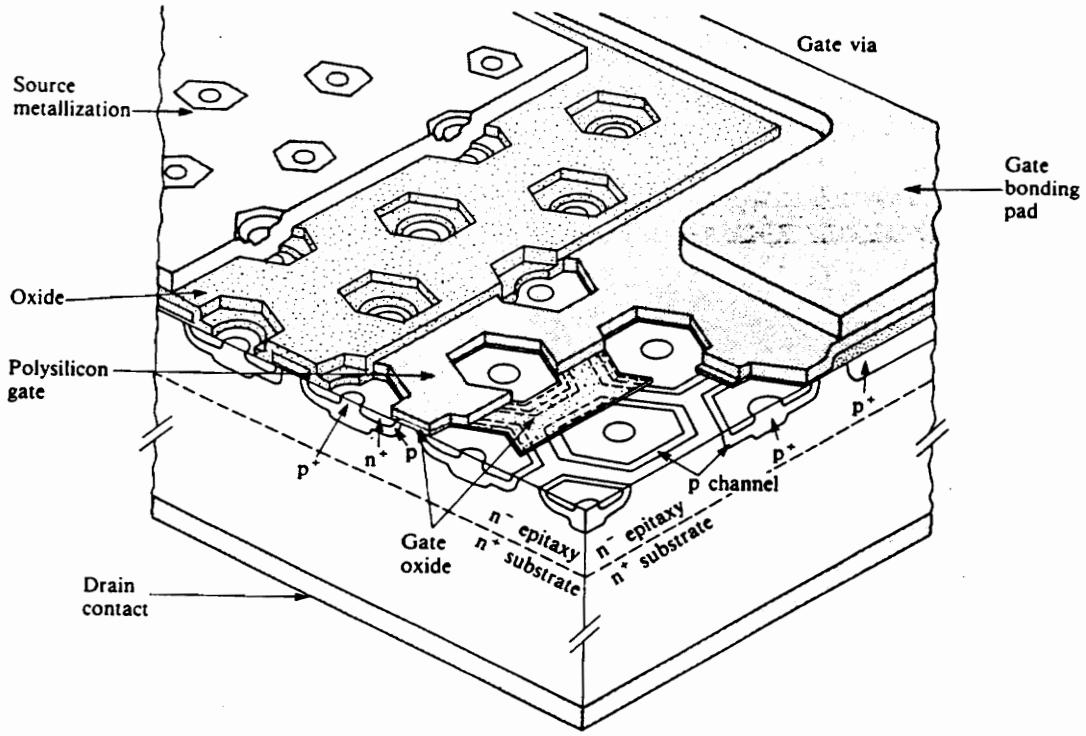



**Figure 4.2.3 HEXFET structure [8]**

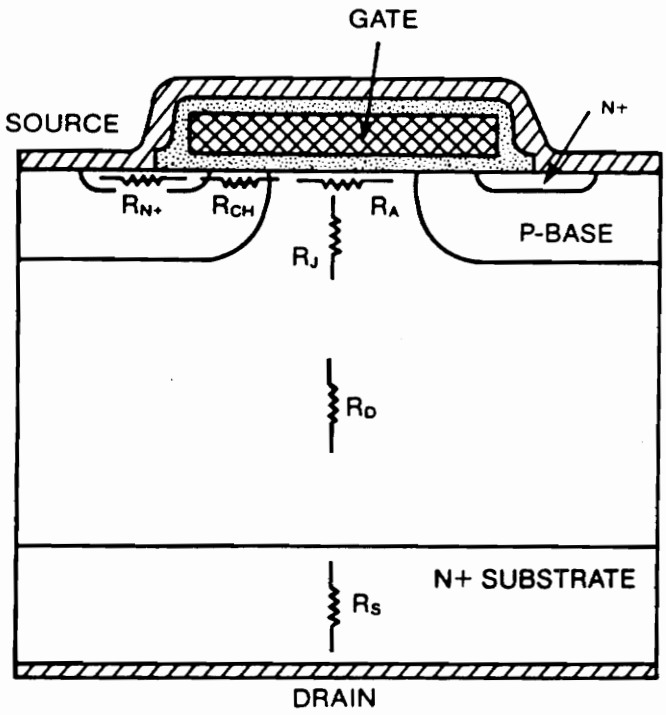



**Figure 4.4.1 Power MOSFET equivalent resistances [12]**

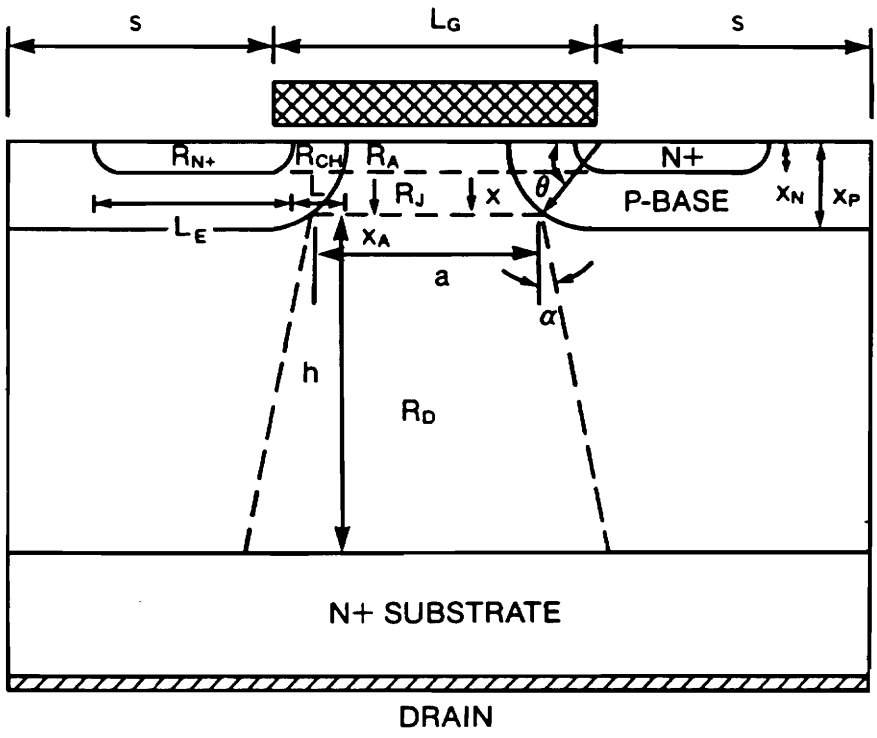



**Figure 4.4.2 DMOS dimensional variables [12]**

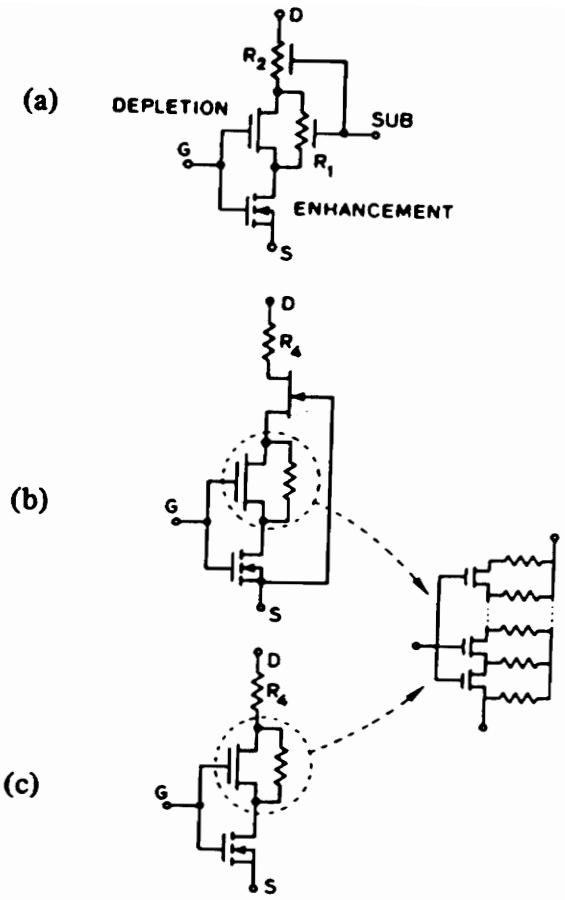



**Figure 4.4.3 Equivalent resistive models [36]**

**(a) LDMOS**
**(b) VDMOS**
**(c) VMOS**

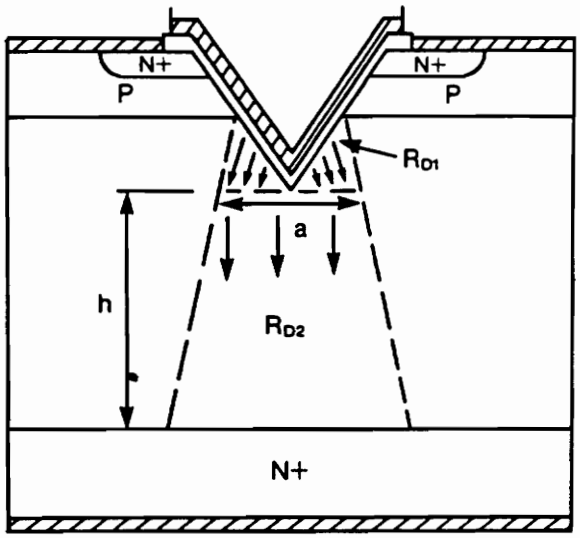



**Figure 4.4.4 VMOS resistance model [12]**

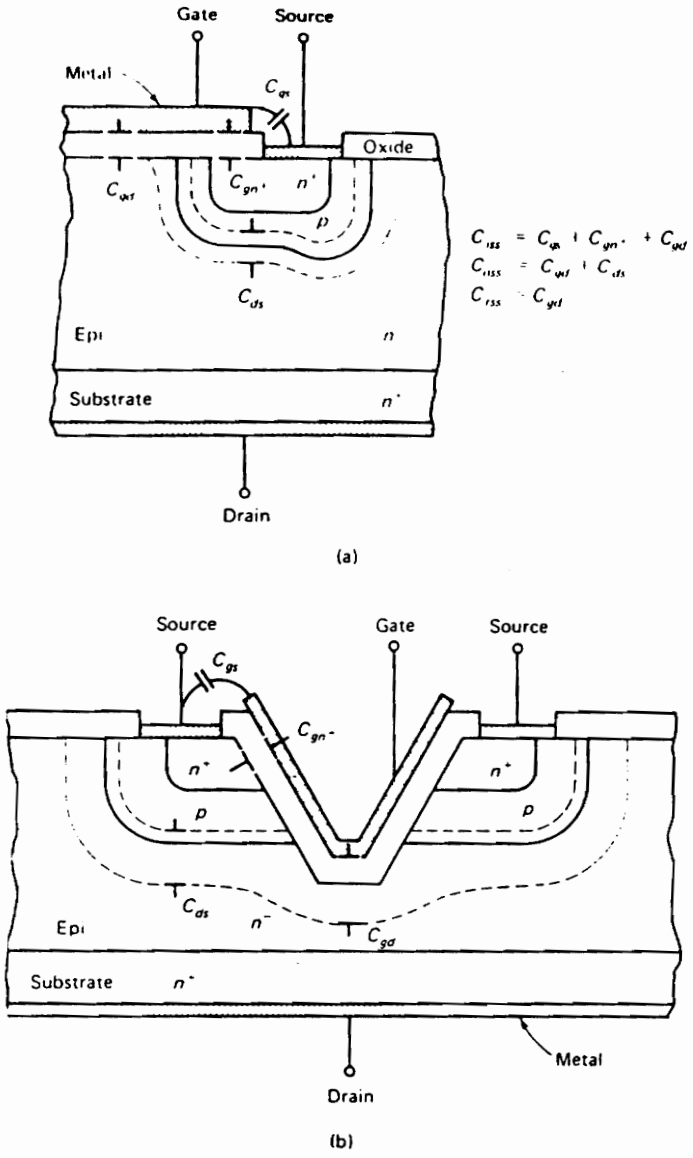



**Figure 4.5.1 Power MOSFET capacitance parameters [11]**

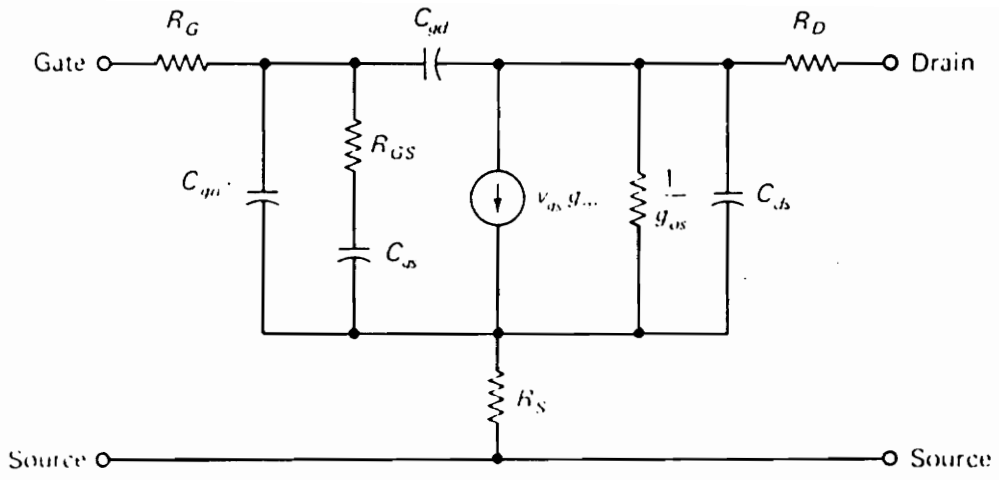



**Figure 4.5.2 Small signal equivalent circuit [11]**

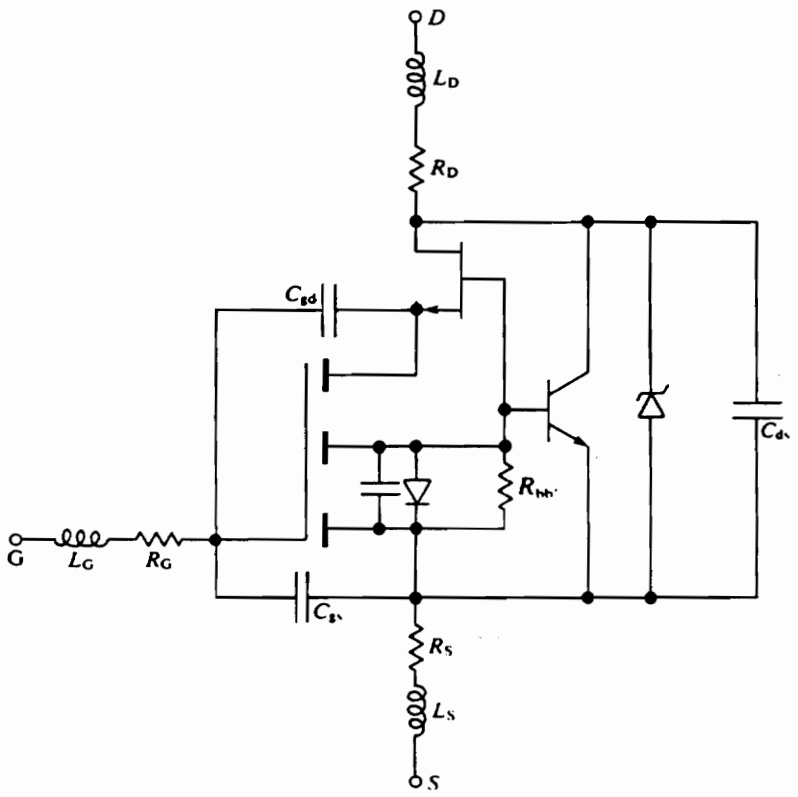



**Figure 4.7.1 Equivalent circuit with parasitics [8]**

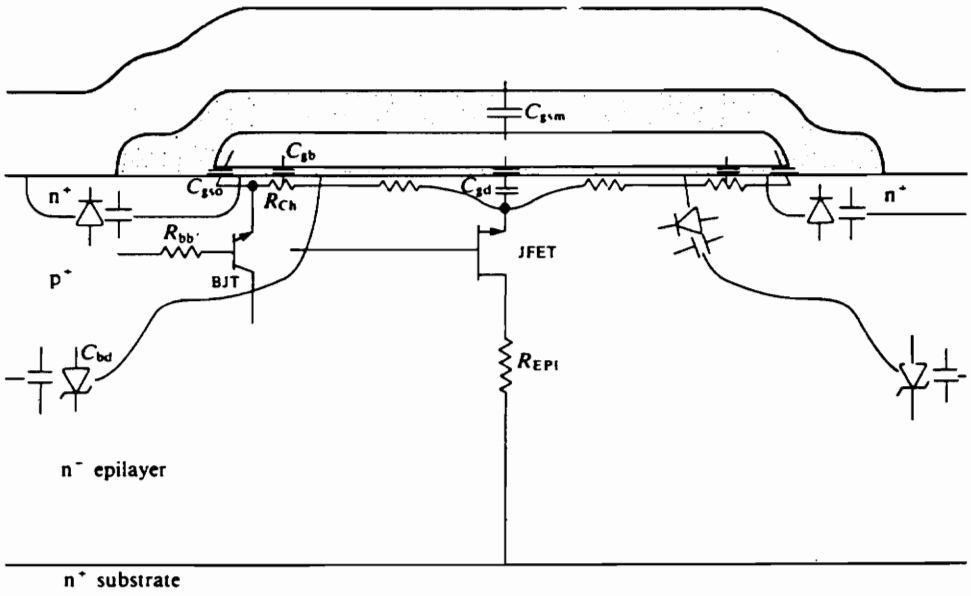



**Figure 4.7.2 Parasitic component origin [8]**

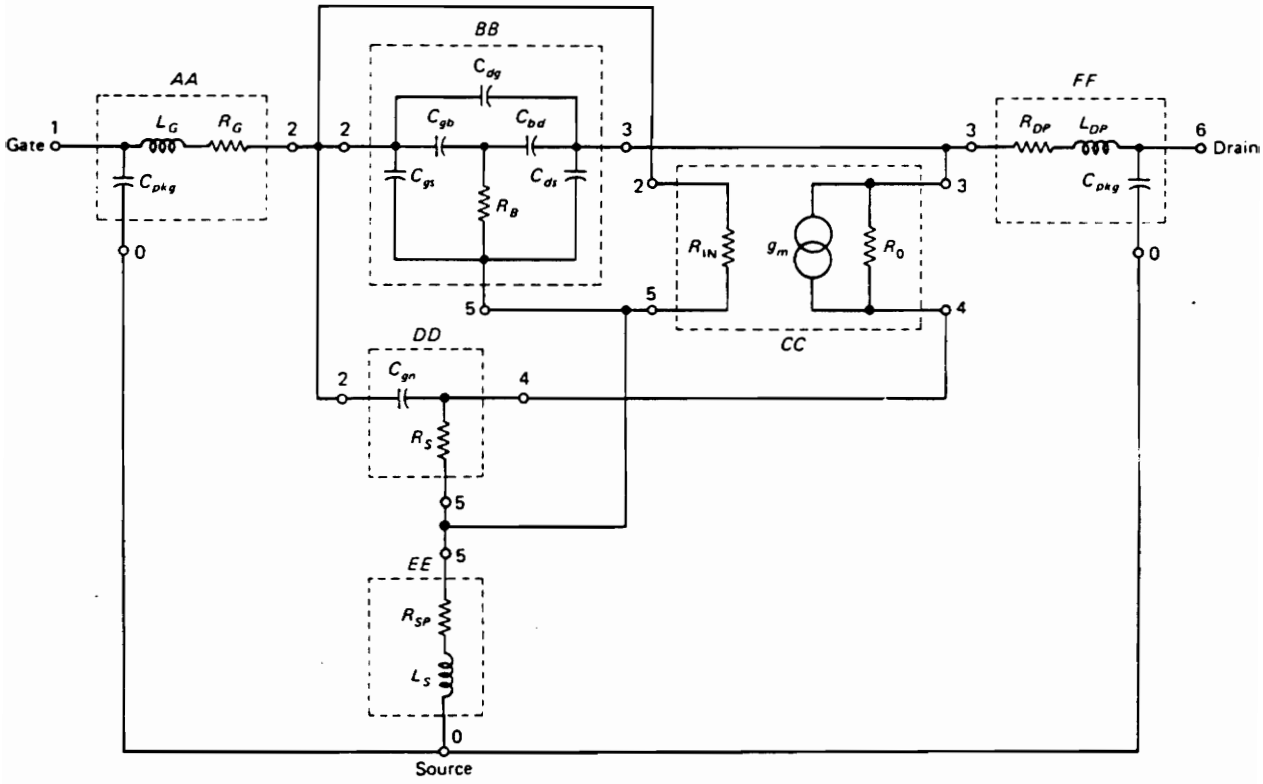



**Figure 4.7.3 VMOS equivalent circuit [8]**

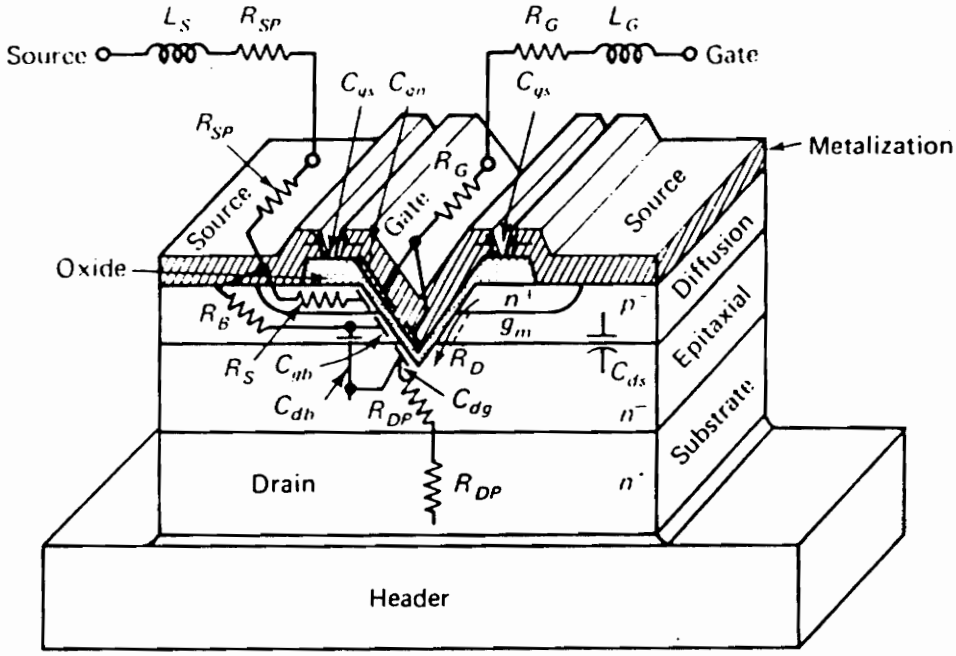



**Figure 4.7.4 Parasitic component origin [8]**

# Chapter V. Time Domain Synthesis Applied to High Frequency Power MOSFETs

## 5.0 Introduction

This chapter will cover the device modeling of a High Frequency Power MOSFET using Time Domain Reflectometry techniques. Experimental results and a device model for the Gate of the MOSFET will be given. The model is obtained using TDR techniques on a packaged MOSFET mounted on a microstrip transmission line configuration. Through the use of the TDR techniques, the effects of the package can be determined and also a device model for the die can also be extracted.

## 5.1 The Time Domain Synthesis Problem

The problem to be solved is to obtain an accurate Gate model for a High Frequency Power Transistor. The device used in these experiments is the Motorola MRF162. This device was chosen for its high frequency ability (400 MHz) and because it is an easily obtainable power MOSFET. The specification sheet is given in Appendix A for convenience.

Previous experiments using TDR methods have used passive devices. Special care has to be used when measuring active devices such as a power MOSFETs. The transistor must be biased so that it does not over heat or exceed its power limits. Also,

special care must be used to isolate the TDR unit from any DC offset imposed by biasing the transistor.

Proper biasing requires the use of a Bias-T. This capacitor-inductor arrangement allows proper biasing of the transistor while blocking DC voltage from entering the TDR unit. The disadvantage the Bias-T imposes is that the blocking capacitor degrades the incident pulse as well as limiting the low frequency range. The next section will give further details on the Bias-T and the limitations.

## 5.2 Experimental Work

First, a special transmission line board had to be developed so that the Gate could be closely matched to the 50Ω coaxial line of the TDR unit. The first step in the development of the test board was to design a microstrip line width as close to the input width of the transistor tabs. This will help to minimize reflections by matching the lines. A substrate developed by Rogers RT/Duroid Microwave Laminates was used because the boards are manufactured for high frequency applications. The board used was the 5880. This provided the closest match of all the available boards. Appendix B shows how the approximate width of the microstrip was developed. Once the approximate width was determined, a pattern of ten different line widths (some larger and some smaller then estimated) was rendered using Autocad. The pattern was plotted at 10:1 onto a piece of Rubylith. This image was photo-reduced to a 1:1 negative. Then a piece of Duroid 5880 was spun with photoresist and exposed using the negative as a mask. After being

developed, the result was ten transmission lines with different widths. Connectors were attached and the impedance measured using TDR techniques. The closest match was then used as a reference and the actual test board was developed with the reference width. The test pattern helps eliminate errors due to plotter inaccuracies, errors in camera settings, errors caused by over exposure and over etching. The times and settings were kept as constant as possible from the test pattern to the test board. The final resultant test board pattern and experimental reflected waveforms are shown in Figures 5.2.1 and 5.2.2, respectively. The microstrip line, on the test board, with the least amount of discontinuity perturbation was used for the input of the Gate (Line 3). The discontinuity caused by the connector appears at 300ps in Figure 5.2.2. For several hundred picoseconds following (300ps to 500ps) the effects caused by this initial discontinuity can be seen. Choosing the transmission line with the smoothest waveform assures that the incident pulse arriving at the transistor is as close too ideal as possible.

The reference waveform was obtained by shorting the end of the transmission line (Fig. 5.2.3). This waveform is multiplied by -2 and shifted to start at zero. The result is a pulse that closely approximates the actual pulse seen by the Gate of the transistor. This reference waveform is used as the step voltage Source in the MTCAP simulations.

The transistor is mounted on the microstrip line in its normal package (CASE 244-04). This is a stud and flange arrangement (see Appendix A). By using the entire package, a complete model can be obtained and the model will contain vital package

characteristics and information. The remainder of the experimental setup is shown in Figure 5.2.4.

The Bias-Ts are Picosecond Labs model #5555. These have a transition duration of 20ps and have an operating range from 100KHz into the Ku band. This will limit the accuracy of the device model to the upper frequencies of its operation. The upper operating range of the transistor is 400MHz; therefore, the model should cover the broad band range from 100MHz to 400MHz. The Power Transistor's high speed operation is heavily dependent on the Gate capacitance. It is the Gate capacitance that limits high frequency operation of the transistor.

To achieve an accurate model, a 1ns time epoch is used with 1000 sampling points. Also, 128 sampling averages are taken which result in a smooth TDR response. The reflections are taken at several bias conditions. The first is obtained for a zero bias Gate and Vds=0,4,8, and 20 volts (Fig. 5.2.5). For the next set of measurements, the Gate is biased at the onset of turn on. This point was experimentally determined to be 2.8 volts. Again, the measurements are repeated for the Drain-Source biasing of Vds=0,4,8,10, and 20 volts (Fig. 5.2.6). Approximate time epochs, as seen in Figures 5.2.5 and Figure 5.2.6, can be attributed to the physical aspects of the package and the Gate. The time epoch between 150ps and 450ps is due to the transistor package. The time epoch between 450ps and 600ps is the Gate response.

## 5.3 Characterization and Modeling

Inspection of the Gate TDR waveforms show that there are two large capacitive discontinuities. The first is centered around 200ps and the second is centered around 500ps. The first caused by the package and the second is caused by the wire bond and the transistor.

The approach to modeling these waveforms with MTCAP is to first model the initial part of the waveform by transmission lines and a capacitor. This simulates the effect of the package. The second step is to model the Gate of the transistor at zero bias condition using a model developed by conventional methods. Then this model is adjusted and simulated using MTCAP.

A simple transistor model (Fig. 5.3.1) is simplified to the equivalent Gate model (Fig. 5.3.2). This model is then preceded by a transmission line and a package model. The data sheet from the Motorola is used to obtain the initial values of the components. The ideal case, at zero bias, is then simulated to see if the measured results are close to what is expected (Fig. 5.3.3). Since the ideal MTCAP model is close to the measured, the modeling process continues by repeating the adjusting and simulating until the two waveforms, simulated and measured, closely match. Last, the initial model is adjusted for each separate bias condition.

The device theory indicates that the input of the Gate will become more capacitive with an increase in the Drain to Source bias. This capacitive increase comes about because of the increase in voltage between the Gate and Drain. On the other hand, the

voltage between the Gate and the Source remains constant (common Source configuration). The object of this modeling is then to raise the capacitance of Cdg and allow the capacitance Cgs to remain relatively constant. This results in one model fitting each curve with just an adjustment in the capacitance Cgd. The chart below shows the acquired values of the model and the calculated values obtained from the specification sheet. The calculations are given in Appendix C.

Calculated values obtained from manufacturers specification sheets

| | Vds=0 | Vds=4 | Vds=8 | Vds=10 | Vds=20 |
|---|---|---|---|---|---|
| Cgd (pF) | 50 | 20 | 11 | 8 | 6 |
| Cgs (pF) | 24 | 20 | 18 | 18 | 19 |

Experimental

| | Vds=0 | Vds=4 | Vds=8 | Vds=10 | Vds=20 |
|---|---|---|---|---|---|
| Cgd (pF) | 21 | 15 | 8 | 4.5 | 3 |
| Cgs (pF) | 6 | 6 | 6 | 6 | 6 |

The matched curves for each bias condition are shown in Figures 5.3.4 through 5.3.8 and the final circuit model is shown in Figure 5.3.9. There is good agreement between the measured and the simulated model for the bias conditions.

## 5.4 Discussions of Experimental Results

The TDR model can be considered accurate in its own right, but some explanation is in order to relate the model values to those that are expected from calculations. The calculated values, shown in the table above, are based on measurements taken at zero Gate bias and zero Drain bias. The modulation frequency used to determine the corresponding capacitance is 1 MHz. These values, derived from the data sheet measurements, provide an approximation of relative capacitance and thus operational frequency. The calculated capacitances represent the total effect of all contributing capacitances as seen at the package inputs. The experimental values are slightly lower because the capacitance listed in the table is only the transistor contribution and not any of the capacitance caused by the package. For example, the calculated values include the lead capacitance of the package as well as the actual device Gate input. Once again, the benefit of TDR techniques becomes obvious, these values can be seen in the reflection waveforms as separate discontinuities (dips in the reflected waveform).

A review of the TDR model and experimental values (Fig. 5.5.9) reveals the package capacitance and the device capacitance. The incoming transmission lines and bridging capacitance C1 are the effect of the package. If these values are added to the capacitance of the terminating model, the experimental values will increase the effective value of the Gate capacitance as seen by the driving circuitry. The model serves as an accurate representation and the table of values serves as a reference to the trend of

decreasing capacitances. As seen in the values above, when the Drain bias increases, the input capacitance to the Gate decreases.

It may seem peculiar that there is such a large input resistance in the Gate model. This value (18Ω) is not so atypical for a power transistor. Gate resistance can be as high as $20\Omega/mm^2$ of die area. Also, a quick estimate of operating frequency is $f=1/(2\pi RC)$. This relies on the fact that the Gate charge limits the operating frequency. In the MRF162 at 400 MHz, we would find the Gate resistance to be approximately 16Ω. As expected, this value falls close to the experimental value.

## 5.5 Conclusion

The Time Domain Technique is used to model the Gate of the MRF162 High Frequency Power Transistor. The waveforms measured from the TDR experiment were matched to obtain a wideband model. The model provides physical insight to the input of the transistor Gate. Both the effects of the package as well as the transistor can be seen in the TDR model and by inspection of the TDR waveforms. This model is good over the broad range from 100MHz to 400Mhz. This technique provides a model for a wide range in contrast to scattering parameter measurements that must be calculated at a particular frequency operation.

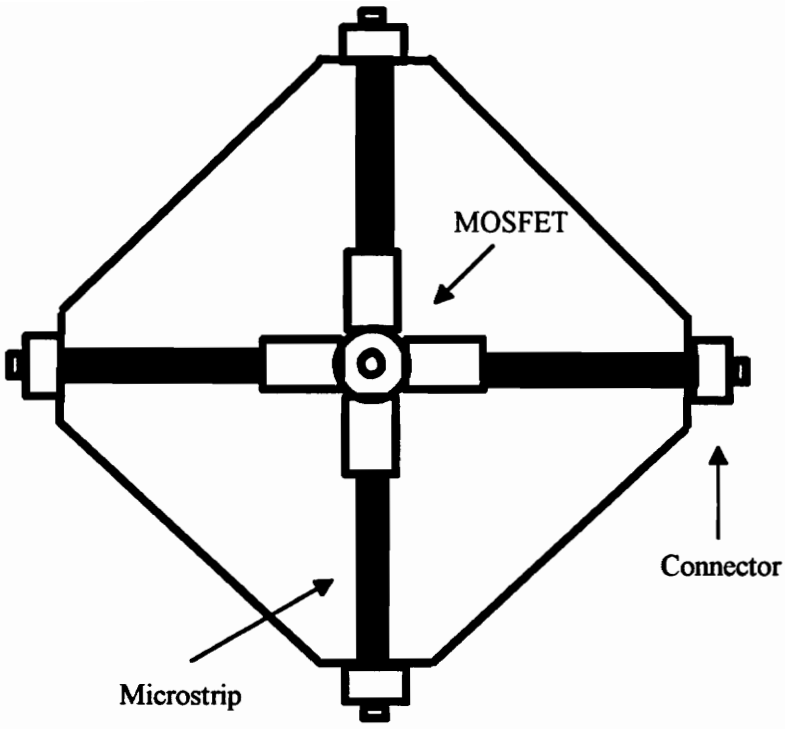



**Figure 5.2.1 Test Board Layout**

# Transmission Line TDR Characteristics

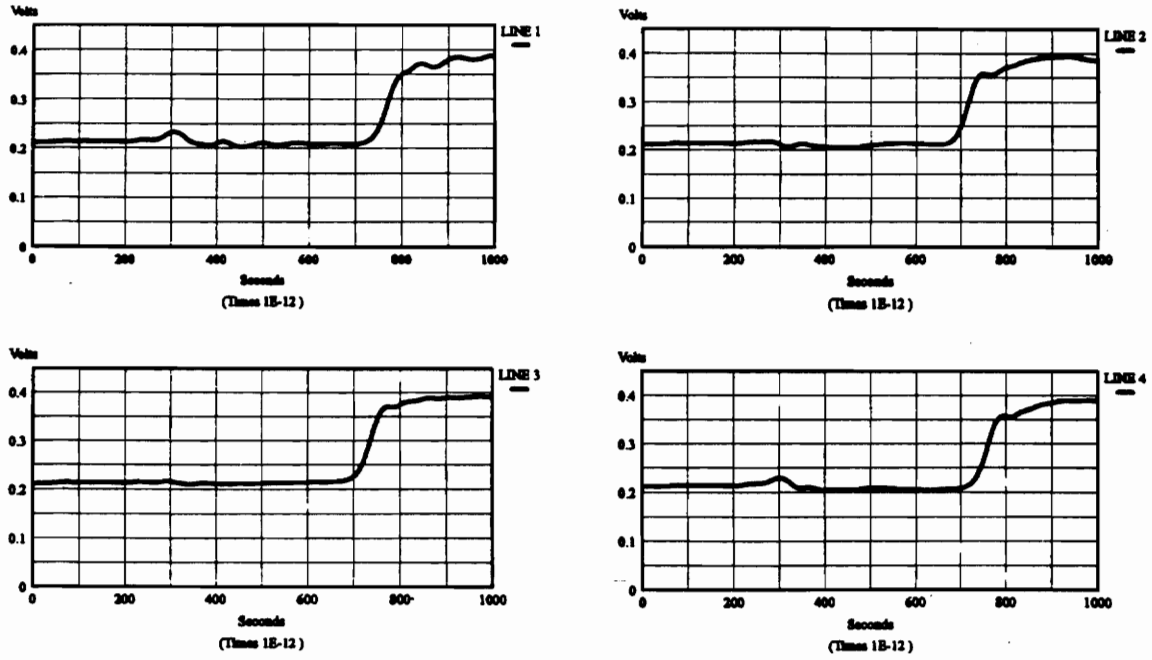



Figure 5.2.2 Test Board TDR Response

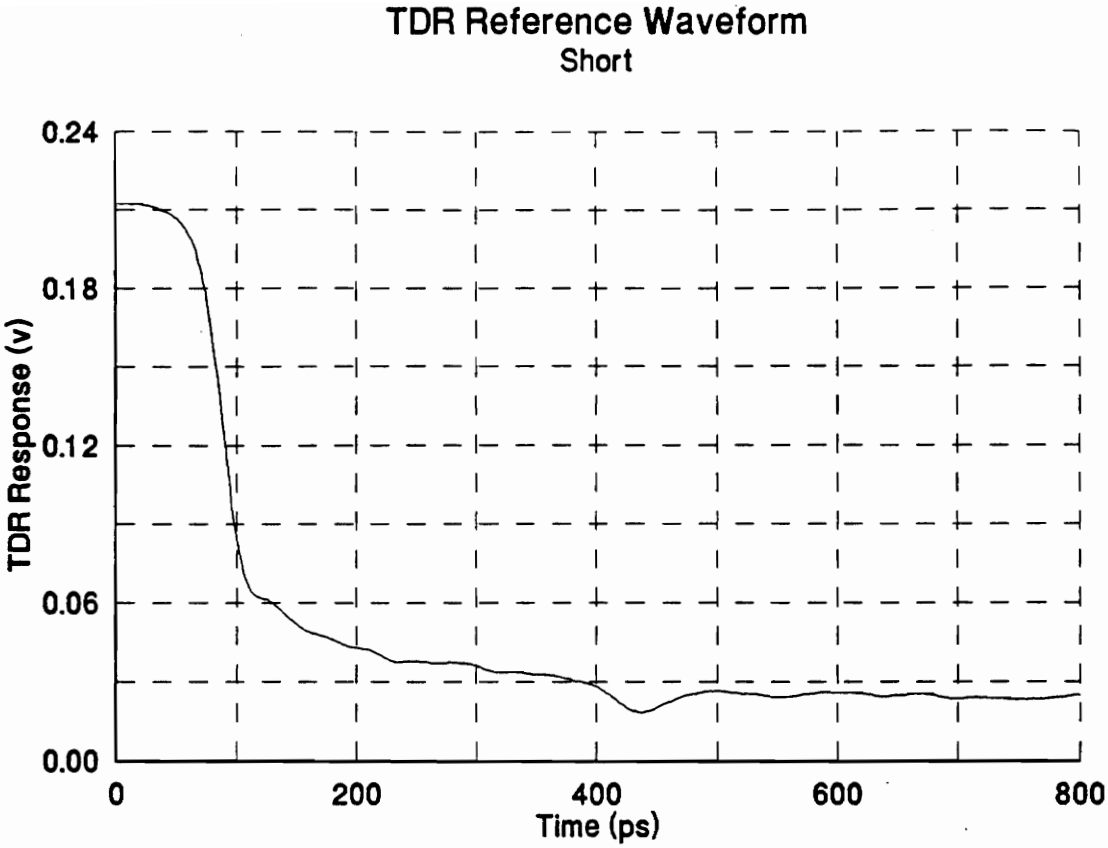



**Figure 5.2.3 TDR Reference Waveform**

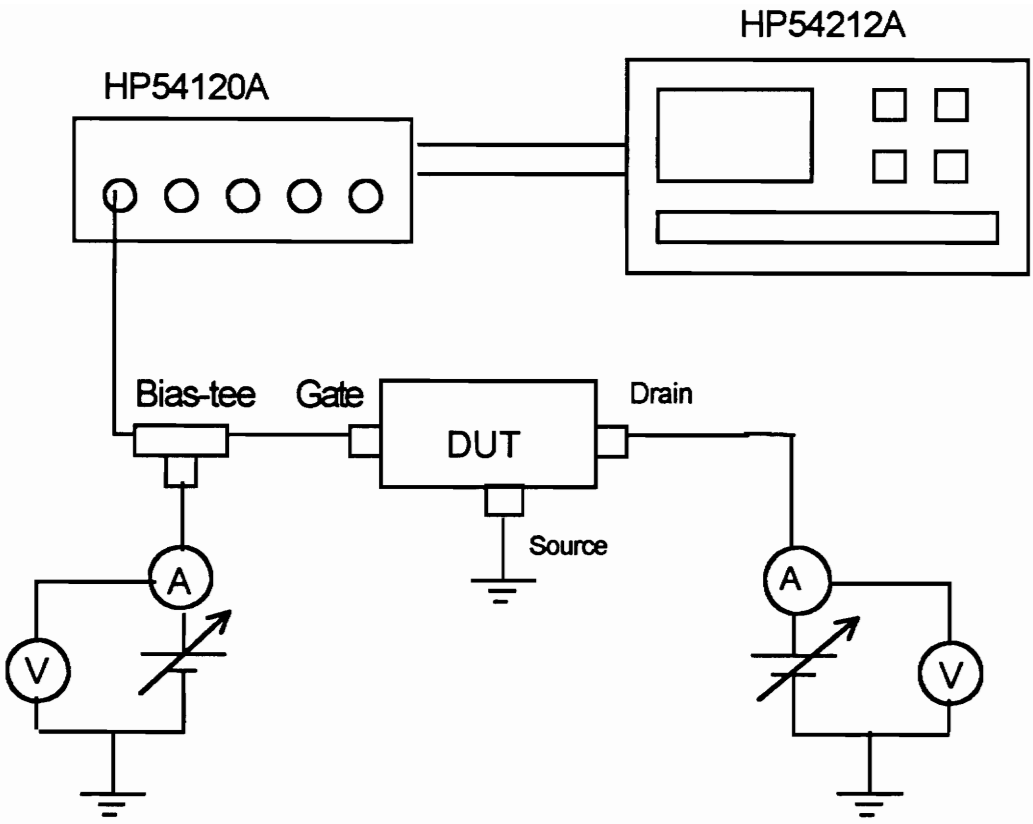



**Figure 5.2.4 Experimental Setup**

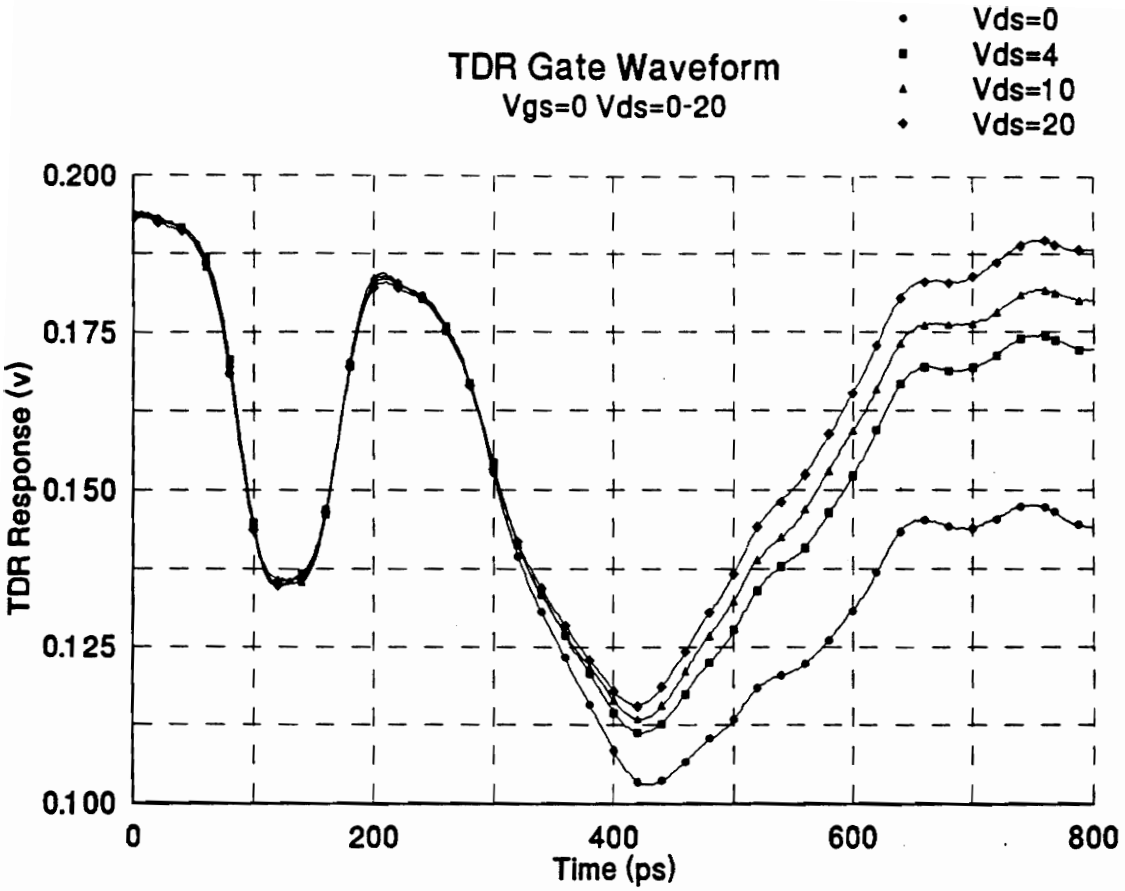



**Figure 5.2.5 Zero Bias TDR Waveforms**

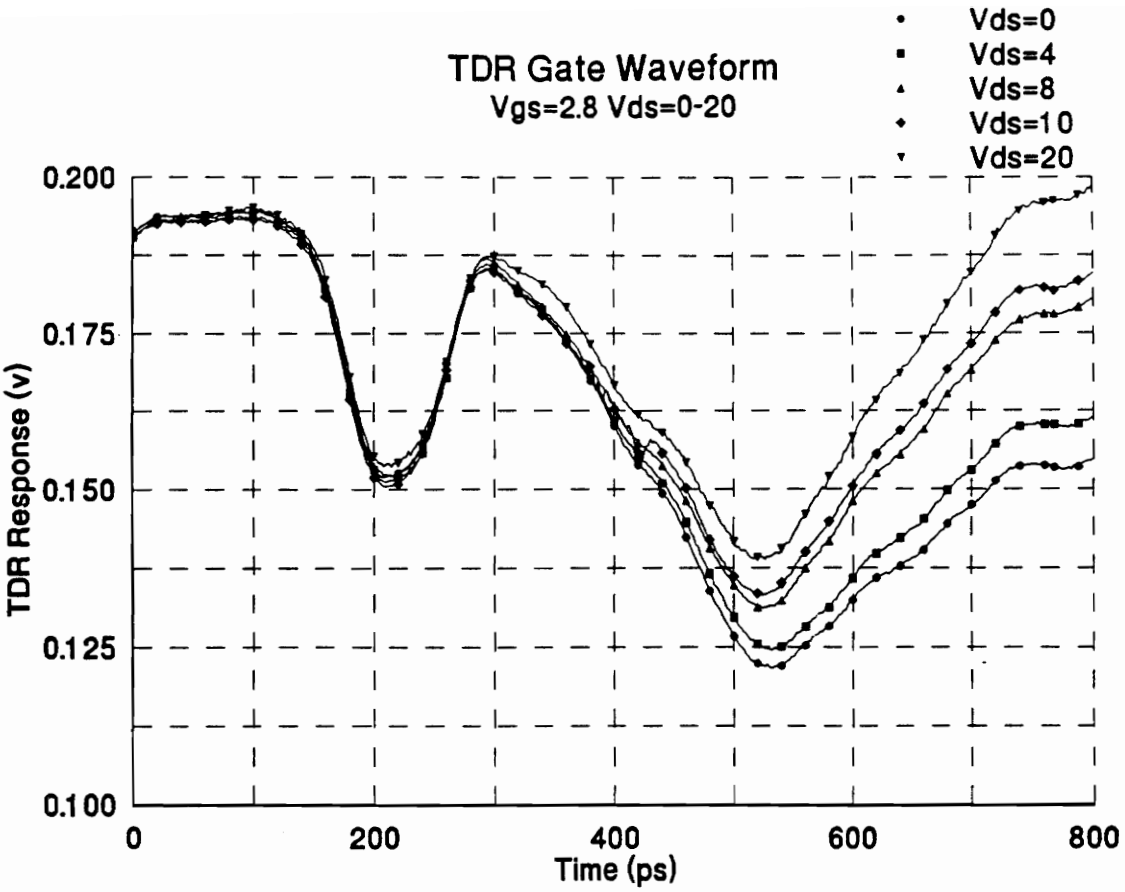



**Figure 5.2.6 Vds=2.8 -- Bias TDR Waveforms**

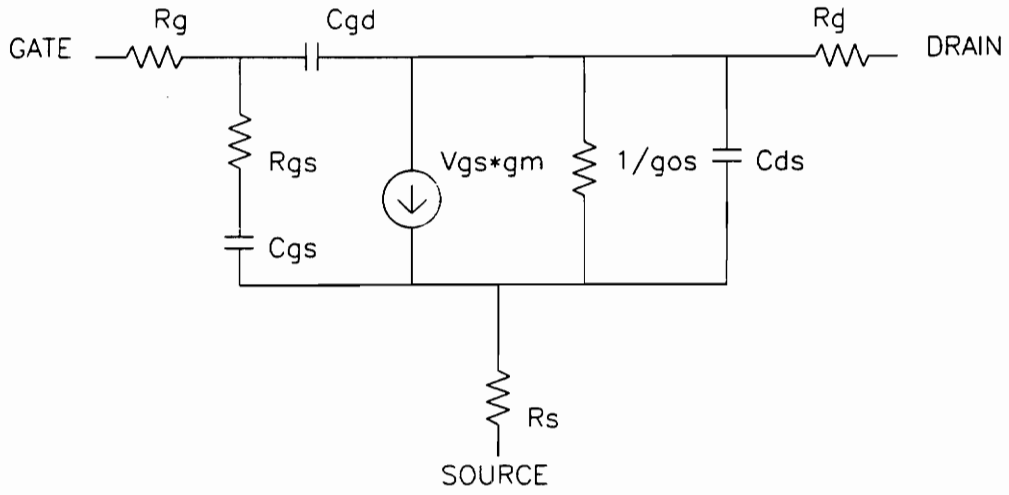



**Figure 5.3.1 Transistor Model**

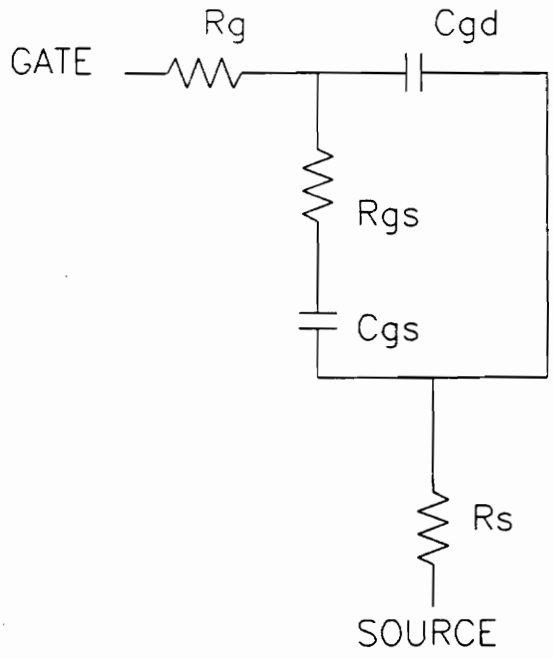



**Figure 5.3.2 TDR Gate Model**

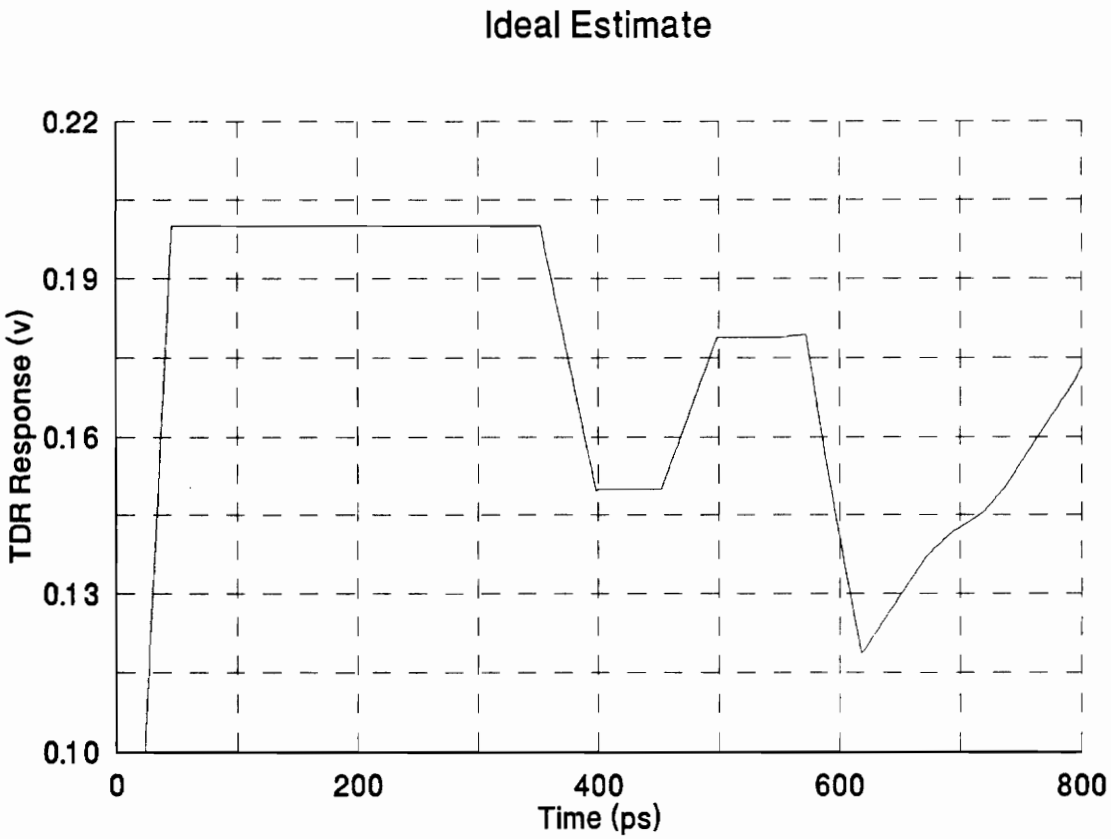



**Figure 5.3.3 Ideal Model at Zero Bias**

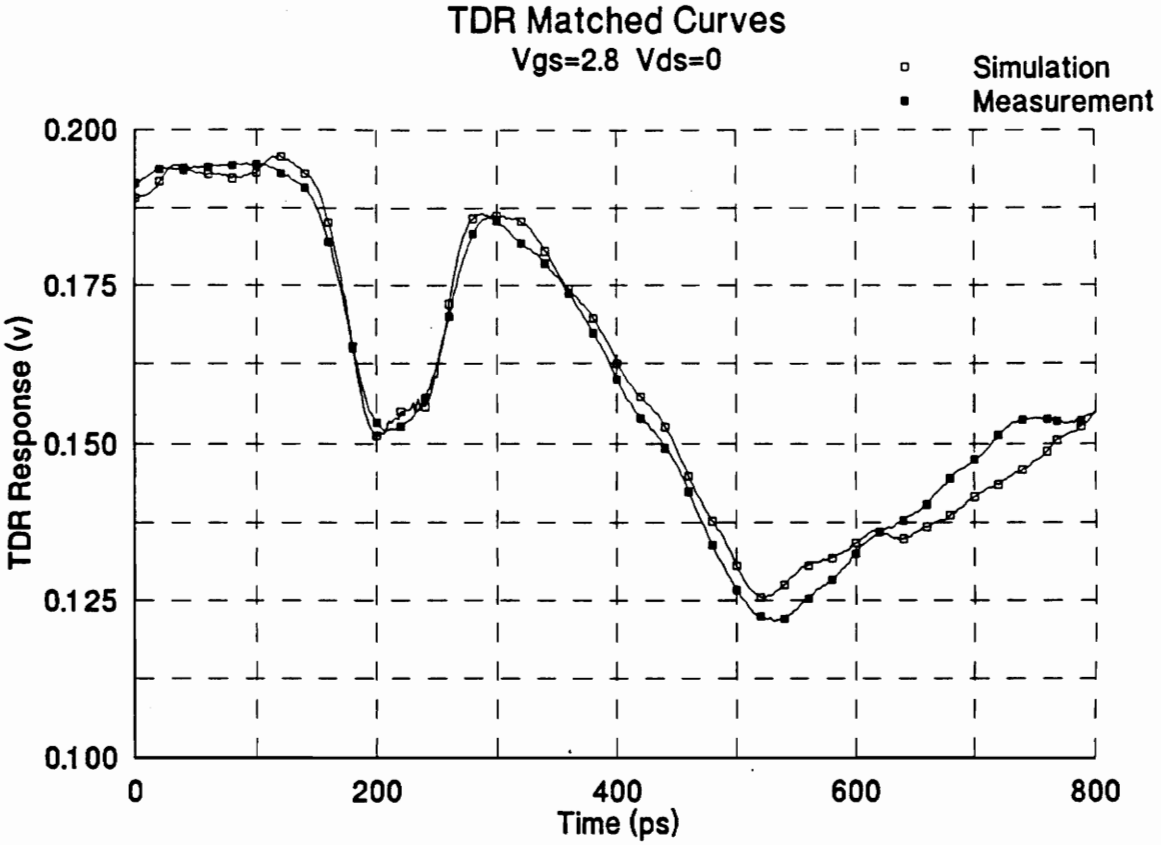



**Figure 5.3.4 TDR Matched Curve Vgs=2.8 Vds=0**

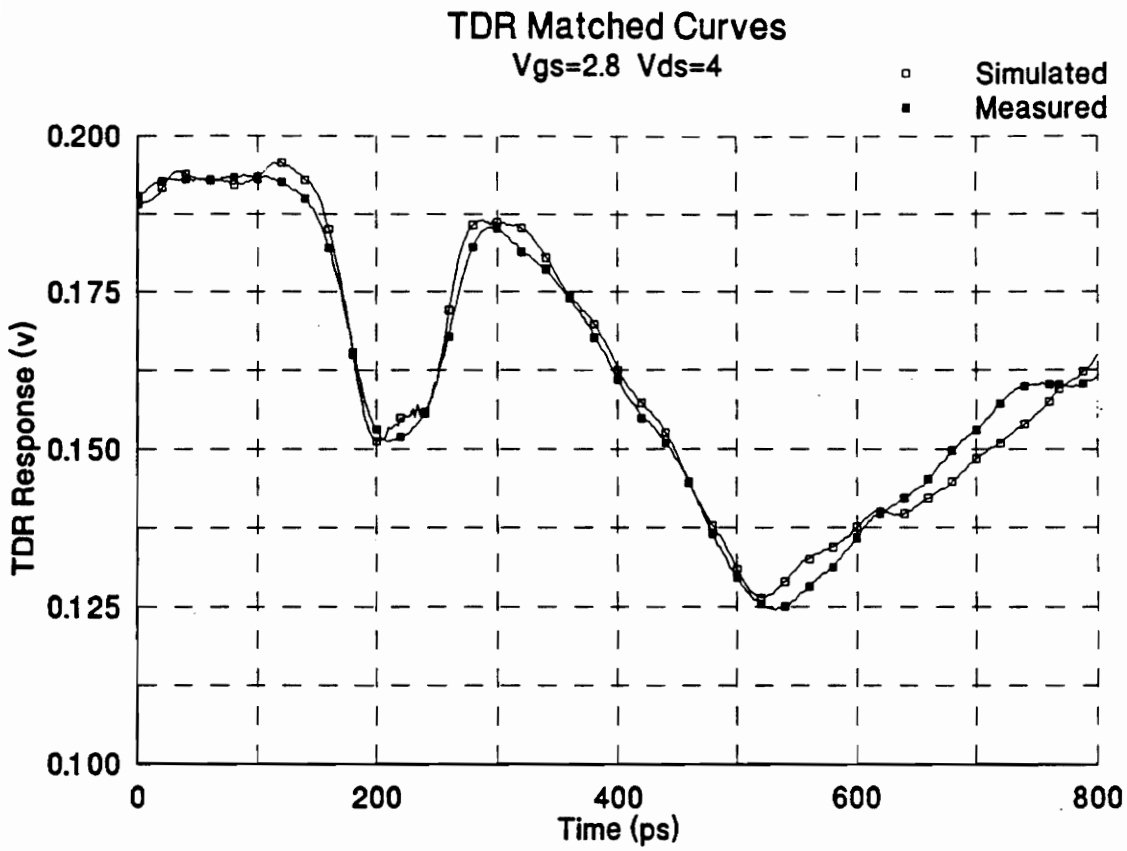



**Figure 5.3.5 TDR Matched Curve Vgs=2.8 Vds=4**

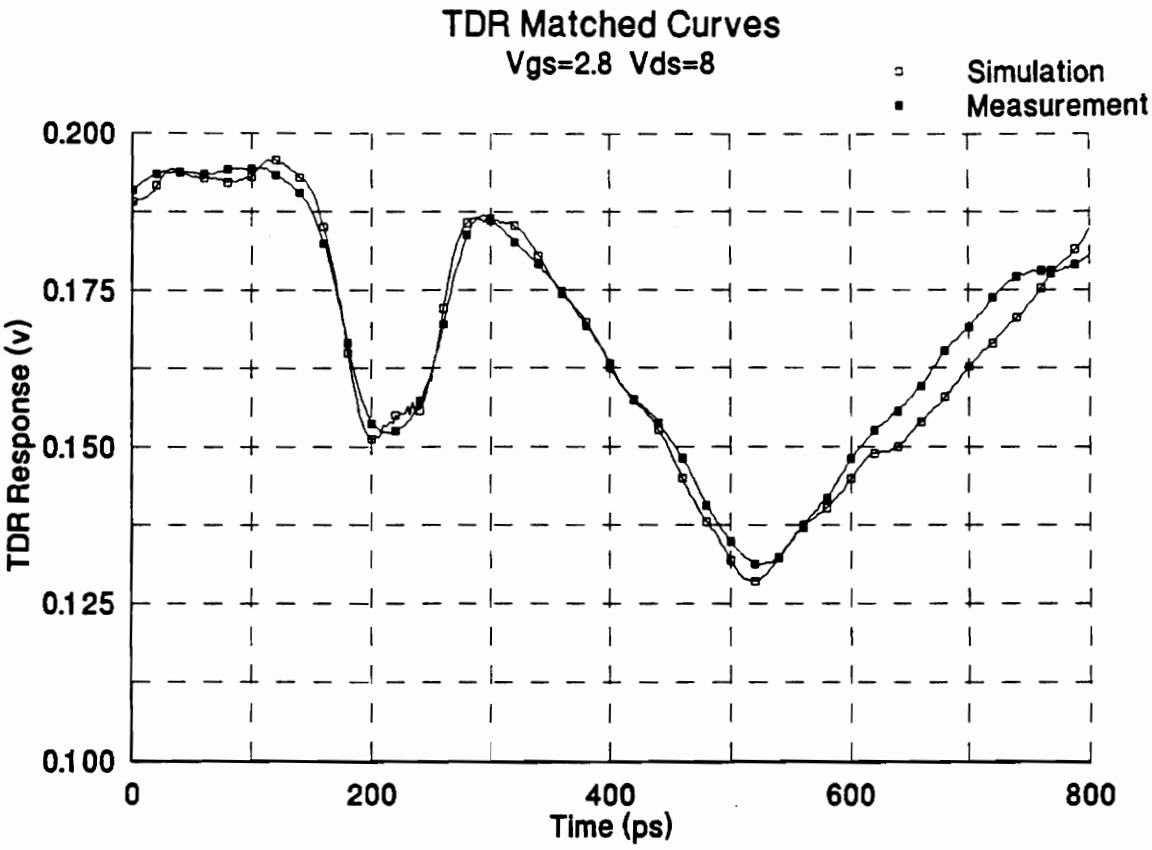



**Figure 5.3.6 TDR Matched Curve Vgs=2.8 Vds=8**

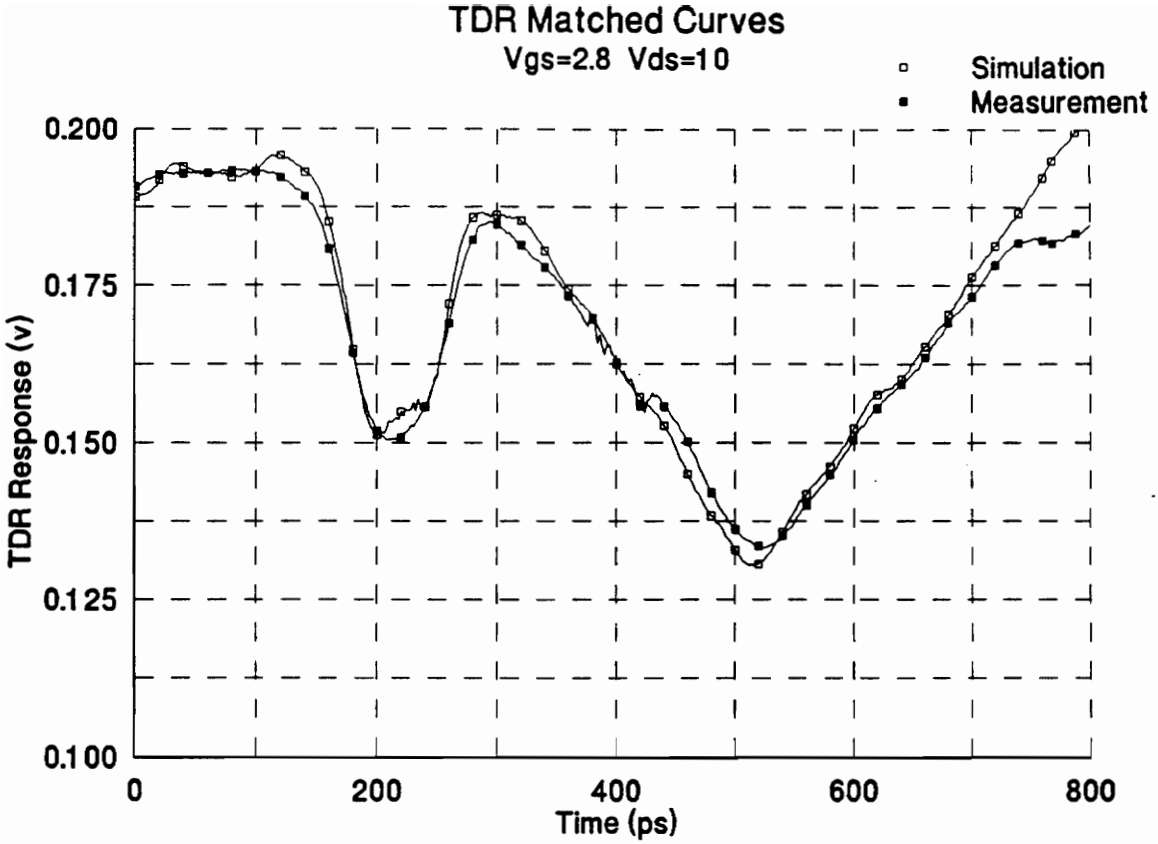



**Figure 5.3.7 TDR Matched Curve Vgs=2.8 Vds=10**

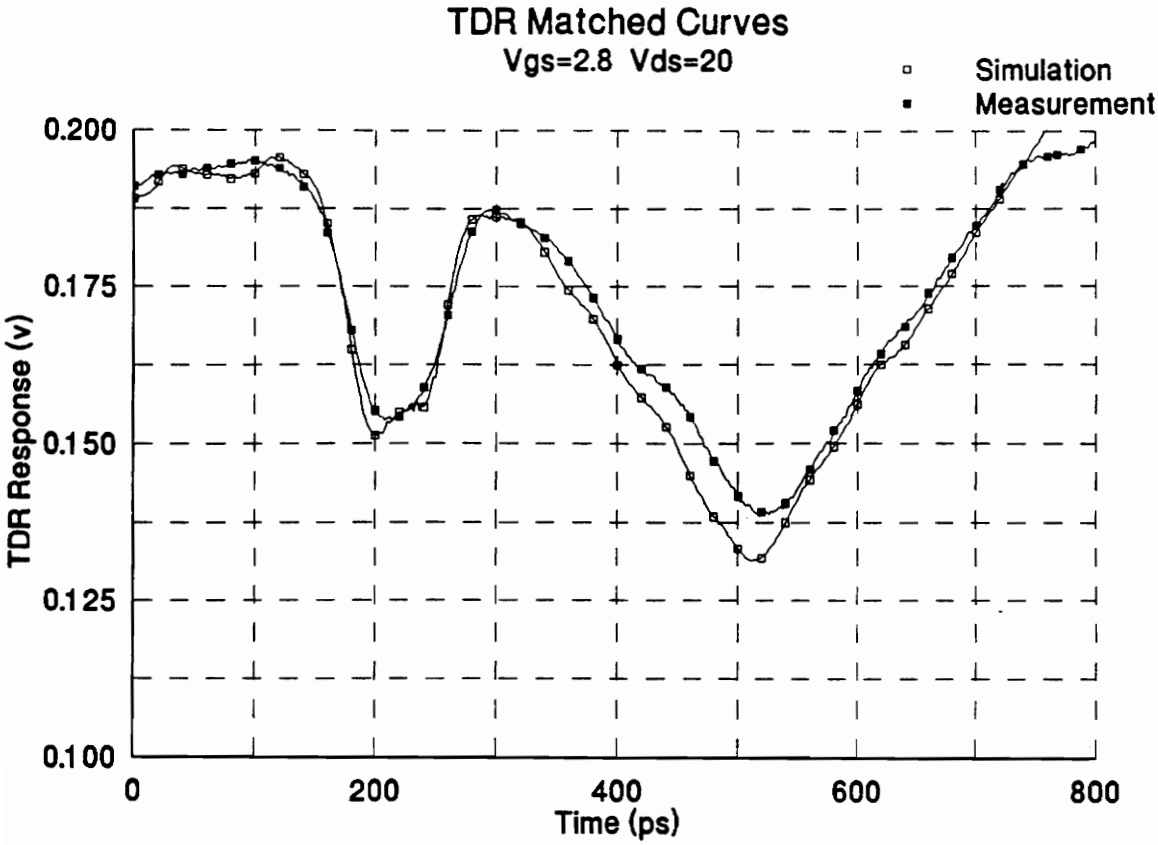
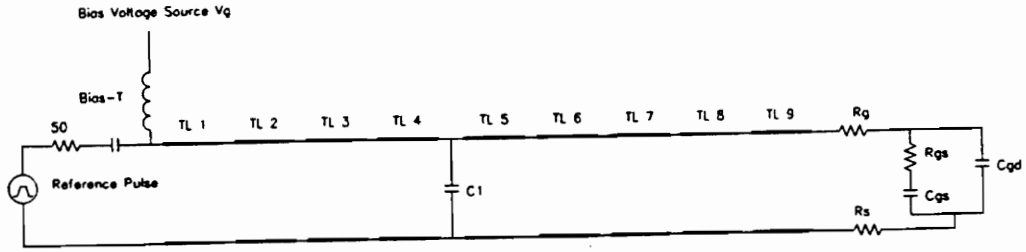



**Figure 5.3.8 TDR Matched Curve Vgs=2.8 Vds=20**




| Transmission Lines | | | Capacitors | |
|---|---|---|---|---|
| No. | Delay (ps) | Impedance(Ohms) | No. | Value (pF) |
| TL1 | 80 | 53 | C1 | 0.2 |
| TL2 | 50 | 51 | Cgs | 6 |
| TL3 | 15 | 48 | Cgd | variable |
| TL4 | 30 | 25 | | |
| TL5 | 10 | 26 | **Resistors** | |
| TL6 | 40 | 48 | No. | Value (Ohms) |
| TL7 | 25 | 32 | Rg | 9 |
| TL8 | 30 | 26 | Rs | 9 |
| TL9 | 20 | 23 | Rgs | 0 |

**Figure 5.5.9 TDR Circuit Model**

# Chapter VI. Conclusion

A High Frequency Power MOSFET wideband Gate model for the Motorola MRF162 High Frequency Power Transistor has been developed and simulated. The device theory predicted that the large capacitive contribution would limit the high frequency operation of the transistor. Also, it was shown that the associated Gate resistance hinders the time the Gate can be charged and discharged. This was also found to be true in the wideband model.

Not only were the device characteristics evident in the wideband model, but the package limitations could also be seen. Through device theory and physical device and package characteristics, an accurate model was achieved. The benefits of this wideband model were also explained.

It was found that the calculated model values followed the experimental values very closely. As expected, the Gate capacitance of the wideband model decreased as the Drain to Source bias increased. The parasitic values found on the data sheets closely followed the wideband model values. Final model verification was obtained from shows good agreement between the measured and the simulated waveform matching using the Modified Transient Circuit Analysis Package (MTCAP). The resultant Gate model obtained is valid for the range of frequencies from 100 MHz up to 400 MHz.

Further work can include continued modeling of the parasitic capacitances and On-resistance. At different bias conditions, the incident pulse could be launched into the

Drain and the Source. The other parasitic capacitances could be determined and the On-resistance evaluated. TDR waveform interpretation and matching takes a great deal of time and insight into the physical realities of the device being tested.

As Power MOSFETs reach further into the market, their replacement of Bipolar Junction Transistors will provide a need for more accurate models. Wideband models will be of great advantage over typical scattering parameter techniques.

# Appendix A

*Motorola Specification Sheets*

MOTOROLA

# SEMICONDUCTORS

## MRF162

**The RF Line**

15 W 2.0-400 MHz

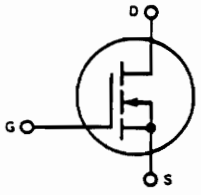
**N-CHANNEL TMOS BROADBAND RF POWER FET**

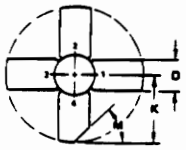
**N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR**

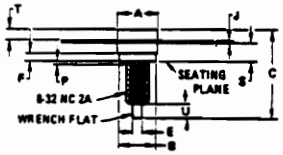
. . . designed for wideband large-signal output and driver applications in the 2.0 to 400 MHz range.

- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 15 Watts
  Minimum Gain = 11 dB
  Efficiency = 50% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested for Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 2.0 dB (Typ) at 300 mA, 400 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

TMOS™




STYLE 3:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 65 | Vdc |
| Drain-Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 65 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | ±40 | Vdc |
| Drain Current — Continuous | $I_D$ | 2.5 | Adc |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 50<br>0.286 | Watts<br>W/°C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 200 | °C |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 3.5 | °C/W |

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

| DIM | MILLIMETERS MIN | MAX | INCHES MIN | MAX |
|---|---|---|---|---|
| A | 7.06 | 7.26 | 0.278 | 0.286 |
| B | 6.20 | 6.50 | 0.244 | 0.256 |
| C | 14.99 | 16.51 | 0.590 | 0.650 |
| D | 5.46 | 5.96 | 0.215 | 0.235 |
| E | 1.40 | 1.65 | 0.055 | 0.065 |
| F | 1.52 | – | 0.060 | – |
| J | 0.08 | 0.17 | 0.003 | 0.007 |
| K | 11.05 | – | 0.435 | – |
| M | 45° NOM | | 45° NOM | |
| P | – | 1.27 | – | 0.050 |
| S | 3.00 | 3.25 | 0.118 | 0.128 |
| T | 1.40 | 1.78 | 0.055 | 0.070 |
| U | 2.92 | 3.68 | 0.115 | 0.145 |

CASE 244-04

TMOS is a trademark of Motorola Inc.

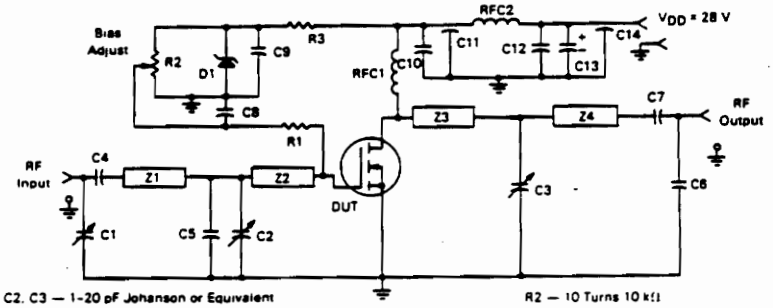


DS5887

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain-Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 5.0 mA) | $V_{(BR)DSS}$ | 65 | — | — | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 28 V, $V_{GS}$ = 0) | $I_{DSS}$ | — | — | 2.0 | mAdc |
| Gate-Source Leakage Current ($V_{GS}$ = 40 V, $V_{DS}$ = 0) | $I_{GSS}$ | — | — | 1.0 | μAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 V, $I_D$ = 25 mA) | $V_{GS(th)}$ | 1.0 | 3.0 | 6.0 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 V, $I_D$ = 250 mA) | $g_{fs}$ | 250 | 400 | — | mmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 28 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | — | 24 | — | pF |
| Output Capacitance ($V_{DS}$ = 28 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | — | 27 | — | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 28 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | — | 5.5 | — | pF |
| **FUNCTIONAL CHARACTERISTICS** (Figure 1) | | | | | |
| Noise Figure ($V_{DS}$ = 28 Vdc, $I_D$ = 300 mA, f = 400 MHz, $Z_S$ = 5.9 + j7.8 Ω, $Z_L$ = 3.78 + j5.75 Ω) | NF | — | 2.0 | — | dB |
| Common Source Power Gain ($V_{DD}$ = 28 Vdc, $P_{out}$ = 15 W, f = 400 MHz, $I_{DQ}$ = 50 mA) | $G_{ps}$ | 11 | 13.6 | — | dB |
| Drain Efficiency ($V_{DD}$ = 28 Vdc, $P_{out}$ = 15 W, f = 400 MHz, $I_{DQ}$ = 50 mA) | $\eta$ | 45 | 50 | — | % |
| Electrical Ruggedness ($V_{DD}$ = 28 Vdc, $P_{out}$ = 15 W, f = 400 MHz, $I_{DQ}$ = 50 mA, VSWR 30:1 at All Phase Angles) | $\psi$ | No Degradation in Output Power | | | |

**FIGURE 1 — 400 MHz TEST CIRCUIT**




C1, C2, C3 — 1-20 pF Johanson or Equivalent
C4, C7 — 270 pF, 100 Mil Chip Cap
C5 — 18 pF Mini-Unieco or Equivalent
C6 — 12 pF, 100 Mil Chip Cap
C8 — 0.01 μF, 50 V Disc Ceramic
C9, C10, C12 — 0.1 μF, 50 V Disc Ceramic
C11, C14 — 680 pF Feedthru
C13 — 20 μF, 50 V
D1 — 1N5925A Motorola Zener
R1 — 10 kΩ, 1/4 W
R2 — 10 Turns 10 kΩ
R3 — 1.6 kΩ, 1/4 W
RFC1 — 10 Turns, 0.300" ID #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200 — 19/48
Z1 — 1.5" × 0.250" Microstrip
Z2 — 0.6" × 0.250" Microstrip
Z3 — 1.3" × 0.250" Microstrip
Z4 — 0.85" × 0.250" Microstrip
Board — Glass Teflon .62 Mils, $\varepsilon_r$ = 2.56

FIGURE 2 — OUTPUT POWER versus INPUT POWER

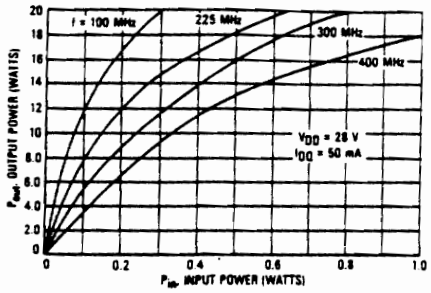



FIGURE 3 — OUTPUT POWER versus INPUT POWER

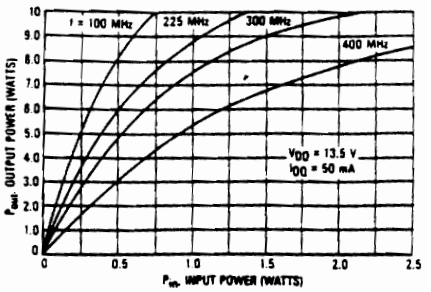



FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

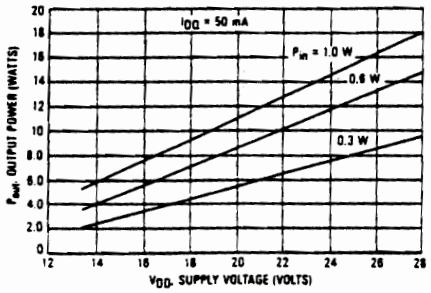



FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 300 MHz

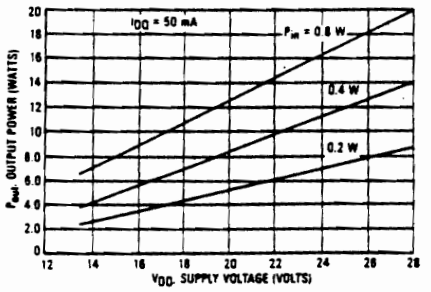



FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

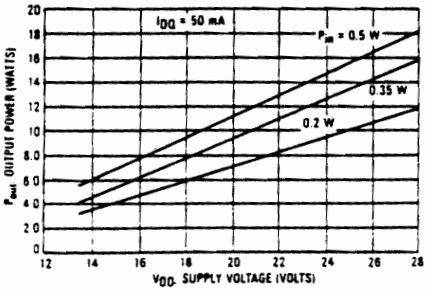



FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

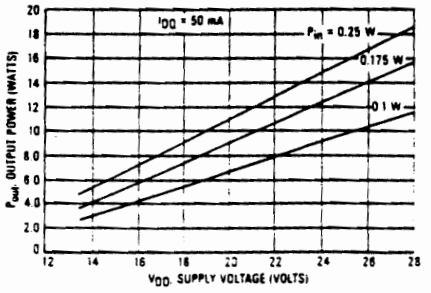


FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

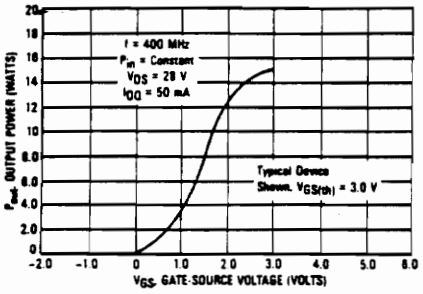



FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

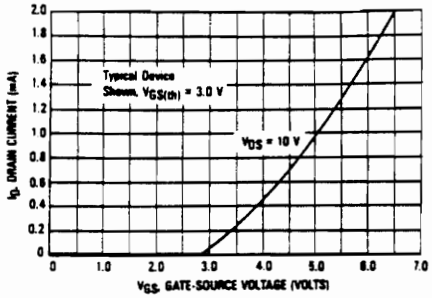



FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

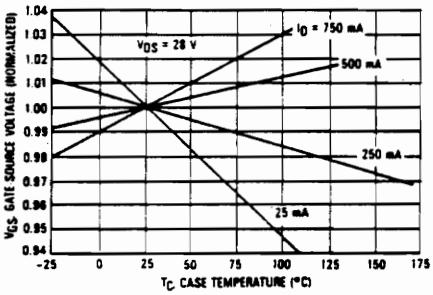



FIGURE 11 — CAPACITANCE versus DRAIN-SOURCE VOLTAGE

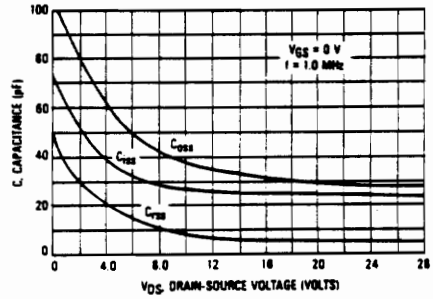


FIGURE 12 — DC SAFE OPERATING AREA

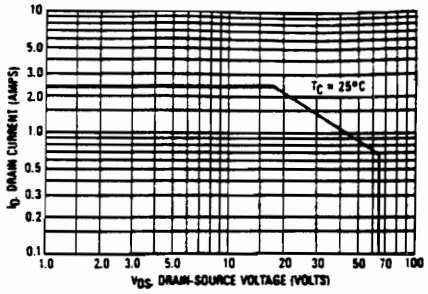
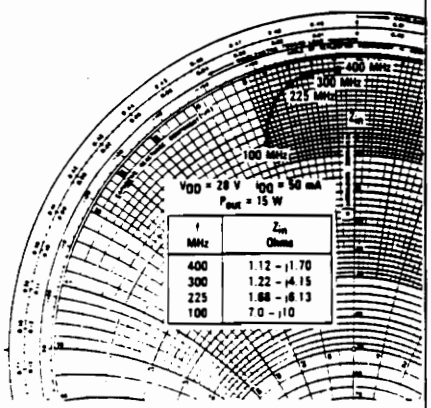
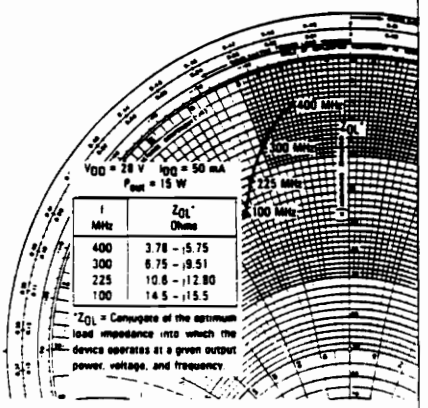



FIGURE 13 — LARGE SIGNAL SERIES EQUIVALENT INPUT IMPEDANCE, $Z_{in}$




| f MHz | $Z_{in}$ Ohms |
|---|---|
| 400 | 1.12 – j1.70 |
| 300 | 1.22 – j4.15 |
| 225 | 1.68 – j6.13 |
| 100 | 7.0 – j10 |

FIGURE 14 — LARGE SIGNAL SERIES EQUIVALENT OUTPUT IMPEDANCE, $Z_{OL}$*




| f MHz | $Z_{OL}$* Ohms |
|---|---|
| 400 | 3.78 – j5.75 |
| 300 | 6.75 – j9.51 |
| 225 | 10.6 – j12.80 |
| 100 | 14.5 – j15.5 |

*$Z_{OL}$ = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 15 – COMMON SOURCE SCATTERING PARAMETERS
50 OHM SYSTEM
$V_{DS}$ = 28 V, $I_D$ = 0.5 A

| f (MHz) | $S_{11}$ | | $S_{21}$ | | $S_{12}$ | | $S_{22}$ | |
|---|---|---|---|---|---|---|---|---|
| | $\|S_{11}\|$ | ∠θ | $\|S_{21}\|$ | ∠θ | $\|S_{12}\|$ | ∠θ | $\|S_{22}\|$ | ∠θ |
| 2.0 | 0.996 | -11 | 34.29 | 171 | 0.007 | +80 | 0.730 | -12 |
| 5.0 | 0.983 | -27 | 33.00 | 159 | 0.016 | +73 | 0.729 | -30 |
| 10 | 0.943 | -51 | 31.76 | 147 | 0.030 | +60 | 0.728 | -57 |
| 20 | 0.871 | -86 | 24.38 | 130 | 0.047 | +41 | 0.726 | -94 |
| 30 | 0.833 | -109 | 18.82 | 118 | 0.054 | +30 | 0.727 | -116 |
| 40 | 0.811 | -123 | 14.93 | 110 | 0.058 | +23 | 0.728 | -129 |
| 50 | 0.796 | -133 | 12.42 | 105 | 0.060 | +18 | 0.729 | -138 |
| 60 | 0.788 | -140 | 10.45 | 101 | 0.061 | +14 | 0.729 | -143 |
| 70 | 0.782 | -145 | 9.13 | 97 | 0.061 | +11 | 0.729 | -148 |
| 80 | 0.779 | -149 | 8.01 | 94 | 0.062 | +8.9 | 0.731 | -151 |
| 90 | 0.777 | -152 | 7.12 | 92 | 0.062 | +7.1 | 0.733 | -153 |
| 100 | 0.776 | -155 | 6.48 | 89 | 0.062 | +5.3 | 0.735 | -155 |
| 110 | 0.775 | -157 | 5.92 | 87 | 0.062 | +3.9 | 0.737 | -156 |
| 120 | 0.775 | -158 | 5.45 | 85 | 0.062 | +2.4 | 0.739 | -158 |
| 130 | 0.775 | -160 | 5.03 | 83 | 0.062 | +1.5 | 0.741 | -159 |
| 140 | 0.775 | -161 | 4.69 | 81 | 0.062 | +0.4 | 0.743 | -159 |
| 150 | 0.775 | -162 | 4.37 | 80 | 0.061 | -0.6 | 0.744 | -160 |
| 160 | 0.777 | -163 | 4.10 | 78 | 0.062 | -1.3 | 0.746 | -161 |
| 170 | 0.777 | -163 | 3.87 | 77 | 0.061 | -2.2 | 0.748 | -161 |
| 180 | 0.778 | -164 | 3.65 | 75 | 0.061 | -2.8 | 0.750 | -161 |
| 190 | 0.780 | -165 | 3.46 | 74 | 0.061 | -3.7 | 0.753 | -162 |
| 200 | 0.781 | -165 | 3.29 | 72 | 0.060 | -4.2 | 0.755 | -162 |
| 225 | 0.784 | -166 | 2.87 | 69 | 0.060 | -5.8 | 0.765 | -163 |
| 250 | 0.788 | -166 | 2.57 | 66 | 0.059 | -7.7 | 0.770 | -163 |
| 275 | 0.790 | -167 | 2.30 | 64 | 0.059 | -9.0 | 0.780 | -163 |
| 300 | 0.792 | -167 | 2.20 | 62 | 0.059 | -11 | 0.795 | -163 |
| 325 | 0.794 | -168 | 1.94 | 57 | 0.059 | -12 | 0.812 | -163 |
| 350 | 0.794 | -169 | 1.78 | 56 | 0.058 | -15 | 0.815 | -163 |
| 375 | 0.799 | -169 | 1.67 | 54 | 0.057 | -16 | 0.826 | -163 |
| 400 | 0.805 | -169 | 1.56 | 51 | 0.055 | -17 | 0.836 | -163 |
| 425 | 0.815 | -169 | 1.45 | 50 | 0.054 | -17 | 0.862 | -163 |
| 450 | 0.825 | -169 | 1.39 | 47 | 0.053 | -17 | 0.860 | -162 |
| 475 | 0.834 | -170 | 1.32 | 45 | 0.052 | -17 | 0.871 | -162 |
| 500 | 0.837 | -170 | 1.23 | 42 | 0.051 | -16 | 0.871 | -162 |
| 525 | 0.838 | -171 | 1.16 | 41 | 0.050 | -14 | 0.872 | -162 |
| 550 | 0.843 | -171 | 1.11 | 39 | 0.048 | -13 | 0.883 | -162 |
| 575 | 0.845 | -172 | 1.07 | 37 | 0.048 | -12 | 0.894 | -162 |
| 600 | 0.855 | -172 | 1.03 | 35 | 0.046 | -10 | 0.901 | -163 |
| 625 | 0.856 | -173 | 0.977 | 33 | 0.045 | -9.0 | 0.905 | -163 |
| 650 | 0.875 | -173 | 0.947 | 32 | 0.044 | -7.0 | 0.921 | -163 |
| 675 | 0.885 | -173 | 0.914 | 30 | 0.044 | -5.0 | 0.938 | -163 |
| 700 | 0.888 | -174 | 0.873 | 27 | 0.043 | -4.0 | 0.949 | -164 |
| 725 | 0.892 | -174 | 0.841 | 27 | 0.042 | -1.0 | 0.947 | -164 |
| 750 | 0.900 | -174 | 0.821 | 26 | 0.043 | -2.0 | 0.970 | -164 |
| 775 | 0.910 | -175 | 0.814 | 24 | 0.044 | -4.0 | 0.978 | -164 |
| 800 | 0.918 | -176 | 0.775 | 22 | 0.045 | -8.0 | 0.978 | -164 |

FIGURE 16 — $S_{11}$, INPUT REFLECTION COEFFICIENT versus FREQUENCY
$V_{DS}$ = 28 V, $I_D$ = 0.5 A

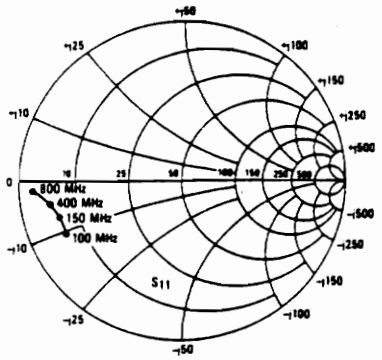



FIGURE 17 — $S_{12}$, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
$V_{DS}$ = 28 V, $I_D$ = 0.5 A

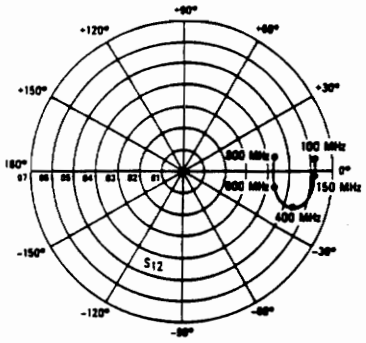



FIGURE 18 — $S_{21}$, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
$V_{DS}$ = 28 V, $I_D$ = 0.5 A

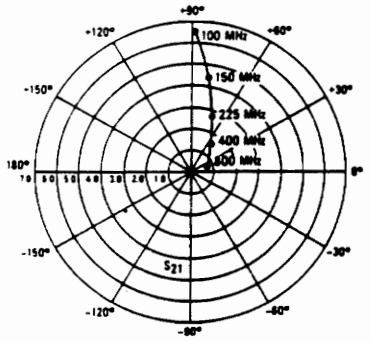
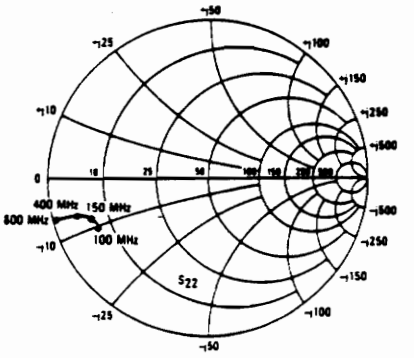



FIGURE 19 — $S_{22}$, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
$V_{DS}$ = 28 V, $I_D$ = 0.5 A



# Appendix B

*Microstrip Calculations*

*Design of Microstrip Waveguide*

W= strip width
h=substrate thickness  Values in
ep=dielectric constant  mills=1/1000 inch
t=metal thichness

$W = 5..200 \qquad \varepsilon p = 2.2 \qquad h = 10 \qquad t = 1.34$

---

$\eta o = 120 \cdot \pi$

$$A1_W = \frac{W}{h} + \frac{1.25}{\pi}\cdot\frac{t}{h}\cdot\left(1 + \ln\left(\frac{4\cdot\pi\cdot W}{t}\right)\right) \qquad A2_W = \frac{W}{h} + \frac{1.25}{\pi}\cdot\frac{t}{h}\cdot\left(1 + \ln\left(\frac{2\cdot h}{t}\right)\right)$$

$$A_W = \text{if}\left[\frac{W}{h} > \frac{1}{(2\cdot\pi)}, A2_W, A1_W\right]$$

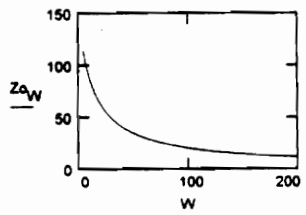
$$F1_W = \left(1 + 12\cdot\frac{h}{W}\right)^{-\frac{1}{2}} + 0.04\cdot\left(1 - \frac{W}{h}\right)^2 \qquad F2_W = \left(1 + 12\cdot\frac{h}{W}\right)^{-\frac{1}{2}}$$

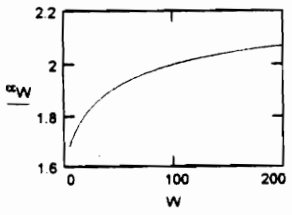
$$F_W = \text{if}\left(\frac{W}{h} > 1, F2_W, F1_W\right)$$

$$\varepsilon_W = \frac{(\varepsilon p + 1)}{2} + \frac{(\varepsilon p - 1)}{2}\cdot F_W - \frac{(\varepsilon p - 1)}{4.6}\cdot\frac{t}{h}\cdot\frac{1}{\left(\sqrt{\frac{W}{h}}\right)}$$

$$Zo1_W = \frac{\eta o}{\left(2\cdot\pi\cdot\sqrt{\varepsilon_W}\right)}\cdot\ln\left(\frac{8}{A_W} + 0.25\cdot A_W\right) \qquad Zo2_W = \frac{\eta o}{\sqrt{\varepsilon_W}}\cdot\left(A_W + 1.393 + 0.667\cdot\ln\left(A_W + 1.444\right)\right)^{-1}$$

$$Zo_W = \text{if}\left(\frac{W}{h} > 1, Zo2_W, Zo1_W\right)$$




$n = 1..100$

| n | $Zo_n$ | $\alpha_w$ |
|---|---|---|
| 1 | 0 | 1.677 |
| 2 | 0 | 1.69 |
| 3 | 0 | 1.701 |
| 4 | 0 | 1.712 |
| 5 | 113.755 | 1.722 |
| 6 | 107.341 | 1.731 |
| 7 | 101.778 | 1.741 |
| 8 | 96.881 | 1.749 |
| 9 | 92.52 | 1.757 |
| 10 | 88.601 | 1.764 |
| 11 | 84.967 | 1.771 |
| 12 | 81.75 | 1.778 |
| 13 | 78.784 | 1.785 |
| 14 | 76.041 | 1.791 |
| 15 | 73.496 | 1.796 |
| 16 | 71.126 | 1.802 |
| 17 | 68.913 | 1.807 |
| 18 | 66.843 | 1.813 |
| 19 | 64.9 | 1.818 |
| 20 | 63.074 | 1.822 |
| 21 | 61.353 | 1.827 |
| 22 | 59.729 | 1.832 |
| 23 | 58.193 | 1.836 |
| 24 | 56.738 | 1.84 |
| 25 | 55.358 | 1.844 |
| 26 | 54.046 | 1.848 |
| 27 | 52.799 | 1.852 |
| 28 | 51.61 | 1.856 |
| 29 | 50.476 | 1.859 |
| 30 | 49.393 | 1.863 |
| 31 | 48.358 | 1.866 |
| 32 | 47.367 | 1.87 |
| 33 | 46.418 | 1.873 |
| 34 | 45.507 | 1.876 |
| 35 | 44.633 | 1.879 |
| 36 | 43.794 | 1.883 |
| 37 | 42.986 | 1.886 |
| 38 | 42.209 | 1.888 |
| 39 | 41.461 | 1.891 |
| 40 | 40.739 | 1.894 |
| 41 | 40.044 | 1.897 |
| 42 | 39.372 | 1.9 |
| 43 | 38.724 | 1.902 |
| 44 | 38.097 | 1.905 |
| 45 | 37.491 | 1.907 |
| 46 | 36.904 | 1.91 |
| 47 | 36.337 | 1.912 |
| 48 | 35.787 | 1.915 |
| 49 | 35.254 | 1.917 |
| 50 | 34.737 | 1.919 |

# Appendix C

*Capacitor Calculations*

## Calculations for Approximate Device Model -- Vds=28V & Vgs=0v @ 1 MHz

$$Crss = Cgd = 5.5pF$$
$$Ciss \approx Cgs+Cgd = 24pF$$
$$Cgs = 24pF - 5.5pF$$
$$Cgs = 18.5pF$$
$$Coss \approx Cds + Cgd = 27pF$$
$$Cds = 27pF - 5.5\ pF$$
$$Cds = 21.5pF$$

## Calculated Values for Approximate Device Model -- Other Bias Conditions & Vgs=0 @ 1 MHz

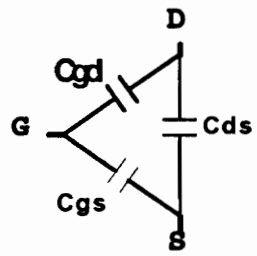
Values From Data Sheet Graph

| | Vds = 0 | Vds = 4 | Vds = 8 | Vds = 10 | Vds = 20 |
|---|---|---|---|---|---|
| Crss | 50 | 20 | 11 | 8 | 6 |
| Ciss | 74 | 40 | 29 | 26 | 25 |
| Coss | 110 | 60 | 42 | 37 | 29 |

Calculated Values

| | Vds = 0 | Vds = 4 | Vds = 8 | Vds = 10 | Vds = 20 |
|---|---|---|---|---|---|
| Cgd | 50 | 20 | 11 | 8 | 6 |
| Cgs | 24 | 20 | 18 | 18 | 19 |
| Cds | 60 | 40 | 31 | 29 | 23 |

**Equivalent Capacitive Model**



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# Vita

Richard W. Hoagland was born in Chatham, New Jersey. The first 17 years of his life were spent inventing new and ingenious ways of avoiding school. The next two years spent at The Peddie School, a small boarding school in central New Jersey, gave him a unique educational experience and an appreciation for individualized learning.

The next five years were spent at Clemson University. During this time, a great deal of experience and friendships were made through a CO-OP with General Electric's Industrial Lighting Division in Hendersonville, North Carolina. After receiving a Bachelor of Science degree and a true appreciation for electronics, Richard went on to receive a Master of Science degree from Virginia Polytechnic Institute and State University.

The next several years of his life will be spent working toward a Ph.D. at the University of Maryland. There he will further concentrate his studies in electronics.