Evaluation and Analysis on the Effect of Power Module Architecture on Common Mode Electromagnetic Interference

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ABSTRACT

Wide bandgap (WBG) semiconductor devices are becoming increasing popular in power electronics applications. However, WBG semiconductor devices generate a substantial amount of conducted electromagnetic interference (EMI) compared to silicon (Si) devices due to their ability to operate at higher switching frequencies, higher operating voltages and faster slew rates. This thesis explores and analyzes EMI mitigation techniques that can be applied to a power module architecture at the packaging level.

In this thesis, the EMI footprint of four different module architectures is measured experimentally. A time domain LTspice simulation model of the experimental test setup is then built. The common mode (CM) EMI emissions that escape the baseplate of the module into the converter is then examined through the simulation. The simulation is used to explore the CM noise footprint of eight additional module architectures that were found in literature. The EMI trends and the underlying mitigation principle for the twelve modules is explained by highlighting key differences in the architectures using common mode equivalent modelling and substitution and superposition theorem. The work aims to help future module designers by not only comparing the EMI performance of the majority of module architectures available in literature but by also providing an analysis methodology that can be used to understand the EMI behavior of any new module architecture that has not been discussed. Although silicon carbide (SiC) modules are used for this study, the results are applicable for any WBG device.

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GENERAL AUDIENCE ABSTRACT

As society moves towards the electric grid of the future, there have been increasing calls for high efficiency, high power density, and low electromagnetic interference (EMI) power electronic converters. EMI is a big problem when using wide-bandgap (WBG) devices as these devices can switch very quickly and handle higher voltages when compared to silicon devices. In this study, ways to reduce EMI in a WBG power module through twelve different types of packaging are explored. Four WBG power modules are designed and fabricated in the lab, whereas a simulation model was created to study the EMI behavior of the remaining eight power module. The EMI behavior of these modules is explained using common mode (CM) equivalent modeling and substitution and superposition theorem. This study is important because WBG devices are becoming more and more popular in power electronic applications. The author hopes the findings and analysis presented in this paper can help future module designers reduce the EMI footprint of modules they design.

To my parents Tahir and Asma Moaz, my sisters Urva and Rida Fatimah, and to my relatives and friends who supported me throughout my academic career.

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Chapter 1: Introduction

1.1 Background

The leading semiconductor choice for power electronics applications has been silicon (Si) for several decades [1]. Although Si-based power electronics provides the benefit of being mature and well-established, the technology is gradually reaching its limitations [2]. Wide-band gap (WBG) semiconductor devices have recently started to attract attention in power electronics due to their higher operating temperatures, faster switching speeds, higher voltage breakdown capability, and lower conduction losses [2], [3]. The intrinsic device properties of silicon (Si, green), and WBG devices such as gallium nitride (GaN, purple) and silicon carbide (SiC, blue) are shown in Figure 1.

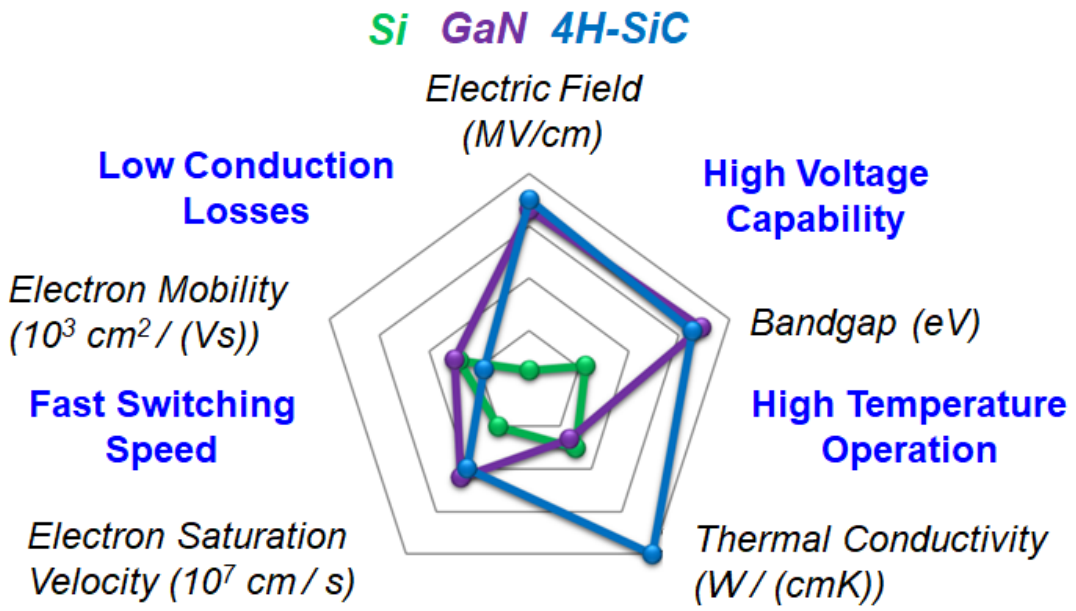


Figure 1: Intrinsic device properties of silicon (Si, Green), gallium nitride (GaN, Purple), and silicon carbide (SiC, Blue)

The higher voltage capability, higher operating temperatures, lower conduction losses, and faster switching speeds of WBG devices result in higher efficiency and power density designs; however, the higher operating frequency, and higher operating voltages also result in faster slew rates, which results in a larger electromagnetic interference (EMI) footprint of the system [4]–[9]. An example of an EMI issue limiting the performance of WBG devices can be found in [10], where a 10 kV, 120 A SiC MOSFET/JBS full bridge module [11] was run in a power electronic building block (PEBB) based impedance measurement unit (IMU) as shown in Figure 2(a). The converter could not be run at full voltage or rated power levels due to EMI issues. It can be seen in Figure 2(b) that the peak of the noise current flowing into the ground through the parasitic capacitance across the direct bonded copper (DBC) substrate in the power module was comparable to the current flowing through the inductor going to the output load (Figure 2(c)). The noise current contaminated the ground of the converter and was causing the controller to malfunction, limiting the operating conditions of the converter. It can therefore be concluded that properly addressing EMI issues is crucial to ensure that the advantages of WBG devices are not undermined. Since the noise current was flowing through the parasitic capacitance across the DBC substrate in the power module, it has therefore become necessary that EMI mitigation is considered in the initial design stages of the power modules.

In this work, the effect of the power module architecture on the common mode (CM) EMI generated by WBG devices is studied. The EMI emissions of a total of twelve different module architectures found in literature are explored, and different analysis techniques are used to explain and compare the EMI spectrum generated by each module.

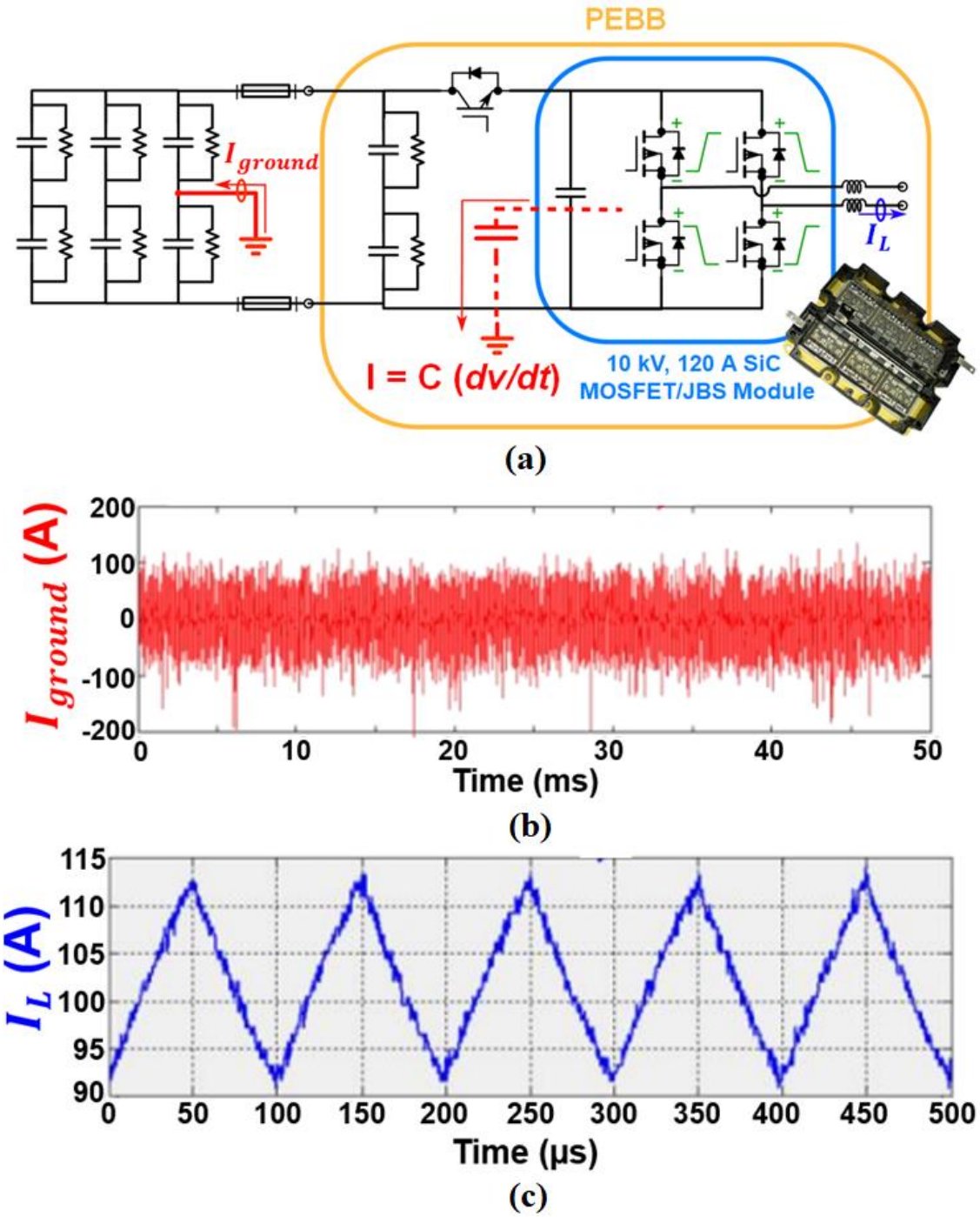


Figure 2: (a) Circuit schematic of 10 kV, 120 A SiC MOSFET/JBS module in PEBB based IMU (b) ground current (c) inductor current from [10]**.**

1.2 Literature Survey

Over the past decade, research efforts have been concentrated on mitigating CM noise issues in WBG devices at various levels of the converter. Solutions such as CM chokes and EMI filters are often implemented at the input of the converter to minimize the amount of CM current flowing into the system [12]–[19]. In [20], a CM filter is integrated inside the module package. These solutions increase the weight and volume of the system and limit the efficiency and power density of the converters [12], [21]. For example, the addition of an EMI filter can occupy nearly one-third of the volume of the converter [22]. Other CM current solutions involve the use of active gate drivers to minimize issues related to CM current [23]. Slowing down the slew rates can reduce noise generated, but also increases switching losses [24]. Active gate drivers employ slew rate control to help achieve a balance between switching losses and EMI noise, but can increase the complexity of the circuitry and controls of the converters [23], [25]. Snubber circuits and ferrite beads can also be used to dampen voltage and current oscillation, which results in lower EMI [26]–[30].

Less work has been dedicated to studying and mitigating CM current at the power module packaging level. It should be noted that reducing the EMI generated at the packaging level will not eliminate the need for a filter, but would minimize the amount of noise that will need to be filtered at the converter level. With the rise of WBG devices, the layout and design of power modules have garnered attention due to the higher sensitivity of WBG devices to parasitic inductances and capacitances [31]–[33]. Since CM current is worsened by these parasitics, which are related to the power module design, EMI mitigation and containment solutions at the package level are being investigated [34].

When it comes to reducing CM noise inside the package, a large portion of the literature is focused on minimizing the power-loop and gate-loop inductances that lead to ringing during switching events. A popular way to reduce the impact of stray inductances is to integrate decoupling capacitors inside the module to reduce the commutation loop [35]. Other designers have attempted to reduce the *dv/dt* of the module by embedding gate resistors to slow down the fast switching transients [36] or embedding resistor-capacitor (RC) snubbers and ferrite beads to reduce voltage ringing during switching events [37]. These techniques help mitigate CM current by reducing the switching speed; this approach offsets the benefits offered by WBG devices.

Other studies have focused on the capacitive coupling to the baseplate to mitigate the flow of CM current. The literature has proposed mitigating CM current by reducing the capacitive coupling of the switching-node to the baseplate present in the power module [38]. In traditional power modules, an insulated substrate is patterned to form a half-bridge configuration, with the switching-node pad being a significant portion of the footprint. This switching-node pad has capacitive coupling across the substrate insulation to the baseplate, creating a critical path for CM current to flow through. This capacitive coupling can be reduced either by shrinking the footprint of the switching-node or increasing the thickness of the insulation dielectric [39]. Other techniques include removing regions of the insulated substrate's bottom copper layer and replacing it with low-permittivity material [40], and canceling the CM current through the baseplate of a single-phase inverter with the input and output impedances of the EMI testbed being made to be [41], [42]. This CM current cancellation is achieved by manipulating the ratio between the switching-node capacitance and the equivalent baseplate capacitance. In addition, it has been shown that reducing the switching-node capacitance of the module and balancing the DC+ and DC- rail parasitics help reduce CM current by minimizing differential mode (DM) to CM conversion [43].

A review of the half bridge module architectures that have been used in literature to explore EMI mitigation at the module packaging level is now presented. In [44], the effect on the EMI performance of a GaN high-electron-mobility transistor (HEMTs) based half-bridge power module is studied with the integration of CM filter capacitors and decoupling capacitors — module architectures similar to Baseline (C_D) (Figure 3(b)) and Baseline (C_y) (Figure 3(c)). Compared to the Baseline architecture (Figure 3(a)), the integration of decoupling capacitors into the module results in mitigation in the CM noise generated in the 40 MHz to 100 MHz range. The integration of CM filter capacitors resulted in significant CM noise reduction in the conducted EMI frequency range. A Baseline (C_D, C_y) architecture (Figure 3(d)), module architecture obtained by combining Figure 3(b) and Figure 3(c), is eventually recommended. In [45], CM filtering capacitors are integrated directly into a SiC JFET based half-bridge power module, resulting in a module architecture similar to Baseline (C_y) shown in Figure 3(c). The EMI performance of the module architecture is compared to a standard Baseline module (Figure 3(a)) by measuring the noise at the line impedance stabilization network (LISN). The highest peak in the EMI spectrum for the noise generated by the Baseline (C_y) architecture showed a mitigation of 10 dB compared to the highest peak in the EMI spectrum of the Baseline module. An average mitigation of 6 dB was measured compared to the Baseline module architecture between 100 kHz to 1MHz. In [46], the EMI performance of a configuration similar to the Baseline (C_D) module architecture (Figure 3(a)) is simulated in a IGBT based half bridge chopper circuit. For the Baseline (C_D) module, the value of decoupling capacitors is varied from 0 to 1 µF and effect on the CM noise generated is simulated. It was observed that the addition of the decoupling capacitors reduces the high frequency noise peaks in the CM noise frequency spectrum, but introduces an additional peak in the frequency spectrum at lower frequencies. CM filtering capacitors are then added across the module terminals,

along with the decoupling capacitors, and the EMI footprint of the converter is experimentally tested. Significant mitigation was seen in the CM noise beyond 3 MHz. A Baseline (C_D, C_y) (Figure 3(d)) architecture is recommended. In [47], Baseline (C_D) and Baseline (C_y) are proposed; however, the integration of capacitors is not discussed. Instead the paper proposes modifying the module geometry and using the parasitic capacitances inside the module to obtain a somewhat similar effect. The architectures are tested as a half bridge operating in a boost converter topology.

Module architectures in literature that use stacked substrates for a lower EMI footprint are now discussed. In [48], the EMI footprint of a SiC half-bridge power module switched in a boost converter configuration is measured with four different module architectures: Baseline (Figure 3(a)), CM Screen (Figure 3(e)), CM Screen (C_D) (Figure 3(f)) and CM Screen (DC Mid) (Figure 3(g)). The EMI footprints of these four module architectures is compared and the CM Screen (DC Mid) architecture is concluded to have the lowest CM EMI in the conducted EMI frequency range — a mitigation of more than 15 dB over a wide frequency range. Although experimental results are provided, analysis of the noise reduction and frequency spectrum for each module architecture is not provided. In [47], the CM Screen (Figure 3(e)) and CM Screen (C_D) (Figure 3(f)) architectures are proposed and tested with half-bridge power modules operating in a boost converter topology. The integration of decoupling capacitors into the architecture for the CM Screen (C_D) is not discussed; however, a somewhat similar effect is achieved by modifying the geometry to take advantage of the module's parasitic capacitances. In [49], the EMI performance of a CM Screen (Figure 3(e)) and a CM Screen (DC Mid) (Figure 3(g)) architecture is compared in the time domain. The largest peak of the noise generated by the CM Screen (DC Mid) module architecture was measured to be ten times lower than the largest peak for the CM Screen module architecture. Little analysis on the mitigation seen is provided. In [50], the EMI performance of a

stacked substrate module architecture for a T-Type NPC power module (Figure 3(h)), made using a hybrid combination of SiC MOSFETs and Si IGBTs, is compared to a baseline single substrate T-Type NPC module architecture. The stacked substrate introduced into the module architecture is intended to act as an EMI shield and is connected to a fixed potential formed by the series connection of decoupling capacitors — a configuration reminiscent of CM Screen (DC Mid) (Figure 3(g)) from an EMI point of view. Experimental results showed a mitigation of up to 21 dB. Although analysis of the EMI results is presented, the analysis is done for a T-Type NPC power module and insights gained are not easily applicable to a half bridge module. In [51], a stacked substrate for half bridge applications is proposed with a CM Screen (DC-) (Figure 3(i)) and CM Screen (DC+) (Figure 3(j)) architecture. No EMI analysis of the architectures is presented. In [52] and [53], a stacked substrate half-bridge power module with a CM Screen (DC-, C_D) architecture (Figure 3(h)) is presented and the EMI performance is compared to a commercially available module with similar specifications. Experimental results showed an average mitigation of up to 14 dB and 25 dB in the noise voltage measured at the LISN, respectively. In [54], local shielding solutions to reduce CM current at the input of a GaN HEMT based half-bridge inverter leg are proposed and attenuation in the CM noise spectra is observed. An architecture similar to the CM Screen (DC+) (Figure 3(j)) architecture is explored. Shielding is also applied to the gate driver and between the thermal pad and the heatsink. A total noise reduction of up to 17 dB was observed. In [37], [40], [55] the CM screen / baseplate in the module architecture was split. All portions of the split CM screen were left floating. This technique can be used to obtain module architectures similar to Figure 3(k).

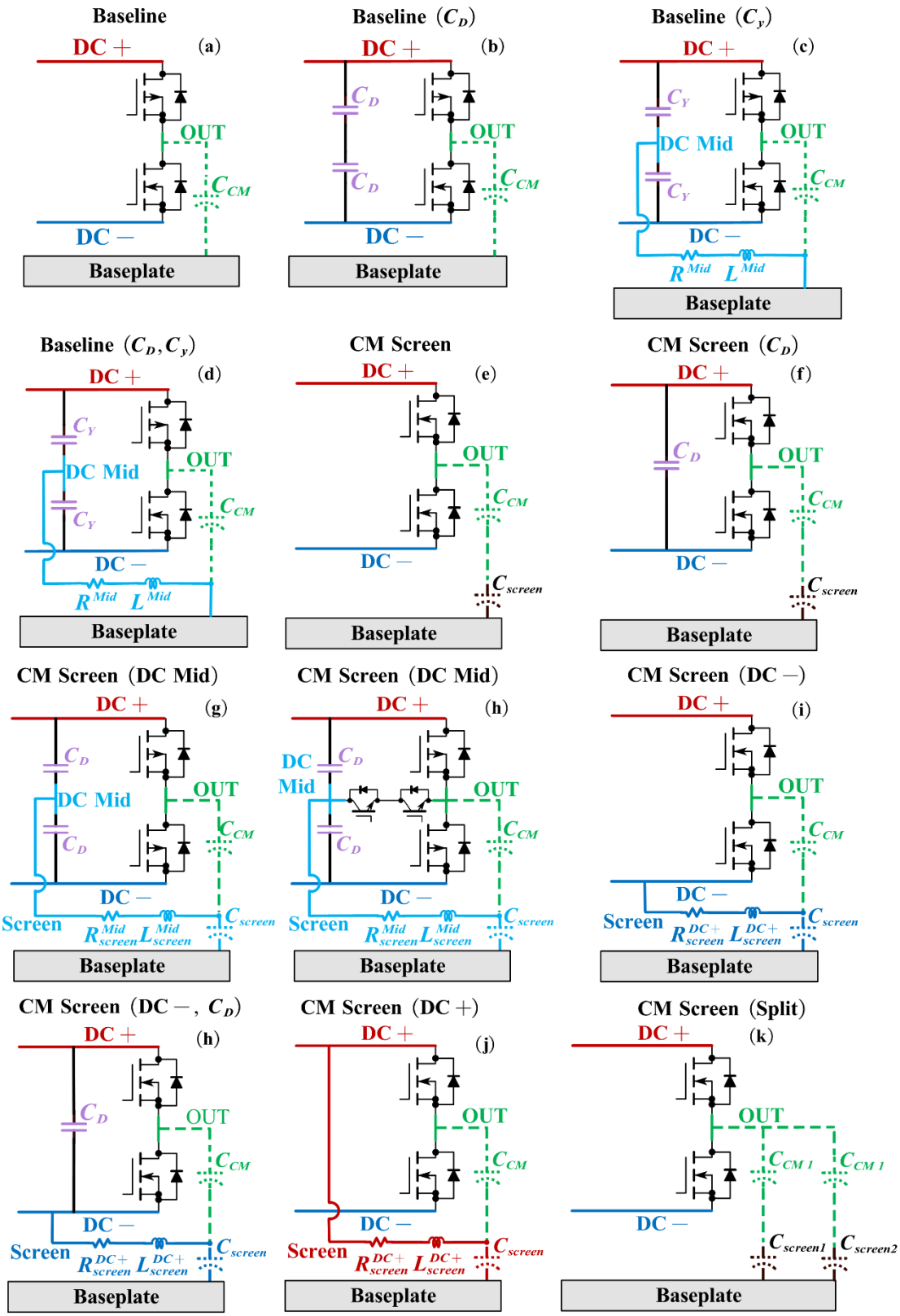


Figure 3: Module architectures explored in literature

Chapter 2: Introduction to Module Architectures

2.1 Introduction

This chapter introduces the twelve module architectures whose EMI footprint would be explored in this thesis. The hardware implementation of four of the module architectures is presented. The hypothetical designs that could be used to implement the remaining eight module architectures is also presented.

2.2 Module Layout

To study the impact of the CM screen, a new module design was developed. The design allows for testing the CM screen under different design conditions and provides insight into the effectiveness of containing CM current within the module. Figure 4(a) shows the topside view of the layout where 1.2 kV, 40 mΩ SiC MOSFETs are used in the half-bridge module. The DC+, DC– and OUT terminal placements are kept consistent between module variations, while allowing the flexibility to connect the screen to different DC nodes.

A side view of the CM screen module is shown in Figure 4(b). The module uses two 0.35-mm-thick alumina DBC substrates stacked together to create the screening layer. Wire bonds are used to electrically connect the top copper layer to the screening layer. This layout enables paralleling of many wire bonds to reduce the impedance to the screening layer.

In the literature, the CM screen is not only used to contain CM current, but also as a path for the commutation loop [52]. This enables a reduction in the power-loop inductance through magnetic field cancellation, which enables cleaner switching events that reduce EMI [52]. To avoid variations in the EMI due to changes in the power-loop inductances, all of the proposed

modules have the commutation loop on the top side of DBC 1 (Figure 4(b)). This allows for the screening layer to be used only to divert CM current and not to serve as part of commutation loop. This enables modification of the screening layer while keeping the power loop inductance consistent between a baseline and CM screen design. ANSYS Q3D simulations show that the power-loop inductance with and without the decoupling capacitors inside the module is 3.5 nH and 7.5 nH at 100 MHz, respectively.

The switching-node capacitance across DBC 1 to the screening layer is denoted as C_{CM}. The screening layer capacitance across DBC 2 to the baseplate is denoted as C_{screen}. Furthermore, C_{CM} is 80.2 pF, and C_{screen} is 436.9 pF for all the module variations. The module design also allows for two paralleled 10 nF decoupling capacitors to be placed in series to minimize the power-loop inductance and form the DC Mid node.

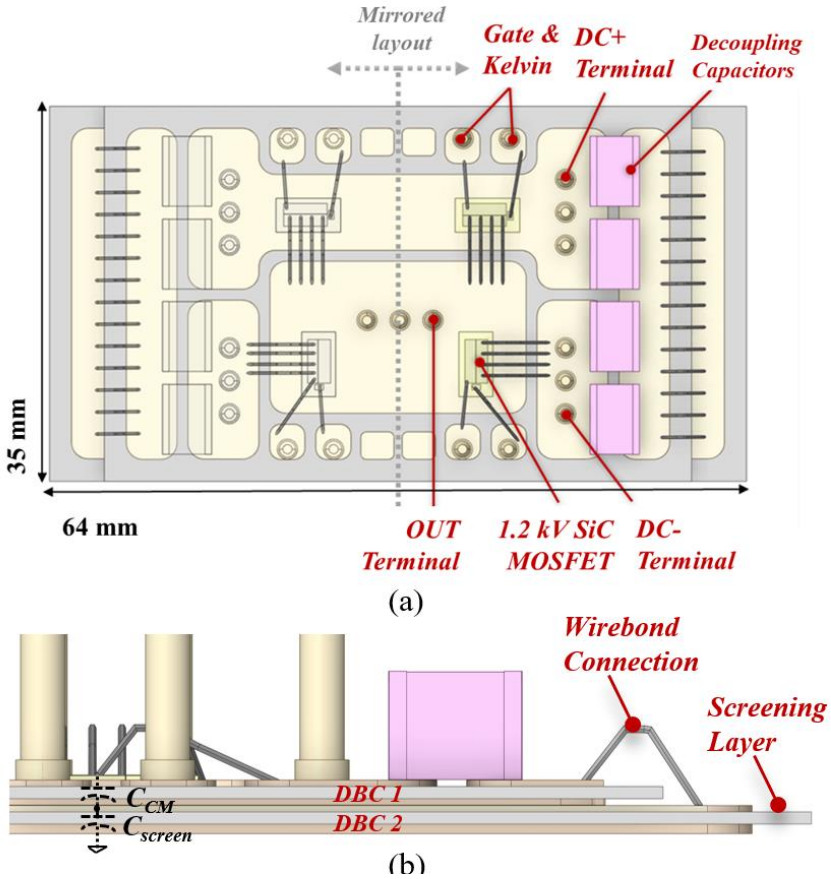


Figure 4: (a) Top view, and (b) side view of common-mode screen module.

2.3 Module Variations Fabricated

The amount of CM current that will be diverted to the DC–bus depends on the high-frequency impedance of the screening layer. For the CM screen to be effective, condition (1) has to be satisfied [48]:

$$Z_{screen} \ll Z_{bp} \tag{1}$$

where Z_{screen} is the impedance of the CM screen to the desired DC node and Z_{bp} is the impedance from the CM screen to the module baseplate. For the case of the CM screen (DC+) and (DC Mid) module in Figure 5(c) and (d), Z_{screen} can be respectively written as:

$$Z_{screen}^{DC+} = j\omega L_{screen}^{DC+} + R_{screen}^{DC+} \tag{2}$$

$$Z_{screen}^{Mid} = j\omega L_{screen}^{Mid} + R_{screen}^{Mid} + Z_{C_D} \quad (3)$$

where L_{screen}^{DC+}, R_{screen}^{DC+} and L_{screen}^{Mid}, R_{screen}^{Mid} are the equivalent inductance and resistance of the wire bonds connecting the screening layer to DC+ and DC Mid nodes, respectively; and Z_{C_D} is the impedance of the decoupling capacitors. For Figure 5(d), Z_{C_D} will be defined as:

$$Z_{C_D} = \frac{1}{j\omega C_D} \quad (4)$$

where C_D is the equivalent capacitance of the decoupling capacitors between the DC Mid and DC+ or DC- nodes respectively.

In both architectures, the impedance to the baseplate can be given as:

$$Z_{bp} = \frac{1}{j\omega C_{screen}} \quad (5)$$

where C_{screen} is the screening-layer capacitance across DBC 2 to the baseplate of the module. Using (2), (3), and (5), the inequality of (1) for the two CM screen modules becomes:

$$j\omega L_{screen}^{DC+} + R_{screen}^{DC+} \ll \frac{1}{j\omega C_{screen}} \quad (6)$$

$$j\omega L_{screen}^{Mid} + R_{screen}^{Mid} + Z_{C_D} \ll \frac{1}{j\omega C_{screen}} \quad (7)$$

where Z_{C_D} is defined according to equation (4). It can be seen from (6) and (7) that it is critical to reduce the parasitic inductance and resistance of the CM screen to be effective in redirecting the CM current to its connected DC node. For the case of the CM screen (DC Mid) module, the decoupling capacitor C_D (20 nF) was selected to be greater than 50 times C_{screen} (436.9 pF) to better divert the CM current from flowing towards the baseplate of the module to the DC Mid node [56]. It should be noted that integrating the decoupling capacitors C_D into the module increases the

footprint of DBC 2 and the value of C_{screen}. For this work, compact ceramic capacitors with high capacitance values were selected to balance the trade-offs between C_{screen} and C_D. Furthermore, the capacitors are C0G type, which means they are stable with variations in temperature and voltage. This allows the CM screen to have the same effectiveness under different voltage and temperature profiles.

With the module design established, four design variations (shown in Figure 5) were developed to study the impact of the module architecture on CM noise reduction. The variations are:

- ***Baseline Module:*** This variation only uses DBC 1. The OUT node is coupled to the baseplate through the switching-node capacitance C_{CM} (Figure 5(a)).
- ***Baseline (C_D) Module:*** This variation is the same as the baseline design but with the addition of integrated decoupling capacitors (Figure 5(b)).
- ***CM Screen (DC+) Module:*** DBC 1 and DBC 2 form a screening layer connected to the DC+ node. The DC+ node is coupled to the baseplate through C_{screen} (Figure 5(c)). There are no integrated decoupling capacitors in this module. The architecture also serves as the CM screen counterpart to the Baseline module.
- ***CM Screen (DC Mid) Module:*** Two series decoupling capacitors are included to create the midpoint DC Mid. DBC 1 and DBC 2 form a screening layer connected to the DC Mid node. The DC Mid is coupled to the baseplate through C_{screen} (Figure 5(d)). This architecture is the CM screen counterpart to the Baseline (C_D) module.

In Figure 5, the high-side and low-side SiC MOSFET dies in the half-bridge schematic are referred to as Q_H and Q_L, respectively. The final module prototypes are shown in Figure 6. Testing

these modules will provide a better understanding of the EMI mitigation associated with redirecting the CM current to different parts of the DC-bus.

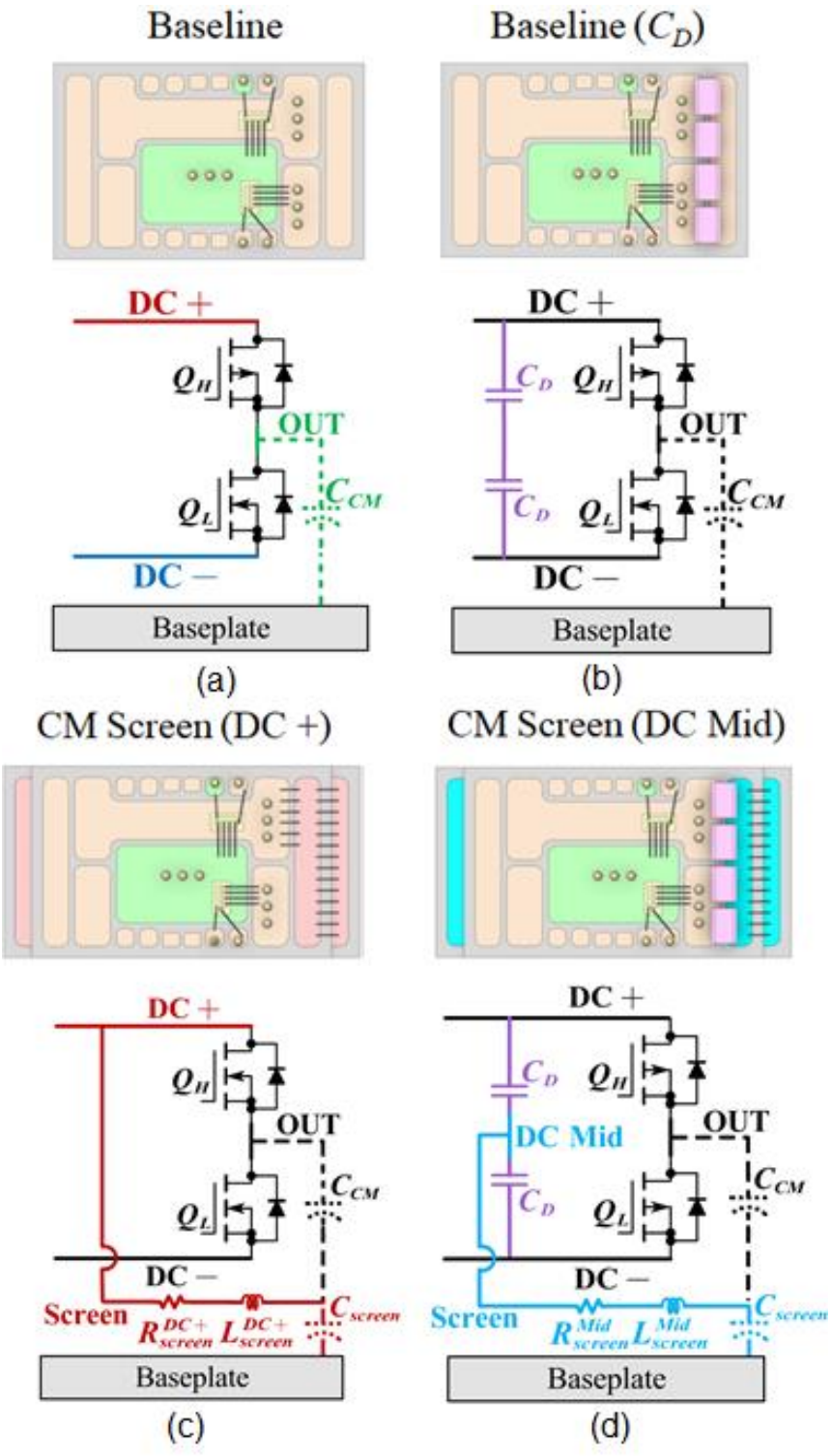


Figure 5: Variation of the module (a) Baseline module with no common-mode (CM) screen (b) Baseline module with no CM screen but with decoupling capacitors, (c) CM screen module with screening layer connected to DC+, and (d) CM screen module with screening layer connected to DC Mid.

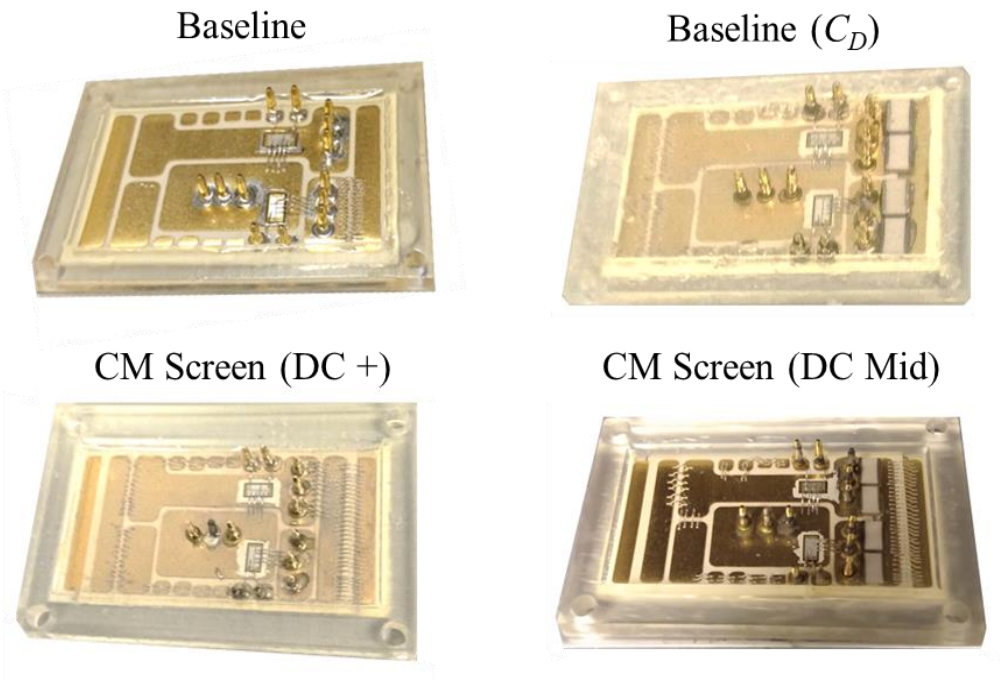


Figure 6: Images of the fabricated CM screen module prototypes.

2.4 Module Variations Simulated

In addition to the four module architectures studied experimentally, eight additional module architectures were simulated to evaluate and understand EMI mitigation using packaging techniques in more detail. The eight module architectures studied are shown in Figure 7. It should be noted that all eight architectures can be fabricated through packaging techniques; however, they were not made due to time limitations.

- ***Baseline (C_y) Module:*** This variation is the same as the Baseline (C_D) design, but the Mid node formed by the addition of integrated decoupling capacitors is shorted to the baseplate (Figure 7(a) and Figure 8(a)).

- ***CM Screen Module:*** DBC 1 and DBC 2 are stacked together to form a screening layer; however, the screening layer is not connected to the any node and left floating. The

architecture serves to show only the effect of stacked substrates on the generated EMI (Figure 7(b) and Figure 8(b)).

- ***CM Screen (C_D) Module:*** This variation is the same as the CM Screen design, but with the addition of integrated decoupling capacitors (Figure 7(c) and Figure 8(c)).

- ***CM Screen (DC+, C_D) Module:*** This variation is the same as the CM Screen (DC+) design but with the addition of integrated decoupling capacitors (Figure 7(d) and Figure 8(d)).

- ***CM Screen (DC-) Module:*** DBC 1 and DBC 2 form a screening layer connected to the DC- node. The DC- node is coupled to the baseplate through C_{screen} (Figure 7(e) and Figure 8(e)). There are no integrated decoupling capacitors in this module.

- ***CM Screen (DC-, C_D) Module:*** This variation is the same as CM Screen (DC-) design but with the addition of integrated decoupling capacitors (Figure 7(f) and Figure 8(f) or Figure 9(a)).

- ***CM Screen (DC+, DC-) Module:*** DBC 1 and DBC 2 form a screening layer that is split similar to what is shown in Figure 3(k). One half is connected to the DC+ node and the other half is connected to DC- node. The screening layer is split such that the OUT node has a capacitive coupling to each pad of the screening layer equal to half of capacitance C_{CM}, and the capacitive coupling each pad of the screening layer has to the baseplate is equal to half of the capacitance C_{screen}. There are no integrated decoupling capacitors in this module (Figure 7(g) and Figure 8(g)).

- ***CM Screen (DC+, DC-, C_D) Module:*** This variation is the same as CM Screen (DC-) design, but with the addition of integrated decoupling capacitors (Figure 7(h) and Figure 8(h) or Figure 9(b)).

In Figure 7, the high-side and low-side SiC MOSFET dies in the half-bridge schematic are referred to as Q_H and Q_L, respectively. Simulating the EMI behavior of these eight module architectures along with the four previously described will provide a better understanding of the EMI mitigation option available at the packaging level. Figure 8 shows hypothetical module layouts for the architectures shown in Figure 7. It should be noted that in Figure 8(f) and (h), the midpoint node has been removed as it was not needed. However, if needed inside the module vias can be used as shown in Figure 9.

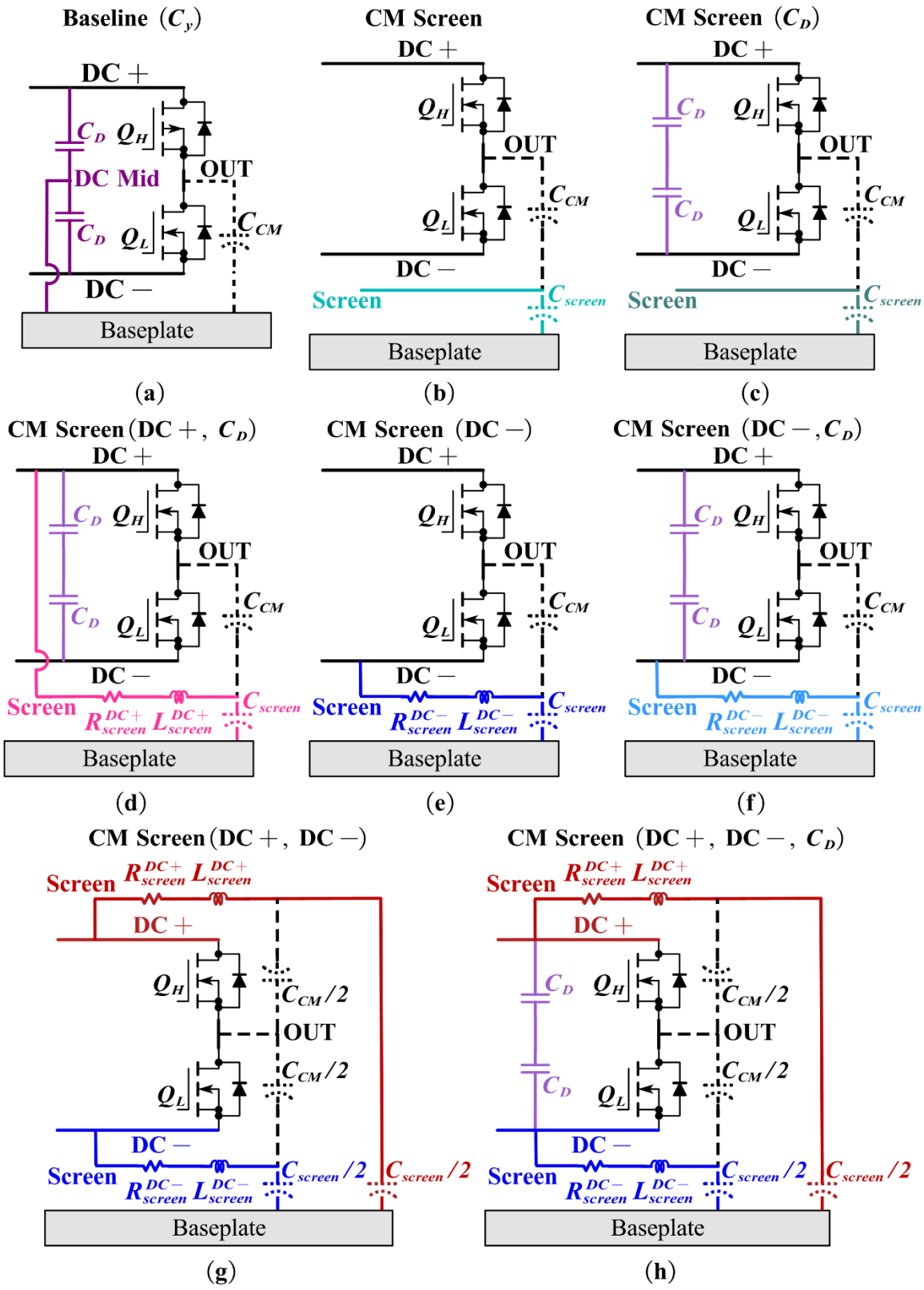


Figure 7: Eight additional module architectures studied through simulation

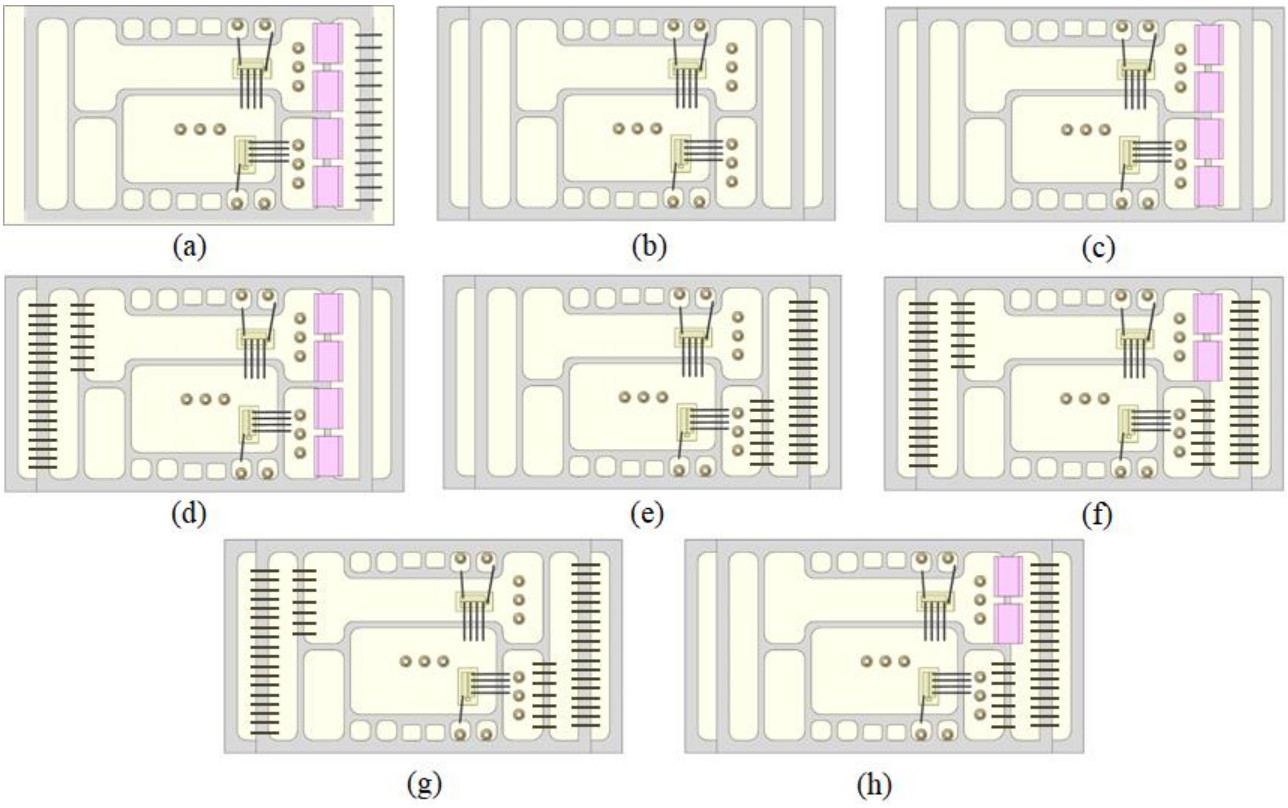


Figure 8: Hypothetical module layouts for the eight additional module architectures

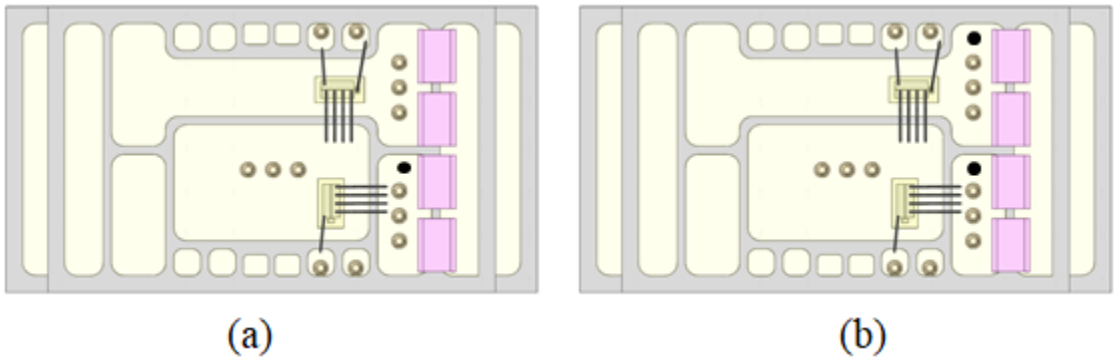


Figure 9: Hypothetical module layouts for (a CM Screen (DC-, C_D) and (b) CM Screen (DC+, DC-, C_D) with vias to ensue DC Mid node inside module

Chapter 3: Experimental Test Setup and Results

3.1 Introduction

The chapter introduces the test setup that was used for experimenting the four implemented module architectures. EMI noise results at the baseplate and the input of the converter with the four implemented module architectures are also presented. The chapter concludes with a preliminary slew rate and efficiency analysis that was done for these four implemented module architectures.

3.2 Test Setup

A test setup was developed to evaluate the level of noise mitigation introduced by each of the module architectures. Experimental results are only obtained for the modules introduced in Section 2.3. The designed testbed switches each module as a buck converter operating at a switching frequency of 100 kHz. All experiments are conducted at an input/output voltage of 600/300 V. The setup is comprised of four main subsystems: LISN, input capacitor C_{in}, power module, and output load. Figure 10 shows the simplified schematic of the setup and outlines the aforementioned subsystems. Details of the various components used in each subsystem have been provided in Table 1. Figure 10 also highlights the measurements recorded for analysis: drain-to-source voltage v_{DS} for the high-side switch Q_H, voltage across output load V_{out}, voltage across input capacitor bank V_{in}, current flowing at input of converter i_{in}, noise current that escapes through the module baseplate into the converter i_{bp}, and CM noise current at the input of the converter i_{input}. The noise i_{bp} and i_{input} is measured for all four module architectures using the same test setup and testing conditions with only the modules swapped. The results presented were consistent and repeatable using the test setup described.

The noise current i_{bp} was measured to experimentally quantify the noise generated by the module that escapes through the baseplate into the converter. It was measured using the method described in [38]. To measure i_{bp}, the module baseplate is clamped onto a heatsink that is physically separated from the copper sheet with the help of non-conductive separators. Current flowing through a conducting wire connecting the heatsink and copper sheet is then measured. The noise current i_{input} is measured to empirically verify the effect of changing the module architecture on the noise flowing at the input of the converter. The noise current i_{input} is measured with a high frequency current transformer (HFCT) clamped around the input terminals of the converter.

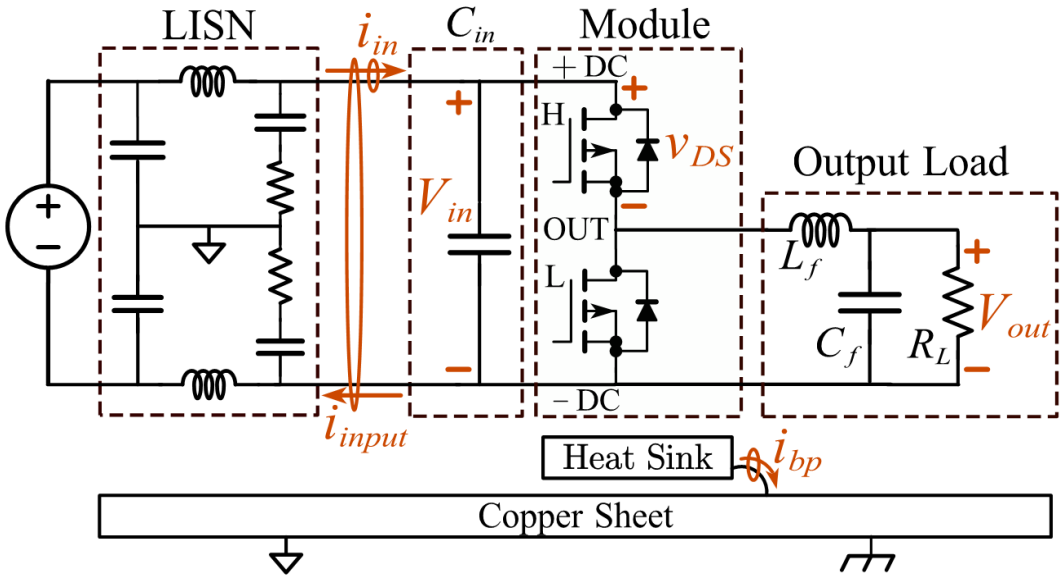


Figure 10: Simplified schematic of EMI test setup for the buck converter.

Table 1: Summary of Setup Specifications

Parameter	Value (Units)
Buck Converter Parameters	
Switching Frequency	100 kHz

V_{in} / V_{out}	600 V / 300 V
Test Setup Parameters	
LISN	LISN LI-1100C
C_{in}	90 µF
C_f	100 µF
L_f	750 µF
R_L	22 Ω
Measurement Probes	
i_{in}, i_{bp}	Tektronix TCP0030A, 120 MHz
i_{input}	ETS-Lindgren 91550–1, 100 MHz
v_{DS}, V_{in} and V_{out}	Tektronix THDP0200, 200 MHz

The testbed was operated at room temperature and all measurements reported were recorded during the electrical steady state. Details of the measurement probes used are provided in Table 1. The analysis in this work is limited to the conducted EMI frequency range (150 kHz to 30 MHz). The measurement probes used were confirmed to have a bandwidth that would allow accurate measurement in the frequency range mentioned. The hardware implementation of the testbed is shown in Figure 11. The copper sheet used in the test setup is connected to earth potential. The time domain measurements for baseplate noise current i_{bp} and input noise current i_{input} were recorded using a rectangular time window of 400 µs, and a sampling frequency of 1.5625 GS/s. The analysis presented is limited to the conducted EMI frequency range, i.e. 150 kHz to 30 MHz.

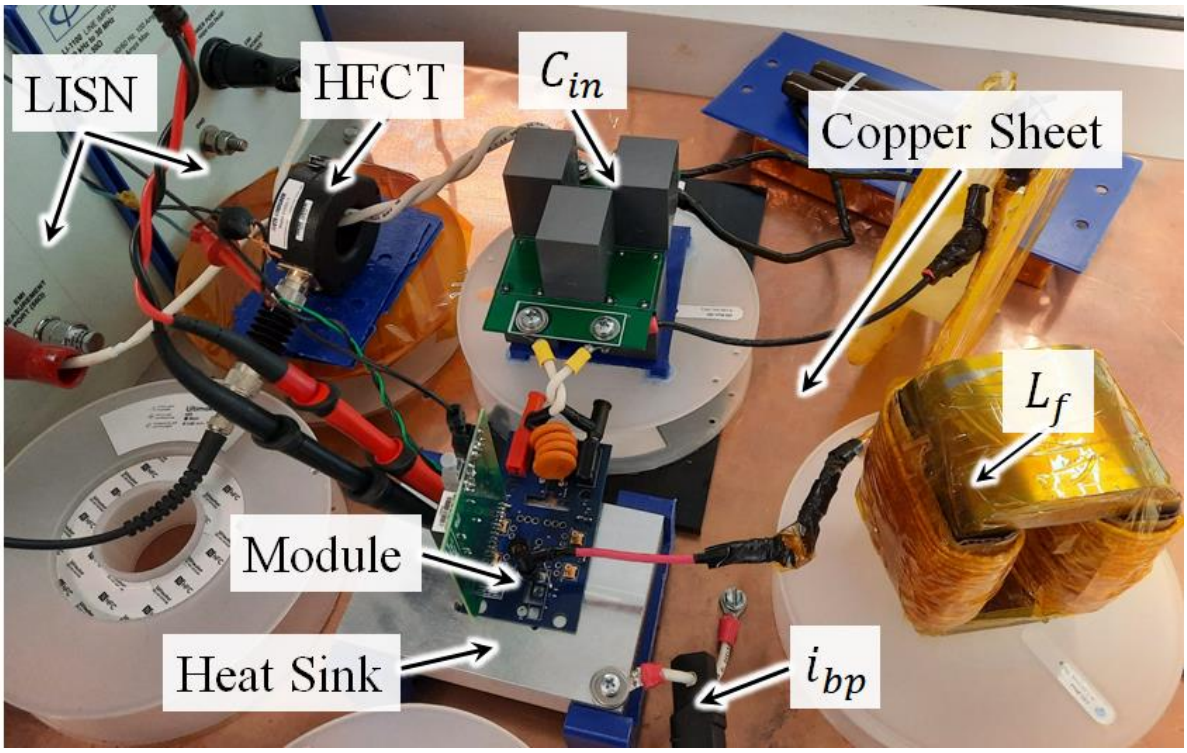


Figure 11: Hardware setup of EMI testbed for buck converter.

3.3 Time Domain Measurement

The relationship between voltage v_{DS}, switching-node capacitance C_{CM}, and generated noise current i_{bp} is explained using the Baseline module architecture shown in Figure 5(a). Figure 12(a) shows the zoomed-in time domain waveform for voltage v_{DS}, and Figure 12(b) shows the noise current i_{bp} being generated at the same instance in time. In the experiments performed, the direction of current is taken as positive if the current is flowing from the heat sink toward the copper sheet, and is taken as negative if it is flowing in the reverse direction.

From Figure 12(a), during the turn-off transient v_{DS} increases to 600 V at a slew rate of 25.6 V/ns. During this event, the change in potential at the OUT terminal discharges parasitic capacitor C_{CM}, causing the current to flow from the module baseplate to the switching-node. During the

voltage transition, a CM current flows from the copper sheet to the OUT terminal, resulting in the discharging of C_{CM} (Figure 12(b)). A negative peak of 2.7 A is observed.

During the turn-on transient v_{DS} falls from 600 V to 0 V at a slew rate of 39.3 V/ns. During this event, the change in potential at the OUT terminal charges parasitic capacitor C_{CM}, causing current to flow from the switching-node to the copper sheet. A positive current peak of 4.1 A is seen during the falling v_{DS} transient in Figure 12. The different current peaks during the rising and falling transitions occur due to different rising and falling slew rates. The turn on transient has a higher *dv/dt*, and hence a larger CM current through the baseplate.

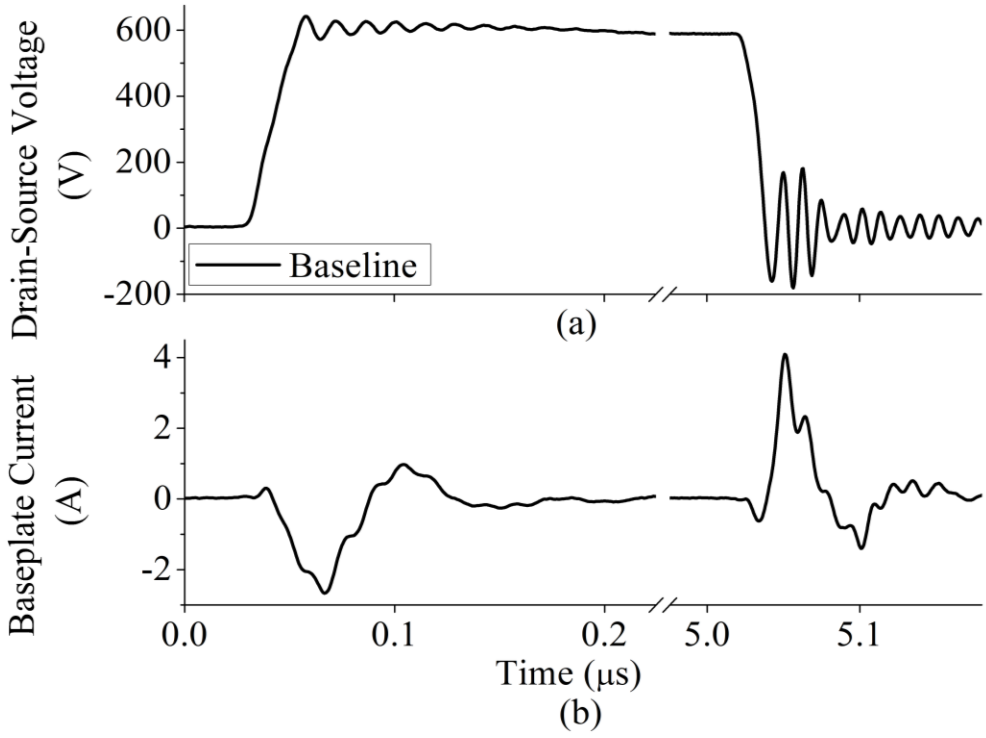


Figure 12: Zoomed-in time domain waveforms for the Baseline module architecture showing (a) high-side SiC MOSFET Q_H drain-source voltage v_{DS} and (b) noise current i_{bp}.

3.4 Baseplate Noise Current

The frequency spectra of the noise current i_{bp} for different module architectures are shown in Figure 13. In Figure 13(a) and (b), the two baseline modules are compared to their CM screen counterpart to observe how integrating a CM screen into the module affects the noise generated at the baseplate. The results confirm that the introduction of the CM screen into the architecture caused noise to be redirected to the respective connected DC node. In both scenarios, a maximum noise reduction of 26 dB is noted, due to the redirection of a portion of noise i_{bp} to the connected DC node. A minimum noise reduction of 21 dB and 26 dB is noted in the 150 kHz – 1.1 MHz frequency range for the Figure 13(a) and Figure 13(b) module, respectively.

In Figure 13(c), the i_{bp} generated by the two CM screen architectures is compared. Results show a maximum mitigation of 13 dB. No significant noise reduction is noted in the 150 kHz to 1.1 MHz frequency range. The mitigation observed can be attributed to the symmetric decoupling capacitances between the DC+ and DC– nodes and the screening layer [43], [57], [58]. This is discussed in more detail later in this thesis. The mitigation seen at frequencies larger than 10 MHz can be linked to the smaller current commutation loop, due to the integrated decoupling capacitors. As previously stated, the power-loop inductance inside the module will reduce from 7.5 nH to 3.5 nH, due to the addition of decoupling capacitors. The measured time domain waveforms for the baseplate noise current of the four module architectures is shown in Figure 14.

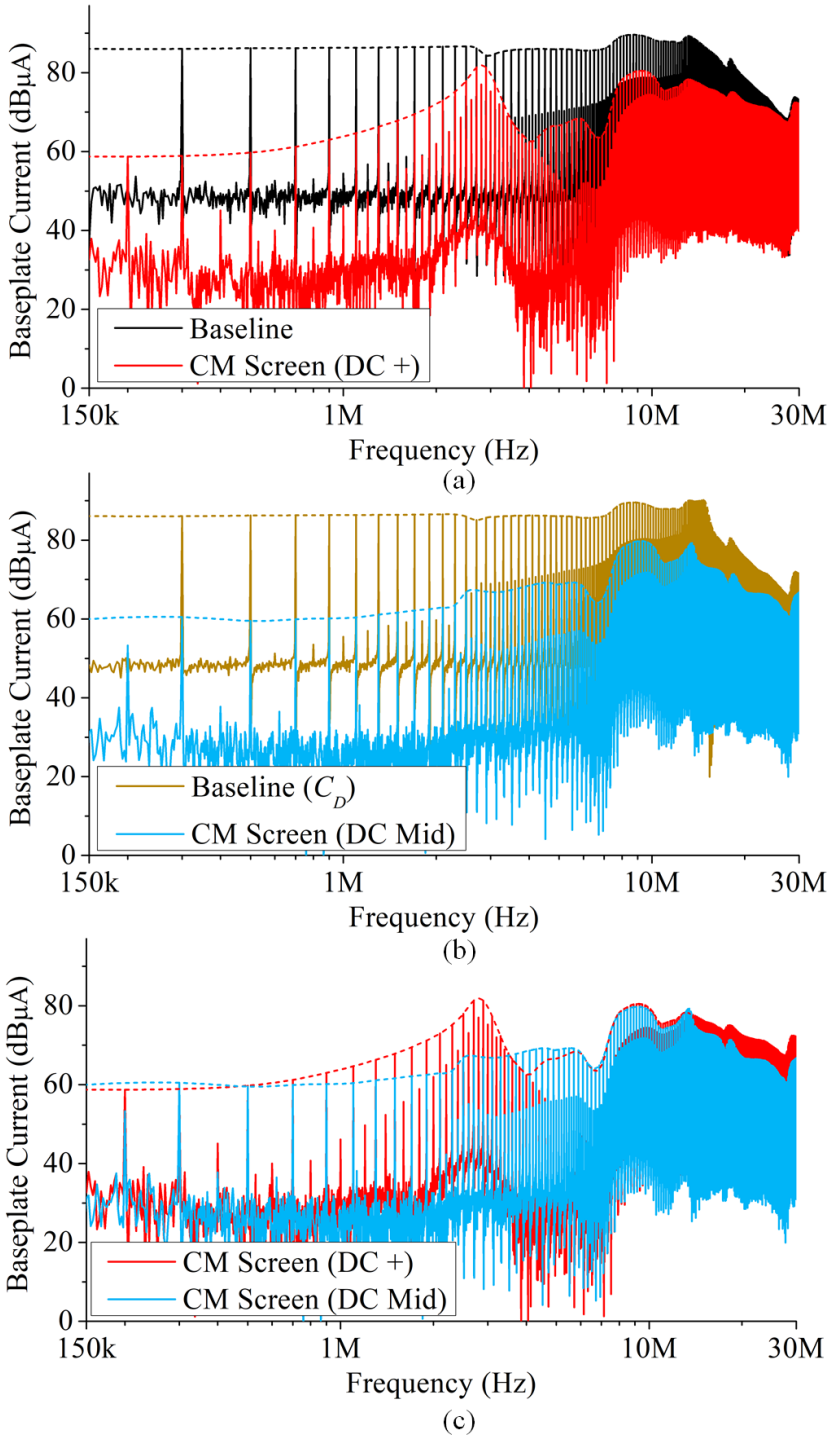


Figure 13: Frequency spectra of noise current i_{bp} for (a) Baseline and CM Screen (DC+) module, (b) Baseline (C_D) and CM Screen (DC Mid) module, and (c) the CM Screen (DC+) and CM Screen (DC Mid) module.

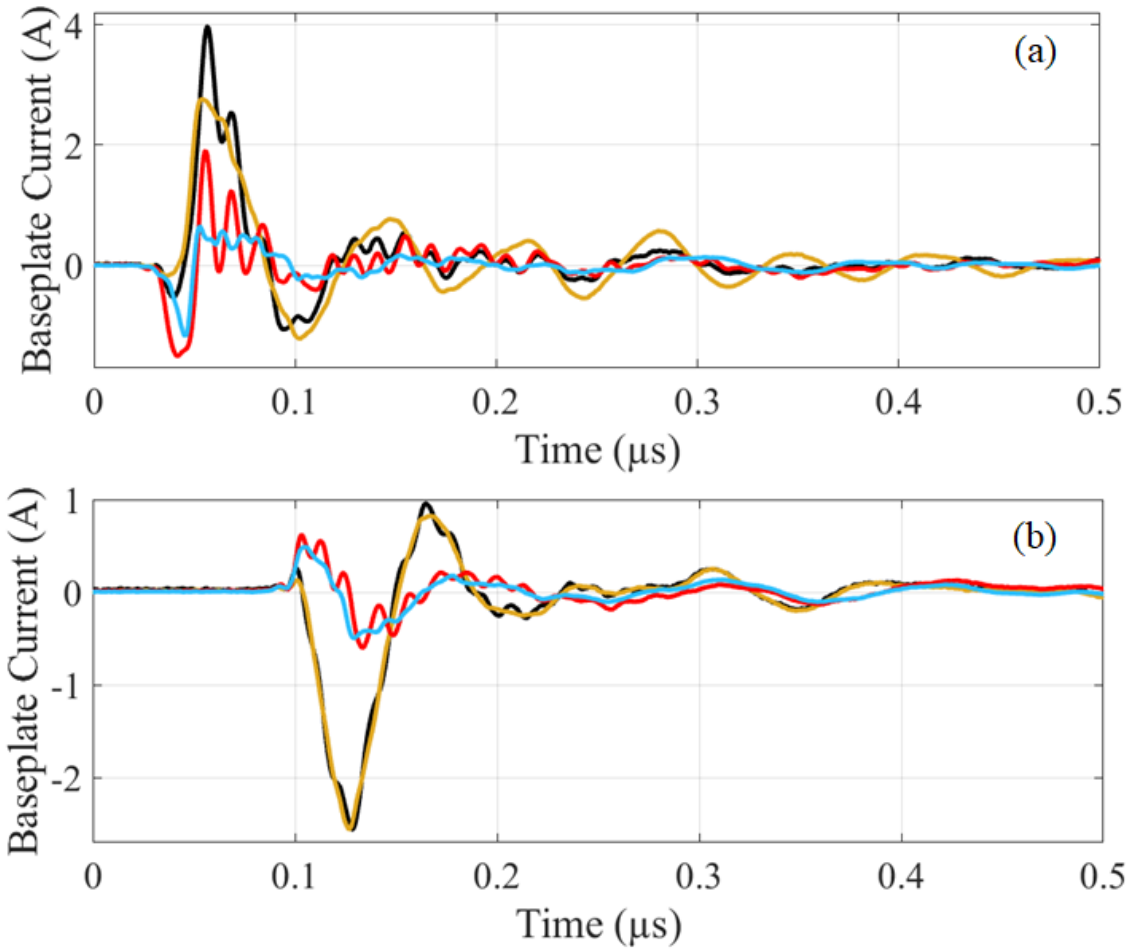


Figure 14: Time domain waveform for i_{bp} during device (a) turn-on and (b) turn-off for module architecture: Baseline (Black), Baseline (C_D) (Brown), CM Screen (DC+) (Red), and CM Screen (DC Mid) (Light Blue).

3.5 Input Noise Current

Similar to the comparison done for i_{bp}, the effect of module architecture on the noise current i_{input} is also investigated. A maximum noise mitigation of 17 dB and 26 dB is observed between the Baseline and CM Screen (DC+) module (Figure 15(a)), and the Baseline (C_D) and CM Screen (DC Mid) module (Figure 15(b)), respectively. A minimum noise reduction of 10 dB is noted in the 150 kHz – 1.1 MHz frequency range for both the comparisons. Larger mitigation is seen in the Baseline (C_D) module and its CM screen counterpart at frequencies greater than 10 MHz.

In Figure 15(c), i_{input} generated by the two CM screen architectures is compared. A maximum mitigation of 18 dB is observed. No significant noise reduction is noted in the 150 kHz – 1.1 MHz frequency range. It is important to note that the noise mitigation seen in i_{input} is different from the mitigation seen in i_{bp}, and that i_{input} has slightly larger magnitudes in the frequency spectrum compared to i_{bp}. The noise current i_{bp} is the noise generated by the module that escapes though the baseplate into the converter and — with the module being the major source of noise generated — is responsible for a significant portion of i_{input}, but not all of it. In particular, noise current i_{input} also incorporates the effect of CM noise generated due to unbalanced impedances inside the converter. Detail on the impact of asymmetries in a buck converter on CM noise generated can be found in [59]. Another example of CM noise that the noise current i_{input} incorporates is the noise flowing through parasitic capacitances outside the module that the converter may have to the copper sheet. The time domain waveform for i_{input} could not be included due to the limitations of the measurement probe used to measure the CM noise at the input of the converter. The high frequency current transformer (ETS-Lindgren 91550–1, 100 MHz) used to measure the noise i_{input} does not output the actual current waveform. Post-processing has to be done in frequency domain — as detailed in the documentation of the probe — before the actual frequency spectrum of i_{input} can be observed.

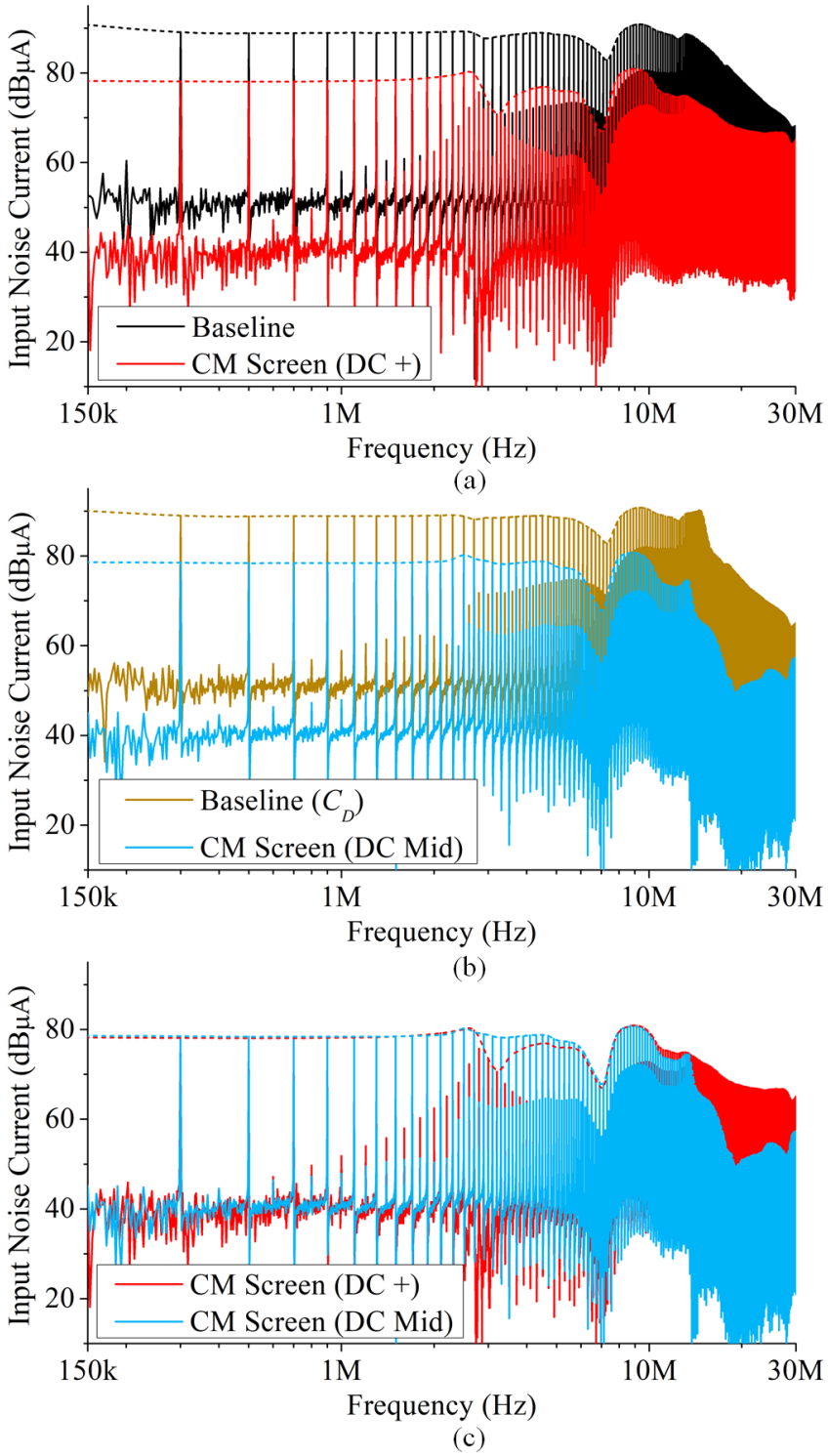


Figure 15: Frequency spectra of noise current i_{input} for (a) Baseline and CM Screen (DC+) module, (b) the Baseline (C_D) and CM Screen (DC Mid) module, and (c) CM Screen (DC+) and CM Screen (DC Mid) module.

3.6 Preliminary Efficiency and Switching Results

The impact of the CM screen architectures on converter efficiency and device slew rates was also investigated. The slew rates for the modules were measured across the drain-to-source voltage v_{DS} for MOSFET Q_H. The efficiency and slew rate measurements were made using a rectangular time window of 800 µs, with a sampling frequency of 6.25 GS/s. The output from the measurement probes i_{in} and V_{in}/V_{out} were measured using probes of bandwidth 20 MHz and 5 MHz, respectively. The efficiency measurements were made a total of five times and the median value is reported in the analysis. The slew rates were measured using probes of bandwidth 250 MHz. Table 2 lists the converter efficiencies and slew rates for each module variation. The efficiencies are reported as a percentage increase and decrease, while keeping the Baseline module as a reference. Comparing the efficiency of the Baseline module to the CM Screen (DC+) module, a decrease of 0.3 % is seen. This decrease in efficiency can be attributed to the increased C_{oss} of the module. Having the CM screen shorted with the DC+ node results in C_{CM} being in parallel with the C_{oss} of the SiC die, thereby increasing the output capacitance of the high-side switch.

Compared to the Baseline module, the Baseline (C_D) and CM Screen (DC Mid) show an increase in efficiency. This increase can be explained by investigating the trends observed in the slew rates in Table 2. The Baseline (C_D) module shows a 47% larger falling slew rate. This increased slew rate can be attributed to the reduced current commutation loop that occurs due to the addition of the decoupling capacitors. Similarly, the CM Screen (DC Mid) module demonstrates a 59% faster falling slew rate. The shorter turn-on time results in lower switching losses and, therefore, an increase in the overall efficiency of the converter. The rising and falling edges for the module architectures are showing in Figure 16.

Table 2: Switching Characteristics and Efficiency

Module Architecture	Converter Efficiency w.r.t Baseline Module	Slew Rate (V/ns)	
		Rising	Falling
Baseline	N.A.	25.6	39.3
Baseline (C_D)	0.2% increase	27.1	57.9
CM Screen (DC+)	0.3% decrease	24.9	41.4
CM Screen (DC Mid)	0.5% increase	25.3	62.3

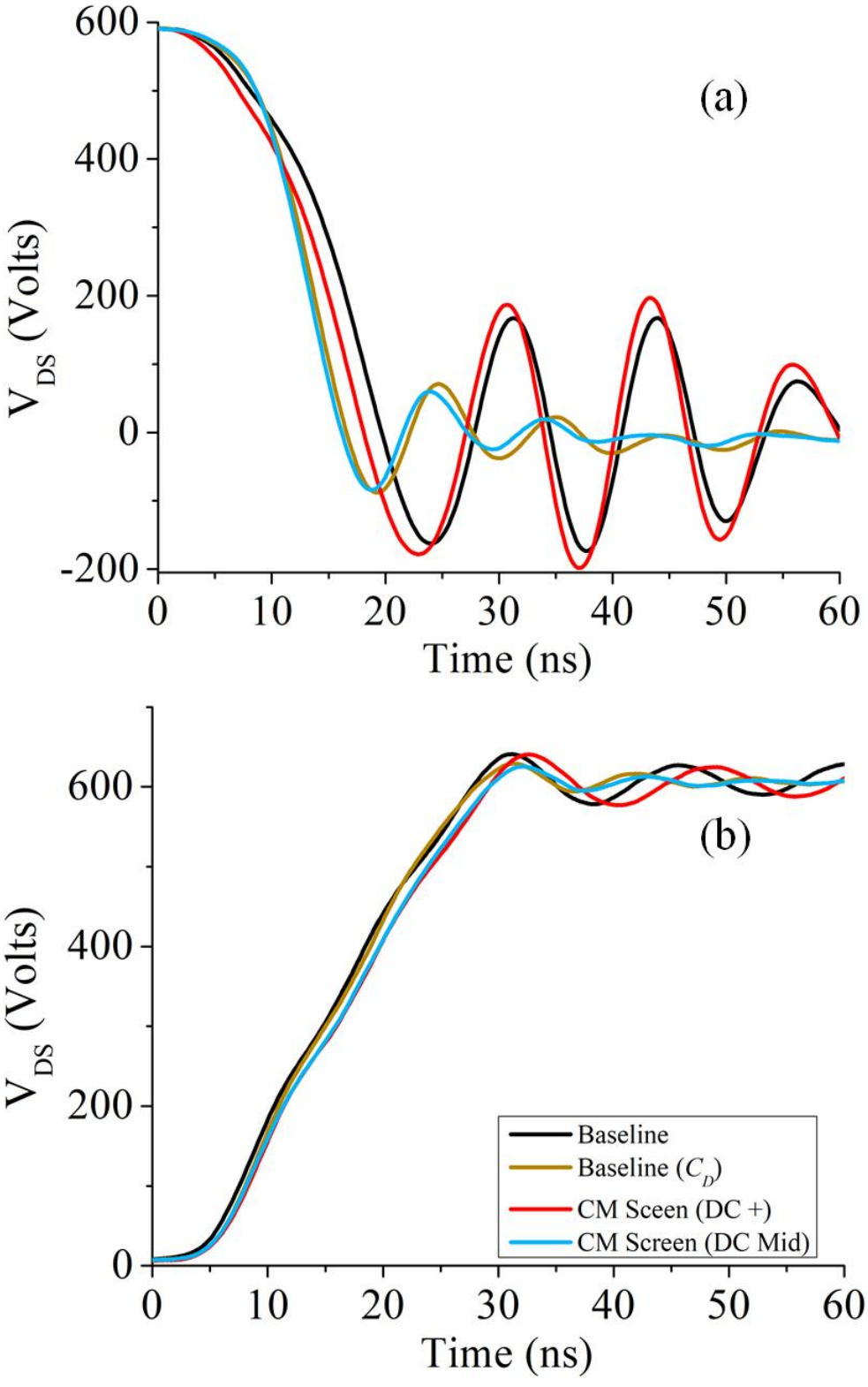


Figure 16: Switching Characteristics (a) Falling Edge (b) Rising Edge

Chapter 4: Simulation and Modeling Techniques

4.1 Introduction

The chapter introduces the simulation and modeling techniques that can be used to explain the EMI results discussed in the previous chapter. The simulation and modeling techniques that were primarily chosen are the: time domain simulation, CM equivalent modeling, and substitution and superposition theorem.

4.2 Time Domain Simulation

Based on the hardware results presented in Figure 13, a simulation model was created for the test setup. Figure 17(a) shows the simulation model with the Baseline module. In Figure 17(a), Z_{Cin} and $Z_{C_{PCB}}$ are the total impedances of the input capacitor bank C_{in} and the decoupling capacitors C_{PCB}, installed on the PCB board used to interface the module with the rest of the converter. The impedances Z_{Cin} and $Z_{C_{PCB}}$ incorporate the equivalent series inductance (ESL) and equivalent series resistance (ESR) of the capacitors. The impedances Z_{Jx} where $x = \{1 - 6\}$ represent the parasitic impedances of the wires connecting the LISN to Z_{Cin}, Z_{Cin} to $Z_{C_{PCB}}$, and of the PCB interfacing $Z_{C_{PCB}}$ to the module architecture.

The impedances Z_{H1} and Z_{H2} are the parasitic impedances of the wire connecting the heat sink to the copper sheet, and of the copper sheet used in the EMI test setup. The capacitance C_{H1} is the parasitic capacitance between the heat sink raised through non-conductive separators and the copper sheet. Estimates of these impedances were obtained using the methodology detailed in [60] with an Agilent 4294A precision impedance analyzer. The simulated noise current i_{bp} is the current flowing through the impedance Z_{H1}. The impedances Z_{Jy} where $y = \{7 - 11\}$ model the

parasitic inductances and resistances inside the module. Capacitances C_{DC+}, C_{DC-}, and C_{CM} are the parasitic capacitances the DC+, DC–, and OUT terminal (Figure 4) have to the baseplate from across the DBC substrate. Estimates of the values of Z_{Jy} were extracted using ANSYS Q3D, whereas C_{DC+}, C_{DC-}, and C_{CM} were measured with the impedance analyzer. The SiC device LTspice model provided by the manufacturer was used for the simulation. The values used for these parameters are shown in Table 3. It should also be noted that the impedances Z_{Jx} (where $x \in 1,2,3 \ldots$, shown in Figure 17(a)) relate to the resistances R_{Jx} and inductances L_{Jx} (shown in Table 5) according to:

$$Z_{Jx} = R_{Jx} + j\omega L_{Jx} \tag{8}$$

The impedances Z_{Cin} and $Z_{C_{PCB}}$ (shown in Figure 17(a)) relate to the parameters shown in Table 3 according to:

$$Z_{Cin} = ESR_{C_{in}} + j\omega ESL_{C_{in}} + \frac{1}{jwC_{in}} \tag{9}$$

$$Z_{C_{PCB}} = ESR_{PCB} + j\omega ESL_{PCB} + \frac{1}{j\omega C_{PCB}} \tag{10}$$

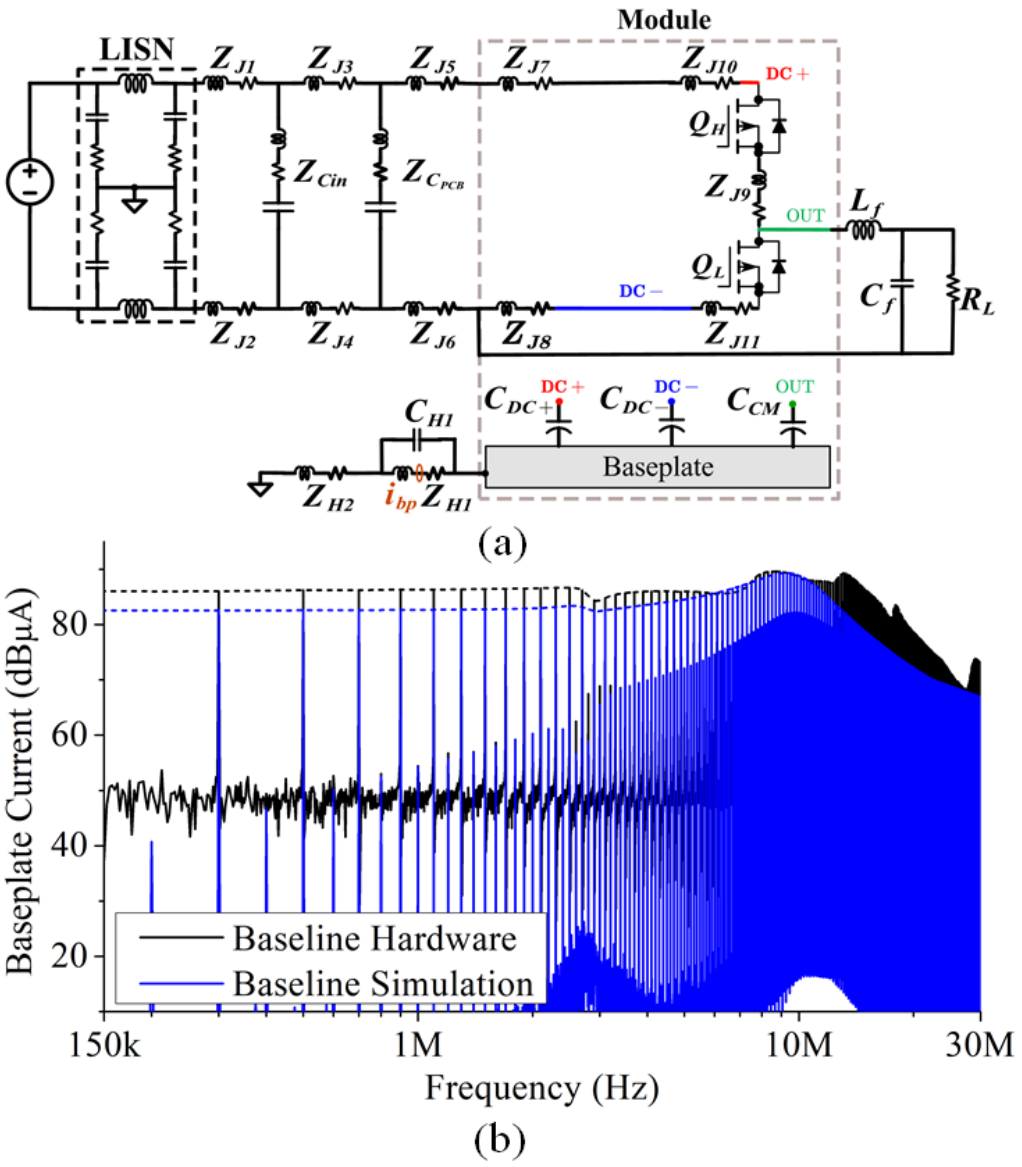


Figure 17: (a) Simulation model of test setup with the Baseline module architecture (b) Comparison of the hardware (Black) and simulation (Blue) results for the frequency spectra of noise current i_{bp} for the Baseline module.

Table 3: Summary of Simulation Parameters

Parameter	Value (Units)	Parameter	Value (Units)
$Q_1 and\ Q_2$	CPM2-1200-0040B	LISN	CISPR Standard
C_{in}	93.6 μF	$ESR_{C_{in}}$	15.59 mΩ

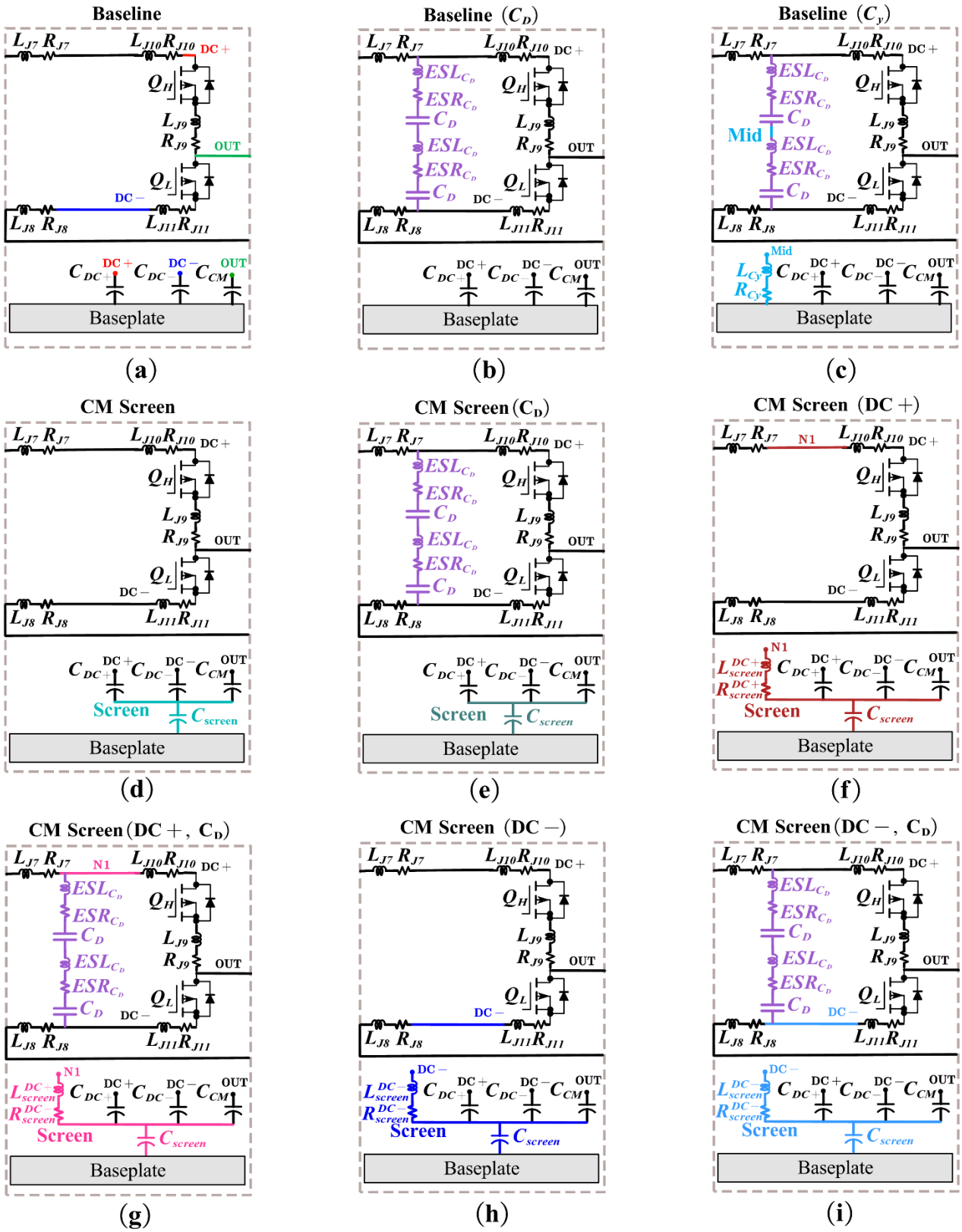
$ESL_{C_{in}}$	1 nH	C_{PCB}	34 nF
ESL_{PCB}	5.6 nH	ESR_{PCB}	35.42 mΩ
L_{j1}	120.78 nH	R_{j1}	150 mΩ
L_{j2}	167.48 nH	R_{j2}	180 mΩ
L_{j3}	24.47 nH	R_{j3}	80 mΩ
L_{j4}	52.47 nH	R_{j4}	80 mΩ
L_{j5}	8 nH	R_{j5}	82 mΩ
L_{j6}	3 nH	R_{j6}	180 mΩ
L_F	750 µH	C_f	100 µF
R_L	22.1 Ω	C_{H1}	6.36 pF
L_{H1}	105 nH	R_{H1}	10 mΩ
L_{H2}	650 nH	R_{H2}	0.5 Ω

In Figure 17(b), the hardware and simulation results for the Baseline module is compared. The frequency spectrum is obtained by running the time domain simulation, followed by the fast Fourier transform (FFT). Between 150 kHz to 10 MHz, a maximum difference of 4 dB was observed in the frequency spectrum. Beyond 10 MHz, the ability of the simulation to predict the noise magnitude decreases and a maximum difference of 10 dB was observed. This is a result of using linear, lumped circuit elements to model parasitics inside the converter and the module, and

the die model used not being accurate at high frequencies [61]–[63]. However, although the ability of the simulation to predict the noise magnitude decreases beyond 10 MHz, Figure 17(b) shows that the model reasonably predicts trends seen in the frequency spectrum: a relatively flat frequency spectrum until the frequency of ~9.9 MHz, beyond which a roll-off is observed.

Similar to the Baseline module, simulation models for the remaining eleven modules were also built. The simulation models for the twelve module architectures are shown in Figure 18. The values for various parasitics are shown in Table 4. Figure 18(a)-(c) shows the three baseline architectures: Baseline, Baseline (C_D), and Baseline (C_y). Figure 18(b) differs from Figure 18(a) in that the decoupling capacitors C_D (along with the equivalent series resistance ESR and inductance ESL) have been integrated into the module architecture. Figure 18(c) differs from the other two baseline architectures in that the baseplate is shorted to the DC mid node created by the series connection of the decoupling capacitors.

Figure 18(d)-(l) shows the nine different CM screen module architectures studied. The module architectures primarily differ based on what node the CM screen is connected to and whether the architecture has decoupling capacitors. In Figure 18(d) and (e) the CM screen is left floating. CM Screen (C_D) (Figure 18(e)) differs from the CM Screen (Figure 18(d)) in that the decoupling capacitors C_D (along with the equivalent series resistance ESR and inductance ESL) have been integrated into the module architecture.


Baseline
Baseline (C_D)
Baseline (C_y)
CM Screen
CM Screen (C_D)
CM Screen (DC +)
CM Screen (DC +, C_D)
CM Screen (DC −)
CM Screen (DC −, C_D)
DC +
DC −
OUT
N1
Mid
Screen
Baseplate
(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(i)

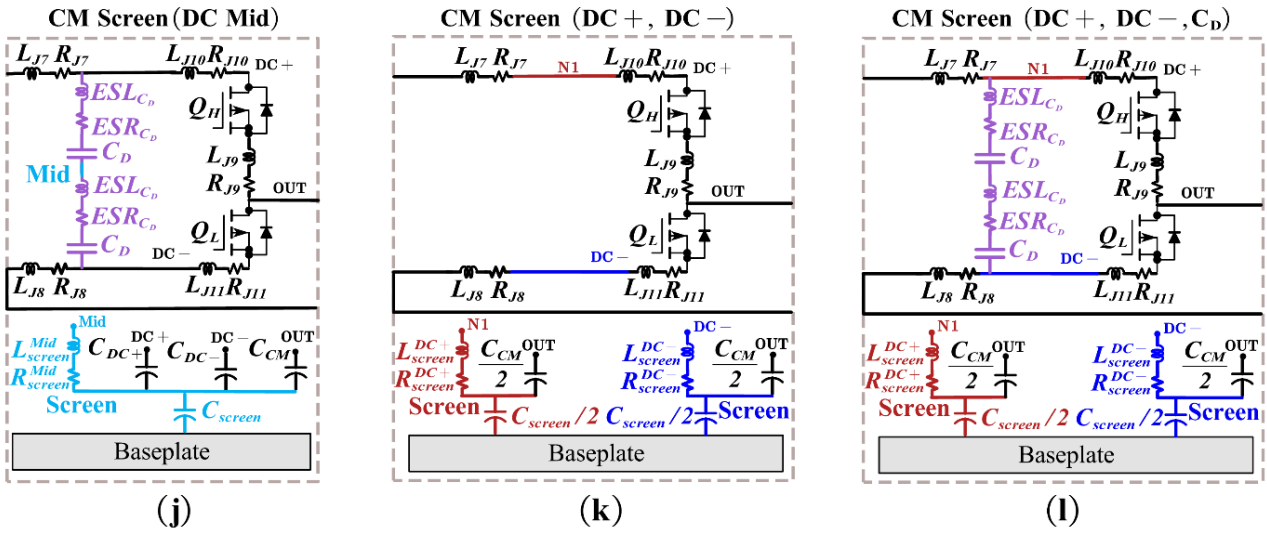


Figure 18: Simulation schematic of the twelve module architectures explored.

Table 4: Summary of Module Architecture Parameters

Parameter	Value (Units)	Parameter	Value (Units)
C_D	14.56 nF	L_{J9}	3.7 nH
ESR_{C_D}	9.9 mΩ	R_{J9}	8 mΩ
ESL_{C_D}	0.25 nH	L_{J10}	3 nH
C_{DC+}	166.3 pF	R_{J10}	8 mΩ
C_{DC-}	24 pF	L_{J11}	3.1 nH
C_{Mid}	35.71 pF	R_{J11}	7.5 mΩ
C_{CM}	80.2 pF	L_{J12}	1 nH
C_{screen}	436.9 pF	L_{screen}^{DC+} and L_{screen}^{DC-}	3.35 nH

		R_{screen}^{DC+}	
L_{J7}	1 nH	and R_{screen}^{DC-}	5 mΩ
		L_{Cy}	1 nH
R_{J7}	8 mΩ	and L_{screen}^{Mid}	
		R_{Cy}	
L_{J8}	1 nH	and R_{screen}^{Mid}	2.25 mΩ
		$C_{DC+}^{Baseline}$	
R_{J8}	7.5 mH	and $C_{DC+}^{CM\ Screen}$	202 pF

The schematics shown in Figure 18(f)-(i) differ from one another based on whether the screen is connected to a positive or negative DC node (labelled N1 or DC-) and whether decoupling capacitors C_D (along with the equivalent series resistance ESR and inductance ESL) have been integrated into the module. Figure 18(j) shows a CM screen module in which the screen is connected to the Mid node, a DC node created by the series connection of the decoupling capacitors C_D. Figure 18(k) and (l) show module architectures in which the screening layer below the switching node OUT has been split into two halves. Half the screening layer is connected to a positive DC node N1 and the other half is connected to a negative DC node DC-. The schematics in Figure 18(k) and (l) differ from one another based on the addition of decoupling capacitors. It should again be noted that although in Figure 18(e), (g), (i) and (l) a Mid node has been created by the series connection of the decoupling capacitors, this has been done for the sake of uniformity in

the module architecture and to facilitate ease of understanding. The Mid node is not needed for these module architectures and a single decoupling capacitor can also be used.

In Figure 19(a), the hardware and simulation results for the Baseline and Baseline (C_D) modules are compared. Between 150 kHz to 10 MHz, a maximum difference of 4 dB was observed in both frequency spectrums. Beyond 10 MHz, a maximum difference of 13 dB was observed for the Baseline and Baseline (C_D) modules. Although the accuracy of the simulation has decreased beyond 10 MHz, it can be seen from Figure 19(a) that the model can predict the trends seen in the frequency spectrum accurately: (1) a relatively flat frequency spectrum is seen until the frequency of ~9.9 MHz, beyond which a roll-off is observed, and (2) a change in the slope of the roll-of occurring at ~13.5 MHz.

In Figure 19(c) and (d) the hardware and simulation results for the CM Screen (DC+) and CM Screen (DC Mid) modules are compared. Results show that between 150 kHz to 4 MHz for the CM Screen (DC+) module, and 150 kHz to 7 MHz for the CM Screen (DC Mid) module; a maximum difference of 12 dB was observed between the hardware and simulation results. From 4 MHz to 7 MHz a maximum difference of 17 dB, and beyond 7 MHz a maximum difference of 14 dB is observed for the CM Screen (DC+) module between the hardware and simulation. The CM Screen (DC Mid) module shows a maximum difference of 20 dB from 7 MHz to 18 MHz between the hardware and simulation results. Similar to the baseline architectures, although the simulation was not able to predict the magnitudes of the frequency spectrum with high fidelity, the model was able to imitate the trends seen with reasonable accuracy: (1) the peak in the frequency spectrum at ~2.7 MHz, (2) the roll-off frequency beginning at a frequency of ~8.29 MHz, and (3) a change in the slope of the roll-of occurring at ~13.5 MHz for the CM Screen (DC Mid) module.

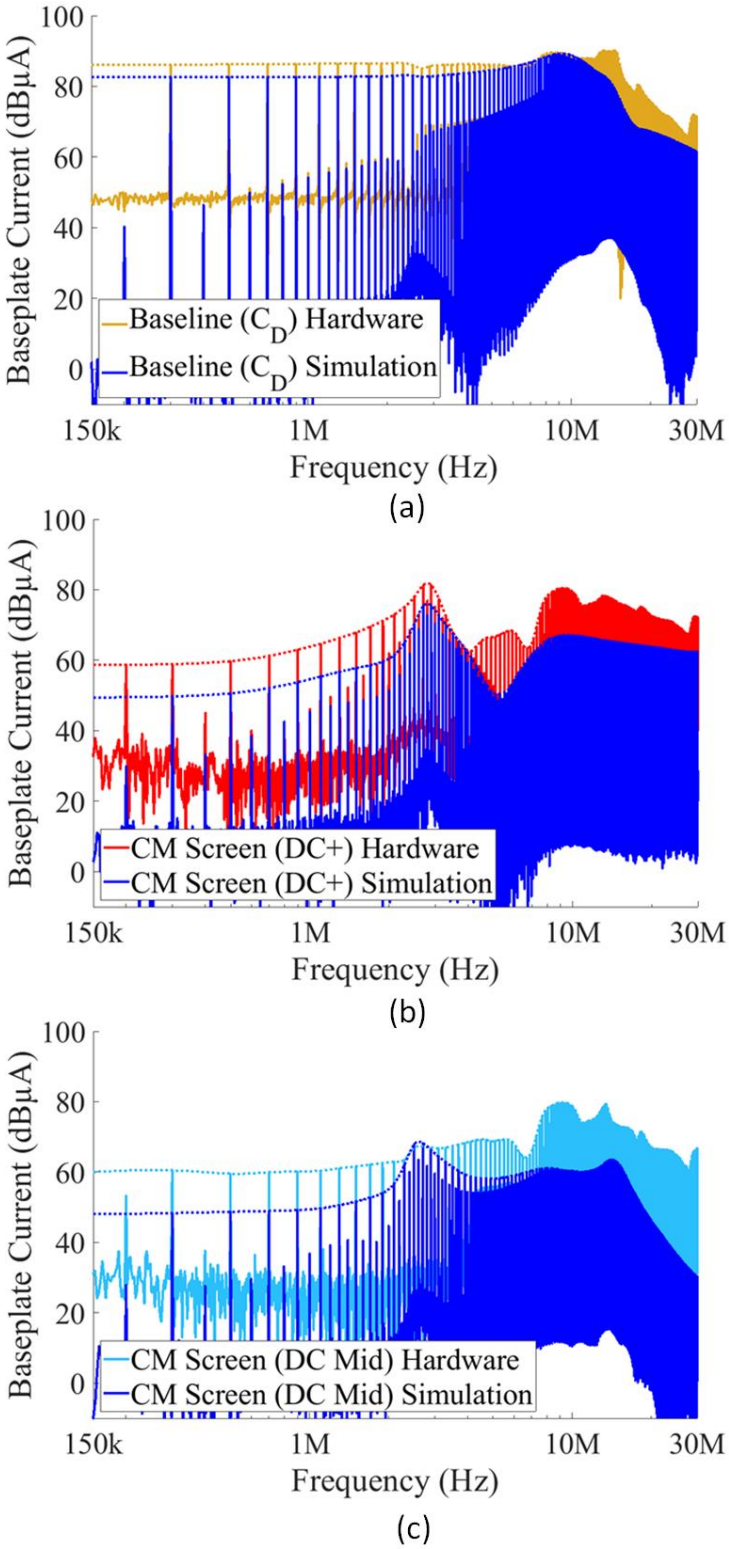


Figure 19: Comparison of the hardware and time domain simulation results for the frequency spectra of noise current i_{bp} for (a) the Baseline (C_D), (b) the CM Screen (DC+) and (c) CM Screen (DC Mid) modules.

The frequency spectra of the noise current i_{bp} for the four experimentally tested module architectures are compared through simulation in Figure 20. In Figure 20(a) and (b), the two baseline modules are compared to their CM screen counterparts, similar to Figure 13(a) and (b). In both scenarios, a maximum noise reduction of 35 dB is noted, which is a 35% increase compared to the hardware results. In Figure 20(c), the i_{bp} generated by the two CM Screen architectures is compared. Although hardware results showed a maximum mitigation of 13 dB between 2.7 MHz and 2.9 MHz, the simulation results show a maximum mitigation of 9 dB, a 30% decrease. The simulation also predicts a high level of mitigation with the CM Screen (DC Mid) module at frequencies larger than 13.5 MHz. It can again be observed that the simulation was not able to predict the mitigation magnitudes in the frequency spectrum with high fidelity: an error of upto 35%; however, the simulation was able to imitate the mitigation trends seen in Figure 13 with reasonable accuracy. For example, in Figure 20(c), the CM Screen (DC+) and CM Screen (DC Mid) modules show similar mitigation trends in the frequency spectrums in the 150 kHz to 500 kHz frequency range. Similarly, the peak in the frequency spectrum at ~2.7 MHz for the CM Screen (DC+) module slightly shifts to a lower frequency for the CM Screen (DC Mid) module. A change in slope in the frequency spectrum of the CM Screen (DC Mid) module at ~13.5 MHz is also predicted by the simulation resulting in the module having lower EMI compared to the CM Screen (DC+) module. The justification for why these trends occur will be presented in Chapter 5. Any prediction about noise mitigation between module architectures made by the LTspice simulation below 10 MHz will be assumed to have an error of 35%.

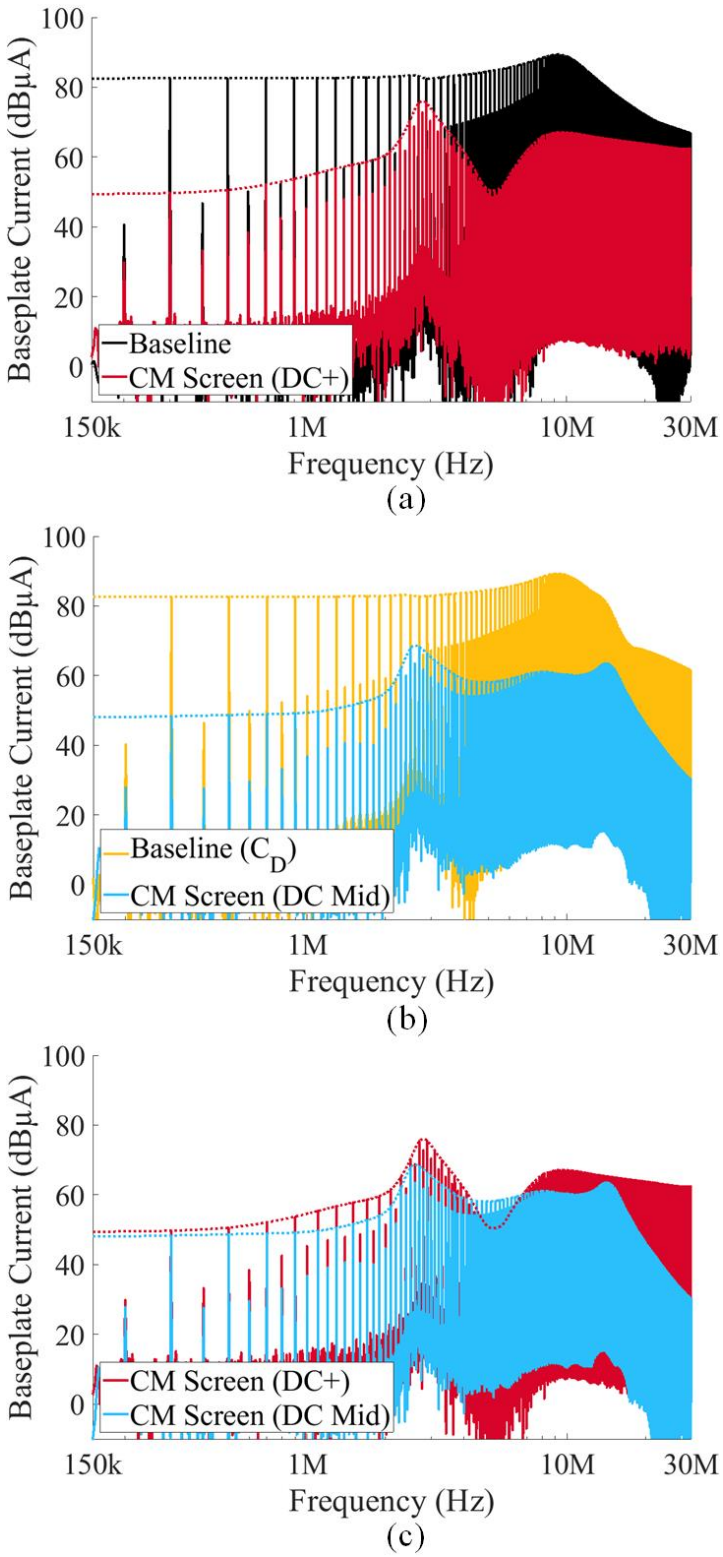


Figure 20: Frequency spectra of noise current i_{bp} from simulation for (a) the Baseline and CM Screen (DC+) modules, (b) the Baseline (C_D) and CM Screen (DC Mid) modules, and (c) the CM Screen (DC+) and CM Screen (DC Mid) modules.

4.3 Common Mode Equivalent Modeling

A common mode equivalent model (CEM) for the test setup is now derived. Since the time domain simulation model in Figure 17(a) is a good approximation of the experimental test setup, the CEM for the simulation model is derived, using the methodology presented in [39], [59], [64].

4.3.1 Two Parallel Wires with Asymmetric Impedances

To derive the CEM of the test setup schematic, the CEM equations of two parallel wires with asymmetric impedances is first derived using the methodology presented in [59]. Two parallel wires with asymmetric impedances are shown in Figure 21(a). The system of equations that define the circuit schematic shown in Figure 21(a) is:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_1 & 0 \\ 0 & Z_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{11}$$

Using the transform definitions for T_N^i and T_N^v and the methodology detailed in [59], the system of equations (11) is decomposed into a system of differential mode (DM) and CM equations. From [59], the linear transformation matrices T_N^i and T_N^v can be expressed as (12) and (13):

$$\boldsymbol{T}_N^i = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 \end{bmatrix} \tag{12}$$

$$\boldsymbol{T}_N^v = \begin{bmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{13}$$

Decomposing system of equations (11) by making substitution $i_\alpha = \left(T_N^i\right)^{-1} i_{DCM}$ for line currents and left multiplying by T_N^v, system of equations (14) is obtained:

$$\begin{bmatrix} v_{12} \\ v_{CM} \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} Z_1 & 0 \\ 0 & Z_2 \end{bmatrix} \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} i_{12} \\ i_{CM} \end{bmatrix} \tag{14}$$

Solving and simplifying system of equations (14), system of equations (15) is obtained:

$$\begin{bmatrix} V_{12} \\ V_{CM} \end{bmatrix} = \begin{bmatrix} Z_1 + Z_2 & \frac{Z_1 - Z_2}{2} \\ \frac{Z_1 - Z_2}{2} & \frac{Z_1 + Z_2}{4} \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{CM} \end{bmatrix} \tag{15}$$

System of equations (15) be also written as system of equations (16):

$$\begin{bmatrix} i_{12} \\ i_{CM} \end{bmatrix} = \begin{bmatrix} Z_1 + Z_2 & \frac{Z_1 - Z_2}{2} \\ \frac{Z_1 - Z_2}{2} & \frac{Z_1 + Z_2}{4} \end{bmatrix}^{-1} \begin{bmatrix} V_{12} \\ V_{CM} \end{bmatrix} \tag{16}$$

System of equations (16) can be simplified to (17):

$$\begin{bmatrix} i_{12} \\ i_{CM} \end{bmatrix} = \begin{bmatrix} \frac{Z_1 + Z_2}{4Z_1Z_2} & \frac{-Z_1 + Z_2}{2Z_1Z_2} \\ \frac{-Z_1 + Z_2}{2Z_1Z_2} & \frac{Z_1 + Z_2}{Z_1Z_2} \end{bmatrix} \begin{bmatrix} V_{12} \\ V_{CM} \end{bmatrix} \tag{17}$$

Extracting the second row from system of equations (17), equation (18) is obtained:

$$i_{CM} = \frac{-Z_1 + Z_2}{2Z_1Z_2} V_{12} + \frac{Z_1 + Z_2}{Z_1Z_2} V_{CM} \tag{18}$$

Equation (18) can be rewritten as (19) and (20):

$$V_{CM} = \frac{Z_1Z_2}{Z_1 + Z_2} i_{CM} + \frac{Z_1 - Z_2}{2Z_1 + Z_2} V_{12} \tag{19}$$

$$V_{CM} = \frac{Z_1Z_2}{Z_1 + Z_2} i_{CM} + \frac{Z_1 - Z_2}{2Z_1 + Z_2} (V_{in} - V_{out}) \tag{20}$$

$$V_{CM} = \frac{Z_1 Z_2}{Z_1 + Z_2} i_{CM} + k_0 (V_{in} - V_{out}) \tag{21}$$

where k_0 is a constant. The CEM associated with equation (20) is shown in Figure 21(b). Using the CEM derived in Figure 21(b), the CEM of the rest of the test setup can be derived.

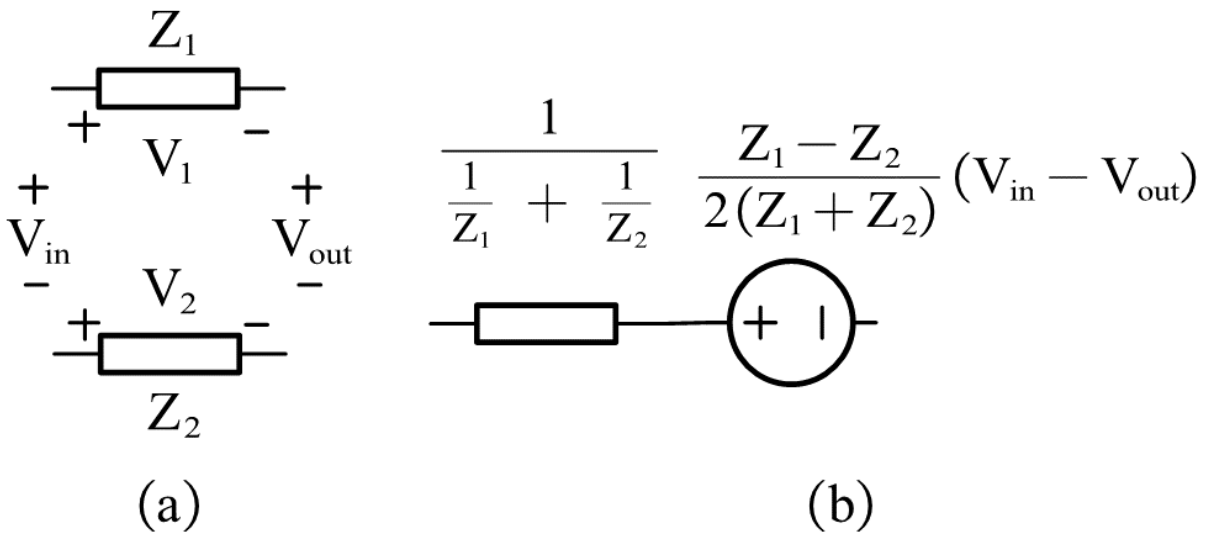


Figure 21: (a) Parallel wires with asymmetric impedances (b) CEM of parallel wires with asymmetric impedances

4.3.2 Module Architectures

The derivation of the CEM of the generalized module architecture is now shown. Figure 22(a) shows a generalized module architecture that can be used to derive the CEM of the twelve-module architecture shown in Figure 18. The generalized module architecture is partitioned as shown in Figure 22(b). An arbitrary point 'p' is selected, and voltages across the switching devices Q_H and Q_L are defined with respect to the arbitrary point 'p'. In Figure 22(b), voltages V_{1p}, V_{2p}, and V_{3p} are the voltages at the DC+, DC-, and OUT terminals of the modules with respect to point 'p'. The MOSFETs Q_H and Q_L in Figure 22(a) are then replaced with voltage potentials V_{1p}, V_{2p}, and V_{3p} such that V_{1p} - V_{2p} and V_{2p} - V_{3p} is the equivalent terminal voltage of the dies during operation of the converter. The DC+, DC-, and OUT terminals of the module can also be referred

to as nodes 1, 2, and 3. The impedance $Z_{\alpha s}$ where α ∈ [1,2,3] is the impedance each node α has to the shielding layer, and $Z_{\alpha h}$ is the impedance each node has to the baseplate that has been shorted to the heatsink. $Z_{\alpha m}$ is the impedance each node α has to a mid-node 'm' that is connected to the screening layer through an impedance Z_{ms}. The current i_{α} where α ∈ [1,2,3] is the noise current that flows into the respective node DC+, DC-, and OUT due to the voltages V_{1p}, V_{2p}, and V_{3p}. The portion of the current i_{α} that flows through the impedance $Z_{\alpha s}$ is referred to as $i_{\alpha s}$, and the portion that flows through the impedance $Z_{\alpha h}$ is referred to as $i_{\alpha h}$. The current $i_{\alpha m}$ refers to the current flowing from the respective node α to the mid node 'm' through impedance $Z_{\alpha m}$.

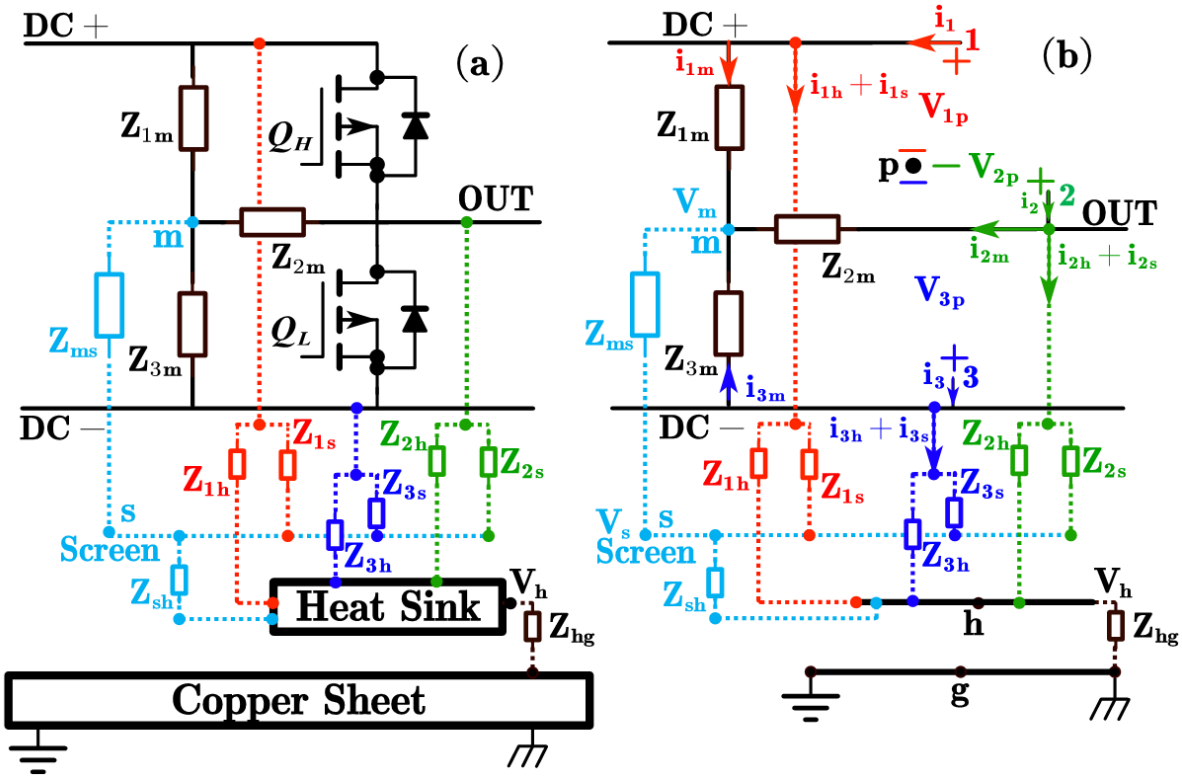


Figure 22: (a) Generalized module architecture with generalized impedances (b) partitioning the module architecture for equivalent circuit model derivation

In Figure 22(b), the voltage V_{hg} — voltage at the heats sink (node 'h') with respect to the copper sheet (node 'g') — can be written as:

$$V_{hg} = Z_{hg}[1 \quad 1 \quad 1]\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{22}$$

Similarly, from Figure 22(b) the voltage V_{sh} — voltage at the screen (node 's') with respect to the heat sink (node 'h') — can be written as:

$$V_{sh} = Z_{sh}(i_{1m} + i_{2m} + i_{3m} + i_{1s} + i_{2s} + i_{3s}) \tag{23}$$

Since $i_\alpha = i_{\alpha m} + i_{\alpha s} + i_{\alpha h}$, equation (23) can be rewritten as (24):

$$V_{sh} = Z_{sh}(i_1 + i_2 + i_3 - i_{1h} - i_{2h} - i_{3h}) \tag{24}$$

However, from Figure 22(b), it can be seen that the currents $i_{\alpha h}$ and current $i_{\alpha s}$ can also be described as shown in (25) and (26):

$$i_{\alpha h} = \frac{V_{\alpha p} + V_{pg} - V_{hg}}{Z_{\alpha h}} \tag{25}$$

$$i_{\alpha s} = \frac{V_{\alpha p} + V_{pg} - V_{sh} - V_{hg}}{Z_{\alpha s}} \tag{26}$$

Replacing equation (22) and (25) into (24), equation (27) can be obtained:

$$\begin{aligned} V_{sh} = (Z_{sh})\left(1 + \frac{Z_{hg}}{Z_{1h}} + \frac{Z_{hg}}{Z_{2h}} + \frac{Z_{hg}}{Z_{3h}}\right)[1 \quad 1 \quad 1]\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \\ -(Z_{sh})\begin{bmatrix} \frac{1}{Z_{1h}} & \frac{1}{Z_{2h}} & \frac{1}{Z_{3h}} \end{bmatrix}\begin{bmatrix} V_{1p} + V_{pg} \\ V_{2p} + V_{pg} \\ V_{3p} + V_{pg} \end{bmatrix} \end{aligned} \tag{27}$$

Similar to voltage V_{hg} and V_{sh}, the voltage V_{ms} — voltage at mid node 'm' with respect to the screen (node 's') — can be written as:

$$V_{ms} = Z_{ms}(i_{1m} + i_{2m} + i_{3m}) \tag{28}$$

Since $i_\alpha = i_{\alpha m} + i_{\alpha s} + i_{\alpha h}$, equation (23) can be rewritten as (29):

$$V_{ms} = Z_{ms}(i_1 + i_2 + i_3 - i_{1h} - i_{2h} - i_{3h} - i_{1s} - i_{2s} - i_{3s}) \tag{29}$$

Using equation (24), equation (29) can be simplified into equation (30):

$$V_{ms} = Z_{ms}\left(-i_{1s} - i_{2s} - i_{3s} + \frac{V_{sh}}{Z_{sh}}\right) \tag{30}$$

Replacing equation (26) into (30) and simplifying, equation (31) can be obtained:

$$\begin{aligned} V_{ms} = (Z_{ms})\left(\frac{1}{Z_{sh}} + \frac{1}{Z_{1s}} + \frac{1}{Z_{2s}} + \frac{1}{Z_{3s}}\right)V_{sh} + (Z_{ms})\left(\frac{1}{Z_{1s}} + \frac{1}{Z_{2s}} + \frac{1}{Z_{3s}}\right)V_{hg} \\ -(Z_{ms})\begin{bmatrix} \frac{1}{Z_{1s}} & \frac{1}{Z_{2s}} & \frac{1}{Z_{3s}} \end{bmatrix}\begin{bmatrix} V_{1p} + V_{pg} \\ V_{2p} + V_{pg} \\ V_{3p} + V_{pg} \end{bmatrix} \end{aligned} \tag{31}$$

To derive the last equation needed for the derivation of the CEM, it is noted in Figure 22(b), equation (32) holds true where $\alpha \in [1,2,3]$:

$$V_\alpha + V_{pg} - V_{ms} - V_{sh} - V_{hg} = i_{\alpha m} Z_{\alpha m} \tag{32}$$

By combining equation (25), (26) and (32), and noting $i_\alpha = i_{\alpha m} + i_{\alpha s} + i_{\alpha h}$, equation (33) can be obtained:

$$V_\alpha + V_{pg} = \frac{\begin{pmatrix} i_\alpha + V_{ms}\left(\frac{1}{Z_{\alpha m}}\right) + V_{sh}\left(\frac{1}{Z_{\alpha s}} + \frac{1}{Z_{\alpha m}}\right) \\ + V_{hg}\left(\frac{1}{Z_{\alpha h}} + \frac{1}{Z_{\alpha s}} + \frac{1}{Z_{\alpha m}}\right) \end{pmatrix}}{\left(\frac{1}{Z_{\alpha m}} + \frac{1}{Z_{\alpha s}} + \frac{1}{Z_{\alpha h}}\right)} \tag{33}$$

Equations (22), (27), (31), and (33) can now be used to derive the CEM equation of the twelve module architectures. For the CEM equation derivation presented in this thesis, the module architectures shown in Figure 18 were simplified to ignore:

1. All inductive parasitics inside the module.
2. The parasitic capacitance C_{H1} (shown in Figure 17(a)).

These simplifications are considered valid as the inductive parasitics inside the module are conventionally very small compared to the inductive parasitics of the converter[33], [65]–[67]. For the application studied the impedance of C_{H1} is also very large compared to the impedance of Z_{H1}. Both statements can be verified using Table 3 and Table 4. The CEM equations for each of the simplified modules is now derived.

4.3.2.1 Baseline and Baseline (C_y) Module

The CEM equation derivation for the simplified Baseline and Baseline (C_y) modules is similar, with the only difference being the value of Z_{1h} and Z_{3h}. To obtain the simplified Baseline module from the generalized module architecture, conditions (34) and (35) need to hold true:

$$Z_{1s} = Z_{2s} = Z_{3s} = Z_{1m} = Z_{2m} = Z_{3m} \to \infty \tag{34}$$

$$Z_{ms} = Z_{sh} \to 0 \tag{35}$$

Applying conditions (34) and (35), equations (22), (27), (31), and (33) become:

$$V_{hg} = Z_{hg}\begin{bmatrix} 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{36}$$

$$V_{sh} = \mathbf{0} \tag{37}$$

$$V_{ms} = \mathbf{0} \tag{38}$$

$$V_{\alpha} + V_{pg} = \frac{i_{\alpha} + V_{hg}\left(\frac{1}{Z_{\alpha h}}\right)}{\left(\frac{1}{Z_{\alpha h}}\right)} = Z_{\alpha h} i_{\alpha} + V_{hg} \tag{39}$$

where $\alpha \in [1,2,3]$.

Plugging equation (36) into equation (39) and expanding α to matrix form, system of equations (40) can be obtained:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \begin{bmatrix} V_{pg} \\ V_{pg} \\ V_{pg} \end{bmatrix} = \begin{bmatrix} Z_{1h} & 0 & 0 \\ 0 & Z_{2h} & 0 \\ 0 & 0 & Z_{3h} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + Z_{hg} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{40}$$

$$V_{ap} + V_{pg} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} Z_{1h} & 0 & 0 \\ 0 & Z_{2h} & 0 \\ 0 & 0 & Z_{3h} \end{bmatrix} i_\alpha + Z_{hg} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} i_\alpha \tag{41}$$

Using the transform definitions for T_N^i and T_N^v and the methodology detailed in [64], system of equations (41) is decomposed into a system of DM and CM equations. From [64], the linear transformation matrices T_N^i and T_N^v can be expressed as (42), and (43):

$$T_N^i = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 & 1 \end{bmatrix} \tag{42}$$

$$T_N^v = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \tag{43}$$

Decomposing system of equations (41) by making substitution $i_\alpha = \left(T_N^i\right)^{-1} i_{DCM}$ for line currents and left multiplying by T_N^v, system of equations (44) is obtained:

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{pg} \end{bmatrix} =$$

$$\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} Z_{1h} & 0 & 0 \\ 0 & Z_{2h} & 0 \\ 0 & 0 & Z_{3h} \end{bmatrix} \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} + Z_{hg} \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} \quad (44)$$

Solving and simplifying system of equations (44), system of equations (45) is obtained:

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{pg} \end{bmatrix} =$$

$$\begin{bmatrix} \frac{4Z_{1h}+2Z_{2h}}{3} & \frac{2Z_{1h}-2Z_{2h}}{3} & \frac{Z_{1h}-Z_{2h}}{3} \\ \frac{-2Z_{2h}+2Z_{3h}}{3} & \frac{2Z_{2h}+4Z_{3h}}{3} & \frac{Z_{2h}-Z_{3h}}{3} \\ \frac{4Z_{1h}-2Z_{2h}-2Z_{3h}}{9} & \frac{2Z_{1h}+2Z_{2h}-4Z_{3h}}{9} & \frac{Z_{1h}+Z_{2h}+Z_{3h}}{9} \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} \quad (45)$$

$$+ Z_{hg} \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix}$$

Now from system of equations (41), it can be also be concluded that system of equations (46) holds true:

$$\begin{bmatrix} V_1 + V_{pg} - V_{hg} \\ V_2 + V_{pg} - V_{hg} \\ V_3 + V_{pg} - V_{hg} \end{bmatrix} = \begin{bmatrix} Z_{1h} & 0 & 0 \\ 0 & Z_{2h} & 0 \\ 0 & 0 & Z_{3h} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (46)$$

Decomposing (46) into system of DM and CM equations by making substitution $i_\alpha = \left(T_N^i\right)^{-1} i_{DCM}$ for line currents and left multiplying by T_N^v, system of equations (47) is obtained:

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM}+V_{pg}-V_{hg} \end{bmatrix} =$$

$$\begin{bmatrix} \frac{4Z_{1h}+2Z_{2h}}{3} & \frac{2Z_{1h}-2Z_{2h}}{3} & \frac{Z_{1h}-Z_{2h}}{3} \\ \frac{-2Z_{2h}+2Z_{3h}}{3} & \frac{2Z_{2h}+4Z_{3h}}{3} & \frac{Z_{2h}-Z_{3h}}{3} \\ \frac{4Z_{1h}-2Z_{2h}-2Z_{3h}}{9} & \frac{2Z_{1h}+2Z_{2h}-4Z_{3h}}{9} & \frac{Z_{1h}+Z_{2h}+Z_{3h}}{9} \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} \quad (47)$$

Substituting (47) into system of equations (45), system of equations (48) is obtained:

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{pg} \end{bmatrix} = \begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM}+V_{pg}-V_{hg} \end{bmatrix} + Z_{hg} \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} \quad (48)$$

However, system of equations (47) can also be written as (49):

$$\begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} =$$

$$\begin{bmatrix} \frac{4Z_{1h}+2Z_{2h}}{3} & \frac{2Z_{1h}-2Z_{2h}}{3} & \frac{Z_{1h}-Z_{2h}}{3} \\ \frac{-2Z_{2h}+2Z_{3h}}{3} & \frac{2Z_{2h}+4Z_{3h}}{3} & \frac{Z_{2h}-Z_{3h}}{3} \\ \frac{4Z_{1h}-2Z_{2h}-2Z_{3h}}{9} & \frac{2Z_{1h}+2Z_{2h}-4Z_{3h}}{9} & \frac{Z_{1h}+Z_{2h}+Z_{3h}}{9} \end{bmatrix}^{-1} \begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM}+V_{pg}-V_{hg} \end{bmatrix} \quad (49)$$

System of equations (49) can then be simplified to (50):

$$\begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} =$$

$$\begin{bmatrix} \frac{Z_{1h}+2Z_{2h}}{6Z_{1h}Z_{2h}} & \frac{-Z_{1h}+Z_{2h}}{6Z_{1h}Z_{2h}} & \frac{-Z_{1h}+Z_{2h}}{2Z_{1h}Z_{2h}} \\ \frac{Z_{2h}-Z_{3h}}{6Z_{2h}Z_{3h}} & \frac{2Z_{2h}+Z_{3h}}{6Z_{2h}Z_{3h}} & \frac{-Z_{2h}+Z_{3h}}{2Z_{2h}Z_{3h}} \\ \frac{-Z_{1h}Z_{2h}-Z_{1h}Z_{3h}+2Z_{2h}Z_{3h}}{3Z_{1h}Z_{2h}Z_{3h}} & \frac{-2Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}}{3Z_{1h}Z_{2h}Z_{3h}} & \frac{Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}}{Z_{1h}Z_{2h}Z_{3h}} \end{bmatrix}$$

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM}+V_{pg}-V_{hg} \end{bmatrix}$$

(50)

Extracting the third row from the system of equations given in (50), equation (51) is obtained:

$$\begin{aligned} i_{CM} = & \frac{-Z_{1h}Z_{2h}-Z_{1h}Z_{3h}+2Z_{2h}Z_{3h}}{3Z_{1h}Z_{2h}Z_{3h}} V_{12} + \frac{-2Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}}{3Z_{1h}Z_{2h}Z_{3h}} V_{23} \\ & + \frac{Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}}{Z_{1h}Z_{2h}Z_{3h}} (V_{CM}+V_{pg}-V_{hg}) \end{aligned} \tag{51}$$

Equation (51) can be rearranged to obtain equation (52):

$$\begin{aligned} & V_{CM}+V_{pg}-V_{hg} = \\ & \frac{Z_{1h}Z_{2h}Z_{3h}}{Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}} i_{CM} - \frac{-Z_{1h}Z_{2h}-Z_{1h}Z_{3h}+2Z_{2h}Z_{3h}}{3(Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h})} V_{12} \\ & - \frac{-2Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}}{3(Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h})} V_{23} \end{aligned} \tag{52}$$

Plugging (52) into third row extracted from the system of equations given in (48), equation (53) can be obtained:

$$\begin{aligned} V_{CM}+V_{pg} = & \frac{Z_{1h}Z_{2h}Z_{3h}}{Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}} i_{CM} - \frac{-Z_{1h}Z_{2h}-Z_{1h}Z_{3h}+2Z_{2h}Z_{3h}}{3(Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h})} V_{12} \\ & - \frac{-2Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}}{3(Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h})} V_{23} + Z_H i_{CM} \end{aligned} \tag{53}$$

Equation (53) can be rearranged to obtain equations (54) and (55):

$$V_{CM}+V_{pg}= \left(\frac{Z_{1h}Z_{2h}Z_{3h}}{Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}}+Z_{hg}\right)i_{CM} - \frac{-Z_{1h}Z_{2h}-Z_{1h}Z_{3h}+2Z_{2h}Z_{3h}}{3(Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h})}V_{12}-\frac{-2Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h}}{3(Z_{1h}Z_{2h}+Z_{1h}Z_{3h}+Z_{2h}Z_{3h})}V_{23} \quad (54)$$

$$V_{CM}+V_{pg}= (Z_{1h}\parallel Z_{2h}\parallel Z_{3h}+Z_{hg})i_{CM}+k_1V_{12}+k_2V_{23} \quad (55)$$

Where k_1 and k_2 are constants. The CEM derived through equation (55) can be seen in Figure 23 with the help of Table 5. In Figure 23, Z_H will be determined by the test schematic and v_{CM}^{p} is the sum of voltage V_{CM} and V_{pg}.

4.3.2.2 Baseline (C_D) Module

To obtain the simplified Baseline (C_D) module from the generalized module architecture condition (56) and (57) need to hold true:

$$i_{1s}=i_{2s}=i_{3s}=i_{2m}\rightarrow 0 \quad (56)$$

$$i_{1m}=-i_{3m} \quad (57)$$

Applying conditions (56) and (57), equation (22), (23), (28), and (33) become:

$$V_{hg}=Z_{hg}[1\ \ 1\ \ 1]\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (58)$$

$$V_{sh}\ =\ \mathbf{0} \quad (59)$$

$$V_{ms}\ =\ 0 \quad (60)$$

$$V_{\alpha}+V_{pg}\ =\ \frac{i_{\alpha}+V_{hg}\left(\frac{1}{Z_{\alpha h}}\right)}{\left(\frac{1}{Z_{\alpha h}}\right)}\ =\ Z_{\alpha h}i_{\alpha}+V_{hg} \quad (61)$$

where $\alpha \in [1,2,3]$.

Plugging in equation (58) into equation (61) and expanding α to matrix form, equation (62) can be obtained.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \begin{bmatrix} V_{pg} \\ V_{pg} \\ V_{pg} \end{bmatrix} = \begin{bmatrix} Z_{1h} & 0 & 0 \\ 0 & Z_{2h} & 0 \\ 0 & 0 & Z_{3h} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + Z_{hg} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{62}$$

It can be seen that equation (40) and (62) are equivalent. Therefore, the CEM equation for the Baseline (C_D) module is the same as the CEM equation of the Baseline and Baseline (C_y) module.

4.3.2.3 CM Screen, CM Screen (CD) and CM Screen (DC Mid) Module

The CEM equation derivation for the simplified CM Screen and the CM Screen (DC Mid) module is similar, with the only difference being the value of Z_{1s} and Z_{3s}. Interpolating the insights gained from the CEM equation derivation of the simplified Baseline and Baseline (C_D) module, the simplified CM Screen and CM Screen (C_D) module should have same CEM equation. To obtain the CEM equation for the simplified CM Screen module from the generalized module architecture condition (63) and (64) need to hold true:

$$Z_{1h} = Z_{2h} = Z_{3h} = Z_{1m} = Z_{2m} = Z_{3m} \to \infty \tag{63}$$

$$Z_{ms} \to 0 \tag{64}$$

Applying conditions (63) and (64), equation (22), (27), (31), and (33) become:

$$V_{hg} = Z_{hg} \begin{bmatrix} 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{65}$$

$$V_{sh} = Z_{sh} \begin{bmatrix} 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{66}$$

$$V_{ms} = \mathbf{0} \tag{67}$$

$$V_{\alpha} + V_{pg} = \frac{i_{\alpha} + V_{sg}\left(\frac{1}{Z_{\alpha s}}\right) + V_{sh}\left(\frac{1}{Z_{\alpha s}}\right)}{\left(\frac{1}{Z_{\alpha s}}\right)} = Z_{\alpha s} i_{\alpha} + V_{sg} + V_{sh} \tag{68}$$

where α ∈ [1,2,3].

Plugging in equation (65) and (66) into equation (68) and expanding α to matrix form, equation (69) can be obtained:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \begin{bmatrix} V_{pg} \\ V_{pg} \\ V_{pg} \end{bmatrix} = \begin{bmatrix} Z_{1s} & 0 & 0 \\ 0 & Z_{2s} & 0 \\ 0 & 0 & Z_{3s} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + Z_{sg} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + Z_{hg} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{69}$$

Equation (69) can be rewritten as equation (70):

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \begin{bmatrix} V_{pg} \\ V_{pg} \\ V_{pg} \end{bmatrix} = \begin{bmatrix} Z_{1s} & 0 & 0 \\ 0 & Z_{2s} & 0 \\ 0 & 0 & Z_{3s} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + (Z_{sg} + Z_{hg}) \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{70}$$

$$V_{\alpha p} + V_{pg} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} Z_{1s} & 0 & 0 \\ 0 & Z_{2s} & 0 \\ 0 & 0 & Z_{3s} \end{bmatrix} i_{\alpha} + (Z_{sh} + Z_{hg}) \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} i_{\alpha} \tag{71}$$

Using the transform definitions for T_N^i and T_N^v and the methodology detailed in [64], system of equations (71) is decomposed into a system of DM and CM equations. From [64], the linear transformation matrices T_N^i and T_N^v can be expressed as (42), and (43).

Decomposing system of equations (71) by making substitution $i_{\alpha} = \left(T_N^i\right)^{-1} i_{DCM}$ for line currents and left multiplying by T_N^v, system of equations (72) is obtained:

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{pg} \end{bmatrix} = (Z_{sh} + Z_{hg}) \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix}$$
$$+ \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} Z_{1s} & 0 & 0 \\ 0 & Z_{2s} & 0 \\ 0 & 0 & Z_{3s} \end{bmatrix} \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} \quad (72)$$

Solving and simplifying system of equations (72), system of equations (73) is obtained:

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{pg} \end{bmatrix} =$$
$$\begin{bmatrix} \frac{4Z_{1s} + 2Z_{2s}}{3} & \frac{2Z_{1s} - 2Z_{2s}}{3} & \frac{Z_{1s} - Z_{2s}}{3} \\ \frac{-2Z_{2s} + 2Z_{3s}}{3} & \frac{2Z_{2h} + 4Z_{3h}}{3} & \frac{Z_{2h} - Z_{3h}}{3} \\ \frac{4Z_{1s} - 2Z_{2s} - 2Z_{3s}}{9} & \frac{2Z_{1s} + 2Z_{2s} - 4Z_{3s}}{9} & \frac{Z_{1s} + Z_{2s} + Z_{3s}}{9} \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} \quad (73)$$
$$+ (Z_{sh} + Z_{hg}) \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix}$$

Now from system of equations (71), it can be also be concluded that system of equations (74) holds true:

$$\begin{bmatrix} V_1 + V_{pg} - V_{sh} - V_{hg} \\ V_2 + V_{pg} - V_{sh} - V_{hg} \\ V_3 + V_{pg} - V_{sh} - V_{hg} \end{bmatrix} = \begin{bmatrix} Z_{1s} & 0 & 0 \\ 0 & Z_{2s} & 0 \\ 0 & 0 & Z_{3s} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (74)$$

Decomposing (74) into a system of DM and CM equations by making substitution $i_\alpha = \left(T_N^i\right)^{-1} i_{DCM}$ for line currents and left multiplying by T_N^v, system of equations (75) is obtained:

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM}+V_{pg}-V_{sh}-V_{hg} \end{bmatrix} =$$

$$\begin{bmatrix} \frac{4Z_{1s}+2Z_{2s}}{3} & \frac{2Z_{1s}-2Z_{2s}}{3} & \frac{Z_{1s}-Z_{2s}}{3} \\ \frac{-2Z_{2s}+2Z_{3s}}{3} & \frac{2Z_{2s}+4Z_{3s}}{3} & \frac{Z_{2s}-Z_{3s}}{3} \\ \frac{4Z_{1s}-2Z_{2s}-2Z_{3s}}{9} & \frac{2Z_{1s}+2Z_{2s}-4Z_{3s}}{9} & \frac{Z_{1s}+Z_{2s}+Z_{3s}}{9} \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} \quad (75)$$

Substituting (75) into system of equations (73), system of equations (76) is obtained:

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{pg} \end{bmatrix} = \begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM}+V_{pg}-V_{sh}-V_{hg} \end{bmatrix} + (Z_{sh}+Z_{hg}) \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} \quad (76)$$

However, system of equations (75) can also be written as (77):

$$\begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} =$$

$$\begin{bmatrix} \frac{4Z_{1s}+2Z_{2s}}{3} & \frac{2Z_{1s}-2Z_{2s}}{3} & \frac{Z_{1s}-Z_{2s}}{3} \\ \frac{-2Z_{2s}+2Z_{3s}}{3} & \frac{2Z_{2s}+4Z_{3s}}{3} & \frac{Z_{2s}-Z_{3s}}{3} \\ \frac{4Z_{1s}-2Z_{2s}-2Z_{3s}}{9} & \frac{2Z_{1s}+2Z_{2s}-4Z_{3s}}{9} & \frac{Z_{1s}+Z_{2s}+Z_{3s}}{9} \end{bmatrix}^{-1} \quad (77)$$

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM}+V_{pg}-V_{sh}-V_{hg} \end{bmatrix}$$

System of equations (77) can then be simplified to (78):

$$\begin{bmatrix} i_{12} \\ i_{23} \\ i_{CM} \end{bmatrix} =$$

$$\begin{bmatrix} \frac{Z_{1s}+2Z_{2s}}{6Z_{1s}Z_{2s}} & \frac{-Z_{1s}+Z_{2s}}{6Z_{1s}Z_{2s}} & \frac{-Z_{1s}+Z_{2s}}{2Z_{1s}Z_{2s}} \\ \frac{Z_{2s}-Z_{3s}}{6Z_{2s}Z_{3s}} & \frac{2Z_{2s}+Z_{3s}}{6Z_{2s}Z_{3s}} & \frac{-Z_{2s}+Z_{3s}}{2Z_{2s}Z_{3s}} \\ \frac{-Z_{1s}Z_{2s}-Z_{1s}Z_{3s}+2Z_{2s}Z_{3s}}{3Z_{1s}Z_{2s}Z_{3s}} & \frac{-2Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s}}{3Z_{1s}Z_{2s}Z_{3s}} & \frac{Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s}}{Z_{1s}Z_{2s}Z_{3s}} \end{bmatrix}$$

$$\begin{bmatrix} V_{12} \\ V_{23} \\ V_{CM}+V_{pg}-V_{sh}-V_{hg} \end{bmatrix}$$

(78)

Extracting the third row from the system of equations given in (78), equation (79) is obtained:

$$\begin{aligned} i_{CM} = & \frac{-Z_{1s}Z_{2s}-Z_{1s}Z_{3s}+2Z_{2s}Z_{3s}}{3Z_{1s}Z_{2s}Z_{3s}} V_{12} + \frac{-2Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s}}{3Z_{1s}Z_{2s}Z_{3s}} V_{23} \\ & + \frac{Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s}}{Z_{1s}Z_{2s}Z_{3s}} (V_{CM}+V_{pg}-V_{sh}-V_{hg}) \end{aligned} \tag{79}$$

Equation (79) can be rearranged to obtain equation (80):

$$\begin{aligned} & V_{CM}+V_{pg}-V_{sh}-V_{hg} = \\ & \frac{Z_{1s}Z_{2s}Z_{3s}}{Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s}} i_{CM} - \frac{-Z_{1s}Z_{2s}-Z_{1s}Z_{3s}+2Z_{2s}Z_{3s}}{3(Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s})} V_{12} \\ & - \frac{-2Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s}}{3(Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s})} V_{23} \end{aligned} \tag{80}$$

Plugging (80) into third row extracted from the system of equations given in (76), equation (81) can be obtained:

$$\begin{aligned} V_{CM}+V_{pg} = & \frac{Z_{1s}Z_{2s}Z_{3s}}{Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s}} i_{CM} - \frac{-Z_{1s}Z_{2s}-Z_{1s}Z_{3s}+2Z_{2s}Z_{3s}}{3(Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s})} V_{12} \\ & - \frac{-2Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s}}{3(Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s})} V_{23} + Z_{sh}i_{CM} + Z_{hg}i_{CM} \end{aligned} \tag{81}$$

Equation (81) can be rearranged to obtain equations (82) and (83):

$$V_{CM}+V_{pg}= \left(\frac{Z_{1s}Z_{2s}Z_{3s}}{(Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s})}+Z_{hg}+Z_{sh}\right)i_{CM} - \frac{-Z_{1s}Z_{2s}-Z_{1s}Z_{3s}+2Z_{2s}Z_{3s}}{3(Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s})}V_{12}-\frac{-2Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s}}{3(Z_{1s}Z_{2s}+Z_{1s}Z_{3s}+Z_{2s}Z_{3s})}V_{23} \quad (82)$$

$$V_{CM}+V_{pg}= (Z_{1s}\parallel Z_{2s}\parallel Z_{3s}+Z_{hg}+Z_{sh})i_{CM}+k_1V_{12}+k_2V_{23} \quad (83)$$

Where k_1 and k_2 are constants.

The CEM derived through equation (83) can be seen in Figure 23 with the help of Table 5. In Figure 23, Z_H will be determined by the test schematic and v_{CM}^{p} is the sum of voltage V_{CM} and V_{pg}.

4.3.2.4 CM Screen (DC+) and CM Screen (DC+, CD) Module

Interpolating the insights gained from the CEM equation derivation of the simplified Baseline and Baseline (C_D) module, the simplified CM Screen (DC+) and CM Screen (DC+, C_D) module should have same CEM equation. To obtain the CEM equation for the simplified CM Screen (DC+) module from the generalized module architecture condition (84) and (85) need to hold true.

$$Z_{1h}=Z_{2h}=Z_{3h}=Z_{2m}=Z_{3m}\rightarrow\infty \quad (84)$$

$$Z_{1m}=Z_{ms}\rightarrow 0 \quad (85)$$

Applying conditions (84) and (85), equations (22), (27), (31), and (33) become:

$$V_{hg}=Z_{hg}\begin{bmatrix}1 & 1 & 1\end{bmatrix}\begin{bmatrix}i_1\\ i_2\\ i_3\end{bmatrix} \quad (86)$$

$$V_{sh} = Z_{sh}[1 \;\; 1 \;\; 1]\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{87}$$

$$V_{ms} = \mathbf{0} \tag{88}$$

$$V_1 + V_{pg} = \frac{\begin{pmatrix} i_1 + V_{sh}\left(\frac{1}{Z_{1s}} + \frac{1}{Z_{1m}}\right) \\ + V_{hg}\left(\frac{1}{Z_{1s}} + \frac{1}{Z_{1m}}\right) \end{pmatrix}}{\left(\frac{1}{Z_{1s}} + \frac{1}{Z_{1m}}\right)} = \frac{i_\alpha}{\left(\frac{1}{Z_{1s}} + \frac{1}{Z_{1m}}\right)} + V_{sg} + V_{sh} = V_{sg} + V_{sh} \tag{89}$$

$$V_2 + V_{pg} = \frac{i_2 + V_{sh}\left(\frac{1}{Z_{2s}}\right) + V_{hg}\left(\frac{1}{Z_{2s}}\right)}{\left(\frac{1}{Z_{2s}}\right)} = Z_{2s} i_2 + V_{sh} + V_{hg} \tag{90}$$

$$V_3 + V_{pg} = \frac{i_3 + V_{sh}\left(\frac{1}{Z_{3s}}\right) + V_{hg}\left(\frac{1}{Z_{3s}}\right)}{\left(\frac{1}{Z_{3s}}\right)} = Z_{3s} i_3 + V_{sh} + V_{hg} \tag{91}$$

Combining equations (89) - (91) into a matrix form, equation (92) can be obtained:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \begin{bmatrix} V_{pg} \\ V_{pg} \\ V_{pg} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & Z_{2s} & 0 \\ 0 & 0 & Z_{3s} \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + (Z_{sg} + Z_{hg})\begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{92}$$

$$V_{ap} + V_{pg}\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & Z_{2s} & 0 \\ 0 & 0 & Z_{3s} \end{bmatrix} i_\alpha + (Z_{sh} + Z_{hg})\begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} i_\alpha \tag{93}$$

A complete derivation for the CEM equation can be done again; however, it can be noticed the system of equations (93) and system of equation (71) are similar, except that $Z_{1s} \to 0$. The CEM equation can therefore be derived from equation (82) by assuming $Z_{1s} \to 0$. The CEM equation for the simplified CM Screen (DC+) and CM Screen (DC+, C_D) module is given in (94)

$$V_{CM} + V_{pg} = (Z_{hg} + Z_{sh}) i_{CM} - \frac{2}{3} V_{12} - \frac{1}{3} V_{23} \quad (94)$$

$$V_{CM} + V_{pg} = (Z_{hg} + Z_{sh}) i_{CM} + k_3 V_{12} + k_4 V_{23} \quad (95)$$

Where k_3 and k_4 are constants.

The CEM derived through equation (95) can be seen in Figure 23 with the help of Table 5. In Figure 23, Z_H will be determined by the test schematic and v_{CM}^p is the sum of voltage V_{CM} and V_{pg}.

4.3.2.5 CM Screen (DC-) and CM Screen (DC-, CD) Module

Interpolating the insights gained from the CEM equation derivation of the simplified Baseline and Baseline (C_D) module, the simplified CM Screen (DC-) and CM Screen (DC-, C_D) module should also have the same CEM equation. To obtain the CEM for the simplified CM Screen (DC-) module from the generalized module architecture condition, (96) and (97) need to hold true:

$$Z_{1h} = Z_{2h} = Z_{3h} = Z_{2m} = Z_{3m} \to \infty \quad (96)$$

$$Z_{3m} = Z_{ms} \to 0 \quad (97)$$

Applying conditions (96) and (97), equations (22), (27), (31), and (33) become:

$$V_{hg} = Z_{hg} [1 \;\; 1 \;\; 1] \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (98)$$

$$V_{sh} = Z_{sh} [1 \;\; 1 \;\; 1] \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (99)$$

$$V_{ms} = 0 \quad (100)$$

$$V_1 + V_{pg} = \frac{i_1 + V_{sh}\left(\frac{1}{Z_{1s}}\right) + V_{hg}\left(\frac{1}{Z_{1s}}\right)}{\left(\frac{1}{Z_{1s}}\right)} = Z_{1s} i_1 + V_{sh} + V_{hg} \quad (101)$$

$$V_2 + V_{pg} = \frac{i_2 + V_{sh}\left(\frac{1}{Z_{2s}}\right) + V_{hg}\left(\frac{1}{Z_{2s}}\right)}{\left(\frac{1}{Z_{2s}}\right)} = Z_{2s} i_2 + V_{sh} + V_{hg} \quad (102)$$

$$V_3 + V_{pg} = \frac{\left(\begin{matrix} i_3 + V_{sh}\left(\frac{1}{Z_{3s}} + \frac{1}{Z_{3m}}\right) \\ + V_{hg}\left(\frac{1}{Z_{3s}} + \frac{1}{Z_{3m}}\right) \end{matrix}\right)}{\left(\frac{1}{Z_{3s}} + \frac{1}{Z_{3m}}\right)} = \frac{i_3}{\left(\frac{1}{Z_{3s}} + \frac{1}{Z_{3m}}\right)} + V_{sg} + V_{sh} = V_{sg} + V_{sh} \quad (103)$$

Combining equations (101) - (103) into a matrix form, equation (104) can be obtained:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \begin{bmatrix} V_{pg} \\ V_{pg} \\ V_{pg} \end{bmatrix} = \begin{bmatrix} Z_{1s} & 0 & 0 \\ 0 & Z_{2s} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + (Z_{sg} + Z_{hg}) \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (104)$$

$$V_{\alpha p} + V_{pg} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} Z_{1s} & 0 & 0 \\ 0 & Z_{2s} & 0 \\ 0 & 0 & 0 \end{bmatrix} i_\alpha + (Z_{sh} + Z_{hg}) \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} i_\alpha \quad (105)$$

A complete derivation for the CEM equation can be done again; however, it can be noticed the system of equations (105) and system of equation (71) are similar except that $Z_{2s} \to 0$. The CEM equation can therefore be derived from equation (82) by assuming $Z_{2s} \to 0$. The CEM equation for the simplified CM Screen (DC-) and CM Screen (DC-, C_D) module is given in (106)

.

$$V_{CM} + V_{pg} = (Z_{hg} + Z_{sh}) i_{CM} + \frac{1}{3} V_{12} + \frac{2}{3} V_{23} \quad (106)$$

$$V_{CM} + V_{pg} = (Z_{hg} + Z_{sh}) i_{CM} + k_5 V_{12} + k_6 V_{23} \quad (107)$$

Where k_5 and k_6 are constants.

The CEM derived through equation (107) can be seen in Figure 23 with the help of Table 5. In Figure 23, Z_H will be determined by the test schematic and v_{CM}^{p} is the sum of voltage V_{CM} and V_{pg}.

4.3.2.6 CM Screen (DC+, DC-) and CM Screen (DC+, DC-, CD) Module

Interpolating the insights gained from the CEM equation derivation of the simplified Baseline and Baseline (C_D) module, the simplified CM Screen (DC+, DC-) and CM Screen (DC+, DC-, C_D) module should have same CEM equation. Furthermore, since the screening layer is split, the CEM for the simplified CM Screen (DC+, DC-) module would be the CEM of the simplified CM Screen (DC+) module and the simplified CM Screen (DC-) module paralleled together. The CEM derived through equations can be seen in Figure 23 with the help of Table 5. In Figure 23, Z_H will be determined by the test schematic.

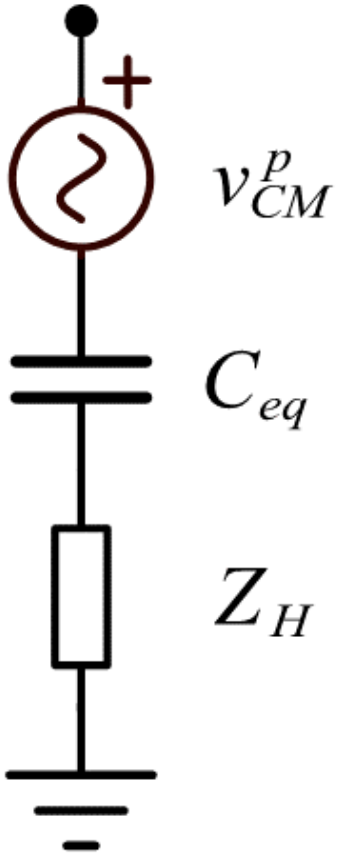


Figure 23: Common mode equivalent model (CEM) of simplifed module architectures

Table 5: Value of Equivalent CEM Capacitance C_{eq}

Simplified Module Architecture	Equivalent CEM Capacitance C_{eq}
Baseline	$C_{DC+} + C_{DC-} + C_{CM}$
Baseline (C_D)	$C_{DC+} + C_{DC-} + C_{CM}$
Baseline (C_y)	$2C_D + C_{CM}$
CM Screen	$\frac{(C_{DC+} + C_{DC-} + C_{CM})(C_{screen})}{C_{screen} + C_{DC+} + C_{DC-} + C_{CM}}$

CM Screen (C_D)	$\frac{(C_{DC+} + C_{DC-} + C_{CM})(C_{screen})}{C_{screen} + C_{DC+} + C_{DC-} + C_{CM}}$
CM Screen (DC+)	C_{screen}
CM Screen (DC+, C_D)	C_{screen}
CM Screen (DC-)	C_{screen}
CM Screen (DC-, C_D)	C_{screen}
CM Screen (DC Mid)	$\frac{(2C_D + C_{CM})(C_{screen})}{C_{screen} + 2C_D}$
CM Screen (DC+, DC-)	$\frac{C_{screen}}{2} + \frac{C_{screen}}{2}$
CM Screen (DC+, DC-, C_D)	$\frac{C_{screen}}{2} + \frac{C_{screen}}{2}$

4.3.3 Test Setup Schematic

Using the CEM derived in Figure 21(b), Figure 23 and the CEM model for LISN derived in [38], the CEM of the test setup schematic shown in Figure 17(a) could be derived. The CEM for the test setup schematic is shown in Figure 24. It is important to note that in Figure 24, the voltage source v_{CM} for the Baseline, CM Screen, CM Screen (DC+), CM Screen (DC-) and CM Screen (DC+, DC-) module is defined as shown in (108):

$$v_{CM} = v\left(V_{in},\ V_{Z_{Cin}},\ V_{Z_{PCB}},\ V_{Q_H},\ V_{Q_L}\right) \tag{108}$$

Where V_{in}, $V_{Z_{Cin}}$, $V_{Z_{PCB}}$, V_{Q_H} and V_{Q_L} is the voltage across the output of the LISN, capacitor Z_{Cin}, capacitor Z_{PCB}, high side die Q_H and low side die Q_L. The voltage source v_{CM} for the Baseline

(C_D), Baseline (C_y), CM Screen (C_D), CM Screen (DC+, C_D), CM Screen (DC-, C_D), CM Screen (DC Mid), and CM Screen (DC+, DC-, C_D) modules is defined as shown in (109):

$$v_{CM} = v\left(V_{in},\ V_{Z_{Cin}},\ V_{Z_{PCB}},\ V_{Z_{C_D}},\ V_{Q_H},\ V_{Q_L}\right) \tag{109}$$

The primary difference between (108) and (109) is that due to the addition of the decoupling capacitors Z_{C_D}, voltage source v_{CM} is also dependent on the $V_{Z_{C_D}}$, voltage across the decoupling capacitors Z_{C_D}. The impedance Z_{C_D} relates to the parameters given in Table 4 according to equation (110):

$$Z_{C_D} = 2ESR_{C_D} + 2j\omega ESL_{C_D} + \frac{2}{jwC_D} \tag{110}$$

In Figure 24, the path outlined in blue is the primary impedance path that the CM current escaping through the baseplate flows through.

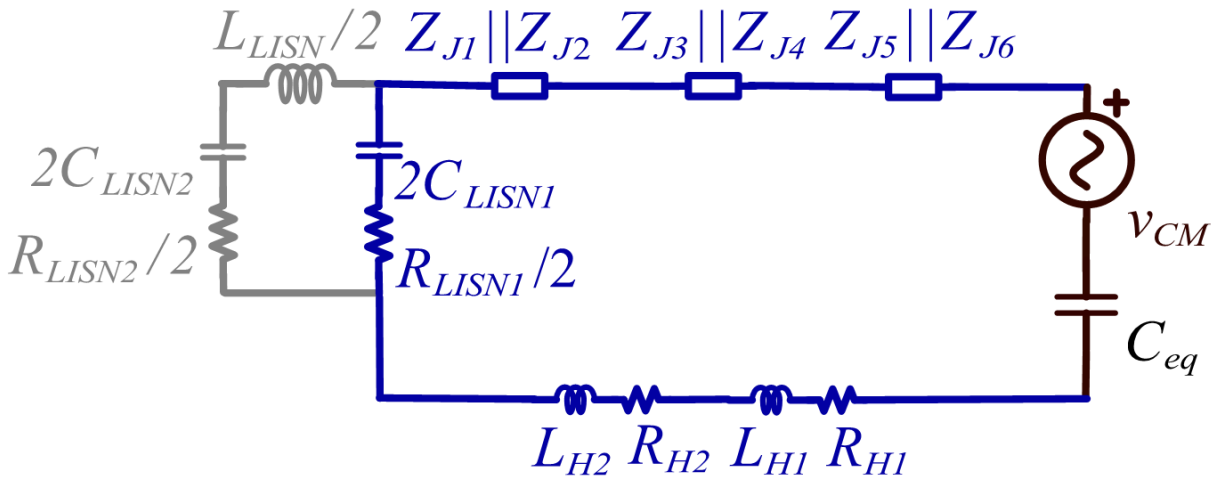


Figure 24: Common mode equivalent model for test setup schematic shown in Figure 17(a)

4.4 Substitution and Superposition Principle

To understand in detail why different module architectures show different levels of noise mitigation, the flow path taken by i_{CM} — the CM noise current flowing through the capacitor C_{CM} (Figure 17(a)) — is looked at more closely. To identify the paths i_{CM} flows through, the substitution theorem and superposition theorem are applied [33], [68]–[70]. Substitution theorem states that the SiC MOSFET dies in an application can be replaced with a voltage or current source having the exact same terminal voltage or current behavior [69]. Either type of source can be used to replace the SiC MOSFET die; however, a substitution that results in the formation of voltage source loops and current source nodes must be avoided [68]. Figure 25(a) shows the simulation model for the CM Screen (DC+) module architecture as an example. Figure 25(b) shows the module architecture after substitution theorem has been applied. It can be seen that the high side switch Q_H has been replaced with a current source i_H, and the low side switch has been replaced with a voltage source v_L. The current source i_H and voltage source v_L have the same respective terminal current and voltage characteristics that MOSFET Q_H and Q_L would have had during the switching operation of the converter and are therefore the main sources of noise escaping the baseplate into the converter.

Since the converter schematic now consists of no non-linear circuit components, superposition is applied. The superposition principle states that the excitations generated by multiple excitation sources present in a circuit is the linear sum of the excitation generated by each individual source. Figure 25(c) and (d) shows the two superposition states of the module architecture. The superposition state of current source i_H (shown in Figure 25(c)) allows the study of the effect di/dt transients, and the superposition state of voltage source v_H (shown in Figure 25(d)) allows the study of the effect the dv/dt transients have on the current escaping the baseplate

of the module into the converter during switching operation of the converter. According to [33], [70], [71], the frequency spectrum of the total noise current i_{bp} that escapes the module baseplate can be equated to the two superposition states shown in Figure 25(c) and (d) through equation (111) - (112):

$$i_{bp}(s) = \frac{i_{bp}^{i_H}}{i_H}(s)\, i_H(s) + \frac{i_{bp}^{v_L}}{v_L}(s)\, v_L(s) \tag{111}$$

$$i_{bp}(s) = K_{bp}(s)\, i_H(s) + Y_{bp}(s)\, v_L(s) \tag{112}$$

Where $i_{bp}(s)$ is the frequency spectrum of the noise i_{bp} that escapes the module into the converter during the actual operation of the converter, $i_{bp}^{i_H}(s)$ and $i_{bp}^{v_L}(s)$ are the frequency spectrum of the noise i_{bp} that escapes the module into the converter during the respective superposition state (Figure 25(c) and (d)). $i_H(s)$ and $v_L(s)$ are the frequency spectrum of the respective terminal current and voltage characteristics of MOSFET Q_H and Q_L during the actual operation of the converter and $K_{bp}(s) = \frac{i_{bp}}{i_H}(s)$ and $Y_{bp}(s) = \frac{i_{bp}}{v_L}(s)$ are the current and admittance transfer function obtained from the two superposition states shown in Figure 25(c) and (d). To evaluate the effect of module architecture on the noise i_{bp}, the transfer functions K_{bp} and $Y_{bp}(s)$ can be plotted with the help of the LTspice simulation model and compared.

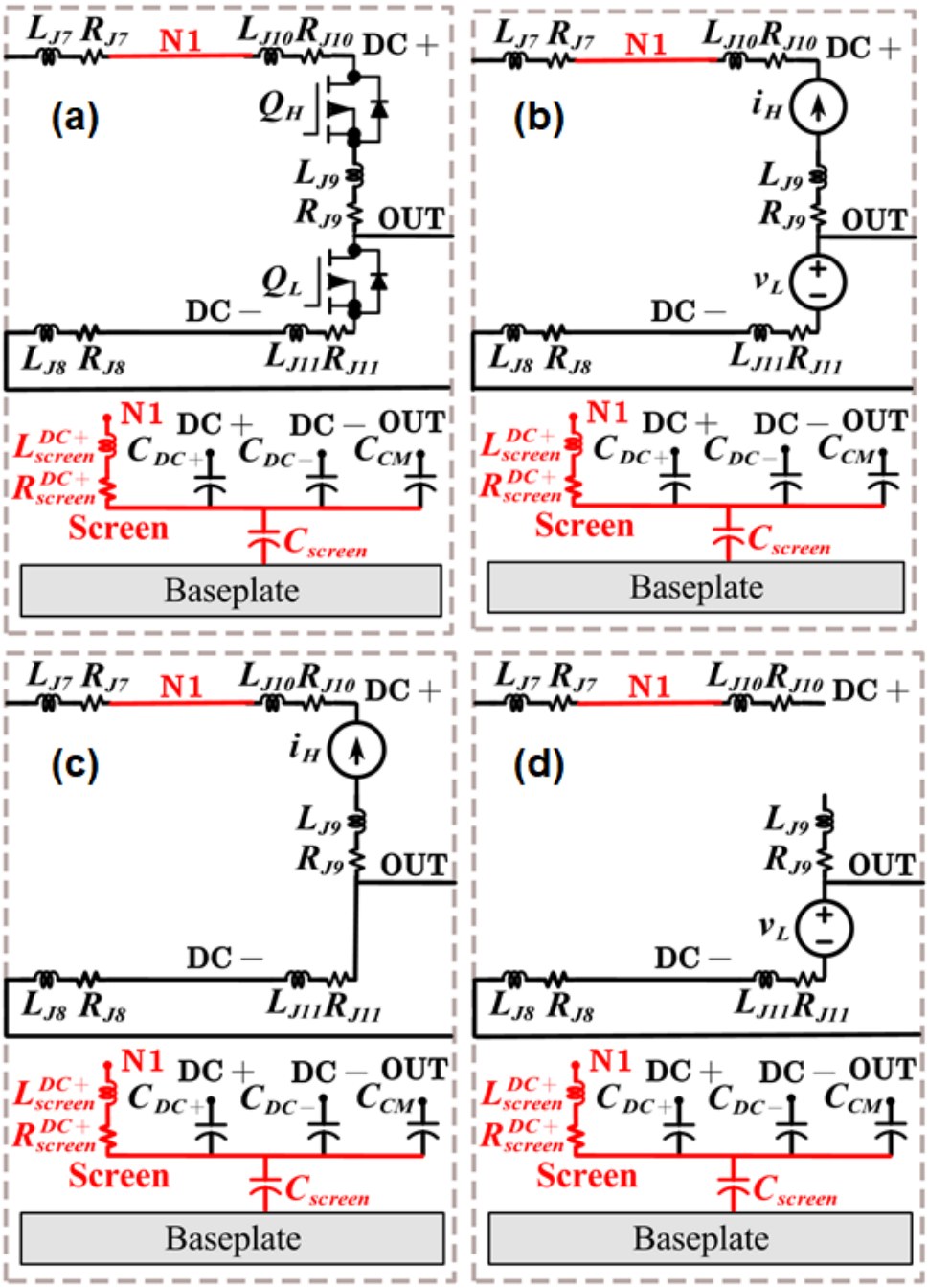


Figure 25: (a) Simulation model for CM Screen (DC+) module (b) simulation model after substitution theorm (c) superposition state used to study the effect of di/dt (d) superposition state used to study the effect of dv/dt.

Chapter 5: Module Architecture Analysis and Guidelines

5.1 Introduction

EMI mitigation results for all twelve module architectures are now provided using the simulation model shown in Figure 17(a) and the module architectures shown in Figure 18. To highlight the insights gained from each module architecture, the results are presented based on the insights the module architecture provides. It is hoped that such an approach will also help by highlighting the similarity between the different module architectures. All EMI results are presented using the Baseline module (Figure 5(a) and Figure 18(a)) as a reference. An explanation for the EMI trends and mitigation results observed is also provided for each module architecture.

5.2 Effect of Stacked Substrate

The stacked substrate architectures are modules that consist of a second screening layer between the power copper pads and the baseplate, but where the screening layer is left floating and not connected to any node inside the module. Two such architectures were studied in this thesis:

- CM Screen module architecture (Figure 7(b) and Figure 18(d))
- CM Screen (C_D) module architecture (Figure 7(c) and Figure 18(e))

Only the CM Screen module architecture will be discussed in this section; the CM Screen (C_D) module will be discussed in a later section when studying the effect of the addition of decoupling capacitors into the module architecture. The CM Screen architecture is replaced in the schematic of the simulation model shown in Figure 17(a). The results for noise i_{bp} compared to

the Baseline module is shown in Figure 26. The CM Screen module architecture shows an EMI noise mitigation of 4 dB when compared to the Baseline module architecture in the frequency range of 150 kHz to 3 MHz.

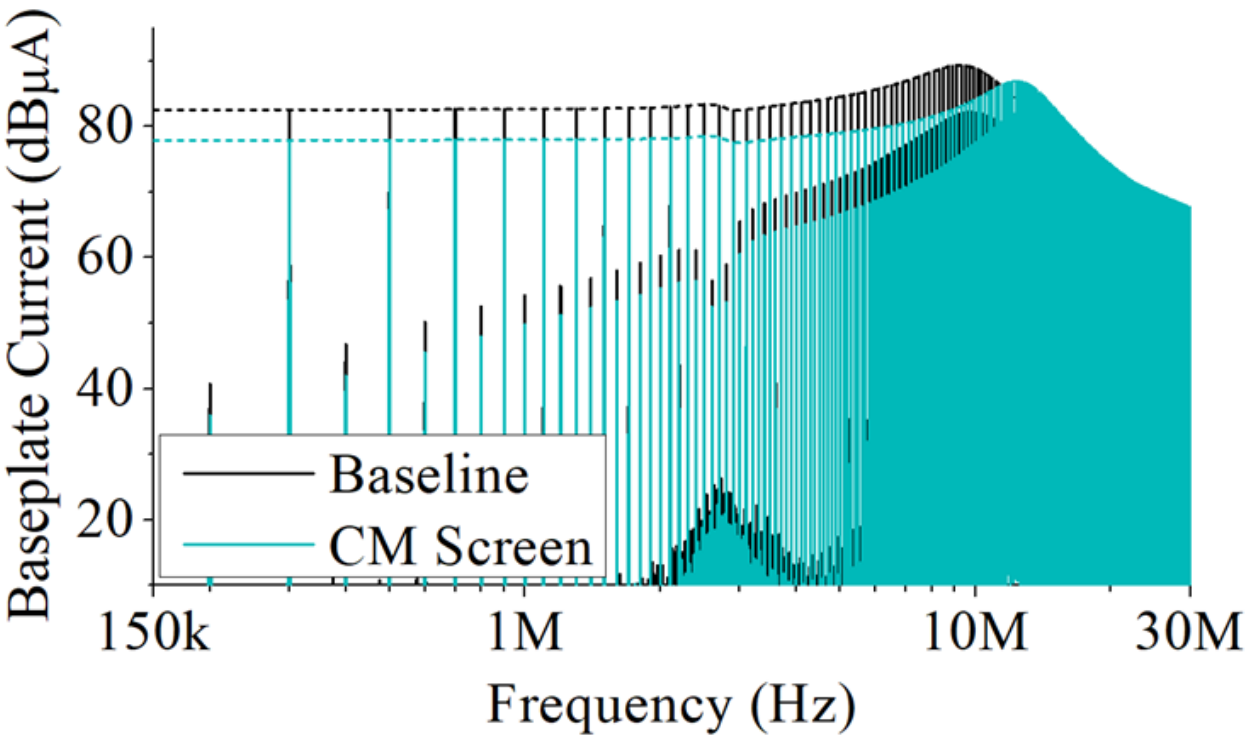


Figure 26: Frequency spectrum of Baseline module (black), CM Screen module (teal) architecture.

The individual trends seen in the frequency spectrum for the CM Screen module architecture is explained. For the stacked substrate module, a relatively flat frequency spectrum is seen until the frequency of ~12.9 MHz, beyond which a roll-off is observed (Figure 26). This is different compared to the Baseline module, in which a relatively flat frequency spectrum is seen until the frequency of ~9.9 MHz. This shift in trend can be explained by looking at the CEM shown in Figure 24 and the equivalent CEM capacitance C_{eq} given in Table 5. For the stacked substrate module architecture, the capacitance C_{eq} is defined according to equation (113).

$$C_{eq}^{\textit{stacked substrates}} = \frac{(C_{DC+} + C_{DC-} + C_{CM})\,(C_{screen})}{C_{DC+} + C_{DC-} + C_{CM} + C_{screen}} \tag{113}$$

For the Baseline module architecture, the capacitance C_{eq} is defined according to equation (114):

$$C_{eq}^{Baseline} = C_{DC+} + C_{DC-} + C_{CM} \tag{114}$$

The roll off is observed to start to occur at the frequency at which the total capacitance C_{tot} of the CEM (equation (115)) resonates with the sum of all the inductances L_{tot} that the noise current i_{bp} flows through in the CEM (equation (116)):

$$C_{tot} = \frac{(C_{eq})\,(2C_{LISN})}{C_{eq} + 2C_{LISN}} \tag{115}$$

$$L_{tot} = L_{H1} + L_{H2} + (L_{J1} \parallel L_{J2}) + (L_{J3} \parallel L_{J4}) + (L_{J5} \parallel L_{J6}) \tag{116}$$

It can be observed that due to the addition of the stacked substrate into the module, the capacitance C_{screen} is now in series with the capacitance $C_{eq}^{Baseline}$, resulting in a lower value of C_{eq}. A lower value of C_{eq} results in a lower value of C_{tot} (equation (115)). Since C_{tot} has decreased while keeping L_{tot} (equation (116)) constant, the frequency at which the resonance interaction between them occurs moves to a higher frequency, therefore resulting in the roll-off to move to a higher frequency.

A comparative analysis of the frequency spectrum of the stacked substrate module architecture compared to the Baseline module is now provided. To understand in more detail why the CM Screen module shows a higher level of noise mitigation compared to the Baseline module, the flow path taken by i_{CM} — the CM noise current flowing through the capacitor C_{CM} — is examined more closely. The CM noise in power electronic applications is mainly generated due to

dv/dt transients during switching [6], [27], [33], [40], [45], [47], [54], [55], [72]–[75]. The superposition state of the voltage source v_L for the baseline module and the stacked substrate module discussed after being introduced into the time domain model (Figure 17) is shown in Figure 27. For this analysis, only the current i_{CM} flowing through C_{CM} is of interest. All other currents flowing in the schematic are ignored. The component of i_{CM} generated due to the voltage source v_L is referred to as i_{CM}^{vL} (shown in green) respectively. It can be seen from Figure 27 that more than one path is available for i_{CM}^{vL} to flow through once the screening layer is reached. The portion of i_{CM}^{vL} diverted away from the baseplate by the CM Screen is referred to as i_{divert}^{vL} and is shown in purple. The portion that flows into the baseplate of the module is referred to as i_{bp}^{vL} and is shown in orange.

It can be seen from Figure 26 that the CM Screen module displays a lower EMI footprint and higher noise mitigation compared to the Baseline module. From Figure 27, it can be observed that compared to the path available to i_{bp}^{vL} in the case of the Baseline module (Figure 27(a)), i_{bp}^{vL} for the stacked substrate module (Figure 27(b)) now has an additional impedance in its path due to C_{screen}. This increase in impedance results in more noise diverted by the parasitic capacitances C_{DC+} and C_{DC-}, whose values are the same as in the Baseline module. From Figure 27(a) and (b), it can be seen that if condition (117) is satisfied, the majority of i_{CM} will prefer to be diverted away from the baseplate. However, it can be seen from Figure 27(b) that even if condition (117) is satisfied, i_{divert}^{vL} still flows through the paths available inside the converter to complete the current loop.

$$\frac{1}{j\omega C_{DC+}} + \frac{1}{j\omega C_{DC-}} \ll \frac{1}{j\omega C_{screen}} \tag{117}$$

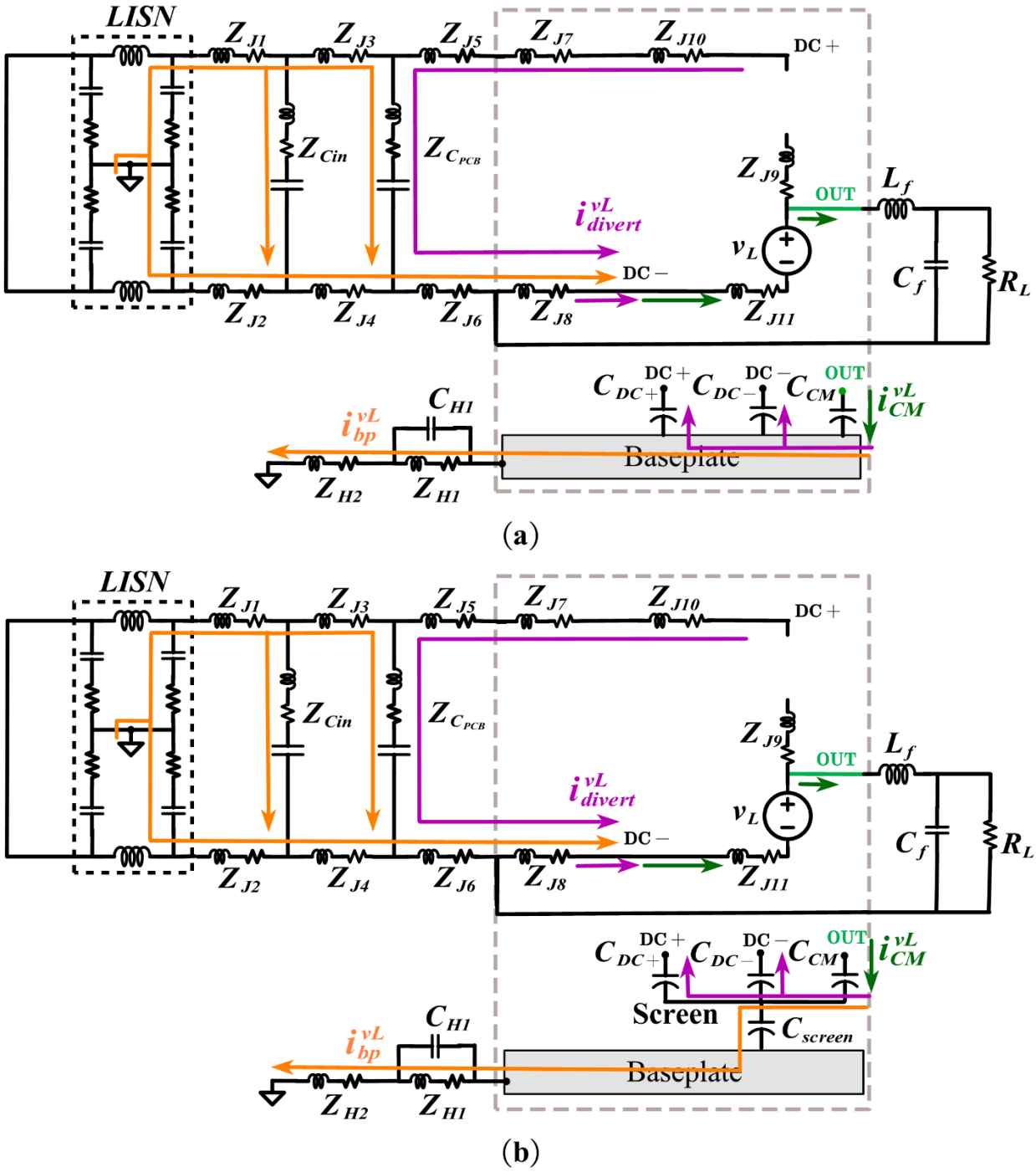


Figure 27: Converter schematic showing path taken by noise current i_{CM} flowing through C_{CM} due to voltage source v_L in (a) Baseline module (b) CM Screen module

The magnitude of the admittance Y seen by the current i_{CM}, i_{divert}, and i_{bp} as a function of voltage source v_L for the Baseline and the CM Screen module architectures is shown in Figure

28(a) and (b). The general form of the magnitude of a transfer function is given in equation (118) . In Figure 28, the admittance seen by current i_{CM}^{vL}, i_{divert}^{vL}, i_{bp}^{vL} as a function of voltage source v_L is shown in green, purple and orange.

$$|Y(s)| = |K| \left| \frac{N(s)}{D(s)} \right| \tag{118}$$

It can be seen from Figure 28(a) that for the Baseline module the magnitude of both Y_{CM}^{vL} and Y_{bp}^{vL} show similar behavior. It is only close to 30 MHz that Y_{CM}^{vL} and Y_{divert}^{vL} start showing similar behavior. This implies that for majority of the conducted EMI frequency range current would prefer to escape the module architecture rather than be diverted back into the module.

It can be seen from Figure 28(b) that for the CM Screen module the magnitude of Y_{CM}^{vL} and Y_{bp}^{vL} are no longer showing similar behavior. The magnitude for Y_{bp}^{vL} is ~4dB smaller compared to Y_{CM}^{vL} at lower frequencies. Compared to Y_{divert}^{vL} for the Baseline module, Y_{divert}^{vL} for the CM Screen module is larger. The comparison of admittance Y_{bp}^{vL} for the Baseline and CM Screen module architecture shown in Figure 29 shows that the addition of impedance C_{screen} into the module architecture results in lower noise escaping the baseplate of the module and larger current being diverted back into the architecture, which reconfirms the conclusion drawn from Figure 26 and Figure 27.

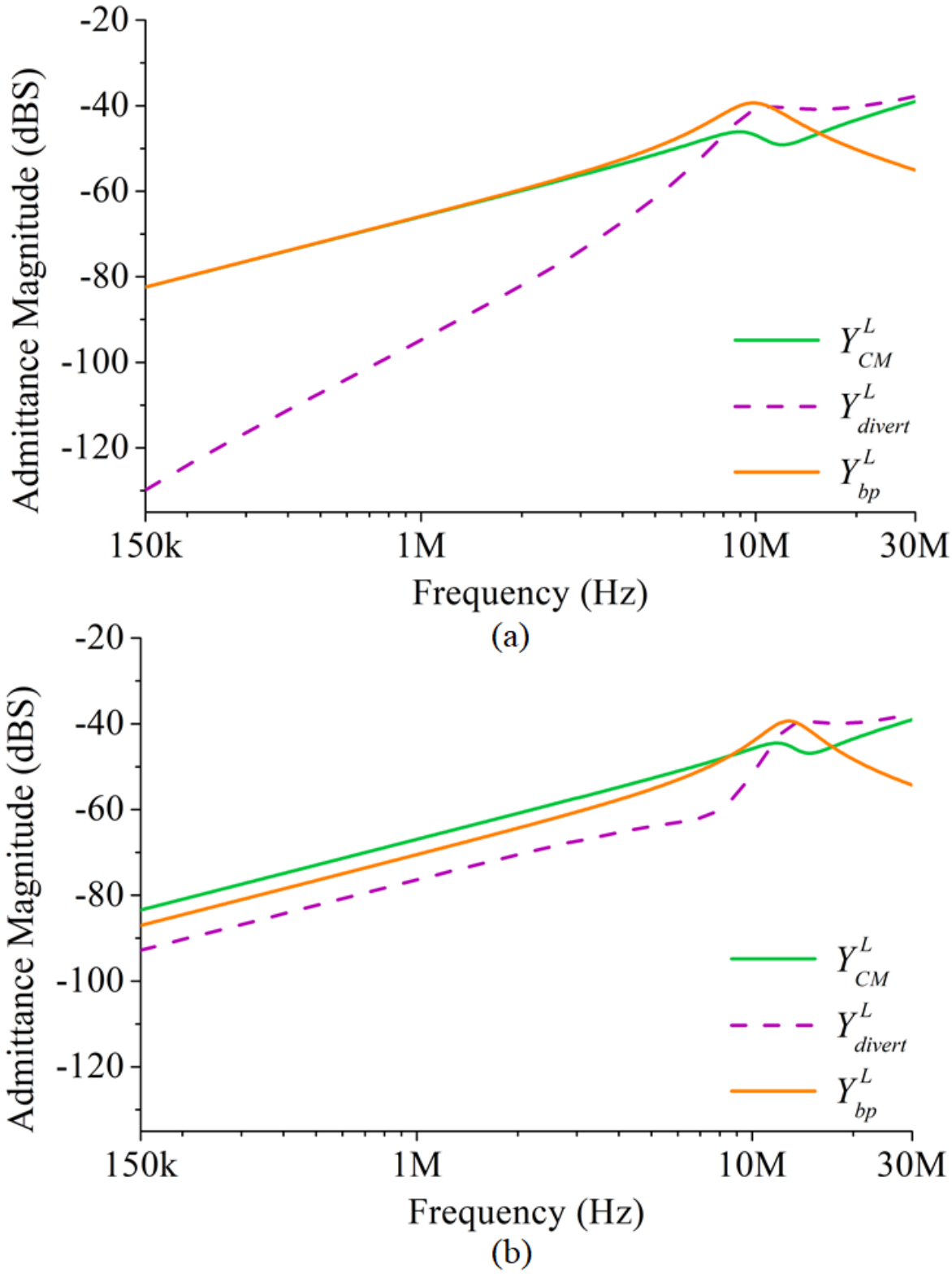


Figure 28: Admittance seen by current i_{CM} (Green), i_{divert} (Purple), and i_{bp} (Orange) as a function of voltage source v_L for (a) Baseline module (b) CM Screen module architecture.

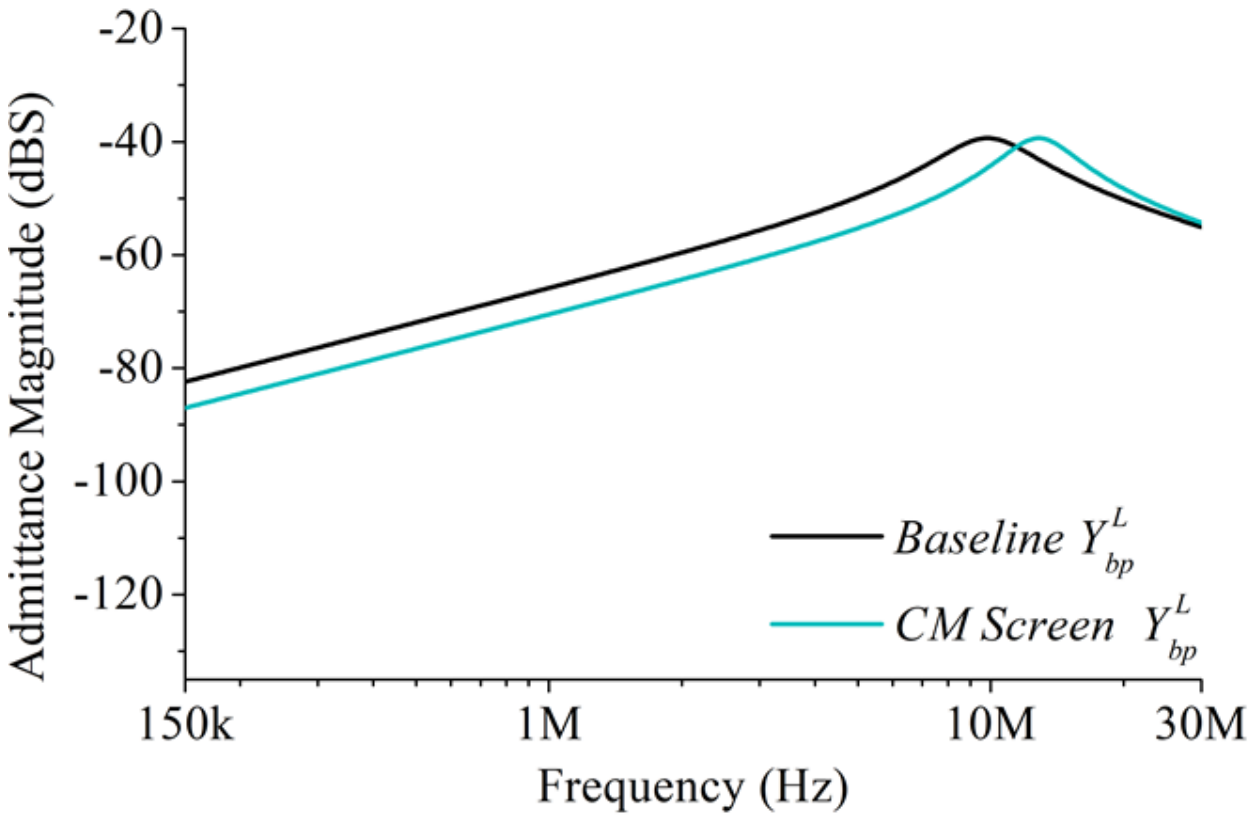


Figure 29: Admittance seen by current i_{bp} as a function of voltage source v_L for (a) Baseline module (Black) (b) CM Screen module (Teal) architecture.

5.3 Effect of Connecting CM screen to DC node in Module Architecture.

The stacked substrate architecture which consist of a screening layer between the power copper pads and the baseplate and the screening layer is connected to a node inside the module is now studied. Module architectures that fall into this category are referred to as CM Screen (DC Node) and CM Screen (DC Node, C_D) module architectures. Seven of the architectures studied fall into this category:

- CM Screen (DC+) module architecture (Figure 5(b) and Figure 18(f))
- CM Screen (DC+, C_D) module architecture (Figure 7(d) and Figure 18(g))

- CM Screen (DC-) module architecture (Figure 7(e) and Figure 18(h))
- CM Screen (DC-, C_D) module architecture (Figure 7(f) and Figure 18(i))
- CM Screen (DC Mid) module architecture (Figure 5(d) and Figure 18(j))
- CM Screen (DC+, DC-) module architecture (Figure 7(g) and Figure 18(k))
- CM Screen (DC+, DC-, C_D) module architecture (Figure 7(h) and Figure 18(l))

In this section, however, only the CM Screen (DC+), CM Screen (DC-) and CM Screen (DC Mid) module architectures will be discussed. The remaining architectures will be discussed in subsequent sections. Each of the three CM Screen (DC Node) architectures is replaced in the schematic of the simulation model in Figure 17(a), and the results for noise i_{bp} compared to the Baseline module is shown in Figure 30.

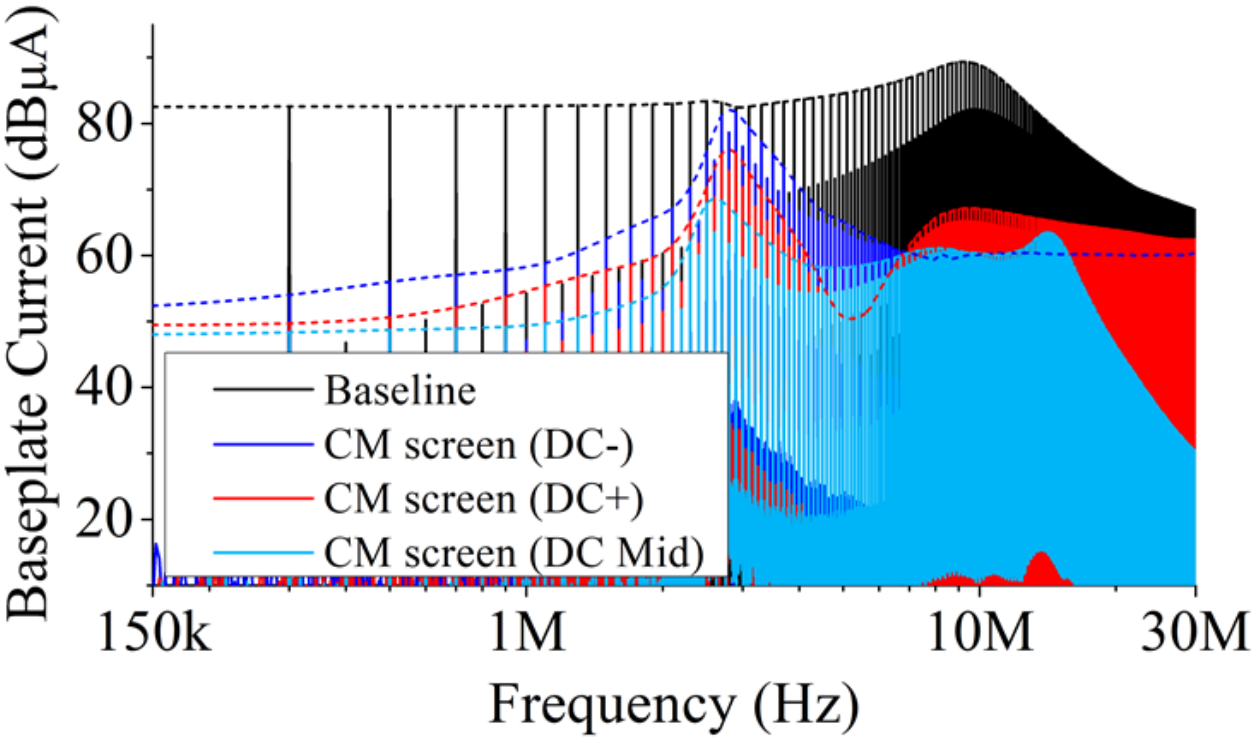
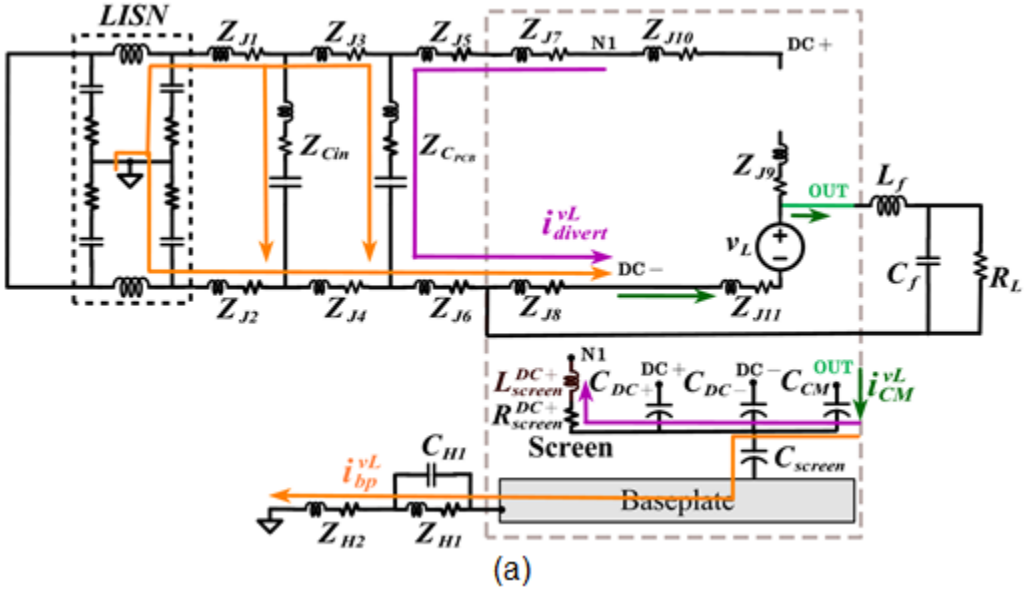


Figure 30: Noise generated at the baseplate with Baseline module (Black), and (a) CM Screen (DC-) module (Blue), CM Screen (DC+) module (Red) and CM Screen (DC Mid) module (Light Blue)

The individual trends seen in the frequency spectrum for the three CM Screen module architectures are explained. In the three module architectures, the roll-off — previously at ~9.9 MHz for the Baseline module — is now observed to occur at a lower frequency of ~8.29 MHz. This shift can be explained by looking at the CEM shown in Figure 18 and the equivalent CEM capacitance C_{eq} given in Table 5. For the three module architectures, the capacitance C_{eq} is defined according to equation (119) (assuming $C_D >> C_{CM}$):

$$C_{eq}^{CM\ Screen\ (DC\ Node)} \approx C_{screen} \tag{119}$$

A comparative analysis of the frequency spectrum for the three architectures is provided compared to the Baseline module. The CM Screen (DC+), CM Screen (DC-), and CM Screen (DC Mid) module architectures are analyzed. Figure 31 shows the superposition state of the voltage source v_L / v_H for the architectures discussed after being introduced into the time domain model (Figure 17).



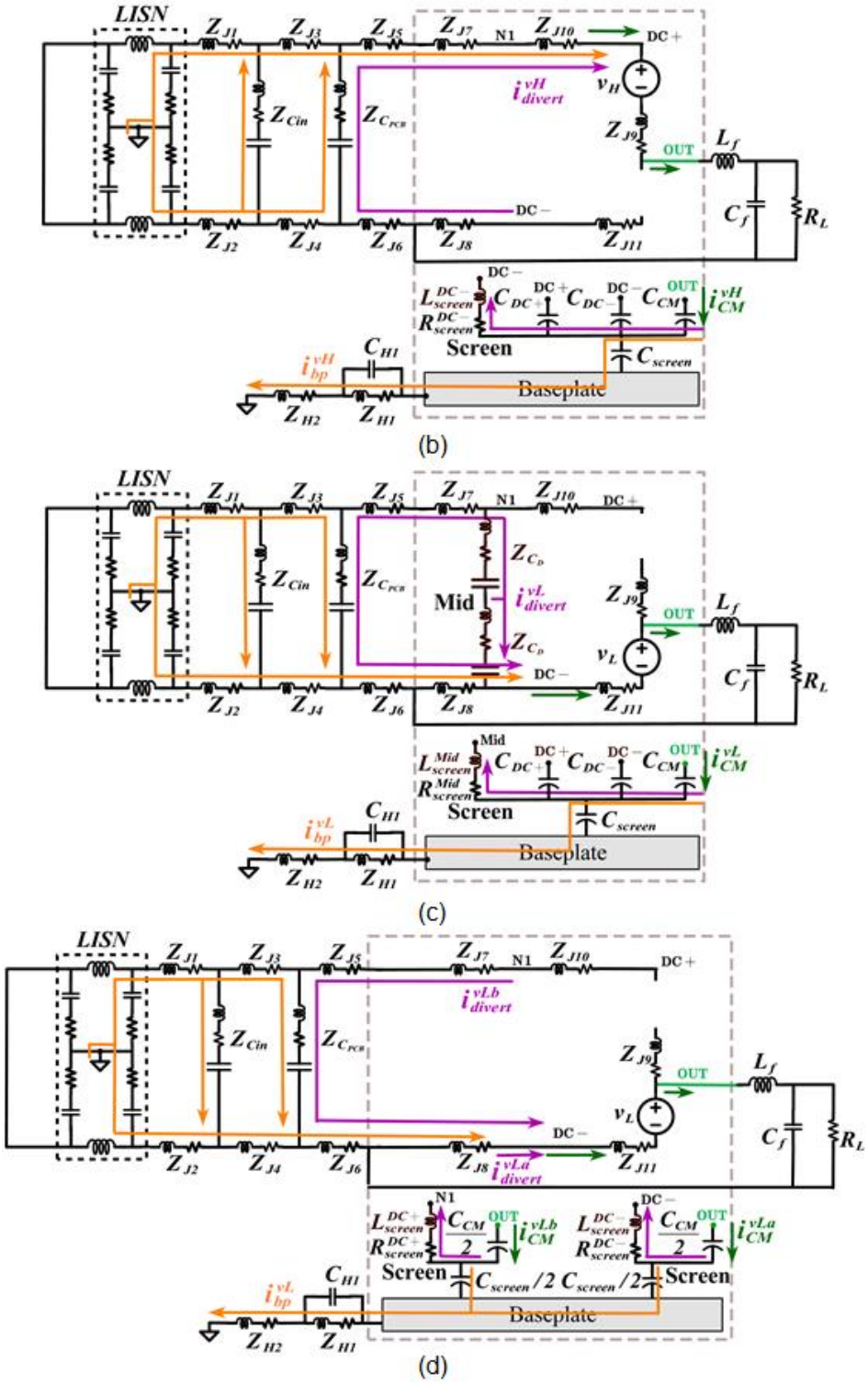


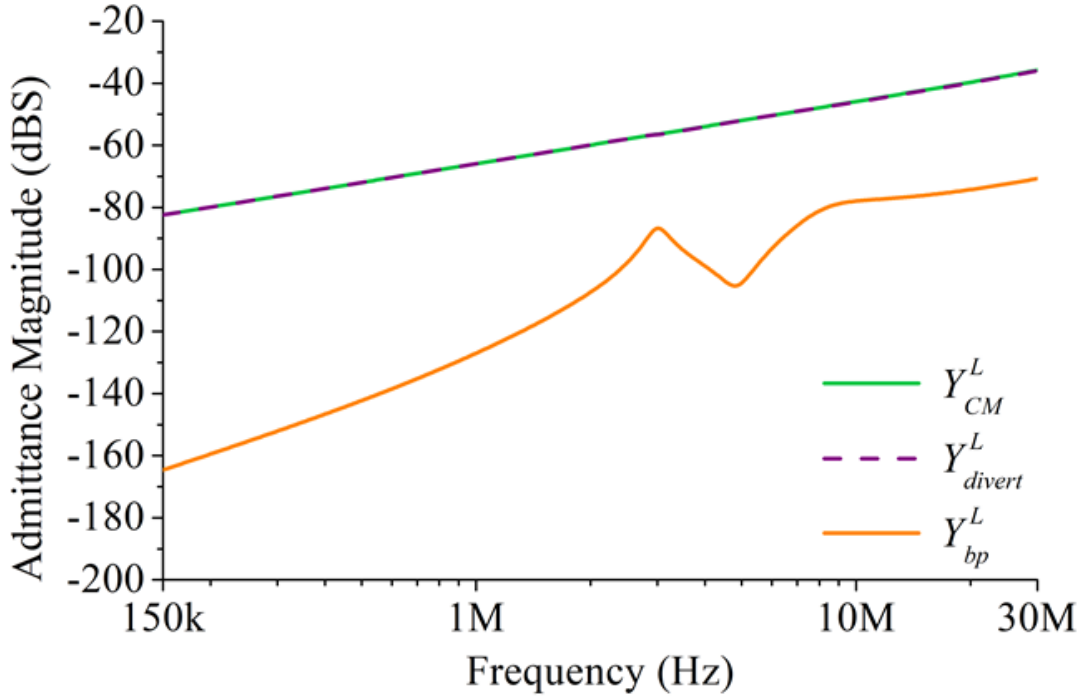
Figure 31: Converter schematic showing path taken by noise current i_{CM} flowing through C_{CM} due to (a) voltage source v_L in CM Screen (DC+) module (b) voltage source v_H in CM Screen (DC-) module (c) voltage source v_L in CM Screen (DC Mid) module and (d) voltage source v_L in CM Screen (DC+, DC-) module architecture.

It can be seen from Figure 30 that the three module architectures display a lower EMI footprint and higher noise mitigation compared to the Baseline module. From Figure 31, it can be observed that compared to the path available to i_{bp}^{vL} in the case of the Baseline module (Figure 27(a)), the i_{bp}^{vL} for the CM Screen (DC Node) modules (Figure 31(a) - (c)) now not only have an additional impedance in its path C_{screen} but also has a low impedance path back to the connected DC node from the CM screen: L_{screen} and R_{screen} (and Z_{C_D} in case of the CM Screen (DC Mid) module). This increase in impedance toward the baseplate and the availability of a low impedance path results in a significant increase in the noise diverted compared to the Baseline module. From Figure 31, it can be seen that if condition (120) or (121) is satisfied the majority of i_{CM} will prefer to be diverted away from the baseplate:

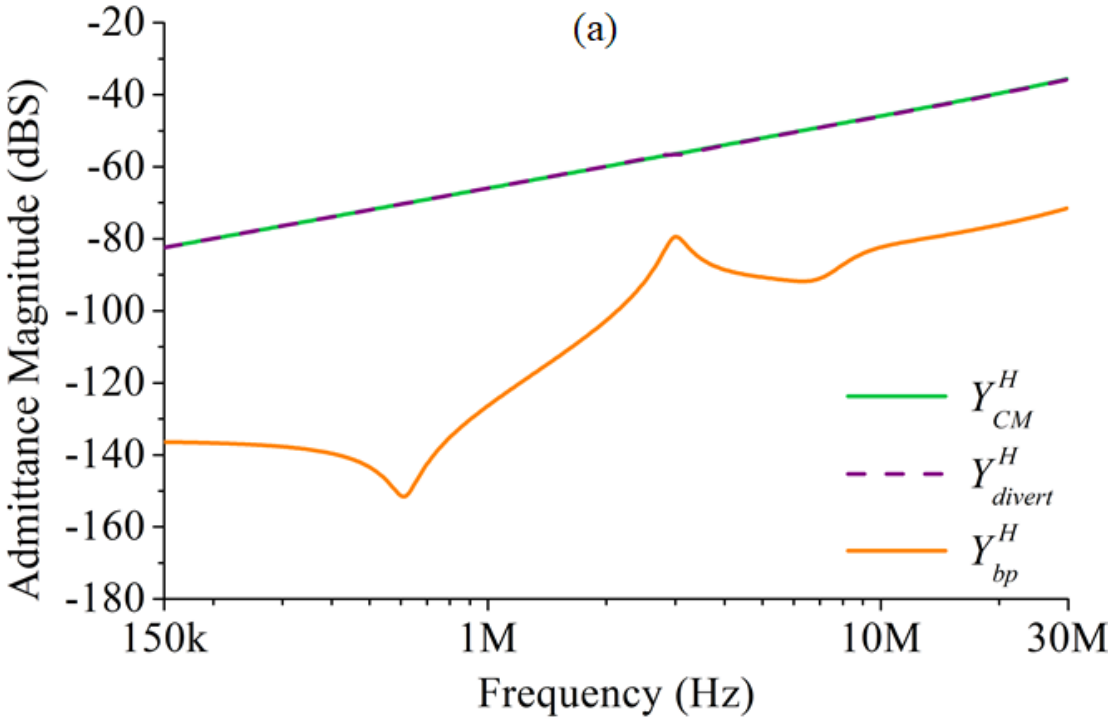
$$j\omega L_{screen} + R_{screen} \ll \frac{1}{j\omega C_{screen}} \tag{120}$$

$$j\omega L_{screen} + R_{screen} + Z_{C_D} \ll \frac{1}{j\omega C_{screen}} \tag{121}$$

The magnitude of the admittance Y seen by the current i_{CM}, i_{divert}, and i_{bp} as a function of voltage source v_L for the CM Screen (DC+) and CM Screen (DC Mid) module architecture, and magnitude of the admittance Y seen by the current i_{CM}, i_{divert}, and i_{bp} as a function of voltage source v_H for the CM Screen (DC-) module architecture is shown in Figure 32(a), (c), and (b), respectively. The magnitude of the admittance Y seen by the current i_{CM}, i_{divert}, and i_{bp} as a function of voltage source v_L for the CM Screen (DC+, DC-) module architecture is also shown in Figure 32(d).


-20
-40
-60
-80
-100
-120
-140
-160
-180
-200
Admittance Magnitude (dBS)
150k
1M
10M
30M
Frequency (Hz)
Y^L_{CM}
Y^L_{divert}
Y^L_{bp}

(a)


-20
-40
-60
-80
-100
-120
-140
-160
-180
Admittance Magnitude (dBS)
150k
1M
10M
30M
Frequency (Hz)
Y^H_{CM}
Y^H_{divert}
Y^H_{bp}

(b)

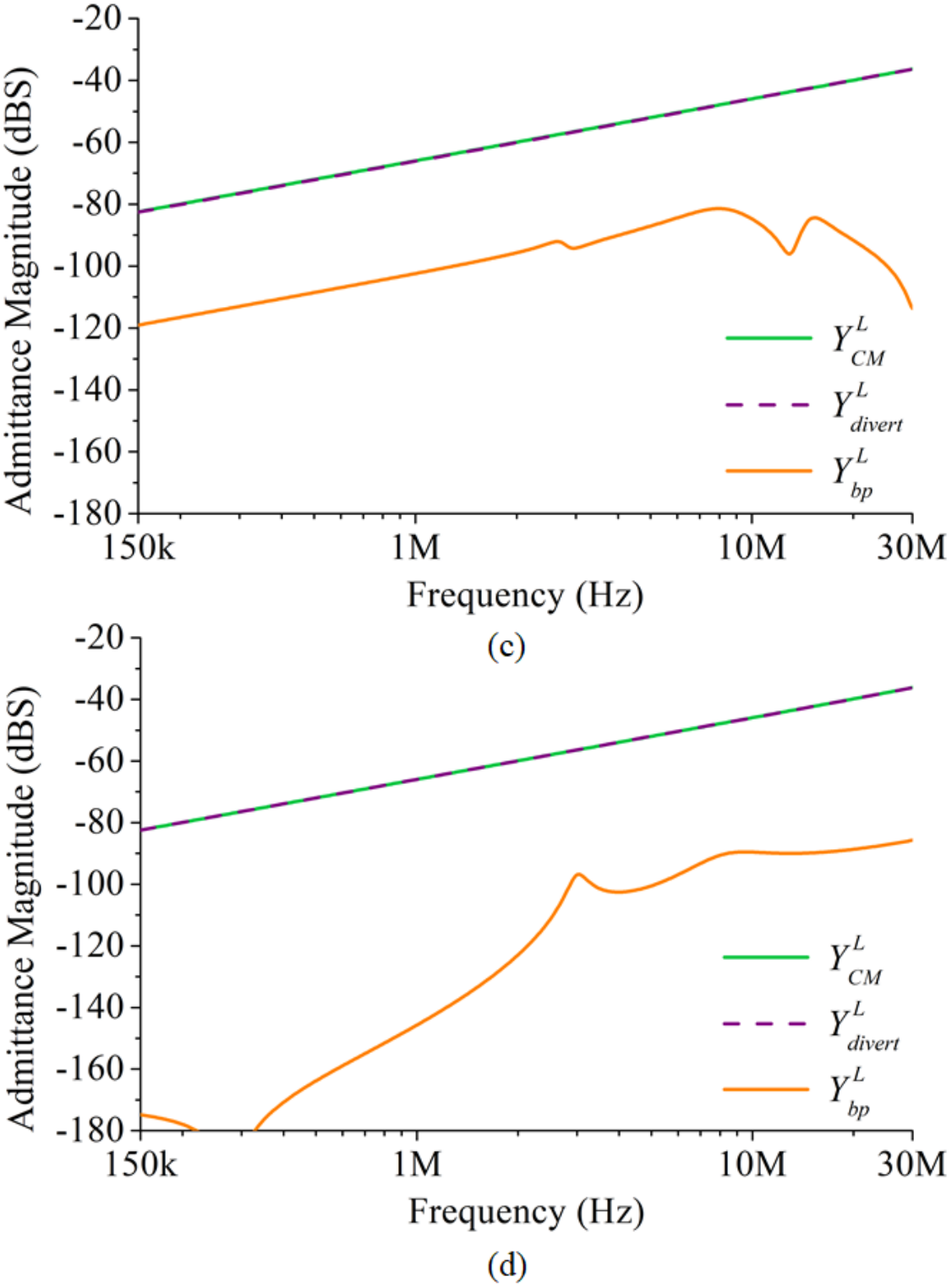


Figure 32: Admittance seen by current i_{CM} (Green), i_{divert} (Purple), and i_{bp} (Orange) as a function of voltage source v_L for (a) CM Screen (DC+) (b) CM Screen (DC-) (c) CM Screen (DC Mid) and (d) CM Screen (DC+, DC-) architecture.

It can be seen from Figure 32 that for the CM Screen (DC Node) module architectures, the magnitude of both Y_{CM}^{vL} and Y_{divert}^{vL} show similar behavior over the entire conducted EMI frequency range. This implies that for the entire conducted EMI frequency range, the current i_{CM} would prefer to be diverted back into the module architecture, rather than to escape through the baseplate. The admittance plots show that the addition of impedance C_{screen} and a low impedance path back to the connected DC node in to module architecture results in lower noise escaping the baseplate of the module and larger current being diverted back into the architecture, which can be confirmed from Figure 30.

5.4 Comparison of CM Screen (DC Node) Module Architectures

The EMI performance of different CM Screen (DC Node) module architectures is now compared. It can be seen from Figure 30 and Figure 32 that different CM Screen (DC Node) modules show different EMI behavior. This can be further confirmed from Figure 33 and Figure 34(a) where the noise current i_{bp} and the admittance Y_{bp} due to the voltage source for all four module architectures is plotted. However, it can be seen that the trends shown by the admittances plotted in Figure 34(a), do not match the trends seen in the frequency spectrums in Figure 33. This is primarily because the assumption that dv/dt is the major source of noise flowing at the baseplate of the converter in (111) and (112) is no longer valid. The major source of noise flowing at the baseplate is now the di/dt transients and instead of the admittance transfer function the current transfer function should be considered. This can be confirmed in Figure 34(b), where the trends seen in the current transfer function match closely with the trends seen in Figure 33. Figure 35 shows the superposition state of the current source i_L / i_H for the architectures discussed after being introduced into the time domain model (Figure 17).

It should be noted that di/dt transients having a larger effect on noise current i_{bp} than dv/dt transients is not due to the converter used being designed poorly. This can be confirmed from Figure 36 where the major portion of noise i_{bp} for the Baseline and Baseline (C_D) module is due to the dv/dt transients (Figure 36(a) and (b)) whereas for the CM Screen (DC+), CM Screen (DC-), CM Screen (DC Mid) and CM Screen (DC+, DC-) modules, the major portion of noise i_{bp} is due to di/dt transients (Figure 36(c) and (d)). It is instead because the CM Screen (DC node) modules effectively screen the noise generated due to the dv/dt as seen in Figure 32, thereby resulting in di/dt being the major source of noise. Instead of only considering the admittance transfer functions, the current transfer function for the CM Screen (DC node) modules is also informative and should be plotted.

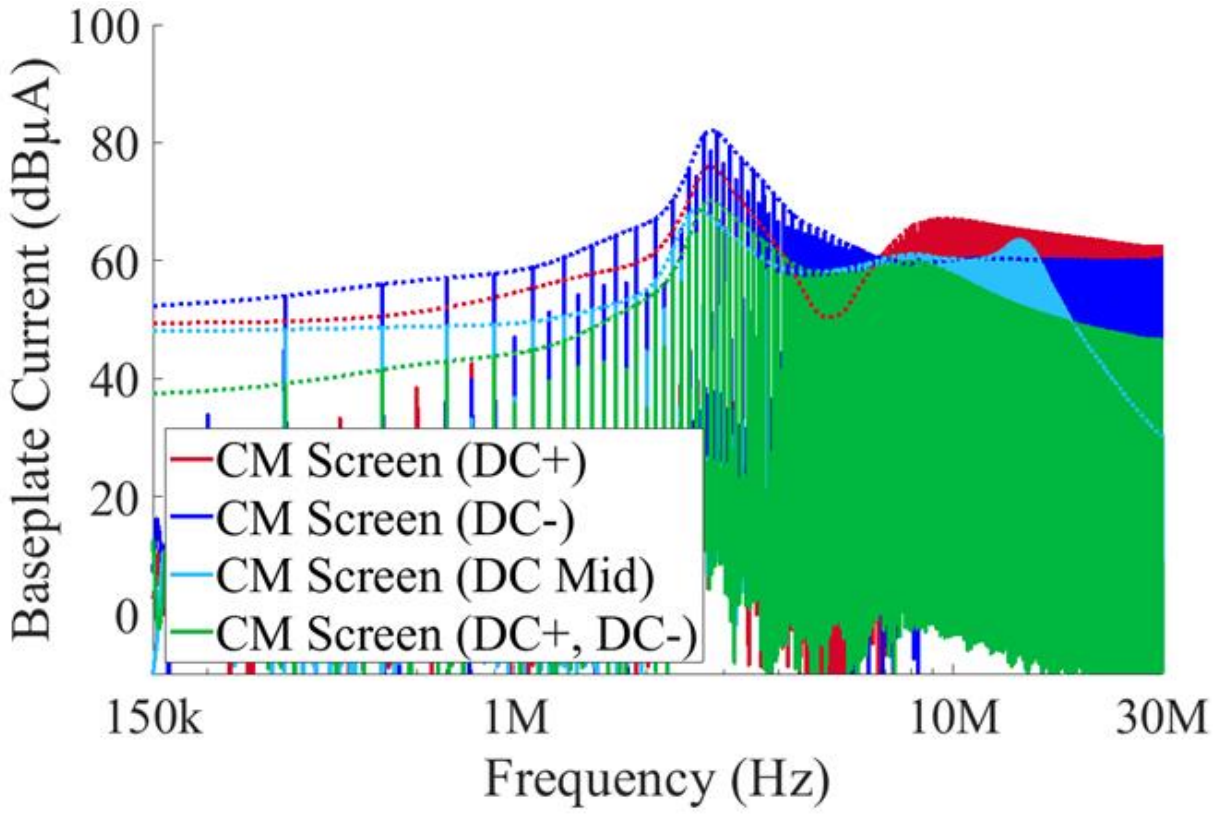


Figure 33: Noise current i_{bp} for CM Screen (DC-) (Blue), CM Screen (DC+) (Red), CM Screen (DC Mid) (Light Blue), and CM Screen (DC+, DC-) (Green)

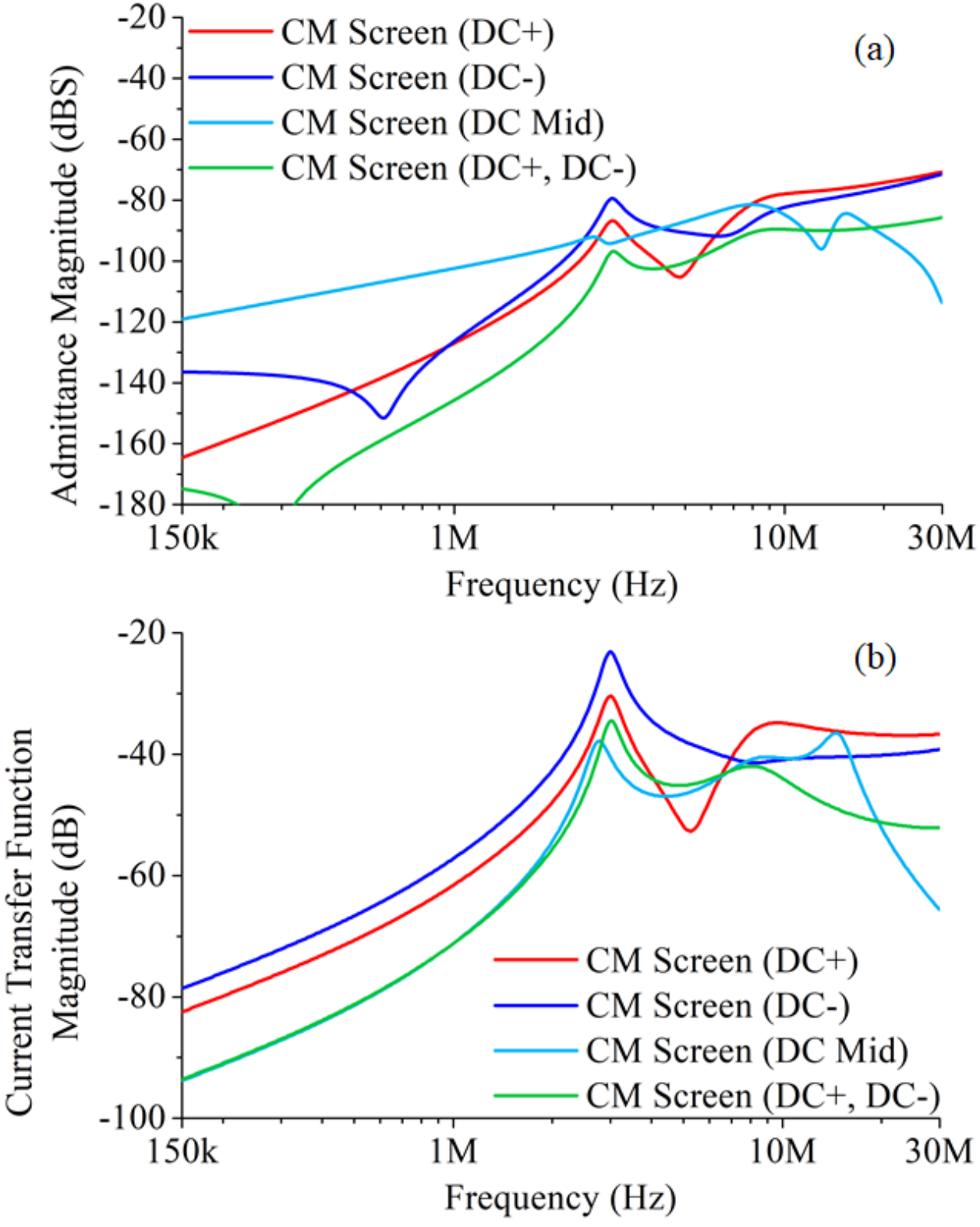
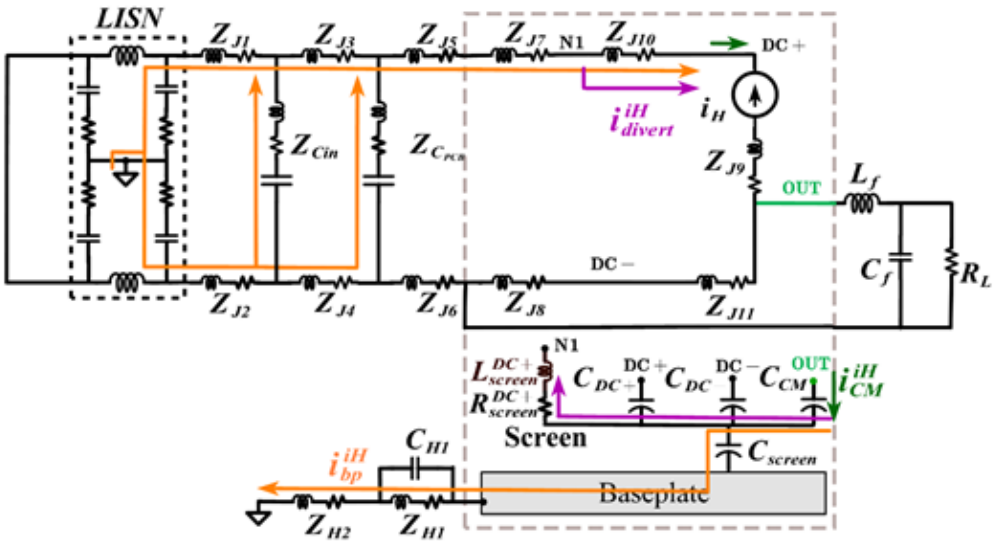
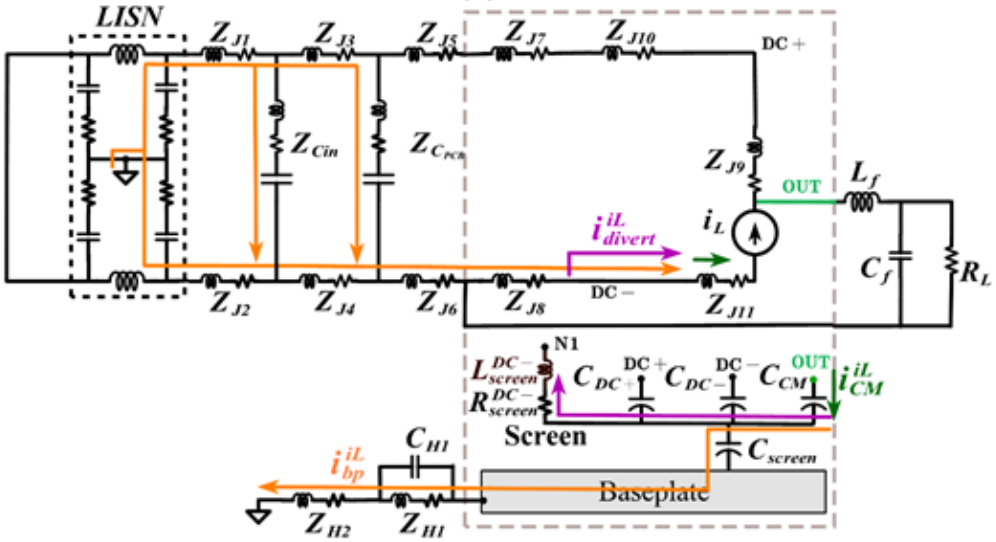


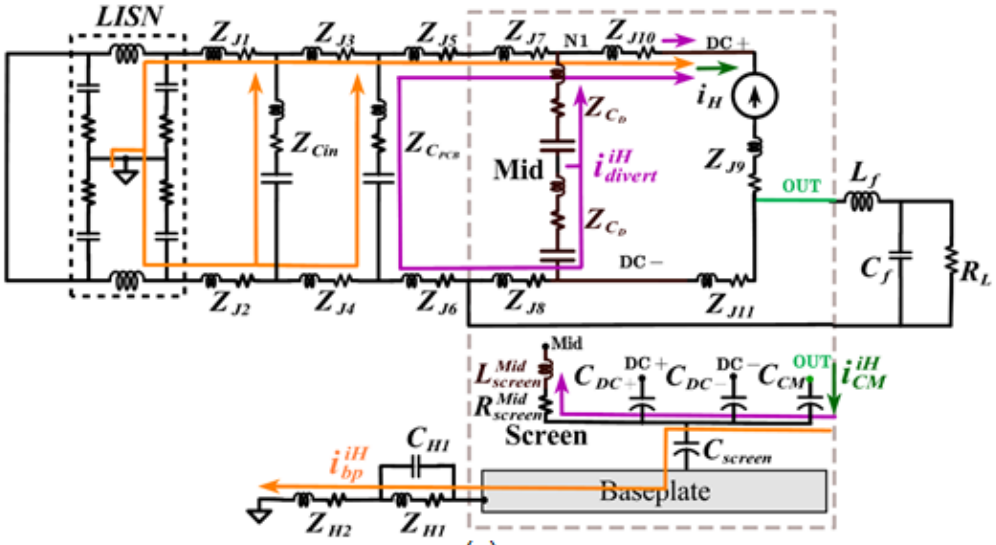
Figure 34: (a) Admittance transfer function and (b) Current transfer function for all four CM Screen module architecture.


LISN
N1
DC +
DC −
OUT
Screen
Baseplate

(a)


LISN
N1
DC +
DC −
OUT
Screen
Baseplate

(b)


LISN
N1
Mid
DC +
DC −
OUT
Screen
Baseplate

(c)

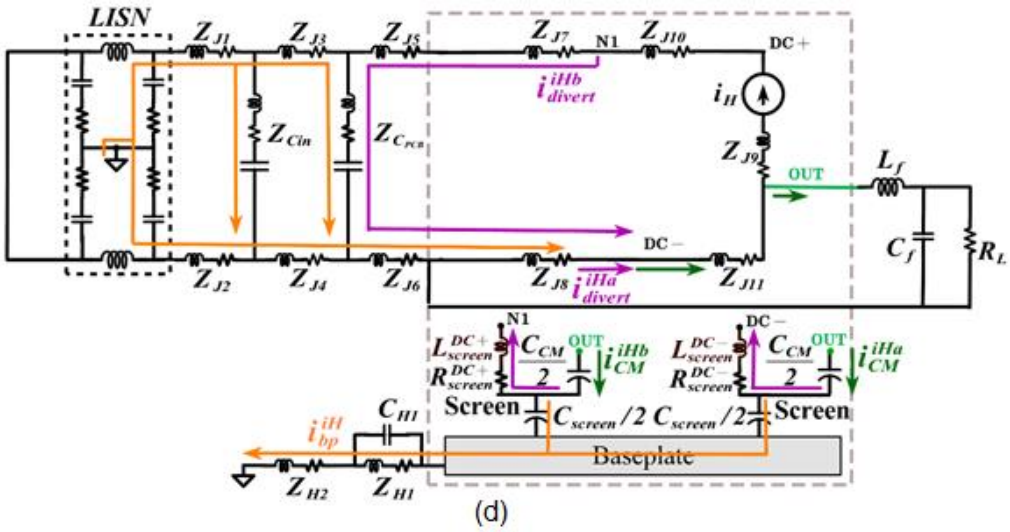
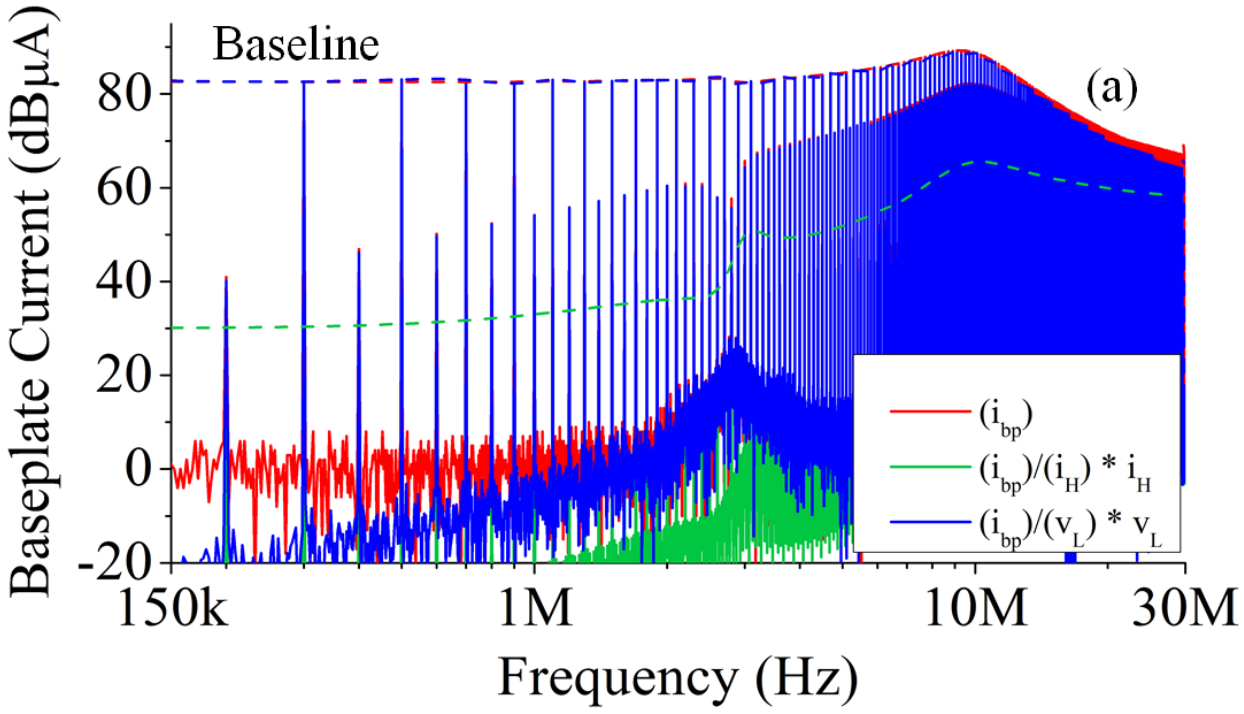
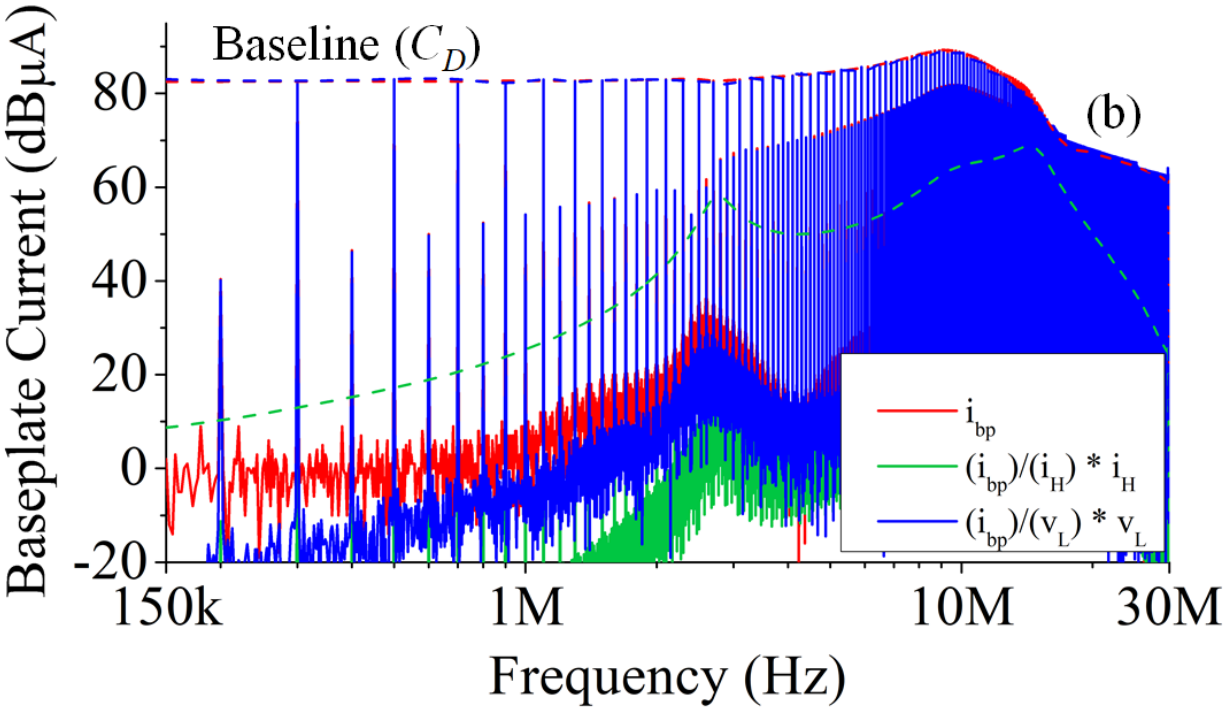
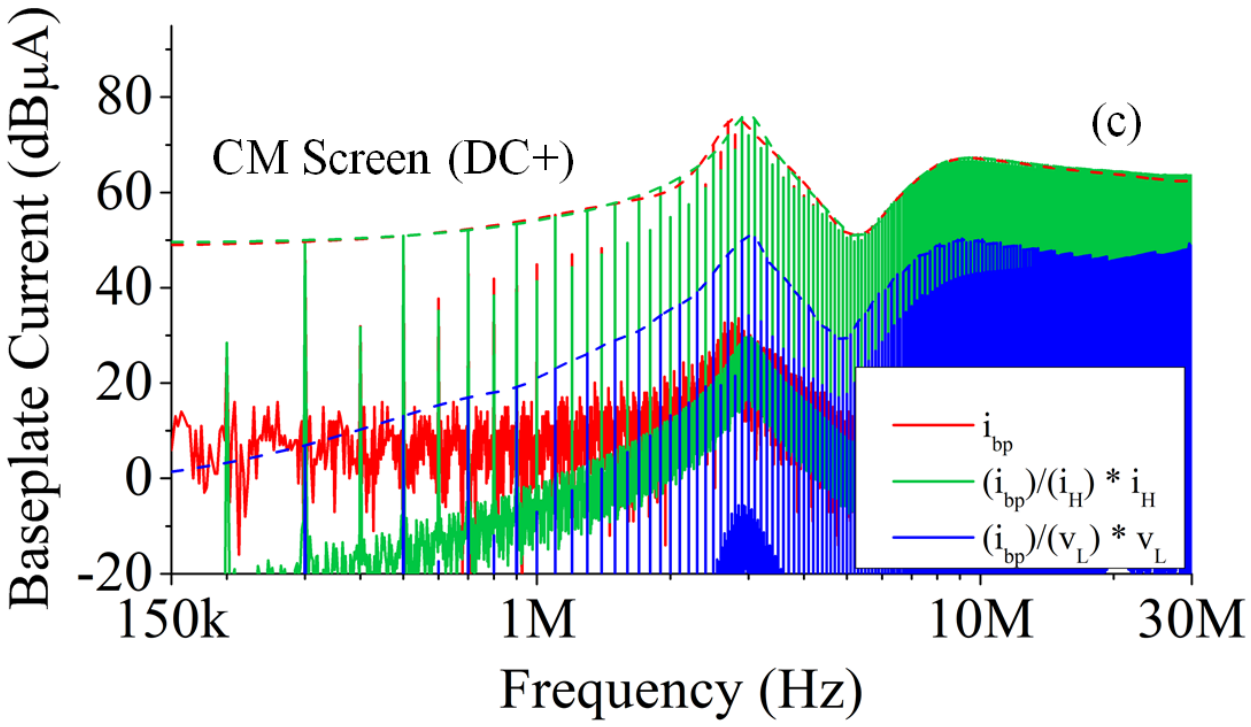
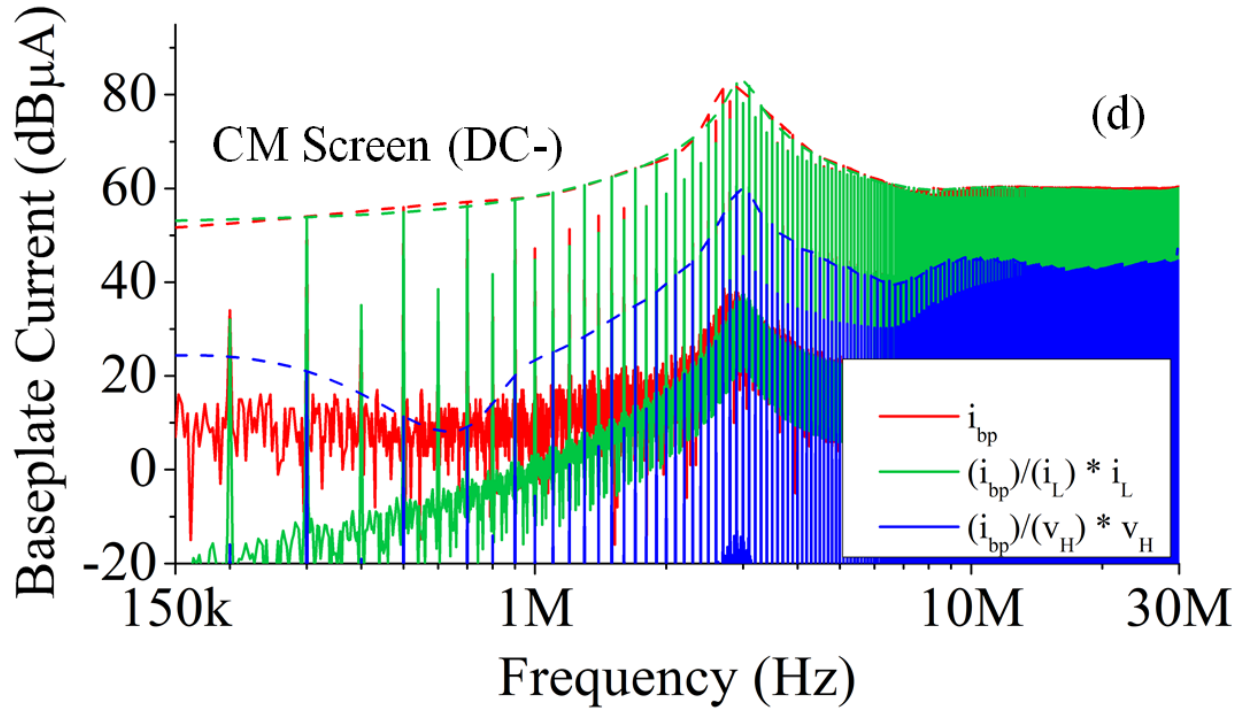


Figure 35: Converter schematic showing path taken by noise current i_{CM} flowing through C_{CM} due to (a) current source i_H in CM Screen (DC+) module (b) current source i_L in CM Screen (DC-) module (c) current source i_H in CM Screen (DC Mid) module and (d) current source i_H in CM Screen (DC+, DC-) module


Baseline
(a)
Baseplate Current (dBμA)
80
60
40
20
0
-20
150k
1M
10M
30M
Frequency (Hz)
(i_bp)
(i_bp)/(i_H) * i_H
(i_bp)/(v_L) * v_L


Baseline (C_D)
(b)
Baseplate Current (dBμA)
80
60
40
20
0
-20
150k
1M
10M
30M
Frequency (Hz)
i_bp
(i_bp)/(i_H) * i_H
(i_bp)/(v_L) * v_L


Baseplate Current (dBμA)
80
60
40
20
0
-20
CM Screen (DC+)
(c)
i_{bp}
$(i_{bp})/(i_H) * i_H$
$(i_{bp})/(v_L) * v_L$
150k
1M
10M
30M
Frequency (Hz)


Baseplate Current (dBμA)
80
60
40
20
0
-20
CM Screen (DC-)
(d)
i_{bp}
$(i_{bp})/(i_L) * i_L$
$(i_{bp})/(v_H) * v_H$
150k
1M
10M
30M
Frequency (Hz)

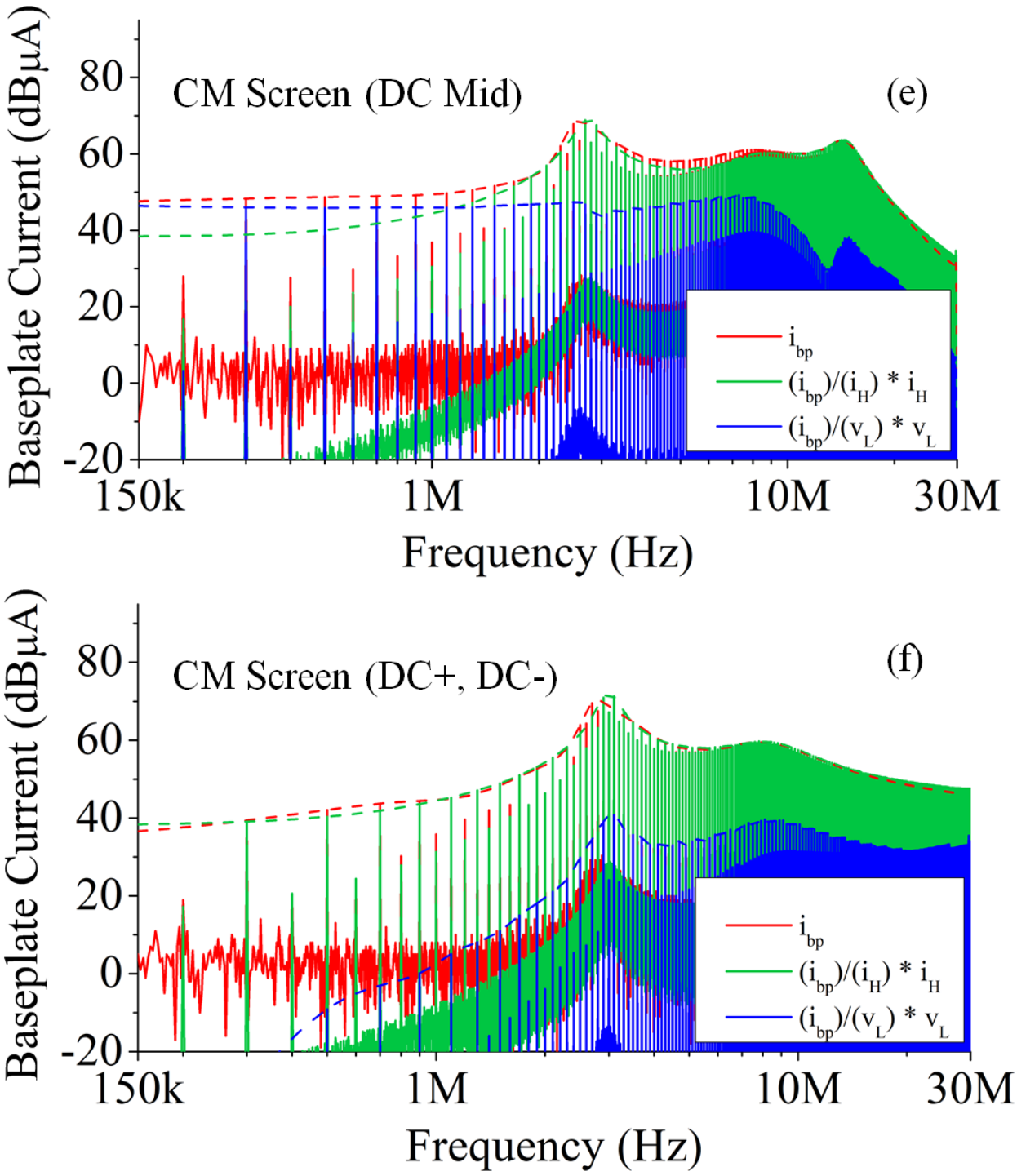


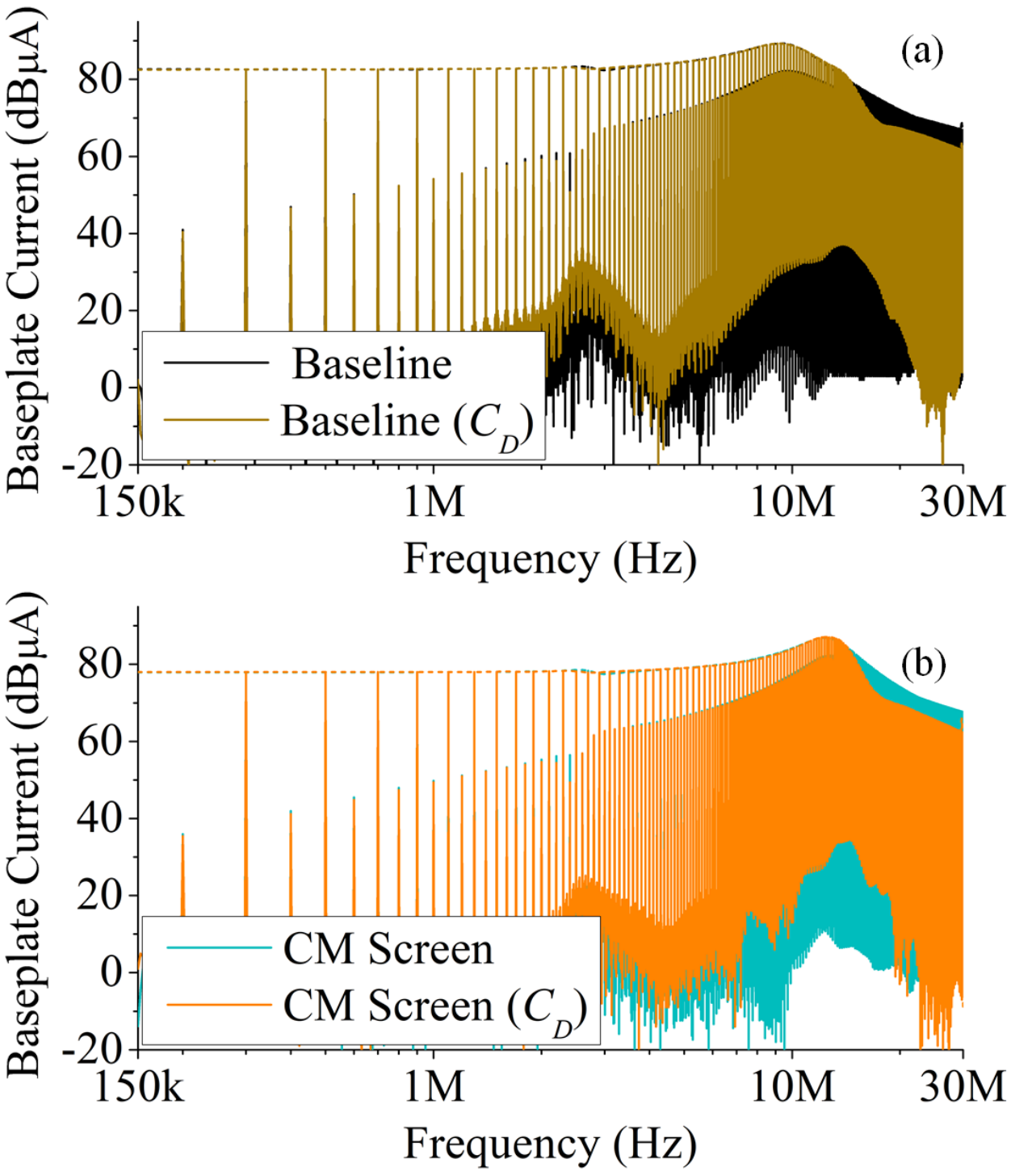
Figure 36: Frequency spectrum of noise current i_{bp} (Red), product of current transfer function and current source i_H (Green) and product of admittance transfer function and voltage source v_L (Blue) for (a) Baseline module (b) CM Screen (DC+) module (c) CM Screen (DC-) module (d) CM Screen (DC Mid) module and (e) CM Screen (DC+, DC-) module.

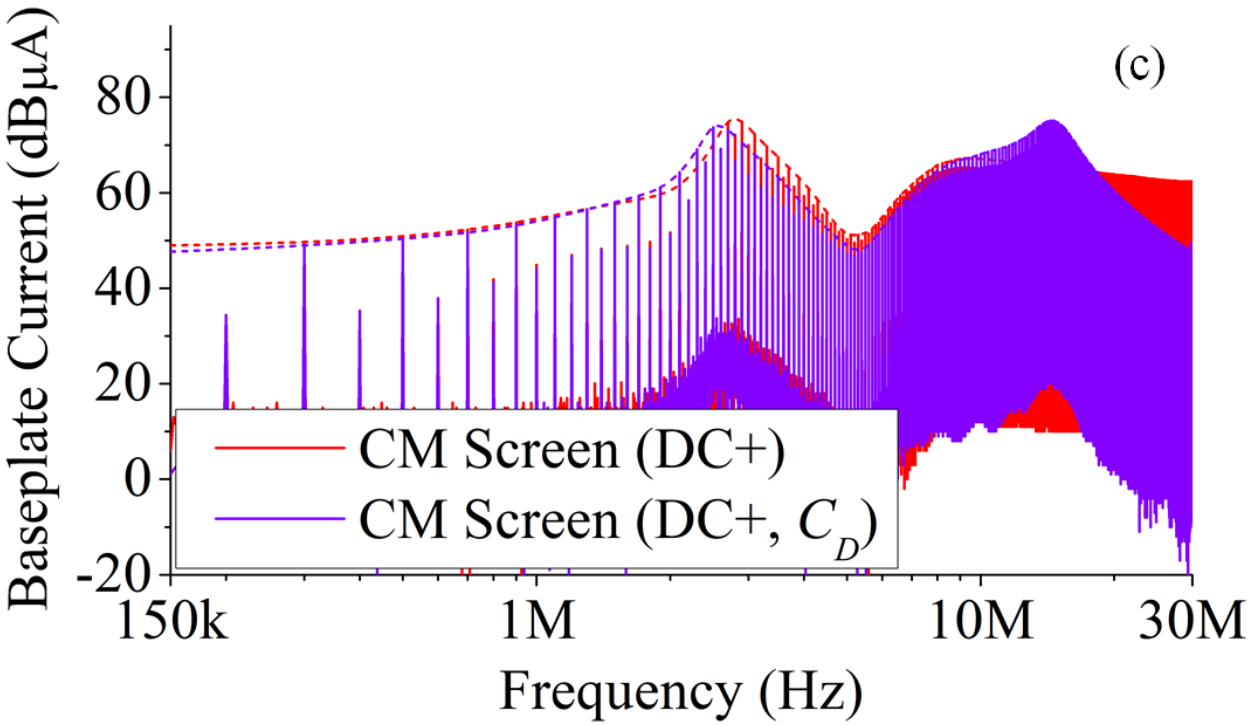
5.5 Effect of Integrating Decoupling Capacitors (C_D) into Module

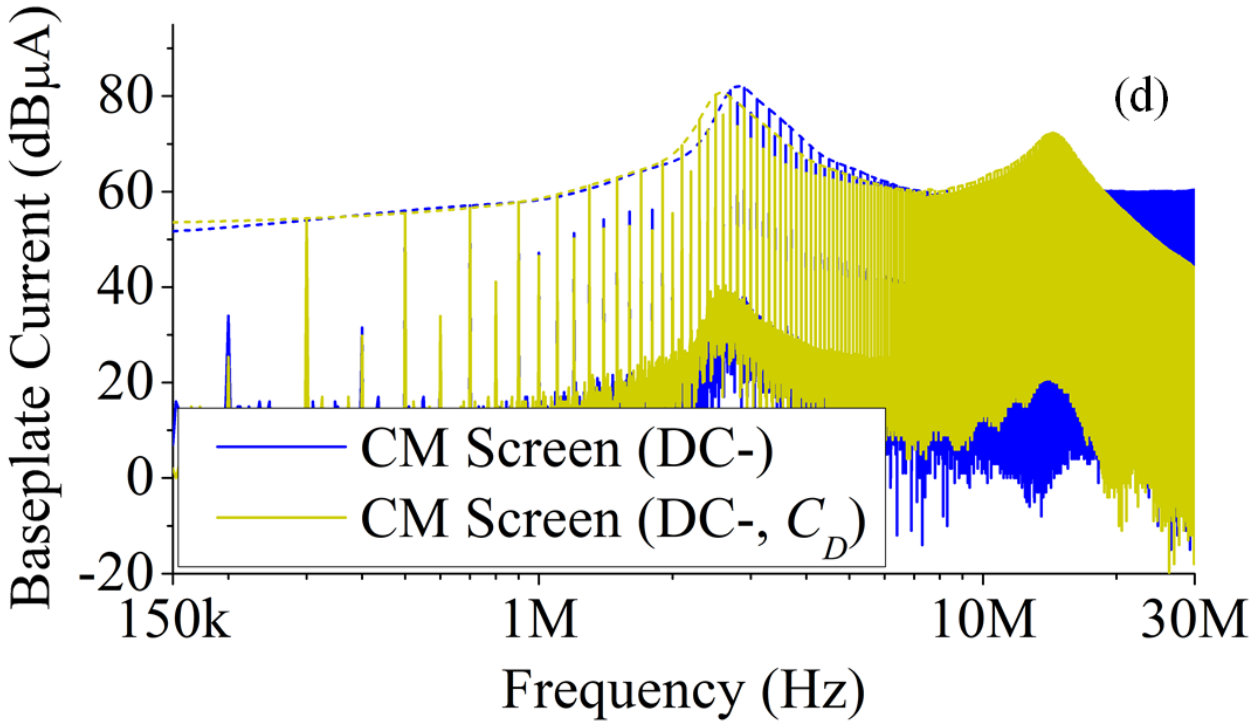
The decoupling capacitor architectures are the architectures which consist of decoupling capacitors into the module. Five of the architectures studied fall into this category:

- Baseline (C_D) module architecture (Figure 5(b) and Figure 18(b))
- CM Screen (C_D) module architecture (Figure 7(c) and Figure 18(e))
- CM Screen (DC+, C_D) module architecture (Figure 7(d) and Figure 18(g))
- CM Screen (DC-, C_D) module architecture (Figure 7(f) and Figure 18(i))
- CM Screen (DC+, DC-, C_D) module architecture (Figure 7(h) and Figure 18(l))

Each of the decoupling capacitor module architecture is replaced in the schematic of the simulation model in Figure 17(a). The result for noise i_{bp} is then compared to the same module architecture without the decoupling capacitor. Comparison of the noise i_{bp} generated by the Baseline and Baseline (C_D), CM Screen and CM Screen (C_D), CM Screen (DC+) and CM Screen (DC+, C_D), CM Screen (DC-) and CM Screen (DC-, C_D), and CM Screen (DC+, DC-) and CM Screen (DC+, DC-, C_D) module architectures is shown in Figure 37. The Baseline (C_y) capacitors and CM Screen (DC Mid) module architecture is not discussed in this section.


(a)
Baseplate Current (dBμA)
80
60
40
20
0
-20
Baseline
Baseline (C_D)
150k
1M
10M
30M
Frequency (Hz)
(b)
Baseplate Current (dBμA)
80
60
40
20
0
-20
CM Screen
CM Screen (C_D)
150k
1M
10M
30M
Frequency (Hz)


(c)
Baseplate Current (dBμA)
80
60
40
20
0
-20
150k
1M
10M
30M
Frequency (Hz)
CM Screen (DC+)
CM Screen (DC+, C_D)


(d)
Baseplate Current (dBμA)
80
60
40
20
0
-20
150k
1M
10M
30M
Frequency (Hz)
CM Screen (DC-)
CM Screen (DC-, C_D)

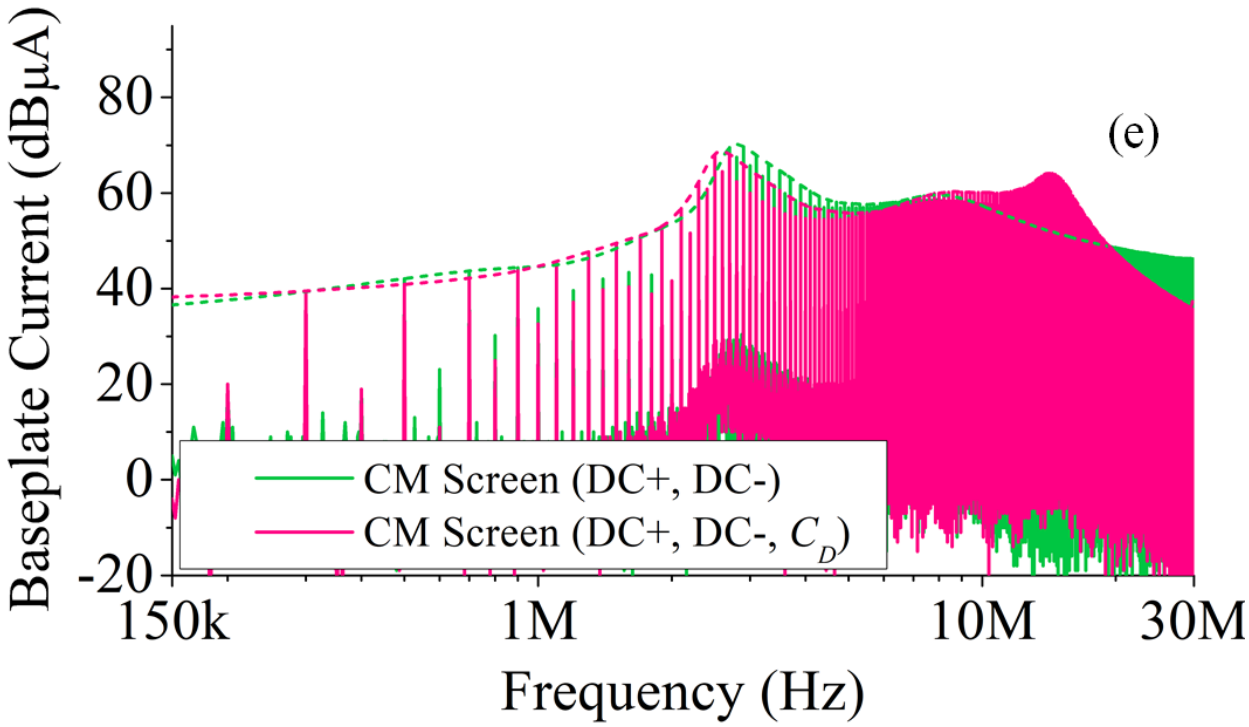


Figure 37: Noise generated at the baseplate with (a) Baseline module (Black), and Baseline (C_D) module (Brown) (b) CM Screen module (Teal), and CM Screen (C_D) module (Orange) (c) CM Screen (DC+) module (Red), and CM Screen (DC+, C_D) module (Purple) (d) CM Screen (DC-) module (Blue), and CM Screen (DC-, C_D) module (Yellow) (e) CM Screen (DC+, DC-) module (Green) and CM Screen (DC+, DC-, C_D) module (Pink).

From Figure 37 it can be determined that the module architectures with the integrated decoupling capacitors see a change in the slope of the roll off at ~13.5 MHz. This change in slope is due to the resonance interaction of the parasitic inductances with the integrated decoupling capacitors as outlined in purple in Figure 38(a). It can also be seen from Figure 37(c)-(e) that the addition of decoupling capacitors results in the resonance peak at ~2.7 MHz to move to a slightly lower resonance frequency. The resonance peak seen at ~2.7 MHz in the module architectures is due to the resonance interaction of the parasitic inductances with the PCB decoupling capacitors C_{PCB} and integrated decoupling capacitors C_D as outlined in purple in Figure 38(b).

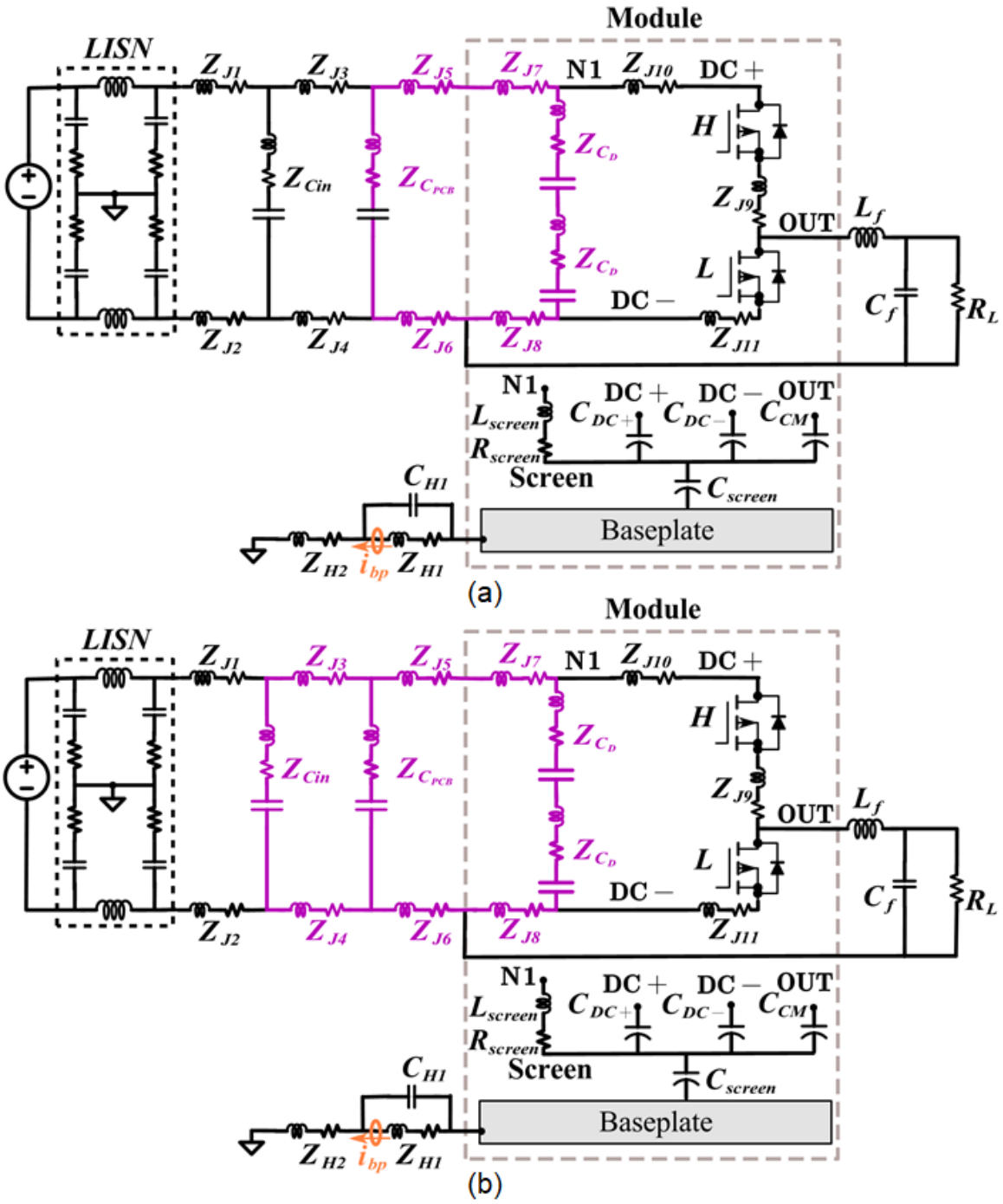


Figure 38: Parasitic inductances that resonate with (a) integrated decoupling capacitors C_D resulting in the change of slope of roll off at ~13.5 MHz (b) PCB decoupling capacitors C_{PCB} and integrated decoupling capacitors C_D resulting in peak at ~2.7 MHz.

The addition of decoupling capacitors on the noise generated can also reduce the inductance in the current commutation loop during switching, therefore reducing ringing. The

reduced ringing then results in lower noise being generated at higher frequencies of the conducted EMI frequency range (Figure 39).

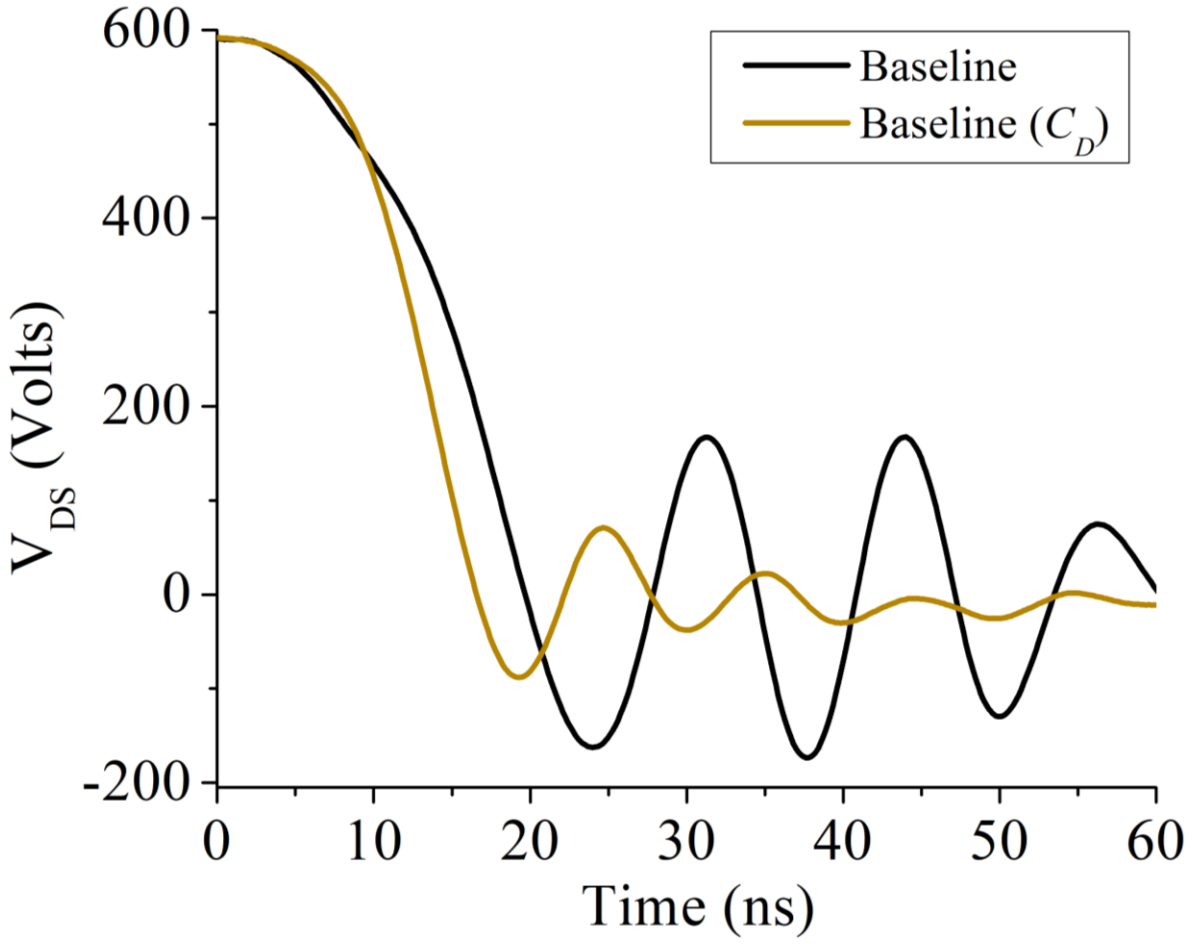


Figure 39: Experimental results showing the effect of integrating decoupling capacitors into module on slew rate and ringing in Baseline and Baseline (C_D) module.

5.6 Effect of Integrating Filter Capacitors (C_y) into Module

The effect of integrating decoupling capacitors into the module architecture and shorting the midpoint formed by the series connection of the decoupling capacitors with the baseplate or CM Screen is now analyzed. Two of the architectures studied fall into this category:

- Baseline (C_y) module architecture (Figure 7(a) and Figure 18(c))
- CM Screen (DC Mid) module architecture (Figure 5(d) and Figure 18(j))

The two module architectures are replaced in the schematic of the simulation model in Figure 17(a). The result for noise i_{bp} is then compared to the Baseline module. Noise i_{bp} generated by the Baseline (C_y) module architecture compared to the Baseline module architecture is shown in Figure 40(a). Noise i_{bp} generated by the CM Screen (DC Mid) module architecture compared to the Baseline module architecture is shown in Figure 40(b). Before the admittance and current transfer function for each module is compared, the decomposition of noise current i_{bp} generated due to dv/dt and di/dt is looked into. Figure 41 shows the decomposition of the portion of noise current i_{bp} due to dv/dt and di/dt for the Baseline (C_y) module. Figure 36(d) shows the decomposition of the portion of noise current i_{bp} due to dv/dt and di/dt for the CM Screen (DC Mid) module. It can be seen from Figure 41 and Figure 36(d) that for both the module architectures the noise generated at lower frequencies of the conducted EMI frequency range is majorly due to dv/dt transients, and the noise generated at higher frequencies of the conducted EMI frequency range is majorly due to di/dt. The admittance and current transfer function for the Baseline (C_y) and CM Screen (DC Mid) module architecture compared to the Baseline module architecture is shown in Figure 42.

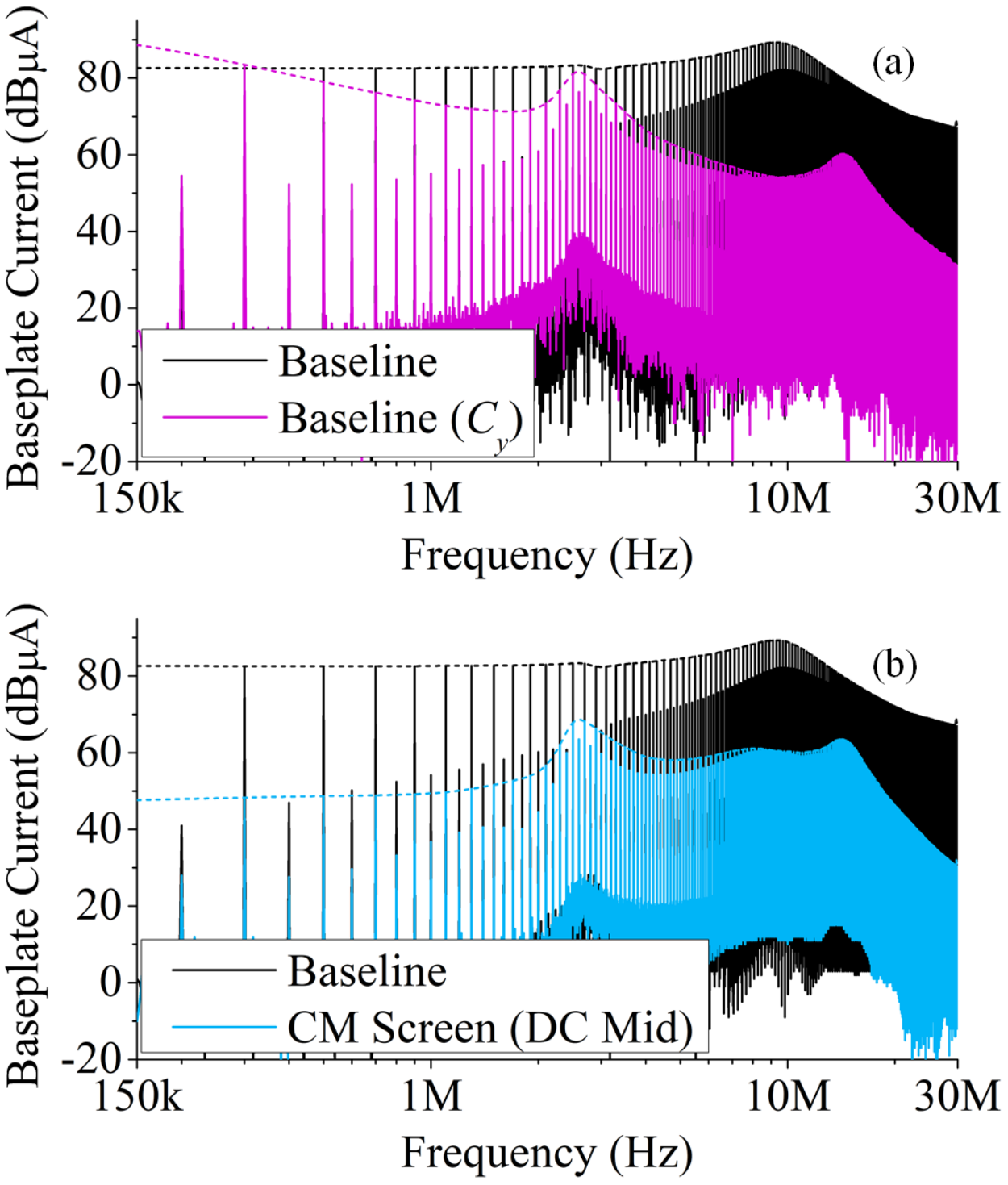


Figure 40: Noise generated at the baseplate with (a) Baseline module (Black), and Baseline (C_y) module (Purple) (b) Baseline module (Black) and CM Screen (DC Mid) module (Light Blue)

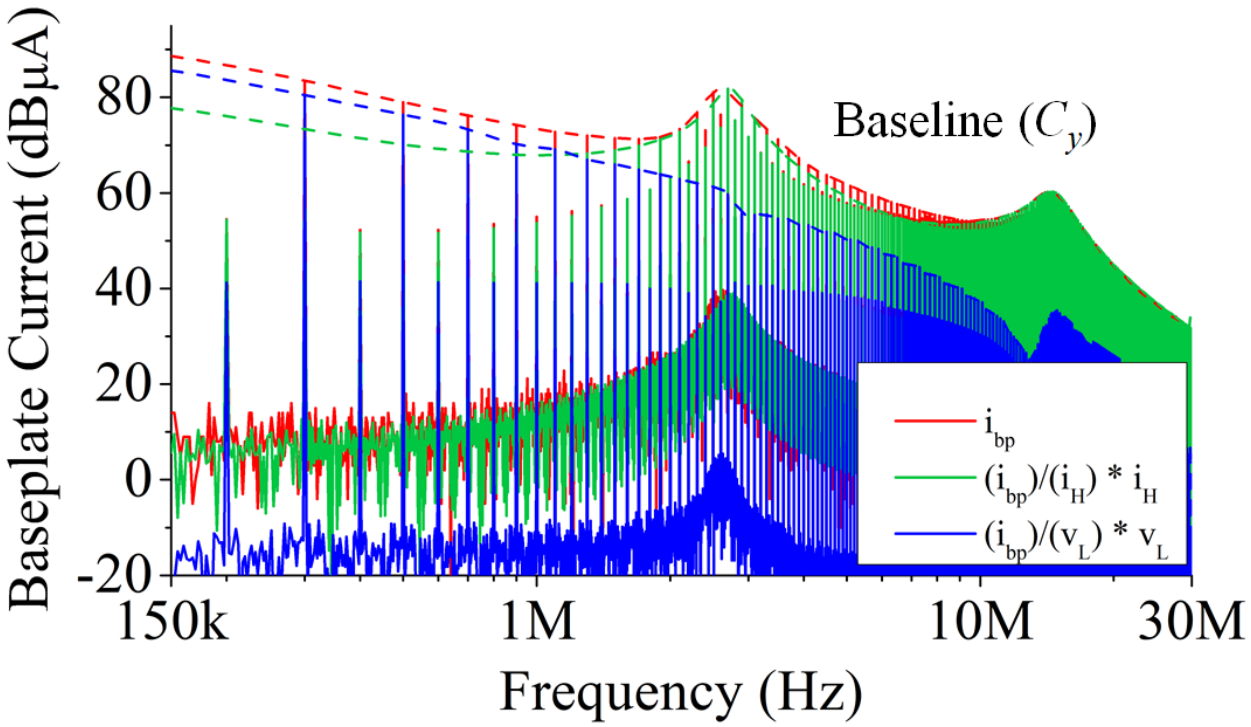


Figure 41: Frequency Spectrum of noise current i_{bp} (Blue), product of current transfer function and current source i_H (Green) and product of admittance transfer function and voltage source v_L (Red) for Baseline (C_y) module.

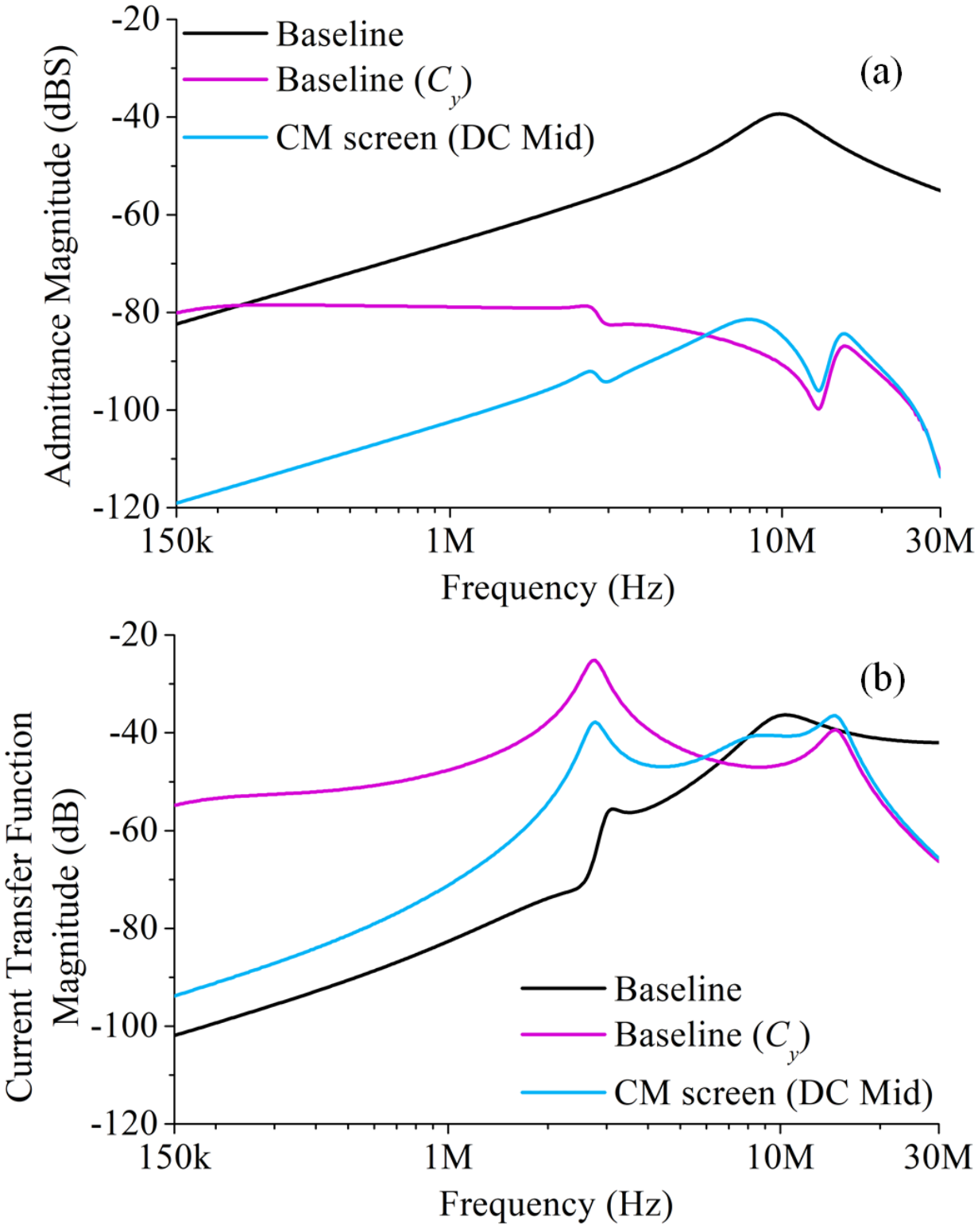


Figure 42: (a) Admittance transfer function Y_{bp} and (b) Current transfer function K_{bp} for Baseline module (Black), Baseline (C_y) module (Purple) and CM Screen (DC Mid) module (Light Blue) architecture.

Unlike the trends seen in the frequency spectrum of the Baseline and Baseline (C_D) modules (Figure 37(a)), the Baseline (C_y) module does not have the relatively flat frequency spectrum at lower frequencies of the conducted EMI frequency range (Figure 40(a)). This trend of the Baseline (C_y) module's frequency spectrum is explained by looking at the simplified CEM derived in Figure 24. For the Baseline (C_y) module, the capacitance C_{eq} is defined according to equation (122):

$$C_{eq}^{Baseline\,(C_y)} = 2C_D + C_{out} \tag{122}$$

As the capacitance C_{eq} has now increased the frequency at which the resonance interaction between L_{tot} and C_{tot} occurs moves to a lower frequency (~1.1 MHz). However, during the frequency range 300 kHz to 4 MHz the dominant impedance seen by the voltage source v_{CM} in Figure 24 is $R_{LISN1}/2$. This can be confirmed by plotting the impedance seen by v_{CM} in the CEM for the Baseline (C_y) module in Figure 43. As a result, no resonance interaction between L_{tot} and C_{tot} is seen. Since the CEM can be simplified to be a resistor in parallel with the noise source v_{cm} the envelope of the frequency spectrum of i_{bp} in this region would be similar to that seen in v_{cm}. This shows that although Baseline (C_y) module has the capability to provide a low EMI footprint, its performance ultimately depends strongly on the application the module is being used in. This is not the case for the CM Screen (DC Mid) module, in which the additional impedance provided by the capacitive coupling from the screen to the baseplate (C_{screen}), could be used to limit the current escaping the module architecture.

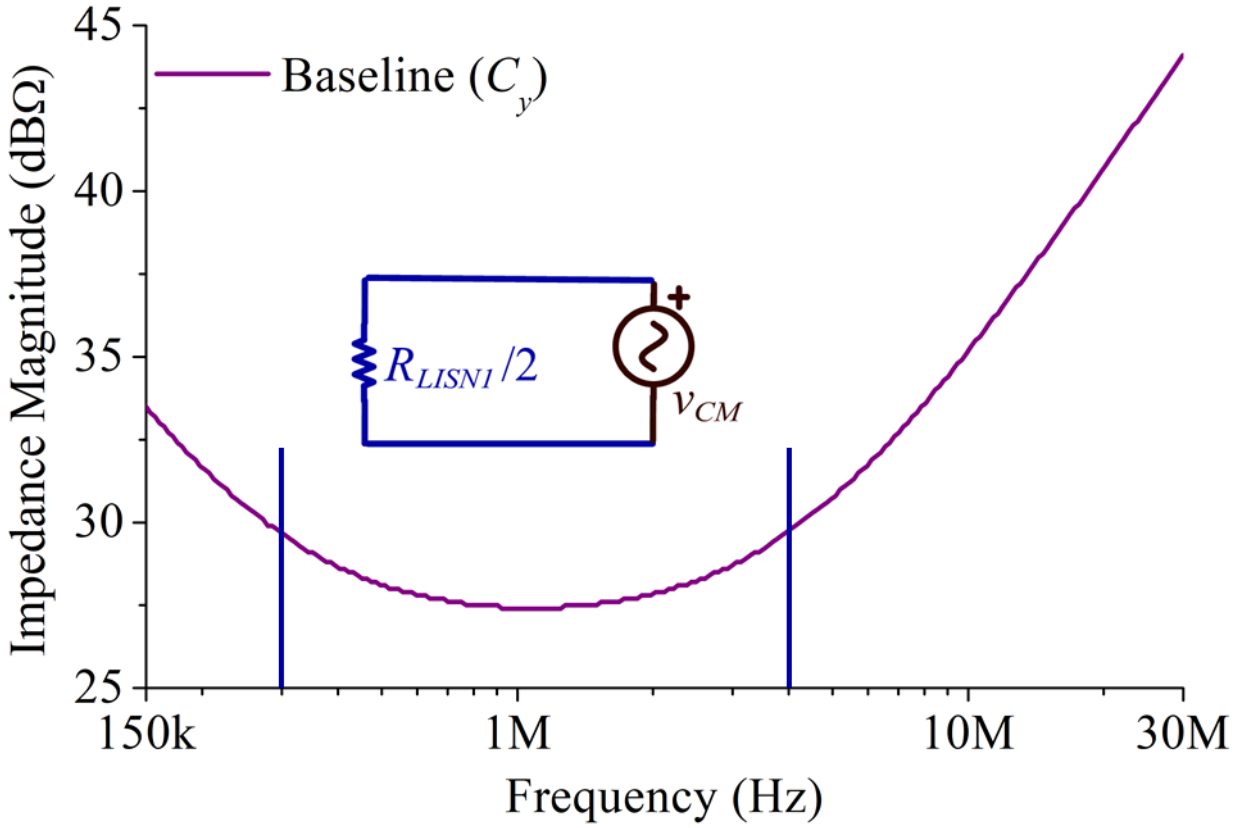


Figure 43: Impedance seen by v_{CM} for Baseline (C_y) module in the conducted EMI frequency range. Frequency range 300 kHz to 4 MHz marked on x-axis.

5.7 Lowest EMI Modules

The EMI performance of three lowest EMI footprint modules — CM Screen (DC Mid), CM Screen (DC+, DC-), and CM Screen (DC+, DC-, C_D) — is compared in Figure 44. It can be seen that at low frequencies of the conducted EMI frequency range the noise at the baseplate of the CM Screen (DC+, DC-) and CM Screen (DC+, DC-, C_D) module has a maximum reduction of up to 9 dB, compared to the CM Screen (DC Mid) module. Keeping in mind that the simulations have shown an error of up to 35%, a maximum reduction of 5.85 dB can be expected. The CM Screen (DC+, DC-) and CM Screen (DC+, DC-, C_D) module also has the additional benefit of either not requiring decoupling capacitors or a mid-point node inside the module architecture. However, it should be noted that the CM Screen (DC+, DC-) and CM Screen (DC+, DC-, C_D)

module would have higher electric field stresses inside the module architecture compared to the CM Screen (DC Mid) module [48]. It should also be noted that for the CM Screen (DC+, DC-) and CM Screen (DC+, DC-, C_D) modules, having the split in the screening below the switching node OUT can result in higher thermal resistance and therefore lower thermal performance, whereas, for the CM Screen (DC Mid) module the lower electric field stress [49] and majority of the noise current i_{CM} being diverted back into the module would allow thinner substrates to be used to allow a reduced thermal resistance [76].

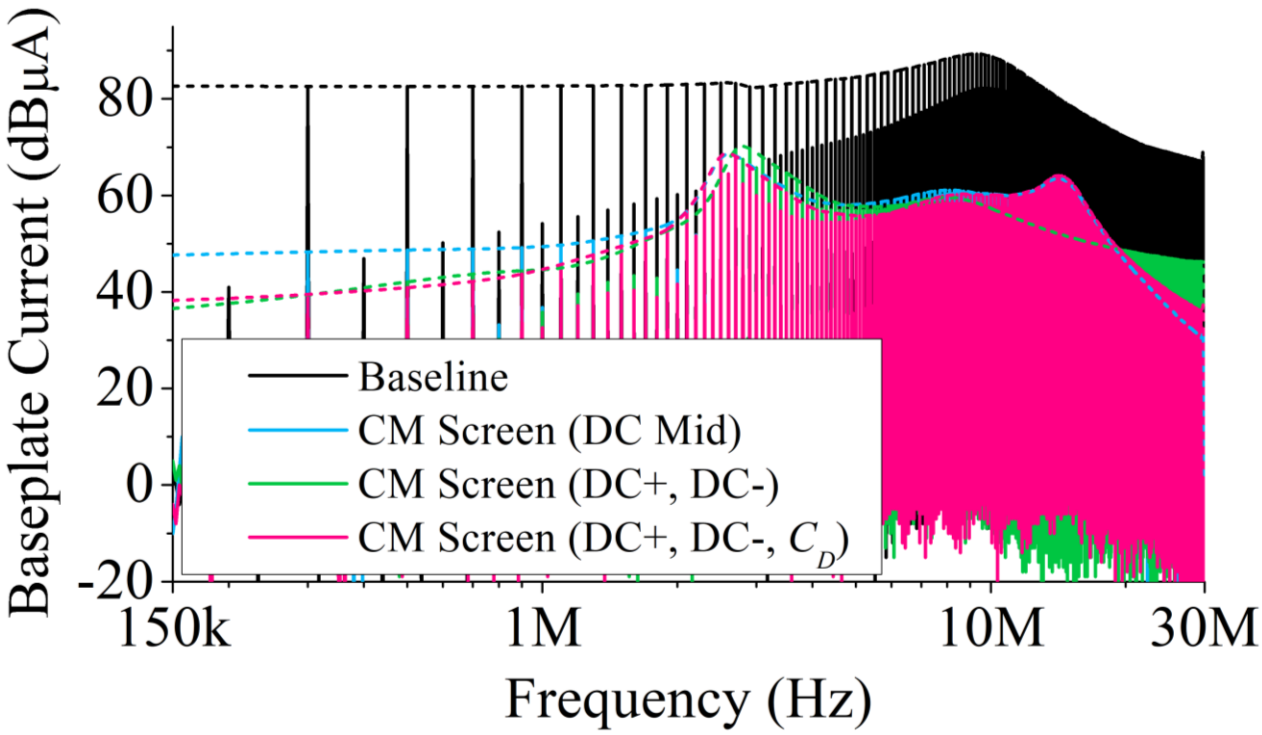


Figure 44: EMI footprint at baseplate of Baseline module (Black), CM Screen (DC Mid) module (Light Blue), CM Screen (DC+, DC-) module (Green) and CM Screen (DC+, DC-, C_D) module (Pink).

Chapter 6: Conclusion and Future Work

6.1 Introduction

This section summarizes the work presented in this thesis. The goal of this work was to evaluate and compare the EMI footprint of twelve module architectures available in literature and to provide an efficient analysis methodology which can be used to explain and analyze the EMI behavior of the modules. With the work presented, detailed insights into how packaging techniques can be used for a lower EMI footprint are obtained. Suggestions for the future development of the work are also provided.

6.2 Summary

The thesis starts by providing a literature review on different module architectures available in literature that have been used to mitigate EMI noise in converters. The twelve module architectures that were selected to be evaluated in this thesis are then introduced. Of the twelve module architectures evaluated, four are experimentally designed and fabricated inside the lab. The EMI performance of the remaining eight is only simulated.

The experimental test setup used to evaluate the four module architectures is then detailed. Measurement results for the noise measured at the baseplate and at the input of the converter are provided. Preliminary results for the efficiency and dv/dt slew rate for the four module architectures are also provided.

The analysis techniques used to understand the EMI behavior of the four module architectures is then introduced. A time domain simulation model is built to evaluate all twelve module architectures. A CEM for each module architectures is also derived. The substitution and

superposition theorem are also introduced. The time domain simulation, simplified CEM, and substitution and superposition theorem are then used to evaluate the twelve module architectures. The EMI behavior of the twelve module architectures is analyzed and insights are gained on the effect of design decisions taken at the packaging level on the EMI footprint of the modules.

6.3 Future Work

In this work, the EMI behavior of only four of the twelve module architectures studied is experimentally verified. The EMI footprint of the remaining eight module architectures is only simulated. Hardware validation for the remaining architectures needs to be undertaken. As a result, eight additional module architectures would need to be designed and fabricated. Alternatively, a new module layout can be designed which allows varying connection to the CM screen and the integration of decoupling capacitors even after the module has been packaged.

In the thesis, only preliminary efficiency and slew rate measurements are presented. The dv/dt, di/dt and slew rates for all the module architectures should be measured and the effect of the module architecture on efficiency be evaluated.

Another path forward would be to continue the analysis presented for full-bridge modules. Full-bridge modules by nature have a lower EMI footprint compared to half bridges, due to symmetry. It would be interesting to evaluate how each of the module architectures will react to this symmetry if the full bridge is made: (1) using two half bridge modules packaged separately (2) an entire H-bridge packaged in one module.

Another option would be to continue the analysis and simulation effort. The time domain simulation of the test setup can be improved to have better correlation between hardware and experiments. The CEM can be derived again for modules that have not been simplified and the

insights gained can then be updated. Frequency domain modeling and its applicability to the study of EMI mitigation techniques at the packaging level can be evaluated.

Another option is to evaluate the thermal, thermo-mechanical performance and reliability of the twelve module architectures. At present only EMI behavior of the module architectures is explored. Other parameters such as thermal performance of modules, reliability of modules and manufacturing complexity should also be considered. Other parameters such as thermal performance, reliability, and manufacturing complexity should also be considered. The four parameters below can then be optimized, and an optimization algorithm presented:

1. EMI
2. Thermal performance
3. Thermo-mechanical stresses
4. Reliability of the module

The work presented in this thesis is merely the starting point for evaluating EMI mitigation techniques that can be applied at the packaging level and there are numerous other possibilities that can be explored. The work presented is hopefully just an initial step in a series of upcoming research efforts. It is truly exciting to be a part of this journey.

Appendix A1: Obtaining Experimental EMI Measurements

A.1 Introduction

In this appendix, recommendations on how to obtain consistent EMI measurements are provided. The effect of connecting the copper sheet used in the EMI test setup to earth, the effect of connecting measurement probes to the EMI test setup, and the effect of increasing input voltage of the test setup on the EMI measurement being taken is discussed. The section also comments on the effect of the length of the time window used to plot the single-sided frequency spectrum of measurement and the ADC bit resolution and sampling time. The chapter concludes by talking about how it can be confirmed if consistent EMI measurements were obtained from the test setup.

A.2 Effect of Earthing on EMI Measurement

The effect of earthing the copper sheet being used in the EMI test setup is discussed. It was observed that taking the EMI measurements with and without the earth connected (Figure 45) results in different EMI measurements at the baseplate (Figure 46). This is primarily because the power supply used contains a complex impedance network between the DC terminals and the earth connection [32]. The inclusion and removal of this impedance results in changes in the EMI spectrum that are observed. For the course of this experiment, the earth connection was left connected to the copper sheet. This decision was made after noting the connection was recommended in the MIL standards [77] .

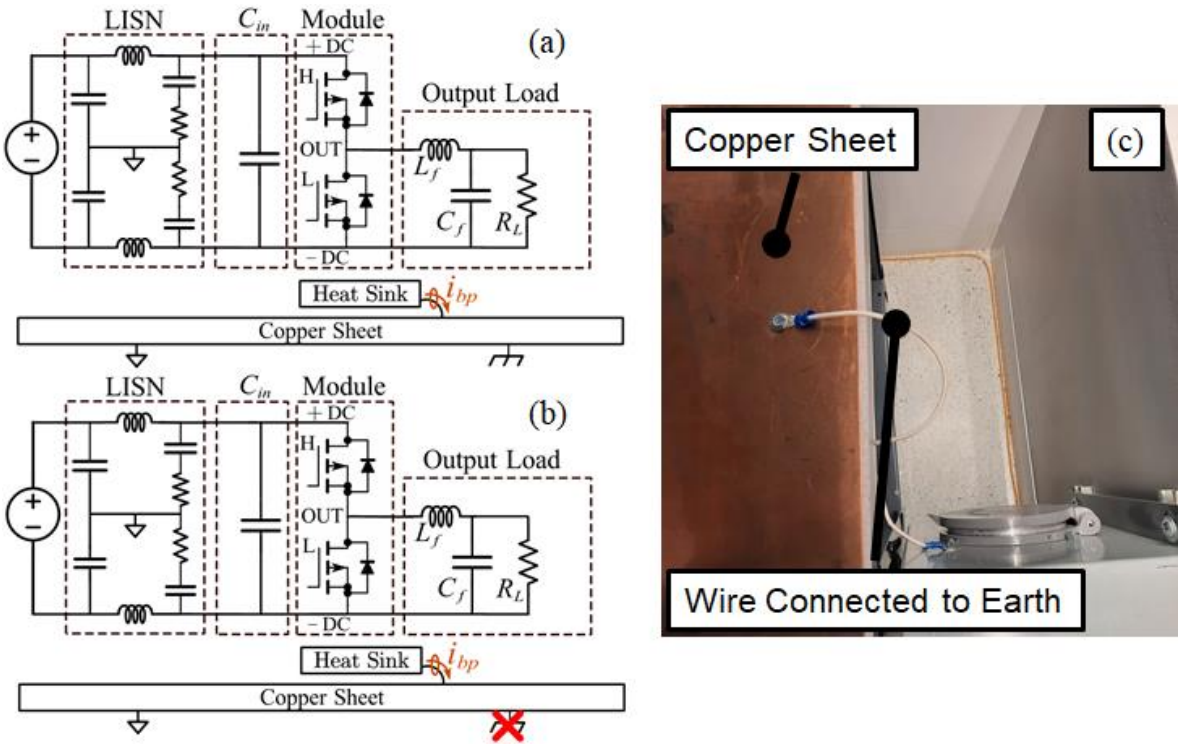


Figure 45: (a) Converter schematic with earth connection (b) Converter schematic without earth connection (c) earth connection made to copper sheet in hardware.

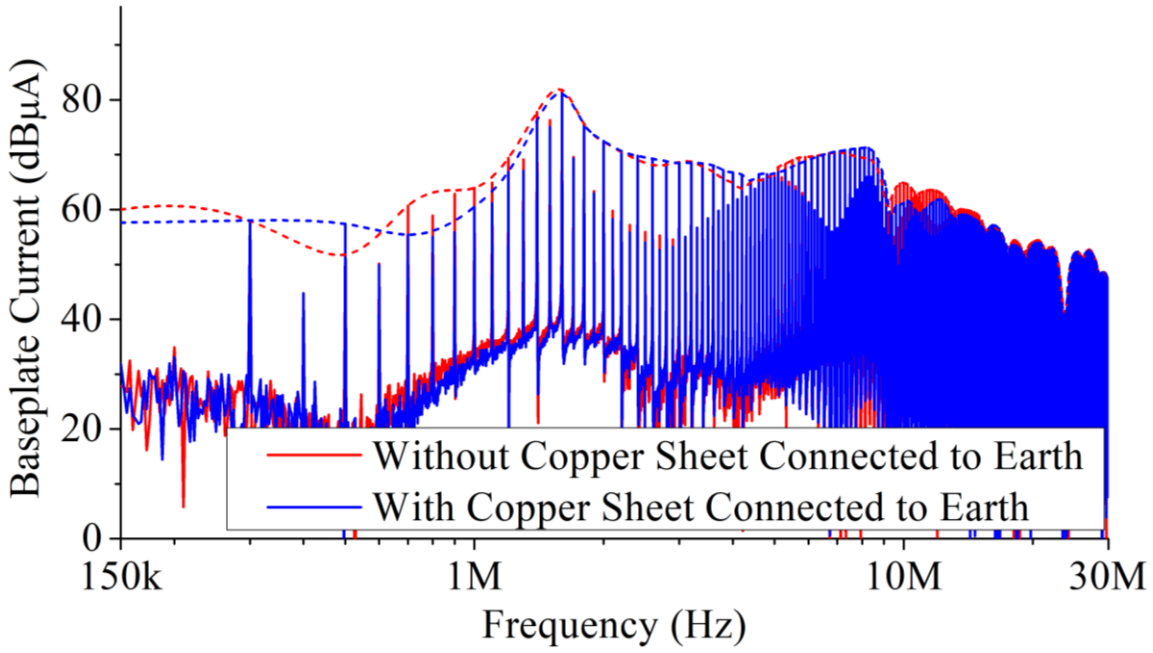


Figure 46: EMI noise measurements at baseplate i_{bp} without (red) and with (blue) copper sheet connected to earth.

A.3 Effect of Probes on EMI Measurement

The effect of the orientation and connection/disconnection of probes on the EMI measurement was also explored. Three experiments were conducted to explore the effect of (1) the connection of the i_{input} high frequency current transformer (HFCT) measurement probe, (2) the v_{ds} and i_L measurement probe, and (3) the effect of the orientation of the probe used to measure i_{bp}.

To explore the effect of connecting and disconnecting the HFCT to the oscilloscope used to record all the measurements, the 50 Ω BNC cable going from the HFCT to the oscilloscope was connected and disconnected, as shown in Figure 47(b). The experimental results can be seen in Figure 48(a). The frequency spectrum of i_{bp} during the experiment conducted with the HFCT connected is shown in red, and the frequency spectrum of i_{bp} during the experiment conducted with the HFCT disconnected is shown in green. It can be seen from Figure 48(a), that the two experiments result in different EMI frequency spectrums. In order to get repeatable EMI measurements, the HFCT was therefore always disconnected unless the i_{input} measurement was needed – in which case the all probes other than HFCT and triggering probes were disconnected.

Similar to the experiment conducted in Figure 47(a), experiments were performed to explore the effect of connecting a current and voltage probe to measure current flowing through output inductor i_L and high side switch voltage v_{DS} to the oscilloscope on the frequency spectrum of i_{bp}. The two probes going to the oscilloscope were connected and disconnected as shown in Figure 47(c). The experimental results can be seen in Figure 48(b). The frequency spectrum of i_{bp} during the experiment conducted with the current and voltage probe connected is shown in red and the frequency spectrum of i_{bp} during the experiment conducted with the current and voltage probe

disconnected is shown in green. It can be seen from Figure 48(a), that the two experiments result in different EMI frequency spectra. In order to get repeatable EMI measurements, all voltage and current probes were therefore disconnected when recording an i_{bp} measurement.

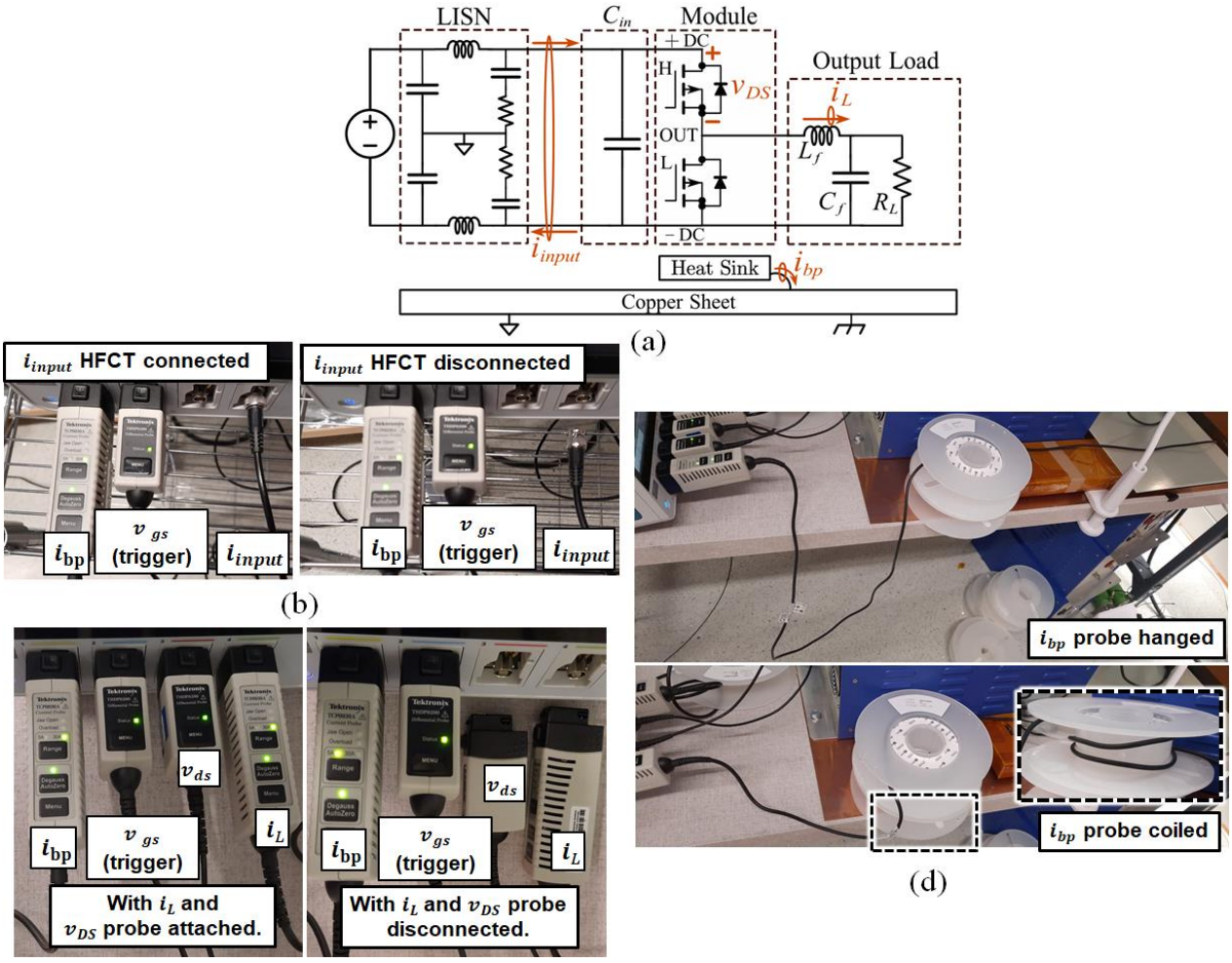
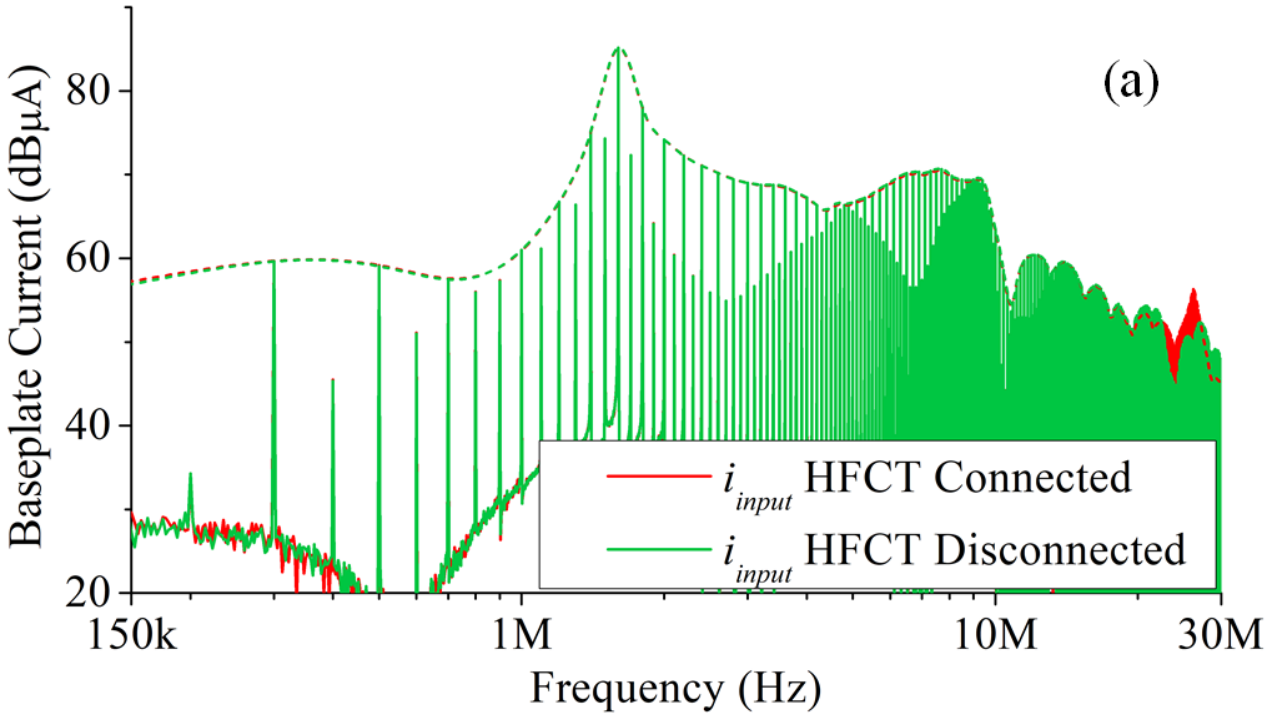
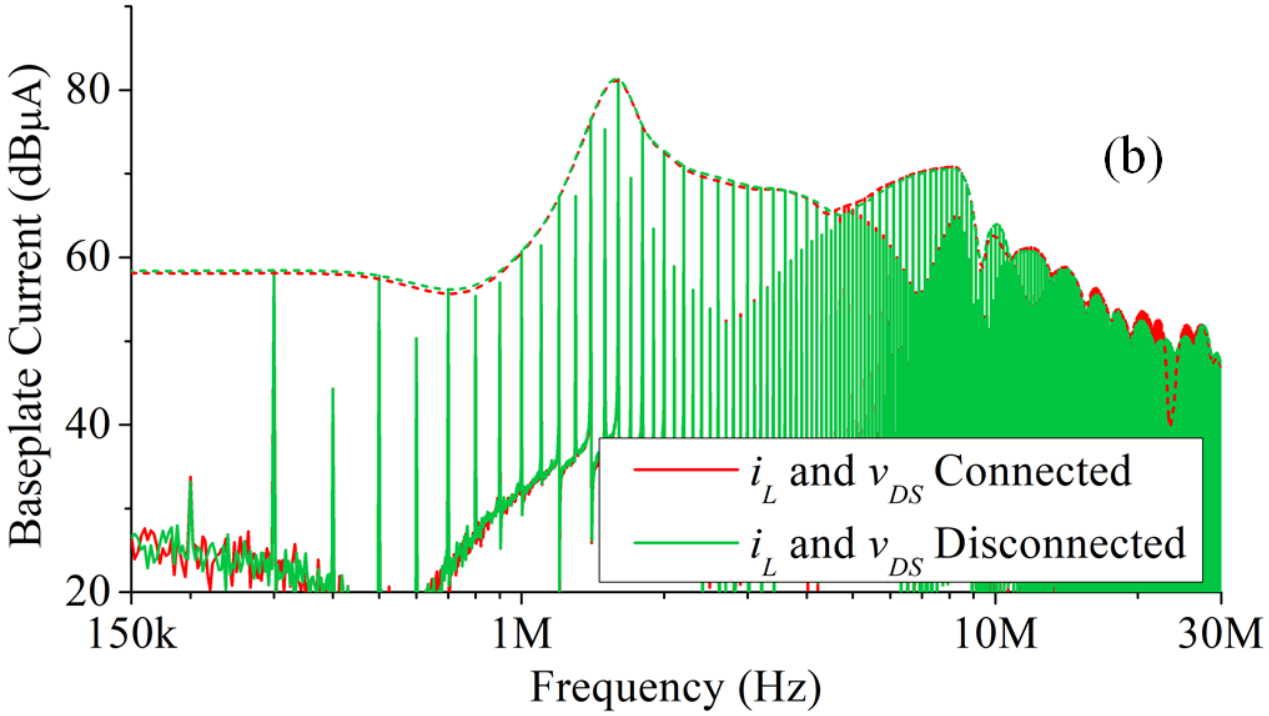


Figure 47: (a) Converter schematic showing placement of all probes (b) Connection and disconnection of i_{input} measurement probe (c) Connection and disconnection of v_{ds} and i_L measurement probe (d) orientation of i_{bp} probe hanged and coiled.

An experiment to see the effect of the orientation of the probe i_{bp} as it is connected to oscilloscope was performed. In the first experiment, the probe wire was left hanging off the table, whereas in the second experiment the wire was coiled around a 3D printed stand. The experimental results can be seen in Figure 48(c). The frequency spectrum of i_{bp} during the experiment

conducted with the wire left hanging is shown in red and the frequency spectrum of i_{bp} during the experiment conducted with the wire coiled is shown in green. It can be seen from Figure 48(a), that the two experiments result in different EMI frequency spectra. In order to get repeatable EMI measurements, the orientation of the i_{bp} probe was always kept constant by either taping it onto the table or by coiling it around a 3D printed stand.


(a)
Baseplate Current (dBµA)
80
60
40
20
150k
1M
10M
30M
Frequency (Hz)
i_{input} HFCT Connected
i_{input} HFCT Disconnected


(b)
Baseplate Current (dBµA)
80
60
40
20
150k
1M
10M
30M
Frequency (Hz)
i_L and v_{DS} Connected
i_L and v_{DS} Disconnected

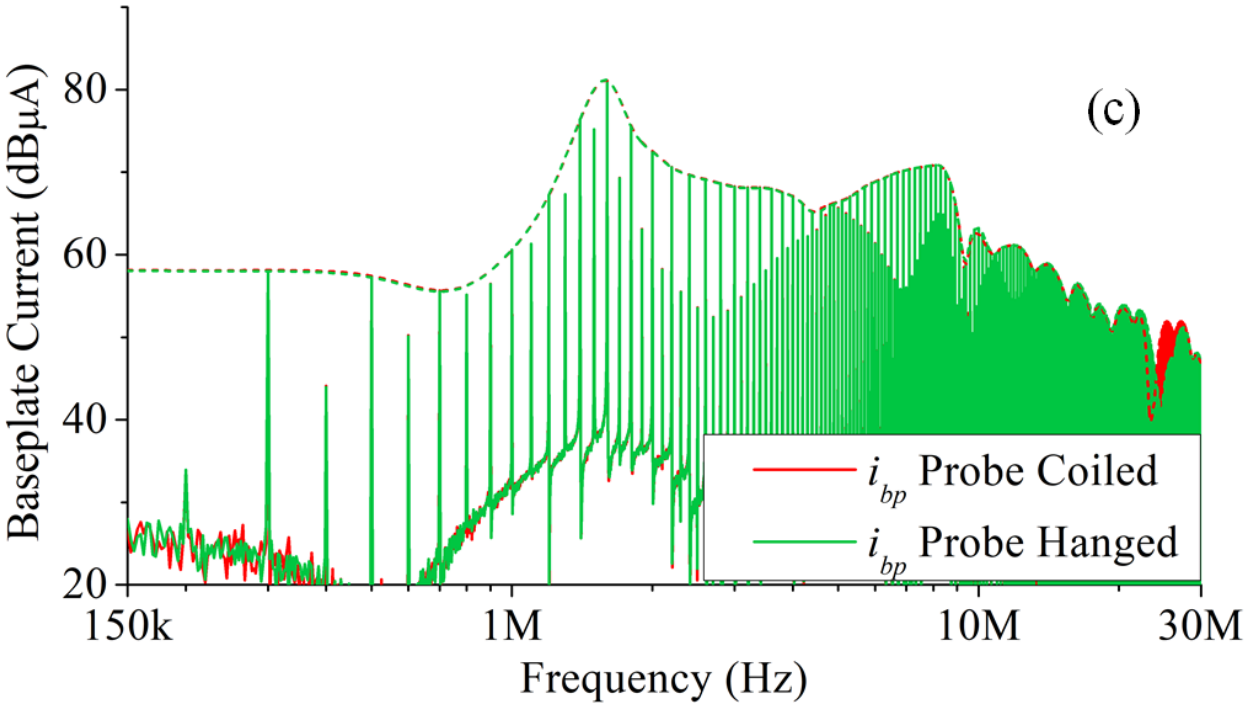


Figure 48: EMI frequency spectrum with (a) connection and disconnection of i_{input} measurement probe (b) connection and disconnection of v_{ds} and i_L measurement probe (c) orientation of i_{bp} probe hanged and coiled.

A.4 Effect of Input Voltage on EMI Measurement

The input voltage of the EMI test setup was varied from 300 V to 600 V, and the effect that variation had on EMI noise measurement i_{bp} was measured. From Figure 49, it was observed that increasing the input voltage increases the gain of the frequency spectrums. However, it should be noted that since the slew rates of the dies are a function of the device voltage, as the voltage is increased the slew rates become larger, therefore resulting in the noise at frequencies closer to the end of the conducted EMI frequency range becoming higher [38], [78].

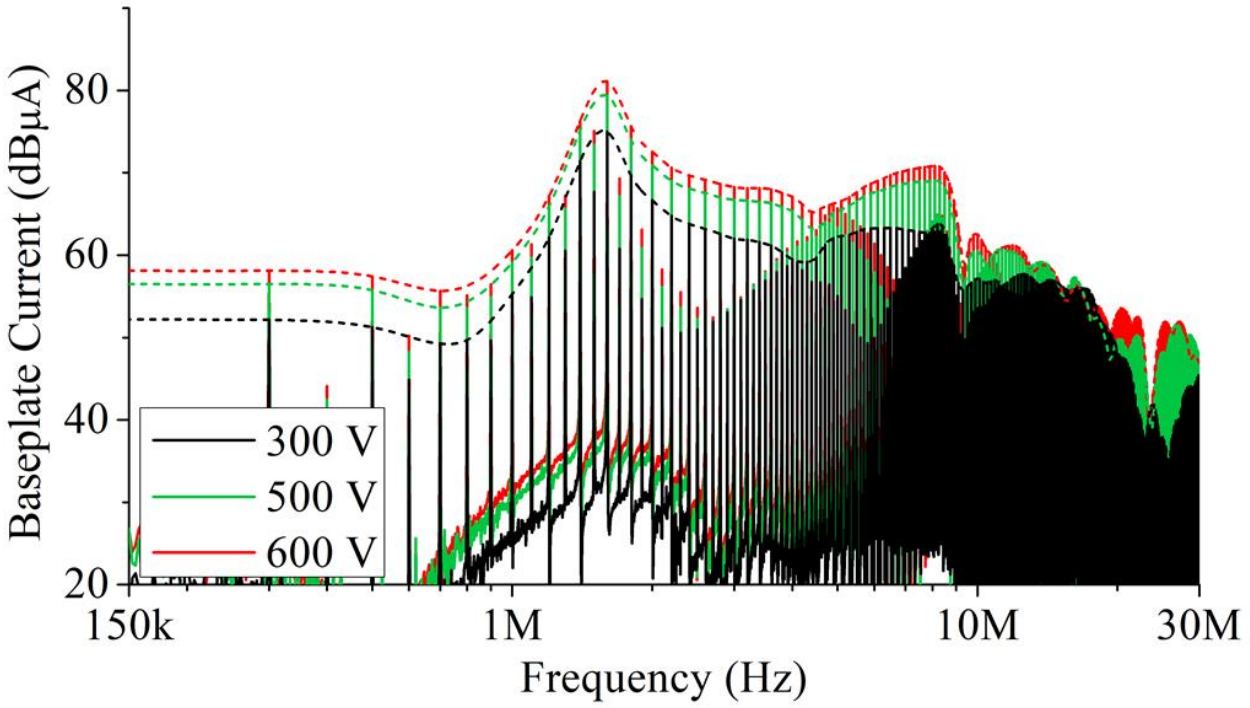
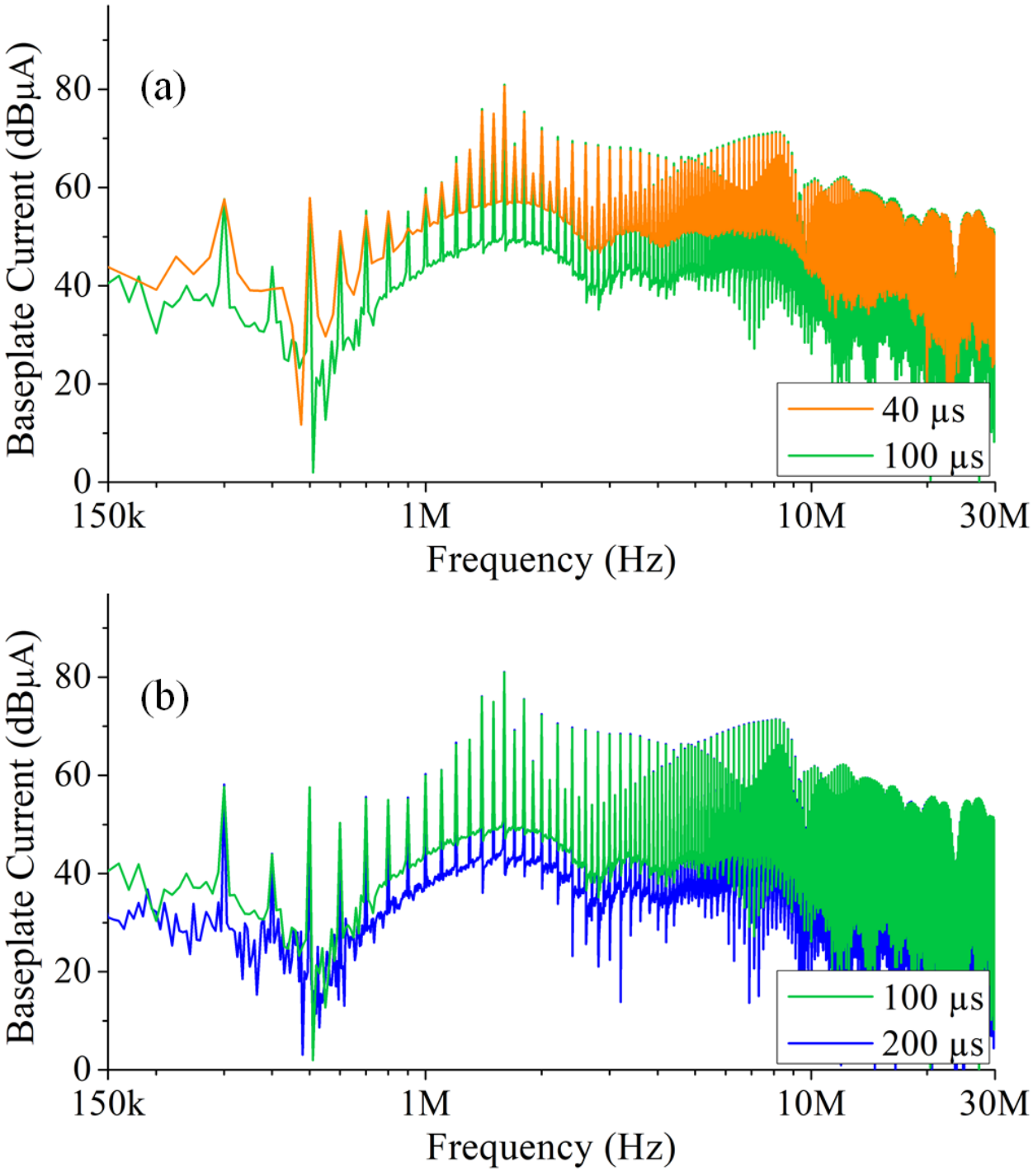


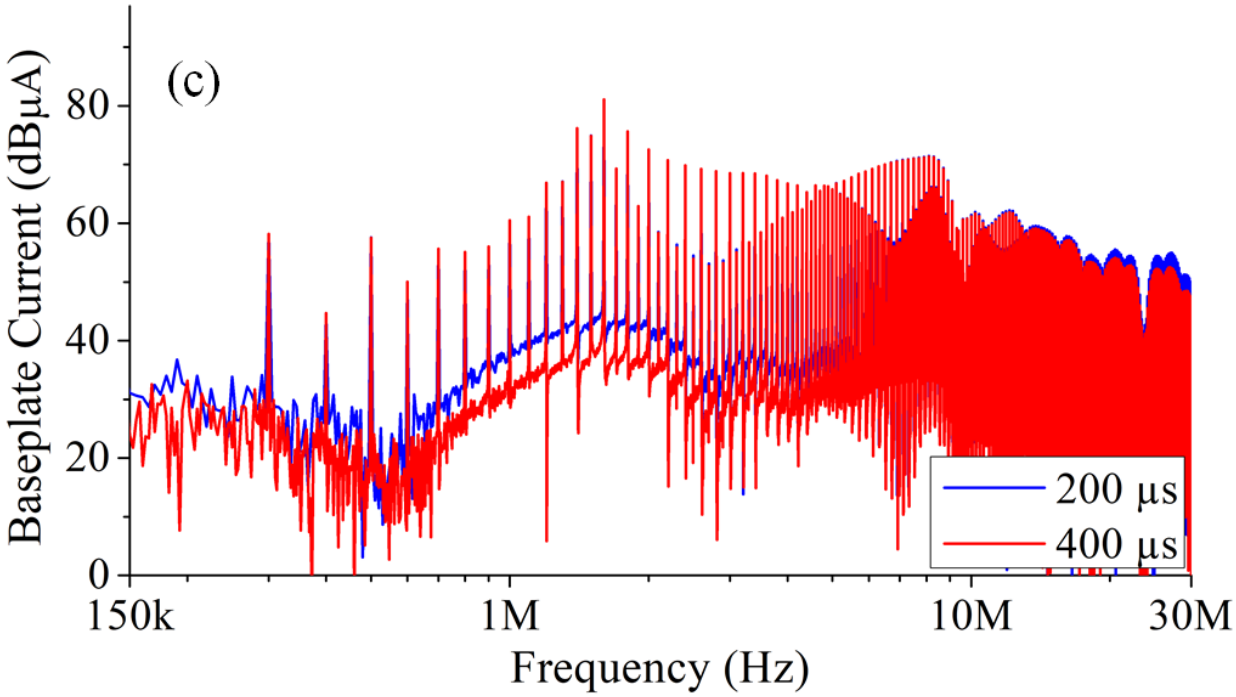
Figure 49: EMI frequency spectrum with input voltage increased to 300 V (black), 500 V (green), and 600 V (red).

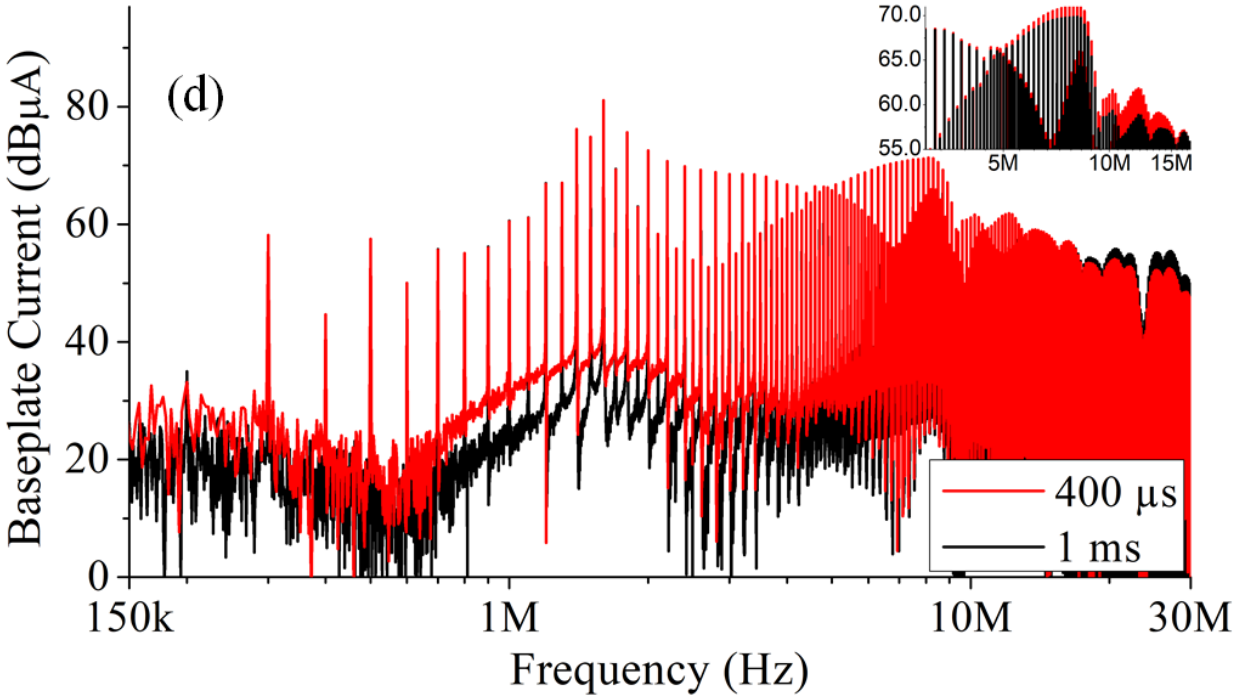
A.5 Effect of Time Window on EMI Measurement

The effect of the measurement time window used to record the EMI measurements was noted. A rectangular time window was selected for the experiments [79]. As the length of the time window increased the resolution of the frequency axis of the frequency spectrum also increases. The frequency resolution is equal to the sampling frequency divided by FFT size [80]. The length of the time window was varied from 40 μs to 2 ms. In Figure 50(a) and (b), the time windows of 40 μs (orange), 100 μs (green) and 200 μs (blue) are compared. It can be seen that the frequency spectrum does not differ by more than 1 dB between the three-time lengths. In Figure 50(c)-(e) the maximum difference between the frequency spectrums for different time lengths in 4 dB. Ultimately, a time window of 400 μs was kept consistent in all the experiments performed. More information on effect of different measurement times can be found in [81]. Spectral leakage should

be kept in mind when choosing a time window. Spectral leakage is the result of an assumption in the FFT algorithm that the signals contained in a time record are periodic at intervals that correspond to the length of the time record [82].




(c)
Baseplate Current (dBμA)
0
20
40
60
80
150k
1M
10M
30M
Frequency (Hz)
200 μs
400 μs


(d)
Baseplate Current (dBμA)
0
20
40
60
80
150k
1M
10M
30M
Frequency (Hz)
70.0
65.0
60.0
55.0
5M
10M
15M
400 μs
1 ms

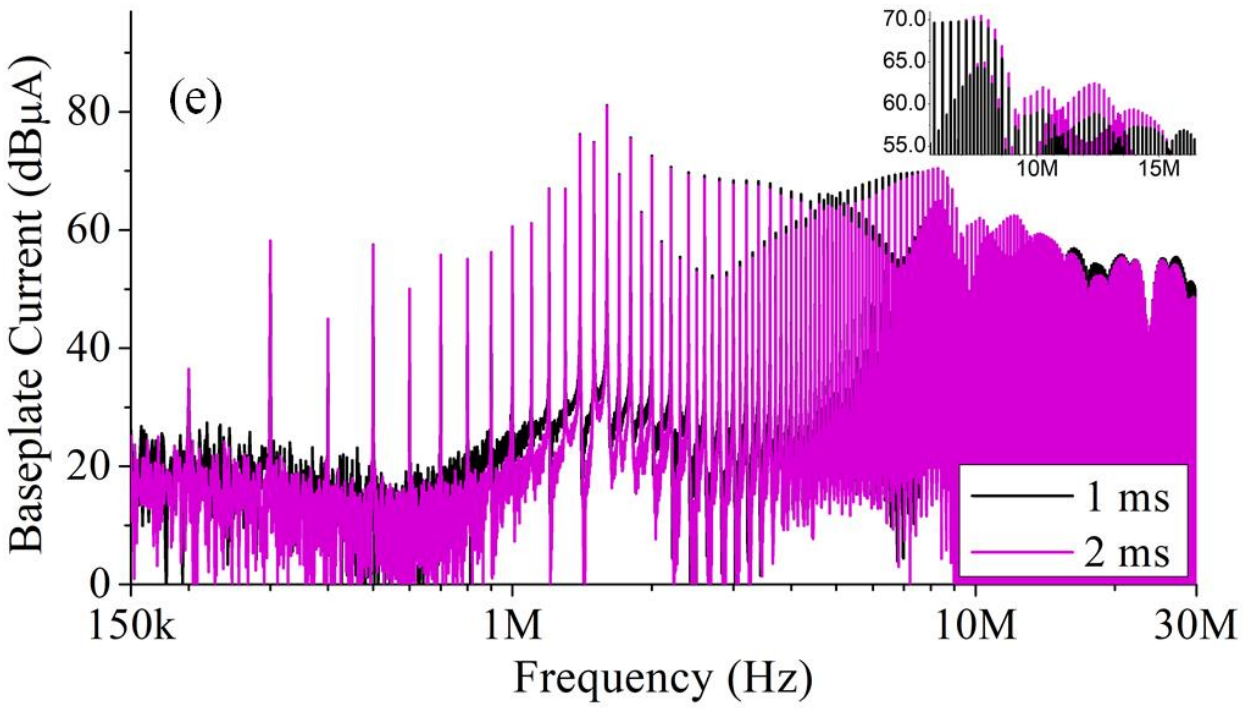


Figure 50: Effect of varying time window used to record time domain waveforms.

A.6 ADC bit Resolution and Sampling Time

The fast Fourier transform function was used in MATLAB to obtain the frequency spectrum from the recorded time domain waveforms [83]. The fast Fourier transform requires appropriate selection of the sampling frequency [80]. The frequency resolution in the frequency spectrum is equal to the sampling frequency divided by FFT size. The sampling frequency and ADC bit resolution at the particular sampling frequency provided by the oscilloscope used - MSO54 – is given in Table 6 [84]. The Nyquist theorem specifies that the sampling frequency should be greater than or equal to twice the bandwidth of the signal being sampled [85]. Since the bandwidth of the current probe being used to measure noise current i_{bp} was 120 MHz, and the bandwidth of HFCT used to measure i_{input} was 100 MHz, a sampling time of more than ten times the bandwidth of the probe was chosen. The maximum ADC bits and sampling frequency that can

be achieved simultaneously is 1.5635 GS/s, 13 bits ADC (in high resolution mode). This sampling time and ADC bit setting was used for all measurements taken.

Table 6: Sampling Frequency and ADC bit resolution options available in oscilloscope MSO54

Sampling Frequency	ADC Bits in Default Mode	ADC Bits in High Resolution Mode
125 MS/s	**12**	**16**
250 MS/s, 312.5 MS/s	**12**	**15**
625 MS/s	**12**	**14**
1.25 GS/s, 1.5625 GS/s	**12**	**13**
3.125 GS/s	**12**	**12**
6.25 GS/s	**8**	**12**

A.7 Confirming Repeatability of EMI Results

To ensure that all EMI results obtained were repeatable and consistent, a fixed methodology was used to obtain all measurements. The purpose of this methodology is to confirm that during the time frame of the experiment, no changes in the test setup occurred that could have resulted in a change in the EMI spectrum of the modules, and that any differences in the spectrum observed are due to the modules themselves. As an example, if the EMI footprint at the baseplate i_{bp} and at the input of the converter i_{input} of three different module architectures were to be compared then the methodology used to obtain these results is shown in Figure 51. The

methodology used to obtain these experiments would be divided into three steps. In step 1, noise current i_{bp} is measured for all three module architectures. Once the measurement for all three module architectures has been recorded the noise i_{bp} for the first module architecture is measured again. If the frequency spectrum of the EMI measurement taken for the first module's architecture at the beginning and end of step 1 is the same, only then is the experiment advanced to step 2 of the methodology. If the frequency spectra for the two experiments are not the same, then the experiment is restarted from the beginning of step 1. It is important to note that it is not compulsory to start with measuring i_{bp}, and that i_{input} can also be measured instead in the first step. However, both measurements should not be measured simultaneously, and depending on which noise measurement is chosen to be recorded first, the next step should alternate to the other noise measurement.

In step 2, noise current i_{input} is measured for all three module architectures. Once the measurement for all three have been recorded the noise i_{input} for the first module architecture is measured again. If the frequency spectrum of the EMI measurement taken for the first module architecture at the beginning and end of step 2 is the same, only then is the experiment advanced to step 3 of the methodology. If the frequency spectrums for the two experiments are not the same, then the experiment is restarted from the beginning of step 1. It is important to note that if i_{input} was measured instead of i_{bp} in step 1, then i_{bp} will be measured in this step.

In step 3, noise current i_{bp} is measured again for all three module architectures. Once the measurement for all three module architectures has been recorded, the noise i_{bp} for the first module architecture is measured again. If the frequency spectrum of the EMI measurement taken for the first module architecture at the beginning and end of step 3 is the same, and if the frequency

spectrum of each module architecture in step 3 is the same as the frequency spectrum of each module architecture in step 1, only then is the experiment concluded and the EMI results declared to be repeatable and consistent. If the frequency spectrums for any module is not the same then the experiment is restarted from the beginning of step 1. It is important to note that if i_{input} was measured instead of i_{bp} in step 1 then i_{input} will be measured again in this step.

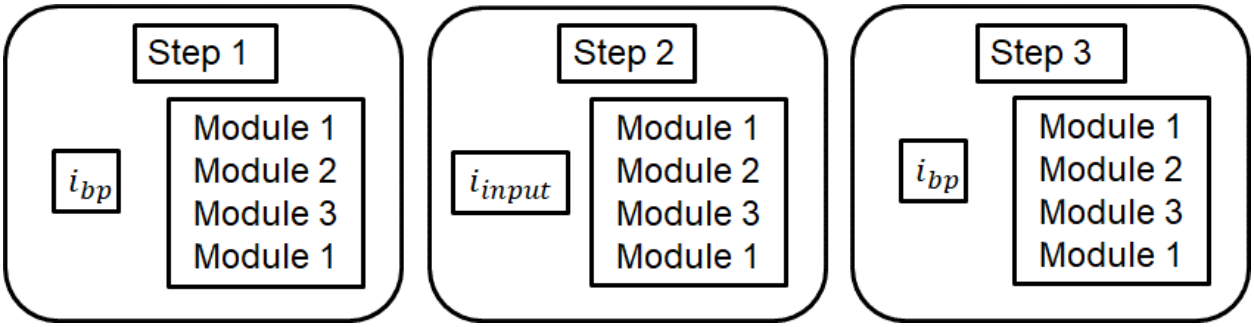


Figure 51: Methodology used to confirm EMI results were repeatable and consistent

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