

# Dynamic Current Sharing Issues with Paralleling SiC Power MOSFETs

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**Abstract**— This work comprehensively evaluates the key factors that impact the dynamic current sharing of paralleling silicon carbide (SiC) MOSFETs at the phase-leg circuit level. The power device matching is necessary and is well-known method to improve current balance. Stray inductance differences in the power loop, gate drive loop, and printed circuit board (PCB) layout are also well-known key factors. In addition to the above conventional sorting and passive matching methods, this paper proposes additional active matching approach by using the negative gate-off voltage, which can not only eliminate switching noise induced false turn on, but also help current sharing with gating signal delay matching similar to adjusting gate resistance. Impact of all key factors have been verified through experimental results.

**Keywords**—SiC MOSFET, Paralleling, Current Sharing, Dynamic Current, Power Modules

## I. INTRODUCTION

There are three levels of paralleling: (1) chip level, (2) device level, (3) phase-leg level, and (4) combination of any of above levels. In terms of device gate structure, there are three typical different device types including trench, trench-assisted planar, and planar [1-3]. Due to negative temperature coefficient (NTC) effect of the threshold voltage ( $V_{th}$ ), paralleling SiC MOSFETs requires substantial efforts of sorting and matching at the chip level [4]. At the device level, additional effort will be at the PCB trace and path balancing [5]. At the phase-leg level, further challenges are gate driving delay matching [6].

The chip level paralleling is typically performed by the chip manufacturer, and the end result is a high-power module which makes it convenient for end users to put the circuit together. The main issue is the high cost associated with the packaging if the quantity is relatively small, and the nonrecurring engineering fee is high. Additional unseen issue is the package related parasitic components due to wire bonding and pin connections inside the module [7].

The device level paralleling can be performed by circuit designers using the commercially available discrete devices. With multiple devices in parallel, the gate driving current is also multiplied, and the output stage of the gate driver typically requires additional amplifying stages such as a pair of totem-pole transistors [8]. The phase-leg level paralleling is to have individual gate drive circuits for each phase leg to avoid excessive gate driving loop length that tends to cause different switching delays between devices.

The combination of device paralleling and phase-leg level paralleling are mainly for large current requirements [9]. In that case, one can increase number of cells per device and/or duplicate multiple sets of paralleled devices or phase legs that

are driven by one gate drive circuit. An example case is the Tesla Model 3 traction motor drive inverter [10]. Its custom-made device or module consists of two SiC chips in parallel. A total of four modules are paralleled to form a switch. For such a multilevel paralleling to ensure equal current sharing is nontrivial due to chip size limit, gate driving capability limit, gate driving path and PCB layout balancing, and power loop parasitic delays [11].

This paper intends to quantify the impact of factors that cause dynamically unbalanced current distribution in SiC MOSFET paralleling. Three different types of gate structures were evaluated. A multiple phase-leg circuit board is designed for double-pulse testing (DPT). Experimental results will show the unbalanced current sharing waveforms due to different factors such as the threshold voltage ( $V_{th}$ ), device type, negative turn-off voltage, gate driver delays, and PCB layout, etc. The bandwidth of voltage and current measurement will also be discussed to show how to achieve high bandwidth measurement while not injecting much power loop parasitic to avoid waveform corruption by the switching induced noises. Through extensive measurement results, the use of negative gating voltage is also proposed as a potential approach for dynamic current sharing.

## II. ANALYSIS OF KEY FACTORS AFFECTING DYNAMIC CURRENT SHARING

Key factors of dynamic current sharing include mismatched  $V_{th}$ , gate driver delays, gate drive loop, PCB traces, and power loop parasitic. The negative temperature coefficient of the threshold voltage comes from device trapping and de-trapping that cause the shift of the transfer characteristic may be alleviated by sorting, but most other factors are all related to the circuit components and layout parasitic, which would also need sorting and matching.

Fig. 1(a) depicts the schematic circuit diagram of a typical paralleled test circuit with two sets of gating circuits to drive two devices under test,  $M_1$  and  $M_2$ . The top two devices serve as freewheeling diodes to circulate the inductor current so their gate and source are shorted individually. Fig. 1(b) shows the switching timing under turn-on and -off conditions. Since the drain-source current  $i_{ds}$  starts rising after the gate-source voltage  $v_{gs}$  reaches  $V_{th}$  during turn on, any mismatch of  $V_{th}$  and delay of  $v_{gs}$  will result in different current rise rates. Similar mismatch will also cause different current fall rates during turn-off dynamic. In this example diagram,  $i_{ds1}$  shares more current during turn on because it may have a smaller  $V_{th}$ . During turn off, the small  $V_{th}$  delays  $i_{ds1}$  falling, so  $i_{ds2}$  drops first, and thus transferring the inductor current to  $i_{ds1}$ , which clearly shows a current bump. Overall, the smaller  $V_{th}$  device shares more current under both turn-on and turn-off transients.

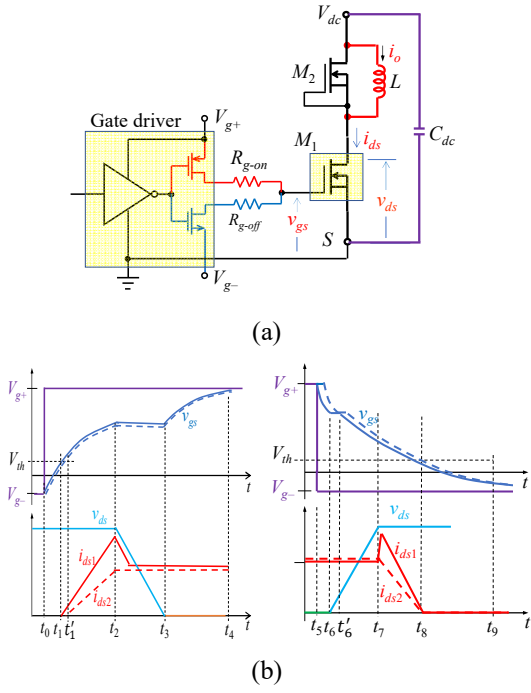


Fig. 1. (a) A typical DPT circuit, (b) MOSFET device switching timing diagram during turn-on and -off dynamics.

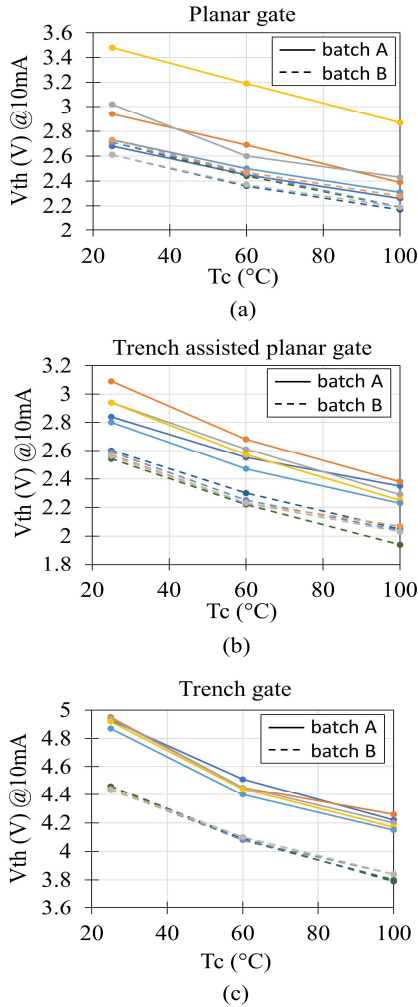


Fig. 2. Threshold voltage test with NTC effect using (a) planar gate devices, (b) trench-assisted planar devices, and (c) trench devices.

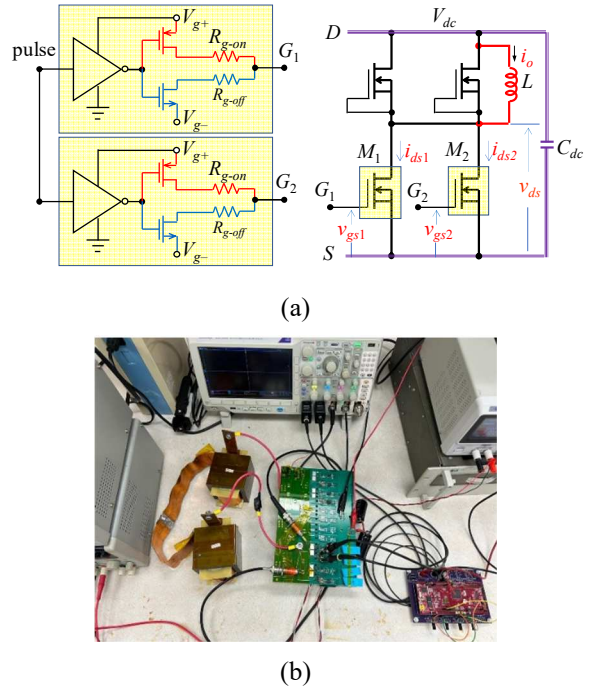


Fig. 3. DPT with (a) two phase-legs gating circuit and (b) its experiment setups.

### III. EXPERIMENTAL SETUP AND RESULTS

#### A. Static $V_{th}$ Sorting Under Different Temperature Conditions

Before performing dynamic pulse testing, three different gate structure devices were sorted to see their  $V_{th}$  variation among 10 samples. Fig. 2 shows their test results with  $V_{th}$  measured at  $I_D = 10$  mA for all devices. The solid line and dashed line represent devices from different batches. In planar gate devices, shown in Fig. 2(a), one of the solid-line samples shows significantly deviated  $V_{th}$ , which can be a good sample for dynamic current sharing comparison under different  $V_{th}$  conditions. The  $V_{th}$  reduction rate as a function of temperature is  $-0.52$  V/°C in average. In Fig. 2(b), the two batches of trench-assisted devices show two distinguishable  $V_{th}$  group among them with approximately 0.2 V between the two groups. This indicates that the two batches of devices might have come from different processes. The  $V_{th}$  reduction rate as a function of temperature is  $-0.60$  V/°C in average. In Fig. 2(c), the two batches show even more distinctive gap on their  $V_{th}$  with about 0.5 V difference out of less than 5-V  $V_{th}$  under the room temperature and the difference maintains near constant throughout the entire temperature range. The  $V_{th}$  reduction rate as a function of temperature is  $-0.76$  V/°C in average. It is also observed that devices from two different batches would have higher deviation which makes current balancing unignorable.

#### B. Dynamic Switching Experimental Setup

Fig. 3(a) depicts the double pulse test circuit diagram with two separate gate drive signals  $G_1$  and  $G_2$  controlling two gate source voltages  $v_{gs1}$  or  $v_{gs2}$ . Fig. 3(b) shows the picture of the experimental setup. The current is measured by a home-made toroid-core current transform (CT) with its output tied to a 2 GHz bandwidth current viewing resistor (CVR). The gate-source signal  $v_{gs}$  is measured with a 1-GHz probe, and the drain-source voltage  $v_{ds}$  is measured with an 800-MHz non-isolated high-voltage probe.

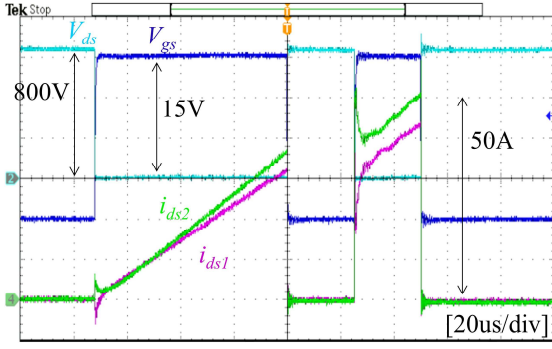


Fig. 4. Current imbalance results with mismatched  $V_{th}$  devices.

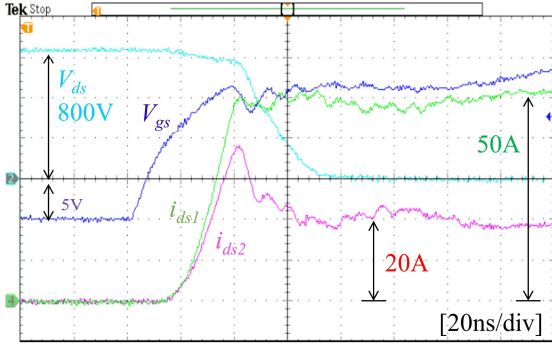


Fig. 5. Exploded view for mismatched  $V_{th}$  under turn-on condition.

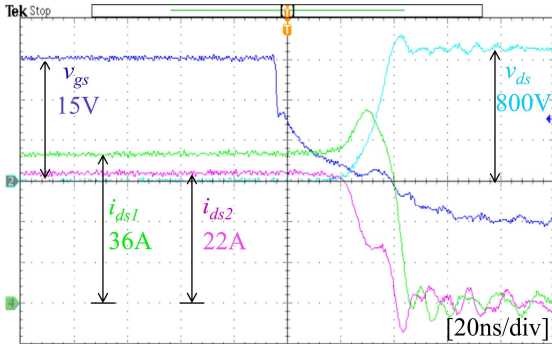


Fig. 6. Exploded view for mismatched  $V_{th}$  under turn-off condition.

Fig. 4 illustrates the measured voltage and current waveforms of two paralleled planar-gate SiC MOSFETs under highly mismatched  $V_{th}$  condition. The two devices with highest and lowest  $V_{th}$  in Fig. 2(a) were selected for this test. This extreme case is to indicate that if the devices were not sorted before paralleling a severe current imbalance will occur. The result can be explained in below exploded views.

### C. Current sharing imbalance due to $V_{th}$ Mismatch

Figs. 5 and 6 show the exploded view of mismatched current under turn-on and -off transients. In this example diagram,  $i_{ds1}$  shares more current during turn on because it has a lower  $V_{th}$ , and thus turning on first to carry more current. In such a short turn-on period, the current was split into 50 A and 20 A between  $i_{ds1}$  and  $i_{ds2}$ , respectively. In other words, it is 70% versus 30% split, as indicated in Fig. 5.

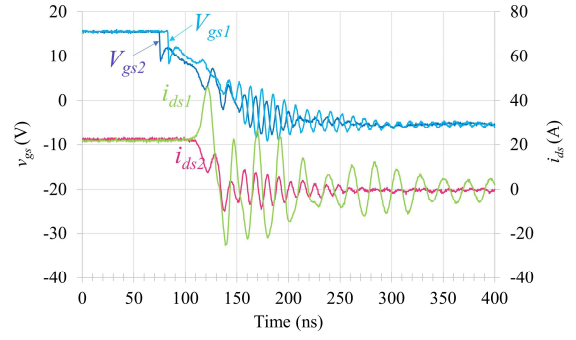


Fig. 7. Current imbalance impact due to mismatched gate-off delay.

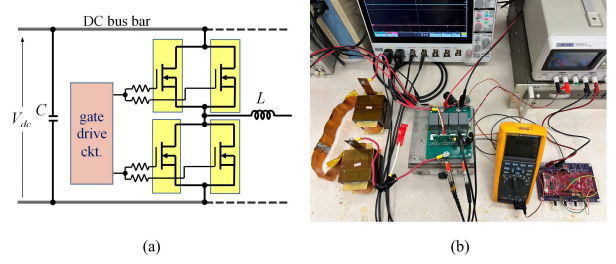


Fig. 8. DPT with (a) two devices in parallel under one gating circuit driving both devices and (b) its experiment setups.

During turn off, with a higher  $V_{th}$ , to  $i_{ds2}$  drops first, and thus transferring more current to  $i_{ds1}$  and resulting a current bump on  $i_{ds1}$ . The detailed turn-off current sharing waveforms can be illustrated in Fig. 6. Before turning off, the total current was split into 36 A and 20 A between  $i_{ds1}$  and  $i_{ds2}$ , respectively. After turn off,  $i_{ds1}$  peaks to 48 A before dropping to zero because  $i_{ds2}$  drops early and transfers more current to  $i_{ds1}$ . Overall, the device with a lower  $V_{th}$  will incur significantly higher current during both turn-on and -off transients as explained in an early section and verified with hardware experiment.

Fig. 6 depicts a case with timing delay due to the gate driver IC mismatches under the turn-off conditions. The gate driver IC used in this test is Infineon 1ED3124MU12H. The datasheet indicated there is a 15 ns typical tolerance. margin of error for each component. In this specific set of ICs, there is 10-ns mismatch. Fig. 7 clearly indicates a significant difference between two device current. The gate drive waveforms indicate that  $v_{gs2}$  drops first, so  $i_{ds2}$  also drops before  $i_{ds1}$ , which transfers a big portion of load current to  $i_{ds1}$ . The test indicates that gate driver turn-on and -off delays also need to be matched before putting in the circuit.

### D. Dynamic Current Sharing Varies with the Negative Gate Drive Voltage

Traditionally, the gate drive resistance was used to adjust the gating delay, and the negative gate drive voltage was used to prevent the noise during switching transition. There is a possibility that the negative gate voltage can help current balance especially during turn-off, because it can create an artificial delay and gate current slew rate which may coincidentally match the timing delay for a pair of devices with the same or nearly the same  $V_{th}$ .

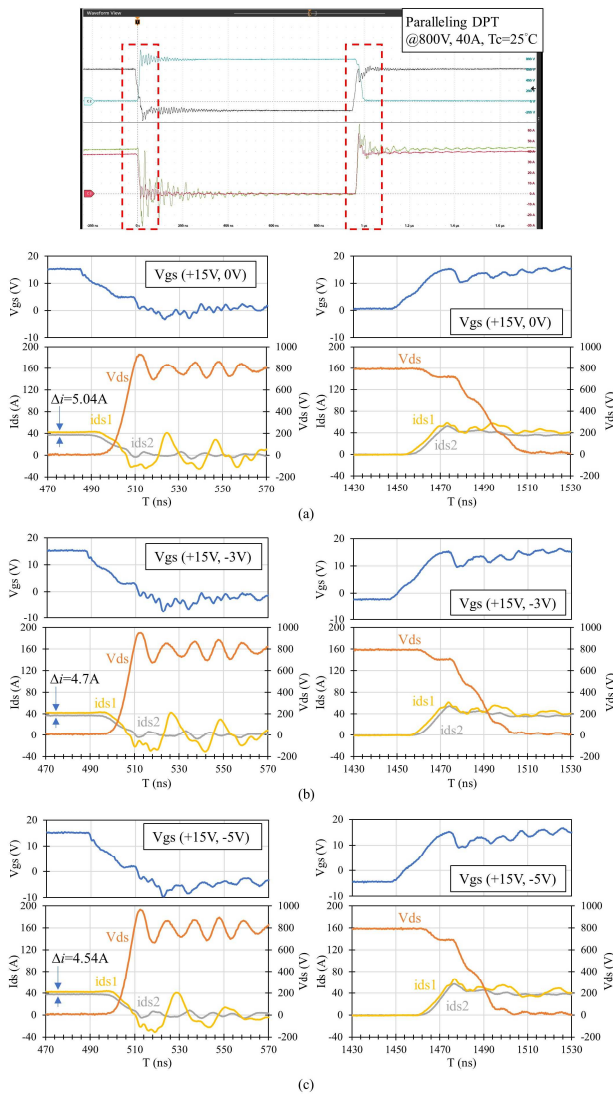


Fig. 9. Impact of turn-off negative voltage on current sharing under  $T_c=25^\circ\text{C}$  and turn-off voltage condition: (a)  $v_{gs} = 0\text{V}$ , (b)  $v_{gs} = -3\text{V}$ , (c)  $v_{gs} = -5\text{V}$ .

The experimental setup for the negative gate-off voltage is depicted in Fig. 8. Unlike the multiple gating circuit shown in Fig. 3, this setup intends to reduce the cost. Paralleling devices at the phase-leg level enables a higher switching frequency, thereby increasing power density. However, using individual gate drivers for each high-side and low-side legs increases costs and can introduce delay time mismatches. In contrast, Fig. 8 utilizes a single gate driver to each legs, with separate connections to the gate resistors for two paralleled devices.

Additionally, to observe the effects of temperature on current sharing, an external heater and thermometer are added in the setup. The trench device, IMZ120R060M1H, is used in this test. Fig. 9 and Fig. 10 compare the 800V, 40A DPT experimental results at the case temperature of  $T_c = 25^\circ\text{C}$  and  $100^\circ\text{C}$ . The gate drive resistance for turn-on and turn-off are  $R_{g,on} = 10\ \Omega$  and  $R_{g,off} = 4.7\ \Omega$ , respectively. Under both temperature test conditions,  $v_{gs}$  varies from 0 to  $-5\text{V}$ .

Fig. 9 compares the turn-on and -off current waveforms under different negative gate-off voltage conditions when  $T_c=25^\circ\text{C}$ . For this device, the manufacturer suggested the gate voltage is 18V for turn on and 0V for turn off. The test condition here is to vary the gate-off voltage from 0 to  $-5\text{V}$ .

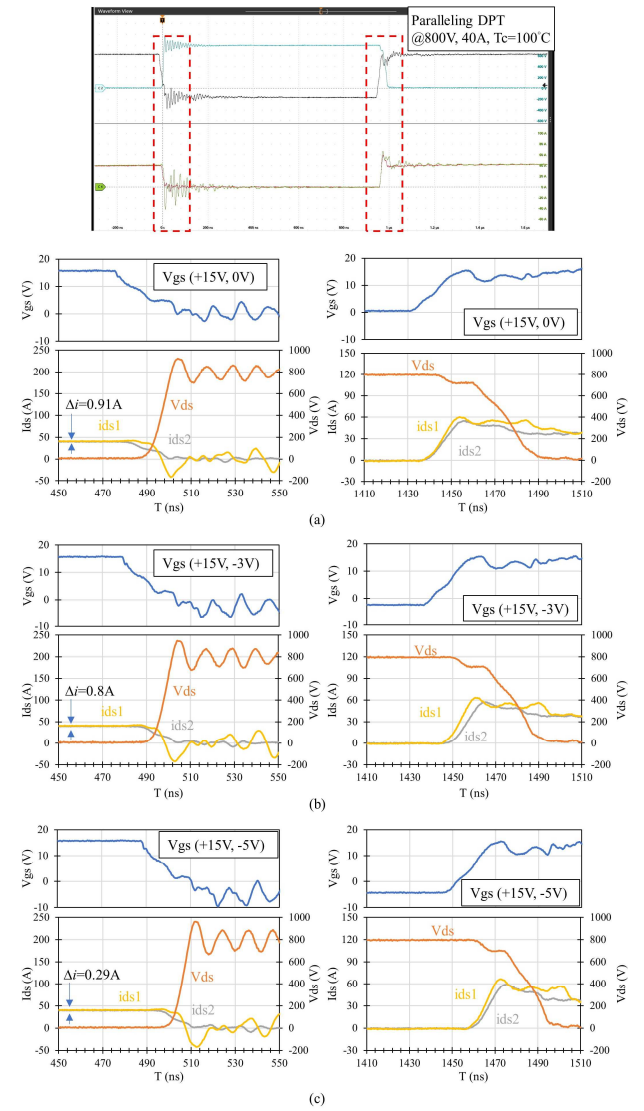


Fig. 10. Impact of turn-off negative voltage on current sharing under  $T_c=100^\circ\text{C}$  and turn-off voltage condition: (1)  $v_{gs} = 0\text{V}$ , (b)  $v_{gs} = -3\text{V}$ , (c)  $v_{gs} = -5\text{V}$ .

Under turn-on condition, the negative  $V_{gs}$  only causes the turn-on delay, which may have implications on turn-on loss but not on the dynamic current sharing. However, the scenario of turn-off conditions shows different results. As the negative  $V_{gs}$  varies from suggested 0V to  $-5\text{V}$ , not only the switching delay occurs, but also the current sharing changes. The current unbalance is improved as the gate-off voltage decreased. The turn-off current ringing appear noticeable which notes that the current oscillation is unavoidable due to power loop and inserted current sensing parasitic inductance. Nevertheless, the gate-off voltage magnitude is shown as a critical factor to the dynamic current sharing, which has not been extensively discussed in the literature.

It is also observed that the initial  $v_{ds}$  drop during the turn-on period, which is caused by the product of the power loop inductance and the device current rise rate, can be used to estimate the loop inductance. In this case, the loop inductances for the two devices are estimated at 28.7 nH and 25.4 nH, respectively. This is the main reason that causes different turn-on current slopes. It also indicates that symmetrical PCB layout is critical to equal current sharing.

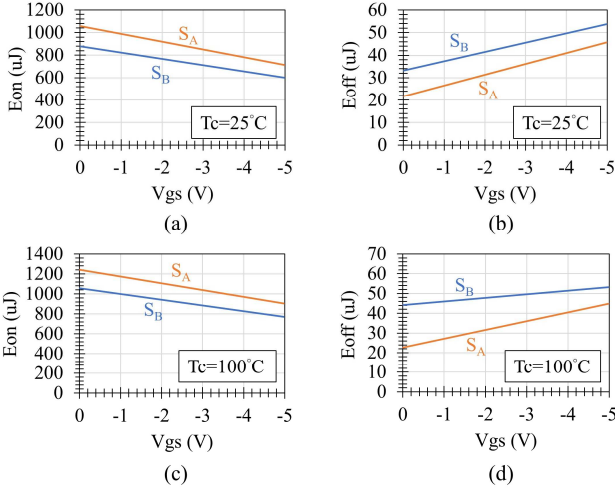


Fig. 11. Turn-on and Turn-off energy under (a), (b)  $T_c=25^\circ\text{C}$  and (c), (d)  $T_c=100^\circ\text{C}$ .

Comparing Fig. 9 and Fig. 10, the current sharing difference at  $V_{gs} = 0$  decreases from 5.04A at  $T_c = 25^\circ\text{C}$  to 0.91A at  $T_c = 100^\circ\text{C}$ . Such a better current sharing gets better due to the positive temperature coefficient (PTC) effect of  $R_{ds(on)}$ . However, the NTC effect of  $V_{th}$  still exists in switching transient period. As indicated in Fig. 9, the unbalanced current between two devices monotonically decreases from 5.04A to 4.54A as the  $V_{gs}$  varies from 0 to  $-5\text{V}$ . Similar phenomena is also found in Fig. 10, the unbalanced current decreases from 0.91A to 0.29A. Overall, both results demonstrate the current sharing is effectively improved via the applied negative  $V_{gs}$ .

Fig. 11(a) and (b) present the turn-on switching energy  $E_{on}$  and turn-off switching energy  $E_{off}$  under  $T_c=25^\circ\text{C}$  conditions. The switching energy is usually used to quantize the dynamic current sharing improvement. The device that denotes as  $S_A$  is a device with a lower  $V_{th}$  and  $S_B$  represents a device with a higher  $V_{th}$ . As the  $V_{gs}$  decreases,  $E_{on}$  of both devices decreases, while  $E_{off}$  increases due to turn-off time delay. In Fig. 10(c) and (d), the results tested under  $T_c=100^\circ\text{C}$  follow the same trend, though the difference in  $E_{off}$  becomes noticeably smaller. The  $E_{off}$  difference in Fig. 10(d) also reduces as the  $V_{gs}$  decreases. Overall, the experimental results show the negative turn-off voltage clearly helps share current in the turn-off period as well as a part of turn-on period.

#### IV. CONCLUSION

This paper comprehensively explored the dynamic current sharing issues with devices from different manufacturers and different key parameters that cause unequal current distribution at the circuit level. Using high bandwidth measurement setup, the paralleled SiC device currents were measured and characterized.

The major contribution is to quantify the current sharing with different key parameters that can impact the dynamic current sharing. A major finding is on the negative gate-off voltage impact to the current sharing. As the traditional

approach of applying a negative gate voltage was to prevent the noise turn-on, this paper found that it can also help current sharing. Experimental results verified the findings under both room and a high case temperature conditions.

In addition to the dynamic current sharing, the impact to the switching energy between different  $V_{th}$  devices were also measured under different negative gate voltage and different temperature conditions. A low  $V_{th}$  device always draws more turn-on energy, but the negative gate voltage helps turn-on loss reduction. On the other hand, a high  $V_{th}$  device always draws more turn-off energy, but the negative voltage under high temperature condition helps balance out the share of turn-off loss due to the added PTC effect of  $R_{ds(on)}$ .

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