Conducted EMI Noise Prediction and Filter Design Optimization

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ABSTRACT

Power factor correction (PFC) converter is a species of switching mode power supply (SMPS) which is widely used in offline frond-end converter for the distributed power systems to reduce the grid harmonic distortion. With the fast development of information technology and multi-media systems, high frequency PFC power supplies for servers, desktops, laptops and flat-panel TVs, etc. are required for more efficient power delivery within limited spaces. Therefore the critical conduction mode (CRM) PFC converter has been becoming more and more popular for these information technology applications due to its advantages in inherent zero-voltage soft switching (ZVS) and negligible diode reverse recovery. With the emerging of the high voltage GaN devices, the goal of achieving soft switching for high frequency PFC converters is the top priority and the trend of adopting the CRM PFC converter is becoming clearer.

However, there is the stringent electromagnetic interference (EMI) regulation worldwide. For the CRM PFC converter, there are several challenges on meeting the EMI standards. First, for the CRM PFC converter, the switching frequency is variable during the half line cycle and has very wide range dependent on the AC line RMS voltage and the load, which makes it unlike the traditional constant-frequency PFC converter and therefore the knowledge and experience of the EMI characteristics for the traditional constant-frequency PFC converter cannot be directly applied to the CRM PFC converter.

Second, for the CRM PFC converter, the switching frequency is also dependent on the inductance of the boost inductor. It means the EMI spectrum of the CRM PFC converter is tightly related the boost inductor selection during the design of the PFC power stage. Therefore, unlike the traditional constant-frequency PFC converter, the selection of the boost inductor is also part of the EMI filter design process and EMI filter optimization should begin at the same time when the power stage design starts.

Third, since the EMI filter optimization needs to begin before the proto-type of the CRM PFC converter is completed, the traditional EMI-measurement based EMI filter design will become much more complex and time-consuming if it is applied to the CRM PFC converter. Therefore, a new methodology must be developed to evaluate the EMI performance of the CRM PFC converter, help to simplify the process of the EMI filter design and achieve the EMI filter optimization.

To overcome these challenges, a novel mathematical analysis method for variable frequency PFC converter is thus proposed in this dissertation. Based on the mathematical analysis, the quasi-peak EMI noise, which is specifically required in most EMI regulation standards, is investigated and accurately predicted for the first time. A complete approximate model is derived to predict the quasi-peak DM EMI noise for the CRM PFC converter. Experiments are carried out to verify the validity of the prediction. Based on the DM EMI noise prediction, worst case analysis is carried out and the worst DM EMI noise case for all the input line and load conditions can be found to avoid the overdesign of the EMI filter. Based on the discovered worst case, criteria to ease the DM EMI filter design procedure of the CRM boost PFC are given for different boost inductor selection. Optimized design procedure of the EMI filter for the front-end converter is then discussed. Experiments are carried out to verify the validity of the whole methodology.

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GENERAL AUDIENCE ABSTRACT

Power factor correction (PFC) converter is widely used in offline frond-end converter for the distributed power systems to reduce the grid harmonic distortion. With the fast development of information technology and multi-media systems, high frequency PFC power supplies for servers, desktops, laptops and flat-panel TVs, etc. are required for more efficient power delivery within limited spaces. Therefore the critical conduction mode (CRM) PFC converter has been becoming more and more popular for these information technology applications.

However, there is the stringent electromagnetic interference (EMI) regulation worldwide. For the CRM PFC converter, there are many challenges on meeting the EMI standards. To overcome these challenges, a novel mathematical analysis method for variable frequency PFC converter is thus proposed in this dissertation. A complete approximate model is derived to predict the quasi-peak DM EMI noise for the CRM PFC converter. Experiments are carried out to verify the validity of the prediction. Based on the DM EMI noise prediction, worst case analysis is carried out and based on the discovered worst case, criteria to ease the DM EMI filter design procedure of the CRM boost PFC are given for different boost inductor selection. Optimized design procedure of the EMI filter for the front-end converter is then discussed. Experiments are carried out to verify the validity of the whole methodology.

To My Parents:

Father: Bailin Wang

Mother: Yuping Liu

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At last, thanks to my parents, I love you.

Best regards,

Zijian Wang

May 4th, 2016

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Chapter 1. INTRODUCTION

1.1. Introduction to EMI and EMC

With the development of power electronics technology, electromagnetic interference (EMI) and electromagnetic compatibility (EMC) issues have become more and more important. By definition, Electromagnetic interference (EMI) is "any electromagnetic disturbance that interrupts, obstructs, or otherwise degrades or limits the effective performance of electronics or electrical equipment" [1]. And electromagnetic compatibility (EMC) is defined as "the ability of a device, unit of equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment" [2]. According to the definition above, there are two aspects related to the EMI and EMC: emission and susceptibility. Emission problems are related to the undesired generation of electromagnetic disturbances by certain sources, and to the methods to reduce such generation and to minimize any remaining disturbance energy leaking into the external environment. Susceptibility or immunity problems, in contrast, are related to the correct operation of electronic or electrical equipment, referred as the "victim", at the presence of unwanted electromagnetic disturbances. In this dissertation, the emission problems and their solutions will be the focus and the susceptibility problems will not be involved.

The emission problems are getting attention in all electronic regions but are appearing to be more and more critical especially in power electronics industry. That is because the high dv/dt nodes and the high di/dt loops in power electronics device are easily becoming the dominant source of the electromagnetic disturbance compared to

other electronic circuits. As an example, Figure 1-1 [3] shows the high dv/dt switching node and high di/dt pulsating current loop in a step-up DC-DC switching mode power supply (Boost converter). For the modern switches with fast switching speed, the dv/dt can be easily more than 10000V/us and the di/dt could be up to 500A/us [4].

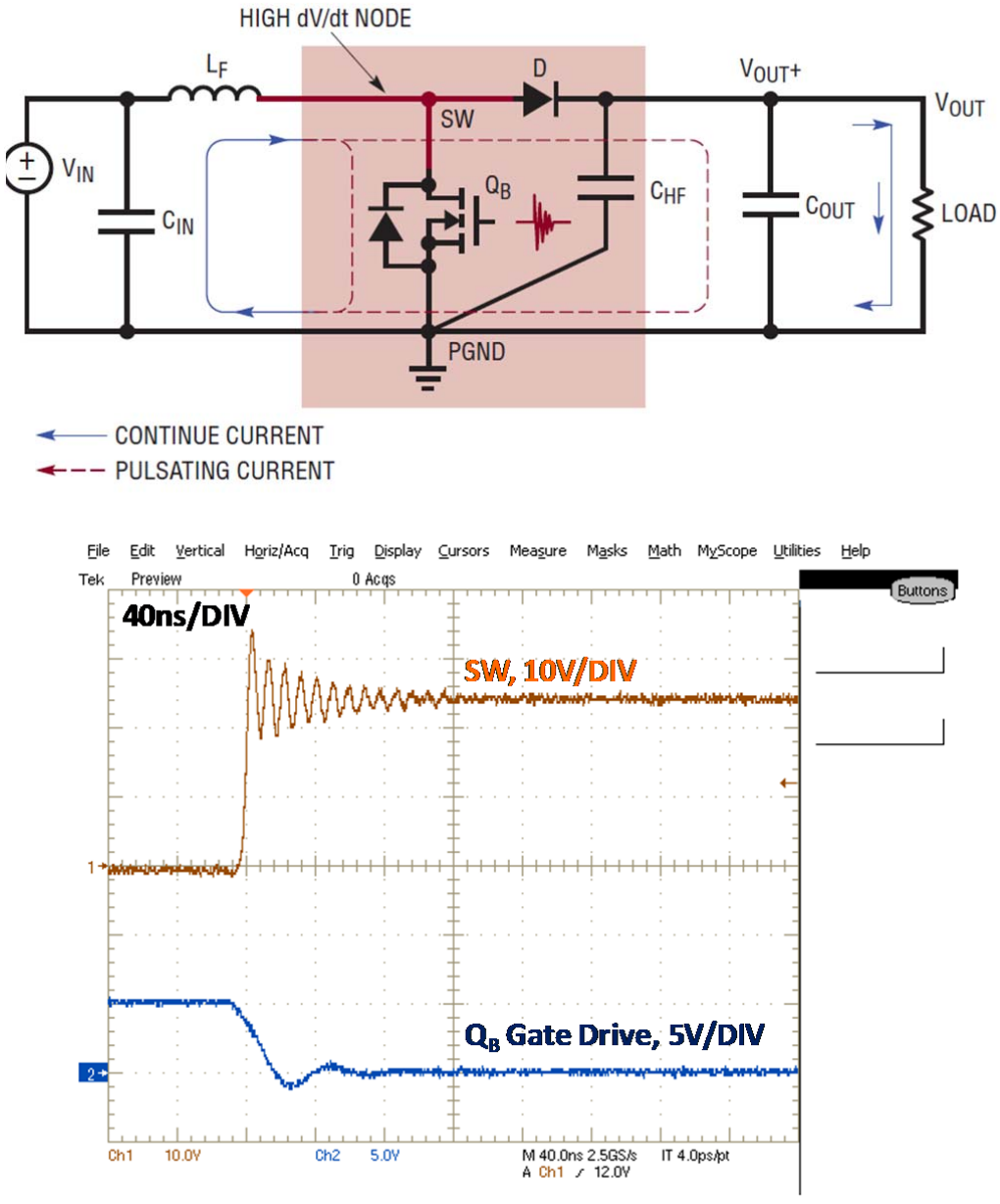


Figure 1-1 High dv/dt node and high di/dt loop in a 12Vin, 24Vout, 5A Boost Converter

The high dv/dt node and the high di/dt loop are noise source. For emission problems, noise propagation paths are also necessary for the "victims" to be "disturbed". There are

typically three different ways for the noise source to interfere with the victim circuit, and they are, respectively,

1) Conductive coupling
2) Radiated coupling
3) Near field coupling

Conductive coupling means that the noise source interferes with the victim circuit through conductors such as the power cords; radiated coupling means the noise source interferes with the victim circuit through radiation, while the near field coupling includes both the capacitive coupling and inductive coupling, which means the interference happens between the energy storage components in the system.

To regulate the EMI emission, a lot of countries in the world have already published the EMC standards, which specify the maximum emission level of the EMI noise, including but not limit to, EN55022 from Europe, GB9254 from China and FCC part 15 from USA. And for different industrial applications, there are special EMC standards such as the CISPR 22 for information technology equipment and CISPR 25 for Vehicles, boats and internal combustion engines. [5] As an example, Figure 1-2 shows the EMC standard for conducted EMI noise in CISPR 22. [6] Therefore, the purpose of EMI analysis are either to identify the EMI noise source, reduce or eliminate it, or to block the path it propagates and finally to make it pass the EMC regulation.

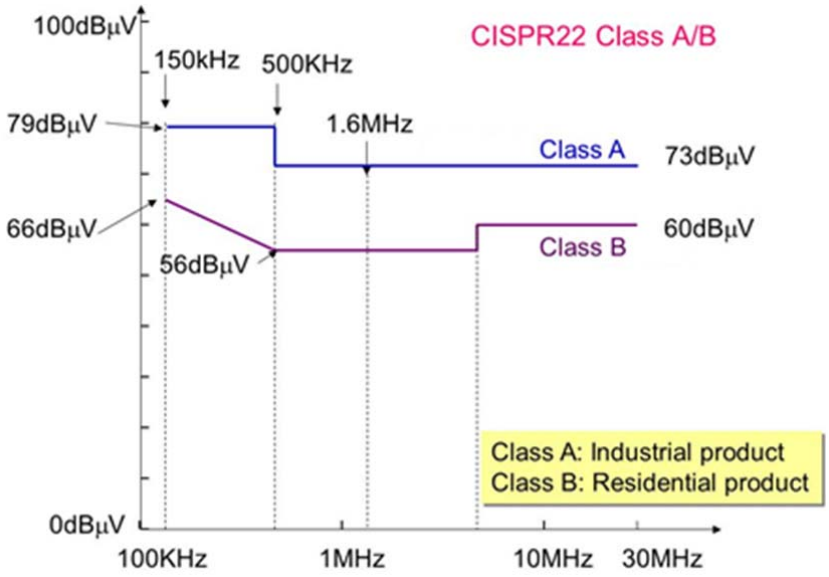


Figure 1-2 CISPR22 Class A/B EMC standards

1.2. Introduction to Constant On-time Boost PFC

1.2.1. Background and Incentive

In this dissertation, conducted EMI noise analysis is the focus rather than the radiated noise. Two most common applications that conducted EMI noise regulation is applied are offline and automotive applications. However, for automotive applications, different manufactures have their own standards to follow besides CISPR 25. Thus without losing the generality, the offline application is chosen to illustrate the concept in this dissertation. However, the methodology can be easily extended to other applications.

For the offline switch mode power supplies (SMPS), the distributed power system (DPS) has been becoming an industry practice as a systematic solution used in information technology applications [7].

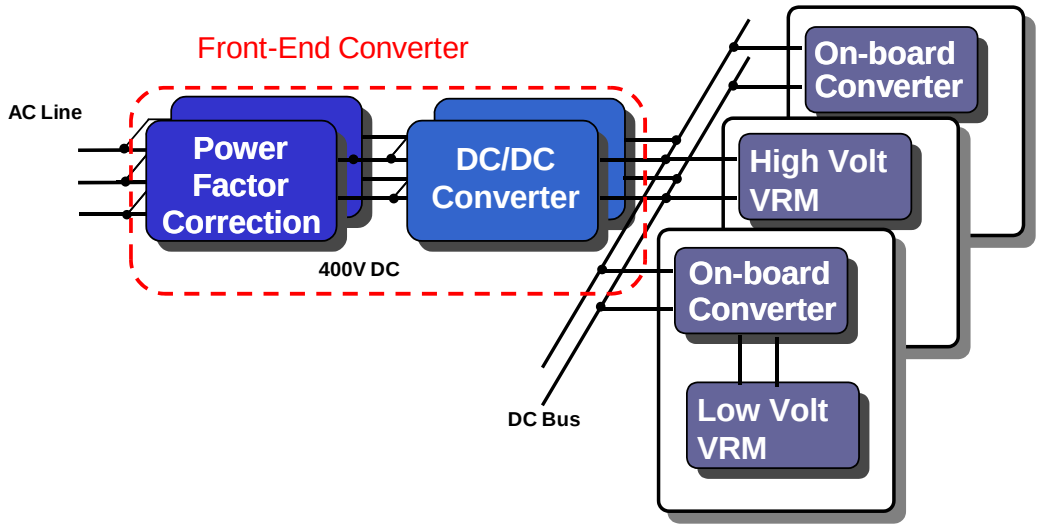


Figure 1-3 Distributed Power System

As shown in Figure 1-3, a typical DPS structure which is often found in laptops,

desktops and servers applications could be divided into two parts, the frond-end converter and the voltage regulator module (VRM). For the front-end converter, the so called computer power supply, it generally adopts a two-stage approach, with the power factor correction (PFC) converter as the first stage and the DC-DC converter as the second stage.

As the power quality is always a major concern, there are stringent international standards which set limits to the input harmonic currents, such as IEC61000-3-2 [8]. As an example, Table 1 shows the harmonic current limits for the Class A equipment. Therefore, the PFC converter is becoming a common practice and has been widely used in front-end converters to help make the AC input current follow the sinusoidal AC input voltage, and thus meet the harmonic current limits.

Table 1 Harmonic current limits for Class A equipment

Harmonic order n	Maximum permissible harmonic current A
Odd harmonics	
3	2,30
5	1,14
7	0,77
9	0,40
11	0,33
13	0,21
$15 \le n \le 39$	$0{,}15\ \frac{15}{n}$
Even harmonics	
2	1,08
4	0,43
6	0,30
$8 \le n \le 40$	$0{,}23\ \frac{8}{n}$

For PFC techniques, the boost converter is inborn a good topology since its input

current is continuous and thus there is less input current distortion. For the continuous conduction mode (CCM) boost PFC converter, average current-mode control is one of the most important control schemes. The diagram of the average current-mode control scheme for CCM boost PFC is shown in Figure 1-4 [9]. Through the current feedback loop, the average inductor current (i.e., AC input current) will be forced to follow the current reference, which is proportional to the sinusoidal AC input voltage. Thus the PFC function is achieved.

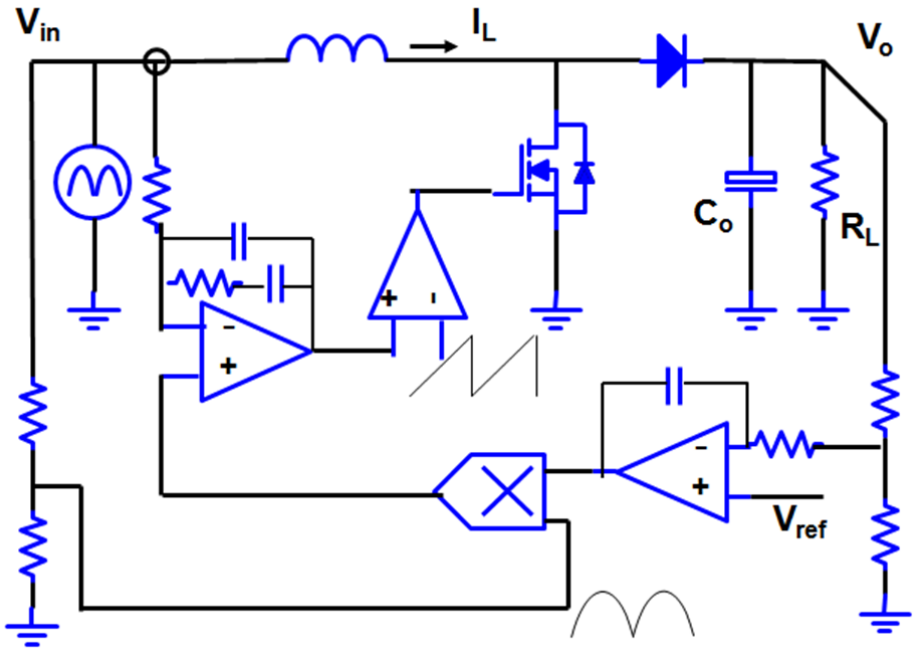


Figure 1-4 Average Current Control Scheme for constant frequency Boost PFC

However, with the fast increasing of the power consumption worldwide, the efficiency for the front-end converter is becoming more and more important. As an example, Figure 1-5 shows the increasing efficiency requirement in industry for the front-end converters. The dashed curves in Figure 1-5 show some of the efficiency requirements from organizations such as 80Plus and Climate Savers. The maroon and the pink solid curves in Figure 1-5 are projected DC-DC and PFC target efficiency,

respectively, based on the red solid curve, which is the total target efficiency for the front end converter by some mainstream computer manufacture.

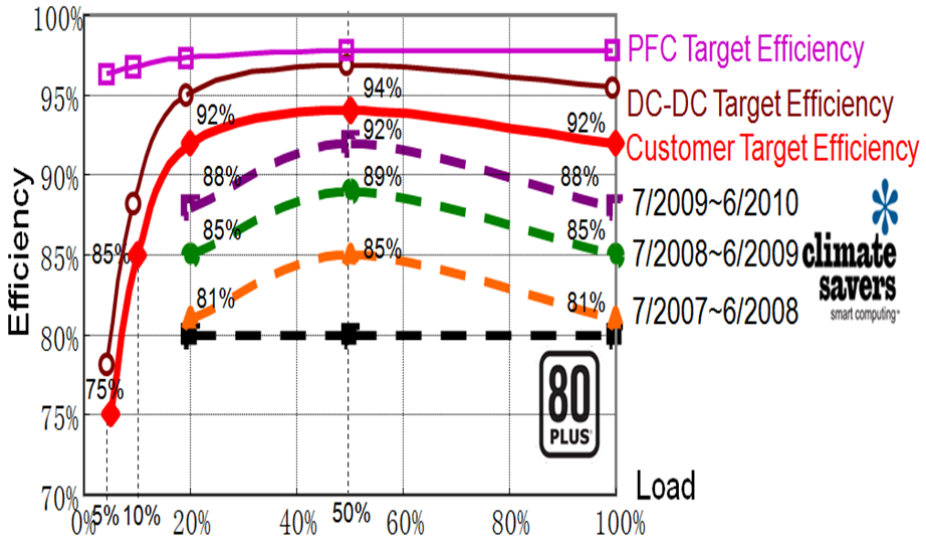


Figure 1-5 Efficiency Requirements for the Front-End Converter

However, with the fast increasing of the power consumption worldwide, the efficiency for the front-end converter is becoming more and more important. As an example, Figure 1-5 shows the increasing efficiency requirement in industry for the front-end converters. The dashed curves in Figure 1-5 show some of the efficiency requirements from organizations such as 80Plus and Climate Savers. The maroon and the pink solid curves in Figure 1-5 are projected DC-DC and PFC target efficiency, respectively, based on the red solid curve, which is the total target efficiency for the front end converter by some mainstream computer manufacture.

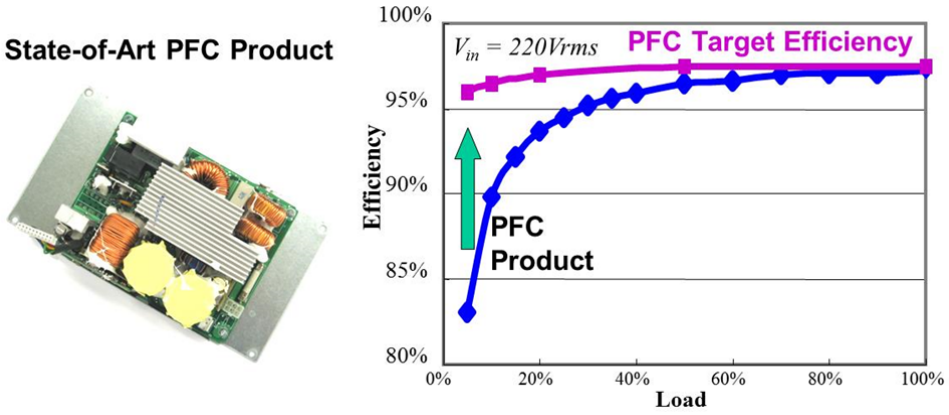


Figure 1-6 Efficiency comparisons between PFC product and the target

To meet the increasing efficiency requirement, power supply companies are trying to use the cutting-edge technology and the latest generation of power components to reduce the power loss. In Figure 1-6, the measured efficiency of one state-of-art CCM Boost PFC converter with average current mode control is compared with the target PFC efficiency shown in Figure 1-5. Although the full load efficiency of this product has already met the target, it clearly demonstrates that there is a big gap, around 6-7%, at 10% load. Now the light load efficiency improvement becomes the most dominant factor in PFC converter design.

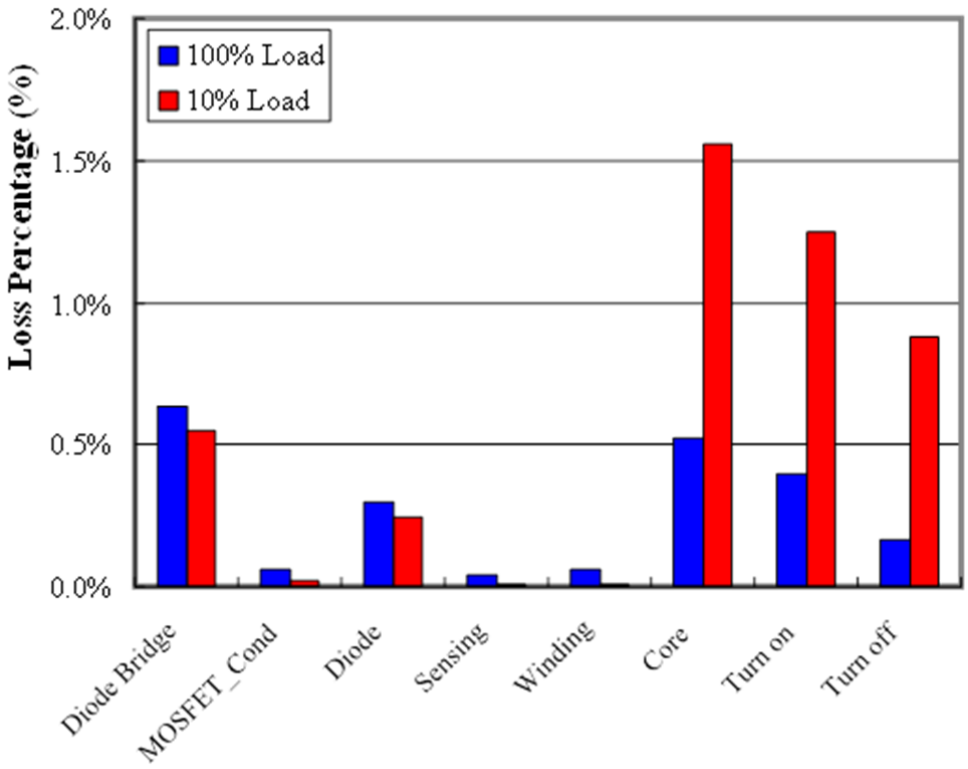


Figure 1-7 Loss break-down in percentage for constant frequency PFC

(Loss Percentage = Loss / Total input power * 100%)

Figure 1-7 shows the comparison of loss break-down in percentage for full load and 10% load conditions in the constant frequency PFC [10]. At full load condition, both conduction loss and switching loss play an important role in the total loss. However, for 10% light load condition, the switching loss is dominant. Therefore to improve light load efficiency, the essential task is to reduce the switching losses. One method which is widely used in VRM converter to improve the light load efficiency is the constant on-time control [11]. As shown as in Figure 1-8, with the constant on-time control, when the load is decreased, the converter will move into discontinuous conduction mode (DCM) and the switching frequency will drop as the load continues decreasing. Since the switching loss is proportional to the switching

frequency, the constant on-time control will definitely help reduce the switching loss and thus increase the efficiency at light load.

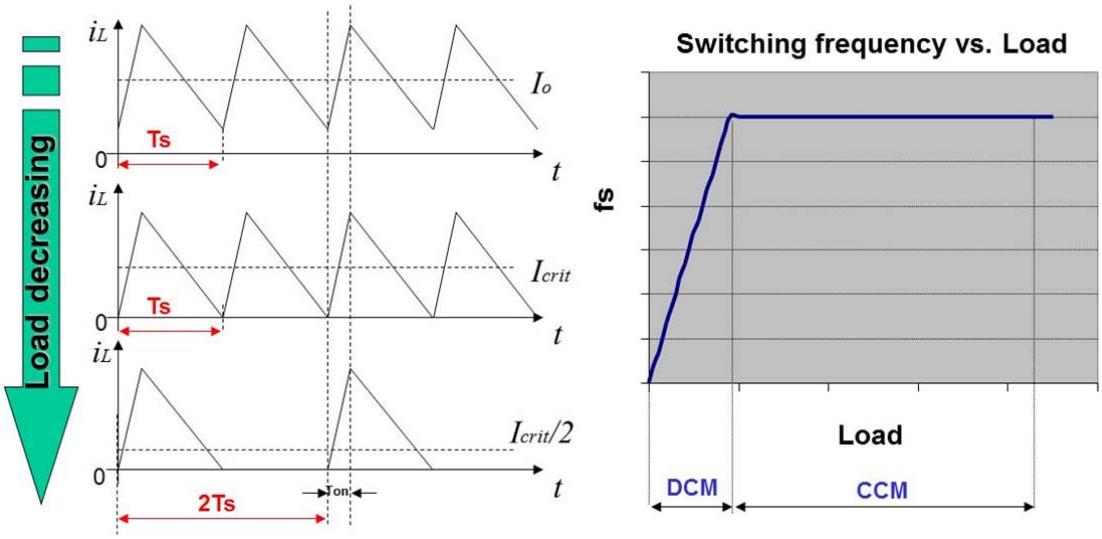


Figure 1-8 Constant on-time control to reduce switching frequency at light load

So the most straight-forward idea would be borrowing the constant on-time control concept and applying it to the PFC converter. The first concern is then, whether it would be causing any detrimental effects on the power factor, which is the fundamental purpose of the PFC converter.

In Figure 1-9, it shows the sketch waveform of the boost inductor current and its average current, the input current, in a Boost PFC with hysteresis control. With the sinusoidal upper and lower current limit, the input current is equal to half of the sum of the upper and lower limit, which is sinusoidal too. And thus the Boost PFC with hysteresis control can achieve very good power factor [12]. By calculating the on time, the period when the inductor current is rising up, we can see that the on time for the Boost PFC with hysteresis control over the half line cycle is almost constant, with only a little discrepancy near the input current zero crossing. Therefore if we apply the

constant on-time control to the same converter, we can expect the similar input current shape. As a quick verification, Figure 1-10 shows the simulation results of the input current and its harmonic current composition at a 1kW constant on-time PFC converter, which can well meet the IEC61000-3-2 Class A limits.

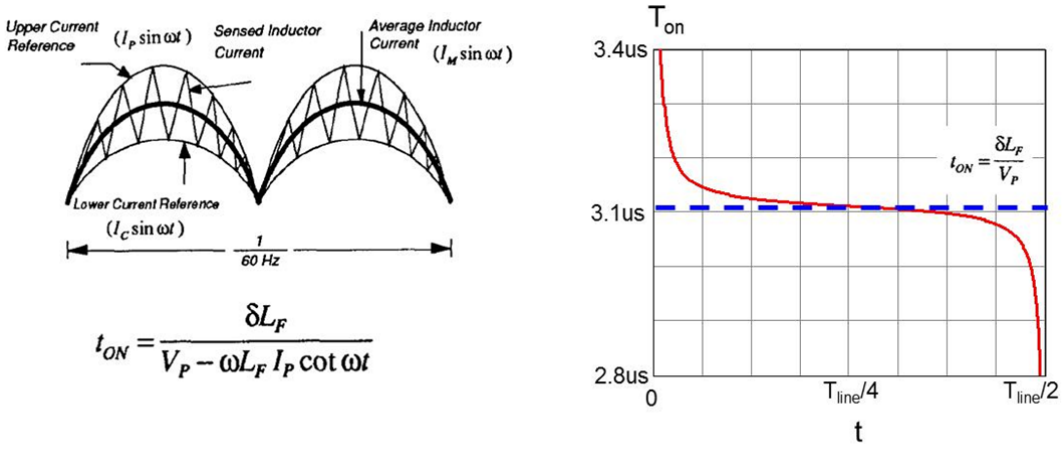


Figure 1-9 On time of Boost PFC converter with hysteresis control

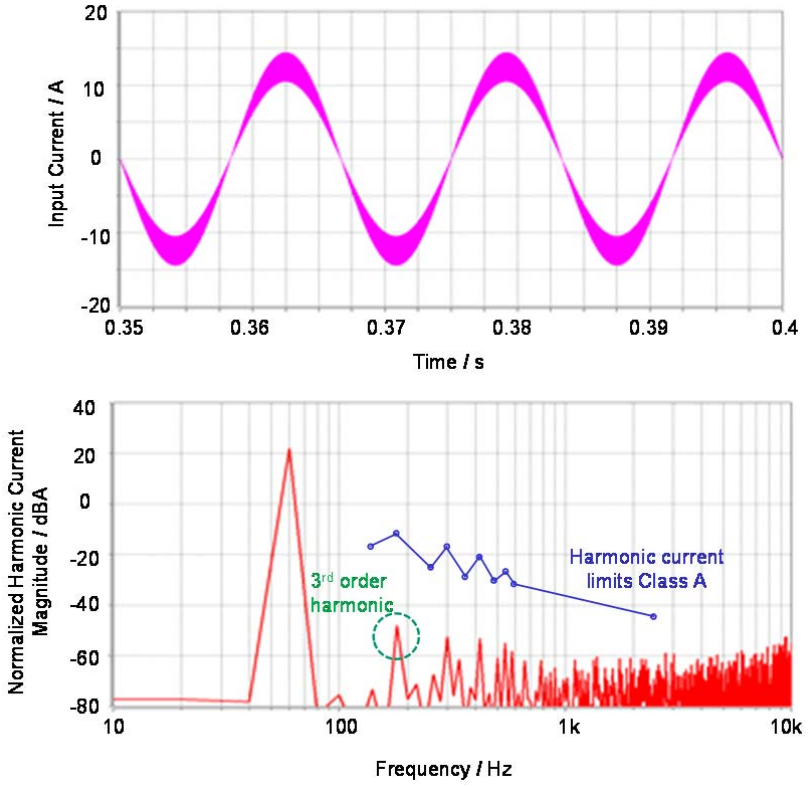


Figure 1-10 Harmonic current Simulation of 1kW constant on-time PFC

1.2.2. Constant on-time control implementation and experiment results

Figure 1-11 shows the general analog control diagram for constant on-time PFC converter [13]. Compared with Figure 1-4, both the constant frequency PFC using average current control and the constant on-time PFC utilize a multiplier to generate the current reference from the AC input voltage. However, for the constant on-time PFC, the current reference serves as the valley current limit of the boost inductor current instead of the average inductor current reference in constant frequency PFC using average current control. When the valley current limit is hit and the boost switch is triggered on, the on time will last for a period of preset Ton. Thus the constant on time PFC can save an error amplifier in the control loop.

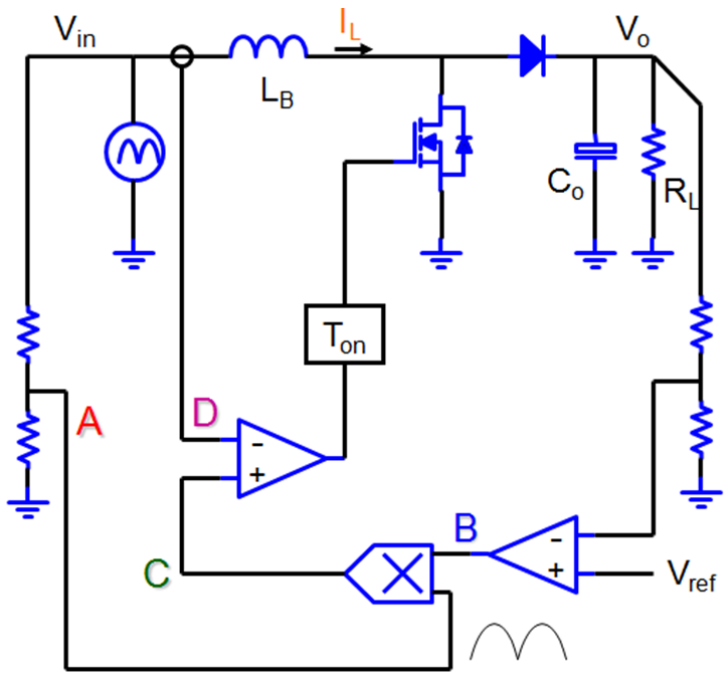


Figure 1-11 Analog control schemes for generalized constant on-time PFC

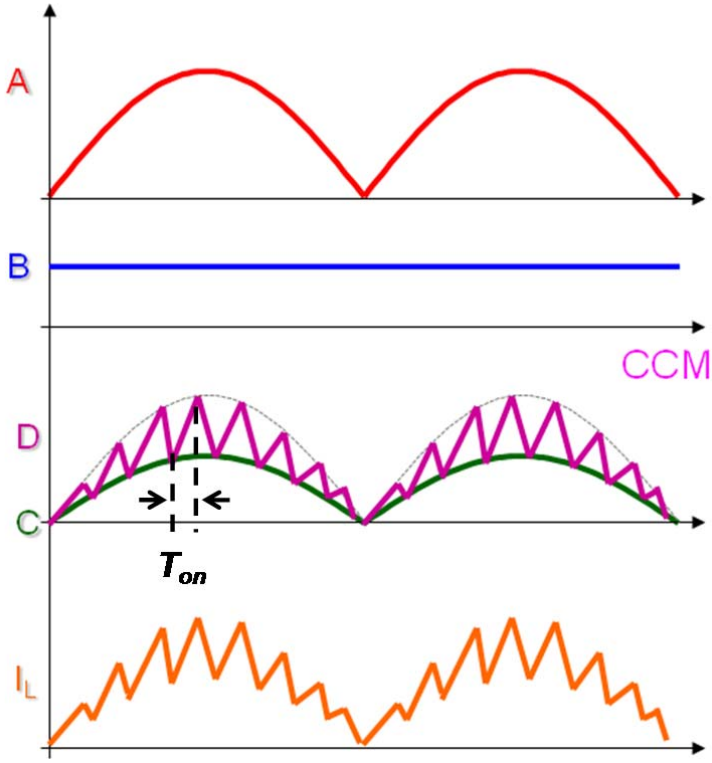


Figure 1-12 Typical Sketch Waveforms for Constant On-time PFC in CCM

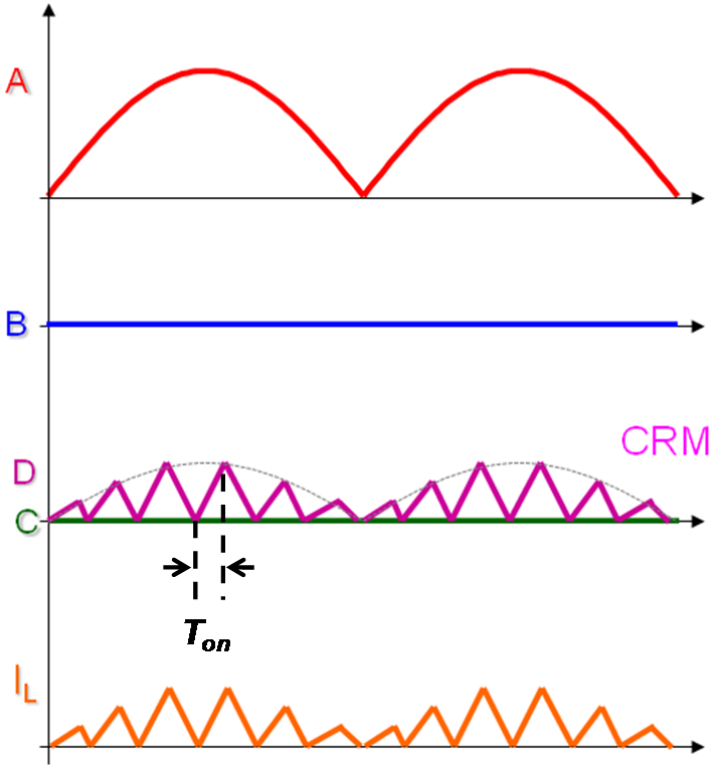


Figure 1-13 Typical Sketch Waveforms for Constant On-time PFC in Boundary Mode

Figure 1-12 – Figure 1-13 show the sketch waveforms of the constant on-time PFC operating in CCM and critical condition mode (CRM, or boundary mode), respectively. For operation in DCM, the control voltage B will need to go negative and thus it requires a negative voltage auxiliary power supply to serve as the valley current limit, which adds the complexity of the analog controller design.

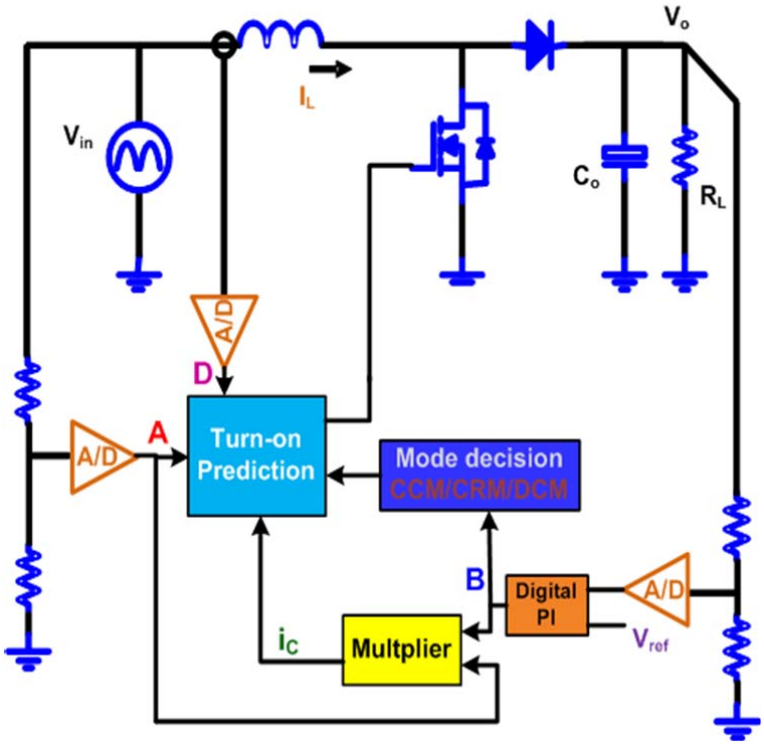


Figure 1-14 Digital control scheme for generalized constant on-time PFC

To overcome the limitation of the analog control scheme, the digital control is utilized to simplify the control logic. Figure 1-14 and 1-15 is the corresponding digital control scheme for generalized constant on-time PFC and its typical sketch waveforms for Constant On-time PFC in DCM. Instead of relying on the negative analog reference signal, the digital PI and multiplier just generate a negative iC value to store in the register. When the inductor current is declining and finally reach zero, a digital ramp is added on the negative iC value and then determine the turning on

instant. Thus the whole control scheme for the CCM, CRM and DCM is unified. . And the prototype of the constant on-time PFC converter based on the digital control scheme is built in CPES to verify the concept. Figure 1-16 and Figure 1-17 show the inductor current experimental waveforms for CCM and DCM, respectively, in a 120VAC, 400Vout, 400W constant on-time PFC.

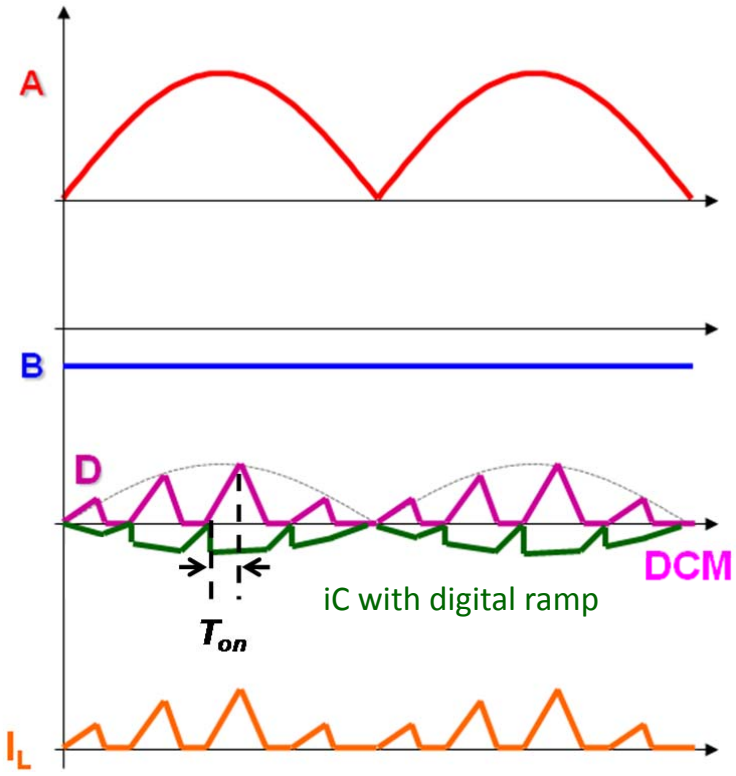


Figure 1-15 Typical Sketch Waveforms for Digital Constant On-time PFC in DCM

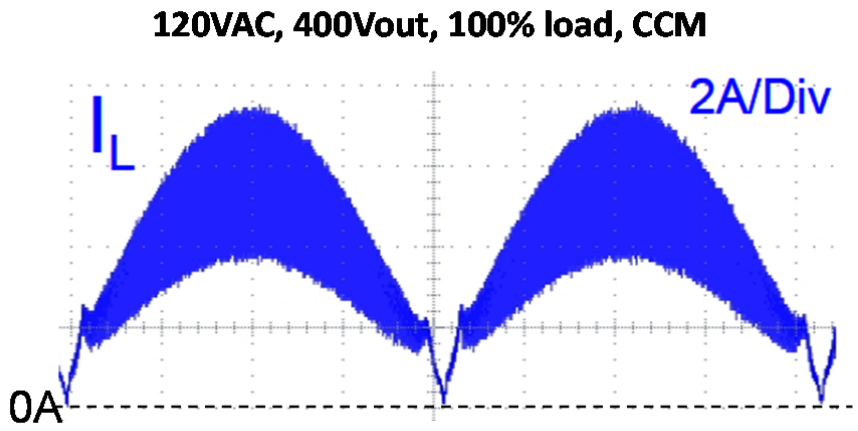


Figure 1-16 Inductor current experimental waveforms for On-time PFC in CCM

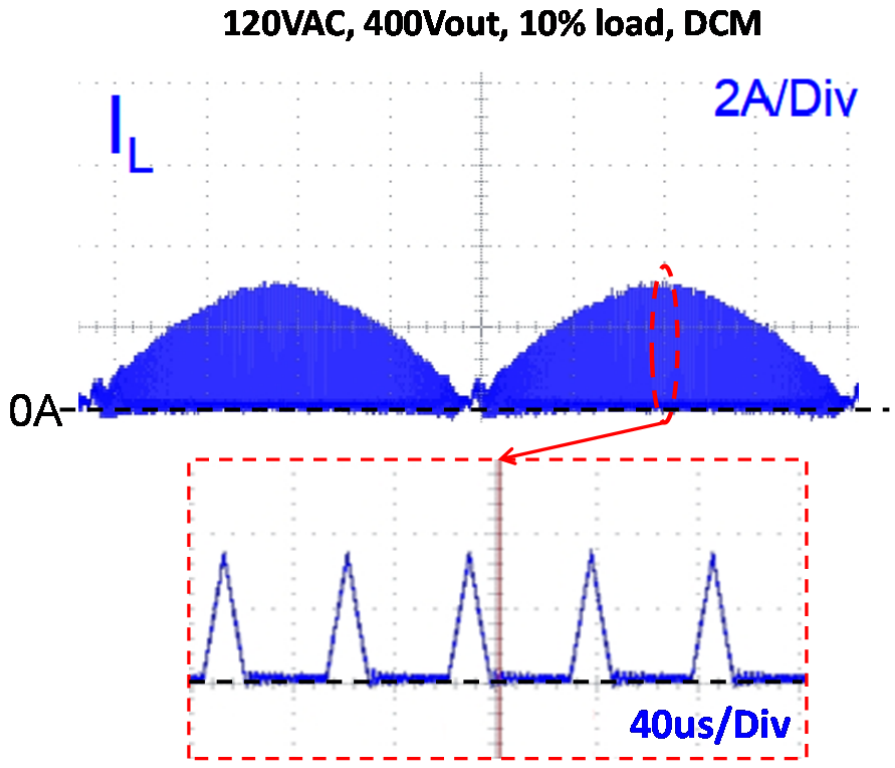


Figure 1-17 Inductor current experimental waveforms for On-time PFC in DCM

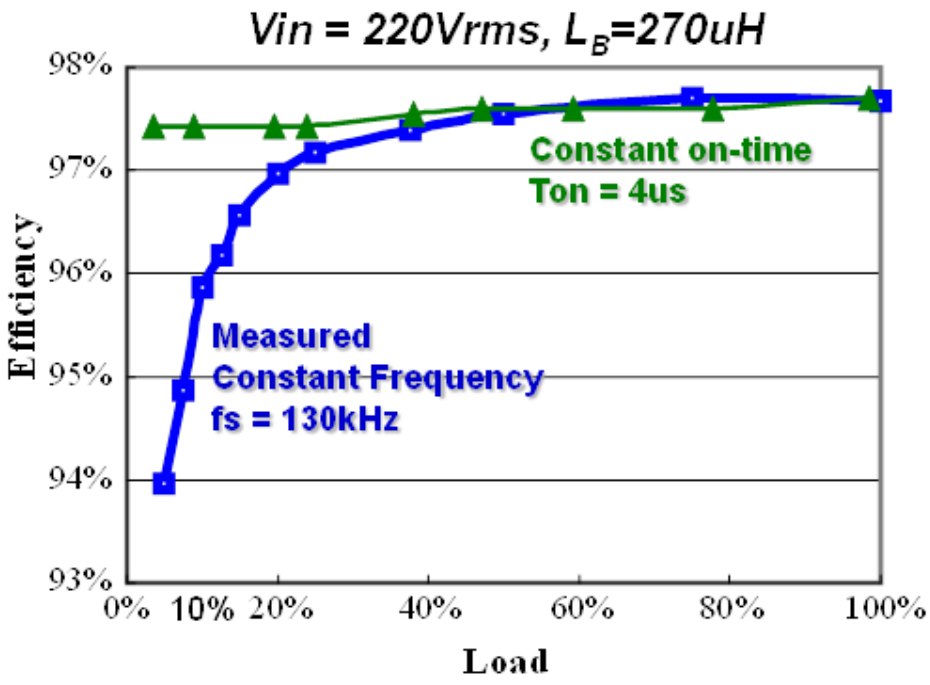


Figure 1-18 Efficiency comparison: constant frequency vs. constant on-time

From Figure 1-15 it is clear that the switching frequency is reduced due to the increased dead time in DCM at light load and the zoom-in waveforms in Figure 1-17 prove its validity. Figure 1-18 [14] shows the measured efficiency comparison between constant frequency PFC and constant on-time PFC, both of which are the start-of-art designs in CPES with the same boost inductor and the same peak inductor current. From the comparison we can see that more than 3% efficiency improvement is achieved at around 10% light load and the efficiency curve for the constant on-time PFC is almost flat for the whole load range.

Although the light load efficiency problem is tackled in the constant on-time PFC, which is the original purpose of such control scheme, this is not the end. The EMI performance of such constant on-time PFC [15], which is mandatory from the

regulation point of view or critical from the design point of view because of the EMI filter design, is not clear yet, which is worth to be further investigated.

1.3. Introduction to Critical Conduction Mode Boost PFC

For the constant on-time PFC converter introduced in Section 1.2, it can operate in continuous current mode (CCM), critical conduction mode (CRM) and discontinuous current mode (DCM) at different load conditions. Particularly, the Critical Conduction Mode Boost PFC has been widely used in industry well before this proposed constant on-time control [21][22][23]. One special merit for CRM Boost PFC is that it relieves the concern of the high frequency EMI noise caused by the reverse recovery procedure of the output diode, which otherwise will be very complicated to deal with. As a very interesting operation mode, some analysis and comparisons are done below between CRM and CCM.

1.3.1. CRM vs. CCM: Negligible output diode reverse recovery

One important benefit of the CRM boost PFC over the traditional constant frequency CCM PFC is its ZCS to minimize the output diode reverse recovery, which not only reduces the reverse recovery related turn-on loss but also reduce the radiated EMI noise [27]. It will be better to understand this procedure with an analytical way to quantify it.

Figure 1-19 shows the typical waveforms of the diode reverse recovery process in a CCM boost PFC and all the relate variables are defined [28]. To calculate the reverse recovery related turning on loss, the key parameter is the total reverse recovery charge, Q_{rr}. The falling slope di/dt of the diode current i_{Diode} when the main switch Q is turned on is limited by the equivalent parasitic inductance $L_{parasitic}$. Since Lparasitic is very small, a huge di/dt up to 500A/us can be expected. However, in a

CRM boost PFC, the di/dt is limited by the boost inductance L_B. Figure 1-20 shows the comparison and the difference.

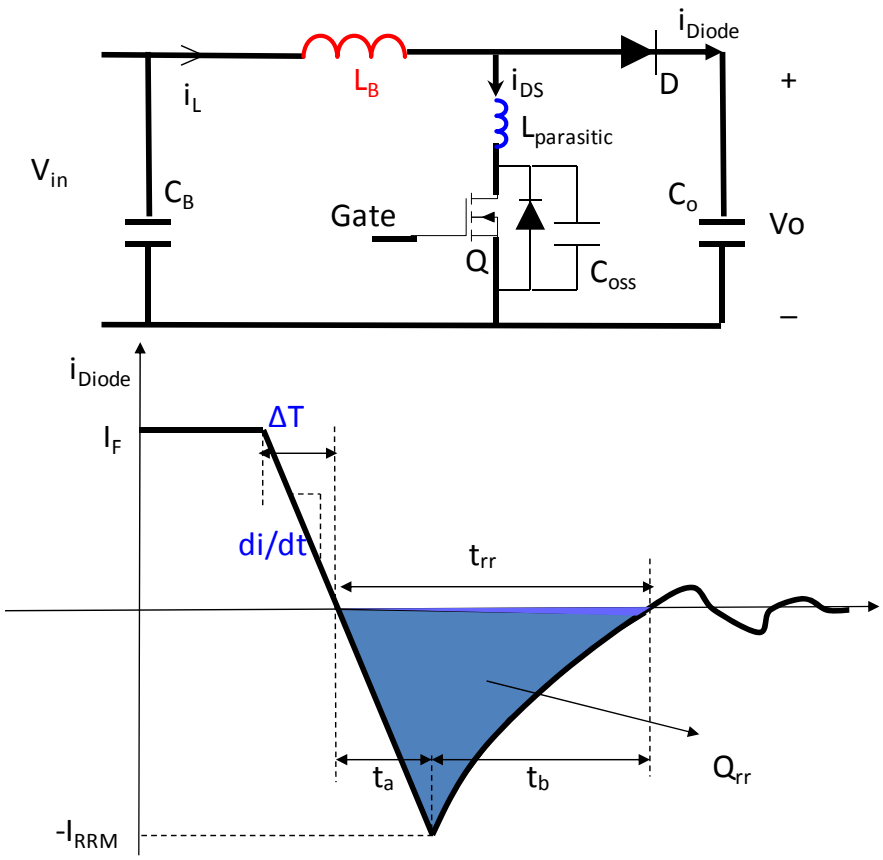


Figure 1-19 Diode reverse recovery sketch in the CCM boost PFC

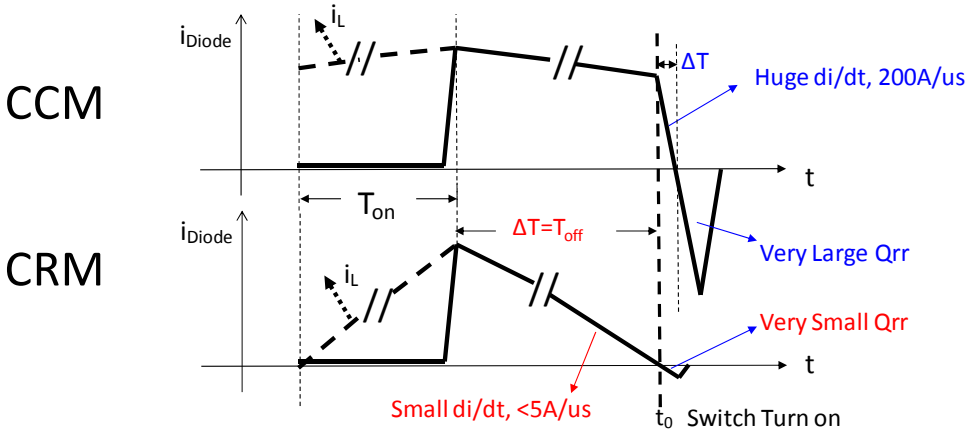


Figure 1-20 Comparison of diode reverse recover process: CCM vs. CRM

To quantify the small Q_{rr} during the diode reverse recovery in the CRM boost

PFC, we need to review the mechanism of the reverse recovery and apply it to the special conditions in the CRM boost PFC. When the inductor current reaches zero, the diode current i_{diode} reaches zero too. Before the inductor current can go negative and the diode is reverse biased, the minority charge stored in the diode need to be first removed. There are two mechanisms for the removal of this charge: the passive removal through the recombination inside the diode and the active removal through the diode reverse recovery current [29]. If we define the minority charge for the CCM/CRM boost PFC Q_0, the recombination charge is Q_C. Then,

$$Q_{rr} = Q_0 - Q_C < Q_0 \tag{1-1}$$

Therefore if we can quantify the value of the Q_0, we have got the upper limit of the reverse recovery charge Q_{rr}.

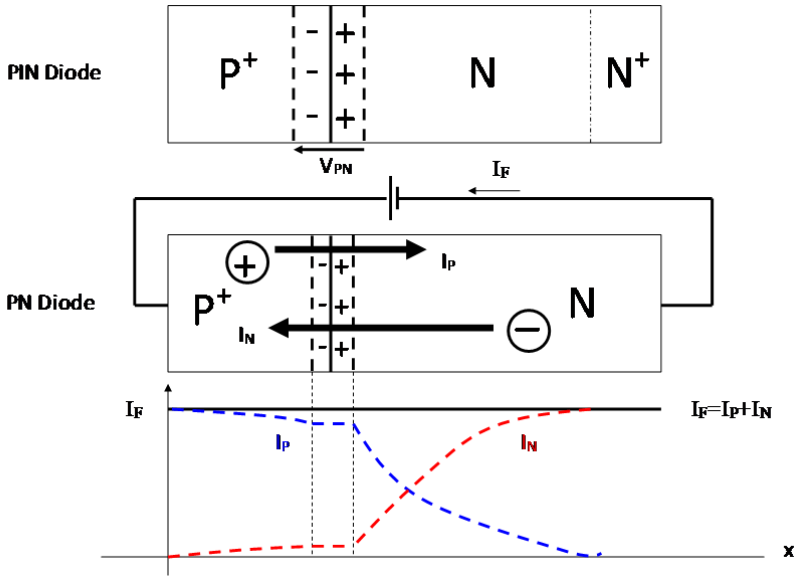


Figure 1-21 Current density distribution inside the PIN diode

As shown in Figure 1-21, inside the PIN diode without any external bias, there is built-in electrical field V_{PN}. With the forward bias, the holes in the anode move into the cathode, generating the current I_P. The electrons in the cathode move

into the anode, generating the current I_N. And the sum of I_P and I_N is equal to the diode forward current. Because the doping concentration of the holes in P+ region is much larger that of the electrons in N region, the density of the electrons, as the minority in the P+ region is much smaller than that of the holes, as the minority in the N region. Then the current density distribution in Figure 1-21 can be approximately simplified as in Figure 1-22.

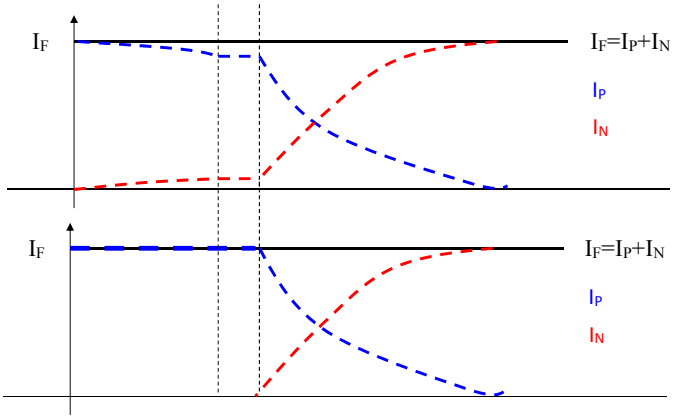


Figure 1-22 Simplified current density distribution inside the PIN diode

If we define the number of the total injected holes to the N region at time t as NP(t), then [30],

$$I_F(t)\mathrm{d}t - q\frac{N_P(t)}{\tau_P}\mathrm{d}t = q\mathrm{d}N_P(t) \tag{1-2}$$

Equation (1-2) can be rewritten as,

$$\frac{\mathrm{d}Q_P(t)}{\mathrm{d}t} + \frac{Q_P(t)}{\tau_P} - I_F(t) = 0 \tag{1-3}$$

Solve equation (1-3) and we can obtain the solution for the minority charge,

$$Q_0 = Q_P(t)|_{t=t0} = \tau_P{}^2\frac{\mathrm{d}i}{\mathrm{d}t}(1-e^{-\frac{\Delta T}{\tau_P}}) \tag{1-4}$$

In equation (1-4), all the parameters are available as shown in Figure 1-20 except for the minority carrier life constant τ_P. Since the Qrr information is often available in the diode datasheet with given di/dt in CCM, we can calculate the τ_P first and then use

it to calculate the Qrr in CRM.

As an example, for the ultra-fast recovery diode MUR860, the Qrr at I_F = 8A and di/dt = 200A/us is 195nC [31]. For the CCM case, the minority charge removal is generally dominated by the reverse recovery current and thus Q0 ≈ Qrr = 195nC. Therefore the calculated result for the τ_P is 40ns for the MUR860. For the CRM boost PFC with the L_B = 200uH, the max di/dt during the half line cycle is 2A/us. Thus the calculated max Q0 is 3.2nC and the max Qrr is even smaller. Another example with the UFRD STTH5L06 gives the result of max Q0 = 6.7nC in CRM, with the minority charge around 200nC in CCM [32]. In a word, the reverse recovery energy is negligible in the CRM boost PFC with several hundred kHz switching frequency, which will be enabling the potential applications with several MHz switching frequency.

1.3.2. CRM vs. CCM: High Frequency Soft-Switching Using GaN Device

Another trend in front-end converter is the more and more demand on smaller size which requires higher and higher power density. With the emerging of the high voltage GaN device, this trend is becoming clearer. Table 2 shows the switching characteristic comparison between GaN HEMT [16] and Si MOSFET [17].

Table 2 Characteristics comparison between GaN HEMT and Si MOSFET

	Parameter	GaN HEMT	Si MOSFET (IPP60R160C6)
Static	V_{DS}	600V	600V
	R_{DS}	0.15Ω/0.18Ω	0.14Ω/0.16Ω
Dynamic	Q_g	6.2nC	75nC
	Q_{gd}	2.2nC	38nC
	E_{oss}	6uJ	11uJ
	Q_{oss}	28nC	130nC
Reverse Operation	Q_{rr}	54nC	8200nC
	t_{rr}	30ns	460ns

It could be seen that with similar Rdson, the GaN HEMT device has much smaller gate charge and reverse recovery charge. It is thus desirable to push the switching frequency of the converter higher to reduce the converter size. A boost converter with 200Vin, 400Vout, 1200W full power is built in CPES and the schematic is shown below [18].

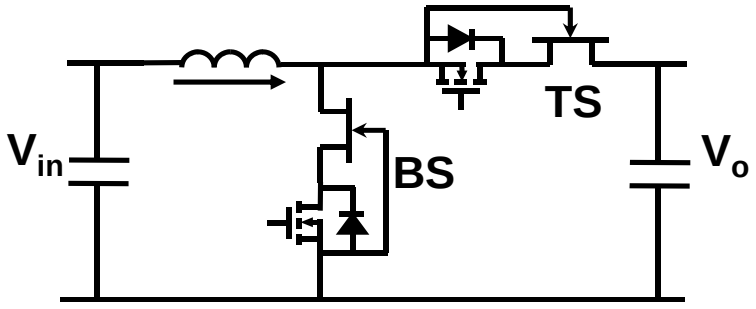


Figure 1-23 Boost converter schematic sketches with cascade GaN device

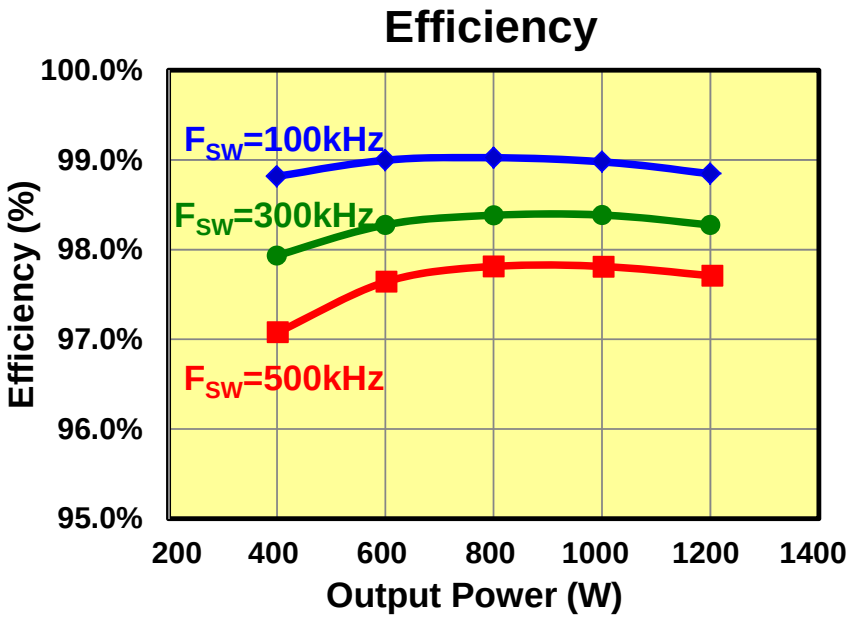


Figure 1-24 Efficiency drop due to increased switching frequency

However, with hard switching, as the switching frequency increased, the switching loss for GaN device is not negligible yet and causing the efficiency drops rapidly. As an example, Figure 1-24 shows the efficiency drop in 200Vin, 400Vout, 1200W full power boost converter using GaN HEMT devices. By simulation, it is discovered most loss is due to the reverse recovery and energy dissipation in the parasitic output capacitance of the GaN HEMT while top switch turns on, shown as in Figure 1-25. To reduce the turn-on switching loss, soft switching techniques are necessary for converters operating beyond MHz. Figure 1-26 shows the key simulation waveforms of CCM hard switching vs. CRM soft switching. As the comparison, Figure 1-27 shows the loss reduction by using the soft switching techniques.

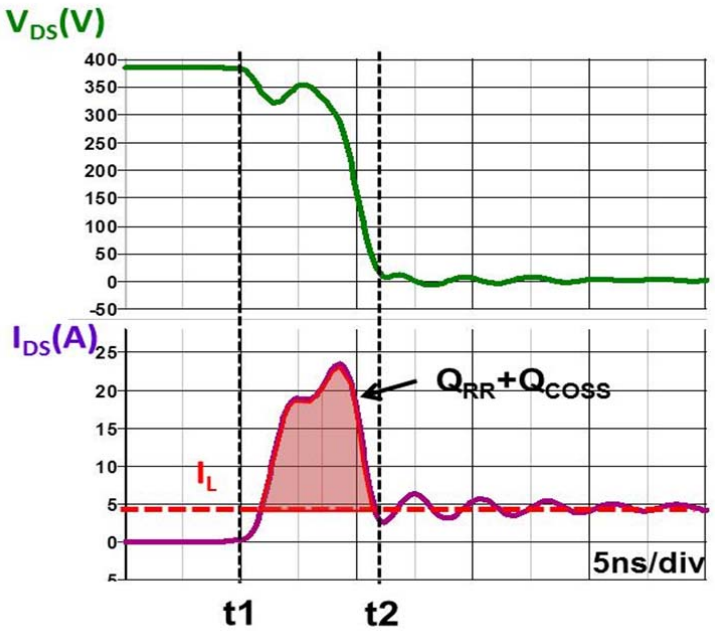


Figure 1-25 Simulation for bottom switch turn-on

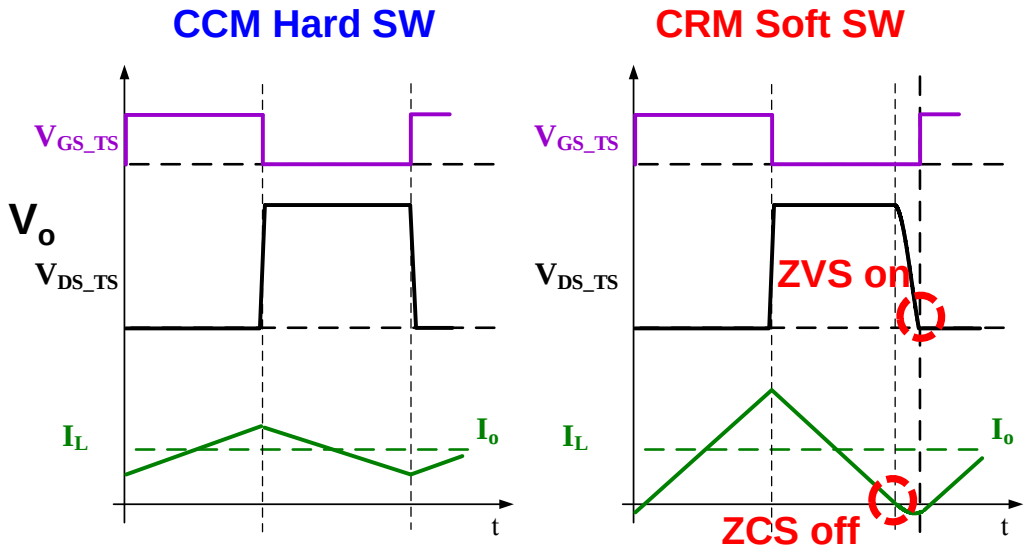


Figure 1-26 Simulation waveforms of CCM hard switching vs. CRM soft switching

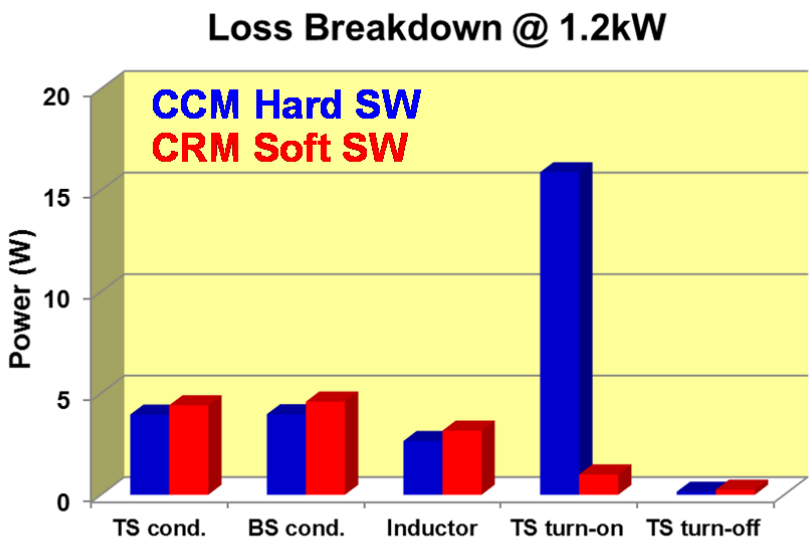


Figure 1-27 Loss reduction by using the soft switching techniques

1.3.3. Critical Conduction Mode PFC control scheme

Similarly, to reduce the turn-on loss and further boost the efficiency of the PFC converter, the soft switching techniques are the key. In recent years, the critical conduction mode (CRM) boost PFC converter is drawing more and more attention [19][20]. It is actually operating in the boundary condition of the CCM and DCM [21], and thus also called boundary condition mode (BCM) PFC and could be considered as a special case of the constant on-time PFC. There are two major control schemes for CRM boost PFC, current mode control [22] and voltage mode control [23], shown in Figure 1-28 and 1-29, respectively.

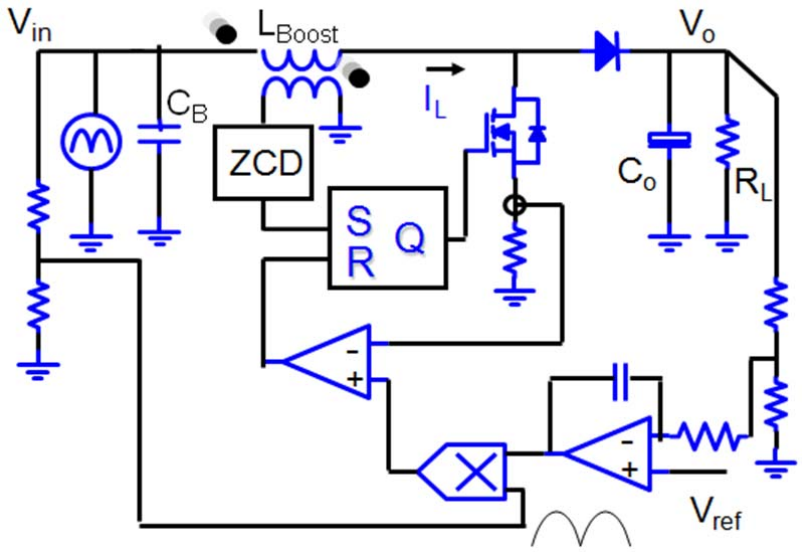


Figure 1-28 Current Mode Control Scheme for CRM Boost PFC

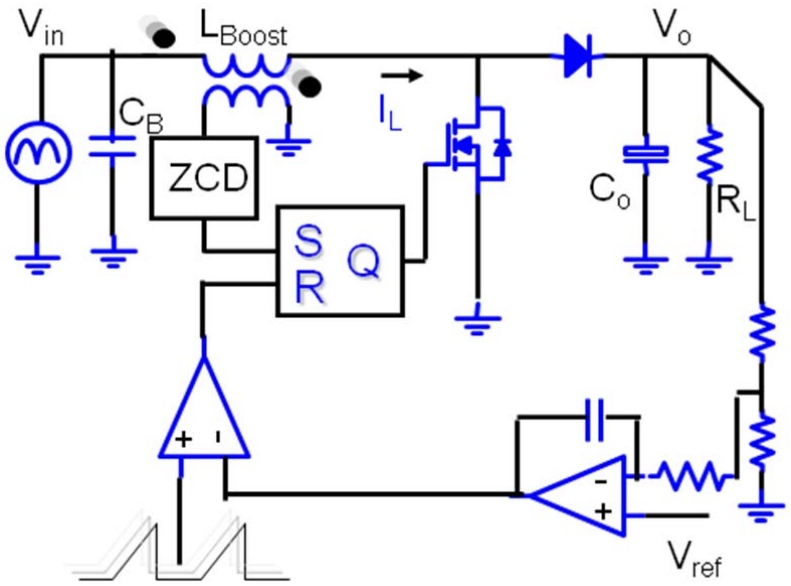


Figure 1-29 Voltage Mode Control Scheme for CRM Boost PFC

Comparing the two control schemes we can find that both control schemes use an auxiliary winding to detect when the inductor current reach zero to achieve zero current turning-on. The difference is the turning-off mechanism. Shown in Figure 1-30, for the voltage mode control, the on time of the switch is determined by the

control voltage, the output of the voltage loop compensator, and a saw tooth waveform with fixed rising slope. After the switch is turned on, the saw tooth waveform will increase and when it is equal to the control voltage, the switch will be turned off and the saw tooth waveform will be reset to zero. Then the inductor current begins to decrease.

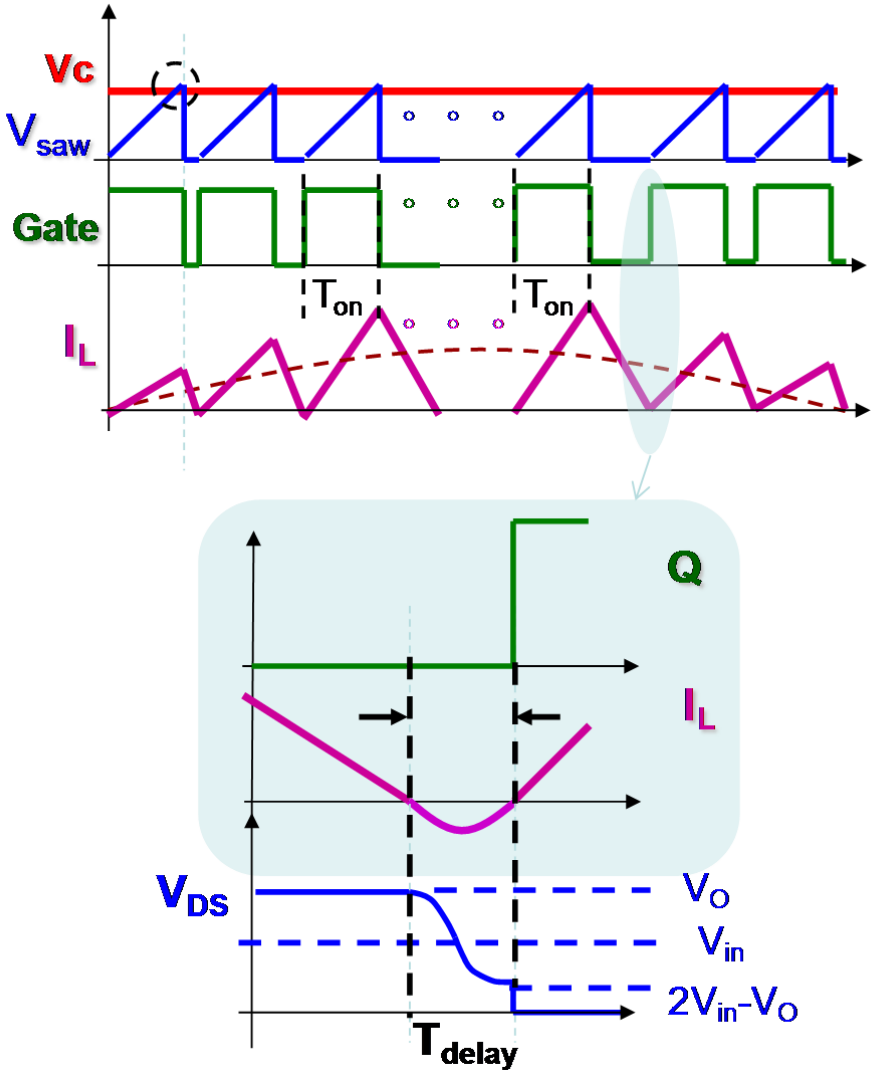


Figure 1-30 Waveforms Sketch for CRM Boost PFC with Voltage Mode Control

(Zooming-in for Valley Switching: 2Vin >= Vo)

For the current mode control, the current reference of the peak inductor current is

obtained by multiplying the sampled input voltage with the control voltage. When the inductor current is equal to the reference, the switch will be turned off.

Compared with the voltage mode control, the current mode control needs extra circuits to sample the input voltage and the drain to source current of the switch and also the multiplier to obtain the current reference. Thus, the simplicity of the voltage mode control makes it more and more popular, especially in interleaved CRM boost PFC converters [24][25][26]. Figure 1-30 shows the detailed waveforms in CRM boost PFC with voltage mode control.

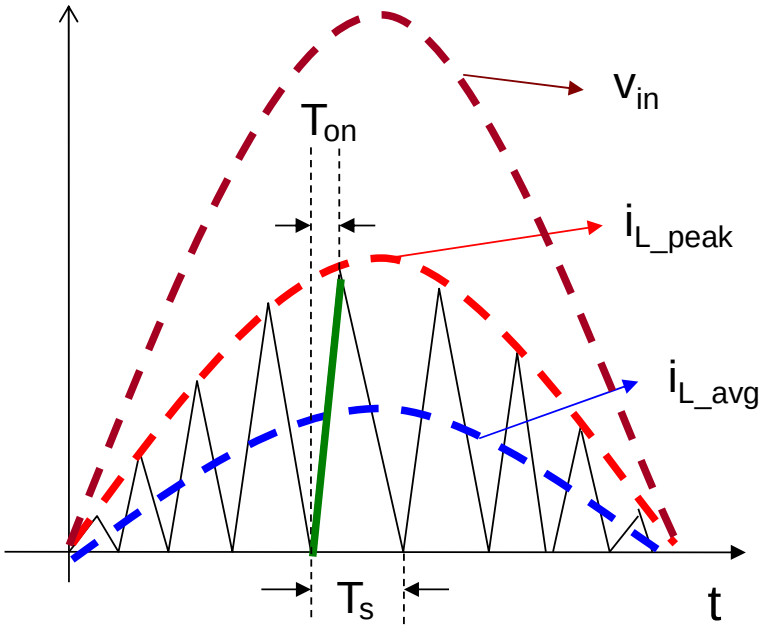


Figure 1-31 Inductor Current Waveform Sketch

Because of the low bandwidth of the voltage feedback loop in the PFC converter, the control voltage can be treated as a constant value in a half line cycle, which means the on time is constant for a half-line cycle. This would guarantee a unit power factor, theoretically, because, as shown in Figure 1-31,

$$i_{L\_avg}(t)=\frac{1}{2}i_{L\_peak}(t)=\frac{1}{2}T_{on}\frac{v_{in}(t)}{L_B}=\frac{1}{2}T_{on}\frac{\sqrt{2}V_{RMS}\left|\sin(\omega t)\right|}{L_B}\propto\sin(\omega t)$$

(1-5)

And it is also shown in Figure 1-30 that when the inductor current decreases to zero, actually the switch will not be turned on immediately but with a short delay, which allows the boost inductor to be resonant with the parasitic output capacitor of the switch and the parasitic capacitor of the output diode. This resonance will help to reduce the drain to source voltage of the switch and thus reduce the turn-on loss. Actually, when the instantaneous input voltage is smaller than half of the output voltage V_O, the V_{DS} can drop to zero and thus zero voltage switching (ZVS) can be achieved. When the instantaneous input voltage is larger than half of the output voltage Vo, valley switching could be achieved, with the minimum $V_{DS}=2V_{in}(t)-V_O$ at turning on instant.

However, the portion of small negative resonant current will add to the input current distortion, especially at high frequency operation. Figure 1-32 [33] show the comparison of the simulated inductor current and input current at low frequency operation and high frequency operation. From the simulation it is clear at high frequency operation the magnitude of the negative resonant current becomes not negligible anymore and the non-energy transfer time around line voltage zero crossing in which the average inductor current is zero is dramatically increased. And therefore the total harmonic distortion is dramatically increased. Such distortion can be compensated through programmed on time control, as explained in [34], to purposely increase the on time near the line voltage zero crossing. Figure 1-34 shows the result

[33] after the programmed on time control is applied and we can see that the input current distortion is greatly relieved. For EMI analysis in this dissertation, since the targeted switching frequency range is below 1 MHz, this small negative resonant current is considered zero for simplicity.

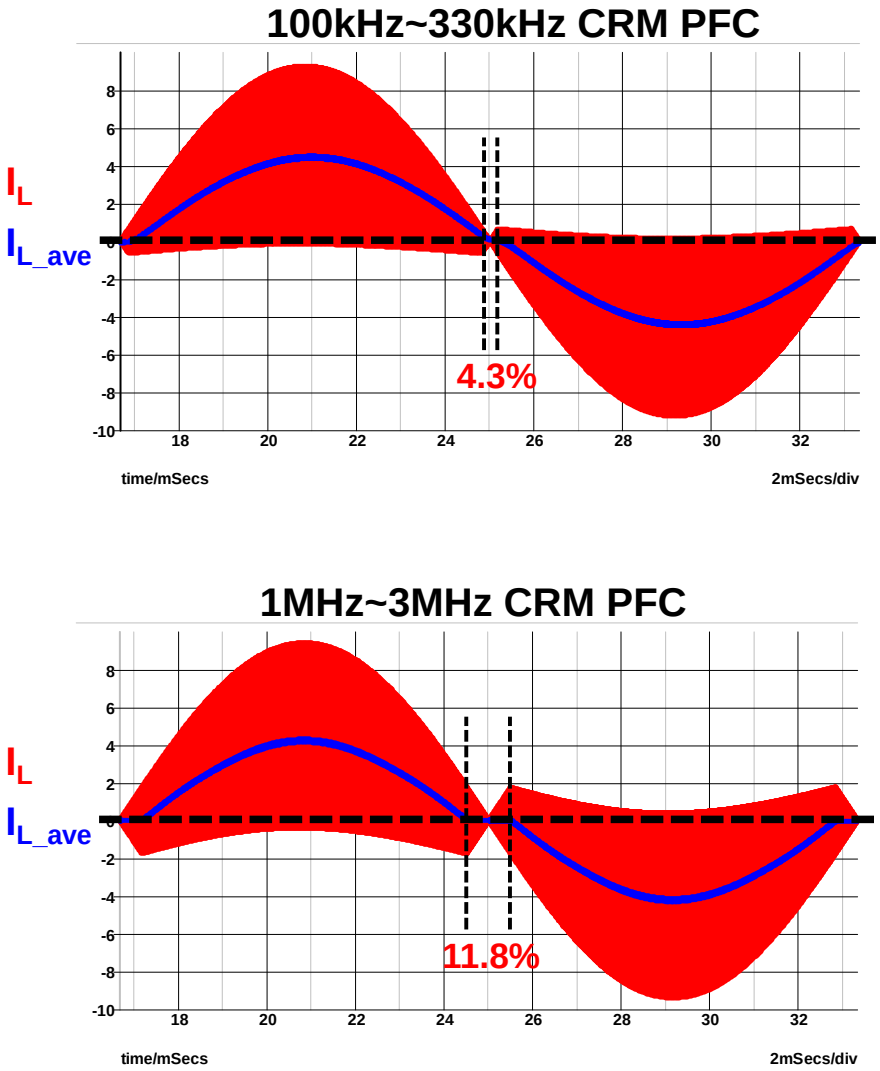


Figure 1-32 comparison of simulated input current [33]

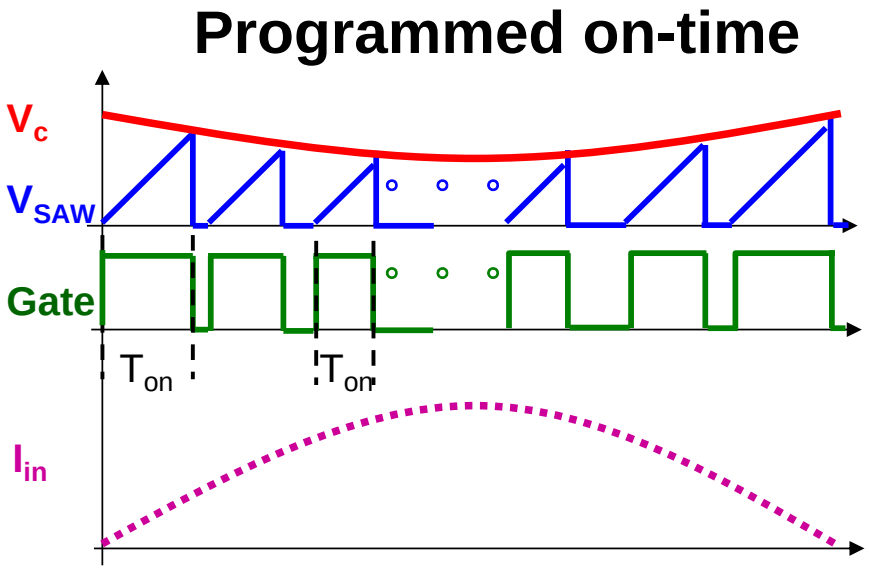


Figure 1-33 Programmed on time control with no zero crossing distortion

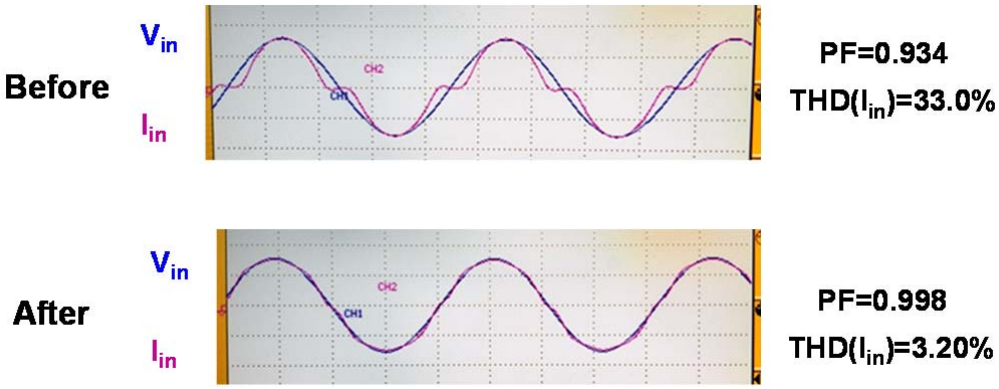


Figure 1-34 Input current THD improvement with programmed on-time control [33]

1.4. EMI challenge on constant on-time PFC and CRM boost PFC

For conducted EMI noise, it is often separated to two categories for easier analysis: DM EMI noise and CM EMI noise. There is a lot of academic research and industry practice focusing on CM EMI noise cancellation [35][36], which greatly reduce the size of the necessary CM EMI filter. However, for DM EMI noise, since it shares the same path with the active power transmission, it is usually very hard to do the noise cancellation. Most of the time, it is solely dependent on the DM EMI filter to attenuate the noise. In this dissertation, the discussion of the EMI noise analysis will mainly focus on the DM EMI noise, though the methodology can be also applied to the CM EMI noise.

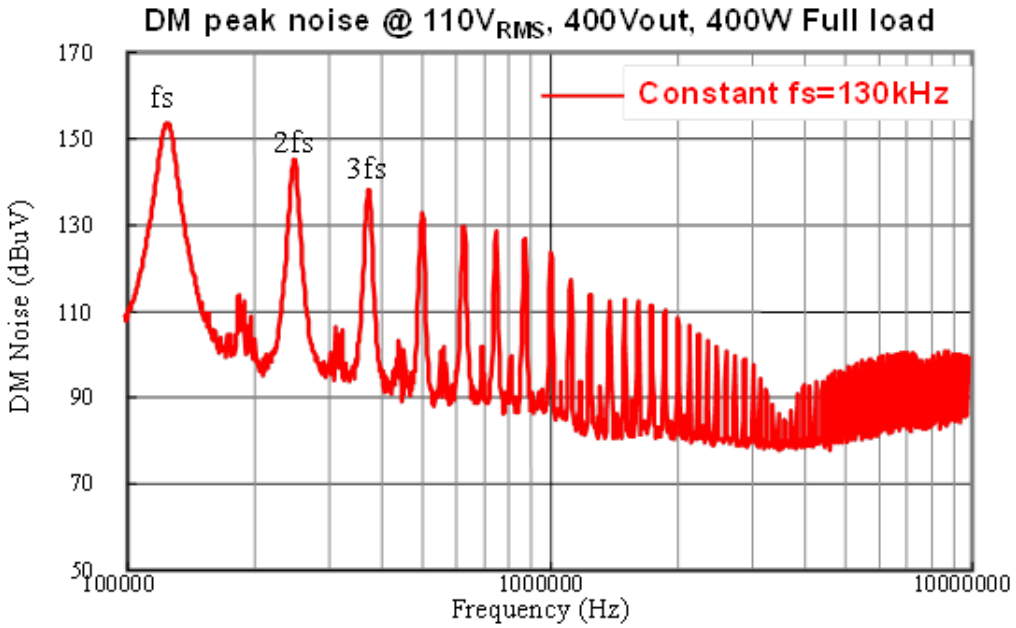


Figure 1-35 DM EMI noise measurements for constant frequency PFC

Figure 1-35 shows the measured DM EMI noise spectrum for a constant frequency PFC with fs = 130 kHz. From the measurement we can see that for constant frequency PFC, the noise spectrum is mainly comprised of several discrete noise

peaks at the fundamental switching frequency and its harmonic frequencies. For CISPR 22, because the standard starts to regulate the EMI noise from 150 kHz, we don't need to worry about the noise peak at 130 kHz. And thus the noise peak caused by the second order harmonics will be the dominant factor for EMI filter design. By applying the Fourier analysis to the constant frequency noise source, it is straight-forward to abstract the amplitude of the second order harmonics, which is corresponding to the noise peak at 260kHz. And further, for given EMI filter structure, the corner frequency of the EMI filter for the constant frequency PFC converter can be obtained. Figure 1-36 shows the relationship between EMI filter corner frequency and the switching frequency, which can be taken as the DM EMI filter design guidance for constant frequency PFC [37].

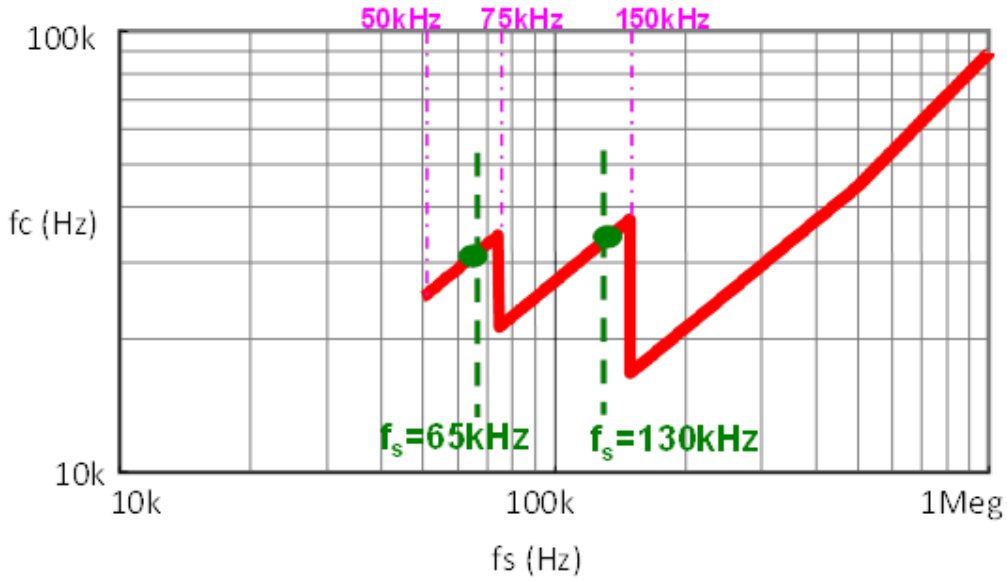


Figure 1-36 DM EMI filter corner frequency fc vs. switching frequency fs

1.4.1. Variable switching frequency and wide frequency range

However, the case for constant on-time PFC and CRM Boost PFC is totally different. Equation (1-6) is the equation for the switching frequency of the constant on-time PFC in CCM over a half line cycle.

$$f_s(t) = \frac{1}{T_{on}}\left(1 - \frac{V_{in}(t)}{V_o}\right) \tag{1-6}$$

And thus the maximum and minimum switching frequency is, respectively,

$$f_{s\_\max} = \frac{1}{T_{on}} \tag{1-7}$$

$$f_{s\_\min} = \frac{1}{T_{on}}(1 - \frac{\sqrt{2}V_{in\_rms}}{V_O}) \tag{1-8}$$

Therefore, the switching frequency is variable during the half line cycle and also dependent on the AC line RMS voltage and the on time selection Ton. The maximum switching frequency is determined by the on time and the minimum switching frequency always happen at the peak input voltage. Figure 1-37 shows the switching frequency profile with different input line and different on time selection. At high line with Ton = 4us, the switching frequency varies in a large range from around 50 kHz to 250 kHz.

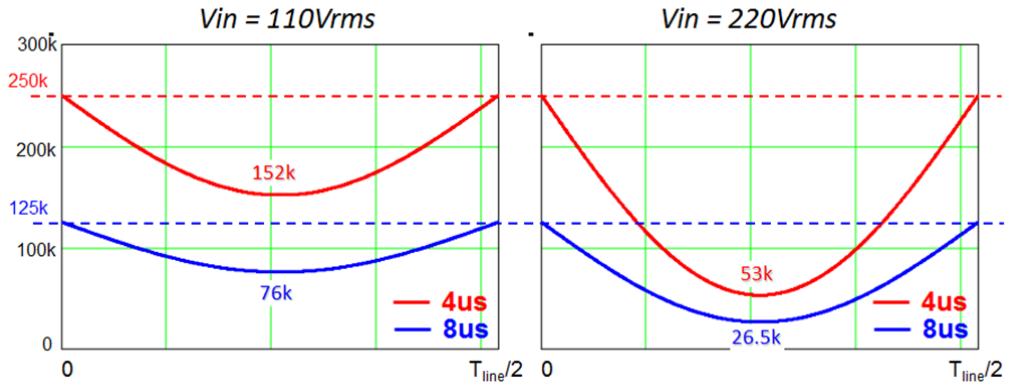


Figure 1-37 Switching frequency profile for constant on-time PFC

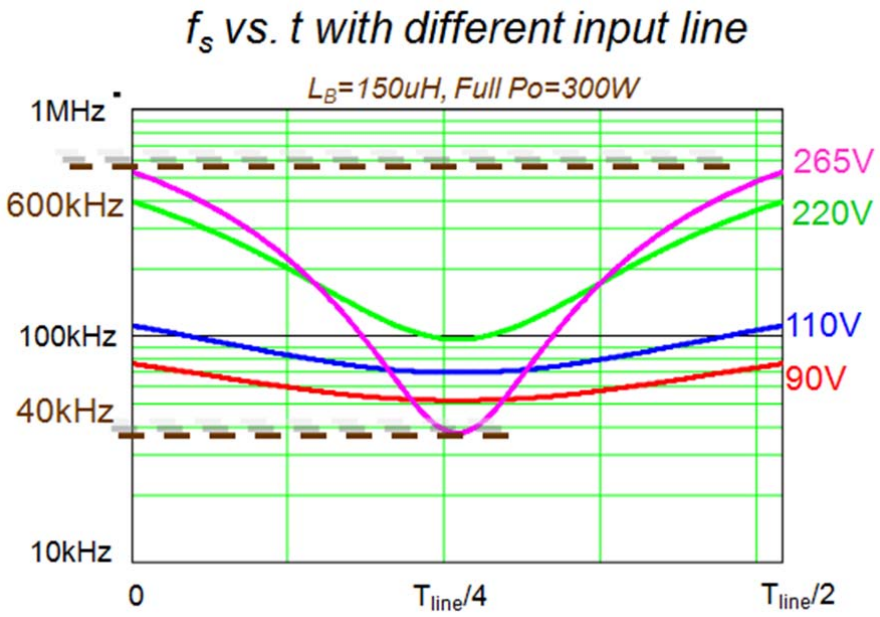


Figure 1-38 Switching Frequency Varies with Input Line for CRM Boost PFC

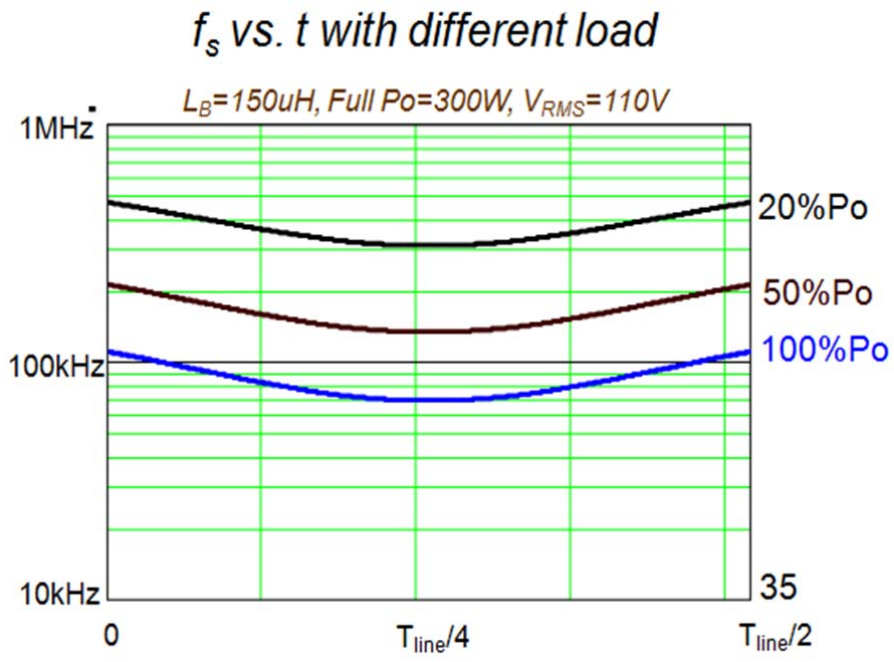


Figure 1-39 Switching Frequency Varies with Output Load for CRM Boost PFC

As for CRM Boost PFC, similar equations for the switching frequency can be derived and as shown in Figure 1-38 and Figure 1-39, it not only varies with the input line voltage, but also varies with load conditions. The frequency range can

be a very wide range from around 40 kHz to roughly 600 kHz.

Variable switching frequency and wide frequency range bring several obvious challenges. First, because the switching frequency is variable during the half line cycle, it is impossible to directly apply the Fourier analysis or even double Fourier analysis to the noise source, making the analytical investigation difficult to move forward. On the other hand, because the switching frequency is also dependent on the input line conditions and other design parameters, these variables make the evaluation of the complete EMI performance rather complex and time consuming if done by EMI measurements.

Second, because of the large switching frequency range, the fundamental noise component and its each order harmonics may overlap with each other, which makes it harder to play the strategy of selecting suitable switching frequency to improve EMI performance. As an example, Figure 1-40 shows the DM EMI noise comparison between constant frequency PFC and constant on-time PFC. For the constant frequency PFC, it is an easy decision to make the switching frequency a little blow 150 kHz, for example 130kHz in this case, to avoid EMC regulation starting from 150 kHz. However, for the constant on-time PFC, effort to make the fundamental components below 150 kHz will move the second order harmonics close to or even cross the 150 kHz. Therefore, frequency selection or design strategy need to be adjusted based on thorough EMI analysis.

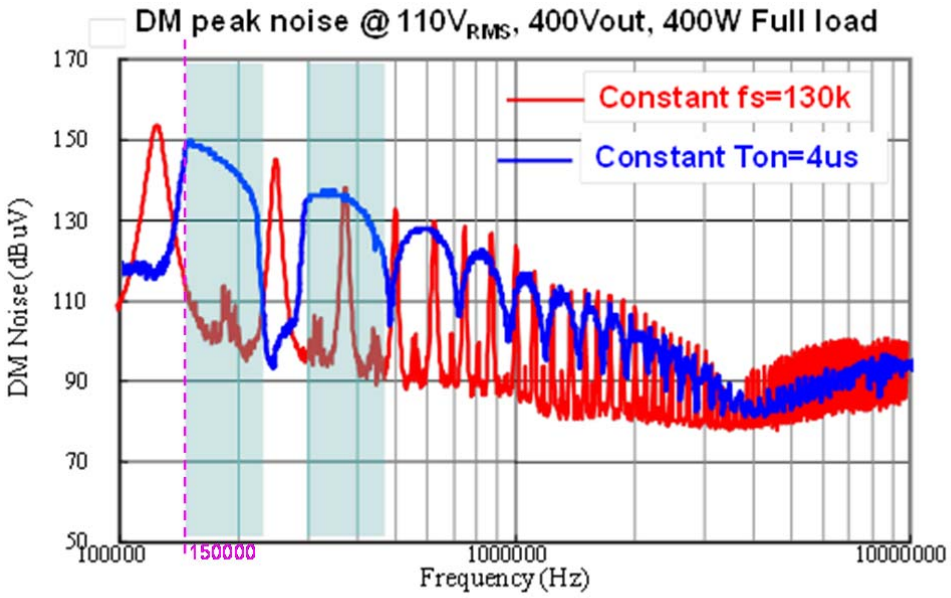


Figure 1-40 DM EMI noise measurement comparisons

1.4.2. Load dependent switching frequency

Another EMI challenge for constant on-time PFC and CRM Boost PFC is that their switching frequency are both load dependent, but in a different way. For constant on-time PFC, it can be illustrated from Fig. 1-15: as the converter moves into DCM mode, further decrease on load will increase the dead time and thus decrease the switching frequency. However, for the CRM Boost PFC, the switching frequency will increase as the load decreases as shown in Fig. 1-36. No matter how the switching frequency changes with the load, the load dependent switching frequency make it rather difficult to get the worst case scenario of the EMI performance, even for a fixed input line condition (in the US or Japan, etc.). As an example, Figure 1-41 and Figure 1-42 show the DM quasi-peak EMI noise measurements at conditions corresponding to the test set up at Figure 1-16 and Figure 1-17.

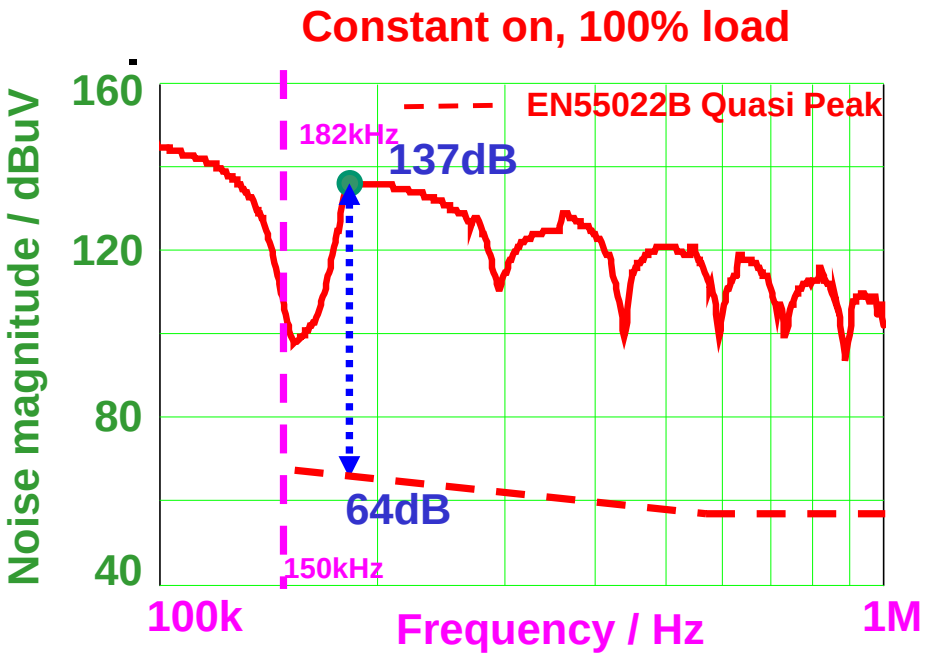


Figure 1-41 DM Quasi-peak EMI noise measurement for 120VAC, 400Vout, 400W Constant On-time PFC

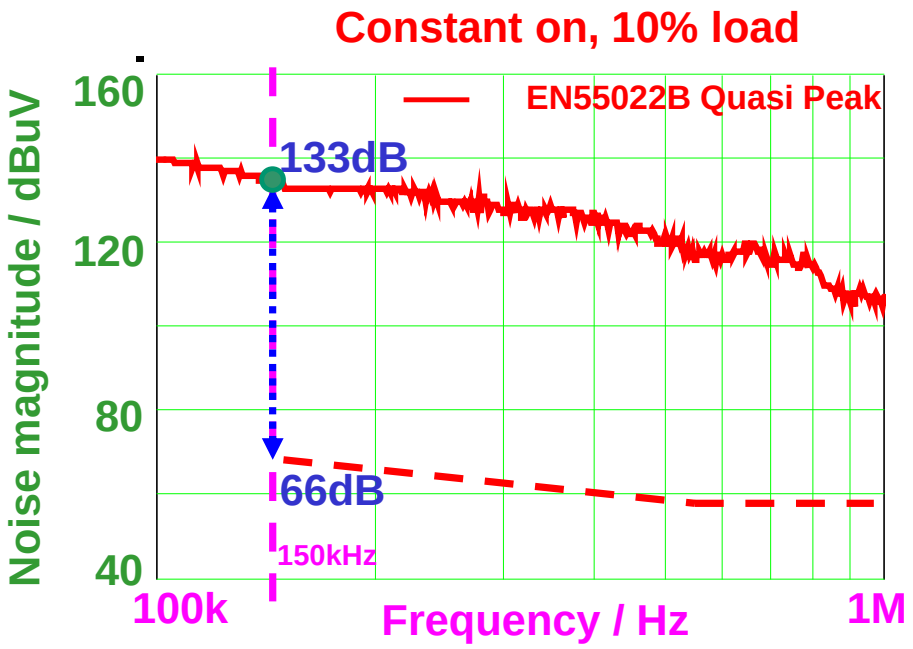


Figure 1-42 DM Quasi-peak EMI noise measurements for 120VAC, 400Vout, 40W Constant On-time PFC

As shown in Figure 1-41, at full load condition, the constant on-time PFC needs at least 73dB attenuation at 182 kHz to meet the EMC standard. This requires a two stage π-filter with the corner frequency of 34 kHz. For light load condition as shown in Figure 1-42, it needs at least 67dB attenuation at 150 kHz to meet the EMC standards. This requires a two stage π-filter with the corner frequency of 32 kHz. Although the absolute maximum noise magnitude above 150 kHz for the full load condition (137dBuV) is higher than that of light load condition (133dB), the noise spectrum at the light load condition actually requires a larger DM EMI filter (lower corner frequency) and thus is a worse case. This is contradictory to our experience in the constant frequency PFC converter. In the constant frequency PFC, the worst case of the DM EMI noise always happens at the full load conditions. In constant on-time PFC, it seems the same conclusion cannot apply and we don't have a clue yet when the worst case of DM EMI noise will happen.

Similar surprise exists in CRM Boost PFC, but in a different way. To analyze and compare the EMI performance at different load conditions without suffering in numerous and time-consuming EMI measurements, an analytical model to quantify the DM EMI noise needs to be developed.

1.4.3. Inductor dependent switching frequency

For CRM Boost PFC, there is one specialty that differentiate it from constant frequency PFC and constant on time PFC. And that is its switching frequency is always related to the inductance of the boost inductor, one of the main passive components in the boost PFC converter design.

With a brief derivation and simplification based on the control scheme introduced in Figure 1-30, the switching frequency of the CRM Boost PFC can be written as,

$$f_s(t) = \frac{V_{in}^2\left(V_o - \sqrt{2}V_{in}\sin(t)\right)}{2L_B P_o V_o} \tag{1-9}$$

As shown in equation (1-9), the switching frequency is inverse proportional to the inductance of boost inductor L_B. Therefore, the design of the boost inductor is not only related to the power converter efficiency anymore, but also related to the frequency distribution of the EMI noise spectrum. Such characteristics enforce the designer of the power converter to consider the influence of the inductance selection on the EMI performance at the very beginning stage of the power converter design and make the design process of the power stage more challenging. However, it also leaves an opportunity to optimize the total solution ahead of time and avoid the time wasting on the iterative design of the EMI filter.

Since the CRM Boost PFC is already widely used in industry for many years, the focus of the EMI analysis for CRM PFC will be on how to make an optimized EMI filter design, which is rather important for the purpose of the high power density design with the trend of high frequency soft switching PFC converter using the GaN devices. Therefore, to avoid either the over-design or the under-design, the worst case of the DM EMI noise spectrum should be investigated and abstracted, which was seldom targeted in the previous research [38][39]. The author hopes to make some development and contributions on this area. A novel mathematical analysis method is thus proposed in this dissertation to overcome the challenge.

1.5. Traditional Conducted EMI filter design

The traditional way to design the EMI filter is first to test the conducted EMI noise of the converter without the EMI filter. Then compared with the standard, the attenuation required at certain frequency is obtained. Then the EMI filter structure and specific filter components are selected such that required attenuation could be achieved. At last, the conducted EMI noise of the converter with the EMI filter is tested to make sure it is below the standard with enough margins.

The first disadvantage of the EMI noise measurement based EMI filter design is that it is complex and high cost. As we have already investigated and shown in Figure 1-43, the LISNs, the noise separator and the spectrum analyzer are the basic equipment necessary for the EMI noise measurement, which means a lot of initial investment and more future maintenance expense that cannot be afforded by small companies or start-up companies, let alone to mention the EMI chamber with low background noise.

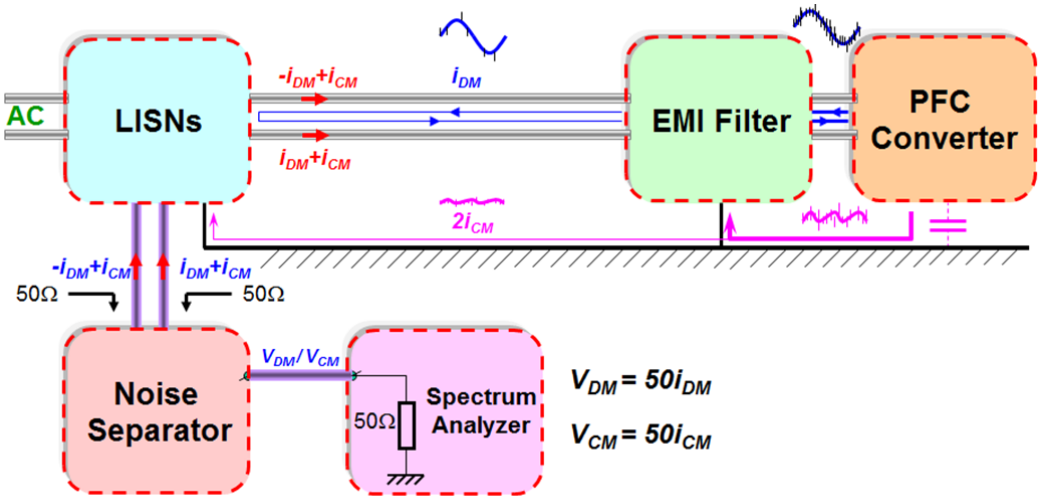


Figure 1-43 Basic blocks for EMI noise measurement in an offline application

The second disadvantage of the traditional method is the long design time. The most part of the design procedure is that a prototype converter need to be implemented, which often takes weeks to months, depending on the complexity of the converter itself. And what is worse, the prototype is usually and has to be designed without any information of the EMI filter. Thus after the EMI filter is designed and implemented, if the total size of the prototype converter and the EMI filter is out of specification, then either the prototype or the EMI filter need to be redesigned. With the prototype converter already implemented, it is often very difficult to further optimize the size and the weight of the EMI filter, and that means quite often the prototype converter itself needs to be redesigned, and several iterations might be necessary to get the correct balanced design or optimized design if possible. More time and cost could be expected. Thus EMI filter design without building the prototype converter would mean great time and cost savings. However, without the physical presence of the prototype converter, we cannot rely on the EMI noise measurement to design the EMI filter.

Simulation method is often used in order to achieve the above mentioned goal. However, power electronics simulation software such as the SABER, the Matlab and the Simplis could only deal with the EMI noise with fixed fundamental frequency and only the peak noise results are available. And EM analysis software such as the EMPro 3D from Agilent requires the complex 3D model of the converter and is mainly for the radiated noise and signal integrity. To develop a general method for constant frequency and variable frequency converters and for different EMI noise detections, the mathematical analysis for the conducted EMI noise prediction would be necessary.

Because the PFC converters are widely used in offline applications, there is a lot of research work being done in the region of EMI analysis for PFC converters [40][41][42][43]. However, all of these research papers are targeting on the EMI characteristics of the CCM boost PFC. The analytical method adopted in these papers generally is the time domain waveform simulation plus the fast Fourier transformation. However, for waveforms with variable switching frequency, fast Fourier transformation would not apply. And there is little research focusing on the EMI characteristics of the PFC converters with variable switching frequency.

In [44], ripple current of the CRM boost PFC is analyzed and DM EMI filters made for CRM boost PFC and CCM boost PFC are compared. However, harmonic current information of the ripple current is not enough to differentiate the EMI performance and thus cannot be directly used to design the DM EMI filter. Meanwhile, the DM EMI filter designed for the CRM boost PFC in this paper is based on one DM EMI noise measurement result at full load conditions, which is not sure yet to be the worst case.

In [45], the EMI performance of a DCM boost PFC with variable switching frequency control is evaluated based on circuit simulation and measurements. This paper focuses on the high frequency EMI noise reduction by proper packaging and PCB layout. More characteristics and EMI filter design criteria for PFC with variable switching frequency still need to be identified.

EMI noise measurements, which are usually used in EMI noise analysis for CCM boost PFC, are definitely the most accurate and reliable tools to investigate the EMI

performance. However, for CRM boost PFC, which is rather unclear in EMI characteristics, it would be quite a time-consuming process to do the investigation based on measurements.

In [46][47][48], different cancellation techniques are introduced to reduce the CM EMI noise. These techniques are based the CM current balance concept, which could be easily to apply to CRM boost PFC to attenuate the bare CM EMI noise. This will aggravate the concern for the DM EMI noise in CRM boost PFC, for which there is no easy way to cancel.

A possible way for ripple current cancellation is to use interleaving techniques. In [49], a novel interleaving technique is used to improve the EMI performance for the constant frequency CCM boost PFC. The impact of the interleaving techniques on the EMI performance for the CRM boost PFC still needs to be clarified.

1.6. Dissertation organization

The objective of this dissertation is to characterize the DM EMI noise of the constant on-time PFC and the CRM boost PFC converter and optimize the design procedure of the EMI filter for the front-end converter.

In Chapter 2, based on the investigation of the function of the EMI spectrum analyzer, different noise detection modes is introduced. Analysis of the DM EMI noise with peak detection for the constant on-time PFC is discussed. A couple of important approximations to simplify the prediction process are proposed. Experiments are carried out to verify the validation of those approximations, which would benefit the later work.

In Chapter 3, the quasi-peak detection, which is specifically required in most EMI regulation standards, is investigated for proper design of the EMI filter and a simplified detection block diagram is obtained. A complete approximate model is derived to predict the quasi-peak DM EMI noise for the CRM boost PFC. Experiments are carried out to verify the validity of the prediction. Based on the DM EMI noise prediction obtained from the approximate mathematical model for CRM boost PFC, worst case analysis is carried out and the worst DM EMI noise case for all the input line and load conditions can be found. With the same concept, the EMI noise characteristics of the interleaved CRM boost PFC are analyzed and the impact of interleaving techniques on its EMI performance is clarified.

In Chapter 4, based on the worst case analysis developed in Chapter 3, criteria to ease the DM EMI filter design procedure of the CRM boost PFC are given for different

boost inductor selection. Optimized design procedure of the EMI filter for the front-end converter is discussed. Experiments are carried out to verify the validity of the design procedure.

Chapter 5 is the summary. Limitation of the prediction model is explained and plan for future work is proposed.

Chapter 2. DM EMI NOISE ANALYSIS FOR CONSTANT ON-TIME PFC

2.1. EMI Detectors in the Spectrum Analyzer

The conducted EMI noise measurement setup specified in CISPR 22 for information technology equipment is shown in Figure 2-1 [50]. After the DM EMI noise and the CM EMI noise are separated by the noise separator, now we can start measuring the original DM or CM EMI noise using the spectrum analyzer. This dissertation is not the handbook for the spectrum analyzer and in no sense it will cover all the details of the spectrum analyzer. However, the concept of the EMI detectors in the spectrum analyzer is a very important one for the EMI noise measurement and will be introduced here.

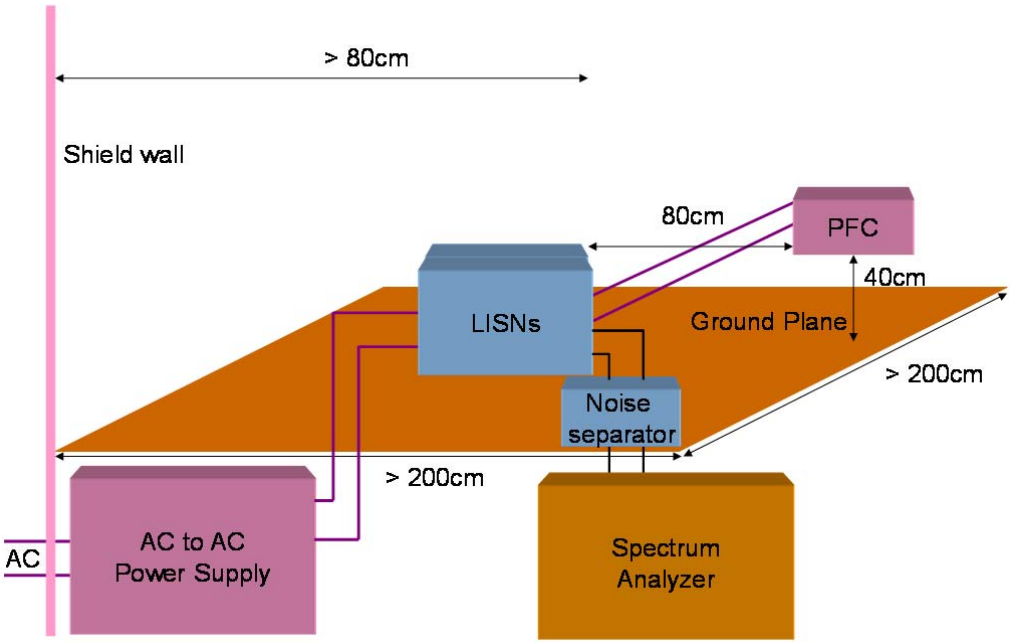


Figure 2-1 CISPR22 specified conducted EMI noise measurement setup

EMI detectors are used to detect certain characteristics of the applied input noise signal in EMI noise measurement. In concept, the detector can be either an electronic circuit or a program algorithm, dependent on whether it is an analog spectrum analyzer or a digital spectrum analyzer. There are three different types of EMI detectors, namely, the peak detector, the quasi-peak detector and the average detector. By definition, a peak detector is the detector with the output voltage of which is the peak value of an applied input noise signal. A quasi-peak detector is the detector with the output voltage of which is a fraction of the peak value and the fraction determined by the repeating frequency of the envelope of the applied input noise signal, a weighing factor that was first developed in AM radio and believed to better indicate the subjective annoyance level experienced by a listener hearing impulsive interference. And an average detector is the detector with the output voltage of which is the average value of the envelope of the applied input noise signal. Each EMI detector is not arbitrarily designed but need to follow the specification of the corresponding EMC standard. The EMI noise measured with different EMI detectors thus can be categorized as the peak noise, the quasi-peak noise and the average noise, respectively. Figure 2-2 shows the potential circuit realization of each detector and the sketch diagram for the measured noise value [51].

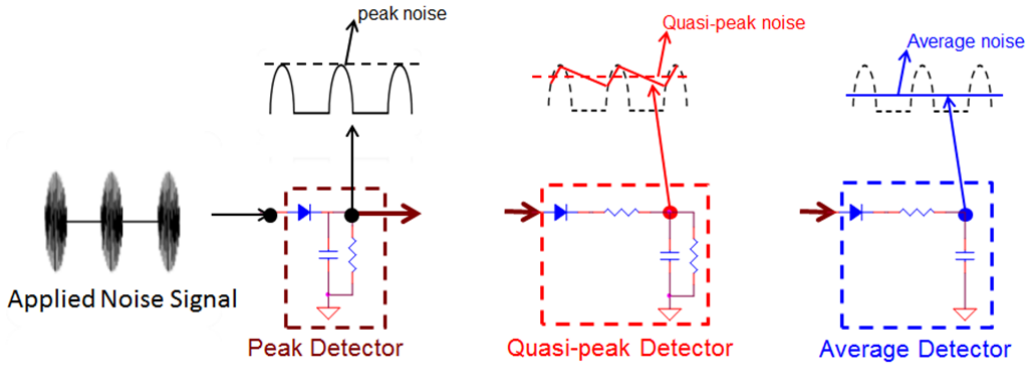


Figure 2-2 Circuit realization for EMI detectors and sketch diagram for noise value

It is noticeable that the noise values measured with different EMI detectors are different (generally peak noise >= quasi-peak noise >= average noise), and also the maximum limit for each type of measured noise is different. In EMC standards such as CISPR 22 and CISPR 25, they are indeed discriminated. Figure 2-3 shows that the peak and quasi-peak noise share the same limit while the average noise has a limit 10dB lower in CISPR 22. In CISPR 25, all of the three types of measured noise have its own limit different with each other. These subdivisions in the EMC standard sometimes play an important role in how to design the power converter and its EMI filters.

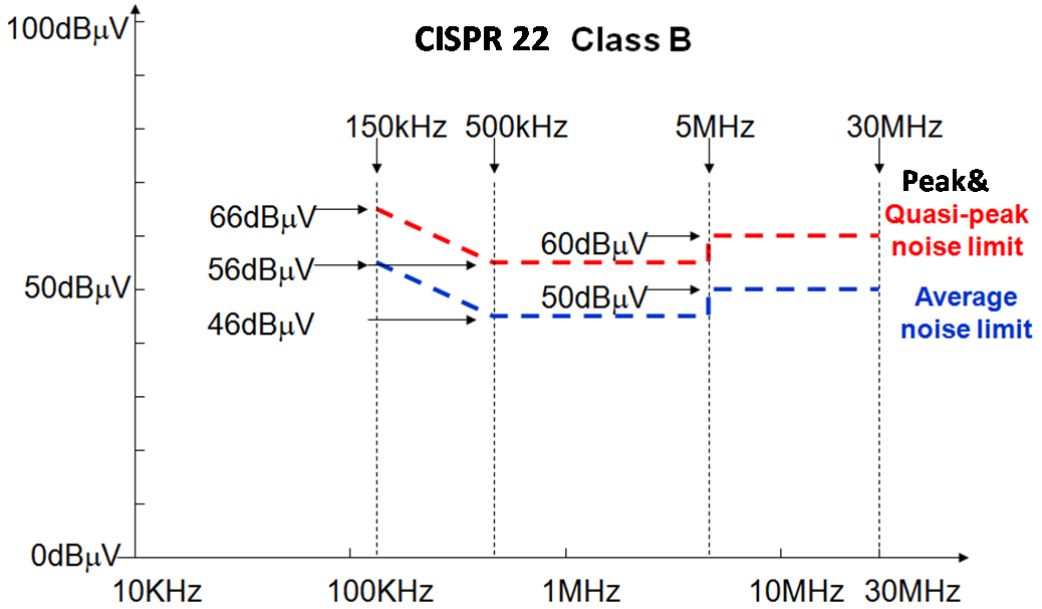


Figure 2-3 CISPR22 EMC standards for noise measured with different detectors

Based on Figure 2-3, it is clear that if peak noise is below the limit, the quasi-peak noise will definitely meet the standard. However, since the limit of the average noise is 10dB lower, it doesn't hold true even if the average noise is always lower than peak noise. And because the magnitude of quasi-peak noise and the average noise both have theoretical relationship with peak noise, as the initial step, peak noise is the straight-forward evaluation of the annoyance level of the noise and will be taken care in the next section.

2.2. DM EMI Peak Noise Analysis for Constant On-time PFC in CCM

2.2.1. Quasi Steady State Approximation

The circuit diagram for the DM EMI noise measurement is shown in Figure 2-4, which is a redrawn diagram from Figure 1-38 using the noise separator and without considering the CM EMI noise propagation path. And accordingly, the simplified DM EMI noise equivalent circuit is drawn as in Figure 2-5.

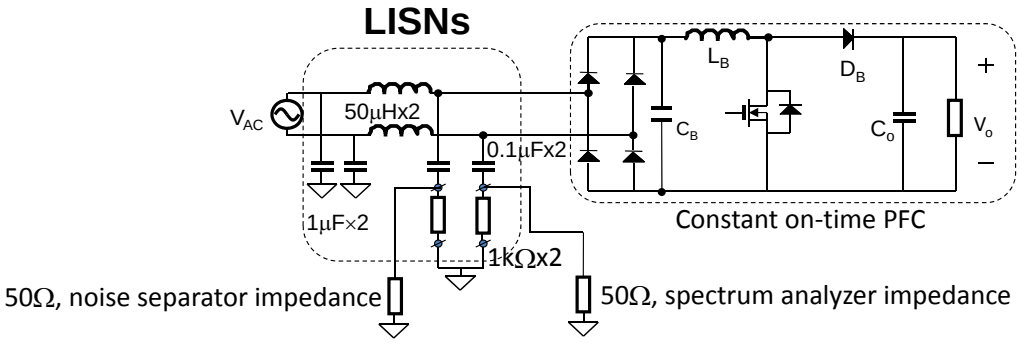


Figure 2-4 DM EMI noise measurement setup for constant on-time PFC

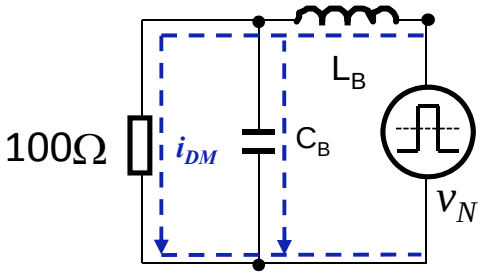


Figure 2-5 Simplified DM EMI noise equivalent circuit for constant on-time PFC

For constant frequency PFC noise analysis, the high voltage square waveforms at the switching node are usually considered as the dominant noise source for both CM and DM EMI noise. However, unlike the CM EMI noise, for the DM EMI noise, the input AC line voltage also acts on the boost inductor and hasdirect impact on the DM EMI network. A better demonstration will be using the inductor current as the noise

source and the modified equivalent circuit is shown in Figure 2-6, where i_N is the inductor ripple current.

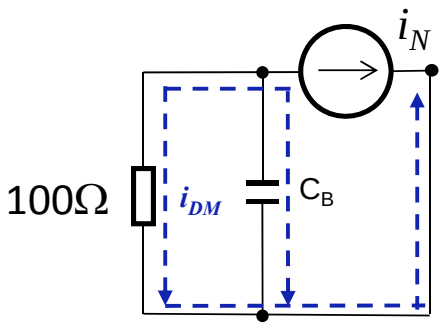


Figure 2-6 DM EMI noise equivalent circuit with current noise source

The advantage of the equivalent circuit in Figure 2-6 is that it avoids the process of discussing the design details of the boost inductor. As long as the inductor current information is available, then the DM EMI noise can be analyzed. Figure 2-7 shows the inductor current sketch in CCM and CRM.

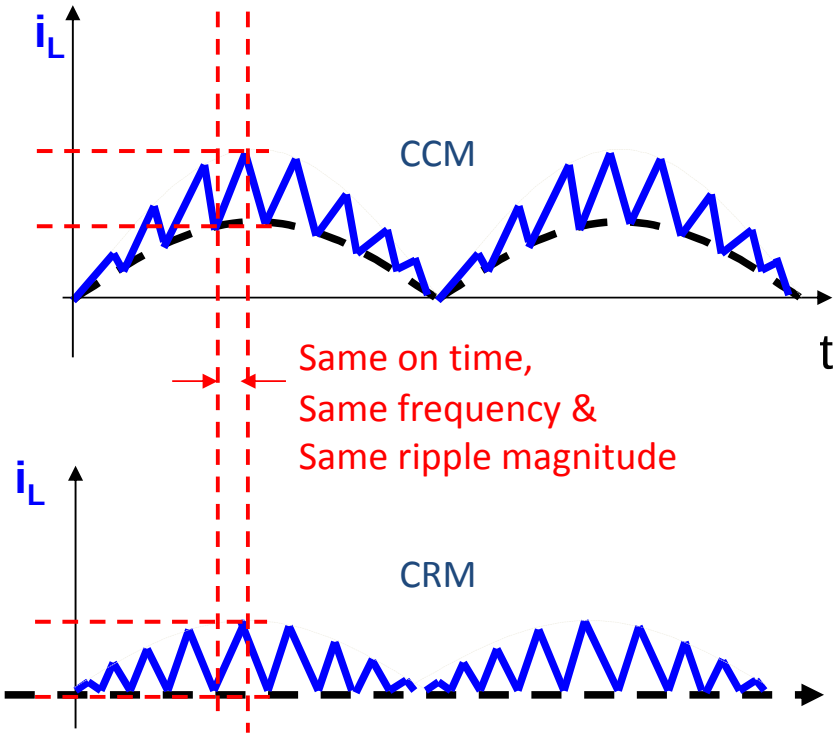


Figure 2-7 Inductor current sketch waveforms in CCM and CRM

As shown in Figure 2-7, as long as the constant on-time PFC converter is operating in CCM&CRM, at any time in the half-line cycle, the ripple current should have the same frequency and the same magnitude, according to equation (2-1).

$$i_{ripple}(t) = \frac{V_{in\_rec}(t)}{L} T_{on} \tag{2-1}$$

Therefore, the inductor ripple current is theoretically identical and according to the equivalent circuit in Figure 2-6, we should be able to make the assumption that the DM EMI noise be the same for different load conditions at given input line voltage and on time selection. Figure 2-8 show the measurement results of the DM peak EMI noise at different load conditions and they are almost identical.

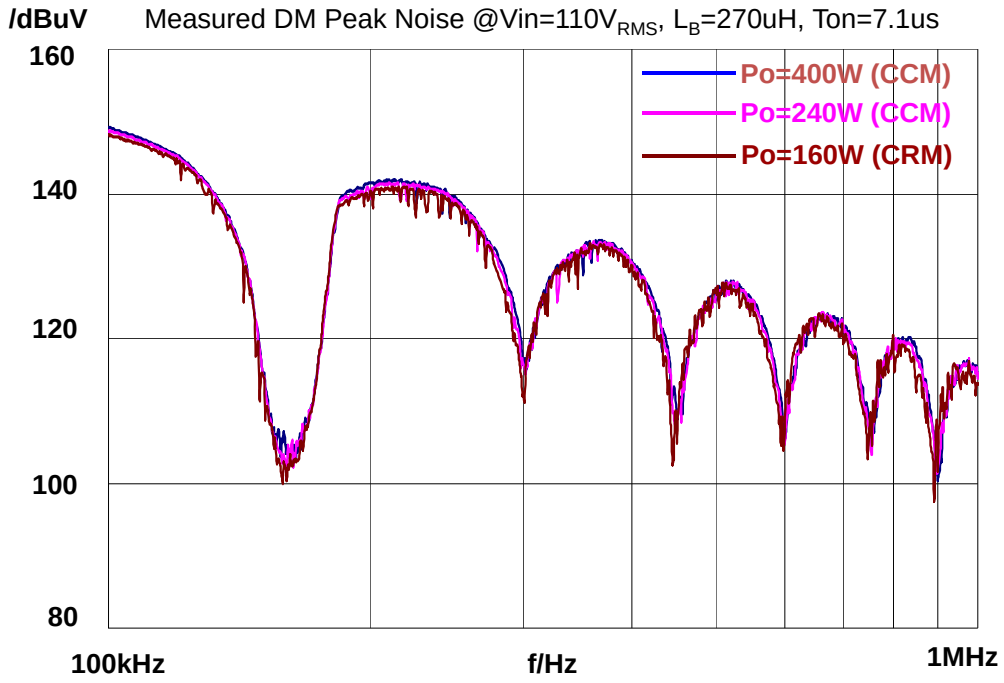


Figure 2-8 DM EMI noise comparisons at different load conditions

Figure 2-8 prove the validity of using the inductor ripple current as the current noise source. Since the noise source is properly identified, the next step would be how to properly analyze the inductor ripple current with different frequency over the

half-line cycle.

In Section 2.1 we have introduced the peak detector in the spectrum analyzer which is used to measure the peak EMI noise. Functionally, the spectrum analyzer is to process the input noise signal and try to capture and hold the maximum value of the harmonic component for given frequency. It doesn't necessarily capture the maximum value at one time but continually update the value while time moves on. Therefore, the spectrum analyzer not only knows the frequency domain information in the input noise signal but also knows its time domain information. In contrast, Fourier analysis theoretically requires the signal with unlimited time to be applied to and thus has the complete frequency domain information but no time domain information. Mathematically, the behavior of the peak noise measurement can be well described by the short time Fourier analysis, which is the time-frequency joint analysis and rather complicated [52]. Therefore, in this dissertation, combining the characteristics of the switching mode power supply, the Quasi Steady State approximation is proposed to analyze the input noise signal, the inductor ripple current, with variable frequency.

Figure 2-9 demonstrate the analysis procedure with the quasi steady state approximation. In order to quantify the noise component at fs, pick the triangular inductor ripple current with the switching period Ts (= 1/fs). Because the switching frequency is generally much higher than the line frequency, in a short time interval of the half-line cycle, there are many triangular inductor ripple current with similar switching period and similar magnitude. Approximately, they can be taken as the periodical signal and have the Fourier analysis applied. As the window of the short time interval moves forward in the half-line cycle, the noise at different frequency could be abstracted.

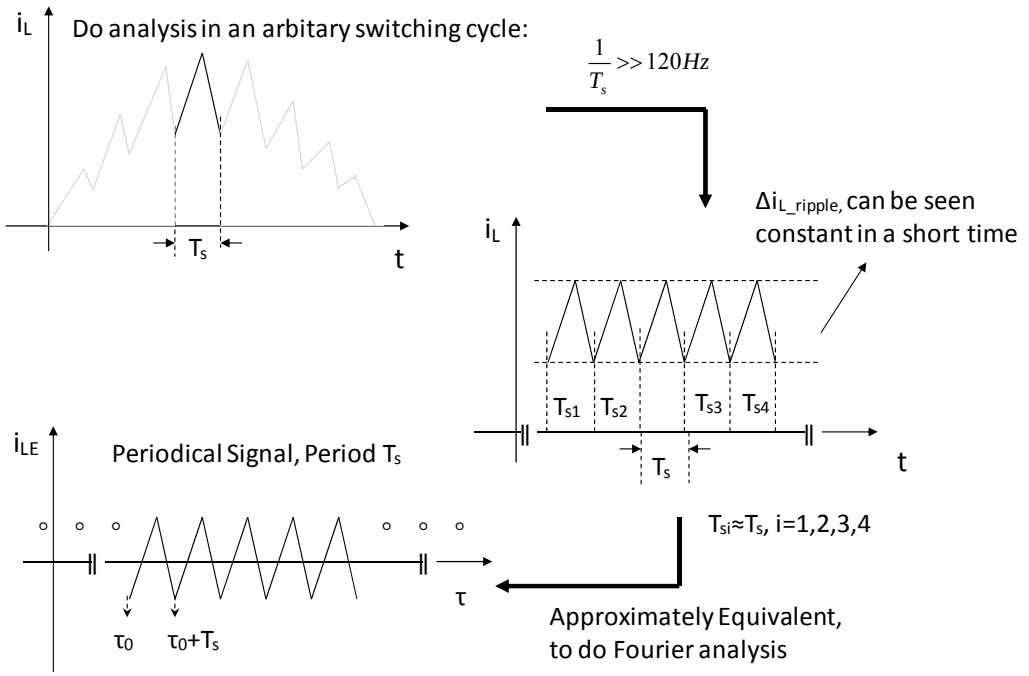


Figure 2-9 Quasi Steady State approximation

2.2.2. Peak EMI noise prediction for constant on-time PFC in CCM

In constant on time PFC, the switching frequency is variable over a half line cycle. When the circuit operates in CCM,

$$f_s(t) = \frac{1}{T_s(t)} = \frac{1 - V_{in}(t)/V_o}{T_{on}} = \frac{1 - \sqrt{2}V_{rms}\sin(\omega t)/V_o}{T_{on}} \tag{2-2}$$

Where, V_{rms} is rms value of the rectified input voltage.

Thus the minimum and maximum switching frequencies are, respectively,

$$\min\ f_s = \frac{1 - \sqrt{2}V_{rms}/V_o}{T_{on}} \qquad \max\ f_s = \frac{1}{T_{on}} \tag{2-3}$$

However, based on the Quasi-Steady-State assumption, within a very short time

interval, the PFC can be seen as a boost converter with constant input voltage. Thus the inductor current ripple can be considered as periodical triangular waveform during the short time interval. The inductor waveform sketch in CCM is drawn in Figure 2-10 and a zoomin in around t_0 is shown in Figure 2-11.

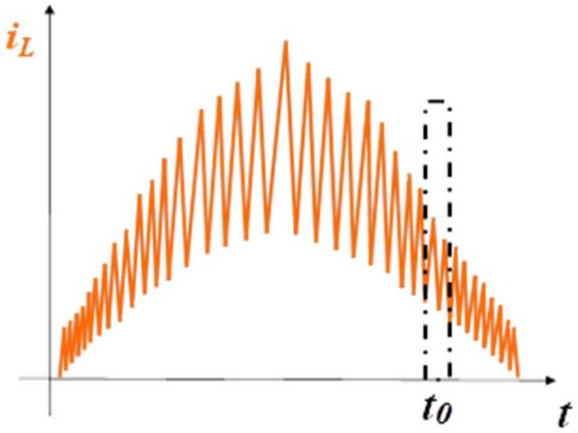


Figure 2-10 Inductor Current Sketches for Constant On-time PFC in CCM

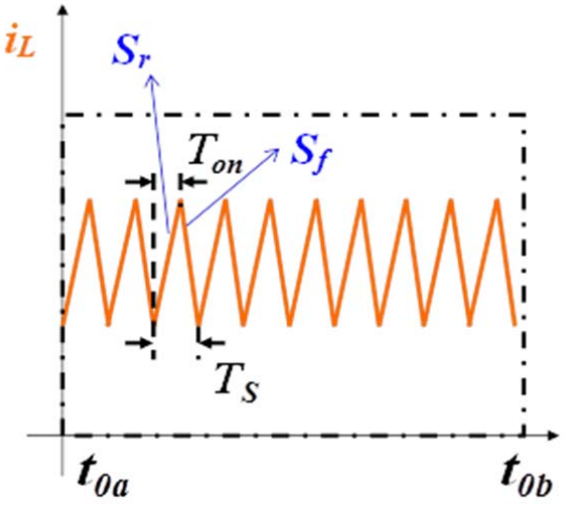


Figure 2-11 Zoom-in around t_0 in Figure 2-10

irp is defined as the ac ripple current.

In Figure 2-11, the rising slope of the ripple current is,

$$S_r = \frac{V_{in}(t)}{L_B} = \left(1 - \frac{T_{on}}{T_s(t)}\right)\frac{V_o}{L_B} \quad (2\text{-}4)$$

And the falling slope of the ripple current is,

$$S_f = \frac{V_o - V_{in}(t)}{L_B} = \frac{T_{on}}{T_s(t)}\frac{V_o}{L_B} \quad (2\text{-}5)$$

Then the ripple current in a switching cycle can be expressed as,

$$i_{rp}(\tau) = \begin{cases} S_r \cdot \tau - \frac{1}{2} S_r \cdot T_{on} = \frac{V_o}{L_B}\left(1 - \frac{T_{on}}{T_s(t)}\right)\tau - \frac{1}{2}\frac{V_o}{L_B}\left(1 - \frac{T_{on}}{T_s(t)}\right)T_{on} & 0 \le \tau < T_{on} \\ \frac{1}{2} S_r \cdot T_{on} - S_f \cdot (\tau - T_{on}) = \frac{V_o}{L_B}\frac{T_{on}}{T_s(t)}\tau + \frac{1}{2}\frac{V_o}{L_B}\left(1 + \frac{T_{on}}{T_s(t)}\right)T_{on} & T_{on} \le \tau < T_s(t) \end{cases} \quad (2\text{-}6)$$

Apply Fourier analysis to the ripple current and the harmonic current amplitude can be derived as,

$$|i_k(f_s(t))| = \frac{1}{k^2}\frac{V_o}{L_B}\frac{1}{2\pi^2 f_s(t)}\left|e^{-jk2\pi f_s(t)T_{on}} - 1\right| \quad (2\text{-}7)$$

Where, ***k*** is the order number of harmonic current and ***k***=1,2,3…

Equation (2-7) is the noise source expression for constant on-time PFC in CCM, which is an explicit equation of the $f_s(t)$.

With the equation of harmonic current amplitude, the DM EMI peak noise now can be calculated. Figure 2-12 shows the comparison between the measured DM peak noise and the predicted DM peak noise. As an example, for the constant on-time PFC with Ton = 7.1us and VIN = $110V_{RMS}$ in CCM, the switching frequency range is from 90 kHz to 140 kHz. In order to predict the noise at 200 kHz, the amplitude of the second harmonic current of the 100 kHz inductor ripple current needs to be calculated

as equation (2-8).

$$I_{ripple\_k=2}\left(2\pi\times 100\text{kHz}\right)=0.317\text{A} \tag{2-8}$$

Because the switching frequency range is from 90 kHz to 140 kHz, the 100 kHz inductor ripple current is the only noise source of which the second order harmonics can have contribution to the noise at 200kHz, thus the calculated value based onthe equation (2-8) will be the peak noise magnitude at 200 kHz. For another example, consider the peak noise at 400 kHz. Because both the third order harmonics of the 133.3 kHz inductor ripple current and the fourth order harmonics of the 100 kHz inductor ripple current can contribute to the noise at 400 kHz, two calculations need to be carried out, as equation (2-9) and (2-10).

$$I_{ripple\_k=3}\left(2\pi\times 133.3\text{kHz}\right)=0.06\text{A} \tag{2-9}$$

$$I_{ripple\_k=4}\left(2\pi\times 100\text{kHz}\right)=0.046\text{A} \tag{2-10}$$

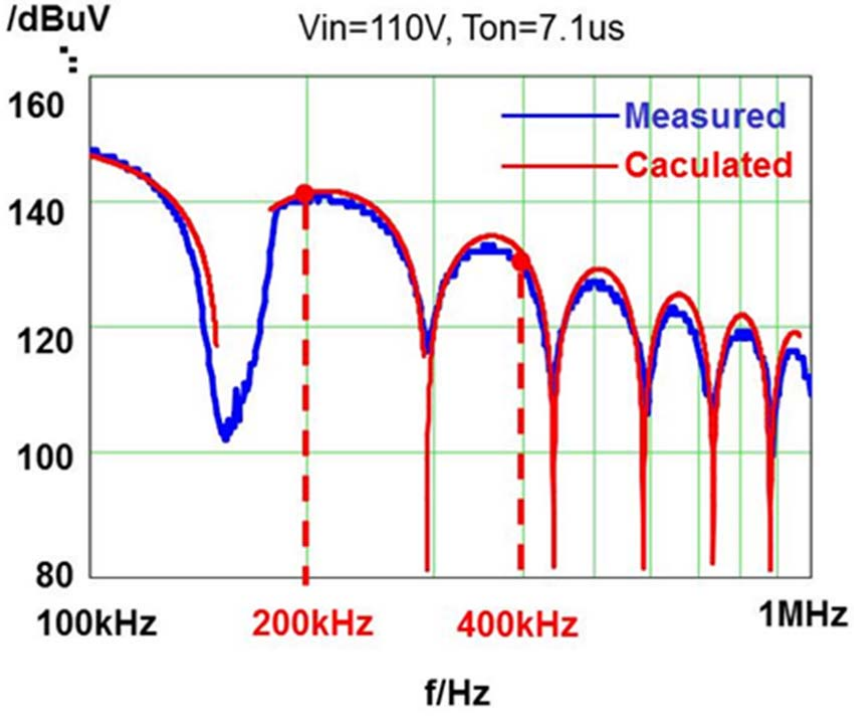


Figure 2-12 Peak noise prediction verification for constant on-time PFC in CCM

Because the 3rd harmonic current of the 133.3 kHz inductor ripple current is

larger than the 4th harmonic current of the 100 kHz inductor current ripple and they are happening at different time instant, the peak detector will hold the maximum value while it is processing the input harmonic current signal and thus the calculated value based on the equation (2-9) will be the peak noise magnitude at 400 kHz.

Going through the same procedure from 100 kHz to 1 MHz, the predicted noise spectrum is obtained. We can see that the predicted peak noise matches the measurement very well and thus will be helpful in DM EMI filter design. One obvious question will be, why not making the noise prediction for the whole noise spectrum from 150 kHz to 30 MHz. The answer is, for high frequency EMI noise more than 1 MHz, the parasitic parameter in the converter will gradually come in and play a more and more important role at frequency higher than 10 MHz. As shown in [53], the EPC of the boost inductor has dramatic influence on the high frequency DM EMI noise. To make the prediction on high frequency DM EMI noise, the equation (2-6) and (2-7) which is to describe the noise source, the inductor ripple current, are not accurate anymore, let alone that there are more other parasitic parameters. And abstracting those parasitic parameters from the converter is not a topic in this dissertation. Luckily, the predictednoise spectrum will still be useful to help design the EMI filter which will be able to handle the EMI noise up to 1MHz.

2.3. On time design based on the predicted EMI noise

One benefit of the EMI noise prediction on the constant on-time PFC is to help to pre-select the value of the on-time. As shown in Figure 1-14, the on-time is the solely crucial design parameter in the constant on-time PFC. Before, when the EMI noise could not be predicted, the efficiency is the only factor which could be considered to determine the selection of the on-time. Now we add another factor to make the on-time selection more reasonable and complete.

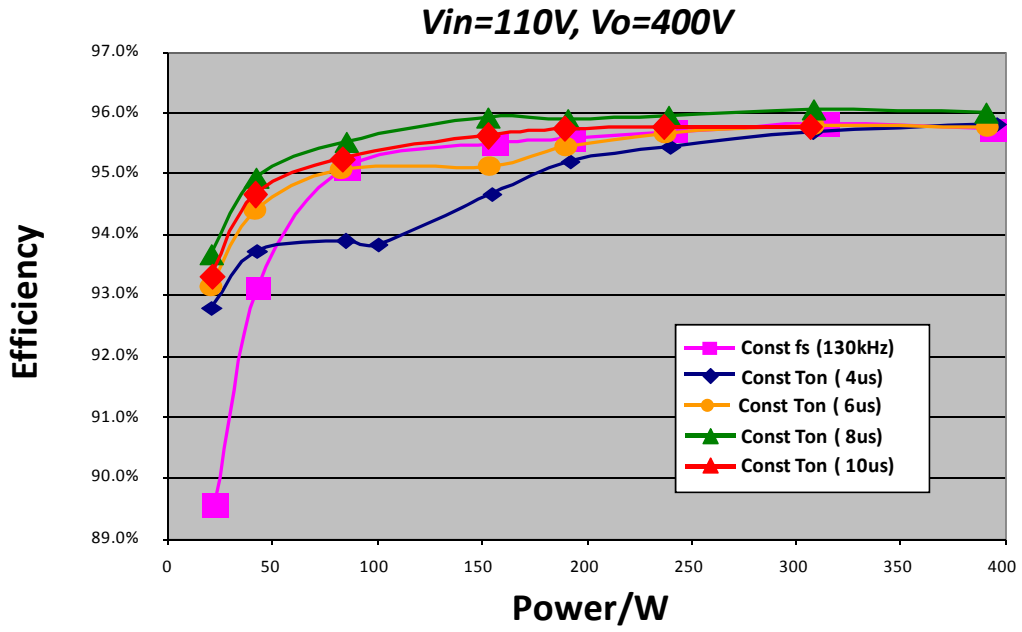


Figure 2-13 Efficiency vs. load in constant on-time PFC

Figure 2-13 shows the efficiency profile for different on-time selections in constant on-time PFC at low line, with the constant frequency case (pink curve) as the reference. From the profile we can see that, when on time is as small as 4us, the efficiency suffers at medium load due to relatively high switching frequency. Increasing the on-time from 4us to 6us, the efficiency improves from medium load to full load and is close to the constant frequency case. The on-time of 8us gives the best

results and beats the constant frequency case for the whole load range. However, further increasing the on-time from 8us to 10us will not improve but deteriorate the efficiency performance due to relatively large current ripple. Figure 2-13 shows us a strong image that 8us is the optimized on-time choice, solely for the purpose of the efficiency. While 8us is definitely a good candidate, it will be better if we can check other performance criteria, such as the related EMI filter size, or the EMI spectrum, using the peak EMI noise prediction.

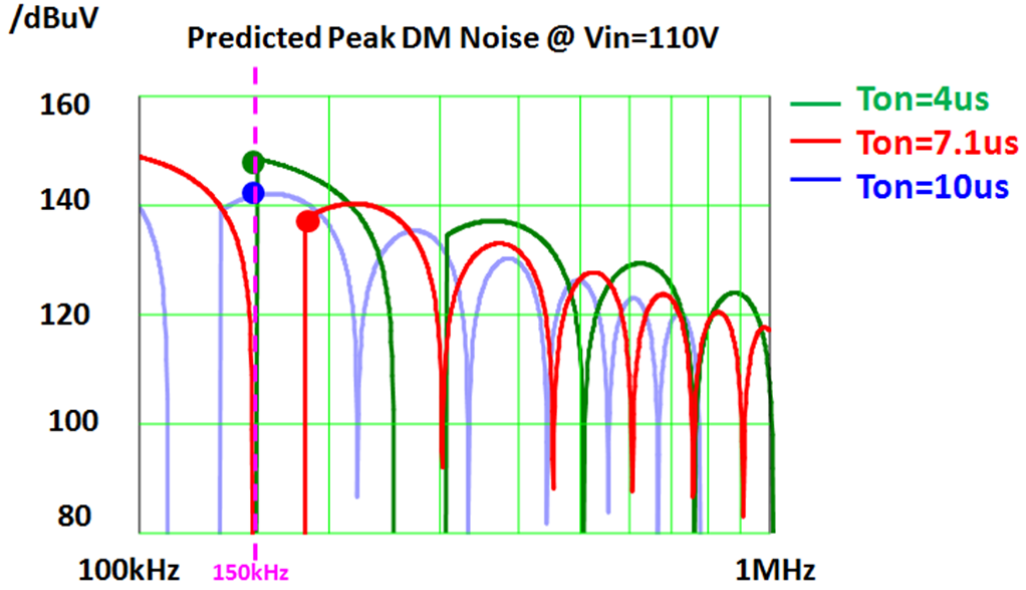


Figure 2-14 Noise spectrums vs. on-time in constant on-time PFC

Figure 2-14 shows the DM EMI noise spectrums for different on-time selections in constant on-time PFC at low line, CCM. From the figure we can see that, when the on-time is 4us, the minimum switching frequency is 150kHz and thus the first noise peak just falls on 150 kHz, the beginning frequency that the EMI standard starts to regulate the EMI noise. Increasing the on-time from 4us to 7.1us, the switching frequency decreases with the maximum switching frequency equal to 150 kHz and thus the fundamental harmonics components falls out of the EMI regulation. The EMI

filter now needs to be designed based on the second order harmonics components. Further increasing the on-time from 7.1us to 10us, the switching frequency will keep decreasing and the second order harmonics components will move left and 150kHz will fall within the second order harmonic components. As shown in Figure 2-14, the three dark solid points are the noise points which determine the size of the EMI filter for each on-time selection. It is clear that comparing Ton=4us with Ton=10us, the noise at Ton=4us requires more attenuation at the same frequency 150 kHz.Thus Ton=10us is a better choice than Ton=4us with regard to the EMI performance, although it has much larger inductor current ripple. However, for Ton=7.1us, it does have a lower noise magnitude at a higher frequency, but it will be dependent on the EMI standard to determine its relative advantage over Ton=10us.

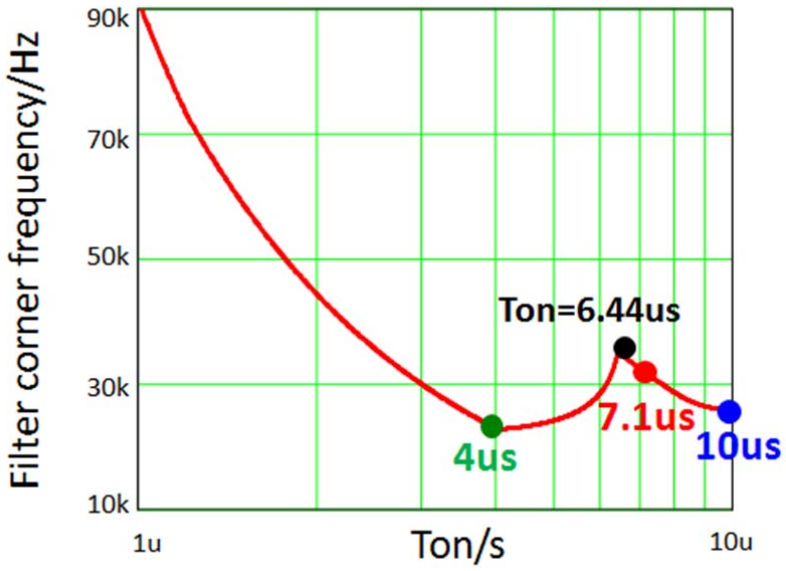


Figure 2-15 Filter corner frequency vs. on-time in constant on-time PFC

Figure 2-15 shows the filter corner frequency of the required EMI filter for different on-time selections in constant on-time PFC at low line, CCM. The filter corner frequency is generally used as a parameter to determine the size of the EMI

filter; the larger the filter corner frequency, the smaller the EMI filter size [54]. More detailed derivation on filter corner frequency will be presented in next chapter. As shown in Figure 2-15, when Ton is below 4us, the minimum switching frequency is higher than 150 kHz.Therefore decreasing Ton means moving the noise spectrum farther away from 150kHz and thus the corresponding filter corner frequency will become larger (the size of the required EMI filter will become smaller). From 4us to 6.44us, the impact of the fundamental harmonics components is fading out while the second order harmonics components have not yet come in to play a role, and thus increasing the Ton will help increase the filter corner frequency. From 6.44us to 10us, the second order harmonics components have already played a role. Continuing to increase Ton means moving the noise spectrum closer to 150 kHz and thus the corresponding filter corner frequency will become smaller.Since choosing Ton that is smaller than 4us means much higher switching frequency and switching loss, the reasonable optimized on-time should be within the range between 6.44us and 8us, combining the efficiency performance previously discussed and the EMI performance. Further optimization should be relying on the specific trade-off of the efficiency and the power density.

2.4. EMI noise spectrum for constant on-time PFC in DCM

The main advantage of the constant on-time PFC over the constant frequency PFC is that at light load the switching frequency of the constant on-time PFC will decrease automatically and thus it can save the switching loss. Figure 2-16 shows the switching frequency profile of the constant on-time PFC at different load conditions with Ton=6.44us. When the load decreases, the constant on-time PFC will finally operate in DCM and the ripple current is changed.The switching frequency in DCM is reduced but still high and variable as in CCM. Essentially, the Quasi Steady State Approximation should be still qualified to be applied to the noise prediction in DCM operation.

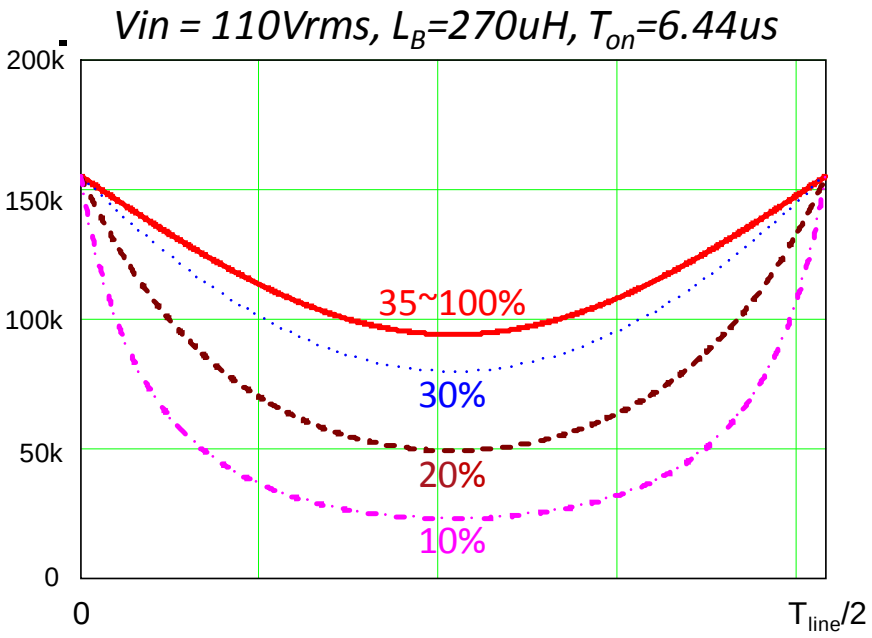


Figure 2-16 Switching freq. at different load conditions for constant on-time PFC

The inductor current waveform sketch in DCM is shown in Figure 2-17. Compared with that in CCM case, for the ac current ripple, the difference is the added-in dead time T_{dead}. Based on the power balance in a half line cycle, the dead

time can be approximately described as,

$$T_{dead}(t) \approx \frac{2\sqrt{2}}{\pi}\frac{V_o}{V_{rms}}\frac{V_{in}(t)}{V_o - V_{in}(t)}\left(\frac{{V_{rms}}^2 T_{on}}{2L_B P_o} - 1\right)T_{on} \tag{2-11}$$

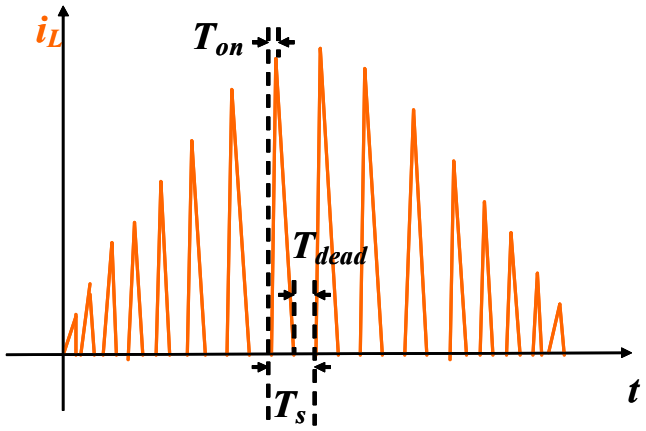


Figure 2-17 Inductor Current Sketch for Constant On-time PFC in DCM

Then the ripple current in a switching cycle can be expressed as,

$$i_{rp}(\tau) = \begin{cases} \dfrac{V_o}{L_B}\left(1 - \dfrac{T_{on}}{T_s(t)}\right)\tau - \dfrac{1}{2}\dfrac{V_o}{L_B}\left(1 - \dfrac{T_{on}}{T_s(t)}\right)T_{on} & 0 \le \tau < T_{on} \\ -\dfrac{V_o}{L_B}\dfrac{T_{on}}{T_s(t)}\tau + \dfrac{1}{2}\dfrac{V_o}{L_B}\left(1 + \dfrac{T_{on}}{T_s(t)}\right)T_{on} & T_{on} \le \tau < T_s(t) - T_{dead}(t) \\ -\dfrac{1}{2}\dfrac{V_o}{L_B}\left(1 - \dfrac{T_{on}}{T_s(t)}\right)T_{on} & T_s(t) - T_{dead}(t) \le \tau < T_s(t) \end{cases} \tag{2-12}$$

Apply Fourier analysis to the ripple current equation (2-12) and the harmonic current amplitude can be derived as,

$$|i_k(f_s(t))| = \frac{1}{k^2}\frac{V_o}{L_B}\frac{1}{2\pi^2 f_s(t)}\left|e^{-jk2\pi f_s(t)T_{on}} - 1 - \frac{T_{on}}{T_s(t) - T_{dead}(t)}\left(e^{-jk2\pi f_s(t)(T_s(t) - T_{dead}(t))} - 1\right)\right| \tag{2-13}$$

Where, k is the order number of harmonic current and k=1,2,3… and $T_s(t)$-$T_{dead}(t)$ can be expressed as a function of $f_s(t)$as,

$$T_s(t) - T_{dead}(t) = \frac{\frac{1}{f_s(t)} - M \cdot T_{on}}{M+1} \tag{2-14}$$

Where, ***M*** is a constant and,

$$M = \frac{2\sqrt{2}}{\pi} \frac{V_o}{V_{rms}} \left(\frac{{V_{rms}}^2 T_{on}}{2 L_B P_o} - 1 \right) \tag{2-15}$$

Equation (2-13) is the noise source expression for constant on-time PFC in DCM. Since $T_s(t)$-$T_{dead}(t)$ can be expressed as a single variable function of $f_s(t)$ as shown in Equation (2-14), Equation (2-13) is an explicit equation of the $f_s(t)$.

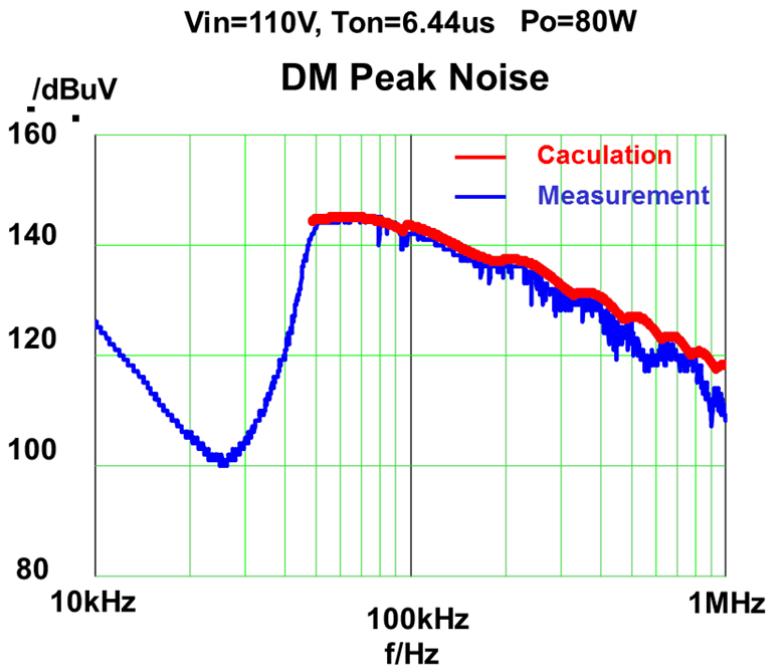


Figure 2-18 Peak noise prediction verification for constant on-time PFC in DCM

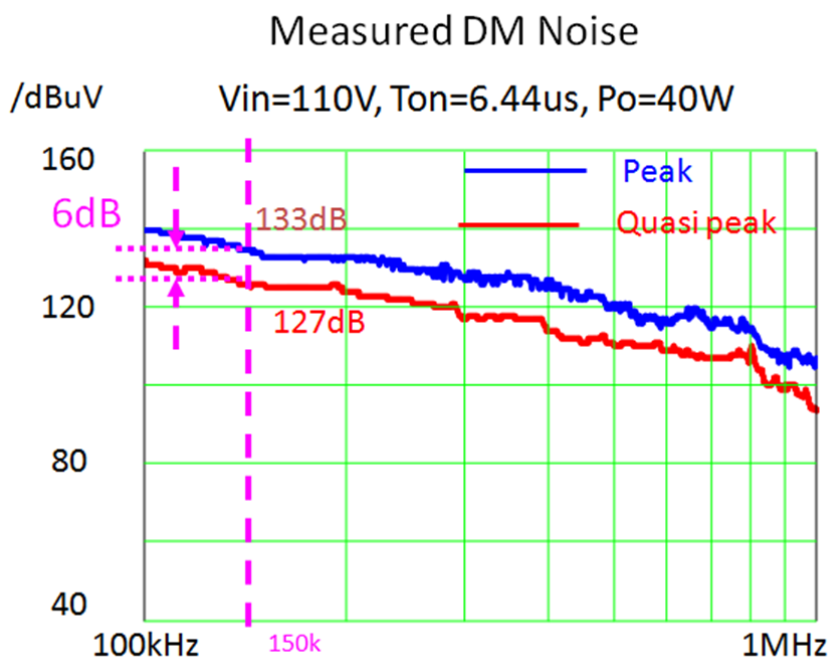


Figure 2-19 Peak and quasi-peak noise comparison for constant on-time PFC in DCM

With the input source modeled, the peak DM EMI noise for constant on-time PFC in DCM can be just predicted in the same way we did in CCM. Figure 2-18 shows the prediction verification using peak noise measurement. With Ton=6.44us and at 20% load, the minimum switching frequency is around 50 kHz as shown in Figure 2-16. We can see that the prediction matches the measurement very well even for DCM operation and further prove the validity of the mathematical model.

This chapter mainly discusses about the peak EMI noise prediction and the important assumption for its feasibility, the Quasi Steady State Assumption. However, as we introduced in the section 2.1, there are two other noise detection mode, the quasi-peak noise detection and the average noise detection. Since the magnitude of the measured peak noise is always higher than the quasi-peak and average noise for the same input noise source, it is the routine to check first whether the peak noise

meets the EMC standards or not. If the answer is yes, then it is not necessary to check either the quasi-peak noise or the average noise [55]. That is why peak EMI noise is so well-known and widely used in industry and why I put it as my first target in noise prediction. However, as shown in Figure 2-19, in many conditions, quasi-peak noise could be much lower than the peak noise, which means EMI filter designed based on the peak EMI noise will be an overdesign and power density of the whole front-end converter will suffer. Therefore it is also interesting to investigate the quasi-peak and the average EMI noise and their influence on the EMI filter design and some of the related research work will be presented in the following chapters.

Chapter 3. DM EMI NOISE ANALYSIS FOR CRITICAL CONDUCTION MODE BOOST PFC

3.1. DM EMI Noise Analysis for CRM Boost PFC

3.1.1. Principle of the Quasi-peak EMI Noise Measurement Procedure

There are two types of EMI noise limits as shown in Figure 2-3. Does that mean we should find the worst case for both quasi-peak DM EMI noise and average DM EMI noise for CRM boost PFC in order to optimize its EMI filter design?

Figure 3-1 and Figure 3-2 are the quasi-peak DM EMI noise and average DM EMI noise measurements, respectively, for a 150Watts CRM boost PFC at input line V_{RMS}=110V with 150uH boost inductor.The measured quasi-peak noise need 49dB attenuation at 150 kHz to meet the quasi-peak noise limit and the average noise need 40dB attenuation at 150 kHz to meet the average noise limit. By comparison, the quasi-peak noise needs 9dB more attenuation at 150 kHz than average noise, which means the quasi-peak DM EMI noise will determine the corner frequency of the DM EMI filter and the filter should be designed based the quasi-peak DM EMI noise.

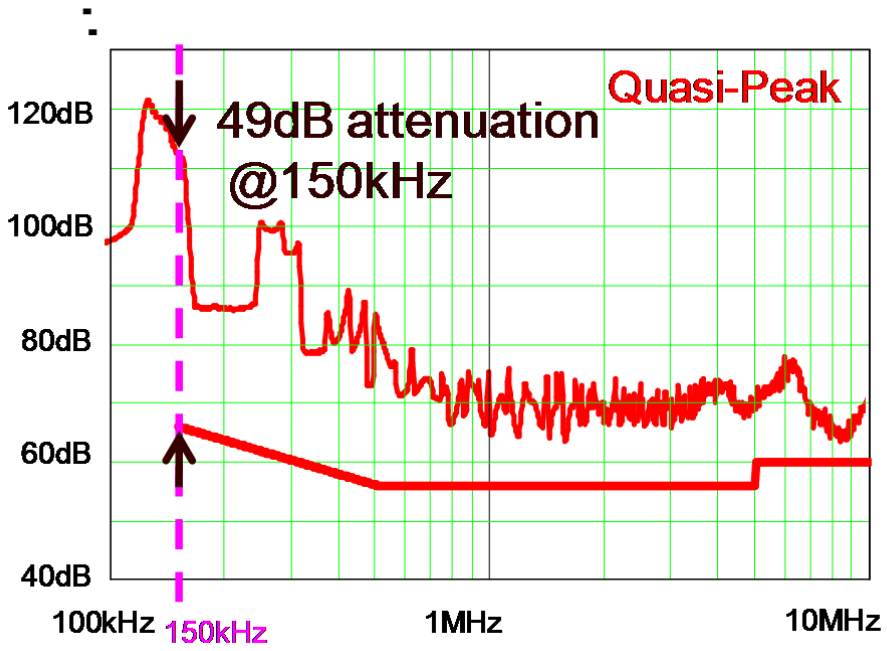


Figure 3-1 Quasi-peak DM EMI Noise Measurement Result for a 150W CRM PFC

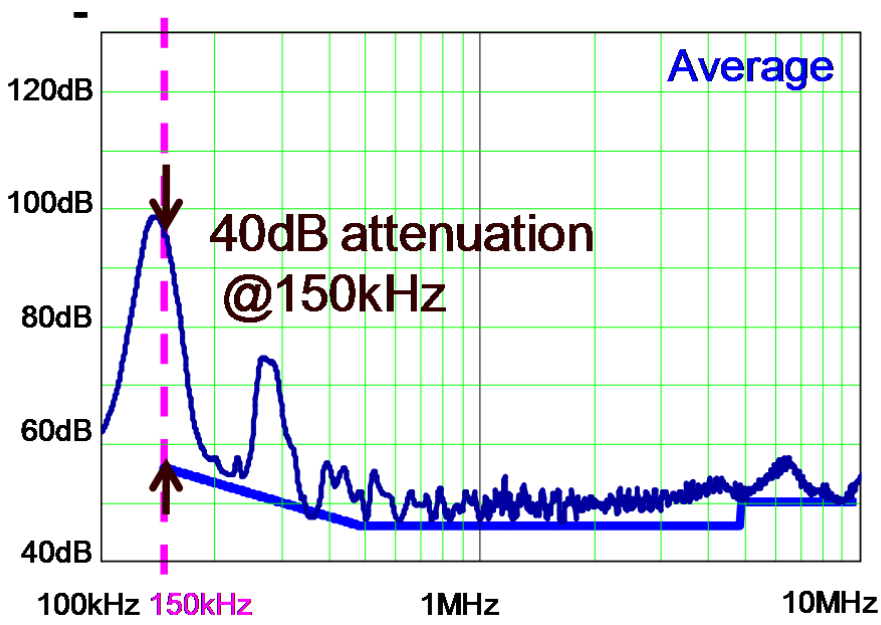


Figure 3-2 Average DM EMI Noise Measurement Result for a 150W CRM PFC

The average noise in CRM boost PFC is at quite low magnitude. For variable switching frequency converter such as the CRM boost PFC, the noise energy is distributed in a wide frequency range, so that for certain frequency, the average noise

is quite small. The same phenomena also appear in the frequency-modulated CCM boost PFC and the reasons are discussed in [56] and [57].

Since for boost PFC with variable switching frequency, the quasi-peak noise is dominant, the rest part of this Chapter will focus on the quasi-peak DM EMI noise.To carry out the quasi-peak noise prediction for CRM boost PFC, the function of the spectrum analyzer when measuring the quasi-peak noise need to be further understood. Based on the investigation of the Agilent E7400A spectrum analyzer, a simplified diagram is shown in Figure 3-3 to illustrate the main procedure of measuring quasi-peak noise.

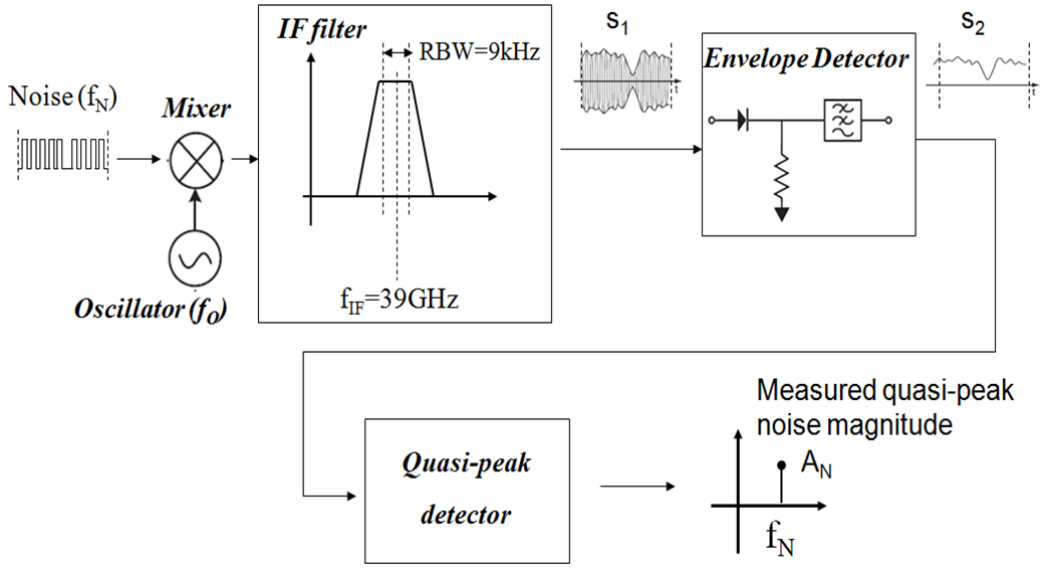


Figure 3-3 Simplified Quasi-peak Noise Measurement Procedure

Mixed with the oscillator signal of the tunable frequency fo, the noise component with frequency f_N will be translated to frequency fo-f_N and fo+f_N in frequency domain. If set fo = f_N+ f_{IF}, then the noise signal with frequency fo-f_N will pass the intermediate frequency (IF) filter with 9kHz bandwidth.

Combined with the function of the oscillator and the mixer, the IF filter equivalently can be seen as a band-pass filter with the tunable center frequency.There is another important link after the IF filter, the envelope detector. To avoid the interference of the oscillator on the noise, the oscillator frequency is much higher, around 39GHz, than the noise frequency. Before the quasi-peak detector to process the quasi-peak noise, the envelope detector is used to filter out the high frequency oscillator information. Then the diagram can be further simplified as in Figure 3-4, with the quasi-peak detector modeled in [58].

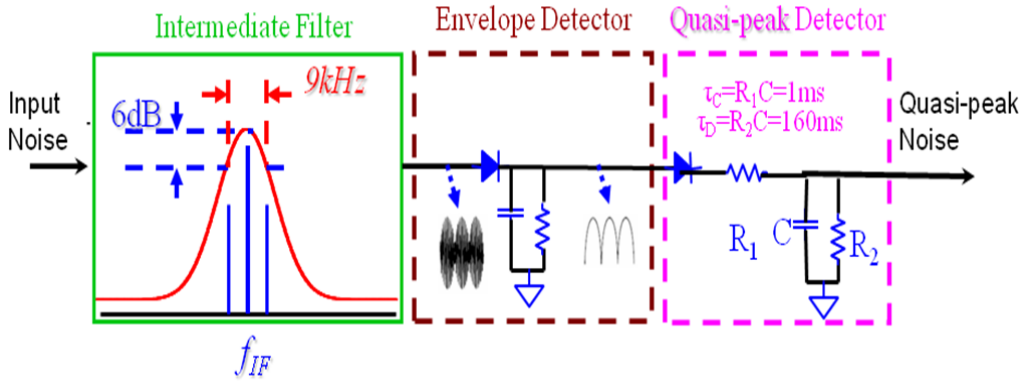


Figure 3-4 Simplified Block Diagram for EMI Spectrum Analyzer in Quasi-Peak Detection Mode

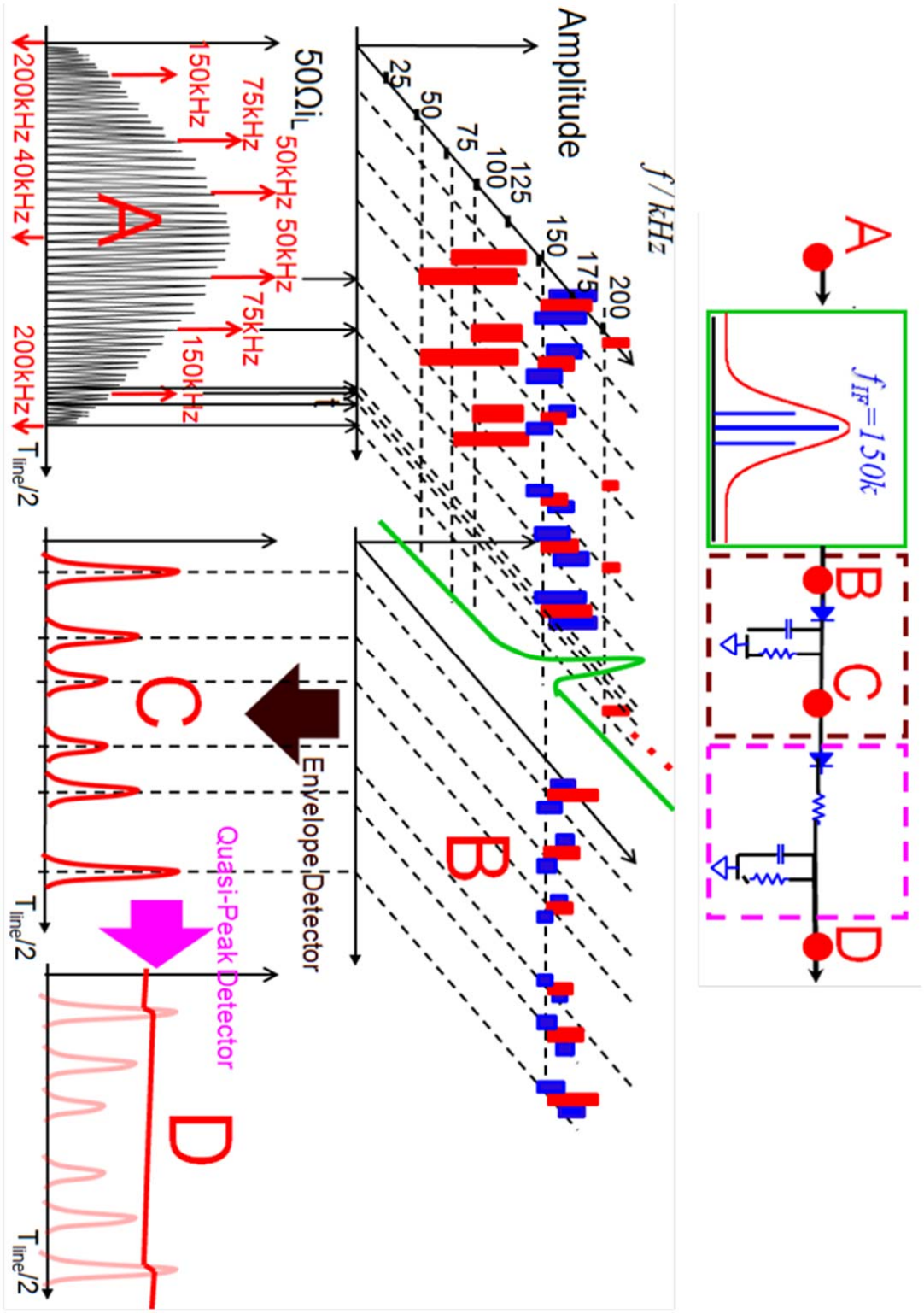


Figure 3-5 Illustration of the Principle of the Quasi-peak DM EMI Noise Measurement for Boost PFC with Variable Switching Frequency

Based on Figure 3-4, it seems that the complete equivalent circuit for quasi-peak DM EMI noise measurement has been obtained. However, it is almost impossible to get any meaningful equations out of this equivalent circuit since both time domain and frequency domain are involved and mixed together in this diagram and the equations will be too complex to be practical if how the measurement is proceeding is not i) fully understood ii) decoupled and simplified. Based on the investigation and understanding of the quasi-peak detection process in Figure 3-4, an exemplar illustration of the measurement process is shown inFigure 3-5.

Because the EMI standard starts to limit the EMI noise from 150kHz, here the intermediate frequency for the intermediate filter is initially selected to be 150kHz as an example.

At the top of Figure 3-5, the simplified block diagram for the EMI spectrum analyzer is shown to make the process easy to understand, with capital letter “A” standing for the input noise voltage, “B” for output of the intermediate filter and input of the envelope detector, “C” for output of the envelope detector and input of the quasi-peak detector and “D” for the measured quasi-peak noise at given intermediate frequency.

At “A”, triangular inductor ripple current with switching frequency range from 40kHz to 200kHz is used as an example. Because the switching frequency is very high, we assume the frequency of the triangular waveform is changing continuously. That means, there should exist triangular waveforms with frequency equals to 50kHz, 75kHz and 150kHz, respectively.

To make the measuring process more clear, the time-domain ripple current waveforms is then transferred to time and frequency domain upward, with x axis as the time, y axis as the frequency, and z axis as the amplitude of the harmonic current. As shown inFigure 3-5, at the beginning of a half line cycle, the triangular ripple current with frequency equal to 200kHz will cause harmonic currents at 200kHz, 400kHz, 600kHz and so on and so forth. A red bar is used in the time and frequency domain to represent the amplitude of the harmonic current. Here, only the 200kHz harmonic current is listed and for simplicity higher order harmonic currents are not drawn in the figure.

When the time moves on, the frequency of the triangular waveforms changes. At a certain time, the triangular waveform with the frequency equal to 150kHz will appear and cause harmonic currents and 150kHz, 300kHz, 450kHz, and so on and so forth. Only the 150kHz harmonic current is listed and others are ignored. Triangular waveforms with the frequency between 200 kHz and 150 kHz will also general harmonic currents, but they are not listed in the figure for simplicity.

With the same principle, the 75kHz and 150kHz harmonic currents caused by the triangular ripple current with the frequency equal to 75kHz and the 50kHz, 100kHz, 150kHz and 200kHz harmonics currents caused by the triangular ripple current with the frequency equal to 50kHz are all listed on the time and frequency domain with the red bars.

Around the time when the triangular ripple current with the frequency equal to 150kHz appears, there are two triangular ripple currents with the frequency equal to

the (150±ζ)kHz before and after it. Here ζ kHz represents the very small frequency difference between two consecutive single-triangular waveforms. The two triangular ripple currents with the frequency equal to (150±ζ)kHz will cause harmonic currents and (150±ζ)kHz, (300±2ζ)kHz, (450±3ζ)kHz, and so on and so forth. Only the (150±ζ) kHz harmonic currents are listed with two blue bars and others are ignored.

With the same principle, the (150±2ζ) kHz harmonic currents caused by the triangular ripple current with the frequency equal to (75±ζ) kHz and the (150kHz±3ζ) kHz harmonics currents caused by the triangular ripple current with the frequency equal to (50±ζ) kHz are all listed on the time and frequency domain with the blue bars.

All the harmonic current components need to pass the intermediate filter before it can contribute to the final quasi-peak noise. Since the intermediate filter is a 9 kHz bandwidth filter with 6dB attenuation, and for this example intermediate frequency is equal to 150kHz, only 150 kHz harmonic current and harmonic currents with close-by frequency can pass through the intermediate filter. All the other harmonic current components are filtered out.Therefore, at “B”, all the 150kHz harmonic currents pass the intermediate filter without any attenuation, shown as the red bars. And all the harmonic currents with frequency close to 150 kHz also pass the intermediate filter, but attenuated to some extent, shown as the blue bars.

Not all the harmonic component with frequency close to 150 kHz are listed or shown at “B”. For example, the (150±2ζ) kHz harmonic currents caused by the triangular ripple currents with the frequency equal to (150±2ζ) kHz are not. This is to

make the figure compact and tidy. If all the harmonic currents with frequency close to 150 kHz are listed, then the red and blue bars at “B” will make a continuous curve. This continuous curve is the amplitude envelope of all the harmonic current components.

The function of the envelope detector is just to catch this amplitude envelope. As a peak detector, the envelope detector actually eliminates the frequency related information and only keeps the amplitude information. Then the harmonic current components in time and frequency domain at “B” can be mapped to the time domain at “C”.

This amplitude envelope will then be fed into the quasi-peak detector, a charging and discharging nonlinear network specified in [59]. Because the charging time constant is much smaller than the discharging time constant, the voltage across the output capacitor of the quasi-peak detector will accumulate andincrease to a steady state value, when the charge and discharge of the output capacitor in a half line cycle should reach a charging balance. Generally because the charging time is quite a small part of the half line cycle, the voltage ripple of the output capacitor is neglected and the steady state value thus could be predicted based on the charging balance and the quasi-peak noise for given intermediate frequency is then obtained.

During this measuring process, one of the characteristics of the PFC converter helps to reduce the complexity of the principle. That is, the minimum switching frequency for the PFC converter has to be always above 20 kHz to avoid generating any audible noise. This means that for two consecutive orders of harmonics currents, the frequency difference is at least 20 kHz and if one is falling in the bandwidth of the

intermediate filter, another would never appear within the bandwidth. For example,the sixth order harmonic current of the 25 kHz triangular ripple current will have contribution to the noise at 150 kHz, but the fifth (125 kHz) or the seventh (175 kHz) order harmonic currents will be totally filtered out and have no impact on the noise at 150 kHz. This leads that, at each time point, only a single bar exists at "B" and makes the mapping from "B" to "C" mathematically possible. Otherwise, since there is no phase information for each harmonic component, it will be impossible to define the amplitude of the noise at any time instant if there is any overlap between two consecutive orders of harmonics currents --- by overlapping, it means both of them pass the intermediate filter. For power applications with typical switching frequency below 10 kHz, the corresponding bandwidth of the intermediate filter defined in the standard is also reduced to 200Hz [60], which makes the mapping principle universally true.

Since the principle of the quasi-peak EMI noise measurement procedure is clear, the mathematical prediction of the quasi-peak DM EMI noise for the CRM PFC could be carried out step by step.

3.1.2. Model of the Input Noise Voltage

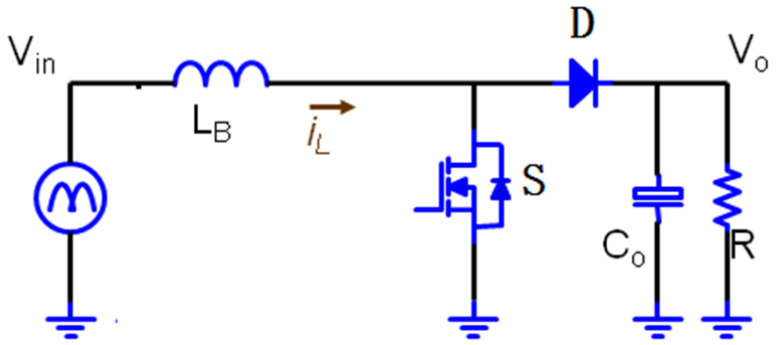


Figure 3-6 Power Stage of the Boost PFC

The model of the input noise voltage is essentially the model of the inductor ripple current. And it could be considered as one special case, the CRM mode in constant on-time PFC. The procedure is the same as that in Chapter 2 and the basic equations are derived below for the CRM PFC.

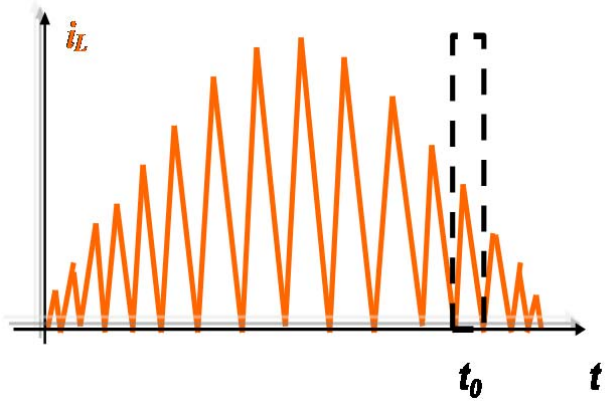


Figure 3-7 Inductor Current Sketch for the CRM Boost PFC

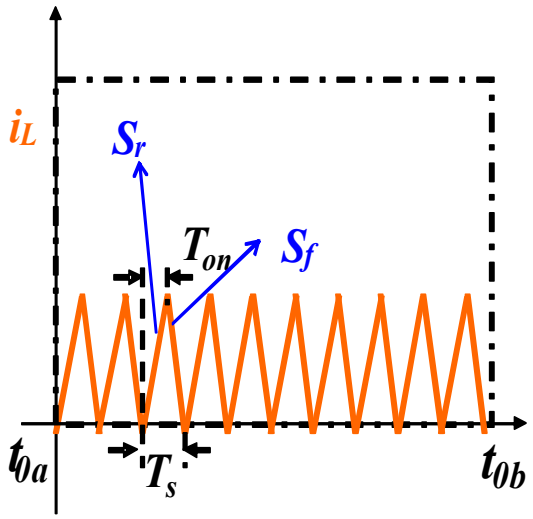


Figure 3-8 Zoom-in around t0 in Figure 3-7

Figure 3-6 is the power stage for boost PFC with all the device, passive components and circuit variables labeled. Take boost PFC in CRM as an example. The sketchedwaveform for the inductor current is shown in Figure 3-7. For the CRM boost PFC with variable switching frequency, Fourier analysis cannot be directly applied to the whole inductor ripple current waveform to extract harmonic current components.

However, the PFC circuit is running at high switching frequency and based on the Quasi Steady State assumption, which is verified in last chapter, within a very short time interval, the input voltage can be seen as a constant and the PFC can be seen as a DC-DC boost converter with that constant input voltage. Thus the inductor ripple current can be considered as periodical triangular waveform during that time interval. A zoom-inof the inductor ripple current at the time interval around time point $t_0$is shown in Figure 3-8.

For the CRM PFC converter, according to the voltage-second balance on the boostinductor, the equation below is always true.

$$T_{on}\frac{V_{in}(t_0)}{L_B}=(T_s(t_0)-T_{on})\frac{V_o-V_{in}(t_0)}{L_B} \tag{3-1}$$

Based on Figure 3-22, the rising slope of the ripple current is,

$$S_r=\frac{V_{in}(t_0)}{L_B}=\left(1-\frac{T_{on}}{T_s(t_0)}\right)\frac{V_o}{L_B} \tag{3-2}$$

And the falling slope of the ripple current is,

$$S_f=\frac{V_o-V_{in}(t_0)}{L_B}=\frac{T_{on}}{T_s(t_0)}\frac{V_o}{L_B} \tag{3-3}$$

Then the ripple current in a switching cycle can be expressed as,

$$i_{rp}(\tau)=\begin{cases} S_r\cdot\tau-\frac{1}{2}S_r\cdot T_{on}=\frac{V_o}{L_B}\left(1-\frac{T_{on}}{T_s(t_0)}\right)\tau-\frac{1}{2}\frac{V_o}{L_B}\left(1-\frac{T_{on}}{T_s(t_0)}\right)T_{on} & 0\le\tau<T_{on} \\ \frac{1}{2}S_r\cdot T_{on}-S_f\cdot(\tau-T_{on})=-\frac{V_o}{L_B}\frac{T_{on}}{T_s(t_0)}\tau+\frac{1}{2}\frac{V_o}{L_B}\left(1+\frac{T_{on}}{T_s(t_0)}\right)T_{on} & T_{on}\le\tau<T_s(t_0) \end{cases} \tag{3-4}$$

Apply Fourier transformation tothis periodical triangular waveformat the time interval around time point $t_0$and the harmonic current amplitude can be derived as,

$$|i_k(f_s(t_0))|=\frac{1}{k^2}\frac{V_o}{L_B}\frac{1}{2\pi^2 f_s(t_0)}|e^{-jk2\pi f_s(t_0)T_{on}}-1| \tag{3-5}$$

Where,

$$f_s(t_0)=\frac{1}{T_s(t_0)} \tag{3-6}$$

And ***k*** is the order number of harmonic current and ***k***=1,2,3…, which are shown in Figure 3-9.Please note that phase information for each order harmonic current is not

interesting and thus not calculated and emphasized.Equation (3-5) would apply for the whole half line cycle, thus,

$$|i_k(f_s(t))| = \frac{1}{k^2}\frac{V_o}{L_B}\frac{1}{2\pi^2 f_s(t)}|e^{-jk2\pi f_s(t)T_{on}} - 1| \tag{3-7}$$

Where,

$$f_s(t) = \frac{1}{T_s(t)} \tag{3-8}$$

And ***k*** is the order number of harmonic current and ***k***=1,2…, which can be shown in Figure 3-10,

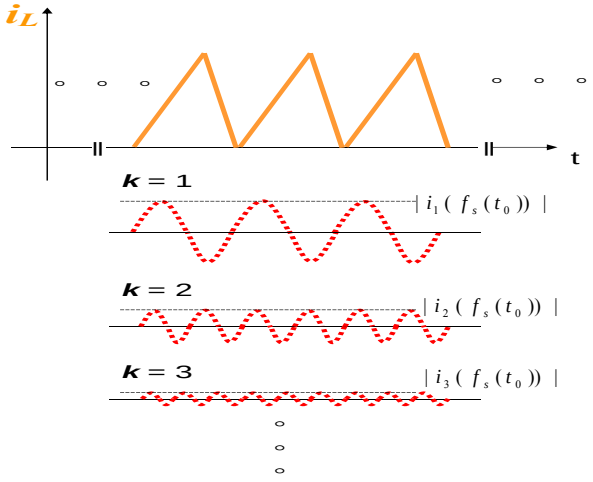


Figure 3-9 Harmonic Current Amplitude at Given Time Interval

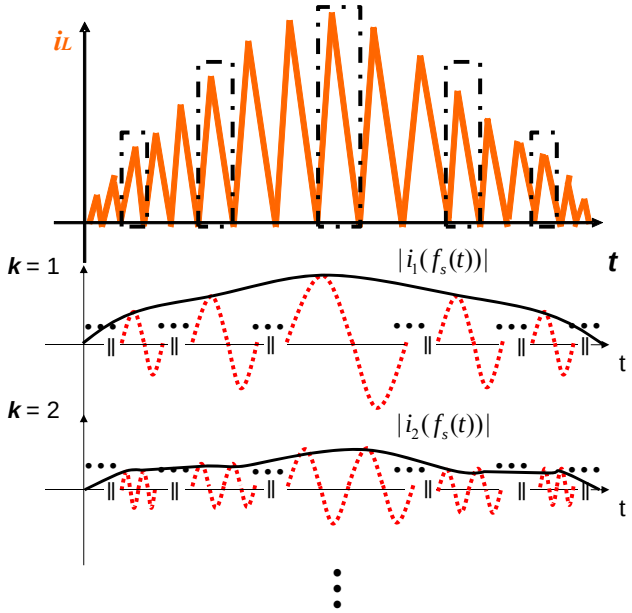


Figure 3-10 Harmonic Current Amplitude for Half Line Cycle

In some casessuch as boost PFC in CRM with maximum frequency limitation, if the boost PFC with variable switching frequency operates in DCM, with dead time T_{dead}then Equation (3-7) could be re-derived as,

$$|i_k(f_s(t))| = \frac{1}{k^2}\frac{V_o}{L_B}\frac{1}{2\pi^2 f_s(t)}\left|\left(e^{-jk2\pi f_s(t)T_{on}}-1\right)-\frac{T_{on}}{\frac{1}{f_s(t)}-T_{dead}}\left(e^{-jk2\pi\left(1-f_s(t)T_{dead}\right)}-1\right)\right| \tag{3-9}$$

Thus the harmonic current frequency and its related amplitude information have already been modeled and will be used in the following noise prediction.

3.1.3. Model of the Intermediate Frequency Filter

All the harmonic current components first need to pass through the intermediate frequency filter. What we most care about is the gain characteristics of the intermediate frequency filter. In the EMC standard [61], the gain characteristics has been specified, which is shown in Figure 3-11.

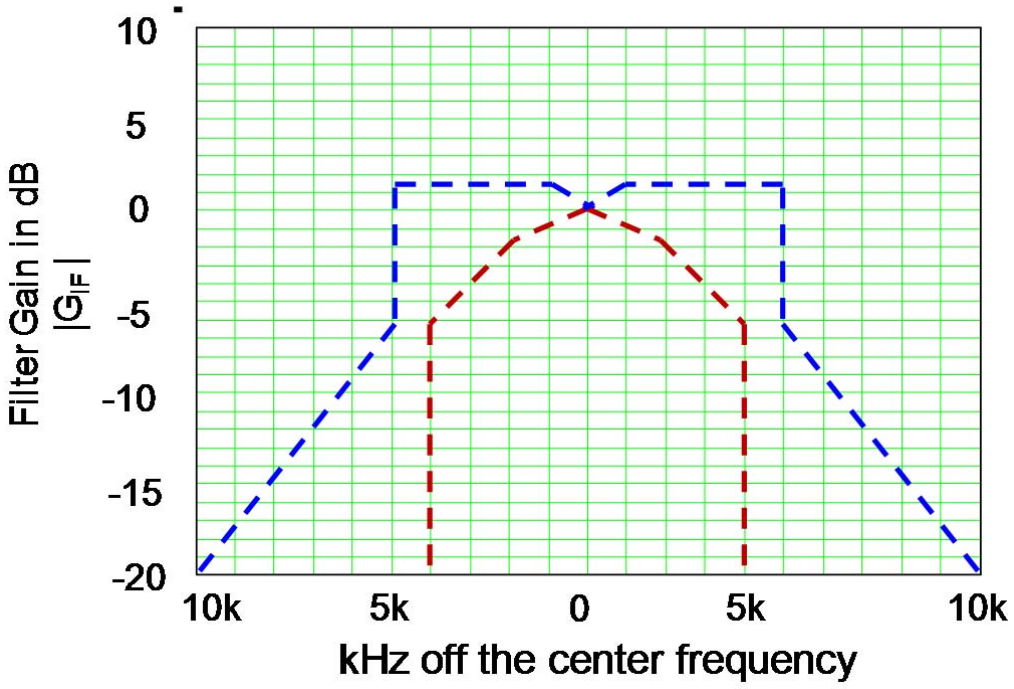


Figure 3-11 Gain Characteristics of IF Filter Specified by IEC CISPR 16-1-1

As shown in Figure 3-11, the x axis is the frequency difference between the frequency of the input noise voltage and the intermediate frequency. The y axis is the corresponding attenuation to the input noise voltage that the intermediate frequency filter need to achieve for given frequency difference. There are two dashed curves in Figure 3-11. The blue dashed curve is the upper attenuation limit and the maroon dashed curve is the lower attenuation limit. The gain characteristics of the intermediate frequency filter in the spectrum analyzer need to fall between these two

attenuation limits. First, when the frequency of the input noise voltage is equal to the intermediate frequency, i.e., the frequency difference is zero, the attenuation should also be zero. That means no attenuation for the input noise voltage at the intermediate frequency, which is already shown in Figure 3-5. Second, for frequency difference between 4 kHz to 5 kHz, 6dB attenuation needs to be achieved. Therefore generally the intermediate frequency filter is characterized as 9 kHz bandwidth with 6dB attenuation.

The actual gain characteristics of the IF filter for different analog spectrum analyzer could be different and are not known. For the most direct way, either the upper lime or the lower limit can be used as the actual gain characteristics. However, it is hard to achieve such gain characteristics for IF filter. A classical type of filer with similar gain characteristics is the Gaussian filter. Is it possible to use Gaussian filter to describe the intermediate filter?

The equation for the gain characteristics of the Gaussian filter is,

$$|G(\Delta f)| = \frac{1}{\sqrt{2\pi}\cdot\sigma} e^{-\frac{(\Delta f)^2}{2\sigma^2}} \tag{3-10}$$

Based on the short discussion about the gain characteristics of the IF filter specified in the EMC standard, Equation (3-10) should satisfy the following two equations,

$$|G(\Delta f = 0)| = 0dB \tag{3-11}$$

and

$$|G(\Delta f = \pm 4.5kHz)| = -6dB \tag{3-12}$$

Because there is only one parameter σ in Equation (3-10), it is impossible for it to

satisfy both Equation (3-11) and Equation (3-12). However, if we simply ignore the non-exponential part in Equation (3-10), then the Equation (3-11) would be satisfied naturally. Then based on the Equation (3-12), we can solve that,

$$\sigma = \frac{9k}{2\sqrt{2\ln 2}} \tag{3-13}$$

Thus, the equation of the gain characteristics of the IF filter can be expressed as,

$$|G_{IF}(f, f_{IF})| = e^{-\frac{(f-f_{IF})^2}{c^2}} \tag{3-14}$$

Where,

$$c = \sqrt{2}\sigma = \frac{9k}{2\sqrt{\ln 2}} \tag{3-15}$$

And f is the frequency of the input noise voltage and f_{IF} is the intermediate frequency. Equation (3-14) can be seen as the expression for gain characteristics of a near Gaussian filter, which is also mentioned conceptually in [62].

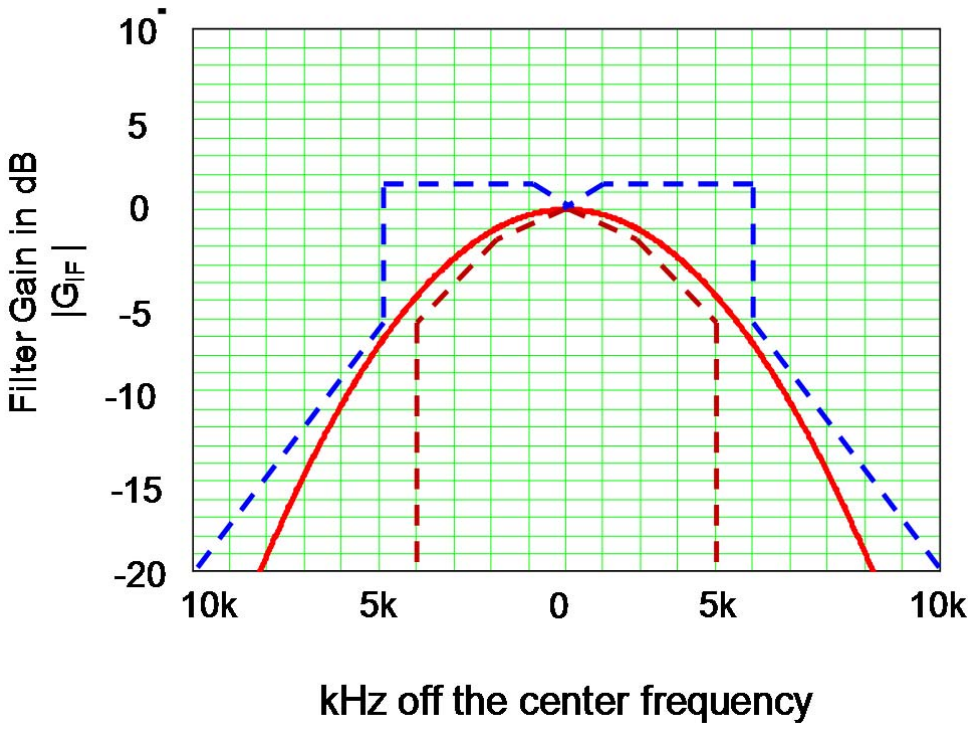


Figure 3-12 Proposed Gain Characteristics of the Intermediate Filter

The gain curve for Equation (3-14) is drawn in Figure 3-12 as the red solid curve and compared with the limits specified by the EMC standard. We can see the gain curve expressed with the modified gain equation fits in the limits very well. It will be good to filter the harmonic currents modeled in Section 3.1.2.

3.1.4. Model of the Output of the Envelope Detector

For kth order input voltage noise, the equation of its amplitude over half-line cycle can be expressed as,

$$V_k(t) = 50\Omega \cdot |\, i_k(\, f_s(t))\,| \tag{3-16}$$

And after passing the IF filter, it will be selectively attenuated. These attenuated high frequency sinusoidal-shaped noise waveforms will continuously pass through the envelope detector. For the kth order noise voltage, the output of the envelope detector would be, shown in Figure 3-13,

$$V_k(t,\, f_{IF}) = 50\Omega \cdot |\, i_k(\, f_s(t))\,| \cdot |\, G_{IF}(kf_s(t),\, f_{IF})\,| \tag{3-17}$$

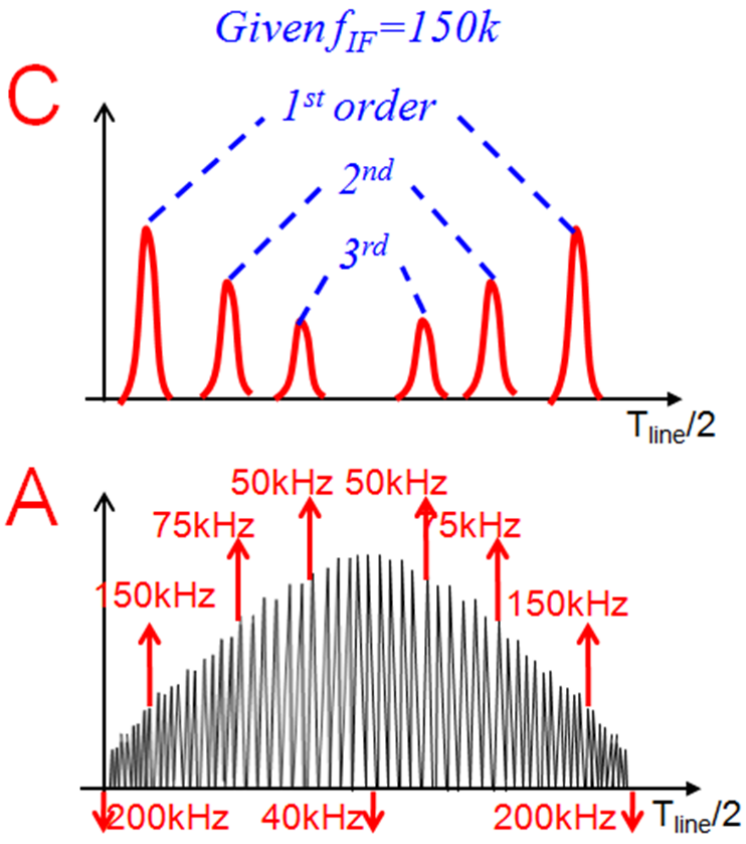


Figure 3-13 Output of the Envelop Detector for the Example

All of these envelope plateaus at "C" are caused by different order harmonic

components and thus appear at different periods of the half line cycle. The total output of the envelop detector would be the sum of all the plateaus,

$$V_{Envelope}(t, f_{IF}) = \sum_{1}^{N} V_k(t, f_{IF}) \tag{3-18}$$

Where,

$$N = [\frac{f_{IF}}{\min f_s}] \tag{3-19}$$

3.1.5. Calculation of the Quasi-peak EMI Noise

Finally the envelope output described in Equation (3-18) is fedinto Quasi-peak detector, which is a charging and discharging network with charging and discharging time constant specified in the standard: charging time constant τ_C=1ms and discharging time constant τ_D=160ms. Because the quasi-peak detector's charge constant is much smaller than the discharge constant, at the beginning the voltage across the output cap will be charged up and finally reach a steady state. This steady state is a charging balance and can be expressed by equation,

$$\int_0^{\Delta T} \left(\frac{V_{Envelope} - V_{Quasi}}{R_1} \right) dt = \frac{V_{Quasi}}{R_2} (\frac{T_{line}}{2} - \Delta T) \tag{3-20}$$

Where, $V_{Envelope}$is known and V_{Quasi} is the unknown variable. ΔT is the total charging period, which is a function of V_{Quasi}.

The analog circuit for the quasi-peak detector in [63] is one possible implementation. Since there is a diode in the quasi-peak detection circuit, it is nonlinear and no analytical solution can be solved for Equation (3-20).Based on the

charging balance on the output cap, for each given f_{IF}, a dichotomy algorithm, shown in Figure 3-14 is proposed in this dissertation to solve Equation (3-20). And then the quasi peak noise value $V_{quasi}(f_{IF})$ can be calculated numerically using this dichotomy algorithm.

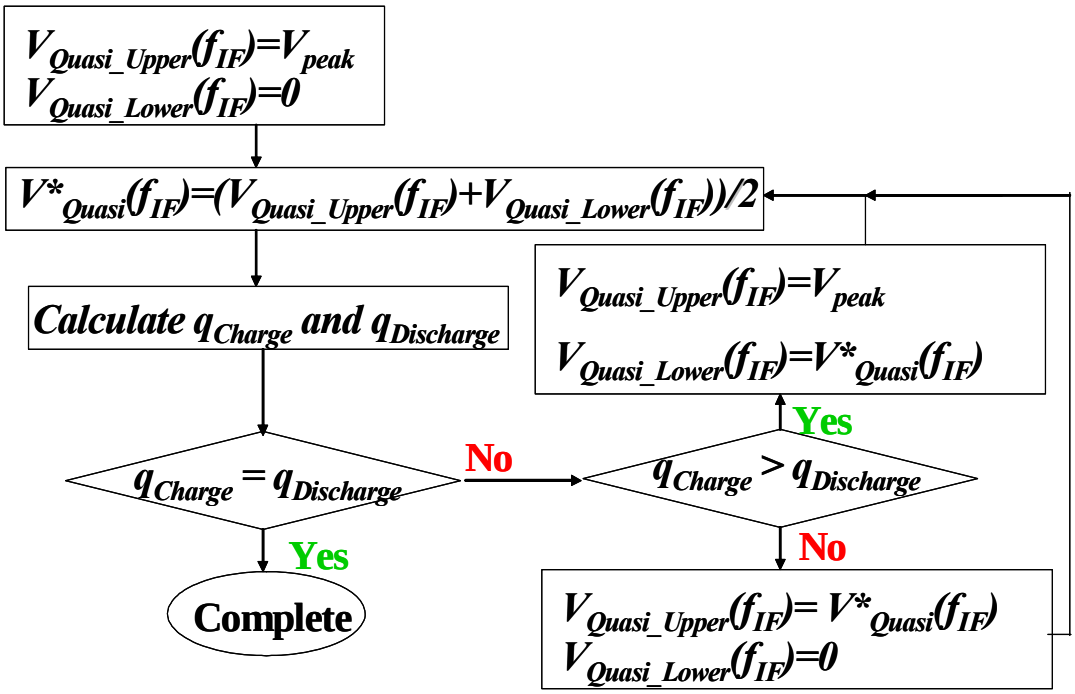


Figure 3-14 Numerical Algorithm Diagram to Calculate Quasi-peak Noise

As shown in the Figure 3-14, to predict the quasi-peak noise, we need to utilize the peak noise for the same frequency as the initial value to begin the iteration. Since the peak noise prediction is already investigated and verified in Chapter 2, we will not duplicate the process here and just integrate it into the quasi-peak noise prediction.

Generally around 10 iterations, a numerical solution with 0.1% accuracy will be achieved and that is considered $q_{Charge}=q_{Discharge}$ and the algorithm completes. Finally we obtain the value of V_{quasi} for an intermediate frequency f_{IF}. The whole noise spectrum results can be obtained by sweeping f_{IF} from 150kHz to 30MHz. However,

when the noise frequency is up to several mega hertz, the circuit parasitic parameter such as the equivalent parallel capacitance of the boost inductor will come into playing an important role and weakening the accuracy of the prediction [64]. In this paper, only noise at low frequency range from 150kHz to 1MHz, which determines the selection of the EMI filter inductance and capacitance [65], is predicted, considering generally minimum switching frequency for PFC converters would be far below 1 MHz.

All above discussionsfrom Section 3.1.1 to Section 3.1.5 only give us one data point, the quasi-peak DM EMI noise value for one given intermediate frequency. We can sweep f_{IF} from 100 kHz to 1 MHz and calculate many data points. Connecting all the data points, we can get the predicted noise spectrum curve shown in Figure 3-15.We can see that the predicted quasi-peak noise matches the measurement very well and thus will be helpful in the optimized design of the DM EMI filter.

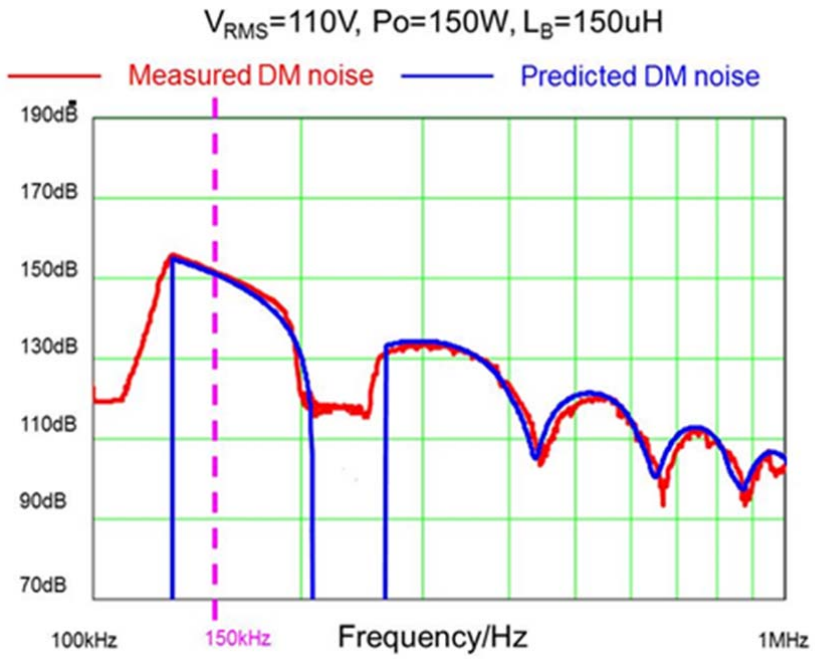


Figure 3-15 Quasi-peak noise prediction verification for the CRM PFC

3.2. DM EMI Noise Worst Case Analysis for Critical Conduction Mode PFC

The prediction of the EMI noise is not the final goal. The fundamental reason for the EMI noise prediction is to find the guidance that how to design the EMI filter and to reduce the whole converter size. In order to design an EMI filter to meet the EMC standard in all line and load conditions, the worst case of the EMI noise needs to be identified. In this chapter, the worst case analysis for the CRM boost PFC is carried out. All the noise used in this chapter is based on the prediction using the mathematical model proposed in Section 3.1.Based on [66], corner frequency of the DM EMI filter would be a good index to evaluate the DM EMI noise. Larger corner frequency means smaller EMI filter size and thus better EMI noise and smaller corner frequency means larger EMI filter size and thus worse EMI noise. So the worst case of the DM EMI noise would be the noise which requires the DM EMI filter with the smallest DM corner frequency.

3.2.1. DM EMI Noise Worst Case Analysis for Single Boost PFC in CRM

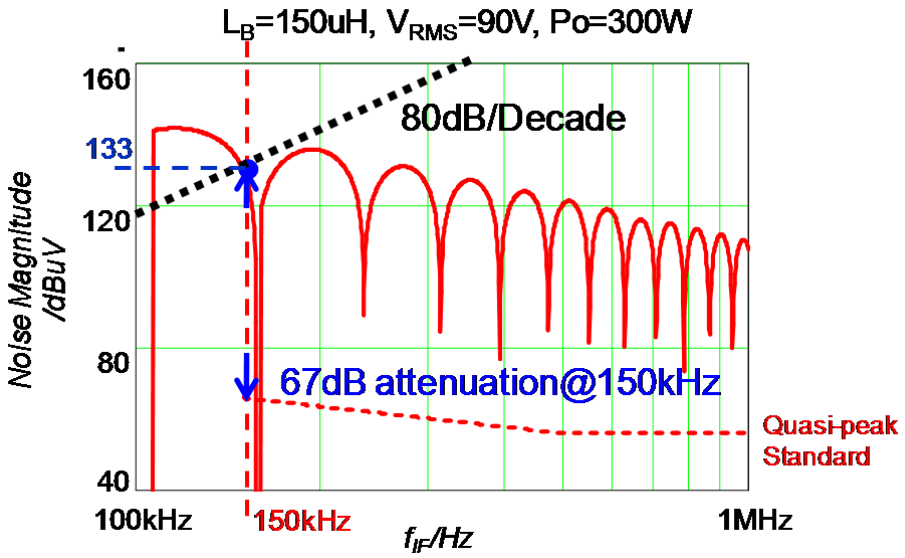


Figure 3-16 DM EMI Noise Prediction at Full Load with V_{RMS}=90V for CRM PFC

As shown in Figure 3-16, for quasi-peak DM EMI noise at V_{RMS}=90V, Po=300W, the noise@150kHz is 133dBuV and needs 67dB attenuation to meet the quasi-peak EMI standard. Because the switching frequency range is from 53 kHz to 79 kHz, the noise at 150 kHz is dominated by the second order harmonic component. The black dotted line with 80dB/decade slope represents the slope of the insertion gain of the 2-stage DM EMI filter, 100dB/decade, plus the slope of the quasi-peak EMI standard from150 kHz to 500 kHz, -20dB/decade. It justifies that if the noise at 150 kHz will be attenuated below the EMI limit by the designed EMI filter, then noise all over the frequency spectrum will also meet the standard. It means for this case, the EMI filter could be designed based on the noise at 150 kHz.

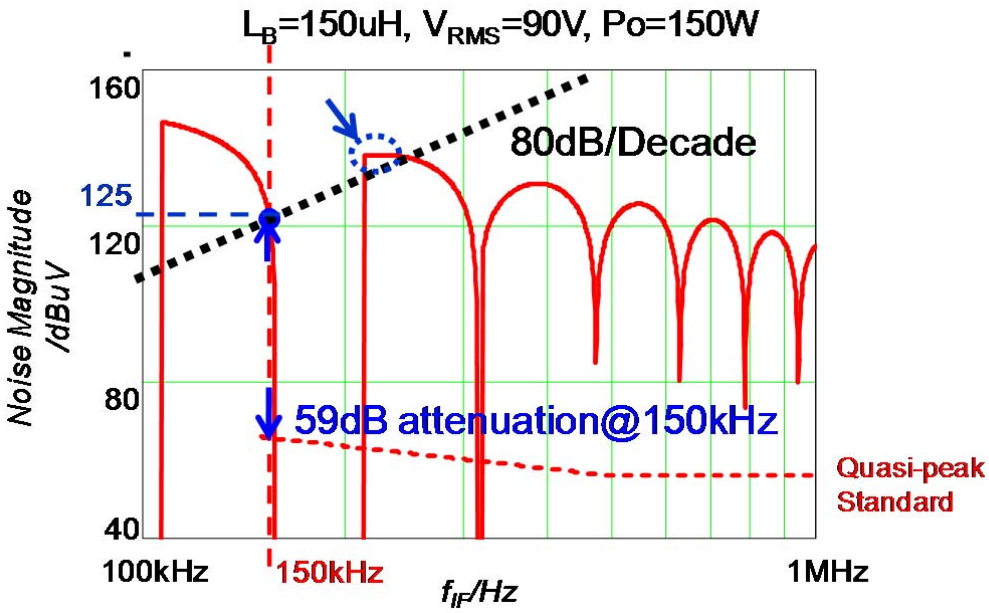


Figure 3-17 DM EMI Noise Prediction at Half Load with V_{RMS}=90V for CRM PFC

Thus, the corner frequency of the two stage DM EMI filter can be calculate as,

$$f_C = \frac{150kHz}{10^{\frac{67dB}{100dB}}} = 32kHz \tag{3-21}$$

We obtain the first data point for the corner frequency of the DM EMI filter.

The quasi-peak DM EMI noise at V_{RMS}=90V, Po=150W is predicted in Figure 3-17. Because the switching frequency range is from 106 kHz to 158 kHz, the noise at 150 kHz is dominated by the first order harmonic component this time. The noise@150kHz is 125dBuV and needs 59dB attenuation to meet the quasi-peak EMI standard. However, the EMI filter could not be designed based on the noise at 150 kHz this time. We can see that the black dotted line with 80dB/decade slope is below the noise dominated by the second order harmonic components encircled by the blue dotted circle.That means, if we design the DM EMI filter based on the noise at 150 kHz for this case, then at certain frequencies, the EMI standard will not be satisfied. Thus, the EMI filter should be designed based on the right noise point, shown in Figure 3-18.

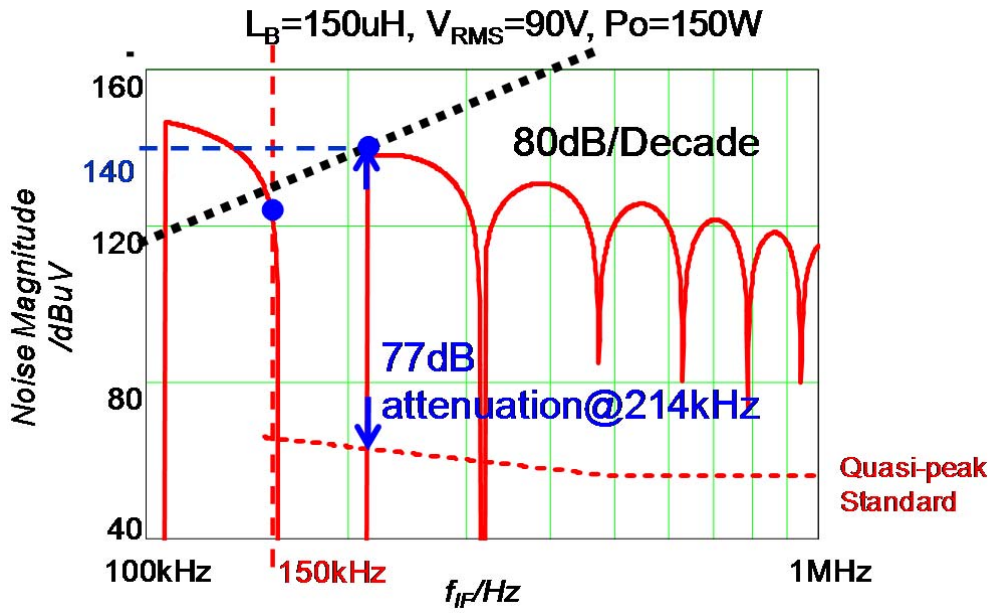


Figure 3-18 Choose Right Noise Point to Design EMI Filter

Thus, the corner frequency of the two stage DM EMI filter can be calculate as,

$$f_C = \frac{214kHz}{10^{\frac{77dB}{100dB}}} = 36kHz \tag{3-22}$$

We obtain the second data point for the corner frequency of the DM EMI filter. And these two data points can be drawn in Figure 3-19.

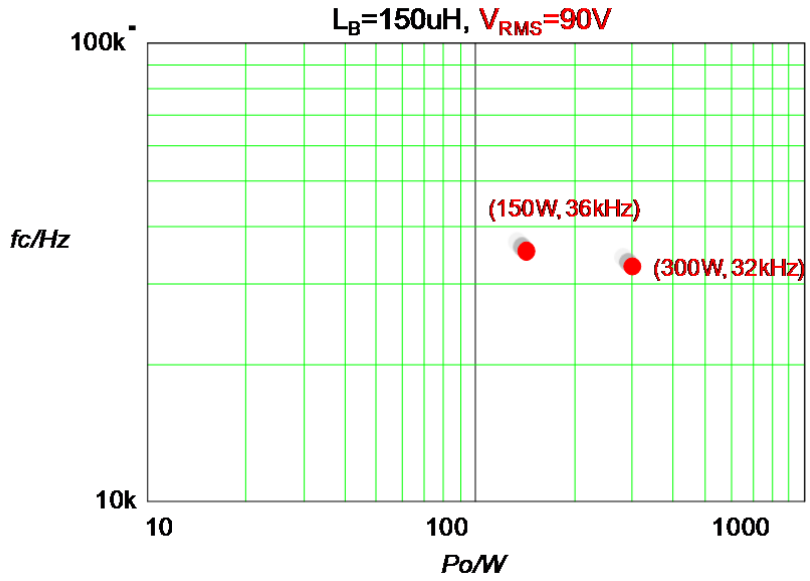


Figure 3-19 Two Data Points for the DM EMI Filter Corner Frequency

The corner frequency of DM EMI filter for 300Watts load is smaller than that for 150Watts, which means it has worse DM EMI noise. If we can draw the corner frequency vs. output power for the whole load range, we should be able to tell what the worst EMI noise case is.

Continuing the corner frequency calculation process for the whole load range, we can draw Figure 3-20. Thus the worst DM EMI noise case for V_{RMS}=90V is at 105W. The predicted DM EMI noise can be drawn inFigure 3-21.

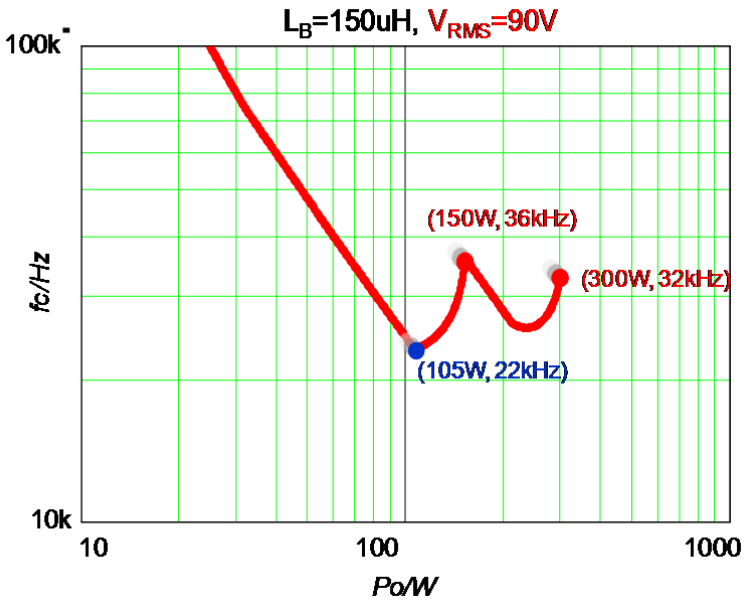


Figure 3-20 Corner Frequency vs. Output Power for V_{RMS}=90V

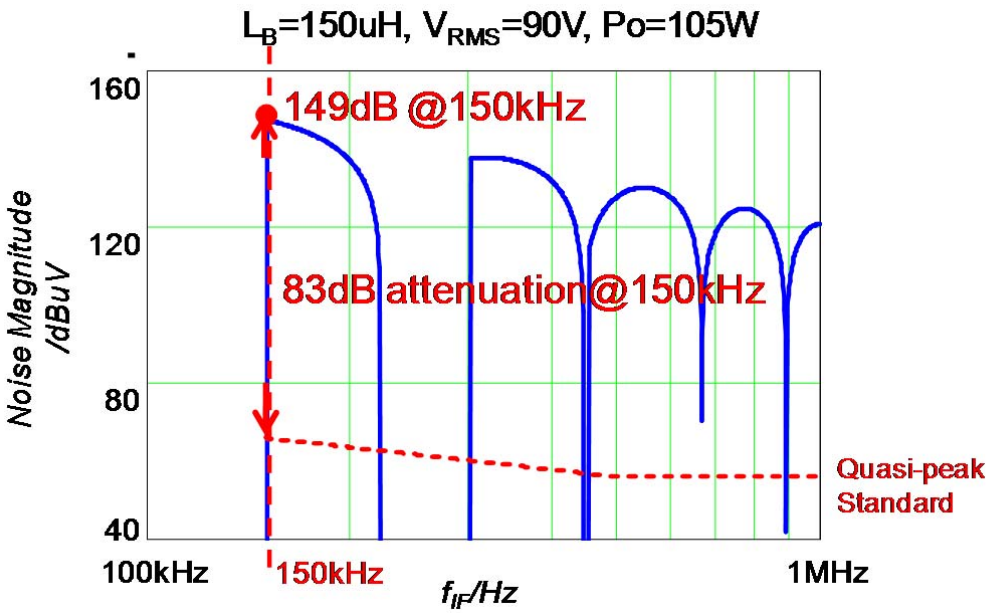


Figure 3-21 Worst DM EMI Noise Case for V_{RMS}=90V

We can see that the peak noise point is just at 150 kHz. And actually the switching frequency range for V_{RMS}=90V, P_O=105W is from 150 kHz to 222 kHz. Thus the first order harmonic component of the 150 kHz current ripple results the

high magnitude noise at 150 kHz, which dominates the EMI filter design.

This worst case is only the local worst case for the V_{RMS}=90V, not the global worst case until all the line conditions are considered. Based on the same principle, Figure 3-22, 3-23 and 3-24 show the corner frequency vs. output power for V_{RMS}=110V, 220V, 265V, respectively.

Put Figure 3-22, 3-23 and 3-24 together, we obtain the complete corner frequency diagram for all line and load conditions as shown in Figure 3-25.

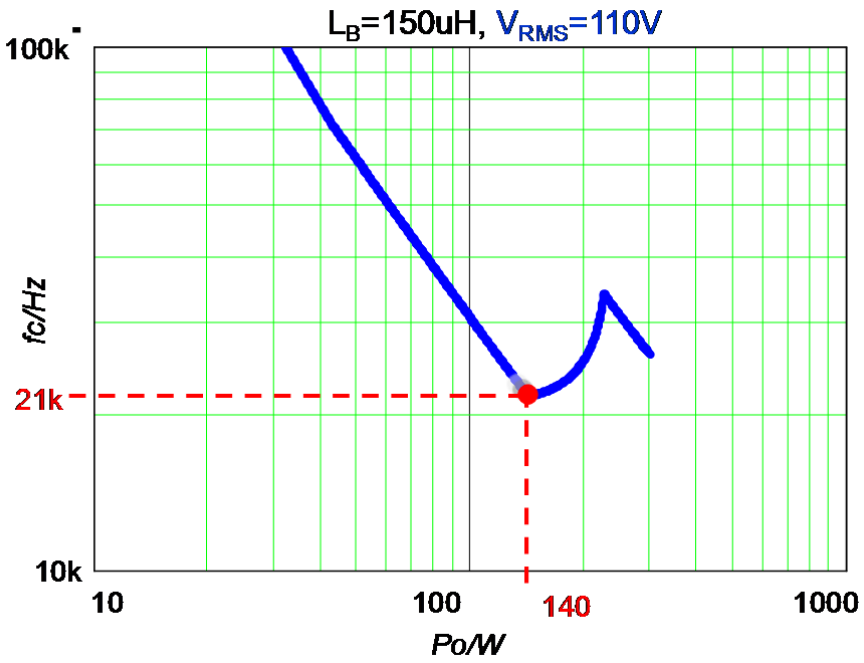


Figure 3-22 Corner Frequency vs. Output Power for V_{RMS}=110V

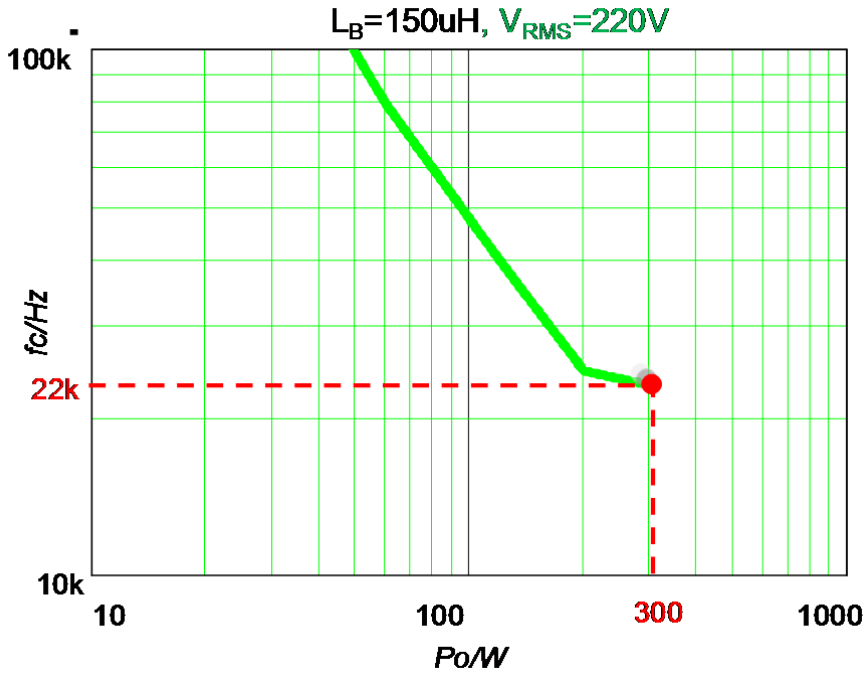


Figure 3-23 Corner Frequency vs. Output Power for V_{RMS}=220V

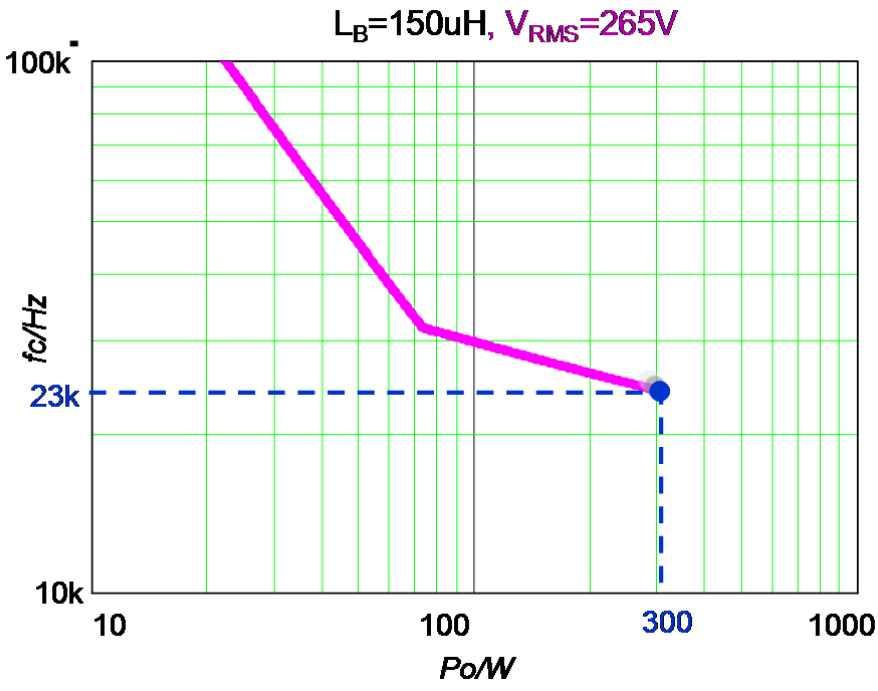


Figure 3-24 Corner Frequency vs. Output Power for V_{RMS}=265V

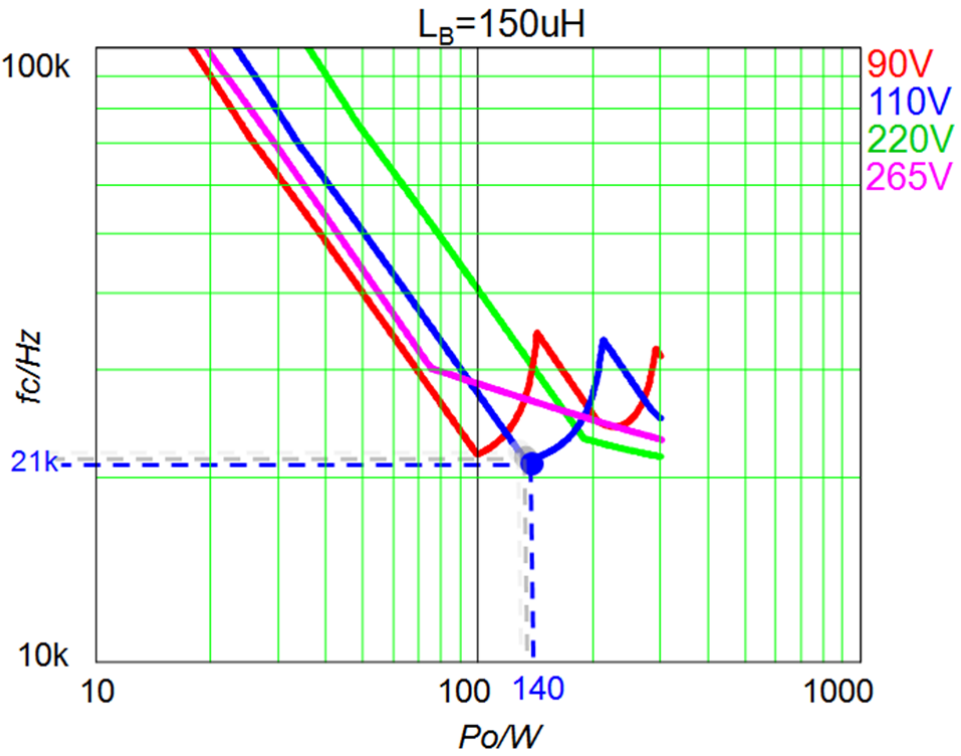


Figure 3-25 Corner Frequency vs. Output Power for All Input Line Conditions with L_B=150uH

Based on Figure 3-25, the worst case for all line and load conditions is easily obtained, it is at low line (V_{RMS}=110V), partial load (Po=140W). Not as expected as in constant frequency CCM PFC, the lowest line (V_{RMS}=90V), full load (Po=300W) is not the worst case and it is not even a bad case. That is because this is variable frequency and you can hardly avoid noise at 150 kHz, which could be dominated by the first order, the second order or even the third order harmonic component.

3.2.2. Filter Design Criteria for Single Boost PFC in CRM

In last section the DM EMI noise worst case is found for a given boost inductance. In practical design, the boost inductance is selected based on the trade off the efficiency and the size of the boost inductor. So generally the boost inductance is the only design variables for the CRM boost PFC.One straightforward method to find the design criteria would be following the same process in section 3.2.1 and finding all the DM EMI noise worst case for different selections of the boost inductance.For example, if L_B=200uH, the Corner Frequency vs. Output Power for All Input Line Conditions then is shown in Figure 3-26.

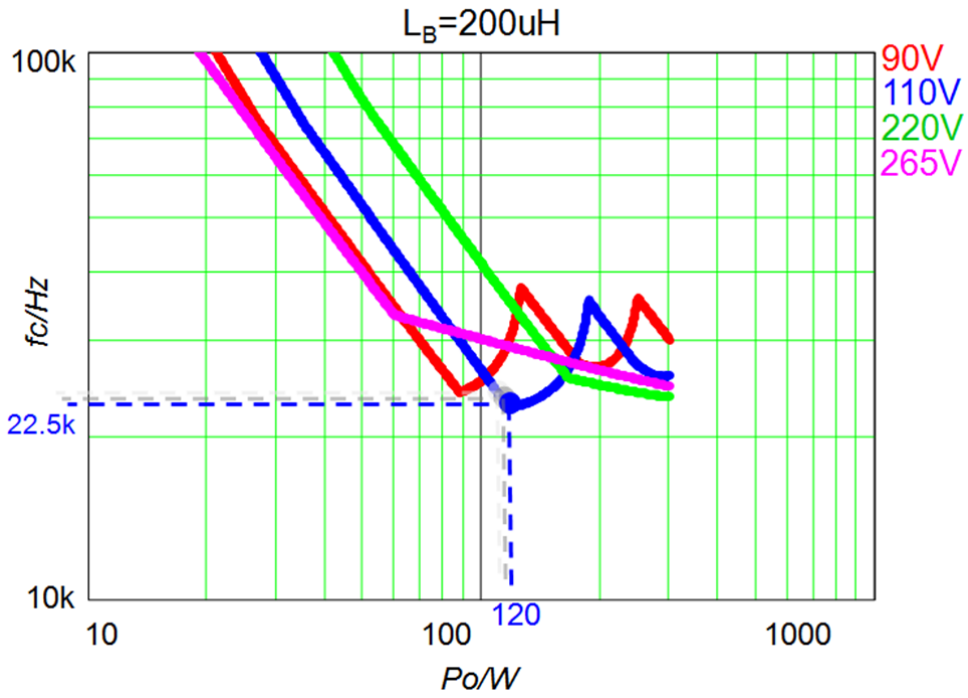


Figure 3-26 Corner Frequency vs. Output Power for All Input Line Conditions with L_B=200uH

So for different selection of boost inductance, we can go through this process repeatedly. Table 3 lists some of the results.

Table 3 Worst fc for different selections of boost inductance

Boost Inductance	Worst fc	V_{RMS}	Load
100uH	19.5 kHz	110V	240W
150uH	21 kHz	110V	140W
200uH	22.5 kHz	110V	120W
250uH	23.5 kHz	220V	300W
300uH	24 kHz	220V	300W

When LB is 300uH, the minimum switching frequency is 20 kHz, shown in Figure 3-27. When LB is larger than 300uH, the minimum switching frequency would be below 20 kHz, and then the audible noise will be a concern. So 300uH is the largest recommended selectable boost inductance.

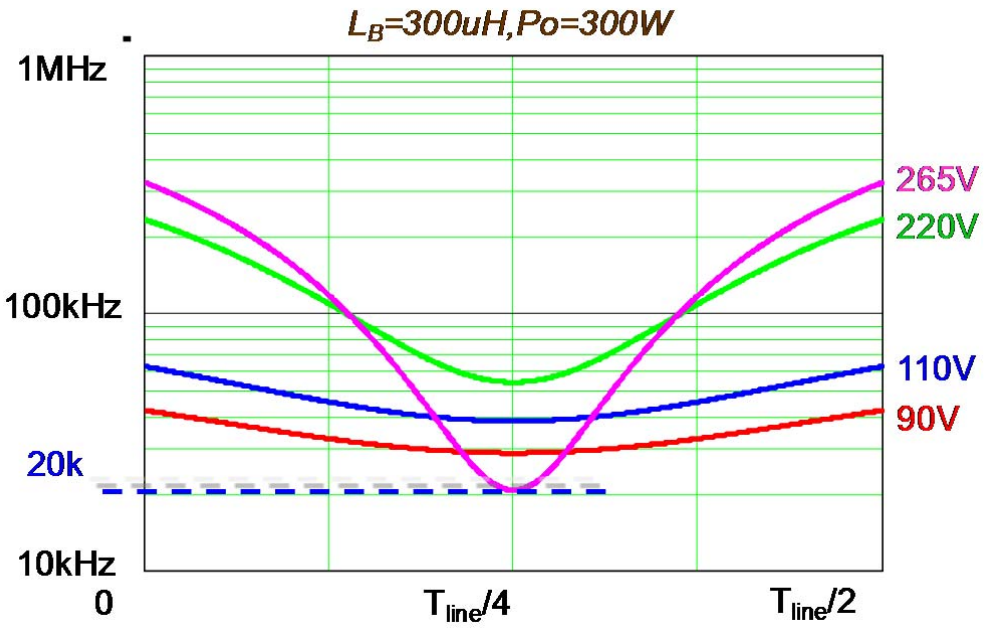


Figure 3-27 Switching Frequency over Half Line Cycle for Different Input Line Voltage

Based on Table 3, worst corner frequency vs. boost inductance could be obtained in Figure 3-28.

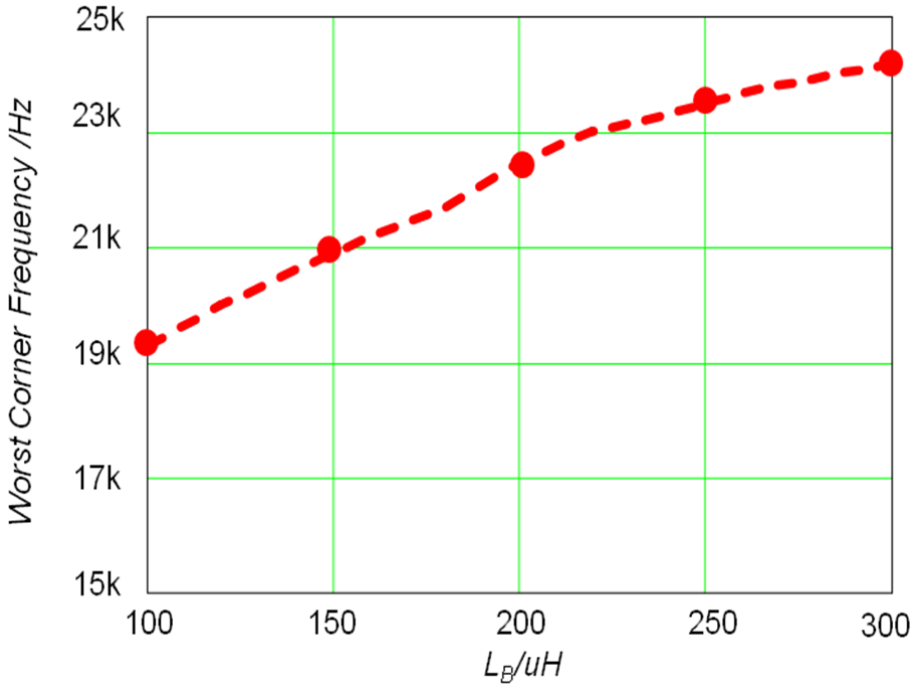


Figure 3-28 Worst corner frequency vs. boost inductance

This curve is valid for different line and load conditions and thus could be used to design the DM EMI filter after selecting the boost inductance, which could help to avoid the over-design or the under-design of the EMI filter.

However, this is a little bit complex to get this curve to help design the EMI filter. Through the analysis, it is also found that the frequency range of the highest line (V_{RMS}=265V) is the largest, and generally includes 150 kHz at full load. That is to say, for the highest line, there is always a current ripple with frequency equal to 150 kHz, whose first order harmonic component will generate noise at 150 kHz. This is surely a bad case. Figure 3-22 and Figure 3-24 are redrawn together, shown in Figure 3-29.

There is 2 kHz difference in corner frequency between worst case for V_{RMS}=265V and the global worst case and equivalently about 4dBuV difference in noise at 150 kHz. So considering the highest line, full load as the worst EMI noise condition would

be a simple way to design the EMI filter as long as some margins are reserved.

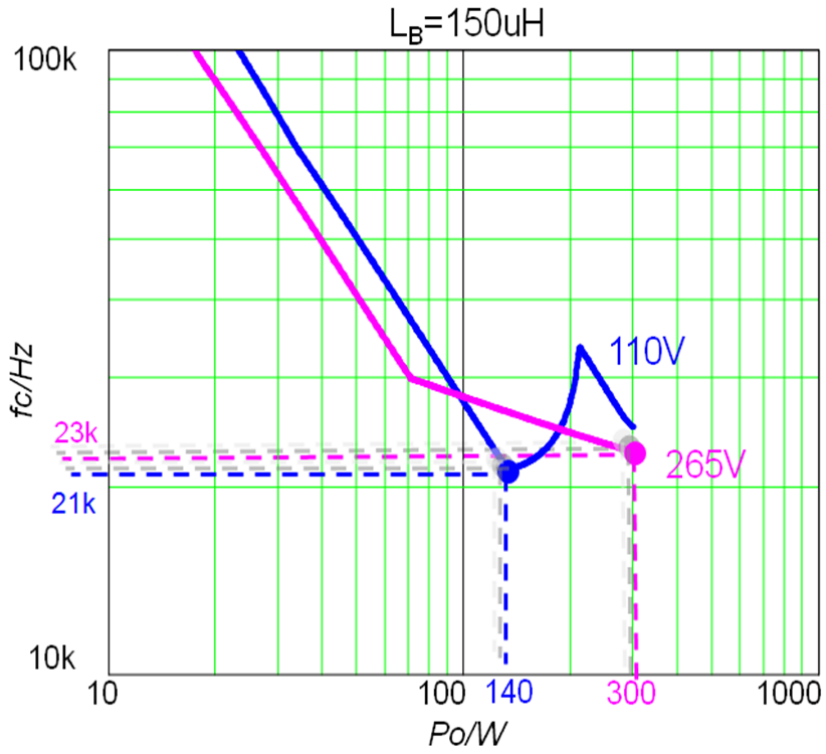


Figure 3-29 Corner Frequency Comparison between V_{RMS}=110V and V_{RMS}=265V

3.2.3. DM EMI Noise Worst Case Analysis for Interleaved Boost PFC in CRM

Interleaving techniques are used in constant frequency CCM PFC to achieve ripple cancellation and improve EMI performance [67]. Its influence on the CRM boost PFC is also an interesting topic. The sketch diagram is shown in Figure 3-30.Figure 3-31 and Figure 3-32 show the calculated ripple current reduction by using 2-channel interleaved CRM boost PFC.

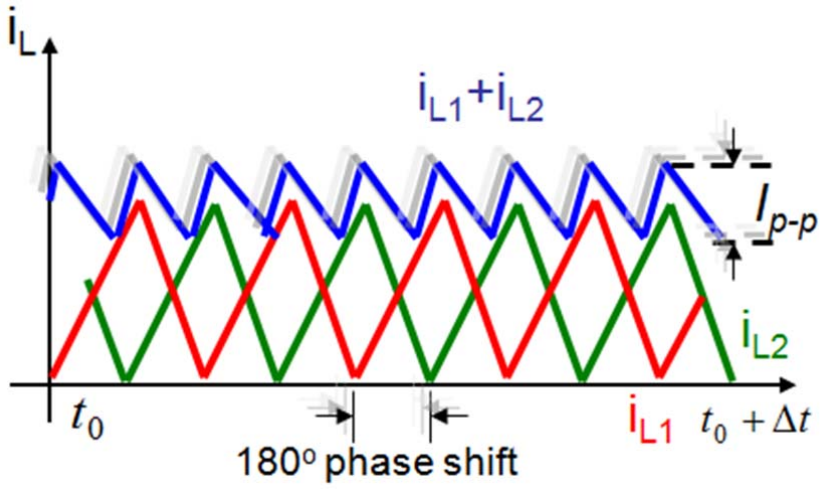


Figure 3-30 Total Inductor Ripple Current Sketch

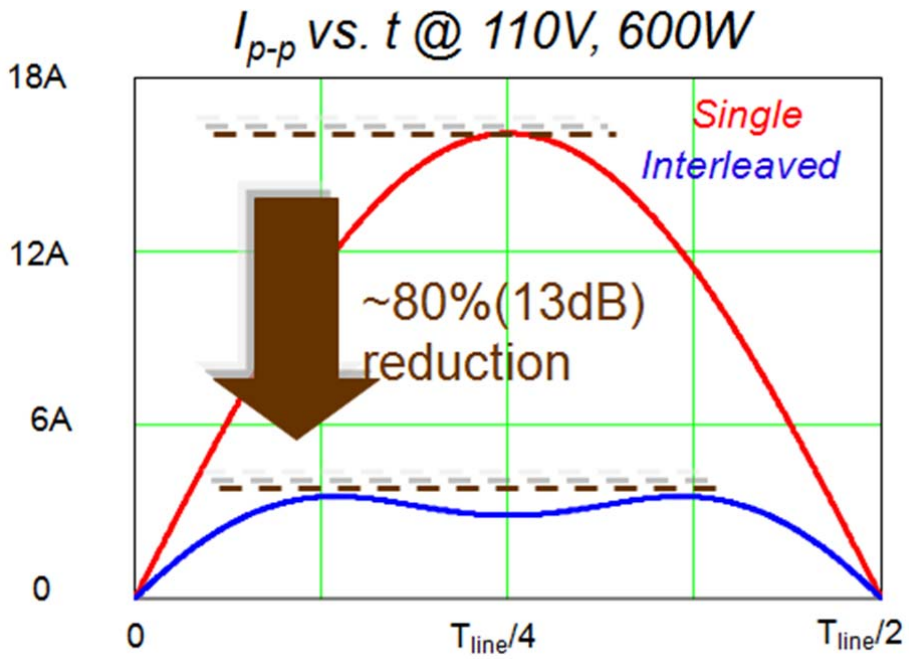


Figure 3-31 Ripple Current Reduction by Interleaving at Low Line

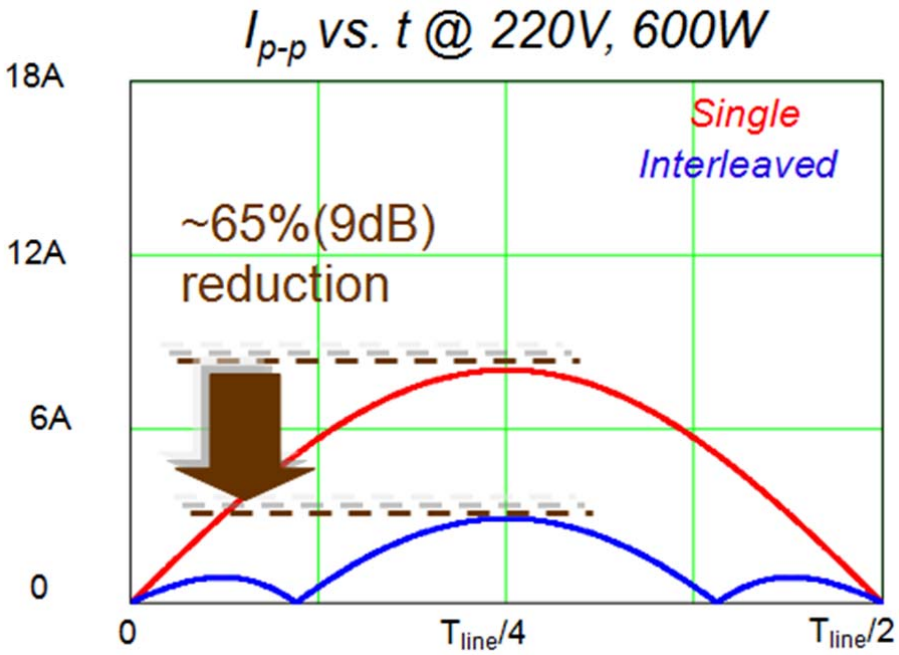


Figure 3-32 Ripple Current Reduction by Interleaving at High Line

From Figure 3-31 and 3-32, we can see at least 9dB ripple current reduction can be achieved. Can the same EMI performance improvement be achieved?

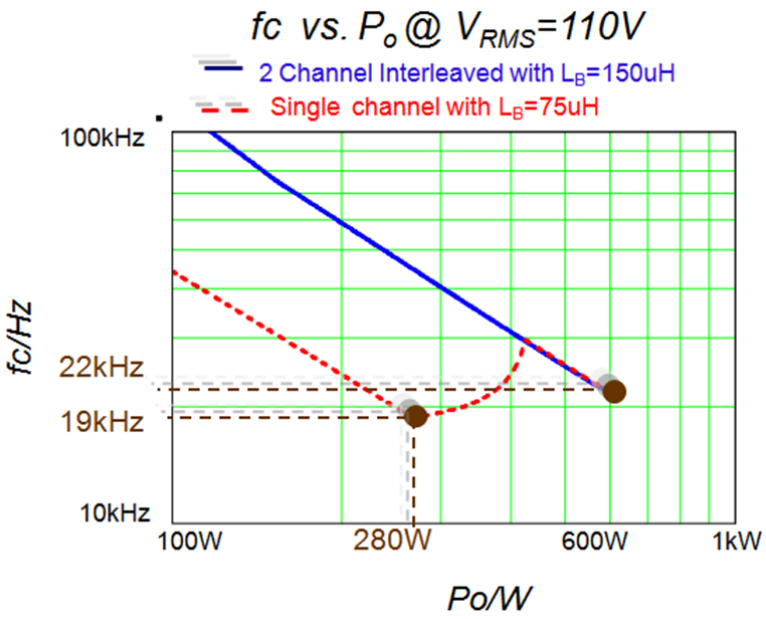


Figure 3-33 DM EMI Filter Corner Frequency Comparison

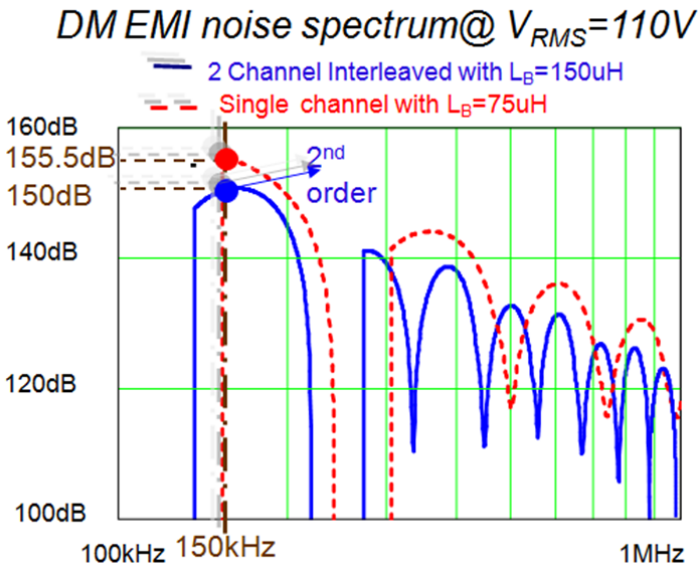


Figure 3-34 Worst Case of DM EMI Noise Comparison

In Figure 3-33, the DM EMI noise worst cases in single channel CRM boost PFC and in 2-channel interleaved PFC are compared. We can see only 3 kHz improvement is achieved. If we compare the corresponding noises in Figure 3-34, we can see for 2-channel interleaved PFC with switching frequency from 71 kHz to 116 kHz,

although the first order harmonic component is cancelled, the second order harmonic component of the 75 kHz ripple, which appears at 150 kHz, diminishes the improvement.One possible way to continue improving the EMI performance on the 2-channel interleaved boost PFC is to push the minimum switching frequency above 75 kHz. For 2 channel interleaved boost PFC, when L_B=80uH, the minimum switching frequency is 76 kHz, when V_{RMS}=265V. The corner frequency analysis with L_B = 80 uH is shown in Figure 3-35.

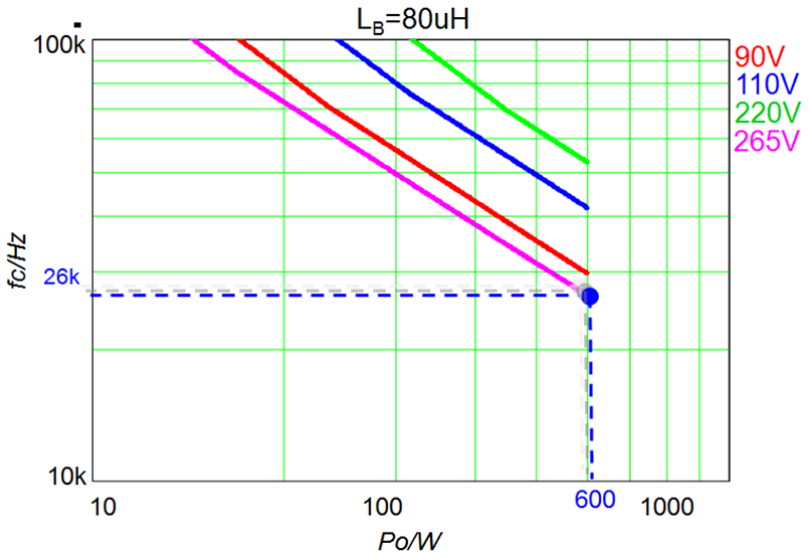


Figure 3-35 Corner Frequency vs. Output Power for All Line Conditions with L_B=80uH

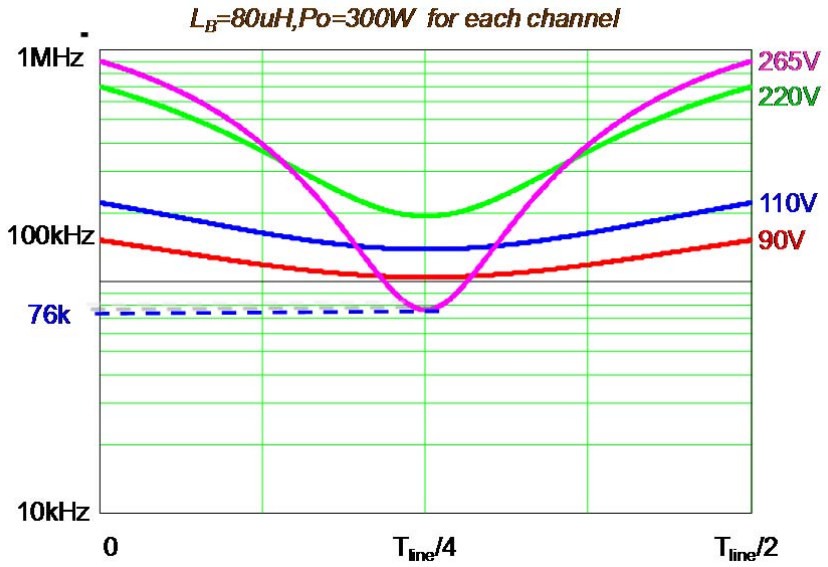


Figure 3-36 Switching Frequency Range of 2-Channel Interleaved CRM PFC for All Line Conditions

We can see that the worst case happens at highest line V_{RMS}=265V, full load 600W, since for lower input line voltage, the minimum frequency is already far away above 75kHz, which can be shown in Figure 3-36.

We can further reduce the boost inductance to benefit the EMI filter design, with the penalty of higher switching loss. The DM EMI filter corner frequency for worst case DM EMI noise for different selection of boost inductance per channel is shown in Figure 3-37.

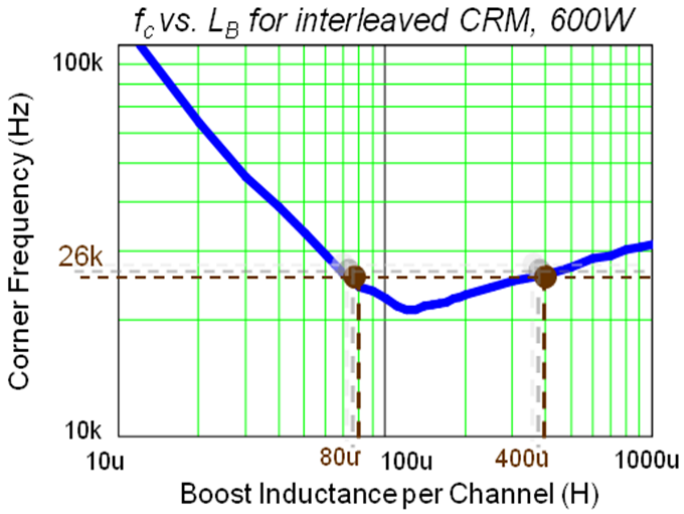


Figure 3-37 Worst corner frequency vs. boost inductance per channel

Either L_B=80uH or L_B=400uH will lead to the same DM EMI filter design (fc=26 kHz in this example). The choice of L_B=80uH has smaller size of boost inductor but higher switching frequency, and the choice of L_B=400uH has larger size of boost inductor but lower switching frequency. Figure 3-37 can help to bring the DM EMI filter into considerationwhen doing the efficiency and size trade-off for the multi-channel interleaved CRM boost PFC.

Chapter 4. EMI FILTER DESIGN OPTIMIZATION BASED ON NOISE PREDICTION

When talking about the practical EMI filter design for the offline power applications, we need to consider both the DM EMI noise andthe CM EMI noise. For offline front-end converter, the isolated DCDC converter is also playing an important part for the CM EMI noise. The EMI test circuit diagram with the LLC converter as the DCDC stage is shown as Figure 4-1.

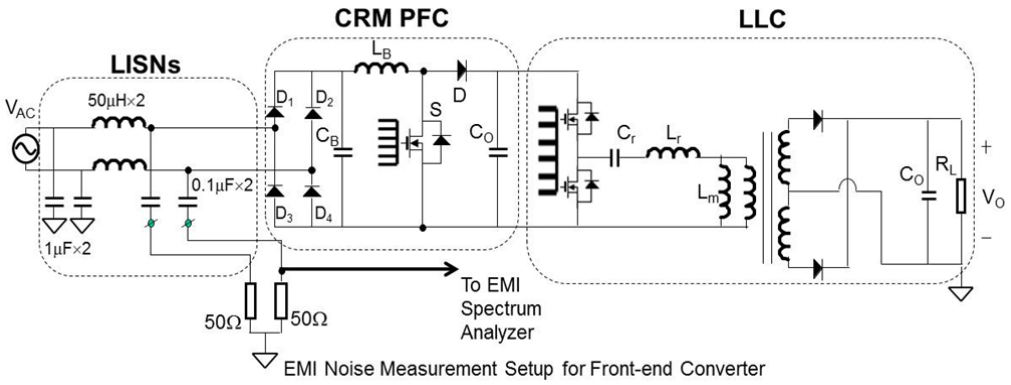
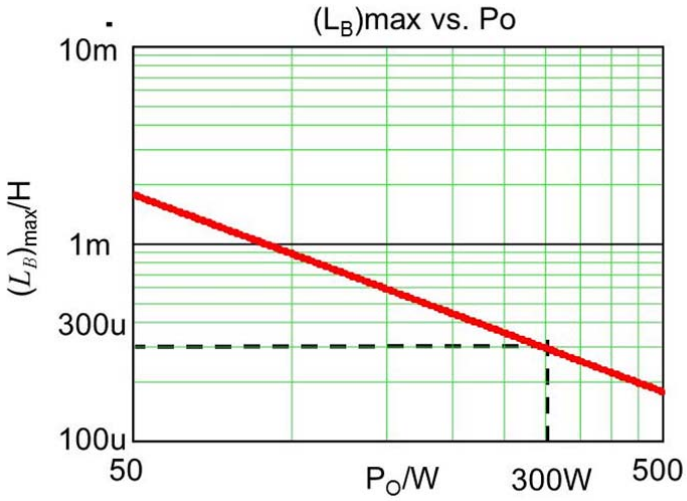


Figure 4-1 EMI test circuit for the offline front-end converter: CRM PFC + LLC

As discussed in previous chapters, the only design parameter for the CRM boost PFC is the boost inductor. So before we start to design the EMI filter for the offline front-end converter, we need first to design the boost inductor for the CRM boost PFC. Figure 4-2 shows the limitation of the max boost inductance for the given full load conditions considering the audible noise issue. As an example, for 300Watts power application, the max boost inductance is 300uH to avoid any audible noise concern. Although we have already got the upper limit for the boost inductance, we cannot determine the selection of the boost inductance because any inductance value below

300uH will be qualified for 300Watts power applications. Figure 4-2 shows the survey of the CRM boost PFC in industry with different power ratings and we can see that the boost inductance range is from 100uH to 1000uH. Therefore the further decision should be dependent on the influence of the inductor on the efficiency and the size of the CRM boost PFC.The specific inductor design procedure needs to be carried out to decide what inductance and inductor to select and use.



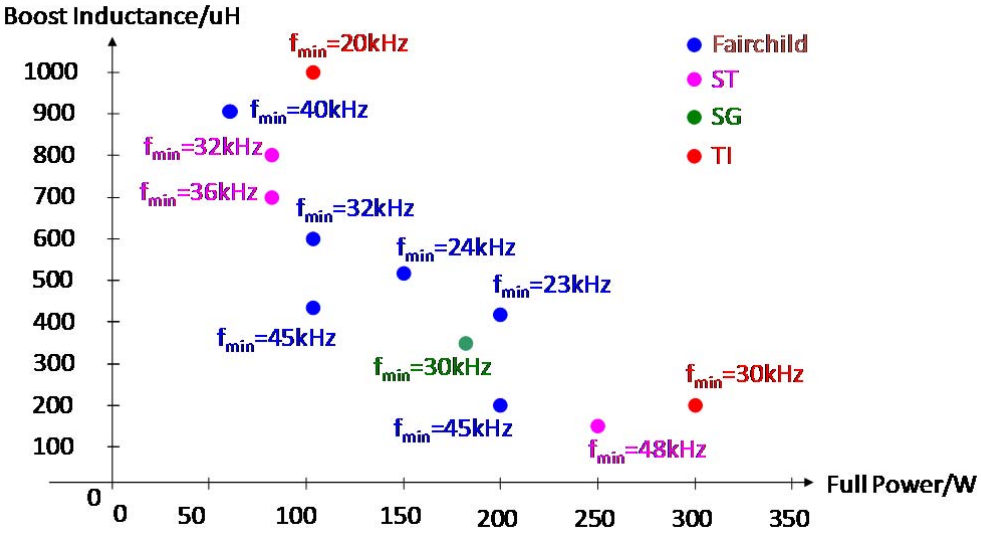


Figure 4-2 Boost inductance survey for CRM PFC in industrial applications

4.1. Boost Inductor Design Preparation for CRM Boost PFC

To design the boost inductor for the CRM boost PFC, first we need to select the core material. Table 4 shows some typical commercialized core material types for different power applications [68]. We can see that for each core material type, there are 3 important indexes, the saturation flux density B_{Sat}, the core loss density and the suitable frequency range. For the CRM boost PFC, the maximum switching frequency increases as load decrease and it can go up to the frequency higher than 1 MHz. However, in typical applications, it is generally limited at 500~600 kHz [69] with the max frequency limit function to avoid too much switching loss. Therefore, the ferrite material should be the suitable material, especially for the Manganese-Zinc Soft Ferrite, which is the low cost, high efficiency choice for inductors designed to operate in the CRM at frequencies above 20kHz, when core loss associated with large flux swing limits the core utilization.

Table 4 Typical Core Materials for Power Applications

Core type	B_{sat}	Relative core loss	Applications
Laminations iron, silicon steel	1.5 - 2.0 T	high	50-60 Hz transformers, inductors
Powdered cores powdered iron, molypermalloy	0.6 - 0.8 T	medium	1 kHz transformers, 100 kHz filter inductors
Ferrite Manganese-zinc, Nickel-zinc	0.25 - 0.5 T	low	20 kHz - 1 MHz transformers, ac inductors

For soft ferrite core material, there are two famous brands, Ferroxcube and EPCOS. Figure 4-3 shows the Ferroxcube ferrite core performance chart with core loss density 500mW/cm^3 at 100 ^{o}C [70] and Figure 4-4 shows the EPCOS ferrite core

performance chart with core loss density 300mW/cm^3 at 100 ^{o}C [71]. From Figure 4-3 we can see that for the frequency range from 20kHz to 500kHz, the 3C96 ferrite material has the highest overall performance factor. And from Figure 4-4 it shows that for the frequency range from 25kHz to 500kHz, the N97 ferrite material has the highest overall performance factor.

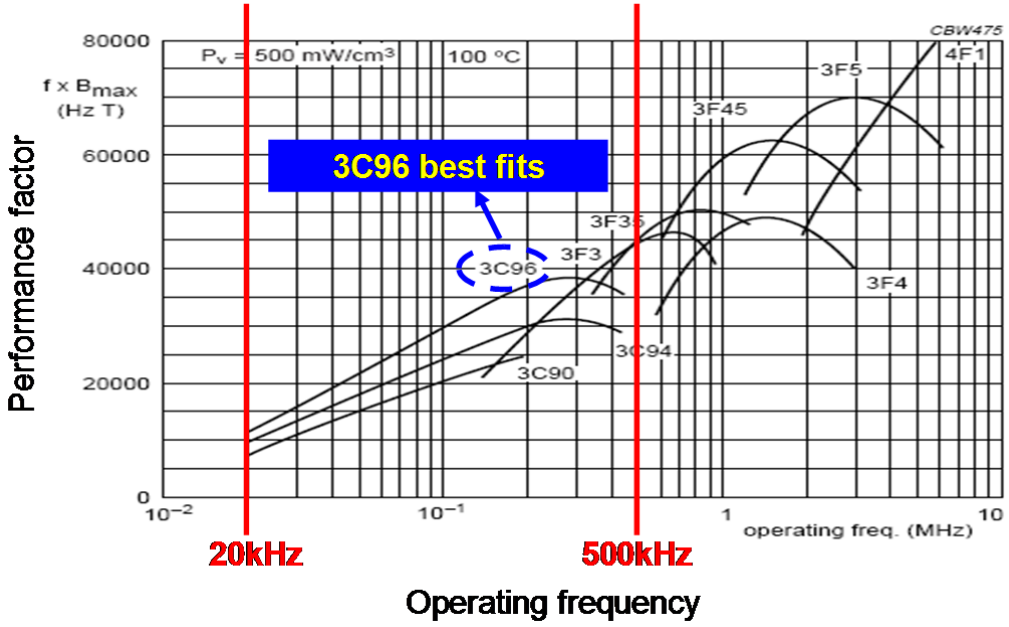


Figure 4-3 FerroxcubeFerrite Core Performance Chart

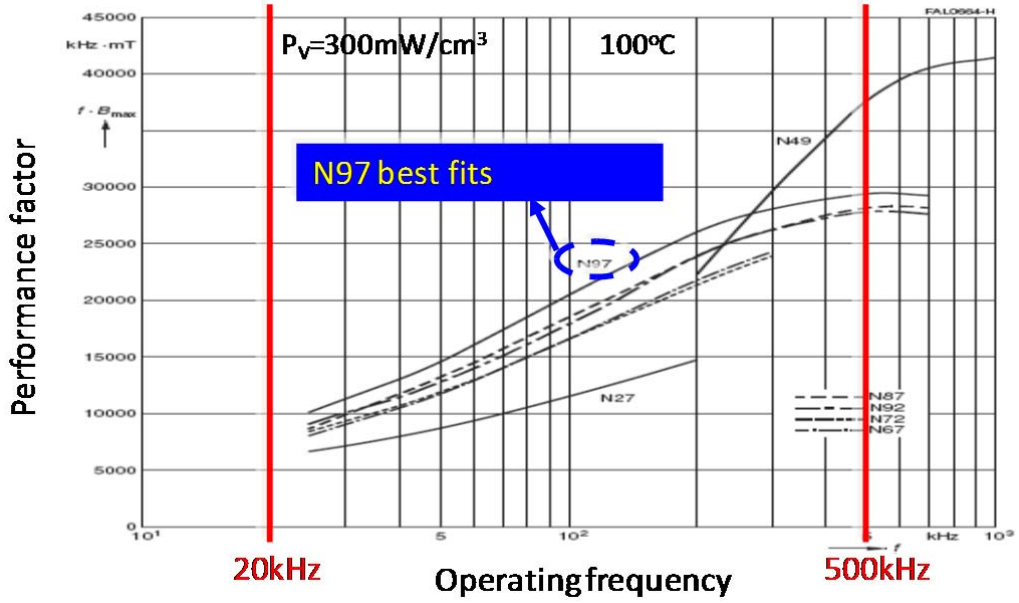


Figure 4-4 EPCOS Ferrite Core Performance Chart

Although from 300 kHz to 500 kHz, 3F3 and N49 ferrite materials has better performance factor than 3C96 and N97, respectively, they will not be qualified at lower frequency with much larger magnetic flux swing. 3F3 and N97 are the balanced choice to get the best overall performance. However, it is hard to compare the performance of 3F3 and N97 since the two performance chart are based on different core loss density, 500mW/cm^3 and 300mW/cm^3, respectively.

To make the fair comparison between 3C96 and N97 ferrite core material, data for the core loss density at the same conditions is necessary. Figure 4-5 and Figure 4-6 show the core loss density characteristics for 3C96 and N97 ferrite material, respectively. Table 5 shows the extracted core loss density data from Figure 4-5 and Figure 4-6, with the same frequency and flux density condition for 3C96 and N97 ferrite material. From Table 5 comparison, we can tell the performance of the N97 is better than 3C96 for the frequency range we are interested in.

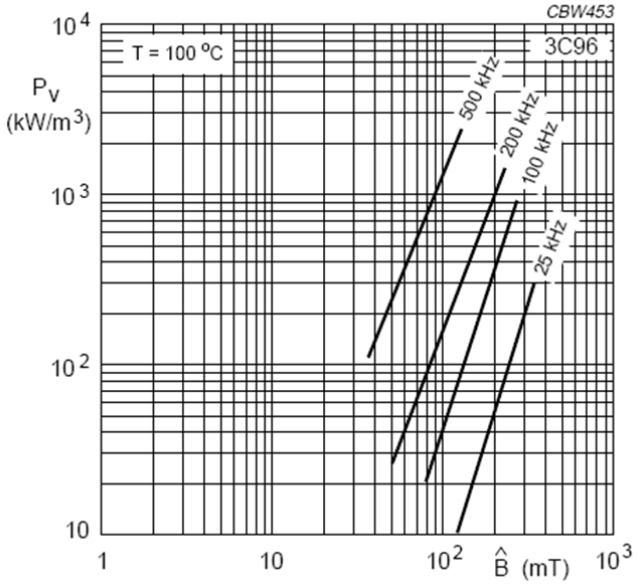


Figure 4-5 3C96 core loss density characteristics

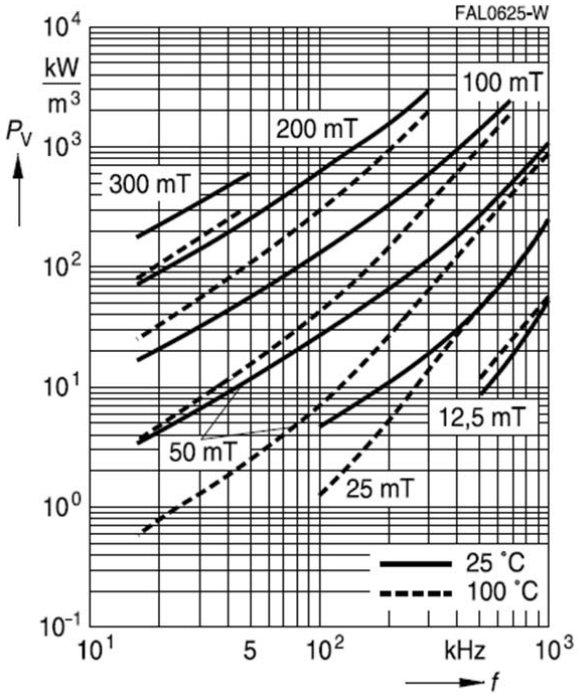


Figure 4-6 N97 core loss density characteristics

Table 5 Core loss density comparison of ferrite core material: 3C96 vs. N97

3C96	N97
$P_V(25kHz,300mT)=200mW/cm^3$	$P_V(25kHz,300mT)=150mW/cm^3$
$P_V(100kHz,100mT)=40mW/cm^3$	$P_V(100kHz,100mT)=40mW/cm^3$
$P_V(100kHz,200mT)=320mW/cm^3$	$P_V(100kHz,200mT)=300mW/cm^3$
$P_V(500kHz,50mT)=250mW/cm^3$	$P_V(500kHz,50mT)=200mW/cm^3$

Therefore we will choose the N97 ferrite core material. After the core material is selected, the next step should be the selection for the core shape and the core size. For 300W PFC power applications, both PQ cores and EFD/ETD cores could be suitable candidates. Generally, PQ cores has much larger effective magnetic cross-sectional

region and thus for given inductance, less turns of windings can be used compared to that of using the EFD/ETD cores, which can help to reduce the AC winding loss. Considering the high switching frequency in the CRM boost PFC, to avoid the ac winding loss, the PQ cores are preferred. Table 6 shows an example of the comparison between the PQ core and the ETD core for a similar power level.

Table 6 Core shape comparison: PQ 32/20 vs. EFD 30/15/9

	PQ 32/20	**EFD 30/15/9**
Mounting Dimensions (L x W x H)	32.3mm x 34.3mm x 20.2mm	34.4mm x 32.5mm x 12.5mm
Ae	154.2mm^2	69mm^2
Ve	7460mm^3	4690mm^3

For further eliminating the AC winding loss, some other measures need to be adopted [72][73]. First, use the litz wire. Second, use small air gap, typically< 1mm, to reduce the loss caused by the fringing effects. Third, design small number of winding layers, typically<=3, to reduce the loss caused by the proximity effects. As shown in Table 6, with the same footprint, the PQ 32/20 has longer window length than that of the EFD 30/15/9, which allows more turns of windings in one layer and help reduce the proximity effects.

Figure 4-7 shows the design results of the inductors with the inductance from 100uH to 300uH as an example. The design is based on the traditional inductor design procedure with max flux density 0.3T and max current density 800A/cm^2, also paying attention to the methods to reduce the AC winding loss. Several iterations are

necessary to finalize the design. And this is the starting point.

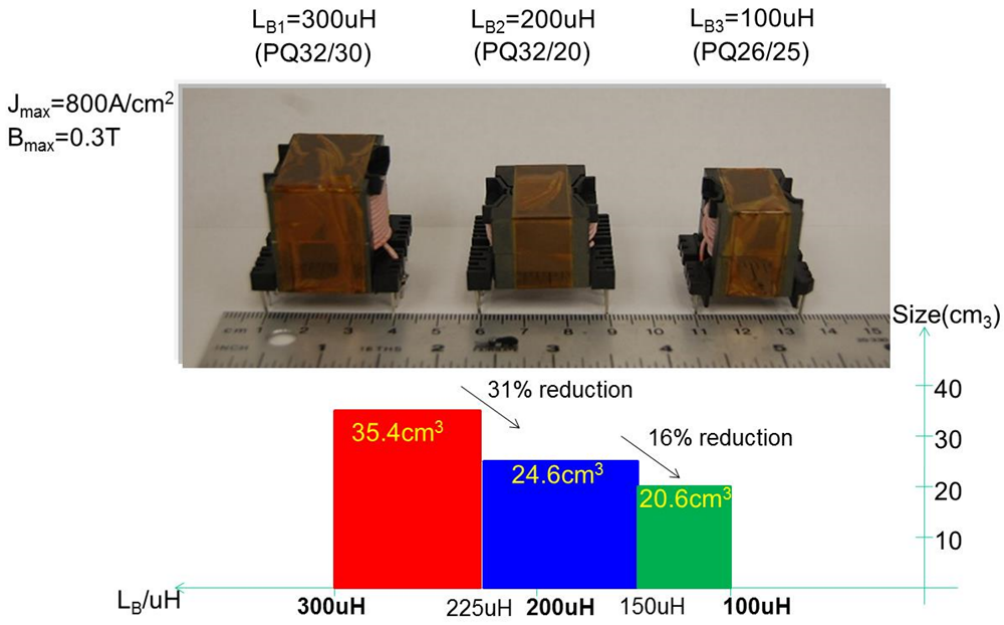


Figure 4-7 size comparison of different boost inductance implementation

4.2. Loss breakdown in the CRM boost PFC

As we have already discussed, the selection of boost inductance for the CRM boost PFC should be a trade-off between the efficiency and the size of the converter. As shown in Figure 4-7, since we have implemented the inductors for different inductance, the other most important part for the concern of the size should be the EMI filter, which can be traced through the previous work, the EMI noise prediction. So before we can go into the EMI filter design optimization, we need to investigate the impact of the boost inductance on the efficiency. A loss breakdown is therefore a necessary step.

Since the reverse recovery related turning on loss can be totally ignored, it will make the prediction of the turning on loss relatively straight-forward. Figure 4-8 shows the power stage of the CRM boost PFC with the zero current detection windings, where the V_{OSS} is the voltage across the parasitic output capacitance of the main switch Q.

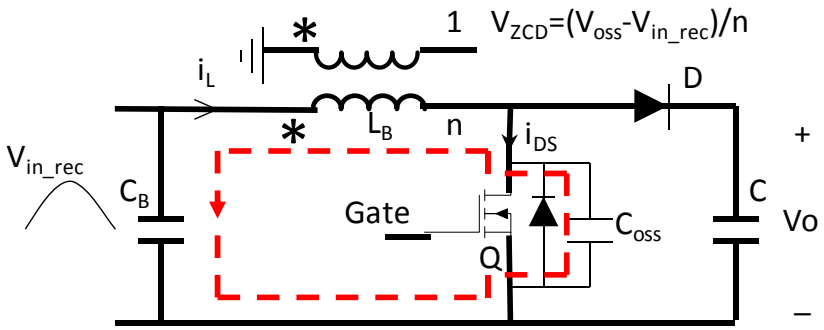


Figure 4-8 CRM boost PFC power stage with the zero current detection

Now the turning on loss is mainly the loss caused by the energy disspition stored in the C_{OSS}. In CRM boost PFC, it utillize the LC resonance to reduce the V_{OSS} before

the turning-on of the main switch Q. Figure 4-9 shows the diagram of this control scheme. From Figure 4-9 we can see that by comparing the zero-current-detection voltage V_{ZCD} with some threshold Vth (Vth = 0 in this case), it will allow some negative inductor current and partial energy stored in the C_{OSS} will be recovered to the input side.When V_{ZCD} = 0, V_{OSS} = Vin_rec, always smaller than the output voltage Vo.

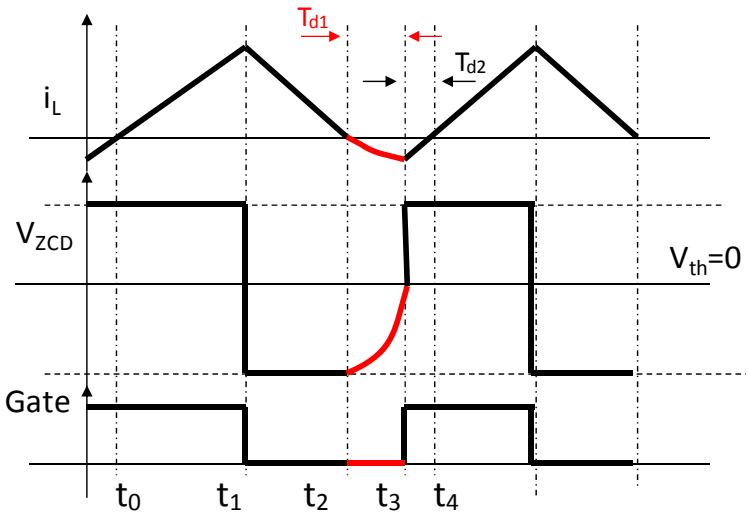


Figure 4-9 Zero current detection control scheme

In Figure 4-9,

$$T_{d1} = \frac{T_R}{4} = \frac{\pi}{2}\sqrt{LC_{oss}} \tag{4-1}$$

And,

$$T_{d2} = \frac{I_{th}}{\left(\frac{V_{in\_rec}(t)}{L}\right)} = \frac{T_R}{2\pi}\frac{V_o - V_{in\_rec}(t)}{V_{in\_rec}(t)} \tag{4-2}$$

Where,

$$T_R = 2\pi\sqrt{L\frac{C_{oss}C_B}{C_{oss}+C_B}} \cong 2\pi\sqrt{LC_{oss}} \tag{4-3}$$

And Ith is the maximum negative inductor current.

In industry practice, a RC delay T_{RC}can be added after the inductor current reaches zero (when V_{ZCD} starts rising up from its negative maximum value, shown as

the time instant t2 in Figure 4-9) to achieve the valley switching. Though the T_{RC}needs to be tuned to get the best performance, roughly it can be estimated as $T_{RC} = T_R/2$. Figure 4-10 shows the vally switching (min V_{OSS} switching) verification test in a CRM boost PFC demo board for both low line and high line conditions.

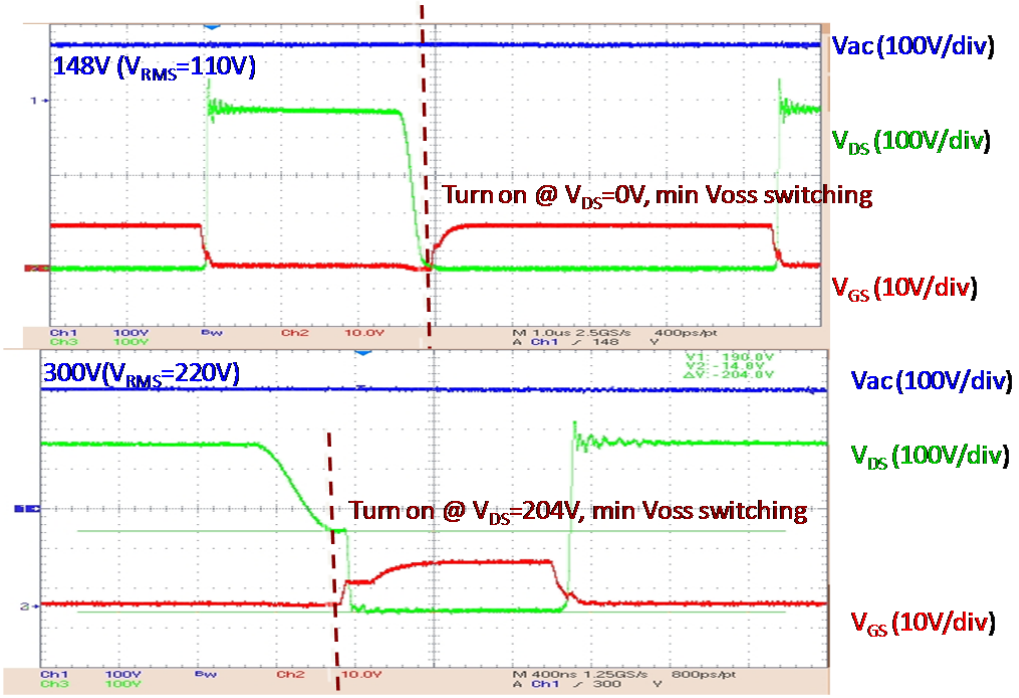


Figure 4-10 Vally switching verification test for CRM boost PFC

Therefore, the average turning on loss in an arbitary switching cycle can be described as,

$$P_{Q\_on\_Ts}(t) = \begin{cases} \frac{1}{2} C_{oss} (2V_{in\_rec}(t) - V_o)^2 f_s(t) & \text{If Vin\_rec(t)>Vo/2} \\ 0 & \text{If Vin\_rec(t)≤Vo/2} \end{cases} \quad (4\text{-}4)$$

Where,

$$f_s(t) = \frac{1}{\frac{2L_B V_o P_{in}}{(V_o - \sqrt{2}V_{in}|\sin(\omega t)|)V_{in}^2} + \frac{T_R}{2}} \quad (4\text{-}5)$$

And then the average turning-on loss in a half line cycle is,

$$P_{Q\_on} = \frac{1}{T_{Halfline}} \int_0^{T_{Halfline}} P_{Q\_on\_Ts}(t)\mathrm{d}t \tag{4-6}$$

For the core loss prediciton, the most famous one is the Steimetz equation [74],

$$\overline{P_v} = k \bullet f^{\alpha} \bullet \hat{B}^{\beta} \tag{4-7}$$

Where,

$\overline{P_v}$ is the time-average core loss per unit volume and $\hat{B}$ is th peak flux density amplitude. And k, α and β are the Steimetz parameters which are abstracted from the core loss density characteristics, such as the examples shown in the Figure 4-6.

The problem with the Steimetz equation is that it is only valid for the sinusoidal excitation. For the core loss prediction with the non-sinusoidal excitation such as the triangular inductor current, there is a lot of academic research. Among them, the generallized Steimetz equation (GSE) and the improved GSE (iGSE) [75] [76] have similar format as the Steimetz equation, straight-forward logic and relatively good accuracy and thus it is often used to predict the core loss in the power converters. For the iGSE, the equation to calculate the core loss is,

$$\overline{P_v} = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{4-8}$$

Where,

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}. \tag{4-9}$$

For N97 core material, k =5.404,α=1.313, β=2.628.

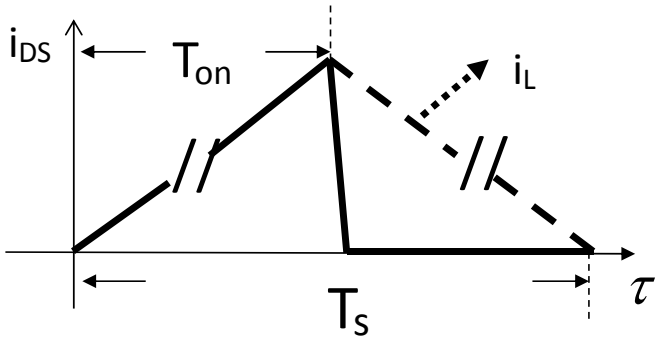


Figure 4-11 Main switch Q drain to source current sketch

For conduction loss, there is mainly the MOSFET conduction loss and the output diode conduction loss and DC winding loss of the boost inductor. Based on the Figure 4-11, the MOSFET drain-to-source current can be written as equation (4-10),

$$i_{DS}(\tau)=\begin{cases}\dfrac{V_{in\_rect}(t)}{L}\tau & 0\le\tau<T_{on}\\ 0 & T_{on}\le\tau<T_s(t)\end{cases} \tag{4-10}$$

In an arbitrary switching cycle, the average MOSFET conduction loss is,

$$P_{Q\_Ts}(t)=\frac{1}{T_s(t)}\int_0^{T_{on}} i_{DS}^2(\tau)R_{ds(on)}d\tau \tag{4-11}$$

In a half line cycle, the average MOSFET conduction loss is,

$$P_{Q\_T_p}=\frac{1}{T_p}\left(\sum_{k=1}^{n}\left(P_{Q\_T_s}\right)_k T_{sk}\right)^{T_{sk}\to dt}\approx\frac{1}{T_p}\int_0^{T_p}P_{Q\_T_s}^2(t)dt=\frac{2P_{in}}{\sqrt{3}V_{in}}\sqrt{1-\frac{8\sqrt{2}V_{in}}{3\pi V_o}}R_{ds(on)} \tag{4-12}$$

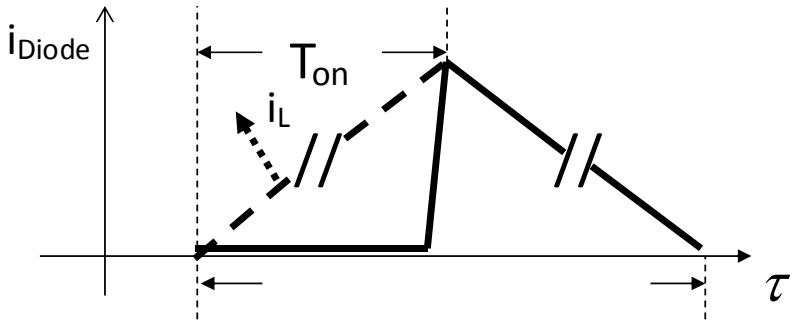


Figure 4-12 Output diode current sketch

In a similar way, based on the Figure 4-12, in an arbitary switching cycle, the output diode conduction losscan be written as equation (4-13),

$$P_{D\_Ts}(t) = \frac{1}{T_s(t)} \int_{Ton}^{T_s(t)} i_{Diode}(\tau) \times V_F(i_{Diode}(\tau)) d\tau \tag{4-13}$$

Where, V_F is the diode forward voltage which can be expressed as the function of the diode forward current through curve fitting.

For other loss such as the diode bridge conduction loss, the loss on the sensing resistor and the driving loss, it is more straightforward. Based on the loss prediction, the efficiency can be calculated and predicted. Figure 4-13 shows the components selection for the 250W CRM boost PFC demo board from STMicroelectronics. The Rsense is for the over current protection purpose and is chosen 165mOhms in this demo board which means the maximum allowable current is 7.3A. With these selected components, the efficiency can be predicted as shown in Figure 4-18. From Figure 4-14 we can see that the predicted efficiency matches the measured efficiency pretty well especially at high line voltage. It is because at low line conditions, the ripple inductor current is much higher, which induces higher AC winding loss that is difficult to predict and not considered in this dissertation. However, it should be good

enough to pre-select the boost inductance for high line applications.

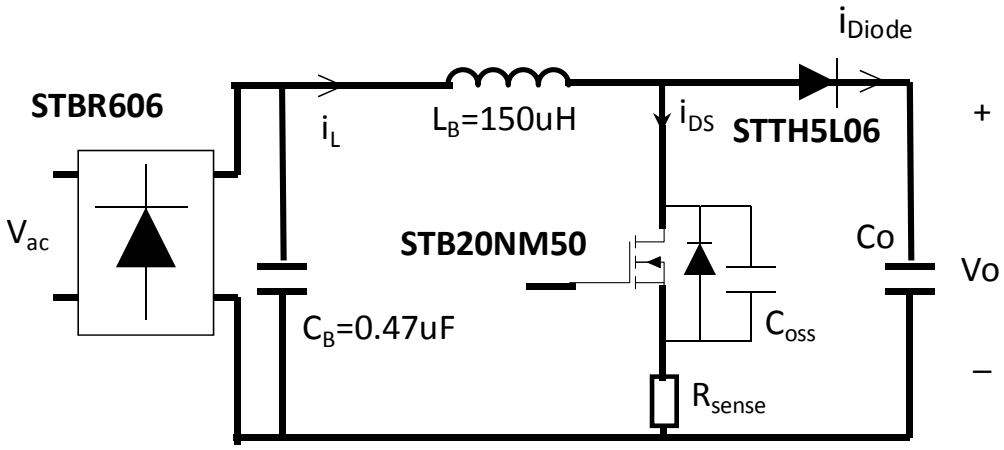


Figure 4-13 Components for demo board from STMicroelectronics

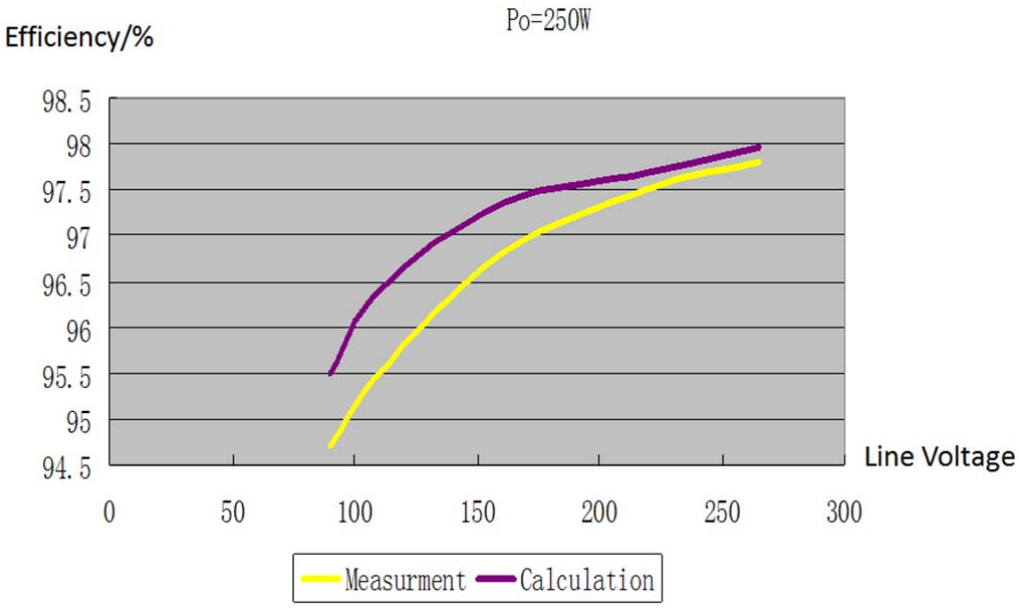


Figure 4-14 Efficiency vs. line voltage for 250W CRM boost PFC demo board

By using the 3 inductors designed in Figure 4-7, the loss breakdown comparison can be carried out among the inductance of 100uH, 200uH and 300uH. Figure 4-15 shows the final results @ $230V_{RMS}$ and 300Watts power. From Figure 4-15 we can see

that, the boost inductance has negligible impacts on the conduction loss as circled in the blue dash lines. And as circled in the red dashed lines, although the boost inductance has impacts on the switching loss, the percentage of the switching loss over the total loss is small and thus the impacts are not important. Here an emphasis should be placed on the turning off loss. For CRM boost PFC, since the turning on loss of the main switch is greatly reduced due to the valley switching, the trade-off often requires using MOSFETs with larger Coss and smaller Rds(on) to balance the switching loss and the conduction loss. With largerCoss, it acts as an efficient snubber and the delay between the V_{DS} increasing and the i_{DS} decreasing is enlarged. Therefore there is less overlap between the V_{DS} and i_{DS} and thus the turning off loss is greatly reduced. This mechanism is explained in [77]. Further details can be referred to [78] and [79].

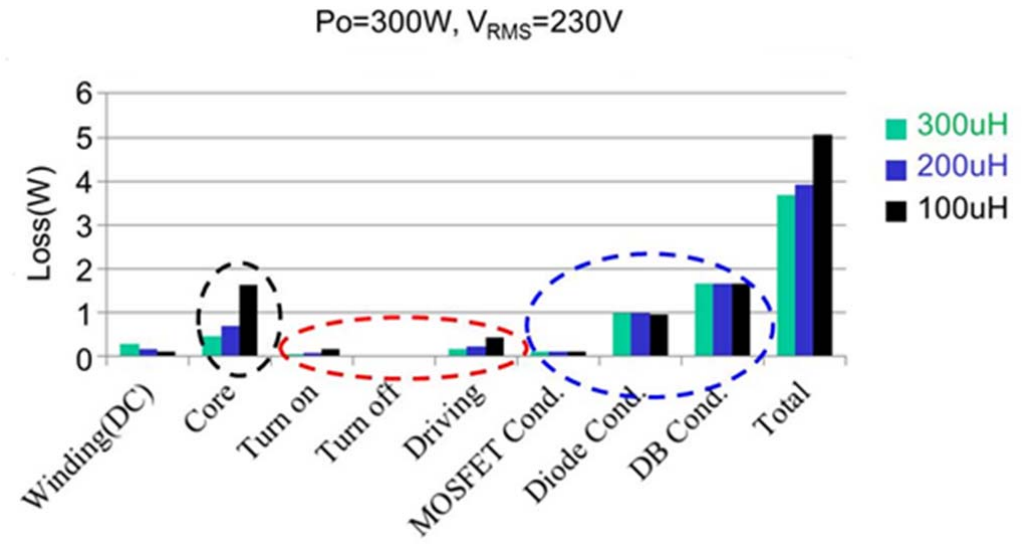


Figure 4-15 loss breakdown comparison of different boost inductance implementation

And so the most dominating factor will be the core loss. While the 100uH inductor has the smallest physical size, its core loss is greatly increased due to the

large flux swing. Meantime, according to the redrawn worst corner frequency vs. Boost inductance in Figure 4-16, the 100uH Boost inductance also means larger DM EMI filter size, which indicates that the total solution size is not necessarily minimized. Comparatively speaking, the 200uH inductor has smaller physical size than that of 300uH but carry out similar total loss. Therefore 200uH is chosen as the first trial of the boost inductance with the total size and efficiency trade-off.

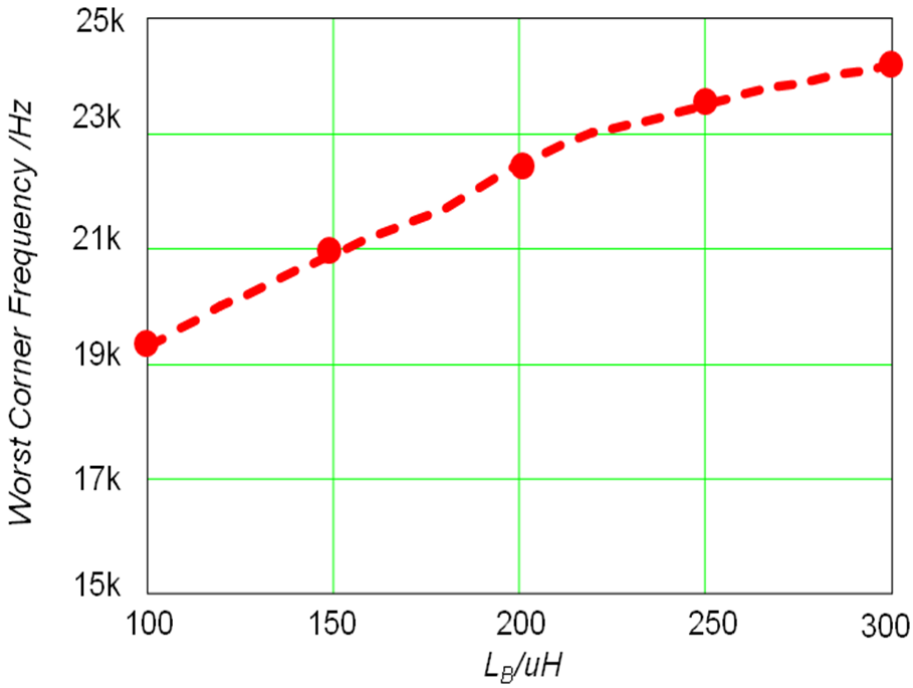


Figure 4-16 Worst corner frequency vs. boost inductance

4.3. EMI filter design based on noise prediction

As shown in Figure 4-16, for 200uH inductance, the corner frequency of the DM EMI filter for the worst case DM EMI noise should be 22kHz, considering using the 2nd stage DM EMI filter, which is based on the noise @120V_{RMS} and 110W.

However, the detailed DM inductance and capacitance value are not be able to be determined with only the corner frequency. Another limit is the maximum DM capacitance which has detrimental effects on the power factor.

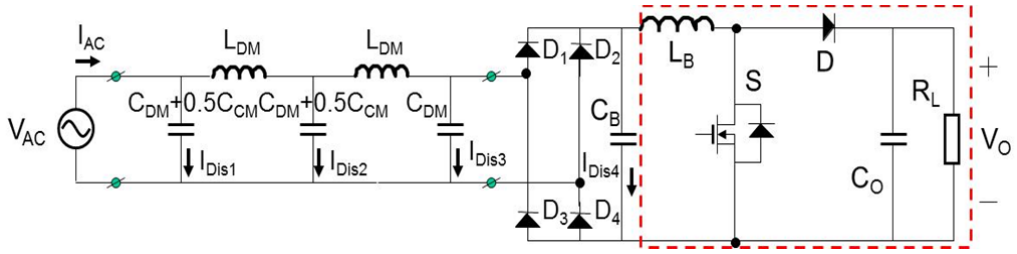


Figure 4-17 PFC power stage with DM EMI filter

As shown in Figure 4-17, DM capacitor will draw displacement current $I_{Dis}$from the input source, cause phase angle $\boldsymbol{\theta}$ between I_{AC} and V_{AC} and degrade the power factor. For line frequency input current with the frequency as low as 120Hz, Figure 4-17 could be simplified as in Figure 4-18.

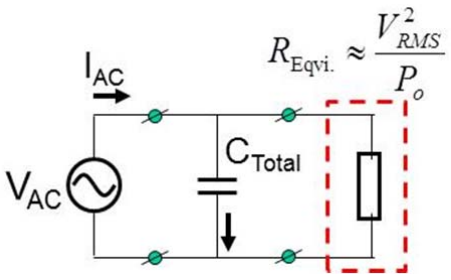


Figure 4-18 Simplification of Figure 4-17

Then the maximum total DM capacitorance could be calculated as,

$$C_{Total} = \frac{\tan[\arccos(pf \cdot \sqrt{1+\mathrm{THD}^2})]}{\omega R_{Equi}} \approx \frac{\tan[\arccos(pf \cdot \sqrt{1+\mathrm{THD}^2})]}{\omega} \frac{P_o}{V_{RMS}^2} \quad (4\text{-}14)$$

Where, the pf is the power factor and the THD is the input current distortion.

Table 7 shows the Power Factor requirement from the energy star [80].

Table 7 Energy start power factor requirement

Energy Star(ENERGY STAR® Program Requirements for Computer Servers):

Power Supply Type	Rated Output Power	10% Load	20% Load	50% Load	100% Load
Dc-Dc (All)	All Output Ratings	N/A	N/A	N/A	N/A
Ac-Dc Multi-output	All Output Ratings	N/A	0.80	0.90	0.95
Ac-Dc Single-output	Output Rating ≤ 500 W	N/A	0.80	0.90	0.95
	Output Rating > 500 W and Output Rating ≤ 1,000 W	0.65	0.80	0.90	0.95
	Output Rating > 1,000 watts	0.80	0.90	0.90	0.95

And for 80plus, its platinum requirement for power factor is 95% @ 50% load. So the power factor for spec. for 300W front-end converter is organized in Table 8.

Table 8 Power factor specification for 300W server application

Power Rating 300W		10% Load	20% Load	50% load	100% load
Power Factor	Energy Star	N/A	80%	90%	95%
	80plus	N/A	N/A	95%	N/A

The THD of the 300W CRM PFC could be simulated and the results are shown in

Table 9.

Table 9 simulated THD for 300W CRM PFC at different loads

Power Rating 300W		10% Load	20% Load	50% load	100% load
THD	230Vrms	27.26%	12.82%	4.92%	1.74%

With the data gathered from Table 8 and Table 9, the max total DM capacitance could be calculated and the results are shown in Table 10.

Table 10 maximum total DM capacitance at different loads

Power Rating 300W		10% Load	20% Load	50% load	100% load
Maximum C_{Total}	Energy Star	N/A	2.2uF	3.62uF	4.94uF
	80plus	N/A	N/A	2.44uF	N/A

Thus the maximum selectable total DM inductance should be below 2.2uF.

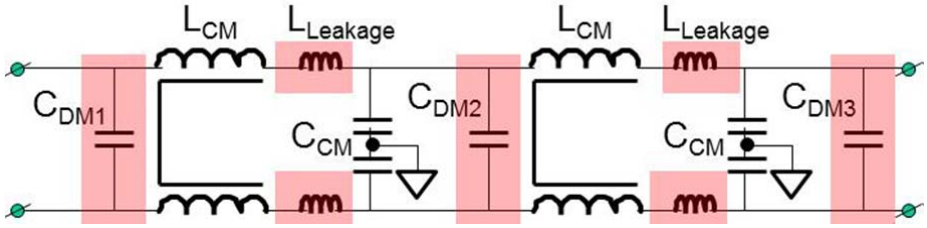


Figure 4-19 Two-stage EMI filter with leakage of CM choke as DM inductor

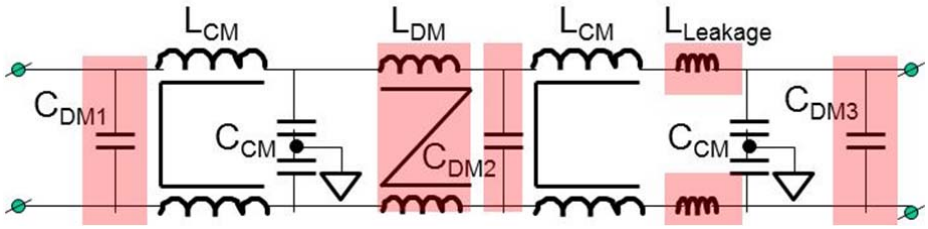


Figure 4-20 Two-stage EMI filter with both leakage and discrete DM choke

After the maximum selectable total DM inductance is determined, the EMI filter structure need to be selected. Figure 4-19 and 4-20 show the most popular two types of EMI filter structure. The first one has the merit of utilizing the leakage inductance of the CM choke as the DM inductor, which could minimize the size of the EMI filter. However, for large DM inductance, it may require larger CM inductance than required by the CM EMI noise attenuation, which will increase the size of the CM choke and weaken the effect of the size reduction. Another concern is that leaked flux might be coupled with other filter components and cause detrimental effects on the filter performance, especially for high frequency noise [81]. Thus, the second type of EMI filter structure is also often seen, with the balance of filter size reduction and better high frequency noise attenuation. The selection of the structure is really dependent on the specific DM and CM EMI noise.

However, from the DM noise prediction results, the required DM inductance could be calculated. For C_{DM1}=C_{DM2}=0.68uF and C_{DM3} = 0.68uF + 0.15uF(CRM PFC input capacitor) = 0.83uF (total DM capacitance 2.19uF), the required DM inductance per stage is 30uH, which might require the CM choke with the inductance ranging from 3-6mH (considering 5~10% leakage inductance).

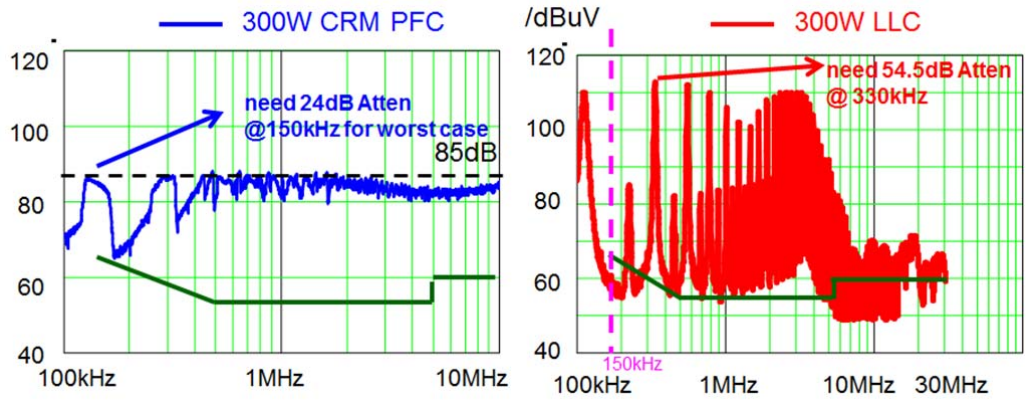


Figure 4-21 CM noise spectrum of 300W CRM PFC and LLC

Now we should put CM EMI noise into consideration.

From Figure 4-21 it is seen that for two stage CM EMI filter, the CRM PFC require the corner frequency of 87kHz while the LLC require the corner frequency of 69kHz due to its much higher noise magnitude. Thus the CM EMI filter should be designed based on the LLC CM EMI noise.

For CM EMI filter design, there is similar dilemma as in DM EMI filter. The maximum CM capacitance should be selected first. Table 11 shows the maximum leakage current required for the IT equipment by IEC60950-1 [82]. Based on the 0.75mA maximum leakage current, the maximum total CM capacitance should be below 9.55nF.

Table 11 Leakage current requirement by IEC60950-1

Max leakage current requirement
IEC-60950-1 (IT Equipment)

Subjects		IEC60950-1
Leakage current	CLASS I	Handheld:**0.75mA**
		Others: 3.5mA
	CLASS II	0.25mA

Figure 4-22 shows the simplified CM EMI filter schematic. Since total CM capacitance should be below 9.55nF, C_Y=2.2nF could be selected. And based on the LLC CM noise, the required CM inductance would be 2.6mH per stage.

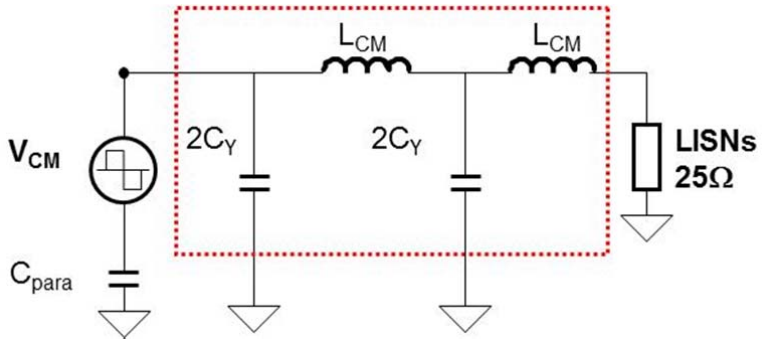


Figure 4-22 Simplified Equivalent CM EMI Filter Schematic

However, considering using leakage inductance as the DM inductance, 2x 3.3mH CM chokes are implemented, which have 30.9uH and 30.3uH leakage inductance, respectively, by measurement.

Figure 4-23 shows the test results with the designed EMI filter. The worst case is at $120V_{RMS}$, 113W by measurement. By previous prediction, it is at $120V_{RMS}$, 110W.The EMI filter is designed based on the DM quasi-peak EMI noise prediction without considering any margin. The filtered quasi-peak noise @ 150 kHz is 64.3dB, 1.6dB below the standard, which further prove the validity of the mathematical model and the noise prediction. However, we do see there is a bump on the filtered average noise around 390kHz, which is a little above the average standard (1dB). It is due to the CM filter is designed based on the measured LLC peak noise as shown in Figure 4-21, but not the average noise. The average CM EMI noise of the LLC converter should be used to determine the noise attenuation.

Figure 4-24 shows the test results using the type II EMI filter with the discrete DM EMI choke. Because the designed filter parameters are almost exactly the same, the measured EMI spectrum is almost exactly the same as previous test results. Bifilar

winding technique is used to reduce the leakage inductance of the CM mode choke and there is no noticeable size reduction. However, the DM choke require around 6.5 cm^3 extra size, shown as in Figure 4-25.

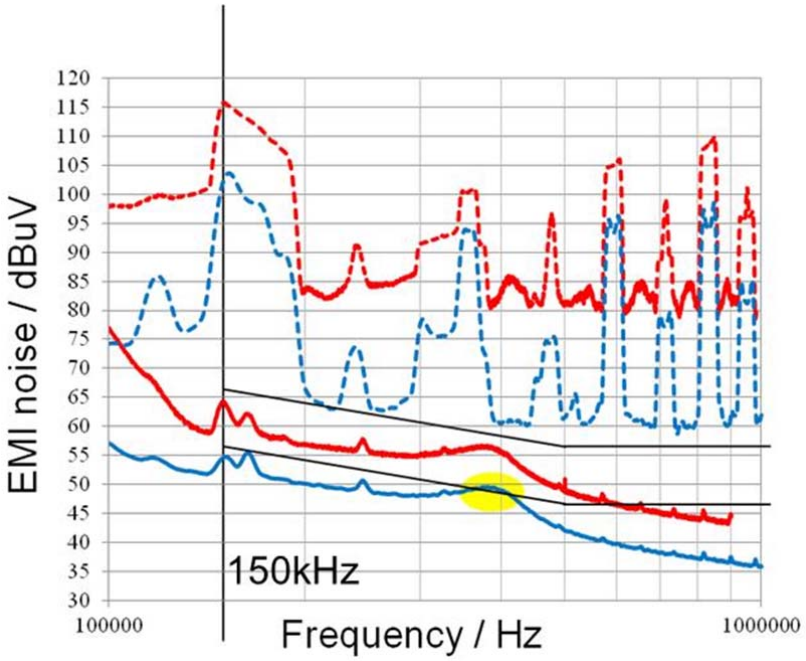


Figure 4-23 EMI noise measurements with and without EMI filter

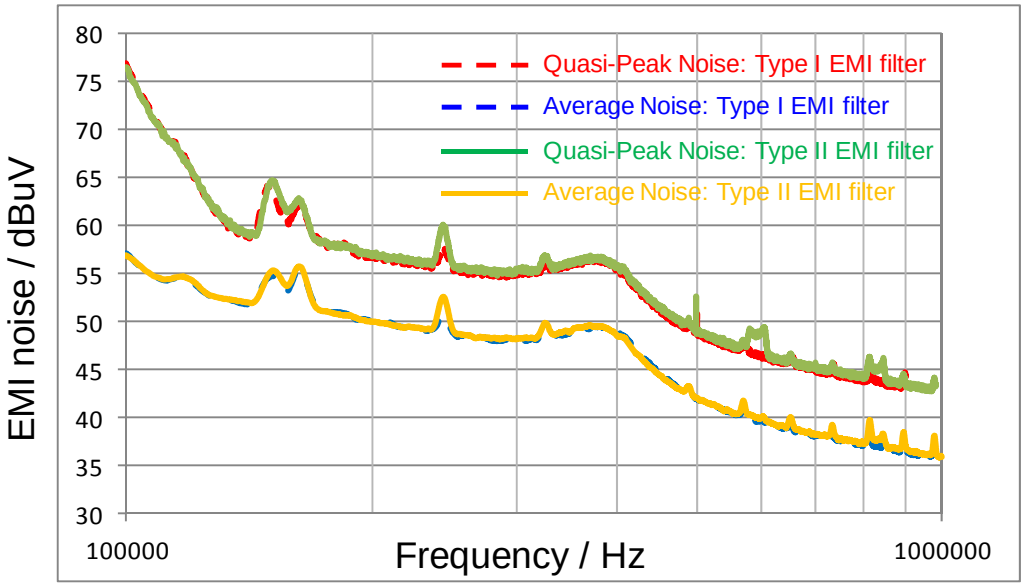


Figure 4-24 EMI noise comparison between type I and type II EMI filter

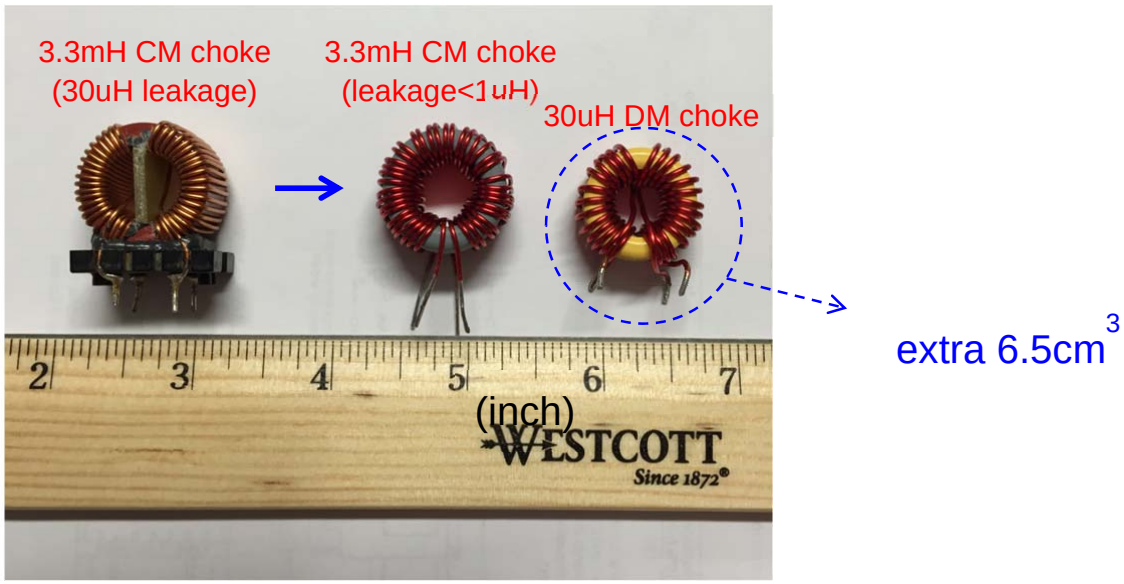


Figure 4-25 size comparison: Type I EMI filter vs. Type II EMI filter

For Type I EMI filter, because the DM inductance is free by using the leakage inductance of the CM choke, choosing a larger boost inductance will not reduce the EMI filter size. However, for Type II EMI filter, the DM choke can be reduced from 6.5cm^3 to 2.7cm^3, with the calculated DM choke inductance reduced from 30uH to 12uH, shown as in Figure 4-26.

Figure 4-26 Type II EMI filter size comparison: L_B = 200nH vs. L_B = 300uH

Size of 3.8cm^3 is saved by using 300uH boost inductor. However, the size of the 300uH boost inductor is 10.8cm3 larger than that of 200uH boost inductor. Therefore, a total size of 7cm^3 can be saved with selecting 200uH as the boost inductance.

Figure 4-27 shows the test results using the designed Type II EMI filter at L_B=300uH. Again, the designed EMI filter based on the predicted EMI noise spectrum can accurately filter out the noise and make it meet the EMI standard as verified in previous case.

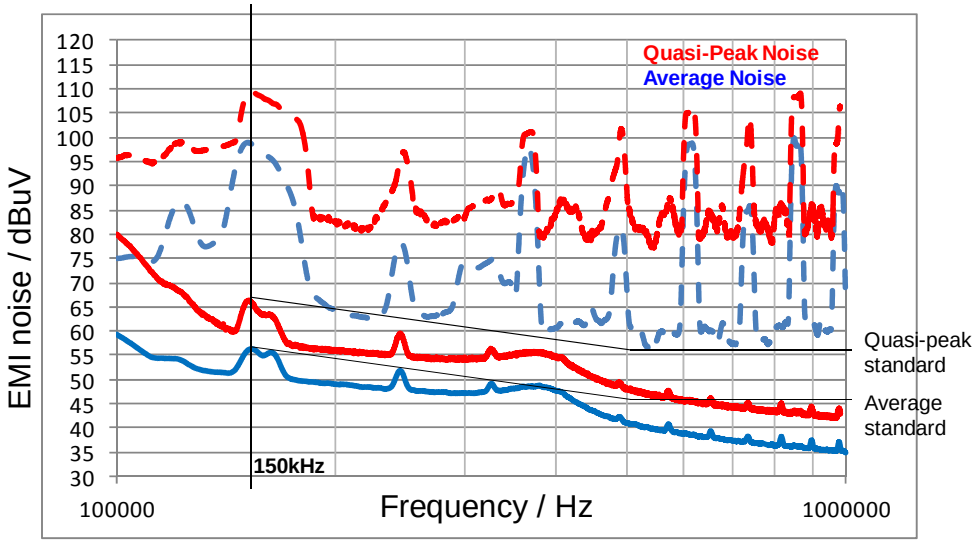


Figure 4-27 EMI noise measurements with and without EMI filter at L_B=300uH

Chapter 5. SUMMARY AND FUTURE WORK

In this dissertation, an approximate mathematical model is proposed to calculate the DM quasi-peak EMI noise for the CRM Boost PFC. Based on the predicted noise spectrum, worst case analysis is carried out to discover the worst case of the EMI performance for CRM boost PFC with different line and load conditions. Design criteria of the DM EMI filter related to the selection of the boost inductance is abstracted. Such design criteria can help to optimize the design of the boost inductor and the EMI filter at the very beginning of the prototype stage for the offline front-end converters.

The measurement of the quasi-peak EMI noise is a rather complex process and in order to be able to predict the noise spectrum, the measuring procedure is well investigated and the main functions of the spectrum analyzer are abstracted and simplified. For the noise source, the harmonic components of the inductor ripple current are analyzed based on the quasi steady state approximation, which enables the utilization of the Fourier transformation. This ignores the frequency modulation effect on the inductor ripple current and will cause some error. However, the comparison between the calculated noise and measurement results shows the good accuracy and the validity of this approximate model on evaluating the EMI performance. In this dissertation, this method is specifically applied to the single channel and interleaved CRM boost PFC with different line and load conditions, and some useful EMI filter design criteria are obtained.

One major limitation of this mathematical model, based on the experimental verification results, is that it can only accurately predict the EMI noise up to around 1 MHz. For CRM Boost PFC with switching frequency below 1MHz, this seems good enough to guide the EMI filter design and facilitate the process of the passive components selection. However, with the emerging of the GaN devices, CRM PFC with multi-MHz switching frequency for high efficiency, high power density applications is gradually taking the trend [83]. How to extend the methodology in this dissertation to higher frequency range will be a very challenging topic. In [84], negative resonant current is included in the noise source calculation, which can help improve the noise prediction accuracy for CRM PFC with MHz switching frequency. In [85], the transition from CM EMI noise to DM EMI noise reveals the importance of the high frequency model for the diode bridge, which cannot just be seen as a short path at low frequency operation. Same rule applies to the boost inductor, the LISNs and so on so forth. Parasitics of all those components along the EMI noise propagation path need to be carefully tackled to get some useful and reasonable results.

Besides the quasi-peak EMI noise measurement, which is targeted in this dissertation, the average EMI noise measurement is another interesting topic. Actually in many automotive applications, the average EMI noise standard is so stringent that the spread spectrum technology [86] is adopted to reduce the average EMI noise and make the converter pass the regulation. In that case, similar methodology developed in this dissertation can be utilized to evaluate the average EMI noise spectrum, to find the worst case scenario and to compare the effectiveness of different spread spectrum technology.

An even more challenging topic will be extending the methodology on DM EMI noise to the CM EMI noise, where its performance is dominated by the parasitic capacitance even at very low frequency range (~kHz) and is very difficult to predict accurately. 3D simulation tool might be necessary to abstract those parasitic values but then it will damage the merit of the simplicity of such mathematical model. However, a good trade-off to balance the calculation speed and the accuracy is worth to be investigated.

At last, as an easier task, to apply the optimized EMI filter design procedure to the interleaved CRM Boost PFC and prove its validity will be the potential future work. Actually in [87] some good research work has been already done, which shows the extendibility of proposed methodology.

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