CHAPTER IV

PROCESSING AND CHARACTERIZATION OF MODULE TO HEATSPREADER INTERFACE

4.1 INTRODUCTION

To successfully implement a packaging concept, it is imperative to resolve many challenging issues related to materials and processing, which will result in improved thermal management of the power electronics modules. Almost every parameter of a power device is a function of temperature. The heat generated by these active devices, which reduces circuit efficiency, may also degrade circuit performance or cause the circuit to fail prematurely. Therefore, packaging engineers must design the mechanical assembly to address the trade-offs of efficiency, reliability and, cost versus thermal performance. In high-power electronics modules, the heat generated by the power devices is transferred to the ambient environment by attaching a heat spreader to the semiconductor package. Once the heat spreader is selected, it has to be attached optimally to the semiconductor package to ensure efficient thermal management through the thermal interface. In most power electronics modules, solder or thermally conductive epoxy is used to eliminate the air gaps by conforming to surface irregularities; however, these bonding agents introduce interfaces and/or interlayers of finite thickness. While strong interfaces are necessary to ensure mechanical integrity of the bonded components, they are responsible for lowering the electrical and thermal conductivities of the assemblage. Thermal resistance of the joint is directly proportional to the interface thickness and inversely proportional to the thermal conductivity of the interface material as well as to the area of the heat transfer. Moreover, these layers are quite non-uniform and consist of voids, which introduces anomalous thermal spreading.

In this part of the research, interfacial thermal resistance of a few common attachment materials (solder and thermally conductive epoxy with conductivity as high as 60W/m-K) between the power module and the heat spreader are characterized. Processing parameters such as applied pressure and environment of the solder reflow and epoxy curing are varied to fabricate test samples for subsequent comparison of the resulting interfaces. Typical attachment materials introduce interfaces and/or interlayers of finite thickness. Acoustic micrography imaging, a non-destructive evaluation tool, is employed to identify the non-uniformity of the interface layers. Scanning acoustic microscopes (SAMs) use an ultrasonic transducer that emits a sound wave through the material being tested. The wave travels through the material, and gets reflected when it strikes interfaces within the material. These reflections are digitally displayed in an image, which allows us to visualize as well as quantize the discontinuities in the sample. Using a scanning acoustic microscope (SAM), a non-destructive inspection tool, we have detected cracks, voiding, coplanarity, and delamination in the interface layer, which correlate to the measured thermal resistance of an interface. This investigation has resulted in optimizing the bonding process of the selected interface material, minimizing the void-content to ensure enhanced thermal management of power modules. Investigating the microstructures of the interfaces would allow us to establish a structure-property relationship of the interface material, leading towards tailoring the bonding process of the interface material for the module to heat-spreader attachment, with a minimized void-fraction to ensure improved thermal management of power modules.

4.1.1 Importance of Thermal Management of Power Modules via Baseplate Attachment

Continuing miniaturization, rising switching frequencies and increasing packaging densities have been the trends for improved performance of electronic components at low cost. In many different application fields

this evolution has led to extremely high loss power densities. The gradual increase of thermal dissipation in a package is depicted for three examples (microprocessors, insulated gate bipolar transistors (IGBT) and solid state lasers) in Figure 4.1.1. A microprocessor in 1990 typically dissipated a loss power no more than 3 W on a chip size of one square centimeter. Nowadays Pentium microprocessors produce a loss power up to 50 W on a chip with about two square centimeters. The rapid development of insolated bipolar field-effect transistors for motor control units has led to loss power densities of about 100 W/cm^2 still showing a slightly increasing tendency. From an electrical design point of view, traditional power modules are normally quite simple; however, these modules are often extremely difficult to fabricate due to high voltages and large currents, resulting in critical thermal management considerations[1,2,3]. High power levels of power electronic modules require thermal management techniques involving large capacity heat spreaders, external cooling mechanism (e.g. airflow) and careful management of interfacial thermal resistance.

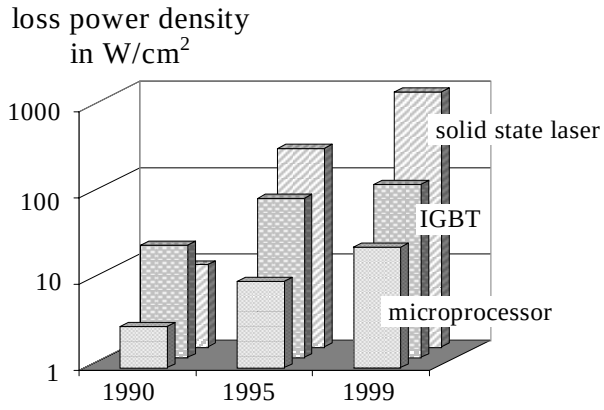


Figure 4.1.1. Increase of loss power density in the last decade in electronic packages[4]

In order to optimize the device/module performance, the operating temperatures have to kept within acceptable range with a well designed thermal management protocol. In most practical applications, the heat generated by the power devices is transferred to the ambient environment. Attaching a heat spreader to the semiconductor package surface facilitates the heat transfer process between the devices and the surrounding environment. Moreover, GE researchers have investigated solder fatigue problem associated with power die attachment with three different types of structures – die on heat sink, die on a BeO substrate attached to a heat sink and die with a BeO substrate attached to a copper base plate, which is then placed on the heat sink. Addition of the copper baseplate between the module and the heatsink significantly improved the thermal fatigue life when exposed to extensive thermal cycling of the structures[5,6]. Significant amount of research has been reported over the years in selecting an optimum heat spreader for specific applications[2,3,7,8,9,10,11,12].

A copper baseplate is by far the most common heat spreader material for power modules due to its high thermal conductivity, easy mechanical handling, galvanic plating, amenability and moderate pricing. However, the CTE mismatch between copper and Si is the primary disadvantage of using a copper baseplate. Consequently, the interface between the substrate and heat spreader is one of the primary failure sources of a power module. The CTE mismatch between the substrate and heat spreader generates a significant amount of thermal stress and mechanical strain on the attachment layer, which is typically made of solder. This situation aggravates under high power cycling and results in crack initiation and increased thermal resistance between chip and the heat spreader. Eupec GmbH has introduced a machined bow in the copper baseplate to match the bowing of the substrate-baseplate system at elevated temperatures. However, a bowed baseplate would require a bowed heat sink in real application, which may not be cost effective.

Over the years, to improve reliability of power modules, researchers have investigated alternative materials to replace the conventional copper baseplate. The most common alternatives are aluminum and copper based metal matrix composites (MMCs)[11,13,14]. While copper/graphite MMCs are very promising as heatspreader materials, to date, they are underdeveloped and not commercially available[11,15]. Researchers at

Lanxide have manufactured AlSiC plates as heatspreader materials[8]. AlSiC baseplates provided better thermal cycling results since the CTE of AlSiC is more closely matched to silicon. However, in-house testing at Lanxide has shown that the engineered baseplates exhibit higher thermal resistance compared to copper baseplates. In addition to high manufacturing cost of AlSiC, the baseplates were plated with nickel and silver to create a solderable surface for subsequent bonding to the module substrate, which added more steps in manufacturing, resulting in higher cost of baseplate fabrication. Furthermore, attachment of an AlSiC heat spreader would be realized only with an epoxy system, which are typically less thermally conductive than eutectic Pb-Sn solder.

Researchers have developed Cu-Mo-Cu and Cu-W-Cu cold-formed sheets to minimize the CTE mismatch problem; however, the manufacturing costs of these tailored materials are significantly higher than that of copper[16]. Structured copper in the form of close-packed individual strands of copper to provide a compliant interface has been used in an experimental basis by GE researchers[5]. While structured copper has a very close match to bulk copper's thermal conductivity, the biggest disadvantage includes an expensive process of manufacturing structured copper. Harris researchers have implemented a low-cost, formable copper-sponge baseplate in the PEBB module version 1.5[2]. However, the natural thermal conductivity of the designed baseplate is not high; moreover, additional processing steps are required to achieve solderable top surface for attachment to the module substrate.

At the present time, alternative solutions to copper baseplate are significantly more expensive and in a cost-driven market of power electronics modules, it is unlikely that expensive baseplate materials such as AlSiC would readily replace the conventional low-cost copper plate. Consequently, in this research, we have selected copper as the heat spreader material and have sought improvements in thermal performance of the attached layers via interface engineering.

4.1.2 Significance of Interface Engineering of the Heatspreader Attachment Process

In most practical thermal management protocols, the heat generated by the power devices is transferred to the ambient environment by attaching a heat spreader to the semiconductor package surface[7,8,9]. Attachment of a heat spreader to a package requires that two solid surfaces be brought together into intimate contact. Unfortunately, solid surfaces are never completely flat or smooth enough to provide a perfect thermal contact. All surfaces have microscopic roughness as well as macroscopic non-planarity. In most cases, as two surfaces are brought together, less than one percent of the surfaces make physical contact while as much as 99% of the surfaces are separated by a thin layer of interstitial air[17]. Although some heat is conducted through the contact points, which are physically connected, most of the heat is handled by the air gaps. Since air is a very poor heat conductor, we need to eliminate the air gaps by using a more conductive material than air, and thus improve the interface thermal performance. Commonly used bonding agents (typically, solder and conductive/non-conductive epoxies) introduce interfaces and/or interlayers of finite thicknesses. When an attachment material is reflowed or cured at the interface, it is assumed that[18]:

- the interface surfaces are wetted by the compound, which drives out all the air pockets in the interface and eliminates the contact resistance component of the total thermal resistance.
- thickness of the interface will decrease in proportion to the applied pressure and will achieve a minimum value, which is dependent on the viscosity of the material and the planarity and curvature of the interface surfaces.

While strong interfaces and/or interlayers are necessary to ensure mechanical integrity of the bonded components, they are responsible for lowering the electrical and thermal conductivities of the assemblage. Each interface decreases the performance of the system substantially as well as increases the manufacturing cost. In reality these layers are non-uniform and consist of voids, which introduce irregular thermal spreading. However, in thermal modeling, these layers are considered uniform and homogeneous, providing excellent thermal contact[19,20,21,22,23,24]. The uncertainty of an interfacial contact resistance can be large due to imperfections at the interface; consequently, the contact thermal resistance becomes a significant factor in determining the total thermal resistance of a package.

Contributions of interfacial contact resistances leading to a total package resistance are ignored by thermal designers as well as the module manufacturers. The only thermal characterization in the power module fabrication process includes a thermal resistance test which measures the junction to case temperature differential. Using the measured ΔT, a software program calculates the device junction thermal resistance, which is provided to the customer. However, the estimated low thermal resistance is extremely unrealistic since the calculation ignores any contribution of the interface contact resistances, which may constitute over 50% of the total package thermal resistance[7,20,21]. To illustrate the issue, we prepared sample structures such as shown in Figure 4.1.2 and used three different interface materials – solder preform, solder paste and silver epoxy, without any applied pressure and following manufacturers' specifications.

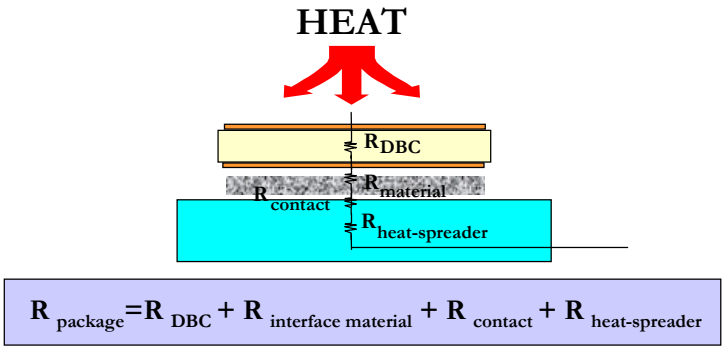
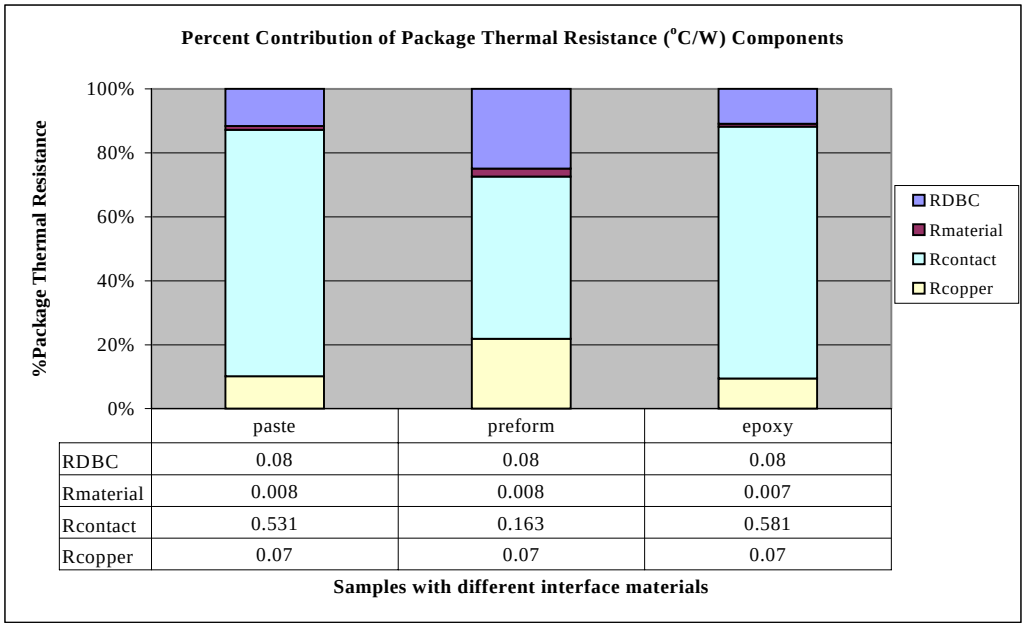


Figure 4.1.2. A cross-section schematic of a typical module substrate to heat spreader interface structure

The following figure shows the different components of the measured package thermal resistance values of the structured samples. The samples were processed with the conventional air reflow or curing without any process optimization.



	paste	preform	epoxy
RDBC	0.08	0.08	0.08
Rmaterial	0.008	0.008	0.007
Rcontact	0.531	0.163	0.581
Rcopper	0.07	0.07	0.07

Figure 4.1.3. Percent contribution of package thermal resistance components

As we can see from the plot, the contact resistance of the interface material ($R_{contact}$) in all cases contributes the largest part of the package thermal resistance. For the solder paste and silver epoxy interfaces, the measured contact resistances constitute over ~70% of the total thermal resistance[25]. This significant amount of contact resistance can be attributed to surface roughness and flatness, process induced

voids and other defects, which are completely ignored in thermal modeling schemes as well as in conventional module fabrication protocol[26].

Despite the importance of this attachment layer, bonding of the heat-spreader to the module substrate is one of the most uncontrolled processes in today's power module fabrication scheme, practiced by the module manufacturers. Typically, a significant amount of solder paste is dispensed on the area to be attached; the two surfaces are brought together and then reflowed in air on a belt oven. The paste is manually dispensed, which results in random thicknesses of the attachment layer from module to module. Moreover, the attachment process is extremely labor intensive since an operator manually moves the two bonding surfaces randomly in a scrubbing action to minimize bubble formation at the attachment layer. As a result, from module to module, the level of voiding with the associated human errors and process inconsistency can be extremely significant. Shown in Figures 4.1.4 and 4.1.5 are the images of a solder and epoxy interface between a commercial power module and the heat spreader of a commercially available power electronic module respectively. The voids and other internal discontinuities of the layers are quite evident, which increases thermal resistance of the interface layer and lowers the module's reliability to a significant extent. Moreover, we notice that the epoxy layer has not spread all over the substrate, leaving some portions of the substrate in poor thermal contact with the heat spreader. In all cases, the voids and other internal discontinuities of the layers are quite evident.

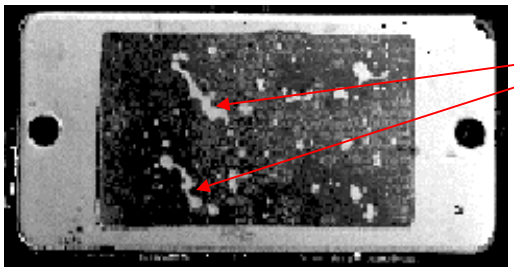


Figure 4.1.4. Solder interface of a power module

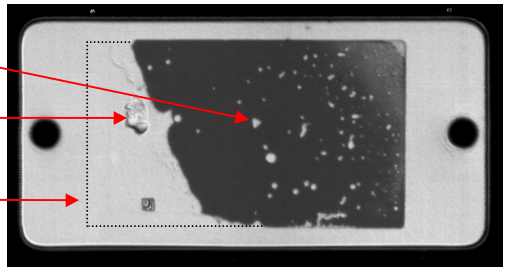


Figure 4.1.5. Epoxy interface of a power module

The significance of the heatspreader attachment layer cannot be overemphasized. First of all, it serves the most critical task of heat dissipation and ensures proper thermal management of a three-dimensional power module structure. Furthermore, from a reliability point of view, the heat spreader attachment layer is the most critical interface of a power module. Researchers at Rockwell Science have performed an extensive amount of thermal cycling on various commercially available power modules. In every case, the interface between the module and the heat spreader was the first joint to collapse[27]. Observed failures at this interface can be attributed to CTE mismatch of thick copper baseplate and the defect-rich attachment layer. Since at the present time, we are limited by the choice of baseplate material, we need to emphasize on the processing of the attachment layer to minimize defects. The presence of voids affects the thermo-mechanical properties of joints, and the growth in voids lessens the strength, ductility, creep, and fatigue life, by coalescing to form ductile cracks and consequently causing failures. The enhanced magnitude of the stresses and strains of solder caused by voids can also cause deterioration of thermo-mechanical properties. Lau et al. has reported the development of a finite element modeling with void diameters of 0.125 to 0.2 mils at various locations in a solder joint[28]. Also, the voids around the center of the joint had higher stresses and strains than those of edge voids. Moreover, voids can also produce hotspots, causing excessive heating[29].

On a more macroscopic view, the thermal resistance of the joint is directly proportional to the interface thickness and inversely proportional to the thermal conductivity of the interface material, as well as to the area of the heat transfer. The rate of conductive heat transfer, Q, across the interface is given by,

$$\mathbf{Q = [kA\,(T_c - T_s)]/L}$$

where, k = thermal conductivity of the interface material,
A = area of heat transfer,
L = interface thickness,

T_c = device case temperature, and

T_s = heat spreader temperature.

Therefore, the thermal resistance of an interface can be expressed as,

$$R_{c\text{-}s} = (T_c - T_s)/Q \qquad \text{or} \qquad R_{c\text{-}s} = L/(kA)$$

Hence, the thermal resistance of the joint is directly proportional to the interface thickness and inversely proportional to the thermal conductivity of the interface material as well as to the area of the heat transfer. Consequently, thermal resistance should be minimized by[30]:

- making the interface as thin as possible,
- increasing thermal conductivity by eliminating interstitial air gaps, and
- providing intimate thermal contact.

In today's module fabrication industry, process optimization for the heatspreader interface is ignored for the most part and therefore, the manufacturers do not have any information on the quality of the bonded interfaces. Quality control of the attachment process is grossly overlooked and hence, any failure of the module is attributed entirely to device interconnection failure. As a result, this research is focused with a systematic approach in evaluating thermal resistance of heat spreader attachment layer and engineering the interface to minimize thermal resistance.

In the following section, we identify the factors and mechanisms contributing to void formation in the heatspreader attachment process.

4.1.3 Factors and Mechanisms Contributing to Void Formation

Voids are defined as cavities and bubbles in solidified solder, which may deteriorate electrical, thermal and mechanical properties of the solder joint[31]. In some cases, the cavities may be filled with flux due to surface roughness and low temperature soldering process[32]. Furthermore, void volumes add to the thickness of the joint volume, thus increasing the joint thickness, resulting in higher thermal resistance. Over the years, researchers have identified several parameters that can be attributed to void formation. These factors can be distributed into four categories - materials, methods and machine, environment and human factors[33]. Each of these categories can be further subdivided into several sub-categories. In the following schematic, all of the factors and their subfactors leading toward void formation are illustrated.

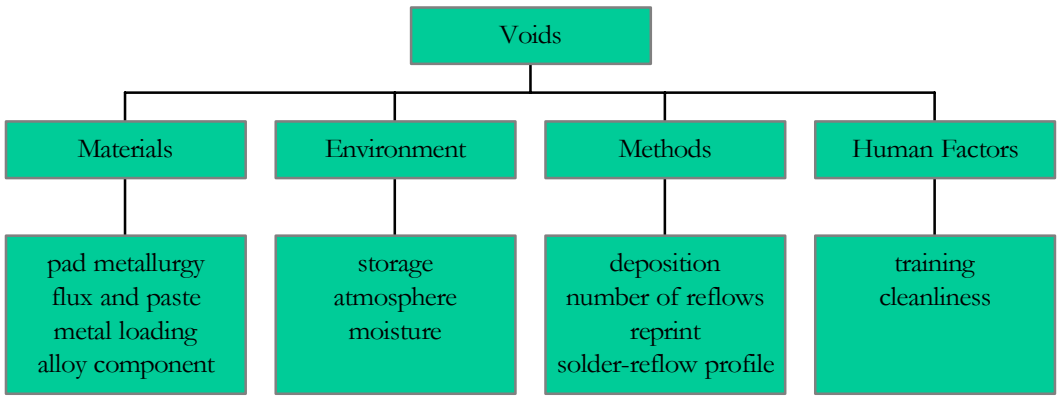


Figure 4.1.6. Factors contributing to void formation

The voiding phenomenon, although being one of the most critical factors in governing interface reliability, is understood only speculatively. We have compiled the following mechanisms that researchers believe to be responsible for void formation.

- mechanical entrapment of air which surrounds the liquid solder material[34]

- flux undergoing a chemical reaction when tarnish films are removed from metallized substrates[35]
- outgassing caused by the flux in the paste[36]
- generated gas by the metallization of substrates, components or the solder powder surface during fluxing[37]
- physical evaporation of the solvents and rheological additives in the paste vehicle; moisture or incomplete curing of the laminate[38]
- amount of outgassing flux, which gets entrapped in the solder during reflow; bubbles within liquid solder[39]
- applied stress during processing[35]
- solidification of molten metals; minimization of free energy which dictates the spherical shape[38]

Although in recent years, a significant amount of research has been devoted to improve the thermal conductivity of the interface materials, thermal conductivity is only one parameter for optimizing the heat transfer. From a materials point of view, a typical solder paste has three main constituents –

- solder balls, which form the main material component
- flux (Rosin activated, Rosin Mildly Activated, Water-soluble and No-Clean), which de-oxidizes the surface for improved wettability, and
- solvent, which acts as a vehicle for the solder to be screen or stencil printed.

Similarly, for silver epoxy, silver particle constitutes about 80-90%, solvent constitutes 5-15% and epoxy resin constitutes the remaining 2-8% of the total composition.

Consequently, the size as well as the weight of the sample to be attached influences the choice of solder paste in two ways. First of all, during the long pre-heat time before reflow cycle, the solvents should not evaporate. Moreover, extreme care must be taken to reduce the occurrence of voids. Large surface area of the copper heat spreader is especially prone to solder voids and typically, the flux activity and not the solder alloy composition or the ball size would act as a critical factor in void formation[40].

The primary concern with voids involves a loss of thermal conductivity, thus an increase in thermal resistance leading to overheating of the die, which leads to an eventual failure by mechanisms such as crack growth due to CTE mismatch. Researchers at Motorola has estimated a 15% change in package thermal resistance as the solder void concentration varied from 0% to 25% in the case of a SOIC8 package[41]. Also, in a range of the attachment layer thickness from 0.25 mil to 0.60 mil, they observed a difference of 25% in the thermal resistance calculation. In addition, voids can cause hotspots by creating areas of poor heat dissipation. Material with the thinnest interface and minimized voids should be selected to ensure minimized interfacial thermal resistance. Therefore, processing parameters and conditions (reflow environment) need to be tailored to minimize the void content and other macroscopic and/or microscopic irregularities in the interface layer and to maximize the homogeneity of the interface layer for maximum heat transfer. A variety of materials and approaches are available for attachment purpose to minimize the thermal resistance of package interfaces. The selection of a particular combination of heat spreader, interface material and the substrate will depend on the design, the quality of the interface material and its proper application, which we seek through the following process optimization schemes as discussed in the next section.

4.2 EXPERIMENTAL PROCEDURE

In this section, we discuss the tailoring of the conventional heatspreader attachment process. Sample test structures are prepared with selected attachment material and tailored reflow/curing profile. Test structures are tested for package thermal resistance using a suitable thermal resistance measurement process. Available test methods are explored and an optimum method for multilayer structure is selected. Finally, a non-destructive detection tool is used to quantize the defects at the interface layers for subsequent correlation.

4.2.1 Process Optimization for Heatspreader Attachment to Module Substrate

Process optimization includes four tasks – selection of the attachment material, tailoring of the reflow profile, application of pressure during bonding and minimizing surface roughness, which are described in the following paragraphs.

4.2.1.1 Selection of a High Thermally Conductive Interface Material

Typically, in a power electronics module, (as shown in Figure 4.1.2), we do not require the interface material to provide an electrical isolation between the substrate and the heat sink since the AlN-DBC clad itself isolates the active copper plane with a thick dielectric ceramic. The selection process for the interface materials to be tested for the MPIPPS packaging application was mostly determined by the intrinsic thermal properties of the materials. In our effort to minimize thermal resistance, the first task is to select a highly thermally conductive attachment material, which will result in a thin interface with minimized thermal resistance by conforming to the surface gaps. Although common heatsink attachment materials such as thermal grease and phase-change materials can conform to the surface irregularities better than solder or epoxy compounds, they do not provide a permanent interface, which is needed for the heatspreader attachment to the power module.

In most electronic packaging applications, the attachment materials are solders and organics. Most common solders are tin-lead alloys, which provide both electrical and thermal paths. Organic attachment materials or epoxies are usually selected based on specific electrical and thermal needs. We have investigated electrically conductive (or insulating) bonding materials in pre-formed films and paste forms containing metallic (or polymeric) powder particles in an organic binder vehicle. These materials are easier to apply and can be processed by a low-temperature curing cycle; however, they generally result in thick interlayers which may have low electrical as well as thermal conductivity because of the organic content. Thermal conductivity of the interface materials has a major impact on the interface resistance, with high k materials having a substantially lower interface resistance. Traditionally, silver particle loaded epoxies have been the most widely used material for package attachment in low temperature, non-hermetic packaging. However, the fundamental limitation in thermal properties of these epoxies does not meet all the demands for electronic packaging[42,43,44]. On the other hand, solder materials are easy to use for attachment applications, where the attaching surfaces are solderable. In the following paragraphs, we describe three different types of attachment materials, which we evaluated as possible candidates for the sample preparation scheme.

Pb-Sn Eutectic Solder: The current wide-spread use of eutectic Pb-Sn solder is a result of the ease with which it wets many metallic surfaces, its high shear strength and fatigue resistance at room temperature, its low cost, and its low processing temperature. Eutectic solders have liquidus and solidus temperatures near each other, which offers benefit for processing. In recent years, solders in a paste form have gained popularity due to its processing advantages. Solder paste is made from the powdered alloys (including tin, lead, silver, indium, gold, antimony and bismuth) and the flux binder system. Our first choice of the interface material is Pb-Sn eutectic solder in preform and paste forms, with a melting temperature of 183^{o}C. After the reflow, the most common cleaning methods are sufficient to remove the flux residues. However, in our case of a sandwiched structure, there is no access to the joint once the solder has reflowed. As a result, we have selected a no-clean flux, eliminating the need for residue cleaning. As per manufacturer's specifications, this solder exhibits excellent wetting of the copper surface and no cleaning is necessary after processing since the residues are not detrimental to the package. This solder can be processed in air or in nitrogen atmosphere, and is specially designed for long stencil/print life.

Silver Filled Epoxy: Electrically conductive epoxies are designed for applications requiring low stress, low volume resistivity and high thermal conductivity. Silver filled epoxies offers the flexibility necessary in the packaging scheme. These materials are cured at elevated temperatures and once cured, no clean up is necessary. They eliminate the biological hazards of using lead in solder applications. They also exhibit excellent adhesion to a variety of substrates satisfying both mechanical and thermal requirements whereas solders only wet certain metals. These materials are available in a wide range of viscosities and thixotropic

indices to meet specific processing needs. Our choice for an electrically conductive epoxy is a one component high temperature conductive adhesive from Diemat. This is a single component, silver filled epoxy designed for high volume manufacturing, low volume resistivity and high adhesion to heatspreader materials.

Thermally Conductive Dielectric Epoxy: These compounds are an improvement on thermal grease as they are converted to a cured rubber film after application at the thermal interface. Initially, these components behave just as thermal greases. These compounds flow as freely as grease to eliminate the voids and to reduce the thermal resistance of the interface. Once the attachment of surfaces is completed and the interface is formed, the compound cures with heat to a rubbery state and develop adhesion properties, which eliminates the need for mechanical fasteners. In recent years, thermal properties of these compounds are being continually improved with the addition of high thermally conductive ceramic fillers such as aluminum oxide, aluminum nitride and boron nitride. We selected Multicure 991 epoxy from Dymax Corporation as a thermally conductive (electrically insulating) epoxy. This is an alumina filled, thermally conductive adhesive for mounting heat sinks and heat sensitive electronic components. Multicure 991 can be used with an activator 501-E, which ensures instantaneous bonding.

The table below summarizes the thermal properties of the selected interface materials for our proposed work on interfacial characterization.

Table 4.2.1. Properties of selected interface materials

Material	Brand	k (W/m-K)	CTE
Pb-Sn Eutectic Solder Preform	63-37 Pb-Sn (fluxless)	50	21-25
Pb-Sn Eutectic Solder Paste	Kester 63-37 (no-clean)	50	25
Silver Epoxy	Diemat DM6030Hk	60	26
TC Dielectric Epoxy	Dymax Multi-Cure 991	~1.5	45

We prepared sample test structures with 1"x1" DBC substrate with same sized copper heatspreader and the selected attachment materials (solder, conductive silver epoxy, dielectric epoxy, thermal grease and interface thermal pad) without any applied pressure. The printed thicknesses of the interface materials were kept the same for all three four types of samples. These samples were tested for their package thermal resistance. Test results of the total thermal resistance of the test structures using the selected interface materials are shown in Figure 4.2.1.

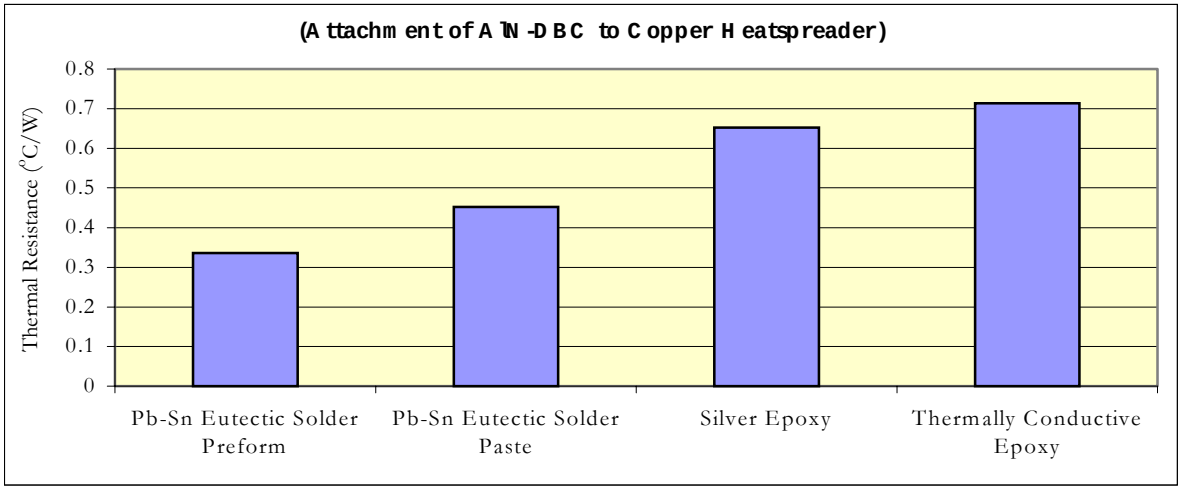


Figure 4.2.1. Package thermal resistance using various interface materials

Based on the thermal resistance data as shown above, we selected solder preform, solder paste and silver epoxy as the candidate materials for our sample preparation. The silver epoxy and the thermally conductive

epoxies seem to exhibit higher resistance than expected. The dielectric epoxy was not selected due to its high thermal resistance. However, the silver epoxy that we used is a research material with a thermal conductivity higher than solder, and therefore, we continued further investigation with this epoxy.

4.2.1.2 Optimization of Reflow Profile

Of all the factors leading towards void formation, the most crucial one is the reflow profile. In this research, we have carefully tailored the reflow profile to minimize the void content. Some of the key features during the solder reflow process are described in the following paragraphs.

Oxidation of Copper Surfaces: Voids can result from poor wetting characteristics, which is common in copper substrates with excessive oxidation at high temperature prior to reflow. In the case of a solder paste with no-clean flux, the oxidation tolerance is very limited and the voiding phenomena is more pronounced[45]. One possible solution to minimize this problem is to reduce the heat energy input prior to solder reflow. In the reflow profile, the heating stage needs to be as short as possible with a linear ramp rate from ambient to the solder melting temperature. At the same time, another research group has shown that a long soak time of 2.5 minutes or higher reduces void content[33]. Furthermore, using a nitrogen atmosphere minimizes the possibility of oxidation during the excessive soak time.

Flux Activity: Flux solvents evaporate during the ramp-up stage of the reflow profile and therefore, the ramp rate as well as boiling point of the solvents affect void formation. At a very slow ramp up rate, the outgassing of flux can occur via diffusion process rather than a rigorous vaporization as seen in the case of fast ramp rate. Hence, voiding is improved by reducing the viscosity of the flux remnant, which can be accomplished to a certain degree using a cooler profile[46,47]. However, researchers do not seem to agree with the theory of reaction gas formation during the oxide removal process. One research group has suggested that the chemical reduction of the metal produces H_2O, H_2 and CO_2[31]; while another group has claimed that the oxide layer is only lifted off the metal without being actually reduced[48]. Another research group has suggested that flux can remove the oxide film from the surface, even when trapped in the molten solder; however, according to Stoke's law, the trapped flux cannot escape and thus becomes an outgassing source for void formation[49]. As a result, the outgassing theory during the flux reaction stage is still under investigation.

DerMarderosian et al. has observed formation of bubbles in liquid solder during reflow using an optical microscope[34]. Solder paste was screened on to a substrate and then a glass slide was placed on top of the solder. The assembly was pre-heated to dry out the solvents in the solder paste. Next, the solder was heated up to its melting temperature where the researchers observed outgassing from both the liquid solder and the paste vehicle. Consequently, the researchers concluded that voiding is not entirely caused by the evaporating solvents of the paste vehicle, rather, it is dominated by the gases generated by chemical reactions during the reflow process.

Dwell Time: Dwell time is defined as the duration above the liquidus state of the solder. As a general rule, dwell time is usually kept as small as possible. Klein et al. has reported that the void content in the solder material increases with an increase in dwell time[50]. However, the melting time must be long enough to ensure a complete melting of solder as well as sufficient wetting of the base metal.

Cooling Rate: Typically, a fast cooling rate is desired to minimize intermetallic formation as well as to ensure fine grain structure in the joint. However, the selection of a cooling rate must take into account the tolerance of the components against thermal shock. Eutectic solder shrinks about 4% during solidification and hence, the interior of a joint will always contain voids since it solidifies last[32].

Surrounding Environment: At the reflow stage, the atmosphere surrounding the molten solder, influences the wetting process and the joint quality. Some researchers have theorized that a reducing atmosphere improves wettability while preventing re-oxidation of molten solder. However, in power electronics packaging industry, almost all solder attachment processes (except the die-attach process) are performed in

air. As a result, in this research, we have investigated the use of nitrogen atmosphere during reflow to verify the atmospheric contribution toward void minimization.

As we can see, most of the attributes leading to void formation are related to the rapid initial ramp rate and the long soak time of a conventional reflow process. As a result, the conventional reflow must be adjusted to provide a slow ramp rate to a low peak temperature, followed by a fast cooling rate, which would ensure an optimum solder reflow.

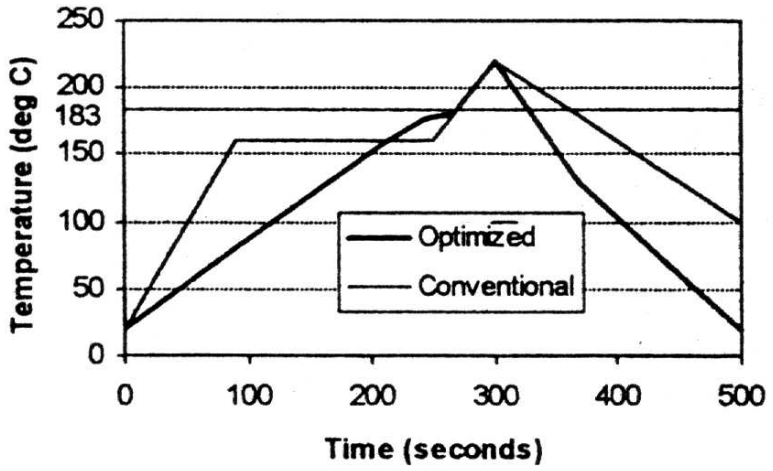


Figure 4.2.2. Optimized profile for solder reflow process[47]

As for the epoxy curing, we used manufacturer's specification. However, it should be noted that, since this material is still a research material, the manufacturer has not determined an optimized curing process of this epoxy yet. The suggested curing of the epoxy is listed in the following table[43].

Table. 4.2.2. Curing conditions of the silver epoxy

Processing step	Temperature (°C)	Ramp Rate (°C/min)	Hold Time (min)
Pre-bake stage	100 - 125	<10	30 - 60
Curing stage	175 - 225	<10	15 - 30

4.2.1.3 Application of Pressure during Reflow and Curing

As mentioned earlier, in an ideal case, thinly applied materials would fill the air gaps and would not increase the distance between the surfaces. However, in a real case, the interface materials do maintain a certain thickness between the surfaces and increase thermal resistance of the joint. Therefore, we need to apply a contact force during the attachment process to spread out the interface material and minimize the thickness. Application of pressure is a large factor in reducing thermal resistance of a joint. The measured thermal interface resistance can be divided into three components as described below:

$$\mathbf{R_{th(total)} = R_{C1} + R_{material} + R_{C2},} \text{ where}$$

$R_{th(total)}$ = total thermal resistance in the joint,
R_{C1} = contact resistance of surface 1,
$R_{material}$ = thermal resistance of the interface material itself, and
R_{C2} = contact resistance of surface 2.

In general, $R_{material}$ can be reduced by applying a pressure while reducing the material thickness. Thermal resistance created by the material itself (assuming void-free case) for a given thickness is constant as a

function of pressure; however, the contact thermal resistances at the interfaces are extremely dependent on pressure[51]. Manufacturers of interface materials often provide thermal resistance data without reporting the applied pressure data (which could be as high as 100 psi), which could be misleading to the package designer.

The minimum applied force required for a good thermal contact will vary from package to package depending on the material's compressibility, surface flatness, surface finish, and area of contact. Typically, there is a minimum contact force that should be applied to the package for contacting; however, any force applied beyond that range would still decrease thermal resistance until the limit that the package can withstand. In most cases, applying a force in the manufacturing or fabrication process is not practical; however, in power module fabrication process, the substrates with power devices and other components would provide sufficient force during the heat spreader attachment process, thus facilitating the removal of airgaps.

4.2.1.4 Minimizing Surface Roughness

In an ideal case, the heat spreader surface should have a flatness and surface finish comparable to that of the silicon device. In high power applications, these requirements are critical and a detailed examination of surface is usually required before any subsequent processing. Surface flatness is measured by comparing the variance of height in a specimen to that of the reference standard. In general, for heat sink attachment, the attachment surface should have less than 4 mil/inch surface flatness to be considered satisfactory[52]. However, in a recent test with TO-204AA package and silicon rubber compound, researchers have shown that interfacial thermal resistance has decreased from 0.75°C/W to 0.38°C/W with a corresponding improvement of surface flatness from 6 mil/inch to 2 mil/inch.

On the other hand, surface finish is defined as the average of the deviations from the mean surface height. For extremely low thermal resistance, the surface finish needs to be in the range of 50 to 60 microinches[52]. However, a fine finish at the surface is not always cost effective, such as in the case of module fabrication protocol. Researchers at Thermalloy has shown that a surface finish between 16 and 64 microinches caused less than 2.5% difference in interface thermal resistance measurements in the presence of voids and scratches within a thermal joint compound[53]. According to mounting specifications, immediately prior to the attachment process, we have employed a fine polishing of the area with steel wool, followed by an acetone and alcohol rinse.

4.2.2 Selection of a Thermal Resistance Measurement Technique

Predicting the thermal performance of a packaged assembly is the weak link in thermal modeling and reliability analysis. Researchers have used finite element modeling, which employs an electrical resistance analog of parallel and series resistors. In general, the test methods are useful with either homogeneous or composite thermally conductive sheet materials. The common test methods measure steady-state heat flux through a flat specimen[54,55]. For the calculation purpose, it is assumed that the materials are homogeneous. In reality, some of the materials are not homogeneous; however, the assumption does not detract from the usefulness of the test methods. The term thermal conductivity applies to homogeneous materials. Thermally conductive insulating materials are usually heterogeneous since they typically include fillers, binders, reinforcements such as glass fiber mesh or a layer of a polymeric film.

A limitation of these test methods involves the uncertainty with respect to specimen thickness whether this parameter should be measured as manufactured or as tested. In most cases, thickness measurements are made at room temperature. Contact pressure, specimen surface characteristics and alternate paths for heat dissipation also influence thermal resistance test data. In some cases, thermal conduction properties are determined under a specific set of conditions, which may not agree well with the conditions in an application environment. In the process of selecting a feasible measurement technique, we have explored the most commonly used methods for interface resistance measurement to verify the applicability of the technique to our specific multilayer structure. In the electronics industry, there are a number of methods that researchers

use to measure thermal resistance of interface materials[56,57,58,59,60,61,62]; however, they can be primarily categorized in two different types of measurement – direct or indirect.

4.2.2.1 Direct Measurement Techniques

In the following paragraphs, the most standard and well accepted direct techniques of measuring thermal resistance are presented[63,64,65]. At the same time, their suitability to our specific research need is also evaluated.

Infrared Thermal Imaging: This technique is based on the emission of radiation as electromagnetic waves from hot bodies. The rate of emission is proportional to the surface emissivity and temperature. Typically, dark objects have high emissivities while shiny objects such as metals tend to have low emissivities, and therefore, surfaces with the same temperature may give different temperature indications, as a result, emissivity needs to be compensated in the analysis of the IR image. IR imaging has limited used in the case of encapsulated or sealed devices since an accurate imaging and thermal calculation is only possible in the case of an open die face. In the case of a multilayer structure such as three-dimensional power module, it would be impossible to detect temperatures of the device as well as of buried interfaces.

Θ_{JC} Tester: This technique involves measurement of a temperature sensitive parameter (TSP) of a device under test. Typically, an electronic device is biased with an idle current, which generates power in the device as well as a junction temperature. The device is then pulsed on with a current for a short period of time, raising its temperature. Once the change in temperature is measured, thermal resistance (Θ_{JC}) can be calculated using the equation: $\Theta_{JC} = \Delta T/P$. Since this technique can be used for sealed or encapsulated devices, it can also be easily adopted for multilayer package structures.

Liquid Crystal Micro-thermography: In this technique, the surface of the sample under test must be exposed before applying a coating of a nematic liquid crystal with a phase transition temperature of 110^{o}C. The liquid crystal material is viewed under a polarizing microscope, which distinguishes the transition. Thermal resistance is determined by placing a thermocouple under the package on the heat sink surface. The bias to the device is increased until a phase transition is observed at the hottest position of the chip. The power is recorded for the transition and the measurement is repeated for a series of different base temperatures with the resulting reference temperatures plotted against dissipated power of the device. Thermal resistance is calculated from the negative slope of the curve. Although, this technique provides accurate results with fine resolutions, it is not well suited for a production or manufacturing process application.

Fiberoptic Thermography Probe: On the surface of the sample, a temperature sensor consisting of a temperature sensitive phosphor mounted at the end of a probe is placed. A filtered zenon flash lamp provides the blue-violet light to excite the phosphor, which exhibits a deep red fluorescence. Once the pulse is over, the decay of the intensity is measured and correlated with the phosphor temperature by comparing the measured decay time with a pre-calibrated table. This technique can measure temperatures with accuracy of $\pm$0.1^{o}C, however, some of the disadvantages include the necessity for unencapsulated device as well as in direct contact with the surface, which may lead to surface damage.

3ω method: In the 3ω method a narrow metal line is deposited on the surface of the sample, which serves as both the heater and the thermometer in the measurement[66,67]. Heat flows radially in the sample and the thermal conductance is extracted from the frequency dependence of the self-heating of the metal line. One major drawback of this test method is that the electrical isolation of the heater/thermometer metallization from the substrate is highly crucial. Sample preparation involves plasma-enhanced chemical vapor deposition of isolating oxide film followed by a photolithographic etching of the oxide layer. Next, the heater/thermometer metallization is deposited on top of the oxide film using evaporation and then finally patterned using photolithography and a chemical etch.

Laser Flash method: In the Laser Flash method, a laser flash is directed on the surface of one component of the bonded assembly and the transient temperature is measured on the surface by an infrared detector[68,69,70,71]. This electrical test method relies on the time dependence of the relative temperature change occurring on the rear face of the specimen. Sample preparation in this test includes coating the test structures with gold as well as a second colloidal carbon layer.

4.2.2.2 Indirect Measurement Techniques

In electronics industry, the indirect techniques are commonly referred to as non-destructive tests. The most common non-destructive measurement techniques are described below.

X-ray Imaging: In this technique, a small amount of radiation is passed through the sample, which creates a shadow image of the materials in the sample. Therefore, it is widely used in detecting voids in a die-attachment layer. One significant disadvantage of x-ray imaging is its inability to detect cold solder joints, which are encountered with solder preforms. A few materials such as silicon and aluminum are transparent to X-rays, while dense materials such as copper, lead and copper/tungsten are difficult to see through with conventional X-ray imaging[7].

Acoustic Micrography Imaging: High-frequency ultrasound waves are passed through a sample and reflected back from various layers, which creates images of internal features of the sample. The degree of reflection is dependent on the acoustic impedance of the different layers within a sample. No special preparations of the samples are needed for the imaging. Thermal resistance measurements can be achieved through a combination of thermal modeling and subsequent recalculations based on voiding. Once a maximum thermal resistance is established for an assembly, corresponding limits on interface voiding can also be incorporated.

Thermal Test Chip: A thermal test chip typically consists of a resistive heater placed on a silicon chip with a sensor diode. Similar to the Theta-JC test, the thermal chip uses a temperature sensitive parameter to determine temperature. However, in this case, the excitation and the measurement circuits are different. The base temperature of the chip is held constant using an infinite heatsink while a small amount of current is applied to the heater element. With a constant applied current, ΔT is calculated by measuring the change in the diode voltage with or without the heating current. Using the sensor junction temperature, case temperature and the dissipated power in the resistive heater, thermal resistance of the package assembly can be calculated.

Upon exploring the available measurement techniques, we have selected the TO-220 thermal chip test technique is one of the most suited methods of measuring thermal resistance of multilayer packages. In this method, thermal resistance is measured indirectly by measurement of temperatures, voltage, current, dimensions and material properties[72,73,74]. A schematic of the test is presented below.

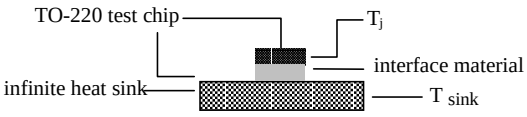


Figure 4.2.3. A schematic of a thermal chip TO-220 test technique

The material under test is placed between a TO-220 transistor and a water-cooled heat sink. The transistor works as a heater while the heat sink maintains a steady heat flux through the sample structure. This test process is widely used by interface material manufacturers due to its minimal sample preparation and adaptability to 3-dimensional structure packages, which imitates the real application environment for the test products. More importantly, this test method has provided excellent consistency of results. In the next section, sample preparation for the TO-220 test and a step by step description of the test method are provided.

4.2.2.3 TO-220 Test Procedure

Components such as a TO-220 package have an integral metal plate, which eliminates the variations in heat flow and cooling paths. Nearly all of the heat produced at the junction leaves through the integral baseplate of the device. The basic procedure for an electrical technique of thermal resistance measurement is the following[40,75,76,77,78]:

Step 1: Calibration of the temperature sensitive parameter (TSPs)

Forward junction voltage drop of a device is linearly dependent on temperature. This unique relationship is used to detect the junction temperature of a device at any given power level. The electrical method of temperature measurement using a TO-220 device is the most accurate technique available to date. At the beginning of the test, the device is calibrated to determine the actual voltage-temperature relationship, using a constant sensing current over temperature. Throughout the thermal resistance measurements of the test samples, we used the same device to maintain consistency and accuracy of the measured data.

Step 2: Application of continuous power and TSP sampling pulses

When the temperature sensitive parameter, i.e., the device is calibrated, we provide test signals to the device. Continuous power of known current and voltage is supplied to the device, while a continuous train of sampling pulse monitors the junction temperature. At this stage, the applied power is adjusted to achieve a sufficient temperature gradient at the junction above the reference temperature. The sampling rate is fast enough so that the device does not get a chance to cool down between the sampling. As the power is being continuously applied, the device case temperature will increase significantly and consequently, a heat sink (equipped with liquid cooling such as chiller) is attached to keep the device under safe operating temperatures and to maintain good resolution in the measurement process.

Step 3: Measurement of junction and reference temperature and applied test power

When the device junction temperature is stabilized, it gets recorded along with the reference temperature and applied power. Typically a thermocouple is used to measure the reference temperature, which is located at the reference point. In this research, the drilled hole in the TO-220 is used to keep the thermocouple during the test sequence in order to measure the reference temperature. Care must be taken not to drill through the transistor body or through the surface as transistor will be damaged and must be discarded. Reference temperature measurement via thermocouples are considered invasive since thermocouples inherently involve contact measurement[79]. In most practical applications, some portion of the heat conducts through the thermocouple, thus registering a cooler temperature reading than the actual reference temperature. This error may be further pronounced if the thermocouple wire is more thermally conductive than the packaging materials. However, in the case of thermally conductive surfaces, as in the cases of DBC substrate and copper heat-spreaders in this research, the errors associated with thermocouple measurements can be minimal. Moreover, the thermocouple needs to be in good contact with the reference for accurate temperature measurement. A good thermal contact between the thermocouple and the heat spreader is assured with applied thermal grease in the port-hole for thermocouple. Thermal grease ensures good thermal contact as well as measurement accuracy. One other key concern is that the thermocouple placement location needs to be consistently same for multiple sample testing. As a result, in our sample preparation phase, extreme caution was practiced while drilling the 1/32" inch hole in the TO-220 device.

Step 4: Calculation of thermal resistance

Using the voltage and current of the transistor, we calculate the power, while the temperature gradient between the transistor case and the heat sink can be measured as $\Delta T_{cs} = T_c - T_s$. Finally, the resistance is calculated as $\Theta_{cs} = \Delta T_{cs}/P$.

4.2.2.4. Sample Preparation and Experimental Setup for Thermal Resistance Measurements

In this research, to represent the interface system of interest (as in the case of a conventional power module), we prepared the sample test structures with DBC substrate with copper heat spreader with the selected

attachment materials (fluxless solder preform, no-clean solder paste and thermally conductive silver epoxy). The bonding copper surfaces of the direct-bond copper with a aluminum nitride (DBC-AlN) substrate and the copper heat spreader are de-greased and cleaned thoroughly in an ultrasonic bath to ensure clean bonding surfaces. Figure 4.2.4 shows the cross section view of the test structure.

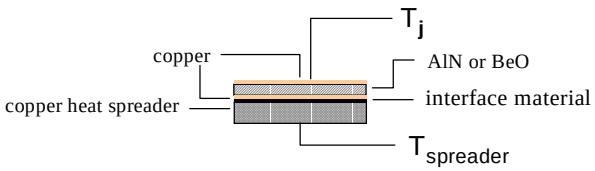


Figure 4.2.4. Cross-section view of the sample test structure for thermal resistance measurement

The top layer is DBC-AlN clad, 45 mil thick (10 mil copper on both sides with 25 mil thick AlN). The next layer is an adhesive layer or the interface layer of solder/epoxy (approximately 2-4 mil thick). Finally, the bottom layer is a 0.25-inch thick copper heat spreader. The dimensions for both the DBC-AlN and copper heat spreader are 0.7" x 0.5", so the interface region is also of the same size. The top copper layer of the DBC substrate makes an exact fit to the TO-220 transistor base, maximizing the heat dissipation in a downward direction.

The only other sample preparation includes drilling a 1/32" hole halfway through the heat spreader to attach a thermocouple, which will measure the heat spreader temperature ($T_{spreader}$). Placement of the thermocouples can also be a factor in the measurement protocol. Consequently, the values presented by materials manufacturers are not in agreement with each other even for similar materials. Motorola uses a technique of placing the thermocouple exactly under the die by reaching through a hole in the heat sink. Thermalloy uses a technique where the thermocouple is soldered to the mounting screw and located on the top portion of the tab between the molded body and the mounting screw. However, these two techniques of placing thermocouples are not applicable to our multilayer test structure. Motorola-specified placement location is not accessible in our structure and the Thermalloy position would blemish the case and added solder may provide results differing up to $1^{o}C/W$ for a TO-220 test package[52]. Consequently, in this research, we followed the JEDEC standard of placing the thermocouple close to the TO-220 die, reaching through a blind hole drilled through the plastic molded body. This specific placement method ensures the recording of the highest temperature on the case, which is essential in our sample structure since the TO-220 is acting as a heat source on top of the DBC substrate[80]; however, the placement of the thermocouple is tedious compared to the other techniques since it involves mechanical drilling.

In this structure, thermal resistance to the heat flow from the heat source to the substrate can be divided into several components. The total thermal resistance across the structure can be expressed as:

$$\mathbf{R_{th} = R_{die} + R_{DBC} + R_{interface} + R_{heat\ spreader}},$$

where, R_{die}, R_{DBC} and $R_{heat\ spreader}$ are the bulk thermal resistances of the thermal chip TO-220, AlN-DBC clad, and the heat spreader respectively. $R_{interface}$ is defined as the total interfacial thermal resistance, consisting of the bulk resistance of the attachment material and the contact resistances occurring at the AlN-DBC to solder/adhesive and the solder/adhesive to heat spreader interface. We assume the resistances to be in series and can be summed up as the total thermal resistance, R_{th}. Once the test measurements of total resistance are completed, we subtract the known bulk resistances from the total resistance to determine the interfacial resistance.

Fabricated test structures were tested for their package thermal resistance using an AnaTech semiconductor thermal analyzer at the R&D facility of the Bergquist Company. Selecting an automated system such as Semiconductor Thermal Analyzer from AnaTech is crucial since an automated test equipment provides the following benefits[81]:

- ease of use,
- less operator dependence on measurement, minimizing human errors,

- consistency,
- accuracy, and
- network capability of data transfer.

Photos of the test facility and setup are shown in Figure 4.2.5. The equipment setup includes an AnaTech Semiconductor Thermal Analyzer with an infinite heat sink.

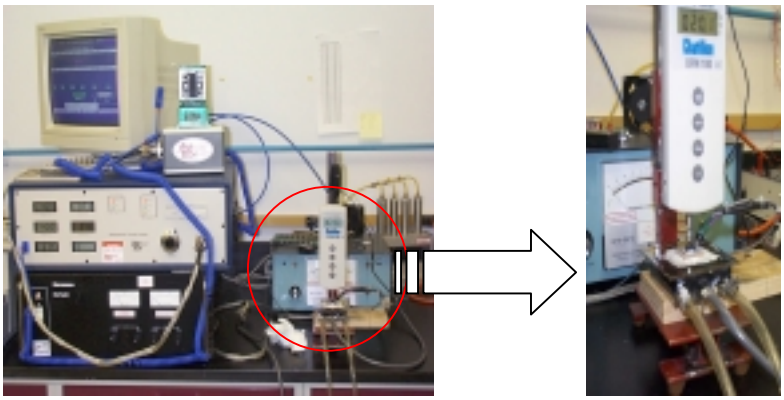


Figure 4.2.5. Schematic of the test setup (courtesy: The Bergquist Company, Edina, Minnesota)

We prepare the TO-220 transistor by drilling a 1/32" hole to the right of the mounting hole. The hole should extend half of the way through the transistor body. The transistor base, the bonding surfaces of the test sample and the infinite heat sink are cleaned to remove grease and dirt. Thermal grease is applied to the back of the TO-220 transistor and to the top of the infinite heat sink to provide an intimate thermal contact during testing. Next, the test structure is placed on the infinite heat sink while the transistor is placed on top of the test sample with both the holes facing the same direction. The pressure mounting hardware is lowered on to the device top and the pressure is adjusted to 20 lbs. At this point, the chiller is turned on to circulate water through the heat sink. We insert the thermocouple leads as far as possible into the drilled holes in the transistor and the copper heat sink of the test structure. With the power supply turned off, we connect the leads to the transistor. Now, the power supply is turned on and the power is adjusted to 40W. The transistor requires about 15 minutes to reach equilibrium. Finally, once the equilibrium is reached, we take the preliminary readings of the thermocouple temperatures and record the exact voltage and current from the power supply. At this point, using the voltage and current of the transistor, we calculate the power, while the temperature gradient between the transistor case and the heat sink can be measured as $\Delta T_{cs} = T_c - T_s$. Finally, the resistance is calculated as $\Theta_{cs} = \Delta T_{cs}/P$. In order to maintain consistency of measured data and to eliminate process variables, we conducted the entire test using the same TO-220 transistor, 40W power and 20lb-pressure[73].

Once the thermal resistance measurements are completed, we implemented acoustic micrography imaging technique to image the interface as well as to quantify the defect contents of the heat spreader attachment layer. In the following section, the fundamentals of the acoustic imaging technique are described.

4.2.3 Acoustic Micrography Imaging as a Defect Detection Tool

In microelectronics applications, X-Ray imaging, TEM, and acoustic micrography imaging are the most common tools for flaw detection. Typically, sample preparation for TEM is labor-intensive, while X-Ray imaging is not suitable to all types of materials. X-Ray imaging is based on the variation of X-Ray attenuation by a solid body. However, the sensitivity of this technique is dependent on the thickness of a material, which the beam needs to penetrate. Moreover, in some cases such as CuW, excessive absorption could make the use of X-Ray unrealistic[82]. Acoustic image scanning of a CuW substrate had revealed a surprisingly high amount of voiding, which was not evident through an X-Ray imaging. One other significant disadvantage of

X-ray imaging is its inability to detect cold solder joints, which are encountered with solder preforms. A few materials such as silicon and aluminum are transparent to X-rays, while dense materials such as copper, lead and copper/tungsten are difficult to see through with conventional X-ray imaging. While ultrasonic imaging easily attains cracks and voids in the solder layer, X-rays will only reveal the absence of solder. Some of the benefits of acoustic imaging over X-Ray imaging are summarized below[5,83]:

- ability to detect defects and flaws in non-metallic materials,
- non-hazardous to operations and has no effect on equipment and materials,
- volumetric scanning ability of metal extending from front surface to the back,
- electronic operations allow instantaneous indication of flaws,
- greater accuracy than other non-destructive methods in determining position, size, orientation, shape, and nature of internal flaws,
- depth-specific information of a defect can be obtained, which is impossible via X-Ray imaging,
- small voids, which are not detectable with X-Ray can be imaged via AMI, and
- materials such as copper-tungsten, which are opaque to X-Ray can be easily imaged via AMI.

Considering the benefits and suitability of AMI to our test samples, we have selected acoustic micrography imaging to detect and quantize flaws at the module to heat spreader interface.

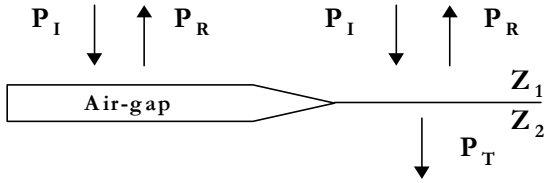
4.2.3.1 Principles of Acoustic Micrography Imaging

When an ultrasonic wave is incident on an interface between two different materials, part of the wave is transmitted while the other part is reflected. The amplitude, time of flight and polarity of the reflected signal provide crucial information about the material, which reflected the acoustic signal. Reflection of an acoustic signal is governed by acoustic impedance of a material, which is the ratio of the acoustic pressure to the particle velocity per unit area; acoustic impedance is defined as the following,

$$Z_i = \rho_i . v_i$$

where, Z_i = acoustic impedance of the material in the ith layer,
ρ_i = density of the material in the ith layer, and
v_i = velocity of sound in the ith layer.

Figure 4.2.6 illustrates the phase inversion principle of acoustic imaging, where a ultrasonic wave is incident on an ideal interface. The amplitude of the incident, reflected and transmitted waves are P_I, P_R and P_T respectively. The materials are assumed to be ideal elastic solids with boundary conditions such that the acoustic pressure and velocity in both materials are equal at the interface and the frequency remains unchanged across the interface. The reflected and transmitted pressure amplitudes can be expressed as the following where Z_1 and Z_2 are the acoustic impedances of materials 1 and 2.



$$P_R = (Z_2 - Z_1)/(Z_2 + Z_1) \qquad P_T = 2Z_2/(Z_2 - Z_1)$$

Figure 4.2.6. Reflection from an air-gap and at a bonded interface

In the following table, acoustic impedances of a few materials are listed.

Table 4.2.3. Acoustic Impedance of Common Packaging Materials[84]

Material	Density	Wavelength (mm) at 25 MHz	Acoustic Impedance (10^6 kg/sec-m^2)
Air (20°C)	0.00	0.014	0.00
Alumina	3.8	0.416	39.56
Aluminum	2.70	0.25	16.90
Copper	8.90	0.188	41.83
Epoxy Resin	1.20	0.104	3.12
Glass (Quartz)	2.70	0.223	15.04
Molding Compound	1.72	0.157	6.76
Silicon	2.33	0.344	20.04
Water (20°C)	1.00	0.059	1.48

Acoustic micrography imaging (AMI) is used in determining different types of defects in various package forms. Of all the applications, AMI has been most successfully implemented in identifying the nature of the die-attach layer. Figure 4.2.7 shows a schematic and an acoustic image of a die-attach layer of a device.

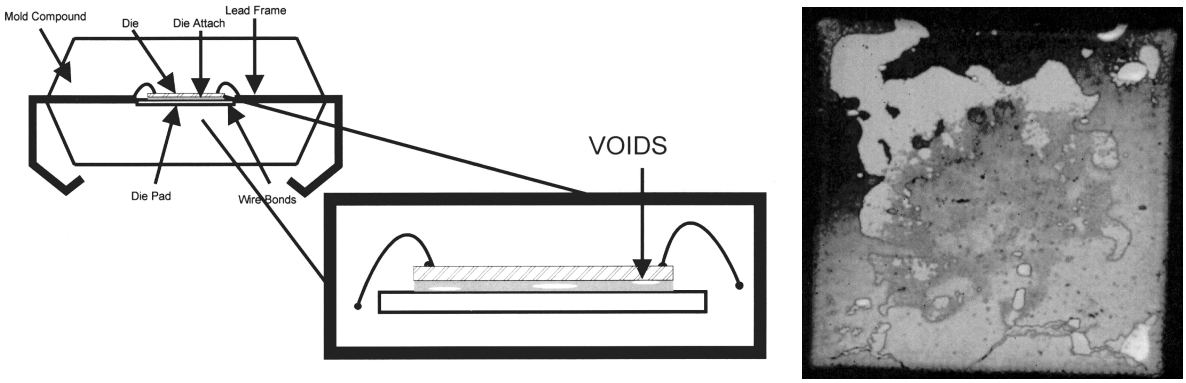


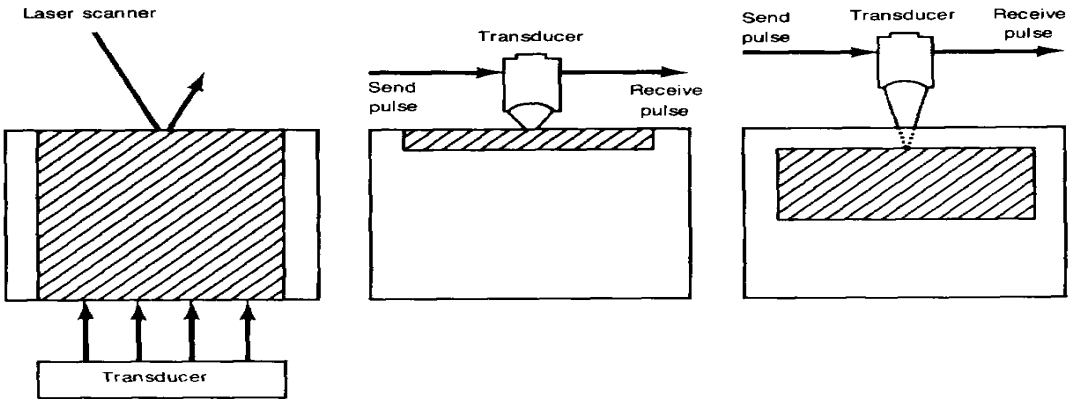
Figure 4.2.7. Die-attach layer characterization by AMI[84]

In a ceramic package, the defects are mainly voids, pinholes and delaminations in wirebonds, substrate metallization, dielectric layers, attachment layers and lid sealing. In a plastic package, typical defects include delamination of the molding compound from the leadframe, cracks in the molding compound, die tilt, and voids in the molding compound, die attach and substrate attach[85,86,87,88]. In real applications, these defects will limit heat dissipation, thus increase thermal resistance and result in eventual failure of the package due to over-heating. Moreover, the defects allow excessive penetrations of moisture, which would eventually lead to corrosion and mechanical failure.

4.2.3.2 Available AMI Techniques

In recent years, acoustic microscopy has emerged as a non-destructive failure analysis tool to evaluate different package designs in the semiconductor industry. There are three types of acoustic microscopes that are utilized in most common applications to study and evaluate interfaces -- the scanning laser acoustic microscope (SLAM); SAM; and the C-mode scanning acoustic microscope (C-SAM). All of the instruments use high frequency ultrasound to detect internal discontinuities in materials and components. The SLAM is a through transmission technique operating at frequencies between 10 and 500 MHz[89,90,91]. SLAM uses a scanning laser detector of the ultrasound images of the internal features of a material. The ultrasonic wave travels through the entire volume of the material and the scanning laser detects the variations in the transmitted ultrasound. On the other hand, SAM is primarily a reflection-based microscope that generates very high-resolution images of a sample surface or a near surface plane. Finally, the C-SAM method uses a pulse-echo microscope that employs a focused transducer to generate and receive the ultrasound beneath the

surface of the sample. In the schematic below, the different acoustic microscopy imaging methods are shown.



(a) SLAM (b) SAM (c) C-SAM

Figure 4.2.8. A comparison of the available three acoustic microscopy techniques[90]

Based on the availability and applicability of the methods to our multilayered structure, we have selected the C-SAM technique to image the interface of the heat spreader attachment material. C-SAM is a pulse-echo microscope that employs a focused transducer to generate and receive the ultrasound beneath the surface of the sample. The transducer is scanned across the sample in several passes for image generation. Scan time varies from seconds to minutes depending on the desired resolution and the area of scan. At the tip of the transducer, a concave lens is attached. The reflective inspection acts on a pulse-echo mode; a reflection from the top of a package returns earlier than a reflection within the package. This time separation is employed to separate layers within a structure.

C-SAM has the ability to perform non-destructive package analysis while imaging the internal features of the package. Ultrasonic waves are very sensitive to the density variations (such as voids or delaminations similar to airgaps) of the surface. C-mode scanning acoustic microscopy uses high-frequency ultrasound to detect internal discontinuities in materials and components. The C-SAM, as shown in Figure 4.2.9, emits acoustic waves in a reflection mode at a specific frequency, typically ranging from 15 to 180 MHz. The distance between the echoes relates to their depth in the device under test. A transducer that alternatively acts as a receiver and sender achieves the reflection. The transducer electronically switches between the transmit and the receive modes. An electronic gate is used to select a specific depth or interface. This microscope generates images by mechanically sweeping a sample while emitting ultrasonic waves from the transducer. The ultrasonic wave uses an inert fluid, such as de-ionized water, as a coupling medium.

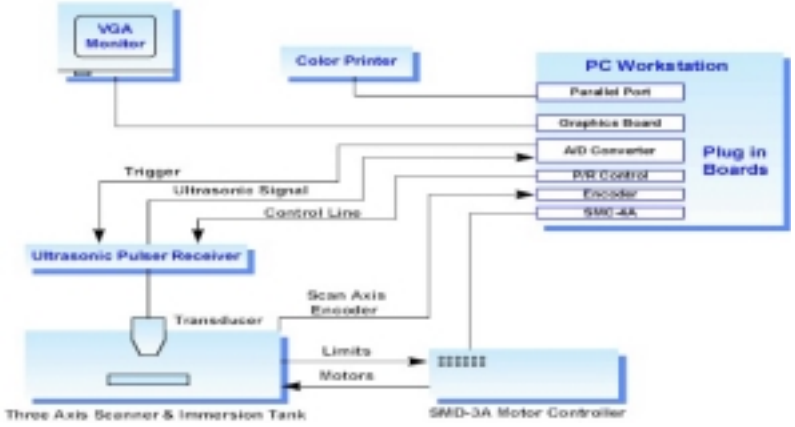


Figure 4.2.9. Block diagram of the C-SAM technique[92]

4.2.3.3 C-SAM Scanning Modes

Several different imaging modes of the C-SAM are discussed in the following paragraphs[90,92,93].

A-Scan: The fundamental information using reflection mode acoustic systems is contained in the A-Scan, which displays the depth information in the sample. Echoes from different interfaces are displayed. The distance between the echoes is related to the depth of the interfaces in the device, and it is expressed as,

D = vt/2, where D = distance, v = velocity of sound, t = time.

A-Scan is a graph of sound intensity against time. The horizontal scale defines the depth within a sample while the vertical scale defines amplitude of the reflected sound wave. In Figure 4.2.10, major peaks of the waveform are labeled to their corresponding interfaces within a package[94]. Once the section to be inspected is identified, the red gate is placed around the layer. Next, the transducer distance is varied to focus the transducer at high sound amplitude. In a conventional imaging technique, a wide gate is placed on the waveform, and consequently, a single image of all layers is projected on to one plane. Also, the system may not be able to detect a defect if an adjacent layer has high intensity than the defect itself.

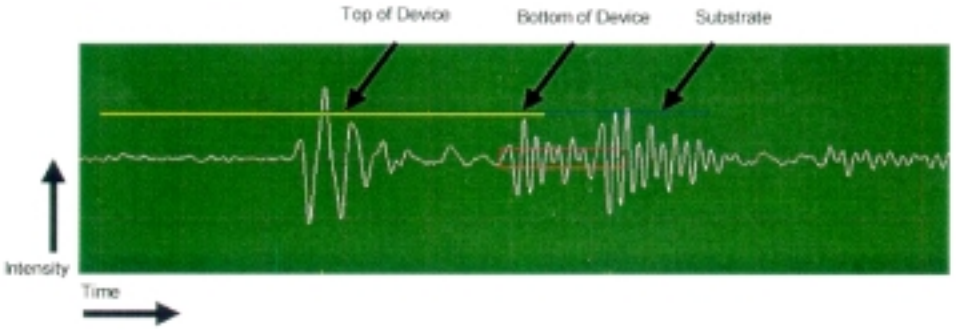


Figure 4.2.10. A typical A-Scan image (with the selected gates) of a device on a substrate[94]

Time of flight scan: In a time-of-flight (TOF) scan, the arrival time of the echo is converted to a gray scale for imaging. This mode provides a general overview of the feature depths and thickness information, which can be projected to a three-dimensional analysis to achieve a perspective of the contour of the interfaces. This specific mode is mostly used in profiling cracks in an IC plastic package, where an isomeric plot of the time-of-flight is acquired simultaneously with the amplitude image to get an enhanced image of the cracks.

B-scan: In this mode, the image displays one dimension of the scan plane on the x-axis and the depth position on the y-axis. The transducer is indexed in the depth direction of the sample to ensure uniform focus throughout the thickness. The time-of-flight data is converted to a depth data so that a cross-sectional image can be obtained. A cross-sectional view, such as a B-scan image can detect the location of a void at a certain thickness of the sample. However, a B-scan image may provide a distorted dimensional information of the device since the object may appear thicker than the actual size. This is due to the fact that B-scan is out of aspect and the horizontal scale is not equal to the vertical scale causing image distortion. Typically, B-scan involves the most complicated and time-consuming analysis of all the available modes.

Interface Scan: The interface scan is most commonly used for imaging delaminations and voids. This method involves gating the reflection specific to the interface under test. At the same time, the transducer is focused onto that specific interface. The acoustic image using an interface scan provides both amplitude and phase of the gated reflection.

Bulk Scan: This technique is employed to portray the acoustic appearance of the bulk specimen, as opposed to a specific interface. The gating of the acoustic signal within the material begins immediately after an

interface echo, and includes all of the area up to the next interface reflection. In the case of a homogeneous material, there will be no significant signal on the image. However, if the material contains voids or other irregularities, they will cause signal reflections to be displayed on the image. The limitation of a bulk scan is that no depth information is supplied in the image. Any defects, between the front surface and the back surface, appear in the image. Obtaining depth information requires additional user interaction and time to view each A-scan or the generation of B-scan, which requires re-scanning the material.

C-SAM images of voids, cracks, disbonds and delaminations are of high contrast, which enables one to distinguish the irregularities from one another. The most important feature of this tool is that it is non-destructive, which gives the researcher more opportunities for further electrical or thermal testing. The commonly available scanning acoustic microscopes (such as Sonix systems) are capable of providing extraordinary resolution. Acoustic image resolution varies with the sample material as well as the frequency of the sound. The tradeoff between a low- and a high-frequency transducer is in the depth of penetration and resolution. The high-frequency transducer provides excellent resolution, while being limited in depth penetration. On the other hand, a low frequency transducer allows more transmission through materials. In the following table, typical resolution and penetration depths for available transducer frequencies are listed.

Table 4.2.4. Resolution and Penetration at Common Operating Frequencies

Frequency	**Wavelength**	**Resolution**		**Typical Depth**
(MHz)	in water (mils)	surface (mils)	interior (mils)	penetration (mils)
30	2	1.4	2.8-7.0	0-280
50	1.2	0.8	1.6-4.0	0-200
100	0.6	0.4	0.8-2.0	0-80
500	0.12	0.08	0.1-0.4	0-1.6
1000	0.06	0.04	0.08-0.2	0-0.8

Consequently, C-SAM as a low-frequency transducer would allow us to image a deep interface, such as the module-to-heat-spreader interface. We can see from the table that a 100 MHz transducer will allow us to penetrate samples up to 80 mil thick and to detect voids as small as 1 mil in diameter.

4.2.3.4 Tomographic Acoustic Micrography Imaging (TAMI™)

In recent years, Sonix has developed a new feature within C-SAM, called TAMI™ (Tomographic Acoustic Micro Imaging) scan, which can supply defect x, y, and z coordinate information without re-scanning for every single layer[92,95,96]. This feature, as shown in Figure 4.2.11, has two advantages: it allows automatic focus adjustments to ensure all depths are in focus and it allows multiple gating to provide images or slices at many different levels (up to 31 slices) within the interlayer. The real advantage is that all 31 images are generated at the same time it takes to do a bulk scan. Therefore, TAMI™ can be easily integrated in the package fabrication process as a standard method of inspecting interface layers. We define the spacing between the TAMI™ images and it is measured in microseconds. This measurement is converted into a millimeter measurement by using the simple formula Distance = Velocity x Time. Therefore, by paging down through the TAMI™ images, we can look deeper within the interface by a given amount.

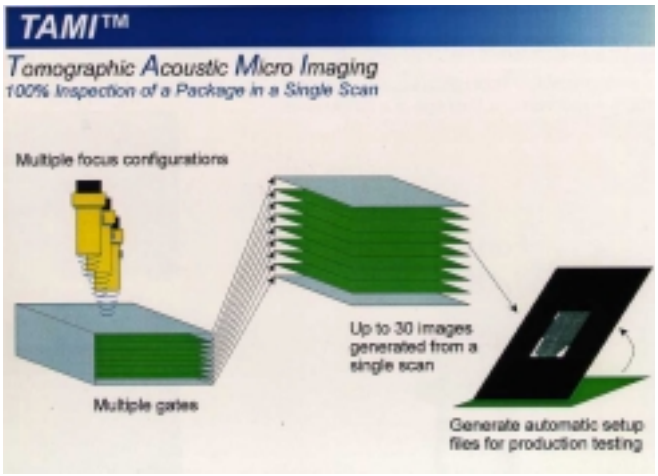


Figure 4.2.11. Schematic of the C-SAM TAMI™ technique[95]

Conventional acoustic imaging could be time consuming and requires a significant amount of expertise to analyze the complex waveforms to determine the layer at which a defect is detected. Ultrasonic parameters such as gate position and focusing need to be adjusted for accurate scanning. For example, in a multilayer structure (such as our test sample), in order to isolate a thin interface, such as a solder layer, a very narrow gate is required, which makes the gate setup extremely crucial and challenging. The problem arises from determining the positive and negative cycles of the A-Scan waveform of the interface under inspection. In most cases, the identification process demands a trial and error method for precise positioning of the gate. As a result, to get an optimal setup, the transducer needs to be focused and the sample needs to be scanned repeatedly.

TAMI™ eliminates all the above mentioned difficulties with the setup and the interpretation of a conventional imaging system. Focusing at an interface is attained by examining C-Scan features rather than maximizing an A-Scan. In a TAMI™ scan, the user sets the start position for the scanning, and the additional gates are automatically set according to the user-defined gate width and spacing. Typically, these gates are set next to each other or in a slightly overlapping manner as shown in Figure 4.2.12. Consequently, the gate width and the frequency of the transducer determine the thickness of each layer.

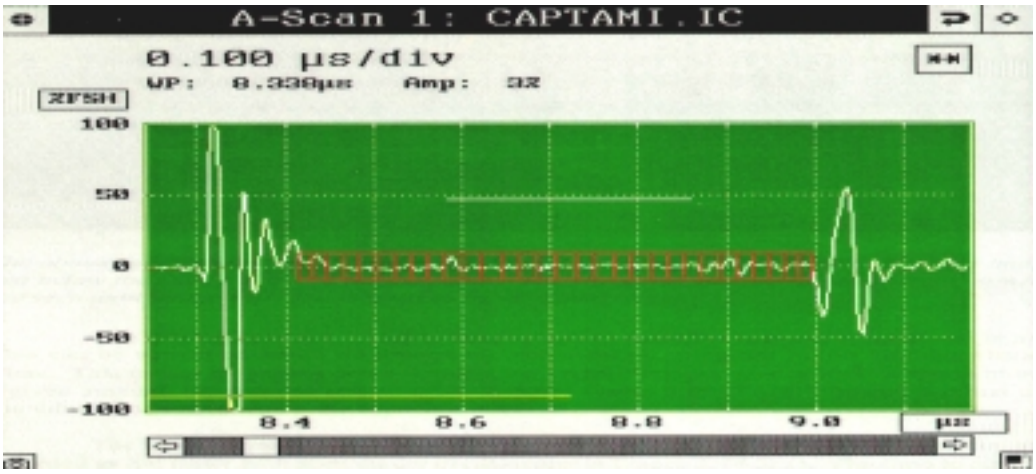


Figure 4.2.12. Gating scheme with TAMI feature[96]

TAMI™ offers specific layer information in an unprecedented easy set up and procedure. TAMI™ provides a C-Scan image of each layer within the specific thickness with an automatic focus adjustment capability. The unique feature of TAMI™ is its capability of acquiring thirty images simultaneously in a single

scan. The user can page down through the layers, identify the defects in different layers and select the interface of one's choice.

Once the TAMI™ images of the entire interface are obtained, we establish a common color palette to distinguish and to identify different types of defects, which are evident in the image. The Flex-Scan™ software, which operates the scanning system, is used to measure the percent threshold values of different colored regions within the user-defined area of an image. Figure 4.2.13 shows an expanded acoustic image of an epoxy interface of a multilayer structure, where the percent threshold values for different regions are also shown. Quantization of defects in all layers is performed and they are added up to establish a minimum limit for defect content throughout the interface.

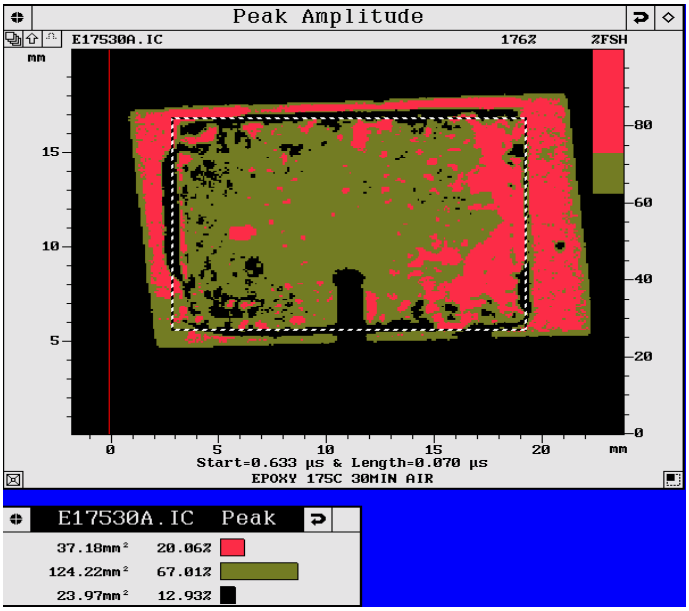


Figure 4.2.13. Acoustic image of an epoxy interface

At the present time, module manufacturers in the U.S., such as Powerex and IXYS perform only a pulsed electrical testing on the fabricated wire-bond modules; however, they do not employ any quality/defect control analysis of any of the attachment layers within the module. Moreover, at the present time in the power module industry, there is no established limit on void-contents for the process of heatspreader attachment. However, in the microelectronics industry, there are several standards for a die-attach process, such as MIL-STD-883, Method 2030: (Ultrasonic Inspection of Die Attach), which can be applied to the heat spreader attachment process as well. According to the above mentioned MIL-STD, a die-attach interface would be unacceptable if the following observations are made[97]:

- contact area voids in excess of 50% of the total intended contact area
- a single void that exceeds 15% of the intended contact area
- a single corner void that exceeds 10% of the intended contact area
- any quadrant in an image (when divided into four equivalent quadrants) exhibiting contact area voids in excess of 70% of the intended quadrant contact area.

Similar standards need to be set for power module interfaces as well. Based on the suitability and non-destructive nature of acoustic micrography imaging technique, AMI can be easily integrated in a production environment, such as in a power module fabrication plant, to inspect the die attach as well as the heatspreader attachment layer, which would allow screening of defective units prior to testing.

In the following section, correlation between measured thermal resistance and the defect content as a function of interface processing parameters are discussed.

4.3 RESULTS AND DISCUSSION

4.3.1 Effects of Processing Parameters on Thermal Resistance and Defect Content

Our objective was to investigate whether the reflow environment and applied pressure during the bonding process effect the resulting interface. Furthermore, since several materials (DBC-AlN clad and the heat spreader) in our structure were copper-based, we explored the effects of oxidation on the thermal resistance during the reflow process as well.

In a typical thermal resistance measurement technique, the test data are influenced by the following parameters:

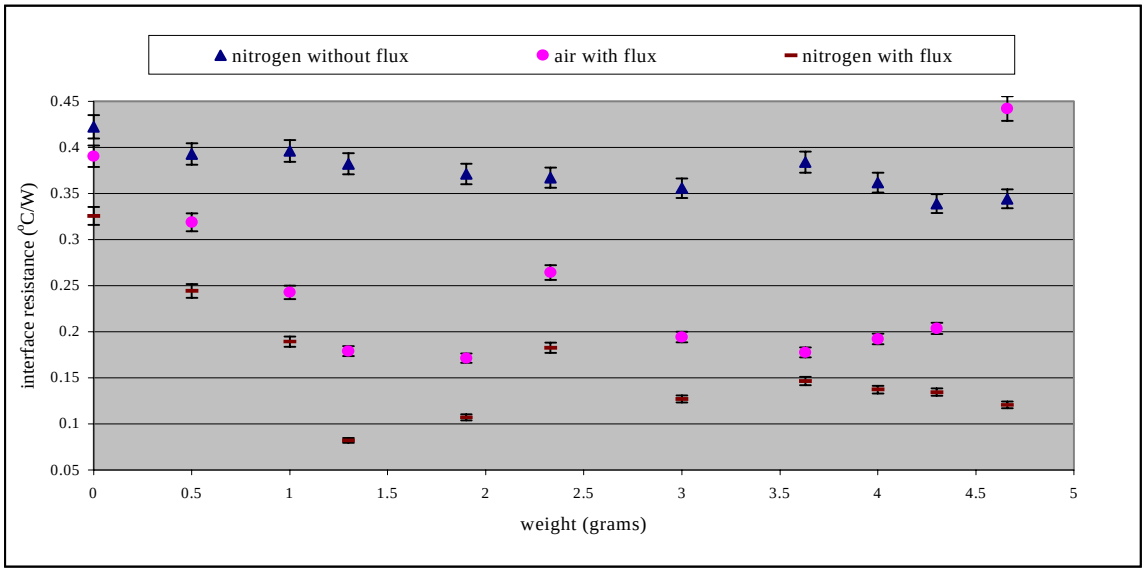
- contact pressure,
- specimen surface characteristics, and
- existence of alternate paths for heat transmission, which is not through the specimen.

In this research, we assume that the specimen surface characteristics constant since a standard surface treatment (cleaning and de-greasing) was given to all test specimens (DBC pieces and copper coupons). We also assume that the heat flowed only through the specimen and not via any other paths. With the applied pressure, the interface gets thinner; therefore, the measured resistance values are scaled to an average thickness of all the samples to eliminate the dependence of thickness with the thermal resistance data. As a result, the measured interfacial resistances, which are illustrated in the following plots, are primarily attributed to the contact resistance as well as defects in the interface material. To better illustrate the effects of processing on the interface, we have subtracted the contribution of the DBC substrate and the copper heatspreader from the measured package thermal resistance using. Consequently, the reported interfacial thermal resistance includes the resistance of the material and the contact resistance only. As mentioned before, we used three different interface materials (solder in preform and paste, and thermally conductive Ag epoxy) to produce three different batches of sample structures for subsequent thermal resistance measurements. We assume that the thermal resistances of AlN-DBC (0.08^{o}C/W) and the copper heatspreaders (0.07^{o}C/W) are the same in all samples[98]. Moreover, all tests were repeated to validate the reproducibility of the data. In the following sections, we illustrate the dependence of thermal resistance and defect contents on the processing conditions -- air vs. nitrogen reflow and increasing pressure on the sample during reflow and curing.

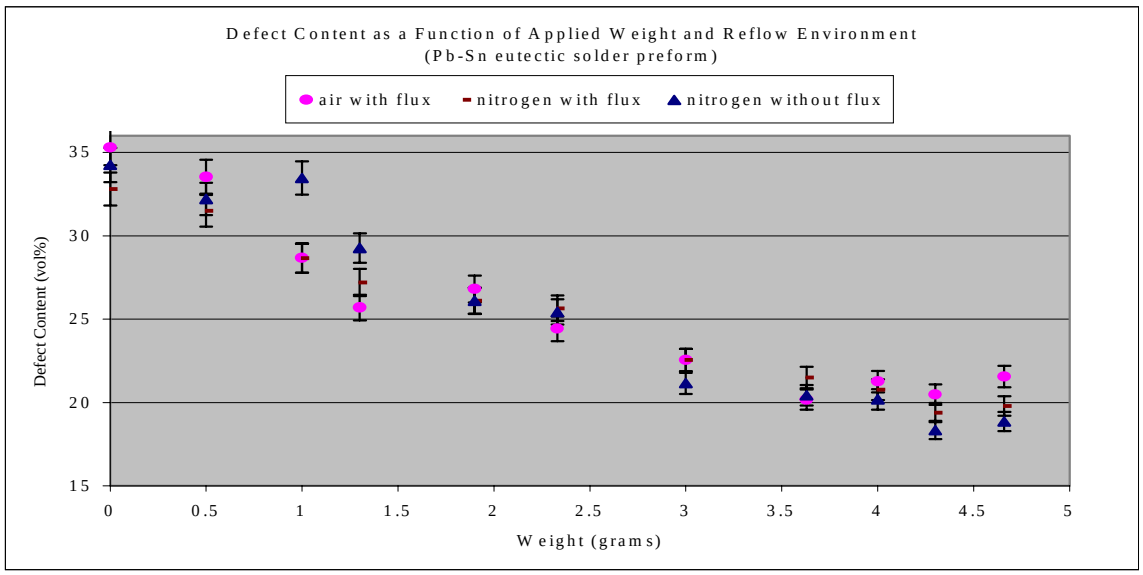
4.3.1.1. Results of Pb-Sn Eutectic Solder Preform Interface

For the samples with solder interfaces, the fixed parameters in the sample preparation include the thickness of the solder preforms or stenciled solder paste layer (~4 mil), and the solder-reflow (liquidus) temperature of 183^{o}C. Variables in the process include weight on the sample during reflow, and more importantly, the reflow environment (nitrogen vs. air) of the samples. The first batch of samples consisted of interfaces with solder preforms. Solder preform that we used in preparing test samples did not contain flux. Therefore, we needed to add a no-clean flux in the case of air reflow, otherwise the copper surfaces would be too oxidized to be wetted by the preform. On the other hand, for a nitrogen reflow, we fabricated test structures with and without the flux. Figure 4.3.1 illustrates the package thermal resistance and defect content as a function of weight on top of the sample, during the reflow process in air and nitrogen.

In the case of air-reflow with flux, interfacial resistance decreases with the addition of weights and reaches a steady state. Beyond that range, the thermal resistance does not improve significantly with the addition of more weights. Similarly, in the case of nitrogen reflow, we observed a significant drop in the interfacial resistance with the addition of weights; then the resistance reaches a steady state. We notice that the thermal resistance values are higher in the case of nitrogen reflow without any flux. Although these samples were reflowed in nitrogen, the bonding copper surfaces may have oxidized, resulting in a weak wetting of the solder preform without the assistance of fluxing agent. On the other hand, we notice that the samples reflowed in nitrogen with the assistance of flux show the lowest thermal resistance values.



(a)



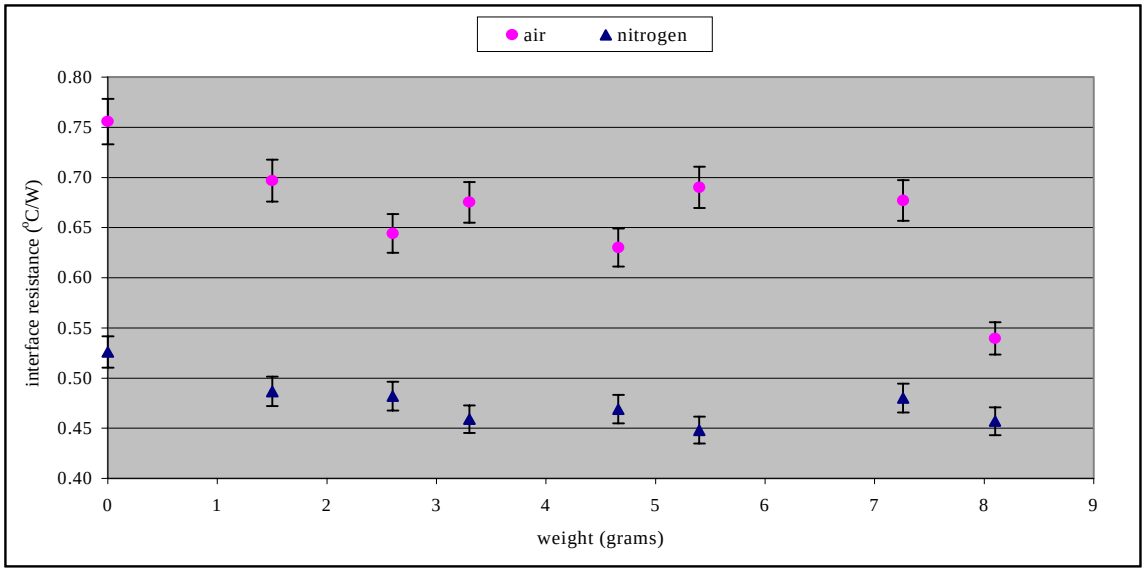
(b)

Figure 4.3.1. Effects of added weight and reflow environment on (a) thermal resistance and (b) defect content (solder-preform)

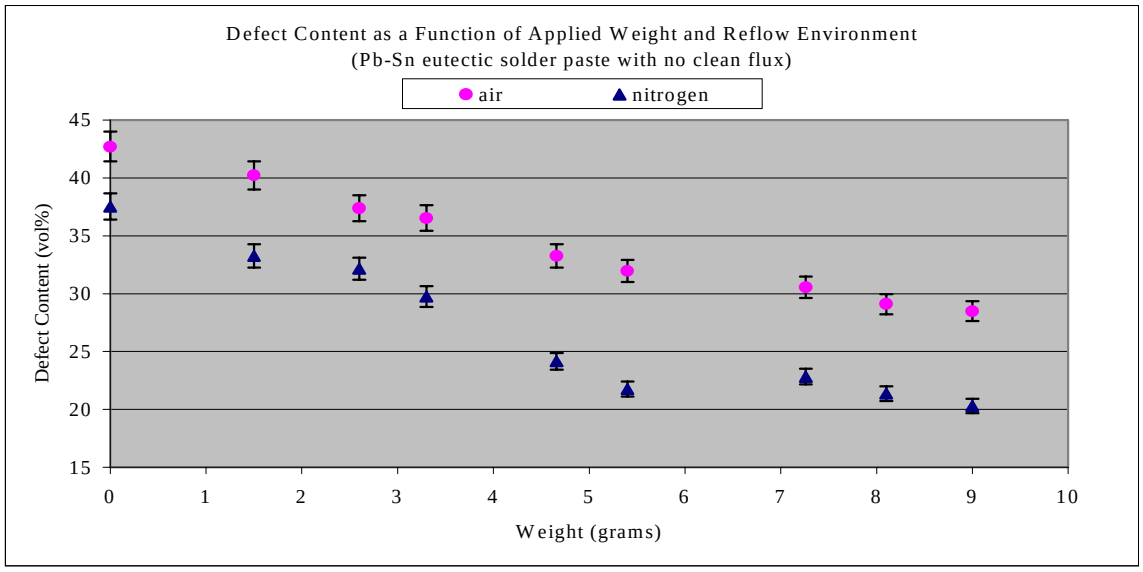
Defect content also drops significantly as weights are added during reflow. After adding three grams of weight, the resulting defect content at the interface almost remains the same. Analyzing the defect content for nitrogen reflowed samples, we observed a steady decrease and saturation beyond three grams of weight on the sample. However, the defect contents are slightly lower in the case of nitrogen reflowed samples as compared to the air-reflowed ones. Samples reflowed in nitrogen without flux shows higher defect contents since the wetting of the copper surfaces was probably not achieved and therefore, significant areas at the interface can be accounted for voids by the acoustic imaging software.

4.3.1.2. Results of Pb-Sn Eutectic Solder Paste Interface

In the second batch of samples, the interface between the DBC piece and the heat spreader was made of Pb-Sn eutectic paste. We repeated the same sequence of process engineering with these samples, as in the case with the fluxless solder preform. We varied the weight on top of the samples while reflowing them in two different atmospheres (air and nitrogen). Figure 4.3.2 represents the package thermal resistance and defect content as a function of weight on top of the sample with a reflow process in air and nitrogen. Interfacial resistance drops with the addition of weights and reaches a steady state. Beyond that range, the thermal resistances seem unaffected by the added weights.



(a)



(b)

Figure 4.3.2. Effects of added weight and reflow environment on (a) thermal resistance and (b) defect content (solder-paste)

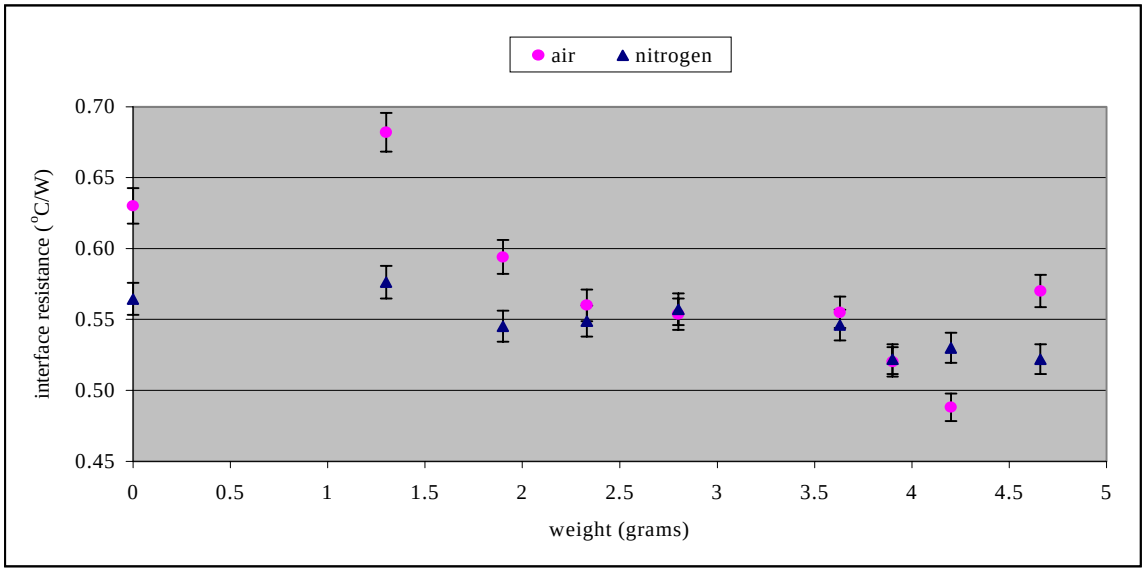
In the case of the solder-paste reflow process in a nitrogen atmosphere, we observe a similar decrease in the interfacial resistance with the addition of weights; then the resistance reaches a steady state. Compared to

the samples with solder preform, these samples (with solder paste interfaces) exhibit slightly higher thermal resistance values when reflowed in air and nitrogen.

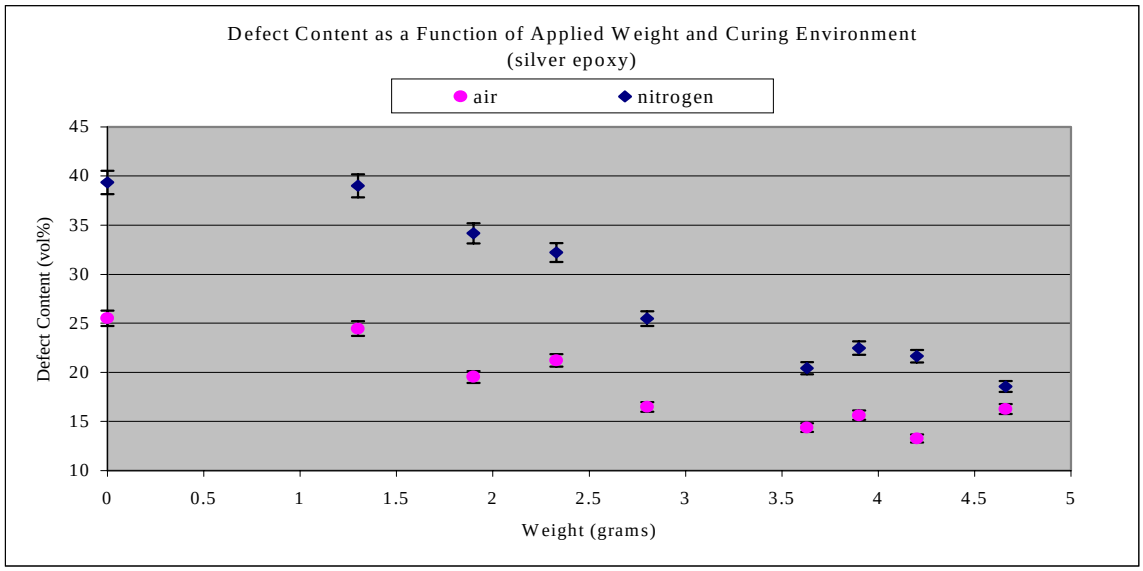
In both cases of reflow (air and nitrogen), the defect content of the interface decreases sharply with the addition of the weight on the sample. Similar to thermal resistance, the defect content also reaches a steady state beyond four grams of weight. However, the decrease of void content in nitrogen reflow is more pronounced than in the case of the air-reflow. In nitrogen reflow, solder interface exhibits defect content as low ~20% while the air-reflowed samples decreases to ~30% void content.

4.3.1.3. Results of Silver Epoxy Interface

The third batch of samples was prepared with the thermally conductive Ag epoxy interface. For the samples with Ag-epoxy interfaces, the fixed parameters include the wet thickness of the screen-printed epoxy. As in the case of the solder materials, we employed the same sequence of tests (curing in air and nitrogen atmosphere with added weights) to the epoxy samples. It is known that several material properties (e.g. porosity, density, thermal conductivity, uniformity etc.) of this adhesive are dependent on the curing conditions and only an optimal curing condition would ensure a thermally enhanced interface[43,71]. Hence, our objective was to investigate if the curing environment (air or nitrogen) affects the package thermal resistance while we varied the weights on top of the samples. The curing temperature and time were kept the same (200°C and 15 minutes respectively) in all sample preparation processes. Figure 4.3.3 depicts the thermal resistance as a function of weight in curing atmospheres of air and nitrogen. As in the previous cases with solder interfaces, there is a significant decrease of thermal resistance of the epoxy interface structures with added weights on the samples during the curing cycle. The thermal resistance curve reaches saturation after an added weight of about three grams. The samples cured in the nitrogen show similar behavior to the air-cured samples. Thermal resistance value decreases up to an added weight of about three grams and then it reaches saturation. Comparing the data between air and nitrogen curing, we see that the thermal resistance values under different curing environments are quite comparable. However, the resistance data seem more uniform in the cases of the nitrogen curing scheme.



(a)



(b)

Figure 4.3.3. Effects of added weight and reflow environment on (a) thermal resistance and (b)defect content (silver-epoxy)

In the case of the epoxy, we observe that the defect contents are actually lower in the case of air as compared to the nitrogen-cured samples. However, with the added weights, in both curing environment, we obtain a defect content of less than 20%. Unfortunately, the exact chemistry of the silver epoxy is not available since the manufacturer is yet to commercialize this epoxy; an optimized processing for this epoxy is still under investigation.

From the discussion above, we can describe thermal resistance in the following mathematical form:

$$\mathbf{R_{th} = f\,(P, S, H, k),}$$

where P, S, H and k stand for applied pressure, surface condition, hardness and thermal conductivity respectively. Defect contents contribute to the terms S and k; defect contribution to the contact resistance is surface dependent while the defects within the interface material affect its thermal conductivity, k. The observations in all three different interface materials from the above plots are summarized below.

- Thermal resistance (scaled for thickness difference of the interface) as well as defect content decreases as a function of applied weight.
- In the case of solder interfaces, defect contents are significantly lower in the case of nitrogen reflow. However, only in the case of epoxy, we observe more defects in nitrogen curing than an air curing.
- The effects of oxidation on thermal resistance are evident when we compare results between a air and nitrogen reflow for any interface. A reflow in a nitrogen atmosphere has consistently produced lower thermal resistance. Nitrogen reflow has the most profound impact in the case of solder paste interface.
- In the case of samples with epoxy, only in a few cases we found comparable thermal resistance values to the solder interface cases. The manufacturer's specified curing schemes for the epoxy interfaces have always resulted in a higher value of the package thermal resistance compared to the soldered interfaces. As a result, even though this novel Ag epoxy is said to be as highly thermally conductive as the Pb-Sn eutectic solder, it has produced inconsistent results and has proven to be less thermally conductive than its solder counterpart.
- On the other hand, eutectic Pb-Sn solder preform with a no-clean flux, reflowed in nitrogen, has provided the least thermally resistant interfaces, particular to our sample geometry and application.

4.3.1.4. Effects of Process Tailoring on Contact Resistance

To further illustrate the contribution of the process optimization to the reduction of thermal resistance, we compare the different components of the package thermal resistance of samples with no processing and an optimized processing. Figure 4.3.4 compares the different components of package thermal resistance between conventional processing and tailored processing. As we can see, the processing protocol with added weight in a nitrogen environment has indeed lowered the thermal resistance in all cases. The most significant reduction of thermal resistance is achieved with solder preform as an interface material.

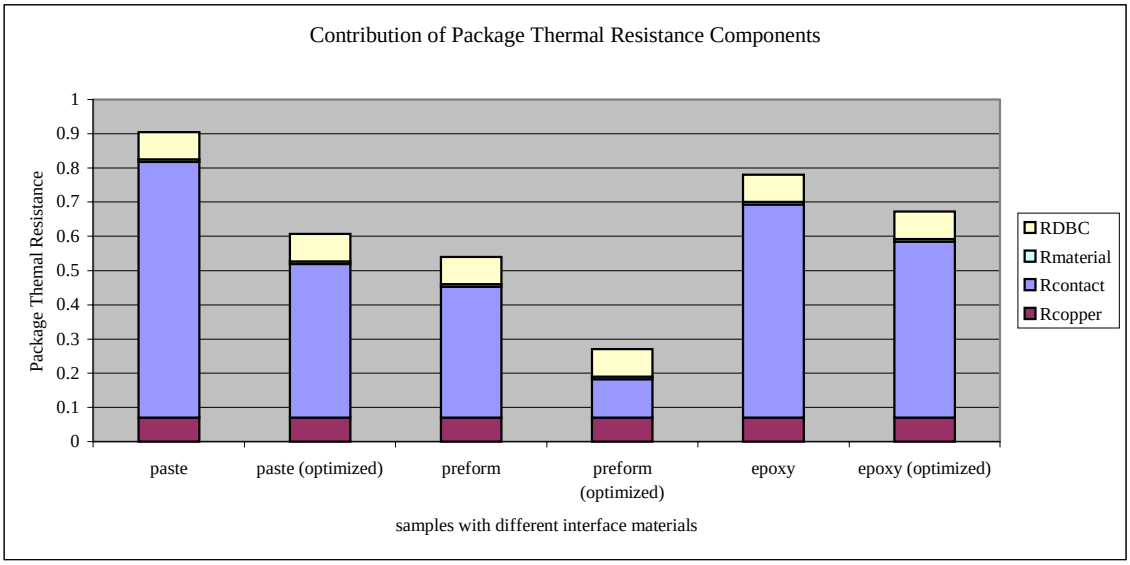


Figure 4.3.4. Comparison of thermal resistance components (conventional processing vs. tailored processing)

The percent contributions of these different components of thermal resistance are shown below.

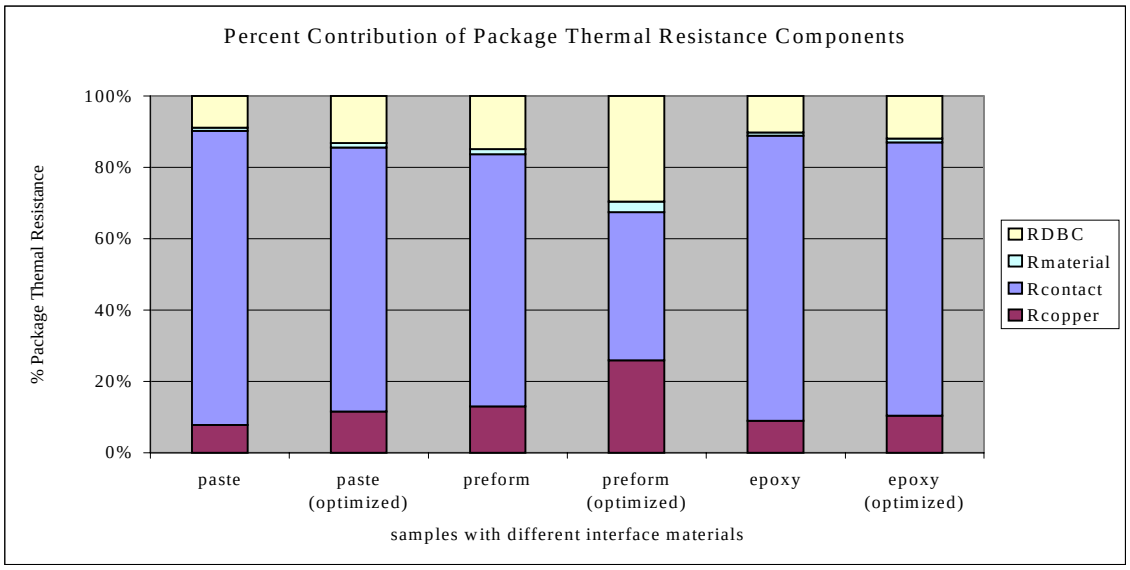


Figure 4.3.5. Comparison of vol% of thermal resistance components (conventional processing vs. tailored processing)

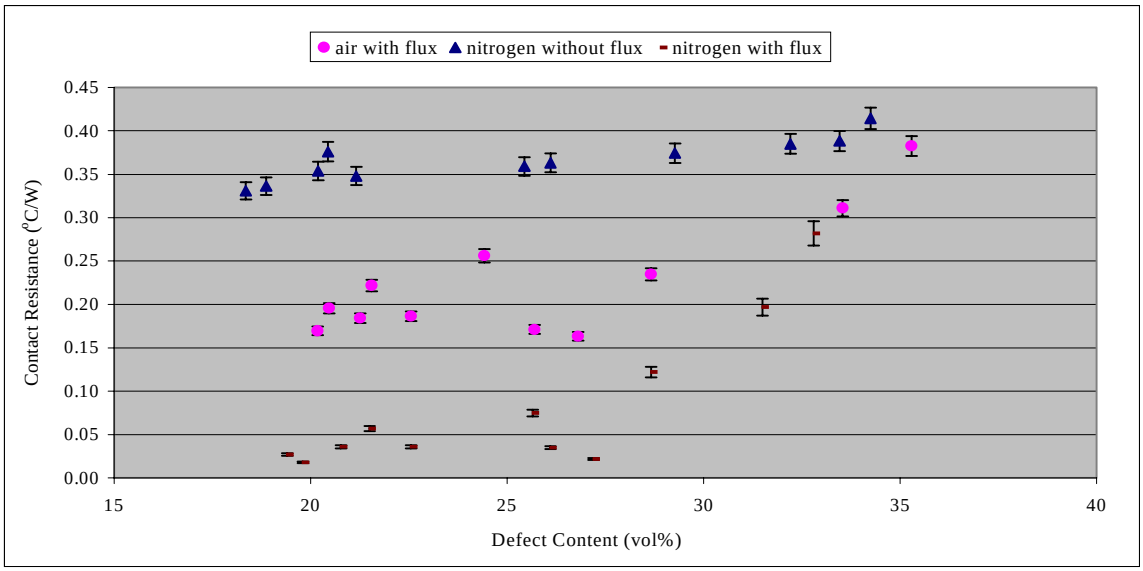
From the figure, we notice that the thickness of the interface material constitutes only a small percentage of the total thermal resistance. Therefore, most of the thermal resistance is attributed to contact resistance, even in the case of a tailored processing. As mentioned before, contact resistance is primarily dictated by surface conditions (roughness, contamination, oxidation etc.) and surface defects. To better understand the

dependence of contact resistance on the defect content, we subtract the materials' contributions of the thermal resistance from the package thermal resistance. In the next section, contact resistance data are correlated with the defect content data to isolate its effects.

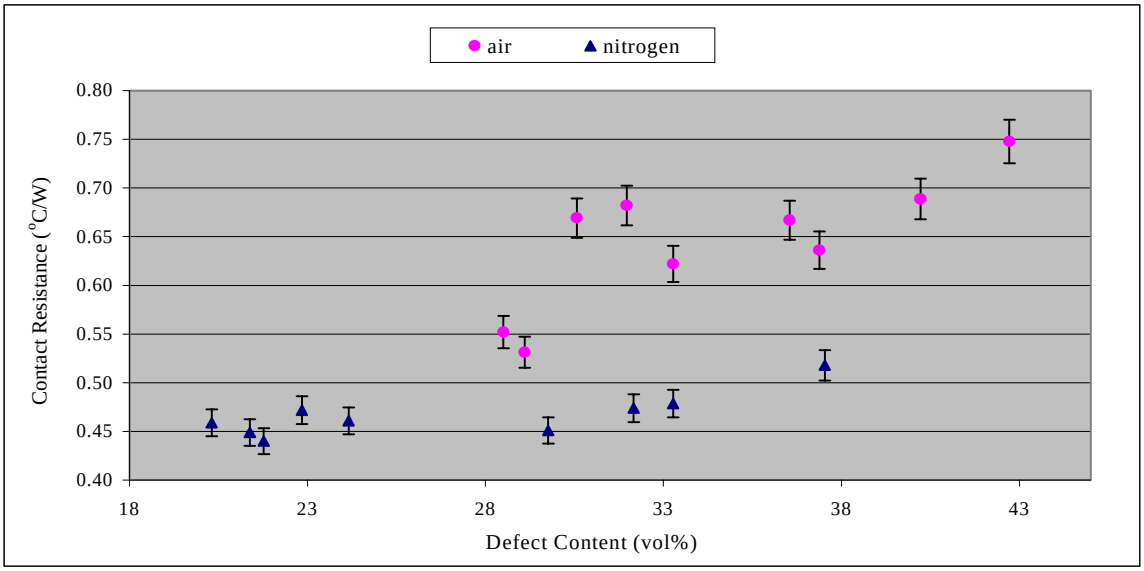
4.3.2 Correlation of Thermal Resistance and Defect Content

Once again, we assume that the thermal resistances of the DBC-AlN and the machined copper heat spreaders are the same for all test samples. Furthermore, we have subtracted the contributions from the interface material. We discuss the correlation of defects with contact resistance for three different interface materials sequentially.

Figures 4.3.6 illustrates the package thermal resistances as a function of defect content in the reflow process in air and nitrogen for solder preform and solder paste.



(a) solder preform



(b) solder paste

Figure 4.3.6. Thermal resistance as a function of defect content (solder)

In the case of solder preforms, in all three cases of reflow, thermal resistance decreases significantly as the defect content decreases. Similar observations are made in the case of solder paste. For the preforms, we notice that the final defect contents are similar in all cases; however, for the paste interfaces, we see that the nitrogen environment produces significantly fewer voids as compared to an air reflow. The most significant drop in contact resistance is shown for the solder preform reflowed in nitrogen with the assistance of a flux. Over all, we notice that the contact resistance values are consistently lower in the case of solder-preform interfaces compared to solder paste interfaces for both reflow environments.

The final batch of samples was prepared with the thermally conductive silver epoxy interface. Figure 4.3.7 depicts the thermal resistance as a function of defect content in curing atmospheres of air and nitrogen.

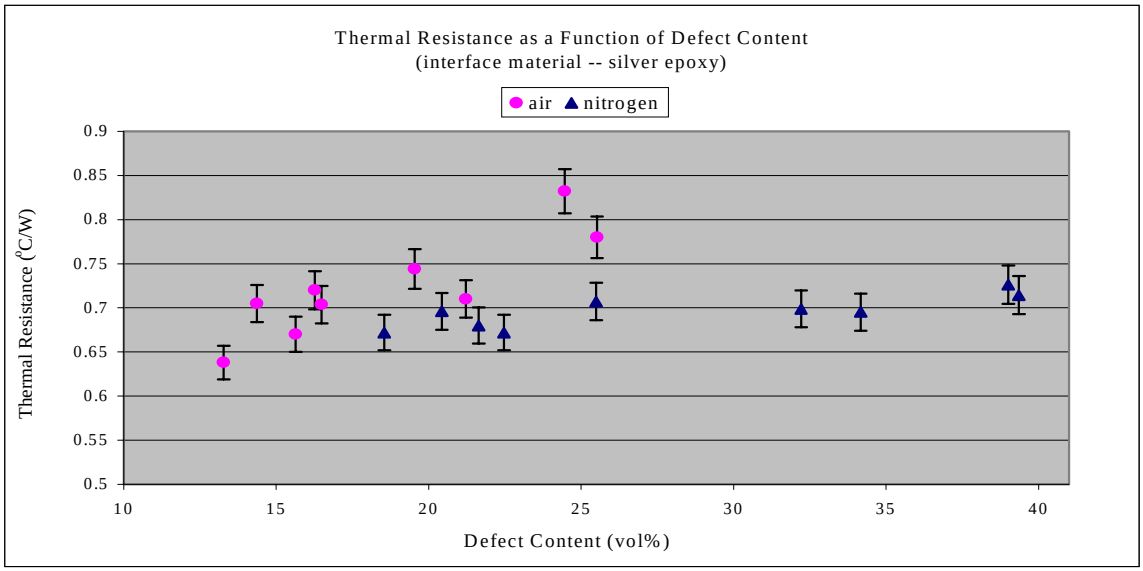


Figure 4.3.7. Thermal resistance as a function of defect content (silver epoxy)

Comparing the data between air and nitrogen curing, we see that the contact resistance values under different curing environments are quite comparable. In the case of the epoxy, we observe that the defect contents are actually lower in the case of air as compared to the nitrogen-cured samples. In an air curing, samples exhibit a sharper drop in thermal resistance as defect content decreases; while in the nitrogen environment curing, the decrease in thermal resistance is not so pronounced.

From the above plots, we notice that for the same interface material with a same defect content results in different thermal resistance values for different reflow environment.

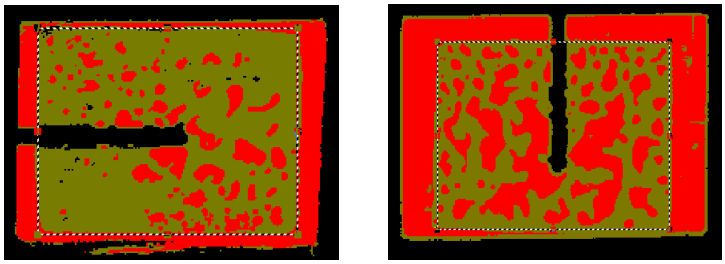
- The difference in the measured thermal resistance may be attributed primarily to the oxidation of the sample surfaces as well as the solder itself. In the case of an air reflow, the copper surfaces of the DBC as well as the copper heatspreader would be significantly oxidized at the peak temperature (220°C) of solder reflow profile. The presence of the oxide layers may have resulted in higher package thermal resistance at the TO-220 test.
- The defect detection at the interface is not fully optimized yet due to inherent limitations of the imaging technique. None of the available techniques can fully account for all voids at the interface. Consequently, further enhancement in the imaging process is required for accurate defect detection.

We also observe that for the same Pb-Sn solder alloy, we obtained different values of thermal resistance under the same applied pressure and same defect content. Measured values for solder preforms are consistently lower than that of the solder paste. Some possible reasons for this observation are listed below:

- When we processed the fluxless solder preform, we had to add flux so that the copper surfaces could wet sufficiently. In the solder paste, metal loading is ~90% while the remaining ~10% includes flux

and solvent. In the case of solder preform, with the addition of the flux, we have in fact, decreased the volume percent of metal loading as compared to the solder paste. Compared to a lower metal loading, in a higher metal loading solder system, the flux action is reduced, thus resulting in poor wetting and more voids. By adding the flux, we have increased the fluxing action of the solder preform as compared to the solder paste. In solder paste, the flux is in direct contact with the surface oxide of the powder as well as the copper surfaces. Therefore, during the reflow, residual oxide may have some flux adhered to it; however, in the case of a solder paste, the greater amount of flux has eliminated the oxide more rapidly and thoroughly, thus leaving fewer spots for the flux to adhere to.

- In another possible scenario, based on the acoustic images (as shown in Figure 4.3.8), solder paste produces more voids at the interface than a solder preform. The voids resulting from a solder paste are randomly distributed all over the surface, which blocks the underlying voids in the material from being detected. Consequently, the calculated total void content of the solder paste may be significantly lower since the imaging cannot account for the voids directly underneath a surface void. However, in the case of a solder preform, the surface voids are not as widely spread as the solder paste and hence, the Flex-Scan software detects more inter-material voids than in the case of a solder paste.



(a) solder preform (b) solder paste

Figure 4.3.8. Acoustic images of Pb-Sn eutectic solder interfaces

4.4 SUMMARY AND CONCLUSIONS

Process optimization and characterization of a power module's heatspreader interface will improve heat transfer and enhance the reliability of the entire module. An interface with minimized voids will improved immunity to thermal fatigue, which is one of the major causes of failures in the present wire-bonded power electronics packages. With this end in view, we have investigated the module-to-heat-spreader interface fabricated with thermally conductive attachment materials (solders and conductive epoxy). Interfacial thermal resistances of multilayer structures are measured and the interfaces are imaged with acoustic microscopy. The utility of a TAMI™ scan as a diagnostic tool for evaluating the module to heat-spreader interface is demonstrated. Correlation between thermal resistance and the defect contents throughout the interface layer are also investigated. Based on our characterization work, we summarize the observations throughout the characterization scheme of interfacial thermal resistance of the heat spreader attachment in the four categories of void formations – materials, methods, environment and human factors respectively.

Materials Category:

- We have found that even the same solder paste alloy with no-clean flux (manufactured by different suppliers) has resulted in different void contents with the same reflow process.
- Void content is dependent on flux content and flux activity. On the preform samples, we added a thin layer of no-clean flux for air as well as nitrogen atmosphere. Addition of this flux increased the flux activity during a perform reflow compared to that of the solder paste reflow. It is most likely that the flux added to the preform had a higher fluxing action than the flux contained in the solder paste. Furthermore, a higher fluxing activity suggests that fluxing reaction and activator induced decomposition

are not the major sources of outgassing. On the other hand, the outgassing of the entrapped flux profoundly affects the void formation and a lower void content indicates a lesser amount of trapped flux. In the case of a solder paste, the flux is in direct contact with the surface oxide of the powders and the surface to be soldered. Consequently, during reflow, any residual oxide can be expected to have some flux adhered to it. In the case of solder preform with added flux, the higher activity flux usually eliminates the oxide more rapidly and more thoroughly, thus leaving fewer spots for the flux to adhere to.

- As the metal content of the solder increases, the amount of oxide on the metal surface also increases. In addition, with the increase of metal loading, the flux content decreases, thus increasing void content. Moreover, tighter packing of the solder powder may create more difficulty for entrapped flux to escape.

Methods Category:

- Higher dispensed or printed volume of solder paste results in higher void content. For thicker interfaces with a same joint area, we have observed more entrapped voids.
- In our sample preparation scheme, solder reflow profile is kept the same for the solder preform and the paste samples. As a result, we assume that solder profile did not affect the observed differences in void content.

Environment Category:

- Void contents in all cases of nitrogen reflow are consistently lower than the air-reflowed samples. In a reduced environment, the effectiveness of fluxing activity improves, thus reducing void content.

Human Factor Category:

- In our sample preparation scheme, all DBC pieces and copper coupons were given the same cleaning treatment before applying solder paste and silver epoxy. Therefore, the human errors are assumed to be the same in all prepared samples.

For an optimized heatspreader attachment process with minimized void content, we must ensure the following:

- use solder preform as the interface material
- use fluxes with higher flux activity;
- use inert reflow atmosphere to improve substrate solderability; and
- minimize surface roughness and maximize surface flatness.

In addition, during the reflow process, void content may be further minimized if the solder is allowed to melt without the module substrate on top. When solder is reflowed in a sandwiched structure, such as in our test samples, voids would inevitably get trapped between the layers. During reflow process, the lower density gases rise to the upper surface; however, the gases do not get the opportunity to escape the joint during molten state. Consequently, random sized voids are formed at the upper surface. Voids may be further reduced by processing the interface in a vacuum environment, which may add to the total manufacturing cost of processing.

Overall, this investigation has resulted in tailoring the conventional attachment process of the selected interface material, (which is typically ignored in the conventional module fabrication protocol), thus minimizing the void-content to ensure enhanced thermal management of power modules. Characterization of the interfaces of these tested samples has allowed us to establish a correlation between interfacial thermal resistance and void formation as a function of process variables, such as applied pressure and process environment. Furthermore, this research provided sufficient evidence for thermal modeling work to include contact resistance, which evidently constituted the largest part of the interfacial thermal resistance.

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