CHAPTER 3

SOFT-SWITCHED QSS BI-DIRECTIONAL INVERTER/CHARGER

3.1 Introduction

As reviewed in Chapter 1, besides some sporadic works on flyback-derived topologies for low-power applications [E21]-[E22], almost all of the developments in the direction of single-stage bi-directional inverter/charger (rectifier) have so far been concentrated on the various modulation and control aspects of the high-frequency isolated cycloconverter- or matrix converter-based topologies [E1]-[E20]. These topologies all involve four-quadrant switches, and their secure operation is always challenging [A65]. The associated PWM sequences are usually complicated.

For the reason of charger operation with power factor correction (PFC), various current-fed topologies have to be placed on the ac output (secondary) side. The effective clamping of the transient voltage appearing on the secondary side is extremely difficult for these topologies because of the complication by the bi-directional nature of the voltage on the secondary bridge. A bi-directional voltage clamp circuit is a necessity for higher power operation. Successful soft-switching schemes have hardly been developed, especially for

converters with a push-pull topology on the dc voltage-fed side where a zero-voltage across the voltage side of the transformer is not possible to create.

In this chapter, a new soft-switched single-phase quasi-single-stage (QSS) bi-directional inverter/charger is proposed. The topology can be derived from the QSS power conversion concept elaborated in Chapter 2, and can also be obtained with direct circuit manipulation. The resulting soft-switched QSS inverter/charger realizes seamless four-quadrant operation in inverter mode, and rectifier operation with unity power factor in charger mode. Simple center-aligned PWM control, single-stage power conversion, standard half-bridge connection of devices, soft-switching (either ZCS or ZVS) for all the power devices, low conduction loss, and high efficiency are among its salient features.

In the remaining sections of the chapter, the circuit topology is derived and its features are summarized in Section 3.2, while its detailed operation principles in both inverter and charger modes are discussed in Section 3.3. A seamless center-aligned PWM and control of the converter system are addressed in Sections 3.4 and 3.5, respectively, a design example and experimental results are presented in Section 3.6, and finally, in Section 3.7, the proposed single-phase QSS inverter/charger is extended to obtain other related bi-directional topologies and unidirectional PFC rectifiers, including a QSS isolated three-phase boost rectifier.

3.2 Soft-Switched QSS Bi-directional Inverter/Charger

3.2.1 Cycloconverter-Based Inverter/Charger

To facilitate discussion and comparison, the bi-directional cycloconverter-based single-stage inverter/chargers with a bi-directional active clamp branch is drawn in Fig. 3.1

[E7] [E12]. Considering the fact that the dc side is usually a low voltage battery, e.g. 12 V or 24 V, a voltage-fed push-pull topology is justified; the ac side voltage is usually much higher, e.g. 110 V or 220 V, and a full-bridge cycloconverter can be used, especially in cases where the power level is relatively high. Because it is desirable to achieve rectification with power factor correction (PFC) when the converter operates in charger mode, the output side has to be current-fed to achieve the required boost action.

The bi-directional active clamp circuit consists of four active switches, S_{c1} - S_{c4}, four directing diodes, D_1 - D_4, and a clamp capacitor, C_c. Coupled with a suitable PWM scheme, it can suppress the otherwise high transient voltage in the cycloconverter and achieve secure operation. However, some severe shortcomings exist in this circuit topology. They include: non-standard device connection in the cycloconverter which deters the use of standard half-bridge modules, high conduction loss on the output side including the clamp circuit, complicated active clamp circuitry and corresponding floating drives, and complicated PWM pattern.

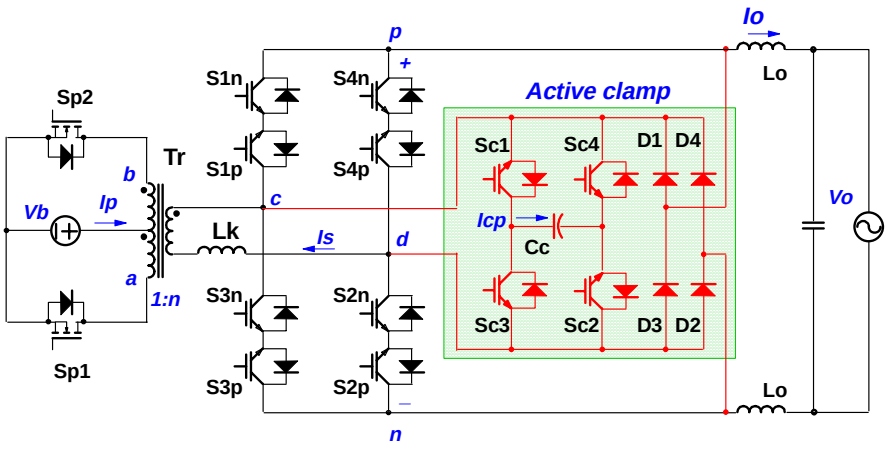


Fig. 3.1. Bi-directional cycloconverter-based single-stage inverter/chargers with a bi-directional active clamp [E7]-[E12].

3.2.2 QSS Bi-directional Inverter/Charger

3.2.2.1 Topology Derivation Using QSS Power Conversion Concept

A conventional two-stage bi-directional inverter/charger is shown in Fig. 3.2. Seen from the dc input side, it can be viewed as a voltage-fed or buck-derived isolated dc-dc converter and a voltage-source or buck inverter in cascading. Because of the bi-directional power flow requirement, each of the two sub-topology needs to be bi-directional.

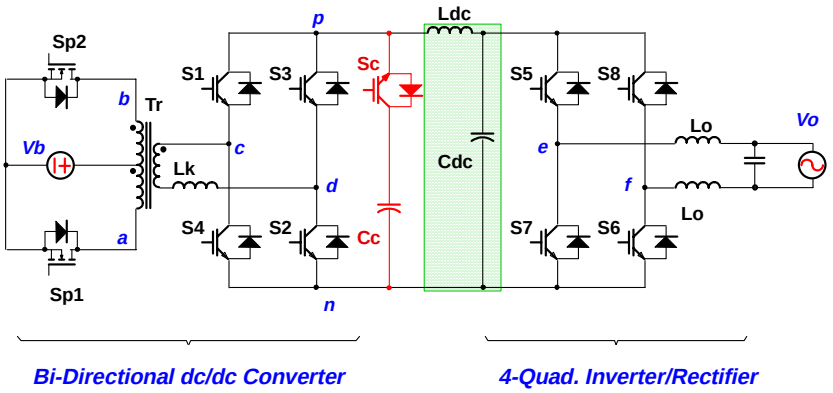


Fig. 3.2. Conventional two-stage bi-directional inverter/charger.

A simple clamp branch composed of S_c in series with C_c can be used to limit the unidirectional transient voltage across *p* and *n*, and achieve ZVS for the first bridge on the secondary side. However, without additional commutation circuitry, the primary push-pull circuit and the second bridge on the secondary side have to switch under hard switching. Also, voltage clamp circuit across primary push-pull switches is a must.

According to the QSS power conversion concept proposed in Chapter 2, the cascading nature of the two buck-derived sub-topology in the two-stage inverter/charger creates a possibility to realize a QSS inverter/charger with the elimination of the dc-link LP filter composed of L_{dc} and C_{dc}. The resulting soft-switched ASS bi-directional inverter/charger is shown in Fig. 3.3.

It is apparent that in the QSS inverter/charger, the active clamp branch is across both secondary bridges, referred to as bridge I and bridge II respectively, as shown in Fig. 3.3. So it is possible to realize soft-switching with that branch for all the power devices in the circuit without any additional circuitry, a clear advantage compared with the two-stage topology.

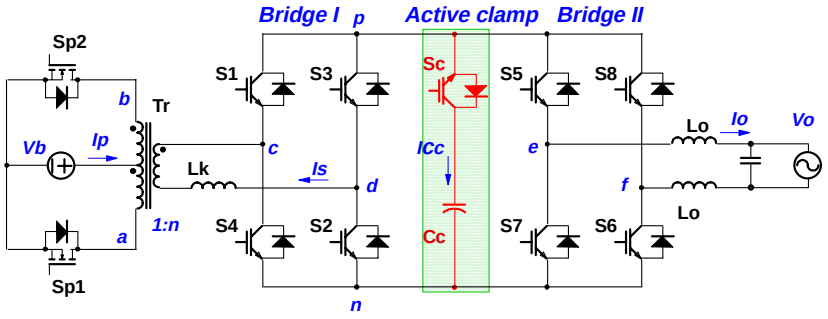


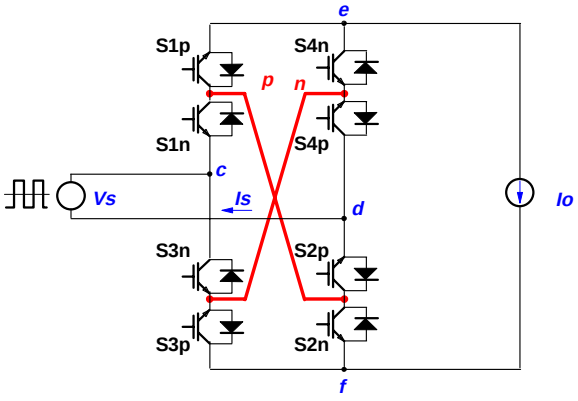
Fig. 3.3. Soft-switched QSS bi-directional inverter/charger with an active clamp.

The analysis in the next section will show that the PWM pattern can also be greatly simplified, and seamless control for four-quadrant operation can be easily realized with the proposed QSS inverter/charger. With the proposed center-aligned PWM pattern, soft-switching can be achieved for all the main power devices.

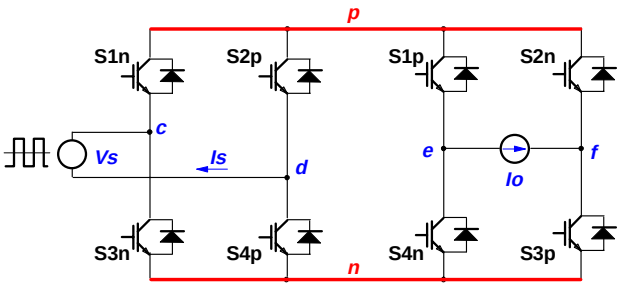
3.2.2.2 Topology Derivation Using Direct Circuit Manipulation

Scrutiny of the cycloconverter topology shown in Fig. 3.1 reveals the fact that shortcut freewheeling paths can be created for the output inductor current, I_o. As illustrated in Fig. 3.4(a) where the voltage across the secondary side of the transformer, V_{ab}, is represented by a square pulsating waveform, and the output inductor current, I_o, by a current source, by adding two extra conduction paths in the converter labeled as *p* and *n*, the output current can now freewheel through only one switch and one diode instead of two switches

and two diodes, thus halving the freewheeling conduction loss. Moreover, this is achieved without affecting the capability for syntheses of the output voltage, V_{of}.



(a) Addition of extra conduction paths.



(b) Stretching and redrawing of the circuit --- QSS topology.

Fig. 3.4. Topological evolution of the proposed soft-switched QSS bi-directional inverter/charger.

The circuit can be easily stretched along the created paths *p* and *n*, and redrawn as shown in Fig. 3.4(b). The resulting topology is exactly the same as the QSS topology shown in Fig. 3.3 which was derived above by means of the QSS power conversion concept. Apparently, the new topology is not only functionally compatible with the original cycloconverter, preserving the basic traits of single-stage power processing, but also has the standard half-bridge device connection. Compared with the original cycloconverter-based topology, the transient voltage clamp circuitry is also greatly simplified.

3.2.3 Features of the QSS Bi-directional Inverter/Charger

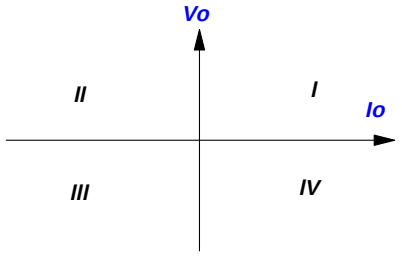
As discussed above, the proposed QSS bi-directional inverter/charger has the following salient features compared to other existing circuit topologies furnishing the same functionality:

- Reduced freewheeling conduction loss;
- Standard half-bridge circuit connection;
- Easier circuit layout;
- Much simplified voltage clamp circuit;
- Reduced loss in voltage clamp circuit;
- Soft-switching for all the power devices;
- Simplified PWM pattern and control;
- Seamless four-quadrant operation.

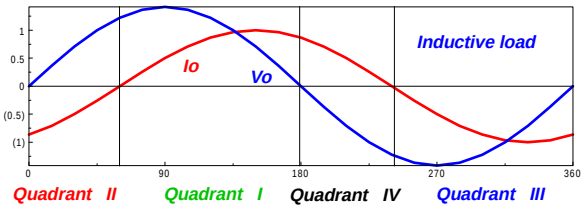
3.3 Operation Principles

In this section, the high-frequency operation principles of the QSS inverter/charger in each operation mode will be discussed. In inverter mode, because the load can assume any power factor, either leading or lagging, the circuit needs to operate in all the four quadrants in the V_o-I_o plane during an output line cycle as indicated in Fig. 3.5(a) and (b). So it is important to develop a seamless PWM pattern which ensures smooth transition between different quadrants. In charger mode, the circuit only needs to operate in quadrants II and IV, as shown in Fig. 3.5(c).

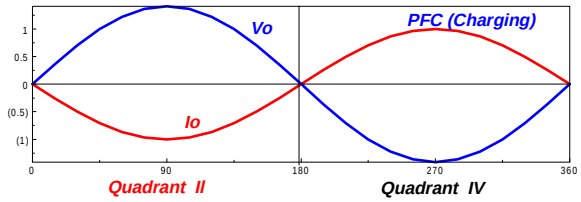
In the following analyses, it is assumed that all the power devices are ideal, and their output capacitance is represented by a lump capacitor C_{pn} (not shown in most of the drawings) across the buses *p* and *n*; and that the inductance of the output filter, L_o, is much higher than the leakage inductance of the transformer seen from the output side, L_k, so that the output current I_o can be considered constant during circuit commutations. The clamp capacitor C_c is temporarily assumed to be large enough such that the variation of its voltage during a high-frequency cycle can be neglected to facilitate the analysis. More detailed analysis about that will be given in the companion paper.



(a) Four-quadrant operation in the Vo-Io plane.



(b) Inverter mode.



(c) Charger (PFC rectifier) mode.

Fig. 3.5. Four-quadrant operation.

3.3.1 Inverter Mode Operation - Four-Quadrant Operation

In inverter mode, circuit operations in quadrants III and IV are exact replicas of those in quadrant I and II except that the PWM signals for the two pairs of diagonal switches in bridge II are swapped. So, only operations in quadrant I and II need to be considered.

To secure transitions between different operating quadrants, a basic invariant PWM pattern which is valid for all operation conditions is highly preferred. In this section, a center-aligned PWM scheme is developed to seamlessly control the QSS inverter/charger. All the necessary switch signals are derived from a simple PWM modulator which uses a triangular carrier. With this PWM scheme, the commutations for the primary push-pull circuit and the first bridge, bridge I as indicated in Fig. 3.5, are always separated from that in the output bridge, bridge II, and always take place when the ac load current is freewheeling in the output bridge. Consequently, all these commutations are lossless because no current needs to be switched. Moreover, 50% fixed duty-cycles are applied to all the switches in the primary side and bridge I, so the primary push-pull circuit and bridge I on the secondary side basically function as a *dc transformer*, which translates the voltage levels on both sides, while the sole objective of the commutations is to maintain the flux balance of the transformer. Real PWM signals are directed only to the output bridge together with the clamp switch.

3.3.1.1 Quadrant I: Inversion or Buck Operation

In quadrant I, both the load current and the required output voltage, V_o^*, which is derived from the feedback control loops, are positive, and power is transferred from the battery side to the output ac side.

In order for the primary side and bridge I to achieve lossless switching, it is mandatory to reset the transformer leakage current to zero during the freewheeling period of the output current. It can be shown that depending on the timing of the active clamp switch relative to the main switches in bridge II, different schemes are possible. Two such schemes will be illustrated below, with one discussed in more detail.

One such PWM pattern is shown in Fig. 3.6 for operation in quadrant I. It is apparent that the control signal for the clamp switch S_c coincides with the output voltage pulse and is the direct output from the PWM modulator with a proper turn-on delay. The equivalent active circuits in each interval within a half high-frequency cycle are drawn in Fig. 3.7.

[t_0-t_1]: Assume that a PWM cycle begins with the peak of the PWM carrier, then the switches on the primary side and bridge I reconnect at the beginning and in the middle of a PWM cycle, and is synchronized with the triangular carrier. At t_0, S_{p2}, S_3 and S_4 are closed under zero current, while the load current is freewheeling through S_6 and the antiparallel diode of S_7, D_7.

[t_1-t_2]: At t_1-ΔT_2, where ΔT_2 is the dead time between the half-bridge switches, S_7 is turned-off without interrupting the circuit operation because in quadrant I, the positive load current can only flow through its diode. At t_1, S_5 in bridge II is turned on, and I_o discharges the parasitic capacitance across the bus, C_{pn}, and the bus voltage decays to zero immediately. At the same time, the battery voltage is exerted on the transformer leakage inductance L_k, and the transformer secondary current I_s starts to ramp up. It should be mentioned that because of the existence of L_k, I_{s5} can only rise at a finite rate determined by nV_b/L_k, where n

is the turns ratio of the transformer as defined in Fig. 3.5. So the turn-on loss of S_5 is very low although it is not strictly ZVS.

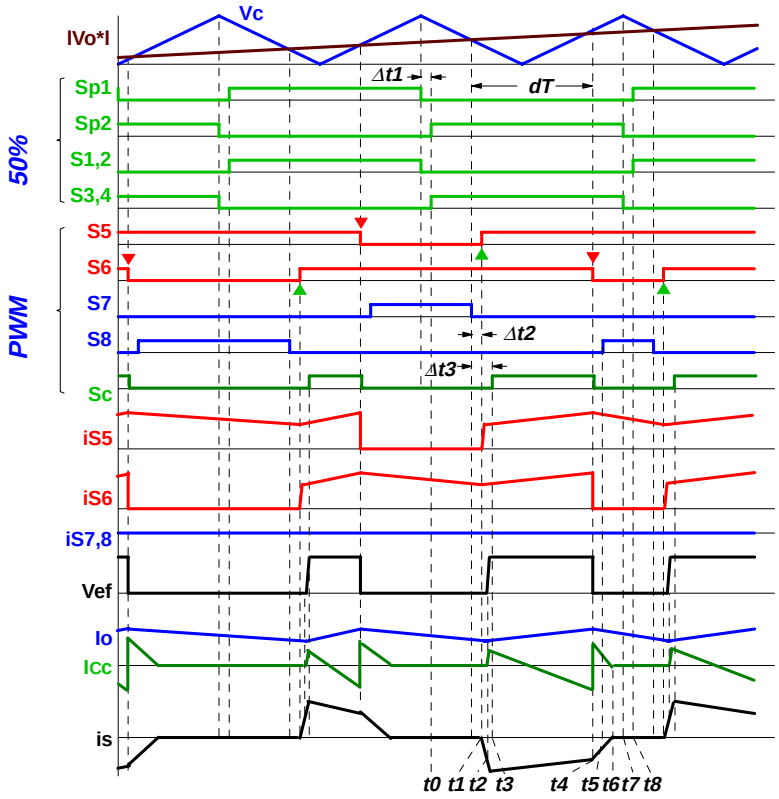
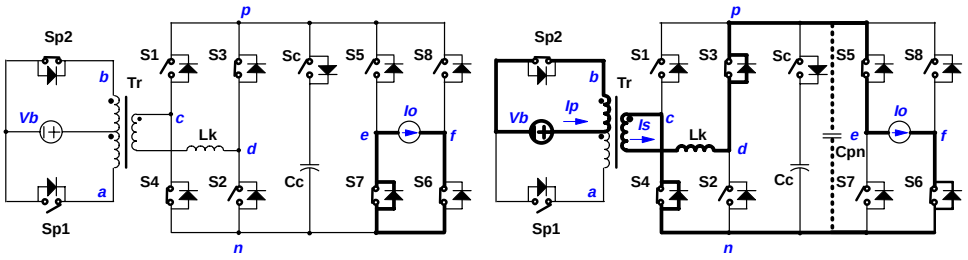


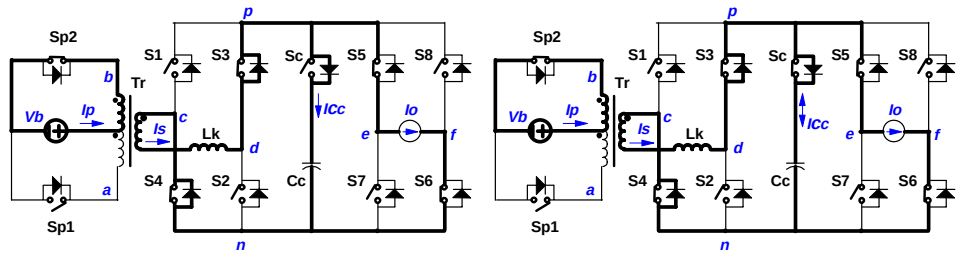
Fig. 3.6. PWM pattern and key waveforms in quadrant I.

[t_2-t_3]: I_s reaches the load current level at t_2, and after that, L_k resonates with C_{pn} to bring the bus voltage V_{pn} quickly up to the clamp capacitor voltage V_{Cc}, and the bus voltage is clamped to V_{Cc}. The resonance between L_k and C_c charges energy into C_c.

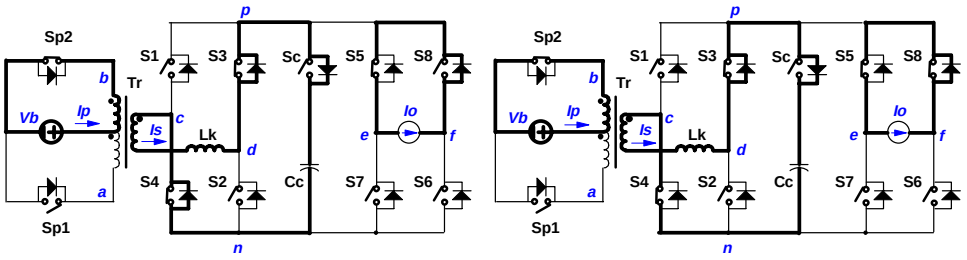
[t_3-t_4]: After a delay time of ΔT_3 from the turn-off of S_7, S_c is turned on under zero voltage. The resonance between L_k and C_c continues. Finally, I_{Cc} reverses its direction, and the energy charged into C_c is dumped to the output. During this interval, the amplitude of I_s keeps decreasing.



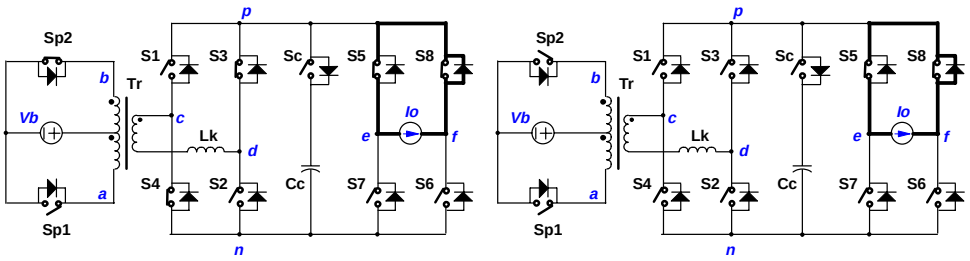
(a) [t0 - t1] (b) [t1 - t2]



(c) [t2 - t3] (d) [t3 - t4]



(e) [t4 - t5] (f) [t5 - t6]



(g) [t6 - t7] (h) [t7 - t8]

Fig. 3.7. Equivalent circuits in a high-frequency cycle in quadrant I.

[t_4-t_5]: Both S_c and S_6 are turned off at t_4, ending the on duty cycle. I_o freewheels through S_5 and D_8. Once S_6 is off, I_{Cc} immediately reverses its direction and the remaining transformer leakage energy charges C_c and L_k is reset.

[t_5-t_6]: At t_5, S_8 is turned on without any interruption to the circuit operation because its diode D_5 is freewheeling the load current.

[t_6-t_7]: I_s resets to zero at t_6, and remains quiescent. The only active part of the circuit is S_5 and D_8 which freewheel the output current.

[t_7-t_8]: At t_7, the primary side and bridge I start to commutate with S_{p2}, S_3 and S_4 turned off under zero current. At t_8, the other half switching cycle is initiated with the complimentary switches being active.

3.3.1.2 Alternative Timing

Figure 3.8 shows another PWM pattern for operation in quadrant I. Actually the only difference from the previous one is that the clamp switch is activated at the beginning of a carrier cycle while all the control pulses for the main switches are kept exactly the same. In this case, during the latter half of the load current freewheeling interval, a reverse current can be built up in the transformer leakage inductance, and that energy is used to discharge the bus voltage down to zero and create the ZVS condition for the bridge II switches before their turn-on. With this pattern, the leakage energy is very easy to reset and lossless commutation for the primary side and bridge I can always be ensured. The only shortcoming of this scheme is that during the on duty cycle, because the clamp switch is off and C_c holds a voltage higher than the reflected source voltage, parasitic ringing on the bus can happen in practice. More detailed analysis on this scheme will not be pursued here.

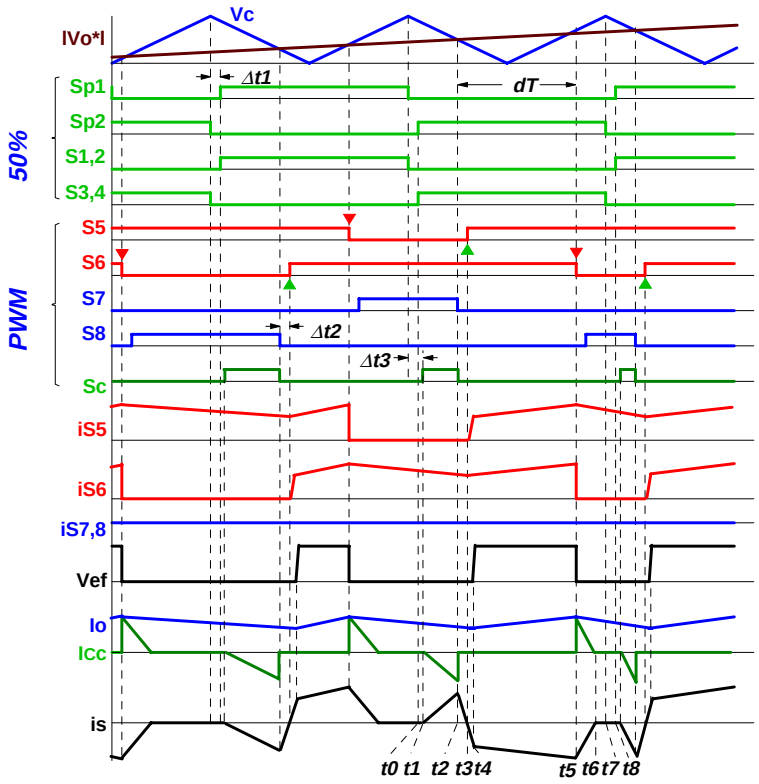


Fig. 3.8. Alternative PWM pattern in quadrant I.

3.3.1.3 Quadrant II: Rectification or Boost Operation

In quadrant II, the synthesized output voltage is positive, but output current is actually negative. This means that the circuit actually operates as an isolated boost converter, and power is transferred back to the battery. The operation is similar to that in rectifier (charger) mode. The PWM pattern and high-frequency waveforms are shown in Fig. 3.9, while the equivalent circuits in each interval are shown in Fig. 3.10. It is clear that the PWM pattern is exactly same as shown in Fig. 3.6 for operation in quadrant I.

[t_0-t_1]: The same as in quadrant I, the primary side and bridge I conduct lossless commutation at the beginning of a carrier cycle. The load current freewheels at bridge II.

[t_1-t_2]: S_7 is turned off at t_1, interrupting the freewheeling path. I_o charges up the bus capacitance rapidly.

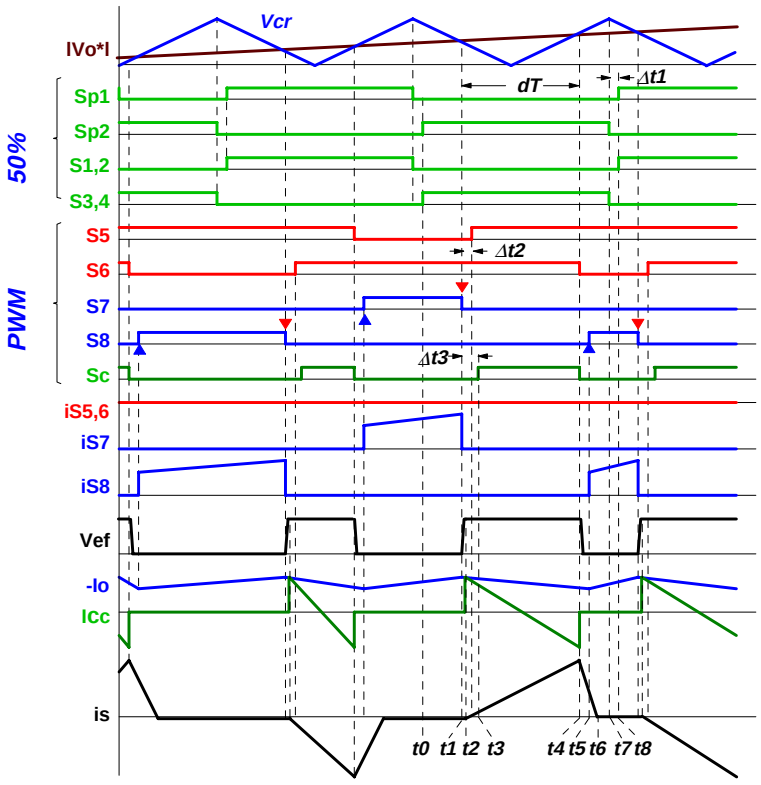


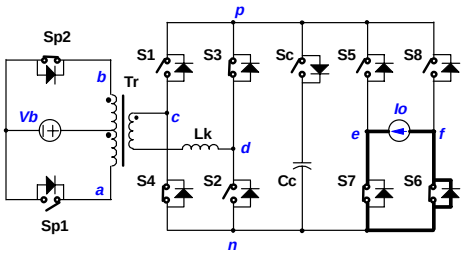
Fig. 3.9. PWM pattern and key waveforms in quadrant II.

[t_2-t_3]: At t_2, the bus voltage reaches V_{Cc}, and C_c is automatically engaged to clamp the bus voltage. The resonance between C_c and L_k makes I_s increase and energy is transferred to the dc side.

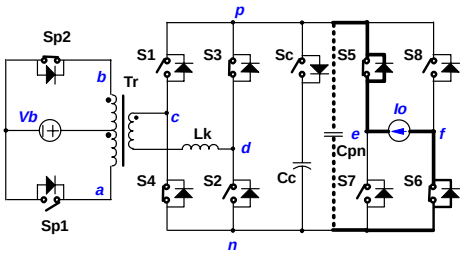
[t_3-t_4]: S_c is turned on under zero voltage at t_3, and I_{Cc} reverses direction later. The behavior of the circuit is exactly the same as other isolated boost converters with an active clamp branch [D6]-[D9].

[t_4-t_5]: S_c is gated off at t_4, the difference between I_s and I_o is used to discharge the bus voltage down to zero.

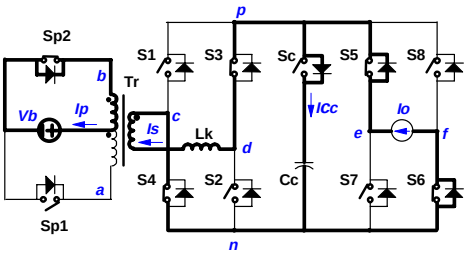
[t_5-t_6]: S_8 turns on under ZVS at t_5, and the output inductor is charged by the load voltage V_o. Meanwhile, I_s continues to be reset by the dc source voltage.



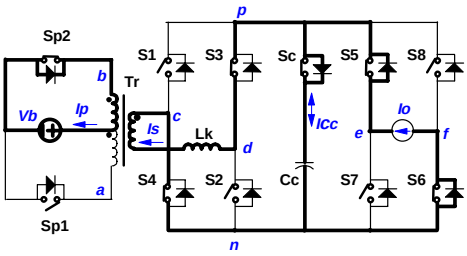
(a) [t0 - t1]



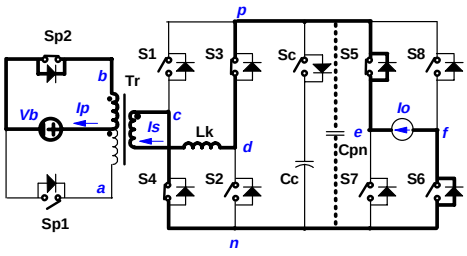
(b) [t1 - t2]



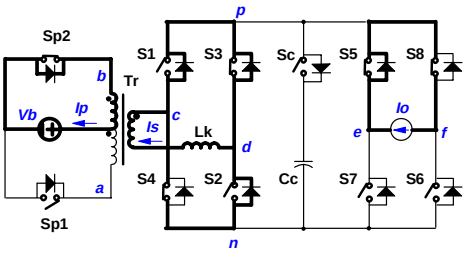
(c) [t2 - t3]



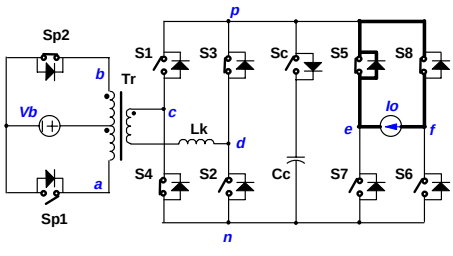
(d) [t3 - t4]



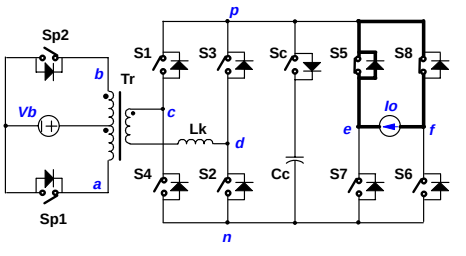
(e) [t4 - t5]



(f) [t5 - t6]



(g) [t6 - t7]



(h) [t7 - t8]

Fig. 3.10. Equivalent circuits in a high-frequency cycle in quadrant II.

[t_6-t_7]: I_s is completely reset at t_6, and kept quiescent.

[t_7-t_8]: At t_7, the primary side and bridge I start to commutate with S_{p2}, S_3 and S_4 turned off under zero current. At t_8, the other half switching cycle is initiated with the complementary switches being active.

It is clear from the foregoing analysis that the proposed center-aligned PWM scheme retains its basic pattern for four quadrant operations. When quadrant change happens, the circuit waveforms will assume different shapes under the same set of gate control signals. This invariant property is essential to simplify the control implementation and maintain highly reliable converter operation.

3.3.2 Charger Mode Operation --- Rectification with PFC

As indicated above, when operated in charger mode, the circuit realizes rectification of ac voltage with PFC, and operates only in quadrants II and IV. Theoretically, the same PWM pattern as in quadrant II presented above can be adopted. The only difference is that in this case, the control voltage is derived from a temperate generated from and synchronized with the available ac voltage. However, in practical terms, the bi-directional, four quadrant nature of the PWM pattern above may potentially leads to loss of control around the zero crossing area within an ac line cycle. The problem can certainly be solved by careful control circuitry design. However, one simple solution is to use a slightly modified PWM pattern for charger operation, which limits bridge II to operation only in two quadrants.

The resultant PWM pattern is shown in Fig. 3.11. Compared to the pattern for quadrant II in Fig. 3.9, it is revealed that the only modification made is that the control signals for S_5 and S_8 are shortened and the upper switches and lower switches are triggered

by the same pulses respectively. With this modification, the switches in bridge II are all off during the discharging interval of the output inductor, i.e. from t_1 thorough t_4+DT_2, and bridge II is basically degenerated into a diode rectifier bridge. As a result, energy in the output inductor can only be dumped to the dc side, the output inductor is ensured to get proper reset and any unwanted digression into operation in quadrants I and III is avoided.

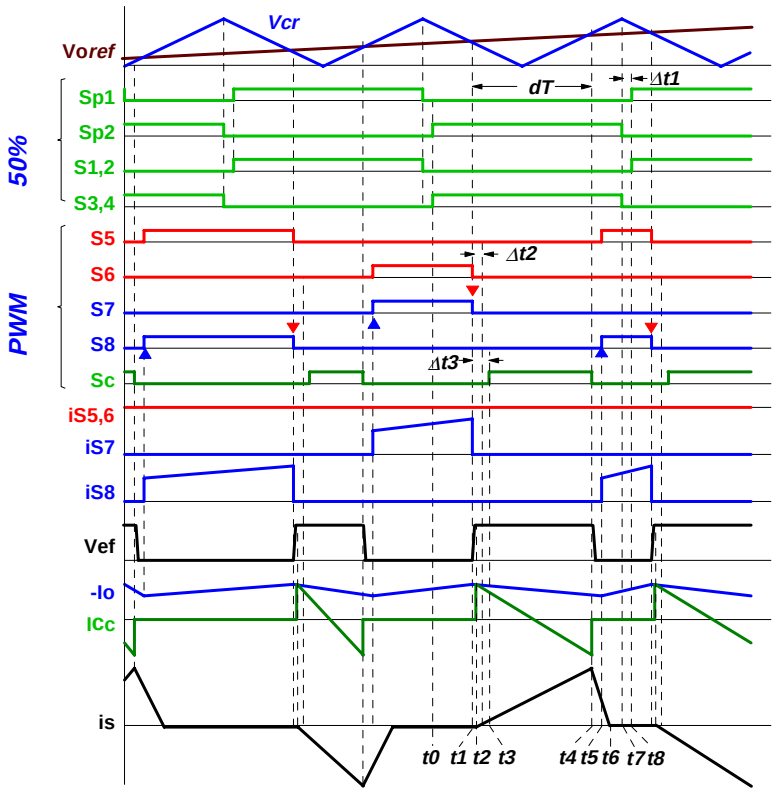


Fig. 3.11. PWM pattern in PFC rectifier mode.

Besides the issue discussed above, all the circuit behavior is the same as that of inverter operation in quadrant II, and the equivalent circuits shown in Fig. 3.10 are also valid except that from t_1 through $t_4+\Delta T_2$, S_5 and S_6 in bridge II stay off. So no further concentration on this topic is necessary.

Finally, it should be mentioned that for operation in quadrants II and IV in both inverter and charger modes, power is transferred to the dc side, so the push-pull switches S_{p1}

and S_{p2} need to function only as a diode. If activated as discussed above, they operate as synchronous rectifiers which can help to reduce the conduction loss on the primary side. However, during t_6 through t_1 in the next half switching cycle, the circuit composed of the primary side and bridge I basically works as a bi-directional dc-dc converter running in discontinuous current mode (DCM). As a result, parasitic oscillation between the leakage inductance of the transformer and the parasitic capacitance across the secondary bus, which will swing the bus voltage at high frequency and cause parasitic loss, is inevitable. One easy way to suppress it is simply to disable the push-pull switches. This modifies the otherwise bi-directional dc-dc converter into a unidirectional one, and most of the parasitic ringing paths are blocked.

3.4 Synthesis of PWM Patterns

The PWM patterns for all the main switches are invariant for operation in the four quadrants in inverter mode, so they can be synthesized with simple circuitry. As shown in Fig. 3.12, the 50% duty-cycles for the switches in the primary side and bridge I are directly obtained by dividing the PWM clock signal, *PWM_CLK*, with proper delay of ΔT_1 inserted between the complementary switch pairs.

A unipolar PWM modulator compares the rectified output voltage command $|V_o^*|$ (V_{oref} in charger mode) with the triangular carrier to obtain the basic PWM signal, *PWM*. All the driving signals for S_c and bridge II switches S_5 through S_8 are generated with some logic manipulation of that signal. The output voltage polarity signal from the controller is used to direct the two long and two short driving signals, as shown in Figs. 7, 9 and 10, to the diagonal switch pairs S_5 and S_6, and S_7 and S_8 in inverter mode. In quadrants I and II where

output voltage reference is positive and V_{o_pol} = 1, the long pulse pair is directed to S_5 and S_6, and the short pulse pair to S_7 and S_8; in quadrants III and IV where V_{o_pol} = 0, they are reversed.

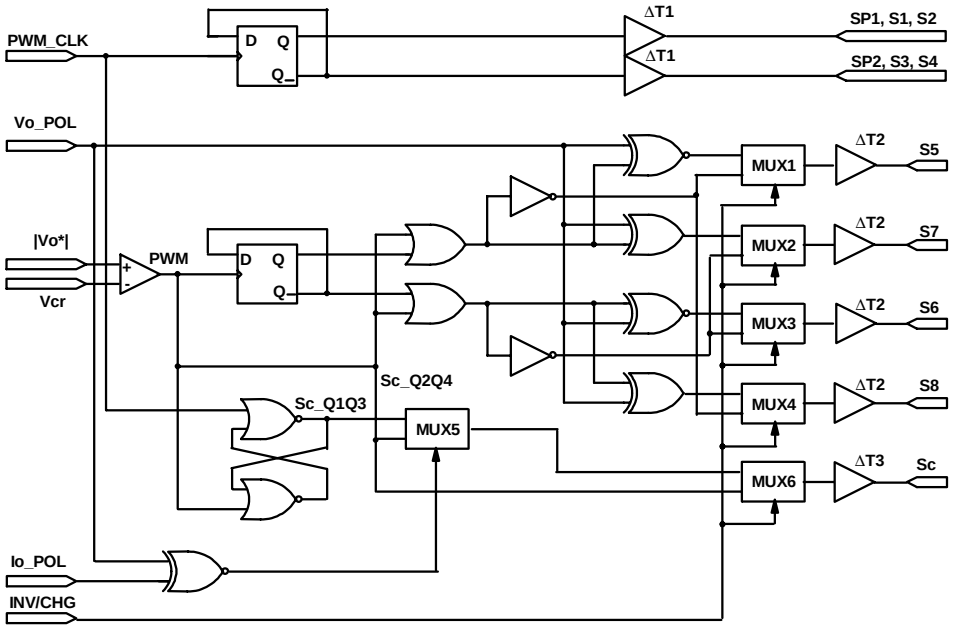


Fig. 3.12. Synthesis of PWM signals.

The PWM signals for inverter and charger modes are multiplexed by the mode control signal *INV/CHG*, and directed to the respective switches. If the PWM pattern shown in Fig. 3.8 is used in quadrants I and III, the control signal for S_c, S_{c_Q1Q3}, needs to be generated with the R-S trigger as shown, and the inductor current polarity signal, I_{o_pol} is used to select the appropriate one to use between S_{c_Q1Q3} and S_{c_Q2Q4} which is the same as *PWM*. Otherwise, if the PWM pattern in Fig. 3.6 is adopted, the position for S_c is invariant for all the bi-directional operating modes, and MUX_5 and MUX_6 can be eliminated and the inductor current polarity information is not needed.

It is noted that although throughout the above discussions, the center-aligned PWM scheme is exclusively considered, it is also possible to achieve similar performance with a

single-sided trailing or leading edge PWM scheme. In that case, the implementation of the PWM modulator is simplified because instead of using a triangular carrier, a saw-tooth carrier, which is normally easier to generate, is adequate.

3.5 System Control

The simplified block diagram of a typical single-stage bi-directional inverter/charger or line-interactive UPS system is shown in Fig. 3.13. when the alternative source, V_g, which can be a stand-alone engine/generator set or the utility line is not available, the inverter/charger operates as an inverter capable of four-quadrant operation, and converts the dc voltage, V_b, into an ac output voltage, V_o, at the line frequency to supply loads with various power factors. The dc source can be a low-voltage battery, or an alternative energy source with battery backup. Once the alternative source is available and stable, it powers both the load and the inverter/rectifier with the activation of the transfer switch, S_t; and the inverter/charger operates in the rectifier or charging mode to replenish the battery. It is usually preferred for the converter to absorb sinusoidal current from the ac source when it operates as a charger to make better utilization of the available ac capacity.

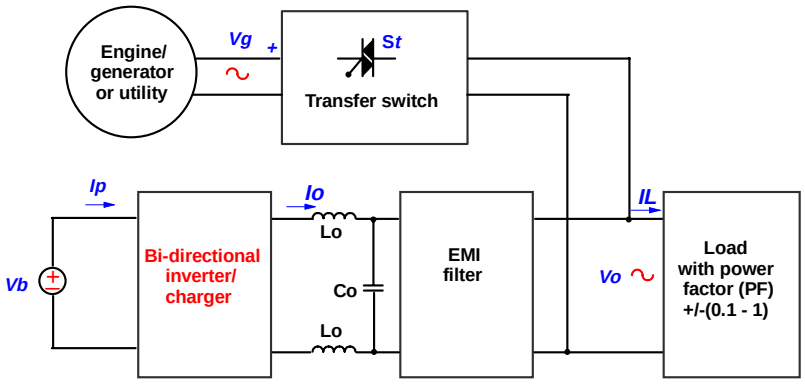


Fig. 3.13. Typical inverter/charger system and line-interactive UPS.

The block diagram of the system control functions necessary for bi-directional power flow control and regulation is shown in Fig. 3.14. The operation mode transfer and control block is responsible for deciding which mode to operate by sensing the availability of an external ac source, V_g, or according to the external or remote command. If V_g is not available, the transfer switch S_t is open, and the mode control switch is set to *INV* position, or $INV/CHG = 1$. In this case, the output ac voltage command V_o^* is given out by the output of the cascaded output voltage and inductor feedback loops. The output voltage reference is generated from a sinusoidal template, V_{sin}, which is always trying to be synchronized with V_g, if any, typically with the help of a phase lock loop (PLL). V_o^* is rectified and both its amplitude and polarity, V_{o_pol}, are fed to the unipolar PWM modulator. $|V_o^*|$ is then compared with the triangular carrier to generate the PWM patterns as discussed above. The bandwidth of the output voltage and current control loops should be designed to be as high as possible to achieve good load regulation and dynamic response, especially under nonlinear load.

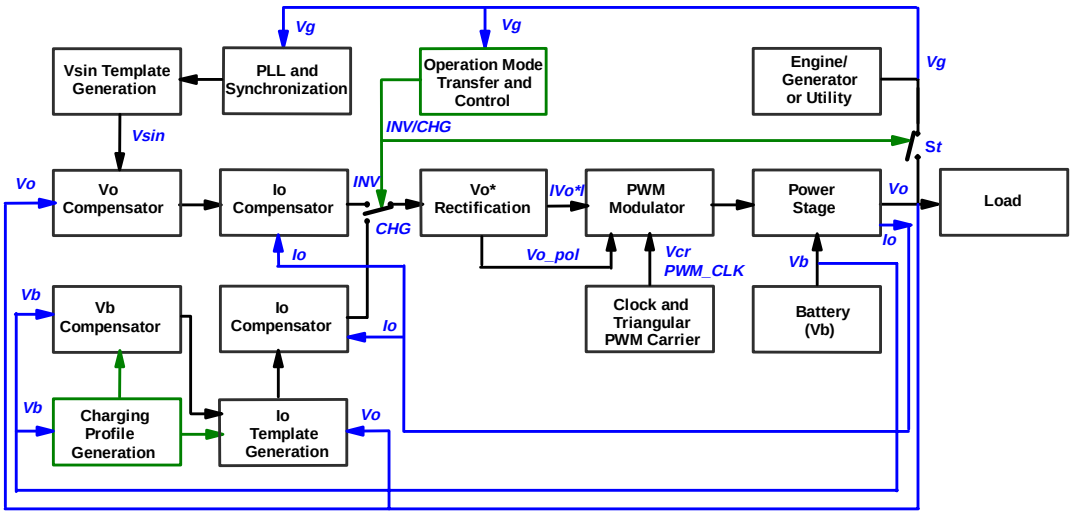


Fig. 3.14. Block diagram of the system control functions.

Once V_g is present, and switching to charger mode is desired, $INV/CHG = 0$, the control signal fed to the PWM modulator, denoted before as V_{oref}, is instead derived from the battery voltage and output inductor current feedback loops in the same way as in regular boost-based PFC rectifier. Certainly, more refined charging scenarios, such as three-stage charging, can be incorporated with the extra charging profile generation block which can override the usually slow battery voltage feedback compensator from time to time.

3.6 Prototype Implementation and Experimental Results

A prototype QSS bi-directional inverter/charger is designed according to the following specifications:

Input battery voltage V_b = 10 - 15.5 V (nominal value V_{bn} = 12 V);

Output ac voltage V_o = 120 V, 60 Hz;

Output power P_o = 3 kVA continuous, and 4 kVA for 3 minutes;

Output voltage THD < 5%;

Load power factor (PF) = +/-0.1 ~ 1;

Charging current I_{ch} = 150 A continuous up to V_b = 14.5 V.

To ensure appropriate voltage scaling in both inverter and charging mode operations, the turns ratio n of the transformer needs to be selected such that $n(V_b^{min} - V_{FET})D_M > V_o^{pk} = \sqrt{2}\, V_o$, where D_M is the maximum duty ratio in the inverter mode, and V_b^{min}, V_{FET}, and V_o^{pk} are the minimum input battery voltage, on-drop voltage on the primary MOSFET switches, and peak output ac voltage, respectively. If D_M = 0.9, V_{FET} = 0.5 V, and V_o = 120 V, then $n > 20$. In reality, n = 21 is selected.

The switching frequency for the prototype is selected to be f_s = 31 kHz, with the P'WM carrier frequency being doubled. The PWM pattern ensures the even distribution of switching losses among the active devices in the output bridge.

The high current and voltage justify the use of IGBT devices for the high side switches. Thanks to the QSS structure, standard low-cost half-bridge IGBT modules can be used. As discussed above, the switches in bridge I always operate under ZCS. As a result, their current rating can be much lower than those in bridge II. As a rule of thumb, devices with half the current rating of those in Bridge II are adequate for them.

On the primary side, the switches are also switched under ZCS. Therefore, there is no transient voltage problem normally related to the push-pull topology switching high current, and low voltage MOSFETs can be adequately used.

The main power stage parameters are as follows:

S_{p1}, S_{p2}: IR3205, 55 V/8 mΩ TO-220 MOSFET, 18 in parallel;

S_1/S_3, S_4/S_2: Toshiba MG50J2YS50, 600 V/50 A IGBT Module;

S_5/S_7, S_8/S_6: MG100J2YS50, 600 V/100 A IGBT Module;

S_C: IXYS IXGN200N60A, 600V/200A in parallel with IR HFA50PA60C diode;

C_C: EC 5MP22K145K, 600 V/1.4 μF film capacitor, 2 in parallel;

T_r: Philips E65-3F3 core, n_p:n_p:n_s = 1:1:21, L_k = 5 μH;

L_o: Magnetics MC1649-1B01 Metglas core, 26 turns, 50 μH each;

C_o: CDE 935C2W20K, 200 V/10 μF film capacitor, 2 in parallel.

Figure 3.15 shows the circuit waveforms in the charging mode under V_o = 120 V, and V_b = 12 V. The charging power P_{cb} absorbed by the low-voltage battery side is 1.4 kW,

and the input power factor reaches 0.973. Because of ZVS operation, the link voltage V_{pn} collapses to zero in every switching cycle, and its waveform is blurred. It is also evident that in the zero crossing area of the line cycle, V_{pn} is held down at zero because the duty cycle is saturated and the output inductor is charged during the compete switching cycles. It can also be seen that the link voltage is well clamped and it fluctuates during a line cycle because the clamp capacitor voltage is a function of the duty-cycle of the converter and the load (output inductor) current.

The test waveforms in the inverter mode with the output inductor current and output voltage feedback loops closed are shown in Fig. 3.16 under V_o = 100 V, V_b = 12 V, and output power P_o = 2.3 kW. It can be seen that output voltage with very low THD is generated and the fluctuation of the clamp capacitor voltage is larger than that in charging mode.

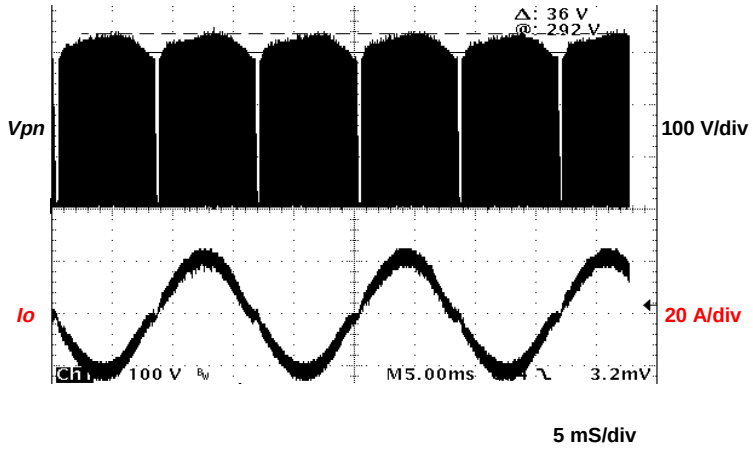


Fig. 3.15. Experimental waveforms in the charging mode with PFC. Upper trace: envelope of the link voltage V_{pn}; lower trace: output inductor current I_o. Test conditions: V_o = 120 V, V_b = 12 V, P_{ch} = 1.4 kW, PF = 0.973.

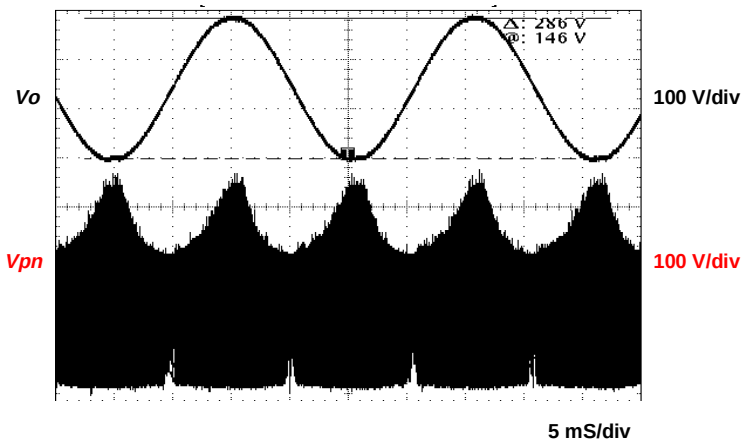


Fig. 3.16. Experimental waveforms in the inverter mode with close-loop control. Upper trace: output voltage V_o; lower trace: envelope of the link voltage V_{pn}. Test conditions: V_o = 100 V, V_b = 12 V, P_o = 2.3 kW.

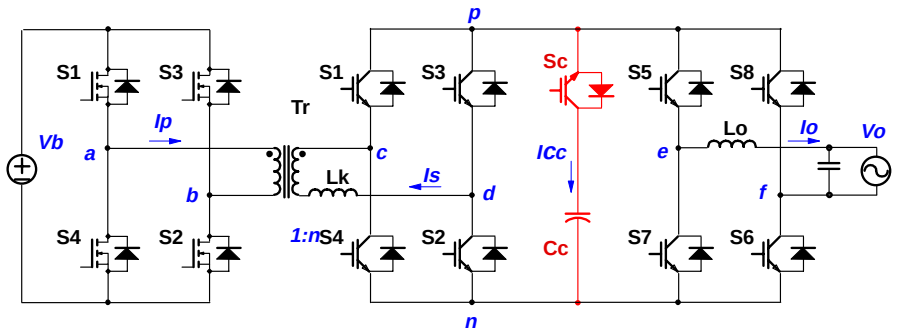
3.7 Extension of the QSS Bi-directional Topology

3.7.1 Other QSS Bi-directional Converter Topologies

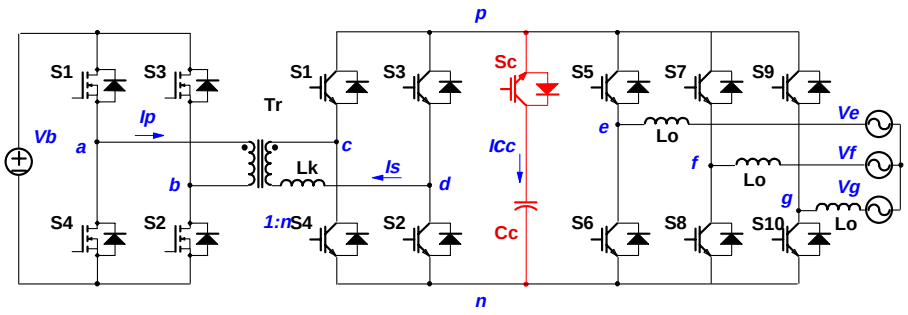
The analysis thus far has been limited to the QSS single-phase inverter/charger with a push-pull circuit on the input dc side. However, the QSS bi-directional inverter/charger topology is more general. In fact it can be easily extended to include circuits, for example, with a voltage-fed full-bridge on the dc side, or with a three-phase output bridge (bridge II), as shown in Fig. 3.17(a) and (b) respectively.

The full-bridge QSS converter possesses two important traits different from its push-pull counterpart. First, primary device voltage is automatically clamped to the input voltage; second, zero transformer excitation can be created by switching the primary full-bridge. As a result, it is possible to shift some of the PWM functions to the primary bridge without concerns about transient voltage on the primary side or incurring high circulation loss. In

fact, it is very beneficial for inverter operation in quadrants I and III when power is delivered to the output, and the power transferring path can be easily interrupted by switching the fast primary switches, usually implemented with MOSFETs. This results in the shifting of switching losses that otherwise happens in the output bridge (bridge II) to the dc side, and the total switching loss is further reduced.



(a) Full-bridge QSS inverter/charger.



(b) Three-phase QSS inverter/charger.

Fig. 3.17. Other QSS bi-directional inverters/chargers.

The three-phase QSS inverter/charger requires only five half-bridge configured switches, compared to 12 discrete switches mandated by the cycloconverter-based topology. Furthermore, all the other advantages of the QSS topology are retained.

3.7.2 QSS Isolated Three-Phase Boost Rectifier

In the case where only unidirectional PFC rectifier operation is needed, the QSS structure can be simplified. In a single-phase case, it can be simplified into a diode rectifier followed by a full-bridge with an active clamp branch, equivalent to the topology presented in [D7]. In the three-phase case, in order to shape the three-phase currents, the ac side bridges could not be simplified [B13]. But in both cases, only single-sided PWM and the corresponding saw-tooth carrier(s) are necessary. Certainly, the dc-side active switches can all be eliminated and replaced with diodes.

The circuits in this family all involve the isolated boost type of operation when the power is enforced to flow from the current-fed side to the voltage-fed side. Although with a simple active voltage clamp branch, the transient voltage can be effectively suppressed theoretically, the voltage overhead necessary on the clamp capacitor, and the transient voltage induced by the parasitic inductance in the layout may limit their applications in high-voltage, high-power off-line applications. For example, for typical telecommunication rectifier applications with a three-phase 380 V +/-20% input, and a nominal 48 V (40 -60 V) output, the steady-state voltage on the primary devices will be $1.414 \times 457 \times 1.5 = 970$ V even in ideal case. If the effect of the leakage inductance of the transformer is considered, the device voltage will be well above 1200 V. In these cases, the QSS isolated buck rectifiers which will be discussed in the next chapter may prove superior in performance.

3.8 Summary

A new soft-switched single-phase quasi-single-stage (QSS) bi-directional inverter/charger (rectifier) topology is derived based on the QSS power conversion concept

elaborated in Chapter II. It is functionally equivalent to the single-stage, cycloconverter-based topology, yet performance-wise, superior to the latter. A simple active voltage clamp branch is used to clamp the otherwise high transient voltage on the current-fed ac side, which is caused by the unavoidable leakage inductance of the transformer, and at the same time, to achieve ZVS for the switches in the output side bridge. Seamless four-quadrant operation in inverter mode, and rectifier operation with unity power factor in charger mode are realized with the proposed uni-polar center-aligned PWM scheme. Single-stage power conversion, standard half-bridge connection of devices, soft-switching for all the power devices, low conduction loss, simple center-aligned PWM control, and high efficiency are among the salient features. Experimental results on a 3 kVA bi-directional inverter/charger prototype validate the reliable operation of the circuit.

Although throughout the above discussions, the center-aligned PWM scheme is exclusively considered, it is also possible to achieve similar performance with the single-sided trailing or leading edge PWM schemes. In that case, the implementation of the PWM modulator is simplified because instead of using a triangular carrier waveform, a saw-tooth carrier waveform is adequate.

The proposed basic QSS inverter/rectifier topology can also be extended to include other single-phase topologies, such as the inverter/rectifier with a full-bridge primary circuit, and the three-phase bi-directional inverter/rectifier. In the three phase case, a QSS isolated three-phase ZVS boost rectifier can be easily obtained by replacing the dc-side switches with diode rectifiers in the bi-directional topology.

The performance limitation of the single-stage or QSS boost bi-directional inverters/rectifiers or isolated three-phase boost rectifiers for high-voltage applications is

also mentioned. The problem is intrinsic to the isolated boost type of converter. The QSS isolated buck ZVZCS rectifiers presented in the next chapter will avoid this problem and have superior performances.