Switching Stage Design and Implementation for an Efficient Three-Phase 5kW PWM DC-DC Converter

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Abstract

With the development of fuel cell based power systems, the need for more advanced DC-DC power converters has become apparent. In such applications DC-DC converters provide an important link between low voltage fuel cell sources and inverter buses operating at significantly higher voltages. Advancements in converter efficiency, cost reduction, and size reduction are the most necessary. These challenges are formidable, even when considering the improvements made to conventional DC-DC topologies. However, it can be possible to achieve these criteria through the implementation of more advanced topologies.

A recently developed efficient three-phase DC-DC topology offers benefits over standard designs. Passive component sizes and output ripple voltage were reduced as a result of an effective boost in switching frequency. Converter output voltage was reached more easily due to an increased transformer voltage boost ratio in addition to the turns ratio. For cost reduction, the converter was designed and built with discrete components instead of more expensive integrated modules.

This thesis presents an overview of the three-phase converter, with a detailed focus on the design, implementation, and performance of the switching stage. The functionality of the three-phase topology is covered along with the selection of converter components. Simulation results are shown for both ideal and real converter models. Considerations for the switching device package with respect to circuit board and heat sinking configurations are discussed in support of the selection of an insulated metal substrate (IMS) circuit board. An effective circuit layout designed to minimize parasitic trace inductances as well as provide favorable component positioning is presented. Experimental converter test results are shown and the causes of undesired effects are identified. Switching stage modifications and their results are discussed along with the benefits of proposed future design enhancements.

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Chapter 1. Introduction

In the field of distributed power generation, DC-DC converters are an important link between low voltage fuel cell sources and 60Hz inverters. A number of conventional and novel DC-DC boost topologies have been applied; with some more suited to specific input and output voltage and current requirements. Fuel cell sources typically provide low voltages which are a function of a number of parameters such as the type of cell and the stack structure used. In order to provide a bus voltage large enough for a 120/240V inverter, the fuel cell voltage must be boosted significantly. For this application, an isolated topology is favored for converter optimization. The three-phase DC-DC converter discussed herein provides a favorable method of boosting a fuel cell voltage for an inverter input. A source voltage ranging between 22V and 48V was established to correspond to a specific solid oxide fuel cell (SOFC) voltage range. For sufficient inverter input voltage margin, a 400V converter output was desired for the entire fuel cell input voltage range. To meet these criteria, the converter consists of a switching stage, a transformer stage, and an output rectifier and filter stage. The focus of this study is the design, construction, implementation, and functionality of the switching stage in its interaction with the transformer stage. Since the operation and interactions of all three stages define the overall converter functionality, they are introduced in detail.

1.1. Half-Bridge and Full-Bridge Topologies

Isolated converter topologies provide advantages in applications requiring large voltage conversion ratios. Transformer isolation can reduce switch and diode device stresses and allows multiple windings or taps to be used to for multiple converter outputs. [1] Two of the most widely used isolated topologies are the half-bridge and full-bridge. Although the half-bridge is more often applied in buck type topologies, its design offers tradeoffs even in boost applications. The full-bridge is a popular design for both buck and boost applications and has become a basis for numerous resonant zero voltage and zero current switching (ZVS, ZCS) schemes. Its design

and functionality offer benefits over other conventional isolated topologies, including the half-bridge. However, it is also subject to tradeoffs which may render it less than optimal for particular applications.

The half-bridge has a low component count, and is therefore less complex than most other topologies. The schematic of a typical half-bridge converter having a diode bridge rectifier is shown in Figure 1-1. Switches S1 and S2, belonging to the same phase-leg, alternately conduct to avoid shoot-through current from the DC source. This produces a primary winding voltage polarity reversal after each switching half cycle to produce both positive and negative transformer magnetizing currents, which is referred to as bidirectional magnetization of the transformer. [2] Therefore, the entire B-H loop of the transformer core can be utilized. [1] This also facilitates transformer volt-second balance to avoid saturation of the transformer core. However, the main disadvantage of the half-bridge topology in boost applications is source voltage utilization. During each half of the switching cycle, a primary transformer voltage of only half the input bus voltage is used. This often requires larger transformer turns ratios to achieve desired output voltages. Furthermore, switch voltage stress remains equal to the full input voltage, while switch current stress is high to compensate for lower primary side voltage.

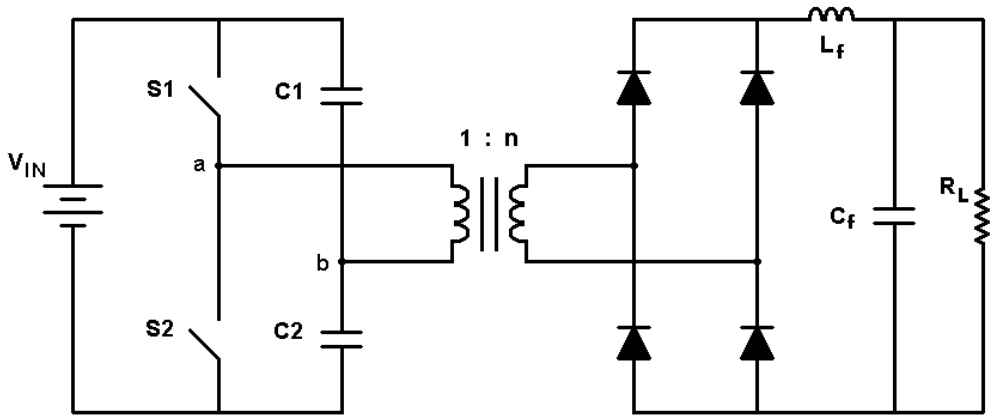

Figure 1-1. Half-bridge topology with full-bridge diode rectifier

The half-bridge can be a cost effective solution for lower boost ratios and lower power levels owing to its simplistic design. At larger boost ratios and higher power levels switching

device and/or transformer costs can become prohibitive. [1] Other design provisions may also need to be made to ensure voltage balancing between switching stage capacitors.

The full-bridge topology eliminates the large switching stage capacitors of the half-bridge, but requires more active devices. A typical full-bridge converter having a diode bridge rectifier is shown in Figure 1-2. For basic pulse width modulation (PWM) operation of the switching stage, switches S1 and S4 simultaneously conduct during one half of the switching cycle, and S2 and S3 conduct during the other half cycle. Like the half-bridge converter, this allows full transformer core utilization and inherent volt second balancing. Yet, unlike the half-bridge, full-bridge primary voltages are equal to the source voltage. Thus, full-bridge transformer turns ratios and switch currents need not be as high to achieve an equivalent voltage boost. Switch voltage stress remains equal to the source voltage. [1]

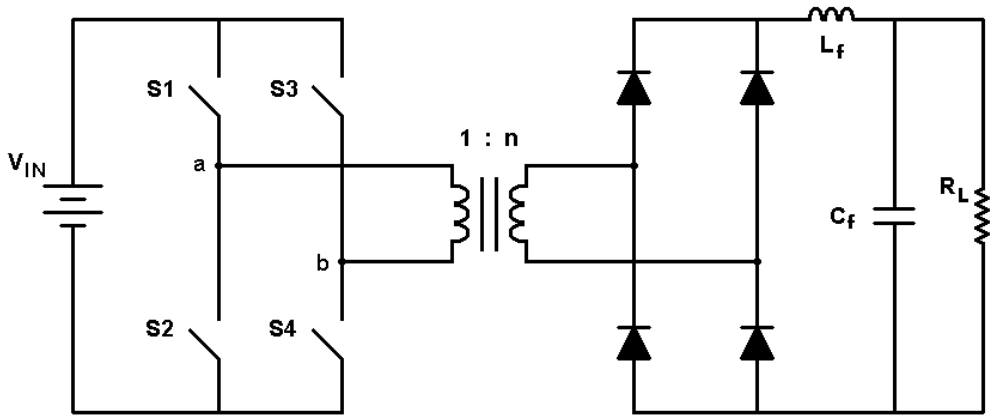

Figure 1-2. Full-bridge topology with full-bridge diode rectifier

The full bridge proves to be a favorable and versatile topology for higher power levels at or above 1kW. Although it has a higher active component count than other isolated boost topologies, device stresses are lower. It is also a favored candidate for soft switching implementation. Often in high power applications a phase shift modulation (PSM) switching scheme is used to achieve ZVS and/or ZCS transitions through the interaction of converter parasitic energy storage elements. [3] Despite its numerous advantages, the full bridge is not always the overwhelming choice for high power boost applications having low source voltages. This is because two switch voltage drops are suffered during each conduction interval. [1] With

significant reductions in semiconductor device conduction losses over the past several years, this factor has become a less of a concern. In fact, it can provide an advantage over other two-switch topologies to aid primary voltage balancing by allowing switch conduction drops to change slightly in the presence of small imperfections in switch timing and conduction drop. [1]

1.2. Push-Pull and Center-Tapped Secondary Topologies

Unlike the half-bridge and full-bridge topologies, the push pull topology uses a center-tapped primary transformer winding configuration. The design offers some advantages over the bridge-type converters, but also exhibits limitations. This is also true for the center-tapped rectifier configuration, which can be applied to either the push-pull or bridge topologies.

The push-pull topology is often used for boost applications having low source voltages. The primary side circuit consists of two alternately conducting switches connected to the source and the center-tapped transformer as shown in Figure 1-3.

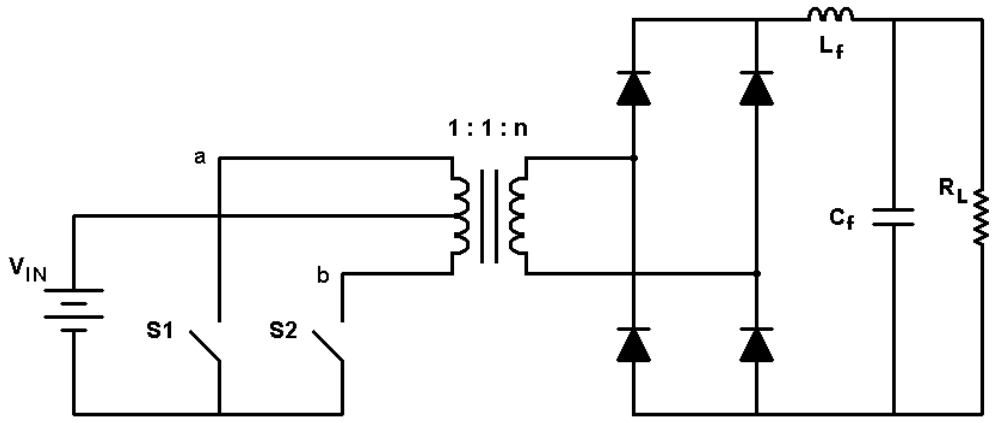

Figure 1-3. Push-pull topology with full-bridge diode rectifier

During each half of the switching cycle, the source voltage is placed across one half of the primary winding with the positive pole remaining at the center tap. Therefore, the full source voltage is utilized, and bidirectional magnetization of the transformer is achieved for full transformer core utilization. These benefits are the same as the full-bridge topology and are achieved with only two switches. Compared to the full-bridge, only one switch conduction loss

is suffered at any time during the switching cycle. Furthermore a reduced device count can provide cost advantages over the full bridge topology. The benefits of this topology have made it popular for applications similar to the one considered in this study. [2,4,5]

However, the push-pull topology has disadvantages. Because only half of the primary transformer winding is used during each switching half cycle, transformer winding utilization is less optimal than in the bridge topologies. [1] For larger primary currents, transformer size may need to be increased to accommodate larger primary windings. Switch voltage stress is also larger than in the bridge topologies. Twice the source voltage appears across a switch during the opposite switch conduction interval. [6] The push-pull converter is also highly susceptible to what is referred to as transformer staircase core saturation. [6] Transformer volt-second imbalances during each switching period compound to produce a net increase in magnetizing current after each switching period, causing core magnetization to step up or down the B-H loop. [7] Although the same switch timing and conduction drop imbalances often occur in the bridge topologies, they are not exacerbated by primary winding asymmetries. Physical asymmetries between the two halves of the center-tapped push-pull primary winding contribute to uneven primary side voltages during the same switching period. Because both the half-bridge and full-bridge topologies use a single non-center-tapped winding, they are immune to this problem.

The center-tapped rectifier configuration is similar to the front stage of the push-pull converter and has many comparable features. It uses two diodes instead of the four required by the full-bridge rectifier, and is shown in Figure 1-4.

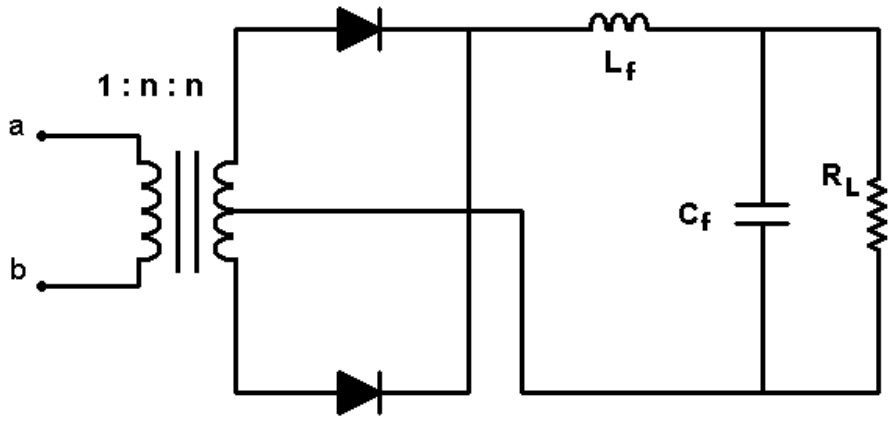

Figure 1-4. Center-tapped secondary side rectifier

The center-tapped rectifier is sometimes used in place of the full-bridge rectifier when fewer diodes and lower conduction drops are desired. Because only one diode conducts in the center-tapped configuration during each switching half cycle, only one diode forward voltage drop is suffered. However, diode voltage stress is equivalent to twice the output voltage, and only half the transformer secondary is used during each switching half cycle.

In most high power, high output voltage applications the benefits offered by the center-tapped rectifier do not outweigh its disadvantages. The transformer secondary winding configuration is more complex, and thus more costly than that of the full-bridge. Furthermore, the cost savings of using only two diodes is offset by the increased cost of diodes having twice the blocking voltage rating. And the reduction in total forward diode voltage drop is nearly insignificant in the presence of high converter output voltages.

1.3. Three Phase Converter Topology

1.3.1. Switching Stage

A three-phase converter improves upon the benefits offered by the full bridge topology. As in a typical DC-DC converter, the three-phase switching stage chops the DC input to create a pulsating voltage waveform for transformer excitation. The switching stage, which is shown in Figure 1-5, consists of three half-bridges in a parallel configuration. As in typical bridge topologies, the upper and lower switches in each of the three phase-legs are alternately switched. The PWM switching sequence of all three phase-legs is identical but not synchronized. Each phase-leg switching period is phase shifted 120 deg from the one preceding it. The voltage waveforms across the bottom switch of each phase-leg are shown in Figure 1-5 for a duty cycle slightly below 33.3%. Although the phase shift angle can be modulated (PSM) as a converter output voltage control parameter, pulse width modulation (PWM) was the only output voltage control parameter used in this study.

The phase shift provides an interleaved three-phase voltage waveform to the input of the transformer stage. This interleaved sequence must produce balanced excitation of the transformer windings, to avoid core saturation and winding current imbalances. Interleaving also

provides a switching frequency advantage by causing the overall transformer stage frequency to be effectively three times the switching stage frequency. After rectification, the effective transformer output frequency is doubled, to six times the switching frequency. The increased rectifier output frequency provides two main benefits. The switching stage can operate at a lower switching frequency to reduce switching losses, and smaller passive output filter components can be used to satisfy converter output ripple voltage specifications.

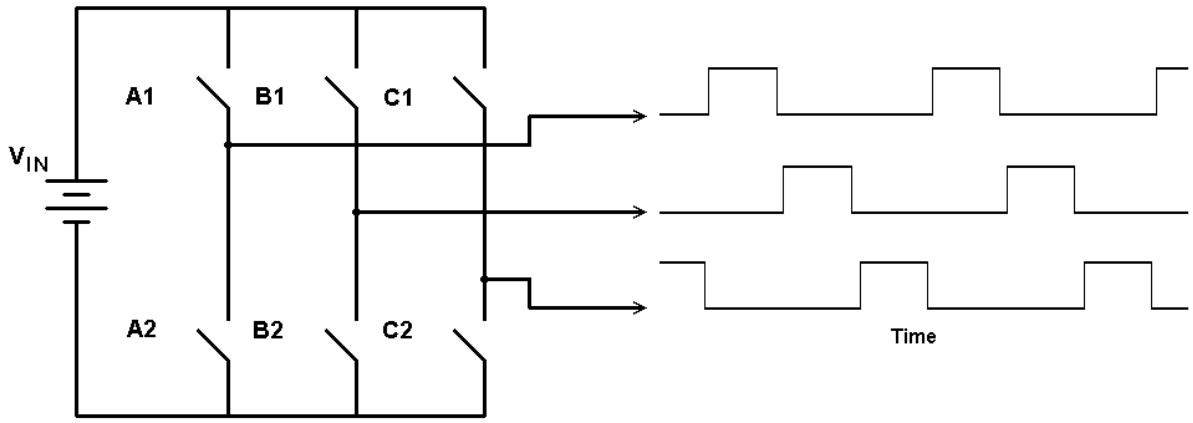

Figure 1-5. Three phase switching stage and midpoint voltage waveforms

Although six switches are required, switch voltage stress is equal to the source voltage, while average switch current stress is reduced below that of the full-bridge configuration. For larger duty cycles in which three switches simultaneously conduct, the two switches on the same side of the DC bus will share the current of the remaining switch. Ideally, this produces an average switch current of approximately 2/3 of the source current for duty cycles approaching 50%. As a result, switch conduction losses are also reduced. Like the full bridge, the three-phase topology also allows zero voltage switching (ZVS) to be achieved. This condition is dependent upon the existence of parasitic elements of the switching stage and the transformer stage, namely output capacitance at the switching device and transformer leakage inductance. Phase-leg dead-time also plays an important role in ZVS for the PWM controlled converter.

1.3.2. Transformer and Output Stages

The transformer stage of the three-phase converter consists of three pairs of primary and secondary windings. The transformer voltage conversion is increased by the winding connections, in addition to the boost provided by the transformer turns ratio. The primary windings of the transformer are connected in a delta configuration with the secondary connected in a wye configuration as shown in Figure 1-6. Although a larger number of windings are required, the transformer winding utilization is similar to the full-bridge topology. When top and bottom switches of the three-phase bridge are conducting, all three primary transformer windings are used. However, as with the primary winding of the push-pull, the three primary windings of the three-phase transformer along with their interconnections must be physically balanced to help prevent staircase core saturation.

Leakage inductance is an important transformer parameter occurring in all transformer isolated topologies, and affects converter efficiency. It is the inductance that is associated with the amount of uncoupled flux between the primary and secondary transformer windings. Unlike transformer magnetizing inductance, energy stored in the leakage inductance is not transferred between the primary and secondary windings. [1] Instead, it is dissipated between the transformer and the switching stage during each switching cycle, unless a ZVS condition is achieved. Therefore, leakage inductance is typically classified as a parasitic element which reduces converter efficiency. Variations in transformer structure can reduce leakage inductance.

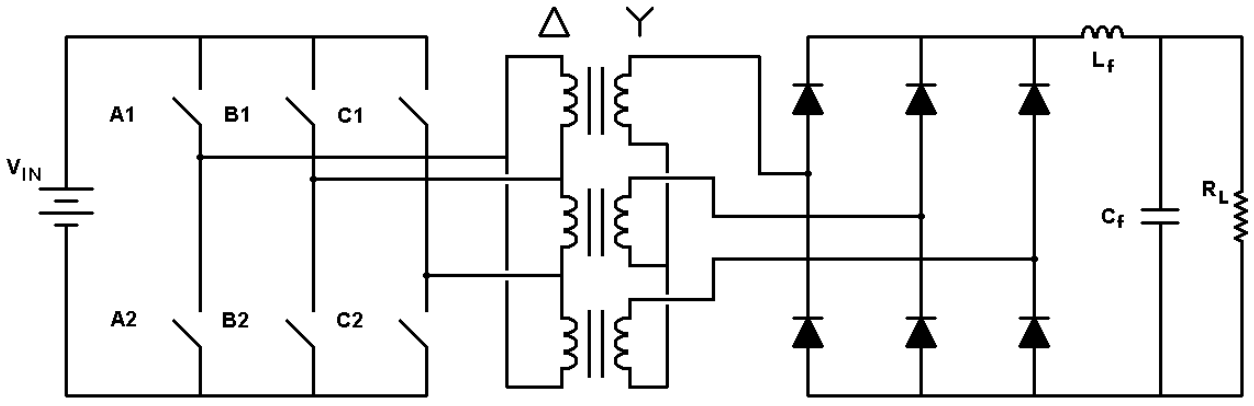

Figure 1-6. Three-phase transformer and output stage configuration

The converter output stage rectifies and filters the three-phase boosted output. The transformer stage is followed by a six-pulse diode rectifier and an output filter as shown in Figure 1-6. The six-pulse rectifier is similar to the full-bridge rectifier with an additional diode bridge. It offers many of the same tradeoffs in component count and cost versus functionality. Yet unlike the full-bridge or center-tapped rectifiers, which produce a ripple voltage of twice the switching stage frequency, the six pulse rectifier doubles the three phase interleaved transformer output frequency to provide a ripple voltage of six times the switching stage frequency. In this case, a second order L-C filter is able to provide better ripple voltage attenuation. Capacitor and inductor sizes can be smaller to achieve a desired ripple magnitude. However, a large capacitor value is used in this design to provide high side energy storage for voltage regulation during load transients. This further reduces output voltage ripple.

1.3.3. Split Output Voltage Bus

The output stage shown in Figure 1-6 provides a single DC voltage output. For the 120/240V inverter design chosen, a split 400V DC output bus was needed with a common midpoint connection. The converter output was split by using two secondary transformer windings of an equal number of turns. Like the first set of secondary windings, the second set is also connected in a wye configuration. The output of the second set of transformer windings is rectified and filtered by a second output stage. The two isolated converter outputs were cascaded together to form a split 400V output bus with a common midpoint as shown in Figure 1-7.

There are both advantages and disadvantages for the split output bus configuration. The most noticeable of these is the disadvantage of using a larger number of secondary side components. Although an extra filter inductor and filter capacitor would be needed for any typical split bus configuration, an additional six diodes are used in this design. Doubling the output side component count increases converter size, weight, and cost. The transformer has also become more complex by requiring two sets of secondary windings with an equal number of turns. Although the overall number of secondary winding turns is roughly the same needed for a single 400V converter output, the total number of secondary turns should also be even in number to produce symmetric output voltages. This limitation could increase the number of secondary

turns needed to achieve an output voltage level. With an increased transformer turns ratio, higher output voltages are yielded for the same converter control parameters. However, the effect is mitigated by high turns ratios, and is therefore less problematic in this converter design.

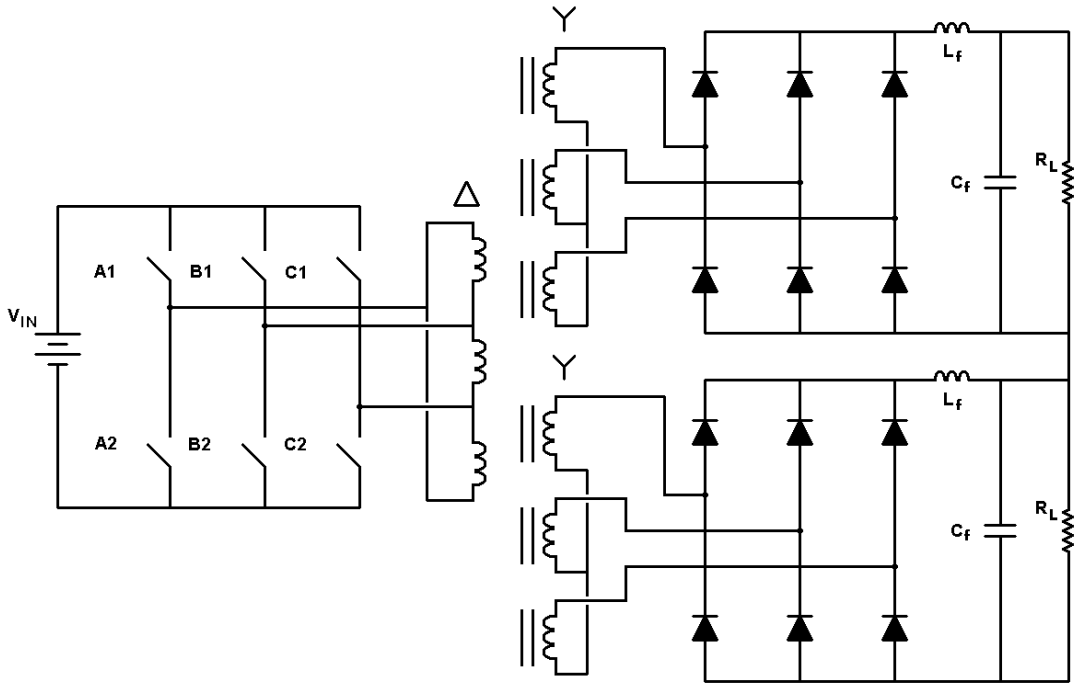

Figure 1-7. DC-DC converter design with split output voltage bus

Although increasing the number of output stage components is a disadvantage both physically and cost-effectively, reductions in component ratings offset these disadvantages by reducing component cost and improving functionality. Reduced diode voltage stress allows rectifier diodes having a lower breakdown voltage rating to be used. Device characteristics such as forward voltage drop, reverse recovery time, and peak reverse recovery current as well as device cost can be reduced. The output filter capacitor voltage requirement is halved in this configuration, reducing capacitor size and cost. Furthermore, capacitor voltage balance issues requiring additional control considerations for other split output topologies are not a factor in this design.

Chapter 2. Converter Design

2.1. Ideal Converter Modeling and Simulation

2.1.1. Preliminary Converter Simulation

Initial modeling and simulation of the converter system was performed with Saber software. Nearly ideal component models were used during early converter simulations in order to verify system operation. For the switching stage, a switch having a parallel body diode was the model used to approximate switching device behavior. This model was selected to verify system operation because of its simplicity. A switching frequency of 33.3kHz was used for phase shifting convenience. However, it was not possible to conduct the simulation with a perfectly ideal model due to convergence errors. Therefore, a switch on-time resistance of 1uΩ and a diode forward voltage drop of 1mV were used to conduct nearly ideal simulations.

The transformer stage was initially modeled in its original one secondary winding configuration as shown in Figure 1-2. Three single-phase ideal DC-DC transformers were connected in a delta-wye configuration. With the assumption that the transformer delta-wye connection would provide a constant voltage boost factor of $\sqrt{3}$ in addition to the turns ratio as in the sinusoidal voltage case, a maximum duty cycle value was selected and the turns ratio was calculated intuitively using (2.1). $V_{IN\text{-}min}$ is the minimum converter input voltage, N is the transformer turns ratio, d_{max} is the maximum operating converter duty cycle, and V_O is the converter output voltage.

$$V_O = V_{IN-\min} \cdot N \cdot \sqrt{3} \cdot \frac{d_{\max}}{0.5} \tag{2.1}$$

The ratio $d_{max}/0.5$ expresses the average duration of input voltage conduction per switching cycle, where 0.5 represents the theoretical maximum duty cycle of 50%. A maximum operating duty cycle value was selected to maintain a safe operating margin from the phase-leg shoot

through condition. Using values of $V_{IN\text{-}min} = 22V$, $d_{max} = 0.45$, and $V_O = 400V$, N was calculated to be 11.66. Therefore, a turns ratio of 1:12 was used in the simulation model.

The rectifier and output filter were also modeled ideally. The six-pulse rectifier was constructed using power diode models (again with 1mV forward voltage drop), and output filter components were modeled without ESR values. Capacitor and inductor values of 100uF and 100uH respectively were used to shorten simulation time.

Simulation results for the minimum input voltage operating condition described above are shown in Figure 2-1. The six switch gating waveforms over one switching period are shown in the top plot. Their labels denote phase-leg and switch position; top (p) or bottom position (n).

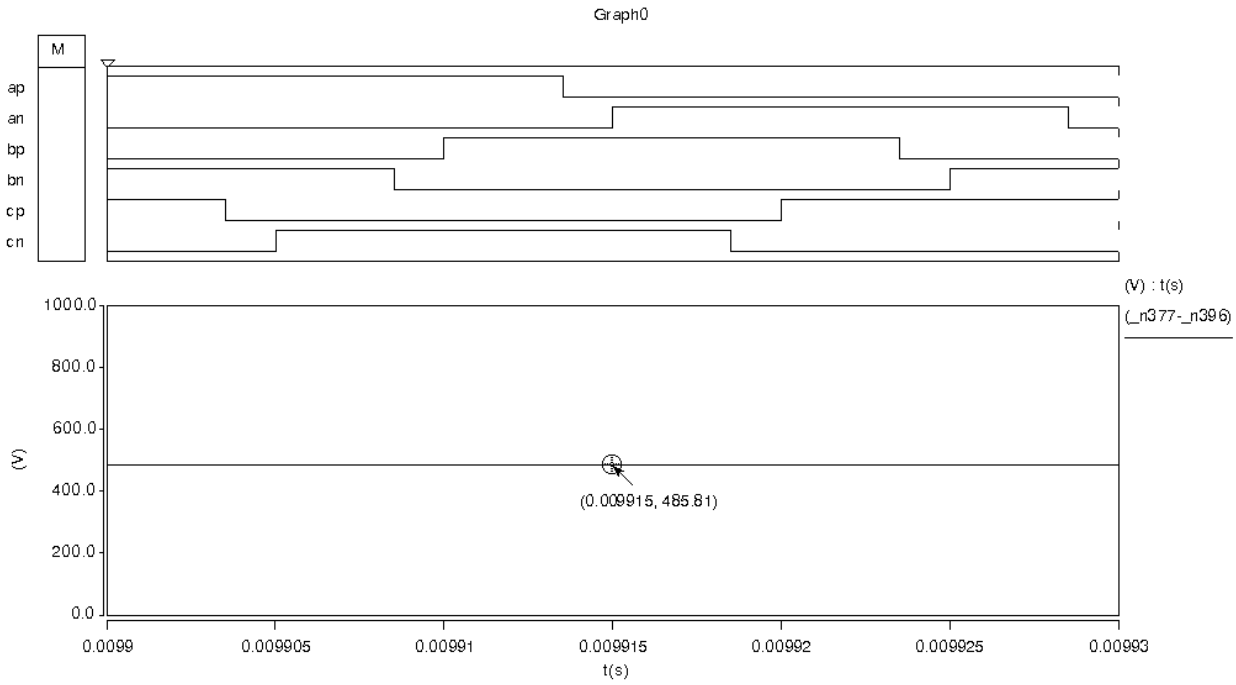

Figure 2-1. Ideal model gate signals and output voltage for $V_{IN\text{-}min}$ at 45% duty cycle

Although the ideal simulation model successfully validates converter functionality, it can be seen that the steady state output voltage of 485.81V is considerably greater than the output voltage value used to calculate the transformer turns ratio in (2.1). Further analysis showed that the transformer voltage boost factor was not a constant $\sqrt{3}$, but was instead a function of duty cycle. These results indicated that although (2.1) may be intuitively logical, it was invalid. Coincidentally, when the corrected voltage boost factor was used, the selected (equivalent)

transformer turns ratio remained unchanged due to an output voltage margin requirement and the need for equal secondary winding turns in the split output configuration. The transformer boost ratio is discussed in more detail in the next section.

2.1.2. Delta-Wye Transformer Boost Ratio Analysis

The converter voltage boost through the transformer stage was accurately modeled using a state analysis approach. Transformer input voltage waveforms were examined with respect to the delta-wye winding configuration. In a typical three phase delta-wye connected transformer with 120 degree phase shifted sine wave excitation, the line-to-line voltage boost ratio is $\sqrt{3}$. This relationship can easily be proven analytically using a phasor diagram. [8] However, for variable pulse width quasi-square wave excitation, the analysis is not so straightforward.

The switching stage gating sequence was studied for various duty cycles to characterize the phase-leg midpoint voltage states. The two discrete values of each gating signal represent the two possible states for each switch. When a gate signal is high, the corresponding switch is in the state of conduction. In the bridge configuration, with a phase-leg comprised of two switches across a DC voltage bus, the phase-leg midpoint voltage state is represented by the states of the top and bottom switch gate signals. Since the two gate signals of each phase-leg are designed to avoid simultaneous high states, only three phase-leg midpoint voltage states are encountered: $V_{mid} = V_{IN}$, $0.5V_{IN}$, 0. These midpoint voltages occur for gate signal states of (H, L), (L, L), and (L, H) respectively, with the first state in each ordered pair representing that of the top switch and the second state representing that of the bottom switch.

The interactions between midpoint voltage states of the three phases were determined in order to characterize the transformer input voltage waveform and the voltage boost ratio. The three equally shifted pairs of phase gate signals produce three shifted phase midpoint voltage states. The duration of midpoint voltage states, which varies with duty cycle, further complicates the analysis. Nevertheless, assuming an ideal transformer, primary winding voltage must be scaled by the turns ratio and completely transferred to the secondary winding. In the delta-wye winding configuration, delta line-to-line voltages are midpoint-to-midpoint voltages of the switching stage phase-legs. Line-to-line voltages on the transformer secondary side are the

differences between two secondary phase voltages. On this basis, transformer voltage boost ratio calculations for various duty cycles were conducted, assuming a transformer turns ratio of 1:1 for simplicity. Calculations for the 33.3% duty cycle case are shown below.

Figure 2-2 shows the six switch gating waveforms over one switching period for a 33.3% duty cycle. The period has been divided into six equal intervals each having a unique set of states. The phase-leg midpoint voltages for each interval are listed in Table 2-1.

Table 2-1. Phase-leg midpoint voltages per interval for the 33.3% duty cycle case

Phase midpoint	1	2	3	4	5	6
A	V_{IN}	V_{IN}	$0.5V_{IN}$	0	0	$0.5V_{IN}$
B	0	$0.5V_{IN}$	V_{IN}	V_{IN}	$0.5V_{IN}$	0
C	$0.5V_{IN}$	0	0	$0.5V_{IN}$	V_{IN}	V_{IN}

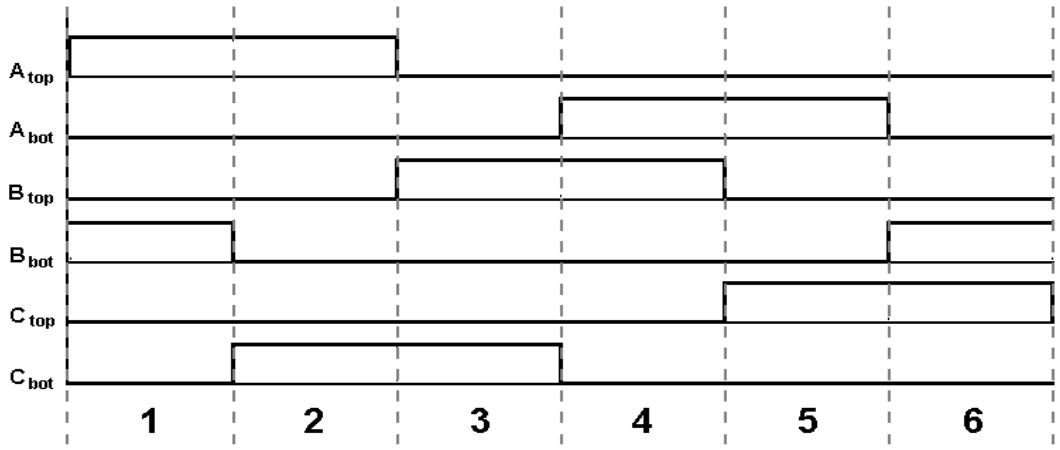

Figure 2-2. Switch gating waveform intervals for the 33.3% duty cycle case

The secondary side line-to-line voltages are calculated using the midpoint voltages in Table 2-1. For the delta-wye winding configuration, secondary side voltage V_{ab} is equivalent to the primary side voltage difference $V_{AB} - V_{BC}$ as shown in Figure 2-3. Likewise, secondary voltages V_{bc} and V_{ca} are equal to primary voltages $V_{BC} - V_{CA}$ and $V_{CA} - V_{AB}$ respectively. [8] Table 2-2 lists primary side voltages V_{AB} , V_{BC} , and V_{CA} as well as secondary side voltages V_{ab} , V_{bc} , and V_{ca} for each interval.

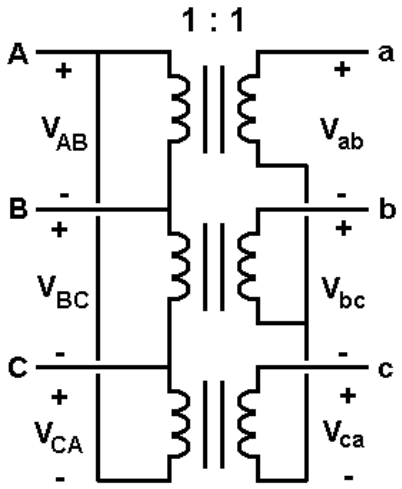

Figure 2-3. Primary and secondary line-to-line voltages

Table 2-2. Transformer primary and secondary side line-to-line voltages per interval

Primary Side Voltages						
V_{AB}	V_{IN}	$0.5V_{IN}$	$-0.5V_{IN}$	$-V_{IN}$	$-0.5V_{IN}$	$0.5V_{IN}$
V_{BC}	$-0.5V_{IN}$	$0.5V_{IN}$	V_{IN}	$0.5V_{IN}$	$-0.5V_{IN}$	$-V_{IN}$
V_{CA}	$-0.5V_{IN}$	$-V_{IN}$	$-0.5V_{IN}$	$0.5V_{IN}$	V_{IN}	$0.5V_{IN}$
Secondary Side Voltages						
V_{ab}	$1.5V_{IN}$	0	$-1.5V_{IN}$	$-1.5V_{IN}$	0	$1.5V_{IN}$
V_{bc}	0	$1.5V_{IN}$	$1.5V_{IN}$	0	$-1.5V_{IN}$	$-1.5V_{IN}$
V_{ca}	$-1.5V_{IN}$	$-1.5V_{IN}$	0	$1.5V_{IN}$	$1.5V_{IN}$	0

It can be seen from the results in Table 2-2 that four unique primary side line-to-line voltages produced only three unique secondary side line-to-line voltages. As an additional calculation check, it was seen that all three primary and secondary voltages summed to zero in each interval. The calculation of secondary side voltages completed the voltage boost ratio analysis of the transformer stage for the chosen operating point. Yet, the effective transformer voltage boost seen at the converter output is dependent upon the transfer of secondary side voltages through the rectifier stage. The diode arrangement of the rectifier is designed to transfer the magnitude of the largest voltage differential between any two rectifier inputs to the converter

output bus. Therefore, for the 33.3% duty cycle case, the converter output voltage is equal to $1.5V_{IN}$, making the effective transformer voltage boost ratio 1.5.

Several other sets of calculations were carried out to determine the voltage boost ratio for different duty cycles. The method of using equally divided gate signal period intervals was continued throughout the analysis. This allowed different rectifier output voltage states to be averaged to accurately determine converter output voltage after filtering. Although phase-leg midpoint voltages and transformer winding configuration determined transformer secondary side voltages, analysis of switch gate signals alone could not always be relied on for the calculation of accurate voltage boost ratios. For low duty cycles of 0% to 16.7%, zero or one of the six switches is gated on at any given time during a switching period. For duty cycles between 16.7% and 33.3%, one or two switches are gated on at any given time during a period. For duty cycles of 33.3% to 50%, two or three switches are gated on at any given time during a period. Whenever three switches are gated on, either two will be top switches and one will be a bottom switch, or two will be bottom switches and one will be a top switch. This will always produce two primary side line-to-line voltages equivalent to the DC bus voltage, with the remaining line-to-line voltage equal to zero. Whenever two switches are gated on, one will be a bottom switch and the other will be a top switch. This will always produce one primary side line-to-line voltage equal to the DC bus voltage, and two primary side line-to-line voltages equal to half the DC bus voltage. Yet, whenever only one switch is gated on, no current path will be formed through any primary transformer windings. Therefore, no line-to-line voltage differentials will exist, as in the case when no switches are gated on. As a result, the voltage boost ratio for 0% to 16.7% duty cycle is zero. For duty cycles between 16.7% and 33.3%, the voltage boost ratio is the weighted average of the boost ratios for intervals in which one and two switches are gated on. Likewise, for duty cycles ranging from 33% to 50%, voltage boost ratios are the weighted averages of boost ratios for intervals having two and three conducting switches.

In the analysis of these cases, the number of period intervals corresponded to the gate signal period divided by the shortest interval between the transitions of any two gate signals. Because there are six gate signals, the number of equal length intervals was always a multiple of six. The number of boost ratio values which can be calculated in the 0% to 50% duty cycle range is therefore half the number of intervals plus one. For example, with six equal intervals, only boost ratios for duty cycles of 0%, 16.7%, 33.3% and 50% can be calculated. To fully

characterize the boost ratio for duty cycles ranging from 0% to 50%, several intervals were used to plot a boost ratio trend line. Matlab code was written to carry out boost ratio calculations based on a specified number of intervals. The boost ratio plot shown in Figure 2-4 was generated in Matlab using 600 gate signal intervals of equal length.

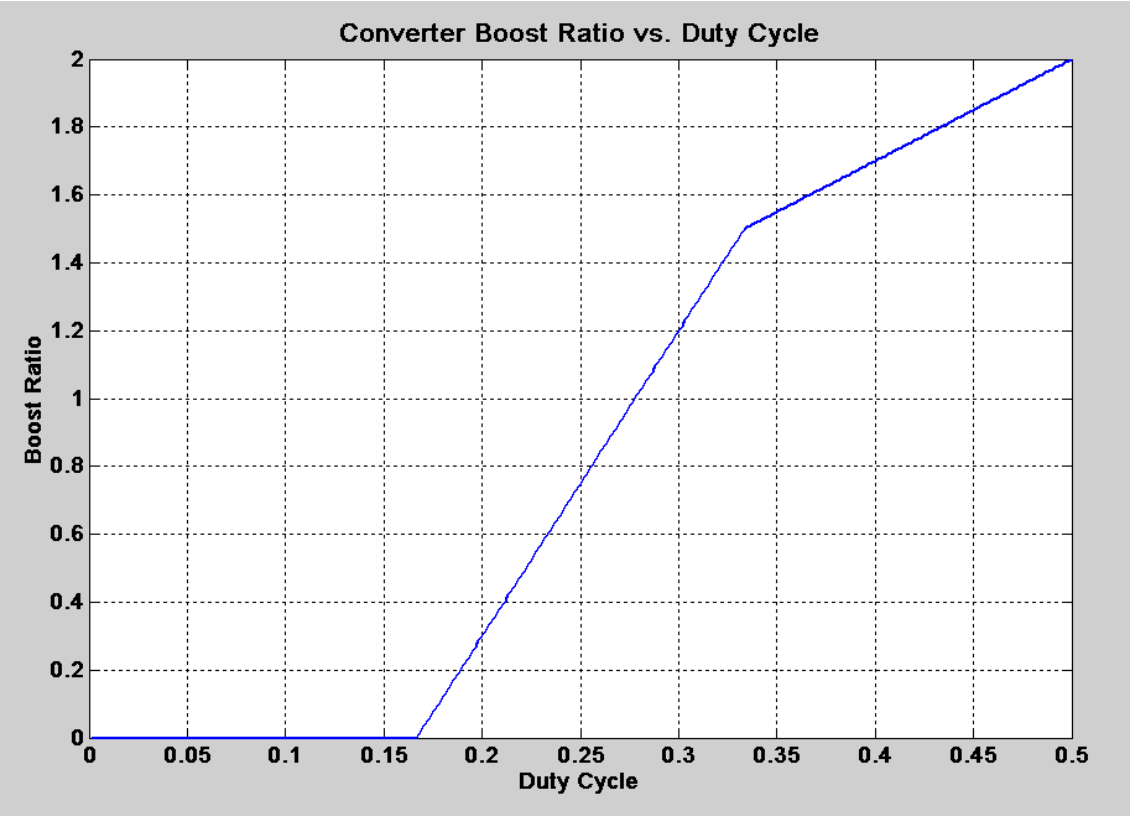

Figure 2-4. Converter voltage boost ratio relationship with duty cycle

The boost ratio characteristic is linear in three regions which meet at two points of discontinuity. The discontinuity points occur at boost ratios of zero and 1.5 corresponding to duty cycles of 16.7% and 33.3%. The piecewise function that defines the boost ratio is given by (2.2) where B and d denote the boost ratio and duty cycle respectively.

$$\begin{aligned} B &= 0 && 0 \le d \le 0.1\overline{6} \\ B &= 9d - 1.5 && 0.1\overline{6} \le d \le 0.\overline{3} \\ B &= 3d + 0.5 && 0.\overline{3} \le d \le 0.5 \end{aligned} \tag{2.2}$$

Expression (2.1), which was an attempt to establish a valid relationship between converter input voltage, output voltage, duty cycle, and transformer turns ratio was replaced by (2.3). The new relationship is based on (2.2), and is valid.

$$V_O = V_{IN} \cdot N \cdot B \tag{2.3}$$

Using (2.2) and (2.3) with the conditions selected to determine the transformer turns ratio: $V_{IN\text{-}min} = 22V$, $d_{max} = 0.45$, and $V_O = 400V$, N was recalculated to be 9.83. However, selecting a turns ratio of 1:10 would only provide an ideal output voltage of 407V. Losses in the real converter would reduce output voltage to below 400V for this turns ratio. Ideally, a ratio of 1:11 would have been chosen to provide sufficient output voltage margin. Instead, an effective 1:12 ratio was selected for the split output configuration for evenly divided secondary windings of 6 turns. Solving (2.3) for output voltage using the previous conditions and N = 12 gives V_o = 488.4 V. As expected, this value agrees very well with the simulated output voltage of 485.8V in the nearly ideal model.

2.2. Active Component Selection

2.2.1. Switch Selection

Power MOSFET devices were an original design choice for the switching stage topology due to their low losses, ease of implementation, ability to operate at high switching frequencies, and low cost. MOSFETs having a voltage rating adequately above the DC input voltage of the converter can have low conduction losses. These losses are a function of MOSFET on-resistance. Because of the positive temperature coefficient of this resistance, MOSFETs can easily be paralleled in high current applications for close current sharing, and to further reduce the on-resistance of the parallel switch network. Switching losses of MOSFETs tend to be lower than those of other devices during hard switching, due to their rapid switching transition characteristics. [9] This allows efficient device operation at higher switching frequencies. Finally, MOSFETs are a comparatively low cost power switching device, especially in discrete form.

A MOSFET switching frequency of 50kHz was selected to allow the transformer and output filter stage components to be small. Although higher switching frequencies were achievable for further passive component size reduction, three noteworthy undesirable tradeoffs exist. First, converter efficiency would be reduced in these cases as a result of increased switching losses at high power levels. Second, converter conduction losses would increase for higher switching frequencies, due to the skin affect. Third, precise digital control for the three phase topology would be increasingly difficult for switching frequencies above 50kHz.

After conducting preliminary converter simulations, optimal power MOSFET devices were sought for switching stage implementation. Ideal converter simulations were no longer pursued to investigate results using ideal power MOSFET models. Most ideal power MOSFET models provided in software simulation packages are either not intended to function above certain power levels, or require application specific user defined parameters to behave properly. Furthermore, ideal power MOSFET models are designed to represent single MOSFET devices and can function poorly when used in applications which require multiple devices connected in parallel.

Although many device parameters were studied during the device selection process, the following parameters were most strongly considered. Low on-resistance, was the most important factor taken into account for conducting large currents while sustaining less power loss. Efficient thermal dissipation capability for removal of heat buildup from the device was important. Device size, package, and mounting configuration were also considered for compact and effective circuit layout. Finally, device availability and cost were considered, as well as ease of implementation and implementation cost.

Power MOSFET device specifications from several manufacturers were reviewed. The search was limited to discrete MOSFETs or easily scalable MOSFET configurations having at least a 75V blocking capability and an on-resistance no greater than 7mΩ. The 75V MOSFET requirement was established to allow sufficient headroom for transient voltage spikes occurring as a result of the interaction between parasitic inductances and large conduction currents. On-resistance was limited at 7mΩ to substantially reduce the number of devices considered and to focus intently on devices offering the lowest conduction losses. Using these selection criteria, the most favorable devices were chosen to be researched more thoroughly. These devices are listed in Table 2-3.

All the selected devices met the electrical specifications outlined. Other factors were analyzed mainly based on considerations related to the device packages. Both of the selected IXYS devices were initially favored based on their superior thermal characteristics. The ISOPLUS package, developed by IXYS, is a through-hole design with an electrically isolated copper back plane. This design allows significant heat conduction through minimal thermal impedance from the device to a heat sink. The IXYS FMM 150-0075P half-bridge device was the more desirable IXYS device for its compact dual MOSFET arrangement and low on-resistance. However, the device package (i4-PAC) is a relatively new package used exclusively by IXYS. Selecting this part over a more standard package could compromise future upgrades to an existing design due to a limited part selection. It was determined that the unique benefits offered by this device were not desirable enough to warrant its associated replacement opportunity risks or its cost. Because the IXUC160N075 device in the ISOPLUS220 package has a pin-out similar to the widely used TO-220AB package, it was given further consideration. [13,15]

Table 2-3. Favorable MOSFETs for switching stage implementation [10-17]

Manufacturer	Part Number	V_{DSS} (V)	$R_{DS\text{-}on}$ (mΩ)	Package
Fairchild	FDB045AN08A0	75	4.5	TO-263
International Rectifier	IRFP2907	75	4.5	TO-247
Fairchild	FDP047AN08A0	75	4.7	TO-220AB
IXYS	FMM 150-0075P	75	4.7	ISOPLUS i4-PAC*
Vishay Siliconix	SUM110N08-05	75	4.8	TO-263
IXYS	IXUC160N075	75	6.5	ISOPLUS 220
International Rectifier	IRF3808	75	7.0	TO-220AB
Fairchild	FQA160N08	80	7.0	TO-3P

*Note: IXYS FMM 150-0075 is a dual pack (half bridge) device.

The device package analysis was continued with a focus on device specifications with respect to package size. Electrical specifications of devices with larger packages (TO-247, TO-3P) were compared to those with smaller device packages (TO-220AB, TO-263). It was determined that although the IRFP2907 and the FQA160N08 have higher current limitations due

to larger die size, larger lead diameter, and a larger surface area from which to dissipate heat, they show no additional reductions in on-resistance for their increased size. Since these devices occupy more circuit area and cost more than comparably rated smaller devices, they were also eliminated from consideration. [11,17]

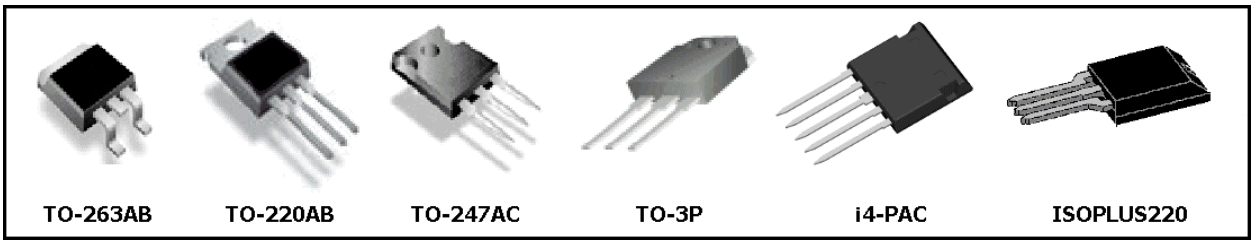

Figure 2-5. MOSFET device packages considered

The TO-263 and TO-220AB packages (including ISOPLUS220) were compared. These three packages are nearly identical in size, but differ in mounting orientation. The 220-type packages are designed for through-hole mounting which typically requires a vertical orientation. Cooling is achieved by fastening the back of the device to a heat sink using screws or clips. However, effective heat sinking of multiple devices is difficult in this configuration due to the conflict that exists between the perpendicular surfaces of the heat sink and the circuit board. The surface mount TO-263 package was selected to eliminate heat sink and circuit board layout complexity. Adequate heat sinking for the TO-263 devices would be achieved through the implementation of an insulated metal substrate (IMS) circuit board. Finalizing the device selection required closer inspection of the FDB045AN08A0 and SUM110N08-05 characteristics, pricing, and availability. Although the two devices were seen to have very similar characteristics, Fairchild claimed a slightly lower on-resistance for the FDB045AN08A0, while Vishay claimed a slightly higher maximum operating junction temperature for the SUM110N08-05. Since neither cost nor availability proved to be a deciding factor between the two, the FDB045AN08A0 was selected for its minimal on-resistance. [10,14]

MOSFET current ratings were also considered during the component selection process, but were not a deciding factor. Current ratings were given more consideration to determine the number of parallel devices required to meet the switching stage conduction requirements. All of the components considered had continuous current ratings sufficient for practical parallel

MOSFET implementation. These values are reported in Table 2-4 for various operating temperatures. Pulsed current ratings of all eight devices were reported to be well in excess of switching stage requirements. The number of parallel devices required was determined by the device current rating. The 80A continuous current rating of the FDB045AN08A0 indicated that at least four devices would be required in parallel to conduct the maximum average converter input current of approximately 250A; assuming 90% efficiency at a 5kW output condition. [10] However, the tradeoffs associated with larger numbers of parallel devices were considered. More devices operating in parallel reduces conduction losses and individual device stresses. Yet it increases circuit layout parasitic components which can adversely affect converter operation. Most notable of these are parasitic inductance of device interconnections and device gate traces, which cause additional device voltage stresses during switching transitions. The TO-263 packages alone have been shown to have an inductance of roughly 5nH at a frequency of 50kHz due to package leads and internal wirebonds. [18] More parallel devices also increases converter cost.

Table 2-4. Continuous drain current ratings and temperatures of favorable MOSFETs [10-17]

Manufacturer	**Part Number**	**I_D (A)**	**T_C (°C)**
Fairchild	FDB045AN08A0	80	145
International Rectifier	IRFP2907	148	100
Fairchild	FDP047AN08A0	80	144
IXYS	FMM 150-0075P	120	90
Vishay Siliconix	SUM110N08-05	110	125
IXYS	IXUC160N075	130	90
International Rectifier	IRF3808	97	100
Fairchild	FQA160N08	113	100

2.2.2. Diode Selection

Based on converter output specifications, diode ratings of 600V reverse blocking voltage, and 50A average forward current were selected. Other specifications such as forward voltage

drop, reverse recovery time, and peak reverse recovery current were strongly considered for device selection. The most common discrete rectifier package offered for the selected power level was the TO-247. Three ultra-fast, soft recovery devices in the TO-247 package were selected for comparison and are presented in Table 2-5. Both the IR and IXYS devices were packaged in a dual rectifier with common cathode three-pin configuration, while the Fairchild device was a two-pin single rectifier package. [19-21]

Low diode forward voltage drop (V_F) was an important consideration to minimize device power consumption. The forward voltage drop values reported in Table 2-5 were estimated from forward voltage drop versus instantaneous forward current curves included in the device data sheets. The values correspond to a forward device current of 50A. However, some testing conditions differed between manufacturers. The V_F value reported for the International Rectifier (IR) device is a maximum value taken at a 125°C junction temperature, while the two other values are reported for junction temperatures of 100°C, and were not indicated as being maximal.

Table 2-5. Favorable diodes for rectifier stage implementation [19-21]

Manufacturer	Part Number	V_F*	t_{rr}	I_{RRM}	Package
Fairchild	RHRG5060	1.5 V	45ns (max)	N/A	TO-247
International Rectifier	HFA50PA60C	1.9 V (max)	23ns (typ)	8 A (typ)	TO-247AC
IXYS	DSEK 60-06A	1.6 V	35ns (typ)	10 A (typ)	TO-247AD

Low reverse recovery time (t_{rr}) and small peak reverse recovery current (I_{RRM}) were important to provide more continuous load current and reduce reverse conduction. The t_{rr} values presented also reflected varied test conditions. Although test conditions of 1A forward current and a 25°C junction temperature were reported for all three devices, the forward current dI_F/dt value for the HFA50PA60C was reported to be 200A/μs while the other devices reported values of 100A/μs. This indicated that the IR device had a faster reverse recovery time based on the magnitude of forward current transients. It was also noted that the given t_{rr} value for the RHRG5060 was a maximal, while those of the other two devices were typical.

Peak reverse recovery current specifications were also compared based on available data. The values listed in Table 2-5 represent peak reverse recovery current specifications associated

with similar test conditions. Fairchild did not specify a peak reverse recovery current for the RHRG5060 device on its data sheet. IR test conditions included a forward current of 25A, a reverse voltage of 200V, a dI_F/dt value of 200A/μs, and a junction temperature of 125°C. Corresponding, IXYS test conditions were $I_F = 30A$, $V_R = 350V$, $dI_F/dt = 240A/\mu s$, and $T_{VJ} = 100°C$. [19-21]

Overall, the IR and IXYS devices appeared to be the best suited for implementation, with the IR device showing slightly more desirable characteristics. Because device cost was not significantly different between the two, the HFA50PA60C by International Rectifier was selected for implementation.

2.3. Passive Component Selection

2.3.1. Transformer Selection

Three single phase planar transformers were chosen for the three phase transformer configuration. Planar transformers provide unique benefits by differing from traditional wire wound transformers in winding arrangement and core geometry. The planar construction uses flat winding layers wound in a spiral pattern and bonded to thin insulating substrates. The layers are stacked inside or around a low profile core. Multiple winding layers can be connected in series to create a desired number of winding turns. The layers can also be tied together in parallel to obtain an equivalent conductor thickness or skin area. This type of winding geometry allows planar transformers to operate at high switching frequencies which can result in further core size reduction and reduced winding losses. The stacked layer arrangement greatly simplifies the production of symmetric windings for transformers having center tapped or multiple primary or secondary side windings. Primary and secondary winding layers can also be stacked alternately to produce higher coupling. In this way, transformer leakage inductance can be reduced for high efficiency operation. Planar transformers exhibit high manufacturability which leads to more repeatability of transformer parameters. This benefits topologies which require multiple closely matched transformers for soft switching and/or delta winding

configurations. Finally, planar core geometry is more suited for heat sink mounting which allows higher transformer power densities to be achieved. [22, 23]

A 2kW planar transformer design from Payton Group International was selected. The transformer listed as type T1000AC-1-6-6; part number 50635 is shown in Figure 2-6. Operating parameters of 50kHz, 112A rms maximum primary current, and 1000V rms minimum dielectric strength were specified. Leakage inductance and magnetizing inductance values for three transformers were measured at 50kHz on the secondary side, with the secondary windings connected in series. Leakage inductances of 4uH $\pm$ 50nH, and magnetizing inductances of 1.9mH $\pm$ 150uH were obtained.

Figure 2-6. 2kW 1:6:6 planar transformer

2.3.2. Filter Component Selection

The output filter inductor and capacitor values were calculated based on maximum ripple current and ripple voltage magnitudes. These values were calculated ideally using a buck converter output filter design approach. This approach is valid when treating the rectifier output voltages and currents as discrete time varying states. With the rectifier output characterized to determine the converter voltage boost ratio, the converter operating conditions yielding maximum inductor current ripple and maximum capacitor voltage ripple were determined.

A peak inductor current ripple no greater than 20% of the average inductor current was desired. The inductor ripple current relationship (change in inductor current) = (ripple current slope)(length of subinterval) was used. [1] Ripple current slope was determined by the inductor voltage (V_L) during one subinterval of the rectifier output voltage cycle. The inductor voltage was defined as the rectifier output voltage minus the converter output voltage ($V_R - V$). To design for the operating point having the largest ripple current, the largest ($V_R - V$) value was found using the voltage boost ratio profile of Figure 2-4. The piecewise function values of the second and third duty cycle intervals (16.7% to 33.3% and 33.3% to 50%) can be represented as the weighted averages of the boost ratio values at the first and last points of each interval. Therefore, the midpoint duty cycle values of the second and third intervals will correspond to the operating points having the largest inductor ripple currents within each of the two intervals. Since the difference between the boost ratio values marking the beginning and the end of the 16.7% to 33.3% duty cycle interval is greater than that of the 33.3% to 50% interval, the 25% duty cycle point corresponds to the maximum inductor ripple current. Equation (2.4) shows the empirical relationship between inductance and inductor ripple current magnitude for this operating condition. Variables N, and T represent the individual output transformer turns ratios (1:6), and the switching stage period (20us for 50kHz) respectively.

$$2\Delta i_{L(\max)} = \frac{N(1.5 \cdot V_{IN} - 0.75 \cdot V_{IN})}{L} \cdot \frac{T}{12} \Rightarrow \Delta i_{L(\max)} = \frac{V_{IN} \cdot N \cdot T}{32L} \tag{2.4}$$

For a 400V converter output at a 25% duty cycle, V_{IN} = 44.4V, based on (2.2) and (2.3). Average inductor current is equal to the converter output current of 12.5A for the 5kW condition. Solving (2.4) for inductance for a 20% ripple current gave L = 66.6μH. Therefore, 70μH inductors were used.

The filter capacitor value was calculated based on the maximum inductor ripple current value. The equation relating the capacitance and capacitor ripple voltage for a buck converter was modified to accurately represent the rectifier output voltage cycle for the 25% duty cycle case. This relation is shown as (2.5). [1]

$$2\Delta V_{C(\max)} = \frac{\Delta i_{L(\max)}}{C} \cdot 0.5 \cdot \frac{T}{12} \Rightarrow \Delta V_{C(\max)} = \frac{\Delta i_{L(\max)} \cdot T}{48C} \tag{2.5}$$

It can be seen from (2.5) that the conditions of maximum capacitor voltage ripple and maximum inductor current ripple coincide. Equation (2.5) was solved under this condition for

capacitance for a ripple voltage of 1V (0.5%) to give a value of 1.04μF. However, a significantly higher value of 2.2mF was used to provide high side energy storage for voltage regulation during load transients.

2.4. Real Converter Modeling and Simulation

After selecting active and passive converter components, a system model was created to simulate real converter operation. Models for the FDB045AN08A0 and HFA50PA60C devices were imported into Saber. The switching stage was modeled using four parallel MOSFETs per converter switch. Three separate transformers having two secondary windings of six turns were used to model the transformer stage. The two rectifier stages were each modeled with six diode device models. The calculated filter inductor value was used for the two output filters along with a filter capacitor value of 100uF to reduce simulation time. For consistency, no resistance modeling was attempted for circuit connections or components, other than the resistive properties included in the device models. However, leakage and magnetizing inductances were used to improve the accuracy of the ideal three winding transformer model.

The leakage and magnetizing inductances were added to the primary windings of each transformer. Because these values were larger and more accurately measured at the secondary side of the transformer, they were divided by the transformer turns ratio squared to give the equivalent primary side values as shown in (2.6) and (2.7). Terms L_{LKP}, L_{LKS}, L_{MP}, L_{MS}, N_P, and N_S represent primary leakage inductance, secondary leakage inductance, primary magnetizing inductance, secondary magnetizing inductance, number of primary winding turns, and number of secondary winding turns respectively.

$$L_{LKP} = L_{LKS}\left(\frac{N_P}{N_S}\right)^2 = 4\mu H\left(\frac{1}{12}\right)^2 = 27.8nH \tag{2.6}$$

$$L_{MP} = L_{MS}\left(\frac{N_P}{N_S}\right)^2 = 1.9mH\left(\frac{1}{12}\right)^2 = 13.2\mu H \tag{2.7}$$

Simulations were run for the 5kW load condition at a minimum converter input voltage of 22V, and a maximum duty cycle of 45%. The steady state output voltage was 463V. Figure 2-7 shows the current and voltage waveforms of one of four MOSFETs on the top switch of

phase A. It can be seen that the simulated operating conditions do not exceed the device ratings, indicating that the minimum number of four parallel devices per switch was sufficient. However, five or six parallel MOSFETs would further reduce device current stress and conduction loss. The number of MOSFETs per switch was given further consideration during circuit layout.

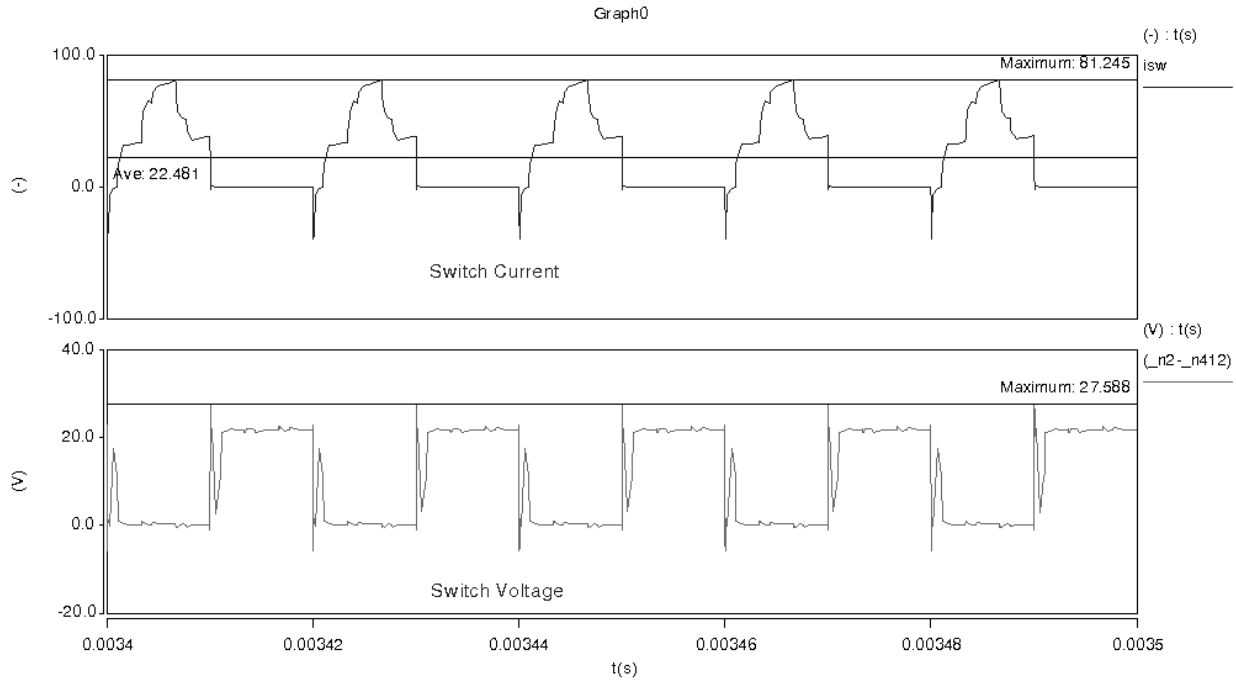

Figure 2-7. Simulated individual MOSFET voltage and current for a 5kW load

Chapter 3. Switching Stage Structure

3.1. Electrical and Thermal Tradeoffs

The design of the three-phase converter switching stage was largely based on thermal management. During the device selection process, component mounting configurations were considered in accordance with two types of circuit board. The selection of the surface mount TO-263 package was made along with the decision to use an Insulated Metal Substrate (IMS) circuit board for sufficient heat dissipation. This design was seen to offer reductions in switching stage layout complexity.

The implementation of through-hole or surface-mount power devices can be complicated by component heat sinking requirements. Conventional FR-4 boards often have through-hole components which stand off the board and are attached to one or more heat sinks. Such a configuration can be complex due to compounding factors. The pins of the device are set into the circuit board, giving the component a natural tendency to stand perpendicular to the circuit. If the component pins are bent to allow its thermally conductive side to sit flat on the board, like a surface-mount package, a conductive pad can be used to aid device heat dissipation. For more heat transfer, larger and thicker pads are needed as board material undesirably serves to thermally insulate the underside of the pad. In many power applications, this cooling method is insufficient and heat sinks must be used. Heat sinking surface-mount devices is more difficult, but can be accomplished by either heat sinking the device pad directly, or using vias for heat transfer.

Through-hole devices can remain in the vertical position to be mounted to heat sinks which stand perpendicular to the board. However, in most cases, the conflicting perpendicular surfaces of the board and the heat sink compromise either circuit layout or heat sink effectiveness. Heat sinks dedicated to individual or multiple devices can be mounted above the board. However, they will most likely occupy circuit area and need to be fastened to the board. A method of fastening the component to the heat sink such as screws or clips must also be used.

In some cases, devices can be positioned near the perimeter of the board to be connected to larger heat sinks that extend past the edge of the board. Such a circuit configuration is often less than optimal and difficult to achieve. A good option is to mount devices on the bottom side of the board and bend their leads 90 degrees to allow the package to be mounted flat onto a large heat sink located below the board. Yet, this configuration is not always achievable and often requires mounting access holes through the circuit board.

To further complicate the heat sinking issue, component heat dissipation can be compromised for non-isolated packages. Because most components have an active terminal backing, they may need to be electrically isolated from the heat sink for cases in which the heat sink is shared by other devices and/or to keep the heat sink de-energized. This requires electrically insulating, thermally conductive material to be placed between the device and the heat sink. Do to conflicting material properties, heat conduction is therefore compromised as a result of electrical isolation.

The IMS circuit board structure provided an effective means of satisfying the electrical and thermal requirements of the switching stage. IMS boards belong to a class of circuit structures having stacked layers specifically designed to increase heat transfer from power dense circuitry. The stack consists of a layer of dielectric material which is bonded to a layer of conducting foil on one side, and a thermally conductive metal substrate on the other. Figure 3-1 depicts a basic IMS circuit board stack structure. The thermal base layer is typically made of copper or aluminum, and serves as a heat spreader to distribute and transfer thermal energy to a heat sink. However, the dielectric layer sets IMS apart from other stacked structures. Unlike direct bond copper (DBC) or thick film structures which use ceramic metallic oxides as a dielectric, IMS uses an epoxy polymer dielectric. In addition to providing electrical isolation between the conducting layers, the epoxy adheres to the layers to mechanically hold the stack together. [24] Although the thermal conductivity of IMS epoxies is lower than that of ceramic dielectrics, the epoxies give IMS structures much more mechanical durability which can lend to higher rated thermal stresses and longer life cycles. [25]

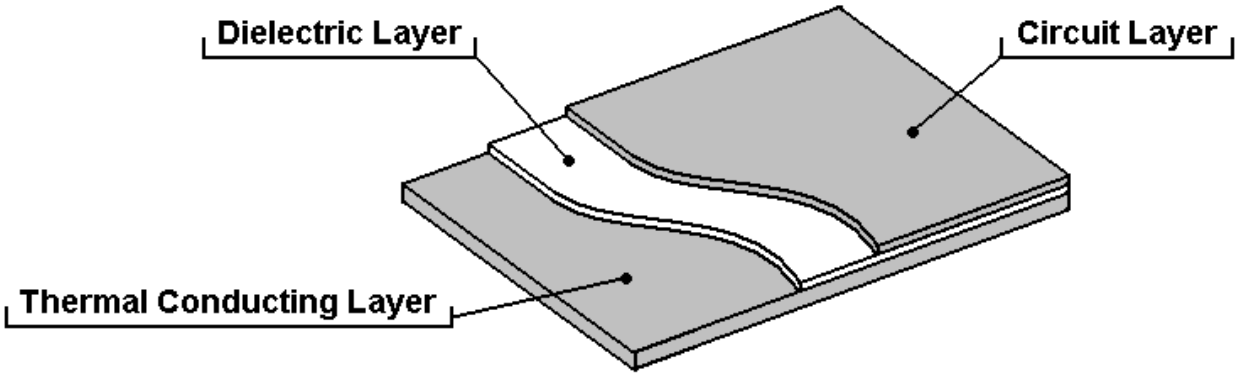

Figure 3-1. Single conducting layer IMS structure

The IMS structure resolves many of the electrical and thermal conflicts associated with conventional FR-4 circuit boards. IMS structures having multiple conducting layers are also available. Devices are surface mounted to the conducting layer(s) of the board, and heat sinking is inherently simplified by the thermal path through the board. A heat sink can be fastened directly to the bottom side of the board for effective heat dissipation. The simplified circuit structure also reduces production complexity and assembly time, thereby lowering manufacturing costs.

3.2. Circuit Design

3.2.1. Switching Stage Layout

A single layer IMS circuit board layout was designed for the switching stage. During the process, several factors were considered. An overall compact circuit configuration less susceptible to parasitic inductance was sought. An effective gate trace layout incorporating gate resistors, as well as a low profile device and bypass capacitor configuration were important. These features would limit overall gate length and allow close proximity of the gate driver. The use of board-mounted high current terminal connectors was considered along with associated mechanical stresses. The resulting design shown in Figure 3-2 successfully achieved these criteria.

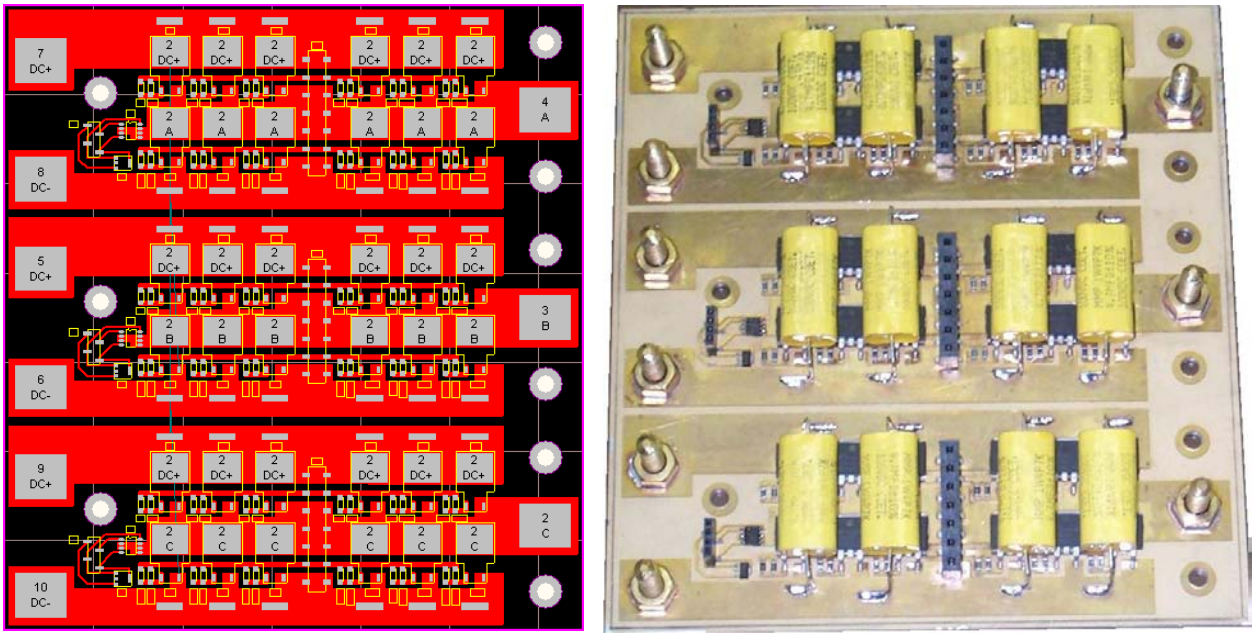

Figure 3-2. Switching stage layout design and implementation

The mean path length from the gate driver to the switching stage devices was designed to be short to reduce gate lead inductance. Because multiple MOSFETs were connected in parallel for each switch unit, the mean gate lead length was minimized by placing the gate drive header in the middle of each phase-leg. Therefore, an even number of six parallel MOSFETs was selected for phase-leg symmetry. In order to avoid the use of a dedicated gate trace layer, gate traces were routed underneath the pins of the TO-263 packages for minimal gate trace length. These traces were separated next to each device to provide positions for two parallel 1206 surface mount gate resistors. MOSFETs were positioned close together to reduce gate trace length and parasitic inductance associated with parallel device interconnections.

However, this left little board space for bypass capacitors to be mounted close to the devices. Bypass capacitors, used to provide switching ripple cancellation across the DC bus on each phase-leg, are most effective when the inductance between them and the switching devices is minimized. Film capacitors were determined to be the best candidates for the bypass application because of their relatively high capacitance per volume, acceptable voltage ratings, and wide variety of geometries. Capacitors having a longer and thinner shape were needed to bridge the phase-leg devices, while maintaining a low phase-leg profile to keep the gate driver

close the switching stage. The maximum temperature ratings of applicable polypropylene and polyester film capacitors were 105ºC and 125ºC respectively. Mounting such capacitors required a lower temperature post reflow process. Conveniently, the stacked MOSFET-capacitor configuration allowed capacitor thermal stress to be reduced during mounting, with the MOSFET packages acting as a thermal buffer between the capacitor and the board.

Board mounting terminals were designed for mechanical stability and to conduct maximum switching stage currents on the input and output sides of the board. After reviewing the products offered by manufacturers of high current circuit board terminals, no products were found to meet the mechanical and current carrying requirements of the IMS board configuration. A threaded connector was desired instead of a large plug type connector to reduce compression and tension forces on the terminal-to-board interface during connection and disconnection. However, the method of mounting the terminal to the board was difficult to determine. Any type of connector intended to be fastened through the board would need to be isolated from the substrate as well as completely flush with its underside. Since this was concluded to be far too difficult to achieve, a simple custom surface mount threaded stud was used.

Brass machine screws having flat hexagonal heads were mounted to the board as shown in Figure 3-2. This type of terminal provided advantages in addition to being inexpensive and readily available. Brass is highly conductive, solderable, and more wear resistant than copper. Furthermore, the base of the terminal has a larger surface for a more secure solder bond to the board, and can be supported using a wrench to greatly reduce solder bond stress under torquing conditions. For mechanical strength and sufficient current capacity, a quarter inch diameter shank was used for the terminals.

3.2.2. Input and Output Busses

The DC input bus for the switching stage was designed to distribute source current to each phase-leg with a minimum number of interconnections. Two copper plates having a thickness of 30mils were used for the positive and negative busses. Holes 1/4in in diameter and larger were drilled in the plates to provide conducting and isolated contact points for the

connectors. The plates were separated by FR-4 insulating material. The three layer bus structure is shown in Figure 3-3.

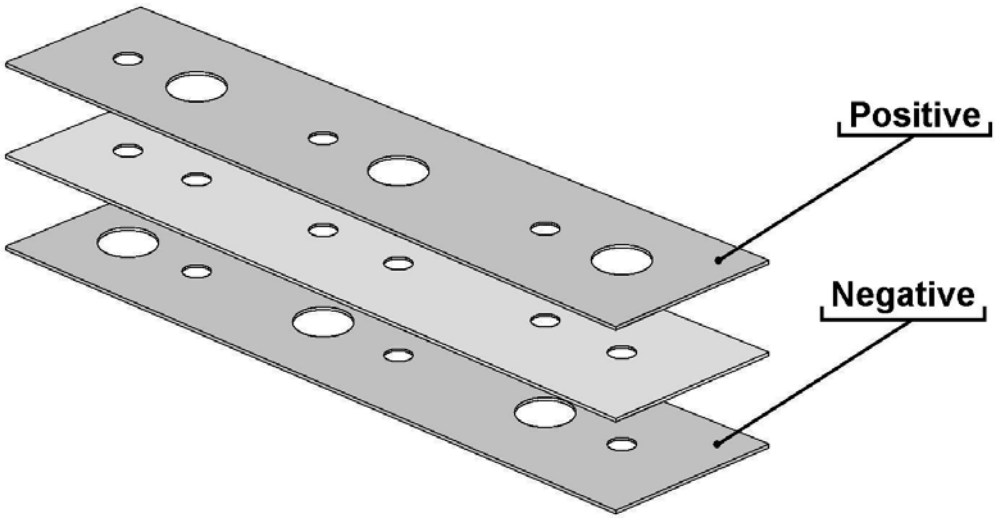

Figure 3-3. DC bus structure

To reduce input voltage ripple, three 3.3mF electrolytic capacitors were mounted vertically underneath the supply side of the bus. Due to their size, the bus was widened to allow them to extend beyond the edges of the heat sink and the power stage board. The bus and supply lines were secured to the switching stage input side board terminals.

The output bus connecting the switching stage to the transformer stage was constructed using individual copper bus connections. These connectors were fabricated from 15mil thick copper sheet. Thicker material was not used because it was seen to be too rigid to allow proper alignment between the transformers and because it was unable to be adequately compressed by the smaller hardware at the transformer primary terminals.

3.2.3. Electrical Considerations

Individual MOSFET gate drive resistor values and associated power ratings were calculated based on the FDB045AN08A0 MOSFET gate voltage versus gate charge curve shown in Figure 3-4. Because a 15V gate driver output was designed to ensure complete device turn on,

a gate charge value corresponding to V_{GS} = 15V was extrapolated from the curve. A value of 128nC was found using an approximate slope of 133mV/nC. The gate drive current was calculated by dividing the gate charge by the MOSFET turn-on time. [26] Selecting a 100ns turn-on time resulted in a gate drive current of 1.28A. The difference between the applied gate voltage and the gate threshold voltage shown on the gate charge curve for a drain current of 80A was estimated to be 9V. Therefore, the gate drive resistance which allows the available 9V to provide 1.28A to the gate is 4.7Ω. [26]

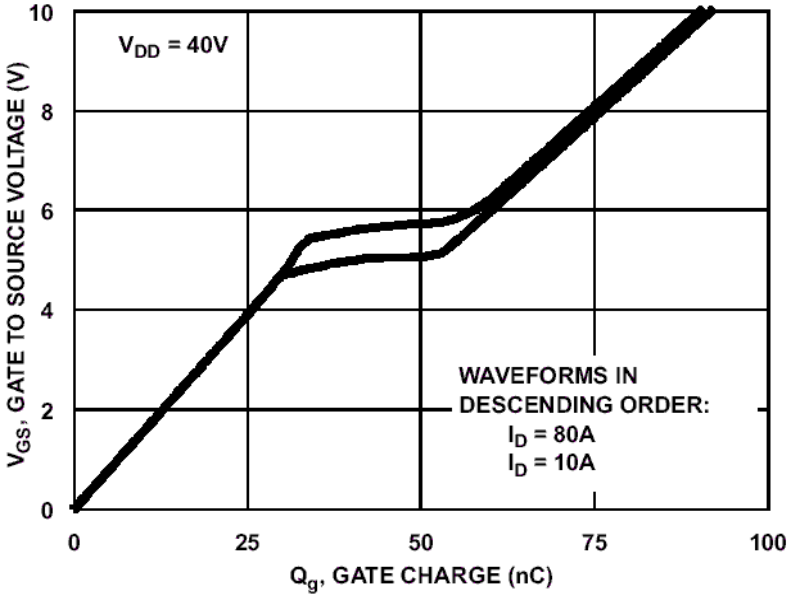

Figure 3-4. FDB045AN08A0 constant gate current gate charge waveforms [10]

The average power dissipated by the gate resistor was also determined. Average gate resistor power is the product of the instantaneous power, the turn-on time, and the MOSFET switching frequency. [26] For the respective values: (9V)(1.28A)(100ns)(50kHz) = 58mW. Based on available 1206 ceramic chip resistor ratings, two 10Ω, 1/8W or 1/4W resistors placed in parallel were sufficient and able provide a large power rating margin.

For the bypass capacitor application, two standard film capacitors having capacitance values greater than 1µF and well suited package dimensions were selected. The capacitors and their specifications are listed in Table 3-1. The length of the capacitor was seen to be inversely proportional to its peak current capability which is given by the capacitance times the maximum

rated voltage transient. However, a sufficient capacitor length was desired to reduce additional inductance from capacitor lead length. Although both parts were used during the course of the study, the length and height of the 761M27551 was more compatible with the circuit layout.

Table 3-1. Bypass Capacitor Specifications

Manufacturer	Part #	V_{DC}	C (µF)	ºC (max)	dV/dt (V/µs)	L, W, H (in)
SB Electronics	761M27551	160	2.7	105	7	1.74 0.53 0.28
Cornell Dubilier	MMP1W4P7K	100	4.7	125	6	1.38 0.73 0.35

Electrical characteristics of the brass terminals were evaluated. The approximate power dissipated over a 0.25in length of connector was determined for maximum terminal current using (3.1), where P_D, I, ρ, L, and A, represent dissipated power (W), current (A), resistivity at ambient temperature (Ω·m), conductor length (m), and average conductor cross sectional area (m^2) respectively. Although (3.1) relates the conductor resistance and associated power dissipation for a constant resistivity, for larger power dissipation values conductor resistivity will increase as a function of temperature. In such cases, (3.2) can be used to determine the resistivity value for the conductor temperature change, where α.is the temperature coefficient of conductor resistivity ($ºC^{-1}$), and ρ_0 is the reference resistivity at temperature T_0. [27] To ensure an adequate design of high current conductors, the largest average bus current per phase was slightly overestimated to be 85A. This value was calculated assuming a 22V source and a worst case 10% converter loss at a full output power of 5kW. Equation (3.1) was solved, using the resistivity of a 70% copper, 30% zinc alloy, for an ambient temperature of 295K (21.85ºC). [28] A power dissipation value of 128mW was obtained. Equation (3.2) was not used to correct for the conductor temperature rise due to the low power dissipation of the connector in the presence of a heat sink.

$$P_D = I^2 \cdot \frac{\rho \cdot L}{A} = 85^2 \cdot \frac{(6.6 \cdot 10^{-8})(0.25 \cdot 0.0254)}{\pi(0.108 \cdot 0.0254)^2} = 128mW \tag{3.1}$$

$$\rho - \rho_0 = \rho_0 \cdot \alpha \cdot (T - T_0) \tag{3.2}$$

3.3. IMS Board Selection

Conductor, dielectric, and base plate materials as well as layer thicknesses offered by the Bergquist Company, a leading manufacturer of IMS boards, were reviewed in detail. Using the IMS design guide provided by Bergquist, the dielectric material was selected first. Unlike conventional IMS dielectric materials, Bergquist dielectrics are a polymer and ceramic blend which have increased dielectric strength and higher thermal conductivity. [25] The multi-purpose (MP) dielectric having a thermal conductivity of 1.3 W/(m·K) was selected based on a switching stage maximum power density in the vicinity of 100W/in^2. The smallest dielectric thickness of 3mils was chosen for a sufficient operating voltage rating of 120V.

Circuit layer copper thickness was selected next. Equation (3.3) shows the relationship between trace width, temperature rise, and current for IMS circuit traces. W, T_S, I, R_S, K_S and T_R represent: trace width (m), dielectric thickness (m), current (A), conductor sheet resistivity (Ω/square), dielectric thermal conductivity (W/(m·K)), and trace temperature rise (K or ºC), respectively. Selecting all other parameters and solving (3.3) for R_S in Ω/square allows a

$$W = \left[\frac{T_S \cdot I^2 \cdot R_S}{K_S \cdot T_R} + T_S^2 \right]^{\frac{1}{2}} - T_S \tag{3.3}$$

$$h = \frac{\rho}{R_S} \tag{3.4}$$

corresponding copper weight to be determined using (3.4), where ρ is the resistivity of copper (Ω·m), and h is the conductor thickness (m). For large temperature rises, the resistivity value used in (3.4) should be the corrected for the conductor temperature rise T_R using (3.2). For small temperature rises a constant resistivity value can be assumed.

Trace thickness for the design was calculated based on switching stage current, minimum trace width, and the selection of a 3mil thick multipurpose dielectric. The largest average bus current per phase of 85A was used in the calculation. The minimum DC bus trace width of 400 mils was also used along with a low trace temperature rise of 0.5ºC and the dielectric parameters, to solve (3.3) for R_S. The trace thickness was determined in (3.4) from sheet resistivity and the resistivity of copper at an ambient temperature of 293K (19.85ºC). [27] Equation (3.2) was not used, since the specified temperature rise caused a negligible increase in copper resistivity.

$$R_S = \frac{K_S \cdot T_R \cdot (W^2 + 2W \cdot T_S)}{I \cdot T_S} = \frac{(1.3)(0.5)((0.4 \cdot 0.0254)^2 + 2(0.4 \cdot 0.0254)(0.003 \cdot 0.0254))}{(85)^2 (0.003 \cdot 0.0254)} = 124 \mu\Omega / sq$$

$$h = \frac{\rho}{R_S} = \frac{1.69 \cdot 10^{-8}}{1.237 \cdot 10^{-4}} (39.37) = 0.0054 in$$

The copper thickness was calculated to be 5.4mils; therefore, standard 4oz/ft^2 copper sheet having a thickness of 5.6mils was selected.

Although several base layer materials were offered, the two most common materials; aluminum and copper, were considered. These base materials were available in standard thicknesses ranging from 20 to 125 mils, with the cost of copper equal to roughly three times the cost of aluminum for a given layer thickness. An aluminum base layer of 0.62 mils was recommended to provide stack rigidity for the 6.5" by 7" board size. [25]

3.4. Skin Effect on Conductors

The skin depths with respect to selected copper trace thickness and brass connector size were determined. The skin affect or depth of penetration of current in a conductor is inversely related to frequency. Higher frequency currents tend to travel along the surface or skin of a conductor, while lower frequency currents propagate through it more uniformly. Often the concept of skin depth is misinterpreted as the conductor depth needed to carry an alternating current of a certain frequency. Instead, it should be regarded as the conductor depth most utilized by an alternating current. The skin depth is defined as the distance in a conductor by which the amplitude of an alternating current is reduced by a factor of e^{-1} or 0.37. [29] The formula used to calculate skin depth is given as (3.5), where f is the frequency of the current (Hz), μ is the permeability of free space ($4\pi \cdot 10^{-7}$ H/m), σ is the conductor electrical conductivity (S/m), and δ is the skin depth (m).

$$\delta = \frac{1}{\sqrt{\pi \cdot f \cdot \mu \cdot \sigma}} \tag{3.5}$$

At a frequency of 50kHz (sinusoidal approximation) the skin depths of copper and brass were calculated and converted to mils to give 11.5 mils and 22.8 mils respectively. The first of these values indicated that increased copper trace thicknesses up to and exceeding 14 mils ($10oz/ft^2$) would be well utilized and provide reduced current densities in both the AC and DC board traces. The skin depth of brass, compared to the connector size selected, indicated that further increases in size would produce less significant benefits.

3.5. Switching Stage Construction

After completing the switching stage design, the board was etched and populated. Constructing the board in-house allowed changes and improvements to be made more easily during the design process. It also allowed faster production times and was most cost effective during the prototyping phase. Several precautions and considerable care were taken during these steps to prevent circuit flaws. The results were quite good.

The first step in the etching process was developing a high contrast scaled negative of the board layout. A black and white negative of the image was printed and used to photo expose the layout onto a transparent film. The film was developed to become the photo etching template for the circuit board.

The IMS board was then prepared for photo exposure. An area of IMS material was cut to be slightly larger than the circuit area. Both surfaces of the material were cleaned using solvents to remove any dirt or oils. The solvents were then rinsed from the board using deionized water, and the surfaces were air dried to prevent the formation of residues. A thin coating of photo-resist gel was then spread uniformly onto the circuit side of the board. The coating was hardened by baking the board at 80ºC for 40 minutes. After cooling, the etching template was placed over the photo-resist surface and secured using tape in an effort to minimize the formation of air pockets between the surface and the template. The board and template were then placed in an ultraviolet exposure chamber for 20 min to develop the photo-resist coating. A photo developer solution was used to dissolve the coating on unexposed areas of the board. During this step, dissolving time was closely monitored and the board was handled with extreme care to avoid peeling of the exposed photo-resist traces.

After rinsing and drying the board, small areas of partially dissolved photo-resist were carefully removed in preparation for etching. The edges and back of the board were sealed with tape to prevent etching of the thermal substrate. The board was then placed in a spray etching machine for several minutes until all exposed copper was removed. It was rinsed thoroughly with water to neutralize and remove etching fluid, and the tape mask was peeled away. The photo resist coating on the traces and any glue left behind by the tape was removed with solvent.

Board fixtures and components were mounted in three stages. Brass connectors were mounted first to establish fixed reference points. Solder paste having a reflow temperature of 220ºC was applied. A template of FR-4 circuit material was made to hold all connectors and terminals in their proper alignment during layout and solder reflowing. The board was then reflowed in a controlled convection oven. At high temperatures, a thin layer of oxide was formed on the exposed copper traces. Before mounting additional components, the oxide was removed from these areas with an abrasive.

Devices and remaining terminals were then positioned and bonded using eutectic solder having a reflow temperature of 180ºC. During this process the template and brass connectors were used to hold the terminals in alignment. Temperatures between 180ºC and 220ºC were used to allow the second stage solder to reflow, while preventing the first stage from reflowing. During this process, the board was heated using either the convection oven or a hot-plate. Although the convection oven was initially used, it retained a large amount of heat after the reflow process was complete. This was less desirable, especially when using IMS board material, which has a large heat capacity. To reduce thermal stresses on devices, a preheated hot-plate was used to rapidly transfer the board through a shorter duration reflow profile. Device temperatures were also reduced in this case, with the top side of the board exposed to ambient air.

Bypass capacitors were mounted last. Because of their lower maximum temperature ratings, they were soldered using a different process. A hot-plate was used to raise the temperature of the board to approximately 160ºC. This was below the maximum operating temperature of the MOSFETs. The film bypass capacitors were then placed over the devices with leads formed to make contact with the traces. A soldering iron was used to momentarily add sufficient heat to bond each capacitor lead to the board. This method reduced the thermal stress on the body of each capacitor. It allowed the capacitors to rest above the surface of the

board, on the thermally insulating epoxy side of the TO-263 packages. The temperature in this region was closer to ambient temperature. Figure 3-5 shows the early converter setup. Although the overall structure of the converter remained unchanged, modifications were made to individual sections during the course of the testing phase.

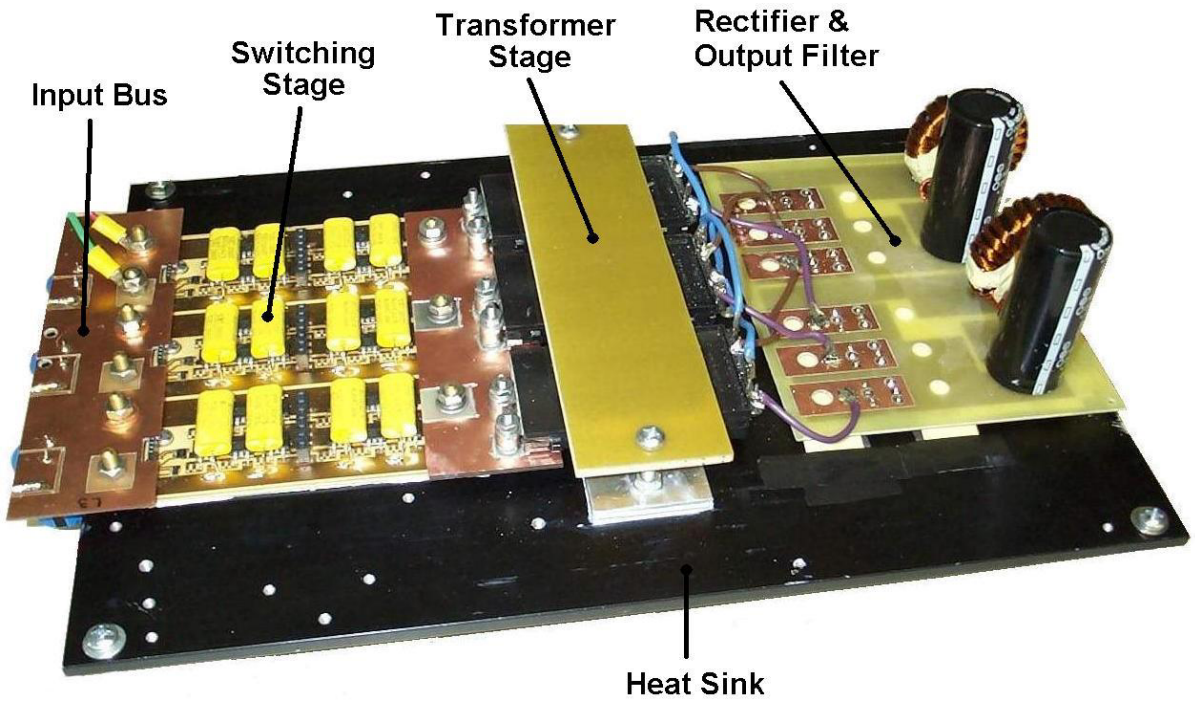

Figure 3-5. Converter Setup

Chapter 4. Converter Testing and Results

4.1. Test Setup

4.1.1. Gate Signal Generation

A digital signal processor (DSP) card and a phase shifting circuit were used to generate gate signal waveforms for the MOSFET gate driver. Initially, a clock frequency of 3.3MHz was used to provide the PWM signals. Because PWM channels of the TMS320LF2407A DSP used are specifically designed to output complementary waveforms, they were not able to provide all six gate signals. The six switching stage gate signals were required to have the same pulse width to provide transformer volt-second balancing. Each phase-leg pair of gate signals required a 180 degree phase shift. Having 120 degree delays between three PWM DSP signals, then delaying each signal by 180 degrees was not the easiest approach. Instead, the signal of one PWM channel was used, and successively phase shifted by 60 degrees five times to provide the six waveforms. Three SN74ACT2228 dual 256-bit FIFO chips were cascaded for the delay circuit. Four individual DSP outputs provided FIFO circuit control. A reset signal triggered at the beginning of each period reinitialized the FIFO read and write pointers; effectively clearing the FIFO memory for the following cycle. The DSP generated clock signal was used as both the FIFO read and write clock signals. A delay set signal was used as the read pointer enable, while the write enable was held high throughout the cycle. [30] FIFO input data lines were either the DSP PWM signal or phase shifted versions of it output by a preceding FIFO chip. The PWM signal duty cycle was controlled using a 5kΩ potentiometer to scale a DSP channel voltage from 0V to 5V. The DSP and FIFO boards were designed to plug directly into the gate drive board and receive power from a 5V linear regulator located on the gate drive board.

A six channel isolated flyback gate driver was used to ensure adequate top and bottom switch driving capability. Although charge pump high-side driver chips were considered, a reliable charge pump gate drive circuit having a negative turn-off voltage was unable to be

implemented. The flyback gate drive board was built for a supply voltage ranging from 20V to 48V and was designed to plug directly into the switching stage board to reduce gate contact resistance and gate lead inductance.

4.1.2. Source and Load Setup

Primarily, two DC power supplies were used throughout the converter testing phase. For low power testing, a 20-to-30V, 1.5kW supply was used. The supply was current limited at 60A for an output voltage of 24V. Before a larger power supply was available, a battery bank was used as an intermediate source during early tests. A 0-to-30V, 330A supply was used for power levels greater than 1.5kW. Although the converter input voltage range exceeded the voltage limits of these sources, the most critical operating points to be tested were those associated with low input voltage and high input current. These conditions produced the highest stresses on the converter stages; especially the switching and transformer stages.

The gate drive circuitry was powered using a 30V, 3A supply. To begin each test, the gate drive was powered before the converter input source was turned on. This prevented space charging of the MOSFET gates to avoid MOSFET conduction in the presence of large available source currents. It also allowed the duty cycle to be verified or reset for a safe converter operating condition before startup.

Two configurable load banks were used during testing. A low power load bank was used for power levels up to 2.6kW, and contained four identical sets of five resistors. Each resistor set consisted of two parallel 500Ω resistors, two parallel 250Ω resistors, and one 250Ω resistor. During early testing, the load bank was configured to provide matched 200V loads for the two converter outputs. To reduce both the number of separate loads needed and the number of measured converter operating parameters for successive tests, the converter outputs were tied at the midpoint to provide a single 400V output. The high power load was used for the 400V output configuration for power levels above 3kW. It was made up of six 9Ω resistances, each rated for 5kW.

4.2. Initial Testing

4.2.1. Calibration of Measurements

The converter was first tested in the split 200V output configuration. Measured operating parameters included input voltage, input current, output voltage 1, output voltage 2, output current 1, output current 2, and duty cycle. Input voltage values were recorded from a digital multi-meter, while the waveform was viewed on one of four oscilloscope channels using a differential probe. Input current values for the tests were recorded on a second scope channel from a 150A rated current probe. In later tests at higher current levels, a calibrated current shunt was used. Output voltages were each recorded from digital multi-meters. Due to the availability of only one additional scope current probe and a limited number of scope channels, one output current was measured using a probe, and the other was measured using a digital current meter. Duty cycle from a selected gate signal was measured on the remaining scope channel.

Converter operating parameters appeared to be correct, but indicated lower than expected converter efficiencies. Input power was calculated as the product of the measured input voltage and current. Output power was calculated as the sum of the voltage and current products of each output. A test result recorded for this condition is shown in Table 4-1.

Table 4-1. Initial converter test result

Duty	V_I	I_I	V_{O1}	V_{O2}	I_{O1}	I_{O2}	P_{O1}	P_{O2}	eff.
39.2%	24.87V	59.75A	201.4V	210.1V	2.87	2.86	578W	601W	79.3%

Inspecting the recorded data and load resistances allowed measurement errors to be identified. The load resistance and measured output current values were used to recalculate output power. Both load resistances were measured at approximately 83Ω before and after the converter test. The calculations predicted approximate total output power and converter efficiency to be 1363W and 91.7% respectively. Furthermore, solving for the load resistances associated with the measured output voltages and currents gave resistance values of 70Ω and 73.5Ω. Since it seemed unlikely that the load resistance values could have changed by

approximately 10Ω when powered for a short time, the output voltages given by the multi-meters were suspected to be incorrect.

Although all four scope channels were in use, channel assignments were changed to measure output voltage. Since the input voltage measured on the multi-meter and scope agreed, the differential probe was moved from the input bus to measure V_{O1}. A similar test was run to give the data in Table 4-2.

Table 4-2. Repeated initial test with scope measured output voltage

Duty	V_I	I_I	V_{O1}	V_{O2}	I_{O1}	I_{O2}	P_{O1}	P_{O2}	eff.
39.0%	24.85V	59.3A	237.3V	209.7V*	2.87	2.85	681W	N/A	N/A

* Read from volt meter

A significantly larger output voltage was measured on the scope. This value also agreed with the measured load resistances. Assuming a second output voltage proportional to V_{O1}, I_{O1}, and I_{O2}, of 235.7V gives an efficiency of 91.8%. The cause of the measurement discrepancies was determined to be the inaccuracy of the multi-meters at high voltage. They were no longer used to measure output voltage. Instead, the converter outputs were connected at the midpoint to reduce the number of output parameters. This allowed a single scope to be used to accurately monitor converter performance.

4.2.2. Initial Results

The converter was tested at source voltages ranging from 22V to 27V for output power levels of 500W to 3.8kW. Table 4-3 shows test results obtained for source voltages of 22V. The first three table entries list test results for the 1.5kW power supply source. It can be seen that the duty cycle required to produce a constant output voltage increased with output power. This was caused by converter conduction losses. Contact resistances between removable connections as well as conductor resistance caused voltage reduction mostly on the primary side of the converter. On this side of the system, the interaction between circuit resistances and high currents slightly reduced the input voltage to the transformer primary, causing transformer output

voltage to be decreased by the amount multiplied by the turns ratio. Therefore, duty cycle needed to be increased to overcome the voltage loss.

Table 4-3. Initial results for minimum source voltage tests, 500W to 3kW

Duty(%)	V_I	I_I	V_O	I_O	P_I	P_O	eff (%)
37.9	21.9	26.6	424.8	1.28	583	544	93.3
39.5	21.9	52.1	421.5	2.52	1138	1062	93.1
40.9	21.8	70.9	425.1	3.38	1546	1435	92.8
42.0	22.0*	158.2	400.3	7.66	3487	3067	88.0
42.1	22.4*	159.5	404.0	7.72	3570	3118	87.3

* Battery source

Converter efficiencies decreased during these tests for increases in power. Although two different sources were used for the tests shown, the results are fairly consistent. During this stage of testing, efficiency reductions were attributed to increased conduction losses. Temperature rises were seen on both the switching and transformer stages to support this claim. Although increased temperatures were still within component operating temperature ranges for short duration tests, results could not be obtained for the highest power levels due to device voltage stress.

Large drain to source voltage overshoots were seen across each MOSFET device immediately following device turn-off. The voltage overshoot refers to the level to which the voltage extends beyond the source voltage. These spikes were attributed to the interactions of MOSFET current and transformer leakage and switching stage trace inductances as well as the inductances of the interconnections between the two stages. As power levels were increased, higher input currents were sourced. The abrupt commutation of the current shared by the device and parasitic inductance elements caused a large voltage transient to be formed across the device despite the presence of device anti-parallel diodes and phase bypass capacitors. Figure 4-1 shows typical MOSFET drain-to-source waveforms at low power.

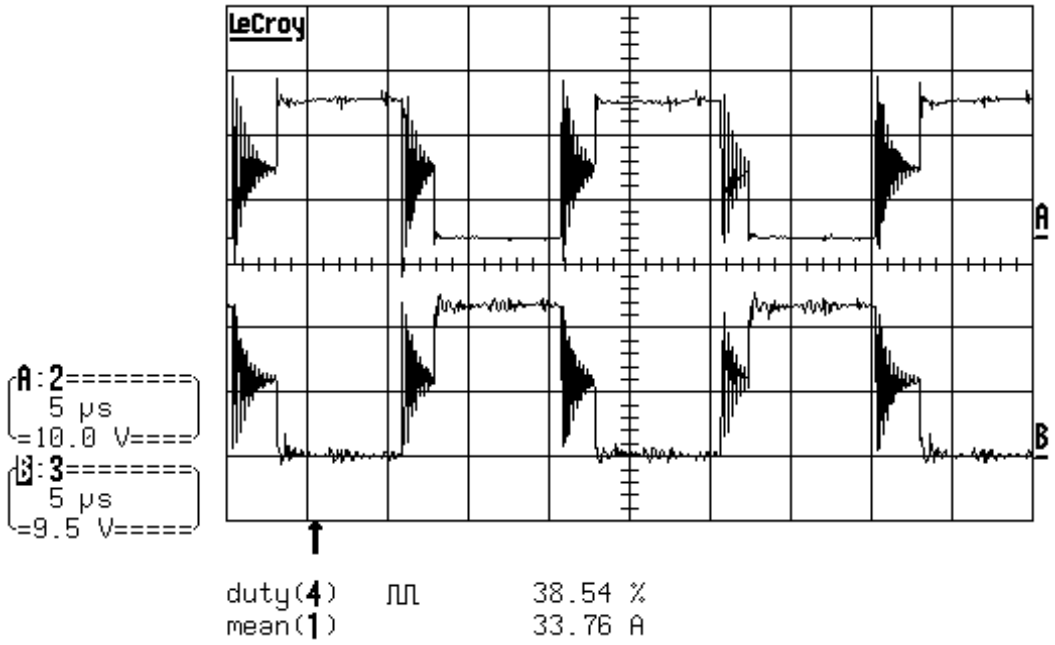

Figure 4-1. Drain-to-source voltage waveforms ($P_O \approx 600W$)

The MOSFET waveforms in Figure 4-1 show the drain-to-source voltage of the top and bottom switches of phase A, respectively. These waveforms should not be confused with the ideal MOSFET gate signals shown in Figure 2-2. In this case, portions of the waveform at low voltage correspond to MOSFET or body diode conduction, while high voltage states represent MOSFET off-state voltage equal to the input bus voltage. The intervals between switch conduction states show the switch voltage during phase-leg dead-time. As expected, the device voltage oscillates as it is gradually damped to half the input voltage during these intervals. The oscillations are the result of energy transfer between the parasitic output capacitance of the MOSFETs and the parasitic inductances. The waveforms were captured for an input current of 33.8A and an output power of approximately 600W. At this current level, the magnitude of the overshoot voltage was small compared to the DC bus voltage, and therefore did not produce a significant increase in MOSFET voltage stress.

Figure 4-2 shows device voltage (Ch 1) and its corresponding gate signal (Ch 4) for an output power of 3.8kW. The voltage seen at the device turn-off exceeds 50V, and is significantly closer to the device breakdown voltage. To reduce the voltage overshoot and damp the voltage oscillations during dead-time, an RC snubber was placed across each device.

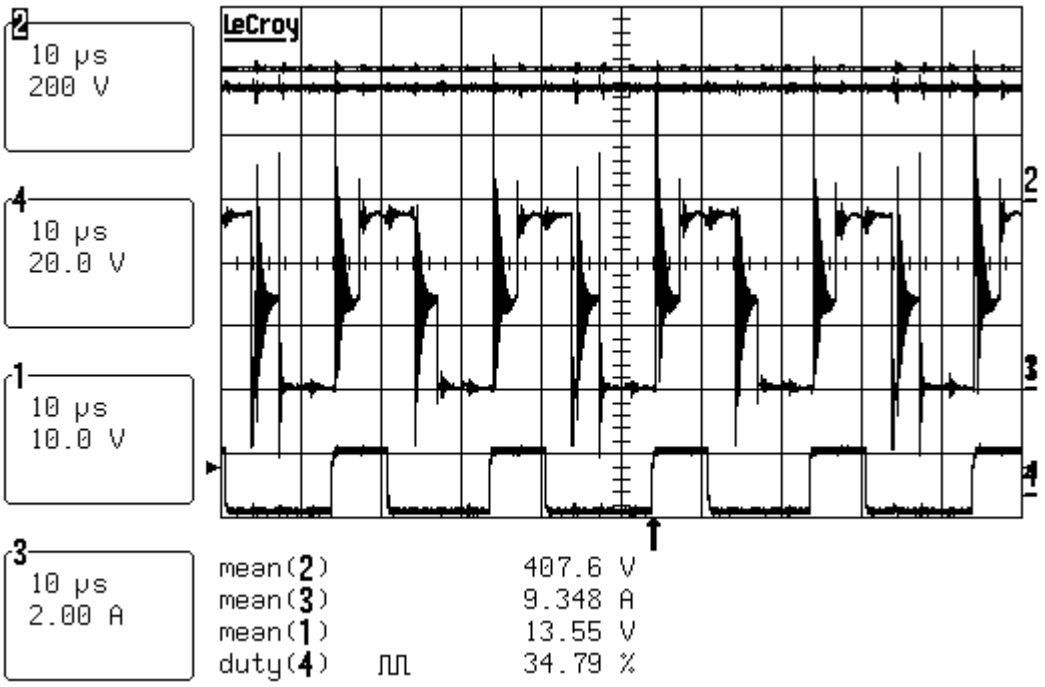

Figure 4-2. Drain-to-source voltage waveform (Ch 1), ($P_O \approx 3800W$)

4.3. MOSFET Snubber

4.3.1. Snubber Design

A passive RC snubber was chosen to damp MOSFET voltage transients. As its name implies, an RC snubber consists of a capacitor and resistor typically placed in series across a switching device. The network is designed to slow voltage transients across the switch and dissipate transient energy. Yet by doing so, the snubber reduces converter efficiency and also slows MOSFET switching speed. [31] Other snubber designs incorporating a diode (RCD) can be used for improved results. However, the implementation of more complex snubbers was not cost effective or practical for the switching stage layout. By carefully selecting snubber values, adverse effects of the RC design can be minimized.

Snubber design guidelines for a series parasitic inductor-capacitor network were considered when selecting snubber values. The guidelines are shown as (4.1) to (4.3). In (4.1),

R represents the snubber resistance, and L_P, and C_P represent the parasitic inductance and capacitance causing the oscillations. In this case L_p was the loop inductance given by the sum of the transformer primary leakage inductance (28nH, assuming one primary winding current) and the parasitic inductances of the switching stage and switching and transformer stage interconnections, including MOSFET inductance. Since the parasitic circuit inductance was assumed to be small compared to the winding leakage inductance, and was unable to be accurately measured, it was omitted from the calculation. The C_P term was set equal to the equivalent MOSFET output capacitance (1nF for FDB045AN08A0). The square root term is equivalent to the characteristic impedance of the parasitic LC network. [31]

Relationship (4.2) shows that the selected snubber capacitance should be large compared to the MOSFET output capacitance. The resulting RC snubber time-constant should be small with respect to the switching period, while large with respect to the voltage rise time expressed as half the measured ringing period. The power dissipation of the snubber is given by (4.3), where P is the snubber power dissipation, V_c is the snubber capacitor voltage, and f_{sw} is the MOSFET switching frequency. [31]

$$R = \sqrt{\frac{L_P}{C_P}} \tag{4.1}$$

$$C >> C_P \tag{4.2}$$

$$P = C \cdot V_C^2 \cdot f_{sw} \tag{4.3}$$

Calculating snubber values and meeting selection guidelines gives:

$R = \sqrt{\frac{L_P}{C_P}} = \sqrt{\frac{28 \cdot 10^{-9}}{1 \cdot 10^{-9}}} = 5.3\Omega$ Select R = 4.7Ω standard value based on availability

Select C = 10nF >> C_P = 1nF

Power dissipation: $P = C \cdot V_C^2 \cdot f_{sw} = 10 \cdot 10^{-9} \cdot 25^2 \cdot 50 \cdot 10^3 = 0.31W$

RC = 53ns << T_{sw} = 20us

$T_{V\_RISE} = 0.5 \cdot \frac{1}{8 \cdot 10^6} = 62.5ns$ which is comparable to RC = 53ns

4.3.2. Snubber Evaluation

The snubber was first incorporated into a converter simulation model for evaluation. Because the Saber converter model did not accurately represent the MOSFET turn-off voltage spike or the voltage ringing during dead-time, a PSpice system model was created. The PSpice model was designed to approximate the MOSFET voltage without the snubber. Figure 4-3 shows the modeled MOSFET voltage waveform for a simulated condition of 3.8kW with parameters comparable to the captured waveform shown in Figure 4-2. The simulated waveform had a duty cycle of 34.5% and showed a parasitic ringing frequency of 6.3MHz, which was close to the ringing frequency of roughly 8MHz measured for the captured waveform. However, the model did not truly represent the amplitude of the voltage spike at device turn-off. Because additional parasitic components such as circuit inductances were not able to be accurately modeled, the amplitude of the voltage spike at device turn-off appears lower in simulation than in the actual system.

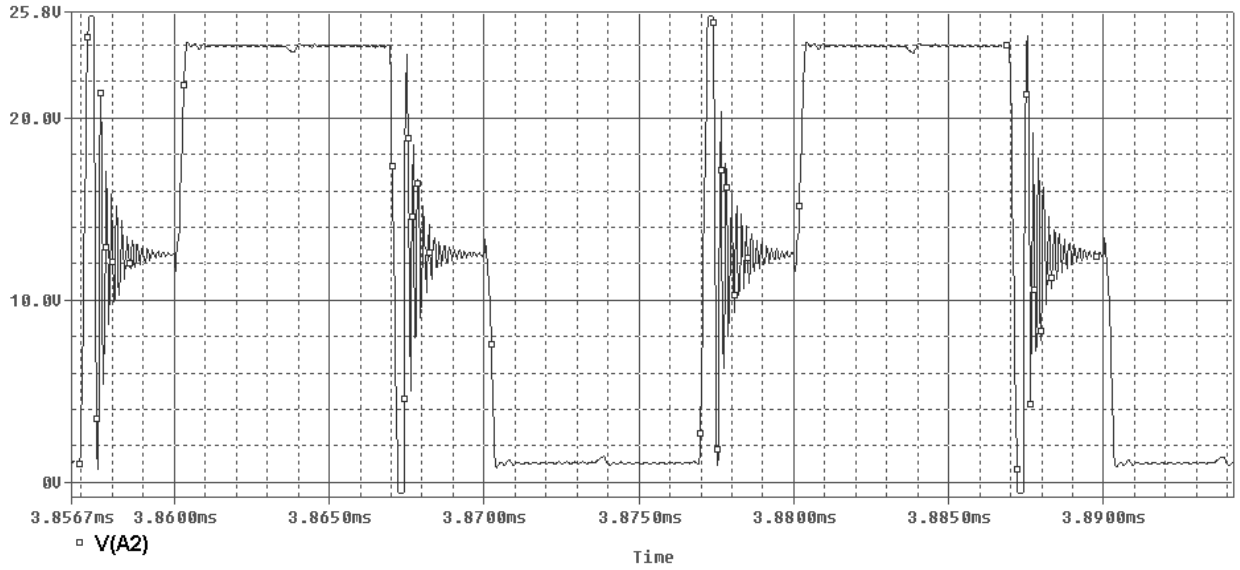

Figure 4-3. Simulated MOSFET voltage waveform

The snubbers were placed into the PSpice converter model, and the model was simulated at the same test condition. Figure 4-4 shows the resulting MOSFET voltage waveform.

Although no attenuation of the voltage spike at the device turn-off was shown, the snubbers significantly damped the parasitic ringing during phase-leg dead-time. They also reduced the parasitic ringing frequency to 2.9MHz, and therefore reduced the switch turn-off voltage rate of rise.

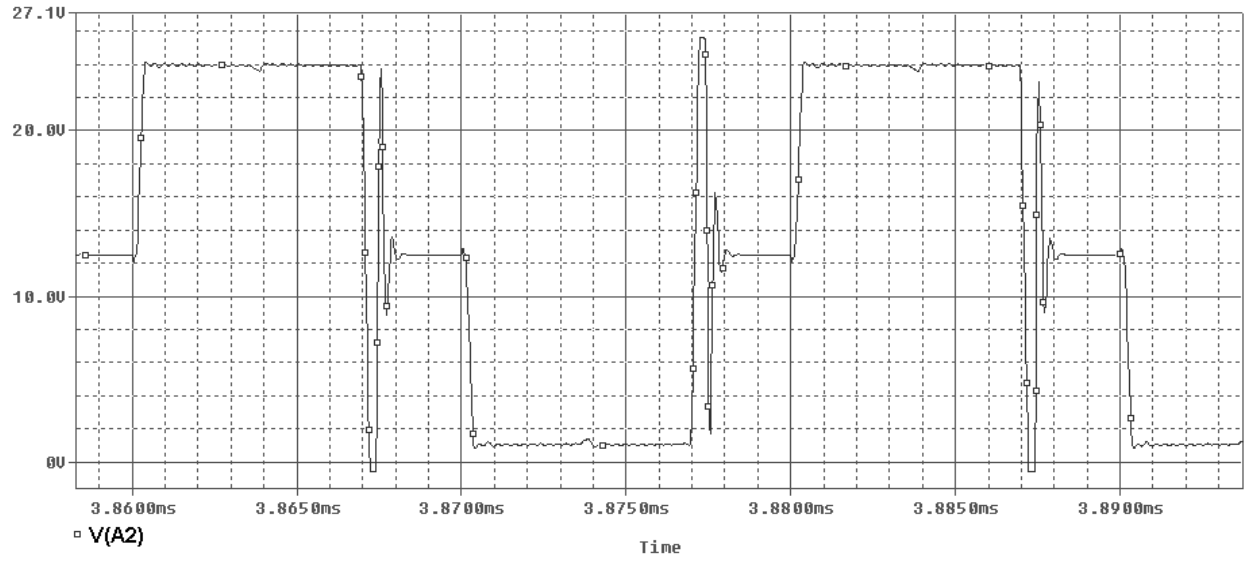

Figure 4-4. Simulated MOSFET voltage with RC snubber

Snubbers were added to the switching stage using low inductance ceramic chip components. The small size of these components allowed the snubbers to be mounted directly across the pins of each device. This configuration further reduced additional parasitic inductance associated with snubber lead length and is shown in Figure 4-5.

Snubber operation was tested at the 3.8kW load condition. Figure 4-6 shows the resulting phase A bottom switch voltage waveform (Ch 1). The results agreed well with simulation. The parasitic ringing was damped during the dead-time period, and the amplitude of the turn-off voltage spike was reduced by nearly 5V. With a more stable switch voltage, longer duration high power tests were run to evaluate converter losses and thermal response.

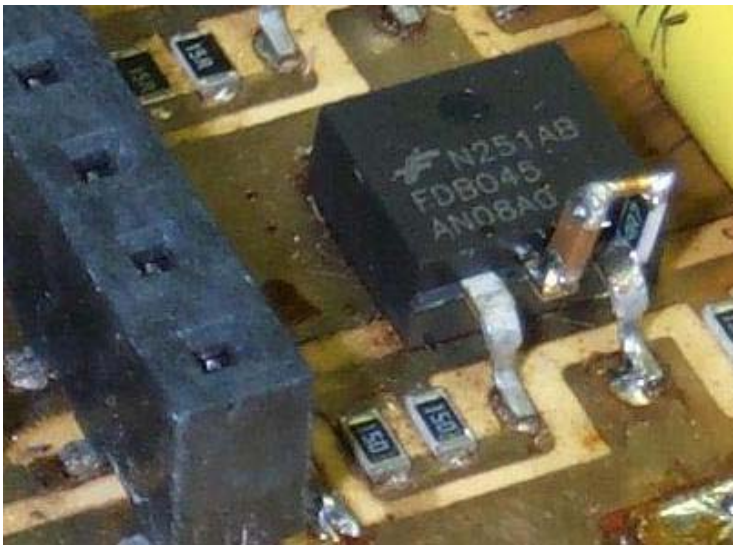

Figure 4-5. Low inductance device mounted snubbers

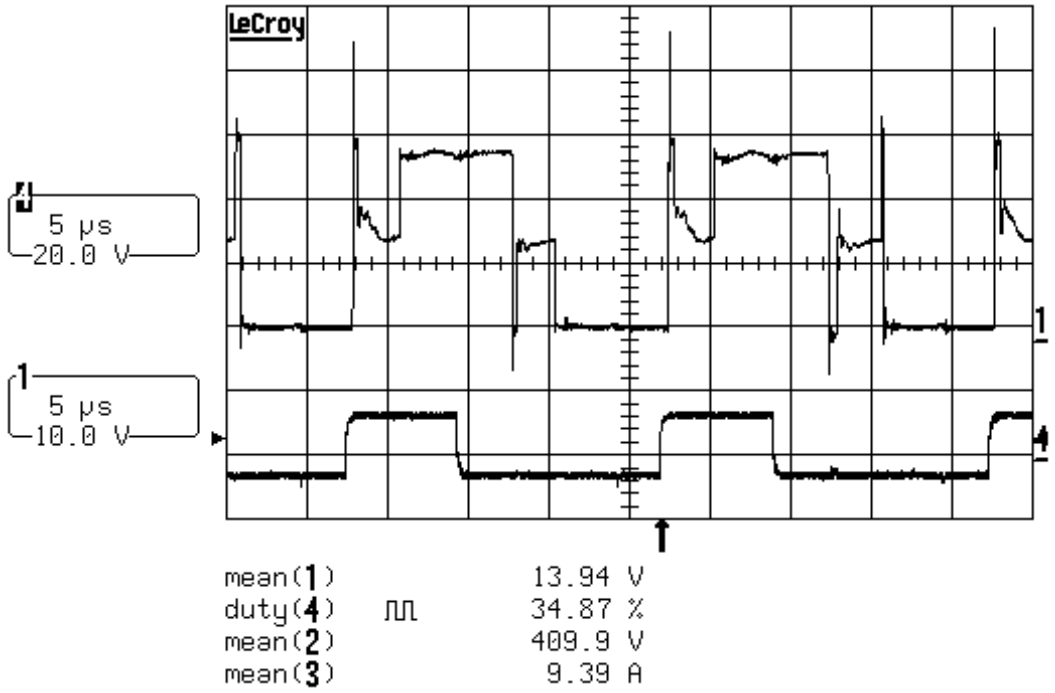

Figure 4-6. Drain-to-source voltage waveform with snubbers (Ch 1), ($P_O \approx 3800W$)

4.4. Timing Imbalance

4.4.1. Temperature Rise

As longer duration test were attempted, transformer and switching stage temperatures increased. This trend escalated dramatically for higher power levels. Of the two stages, the transformers were seen to have a much more rapid temperature rise. Starting from an ambient temperature of approximately 23ºC, within the first minute of operation at the 3kW load condition, transformer temperatures rose to over 60°C. These values were measured using a thermocouple and an infrared temperature meter. The rate of temperature rise slowed only slightly as temperatures continued to increase toward a high temperature thermal equilibrium. Tests were stopped before the 100°C transformer temperature rating was reached. Table 4-4 shows converter data for a one and a half minute 3kW test.

Table 4-4. 3kW test results for a 1.5min test

Duty	V_I	I_I	V_O	I_O	P_I	P_O	eff.
41.9%	22.0V	155.5A	391.1V	7.49	3413W	2929W	85.8%

Converter efficiency was lower by nearly 2% for the 1.5 minute test. These results along with the data in Table 4-3 showed that reductions in efficiency were much greater for proportional increases in power. The trends were believed to be caused by circulating currents within the delta windings of the transformer primary. This accounted for the larger conduction losses and increased transformer temperatures at higher power levels. Transformer winding imbalances are a known cause of circulating currents in converter systems having multiple primary windings. Although mismatches between transformers always exist to some degree, planar transformers benefit from an accurate and repeatable design. Therefore it seemed unlikely that circulating currents large enough to produce the effects could be caused only by mismatches in transformer winding resistances and inductances. It was more likely that differences in transformer primary side contact resistances would have greater effects. [32] System simulations showed that timing imbalances in the switch gate signals played a large role in the creation of

circulating currents within the delta connected primary. With asymmetric switching transition times, conduction intervals vary between windings causing disproportionate differences between current levels in the primary and secondary windings. Figures 4-7 and 4-8 show phase B transformer primary winding current, secondary winding current, and secondary winding current scaled by the transformer turns ratio for a more visible comparison.

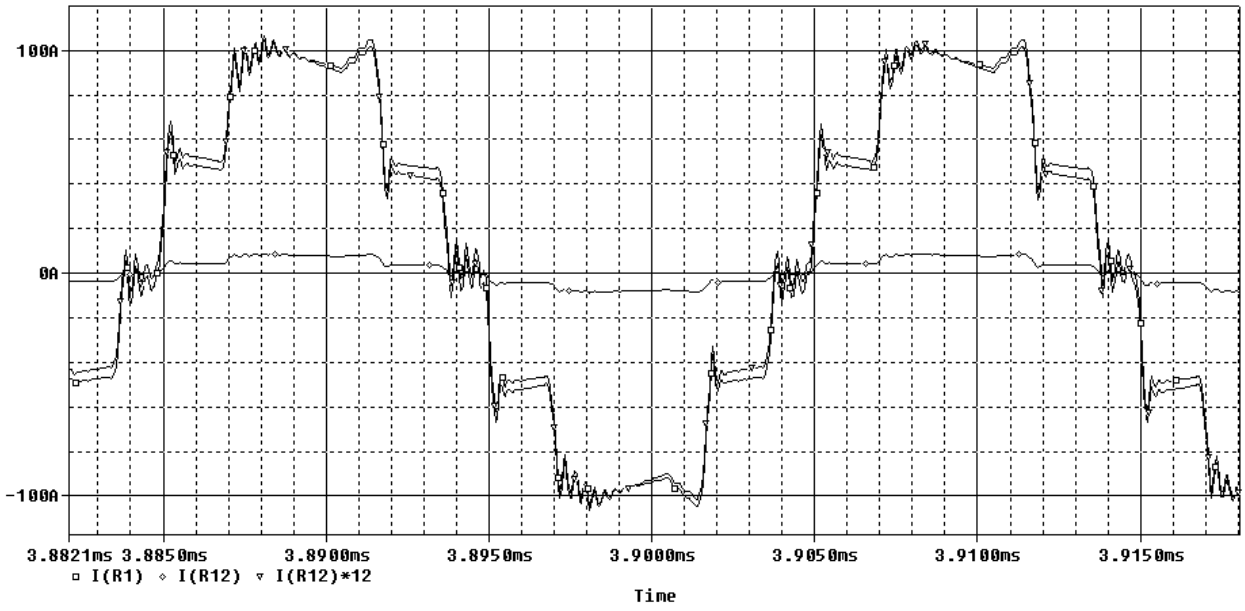

Figure 4-7. Simulated phase B primary and secondary winding currents 40% duty, 3kW

Figure 4-7 shows these results for balanced switch timing, while Figure 4-8 illustrates the effects for an additional 1μs phase shift of the phase B top switch. The primary current and scaled secondary current waveforms of Figure 4-7 agree well with only slight differences which are balanced on both sides of the waveform. However, the single imbalance of only 1μs caused a significant current imbalance in the waveforms of Figure 4-8. The imbalance reflects primary current which is not transferred to the secondary and therefore circulates within the delta windings. For switch timing imbalances affecting all three phases, circulating currents are increased, especially for high power tests having higher current levels.

Although gate signal timing imbalances also produce net changes in transformer volt-second balance leading to core saturation, this effect was not fully observed. In these cases, transformer magnetizing current imbalances are far smaller than the imbalances in load currents.

Changes in MOSFET conduction drops were believed to compensate the imbalance and prevent core saturation. [1] In such cases, core flux could operate about a small offset instead of the origin of the B-H loop. Increases in several MOSFET conduction drops would account for the increased power dissipation and corresponding temperature rise of the switching stage.

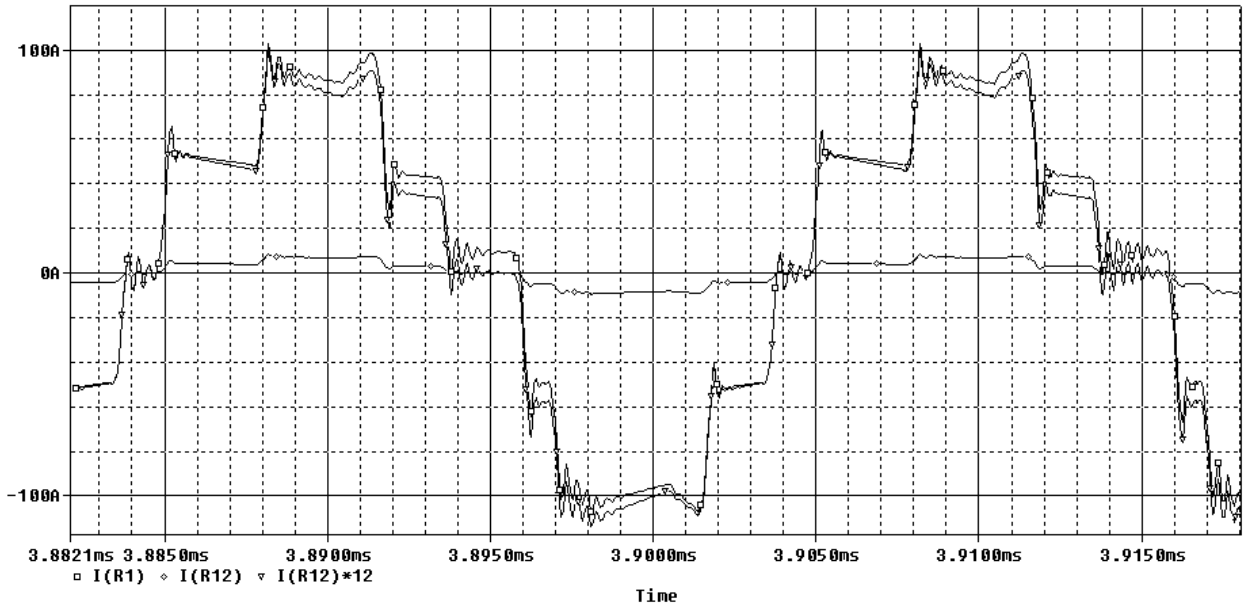

Figure 4-8. Repeated simulation with 1μs phase shift error on phase B top switch

4.4.2. Timing Improvements

The outputs of the DSP and FIFO circuit were considered in more detail. The focus was placed on the three most critical DSP signals affecting gate waveform symmetry. These signals were the clock, delay set, and PWM signal itself. It was determined that the FIFO clock frequency could be increased from 3.3MHz to 10MHz. This adjustment was made to provide three times more resolution for PWM signal transitions. If a PWM signal transition was to be executed immediately at the beginning of a clock cycle, the transition would not take place until the end of that clock cycle. Therefore the largest PWM signal error (not phase shift error) for the 3.3MHz clock was 0.3us as opposed to 0.1us for the 10MHz clock.

The accuracy of the delay set signal was also improved. With the change in clock frequency, a new delay value was needed for the 60 degree phase shifts. Due to the increase in clock frequency, this value was also able to be made more accurate. However, by using the same delay set signal to successively shift five PWM signals, error in the delay value caused phase shifting errors to accumulate. The last signal output by the FIFO circuit was shifted from the original DSP signal by 300 degrees, with an error of five times the delay value. For this reason, great care was taken to make sure the delay value was as accurate as possible.

The accuracy of the PWM signal was also affected by its means of duty cycle control. The scaled voltage determined by the set point of the 5kΩ potentiometer was subject to common-mode noise. The noise caused the duty cycle of the PWM signals to fluctuate slightly. To eliminate the fluctuations, duty cycle adjustment was implemented digitally using two momentary contact switches to increase and decrease the duty cycle by small set increments.

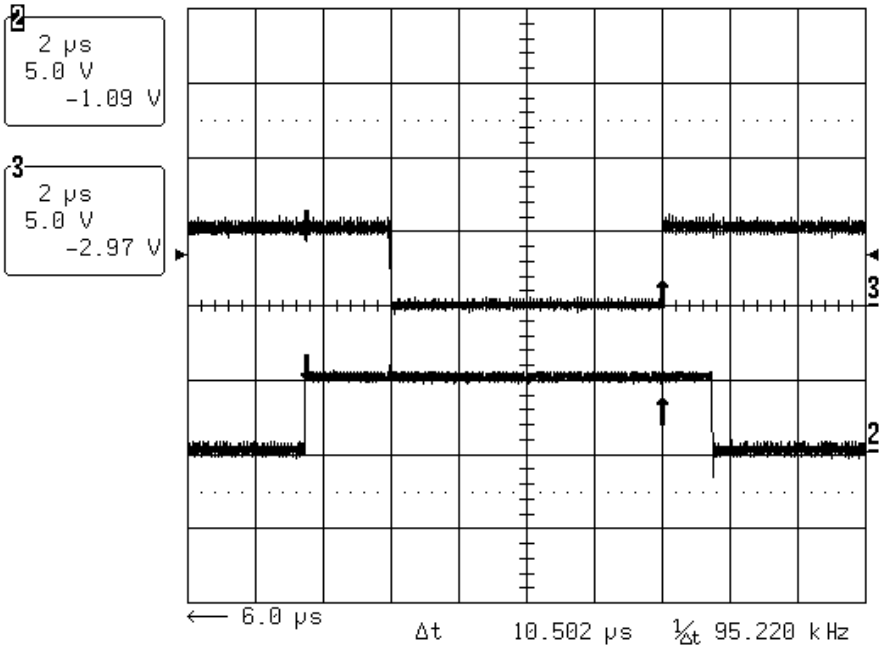

Figure 4-9. Phase C top and bottom switch logic level gate signals

Overall, the resulting gate signals were greatly improved. Although phase shifting of the channels was not exact, phase gate signal pairs showed shift errors of only 0.5µs. The shift between these signal pairs represented the summations of three 60 degree phase shifts and the

associated 60 degree shift error. Therefore, the 60 degree shift error was calculated to be 0.167μs or 5% of the shift. Figure 4-9 shows the shift of a captured pair of phase C top and bottom switch gate signals respectively for a duty cycle of 40%. The FIFO waveforms have logic levels of 0V and 5V and are inverted for the inverting gate driver circuit.

Chapter 5. Final Modifications and Testing

5.1. Continued Testing

5.1.1. Switching Stage Changes

In an effort to reduce switching stage parasitic components, the number of parallel MOSFETs per switch was dropped from six to four. Switch ratings were still adequate up to full power for this number of devices. However, this was done mainly to determine whether transient spikes would be reduced over the range of power levels previously tested. The original switching stage board had been modified several times during a three week testing phase of a different project for which the board was used. These modifications had compromised the state of the board. The switching stage board was replaced with an untested board which had been held in reserve for a lower input voltage application. The second board was populated with FDB035AN06A0 devices. These were 60V, 80A rated MOSFETs having an on resistance of 3.5mΩ, belonging to the same family of devices as those previously used. Low power tests were begun without the use of snubbers.

5.1.2. 33% Duty Cycle Anomaly

The board was first tested near 500W. Table 5-1 lists data from the first two test conditions. An input voltage of 25V was used for moderate input currents. This caused duty cycles to fall below 33.3% under the light loads. Efficiencies in this operating region were lower than the efficiencies for duty cycles above 33.3%. This was mainly attributed to more frequent and longer duration anti-parallel diode conduction. Diode conduction was increased as a result of more frequent discontinuous current conduction in the MOSFETs during transitions between intervals of one and two conducting switches in the 16.6% to 33.3% duty cycle range. The

forward voltage drop of the anti-parallel diode is approximately 1V which accounts for about 4% of a 25V converter input. Another factor is that duty cycles in this range were encountered for light load conditions in which transformer core losses produced a larger percentage of total converter power loss.

Table 5-1. Low power test results for the 60V switching stage

Duty	V_I	I_I	V_O	I_O	P_I	P_O	eff.
30.1%	25.0	15.5	404.4	0.88	387	356	92.0%
32.1%	25.0	29.2	399.8	1.70	730	678	93.1%

The MOSFET voltage waveform was seen to fluctuate during the second test condition causing large MOSFET voltage transients and wide output voltage variations. The test data listed in Table 5-1 for this condition was obtained from the point at which the data was captured. The converter was powered down, and gate signals were reset and verified to be correct. The test condition was repeated and again gave chaotic behavior. Figures 5-1 and 5-2 show captured MOSFET voltage waveforms for the second test point listed in Table 5-1, and the repeated test, respectively. The two captures show very different results. The first MOSFET voltage waveform shows large voltage transients at both the device turn-off and at the turn-on of the opposite switch on the phase-leg. Yet, the change in switch timing was a greater concern. The conduction interval of the opposite switch (in this case the upper phase-leg switch), marked by the high state of the waveform, was shifted leftward. The effect was even more pronounced in the second waveform which shows even larger voltage spikes due to the overlap of the turn-off and turn-on transients. In this case, the amplitude of the spikes reached the 60V MOSFET rating. The waveform was captured and the converter was shut down immediately. The difference in output voltage for the two test points was also of interest. An output of 423V was reached for the second test. Although all switch waveforms were not able to be monitored simultaneously, the voltage increase could be explained by an increase in the shared conduction times of the top switch of phase C and the bottom switch of phase A. However, these switching imbalances did not cause any immediately noticeable transformer core saturation.

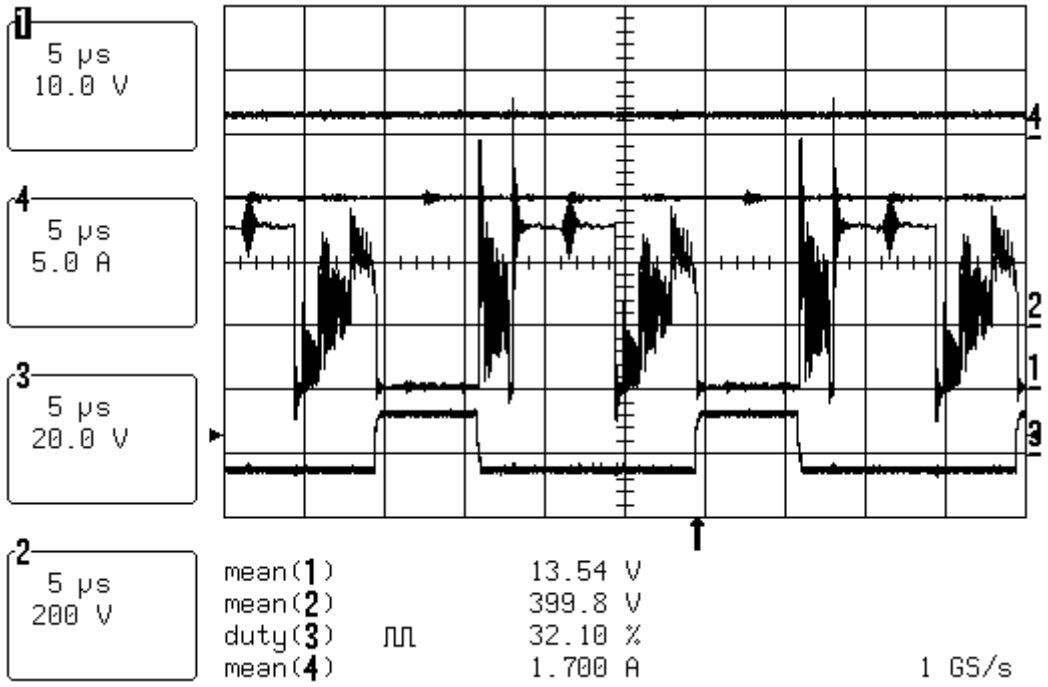

Figure 5-1. Table 5-1 test, phase C bottom MOSFET voltage (Ch1)

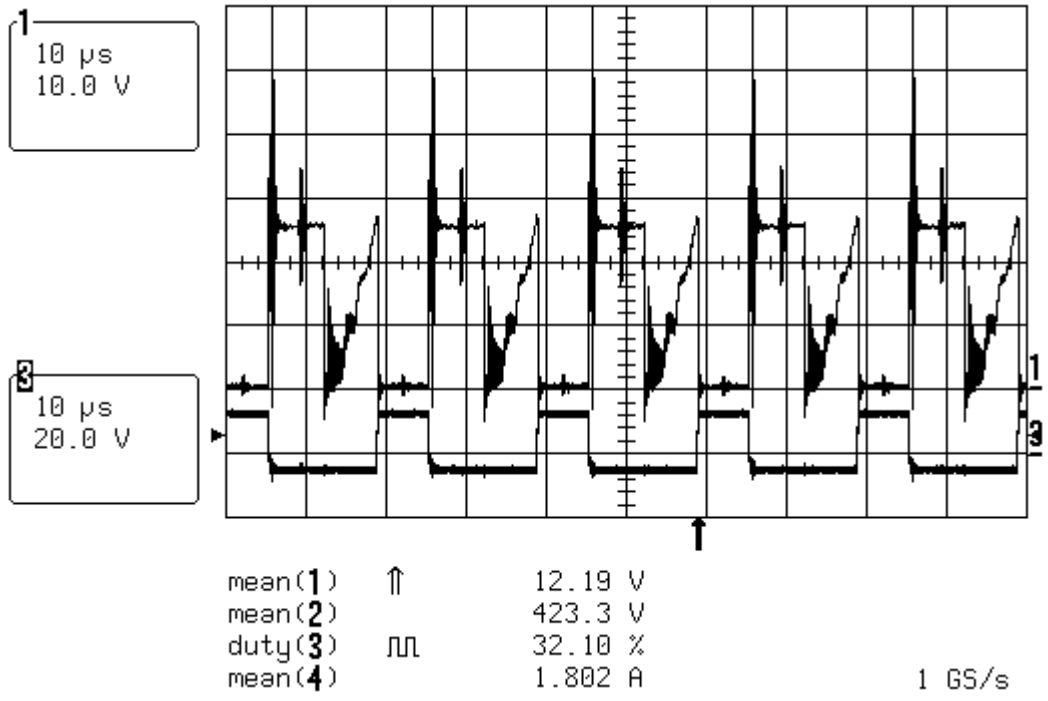

Figure 5-2. Repeated 32% duty cycle test, phase C bottom MOSFET voltage (Ch 1)

Other short duration tests were run for increased duty cycles. The duty cycle was moved to 33.1% with all other parameters unchanged. MOSFET voltage fluctuations were still seen, and the amplitude of the voltage spike was only decreased by about 5V. These tests were not repeated to collect additional data to more readily determine the causes of the voltage fluctuations. Once a condition was seen to potentially damage the switching stage, a new test point was selected. The duty cycle was then moved to 34.1% and the input voltage was dropped to 20V to reduce the amplitude of the voltage transients. Although output voltage was decreased, the results showed proper shifting between the phase-leg switch transitions. This caused a decrease in the amplitude of the voltage spike. Figure 5-3 shows the captured waveform from this test. When the converter was tested again under the same conditions with a duty cycle of 36.1%, the voltage spike at the turn-on of the upper switch showed a peak of only 28V. The spike at the lower switch turn-off was also reduced to 24V.

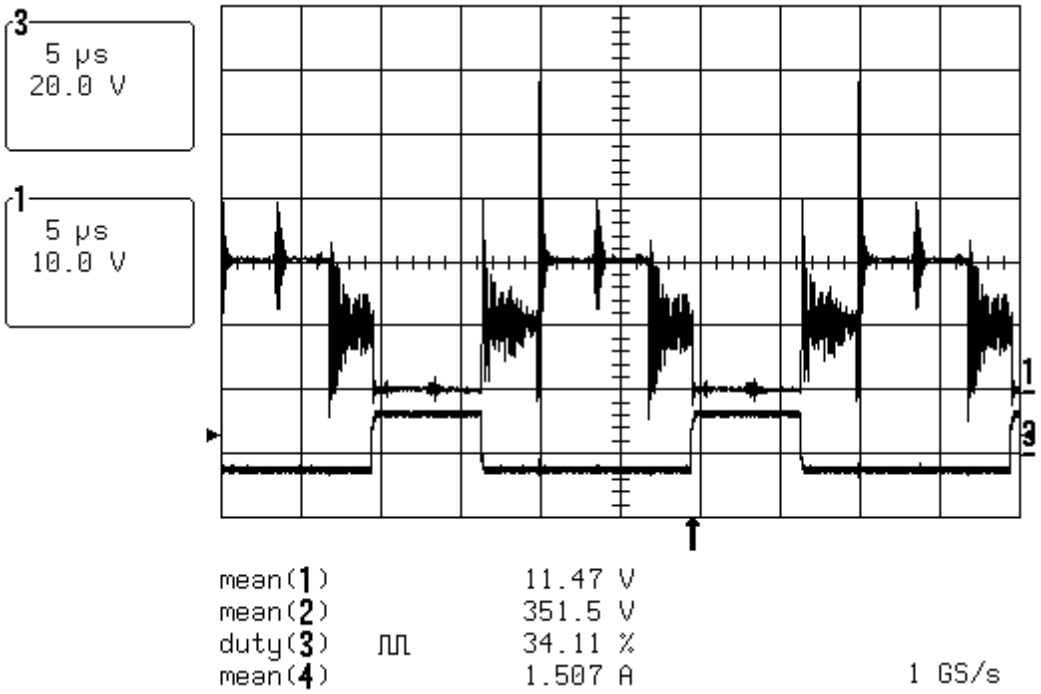

Figure 5-3. 34% duty cycle test, phase C bottom MOSFET voltage (Ch 1)

The phenomenon of switch voltage instability was seen only during tests with duty cycles close to 33.3%. It was not determined whether the shifting of the switch conduction intervals

came as a result of similar shifts in switch gate signals, or if gate signals remained unaffected and switching stage effects alone caused the discrepancies. The 33.3% duty cycle condition is a point of discontinuity between two and three conducting switches. When two opposite switch transitions are made in close proximity, voltage stresses are caused by forced changes in inductor currents within the transformer primary.

5.2. Voltage Transient Analysis

To gain more insight about the effects that caused the voltage spikes at the switch turn-off and at the opposite device turn-on transitions, interactions between switch timing and transformer leakage inductances (including circuit loop inductances) were analyzed in detail. Primary leakage currents oppose the commutation of magnetizing and load current to the transformer secondary side during switching transitions. Unlike magnetizing and load currents which freewheel through the rectifier stage following switch transitions, leakage currents are uncoupled and must be dissipated between the primary and switching stages. [3]

The formation of voltage spikes at the switch turn-off condition was first reviewed in detail. Figure 5-4 provides a simple illustration of the switching and transformer primary stages which is useful in conducting the analysis. Switches consisting of parallel MOSFETs are represented by single-pole-single-throw switches. In parallel with each switch is a capacitor and diode representing the output capacitance and anti-parallel diode of each MOSFET. The delta connected windings represent leakage inductances.

To begin the analysis, a typical set of switch states was assumed. Continuing with the analysis of the phase C bottom switch waveform, an interval was chosen in which switches B1 and C2 are conducting and all remaining switches are off. At the steady state condition during this interval, primary current from the source flows through B1 and out of point b toward the delta. This current is divided at the node shared by La and Lc. Two-thirds of the current flows through Lc and one-third flows through the series combination of La and Lb, assuming a balanced set of interconnections and transformers. The divided current sums back together at the node shared by Lb and Lc and flows into point c where it passes through C2 to return to the source. At the end of the interval, C2 is turned off. Inductor currents do not react immediately

to this transition and continue to flow out of point b and into point c. As the inductor current continues to flow into point c, it charges the output capacitance of C2 while discharging that of C1. If the leakage current is sufficient to fully discharge the C1 output capacitance, the anti-parallel diode of C1 should become forward biased, clamping the voltage at point c to the DC bus voltage. However, in some cases either the forward recovery time of the diode is not short enough or the switch output capacitances do not share the current equally. This allows the voltage at point c to rise above the bus voltage causing a spike. The energy stored in the output capacitances of switches C1 and C2 then oscillates back and forth between the leakage inductance as it is gradually damped by the resistance of the loop. This gives rise to the voltage ringing seen during the phase-leg dead-time.

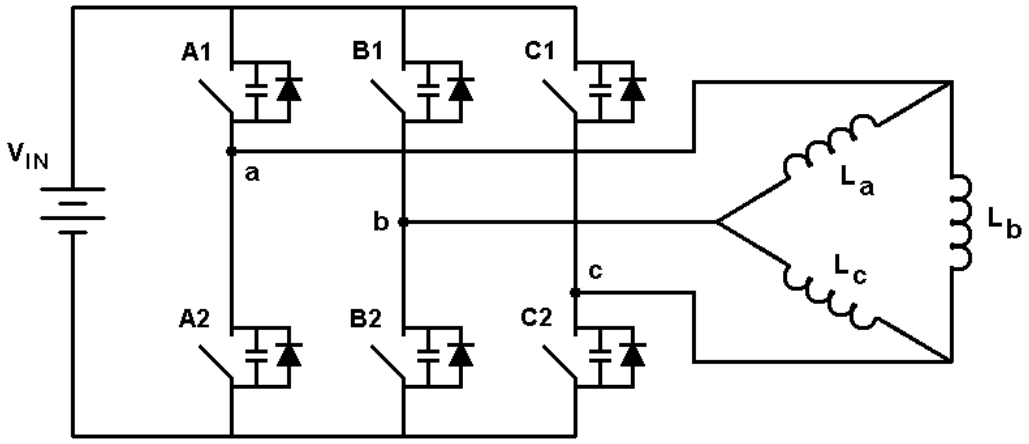

Figure 5-4. Switching stage and transformer primary model

The voltage spike seen across the bottom switch at the turn-on of the upper switch for duty cycles approaching 33.3% can also be explained by considering switch timing effects on the model of Figure 5-4. Switch gate waveforms were shown in Figure 2-2 for the 33.3% duty cycle. For a duty cycle slightly below 33.3%, switch transitions will not take place simultaneously. In this case, almost immediately after C2 has been turned off, A2 is turned on. A2 then conducts with B1. Source current flows out of point b and is divided in a two-to-one ratio between La and the series combination of Lb and Lc. The currents recombine at the node shared by La and Lb, flow into point a, and return to the source through A2. At the end of the interval, B1 turns off. The current, which is shared by the inductors, continues to flow out of

point b charging the output capacitance of B1 and discharging that of B2. This causes the potential at point b to fall rapidly toward zero. Depending on the magnitude of the current and whether or not the anti-parallel diode of B2 conducts, the voltage at point b can be driven below zero. Additional voltage and current interactions result between the switching stage and the delta connection. As the potential of point b becomes lower, the voltage polarity between points b and c would be reversed. While B1 was conducting, point b was held at bus voltage and point c was at half the bus voltage, assuming equal off-state resistances between switches C1 and C2 and a balanced delta. The polarity reversal would force against the current flowing through Lc. As a result, this current would increase in the opposite direction (decrease in the same direction). If point c was to remain at half the bus voltage, the polarity across Lb would remain the same, and its current would continue in the same direction. However, another conflict would exist in this case. If the current increased in the opposite direction through Lc while the current through Lb continued to flow, another current would need to enter the node shared by Lb and Lc. This current would be sourced through point c. In order to source such a current, the output capacitance of C2 would begin to discharge, forcing the voltage at point c toward zero and reducing the potential between points b and c. This result was seen during converter operation and is clearly visible in Figure 5-1. The effects resulting from the reduction of the voltage at point b after the turn-off of B1 do not all take place in discrete succession as described above. However these effects describe the conflicting forces that are obeyed simultaneously following the transition. The resulting decrease in voltage at point c reduces or eliminates all inductor voltages in the delta while point b is low. With the duty cycle slightly below 33.3%, C1 is turned on almost immediately after B1 is turned off. If the duty cycle is close enough to 33.3%, C1 will be turned on while the voltage at point c is still reduced from the condition resulting from the turn-off of B1. When C1 is turned on, its output capacitance is discharged through the switch. The potential at point c rises as source current begins to flow through C1; rapidly charging the output capacitance of C2. The current flowing through C1 also begins to flow out of point c toward the delta to charge the inductors. As the output capacitance of C2 becomes charged to the bus voltage, the current charging the capacitance will decrease. However, the rate at which it decreases cannot exceed the rate of current increase into the node shared by Lb and Lc. In this case, the current charging the output capacitance of C2 will continue to charge the output capacitance to a voltage greater than the bus voltage. This is assuming that the anti-parallel

diode of C1 does not clamp the voltage across C2 at the bus voltage. This condition produces the voltage spike across C2 which is seen at the turn-on of C1 for duty cycles approaching 33.3%.

Similar transient effects take place for duty cycles slightly above 33.3%. Although Figure 5-3 was captured for a test condition having a PWM duty cycle of 34.1%, a small phase shift error existed between the gate signals of C1 and C2. The error caused C1 to be turned on after B1 was turned off. This is indicated by both the rightward shift of the high state of C2 and by the low state immediately preceding it. However, when C1 is gated on just before B1 is gated off, a large voltage spike will still occur across C2. The effects that cause the spike are the same as those occurring for duty cycles slightly below 33.3%. In either case the transients associated with two switch transitions are shared. As duty cycles are moved away from the 33.3% value, transient effects become separated, and a reduction in the spike across C2 caused by the turn-on of C1 is seen. Figure 5-5 shows the resulting C2 MOSFET voltage waveform for an increased duty cycle of 36.1% for the same test conditions of Figure 5-3.

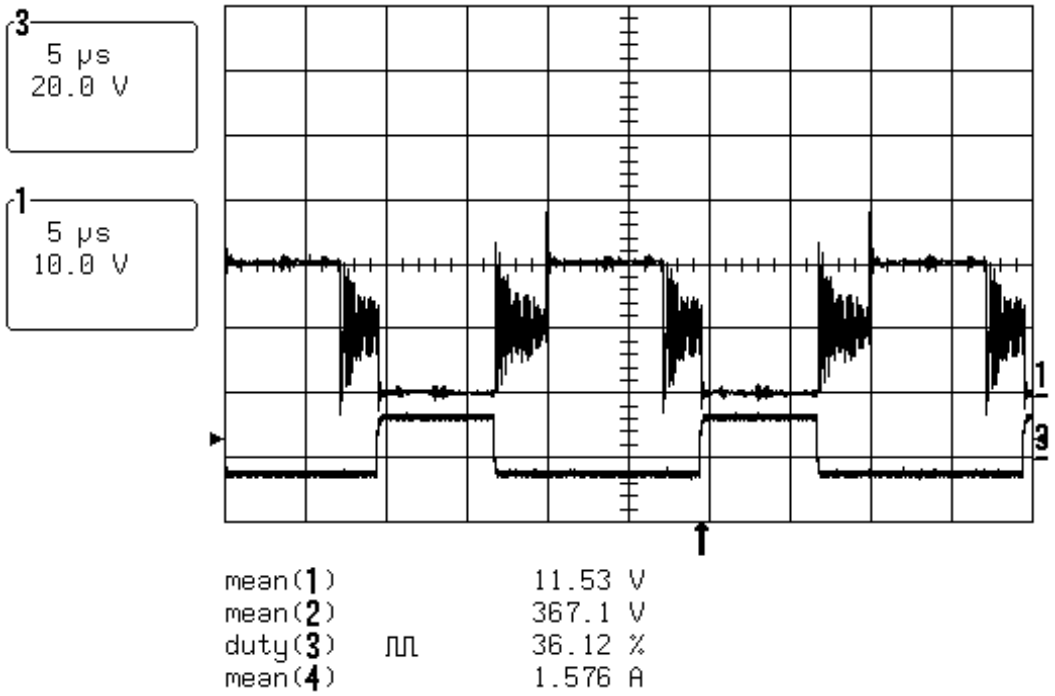

Figure 5-5. 36% duty cycle test, phase C bottom MOSFET voltage (Ch 1)

The transient analyses discussed, addressed the individual and shared effects of only three different switch transitions. The same principles that were used to determine voltage and current responses in these cases can be applied to the remaining nine switch transitions taking place over the rest of the switching period. The effects in the other cases are either identical or very similar to those discussed.

5.3. Testing Above 33.3% Duty

After analyzing the adverse effects on converter operation for duty cycles near 33.3%, testing was continued for increased duty cycles and loads. In these cases, high efficiencies were obtained. Table 5-2 lists converter parameters for subsequent tests at nominal 20V and 24V input voltages. The first two tests listed showed very high efficiencies. Although these figures are approximately correct, small scope channel offsets were taken into account for efficiency corrections in all following tests. Typically, corrected efficiencies differed by between one and two percent from the values calculated directly from instrument readings. The last two tests list corrected efficiencies for a 24V input and a lower duty cycle. Because the power level was increased, input voltage was raised to reduce voltage spikes resulting from higher input currents. As a compromise, duty cycle was lowered toward the discontinuity point. These tests ran stably and yielded favorable efficiency values.

Table 5-2. Increased duty cycle test results for the 60V switching stage

Duty	V_I	I_I	V_O	I_O	P_I	P_O	eff.
41.1%	19.9	35.9	401.9	1.72	714	691	96.9%
41.6%	19.9	53.4	399.3	2.56	1062	1024	96.4%
35.6%	23.7	83.2	415.2	4.49	1970	1863	94.6%*
35.6%	23.6	95.1	410.2	5.16	2242	2117	94.4%*

* Figures corrected for scope channel offsets

The second and fourth tests were each repeated for two minute runs. During this testing phase, thermal grease was not used at the switching stage board and heat sink interface.

However, as a result of high efficiencies, temperature rises did not exceed 20°C for either the switching or transformer stages without any forced air cooling. The corrected efficiency at the end of the 2.1kW test was 94.2%. The corresponding phase C bottom MOSFET voltage waveform for the test condition is shown in Figure 5-6.

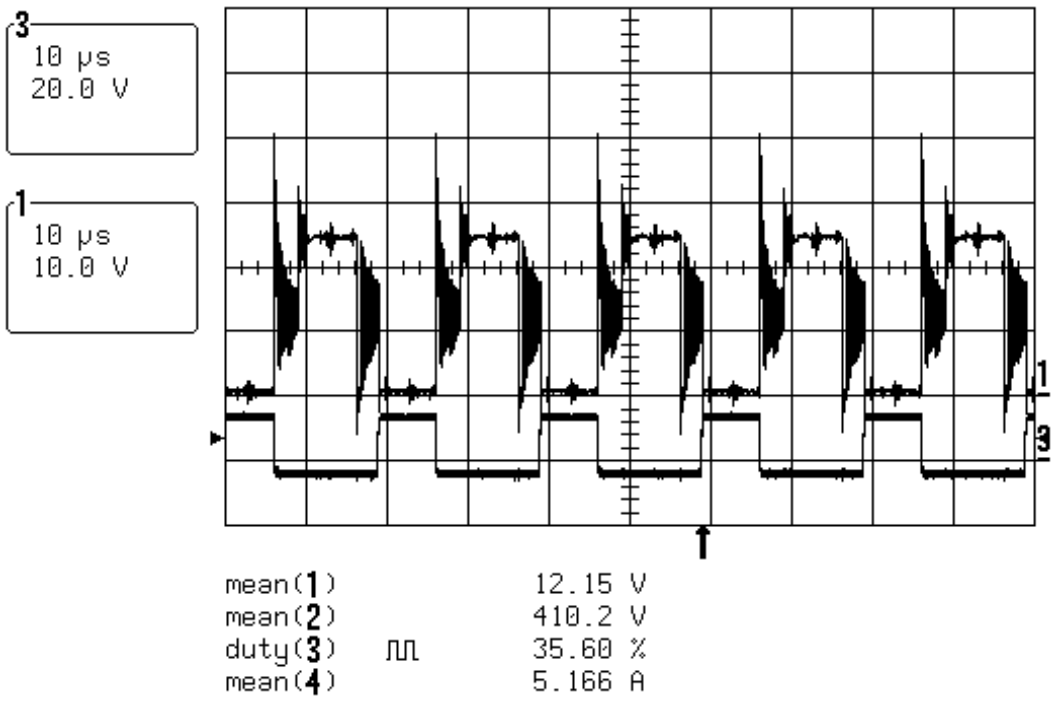

Figure 5-6. 2.1kW test, phase C bottom MOSFET voltage (Ch 1)

Transient voltage spikes reached 40V for the 2.1kW test. Although MOSFET snubbers were not included in the switching stage being tested, it was determined that they may not have been able provide enough voltage spike reduction for testing over the entire load range with the 60V rated MOSFETs. Instead, the focus was shifted toward an improved board design using the 75V MOSFETs.

5.4. *Improved Switching Stage Design*

Modifications were made to the existing switching stage board design to provide improvements for the final switching stage. The size of the board layout was reduced to accommodate four parallel MOSFETs instead of the six devices used in the original design. The shortened traces provided reductions in parasitic circuit inductance and trace resistance. This design required less board area and shortened the overall converter length. The modified board layout is shown in Figure 5-7.

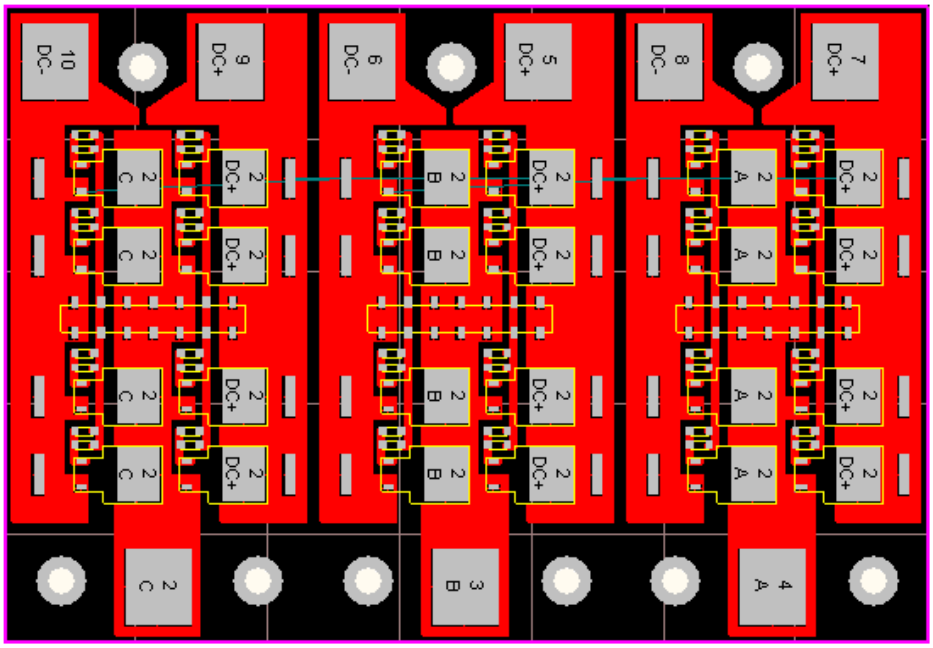

Figure 5-7. Modified switching stage layout design

A new IMS board structure was also selected. The thickness of the circuit layer was increased from 4oz/ft^2 (5.6mils) to 10oz/ft^2 (14mils). Thicker copper traces provided three main advantages. Most obviously, it provided a decrease in trace resistance to lower conduction losses. However, it also offered improved heat spreading for the surface mounted components. Finally, it gave more rigidity to surface mount threaded connectors under tension and torque conditions. The IMS dielectric layer was not changed, but the substrate layer was. Based on the circuit layer thickness chosen, a copper substrate was selected to provide uniform thermal

expansion between the circuit and base layers during board population and operation. This improved board flatness compared to the copper/aluminum structure previously used, allowing better board contact with the surface of the heat sink.

A new template fixture to position the board connectors was made for the new layout. The terminals were held in place by the fixture during the high temperature reflow process in the convection oven. Devices and gate resistors were then mounted using the convection reflow process with standard eutectic solder. Finally, bypass capacitors were mounted using the lower temperature soldering process.

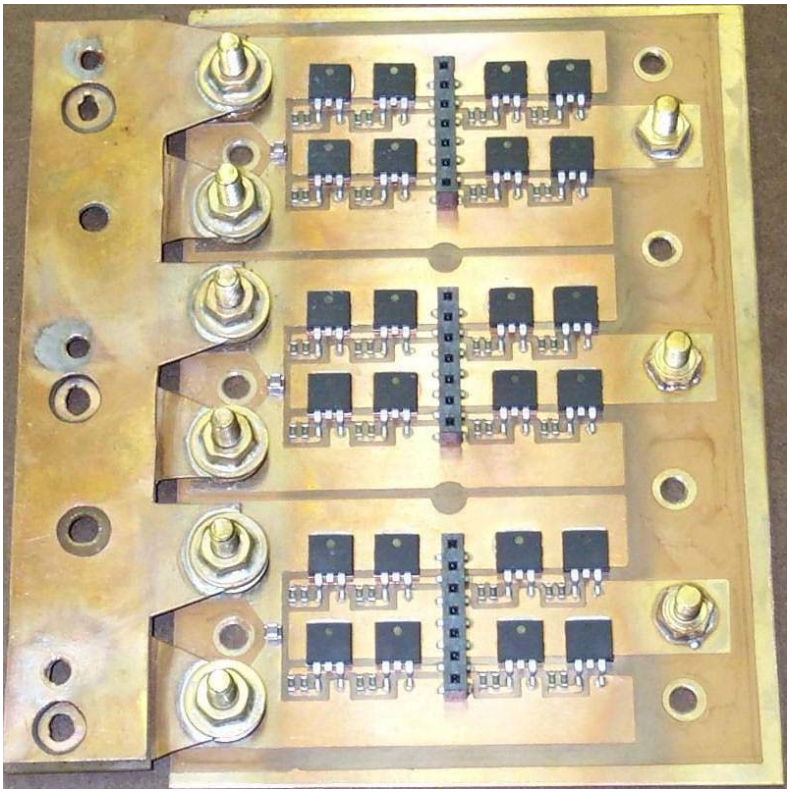

Figure 5-8. Improved switching stage and input bus

The input bus design was also modified. A new parallel plate bus similar to the one previously used was integrated into the switching stage. To reduce contact resistance especially for high input currents, the bus was solder bonded in addition to being mechanically fastened for support. However, this prevented the bus from being removed during switching stage repairs. For this reason, and to provide more input ripple current suppression, removable 6.8mF screw-

mount electrolytic capacitors were used to replace the 3.3mF through-hole mounted capacitors. The improved bus structure occupied less space on the edge of the board which further helped to reduce board size. Holes were placed between the capacitor mounting locations for fastening the power supply terminals. This reduced the average current path length to the terminals of each phase, while reducing stresses on individual board mounted terminals. Figure 5-8 shows the revised switching stage and input bus without input or bypass capacitors.

5.5. Final Testing

The initial tests with the new switching stage design were problematic. During the first low power test, MOSFET gate failures occurred on phase B. The failures were attributed to partially damaged device gates during the reflow process. However, a sporadic gate signal glitch was also suspected. The glitch was thought to exist when the constant PWM duty cycle value viewed on the scope changed drastically for one scope sample. Since no changes in the PWM waveform were seen, and the glitch could not be triggered on, the effect was later thought to be only a scope sampling error. The failed devices of the switching stage were individually replaced, while attempting to minimize the amount of overall board heating. The temperature of the board was raised with a hot-plate, while a soldering iron was used to elevate the temperature at the locations of the devices. However, during low power testing of the repaired switching stage, MOSFET gate failures occurred on phase C. Again, the effect was attributed to thermally compromised MOSFET gates.

All MOSFET devices were replaced using an improved short duration reflow process. A hot-plate was preheated to reflow temperature and the switching stage board was transferred to it. This allowed the board to quickly ramp up to reflow temperature and be removed from the heat source when reflowing was complete.

Testing was resumed with the revised switching stage. Improved results were obtained for power levels up to 2.5kW and are listed in Table 5-3. The first two data sets were collected from the converter prior to another switching stage failure at the gates of two MOSFETs on phase C. The failure occurred during a duty cycle adjustment. In addition, the two negative voltage regulators on phase C of the gate driver board failed along with a hex inverter chip on the

FIFO board as a result of the surge current drawn by the faulted gates. In this case, it was unlikely that the effects resulted from a partial damaging of devices during switching stage construction. Concerns were also raised about whether any of the past device gate faults were actually caused by thermally damaged gates. A close inspection of the gate driver and switching stage interface revealed another possible cause of the gate failures. It was seen that although the gate drive pins and the switching stage header lined up properly in the lateral direction, the spacing between the headers of phases B and C was about 20mils greater than that between the headers of phases A and B. The headers were unable to be accurately repositioned without the use of the terminal fixture which would require a reflow soldering process. Although the gate drive pins were able to be inserted into the headers, contact between the terminals was less optimal for shallow pin insertion depths. Unfortunately, the decreased width of the revised switching stage caused the gate drive board to sit above the output terminals to the transformer stage. The terminals were shortened as shown in Figure 5-8 to allow the gate drive board to sit low enough for its pins to plug into the switching stage headers. However, the pin insertion depth was shallower than in the previous design. It seemed likely that the gate drive assembly was moved enough during a duty cycle adjustment to cause changes in gate drive connections, thereby inducing the switching stage faults. For the later tests, the gate drive board was plugged into the switching stage as securely as possible, and the duty cycle was not changed during converter operation.

Table 5-3. Test results for the redesigned 75V switching stage

Duty	**V_I**	**I_I**	**V_O**	**I_O**	**P_I**	**P_O**	**eff.**
38.1%	20.0	17.5	394.5	0.812	351	320	91.4%*
40.1%	20.2	52.1	398.0	2.56	1054	1019	96.7%*
41.1%	20.3	52.9	407.3	2.48	1074	1011	94.1%
40.1%	21.7	87.5	415.2	4.25	1897	1764	93.0%
40.1%	21.6	102.0	410.2	5.15	2207	2114	95.8%
40.1%	21.6	130.7	399.7	6.69	2821	2673	94.8%

* Test points before gate driver failure.

Unlike the last two test results shown in Table 5-2, low input voltages were used for the tests listed in Table 5-3. Low input voltages allowed duty cycle values near 40% for more stable converter operation. The data shows corrected efficiencies for the tests, which were high considering the larger on-resistance of the 75V MOSFETs. The 1kW test was repeated for a two minute run in which converter efficiency was reduced by less than one-tenth of a percent and switching stage and transformer temperature rises were below 20°C. As with all previously calculated efficiencies, the values were approximate and showed some variations due to measurement error. Correcting the values for instrument offsets improved their accuracies especially for higher power levels. In higher power tests, voltages and currents were larger making fluctuations in instrument offsets comparatively less significant. The overall trend in converter efficiency was dramatically improved from previous tests conducted at high power levels.

Testing was halted at the 3kW load condition. Another series of device gate failures prevented continued testing beyond the last data point in Table 5-3. At the 3kW test point, multiple gate failures occurred on all three switching stage phases. The cause of the failures was believed to be related to either a gate signal glitch or a poor connection at the gate driver and switching stage interface. Because both the time and materials required to repair the switching stage in this phase of the project were unavailable, testing was stopped. Overall, the functionality of the switching stage design in conjunction with the transformer and output stages was proven successfully over a large portion of the converter operating range.

5.6. Conclusions and Future Work

The goals of this project were to design, build, and test, the front stage of a low cost, highly efficient, PWM controlled, 5kW DC-DC converter. A hybrid three-phase converter topology offering benefits in component size reduction, voltage boost ratio, and reduced output ripple was selected. The system functionality was characterized and simulated to show favorable results. During this analysis, it was determined that the converter voltage boost ratio was greater than initially predicted over a range of high duty cycles. However, two points of discontinuity were found in the operating region of the boost profile. The effects of the 33.3% duty cycle

discontinuity point were seen to compromise converter operation during the testing phase. Simultaneous transient effects caused instability between the switching and transformer stages. These effects were determined to be potentially harmful to the switching stage devices and were therefore avoided in further tests.

A detailed switching stage design process followed the topology characterization. Circuit configurations were strongly considered for adequate thermal dissipation in conjunction with low circuit inductance and available device ratings and associated packages. A superior low cost device offered in the surface mount TO-263 package was selected along with an IMS board structure. The switching stages were able to be constructed and modified in-house during the prototyping phase, and performed well both thermally and electrically during testing. However, for future board revisions and testing, more precise switching stage manufacturing procedures such as solder reflowing and accurate terminal placement would enhance overall switching stage performance and reliability. Making repairs to the discrete design was also more difficult and time consuming with the IMS material, due to its large heat capacity. Component replacements required either a reflow process or an increase in overall board temperature in addition to localized heating. These procedures required bypass capacitors, having lower temperature ratings, to be removed and replaced in separate heating processes before and after modifications were made at the device level.

Overall, the transformer stage performed well considering its implementation. Planar transformers were the best choice for close transformer matching and reduced parasitic elements. However, it was difficult to ensure that external connections among the transformers and between the switching stage did not contribute to any small imbalances. Although the converter boost ratio was enhanced by the transformer topology, the delta configuration of the primary allowed currents to circulate within the loop for switch timing imbalances. At lower power levels, the adverse effects were less severe and as a result, converter performance was closer to ideal. In future development of this converter topology, steps should be taken to provide matched interconnections between the transformers and the switching stage. Also, a more thorough investigation of the magnitudes of circulating currents within the delta should be undertaken if the topology is to be used in high power applications.

The interactions between input currents and parasitic inductances in the transformer and switching stages, as well as those of their interconnections, were determined to be the major

causes of large switch voltage transients. Snubbers were proven to reduce transient ringing, but were less effective in reducing peak switch voltage stresses. The criteria of low system cost and system integration were conflicting. The design of the system stages using discrete components achieved low system costs but undesirably increased the parasitic inductances of the system. However, the considerations made during the design phase allowed the converter to perform well over a large range of input current.

Gate signals and associated timing for the switching stage were generated using a DSP during converter evaluation. This approach was used to provide a configurable interface for any system adjustments needed during prototyping and testing. The off-the-shelf hardware used during the tests was more costly than alternative controller chips which would likely be used in final system implementation. The DSP and FIFO clock frequencies also introduced small errors in PWM and phase shift signals which became compounded by the FIFO circuit. In future testing, phase shifting PWM controller gate signal generators should be developed to provide accurate switch gating.

The converter was successfully tested for power levels above half of its full power design specification. These tests were conducted over maximum switching stage stress conditions having low input voltage and high input current. Despite the increased switching stage conduction losses for these conditions, efficiency values obtained for the tests were consistently near 95%. In addition, the thermal transients of the system remained well within an acceptable range. The single output stage configuration of the three-phase topology, which was not implemented in this design, would likely exceed the efficiency values obtained for the split output configuration. A single six-pulse rectifier could offer reductions in diode voltage drop which would lead to increased converter efficiencies.

The three-phase DC-DC converter provides unique benefits over other conventional isolated boost topologies. The work conducted on this project led to a better understanding of topology functionality as well as the identification of unique factors affecting converter performance in the selected implementation. The two most significant findings of this study are:

- Boost ratio characterization over the 0% to 50% duty cycle range for a delta-wye connected transformer stage
- Identification and analysis of converter instability at the 33.3% boost ratio discontinuity point

Many of the obstacles encountered during the design and testing phases were related more to complications resulting from conflicting design goals than to topology idiosyncrasies. The discrete implementation of the system was challenging yet ultimately successful. However, the overall outcome suggested that an integrated system design may provide more favorable results.

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Vita

Damian Patrick Urciuoli was born in Pompton Plains, New Jersey on February 28, 1979. He enrolled as an engineering student at Virginia Tech in August 1997.

In the summer of 1999 he began work as a coop student with the Naval Surface Warfare Center (NSWC) Power Distribution Systems Branch in Philadelphia, Pennsylvania. Here he helped test and evaluate an intelligent fault detection system designed for flight 2A destroyers. In the spring and summer of 2000 and 2001, he continued work with the NSWC Electric Machinery Systems Branch. Here he served as a member of a superconducting homopolar motor test project team. His responsibilities included the assembly and disassembly of the motor, the configuration and management of the motor data acquisition system, as well as data reduction and the analysis of motor performance.

He received his bachelors degree in Electrical Engineering from Virginia Tech in May 2002. In August 2002 he returned to Virginia Tech to complete his five year bachelors/masters degree program. During this time he worked as a graduate research student under Dr. Jason Lai in the Center for Power Electronics Systems Laboratory and the Future Energy Electronics Laboratory.