3.1 Transmitter

The transmitter supports the uplink of the W-CDMA system. It provides a digital interface for the baseband processor. The baseband processor sends the spread baseband signal through the digital interface to the transmitter. The transmitter modulates the baseband signals on a radio frequency (RF) carrier. The modulated RF signal is then amplified, filtered and transmitted to the base station through the air link. To combat the near-far problem, the transmitter operates in conjunction with a transmit power control (TPC) to maintain the transmit power at an appropriate level. The control determines the power level based on the digital command from the baseband processor. Figure 10 is a block diagram of the transmitter.

3.1.1 Block Diagram

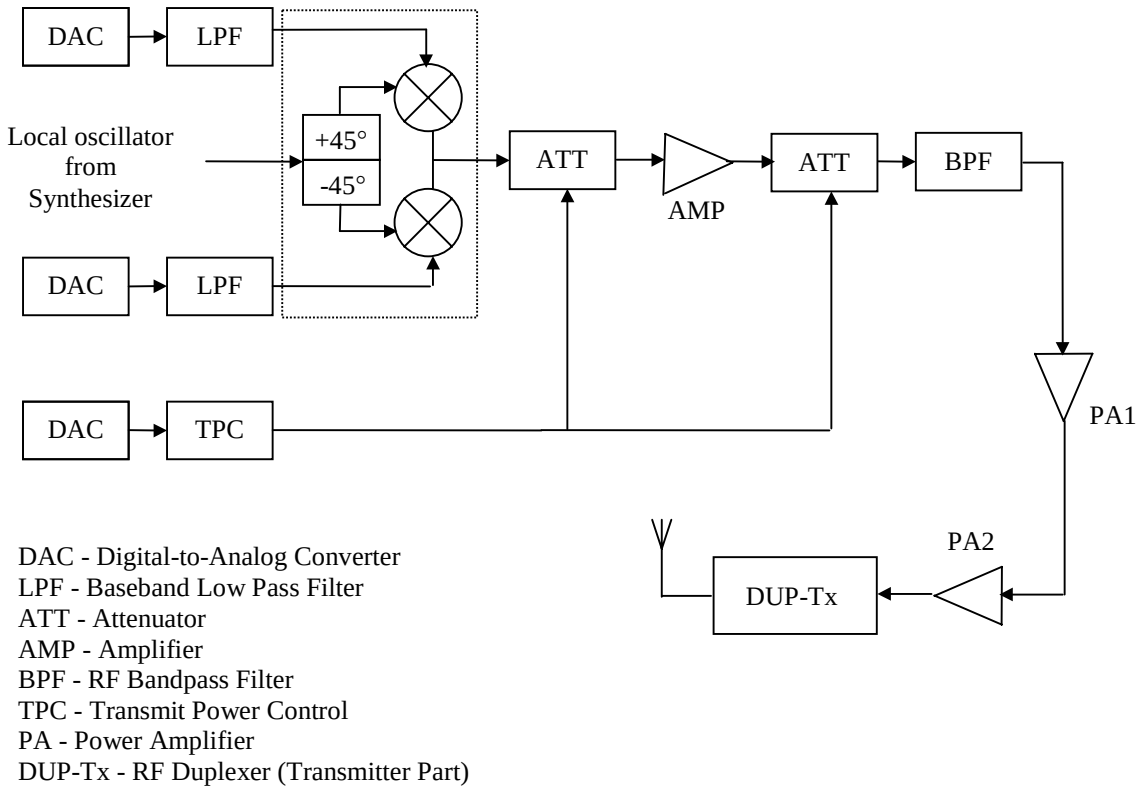

Figure 10. Transmitter block diagram.

3.1.2 Technical Specifications

The key specification for the transmitter is to deliver transmit power at 1.6 W +20%, -50% over the transmitting band (1920 – 1980 MHz). A digital command from the baseband processor can control the transmit power over a 70dB range. The digital command is 7-bits long. The command code is a binary number between 0000000B and 1000110B (or 0 to 70 decimal). The code 0000000B produces the maximum power output, while the code 1000110B produces 70dB less than the maximum output. The power control cycle time is 0.625ms.

The data rate is 128Kbps. The data sequence is spread with the spreading codes at 4.096Mcps chip rate. The modulation type is QPSK. The baseband processor sends the direct (I) and quadrature (Q) baseband signals to the transmitter in two separate channels. The baseband processor samples the baseband signals at 32.768Msps. The sample rate is eight times the chip rate. The signals are sent in 8-bit digital format. The transmitter digital-to-analog converters (DAC) reconstruct the analog signals and these signals are filtered by 0.22 roll-off, square root raised cosine (RRC) filter. The resulting analog signals are applied to the transmitter modulator.

As mentioned in Section 2.6 of the system overview, the zero guard bands between adjacent channels of the W-CDMA systems imposes a stringent requirement on the adjacent channel power. The adjacent channel power is measured with modulated signals. The adjacent channel power of the output spectrum is 40dBc less than the inband output power. The inband power is the total power in a 4.096MHz bandwidth about the carrier frequency. The adjacent channel power is the total power in the 4.096MHz bandwidth about the frequency that is ±5MHz away from the carrier frequency. The next adjacent channel power is the total power in the 4.096MHz bandwidth about the frequency that is ±10MHz away from the carrier frequency. The next adjacent channel power is 60dBc less than the inband power.

The spurious and intermodulation emission is measured with a continuous wave (CW). The emission should be 60dBc less than the CW carrier.

The full specifications of the transmitter are listed in Appendix A.

3.1.3 Design Approach and Analysis

3.1.3.1 Peak-to-Average Factor

As mentioned the system overview, a QPSK signal after pulse shaping will lose its constant envelope property. Non-linear power amplification of a non-constant envelope signal causes spectral regrowth. Understanding the peak-to-average factor of the QPSK signal is important in selecting the power amplifiers to avoid non-linear amplification.

A simulation was performed to find the peak-to-average factor based on the model shown in Figure 11.

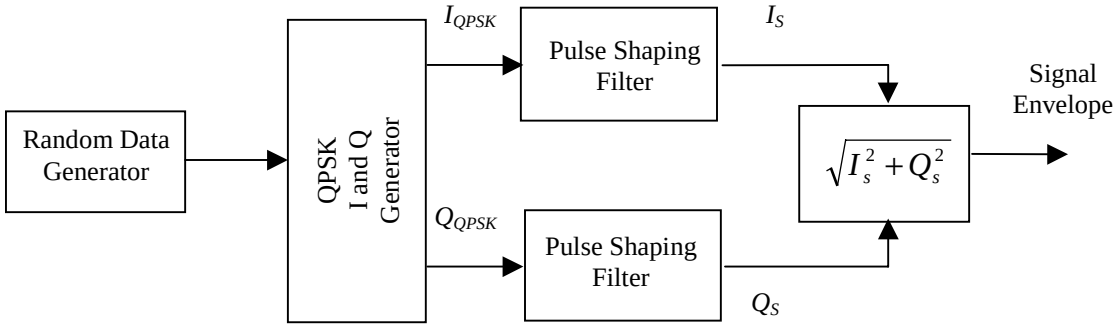

Figure 11. Simulation model for QPSK peak-to-average factor.

The model in Figure 11 is hypothetical. It does not include the W-CDMA spreading process but a random data generator was used to approximate the PN sequence. The QPSK modulation scheme is defined in Table 3 [12].

Table 3. The QPSK modulation scheme.

Two Consecutive Bits	Signal Phase
00	225°
01	135°
10	315°
11	45°

The pulse shaping filters are 0.22 roll-off, square root raised cosine filters. The filter outputs are used to evaluate the signal envelope. The model is based on the complex baseband envelope which avoids the necessity of simulating the high frequency carrier.

QPSK

QPSK is a bandwidth efficient modulation scheme. As compared to the BPSK modulation scheme, QPSK gives the same BER performance but carries twice the data rate in the same bandwidth. The implementation of modulation and demodulation is simple, and, therefore, QPSK is very attractive for use in wireless communications.

The phase of a QPSK signal can take one of four possible values. The four values are equally spaced. They are practically chosen to be 45°, 135°, 225° and 315°. The QPSK can be mathematically represented by [13]

$$S_{QPSK}(t) = A \cdot \cos\left[2\pi f_c \cdot t + \theta_i(t)\right] \qquad (3.1.1)$$

where

$0 \le t \le T_s$: T_s is the symbol duration.

$i = 1, 2, 3, 4.$

$\theta_1 = \frac{\pi}{4}, \quad \theta_2 = \frac{3\pi}{4}, \quad \theta_3 = \frac{5\pi}{4}, \quad \theta_4 = \frac{7\pi}{4}.$

A : signal amplitude.

f_c : carrier frequency.

For a symbol interval, (3.1.1) can be written as

$$S_{QPSK}(t) = A \cdot \cos[\theta_i(t)] \cdot \cos(2\pi f_c \cdot t) - A \cdot \sin[\theta_i(t)] \cdot \sin(2\pi f_c \cdot t) \quad (3.1.2)$$

The direct (I) and quadrature (Q) components of the signal are defined as

$$I_{QPSK}(t) = A \cdot \cos[\theta_i(t)] \quad (3.1.3)$$

$$Q_{QPSK}(t) = A \cdot \sin[\theta_i(t)] \quad (3.1.4)$$

The I and Q components are baseband signals that ease the simulation.

Square Root Raised Cosine Filter

The pulse shaping filter is a square root raised cosine filter. The pulse shaping reduces the intersymbol effects and the spectral bandwidth of baseband signals. The roll-factor of the filter is 0.22. The transfer function of the filter in frequency domain is given by [14]

$$H_{RRC}(f) = \begin{cases} 1 & 0 \le |f| \le \dfrac{1-\alpha}{2T_s} \\ \sqrt{\dfrac{1}{2}\left\{1+\cos\left[\dfrac{\pi T_s}{\alpha}\left(|f| - \dfrac{1-\alpha}{2T_s}\right)\right]\right\}} & \dfrac{1-\alpha}{2T_s} < |f| \le \dfrac{1+\alpha}{2T_s} \\ 0 & |f| > \dfrac{1+\alpha}{2T_s} \end{cases} \quad (3.1.5)$$

where

α : is the roll-off factor.

Figure 12 illustrates the ideal spectral characteristic of the square root raised cosine filter with a 0.22 roll-off factor. The x-axis is normalized to the symbol rate. As shown in the figure, the filter response is absolute zero after $0.61/T_s$.

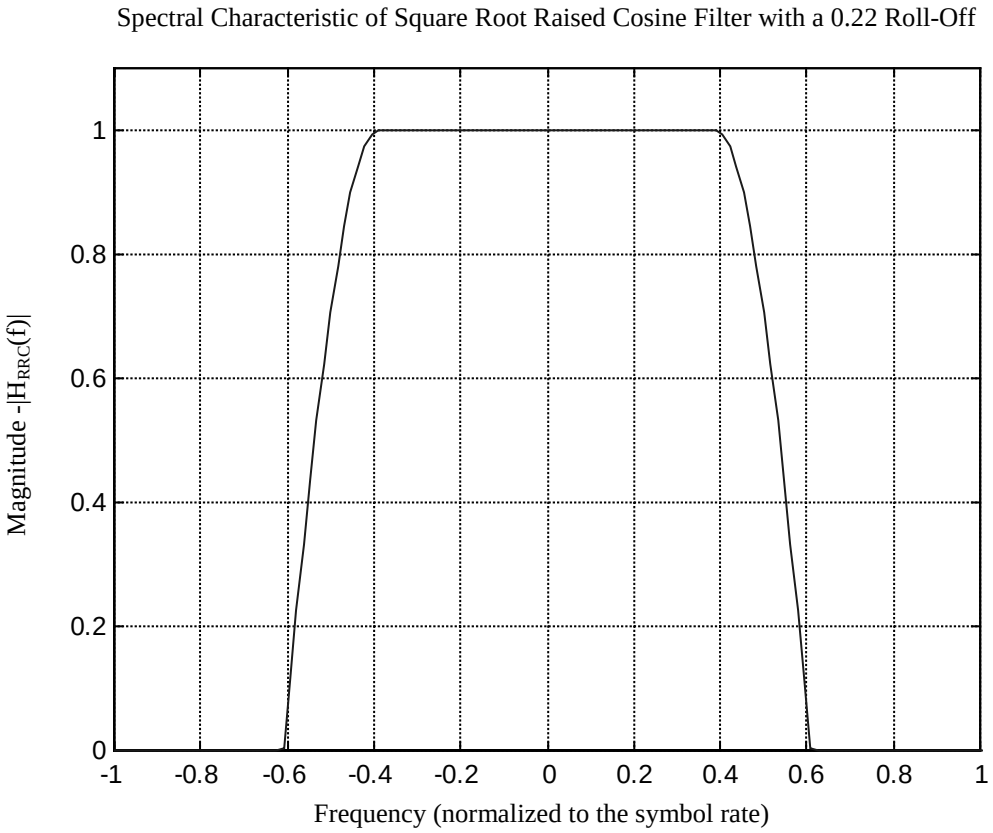

Figure 12. Spectral Characteristic of square root raised cosine filter with a 0.22 roll-off.

The number of points used to sample the spectrum is 1024. An Inverse Fourier transform (IFT) is used to obtain the time-domain impulse response of the filter. However, the resulting filter is non-causal. The impulse response is an infinite time waveform about the time zero. This impulse response cannot be implemented practically. Thus, the impulse response is delayed by four symbol intervals. The first eight symbol intervals are considered and the rest are truncated. Figure 13 shows the delayed and truncated impulse response of the filter.

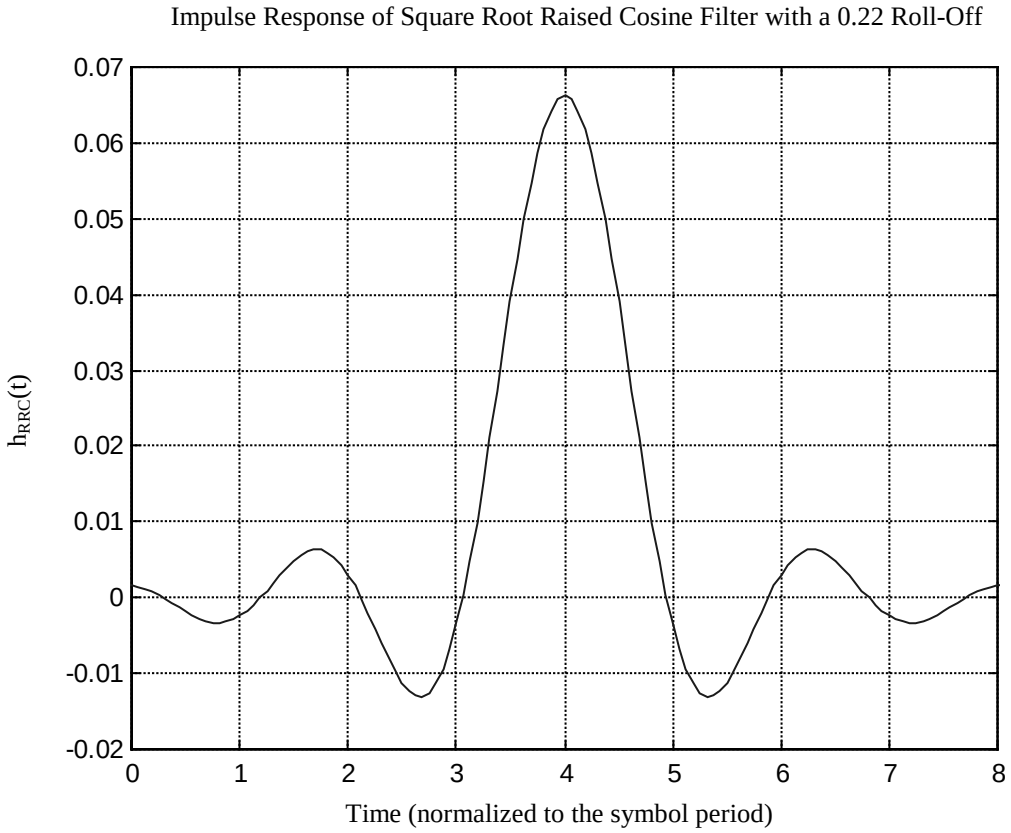

Figure 13. Delayed and truncated impulse response of the square root raised cosine filter with a 0.22 roll-off.

Pulse Shaped I and Q signals

Pulse shaping is done by passing the I and Q signals through the filters individually. Mathematically, it is equivalent to convolve the signals with the impulse response.

$$I_s(t) = I_{QPSK}(t) \otimes h_{RRC}(t) \tag{3.1.6}$$

$$Q_s(t) = Q_{QPSK}(t) \otimes h_{RRC}(t) \tag{3.1.7}$$

Simulation

A simulation was used to generate 512 bits of random data. Two bits form a QPSK symbol. The QPSK symbols generate the I and Q symbols. Each symbol is sampled for 16 samples. Convolution is performed on the I and Q sampled sequences with the filter impulse response. Figure 14 shows a 50-sample segment of the I and Q signals before and after pulse shaping.

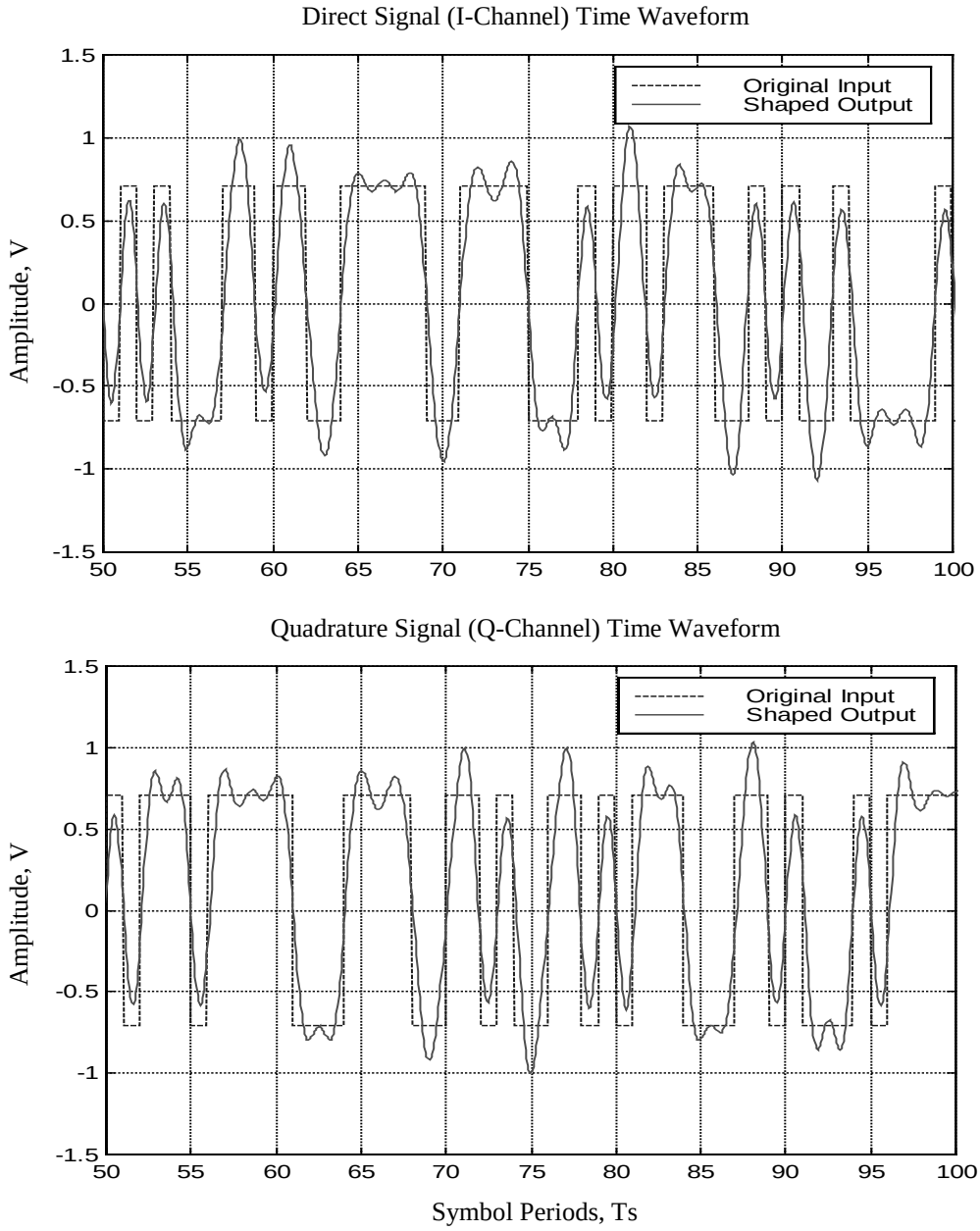

Figure 14. A 50-sample segment of the I and Q signals before and after shaping.

The complex envelope of the pulse shaped QPSK signals for the 50-sample segment is shown in Figure 15.

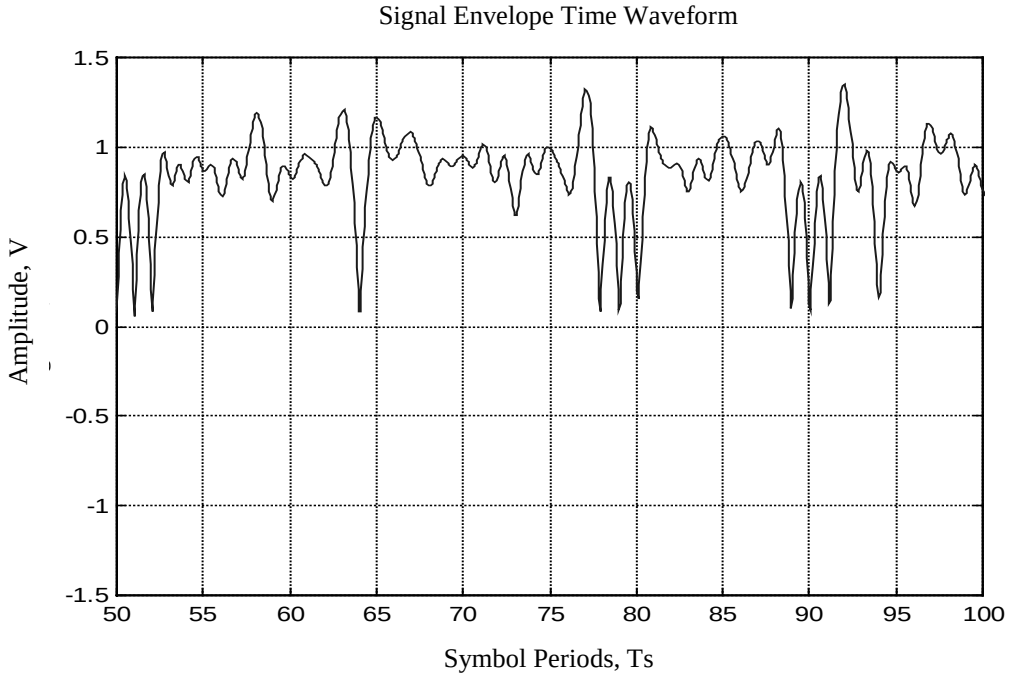

Figure 15. The shaped signal envelope of the 50-sample segment.

Referring to the Figure 14, the original I and Q signals are digital waveforms and the amplitude is -0.707V or 0.707V. This results in unity envelope amplitude. Figure 15 shows that the envelope of the shaped signal is no longer constant. The peak-to-average factor can be found from the simulated samples of the signal envelope waveform by (3.1.8).

$$F_{pk/avg} = \frac{\max(\sqrt{I_s^2(k) + Q_s^2(k)})}{\frac{1}{N} \cdot \sum_{k=1}^{N} \sqrt{I_s^2(k) + Q_s^2(k)}} \qquad (3.1.8)$$

where

N : total number of samples

k : sample index from 1 to N

Evaluating (3.1.8) results in a peak-to-average factor of approximately 4.6dB.

3.1.3.2 Power Amplifier Requirement

According to the specifications, the average output power of the transmitter should be 1.6W within a tolerance of -50% to +20% at the antenna port. The stringent adjacent channel power requirement and the non-constant envelope QPSK signal prevent the use of high-efficiency non-linear amplifiers. However, the use of linear power amplifiers for high output power results in much higher power drain and implementation cost. To compromise the shortcomings of linear amplification, we set the target output power of the transmitter at 1W or 30dBm.

As shown in the block diagram in Section 3.1, there is a duplexer filter before the power is delivered to the antenna. The insertion loss imposed by the filter is unavoidable. This insertion is estimated to be 1.5dB. Thus, the power amplifier has to deliver 31.5dBm average power. The power amplifier should not introduce non-linear distortion at the peak of the QPSK signal that has a 4.6dB peak-to-average factor. Thus, the power handling capability of the amplifier should be 36dBm or more. Power amplification of the modulator output level to 30dBm is difficult to achieve in one stage. Two-stage power amplifiers were used.

3.1.3.3 Receiver Desensing

The power amplification not only boosts the power level of the desired transmit signal but also raises the noise floor of the spectrum. The rise of the spectrum noise floor can include the receiving band (2110-2170MHz) which is 190MHz higher than the transmitting band. However, the transmitter and the receiver share an antenna through the duplexer. The duplexer is a three-port filter. The three ports accommodate the transmitter, the receiver and the antenna simultaneously. The use of the duplexer saves an antenna. On the other hand, it introduces a physical path between the transmitter and the receiver. If the power in the receiving band due to the transmitter is not properly suppressed, turning on the transmitter will degrade the receiver sensitivity. This phenomena is called receiver desensing.

A power budget study is done to ensure no receiver desense. Figure 16 depicts the specified transmit power spectrum.

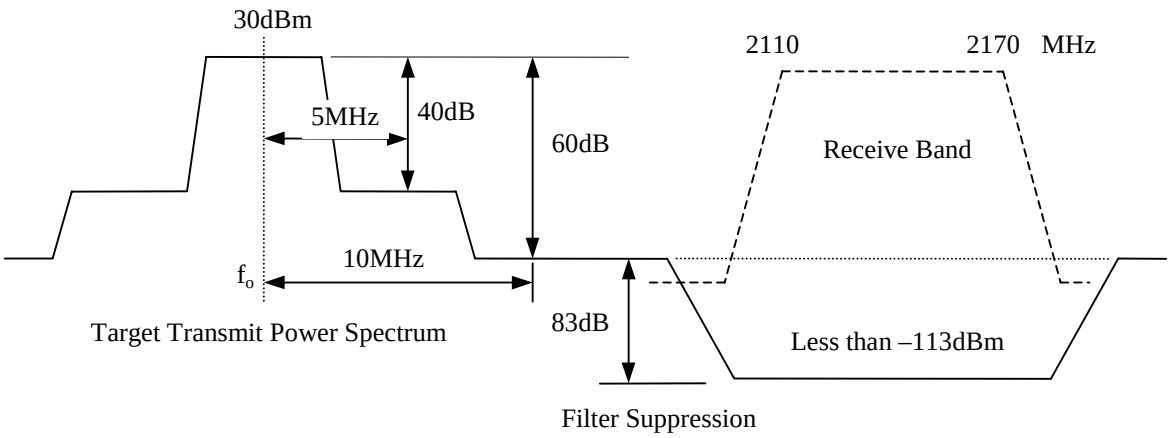

Figure 16. The specified transmit power spectrum.

The transmit power spectrum specifies for a 30dBm transmit carrier. The adjacent channel power and out-band suppressions are 40dBc and 60dBc respectively. The transmit power spectrum has 60dB suppression in the receiving band. The noise floor in the receiving band due to the transmitter is –30dBm (i.e. 30dBm – 60dB). This noise floor is much greater than the specified –113dBm receiver sensitivity. The transmitter can cause serious receiver desense.

Filtering the transmit power spectrum is necessary to drive down the noise floor in the receiving band by 83dB or more. The duplexer and the RF bandpass filter (BPF) in the transmitter are the devices used to provide the suppression. They will be discussed in the circuit level design section.

3.1.3.4 Transmit Power Control (TPC)

The transmitter should provide 70dB transmit power control range. Specifying the target output power as 30dBm, the range of the transmit output power is from –40dBm to 30dBm. In order to achieve the power control, RF attenuators are used to adjust the power amplifier drive level. It is difficult to use one attenuator to provide the 70dB control range. The board feed-through can limit the maximum isolation between two nodes on the printed circuit board. If the intended attenuation of an attenuator is greater than the board feed-through, the attenuation becomes board limited rather than device limited. The attenuation of the attenuator beyond the board limit becomes unpredictable. Two attenuators were employed in the transmitter chain to ensure that the attenuation is device limited.

3.1.4 Circuit Level Design

Following the flow of the signal as shown in the block diagram in Section 3.1.1, the discussion of this section proceeds from the digital interface to the duplexer. Detailed schematics are in Appendices C-1 and C-2. The discussion of the circuits refers to the schematics for the component designators. The hardware implementation of the transmitter comprises five assemblies. They are the digital-to-analog board, the modulator board, the power control, the power amplifier and the duplexer. Each assembly is discussed in following sub-section.

3.1.4.1 Digital-to-Analog Conversion (DAC) Board

The DAC board provides the interface between the baseband processor and the transmitter. It accepts the I and Q baseband signals in 8-bit digital format from the baseband processor and outputs the I and Q signals in analog form to the modulator. Figure 17 is the DAC block diagram. The full schematic is in Appendix C-1.

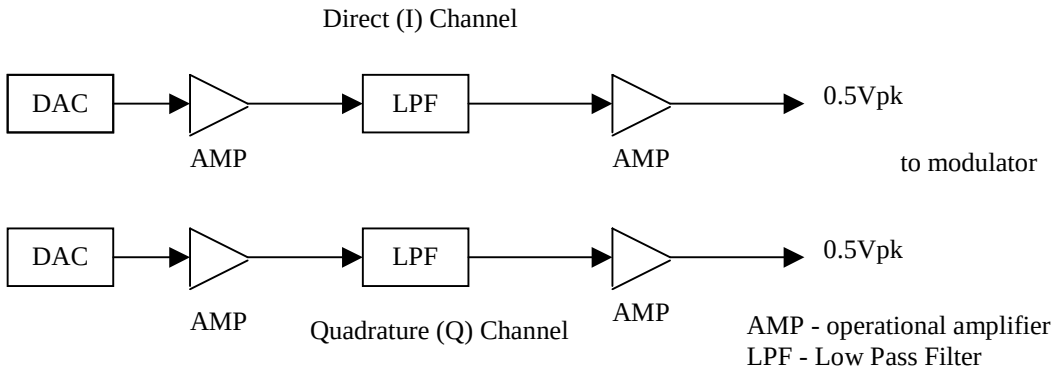

Figure 17. Block diagram of the DAC board.

AD9708 DAC

The AD9708 is a 8-bit digital-to-analog converter from Analog Devices. There are two AD9708's (Appendix C-1: U1, U3) on the board. Each device corresponds to one (I or Q) baseband channel. They convert the digital baseband signals from the baseband processor to analog signals. The devices are capable of 100Msps but actually operate at 32.765Msps. The devices are set for a full range differential output at 0.5V peak.

AD8072 Operational Amplifier

The outputs of the DACs are connected to the Analog Devices AD8075 operational amplifiers. There are two AD8075's (Appendix C-1: U2, U4) on the board. Each device corresponds to one baseband channel. Each AD8075 package contains two operational amplifiers. One of the amplifiers buffers the DAC from the baseband low pass filter (LPF) and provides a voltage gain of two. The other amplifier buffers the LPF output from the modulator. The voltage gain of this amplifier is adjusted so that the full-scale output to the modulator is 0.5V peak.

Baseband Low Pass Filter

The baseband low pass filters are from Soshin. They are 0.22 roll-off square root raised cosine filters. There are two filters (Appendix C-1: F1, F2) on the board. Each filter corresponds to one baseband channel. They are pulse shaping and anti-aliasing filters. Pulse shaping is performed to limit the baseband signal bandwidth. The DAC outputs are composed of the baseband spectrum and the replicas of the baseband spectrum at every integer multiple of the 32.768MHz sampling frequency. The filters remove all the replicas to prevent aliasing. The measured frequency response of the filter is shown in Figure 18.

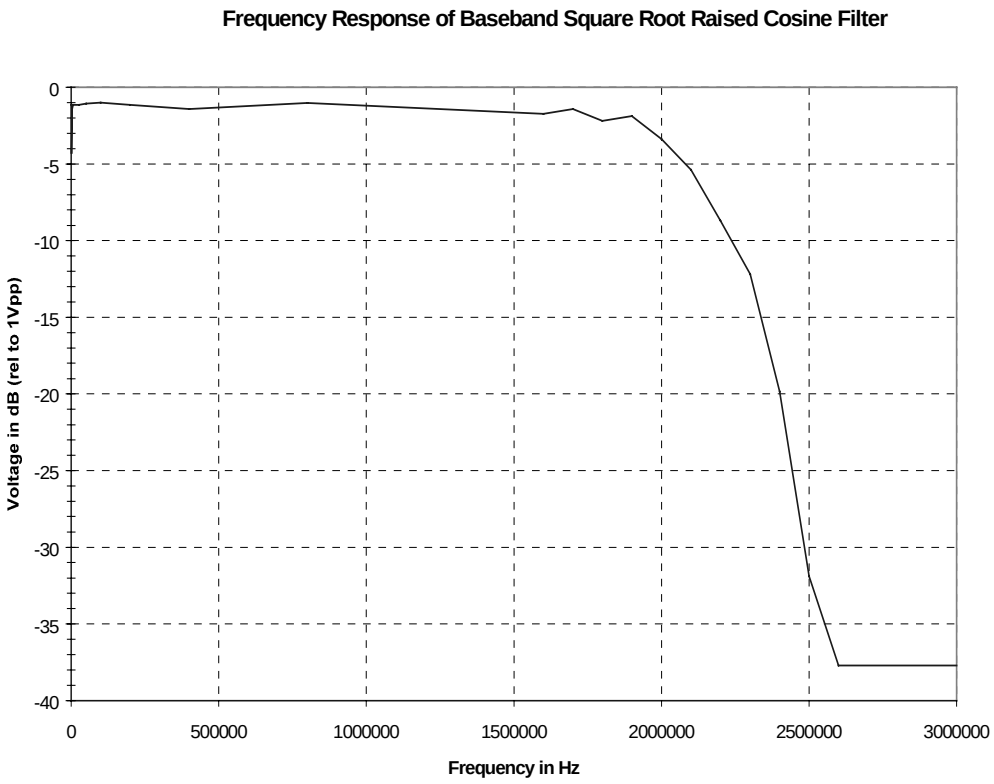

Figure 18. Frequency response of the Soshin baseband low pass filter.

The filter starts to roll-off at 1.6MHz and the absolute cut-off is at 2.6MHz. Comparing the theoretical response of the filter given in Figure 12 of Section 3.1.3.1 that the actual roll-off starts at 1.64MHz and the absolute cut-off is 2.46MHz. There are small

differences between the theoretical values and the measured values. These are the measurement errors. The measurement error at the absolute cut-off is larger because the signal to be measured at the absolute cut-off is small. The measurement accuracy is more vulnerable to the noise influence in the system.

3.1.4.2 Modulator Board

The modulator board performs the modulation and power control functions. Figure 19 is the block diagram. The full schematic is in Appendix C-2.

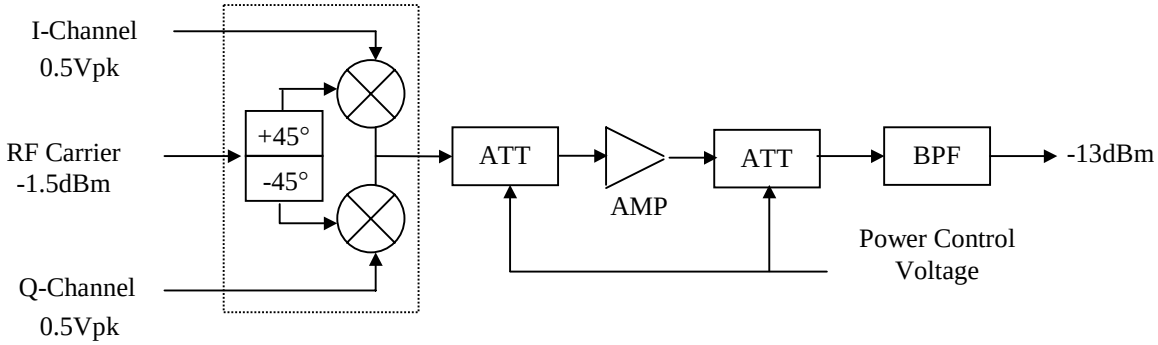

Figure 19. Block diagram of the modulator board.

RF2422 Modulator

The modulator chip (Appendix C-2: U4) is a RFMD RF2422. It modulates the baseband signals on the RF carrier (1.92GHz – 1.98GHz). The RF carrier level is set at –1.5dBm, while the both I and Q baseband signal levels are set at 0.5V peak. This baseband input was set to maintain low adjacent channel power. The modulated output has 50dB adjacent channel power suppression that gives 10dB margin for the subsequent power amplifier with respect to the –40dBc specification.

AT-108 Attenuator

There are two M/A COM AT-108 attenuators on the modulator board. One (Appendix C-2: U2) is at the modulator output and the other (Appendix C-2: U1) is at the output of an amplifier. The attenuator has 40dB attenuation range but the design makes use of a 35dB range to meet the 70dB control range requirement. The attenuation is determined by a control voltage from the transmit power control. The control voltage can run between 0 to 5V. A 5V voltage gives a minimum attenuation of 3.5dB which is the insertion loss of the attenuator. As the voltage decreases, the attenuation increases till the total attenuation is 43.5dB (the 40dB attenuation plus the 3.5dB insertion loss). For the 35dB attenuation range, the minimum control voltage is set at approximately 0.5V.

Amplifier

A Mini-Circuits ERA-5 monolithic amplifier (Appendix C-2: U3) is used as a gain block to compensate for the miscellaneous losses in the circuit, such as the insertion losses of the attenuator and the filter. The gain of this amplifier is 20dB. This amplifier has 50Ω standard input and output ports. It is easy to use and stable. The bias circuit is simple as shown in Figure 20 [15].

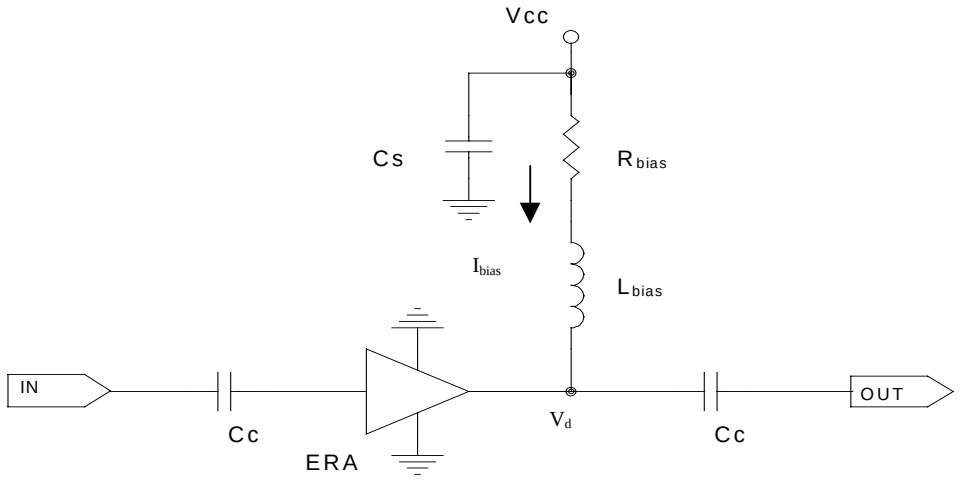

Figure 20. Bias Configuration for ERA amplifiers.

The RF choke should be chosen such that its reactance is at least 500Ω. Based on this criterion, a 39nH choke is used.

The ERA-amplifiers are biased with a supply voltage (V_{cc}) higher than the device voltage (V_d) for stable performance. The higher supply voltage allows larger bias resistances (R_{bias}) and hence the variation of the bias conditions against temperature is reduced [15]. However, a large voltage difference is not favorable to the use of chip resistors because more voltage difference causes more power dissipation in the bias resistor. To allow the use of chip resistors, the 6V supply is chosen. The bias resistance is calculated (3.1.9) based on the bias parameters of the amplifiers from the data sheets.

$$R_{bias} = \frac{(V_{cc} - V_d)}{I_{bias}} \tag{3.1.9}$$

RF Bandpass Filter (BPF)

This is a dielectric filter (Appendix C-2: U7) from Soshin. Its passband band covers the transmit band with a 2.5dB insertion loss. Its out-band rejection is 30dB. It removes the spectral impurity of the signals. As mentioned in Section 3.1.3.3, there is a need for 83dB power suppression in the receiving band. This BPF produces 30dB of the suppression.

Resistive Pad

There are two π-type resistive pads. Resistance values for π-type resistive attenuator is given in [16]. One (Appendix C-2: R11, R13, R16) is at the output of the modulator chip and the other (Appendix C-2: R70, R71, R72) is at the output of the RF BPF. The use of the pads improve the stability of the PA driver. They set the output level of the modulator at –13dBm. The –13dBm output level prevents the subsequent power amplifier from operating in saturation to ensure good adjacent channel power suppression.

3.1.4.3 Transmit Power Control (TPC)

The TPC resides on the automatic frequency control (AFC) board that will be discussed in the receiver section. The control includes an ADC and a level shifting circuit as shown in the block diagram in Figure 21. The schematic is in Appendix C-5.

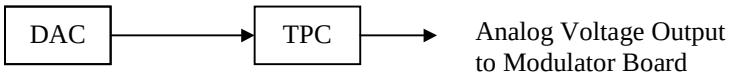

Figure 21. Block diagram of the power control.

The TPC accepts a 7-bit digital command from the baseband processor and provides a scaled analog voltage to drive the attenuator on the modulator board. The control voltage is connected to the two attenuators in parallel. The required attenuation is evenly distributed between the two attenuators. The command code is between 0000000B and 1000110B (or 0 to 70 decimal). The analog voltage output is from 5V to 0.5V. The code 0000000B produces 5V analog voltage output, while the code 1000110B produces 0.5V analog output.

AD557 DAC

The AD557 (Appendix C-5: U5) is a 8-bit digital-to-analog converter (DAC) from Analog Devices. It is the interface between the baseband processor and the TPC. The DAC has one bit more than the command length. In order to fully utilize the output range of the DAC, the command digits are tied to the most significant 7-bits of the DAC and the least significant bit is held high. Thus, the command is effectively multiplied by a factor of 2. Table 4 lists the input-output relationship of the DAC.

Table 4. The input-output relationship of the DAC.

Output Power	Command	AD557 DAC out (V)
30dBm maximum	0000000	0.01
-40dBm minimum	1000110	1.41

The 10mV residual voltage is a result of the least significant bit being tied high. The maximum output settling time of the DAC is 1.5μs so that the DAC easily supports the 0.625ms power control cycle time.

Level Shifting Circuit

The level shifting circuit is built with a LM6132 (Appendix C-5: U10) chip from National Semiconductor. The device contains two operational amplifiers. The two amplifiers form a two-stage level shifting circuit. The 1st stage is a voltage follower (Appendix C-5: U10A) required to buffer the DAC output. The 2nd stage is an inverting amplifier (Appendix C-5: U10B) needed to produce the phase inversion and the level shifting as shown in Table 5.

Table 5. The input-output relationship of the level shifting circuit.

Output Power	Analog in from DAC (V)	Analog out (V)
30dBm maximum	0.01	5
-40dBm minimum	1.41	0.5

The exact level shifting is not well defined in practice because of the variation of the RF attenuation. Two variable resistors (VR) are used to provide the adjustment of the level shifting so that the variation can be compensated. One VR (Appendix C-5: R19) is used to shift the analog output up or down. The other VR (Appendix C-5: R18) is used to set the slope of the input-output relationship. The two adjustments provide the flexibility to set the maximum and minimum of the analog output.

3.1.4.4 Power Amplifier

The power amplifier boosts the –13dBm transmit signal from the modulator board to 31.5dBm. The output should have 40dBc or more adjacent channel power suppression.

The required gain of the amplifier is 44.5dB. As mentioned in Section 3.1.3.2, the power handling capability of the amplifier should be 36dBm to address the 4.6dB peak-to-average factor of QPSK signals.

The power amplifier is a two-stage implementation for the high gain and high power requirement. Figure 22 is the block diagram.

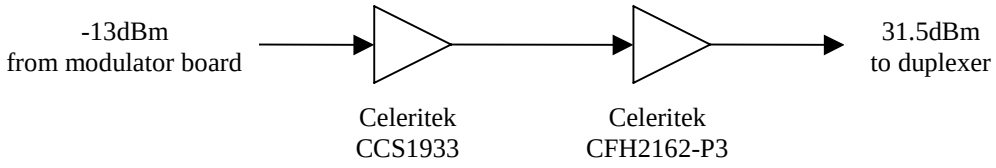

Figure 22. Two-stage power amplifier.

Both stages are built with Celeritek devices. The 1st stage is the CCS1933 evaluation board from Celeritek. The first trial of the power amplifier implementation only utilized the CCS1933. However, the adjacent channel power suppression was unsatisfactory because the CCS1933's power handling capability is 33dBm (3dB below the requirement). To address this problem, a 2nd stage is to be added after the CCS1933. CFH2162-P3 was chosen for this stage because it has 36dBm power handling capability.

The 1st stage of the CCS1933 evaluation board produces 35dB gain and boosts the transmit power to 22dBm. Experiments reveal that the adjacent channel power suppression at the 22dBm power output is 41dBc.

The CCS1933 board consists of a driver amplifier (CMM1301) and a matched power amplifier (CFK2162-P3). Both of them operate from a 5Vdc supply. The CMM1301 drive amplifier is biased for 150mA drain current with a negative gate voltage. The CFK2162-P3 power amplifier is matched on board for 50Ω. It is biased for 1.2A drain current with another negative gate voltage. Both the negative gate voltages are derived from a –5Vdc supply through resistive potential dividers. The potential dividers are built

with multi-turn potentiometers to facilitate a precise bias adjustment. To prevent damage to the two amplifiers, the negative bias voltages must be applied to the amplifiers before the 5Vdc drain supply.

The 2nd stage being considered is the Celeritek CFH2162-P3 power amplifier. The 1dB output compression point of the amplifier is 36dBm. This meets the required power handling capability of 36dBm. The input to this amplifier is around 22dBm and the amplifier delivers 31.5dBm transmit power. The 31.5dBm output power is 4.5dB below the 1dB output compression point so that linear operation of the amplifier will contribute insignificant adjacent channel power. Thus the specified 40dBc adjacent channel power suppression can be achieved.

3.1.4.5 Duplexer – Transmitter part

The duplexer was designed and built by Dr. Sweeney. It is a three-port filter device. It includes a transmitting bandpass filter and a receiving bandpass filter. The use of the duplexer allows the radio to simultaneously transmit and receiver on a single antenna. This saves the cost of a separate antenna and eases the system construction. Figure 23 depicts the physical layout of the duplexer.

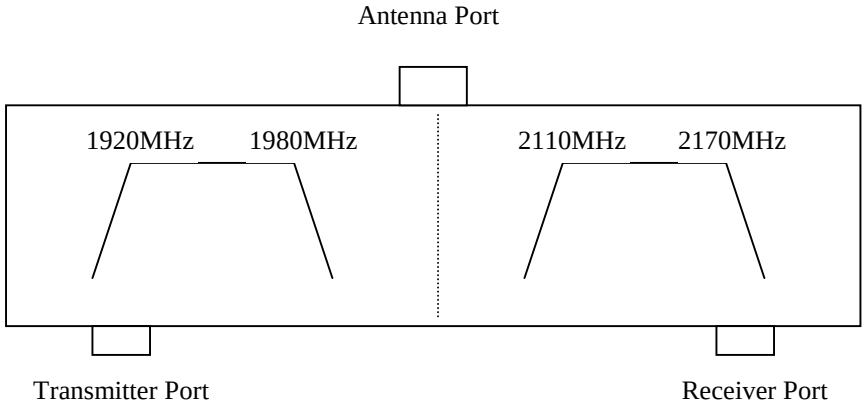

Figure 23. Physical layout of the duplexer.

The output of the power amplifier is connected to the transmitter port of the duplexer. The insertion loss of the duplexer in the transmitting band is 1.5dB. Thus the available transmitter power at the antenna is 30dBm. As mentioned in Section 3.1.3.3, the use of the duplexer may cause the receiver desense if the suppression of the noise at the receiving band is not adequate. The transmitting bandpass filter of the duplexer is designed to have a notch at the receiving band. The notch gives 70dB rejection to the receiving band. This 70dB rejection and the 30dB rejection from the RF BPF makes up 100dB receiving band rejection that is higher than the required 83dB rejection. Thus the receiver desense problem is well addressed. Figure 24 shows the simulated characteristics of the duplexer.

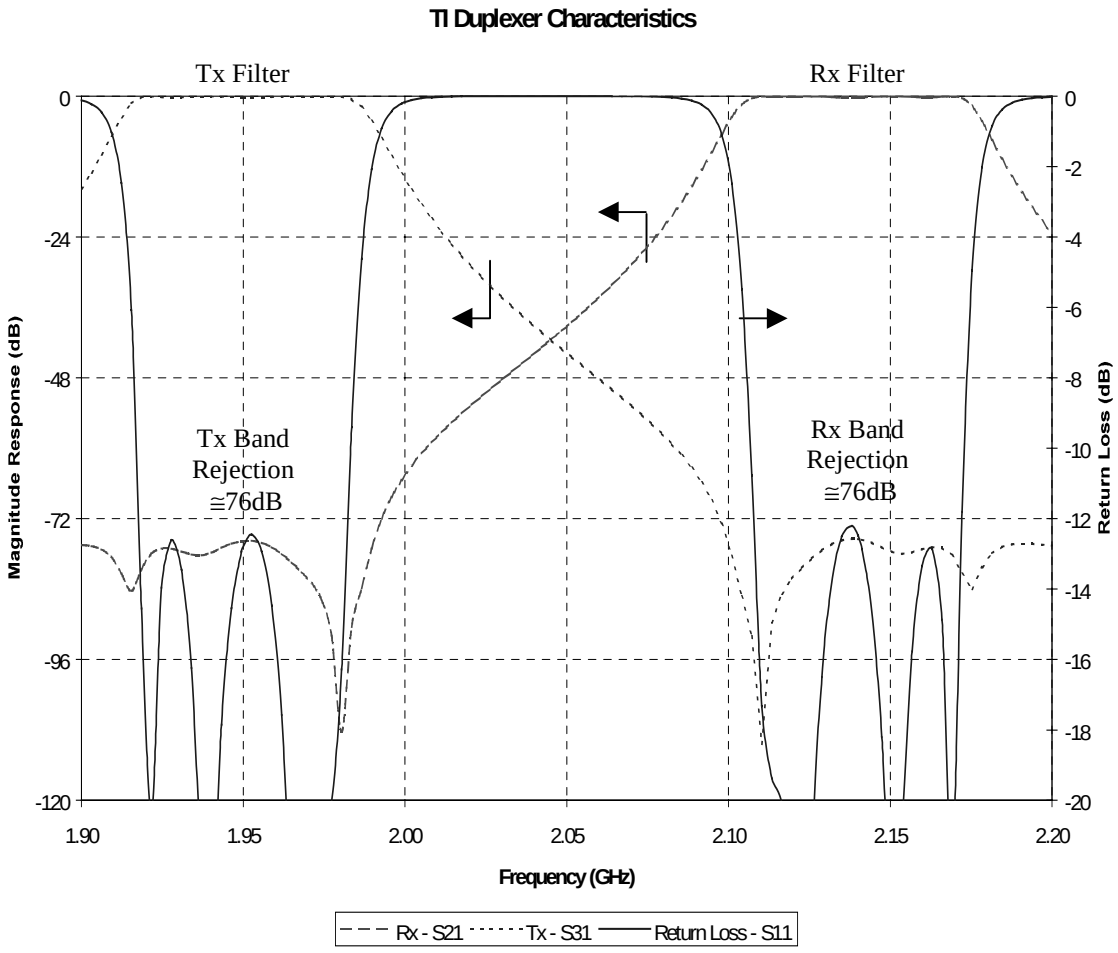

Figure 24. Duplexer Characteristics.

The receiving filter response curve (Rx-S21) shows that the transmit power rejection is approximately 76dB. The transmitting bandpass filter also provides approximately 76dB rejection to the receiving band as shown in the transmitting filter response curve (Tx-S31). The return losses of the filter in the receiving band and the transmitting band are both approximately 13dB as shown the return loss curve (Return Loss–S11).

The measured performance of the duplexer is tabulated in Table 6. The measured data match the simulated data well.

Table 6. Measured performance of the duplexer.

	Transmitting Band	Receiving Band
Insertion Loss (dB)	1.8	1.0
1dB Bandwidth (MHz)	71.3	66.3
3dB Bandwidth (MHz)	76.3	73.8
Receiving Band Rejection (dB)		
2110 MHz	74	
2140 MHz	71	
2170 MHz	72	
Transmitting Band Rejection (dB)		
1920 MHz		74
1950 MHz		73
1980 MHz		74