Inverter Dynamic Electro-Thermal Simulation with Experimental Verification

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Abstract

A full electro-thermal simulation of a three-phase space-vector-modulated (SVM) inverter is performed and validated with measurements. Electrical parameters are extracted over temperature for the insulated gate bipolar transistor (IGBT) and diode electro-thermal models. A thermal network methodology that includes thermal coupling between devices is applied to a six-pack module package containing multiple IGBT and diode chips. The electro-thermal device models and six-pack module thermal model are used to simulate SVM inverter operation at several power levels. Good agreement between model and measurement is obtained for steady state operation of the three-phase inverter. In addition, transient heating of a single IGBT in the six-pack module is modeled and validated, yielding good agreement.

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Chapter 1. Introduction

1.1 Background

Increasing needs for higher power density power electronics places greater demands on improving the quality of understanding of interactions between thermal and electrical properties of semiconductor devices. The insulated gate bipolar transistor (IGBT) module has become the switching device of choice for medium to high power applications during the past decade. These modules contain multiple IGBT and diode chips mounted on a common base-plate with an insulating medium.

There is a strong demand on modeling an entire system, both electrically and thermally, during the early stages of a design. Power systems are becoming greater in density and smaller in size. As a result, electro-thermal models are more important then ever before. Thermal coupling becomes more of a factor due to the close proximity of power devices, thus affecting system layout. A system engineer now has a tool that directly couples electrical and thermal parameters to better aid in design considerations. To reduce heat coupling between devices, for example, an engineer can adjust gate control to reduce the peak instantaneous junction temperature, thus allowing for closer device to device spacing. This analysis cannot be done with a thermal software package alone. With the complexity of system level design, comes the need for more complete and complex models, and this research accomplishes just that. A fully coupled, space vector controlled

voltage source inverter is modeled both electrically and thermally for the first time. Accurate thermal and electrical control models are developed herein, and tied to existing electro-thermal semiconductor device models to describe the entire system.

A physics-based IGBT model for the SABER® [1] circuit simulator has been previously developed and experimentally verified for power electronic circuit operating conditions [2]. The temperature-dependent IGBT parameters are included into a newly developed dynamic electro-thermal IGBT model for the SABER® circuit simulator [3]. An IGBT model parameter extraction sequence called IMPACT has also been developed [4] and used to characterize various IGBT's from different manufacturers. The IMPACT software package is used in this work to extract IGBT temperature and non-temperature dependent parameters needed for the electro-thermal IGBT.

A physics-based electro-thermal unified diode model for the SABER® circuit simulator has been previously developed and experimentally verified for power electronic circuit operating conditions [5]. The temperature and non-temperature dependent parameters for the diode are extracted and used in the unified diode model using the sequence developed in [4].

Traditional circuit simulators such as SPICE include temperature dependence, but the temperature must be chosen by the user once prior to simulation and remain constant during simulation. This approach does not accurately describe the thermal behavior of the device during operation. The devices are heated significantly by the power dissipated within the device (self-heating) and by power dissipated within adjacent devices (thermal coupling). The IGBT and diode electro-thermal models are capable of simulating self-

heating effects, and due to this work, can be coupled together to simulate the device-device interaction through thermal coupling.

The thermal network component models, developed in [3], are not applicable to high power modules because high power devices contain multiple chips within the same package that require heat conduction through the electrical isolation layers. Furthermore, the devices and modules are typically used with larger multi module heat sinks and have a highly non-uniform surface temperature. As a result of the close proximity of the IGBT and diode chips, thermal coupling within the module must be considered for effective computer aided design of the power electronic system. Thermal coupling was considered for a half bridge IGBT electro-thermal module which utilized a direct bond copper layer (DBC) between the IGBT and diode chips of a single phase inverter circuit [6]. The thermal module studied in this work comprises a three-phase inverter that contains all six IGBTs and diodes in one package. A more advanced coupling network must be considered within the DBC and base-plate layers between not only the IGBT and diode chips of a single phase, but between IGBT and diode chips of all phases.

Previously, the dynamic performance of the electro-thermal IGBT model was studied in the simulation of a single-phase sinusoidal pulse width modulated (PWM) inverter circuit [7]. In this previous work, simulation techniques were developed to arrive at steady state conditions. The simulation results were never compared with hardware performance. Electro-thermal diode models were not included in this previous work and only single IGBT packages were considered. The fully-coupled six pack IGBT electro-thermal model containing multiple IGBT and diode chips is used in this work to simulate a three phase space vector modulated (SVM) voltage source inverter (VSI). The steady-

state IGBT temperature is monitored and used for model validation under three different loading conditions. The transient thermal response of the model is validated using a high speed transient thermal response measurement tool developed in [8].

1.2 Thermal Model Methodology

It is well-known that heat flows from a region of higher temperature to a region of lower temperature, and can be described by the heat diffusion equation [9].

$$A\rho c\frac{\partial T}{\partial t} = Ak\frac{\partial^2 T(z)}{\partial z^2} \tag{1.1}$$

A temperature gradient T exists across a finite element z. A represents the area perpendicular to heat flow. ρ is the density of the material which the heat travels. k and c represent the thermal conductivity and specific heat of the material respectively. Several methods have been developed to solve the heat diffusion equation. Some of these methods, described in [3], include steady-state Fourier series solution, convolution of the thermal step response with analytical power dissipation functions, empirical extraction of thermal network element values from the measured step response, physics-based thermal resistance and thermal capacitance network element analysis, and three-dimensional finite difference and finite element simulations. The limitations of these approaches are described in detail in [3], but the main point is that all of the methods have limitations that prevent efficient dynamic electro-thermal simulation.

Using the appropriate symmetry conditions in the discretization of the nonlinear second order partial differential heat diffusion equation, the heat diffusion equation can be

mathematically modeled by a first order ordinary differential equation [3]. Details of this derivation are given in chapter 3.

Once discretized, this first order equation can be modeled by an equivalent electrical circuit. Resistors are used to describe the thermal resistance to the flow of heat energy, while capacitors are used to model the thermal time constants under transient heating conditions. Steady state occurs when the quantity of heat generated by a device is equal to the quantity of heat being removed from it.

The different thermal networks describing heat flow are shown in Figure 1.1 (a-d).

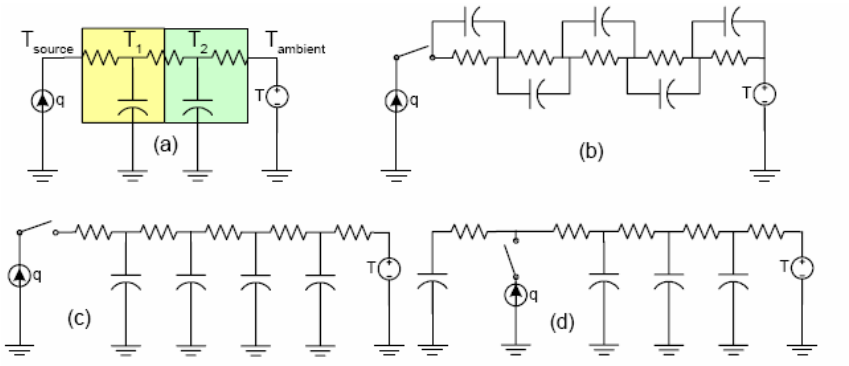


Figure 1.1. Example of one-dimensional thermal networks: (a) general approach; (b) Fosternetwork; (c) Cauer network for a top uncovered device; (d) Cauer network for a top covered device [10].

In [10], the author describes the difference between each of the networks shown in Figure 1.1. Figure 1.1 (b-d) represent the Foster network, the Cauer network, and Cauer network for a top-covered device, respectively.

The author points out that only the Cauer circuits are suitable for faithfully representing the system from the physical point of view. In the electrical circuit, the current flowing across the capacitor during a dynamic regime is the same on both sides of the device due to the symmetrical variation of the positive and negative electric charges. Thermal circuits have no quantities equivalent to negative electric charge. Only the heat flow on

one side of the capacitor has a real meaning, therefore the Cauer networks, with the capacitors grounded on one side, are more suitable as a thermal analogy [10].

Motorola uses the RC equivalent electrical circuit to describe the thermal behavior of their electrical devices [11]. Figure 1.2 shows the equivalent circuit that Motorola uses to describe the thermal heat flow.

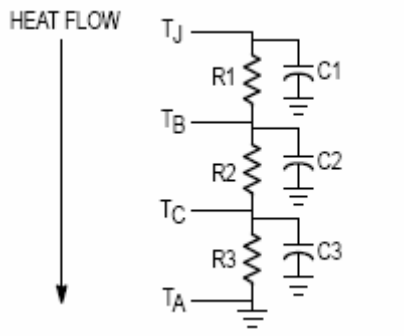


Figure 1.2. Motorola Equivalent thermal circuit [11].

Resistor *R1* is the thermal resistance from the device's junction to its die–bond. Resistor *R2* is the thermal resistance from the die–bond to the device's case. Resistor *R3* is the thermal resistance from the device's case to ambient. The thermal resistance from the junction to a reference point is equal to the sum of the individual resistors between the two points. For instance, the thermal resistance $R_{\theta JC}$ from junction–to–case is equal to the sum of resistors *R1* and *R2*. The thermal resistance $R_{\theta JA}$ from junction–to–ambient, therefore, is equal to the sum of resistors *R1*, *R2* and *R3*. The capacitors shown model the transient thermal response of the circuit. When heat is instantaneously applied and or generated, there is a charging effect that takes place. This response follows an RC time constant determined by the resistor–capacitor thermal network. Thermal resistance, at a

given time, is called transient thermal resistance, $R_{\theta JR}(t)$. Device datasheets will give the parameters $R_{\theta JC}$, $R_{\theta JA}$ and $R_{\theta JR}(t)$ for any given device [11].

The author in [12] proposes an IGBT thermal model whose parameters are extracted from transient thermal resistance measurements. The author points out that the parameters given in datasheets, such as the parameters described above from Motorola, use an ideal heat sink or case temperature during measurement. This is not accurate since the IGBT package usually interfaces with a non-ideal heat sink in real-world applications, e.g., inverters. The same thermal network seen in Figure 1.2 is used for the IGBT thermal model in [12], but the parameters are extracted from transient thermal resistance measurements using a non-ideal heat sink. The transient thermal resistance $R_{\theta JC}(t)$ from junction-to-case and $R_{\theta CA}(t)$ from case-to-ambient are measured. The author points out that measuring the thermal transient resistance from case-to-ambient $R_{\theta CA}(t)$ is more realizable than measuring the thermal transient resistance from junction-to-ambient $R_{\theta JA}(t)$. The thermal transient resistance $R_{\theta JA}(t)$ is therefore derived from the other two measurements using Fourier series expansions. Finally, the resulting RC combinations needed for the IGBT thermal model can be extracted from the measured data.

The thermal methodology developed in this work is primarily based on the work developed by Hefner [3] and is described below. Hefner's thermal model is based on the general approach seen in Figure 1.2 (c). While this approach is widely used, Hefner uses a more advanced algorithm when calculating the parameters that describe the thermal resistances and capacitances making up the thermal networks. Hefner develops a thermal network for the silicon chip, package, and heat sink. The silicon chip thermal model considers the nonlinear thermal conductivity of silicon and includes a distributed heat

source option that calculates the power dissipation density as a function of depth into the chip. In calculating thermal resistance within the package layers, Hefner uses an approach known as the effective heat flow area approach which describes the two dimensional lateral heat spreading effect and the main heat flow area from the bottom of the silicon chip all the way down to the bottom of the base-plate. All heat flow outside the main heat flow area is accounted for by an additional node called the periphery node. Hefner also proposes a grid spacing (RC combinations) that increases logarithmically with distance from the heat source (Tj node) to maximize computation efficiency and to more accurately represent the dynamic temperature distribution for the applicable range of heating rates.

Again, the techniques described above for a single chip package, are extended in this work for a multi-chip package. Lateral thermal coupling is developed and based on the techniques developed in [6].

1.3 Electro-thermal Model

The electro-thermal model for the IGBT has been developed by Hefner and is a standard library part in the SABER® circuit simulator. The electro-thermal diode model also is a standard library component and is based on the unified diode model developed in [5]. These models make up the system level simulation and are coupled with the newly developed six-pack thermal model.

The electro-thermal models for power semiconductor devices connect to both the electrical and thermal networks. The IGBT electro-thermal model has three electrical

terminals and one thermal terminal. The IGBT electrical terminals are connected to the electrical network component models, and the thermal terminal is connected to the thermal network component models. The electro-thermal diode also has two electrical terminals and one thermal terminal.

To couple the electrical and thermal networks, the IGBT and diode electro-thermal models describe the instantaneous electrical behavior in terms of the instantaneous temperature of the device silicon chip surface Tj (temperature at the device thermal terminal). The temperature dependent electrical models are based upon temperature-dependent IGBT and diode model parameters and the temperature-dependent physical properties of silicon. The IGBT and diode electro-thermal models also calculate the instantaneous power dissipation from the internal components of current since a portion of the electrical power delivered to the device terminals is dissipated as heat and the remainder charges the internal capacitances. The dissipated power calculated by the electrical model supplies heat to the surface of the silicon chip thermal model through the thermal terminal [3]. Figure 1.3 shows the electro-thermal model for the IGBT, for example, and the corresponding electrical and thermal terminals.

The electrical type terminals have units of voltage (V) across the terminals and units of current (A) flowing through the terminals, whereas the thermal type terminals have units of temperature (K) across the terminals and units of power (W) flowing through the terminals.

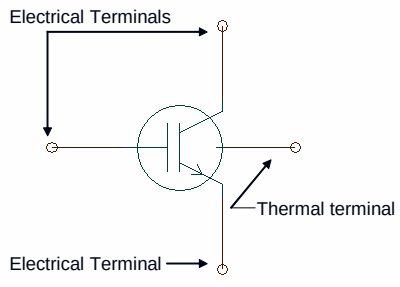


Figure 1.3. Electro-thermal symbol for the IGBT.

The temperature-dependent and non temperature-dependent electrical parameters are needed to use the SABER® IGBT and diode models. These parameters are extracted using advanced parameter extraction sequences. Once the parameters are validated, the user imports them into the corresponding models and the models are then ready to use for simulation.

1.4 Electro-thermal System Simulation

An electro-thermal simulation of an IGBT pulse width modulated (PWM) inverter was previously studied in [7]. A full-bridge voltage source inverter was constructed with four electro-thermal IGBTs and four non electro-thermal diodes. The electro-thermal IGBT models were connected to four corresponding silicon chip, package, and heat sink thermal networks. The thermal networks did not need to consider any heat coupling because each IGBT had its own package and heat sink. And since regular diode models were used, there was not any thermal interaction studied between the IGBT and diode. The main purpose of the work in [7] was to study the dynamic electro-thermal behavior that would exist within a real system containing PWM gate-drive control and loading

conditions. The thermal response of the thermal network was studied over one switching cycle (20 kHz). The anode voltage and anode current of the IGBT was examined in parallel with the chip junction temperature. Losses were calculated at turn on and turn off. The dynamic response of the chip junction temperature was directly determined by the switching and conduction losses. This analysis is very useful because the dynamic thermal response can be directly coupled to the electrical behavior of the IGBT. The effects of the temperature dependent parameters of the IGBT can be better understood thermally and electrically. This aids the engineer to better understand the entire system behavior thermally and allow for better layout and cooling considerations.

The dynamic and steady-state behavior of the system was also analyzed from a full start up condition. The procedure for achieving this is described in chapter 4 since the time constants for an entire startup can be very long in simulation time. It is important to understand the thermal response for both high and low frequencies. The high-frequency response is due to the switching frequency and the low frequency is a result of the 60 Hz load variation. The simulation was never validated with measured results.

In the work presented here, we extend the system level simulation studied in [7] to include a three-phase space vector modulated inverter with a fully coupled electro-thermal model made up of IGBTs and diodes. Steady-state and transient conditions are validated with electrical and thermal measurements. Previously, only thermal steady state performance/validation of a half bridge electro-thermal model was presented in [6]. Thermal coupling was considered between three half-bridge modules through a common heat sink and validated with measurement.

Other authors have also tried their hand at transient electro-thermal IGBT simulations. The author in [13] proposes an electro-thermal model for the IGBT with a proposed parameter definition method for the electrical IGBT model within the SIMPLORE circuit simulator. Validation is achieved by comparison of thermal pulses within the simulator with measured results. The IGBT electrical model within the SIMPLORE circuit simulator describes three temperature dependent parameters including the BJT saturation current, base-resistance of the BJT, and the time constant of the IGBT turn off tail current. Model validation of these parameters is achieved with measured and simulated results of the V_{CE}-I_C characteristic over temperature. The author proposes a new thermal model seen in Figure 1.4 to try and overcome the difficulties of modeling the three dimensional lateral thermal spreading. The impedance $Z_{th(t)}$ in Figure 1.4 is chosen to match the results achieved in a 3D thermal solver called FEM. The author also considers an additional impedance for thermal "interference" between possible adjacent devices.

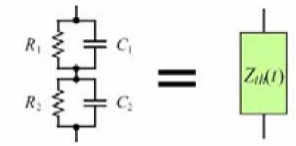


Figure 1.4. Proposed compact thermal model [13].

In [13], two parallel IGBTS are connected and simulated using the proposed electrical and thermal models to study the effects of thermal "interference". Some difficulties were encountered during this simulation. Because the electrical model demands very small time steps, very high unexplained dissipated powers were sometimes encountered which caused junction temperatures to be predicted in the thousands of degrees. This problem

was eliminated by using average powers over different spans of time to be applied to the compact thermal model [13].

The model developed in this work contains the same temperature dependent parameters developed in the SIMPLORE model. The simulation difficulties associated with small time step in the SABER® circuit simulator were not seen and may be a result of a more robust IGBT electro-thermal model. For example, the number of thermal nodes and grid spacing is optimized for simulator performance. Three dimensional lateral heat spreading is taken care of with the effective heat flow area approach and a distributed heat source option in the silicon chip model may allow for more reasonable junction temperatures (i.e. the heat is not all dissipated at the junction but distributed through the chip). The coupling used in both models is very similar.

In a recent paper, [14], the author presents a simplified electro-thermal methodology. Instead of using physics-based models to accurately describe the very important switching losses, dependent sources are used to make linear approximations of switching loss. The assumed linear approximation of the switching characteristic is shown in Figure 1.5.

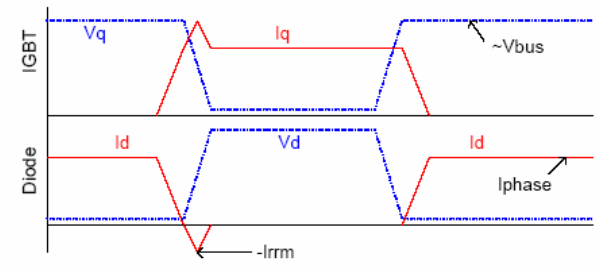


Figure 1.5. Idealized switching waveforms [14].

The proposed model in [14] approximates the waveforms in Figure 1.5 with square waveforms as seen in Figure 1.6. Here logic devices along with dependent sources are used to reproduce the idealized square wave-forms in Figure 1.6. The overall losses in Figure1.6 are the same as those in Figure 1.5. The calculated power dissipation acquired from these waveforms would be used in a thermal network. The idea is to remove the very long simulation time associated with switching transitions, where a very small time step is required to resolve the nonlinear physics based models.

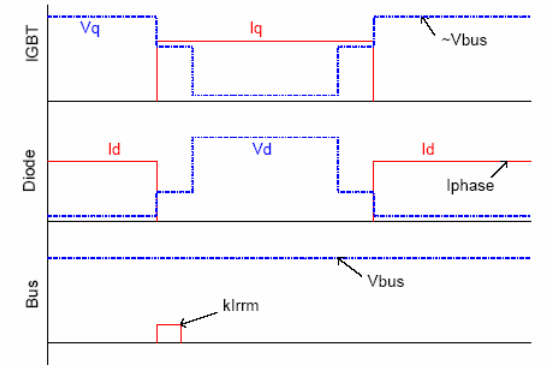


Figure 1.6. Approximated waveforms to Figure 1.5 [14].

This simplified model results in very fast simulation time, but knowledge of the power dissipations and assumed switching losses need to be known ahead of time. This would require accurate measurements. Switching loss is highly dependent not only on the device and on the device properties, but the system the device would be used in. For example, certain control schemes can be implemented to lower switching loss. Therefore a full system would be required each time a model is to be created. While the simulation and model would be very robust, the actual measurements required to create the model may be unrealizable.

1.5 Summary

This work presents a fully coupled dynamic electro-thermal model of a three phase IGBT power module. Temperature and non temperature dependent parameters of six IGBTs and six diodes are extracted using an advanced parameter extraction program. These parameters are used within the existing physics based electro-thermal semiconductor models available in the SABER® circuit simulator. The effective heat flow approach [3] is used to describe the thermal behavior of the six-pack module. An advanced thermal coupling network is considered for the first time to describe the coupling between six IGBTs and six diodes within the module. A space vector modulated voltage source inverter is simulated for the first time with the fully coupled dynamic electro-thermal model. Transient and steady state thermal behavior of the system hardware is used to validate the electro-thermal model under three different power levels.

We begin with the extracted temperature and non temperature dependent electrical parameters for both the IGBT and diode. These parameters are used within the physics based models within the SABER® circuit simulator. The details of these parameters are given in chapter 2. A detailed thermal network with advanced coupling consideration is described in chapter 3. Chapter 4 presents the system level simulation of the three phase space vector modulated voltage source inverter with validation. Chapter 5 will describe the major contributions and future work.

Chapter 2. Parameter Extraction for Electro-thermal IGBT and Diode

2.1 Introduction

This chapter describes the methodology for modeling the electrical behavior of the IGBTs and diodes used in a six-pack three phase power module. The traditional way of modeling semiconductor models in SPICE-based circuit simulators has been to use linear approximations to describe the forward and reverse operating characteristics. While there are some SPICE-based physics based semiconductor models, the temperature used by the device models are chosen by the user prior to simulation and remains constant during the simulation. The models used in this work contain temperature dependent model parameters obtained by using extracted values of the model parameters versus temperature. An accurate extraction sequence is needed to resolve the temperature dependence of the model parameters. The advantage of using physics-based models for semiconductor devices is that the well known temperature dependent properties of silicon can be used to describe the temperature dependence of the model, and only a few temperature dependent model parameter expressions must be developed to describe the device to be modeled.

The electrical models developed in this chapter are coupled with the thermal models developed in chapter three to create a fully coupled dynamic electro-thermal model to be used in a full three phase vector controlled system simulation. Inverter applications

dissipate a large amount of heat in their semiconductor devices, mainly due to the high switching losses, and accurate models are needed for system level simulation to predict these losses. This chapter presents the extracted temperature and non temperature dependent model parameters for both the IGBT and diode.

2.2 Diode Model

The extracted diode parameters and temperature dependent coefficients are used in an existing electro-thermal unified diode model in SABER® [5]. The unified diode model represents the unification of low-power, microelectronic diode modeling technology and the latest developments in high-power diode modeling [5]. This model allows the user to describe either low or high power diodes.

We begin with describing the forward-bias operating region. The DC characteristics are shown in Figure 2.1. The effects shown are low-level depletion recombination, normal low-level injection, high-level injection, emitter recombination, and series resistance.

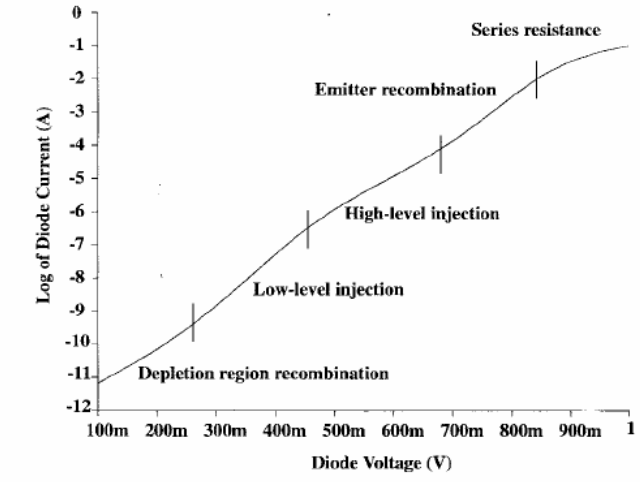


Figure 2.1. Forward dc characteristics of diode model [5].

The objective of the thesis is to describe a process of electro-thermal system simulation. Therefore, it is not important for us at this time to describe the entire diode forward characteristic as seen in Figure 2.1. For now we will concern ourselves with modeling more the diode operating region we expect in system level simulation. This does not include the current densities that would be described by the depletion region recombination or the emitter recombination. More importantly, we will include the low-level and high-level injection and series resistance effects typically seen in power diodes. We remove the recombination effect by setting the diode parameter, *ISR*, to be zero. We will also not include the emitter recombination effect by setting the diode parameter, *ISE*, to be zero. The following expression is the classical expression describing low-level injection [5].

$$i_{Ldiode} = ISL \cdot (e^{\frac{V_j}{NL \cdot V_T}} - 1) \tag{2.1}$$

An equivalent expression is used for high level injection. This effect is present in the power diodes and should be modeled. An attempt was made to model this effect. Parameters were extracted over temperature, but results showed that there were not enough points taken to accurately describe the high level injection over temperature. This is saved for future work. For now we will make use of (2.1) to describe as closely as possible both the low and high level injection regions. The equation describing high level injection is the same equation as (2.1) with *ISL* and *NL* replaced with *ISH* and *NH* respectively. From a system level simulation standpoint, matching the exact forward I-V curve is not necessary because this will not affect the conduction losses significantly. Equation 2.1 is good enough.

Figure 2.2 shows the measured forward I-V curves over several temperatures for the diode modeled in this work. It can be seen from the curves that the saturation current goes up as a function of temperature. This has the effect of shifting the curves to the left. Also, the mobility goes down with temperature causing the on resistance, R_{on}, to increase thus decreasing the slop of the I-V curve in the higher current region.

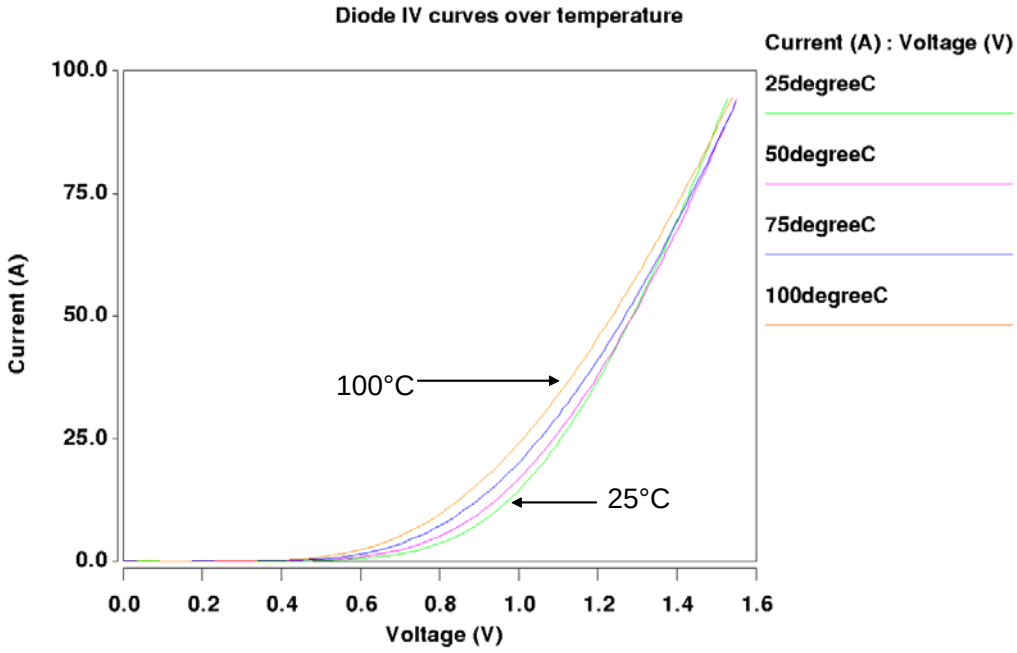


Figure 2.2. Measured forward IV curves over temperature.

From (2.1), the parameters *NL* and *ISL* need to be determined. Both of these parameters are a function of temperature and need to be extracted and described over temperature. We note that the parameter V_T is also a function of temperature and is a well known property of silicon and not described in this chapter.

The first step in extracting the above mentioned parameters is to determine the diode equivalent series resistance. This is proportional to the inverse slope of the forward I-V

curve in the high level injection region (higher current). Figure 2.3 shows the equivalent series resistance and how the junction voltage of the diode, V_j, and the actual measured voltage, V_D, are related.

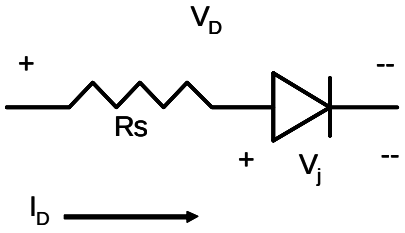


Figure 2.3. Assumed topology described by (2.1).

The junction voltage, *Vj*, is calculated from Figure2.3.

$$V_j = V_D - I_D \cdot R_s \tag{2.2}$$

The measured diode voltage, $V_{D,}$ and the measured diode current, $I_{D,}$ are used with (2.2) in (2.1) to extract the diode parameters *ISL* and *NL*, where i_{Ldiode} is replaced with the measured data I_D. Taking the log of (2.1):

$$\log I_D = \log(ISL(e^{\frac{V_j}{NL \cdot V_T}} - 1)) \tag{2.3}$$

Expanding (2.3) and simplifying:

$$2.3 \log I_D = 2.3 \log(ISL) + \frac{V_j}{NL \cdot V_T} \tag{2.4}$$

Equation 2.4 is a linear relationship and the slope and y intercept of the data points can be used to determine *NL* and *ISL*. Table 2.1 shows the extracted values for *ISL*, *NL* , and the diode equivalent series resistance *Rs* for each temperature.

Table 2.1 Extracted Forward Diode parameters over temperature

	Rs	**ISL**	**NL**
25 degree C	0.004325	0.00125	3.8922
50 degree C	0.0047	0.00285	3.8203
75 degree C	0.00515	0.005	3.623
100 degree C	0.00555	0.015	3.6161

The next step is to determine the temperature dependent behavior of *Rs*, *NL* and *ISL*. The temperature dependence of all the following temperature dependent diode parameters is given in [5]. The temperature dependence of *Rs* is given by:

$$Rs(T) = Rs(T_{nom}) \cdot (1 + TRS1(T - T_{nom}) + TRS2(T - T_{nom})^2) \qquad (2.5)$$

The temperature dependent coefficients needed are *TRS1* and *TRS2*. The temperature dependence of *NL* is given by:

$$NL(T) = NL(T_{nom}) \cdot (1 + TNL1(T - T_{nom}) + TNL2(T - T_{nom})^2) \qquad (2.6)$$

The temperature dependent coefficients extracted from (2.6) are *TNL1* and *TNL2*. The temperature dependence of *ISL* is given by:

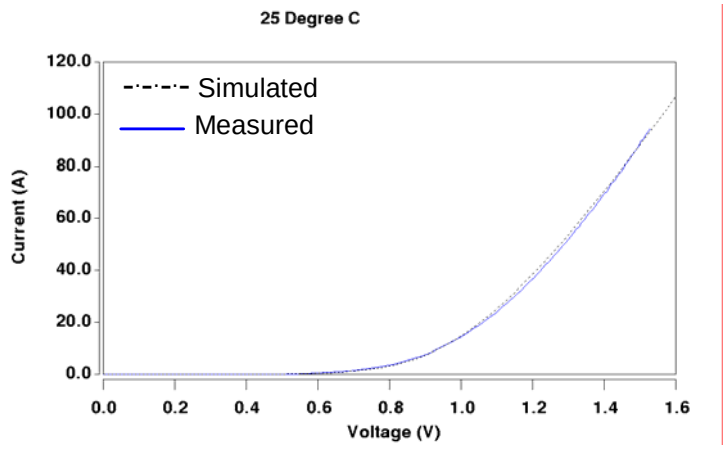
$$ISL(T) = ISL(T_{NOM}) \cdot \left(\frac{T}{T_{NOM}} \right)^{\frac{XTI}{n}} \cdot e^{\left(\frac{T}{T_{NOM}} - 1\right) \cdot \left(\frac{E_g}{n \cdot V_T} \right)} \quad (2.7)$$

Where the bandgap voltage, Eg, is a well predicted temperature dependent semiconductor property. *XTI* describes the temperature dependence of *ISL*. Table 2.2 shows the extracted temperature dependent coefficients extracted from the above equations describing the temperature dependent parameters.

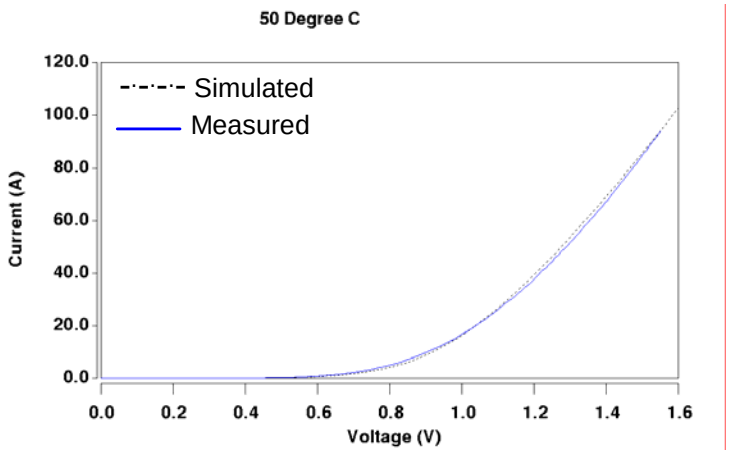
Table 2.2 Temperature dependent coefficients

TRS1	3.12E-03
TRS2	1.39E-05
TNL1	-6.35E-04
TNL2	-4.14E-06
XTI	-2.36E+00

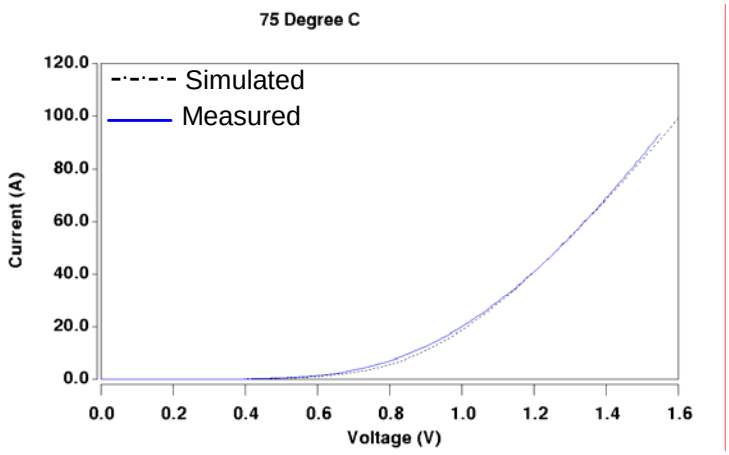
Figure 2.4 (a-d) shows the forward characteristics of both the measured and simulated diode characteristics. The measured data is shown in blue and the simulated result is shown in the dotted black in the following figures. The model does a reasonable job predicting the forward characteristics over temperature, thus validating the parameters and coefficients described above.


25 Degree C
Simulated
Measured
Current (A)
120.0
100.0
80.0
60.0
40.0
20.0
0.0
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
Voltage (V)

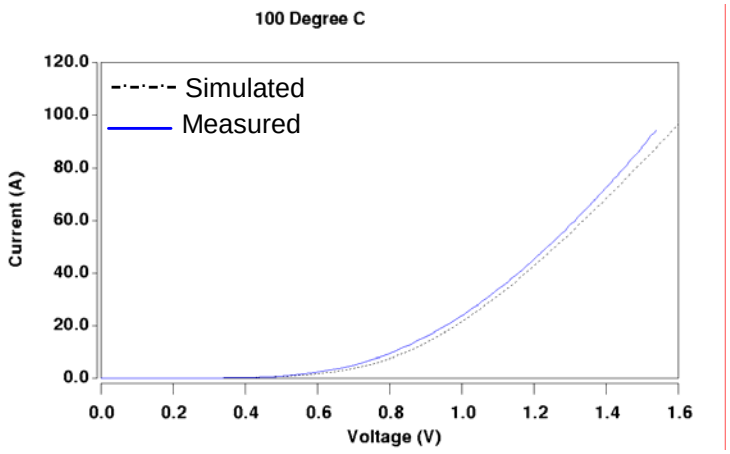
(a)


50 Degree C
Simulated
Measured
Current (A)
120.0
100.0
80.0
60.0
40.0
20.0
0.0
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
Voltage (V)

(b)


75 Degree C
Simulated
Measured
Current (A)
120.0
100.0
80.0
60.0
40.0
20.0
0.0
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
Voltage (V)

(c)



(d)

Figure 2.4. Measured versus simulated forward diode characteristics over temperature.

The unified diode models the reverse bias operating region, but again from a standpoint of system level simulation, this region of operation is not necessary to describe. The reverse bias operating area does not contribute to the overall losses when compared to the forward and transient losses, therefore we disable this feature by setting ISZ to be undefined.

The most important feature to capture in the diode model is the transient characteristic. The diodes behavior during transients directly contributes to the high energy losses that occur in real system behavior. The diode reverse recovery characteristic for example directly relates to the high turn on losses seen by the IGBT in inverter applications. The peak current that the IGBT has to handle is directly related to how well the diode behaves during the reverse recovery. The next discussion describes the modeling of the diode reverse recovery behavior [15].

Reverse recovery occurs when a forward conducting diode is rapidly turned off. The charge that is built up in the diode while it is forward biased must be removed before the

device can settle into steady state. Figure 2.5 shows the power diode, PIN, carrier distribution profile and potential distribution for high level injection conditions.

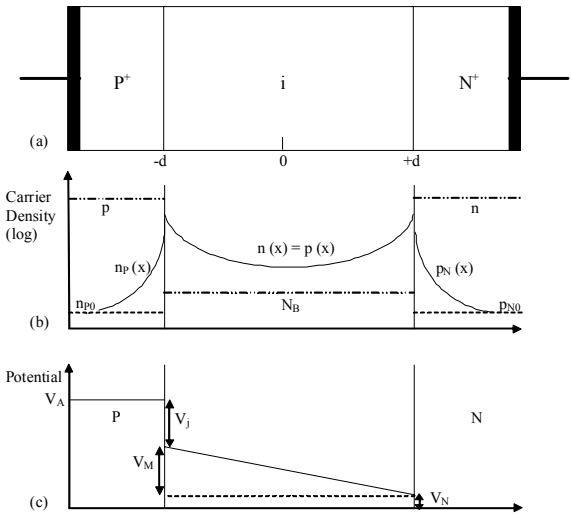


Figure 2.5. (a) PiN diode representation, (b) corresponding carrier distributionprofile, and (c) potential distribution for high-level injection conditions [15].

During forward bias, charge is distributed in the lightly doped i region in catenary fashion such that *n(x)=p(x)*. When the device is switched off, charge can either recombine, diffuse out of the lightly doped region, or be swept out due to a high field. The unified diode model accounts for all of these possibilities [15]. Either way, a large reverse current has to account for this charge removal. Figure 2.6 shows the relationship between the diode voltage and current when commanded to turn off. The diode does not start to block voltage until the diode hits the peak reverse recovery current. At this point, the charge density at the junction has decreased to zero and the depletion region can start to support the voltage and sweep out the rest of the charge.

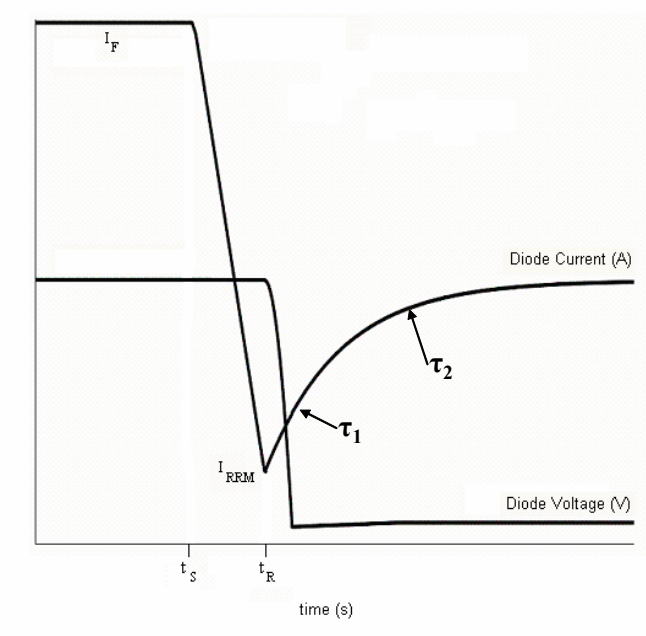


Figure 2.6. Ideal reverse recovery characteristics for PiN diode [19].

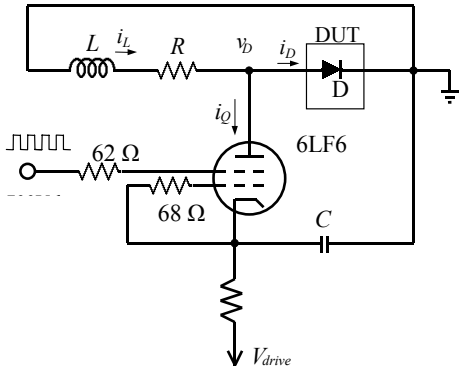
The model parameters *TSW* and *TM*, along with *TT*, control the charge sweep out effect and diffusion effect, respectively. The two time constants, τ_1 and τ_2, seen in Figure2.6 are calculated as follows [5]:

$$\tau_1 = \frac{TT \cdot TSW}{TT + TSW} \tag{2.8}$$

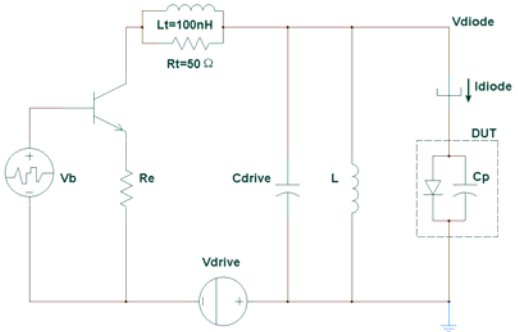
$$\tau_2 = \frac{TT \cdot TM}{TT + TM} \tag{2.9}$$

Figure 2.7 (a) shows the test circuit used for characterizing the Si diodes for reverse recovery, and Figure 2.7 (b) shows the behavioral representation including parasitic elements used for diode model validation. It is important to note that the test circuit in Figure 2.7 (a) is well-characterized, meaning that the values of all circuit components and parasitic elements are known. To operate the test circuit in Figure 2.7 (a), first the

vacuum tube is turned on to establish the test current i_L in the inductor L. Once the test current is reached, the tube is ramped off and the inductor current is commutated to the Device Under Test (DUT). To initiate the reverse recovery test, the tube is ramped on with a well-controlled di_Q/dt at the tube anode. This results in a negative di_D/dt being applied to the DUT. As the diode begins to recover the diode voltage v_D rises toward the power supply voltage V_{drive} completing the recovery test [16].



(a)



(b)

Figure 2.7. High-speed reverse recovery test circuit and (b) behavioral model of reverse recovery test circuit in (a) [16].

The circuit of Figure 2.7 (a) uses a 6LF6 vacuum tube as a driver device in place of the usual MOSFET to achieve low parasitic capacitance at the DUT anode and an extremely

fast switching speed. The 51 Ω resistor R isolates the DUT from the parasitic capacitance of the 30 mH inductor L and is also used to quickly reset the inductor current to zero after each test. The dv/dt of the square wave applied to the tube screen is varied to achieve different di_D/dt values for the DUT [16].

Figure 2.7 (b), uses an ideal bipolar transistor model with an emitter follower resistor, R_e, to emulate the di_D/dt applied by the tube. The bipolar transistor model capacitance parameters are set to zero and replaced by the 40 pF output capacitance of the tube (combined with C_{drive} in Figure 2.7 (b)). The next most important parasitic elements of the test circuit are the 100 nH tube inductance L_t and the 50 Ω tube resistance R_t that result in a small voltage overshoot near the end of the diode current recovery waveform. The inductor L remains at 30 mH as in Figure 2.7 (a). The pulse width of the signal generator V_b is varied to determine the forward current for the reverse recovery test, and the rise time of V_b determines the di_D/dt applied to the DUT at turn off [16].

Figure 2.8 shows the measured results of the diode reverse recovery over different temperatures.

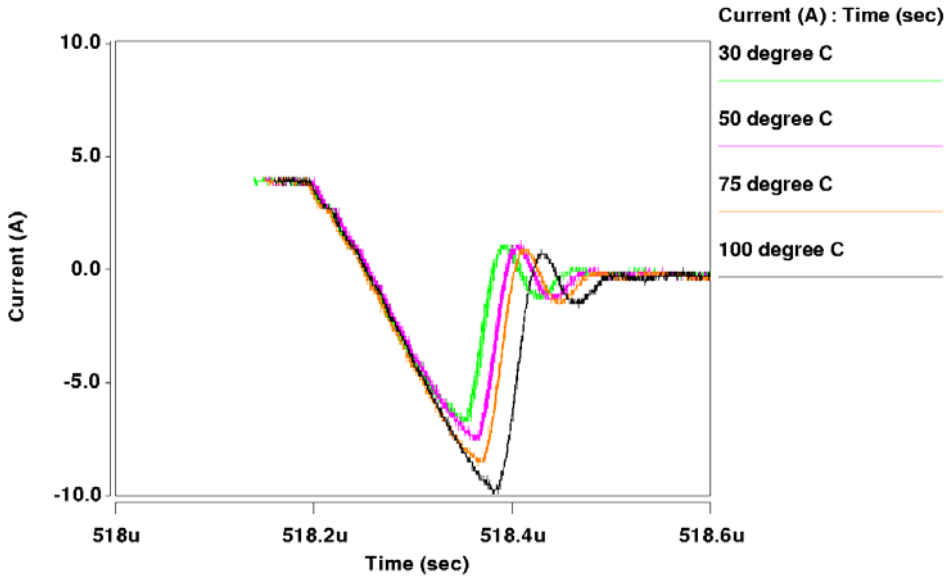


Figure 2.8. Measured Reverse Recovery of Diode.

The circuit in Figure2.7 (b) is implemented in SABER® to extract the diode parameters *TT*, *TM*, and *TSW* over temperature. The parameters are varied until the simulated results produce the same time constants and reverse peaks as the measured results seen in Figure 2.8. Table 2.3 shows the extracted values for *TT*, *TM*, and *TSW*.

Table 2.3 Extracted Diode Reverse Recovery Parameters over Temperature

	30 Degree C	50 Degree C	75 Degree C	100 Degree C
TT	165n	190n	235n	300n
TSW	130n	130n	130n	130n
TM	20n	20n	20n	20n

The diode parameter, *TT*, shows temperature dependence. The other parameters *TSW* and *TM* did not show a significant change over temperature and are left constant. While these parameters do vary over temperature, there is not a significant change that would affect

the simulation from a system point of view. The temperature dependence of *TT* is known to be the following [16]:

$$TT(T) = TT(T_{nom}) \cdot \left(\frac{T}{T_{nom}} \right)^{\beta} \tag{2.10}$$

Using the parameters in Table 2.3, β in (4.10) was calculated to be 1.71.

Figure 2.9 shows the simulated results of the diode reverse recovery over temperature using the parameters extracted above.

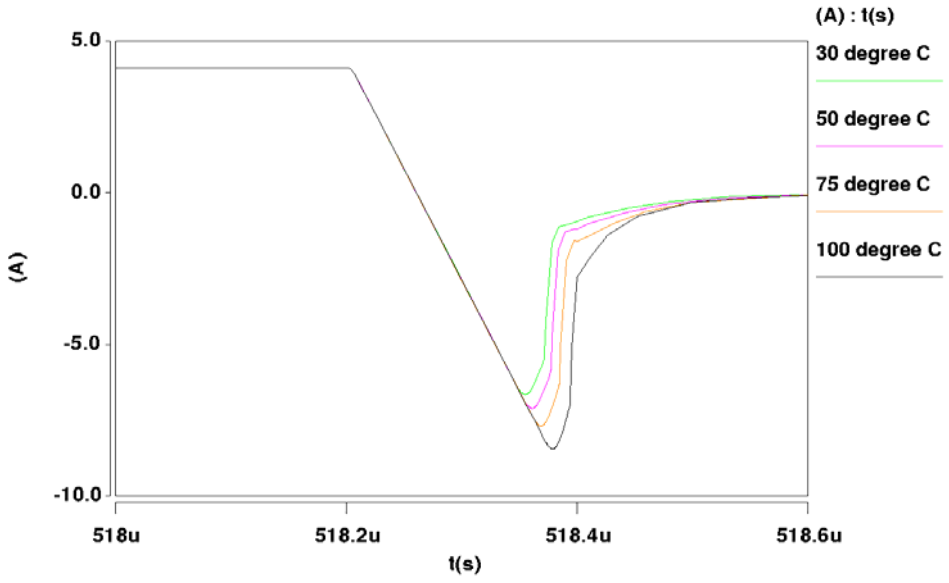


Figure 2.9. Simulated Reverse Recovery of Diode.

Figures 2.8 and 2.9 both show that the peak reverse recovery increases in magnitude with temperature. This will lead to greater losses in the inverter simulation as temperature increases because the IGBT will have to support a larger current at turn on along with the bus voltage. This is because lifetime increases with temperature. Therefore more charge is present in the base region and needs a greater amount of reverse current to remove all

the charge. The time constants and reverse current peaks of the simulated results do not match exactly the same with measured. Not enough temperature points were taken to accurately describe the temperature dependence. The reverse current peaks trends and time constants are still very close.

2.3 IGBT Model

The electrical parameters for the IGBT model, developed by Hefner for the SABER® simulator, are described in this section. Figure 2.10 shows one-half of the symmetric IGBT cell consisting of the MOSFET and bipolar equivalent circuit components [2].

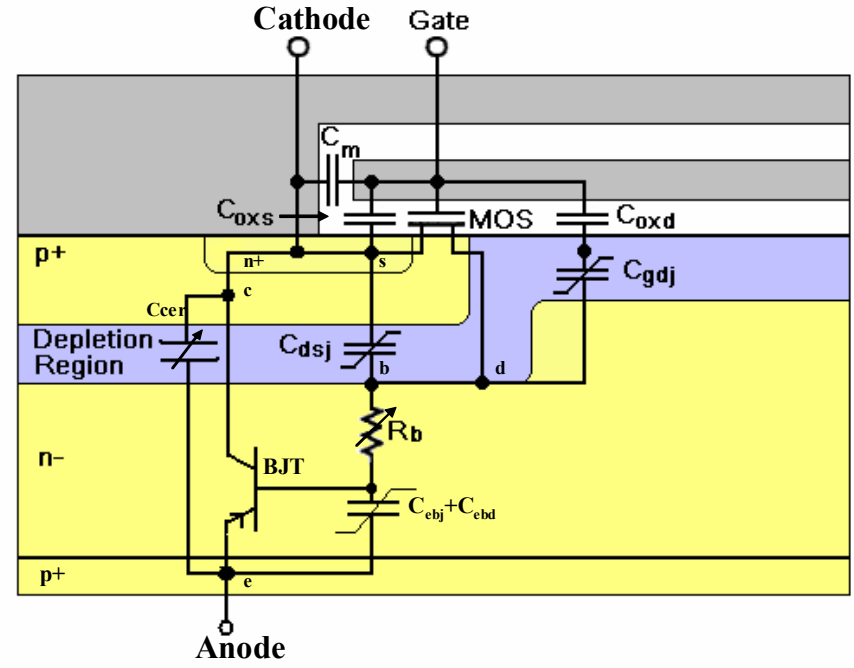


Figure 2.10. IGBT equivalent circuit model superimposed on one half of the symmetric IGBT cell [2].

In Figure 2.10, MOS represents the MOSFET channel, *Rb* is the undepleted base or drift region resistance, *Cdsj* is the non-linear drain-source junction capacitance, *Cgdj* is

the non-linear gate-drain overlap depletion capacitance, *Coxd* is the constant gate-drain overlap oxide capacitance, *Coxs* is the constant gate-source overlap oxide capacitance, and *Cm* is the constant gate-source metallization capacitance. *Cebd* is the emitter-base diffusion capacitance and *Cebj* is the Emitter-base depletion capacitance. *Ccer* is the collector-emitter redistribution capacitance. The BJT represents the equivalent pnp transistor that exists within the IGBT [2].

A positive gate bias applied will cause the p-base region underneath the gate to invert thus allowing electrons to flow from the n+ to the n-drift region. This provides the base current for the vertical P-N-P transistor in the IGBT structure. Holes are injected from the p+ region on the Anode side to the n-base region. Thus the characteristics of both the MOSFET and internal PNP transistor will determine the overall current capability of the IGBT [2].

To model a particular IGBT, an extraction sequence is needed to determine the values of all of the model parameters from electrical measurements. The extraction process divided into a sequence of steps where only a few unknown parameters are obtained at each step. This is done by selecting electrical characteristics that isolate a few unknown parameters at a time and fitting the measured data to the corresponding model equation. The parameters obtained at each step are then used as known values in subsequent steps. In general, dynamic measurements are used first to access the internal bipolar transistor. The internal MOSFET characteristics are then calculated using the bipolar current gain characterized in previous extraction steps. Table 2.4 is a list of IGBT model parameters, the electrical characteristics that are used to extract each parameter, and the name of the automated extraction program that implements the extraction step. The parameters are

listed in the order that they are extracted [4]. In the first step, the device active area is extracted by visual inspection of the chip size.

Table 2.4 Parameters, Extraction Programs and Characterisics

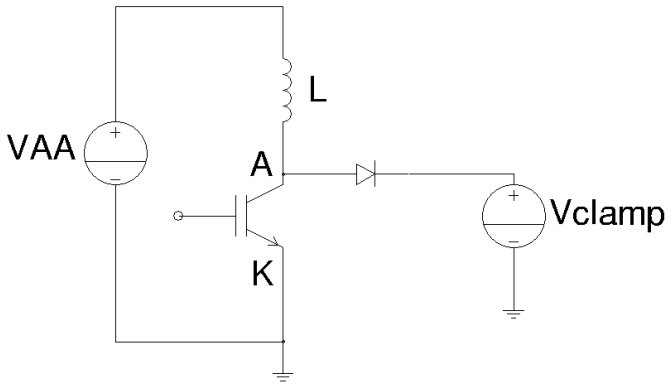
Parameter symbol	Parameter name	Program	Extraction Characteristic
A	Device active area		Chip Size
τ_{HL}	Lifetime	LFTMSR	Low V_A decay rate
I_{sne}	Emitter Electron Saturation Current	BTAMSR	Tail Size vs. Current Tail Size vs. V_A
W_B	Metallurgical base width		Tail Size vs. V_A
N_B	Base Doping concentration		
V_T	Threshold voltage	SATMSR	Saturation current vs. Vgs Saturation current vs. Vgs
$K_p = K_{psat}$	Saturation region transconductance		High saturation current vs. Vgs
θ	Transverse electric field parameter		Low saturation current vs. Vgs
K_{fl}	Low current transconductance factor		Low saturation current vs. Vgs
dV_{Tl}	Low current threshold voltage differential		
$K_{plin} = K_p \cdot K_f R_s$	Linear region transconductance parameter	LINMSR	On-state voltage vs. Vgs
N_b	Drain series resistance		On-state voltage vs. Vgs
	Drift region dopant density		On-state voltage vs. Vgs
$C_{gs}C_{oxd}$	Gate-source capacitance	CAPMSR	Gate charge at low gate voltage
A_{gd}	Gate-drain overlap oxide capacitance Gate-drain overlap area		Gate charge at high gate voltage
V_{Td}	Gate-drain overlap depletion threshold		Gate-drain charge Gate-drain charge

2.3.1 LFTMSR

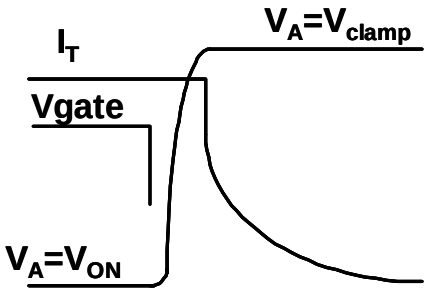
To extract the minority carrier lifetime parameters, τ_{HL} and $I_{K,\tau}$ in (4.10), the turn off tail current for a constant voltage condition is first measured and transferred to the appropriate software. The exponential current decay rate versus current of the data is fitted to the model equation for constant voltage current decay [4].

$$\frac{d\ln I_T}{dt} \equiv \frac{dI_T}{I_T} = -\frac{1}{\tau_{HL}}\left(1+\frac{I_T}{I_{k,\tau}}\right) \tag{2.11}$$

The anode turnoff current, I_T, waveform is generated using a clamped large inductive load. This circuit is ideal because it simulates an actual power switching interval for the device where a constant voltage/current condition exists at turn-off. The power dissipation during turn off of the IGBT is directly related to the minority carrier lifetime. The lifetime determines how fast the minority carriers in the IGBT base region, n- in Figure 2.10, can be removed.



(a)



(b)

Figure 2.11. Clamped Inductive Load Test Circuit (a), IGBT Anode voltage and Current at turn off (b) [4].

A large inductor is used because it results in a large current tail and maintains a constant current. Figure 2.11(a-b) shows the test circuit along with the appropriate Anode voltage and Anode current generated at turn off. Initially, the IGBT is turned on and the inductor is charge up to an appropriate load current, I_T, seen in Figure 2.11 (b). When the gate voltage is turned off, the Anode voltage rises to the clamp voltage. The diode then clamps the anode voltage to the clamp voltage and the constant current from the inductor is maintained in the diode. When the clamp voltage is reached, the anode

current of the IGBT initially drops very rapidly due the majority carrier MOS channel being removed. The remainder of the current, minority carriers in the IGBT base-region, tails off slowly, where the time constant of this decay is given by (4.10).

The IMPACT program to measure the tail current is called LFTMSR. First the tail current is captured from the scope and transferred to the software. Figure 2.12 shows the user interface panel used by the LFTMSR program. Note that we are not using a buffer layer device. The top of the panel shows the measured turn off tail captured from the scope and transferred to the LFTMSR program. The bottom panel shows the resulting current decay rate data versus current (green) obtained from the left hand side of (4.10). The number of points used in the numerical derivative calculation is specified by the user. The red curve in the bottom panel shows the least squares fit of the data to the equation on the right hand side of (4.10) where the values of τ_{HL} and $I_{K,\tau}$ calculated from the fit are displayed in the numerical display boxes. The zero current intercept is equal to $1/\tau_{HL}$ and the slope is used to extract $I_{K,\tau}$. The *Imaxlim* and *Iminlim* are needed to eliminate the high and low current effects not described in (4.10) [4].

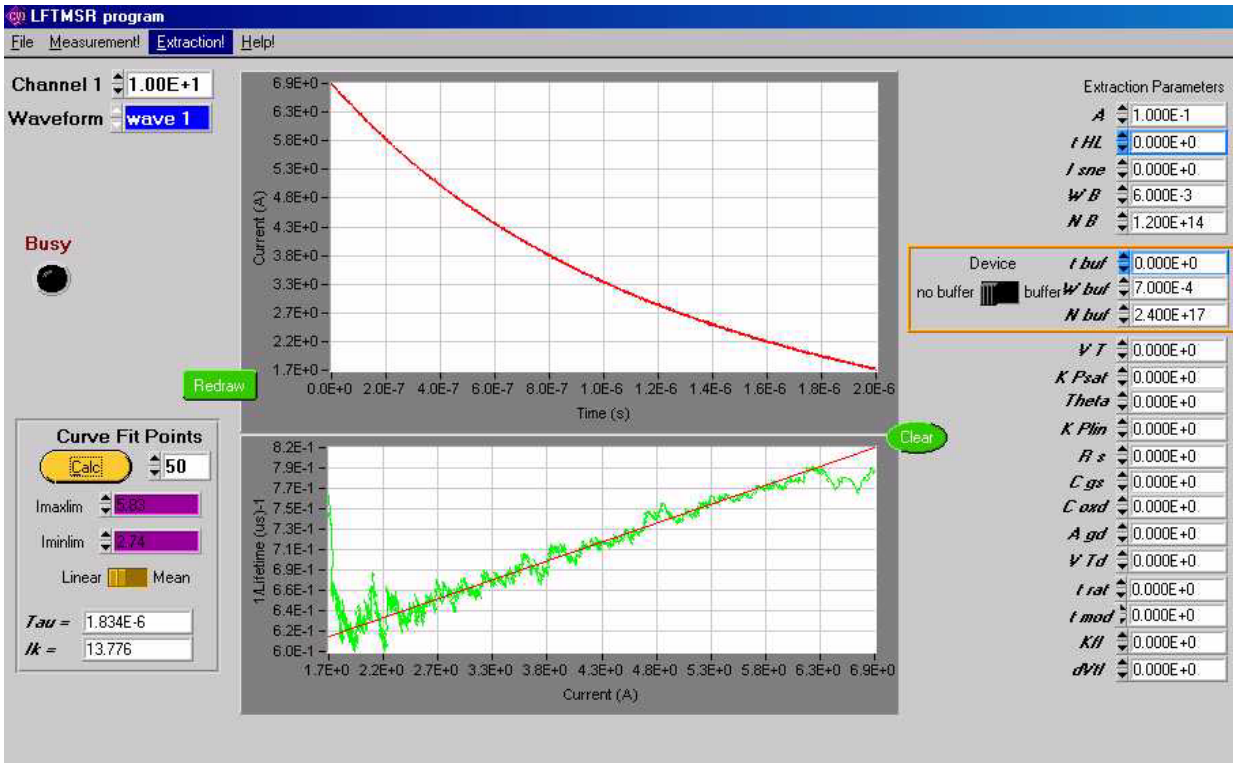


Figure 2.12. LFTMSR user interface [4].

The lifetime parameter, τ_{HL}, is a function of temperature. Therefore this parameter needs to be extracted over temperature and its temperature dependent parameter needs to be calculated from the following equation [3]:

$$\tau_{HL}(T_j) = \tau_{HLO}\left(\frac{T_j}{T_o}\right)^{\tau_{HL1}} \tag{2.12}$$

The resulting lifetime parameters and temperature dependence fit is shown in Figure2.13.

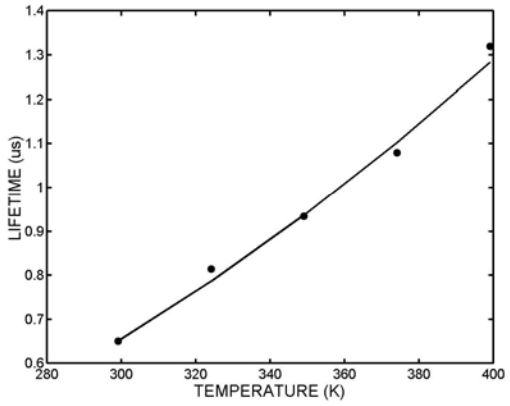


Figure 2.13. Lifetime vs. Temperature.

It can be seen in Figure 2.13 that lifetime increases with temperature and this will result in a larger current tail during turn off thus increasing the switching turn off loss.

2.3.2 BTAMSR

The relative size of the turn-off current tail versus anode current and anode voltage is used to extract the emitter electron saturation current *Isne*, the metallurgical base width *Wb*, and the base doping concentration *Nb*. The extraction software determines the relative size of the tail by using the following equations [4]:

$$\beta_{tr,V} = \frac{I_T(0^+)}{I_T(0^-) - I_T(0^+)}\Big|_{VA=cons\tan t} = \beta^{\max}{}_{tr,V}\left(1 + \frac{I_T(0^+)}{I_k}\right)^{-1} \qquad (2.13)$$

where

$$\beta^{\max}{}_{tr,V} = \left(\left(\frac{W}{L}\right)^2 \frac{\coth(\frac{W}{L})}{2\tanh(\frac{W}{2L})} - 1 \right)^{-1} \tag{2.14}$$

and

$$I_{sne} \equiv \frac{\tanh^2(\frac{W}{2L})}{(\frac{W}{L})^4} \left(\frac{(4qn_i AD_p)^2}{L^2(1+\frac{1}{b})} \right) \cdot \frac{1}{\beta^{\max}{}_{tr,V} I_k} \tag{2.15}$$

First the BTAMSR program plots the tail current waveform and determines the initial current $I_T(0+)$ and the initial current drop off magnitude $I_T(0-)$. This information is used to build the β_{tr} versus tail current relationship to extract I_{sne}, W, and $b^{max}{}_{tr}$ using the equations (4.12-4.14). Figure 2.14 shows the user interface of the BTAMSR program. The top panel shows the measured tail current for two different initial currents, $I_T(0+)$. β_{tr} is then determined and the inverse is plotted versus initial tail currents $I_T(0+)$ seen in the bottom panel of Figure 2.14. A least squares fit is performed on the bottom curve to extract $b^{max}{}_{tr}$ and I_{sne}. The slope of the bottom curve is $1/(I_k\, b^{max}{}_{tr})$ with a zero current intercept of $1/ b^{max}{}_{tr}$. The slope is used with (4.14) to calculate I_{sne} [4].

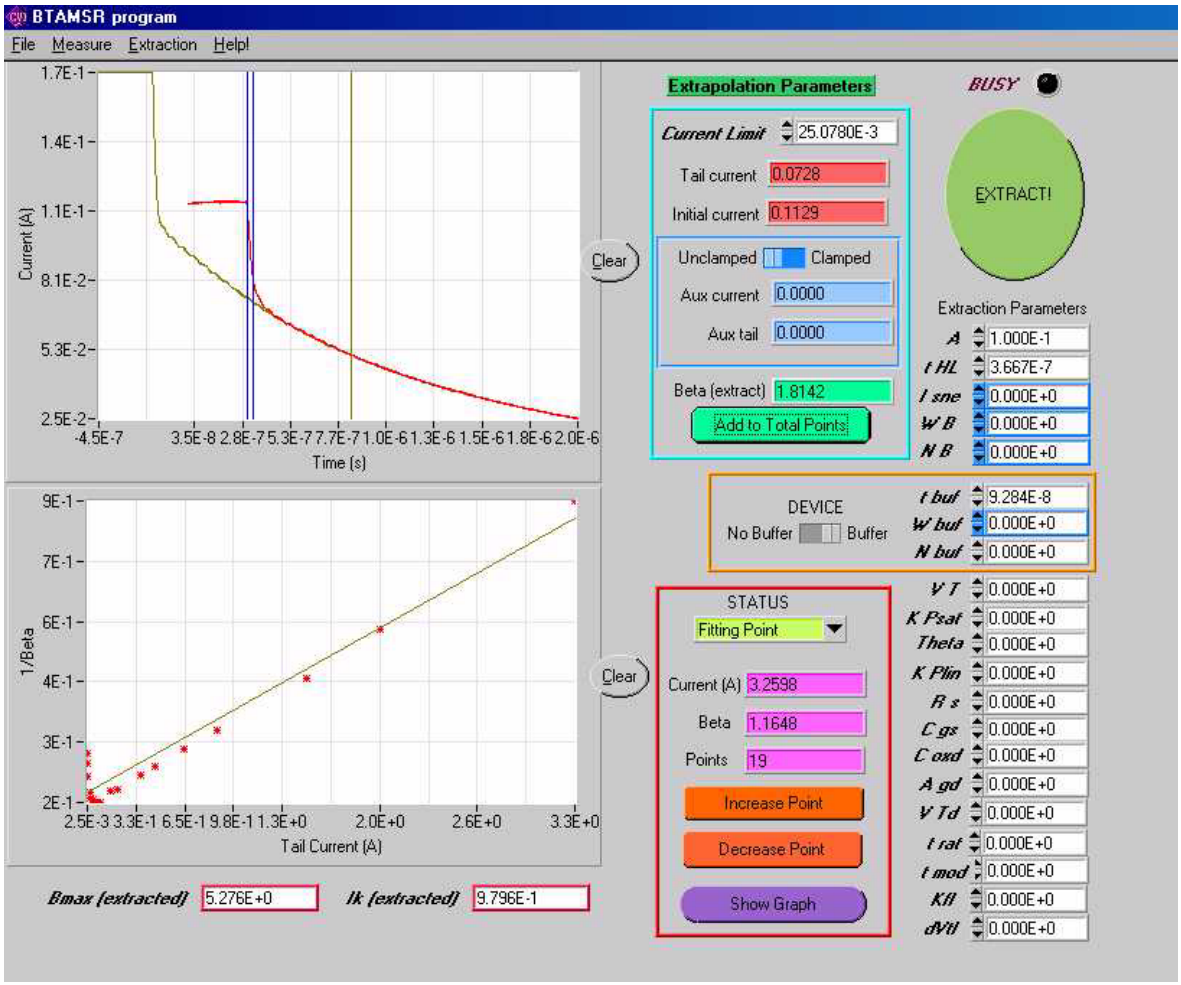


Figure 2.14. BTAMSR user interface [4].

Figure 2.15 shows the BTAMSR sub-panel to extract W_B and N_B.

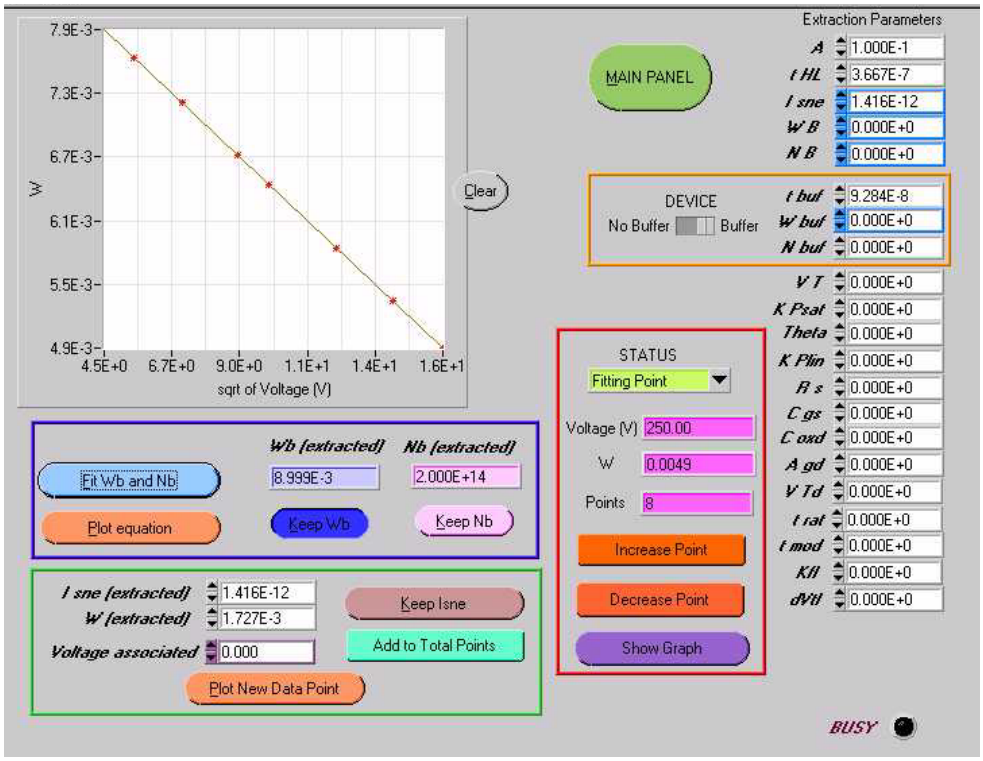


Figure 2.15. BTAMSR sub panel to calculate WB and NB [4].

The emitter electron saturation current is also a function of temperature and is given as follows [3].

$$I_{sne}(T_j) = \frac{I_{sneo}\left(\frac{T_j}{T_o}\right)^{I_{sne1}}}{\exp\left(14000(1/T_j - 1/T_o)\right)} \tag{2.16}$$

The results obtained by BTAMSR turned out to be bad data. Assumptions had to be made according to the data sheet parameters. Future work would include a more in depth parameter extraction for I_{sne}.

2.3.3 SATMSR

The saturation current versus gate voltage is used to extract the internal MOSFET transconductance parameters for the saturation region K_{psat}, the high current region θ, the low current region K_{fl} and d_{VTl}, and the threshold voltage V_T. To perform the extraction, the IGBT saturation current is measured versus gate voltage and divided by the current gain of the internal bipolar transistor (calculated using the parameters obtained by the previous two extraction programs) to obtain the internal MOSFET saturation current $I^{sat}{}_{mos}$. The value of the square root of $I^{sat}{}_{mos}$ versus gate voltage is then used to extract the parameters of the internal MOSFET [4].

Figure 2.16 shows the user interface for the SATMSR program. The upper curve shows the saturation current versus gate voltage obtained from the TEKTRONIX curve tracer. The internal transistor gain is calculated first and then the MOSFET saturation current is extracted using the following relationship [4].

$$I^{sat}{}_{moss} = I^{sat}{}_{T}(1+\beta_{ss}) \tag{2.17}$$

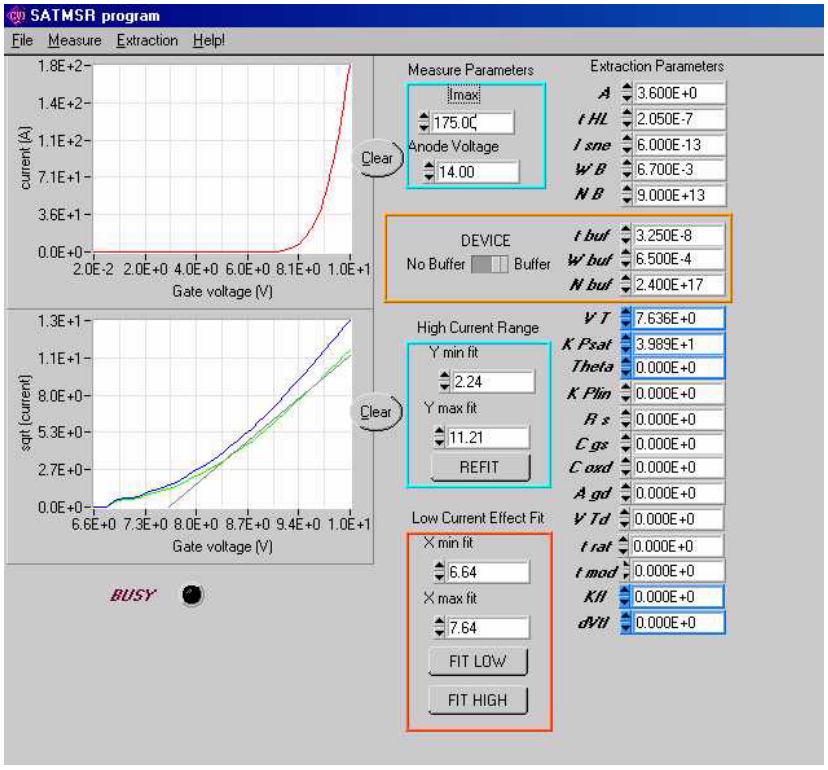


Figure 2.16. User interface for SATMSR [4].

The square root of $I^{sat}{}_{mos}$ and $I^{sat}{}_{T}$ are plotted in the bottom curve (green and blue curves respectively) of Figure2.16.

A least squares fit is then performed on the following equation to extract V_T and K_{Psat} [4].

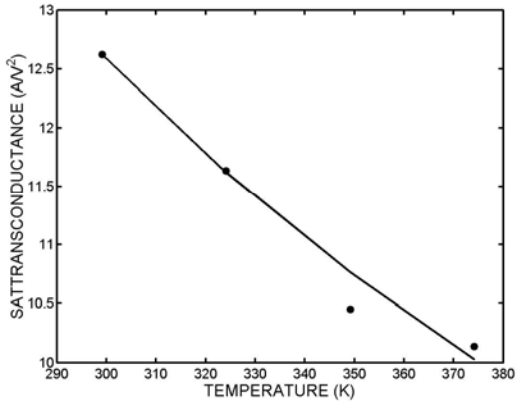
$$\sqrt{I_{mos-sat}} = \sqrt{\frac{K_{psat}}{2}}(V_{gs} - V_T) \tag{2.18}$$

The saturation transconductance, K_{psat} , and threshold voltage V_T is a function of temperature and given by [3]:

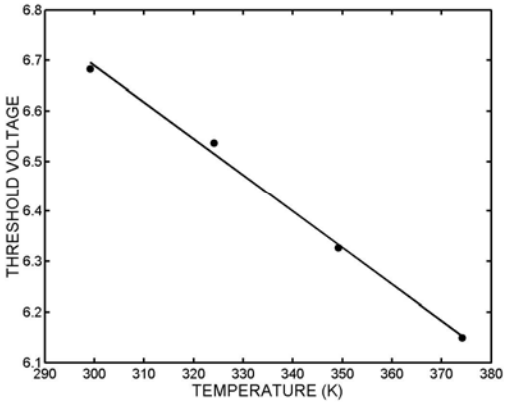
$$K_{psat}(T_j) = K_{posat}(T_o / T_j)^{K_{p1sat}} \tag{2.19}$$

$$V_T(T_j) = V_{TO} + V_{T1}(T_j - T_o) \tag{2.20}$$

Figure 2.17(a,b) shows the extracted values for K_{psat} and V_T over temperature.



(a)



(b)

Figure 2.17. Saturation Transconductance (a), Threshold Voltage (b) vs. Temperature

Once again, as was the case with the diode, the low and high current effects of the device are not modeled in this work. Again from a system level simulation stand point, these effects are not important. The parameters that model the low and high current effects, the high current region θ, the low current region K_{fl} and d_{VTl}, are saved for future work.

2.3.4 LINMSR

The linear region on-state voltage versus gate voltage for a constant anode current is used to extract the linear region transconductance K_{plin} [4].

Figure 2.18 shows the user panel for the LINMSR program. The curve generated in the top of the panel is the anode voltage versus gate voltage pairs that result in constant current. The bottom curve shows a least squares fit to the parameter equation describing the linear region of the device [4].

$$V_{on} = V_r + \frac{I_T}{K_{plin}\left(V_{gs} - V_T\right)} \tag{2.21}$$

where,

$$V_r = (R_b + R_s)I_d + \frac{I_d\theta}{K_{plin}} \tag{2.22}$$

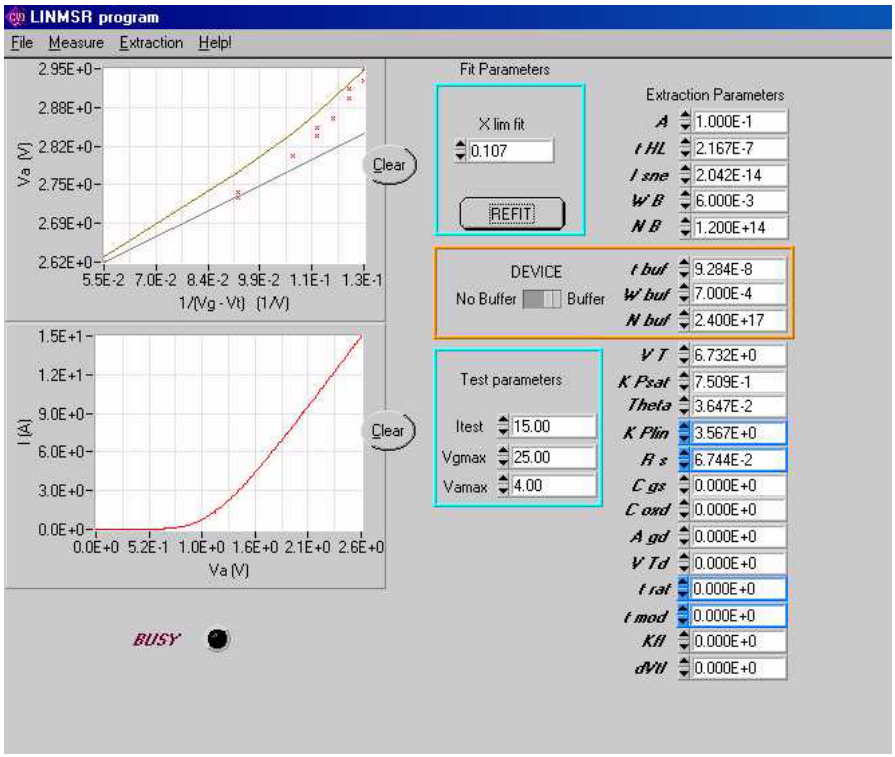


Figure 2.18. LINMSR user interface [4].

The slope of the linear fit determines K_{plin} and the intercept determines V_r.

The temperature dependence for K_{plin} is given by [3]:

$$K_{plin}(T_j) = K_{polin}(T_o / T_j)^{K_{p1lin}} \tag{2.23}$$

Figure 2.19 shows the measured values for K_{plin} over temperature.

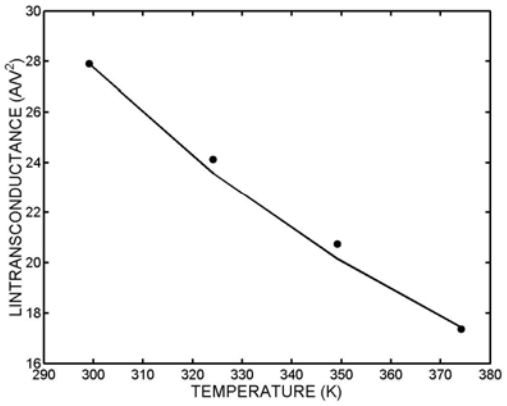
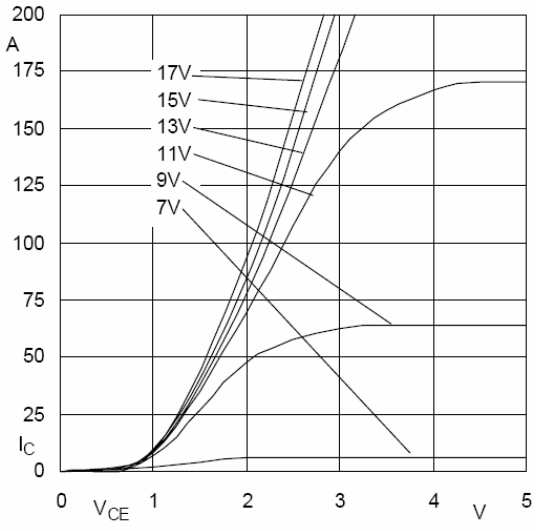
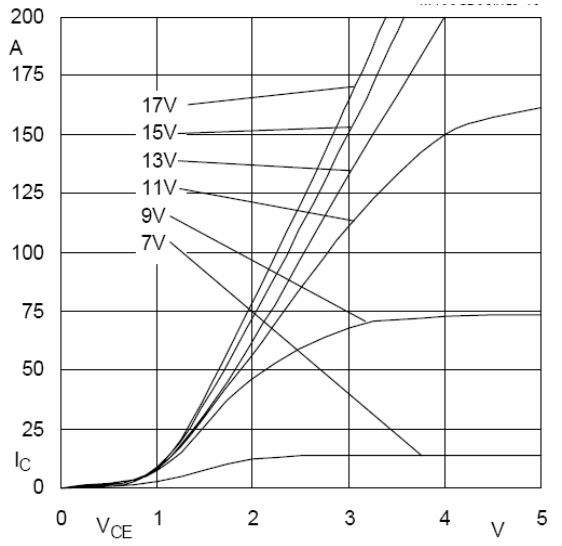


Figure 2.19. Linear Transconductance vs. Temperature.

Figure 2.20 (a and b) show the forward I-V curves given from the module datasheet [26] at both 25 and 125 degree C. Figure 2.21 shows the simulated forward I-V curves at 25 and 125 degree C.



(a) 25 degree C



(b) 125 degree C

Figure 2.20 Forward I-V curves for IGBT (a) 25 degree C, (b) 125 degree C [26]

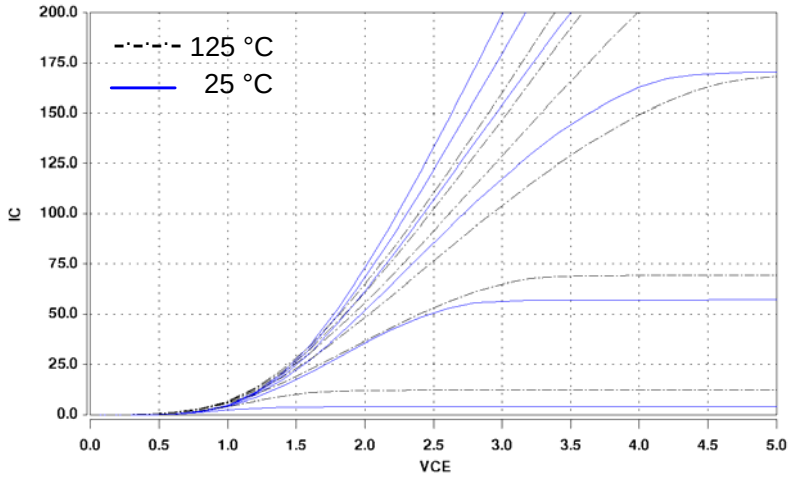


Figure 2.21 Simulated forward I-V curves for IGBT at 25 and 125 degree C

2.3.5 CAPMSR

To begin the extraction of the transient parameters, the gate charge characteristics are captured on the oscilloscope. The gate charge characteristics are acquired by applying a constant gate current to the gate of the IGBT. These waveforms are shown in the top graph of the front panel for the CAPMSR program, illustrated in Figure 2.22. This program uses the gate- and gate-drain charge characteristics including the effects of negative gate voltage inversion of the gate-drain overlap region to extract the gate-source capacitance *Cgs*, the gate-drain overlap oxide capacitance *Coxd*, the gate-drain overlap area *Agd*, and the gate-drain overlap depletion threshold *VTd* [4].

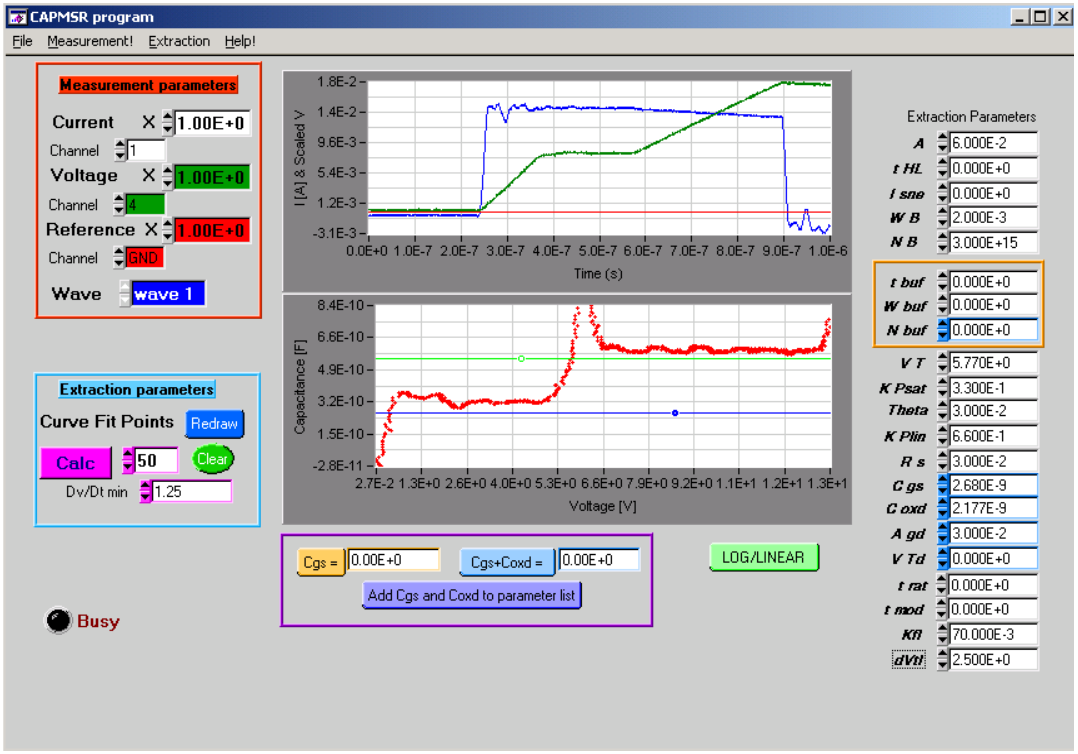


Figure 2.22. CAPMSR user interface [4].

The first step in the extraction involves the extraction equation:

$$C(V) = \frac{I}{dV/dt} \tag{2.24}$$

Using equation (4.21), the program calculates C(V) vs. voltage curve, as shown in the bottom graph on the front panel in Figure 2.22. The user controls the minimum value of *dV/dt* and the number of derivative points for each calculation. The values of *Cgs* and *Coxd* are determined from *Ig* and *dVgs/dt* during the positive voltage portion of gate charge curve. For positive values of gate voltage, there are essentially three distinct phases in the gate voltage waveform. During the first phase, *Vgs* rises with a constant slope as the constant gate current charges the constant gate-source capacitance *Cgs*. Therefore, it is during this portion of the gate voltage waveform that *Cgs* is extracted by dividing the digitized values of the gate current waveform by the time rate-of-change of the digitized gate voltage waveform [4].

During the second phase or plateau region of the gate voltage waveform, *Vgs* remains relatively constant, and *Vd* falls as the gate current charges the two-phase, voltage dependent gate-drain capacitance *Cgd*. Therefore, the voltage dependence of the gate drain depletion capacitance is obtained by dividing the digitized values of the gate current waveform by the time rate-of-change of the gate-drain voltage computed from the digitized values of gate and anode voltage waveforms [4].

During the third phase of the gate voltage waveform, *Vd* remains relatively constant, and *Vgs* rises as the gate current charges the sum of the gate-drain overlap oxide

capacitance *Coxd* and the gate source capacitance *Cgs*. Now, it is possible to extract *Coxd* from the previously extracted value of *Cgs* in the first phase [4].

In the bottom graph of Figure 2.22, the cursors are placed on the flat portions of the numerically calculated capacitance versus voltage curve that corresponds to the section of the gate voltage waveform that is due to *Cgs* and that due to *Cgs* and *Coxd*, as explained above [4].

2.4 Summary

Electrical parameters for both temperature and non temperature dependent were extracted for both the IGBT and diode. High and low current effects were neglected as they do not need to be modeled for the system level simulation. Table 2.5 shows a summary of the parameters that were extracted and used in the model.

Table 2.5 Electro-thermal parameters for IGBT and diode

IGBT Electrical Parameters	**Description**
A = $1cm^2$	IGBT chip Area
I_{sneo} = 1.5 x 10^{-12} A	Emitter electron Saturation Current
W_b = .015 cm	Metallurgical drift region width
V_{TO} = 6.4 V	MOSFET channel threshold voltage
N_b = 1.5 x $10^{14}cm^{-3}$	Base dopant density
K_{plino} = 23 A/V^2	Linear region transconductance
K_{psato} = 11.5 A/V^2	Saturation region transconductance
τ_{HLO} = .651 μs	High level minority carrier lifetime
C_{gs} = 3.98 nF	Gate-source capacitance
C_{oxd} = 15.1 nF	Gate-drain overlap oxide capacitance
IGBT thermal Dependent Coefficients	**Description**
τ_{HL1} = 2.365	High Level minority carrier lifetime temp. coeff.
I_{sne1} = 1.189	Emitter electron saturation current temp. coeff
V_{T1} = -7.2mV/K	MOSFET channel threshold voltage temp. coeff.
K_{plin1} = 1.0286	Linear region transconductance temp. coeff
K_{psat1} = 2.1032	Saturation region transconductance temp. coeff.
Diode Electrical Parameters	**Description**
ISL = 1.25 mA	Saturation current for low level recombination
NL = 3.89	Emission coefficient for low level injection
BV = 600 V	Breakdown voltage
C_{JO} = 3 nF	Zero-bias junction capacitance
TSW = 130 ns	Charge Sweep out time
TT = 165 ns	Carrier Lifetime
Diode thermal Dependent Coefficients	**Description**
X_{TI} = -2.36	ISL temperature exponent
T_{NL1} = -6.35 x 10^{-4}	Linear NL temperature coefficient
T_{NL2} = -4.14 x 10^{-6}	Quadratic NL temperature coefficient
BETA = 1.71	Temperature exp. of carrier lifetime TT
BETASW = 1 x10^6	Temperature exp. of carrier lifetime TSW

Chapter 3. Six-Pack IGBT thermal model methodology

3.1 Introduction

A fully coupled thermal model for a six-pack IGBT power module containing IGBTs and anti-parallel diodes is presented in this chapter. The heat flow through the silicon chip, module package and base-plate for a six-pack IGBT is fully described with lateral heat coupling effects.

The temperature at various positions within the silicon chips, module package, and base-plate are defined to be simulator system variables so that the temperature distribution is solved for by the simulator in the same manner as the simulator solves the node voltages of the electrical network. The equations describing the heat flow between the internal thermal nodes and the heat storage at the thermal nodes are obtained by discretizing the nonlinear heat diffusion equation. In the discretization process, a grid spacing that increases logarithmically with distance from the heat source is used to maximize computation efficiency and to accurately represent the dynamic temperature distribution for the applicable range of heating rates [3].

The three dimensional heat-flow is accounted for using symmetry in the discretization of the heat equation for each region of the component. The silicon chip thermal model is based upon the one dimensional heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The package and base-plate model describes the two

dimensional lateral heat spreading and the heat capacity of the periphery of the package by using the effective heat flow area approach [3]. Lateral heat coupling must be described between all IGBTs and diodes.

3.2 Heat Diffusion Equation

To derive the non linear heat diffusion equation we start with Figure 3.1. The following discussion is based upon the equations given in [9]. Two different temperatures, *T1* and *T2*, result in the heat flow represented by Q_z in the vertical *z* direction. This change in temperature over the distance d_z results in a temperature gradient.

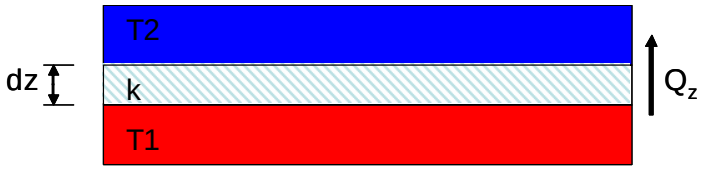


Figure 3.1 Thermal Gradient illustration

The following equation describes the one-dimensional temperature gradient that exists in Figure 3.1:

$$Q_z(z) = -k\frac{\partial T(z)}{\partial z} \tag{3.1}$$

where k is the thermal conductivity of the material that the heat passes through and Q_z is the amount of heat crossing a unit area, A, of a plane (in the z direction normal to the plane) per unit time.

If we let q_z represent the amount of heat energy per unit volume, we can describe the increase per unit time in the amount of heat energy contained in a slab of material with thickness dz seen in Figure 3.1.

$$\frac{\partial}{\partial t}(q_z A dz) = AQ_z(z) - AQ_z(z+dz) \tag{3.2}$$

Expanding on (3.2)

$$\frac{\partial}{\partial t}(q_z dz) = Q_z(z) - [Q_z(z) + \frac{\partial Q_z(z)}{\partial z} dz] \tag{3.3}$$

$$\frac{\partial q_z}{\partial t} = -\frac{\partial Q_z(z)}{\partial z} \tag{3.4}$$

Substituting (3.1) into (3.4)

$$\frac{\partial q_z}{\partial t} = k\frac{\partial^2 T(z)}{\partial z^2} \tag{3.5}$$

Equation (3.5) also can be written as:

$$A\rho c\frac{\partial T}{\partial t} = Ak\frac{\partial^2 T(z)}{\partial z^2} \tag{3.5}$$

Equation (3.5) is known as the heat diffusion equation where ρ is the density of the material with units g/cm^3 and c is the specific heat of the material with units J/gK. It should be noted that the heat diffusion equation describes the temperature gradient in

all three dimensions of the rectangular coordinate plane (x,y,z). Here we assume y and x axis symmetry and the equation simplifies to a one dimensional heat flow in the z direction.

If we use enough finite points (thermal nodes, z_i, in the thermal network) to describe the z axis, we can discretize the heat diffusion equation into a finite number of first order ordinary time-dependent differential equations. This is done by integrating the heat diffusion equation across the thermal element (a and b) in Figure 3.2 and applying finite differences to evaluate the spatial derivatives [3]. Integrating the heat diffusion equation across the elements a and b in Figure3.2:

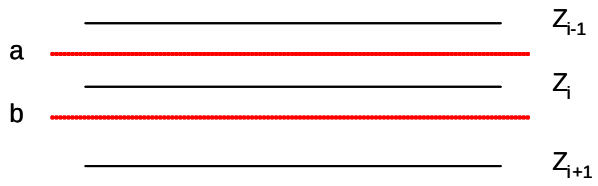


Figure 3.2. Discretization of the heat diffusion equation.

$$\int_a^b Ak\frac{\partial^2 T(z)}{\partial z^2}dz = \int_a^b A\rho c\frac{\partial T(z)}{\partial t}dz \tag{3.6}$$

where a and b are

$$a = \frac{z_{i-1}+z_i}{2}, b = \frac{z_i+z_{i+1}}{2} \tag{3.7}$$

The integration results in

$$Ak[\frac{\partial T(z)}{\partial t}\Big|_b - \frac{\partial T(z)}{\partial t}\Big|_a] = A\rho c[b-a]\frac{\partial T}{\partial t} \tag{3.8}$$

Using the central difference finite formula for approximating first order derivatives [17], (3.8) can be further written as:

$$Ak[\frac{T_{i+1}-T_i}{z_{i+1}-z_i}-\frac{T_i-T_{i-1}}{z_i-z_{i-1}}]=A\rho c[\frac{z_i+z_{i+1}}{2}-\frac{z_{i-1}+z_i}{2}]\frac{\partial T}{\partial t} \tag{3.9}$$

Simplifying (3.9):

$$Ak\frac{T_{i+1}-T_i}{z_{i+1}-z_i}-Ak\frac{T_i-T_{i-1}}{z_i-z_{i-1}}=A\rho c[\frac{z_{i+1}-z_{i-1}}{2}]\frac{\partial T}{\partial t} \tag{3.10}$$

If we let

$$R_{i,i+1}=\frac{z_{i+1}-z_i}{Ak_{i,i+1}} \tag{3.11}$$

$$C_i=A\rho c\left(\frac{z_{i+1}-z_{i-1}}{2}\right) \tag{3.12}$$

$$H_i=C_i\bullet T_i \tag{3.13}$$

(3.10) can now be written as

$$\frac{T_{i+1}-T_i}{R_{i,i+1}}-\frac{T_i-T_{i-1}}{R_{i-1,i}}=\frac{dH_i}{dt} \tag{3.14}$$

Equation (3.14) has the same structure as the equation a circuit simulator would use to solve a simple R-C circuit with voltages and currents at an electrical node. Therefore, the solution to the R-C electrical circuit will be the same as the solution to (3.14) and we can use an R-C network to model the thermal heat flow. In the thermal network, H represents the heat energy at a thermal node z_i and R represents the thermal resistance between nodes. The through variable becomes power and the

across variable becomes temperature. The powers are summed at a specific thermal node z_i and are equal to the derivative of the heat energy [3]. Table 3.1 summarizes the analogy between electrical and thermal circuits.

In the discretization process of (3.5), it is assumed that the temperature gradient and thermal conductivity do not vary substantially between adjacent grid points. Therefore, the accuracy of the thermal component model is determined by the number and locations of the thermal nodes within the component. For high power dissipation levels during short periods of time (e.g. transients), the silicon chip surface temperature rises faster than the heat diffuses into the chip, and a high density of thermal nodes is required at the silicon chip surface. However, the thermal gradients disperse as the heat diffuses through the chip, so a grid space that increases logarithmically with distance from the heat source (silicon chip surface) results in the minimum number of thermal nodes is required to describe the temperature distribution for the range of applicable power dissipation levels [3].

Table 3.1 Electrical to thermal analogies

Electrical		Thermal	
Parameter	Units	Parameter	Units
Voltage	V	Temperature	K
Current	$A = \frac{C}{s}$	Heat Flow	$W = \frac{J}{s}$
Conductivity σ	$\frac{A}{V \times cm}$	Conductivity k	$\frac{W}{K \times cm}$
Stored Charge	C	Stored Heat	J
Electrical resistance	$\frac{V}{A}$	Thermal resistance	$\frac{K}{W}$
Electrical Capacitance	$\frac{C}{V}$	Thermal Capacitance	$\frac{J}{K}$

3.3 Thermal model development of power module

The equations describing the thermal network discussed in this chapter are implemented in a language called MAST® [18]**.** The module modeled in this chapter is shown in Figure3.3

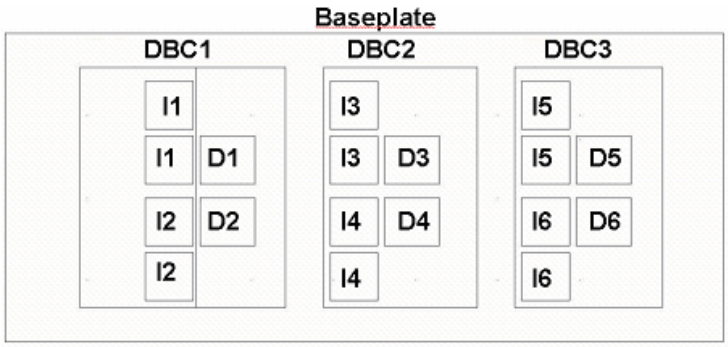


Figure 3.3. IGBT six-pack module.

There are three DBC (Direct Bonded Copper) structures mounted on one base-plate. Each DBC structure contains two IGBTs and two diodes. Each IGBT is a paralleled combination of two silicon chips. Only one silicon chip is used for each diode.

The thermal model is divided into 12 thermal networks with a thermal network designated for one device. Within each network, three sections are considered. One section is designated for the silicon chip and the others for the DBC and base-plate layer respectively. Lateral coupling between the networks is also included.

As stated before, we need to represent the heat flow in the z direction with thermal nodes z_i where we define the appropriate thermal resistances and heat capacitances at each node. Figure 3.3 shows the different layers, not drawn to scale, within the module that will contain the thermal nodes making up the thermal network.

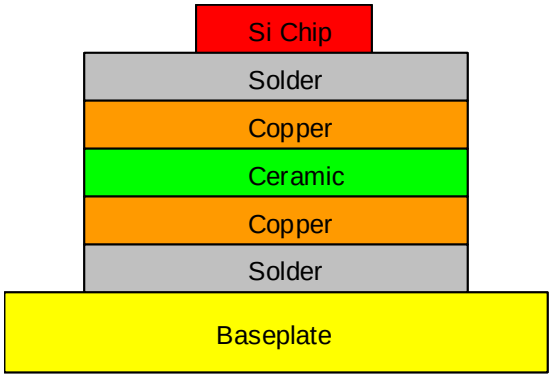


Figure 3.4. Thermal layers to be modeled by thermal network within power module.

The silicon chips that make up the IGBTs and diodes are mounted on a DBC with an insulation layer (ceramic) between the top and bottom. The DBC is mounted on a copper base-plate.

In order to accurately model the 3 dimensional heat spreading effect within the module, the effective heat flow area approach is used. The effective heat flow approach describes a heat flow area that increases with depth into the package. This is done by combining the components of heat flow area due to cylindrical heat spreading along the edges of the chip, the spherical heat spreading at the corners of the chip, and the rectangular coordinate component of heat flow directly beneath the chip [3].

Figure 3.4 shows the thermal network structure. A power source representing the power dissipated across the device feeds into an R-C network. Each capacitance represents a thermal node and a thermal resistance connects between thermal nodes. Figure 3.4 only illustrates a representation of the thermal network and does not show all the nodes or lateral coupling modeled in this work.

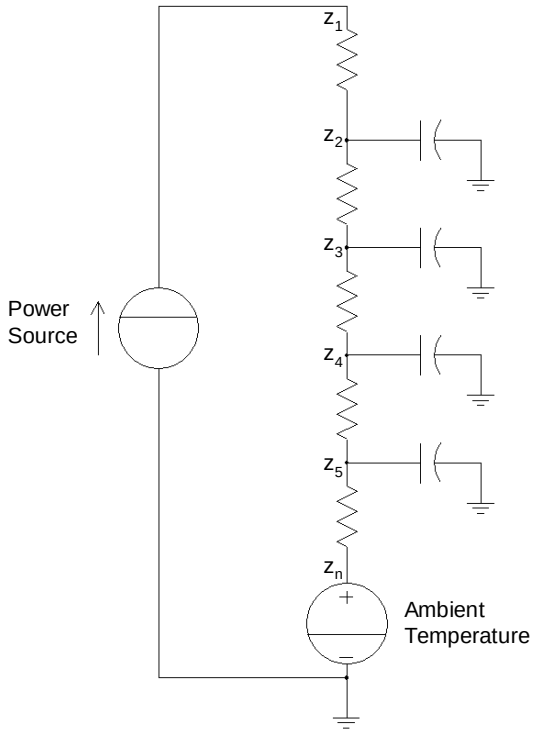


Figure 3.5. Thermal Network.

3.3.1 Silicon Chip Thermal Model

The silicon chip thermal model is based upon the rectangular heat equation (3.5) and includes the nonlinear thermal conductivity of silicon. The silicon chip model is the same model developed by Hefner and is a standard SABER® part. The chip thermal model also includes a distributed heat source option if the parameter $w_p>0$, where the power density as a function of depth into the chip z is given by (3.15). All the following equations describing the silicon chip thermal model are based upon the equations given in [3].

$$P(z,t) = \begin{pmatrix} P_T(t) \cdot \dfrac{1-\lambda_z / w_p}{1-\lambda/2}, z \le w_p \\ 0 \end{pmatrix} \tag{3.15}$$

The heat source of (3.15) is triangular if the model parameter $\lambda = 1$ corresponding to a depletion region that extends from the surface into the chip, or trapezoidal if $0 < \lambda < 1$ corresponding to a depletion region that is terminated by a high doped layer at w_p. For $\lambda = 0$, the power density is constant between 0 and w_p. The module modeled here is not a buffer layer device, thus resulting in a triangular heat source ($\lambda = 1$).

The silicon chip thermal model calculates the fraction of heat source power that is dissipated in each thermal element within the heat source f_i (i.e. fraction of power dissipated between $(z_{i-1}+z_i)/2$ and $(z_i+z_{i+1})/2$). The heat source power into each node during simulation is then calculated using the following:

$$P_{di} = P_{d1} \cdot \frac{f_i}{f_1} \tag{3.16}$$

where the power from the heat source into node 1 is given by

$$P_{d1} = \frac{(T_j - T_1)}{R_{j1}} \tag{3.17}$$

The j in the above equations indicates the top of the silicon chip designated as the chip junction.

A logarithmically spaced grid may be used by the chip thermal model to minimize the number of nodes required to accurately represent the dynamic temperature distribution for the full range of applicable power dissipation levels. To aid in the visualization of the transient temperature distribution, a quasi-logarithmically spaced

grid is used that consists of an evenly spaced grid within segments where the segment size increases logarithmically with distance from the heat source [3].

The node positions, chip area, and instantaneous node temperatures are used to evaluate the model the model functions $R_{i,i+1}$, H_i, and P_{di} that are used by the equations section of the MAST® template. The node positions, heat capacitances, and fraction of power dissipated within each element are calculated in the parameters section because they only need to be calculated once and do not depend on the simulator system variables.

3.3.2 DBC/Base-plate

Figure 3.5 shows the nodes that make up the package and base-plate thermal networks. Heat coupling is not shown in this figure.

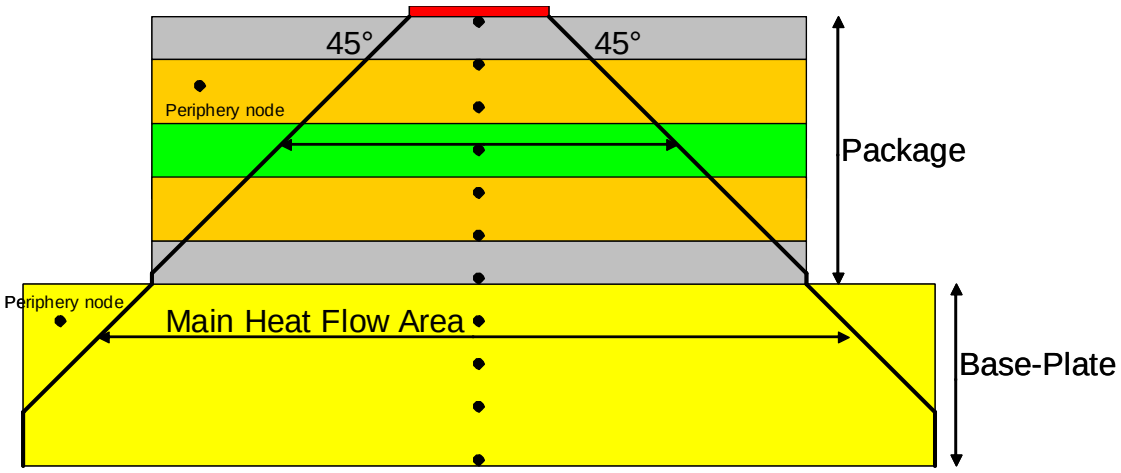


Figure 3.6. Spacing of thermal nodes within package and base-plate model.

The heat spreads from the bottom of the IGBT and Diode chip downward through the package at an assumed 45 degree angle represented by the black projected lines in Figure 3.5. The area within the interior of the two projected lines represent the effective heat flow area and everything outside represents the periphery area. The periphery area is described by one thermal node and represents the remainder of heat capacitance not accounted for in the main heat flow area of the package and base-plate. As shown in Figure 3.5, there are a total of eleven evenly spaced nodes from the bottom of the silicon chip to the bottom of the base-plate and two periphery nodes. Not shown in the figure are the thermal nodes that make up the silicon chip, but the silicon chip thermal network connects to the package and base-plate thermal networks.

Figure 3.5 illustrates also that the heat cannot spread laterally beyond the edges of the DBC or base-plate. The radius, (*rxpci, rxmci, rypci, rymci, rbtci, rxpdi, rxmdi, rypdi, rymdi, rbtdi*) shown in Figure 3.6, that the heat spreads at each node z_i is limited by the distance from each edge of the chip to the edges of the DBC, base-plate or adjacent chip. Figure 3.6 shows a detailed schematic of the radial heat boundaries of one phase of the module. The outer edges of the figure represent the edge of the DBC if we are considering the DBC thermal network or the edge of the base-plate if we are considering the base-plate thermal network.

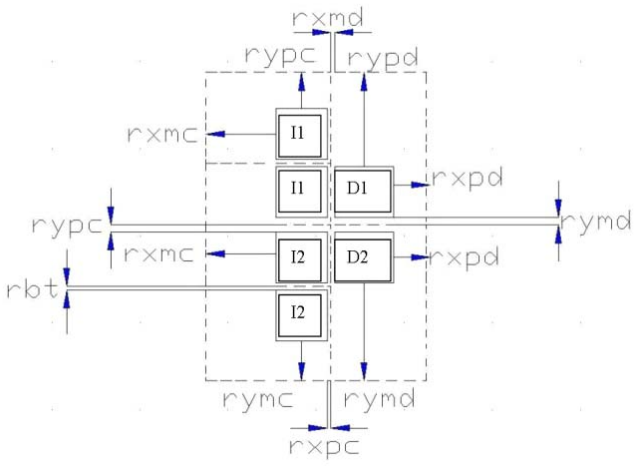


Figure 3.7.Boundary conditions for radial heat flow.

The dotted lines in Figure 3.6 indicate the radial boundary conditions between chips. The radius that the heat spreads at each node is in the same direction and limited by, for example in the positive x direction of the IGBT chip, the corresponding boundary.

$$r_{xpci} = \begin{Bmatrix} z_i \; for \; z_i \le xchedpc \\ xchedpc \; for \; z_i > xchedpc \end{Bmatrix} \tag{3.18}$$

Note also that the heat does not spread beyond the midpoint between chips.

The total effective area, A_{zi}, at each node depth is calculated from the one-quarter cylinders at each edge of the chip, one-eighth spheres at each corner of the chip where one-half of the heat spreading is assumed to be towards the package case, and the rectangular area directly beneath the chip [3].

$$A_{cylzi} = \frac{\pi}{4} L_{ch}(r_{ymci} + r_{ypci}) + 2\frac{\pi}{4} W_{ch}(r_{xmci} + r_{xpci}) + \frac{\pi}{4} L_{ch}(2r_{bti}) \tag{3.19}$$

$$A_{sphzi} = \frac{\pi}{4}(r_{ymci} + r_{ypci})(r_{xmci} + r_{xpci}) + \frac{\pi}{4}(2r_{bti})(r_{xmci} + r_{xpci}) \tag{3.20}$$

$$A_{rect} = W_{ch} L_{ch} \tag{3.21}$$

$$A_{zi} = A_{cyli} + A_{sphi} + A_{rect} \tag{3.22}$$

W_{ch} and L_{ch} represent the chip width and length respectively.

Figure 3.7 illustrates the heat flow structure assumed in the above equations.

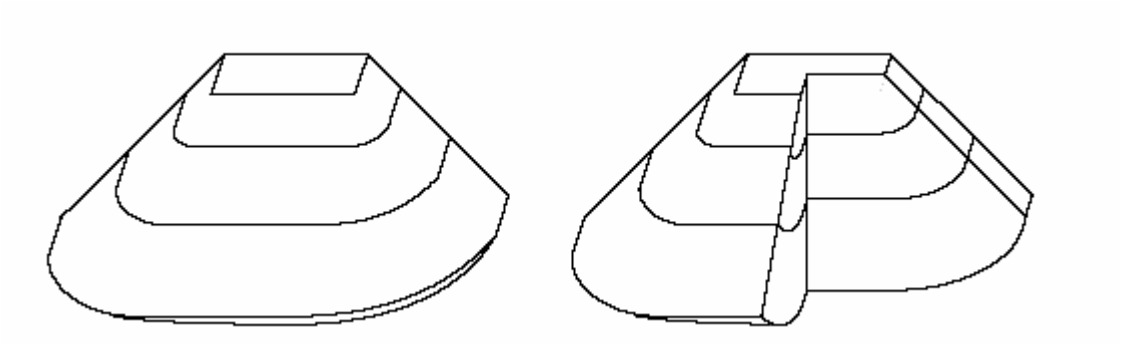


Figure 3.8. Three dimensional perspective of thermal nodes [16].

The effective areas for each of the nodes are calculated in the parameter section of the SABER® model and take in consideration the boundaries of the package. The area changes with depth into the module, and the thermal conductivity changes with the materials involved between each pair of nodes. These values are used to calculate the thermal resistance between nodes using:

$$R_{th} = \frac{d}{k_f A} \tag{3.19}$$

where R_{th} is the thermal resistance, k is the thermal conductivity, A is the average effective heat flow area between nodes, and d is the distance between nodes. Note that equation (3.19) is derived from the heat diffusion equation in rectangular coordinates (3.11). The heat flow area, A, used in (3.19) assumes the area being

composed of cylindrical and spherical components of heat flow as well as rectangular components. For (r_{i+1}-r_i<<r_i), one can find from taylor series expansion that the expressions for thermal resistance and capacitance in spherical and cylindrical coordinates are equal to the thermal resistance and capacitance in rectangular coordinates. This is true if the heat flow area used in (3.19) is replaced by the spherical and cylindrical heat flow area components. This is a reasonable approximation because the heat flow area is dominated by the rectangular area of the chip for small distances into the package and the cylindrical and spherical components of heat flow are only important for larger distance into the package where (r_{i+1}-r_i<<r_i) is satisfied [3].

Figure 3.5 shows that the volume of material between any two nodes can be composed of several materials. Therefore when calculating the thermal resistance between nodes, a fractional thermal conductivity, k_f, is calculated in the model which accounts for the different material that the heat flux may pass through between nodes. Figure 3.8 shows an example situation to calculate the thermal resistance between any two nodes in the DBC. Note that the thermal resistance between *node0* and *node1* and the thermal resistance between *node5* and *node6* describe half the distance than that of the other nodes.

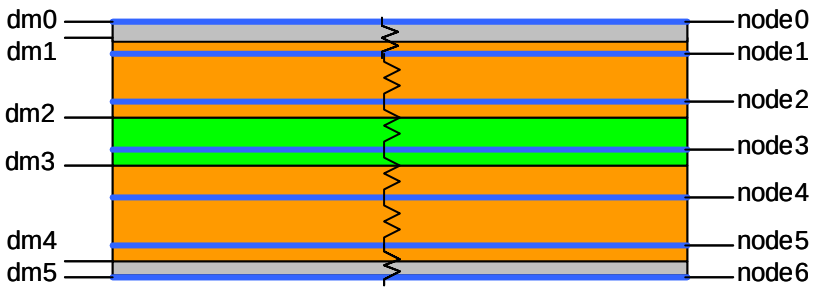


Figure 3.9. Thermal Resistance Calculation.

First, the fractional thermal conductivity, k_f, must be calculated. The following code snippet from the MAST® model shows the calculation of k_f and the thermal resistance between *node0* and *node1*, R_{01}, as an example.

```
# node1

db0=dm0
db1=dm1
db2=dm2
db3=dm3
db4=dm4
db5=dm5

    if (dm0>node1) db0=node1
    if (dm1>node1) db1=node1
    if (dm2>node1) db2=node1
    if (dm3>node1) db3=node1
    if (dm4>node1) db4=node1
    if (dm5>node1) db5=node1

    if (dm0<node0) db0=node0
    if (dm1<node0) db1=node0
    if (dm2<node0) db2=node0
```

if (dm3<node0) db3=node0
if (dm4<node0) db4=node0
if (dm5<node0) db5=node0

far1=2*(db1-db0)/depth
fbr1=2*(db2-db1)/depth
fcr1=2*(db3-db2)/depth
fdr1=2*(db4-db3)/depth
fer1=2*(db5-db4)/depth

R_{01}=depth*(far1/ka+fbr1/kb+fcr1/kc+fdr1/kd+fer1/ke)/(a0+a1)

The thermal conductivities *ka*, *kb*, *kc*, *kd*, *ke* represent the thermal conductivities of each material making up the DBC. The quantities *ah* and *a1* represent the total effective heat flow area at *node0* and *node1* respectively.

The thermal capacitance is given by

$$C_{th} = v\rho c \tag{3.20}$$

where v is the volume between nodes, ρ the density of the material between nodes, and c the specific heat of the material between nodes. The thermal capacitance is used to calculate the heat energy at each node, H_i, from (3.14). Again we must take into account that different materials will determine the total heat energy at a given node. Figure 3.9 shows how thermal capacitance is calculated. The thermal capacitance is not placed between thermal nodes, but rather between the elements that describe (3.12).

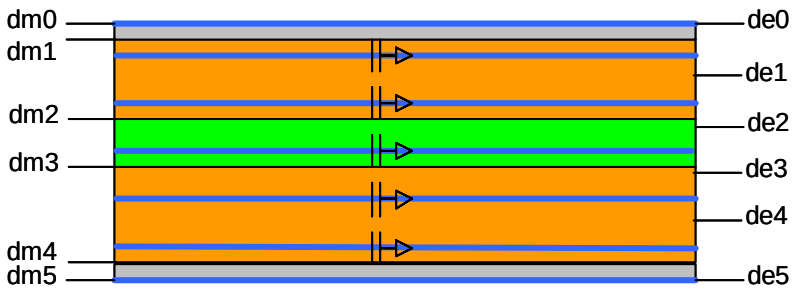


Figure 3.10. Thermal Capacitance calculation.

The following code snippet shows how the thermal capacitance is calculated within the MAST® model:

```
# node1

db0=dm0
db1=dm1
db2=dm2
db3=dm3
db4=dm4
db5=dm5

    if (dm0> de1)  db0=de1
    if (dm1> de1) db1= de1
    if (dm2> de1) db2= de1
    if (dm3> de1) db3= de1
    if (dm4> de1) db4= de1
    if (dm5> de1) db5= de1

    if (dm0<de0) db0=de0
    if (dm1< de0) db1= de0
    if (dm2< de0) db2= de0
    if (dm3< de0) db3= de0
    if (dm4< de0) db4= de0
    if (dm5< de0) db5= de0
```

far1=2*(db1-db0)/depth
fbr1=2*(db2-db1)/depth
fcr1=2*(db3-db2)/depth
fdr1=2*(db4-db3)/depth
fer1=2*(db5-db4)/depth

hca=rowa*ca
hcb=rowb*cb
hcc=rowc*cc
hcd=rowd*cd
hce=rowe*ce

c1=v1*(hca*fac1+hcb*fbc1+hcc*fcc1+hcd*fdc1+hce*fec1)

The material properties *hci*, *rowi*, *ci* describe the heat energy, density, and specific heat of material *i* respectively. The volume describes the heat volume at a given node within the effective heat flow area. All remaining heat volume is accounted for with the periphery node or coupling node.

The silicon chip, DBC and base-plate thermal networks are calculated in different MAST® templates and their corresponding thermal networks are connected within the highest level calling program shown later. Since the thermal networks are calculated separately, the heat flow area at the bottom of the silicon chip and DBC are used as the rectangular portion of heat flow at the top of the DBC and base-plate respectively.

3.3.3 Thermal Coupling Consideration

Each device contains a vertical thermal network to describe the heat flow vertically from the top of the silicon chip to the bottom of the base-plate. However, each device shares a common DBC while all the devices share a common base-plate. Therefore horizontal heat flow has to be considered between the devices through DBC and base-plate layers. The thermal model contains a DBC and base-plate coupling consideration.

Because each DBC layer contains four devices, horizontal heat flow coupling must be considered between each vertical thermal network through the DBC. A coupling resistor is placed between the case nodes of the top IGBT chip and diode. The case node is the bottom node of the DBC layer that connects to the base-plate layer. Another coupling resistor is placed between the case nodes of the top IGBT and bottom diode. Finally a resistor is placed between the case nodes of the bottom IGBT chip and diode. The resistance is calculated using (3.19) where the area represents the average heat flow area between the devices considered where the horizontal heat flow is bounded by the conditions seen in Figure 3.6. The thermal conductivity used in (3.19) is an average thermal conductivity, k_p, of all DBC layers. It should be noted that the periphery resistance is calculated in the same manner because both coupling and periphery resistances describe horizontal heat flow. Figure 3.10 shows one segment of the DBC coupling network. The nodes are marked as the temperature at the case of either the top IGBT or bottom diode. For example, T_{casect} designates the temperature at the case of the top IGBT chip. The coupling resistors are designated

as the thermal resistance between the nodes. For example, R_{cdt} is the thermal resistance between the top IGBT and top diode. Each DBC contains one coupling network describing coupling through the DBC between devices.

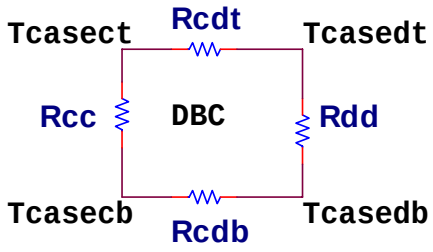


Figure 3.11. Thermal Coupling network of DBC.

A more complicated coupling network is considered for the base-plate layer. Not only is there device to device coupling through the base-plate, but now horizontal heat coupling must be considered between each DBC of the module through the base-plate.

The same coupling network seen in Figure 3.10 describes device to device coupling through the base-plate. Another coupling network must be considered between DBC's since each DBC shares a common base-plate. A capacitance is considered between DBC layers and represents the heat capacitance not accounted for in the vertical thermal networks. All remaining volume is accounted for in the periphery nodes. Figure 3.11 shows the coupling network of the base plate. A temperature is calculated at the node between DBC layers. For example, *Tbt12* designates the temperature between DBC1 and DBC2.

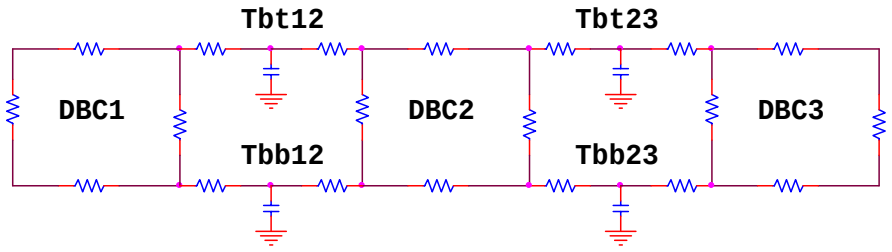
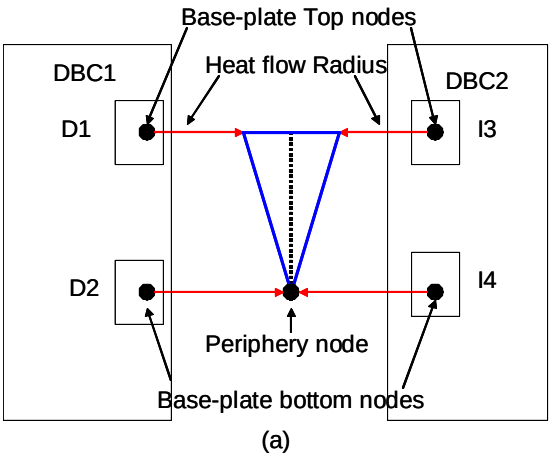


Figure 3.12. Thermal Coupling network of Base-plate.

Again (3.19) is used to calculate thermal resistance where the thermal conductivity is that of copper. In order to calculate the thermal capacitance shown in Figure3.11, the heat flow volume needs to be calculated between DBC layers. Therefore the radial heat-flow between (D1-IGBT3, D2-IGBT4) and (D3-IGBT5, D4-IGBT6) needs to be determined. Without knowing the boundary conditions ahead of time, the MAST® model considers a few different scenarios that could exist. Figure 3.12 shows these different scenarios between DBC1 and DBC2 as an example.



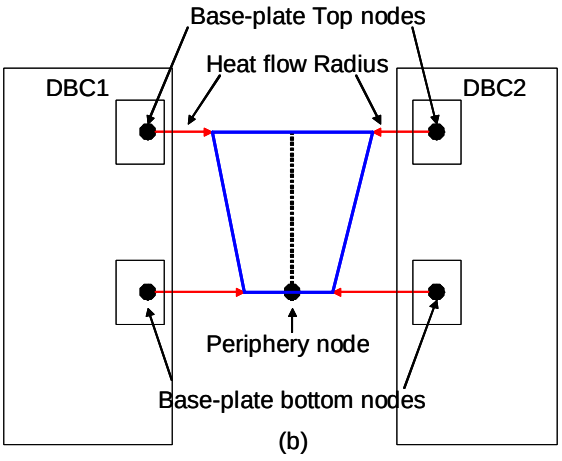


Figure 3.13. Heat coupling volume scenarios.

The red arrows in Figure3.12 designate the heat flow radius at the given depth. We consider the top and bottom of the base-plate. The first scenario, (a), exists when the heat flow radius of the diode and adjacent IGBT meet at the bottom or any where before the bottom of the base-plate. The heat capacity volume that needs to be accounted for with a heat capacitance traces out a triangle (blue outline in Figure 3.12). The volume is easy to calculate. The next scenario, (b), exists when the heat flow radii never meet. Thus the volume traces out the volume seen in Figure 3.12 (b). The coupling node is always placed at the midpoint between heat flow radii at the bottom of the base-plate. Again, all volume not accounted for in the heat coupling or main effective heat flow area is accounted for in the periphery node.

3.3.4 MAST® model Development

The thermal networks described above are implemented in a hierarchy of MAST® templates. At the beginning of each template there are parameters that the user enters. These parameters may include material properties of the DBC as seen in Figure 3.3, or internal geometries of the module needed to calculate the thermal networks and boundary conditions. In some cases, parameters that have been calculated in one template may be used as parameters to another template. For example, the coupling volume calculated in the DBC coupling template program is passed to the base-plate coupling template. At first, an attempt was made to pass these parameters between templates during the netlist, but SABER® cannot do this. Therefore, parameters calculated in one template and needed by another template need to be calculated during an initial netlist. The user passes these calculated parameters to the remaining templates and runs another netlist. This can be achieved because the parameters are not time dependant vars and therefore only need to be calculated once prior to simulation. Table 3.2 shows the material properties that make up each DBC.

Table 3.2 Material properties for DBC model

	Specific Heat $J \cdot kg^{-1} \cdot K^{-1}$	Thermal Conductivity $W \cdot m^{-1} \cdot K^{-1}$	Density $kg \cdot m^{-3}$
Cu	390	400	8900
Solder	150	50	8500
AIN	820	150	3250
Chip	700	150	2330

Table 3.3 shows the effective heat flow areas for the IGBT and diode DBC and base-plate layers that were calculated in the parameters section of the template. The area obviously increases with depth into the chip.

Table 3.3 Effective Heat Flow areas

	Diode	IGBT
a1	0.5848	1.0264
a2	0.6366	1.1235
a3	0.6898	1.2208
a4	0.7332	1.2739
a5	0.7779	1.3285
ac	0.7977	1.3452
ah	0.8626	1.4485
a1	0.9882	1.6211
a2	1.1294	1.7756

Figure 3.13 shows the hierarchy structure of the MAST® thermal model. There is one main calling program which links to the actual SABER® symbol created for simulation. Within the central calling program, a series of templates are called.

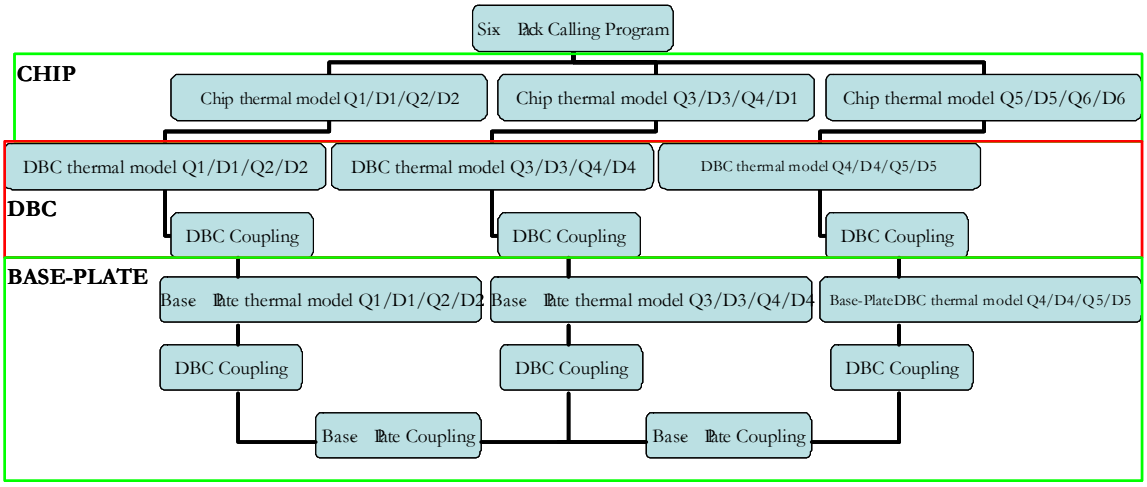
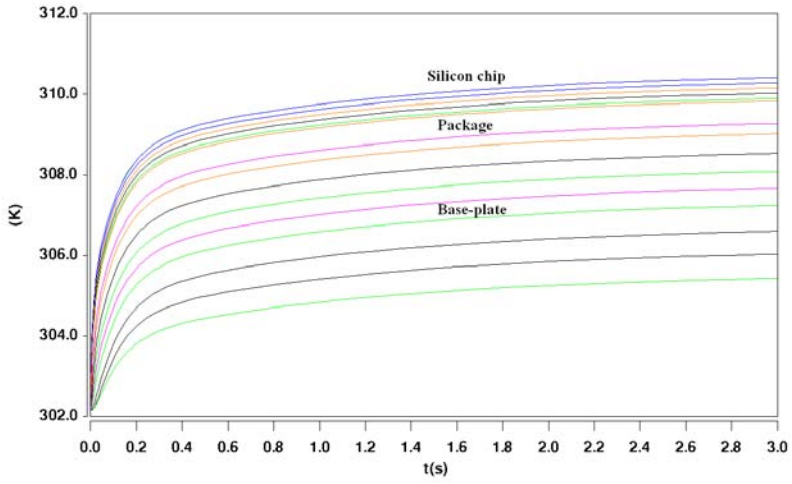


Figure 3.14. Thermal MAST® model hierarchy.

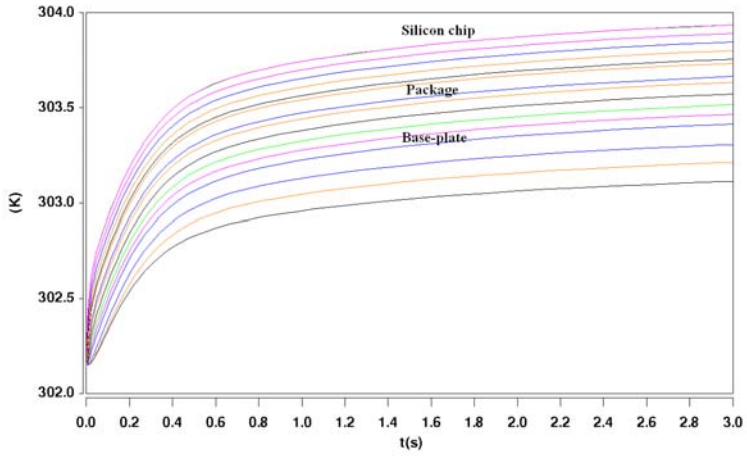
Figure 3.13 shows how the nodes are connected as well as which template is called. First twelve thermal networks are calculated for each silicon device. Each network connects to another twelve thermal networks for the DBC layer. The bottom nodes of each DBC make up a coupling network. These nodes than connect to another twelve thermal networks for the base-plate. The bottom nodes of the base-plate also form two coupling networks. The DBC coupling program is called first to calculate device to device coupling through the base-plate. Then the base-plate coupling program is called for coupling between DBC's.

3.4 Thermal Model Simulation

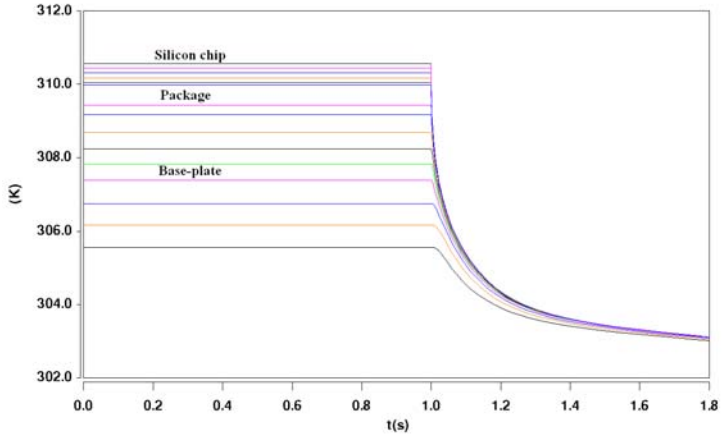
The thermal model is simulated in SABER® sketch. Pulsed power sources are used as inputs to the thermal model. The base-plate connects to a constant ambient temperature through a thermal resistance representing a thermal resistance that may exist between the base-plate of the module and a temperature controlled heat sink. A higher magnitude power pulse was used for the IGBT to simulate the inverter operation where the power dissipation of the IGBT is higher due to switching losses. Figure 3.14 (a-d) shows the thermal heating and cooling of the IGBT and diode respectively. All thermal nodes are shown and represent the temperatures from the top of the silicon chip junction to the bottom of the base-plate.



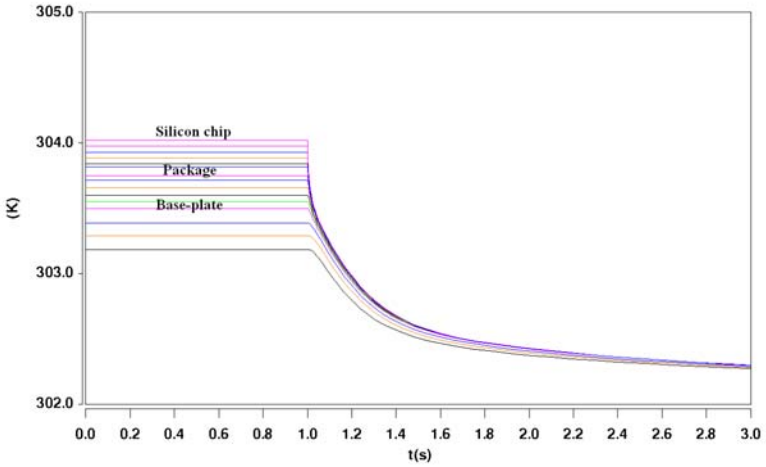
(a) IGBT heating



(b) Diode Heating



(c) IGBT cooling



(d) Diode cooling

Figure 3.15. Transient heating and cooling of IGBT and diode.

It should be noted that the temperatures at or near the silicon chip thermal model are closer in magnitude between adjacent nodes than in the package and base-plate thermal models. Recall that the silicon chip thermal model contains a distributed heat source option where the power distributed into each thermal node may only be a fraction of the total power coming into the junction terminal. This will result in different temperature gradients between adjacent nodes. This is why there needs to be a greater number of thermal nodes near the top of the chip to accurately describe the heat flow.

Since the diode temperatures run cooler than the IGBT, a temperature gradient will exist between the IGBT and diode. The coupling networks describe this behavior. The coupling node temperatures placed in the base-plate are shown in Figure 3.15.

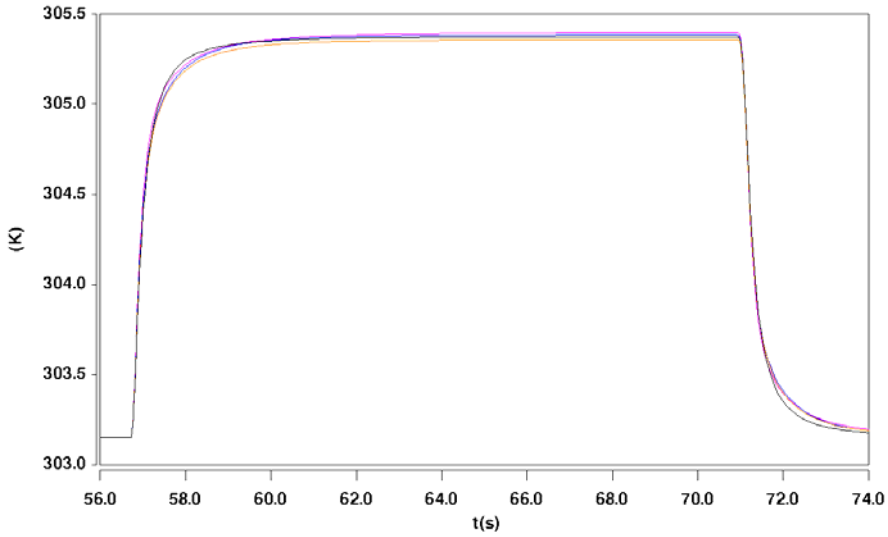


Figure 3.16. Base-plate Coupling nodes between DBC layers.

Chapter 4. Inverter Dynamic Electro-Thermal Simulation with Experimental Verification

4.1 Introduction

In this chapter, simulated and measured electro-thermal results are presented for a space vector modulated (SVM) three-phase inverter using multiple IGBTs and diodes in a six pack module package. The electro-thermal model is comprised of the electrical parameters extracted in chapter 2 for the IGBT and diode and the thermal model developed in chapter 3. The models and simulation are experimentally validated for the electrical and thermal, steady-state and transient condition of the inverter.

To perform electro-thermal simulations using the SABER® circuit simulator, the compact electro-thermal models for power semiconductors devices are connected to both the electrical and thermal networks. For example, the IGBT electro-thermal model has three electrical terminals (gate, collector, and emitter) and one thermal terminal for the junction temperature. The IGBT electrical terminals are connected to other electrical network components of the inverter, and the thermal terminal is connected to the thermal network component models such as the chip, six-pack module package, and heat sink.

In order to couple the electrical and thermal networks, the IGBT electro-thermal model describes the instantaneous electrical behavior in terms of the instantaneous temperature of the device silicon chip surface T_j (temperature at the device thermal terminal). The

temperature dependent electrical model is based upon temperature dependent IGBT model parameters and the temperature dependent physical properties of silicon. The IGBT electro-thermal model also calculates the instantaneous power dissipation that supplies heat to the surface of the silicon chip thermal model through the thermal terminal. The electrical type terminals have units of voltage (V) across the terminals and units of current flowing through the terminals, whereas the thermal terminals have units of temperature (K) across the terminals and units of power (W) flowing through the terminals. Figure 4.1 shows a diagram of the structure of the electro-thermal semiconductor device models.

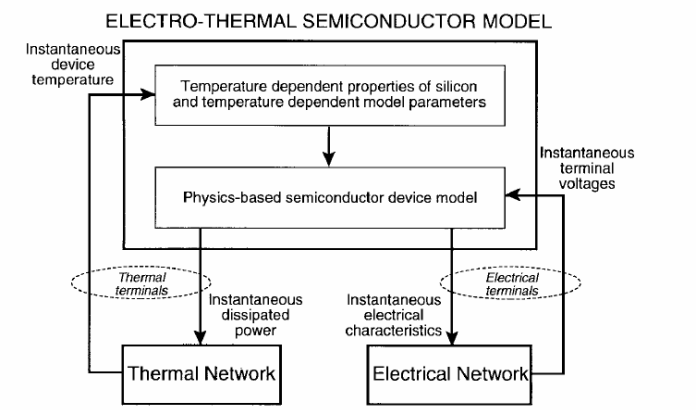
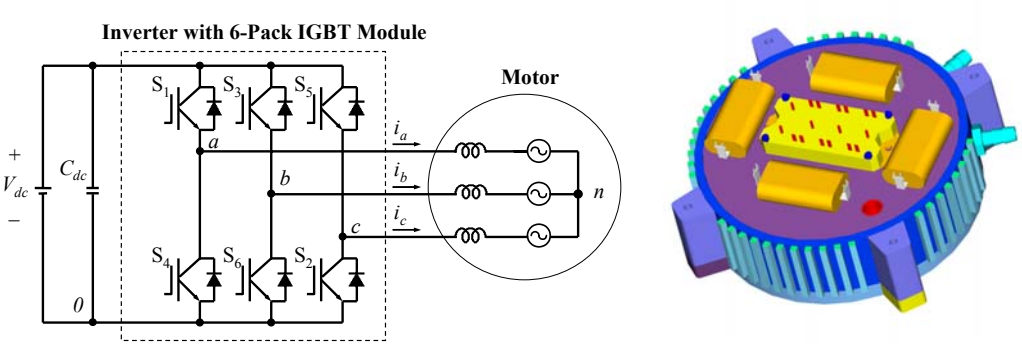


Figure 4.1. Diagram of the structure of the electro-thermal semiconductor device models [3].

4.2 Inverter simulation and model validation

4.3.1 Inverter Circuit and Basic Operation Inverter Operation

Figure 4.2 (a) shows the circuit diagram of a 6-pack IGBT module based inverter for a 10-kW ac motor drive. The module is mounted on a motor end plate, as shown in Figure 4.2 (b). The picture also indicates that four high-frequency dc bus capacitors, represented by C_{dc}, are surrounding the module to ensure sufficient ripple current absorption.



(a) **(b)**

Figure 4.2. The three-phase inverter motor drive using a 6-pack IGBT module: (a) circuit diagram; (b) physical mounting of the IGBT on a motor end plate.

The inverter is controlled using Space Vector Modulation (SVM) and is based upon the allowable switching states of the inverter. There are numerous SVM methods to synthesize the desired output line to line voltage. Some SVM methods emphasize the output waveform quality, and some emphasize the efficiency. The following discussion, figures, and equations are based on the SVM development from [19].

Space vector modulation is based upon the vector space of the phase voltages (a, b, and c) which produce line to line voltages (*ab*, *bc* and *ca*) in the alpha-beta ($\alpha\beta$) coordinate

plane. Figure 4.3 shows the relationship between the coordinate systems, *abc* and *αβ*. The line-to-line voltages (*ab*, *bc* and *ca*) do not have a gamma (*γ*) component in this plane because the neutral line is isolated.

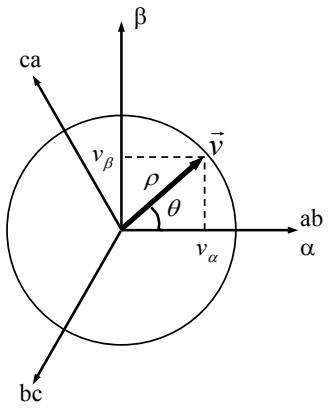


Figure 4.3. Voltage space vector representation [19].

The line-to-line voltage space vector is converted to *αβ* vector space through a transformation matrix.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = T_{\alpha\beta/abc} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix}, \text{where } T_{\alpha\beta/abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \tag{4.1}$$

The desired line-to-line voltage in *αβ* vector space can also be defined as a rotating reference vector:

$$\vec{v}_{ref} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \rho \cdot e^{j\theta} \tag{4.2}$$

$$\rho = \sqrt{v_\alpha{}^2 + v_\beta{}^2} \tag{4.3}$$

$$\theta = \tan^{-1}\left(\frac{v_\alpha}{v_\beta}\right) = \omega t \tag{4.4}$$

To determine the magnitude of this vector, ρ, we look at all the possible switching states of the inverter. Figure 4.4 shows the allowed switching states for each phase.

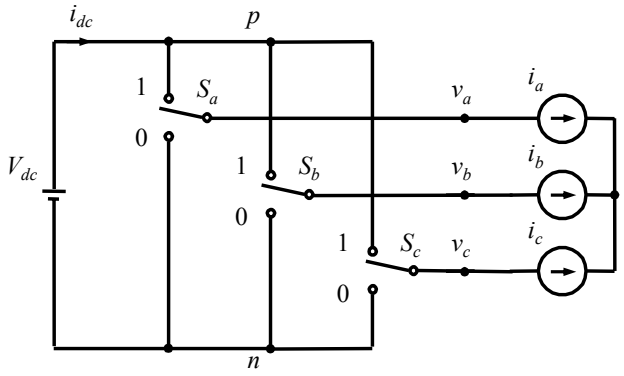


Figure 4.4. Three-phase inverter switching state representation [19].

Table 4.1 shows the voltages and currents in each possible state.

Table 4.1 Allowable switching states of three phase inverter

S_a	S_b	S_c	Switching State	i_{dc}	v_{ab}	v_{bc}	v_{ca}	ρ	θ(°)
0	0	0	V0	0	0	0	0	$\sqrt{2}V_{dc}$	0
0	0	1	V5	i_c	0	$-V_{dc}$	V_{dc}	$\sqrt{2}V_{dc}$	-90
0	1	0	V3	i_b	$-V_{dc}$	V_{dc}	0	$\sqrt{2}V_{dc}$	150
0	1	1	V4	i_b+i_c	$-V_{dc}$	0	V_{dc}	$\sqrt{2}V_{dc}$	-150
1	0	0	V1	i_a	V_{dc}	0	$-V_{dc}$	$\sqrt{2}V_{dc}$	30
1	0	1	V6	i_a+i_c	V_{dc}	$-V_{dc}$	0	$\sqrt{2}V_{dc}$	-30
1	1	0	V2	i_a+i_b	0	V_{dc}	$-V_{dc}$	$\sqrt{2}V_{dc}$	90
1	1	1	V7	$i_a+i_b+i_c$	0	0	0	$\sqrt{2}V_{dc}$	0

There are eight switching states. States *V1-V6* all have the same magnitude, but different phase angles. The following equation calculates this magnitude for state *V1* as an example:

$$\vec{V}1 = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} V_{dc} \\ 0 \\ -V_{dc} \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}} \cdot V_{dc} \\ \sqrt{\frac{1}{2}} \cdot V_{dc} \end{bmatrix} \tag{4.5}$$

$$\rho = \sqrt{(\sqrt{\frac{3}{2}} \cdot V_{dc})^2 + (\sqrt{\frac{1}{2}} \cdot V_{dc})^2} = \sqrt{2} V_{dc} \tag{4.6}$$

Switching state *V0* and *V7* both have a magnitude of *0* and are designated the zero switching states. This state can be realized by turning on all the upper switches or lower switches. Figure 4.5 shows each switching state vector. Switching state *V0* and *V7* are the center point in the figure. The vectors (*V1*-*V6*) trace out a hexagon divided into six sectors designated (*I*-*VI*) sixty degrees apart shown in Figure 4.5. These vectors represent the three phase voltages in vector form that can be obtained at the output [14]. Using vector *V1* as the example, the corresponding switching state (100) means phase-a upper switch *S1* is turned on, while phase-b and -c upper switches *S3* and *S5* are turned off. It should be noticed that upper and lower switches in each phase should be switched complimentarily. Thus switching state (100) also means phase-a lower switch *S4* is turned off, and phase-b and -c lower switches *S6* and *S2* are turned on.

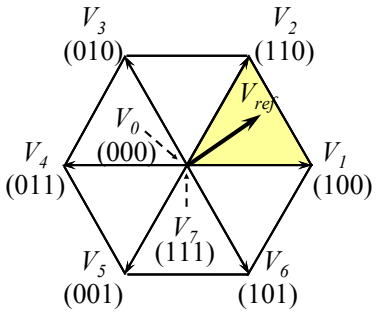


Figure 4.5 Sector partition in a space vector diagram [19].

There are three steps in performing space vector modulation:

1- Choice of switching state vector to synthesize the desired output vector V_{ref}
2- Calculate the duty ratio of chosen switching state vectors
3- Make the sequence of chosen switching state vectors

***1*:**

To synthesize the vector V_{ref}, we choose two adjacent vectors (V_N and V_{N+1}) and a zero vector (V_0) to satisfy the definition of high frequency synthesis. Figure 4.6 describes graphically the definition of high frequency synthesis and (4.7) describes mathematically the definition.

$$\int_0^{Ts} \vec{V}_{ref}\, dt = \int_0^{T1} \vec{V}_N\, dt + \int_{T1}^{T1+T2} \vec{V}_{N+1} dt + \int_{T1+T2}^{Ts} \vec{V}_0\, dt \qquad (4.7)$$

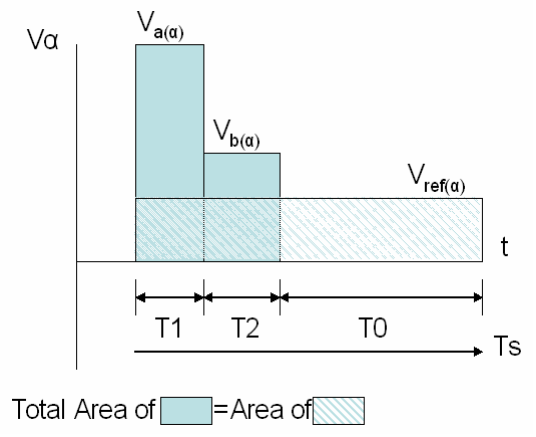


Figure 4.6 Definition of High Frequency synthesis [19].

In order to minimize the number of switching and harmonic distortion, we choose the minimum number of switching state vectors adjacent to the vector V_{ref} from Figure 4.5. Below is a table showing the chosen switching vectors depending on the location of the vector V_{ref}.

Table 4.2 Chosen Switching States in each sector

V_{ref} location	Chosen Vectors V_N, and V_{N+1}
Sector I	V_1 and V_2
Sector II	V_2 and V_3
Sector III	V_3 and V_4
Sector IV	V_4 and V_5
Sector V	V_5 and V_6
Sector VI	V_6 amd V_1

2:

The duty ratio for each switching vector will be calculated from the Figure 4.7:

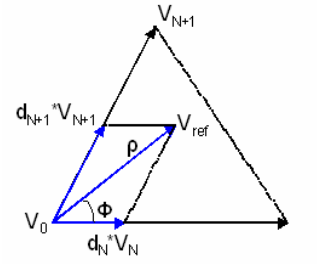


Figure 4.7. Switching vector demonstrating duty ratio calculation [19].

In one switching period, T_s, V_{ref} remains constant:

$$\vec{V}_{ref} \cdot T_s = \vec{V}_N \cdot T_N + \vec{V}_{N+1} \cdot T_{N+1} \qquad (4.8)$$

$$\rho \cdot \begin{bmatrix} \cos\phi \\ \sin\phi \end{bmatrix} \cdot T_s = \|V_N\| \cdot \begin{bmatrix} 1 \\ 0 \end{bmatrix} \cdot T_N + \|V_{N+1}\| \cdot \begin{bmatrix} \cos 60^\circ \\ \sin 60^\circ \end{bmatrix} \cdot T_{N+1} \tag{4.9}$$

where:

$$\phi = \theta - (N-1) \cdot 60^\circ - 30^\circ \tag{4.10}$$

N in the above equations refers to the sector number (1-6). The duty calculations are given as:

$$\frac{T_N}{T_s} = d_N = \frac{2}{\sqrt{3}} \cdot \frac{\rho}{\|V_N\|} \cdot \sin(60^\circ - \phi) \tag{4.11}$$

$$\frac{T_{N+1}}{T_s} = d_{N+1} = \frac{2}{\sqrt{3}} \cdot \frac{\rho}{\|V_{N+1}\|} \cdot \sin\phi \tag{4.12}$$

$$d_0 = 1 - d_N - d_{N+1} \tag{4.13}$$

Solving the above equations and using table 4.1.:

$$d_N = \frac{V_M}{V_{dc}} \cdot \sin(60^\circ - \phi) \tag{4.14}$$

$$d_{N+1} = \frac{V_M}{V_{dc}} \cdot \sin\phi \tag{4.15}$$

V_M is the peak to peak line to line output voltage to be synthesized.

The modulation index, M, is defined as:

$$M = \frac{V_M}{V_{dc}} \tag{4.16}$$

3:

In this particular inverter control, the sequence of chosen switching state vectors for sector I is shown in Figure 4.8. The sequence in Figure 4.8 also indicates the switch turn-

on or -off duties for the shaded sector that is enclosed by (V_1, V_2) and zero vectors (V_0, V_7). Time intervals or duty cycle periods T_0, T_1 and T_2 are calculated by the digital signal processor (DSP) in every switching cycle T_s. The duty cycle periods should satisfy $V_{ref} = (V_1 \cdot T_1 + V_2 \cdot T_2)/T_s$ and $T_s = T_0 + T_1 + T_2$. The turn-on period of the phase-a upper switch is the sum of $T_1 + T_2 + T_0/2$, the turn-on duty of phase-b upper switch is the sum of $T_2 + T_0/2$, and the turn-on duty of phase-c upper switch is $T_0/2$. Similar switching patterns can be applied to other sectors.

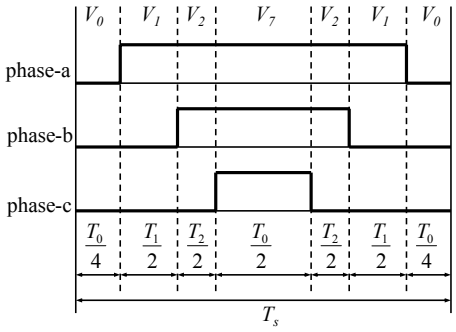


Figure 4.8. Space vector modulation diagram timing diagram of the SVM inverter control algorithm [19].

4.3.2 Experimental Validation of 6-pack Thermal Model

The test circuit of Figure 4.9 is used to independently validate the performance of the 6-pack module package thermal model. The test circuit uses the temperature sensitive parameter (TSP) method to measure the IGBT chip transient temperature response where the gate-cathode threshold voltage is the TSP [8]. Either upper or lower IGBTs (IGBT1 or IGBT2) can be used; the unused devices of the six-pack are disabled by connecting their gate and cathode terminals together as shown. Neither diode is forward biased during the measurements.

The cathode of the test IGBT is connected to a pulsed constant current source that is referenced to ground, and the anode of the IGBT is connected to a heavily-bypassed voltage supply, also referenced to ground. The gate of the IGBT is grounded through a 470 Ω resistor that serves as a damping resistor to prevent oscillation. This circuit arrangement causes the IGBT to operate in the active or linear region during the heating phase of the measurement. There is a small auxiliary current source comprised of a 62 V voltage supply and 7.5 kΩ resistor as shown in Figure 4.9 which is used to limit the amplitude of the measured switching voltage that appears on the cathode, and to provide the capability of using the TSP measurement during the cooling phase. The cathode voltage is applied to channel 1 of a digitizing oscilloscope, and the gate voltage is applied to channel 2 of the oscilloscope. The data acquisition is used to provide a differential gate-to-cathode measurement because a substantial voltage transient appears at the gate during switching [8].

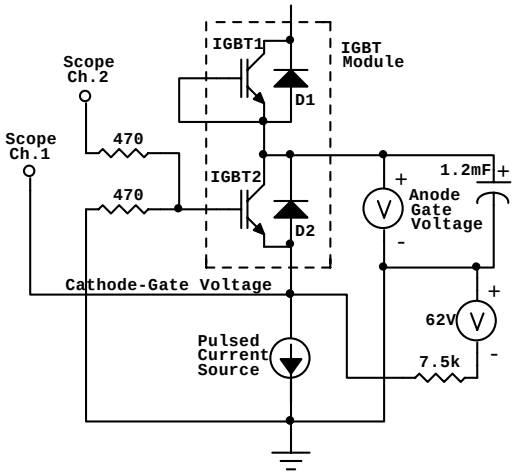


Figure 4.9. High Speed IGBT Thermal transient test circuit [8].

The measurement of the IGBT transient heating requires two parts. First, a calibration consisting of the measurement of the cathode to gate voltage, the TSP, must be made at known IGBT operating conditions and at a series of known temperatures. The operating conditions that need to be specified include anode to cathode voltage and anode current. Known temperatures are provided by having the IGBT module mounted on a heat sink that is heated at various temperatures by heating resistors under computer control. It is very important to use very short pulses during the calibration of the TSP as to avoid significant chip heating. The result of the calibration is an established relationship between chip temperature and the TSP value.

Second, the IGBT is subjected to a longer pulse under a temperature controlled heat sink. The same anode current and voltage conditions are used for the transient heating pulse as for the TSP calibration pulse. During the transient heating pulse, the IGBT chip increases in temperature, and the heat propagates through the chip, DBC, and base-plate layers. The TSP value is recorded and mapped into temperature using the calibration data. Depending on the length of the pulse, the heat may not propagate all the way to the bottom of the base-plate. Higher power pulses require shorter duration pulses as to not destroy the device. Therefore the heat does not propagate all way through the DBC to the base-plate and may not show good validation of the model. Therefore lower power pulses are needed so a longer duration pulse can be achieved without destroying the device. This will allow validation of heat propagation through the entire device [8].

Figure 4.10 shows the transient heating of the IGBT captured during measurement. As the IGBT gets warmer, the cathode voltage rises and is converted to temperature using the calibration data. The cathode voltage is measured with one scope probe while the gate

voltage is measured with another. The two channels are subtracted to obtain the gate-cathode voltage. During the heating pulse, the gate-cathode voltage rises. This is a result of threshold voltage temperature dependence. As temperature increases, the threshold voltage decreases [8].

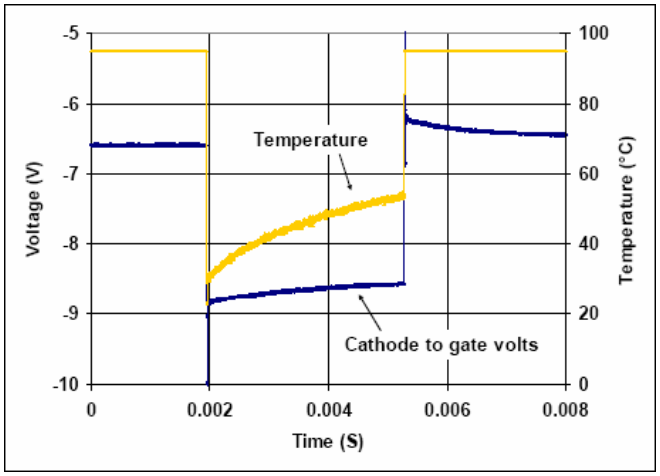


Figure 4.10 Measured cathode to gate voltage mapped to temperature. Portions of the temperature waveform are truncated to 95 °C [8].

Figure 4.11 shows the measured and simulated transient thermal response of the 6-pack module package to heating one IGBT at different power levels: 380 W, 950 W, and 2700 W. The simulations were run in SABER® using a constant power pulse source connected to the IGBT thermal module model. Only one IGBT is connected to the power source. A constant temperature source is connected to the base plate of the module representing the constant heat sink temperature used in the experiment.

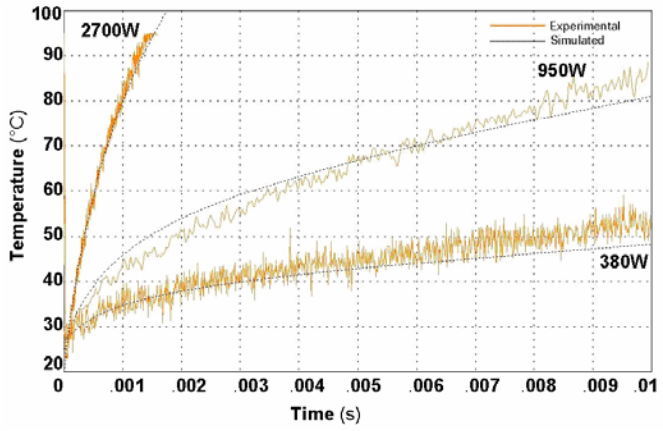


Figure 4.11 Simulated transient thermal response of 6-pack module for heating of single IGBT under various power conditions with experimental verification using high-speed temperature sensitive parameter measurement.

4.3.3 Inverter Simulation and Experimental Verification

The inverter simulation was implemented in SABER® using the physics based electro-thermal models for the IGBTs and diodes. The SVM control scheme was implemented in a SABER® MAST® model. In the MAST® model, the duty ratios were calculated based on the modulation index, switching frequency, and bus voltage. The model for the IGBT gate drivers are behavioral models, which convert the digital inputs (logic signals) created from the SVM MAST® model to the appropriate analog IGBT gate-drive signals. The drive capability and the output rise and fall times of the gate driver directly impact the *di/dt* of the inverter, thus affecting switching losses. All these parameters, along with the gate drive resistor, need to be taken into account to accurately predict the *di/dt* of the inverter. The gate drive chip used in hardware is the Hewlett Packard HCPL-316J [27]. The typical layout of the gate driver is shown in Figure 4.12.

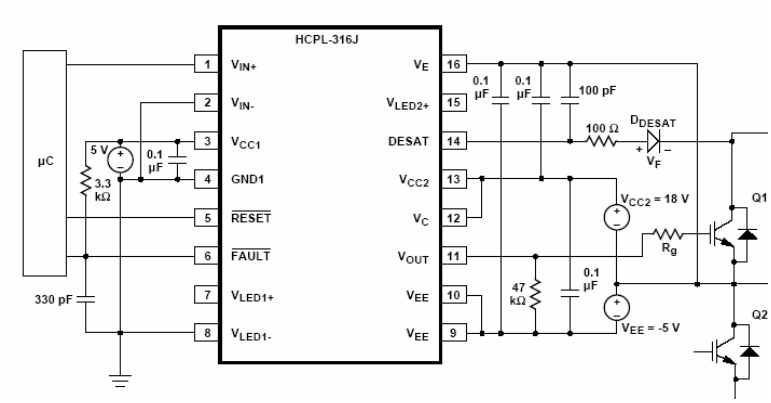


Figure 4.12 IGBT gate drive layout [27].

Figure 4.13 shows a closer look at the internal circuitry of the chip.

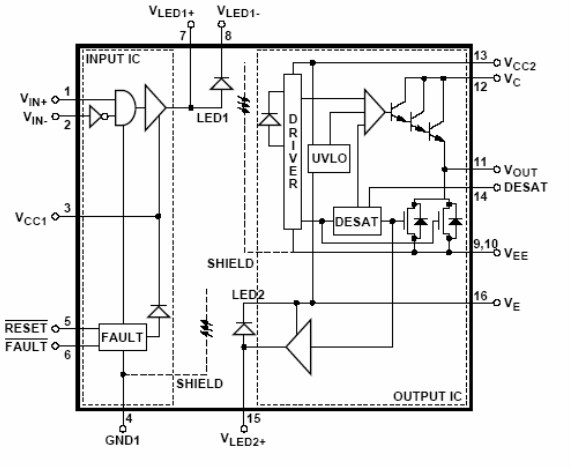


Figure 4.13 Internal circuitry of HCPL-316J [27].

A closer look at the IGBT gate drive signal, V_{out} seen in Figure 4.13, is determined by either V_{CC2} minus three diode drops or V_{EE}. For the model in this work, we will set V_{out} = 18-(3x.7) = 15.9 V and V_{EE} = -5 V. These voltages will be used to drive the IGBT. Next we will consider the drive capability of the chip. Figure 4.14 shows the output current capability of the chip versus gate drive resistance.

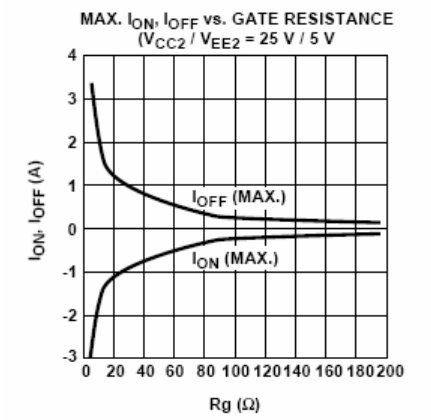


Figure 4.14 Drive capability of HCPL-316J [27].

We will model the output drive capability of the chip with a resistor. If we assume there is no external gate drive resistor, R_G, then one can infer from Figure 4.14 that the maximum output current the chip can produce is about 4 A. The measurement was taken with V_{CC2} = 25 V. Therefore the resistor that we will use to model the drive capability is 25V/4A = 6.25 Ω. We will add this value to the external gate resistor used in hardware which was equal to 10 Ω. The rise and fall time given by the datasheet is equal to about .1us [27].

Figure 4.15 demonstrates the functional circuit implemented in SABER®, where each IGBT (Q) and diode (D) correspond to those of Figure 3.3. The gate terminals of the IGBT are tied to the behavior gate drive model (not shown). The thermal terminals on the IGBT's and diodes connect to the six-pack IGBT thermal model via a common net name. The motor is modeled as an inductor-resistor network on each phase as shown. The inductors are 1mH and resistors are 2.2 Ω. The module base-plate used in hardware is mounted on a temperature controlled heat sink; likewise, the thermal model in the simulation connects the module base-plate to a constant temperature source. This is designated as Ambient in the figure. An effective thermal resistance designated $R_{thermeff}$ is

shown, which includes an insulating layer of Thermstrate^{TM} placed between the base-plate and heat sink. The thermal resistance of the Thermstrate^{TM} was determined to be 0.025°C-in^2/W. Each thermal node of the base-plate was given a thermal resistance based on the effective heat flow area at that node. The thermal resistances of each node were then combined in parallel to give the effective thermal resistance $R_{thermeff}$ shown in Figure 4.15.

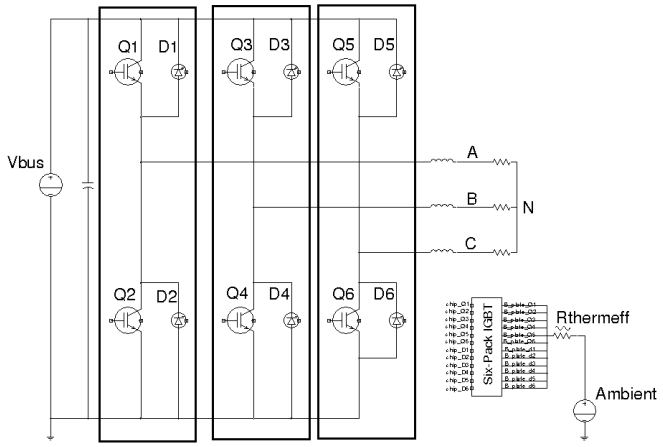


Figure 4.15. Functional circuit used in the simulation.

The temperatures at several points in the inverter system were monitored with thermocouples, and the temperature monitored at the IGBT base-plate was used for thermal validation. Both transient and steady state temperatures were recorded and analyzed.

The inverter was pulsed with a series of different power levels and base-plate temperature measurements were made as shown in Figure 4.16. Three power levels designated Case1 (4 kW), Case2 (7 kW), and Case3 (11 kW) are used for model validation. All three cases use a modulation index of 0.8 and switching frequency of 10 kHz. The active time for each inverter power level is long enough for the inverter and

thermal network being validated to reach a steady-state condition. Also shown on the figure is the average temperature that was measured.

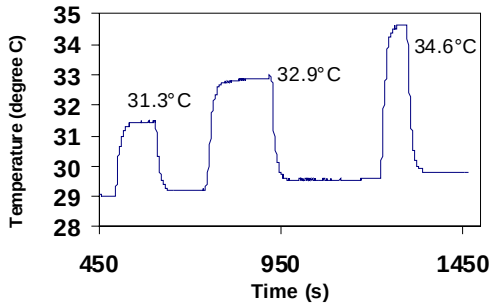


Figure 4.16. Measured transient heating of single IGBT under various power conditions.

As seen in Fig 4.16, it takes 50 to 100 seconds to arrive at a thermal steady-state condition. This is very difficult to do with limited storage space and computational speed in the simulator. To account for this difficulty, a four-step iterative process is used to determine the initial condition for the IGBT temperature [7].

1- First, a full electro-thermal simulation of the inverter is performed over a few 60 Hz cycles (three in this case).

2- The average dissipated power is determined for each device using the Wave-Calc waveform calculator in SABER® Scope to integrate the dissipated power over a complete 60 Hz cycle.

3- The calculated value of the average power is then used in a pulsed power source into the thermal model to determine an initial temperature condition for the IGBT.

4- Another full electro-thermal simulation is performed with the initial temperature condition found in step 3.

This iterative process is repeated until the average power converges to steady state. Figure 4.17 shows all three phase currents for two 60 Hz cycles of Case 3, and Figure 4.18 shows the corresponding chip junction temperatures for each phase. Notice the

IGBT junction temperatures have spikes occurring at the switching frequency, 10 kHz. This is due to the switching losses. The 60 Hz variations of the IGBT chip surface temperatures are due to the sinusoidal load current variation. Obviously the highest magnitude of temperature occurs during the peak amplitude of load current.

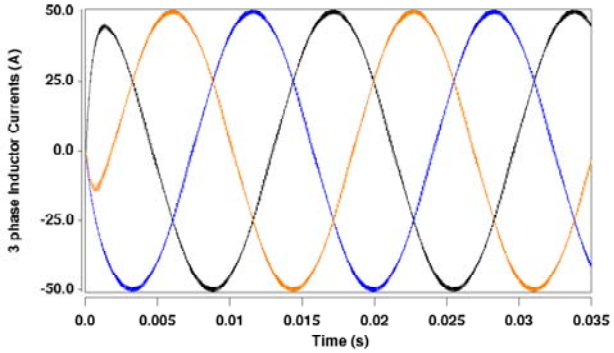


Figure 4.17. Simulated three-phase inverter current waveform for each phase in a two 60 Hz cycles of the inverter for the 10.8 kW condition.

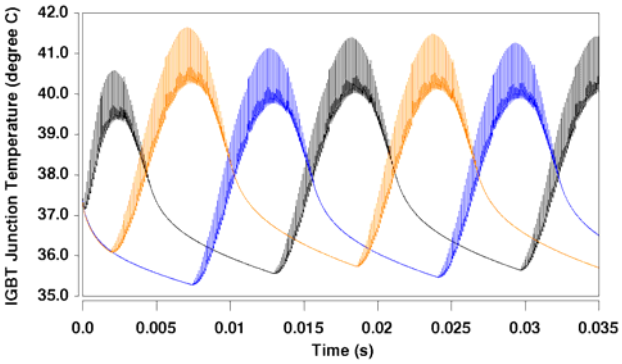
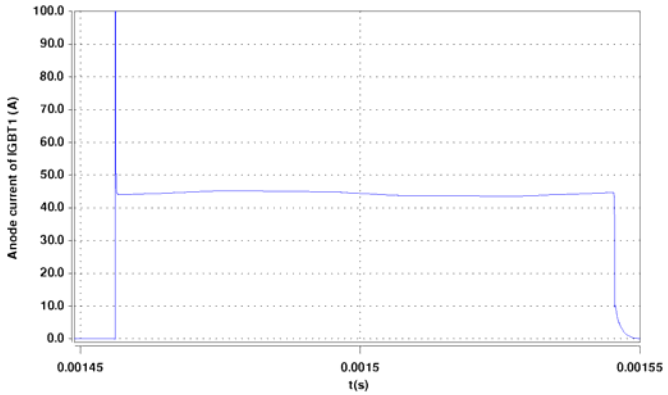


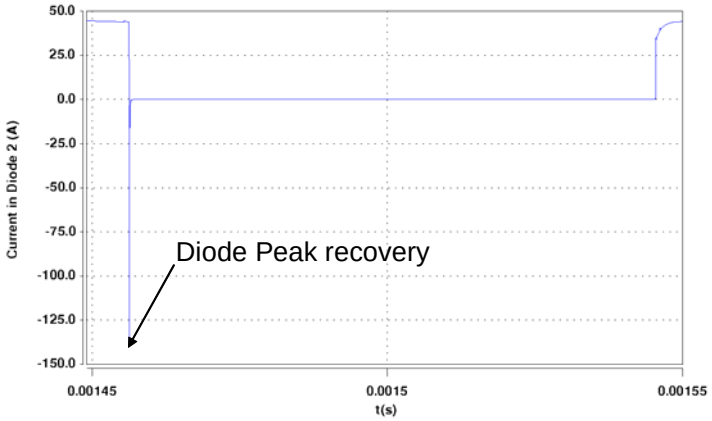
Figure 4.18. Simulated three-phase inverter IGBT chip junction temperature waveform for each phase in two 60 Hz cycles of the inverter for the 10.8 kW condition.

The current in each phase is conducted through an IGBT and anti-parallel diode. Considering phase "a" for a moment made up of *Q1*, *Q2*, *D1* and *D2*. When the inductor load current is positive, the current is carried through *Q1* and *D2*. When the load current goes negative, the current is carried through *Q2* and *D1*. Other phases operate in the

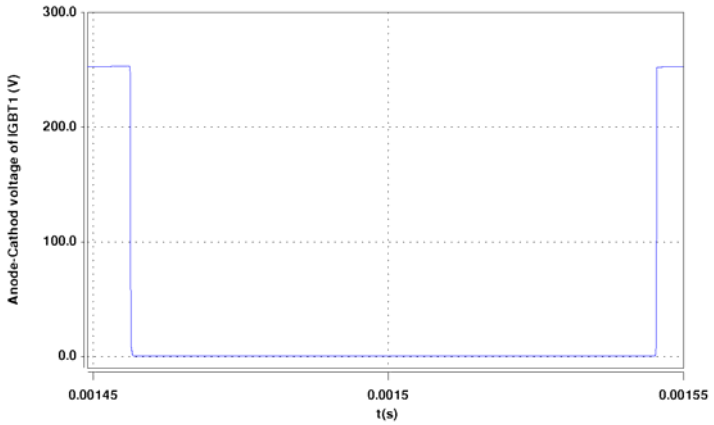
same manner. The next set of figures shows a switching cycle condition for IGBT 1 designated *Q1* in Fig 4.12. The IGBT anode current, current though *D2*, anode voltage, power dissipation, energy and IGBT chip surface temperature for Case 3 are shown in Figure 4.19 (a-f).



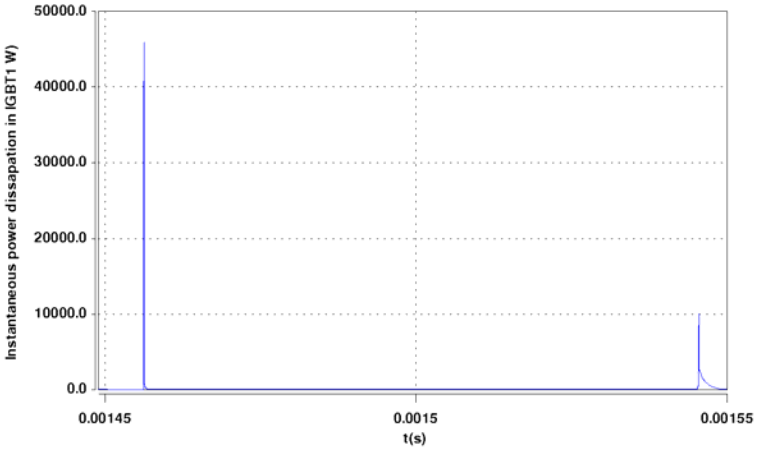
(a)



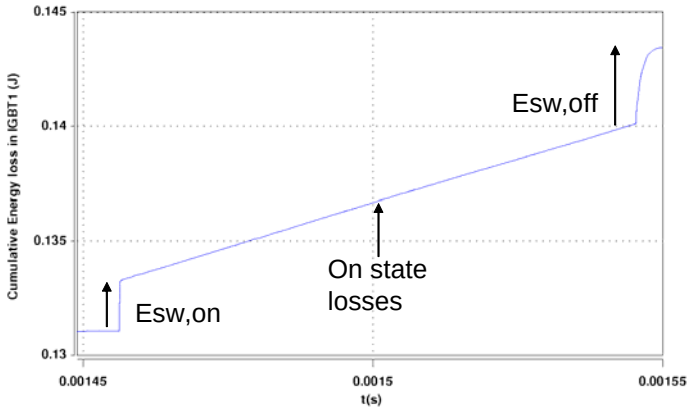
(b)


300.0
200.0
100.0
0.0
Anode-Cathod voltage of IGBT1 (V)
0.00145
0.0015
0.00155
t(s)

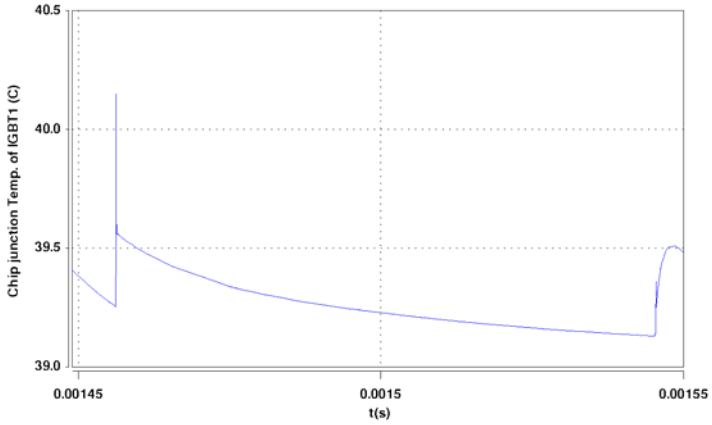
(c)


50000.0
40000.0
30000.0
20000.0
10000.0
0.0
Instantaneous power dissapation in IGBT1 W)
0.00145
0.0015
0.00155
t(s)

(d)



(e)



(f)

Figure 4.19 Simulation results of one 10 kHz switching cycle for the (a) IGBT anode current, (b) current though D2, (c) anode voltage,(d) power dissipation, (e) energy and (f) IGBT chip surface temperature for Case 3.

The spike at turn-on occurs because *Q1* is forced to block the full supply voltage of 252 V and a current that is larger than the load current during the reverse recovery of *D2*. This reverse recovery spike from the diode can be seen in Figure 4.19 (b). In practice, this turn-on energy/loss, *Esw-on* seen in Figure 4.19 (d), can be reduced by using a larger

IGBT gate resistance. A larger gate drive resistor will reduce the *di/dt* of the inverter which in turn reduces the peak diode reverse recovery. However, this results in higher over all duty cycle loss because the device takes longer to turn on. Not only do the gate drive parameters affect the *di/dt* of the inverter, but it has been shown in [28] that circuit parasitics impact the *di/dt* of the inverter as well. Gate inductance and package inductance within the module can reduce the *di/dt* of the inverter. Actual parasitic values for a typical IGBT power module are given in [29]. Modeling all the module parasitics within the module is beyond the scope of this thesis. Once the reverse recovery of *D2* is complete, the voltage across *Q1* drops and approaches the IGBT on-state voltage.

The instantaneous power dissipation is now determined by the product of the on-state voltage and load current. This power dissipation makes up the on-state or conduction losses. The power dissipation during the on-state condition of the switching cycle is much smaller than the power dissipation seen during switching, but is much longer in duration. Therefore, the energy-loss waveform of Figure 4.19 (e) rises with a constant slope (determined by the load current and IGBT on-state voltage) during the on-state phase of the switching cycle.

Simulated voltage and current waveforms are shown in Figure 4.20 for a single turn-off event for *Q1*. When *Q1* is commanded to turn off, the anode-to-cathode voltage rises. This voltage is eventually clamped by *D2* at the bus voltage of 252 V plus the on-state voltage of *D2* because constant current is maintained in the load inductance. The anode current through *Q1* then drops rapidly due to the channel being cut off. A slow decaying tail follows which is caused by the stored charge in the base region of *Q1*. This decaying

tail increases as temperature increases and leads to higher losses because the lifetime increases with temperature.

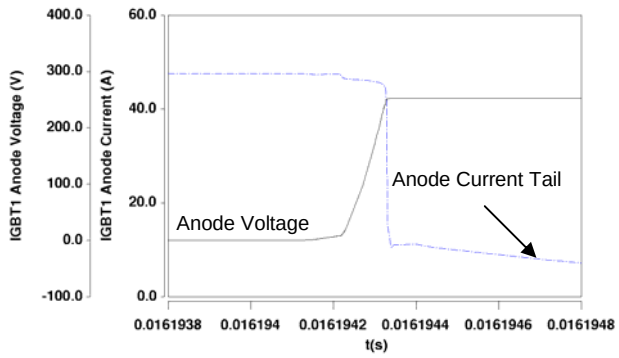


Figure 4.20. Turn off waveforms of IGBT1.

Thus, a large anode-cathode voltage and current exist at the same time, resulting in a large power dissipation and temperature spike at turn-off. Although the power dissipation level is not as high as during the turn-on event, the turn-off switching time is much longer due to the slowly decaying excess carriers in the IGBT base. Thus, the turn-off switching energy $E_{sw,off}$ indicated in Figure 4.19 (e) is larger than the turn-on energy.

Figure 4.21 shows the simulated relationship between the IGBT chip surface temperature, T_j, the package header chip interface T_h, and the package case base-plate interface T_c. The chip junction is the only node that has a thermal response to the high switching frequency. This is because the other two nodes have higher capacitive energies and only respond to the lower frequency. As a result, the lower nodes only respond thermally to the 60 Hz load variation. As the nodes get even further down into the module towards the bottom of the base-plate, there is not much thermal response to the 60 Hz. The high capacitive energies of these lower nodes do not respond to the lower

frequency, but take much longer to reach steady state condition. This is the reason for initial conditions in the electrical simulation. It will be shown later, that these lower nodes take a few seconds or even minutes to reach steady state.

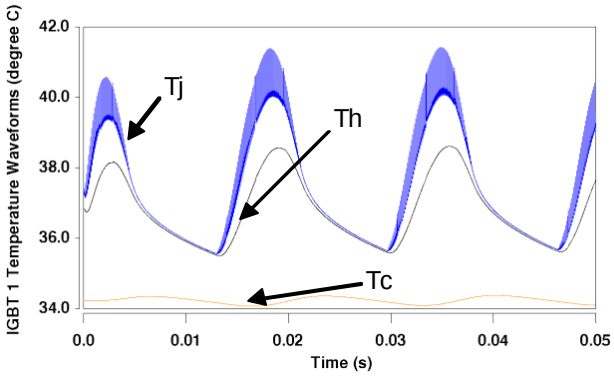


Figure 4.21. Temperature waveforms of IGBT1 showing surface Tj, header chip interface Th, and case base-plate interface Tc.

The temperature T_c in Figure 4.21 shows the instantaneous base-plate temperature of IGBT 1 for case 3, resulting from the full electro-thermal simulation. Figure 4.22 shows the average base-plate temperature, used for model validation, of IGBT1 resulting from a thermal simulation of each case. The thermal simulation uses a constant power pulse equal to the average steady state power measured in the full electro-thermal simulation. The power pulse is used as an input to the thermal model network. Note, the time scale of Figure 4.22 differs from the time scale of Figure 4.16 because only steady state operation is required for validation and thus does not require the same amount of time shown in Figure 4.16. The average power dissipated in the IGBTs and diodes for each case was calculated as shown in Table 4.3. Table 4.4 compares the measured and simulated results for all three cases.

Figure 4.23 illustrates device-device coupling effects considered in the six-pack module by showing the difference in average DBC temperatures of *D1* for each power pulse. Note that with device-device coupling, *D1* is a few degrees warmer due to heat coupling through the DBC between *Q1*, *D1*, *Q2*, and *D2*.

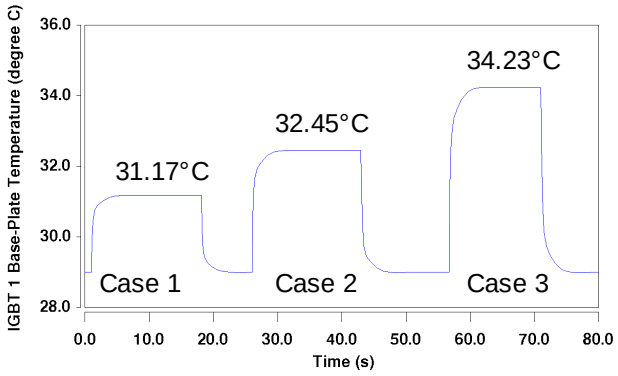


Figure 4.22. Base-plate temperatures of IGBT1 for the cases shown in Table 4.2.

Table 4.3 Average Steady State Power for each case

	IGBT	Diode
Case 1	17 W	1.5 W
Case 2	27 W	2.2 W
Case 3	41 W	2.9 W

Table 4.4. Measured vs. Simulated Results

Case 1 – 150 V Bus Voltage	Simulated	Measured
Output current (rms)	20.9 A	22.6 A
Average steady state temperature	31.17 °C	31.3 °C
Case 2 – 200 V Bus Voltage	Simulated	Measured
Output current (rms)	27.95 A	30.02 A
Average steady state temperature	32.45 °C	32.9 °C
Case 3 – 252 Bus Voltage	Simulated	Measured
Output current (rms)	35.1 A	38.35 A
Average steady state temperature	34.23 °C	34.6 °C

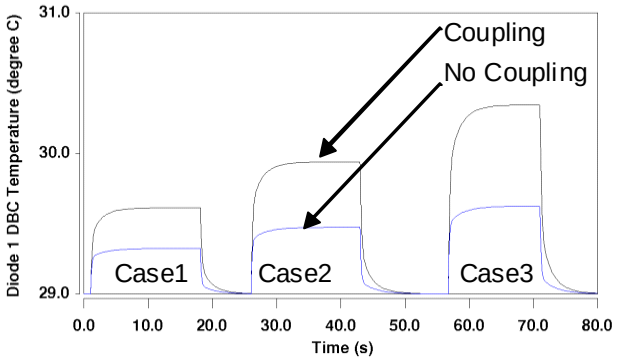


Figure 4.23. DBC temperatures of Diode 1 for each case in Table 2, both with and without device-device coupling.

Chapter 5. Conclusion

5.1 Major Contributions

Electro-thermal modeling approaches have been widely used within different circuit simulators. The detail and complexity of the electro-thermal model within this work is the major difference between these previous developed models. Electrical parameters were extracted over temperature for both the insulated gate bipolar transistor (IGBT) and diode electro-thermal models from actual devices used within system level hardware. A thermal network methodology that includes thermal coupling between devices was applied to a six-pack module package for the first time within the MAST® language.

The first fully coupled dynamic electro-thermal three phase inverter simulation was performed under several power levels. Good agreement between model and measurement was obtained for steady state operation. In addition, transient heating of a single IGBT in the six-pack module under high power heating conditions has been modeled and validated, yielding good agreement using the advanced temperature sensitive parameter approach (TSP) developed in [8].

This thesis describes a process for electro-thermal simulation. The parameter extraction sequence was not developed by the author for example, but used with existing thermal modeling techniques to develop a methodology for electro-thermal simulation. Existing validation circuits and techniques were used as well for model validation. This is the first time that these disciplines (i.e. thermal modeling, parameter extraction and validation

techniques) have been coupled together to produce a fully coupled dynamic system level simulation.

5.2 Future Work

Future work should include further thermal validation. Transient heating of the inverter can be validated for example, along with steady state operation at a few more points within the inverter system. Temperature dependent parameters can be extracted and validated over a wider range of temperature points. Certain parameters were removed or approximated depending on their contribution to the system level point of view. The parameter extraction should be revisited and "tweaked" to gain more accuracy. The system simulation can be studied under different operating conditions such as startup or short circuit conditions. A more accurate heat sink model can be developed to more accurately describe the water cooled system. An actual SABER® electro-thermal motor model can be included at the output of the inverter and validated with measurement. The thermal models can be further "bullet proofed" to allow for better convergence by the simulator and improve simulation time. Further analysis of circuit and module parasitics can be modeled and validated.

Appendix A References

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