High-Frequency Design Consideration and EMI Mitigation in SiC-Based Multilevel Converters

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Abstract

Medium Voltage (MV) power conversion systems are essential in high power applications to address the increasing demand of energy and the increasing penetration of renewable energy sources. MV power electronics converters are the key elements for power conversion in MV systems and are the focus of this study.

Multilevel converter topologies are promising topologies in MV applications because of their reduced voltage stress on devices, excellent output quality, reduced semiconductor losses, lower common mode voltage among other advantages. However, they may suffer from the large number of switching devices and capacitors, as well as the need to regulate capacitor voltages. SiC MOSFETs can achieve higher switching speeds, higher switching frequencies, higher voltage ratings, higher operation temperatures compared to traditional Si devices. They have shown promise to increase the efficiency and power density of the converters, but may suffer from higher voltage overshoots, increased Electromagnetic Interference (EMI) emission and so on.

In SiC-based multilevel converters, the features of multilevel topologies, and the features of SiC MOSFETs are coupled together. The benefits, challenges, and solutions of using SiC MOSFETs in multilevel converters are studied explicitly in this work. With the high switching

speeds and high switching frequencies of SiC MOSFETs, and the large number of switches and capacitors in multilevel topologies, SiC-based multilevel converters need to be studied while considering high-frequency voltage and current behaviors and the interactions among them at different locations.

Firstly, the use of SiC-based multilevel converter in the high-speed motor drive application is explored. A three-phase inverter is designed and built employing five-level Stacked Multicell Converter topology and SiC MOSFETs. The benefits and challenges of using multilevel converter topology and using SiC MOSFETs for this application are explored. A fitting topology is selected, and a prototype is designed, both with attentions paid to deal with the high switching speeds of SiC MOSFETs. The inverter is verified through experiments to meet all specifications with a high efficiency.

Then a unique type of converter, converters with Integrated Capacitor Blocked Transistor (ICBT) cells are studied. Unlike the traditional methods, there are no fast-developing voltage unbalances, or high cell capacitor voltage ripples in ICBT-based converters. The ideal operation principle is analyzed and verified by the simulation results. Then the impacts of non-idealities on the operation are analyzed, and a control method is proposed for this type of converter. The operation and control of ICBT-based converters are verified by experimental results to achieve low cell capacitor voltage ripples and excellent voltage balance in Medium Voltage high power applications.

Lastly, the conducted EMI emission in SiC-based multilevel converters are studied. Four SiC-based multilevel converters are studied, with the focus on the power circuit in one converter and the auxiliary circuits in the other three converters. The complexity of noise generation and propagation in multilevel converters is presented. The conducted EMI disturbances are experimentally evaluated, analyzed, and effectively mitigated in all four cases.

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General Audience Abstract

Medium Voltage (MV) power conversion systems are essential in high power applications to address the increasing demand of energy and the increasing penetration of renewable energy sources. MV power electronics converters are the key elements for power conversion in MV systems and are the focus of this study.

Multilevel converter topologies are promising topologies in MV applications because of their reduced voltage stress on devices, excellent output quality among other advantages. However, they may suffer from the large number of switching devices and capacitors. SiC MOSFETs are promising switching devices in MV applications as they can increase the efficiency and power density of the converters. However, the high switching speeds and high switching frequencies of SiC MOSFETs may lead to higher voltage overshoots, increased Electromagnetic Interference (EMI) emission and so on. The benefits, challenges, and solutions of using SiC MOSFETs in multilevel converters are studied explicitly in this work.

Firstly, the use of SiC-based multilevel converter in the high-speed motor drive application is explored. A three-phase inverter is designed and built. The benefits and challenges of using multilevel converter topology and using SiC MOSFETs for this application are explored. The inverter is verified through experiments to meet all specifications with a high efficiency. Then

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Chapter 1. Introduction

1.1 Application Background

An increasing demand of energy and an increasing penetration of renewable energy sources are two among many features in recent research and industrial applications of electric power conversion. Medium Voltage (MV) systems are essential in these high power applications as they can transfer higher power with lower currents, and therefore have lower conduction losses and lower copper cost, compared to Low Voltage systems. MV systems have been studied or utilized in a variety of application such as machine drives [1]-[3], wind turbine systems [4]-[6], photovoltaic power plants [7]-[9], shipboard power systems [10]-[12], railway systems [13]-[15], etc.

The dc grids are preferred over the traditional ac grids in MV systems nowadays as they exclude bulky line frequency transformers, thus significantly reduce the system overall size and weight [16]. Dc transmission and distribution systems have reduced power losses also because of the absence of reactive currents and because of less conversion stages when integrating dc-based generation units and supplying dc-based loads [17]. In addition, using dc grids also eliminates reactive voltage drop and the need for phase angle synchronization [18].

MV power electronics converters, especially MV dc-dc converters, MV dc-ac converters and MV ac-dc converters, are the key elements for power conversion in MV systems, and are the focus of this study.

1.2 Multilevel Converter

The concept of multilevel converter topologies was born in 1975 when Baker and Bannister proposed a topology that is later known as the Cascaded H-Bridge converter [19]. Since then, numerous different multilevel topologies have been proposed. Some of the most classic and commonly used topologies include Diode Clamped Converter [20], Active Neutral Point Clamped Converter [21], Flying Capacitor Converter [22], Modular Multilevel Converter [23]. Most of the converts in MV systems [1]-[15] employ multilevel topologies. While multilevel converters can be categorized into voltage source multilevel converters and current source multilevel converters [24]-[26], only the voltage source multilevel converters are studied in this work.

One of the most important advantages of multilevel converters is the reduced voltage stress on switching devices. When a switching device is in the off state, it is clamped by another device to an internal capacitor, or by multiple devices to multiple internal capacitors. As a result, a switching device only needs to block a fraction of the converter dc bus voltage, which means the converter voltage ratings can be increased without being limited by the available device voltage ratings.

Another important advantage of multilevel converters is the excellent output quality. Unlike in two-level converters where the converter output voltage switches between the positive and negative converter dc bus, a voltage step in multilevel converters is only a fraction of the converter dc bus voltage. With the small voltage steps, the converter output can track the reference more accurately and has lower distortion compared to traditional two-level converters. Therefore, the requirement for the output filter can be reduced or even eliminated.

In multilevel converters, the converter output is determined by the switching states of multiple switch pairs. The converter output changes more frequently than each single switch pair, with proper modulation methods such as the phase disposition modulation or the phase shift modulation [27]. The converter has an equivalent switching frequency higher than the actual device switching frequency, achieving high quality output and low device switching loss at the same time.

With the smaller voltage steps, the multilevel converters intrinsically have lower common mode voltage and low output *dv/dt* compared to two-level converters. Moreover, with more switching states, multilevel converters have the flexibility to further reduce or even eliminate the common mode voltage [28]-[30].

While the multilevel converters have such significant advantages that they are usually the preferred topology choices in MV systems, they have some drawbacks and challenges. An obvious drawback is the large number of switching devices and internal capacitors, as well as the corresponding auxiliary circuits such as gate driving circuits and sensing circuits. In addition, the switching devices and capacitors may have different voltage ratings, current ratings, or loss profiles, limiting the modularity of some topologies [31], [32]. When the number of converter voltage levels increases, the component count, footprint, cost, control complexity all increase, which may comprise the performance of the converter or even make the converter realization impractical [33].

In multilevel converters, the multiple output voltage levels and reduced device voltage stressed are achieved by having capacitors as internal energy storage and connecting them to the converter output and to switching devices in different ways. Therefore, it is essential that all the capacitor voltages are around the rated values at all time so that the converter can have high quality output and all the components in the converter operate within the safe condition. However, as the capacitors are connected in turn to the converter output, they are charged, discharged, and bypassed alternatively. The capacitor voltages may have large ripples or even offsets from the rated values. Additional balancing circuits [34], [35], capacitor voltage control methods [36]-[38], capacitors with high capacitance values are some common measures to ensure good capacitor voltages.

1.3 SiC MOSFET

SiC is one of the wide bandgap materials and has several superior physical properties compared to Si including nearly three times the bandgap energy, ten times the breakdown field strength, twice the saturation drift velocity, more than twice the thermal conductivity [39]. SiC MOSFET is the most popular type of SiC switches because of its controlled turn-on and turn-off, and “normal-off” feature. Although SiC MOSFET prototypes were reported in the 1990s [40], [41], the first commercial product was not released until in 2011 [42].

One of the most significant advantages of SiC MOSFETs is the high switching speed. Compared to Si switches, SiC MOSFETs have higher saturation drift velocity and lower input capacitance, and therefore higher switching speed [43], [44]. With a faster switching transition, the duration of voltage-current overlap is shorter, therefore the related loss is lower. The fast switching speed and the lower switching loss of SiC MOSFETs contribute to the capability of operating at high switching frequency. With high switching frequencies, the size of passive components can be reduced, and the power density can be increased [45], [46].

The high critical electric field of SiC enables the SiC switches to achieve high breakdown voltage ratings. The device layer can be made thinner at the same breakdown voltage level, reducing the on-state resistance and therefore the conduction loss, and leading to lower parasitic capacitances and therefore higher switching speed and lower switching loss [44], [47]. 15 kV SiC MOSFETs have been reported while the highest voltage for Si IGBT is limited to 6.5 kV with reasonable performance [48]-[50]. With SiC MOSFETs, the converter voltage rating can be increased.

SiC MOSFETs have high maximum junction temperature of over 200 °C compared to typically 125 °C for Si IGBTs [51]-[53]. The high maximum junction temperature, together with the reduced losses and better thermal conductivity, largely reduces the cooling requirement for SiC MOSFETs, increasing the power density of the system [47], [54]. The superb thermal performance also enables SiC MOSFETs to operate in harsh environments that was previously impossible with Si devices.

The benefits of using SiC MOSFETs in MV converters have been proved to achieve much lower losses, better efficiency and smaller system size compared to using Si IGBTs or Si MOSFETs [53], [55]-[61].

However, high switching speeds of SiC MOSFETs also bring challenges. In power converters, parasitic inductors and parasitic capacitors always exist. Despite the extremely low inductance or capacitance values, they may have significant impact on the device switching performance with high *dv/dt* and *di/dt* of SiC MOSFETs during the switching transitions. Specifically, the parasitic inductor in a switching commutation loop experiences high *di/dt*, introducing voltage overshoot and brings extra voltage stress. The parasitic inductor resonates with the parasitic capacitors of devices and the parasitic capacitor of the load inductor, causing high-frequency oscillation, leading to higher switching loss [62]-[64]. The common source parasitic inductor shared by the commutation loop and the driving loop affects the device gate-source voltage and contributes to the voltage overshoot and extra switching loss [65], [66].

Another main challenge when using SiC MOSFETs is dealing with increased Electromagnetic Interference (EMI) emission. In power converters, parasitic capacitor exists between any two closely located conductors. The parasitic capacitors experience high *dv/dt* during switching transitions and are the main coupling paths of conducted EMI emission. Both the high switching speeds and the high switching frequency of SiC MOSFETs significantly increase the EMI emission, the former in the very high frequency range and the latter in a broader frequency range [67]-[69]. Furthermore, the high-frequency voltage and current ringing during switching transitions also adds to the EMI emission [62]. If not considered or attenuated, the high EMI may interrupt the correct function of the converter, or other components connected to the converter [59], [70], [71].

1.4 SiC-Based Multilevel Converter

Multilevel converters are promising topology candidates for MV systems and SiC MOSFETs are promising switching device candidates for MV systems. Therefore, it can be expected that SiC-based multilevel converters are promising solutions as the power converters in MV systems.

In SiC-based multilevel converters, the benefits and challenges of multilevel topologies, and the benefits and challenges of SiC MOSFETs are coupled together. Some of the overall performances are clear, for example: the reduced device voltage requirement feature of multilevel topologies and the high breakdown voltage rating of SiC MOSFETs help SiC-based multilevel converters to achieve high converter voltage ratings [72]-[76]; the small voltage steps, the increased equivalent switching frequency of multilevel topologies and the high switching frequency capability of SiC MOSFETs help SiC-based multilevel converters to achieve excellent output quality and reduced sizes of passive components [77]-[81]. Some of the overall performances are not so clear, for example: the large number of switching devices in multilevel converters complicate the EMI emissions; the high switching speeds and high switching frequency operation of SiC MOSFETs may affect the converter operation condition and control.

Most of the popular multilevel topologies [19]-[23] were proposed nearly a decade or even several decades before the commercialization of SiC MOSFETs. They were proposed to be realized with Si switching devices and that has been the case for decades. With the unique properties of SiC MOSFETs, the multilevel converter topologies need to be reexamined.

1.5 Dissertation outline

When employing multilevel topologies and using SiC MOSFETs as switching devices, it is important to explore how their features affect each other, how to fully exploit the advantages and how to handle the challenges, which are the focuses of the study. Specifically, with the high switching speeds and high switching frequency operation of SiC MOSFETs, and the large number of switches and capacitors in multilevel topologies, SiC-based multilevel converters need to be studied while considering high-frequency voltage and current behaviors and the interactions among them at different locations.

In Chapter 1, the research background and motivation are introduced.

In Chapter 2, a three-phase inverter is designed and built for the high-speed motor drive application. The benefits and challenges of using multilevel converter topology and using SiC MOSFETs for this application are explored. A fitting topology is selected, and a prototype is designed, both with attentions paid to deal with the high switching speeds of SiC MOSFETs. The inverter is verified through experiments to meet all specifications with a high efficiency.

In Chapter 3, a unique type of converter, converters with Integrated Capacitor Blocked Transistor (ICBT) cells are studied. The ideal operation principle is analyzed and verified by the simulation results. Then the impacts of non-idealities on the operation are analyzed. The cell capacitor voltage unbalance mechanisms are analyzed, based on which a control method is proposed for this type of converter. The analyses and the proposed control method are verified by experimental results.

In Chapter 4, the conducted EMI emission is analyzed, which is one of the biggest challenges when using SiC MOSFETs. Four SiC-based multilevel converters are studied, with the focus on the power circuit in one converter and the auxiliary circuits in the other three converters. The complexity of noise generation and propagation in multilevel converters is presented. The conducted EMI disturbances are experimentally evaluated, analyzed, and effectively mitigated in all four cases.

Chapter 5 summarizes the work and presents the plan of future work.

Chapter 2. Design of a Five-Level Stacked Multicell Converter for High-Speed Motor Drive Application

In this chapter, a three-phase five-level Stacked Multicell Converter (SMC) using SiC MOSFETs is designed for high-speed motor drives. The specifications of the prototype are shown in Tab. 2-1.

Tab. 2-1 Specifications of the inverter prototype.

Parameter	Value
Active Power	5 kW
DC Bus Voltage	750 V
Output Line RMS Voltage	460 V
Output Frequency	600 ~ 3000 Hz

2.1 Introduction

High-speed motors have been widely used in industrial applications such as flywheel energy storage systems [82]-[86], compressors [87]-[91], aerospace systems [92]-[96], railway systems [97]-[101], automotive systems [102]-[105] and so on. Compared to 50 Hz or 60 Hz drives, high-speed motor systems have lower weights and volumes, therefore can achieve higher power densities [106].

One major challenge of high-speed motor drives is generating high quality output voltages at high output frequencies, especially with the low inductances of the high-speed motors. Otherwise, the output currents will have high ripples, leading to high losses in the machines [107]. The switching frequency of Si switching devices is limited to around 20 to 30 kHz. Together with the traditional two-level topology, this solution cannot generate high quality output voltages beyond several kilohertz. Therefore, passive filters, such as LC filters, are required at the inverter outputs to limit the magnitudes of the harmonics in the currents [108].

Multilevel converters have small voltage steps and high equivalent switching frequencies while keeping low device switching frequencies. Both features lead to higher output quality compared to the two-level converter and therefore are good topology candidates for the application [109], [110].

On the other hand, SiC MOSFETs have higher switching speeds and lower switching losses compared to traditional Si devices. When using SiC MOSFETs, the switching frequency of the converter can be increased to improve the output quality with similar or even lower switching losses compared to when using Si devices. SiC MOSFETs are good device candidates for the application [111].

Another major challenge of high-speed motor drives is restraining the over-voltages along the motor cables caused by the voltage reflection, otherwise the over-voltages may lead to insulation deterioration and high bearing currents [112], [113]. The voltage reflection phenomenon generally exists in all motor drive systems but is more serve in high-speed motor drives where the switching frequencies are high and the switching pulses are short [114]. The voltage on the motor terminal could be the result of several voltage pulses at the inverter terminal, instead of being the result of one voltage step change at the inverter terminal. Similar with when trying to meet the harmonic requirement, passive filters, such as LC filters, RC filters, RLC filters, are required at the inverter outputs to limit the *dv/dt* of the voltages applied to the motor cables [115]-[119].

The small voltage steps of multilevel converters not only improve the output quality, but also reduce the over-voltage, as the magnitudes of voltage step changes at the inverter terminal are smaller. The detailed comparison will be shown later in Section 2.2.1.

However, the short turn-on time and turn-off time of SiC MOSFETs will increase the over-voltage, as the voltage overshoot increases with shorter rise time or fall time of the voltage pulses [119]. When using SiC MOSFETs in high-speed motor drive applications, additional measures need to be taken to address the over-voltage concern.

Meanwhile, like any power electronics systems, a high efficiency is desired. In the motor drive system in [120], the inverter has an efficiency of 97%, the filter has an efficiency of 98%, the motor has an efficiency of 93%, and the overall system efficiency is 88%. In the motor drive system in [121], the semiconductor loss in the inverter is 0.50% of the total power, the loss of the inverter filter is 0.41% of the total power. The semiconductor loss is usually the main contributor of the losses in the inverter and can be potentially reduced employing SiC MOSFETs. The loss of the filters is usually less than but comparable to the semiconductor loss. In addition, the use of filters introduces additional loss in the inverter because of the charging and discharging currents of the filtering capacitors [113]. If the designed converter can reduce or eliminate the requirements of the filters, the loss and volume of the filters can be reduced or eliminated. Both the efficiency and the power density of the system can be improved.

Therefore, the objective of this design is to achieve a high efficiency, high power density high-speed motor drive with the specifications listed in Tab. 2-1 while meeting both the power quality requirement and the over-voltage restraint. Specifically, the output current should have a Total Harmonic Distortion (THD) of less than 5% when considering up to 20th order harmonics, and the maximum voltage value on the motor terminal should be less than twice of the dc bus voltage value.

2.2 Topology Selection

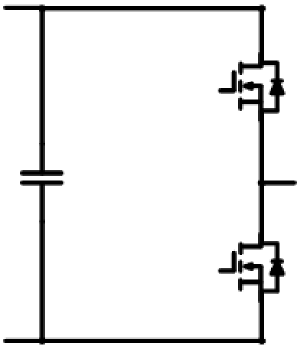
In this section, multilevel converter topologies with different numbers of voltage levels are first compared with the traditional two-level converter topology. Then different topologies with the same number of voltage levels are compared. One topology is selected eventually, and its operation principle is explained.

2.2.1 Comparison of Topologies with Different Voltage Levels

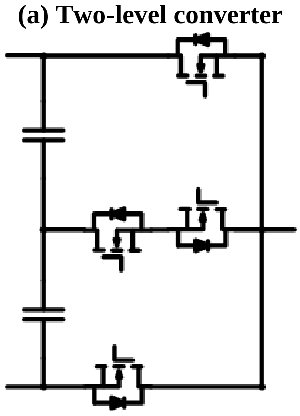
Two-level converter, three-level converter and five-level converter are compared through simulations with the focus on the output quality and the maximum over-voltage at the motor terminal.

One phase leg of a two-level converter is shown in Fig. 2-1(a). The three-level T-type converter is chosen as the representative of three-level converters, with one phase leg shown in Fig. 2-1(b). The five-level SMC is chosen as the representative of five-level converters, with one phase leg shown in Fig. 2-1(c). Most of the other three-level topologies and five-level topologies have similar performance in terms of output voltages, when compared to three-level T-type converter and five-level SMC respectively.

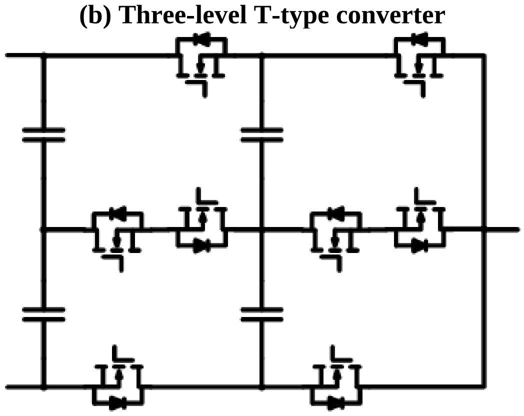
Three converters are simulated in MATLAB / Simulink with the same specifications, which are shown in Tab. 2-1, the same device switching speed of 20 V/ns and the same device switching frequency of 40 kHz. 4-meter motor cables are connected between the converter and the motor, and each cable is represented by a 10-section distributed parameter model [119]. The three-phase motor is represented by a high frequency model [118].



(a) Two-level converter



(b) Three-level T-type converter

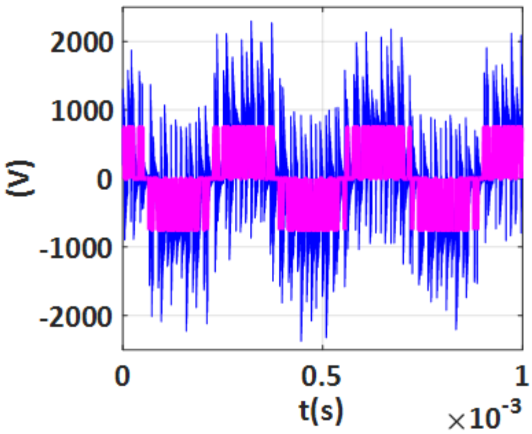


(c) Five-level Stacked Multicell Converter

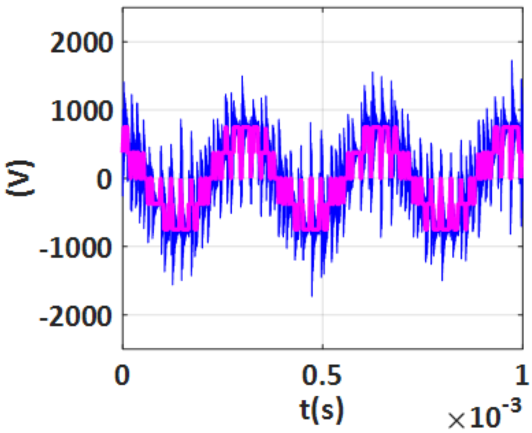
Fig. 2-1 Topologies of converters with different numbers of voltage levels.

The simulation results are shown in Fig. 2-2 and Tab. 2-2. In each subfigure, the pink waveform represents the line-to-line voltage at the inverter terminal, which always has a maximum magnitude of dc bus voltage, 750 V.

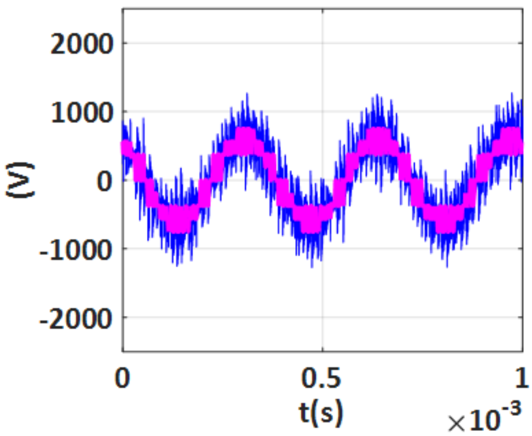
For the three topologies, the phase output voltage has two, three and five voltage levels respectively and therefore the line-to-line output voltage has three, five and nine voltage levels respectively. The magnitude of the voltage step decreases, and the output quality increases with a higher number of output voltage levels. The latter can be clearly observed from output voltage THD and output current THD in Tab. 2-2.



(a) Two-level converter



(b) Three-level T-type converter



(c) Five-level Stacked Multicell Converter

Fig. 2-2 Line-to-line voltages at inverter terminal and motor terminal.

Tab. 2-2 Topology comparison results.

	Two-Level Converter	Three-Level T-Type	Five-Level SMC
Output Voltage THD	71.9%	43.3%	26.3%
Output Current THD	15.6%	10.0%	3.8%
Maximum Over-Voltage p.u.	3.06	2.25	1.73

In each subfigure of Fig. 2-2, the blue waveform represents the line-to-line voltage at the motor terminal, which has a larger value than the voltage at the inverter terminal because of the voltage reflection. As the magnitude of the voltage step decreases with a higher number of output voltage levels, the maximum over-voltage value at the motor terminal is reduced.

With the superb output performance of the five-level converter, the requirements of the power quality filter and the over-voltage mitigation filter can both be largely reduced. With the specifications and the requirements of this study, the over-voltage mitigation filter is not needed when employing the five-level converter topology. The power quality filter is not needed either with the five-level converter topology and the selected switching frequency, which will be shown later in Section 2.3.1. Therefore, the five-level converter topology is selected over the two-level topology and the three-level topology.

2.2.2 Comparison of Different Five-Level Topologies

Different five-level topologies are compared. All the following topologies have the same output voltages, and therefore the same output quality and the same maximum over-voltages. However, different topologies may have different numbers of switching devices and capacitors, and different ratings of switching devices and capacitors. They could be controlled by different modulation methods and may also have different losses.

Fig. 2-3 and Tab. 2-3 shows the configuration and the switching states of one five-level Active Neutral Point Clamped (ANPC) converter [21] phase leg respectively. The phase leg is equivalently a three-level Neutral Point Clamped (NPC) inner cell and a three-level Flying Capacitor (FC) outer cell, and has two dc capacitors and one flying capacitor. The output voltage is defined as the voltage from the middle point of the dc bus to the output terminal.

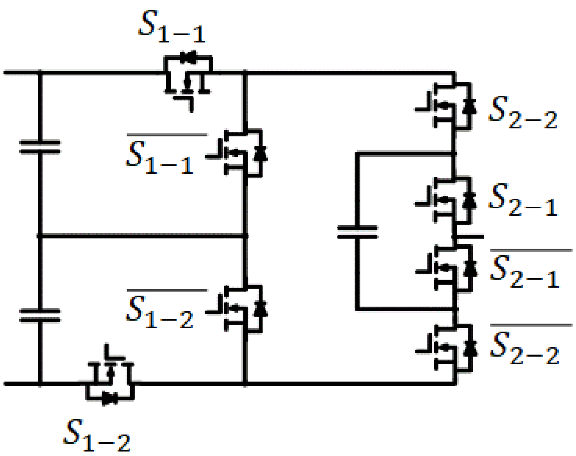


Fig. 2-3 Configuration of one five-level ANPC converter phase leg.

Tab. 2-3 Switching states of one five-level ANPC converter phase leg.

S_{1-1}	S_{1-2}	S_{2-1}	S_{2-2}	V_{out}
1	0	1	1	$V_{dc}/2$
1	0	1	0	$V_{dc}/4$
1	0	0	1	$V_{dc}/4$
1	0	0	0	0
0	1	1	1	0
0	1	1	0	$-V_{dc}/4$
0	1	0	1	$-V_{dc}/4$
0	1	0	0	$-V_{dc}/2$

In a five-level ANPC phase leg, the four switching devices in the outer cell, S_{2-1}, $\overline{S_{2-1}}$, S_{2-2} and $\overline{S_{2-2}}$, switch at the switching frequency. The four switching devices in the inner cell, S_{1-1}, $\overline{S_{1-1}}$, S_{1-2} and $\overline{S_{1-2}}$, switch at the line frequency, and have lower switching losses.

As mentioned in Section 1.3, when employing SiC MOSFETs, it is very important to minimize the commutation loops to minimize the issues caused by the high switching speeds. In a five-level ANPC phase leg, some switching transitions involve longer commutation loops than the other switching transitions. For example, during the transition between the first and the second state in Tab. 2-3, the current path changes between the path of $S_{1-1} - S_{2-2} - S_{2-1}$ and the path of $\overline{S_{1-2}} - \overline{S_{2-2}} - S_{2-1}$. Therefore, switch S_{1-1}, $\overline{S_{1-2}}$, S_{2-2} and $\overline{S_{2-2}}$ need to be placed close to each other to reduce the parasitic inductance of the commutation loop. Similarly, switch $\overline{S_{1-1}}$, S_{1-2}, S_{2-2} and $\overline{S_{2-2}}$ need to be placed close considering the transition between the sixth and the eighth states. Then six switches, S_{1-1}, $\overline{S_{1-1}}$, S_{1-2}, $\overline{S_{1-2}}$, S_{2-2} and $\overline{S_{2-2}}$, all need to be placed close together. In addition, every device needs to have its own driving circuit nearby and needs good heat dissipation. It is hard to achieve all three at the same time in practice.

Fig. 2-4 and Tab. 2-4 shows the configuration and the switching states of one five-level Switch Gear Cell (SGC) converter [122] phase leg respectively. The phase leg is equivalently a three-level T-type inner cell and a three-level H-bridge outer cell, and has two dc capacitors and one flying capacitor.

In a five-level SGC phase leg, two of the switching devices in the outer cell, S_{2-1} and $\overline{S_{2-1}}$, switch at the line frequency. The other two switching devices in the outer cell, S_{2-2} and $\overline{S_{2-2}}$, switch at the switching frequency. The four switching devices in the inner cell, S_{1-1}, $\overline{S_{1-1}}$, S_{1-2} and $\overline{S_{1-2}}$, switch at the switching frequency, but each pair only switches in either the positive half or the negative half of the line cycle.

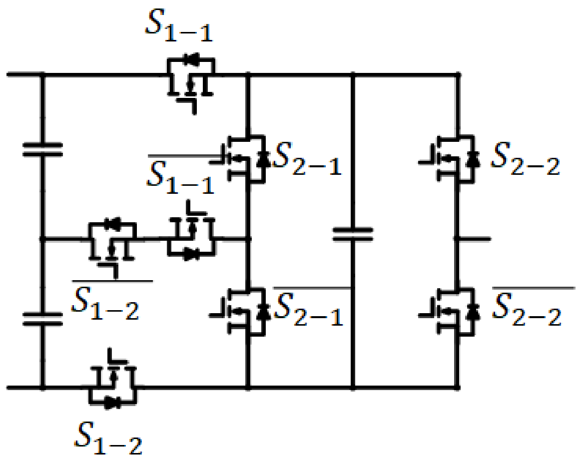


Fig. 2-4 Configuration of one five-level SGC converter phase leg.

Tab. 2-4 Switching states of one five-level SGC converter phase leg.

S_{1-1}	S_{1-2}	S_{2-1}	S_{2-2}	V_{out}
1	0	0	1	$V_{dc}/2$
1	0	0	0	$V_{dc}/4$
0	0	0	1	$V_{dc}/4$
0	0	0	0	0
0	0	1	1	0
0	0	1	0	$-V_{dc}/4$
0	1	1	1	$-V_{dc}/4$
0	1	1	0	$-V_{dc}/2$

The SGC converter also suffers from long commutation loops which involve switching devices in both the inner cell and the outer cell. Specifically, during the transition between the second and the fourth state in Tab. 2-4, the current path changes between the path of $S_{1-1} - \overline{S_{2-2}}$ and the path of $\overline{S_{1-2}} - \overline{S_{1-1}} - \overline{S_{2-1}} - \overline{S_{2-2}}$. Therefore, switch S_{1-1}, $\overline{S_{1-1}}$, $\overline{S_{1-2}}$, and $\overline{S_{2-1}}$ need to be placed close to each other to reduce the parasitic inductance of the commutation loop. Similarly, switch $\overline{S_{1-1}}$, S_{1-2}, $\overline{S_{1-2}}$ and S_{2-1} need to be placed close considering the transition between the fifth and the seventh states. Then six switches, S_{1-1}, $\overline{S_{1-1}}$, S_{1-2}, $\overline{S_{1-2}}$, S_{2-1}, and $\overline{S_{2-1}}$ all need to be placed close. It is hard to achieve a good layout design. In addition, two devices in the inner cell, S_{1-1} and S_{1-2}, have high voltage stress of three quarters of the dc bus voltage.

Fig. 2-5 and Tab. 2-5 shows the configuration and the switching states of one five-level SMC converter [123] phase leg respectively. The phase leg has two stacks and two cells, is equivalently two three-level T-type cells connected in series, and has two dc capacitors and two flying capacitors.

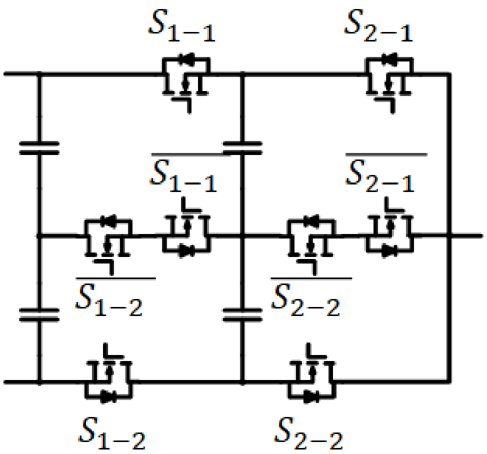


Fig. 2-5 Configuration of one five-level SMC converter phase leg.

Tab. 2-5 Switching states of one five-level SMC converter phase leg.

S_{1-1}	S_{1-2}	S_{2-1}	S_{2-2}	V_{out}
1	0	1	0	$V_{dc}/2$
1	0	0	0	$V_{dc}/4$
0	0	1	0	$V_{dc}/4$
0	0	0	0	0
0	0	0	1	$-V_{dc}/4$
0	1	0	0	$-V_{dc}/4$
0	1	0	1	$-V_{dc}/2$

In a five-level SMC phase leg, all eight switching devices switch at the switching frequency, but each pair only switches in either the positive half or the negative half of the line cycle.

In a SMC phase leg, each switching transition always only happens inside either the inner cell or the outer cell, and always only happens either between the positive path and the middle path, or between the middle path and the negative path. Therefore, only the four devices in a cell need to be placed close, and the placement of the devices in different cells are not critical. This significantly simplifies the layout design.

Fig. 2-6 and Tab. 2-6 shows the configuration and the switching states of another version of five-level SMC converter [123] phase leg respectively. The phase leg is equivalently a three-level T-type inner cell and a three-level NPC outer cell, and has two dc capacitors and two flying capacitors.

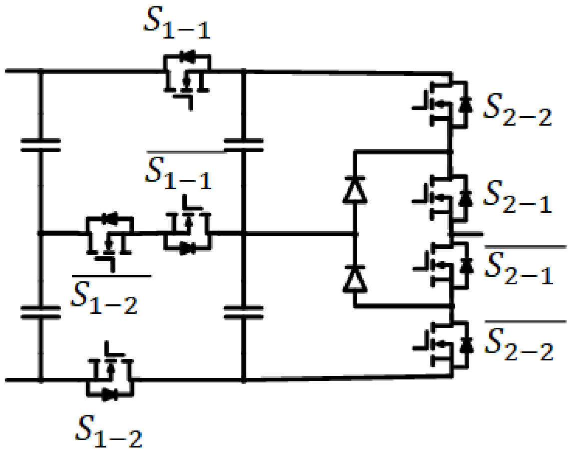


Fig. 2-6 Configuration of one five-level SMC converter phase leg with an NPC outer cell.

The switching states for the two types of five-level SMC listed in Tab. 2-5 and Tab. 2-6 are the same. Despite the different configuration, the modulation is the same. In a five-level SMC phase leg with an NPC outer cell, all eight switching devices switch at the switching frequency, but each pair only switches in either the positive half or the negative half of the line cycle. The advantage of this version of topology is that the voltage stresses of two switching devices in the outer cell, S_{2-1} and S_{2-2}, are reduced from half of the dc bus voltage to a quarter of the dc bus voltage. Lower rated switching devices can be used. However, the two diodes bring additional losses.

Tab. 2-6 Switching states of one five-level SMC converter phase leg with an NPC outer cell.

S_{1-1}	S_{1-2}	S_{2-1}	S_{2-2}	V_{out}
1	0	1	0	$V_{dc}/2$
1	0	0	0	$V_{dc}/4$
0	0	1	0	$V_{dc}/4$
0	0	0	0	0
0	0	0	1	$-V_{dc}/4$
0	1	0	0	$-V_{dc}/4$
0	1	0	1	$-V_{dc}/2$

In a five-level SMC phase leg with an NPC outer cell, the switching transition also only happens inside one cell. Only the four devices in a cell need to be placed close, and the placement of the devices in different cells are not critical.

Fig. 2-7 and Tab. 2-7 shows the configuration and the switching states of one five-level Flying Capacitor converter [22] phase leg respectively. It is another version of five-level SMC as well, with one stack and four cells.

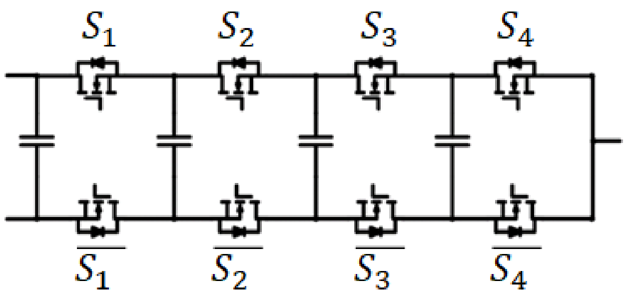


Fig. 2-7 Configuration of one five-level FC converter phase leg.

In a five-level FC phase leg, all eight switching devices switch at the switching frequency. However, the switching frequency should be halved when compared to the other topologies to keep the same equivalent switching frequency. All devices only need to block one quarter of the dc bus voltage. But the topology suffers from additional conduction losses as well because the phase leg always has four devices conducting at the same time.

Tab. 2-7 Switching states of one five-level FC converter phase leg.

S_1	S_2	S_3	S_4	V_{out}
1	1	1	1	$V_{dc}/2$
1	1	1	0	$V_{dc}/4$
1	1	0	1	$V_{dc}/4$
1	0	1	1	$V_{dc}/4$
0	1	1	1	$V_{dc}/4$
1	1	0	0	0
1	0	1	0	0
1	0	0	1	0
0	1	1	0	0
0	1	0	1	0
0	0	1	1	0
1	0	0	0	$-V_{dc}/4$
0	1	0	0	$-V_{dc}/4$
0	0	1	0	$-V_{dc}/4$
0	0	0	1	$-V_{dc}/4$
0	0	0	0	$-V_{dc}/2$

As a summary, all the above five topologies have eight active switching devices per phase leg. They have the same output voltages, same number of switching transitions, and then similar total switching losses. The ANPC and SGC have some long commutation loops while the three versions of SMC only have short commutation loops. The SMC with an NPC outer cell and the FC are able to reduce the voltage rating requirements for some switches but have higher total conduction losses. Therefore, the original five-level SMC with two stacks and two cells is selected as the inverter topology in this study.

2.2.3 Operation Principle of Five-Level Stacked Multicell Converter

Fig. 2-5 and Tab. 2-5 already shows the configuration and the switching states of one five-level SMC converter phase leg respectively. More details about its operation will be explained.

For a three-phase SMC converter, three phase legs share the dc bus and two dc bus capacitors. The rated voltage of each dc bus capacitor is half of the dc bus voltage. Each phase leg has two flying capacitors. The rated voltage of each flying capacitor is one quarter of the dc bus voltage.

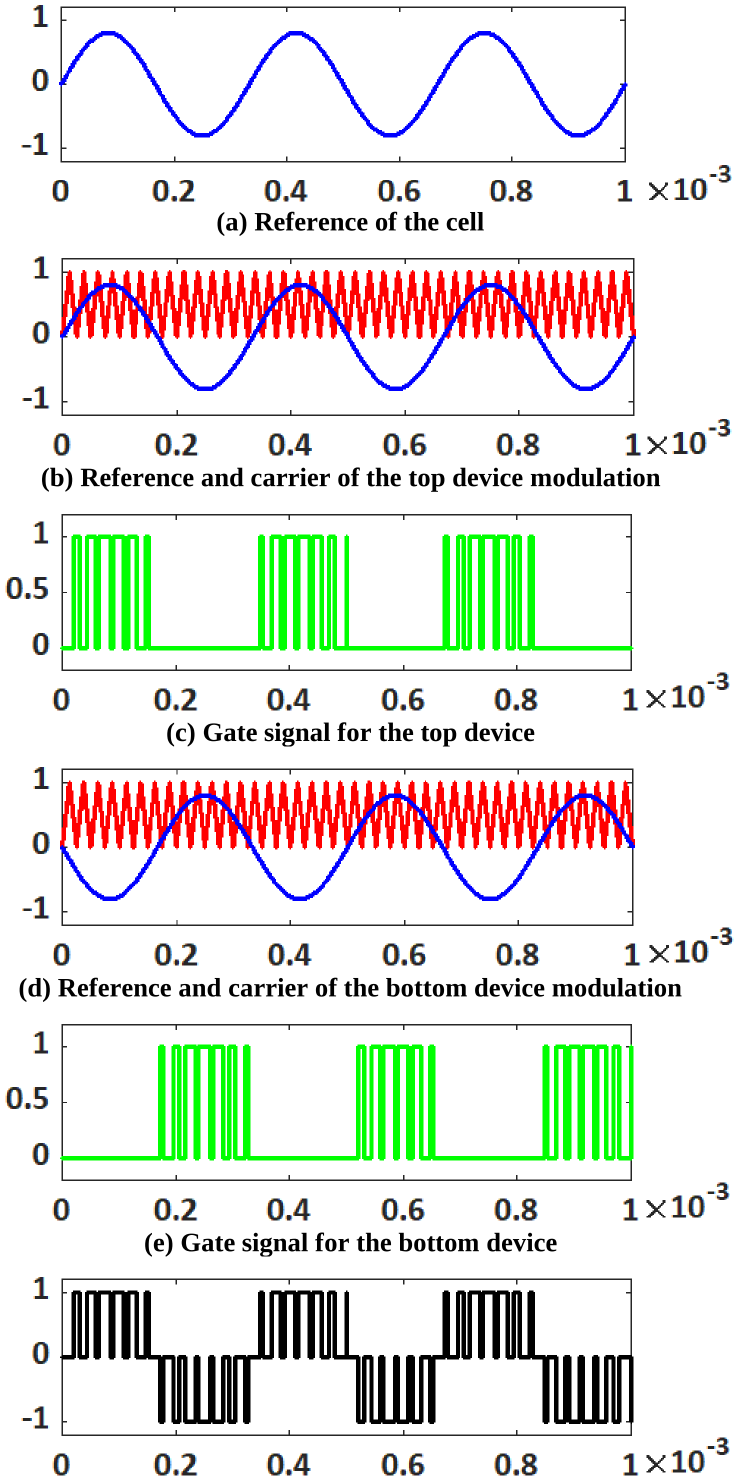
Each phase leg has eight switching devices. With the switching states shown in Tab. 2-5, the maximum voltage stress for each top device or bottom device is half of the dc bus voltage, the maximum voltage stress for each middle device is one quarter of the dc bus voltage.

The modulation of a three-level T-type phase leg is applied to each cell. The modulation of the inner cell is shown in Fig. 2-8. Fig. 2-8(a) shows the ac reference of the cell. Fig. 2-8(b) shows the reference and the triangular carrier of the modulation for the top device S_{1-1}, where the reference of the top device is the same as the reference of the cell. Fig. 2-8(c) shows the resulting gate signal for the top device. Fig. 2-8(d) shows the reference and the triangular carrier of the modulation for the bottom device S_{1-2}, where the reference of the bottom device is the reverse of the reference of the cell, and the carrier of the bottom device is the same as the top device. Fig. 2-8(e) shows the resulting gate signal for the bottom device. Fig. 2-8(f) shows the resulting output voltage of the inner cell in per unit, when ignoring the voltage ripples on the dc capacitors and the flying capacitors, which equals to:

$$V_{out1,pu} = S_{1-1} - S_{1-2} \tag{2-1}$$

The output voltage of the inner cell equals to:

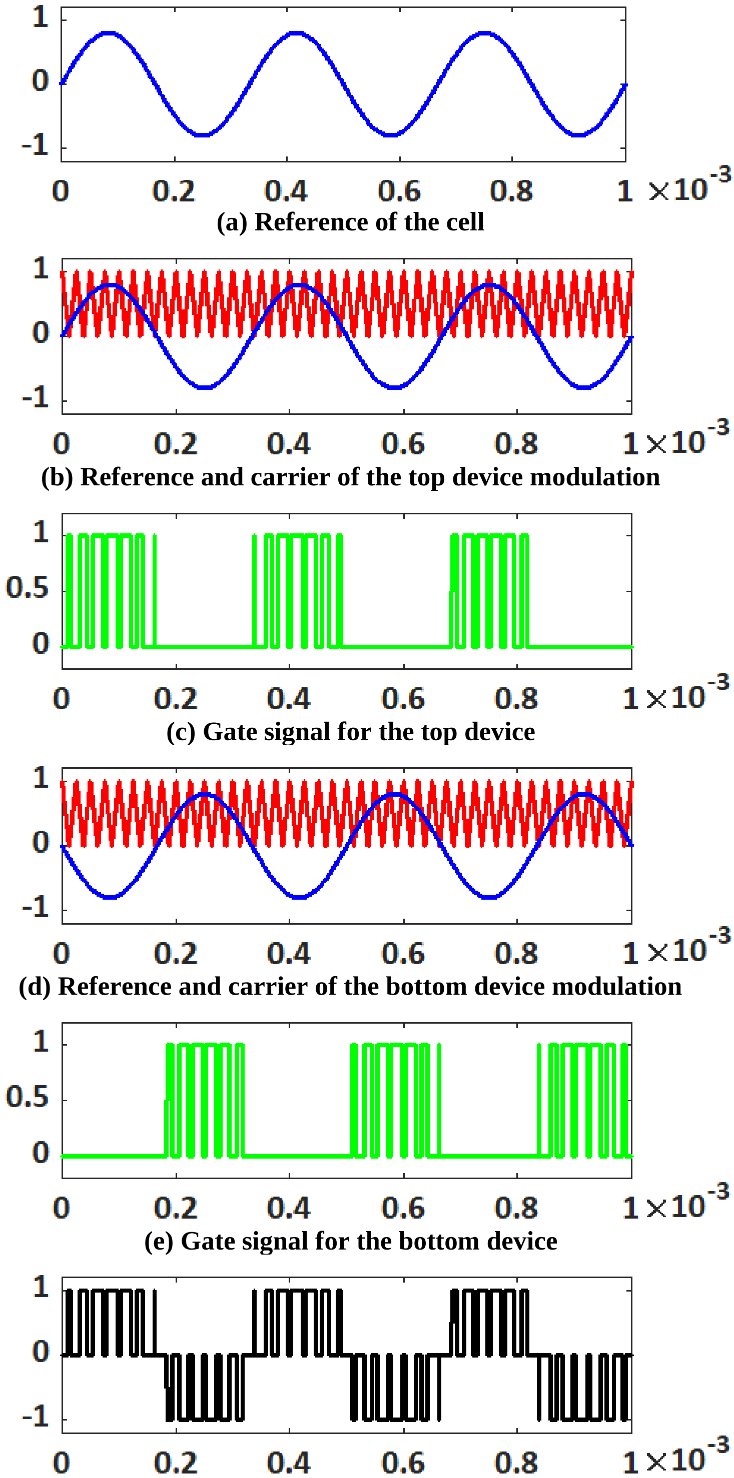
$$V_{out1} = V_{out1,pu} \times \frac{V_{dc}}{4} \tag{2-2}$$



(a) Reference of the cell
(b) Reference and carrier of the top device modulation
(c) Gate signal for the top device
(d) Reference and carrier of the bottom device modulation
(e) Gate signal for the bottom device
(f) Output voltage of the cell in per unit

Fig. 2-8 Modulation of the inner cell.

The modulation of the outer cell is shown in Fig. 2-9. The outer cell shares the same ac reference, but the triangular carriers have 180° phase shift compared to the inner cell.



(a) Reference of the cell
(b) Reference and carrier of the top device modulation
(c) Gate signal for the top device
(d) Reference and carrier of the bottom device modulation
(e) Gate signal for the bottom device
(f) Output voltage of the cell in per unit

Fig. 2-9 Modulation of the outer cell.

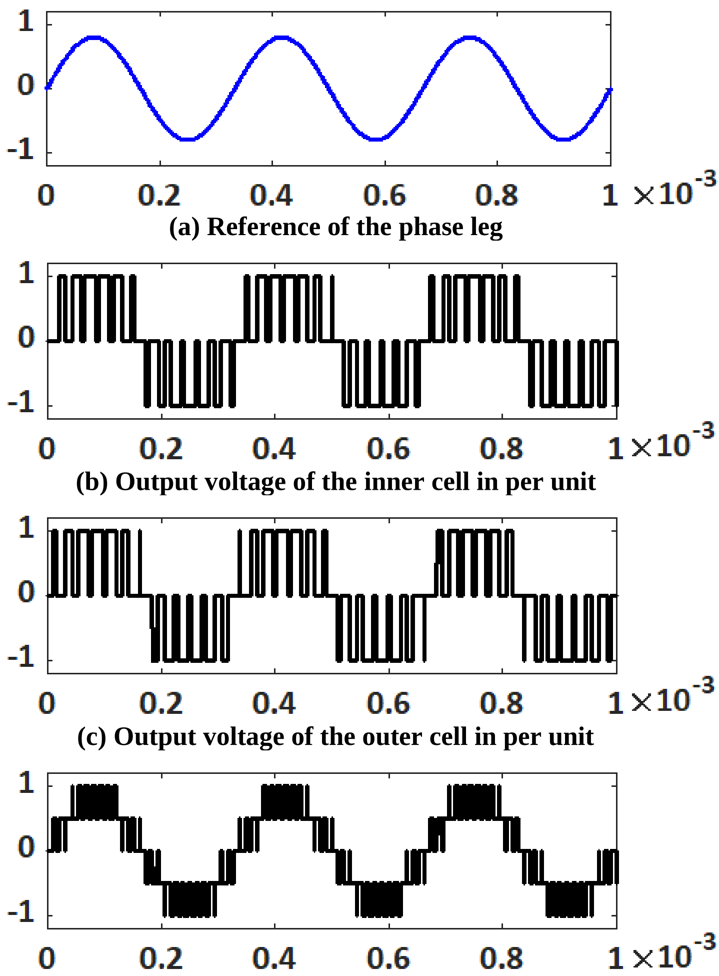
Fig. 2-10 shows the ac reference of the phase leg, the output voltages of the two cells in per unit, and the phase leg output voltage in per unit. The ac reference is the same for the phase leg and the two cells. The phase leg output voltage in per unit equals to:

$$V_{out,pu} = \frac{(V_{out1,pu} + V_{out2,pu})}{2} \tag{2-3}$$

The output voltage of the phase leg equals to:

$$V_{out} = V_{out,pu} \times \frac{V_{dc}}{2} \tag{2-4}$$

$$V_{out} = V_{out1} + V_{out2} \tag{2-5}$$



(a) Reference of the phase leg

(b) Output voltage of the inner cell in per unit

(c) Output voltage of the outer cell in per unit

(d) Output voltage of the phase leg in per unit

Fig. 2-10 Modulation of a SMC phase leg.

The output voltage of each cell has three voltage levels and follows the ac reference. The output voltage of the phase leg has five voltage levels and follows the ac reference. The phase-shifted modulation equivalently doubles the switching frequency. The output voltage always switches between the two nearest voltage levels, resulting in the highest output quality and the lowest voltage step changes. At the same time, the natural balancing of the flying capacitor voltages is theoretically ensured [34], [124].

2.3 Prototype Design

After the topology is selected and with the understanding of the converter operation, a prototype is designed while meeting the specifications and requirements.

2.3.1 Switching Frequency Selection

A higher switching frequency helps to improve the output voltage quality but meanwhile increases the switching losses of the switching devices. It also affects the flying capacitor design. Fig. 2-11 shows the relationship between the switching frequency and the output current THD at 3 kHz output line frequency without any additional filters. The inductance on the load side 0.5 mH per phase, which is the impedance of the motor. The output current THD values are acquired based on the inverter simulation results in MATLAB / Simulink.

The switching frequency is selected to be 40 kHz to meet the output current THD requirement of 5%, while also limiting the device switching losses.

2.3.2 Capacitor Selection

The voltage rating of each dc capacitor needs to be higher than half of the dc bus voltage, 375 V. The voltage rating of each flying capacitor needs to be higher than a quarter of the dc bus voltage, 187.5 V. The capacitances are selected to limit the voltage ripples so that the output voltages have high quality.

Equation (2-6) and (2-7) show the relationship between two dc capacitor currents. $i_{c,dc,p}$ is the current through the positive dc capacitor, $i_{c,dc,n}$ is the current through the negative dc capacitor. $i_{m,a1}$ is the current through the middle path of the inner cell in phase a, which is the drain current of switch $\overline{S_{1-2}}$ in phase a. $i_{m,b1}$ and $i_{m,c1}$ is the current through the middle path of the inner cell in phase b and in phase c respectively.

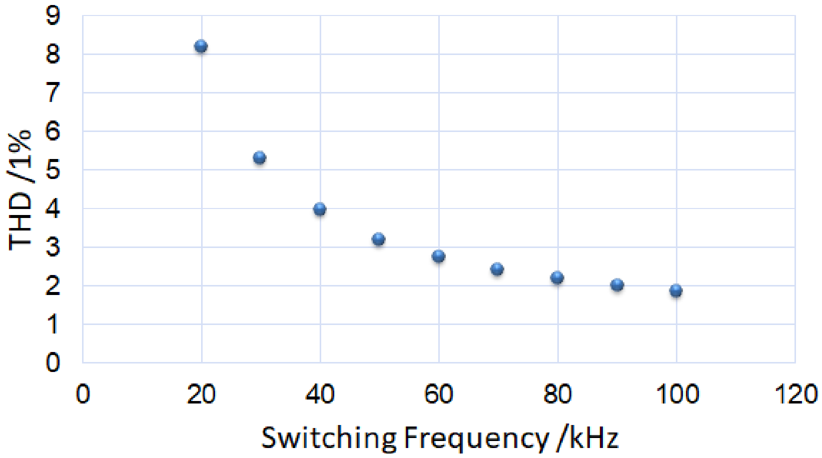


Fig. 2-11 Output current THD at 3 kHz line frequency without filters.

$$i_{c,dc,p} + i_{c,dc,n} = 0 \tag{2-6}$$

$$i_{c,dc,p} - i_{c,dc,n} = i_{m,a1} + i_{m,b1} + i_{m,c1} \tag{2-7}$$

The sum of the two dc capacitor currents is zero as the total dc bus voltage is kept constant. The difference of the two currents is the three-phase total of inner cell middle path currents, each of which repeats every line cycle and there is 120° phase shift among each other. As a result, each dc capacitor voltage has a ripple at three times of output line frequency, and the magnitude of the ripple decreases with a higher line frequency.

Equation (2-8) shows the current through the positive flying capacitor in phase a, which equals to the difference between the two adjacent top switch currents. $i_{c,fc,ap}$ is the current through the positive flying capacitor in phase a. $i_{t,a1}$ is the current through the top path of the inner cell in phase a, which is the drain current of switch S_{1-1} in phase a. $i_{t,a2}$ is the current through the top path of the outer cell in phase a, which is the drain current of switch S_{2-1} in phase a. $S_{1-1,a}$ is the gate signal for the top switch in the inner cell of phase a, $S_{2-1,a}$ is the gate signal for the top switch in the outer cell of phase a. i_o is the phase leg output current of phase a.

$$i_{c,fc,ap} = i_{t,a1} - i_{t,a2} = \left(S_{1-1,a} - S_{2-1,a}\right) \times i_{o,a} \tag{2-8}$$

As the two top switches have similar duty ratios in each switching cycle, the flying capacitor voltage is approximately balanced in each switching cycle, the magnitude of the ripple decreases with a higher switching frequency. The conclusion applies to all six flying capacitors in three phase legs.

The required capacitances are determined based on the above voltage ripple analyses. 40 μF is required for each dc capacitor so that the voltage difference between the two dc capacitors is less than 5%. Three 22 μF, 450 V film capacitors [125] are connected in parallel for each half of the dc bus.

Fig. 2-12 shows the relationship between the switching frequency and the required capacitance value of the flying capacitor to achieve 2% voltage ripple. The required capacitance is inversely proportional to the switching frequency. With 40 kHz switching frequency, 17 μF is required for each flying capacitor. One 18 μF, 300 V film capacitor [126] is used for each flying capacitor.

2.3.3 Switching Device Selection

The maximum voltage stress of each top or bottom switch is half of the dc bus voltage, 375 V. The maximum voltage stress of each middle switch is a quarter of the dc bus voltage, 187.5

V. Different SiC MOSFET products from Wolfspeed [127] and Rohm [128] are compared. Only the products with availability at the time was considered.

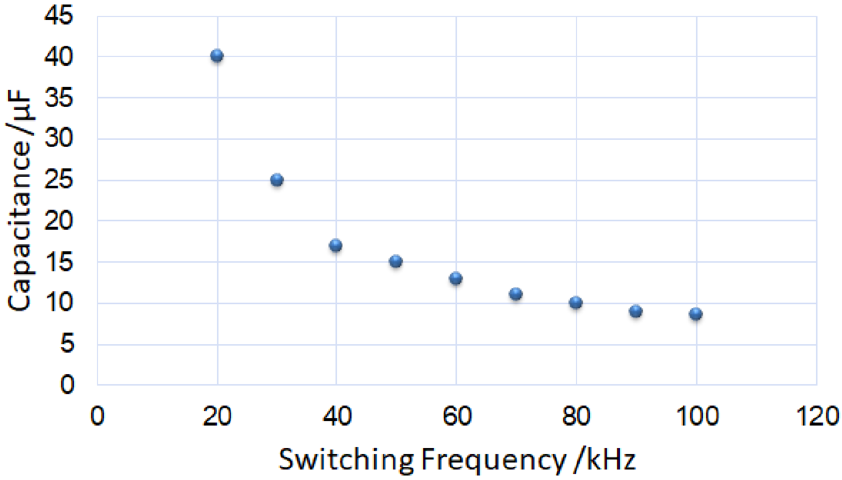


Fig. 2-12 Required capacitance of flying capacitors to achieve 2% voltage ripple.

The voltages across the devices and the currents through the devices are recorded from the circuit simulation in MATLAB / Simulink. Using the recorded data and the loss characteristics in the datasheet, the conduction losses, the switching losses and the driving losses of the devices are calculated in MATLAB. Alternatively, the conduction losses and the switching losses can be directly simulated with the device models in PLECS. The loss estimation results using the two methods are the same.

Tab. 2-8 shows the key ratings and estimated losses of some SiC MOSFETs. The three listed SiC MOSFETs have the lowest total semiconductor loss among all available SiC MOSFETs. It is assumed that the same device is used for all the switches in the converter in each case. The shown losses are the sum of all the twenty-four devices in the converter, with 3 kHz output line frequency. The losses do not change much with the output frequency.

Although the three devices have very similar total loss, the ratios of conduction loss, switching loss and driving loss are quite different. This is expected as a larger die size in the device decreases the on-state resistance and therefore the conduction loss, but increases the parasitic capacitances and therefore the switching loss and the driving loss. This can be taken into consideration when a thorough optimization is conducted. For example, if using C3M0065090J, the switching frequency can be set to be higher to increase the output quality and reduce the required capacitance for flying capacitors without suffering much from additional losses. The C3M0065090J SiC MOSFET from Wolfspeed is selected for low total loss and low cost. In addition, it is a surface-mounted device and therefore is easy for manufacturing.

Tab. 2-8 Switching device comparison of SiC MOSFETs.

Manufacturer	Wolfspeed	Wolfspeed	Rohm
Part Number	C3M0065090J	C2M0025120D	SCT3030AL
Drain-Source Voltage	900 V	1200 V	650 V
Drain Current	35 A	90 A	70 A
Total Conduction Loss	16.99 W	6.54 W	9.15 W
Total Switching Loss	1.55 W	9.17 W	7.80 W
Total Driving Loss	0.54 W	3.89 W	2.25 W
Total Loss	19.08 W	19.60 W	19.20 W

For comparison, the semiconductor losses when using Si MOSFETs are also estimated, with the key ratings and estimated losses shown in Tab. 2-9. The on-state resistance of this device is very similar as the C3M0065090J SiC MOSFET. Therefore, the conduction losses of the two devices are very similar, with the difference being less than 10%. However, the parasitic capacitances of the APT47N60BC3 Si MOSFET, including the input capacitance, the output capacitance, and the reverse transfer capacitance, are ten to forty times higher compared to C3M0065090J SiC MOSFET. Therefore, the switching losses and the driving losses are both more than ten times higher compared to C3M0065090J SiC MOSFET.

Tab. 2-9 Switching device comparison of Si MOSFET.

Manufacturer	Microsemi
Part Number	APT47N60BC3
Drain-Source Voltage	600 V
Drain Current	47 A
Total Conduction Loss	15.68 W
Total Switching Loss	20.57 W
Total Driving Loss	6.14 W
Total Loss	42.39 W

The loss breakdown of each switch when using C3M0065090J SiC MOSFET is shown in Tab. 2-10. All the top and bottom switches have the same average losses, and all the middle switches have the same average losses because of the symmetric operation.

Tab. 2-10 Loss breakdown of switches.

	Top or Bottom Switch	Middle Switch
Conduction Loss	1.01 W	0.41 W
Switching Loss	0.13 W	<0.01 W
Driving Loss	0.02 W	0.02 W
Total Loss	1.16 W	0.43 W

With the selected device and the intended operation condition, a top or bottom switch has a total loss nearly three times compared to a middle switch. A middle switch has much higher conduction loss than switching loss and driving loss, with the latter two combing for less than 5% of the total losses. Therefore, devices with large die sizes can be used as the middle switch to reduce the conduction loss to further decrease the total semiconductor losses. However, the same device is used for all the switches in the converter in this study.

Because of the low total loss of the devices, natural convection cooling is used instead of forced air cooling. Heatsinks [129] are mounted with thermal tapes [130] for all top and bottom devices.

2.3.4 PCB Design

The converter has three identical phase legs, each of which includes two similar cells. The schematic and layout design are focused on one cell first and then extended to the other cells.

Fig. 2-13 shows the top view of one inner cell. The cell is 4.2 inches long and 2.8 inches wide. The four switching devices are placed in the middle of the cell with a two-by-two arrangement. The middle devices, which are the two in the lower half in the layout, are placed next to each other because the source terminals of these two devices needs to be connected together and placed close. Then the top device and bottom device are placed in the upper half in the layout. Each switching device has its own driving circuit next to itself. The selected C3M0065090J SiC MOSFET has additional driving source terminal to achieve superb switching performance. Therefore, driving these four devices prefers four isolated power supplies instead of three if using other types of devices in a three-level T-type cell.

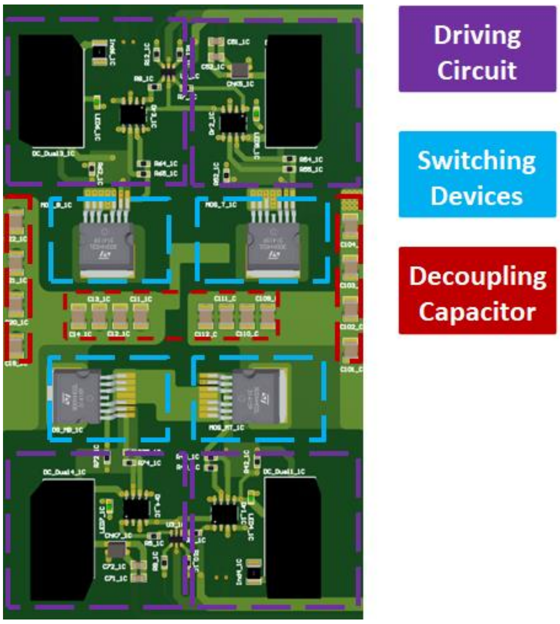
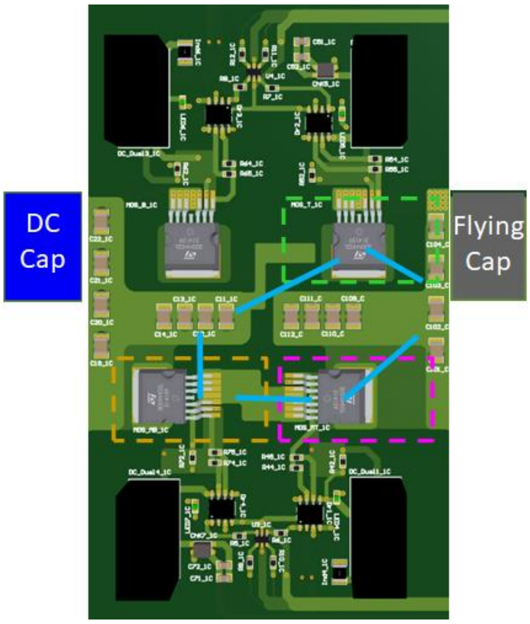


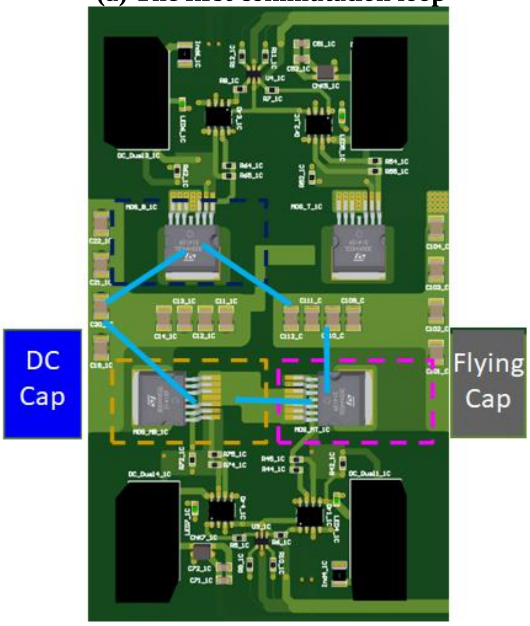
Fig. 2-13 Top view of an inner cell.

The commutation loops need to be minimized to avoid increased voltage overshoot, increased loss, and increased EMI emission. One T-type cell has three conduction paths: through the top device, through the bottom device, or through two middle devices. The commutation between top and bottom paths is avoided through the modulation. Then there are two commutation loops, one consists of the top and middle paths, and another consists of the bottom and middle paths. A loop in the inner cell also includes a dc capacitor and a flying capacitor. A loop in the outer cell includes a flying capacitor.

Fig. 2-14 shows the two commutation loops in an inner cell. The first one consists of the top device, two middle devices, the positive dc capacitor, the positive flying capacitor, the decoupling capacitors in parallel with the positive dc capacitors, and the decoupling capacitors in parallel with the positive flying capacitor. The second one consists of the bottom device, two middle devices, the negative dc capacitor, the negative flying capacitor, the decoupling capacitors in parallel with the negative dc capacitor, and the decoupling capacitors in parallel with the negative flying capacitor. Film capacitors are used as the dc capacitors and flying capacitors. Because of the required capacitances, the physical sizes of the capacitors are big, and they are placed to the left or right of each cell. The traces connecting between switching devices and capacitors are inevitably long, leading to high parasitic inductances. Decoupling capacitors are placed around and close to switching devices to reduce the parasitic inductances. In addition, ceramic capacitors are used as the decoupling capacitors, which have smaller equivalent serial inductance (ESL) values compared to the film capacitors, further reducing the loop inductance.



(a) The first commutation loop



(b) The second commutation loop

Fig. 2-14 Commutation loops in an inner cell.

As the switching devices have high *dv/dt* during switching transients, capacitive coupling needs to be minimized to prevent the signals in auxiliary circuits being polluted by power circuits. With the layout shown in Fig. 2-13, the main power is transferred from left to right through the switching devices in the middle of the cell, while the auxiliary power and signals are transferred from right to left at either the top or bottom of the cell. There is no overlap between power circuits and auxiliary circuits, minimizing capacitive coupling between them.

Every two cells are connected in series with two flying capacitors in between to form a phase leg. Three phase legs are placed in parallel for the whole inverter. DC capacitors are placed to the left of the three phase legs. Connectors for the power circuit and connectors for the auxiliary circuits are placed nears the edges of the board. The top view of the converter is shown in Fig. 2-15. The whole board is 14.6 inches long and 10.1 inches wide.

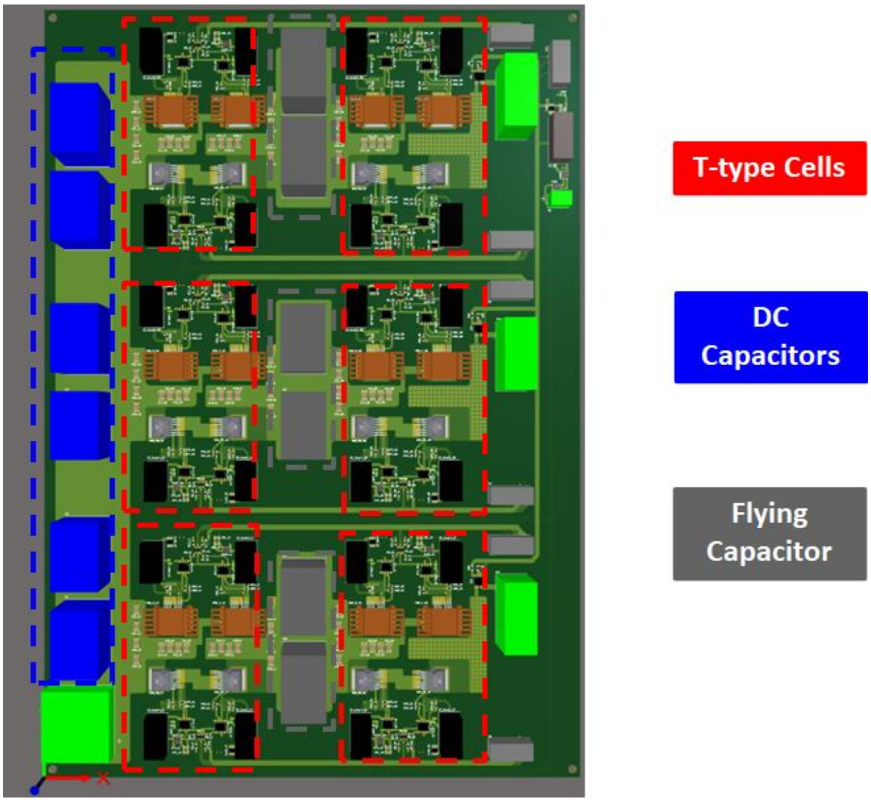


Fig. 2-15 Top view of the three-phase converter.

2.4 Experimental Results

The inverter prototype is connected to a dc voltage source and a three-phase RL load. The output voltage of the dc source is set to be 750 V, which is the input voltage to the inverter prototype. The inductance of the load inductor is 0.5 mH per phase. Because of the availability, the resistance of the load resistor is 30 Ω per phase, which is smaller compared to the originally specified operation condition. The output power in the test is controlled to be 5 kW. Then the output voltages are smaller, and the output currents are larger compared to the originally specified operation condition.

A control board featuring Texas Instruments TMS320C28343 Delfino Microcontroller (MCU) [131] and Lattice LCMX02-4000HC Complex Programmable Logic Device (CPLD) [132] is used for the control calculation.

2.4.1 Converter Outputs

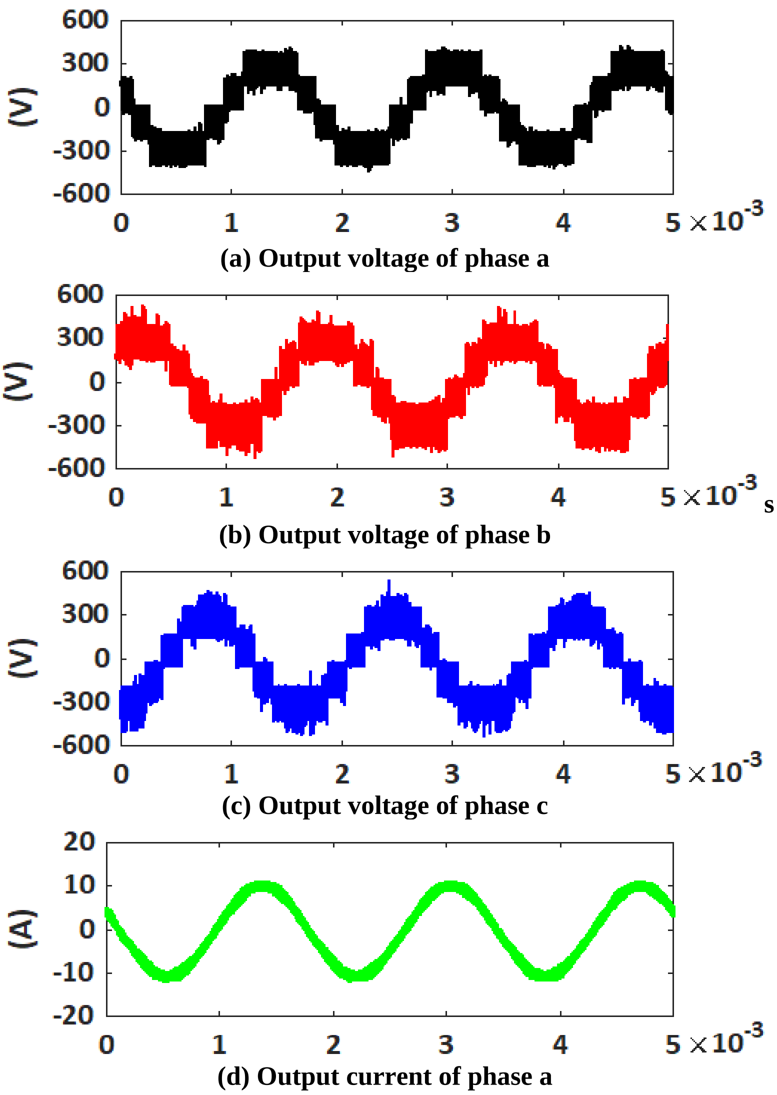
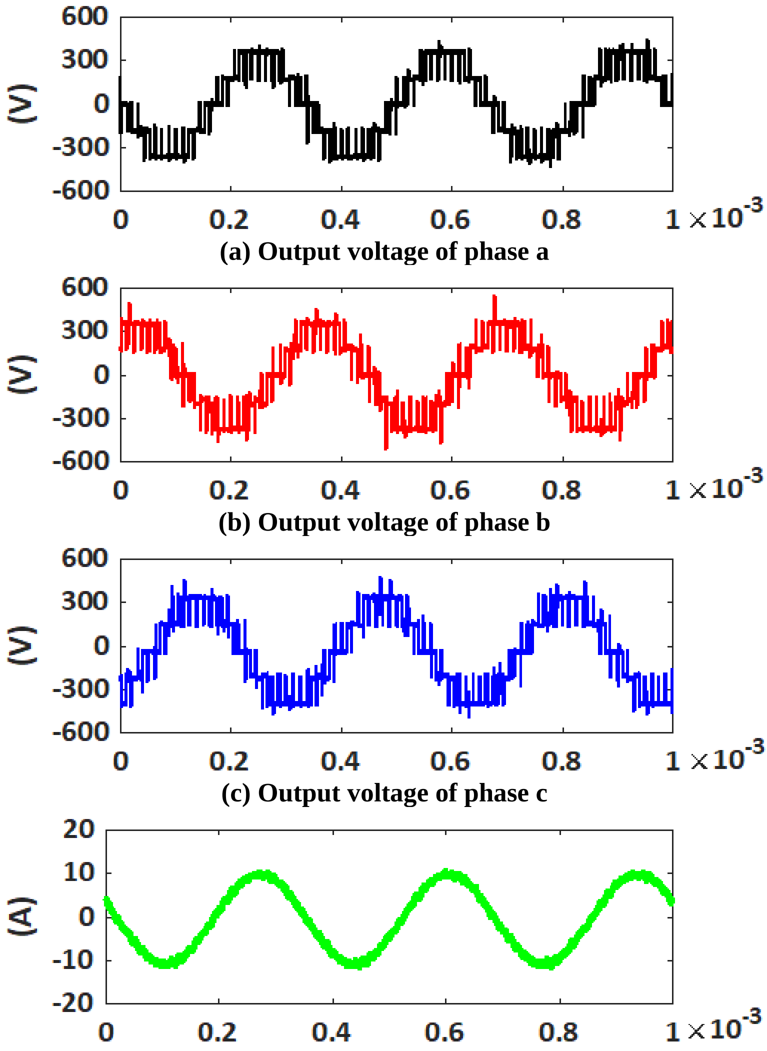


Fig. 2-16 Output voltages and current at 600 Hz line frequency.

Fig. 2-16 shows the measured output voltages of three phases and the output current of phase a at 600 Hz output line frequency for three line cycles. The five voltage levels at each phase can be clearly observed.

Fig. 2-17 shows the measured output voltages of three phases and the output current of phase a at 3000 Hz output line frequency for three line cycles. The five voltage levels at each phase can be clearly observed. With the same switching frequency and a higher line frequency, there are less switching actions in each line cycles.



(a) Output voltage of phase a

(b) Output voltage of phase b

(c) Output voltage of phase c

(d) Output current of phase a

Fig. 2-17 Output voltages and current at 3000 Hz line frequency.

2.4.2 DC Capacitor Voltages

Fig. 2-18(a) shows the measured two dc capacitor voltages at 600 Hz output line frequency for three line cycles. Fig. 2-18(b) shows the sum of the two dc capacitor voltages, which is the dc bus voltage. Fig. 2-18(c) shows the measured output current of phase a.

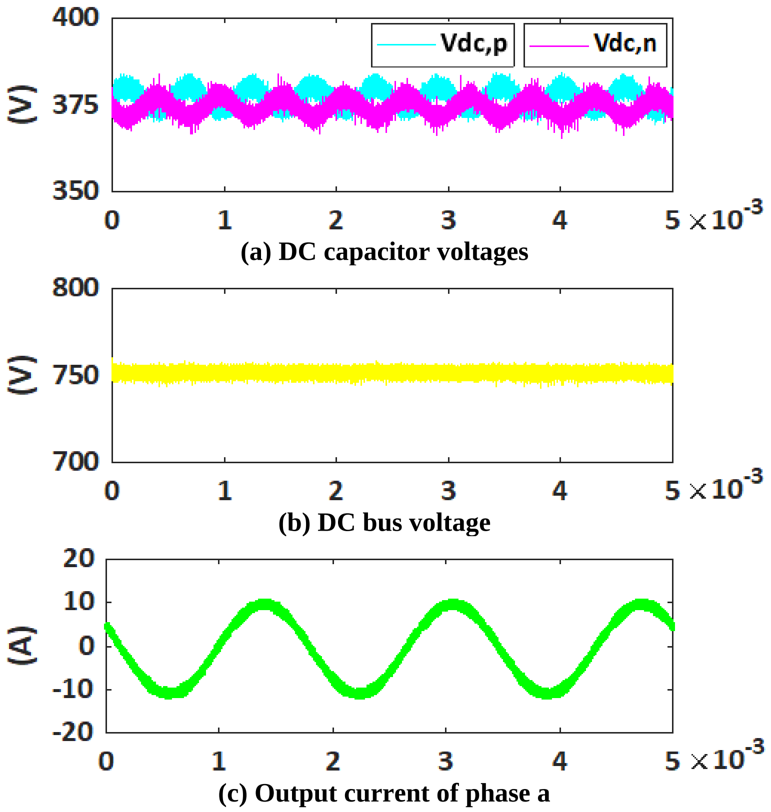


Fig. 2-18 DC capacitor voltages and current at 600 Hz line frequency.

The difference between the average values of the two dc capacitor voltages is 2.5 V, which is 0.7% of the rated value. It is negligible and could be caused by the discrepancy of the two probes. The peak-to-peak voltage ripple on one capacitor is around 5.9 V, which is 1.6% of the rated value. Compared with the output current, it can be clearly seen that the frequency of the dc capacitor voltage ripple is three times of the output line frequency.

Fig. 2-19(a) shows the measured two dc capacitor voltages at 3000 Hz output line frequency for three line cycles. Fig. 2-19(b) shows the sum of the two dc capacitor voltages, which is the dc bus voltage. Fig. 2-19(c) shows the measured output current of phase a.

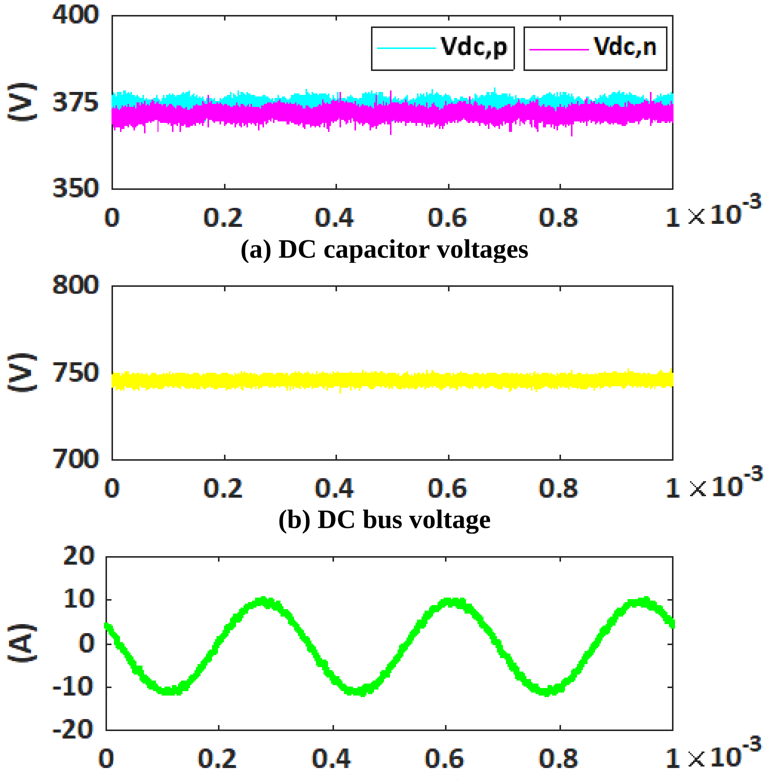


Fig. 2-19 DC capacitor voltages and current at 3000 Hz line frequency.

The difference between the average values of the two dc capacitor voltages is 2.2 V, which is 0.6% of the rated value. It is negligible and could be caused by the discrepancy of the two probes. The peak-to-peak voltage ripple on one capacitor is around 1.4 V, which is 0.4% of the rated value. Compared with the output current, it can be clearly seen that the frequency of the dc capacitor voltage ripple is three times of the output line frequency. With a higher line frequency, the magnitude of the voltage ripple is smaller.

2.4.3 Flying Capacitor Voltages

Fig. 2-20 shows the measured two flying capacitor voltages in phase c at 3000 Hz output line frequency for three line cycles.

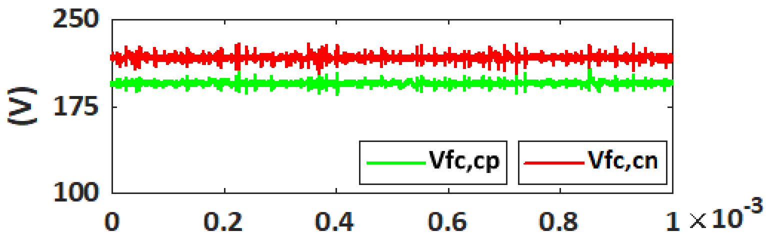


Fig. 2-20 Flying capacitor voltages and output current of phase c.

The average voltage of the positive flying capacitor is 194.9 V, which is 3.9% higher than the rated voltage. The average voltage of the negative flying capacitor is 217.1 V, which is 15.8% higher than the rated voltage. The other four flying capacitors in phase a and b also have different offsets from the rated value. It is important to have the flying capacitor voltages close to the rated value, otherwise it might affect the safe operation of flying capacitors and switching devices. In this case, the voltages of the dc capacitors are correct and the voltages of the two flying capacitors in phase c are higher than the rated value, then the two flying capacitors and all the devices in the outer cell of phase c will need to withstand higher voltages.

Unbalanced flying capacitor voltages also affect the output quality. Fig. 2-21 shows the output voltage of phase a with 3000 Hz output line frequency and 300 V dc bus voltage for three line cycles. The five voltage levels can still be observed. However, only four of them have the rated value. The second voltage level should have a value of half of the dc bus voltage but is either higher or lower than that. The reason is that the positive flying capacitor voltage value is not correct. This will introduce a harmonic in the output voltage at the switching frequency.

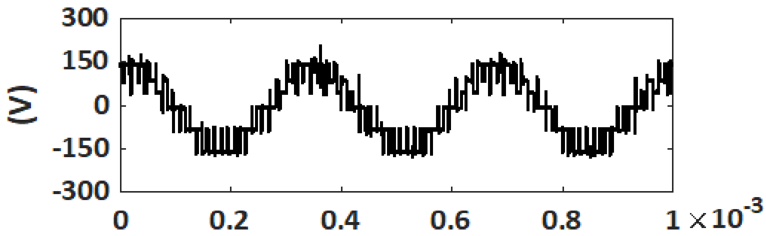


Fig. 2-21 Output voltage of phase a with unbalanced flying capacitor voltages.

Although the flying capacitor voltages are theoretically naturally balanced with the phase-shifted modulation, the natural balancing property highly depends on the accuracy of the gate signals. With accurately phase-shifted gate signals, any unbalance flying capacitor voltages will introduce high frequency switching harmonics in output voltages, and then in output currents, which in turn will adjust the flying capacitor voltages [34], [124]. However, if the devices do not turn on or off at the exact intended moments, the flying capacitor currents will be affected. When the capacitor charges from two nonideality equal to each other, the flying capacitor voltage will settle, but at a value which are away from the rated value [133]. In the built inverter prototype, different control and gate driving channels have different delay values, different switching devices have different switching characteristics, leading to the offsets of the flying capacitor voltages.

In each switching cycle, the second type of additional charge to the flying capacitor only depends on the timing error of the switching actions and the output current. However, the first type of additional charge depends on the flying capacitor voltage offset from the rated value, the load impedance, the duty ratio, and the switching period. Therefore, with the same converter outputs, the same load, and a higher switching frequency, the flying capacitor voltage will have a larger offset to compensate the additional charge caused by the timing error when the steady state is achieved. With a high switching frequency in the prototype, the unbalance of flying capacitor voltages is significant.

According to Equation (2-8), the gate signals of the two cells can be slightly adjusted to compensate the offsets. A 0.1% adjustment on the duty ratio is used to adjust the positive flying capacitor voltage in phase c, a 0.2% adjustment on the duty ratio is used to adjust negative flying capacitor voltage in phase c. Fig. 2-22 shows the measured two flying capacitor voltages in phase c with the compensation at 3000 Hz output line frequency for three line cycles.

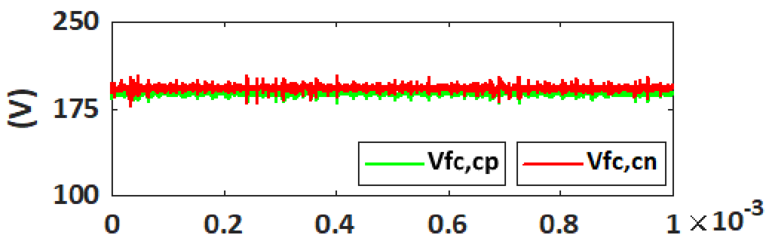


Fig. 2-22 Flying capacitor voltages of phase c with duty ratio compensation.

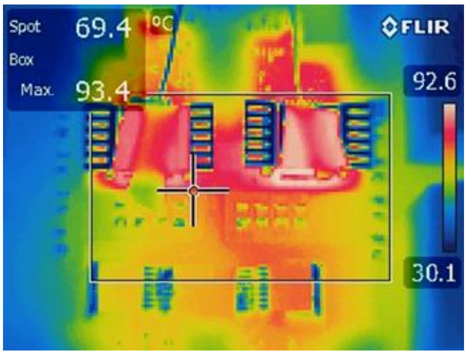
The average voltage of the positive flying capacitor is 188.5 V, the average voltage of the negative flying capacitor is 192.8 V. Both are very close to the rated voltage of 187.5 V. The duty ratios in phase a and b are compensated as well to adjust the other four flying capacitor voltages. It should be noted that the results shown in Fig. 2-16 and Fig. 2-17 are with the duty ratio compensation.

Because of the lack of flying capacitor voltage sensing, only open-loop compensation is implemented in this study. In practical, it is preferred to sensor all the flying capacitor voltages, and implement a closed-loop control, to adjust duty ratios based on the sensed flying capacitor voltages and output currents. However, the voltage sensing may introduce additional EMI emission in the auxiliary circuits, as shown in Section 4.3, and needs to be implemented with great care.

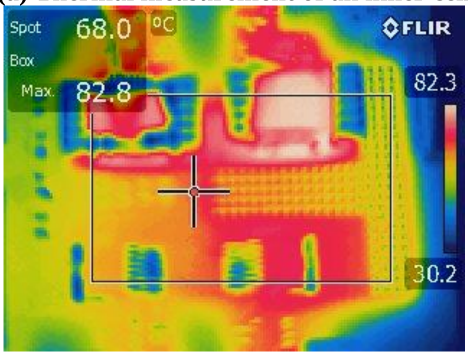
2.4.4 Thermal Measurement

Fig. 2-23 shows the thermal measurements of two cells in the same phase leg. The maximum temperature measured is about 93 °C at drain pads of the top and bottom devices in the inner cell, and about 83 °C at drain pads of the top and bottom devices in the outer cell. The devices in the two cells have the same losses. However, the outer cell has fewer decoupling capacitors and therefore has better heat dissipation and lower temperatures.

The measured efficiency of the whole converter is 98.5%. The losses are higher than the original estimation. One main reason is that the original estimation does not consider the increased conduction loss with a higher junction temperature. Another main reason is that the test condition is slightly different, and the losses are higher with higher current magnitudes. The losses from the capacitors, traces and planes also contribute to the total losses but should be much lower than the semiconductor losses.



(a) Thermal measurement of an inner cell



(b) Thermal measurement of an outer cell

Fig. 2-23 Thermal measurements.

2.5 Summary

A three-phase five-level Stacked Multicell Converter using SiC MOSFETs is designed, built, and experimentally verified.

The five-level SMC topology is explored for the high-speed motor drives application. It has higher output voltage quality and lower voltage reflection over-voltage than two-level and three-level topologies. The significant reduction of the over-voltage when employing the five-level topology is especially important when using SiC MOSFETs as the switching devices, as both the high switching speeds and high switching frequency increase the magnitude of the over-voltage. The five-level SMC has shorter commutation loops, lower losses compared to other five-level topology candidates.

The switching frequency, dc capacitors, flying capacitors, and switching devices are selected to meet the specifications and requirements. The PCB layout design is finished with a modular design approach. In the layout design, attention was paid to minimize driving loops, minimize commutation loops, and minimize coupling between power circuits and auxiliary circuits.

The prototype is validated through experiments to have five output voltage levels at each phase, rated dc capacitor voltages and rated flying capacitor voltages. The measured efficiency of the prototype is 98.5%.

With this design, there is no need for additional filters. The converter output quality is good enough thanks to the high output quality feature of the five-level topology and the high switching frequency capability of SiC MOSFETs. The over-voltage is low enough thanks to the small voltage steps of the five-level topology. Therefore, the design not only achieves a high efficiency of the inverter, but also eliminates the losses and sizes of the filters.

Although different five-level topologies have the same output voltages, some of them have long commutation loops while the others only have short commutation loops. This may not be an issue with the low switching speeds of Si devices but could be critical with the high switching speeds of SiC MOSFETs. It is a challenge and has to be taken into consideration when using the state-of-art SiC MOSFETs to realize some traditional multilevel topologies.

It is found that the implemented phase-shifted PWM is not sufficient to ensure the self-balancing of the flying capacitor. This may also not be severe with the low switching frequency operation of Si devices but could be significant with the high frequency operation of SiC MOSFETs. Higher accuracy is required when controlling SiC MOSFETs in multilevel converters.

Chapter 3. Operation and Control of Converters with Integrated Capacitor Blocked Transistor Cells

In this chapter, the operation and control of converters with Integrated Capacitor Blocked Transistor (ICBT) Cells are studied and experimentally verified.

3.1 Introduction

As introduced in Chapter 1, there is need of increasing the voltage ratings of power converters. Medium voltage and high voltage systems have seen increasing development while having medium voltage and high voltage power electronics converters as the key components for power conversion [1]-[15], [134]-[138]. Meanwhile, power semiconductor devices have been also progressing promisingly into the medium voltage range [48]-[50], [139]-[144]. However, the maximum desired voltage rating of a converter can still be higher than the maximum available voltage rating of a single device. Sometimes power conversion cannot be achieved by simply using a pair of complementary switches as a phase leg.

One method to achieve higher converter voltage rating is connecting multiple devices in series to create an equivalently high-voltage device. The control principle is very simple, the series-connected devices are controlled to switch synchronously. The main challenge of this method is to deal with the voltage unbalance among the devices during the short turn-off transient and the off state so that each device operates in the safe range. The passive balancing circuits, for example RC circuits or RCD circuits, are usually placed in parallel with the switching devices [145]-[147]. However, they suffer from increased loss, increased volume, and increased switching time. The active balancing circuits control the timing or the speed of the turn-off transitions [148]-[150] but need to be fast and accurate to function among the short turn-off transition. In addition, the active balancing circuits generally do not work when the device current is negative, and may not work when the turn-off transition is initiated by an over-current protection instead of by the control circuit.

Another method is employing multilevel topologies to reduce the voltage rating requirement of switches while multilevel topologies also provide other benefits, as introduced in Section 1.2. Capacitors are commonly used as internal energy storage and they make it possible for switching devices to block only a fraction of the whole converter bus voltage. As the capacitors take part in the power conversion, high capacitances are usually required in high power, 60 Hz systems to keep the voltage ripples small. As can be observed in multilevel converter prototypes of different topologies [151]-[153], capacitors take considerable volume and result in low power density of the converters. The magnitude of the voltage ripple is usually reversely proportional to the line frequency, so some topologies are limited in low line frequency applications and dc-dc applications.

Integrated Capacitor Blocked Transistor (ICBT) cells [154] provide an alternative solution to transfer high power in medium voltage or high voltage systems. One ICBT cell operates as a single switching device, series-connected ICBT cells operate as series-connected devices but generate little additional losses and do not require fast balancing control. Converters with ICBT cells have the modularity and scalability as MMCs, but do not require high cell capacitances.

Operation modes similar with ICBT cell operation can be found in [155]-[158], but the operation with only an arm instead of the whole phase leg, and the operation with a big series-connected resistor in the arm, do not represent the real conditions.

This study provides detailed analyses of converters having ICBT cells and accordingly proposes a control method for converters having ICBT cells. Section 3.2 explains the operation principle and analyzes the impacts of non-idealities. Section 3.3 analyzes the capacitor voltage balance in each converter arm. Section 3.4 proposes a control method for the ICBT-based converters. Section 3.5 presents the experimental results.

3.2 Operation Principle

Firstly, the operation principle of ICBT-based converter is analyzed.

3.2.1 Ideal Operation

Fig. 3-1 shows the configuration of an ICBT cell. It consists of a pair of complementary switches and a cell capacitor, similar as a Half-Bridge cell in MMCs. But its operation is different. The bottom switch is defined as the main switch and the top switch is defined as the auxiliary switch.

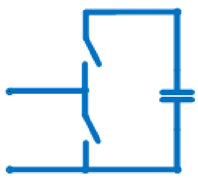
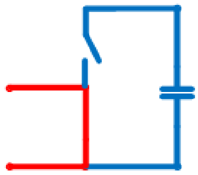
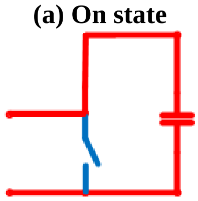


Fig. 3-1 Configuration of an ICBT cell.

Two switching states of an ICBT cell are shown in Fig. 3-2. When the main switch is on and the auxiliary switch is off, the voltage across the cell output terminals is zero; when the auxiliary switch is on and the main switch is off, the current through the cell output terminals reduces to zero quickly, which will be shown later. As the voltage across the cell is zero in one state and the current through the cell is zero in the other state, the two switching states of an ICBT cell are similar as the switching states of a single device. The first state is defined as the "on" state, and the second state is defined as the "off" state.



(a) On state



(b) Off state

Fig. 3-2 Switching states of an ICBT cell.

Fig. 3-3 shows the configuration of an ICBT-based phase leg. Each arm has four series-connected ICBT cells. There are no desired arm inductors. The converter has the modularity and scalability features like MMCs. The cells in the same arm are controlled to operate synchronously and the cells in the opposite arms are controlled to operate complementarily. The control principle is simple and is similar as series-connected switching devices.

To explain the fundamental operation principle, in Section 3.2 it is assumed that all cells switch instantly, the cells in the same arm switch synchronously, and the cell capacitors in the same arm share the same voltage value.

When the upper arm cells are all on and the lower arm cells are all off, an RLC circuit is formed in the phase leg, Equation (3-1), (3-2) and (3-3) can be derived.

$$V_{dc} = 4V_{c,l} + \left(r + l\frac{d}{dt}\right)(i_u + i_l) \tag{3-1}$$

$$I_o = i_u - i_l \tag{3-2}$$

$$C\frac{dV_{c,l}}{dt} = i_l \tag{3-3}$$

Where V_{dc} is the voltage of the converter dc bus, $V_{c,l}$ is the voltage of each lower arm cell capacitor, r and l are the parasitic resistance and inductance of each arm respectively, i_u and i_l are the upper arm and lower arm currents respectively, I_o is the phase output current, C is the cell capacitance.

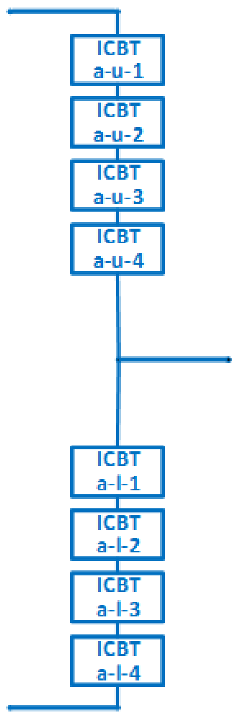


Fig. 3-3 Configuration of an ICBT-based phase leg.

Equation (3-1) describes the voltage relationship between the converter dc bus and an ICBT-based phase leg. The converter dc bus voltage equals to the total cell capacitor voltages in the lower arm, plus the voltage drops on the parasitic passive components in the phase leg. Equation (3-2) describes the current relationship between the two arms and the converter phase leg out. The phase leg output current equals to the difference between two arm currents. The direction of each arm current is defined as from the top to the bottom. Equation (3-3) describes the voltage and current relationship in the lower arm. Each cell capacitor current in the lower arm equals to the lower arm current, and changes the cell capacitor voltage accordingly. The solutions of the equations are shown in Equation (3-4) and (3-5).

$$i_l(t) = Ae^{-\alpha t}\sin(\omega_d t + \varphi) \tag{3-4}$$

$$V_{c,l}(t) = \frac{V_{dc} - r \times I_o}{4} - rAe^{-\alpha t}\sin(\omega_d t + \varphi) + 2l\omega_d Ae^{-\alpha t}\cos(\omega_d t + \varphi) \tag{3-5}$$

The dynamic can be described by Equation (3-6) and (3-7) and is mainly decided by the values of parasitic resistance, parasitic inductance, and cell capacitance.

$$\alpha = \frac{r}{2l} \tag{3-6}$$

$$\omega_d = \sqrt{\frac{1}{2lC} - \frac{r^2}{4l^2}} \tag{3-7}$$

The solutions also depend on the initial conditions, which are described by Equation (3-8) and (3-9).

$$\varphi = \tan^{-1}\left(\frac{\Delta i_l(0)}{\Delta V_{c,l}(0) + r \times \Delta i_l(0)} \times 2l\omega_d\right) \tag{3-8}$$

$$A = \frac{\Delta i_l(0)}{sin(\varphi)} \tag{3-9}$$

Where $\Delta i_l(0)$ and $\Delta V_{c,l}(0)$ represent the initial conditions and are defined as the errors between the initial values and the steady states values, in the lower arm current and the lower arm cell capacitor voltage respectively.

$$\Delta i_l(0) = i_l(0) - i_l(\infty) \tag{3-10}$$

$$\Delta V_{c,l}(0) = V_{c,l}(0) - V_{c,l}(\infty) \tag{3-11}$$

Because of the absence of the designed arm inductors, arm currents change fast and are expected to settle around the stead state values within the duration of one switching state. The steady state values of this switching state are shown in Equation (3-12) and (3-13).

$$i_{l,1}(\infty) = 0 \tag{3-12}$$

$$V_{c,l,1}(\infty) = \frac{V_{dc} - r \times I_o}{4} \tag{3-13}$$

The lower arm current reduces to zero, and so do the cell capacitor currents of the cells in the "off" state. The capacitor voltage values of those cells mainly depend on the dc bus voltage and the number of cells, with a small offset related to the parasitic arm resistance and the phase output current.

The steady state value of the upper arm current during this switching state can also be solved and is shown in Equation (3-14).

$$i_{u,1}(\infty) = I_o \tag{3-14}$$

The upper arm current equals to the phase leg output current.

Similarly, during the other switching state when the upper arm cells are all off and the lower arm cells are all on, the dynamic is similar, and the steady state values can be solved and are shown in Equation (3-15), (3-16) and (3-17).

$$i_{u,2}(\infty) = 0 \tag{3-15}$$

$$V_{c,u,2}(\infty) = \frac{V_{dc} + r \times I_o}{4} \tag{3-16}$$

$$i_{l,2}(\infty) = -I_o \tag{3-17}$$

As can be observed from Equation (3-12), (3-14), (3-15) and (3-17), the arm that has the cells in the on state conducts the phase leg output current, the other arm has the cells in the off state and only blocks the converter dc bus voltage. The two arm currents are similar with the two device currents in a traditional two-level converter.

The cell capacitor is bypassed during the on state of the cell and its voltage will not change. It is connected into the converter arm during the off state of the cell, but its current reduces to zero quickly. As can be observed from Equation (3-13) and (3-16), each cell capacitor voltage is around a quarter of the converter dc bus voltage, so that a higher converter voltage rating can be achieved with lower-rated devices when using ICBT-based converter phase legs. Although the voltage ripple changes with the output current, the voltage ripple magnitude does not change with the line frequency. Converters having ICBT cells can operate in low line frequency condition or even dc-dc mode.

The power is directly transferred through the ICBT cells during their on state, unlike in MMCs where the power is transferred indirectly through the cell capacitors. Therefore, high cell capacitances are not required in ICBT cells, the size of the capacitors can be much smaller.

Similar as in MMCs, each switching device in ICBT-based converters always blocks the corresponding cell capacitor voltage when not conducting. When connecting multiple ICBT cells in series, there is no balancing issue among devices if the capacitor voltages are regulated.

In addition, there are no arm inductors in ICBT-based converters, which may contribute significantly to the size and weight to traditional MMCs [159]. The size, weight and loss of the arm inductors are eliminated in ICBT-based converters, increasing the power density and efficiency.

3.2.2 Loss Analysis

During the on state of an ICBT cell, the main device conducts the current and has conduction loss. During the off state, the current flows through the auxiliary device but it reduces to zero quickly, so the conduction loss is negligible. The total conduction loss of an ICBT cell should be similar as a single device and it is mostly dissipated at the main device.

Consider a switching transition when the cells in the upper arm turn off, the cells in the lower arm turn on, and the phase leg output current is positive. There are turn-off losses at the main devices but little losses at the auxiliary devices in the upper arm cells. There are little switching losses at all devices in the lower arm cells as the switching currents are zero. For the other switching transition when the cells in the upper arm turn on, and the cells in the lower arm turn off, there are turn-on losses at the auxiliary devices in the lower arm cells but little switching losses at the other switches.

When the phase leg output current is negative, there are turn-on losses at the auxiliary devices in the upper arm cells in the first transition, and turn-off losses at the main devices in the lower arm cells in the second transition.

Therefore, for the ICBT-based phase leg shown in Fig. 3-3, despite having two devices per cell and eight cells per phase leg, only four devices have switching losses in each switching transition. The location of the four devices that have switching losses change with the polarity of the phase leg output current and the type of the switching transition. The total switching loss of an ICBT-based phase leg is similar as a phase leg consisting of series-connected switches of the same kind.

3.2.3 Simulation Results

An ICBT-based Buck converter is built in PLECS. The specifications are shown in Tab. 3-1. A small resistor of 0.1 Ω and a small inductor of 1 nH is placed in each arm to represent the parasitic passive components. The inductance is set to be very low to illustrate the ideal operation. The simulation results are shown for five switching cycles in Fig. 3-4.

Tab. 3-1 Specifications of an ICBT-based Buck converter.

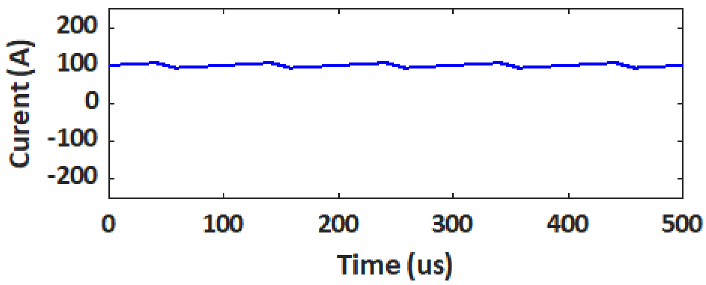
Parameter	Value
Active Power	2 MW
DC Bus Voltage	24 kV
Output Voltage	20 kV
Switching Frequency	10 kHz
Cell Capacitance	32.5 μF

As can be observed in Fig. 3-4(a)-(c), the two converter arms conduct the phase leg output current alternatively. The upper arm current approximately changes between the output current and zero, the lower arm current approximately changes between the reversed output current and zero. The currents behave similarly as in a traditional two-level inverter with two single switching devices per phase leg. The series-connected ICBT-cells operate as an equivalently high-voltage switching device.

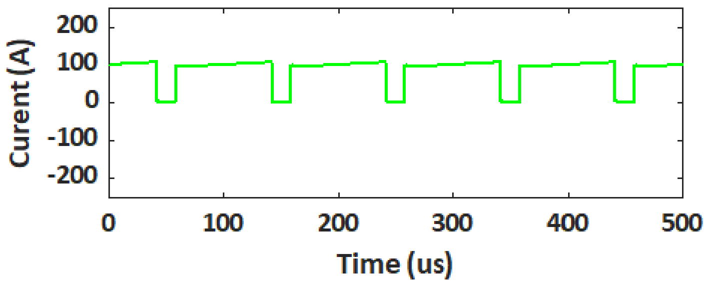
The capacitor voltage shown in Fig. 3-4(d)-(e) match with the values in Equation (3-13) and (3-16). Each cell capacitor voltage is close to one quarter of the converter dc bus voltage. There is little voltage ripple at each cell capacitor.

Then an ICBT-based H-bridge inverter is built in PLECS. The specifications are shown in Tab. 3-2. The simulation results are shown for three line cycles in Fig. 3-5.

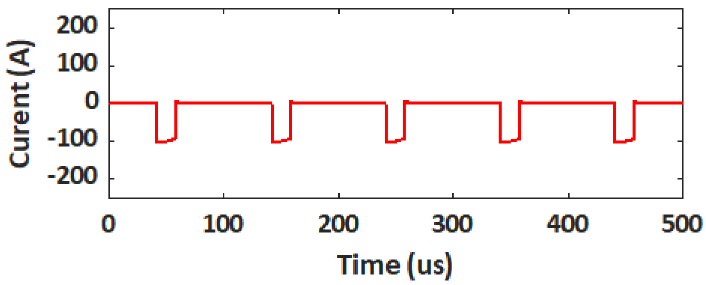
Similarly, the two converter arms conduct the phase leg output current alternatively. The magnitudes of the arm currents approximately follow the magnitude of the phase leg output current.



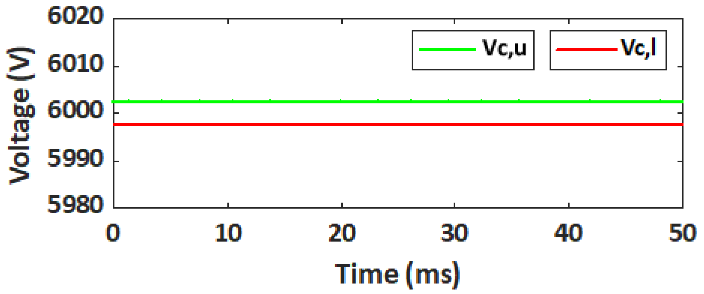
(a) Output current



(b) Upper arm current



(c) lower arm current



(d) Cell capacitor voltages

Fig. 3-4 Simulation results of an ICBT-based Buck converter.

The capacitor voltage shown in Fig. 3-5(d)-(e) match with the values in Equation (3-13) and (3-16). The peak-to-peak ripple is less than 0.2% of the rated value.

The semiconductor losses of the ICBT-based converters can also be simulated with the simulation models. Preliminary loss characteristics of 10 kV, 240 A XHV6 SiC MOSFET modules from Cree/Wolfspeed [160] are used. Tab. 3-3 shows the loss breakdown results for the ICBT-based converters in dc and ac operation modes.

Tab. 3-2 Specifications of an ICBT-based inverter.

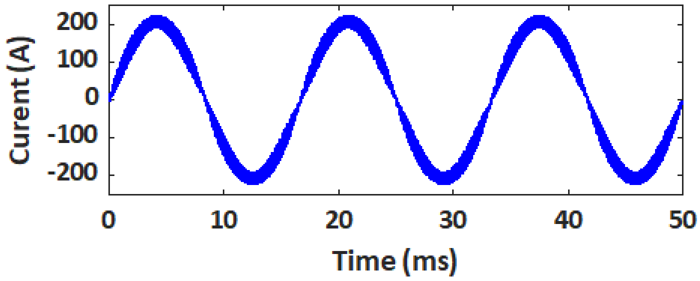
Parameter	Value
Active Power	2 MW
DC Bus Voltage	24 kV
Modulation Index	0.80
Line Frequency	60 Hz
Switching Frequency	10 kHz
Cell Capacitance	32.5 μF

For comparison, another two converters are built by using series-connected switching devices, with the same specifications and loss characteristics, and with the assumption of ideal voltage balance. The results are shown in Tab. 3-4.

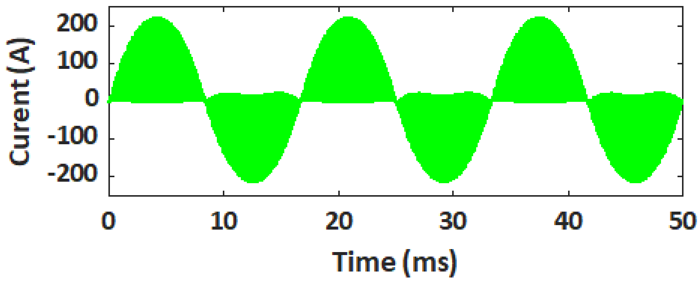
Comparing the results in Tab. 3-3 and Tab. 3-4. ICBT-based converters have very similar total losses compared with converters with series-connected switching devices, with the differences being less than 2%, despite having doubled switching device count. It should be noted that the series-connected switches may have addition losses from the balancing circuits.

Specifically, the conduction loss distributions between the upper arm and the lower arm, or between the top device series and the bottom device series, are the same. Given the operation principle of ICBT-based cells, the conduction losses are mainly dissipated at the main devices.

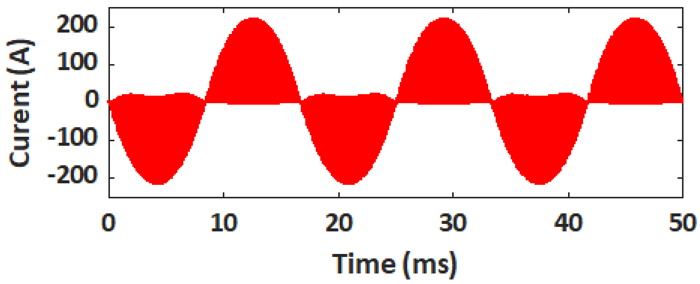
However, the switching loss distributions are very different between two types of converters. For series-connected switches, they have turn-on losses and turn-off losses when having positive device currents but little switching losses when having negative device currents. For ICBT cells, they only have device turn-off losses at the main switches during the cell turn-off transition with positive cell currents, and only have device turn-on losses at the auxiliary switches during the cell turn-off transition with negative cell currents. As the upper arm and lower arm conduct currents of different polarities, the total switching loss remain similar.



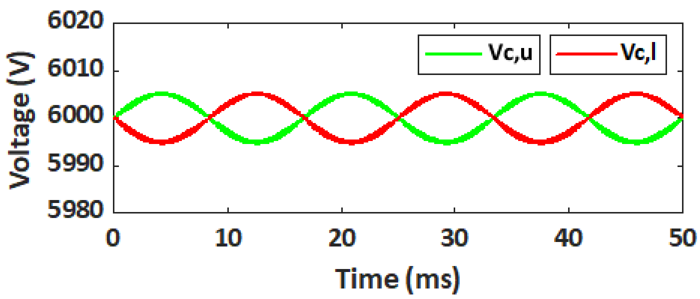
(a) Output current



(b) Upper arm current



(c) lower arm current



(d) Cell capacitor voltages

Fig. 3-5 Simulation results of an ICBT-based inverter.

Tab. 3-3 Semiconductor loss breakdown in ICBT-based converters.

(a) Buck converter

	Upper Arm	Lower Arm
Total Conduction Loss	0.65 kW	0.13 kW
Total Switching Loss	1.40 kW	5.18 kW

(b) H-bridge inverter

	Upper Arms	Lower Arms
Total Conduction Loss	1.69 kW	1.69 kW
Total Switching Loss	7.50 kW	7.50 kW

Tab. 3-4 Semiconductor loss breakdown in converter phase legs with series-connected switching devices.

(a) Buck converter

	Top Device Series	Bottom Device Series
Total Conduction Loss	0.65 kW	0.13 kW
Total Switching Loss	6.55 kW	0

(b) H-bridge inverter

	Top Device Series	Bottom Device Series
Total Conduction Loss	1.70 kW	1.70 kW
Total Switching Loss	7.30 kW	7.30 kW

3.2.4 Impact of Parasitic Impedances

As mentioned in Section 3.2.1, there are no arm inductors in ICBT-based converters. The parasitic arm inductance is mainly the result of the connections within in the cells and between the cells. Similarly, the parasitic arm resistance is mainly the result of the connections, but also include the on-state resistance of the switching devices.

Considering Equation (3-4) and (3-5), the coefficient of α needs to be large enough, to guarantee that the arm current and the cell capacitor voltage can reach the steady state values within every switching state. Otherwise, the cell capacitors might be charged or discharged in consecutive switching cycles, until a new steady state is achieved where the cell capacitors have large offsets compared to the ideal steady state values, and the arm currents have large magnitudes compared to the magnitude of the phase leg output current.

A criterion for the coefficient of α could be:

$$\alpha \times (t_1, t_2)_{min} \geq 3 \tag{3-18}$$

Where t_1 and t_2 are the duration of the two switching states respectively, which depends on the switching frequency and the duty ratio. The shorter switching state is the more critical one. If the exponential terms in Equation (3-4) and (3-5) can decrease by e^3, it can be considered that the steady state is approximately reached.

For the ICBT-based Buck converter simulated in Section 3.2.3, the duration of the shorter switching state is:

$$(t_1, t_2)_{min} = \left(1 - \frac{V_{out}}{V_{dc}}\right) \div f_{sw} = 16.67\ \mu s \tag{3-19}$$

Where V_{out} is the output voltage, V_{dc} is the converter dc bus voltage, f_{sw} is the switching frequency. Therefore, the coefficient of α needs to be larger than:

$$\alpha \geq 1.8 \times 10^5\ s^{-1} \tag{3-20}$$

The on-state resistance of each switching device is 19.4 mΩ. There are four switching devices connected into the arm at each time, the total resistance of which is 77.8 mΩ. Assuming the parasitic resistance from the connections is twice of the resistance of the devices, then the total parasitic resistance of each arm is:

$$r = 0.23\ \Omega \tag{3-21}$$

Then the total parasitic inductance of each arm needs to be lower than:

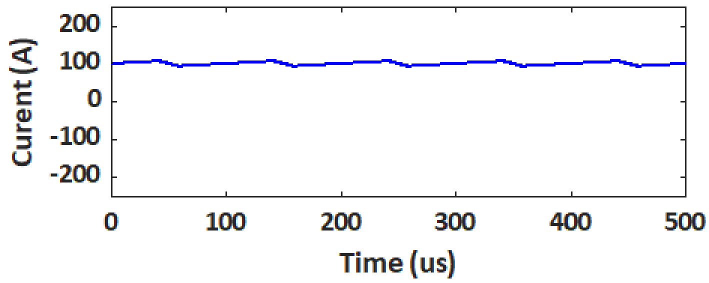
$$l \leq 0.65\ \mu H \tag{3-22}$$

The ICBT-based Buck converter is simulated again with the updated parasitic arm resistance of 0.23 Ω, and different parasitic arm inductance values. The simulation results are summarized in Tab. 3-5. The simulated waveforms when the inductance value is 1.30 μH, twice the critical value, is shown in Fig. 3-6.

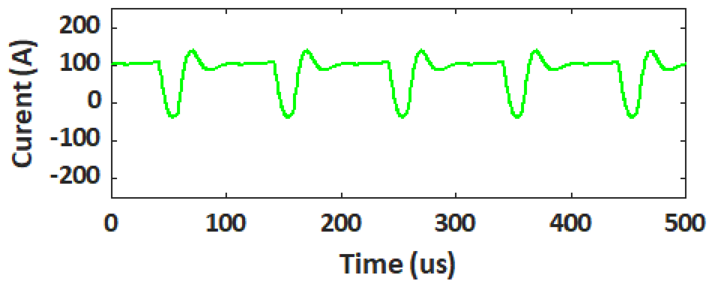
Tab. 3-5 Simulation results comparison with different parasitic arm inductances.

		l	***l***	***l***
Arm Current Maximum Magnitude	Upper	121 A	138 A	173 A
	Lower	126 A	135 A	159 A
Cell Capacitor Voltage	Upper	6005 V	6005 V	6014 V
	Lower	5994 V	5994 V	5996 V
Total Conduction Loss	Upper	0.67 kW	0.70 kW	0.82 kW
	Lower	0.15 kW	0.18 kW	0.30 kW
Total Switching Loss	Upper	1.42 kW	1.87 kW	2.48 kW
	Lower	5.20 kW	5.84 kW	7.22 kW
Total Semiconductor Loss		7.44 kW	8.59 kW	10.82 kW

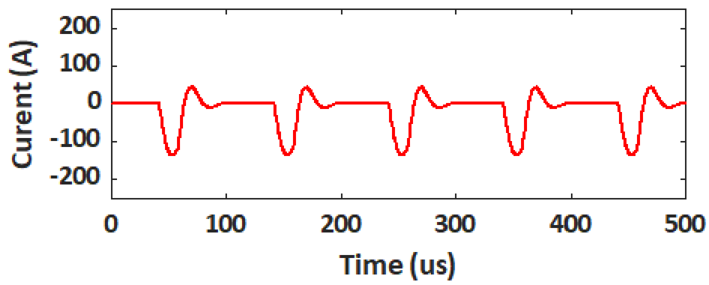
Comparing the results in Fig. 3-4 and Fig. 3-6, the converter output current does not change. However, because of the low value of coefficient of α, which comes from the high parasitic arm inductance value, there is significant resonance between the arm currents and cell capacitor voltages. The currents and voltages can settle to the steady state values during the longer switching sate when the lower arm cells are off, but cannot reach the steady state in the shorter switching state. Tab. 3-5 lists the maximum magnitude of each arm current. With a higher parasitic inductance value, the maximum magnitude of each arm current increases. When the parasitic inductance value is 3.25 μH, five times the critical value, the maximum current magnitude in the arms could be as high as 173 A, which is more than 50% higher compared to the phase leg output current magnitude.



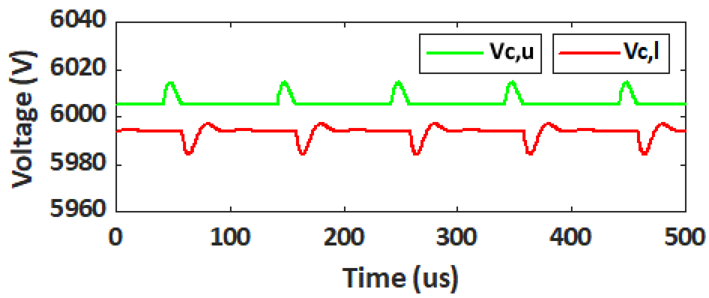
(a) Output current



(b) Upper arm current



(c) lower arm current



(d) Cell capacitor voltages

Fig. 3-6 Simulation results of an ICBT-based Buck converter with high parasitic inductances.

With excessive arm currents, the semiconductor losses increase accordingly. When the parasitic inductance value equals to the critical value, the total loss is 7.44 kW. It is only 1% higher compared to the total loss with the ideal operation, which is 7.36 kW in Tab. 3-3 (a). When the inductance value increases to twice the critical value, the total loss is 17% higher. When the inductance value increases to five times the critical value, the total loss is 47% higher.

Tab. 3-5 also lists the cell capacitor voltages during the on state of the cells. The values only increase slightly, by less than 0.2% even with inductance values being five times the critical value. However, with an even lower α value or a short switching state, the voltages may have significantly higher values. Together with the switching ripples, the safe operation of the switching devices and capacitors may be affected.

The aforementioned higher cell capacitor voltage values can be avoided if the arm current of the arm having the cells in the "off" state settles to zero at the end of each switching state. This is similar as ensuing the reset of the transformer in Forward converters [161].

One way to help the currents and voltages to reach the stead state is by having a high enough value of the coefficient of α. It is desired to have a low parasitic inductance value in the arm. Similar as in Forward converters [161], additional components can also be helpful. For example, small resistors can be placed in series with the cell capacitors to increase the value of the coefficient of α, without increasing the losses much.

Based on Equation (3-3)-(3-11), another solution to is by changing the initial conditions of the switching states. It can be achieved by altering the switching transients and will be shown in Section 3.2.5.

3.2.5 Impact of Dead-times

The analyses in Section 3.2.1 and the simulation results in Section 3.2.3 demonstrate the operation principle of ICBT cells. One ICBT cell operates as a single switching device, series-connected ICBT cells operate as an equivalently high-voltage switching device. However, an

ICBT cell cannot cut off the current by itself as a single device does. Instead, the current is reduced to zero by the collaboration of all the cells in a phase leg.

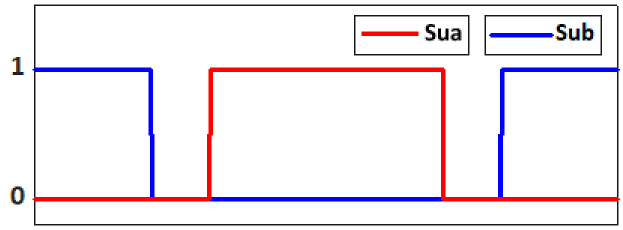
In the traditional two-level converter, a dead-time is applied to the pair of complementary switches to avoid the shoot-through. Similarly, in each ICBT cell, a dead-time is required for the complementary switches to avoid the shoot-through in the cell. This dead-time is named as the power cell dead-time, $t_{td,1}$, defined as the time duration after turning off one switch and before turning on the other switch. The value of the power cell dead-time is set to be the same for all the cells and is decided according to the switching device characteristics.

Meanwhile, another type of dead-time is required between the cells in the upper arm and the cells in the lower arm to avoid all cells in both arms being on together. This dead-time is named as the phase leg dead-time, $t_{td,2}$, defined as the time duration after turning off the main switches in one arm and before turning on the main switches in the other arm.

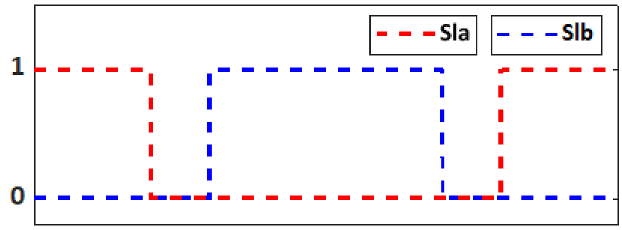
In addition, all cells in both arms cannot be off together, otherwise all the cell capacitors in a phase leg will be connected in series and to the converter bus and lead to the shoot-through in the phase leg. The duration after turning off the auxiliary switches in one arm and before turning on the auxiliary switches in the other arm, $t_{td,2,off}$, has the relationship with the other dead-times as described in Equation (3-23). All three dead-times need to be long enough to ensure safe operation.

$$t_{dt,2,off} = 2 \times t_{td,1} - t_{td,2} \tag{3-23}$$

Fig. 3-7, Fig. 3-8, and Fig. 3-9 show the gate signals in a phase leg for one switching cycle, when the dead-times have different values. In the figures, S_{ua} is the gate signal for the main switches in the upper arm, S_{ub} is the gate signal for the auxiliary switches in the upper arm, S_{la} is the gate signal for the main switches in the lower arm, and S_{lb} is the gate signal for the auxiliary switches in the lower arm. The power cell dead-time $t_{td,1}$ is the time duration when S_{ua} and S_{ub} are both low, and the time duration when S_{la} and S_{lb} are both low. The phase leg dead-time $t_{td,2}$ is the time duration when S_{ua} and S_{la} are both low. $t_{td,2,off}$ is the time duration when S_{ub} and S_{lb} are both low. All three types of dead-times need to be long enough.



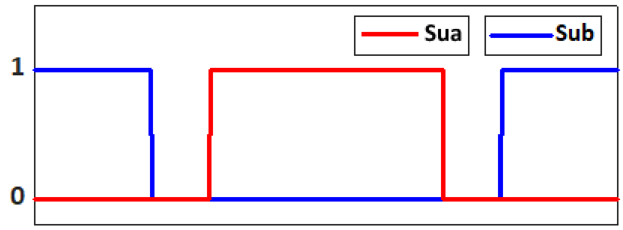
(a) Gate signals in the upper arm



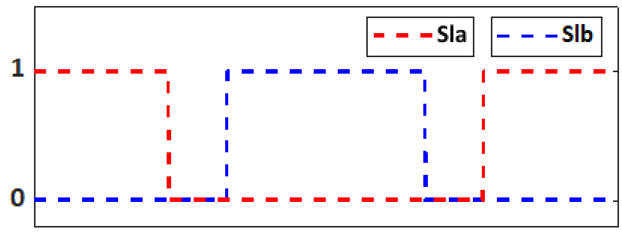
(b) Gate signals in the lower arm

Fig. 3-7 Gate signals in a phase leg when $t_{td,1} = t_{td,2}$.

Different dead-time values may affect the switching transitions. Firstly, consider the case when the phase leg output current is positive, and consider the first transition in the figures, when the upper arm cells are turned on and the lower arm cells are turned off. Fig. 3-7 represents the case that the phase leg dead-time is the same as the power cell dead-time. At the beginning of the transition, the current flows though the main switches in the lower arm. It starts to commute to the auxiliary switches in the lower arm and the main switches in the upper arm when turning on S_{ua} and S_{lb}. After that, the switching transient is finished, the new switching state starts, and the RLC circuit is formed. The upper arm current will change from zero to the phase leg output current, the lower arm current will change from the reversed phase leg output current to zero.



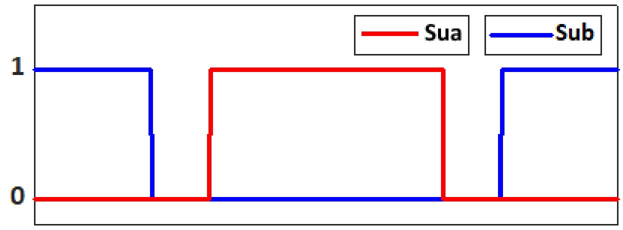
(a) Gate signals in the upper arm



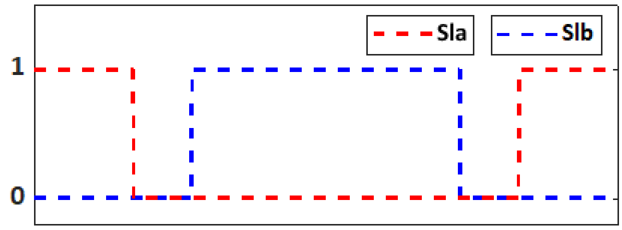
(b) Gate signals in the lower arm

Fig. 3-8 Gate signals in a phase leg when $t_{td,1} > t_{td,2}$.

Fig. 3-8 represents the case that the phase leg dead-time is shorter than the power cell dead-time. The current starts from flowing through the main switches in the lower arm. After turning on S_{ua}, the main switches in the upper arm cells start to conduct current, the cell output voltages of the upper arm cells change from the cell capacitor voltage to zero. However, the lower arm current still flows through the diodes of the main devices in the lower arm cells and the cell output voltages of the lower arm cells are still zero. The converter dc bus voltage is applied to the parasitic arm inductors in the phase leg and increase the arm currents in both arms, until the cell output voltages of the lower arm cell change from zero to the cell capacitor voltages. This happens when S_{lb} is turned on, or the lower arm current changes polarity from negative to positive and commutes to the diodes of the auxiliary switches in the lower arm. After that, the switching transient is finished, the new switching state starts, and the RLC circuit is formed. However, the initial conditions of the switching state are different because the arm currents already increase during the transient. When the new switching state starts, the initial errors in the arm currents are smaller, and the magnitudes of the arm current resonances during the switching state will be smaller.



(a) Gate signals in the upper arm



(b) Gate signals in the lower arm

Fig. 3-9 Gate signals in a phase leg when $t_{td,1} < t_{td,2}$.

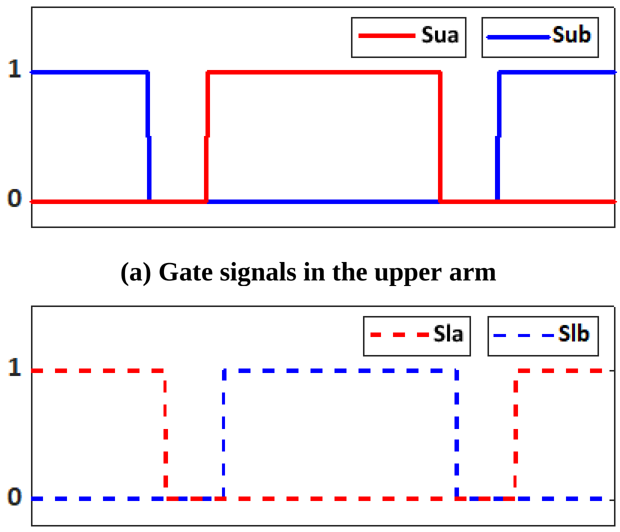
Fig. 3-9 represents the case that the phase leg dead-time is longer than the power cell dead-time. The current starts from flowing through the main switches in the lower arm. After turning on S_{lb}, the auxiliary switches in the lower arm cells start to conduct current, the cell output voltages of the lower arm cells change from zero to the cell capacitor voltages. However, the cell output voltages of the upper arm cells still equal to cell capacitor voltages. The converter dc bus voltage is reversely applied to the parasitic arm inductors in the phase leg and decrease the arm currents in both arms. As soon as this happens, the upper arm current will become negative and it starts to flow through the diodes of the main switches in the upper arm cells, the cell output voltages of the upper arm cell change from the cell capacitor voltages to zero. After that, the switching transient is finished, the new switching state starts, and the RLC circuit is formed. However, S_{ua} needs to be turned on soon after, otherwise the increase of the upper arm current will be interrupted after it becomes positive and starts to flow through the diodes of the auxiliary switches in the upper arm cells. After S_{lb} is turned on and before S_{ua} is turned on, the parasitic arm inductor resonates with the output capacitors of the devices in the upper arm cells. The upper arm current change around zero. When S_{ua} is turned on, it is not sure if the arm current is positive or negative, so the initial errors in the arm currents could be larger or smaller.

Then consider the other transition when upper arm cells are turned off and the lower arm cells are turned on. Fig. 3-7 represents the case that the phase leg dead-time is the same as the power cell dead-time. At the beginning of the transition, the current flows though the main switches in the upper arm. It starts to commute to the auxiliary switches in the upper arm and the main switches in the lower arm when turning off S_{ua} and S_{lb}. The cell output voltages of the upper arm cells change from zero to the cell capacitor voltages. However, the cell output voltages of the lower arm cells do not change instantly with zero cell currents, and still equal to cell capacitor voltages. The converter dc bus voltage is reversely applied to the parasitic arm inductors in the phase leg and decrease the arm currents in both arms. As soon as this happens, the lower arm current will become negative and it starts to flow through the diode of the main switches in the lower arm cells, the cell output voltages of the lower arm cell change from the cell capacitor voltages to zero. After that, the switching transient is finished, the new switching state starts, and the RLC circuit is formed. The upper arm current will change from the phase leg output current to zero, the lower arm current will change from zero to the reversed phase leg output current.

Fig. 3-8 represents the case that the phase leg dead-time is shorter than the power cell dead-time. At the beginning of the transition, the current flows though the main switches in the upper arm. When turning off S_{lb}, the cell output voltages of the lower arm cells do not change with zero cell currents. The current commutation starts when turning off S_{ua}, and is the same as the previous case when the phase leg dead-time is the same as the power cell dead-time.

Fig. 3-9 represents the case that the phase leg dead-time is longer than the power cell dead-time. At the beginning of the transition, the current flows though the main switches in the upper arm. After turning on S_{ua}, the auxiliary switches in the upper arm cells start to conduct current, the cell output voltages of the upper arm cells change from zero to the cell capacitor voltages. However, the lower arm current still flows through the auxiliary switches in the lower arm cells and the cell output voltages of the lower arm cells still equal to the cell capacitor voltages. The converter dc bus voltage is reversely applied to the parasitic arm inductors in the phase leg and decrease the arm currents in both arms, until the cell output voltages of the lower arm cells change from the cell capacitor voltages to zero, which happens when S_{lb} is turned off, or until the cell output voltages of the upper arm cells change from the cell capacitor voltages to zero, which happens when the upper arm current changes polarity from positive to negative and commute to the diodes of the main switches in the upper arm. After turning off S_{lb}, the switching transient is finished, the new switching state starts, and the RLC circuit is formed. However, when the new switching state starts, both arm currents already decrease, the initial errors in the arm currents are smaller, and the magnitudes of the arm current resonances during the switching state will be smaller.

To summarize the above results, optimal gate signals are shown for one switching cycle in Fig. 3-10. The phase leg dead-time is set to be shorter than the power cell dead-time in the first switching transition, but longer than the power cell dead-time in the second switching transition. The gate signals can be achieved by delaying all gate signals in the lower arm.



(a) Gate signals in the upper arm

(b) Gate signals in the lower arm

Fig. 3-10 Optimal gate signals in a phase leg to reduce current resonance magnitudes.

When the phase leg output current is negative, following the same analysis, the optimal gate signals can be achieved by delaying all gate signals in the upper arm.

With the optimal gate signals, the arm currents are forced to change rapidly during the switching transitions and the initial errors in the arm currents when the new switching state starts can be smaller.

However, this is not necessary and might be difficult to achieve when the parasitic arm inductance is low and the value of the coefficient of α is large. During the delayed period, the converter dc bus voltage is either directly applied, or reversely applied to the total parasitic inductors in the phase leg. The magnitude of the desired current change equals to the magnitude of the phase leg output current. Therefore, the desired delay period is:

$$t_{delay} = \frac{2l \times I_o}{V_{dc}} \tag{3-24}$$

Where l is the parasitic arm inductance, I_o is the phase leg output current, V_{dc} is the converter dc bus voltage. With the specifications of the simulated ICBT-based Buck converter in Section 3.2.3, and assuming the inductance value being twice the critical value, the desired delay period is only 10.8 ns. This requires the control circuit to have very high accuracy, especially if the load current can be changing, for example in the ac operation. In addition, this adds to the complexity of the converter control. Therefore, it is preferred to have low parasitic arm inductances other than using the delayed gate signals to mitigate the high arm current magnitudes. The power cell dead-time and the phase leg dead-time are set to be the same hereafter, except for some experimental results in Section 3.5.3.

3.3 Cell Capacitor Voltage Balance

In Section 3.2, it is assumed that all the cells in the same arm operate synchronously and all the cell capacitors in the same arm share the same voltage value. However, that cannot be guaranteed in the real practice. The existence of parasitic capacitors and the difference among gate signal are two factors that may interrupt the cell capacitor voltage balance. Their impacts are analyzed in this section.

For simplicity, an ICBT-based phase leg with two cells per arm is analyzed hereafter. The conclusion can be applied to the phase legs with more cells per arm.

3.3.1 Impact of Parasitic Capacitors

In power converters, parasitic capacitors generally exist between any two closely located conductors. During the switching transients, the voltages across the parasitic capacitors may change, leading to small currents through the capacitors, affecting the converter operation in different ways. It is well known that the parasitic capacitors between device terminals are the main factors determining the switching performance of the switching devices [64], [162], and the parasitic capacitors between device terminals and ground are main factors determining the EMI emission of the converters [163]-[165]. In [166] and [167], it is shown that the parasitic capacitors between device terminals and ground influence the voltage sharing among series-connected switching devices.

The parasitic capacitors between device terminals and ground are mainly determined by two factors. The first is the packaging of the switching devices, including but not limited to, the dimensions and the positions of the conductors. The second is the external placement and connection of devices and heatsinks. It is assumed that each cell has a grounded heatsink and the cells are built in the same way. Therefore, for the devices in different cells, they have similar parasitic capacitors from their terminals to ground. The grounding of the converter does not impact the following analyses much. It is assumed that the negative rail of the converter dc bus is grounded. To analyze only the impact of parasitic capacitors, it is assumed that all the devices are identical, the gate signals are perfectly synchronized.

As the gate terminal of a switching device is usually small in size, the parasitic capacitor between a gate terminal and ground has a low capacitance value, around several picofarad. During switching transients, the voltage across a gate terminal parasitic capacitor approximately changes with the potential of the source terminal of the corresponding switching device. The small discharging or charging current through the parasitic capacitor will adds to or subtracts from the current from the gate driving circuit to the device gate terminal, speeding up or slowing down the switching of the device. For devices at different locations, the terminals experience different voltage changes during the same switching transient, causing different currents through the parasitic capacitors, then different device gate terminal currents and different switching speeds.

To better illustrate the mechanism, a Buck converter is built in LTspice with the phase leg consisting of series-connected switches. The specifications of the converter are shown in Tab. 3-6. The circuit diagram of the phase leg is shown in Fig. 3-11. The simulation model for 10 kV, 40 A XHV9 SiC MOSFET modules from Wolfspeed is used to accurately simulate the switching transients. A 5 pF parasitic capacitor is added between each device gate terminal and ground.

The simulation results of the upper arm during a switching transition when the devices turn off in the upper arm, the devices turn on in the lower arm are shown in Fig. 3-12. Fig. 3-12(a) shows the voltages across two device gate terminal parasitic capacitors in the upper arm. Before the transition, both devices are on, the voltage potentials of two device gate terminals are around the dc bus voltage. After the transition, both voltage potentials will decrease. However, for the first device from the top, the voltage potential decreases by approximately half of the dc bus voltage, while for the second device, the voltage potential decreases to around zero.

Tab. 3-6 Specifications of a Buck converter.

Parameter	Value
DC Bus Voltage	12 kV
Output Voltage	7.5 kV
Output Current	25 A
Switching Frequency	10 kHz

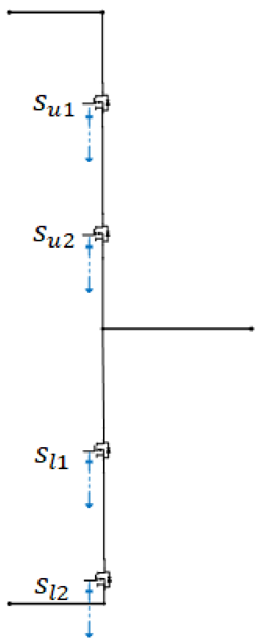
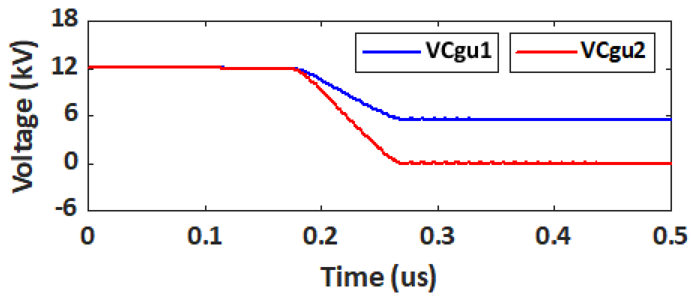


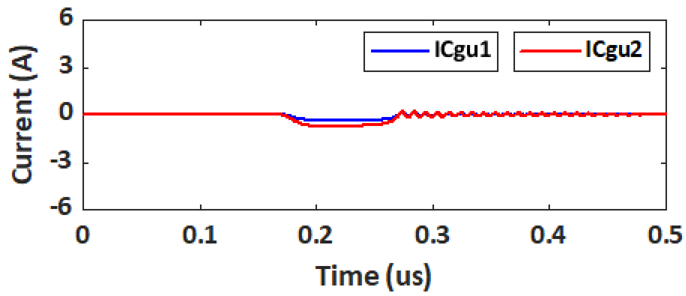
Fig. 3-11 A phase leg with two series-connected switches per arm.

Fig. 3-12(b) shows the currents through two parasitic capacitors. There are discharging currents through both capacitors, as the voltages across both capacitors reduce. The discharging current at the second device has twice the magnitude as the voltage change is twice.

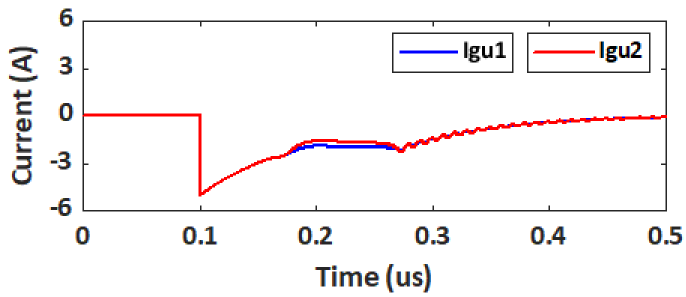
Fig. 3-12(c) shows the currents into the two device gate terminals. The device gate terminal discharging current equals to the gate driving circuit current minus the discharging current of the parasitic capacitors. Both gate terminal currents have smaller magnitude than designed and the magnitude of the gate terminal current in the second device is lower because more current is divided to discharge the parasitic capacitor.



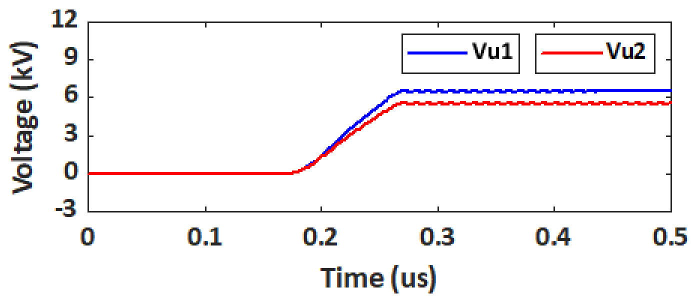
(a) Gate terminal parasitic capacitor voltages



(b) Gate terminal parasitic capacitor currents



(c) Device gate terminal currents



(d) Device voltages

Fig. 3-12 Simulation results with two series-connected switches per arm.

Fig. 3-12(d) shows the drain-to-source voltages of two devices. The first device has a faster switching speed because of the larger gate current. Then it blocks higher voltage than the second device after the switching transition finishes. The voltage difference between the two devices is 0.96 kV, which is 16% of the rated voltage for each device.

Similar phenomenon exists among series-connected ICBT cells. Fig. 3-13 shows an ICBT-based phase leg with two ICBT cells per arm. Then a Buck converter with the ICBT-based phase leg is built in LTspice, with the same specifications are shown in Tab. 3-6. The same switching device simulation model is used, and the same 5 pF parasitic capacitor is added between each device gate terminal and ground. The parasitic arm inductance is 0.1 μH, the parasitic arm resistance is 0.2 Ω, the cell capacitance is 0.1 μF.

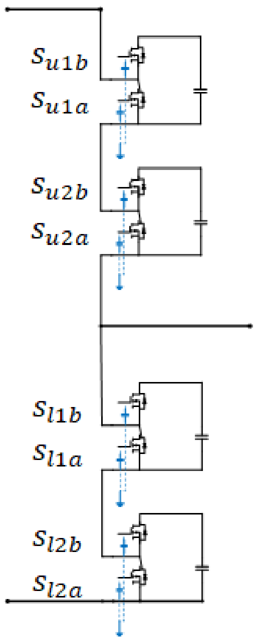
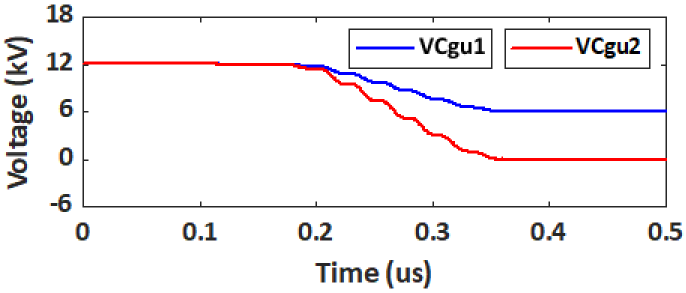


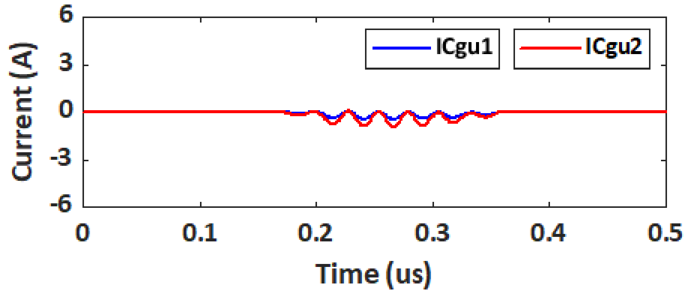
Fig. 3-13 An ICBT-based phase leg with two cells per arm.

The simulation results of the upper arm during a switching transition when the cells turn off in the upper arm, the cells turn on in the lower arm are shown in Fig. 3-14. Fig. 3-14(a) shows the voltages across two bottom device gate terminal parasitic capacitors in the upper arm. The voltage of the parasitic capacitor in the first cell decreases from the converter dc bus voltage to half of the converter dc bus voltage. The voltage of the parasitic capacitor in the second cell decreases from the converter dc bus voltage to zero.

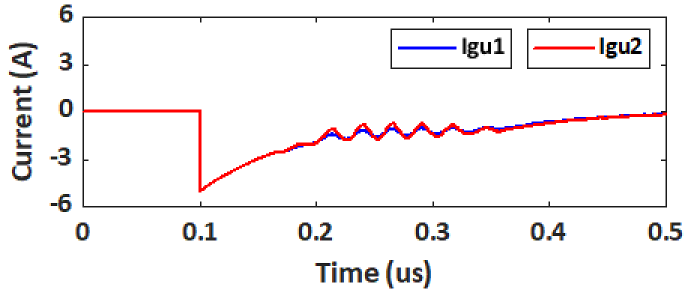
Fig. 3-14(b) shows the currents through two parasitic capacitors. There are discharging currents through both capacitors, and the current at the capacitor in the second cell has twice the magnitude as the voltage change is twice.



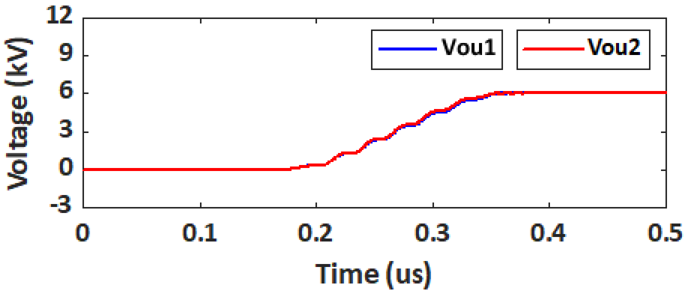
(a) Bottom device gate terminal parasitic capacitor voltages



(b) Bottom device gate terminal parasitic capacitor currents



(c) Bottom device gate terminal currents



(d) Cell output voltages

Fig. 3-14 Simulation results with two ICBT cells per arm: transition I.

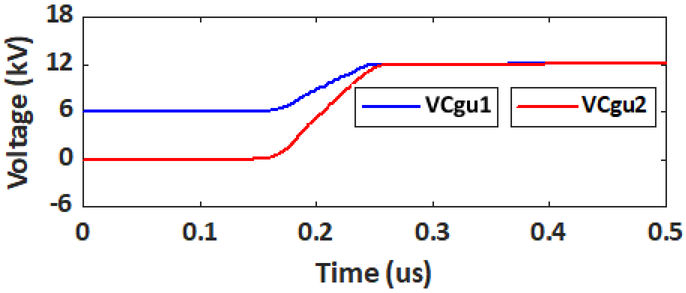
Fig. 3-14(c) shows the currents into the two bottom device gate terminals. Both gate terminal currents have smaller magnitude than designed and the magnitude of the gate terminal current at the bottom device in the second cell is lower because more current is divided to discharge the parasitic capacitor.

Fig. 3-14(d) shows the two cell output voltages, which are the same as the drain-to-source voltages of two bottom devices. Although the two cells have different switching speeds, the two cell output voltages are similar after the switching transition finishes. This is because each bottom device blocks its corresponding cell capacitor voltage, instead of sharing the whole converter dc bus voltage directly.

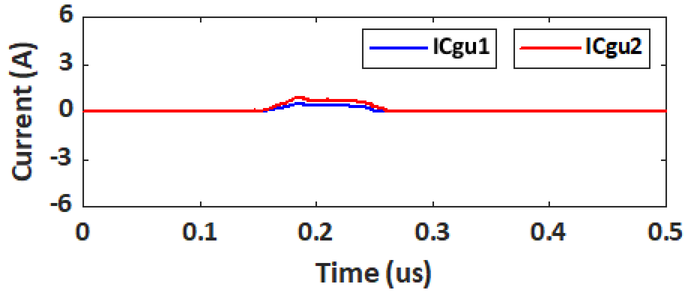
Similar phenomenon exists during the other type of the switching transition. The simulation results of the upper rm during a switching transition when the cells turn off in the upper arm, the cells turn on in the lower arm are shown in Fig. 3-15. Fig. 3-15(a) shows the voltages across two bottom device gate terminal parasitic capacitors in the upper arm. The voltage of the parasitic capacitor in the first cell increases from half of the converter dc bus voltage to the converter dc bus voltage. The voltage of the parasitic capacitor in the second cell increases from zero to the converter dc bus voltage.

Fig. 3-15(b) shows the currents through two parasitic capacitors. There are charging currents through both capacitors, and the current at the capacitor in the second cell has twice the magnitude as the voltage change is twice.

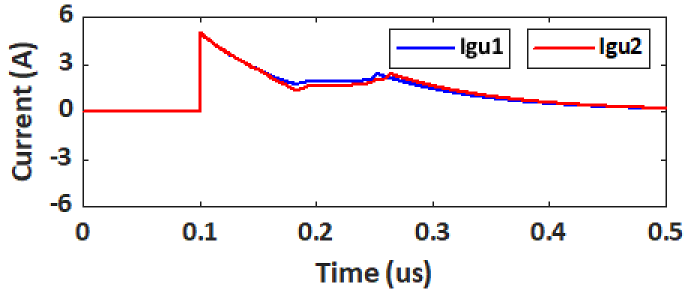
Fig. 3-15(c) shows the currents into the two bottom device gate terminals. Both gate terminal currents have smaller magnitude than designed and the magnitude of the gate terminal current at the bottom device in the second cell is lower because more current is divided to charge the parasitic capacitor.



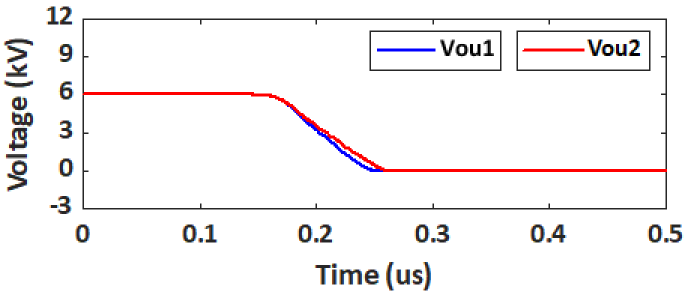
(a) Bottom device gate terminal parasitic capacitor voltages



(b) Bottom device gate terminal parasitic capacitor currents



(c) Bottom device gate terminal currents



(d) Cell output voltages

Fig. 3-15 Simulation results with two ICBT cells per arm: transition II.

Fig. 3-15(d) shows the two cell output voltages. Both voltages approximately change from half of the converter dc bus voltage to zero. As the bottom device in the second cell has lower gate current, it turns on slower. The cell output voltage of the second cell is slower compared to the first cell.

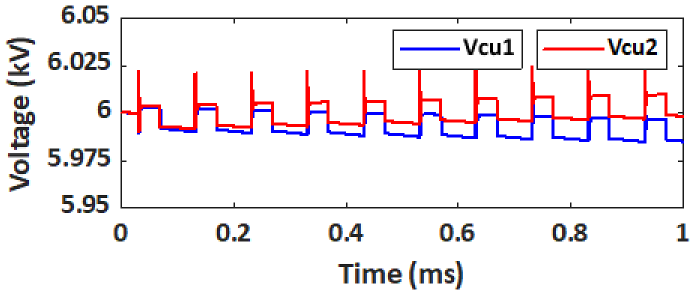
As a summary, the gate terminal parasitic capacitors located around different switching devices experience different voltage changes during switching transients and therefore have different impacts on the switching devices, causing different switching speeds. The exact impact depends on the load current polarity, switching transition type, and the cell location.

When the cells have different switching speeds, the cell capacitors are connected to or disconnected from the arm in different ways, leading to slightly different cell capacitor charges during the switching transitions.

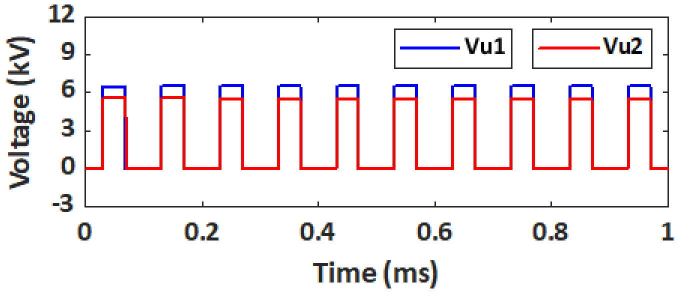
Fig. 3-16(a) shows the two cell capacitor voltages in the phase leg with two ICBT cells per arm for ten switching cycles. The cell capacitor voltages are the voltages that the devices need to block. Because of the different switching speeds, after each turn-off or turn-on transition, the cell capacitor voltage difference changes slightly. With 0.1 μF cell capacitance, the voltage difference between the two cell capacitors is 0.013 kV, which is 0.22% of the rated voltage for each cell, after ten switching cycles.

For comparison, Fig. 3-16(b) shows the two device voltage in the phase leg with two series-connected devices per arm for ten switching cycles. After each turn-off transition, there is a voltage difference of 0.96 kV between the two devices. But after each turn-on transition, the device voltage difference is reset to 0.

In ICBT-based converters, the voltage unbalance develops much slower than the voltage unbalance among series-connected devices. The voltage unbalance keeps accumulating on the cell capacitors and needs to be controlled. However, the requirement on the control bandwidth is largely reduced.



(a) Cell capacitor voltages in phase leg with ICBT cells



(b) Device voltages in phase leg with series-connected switches

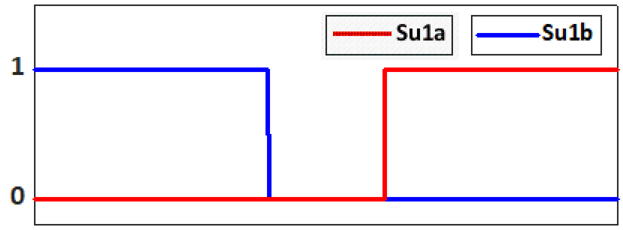
Fig. 3-16 Voltage unbalance comparison.

By using series-connected ICBT cells, it also provides the possibility to avoid the gate terminal parasitic capacitors from affecting capacitor voltage balancing. This can be achieved if the heatsinks are not grounded but instead connected to a local reference point in the corresponding cell. For example, the heatsink can be connected to the middle point, or the negative terminal, or the positive terminal of the cell capacitor. Theoretically, this will eliminate the impact of gate terminal parasitic capacitors on the voltage balancing because the voltage changes across gate terminal parasitic capacitors in different cells will be the same.

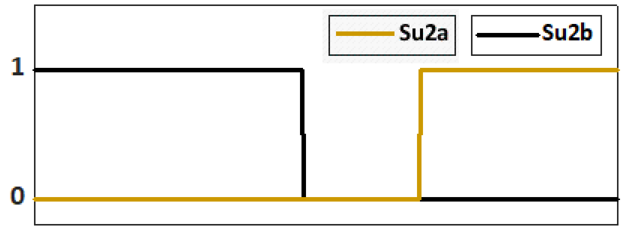
3.3.2 Impact of Gate Signal Delays

The series-connected ICBT cells are supposed to operate synchronously. However, that cannot be guaranteed as different channels of control and gate driving circuits always have slightly differences.

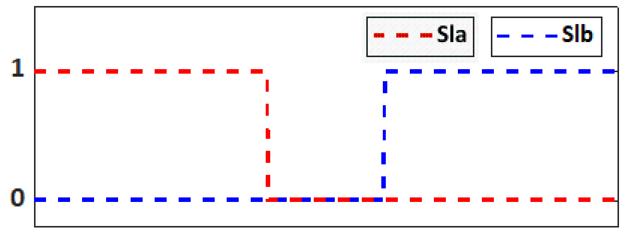
The ICBT-based phase leg with two ICBT cells per arm shown in Fig. 3-13 is studied. Fig. 3-17 shows the gate signals in a phase leg during a switching transition when the cells turn on in the upper arm, the cells turn off in the lower arm, while the two gate signals for the second cell in the upper arm are slightly delayed compared to the gate signals for the other three cells.



(a) Gate signals for the first cell in the upper arm



(b) Gate signals for the second cell in the upper arm



(c) Gate signals for the two cells in the lower arm

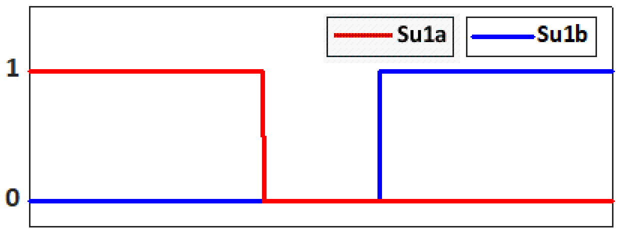
Fig. 3-17 Gate signals in a phase leg with turn-on delay in the upper arm.

Firstly, consider the case when the phase leg output current is positive. When S_{u1a} changes from low to high, the cell output voltage of the first upper arm cell changes from the cell capacitor voltage to zero. At the same time, S_{lb} changes from low to high, the cell output voltages of the two lower arm cell changes from zero to the cell capacitor voltages. The cell output voltage of the second upper arm cell does not change instantly and still equals to the cell capacitor voltage. Then there is a voltage difference in the phase leg, which equals to one cell capacitor voltage and is reversely applied to the parasitic inductors in the phase leg and decrease the arm currents in both arms. As soon as this happens, the upper arm current will become negative and it starts to flow through the diode of the main switch in the second upper arm cell, the cell output voltage of the cell changes from the cell output voltage to zero. After the first upper arm cell turns on and before the second upper arm cell turns on, the first upper arm cell capacitor is bypassed while the second upper arm cell capacitor is still connected into the arm. Therefore, the two upper arm cell capacitors have slightly different charges because of the delay. However, because the arm current is around zero during this time, this delay does not change the cell capacitor voltages much. The duration is mainly decided by the cell capacitor voltage, parasitic arm inductance, and the output capacitors of the devices. A longer delay in the gate signals for the second upper arm cell will not lead to larger cell capacitor difference.

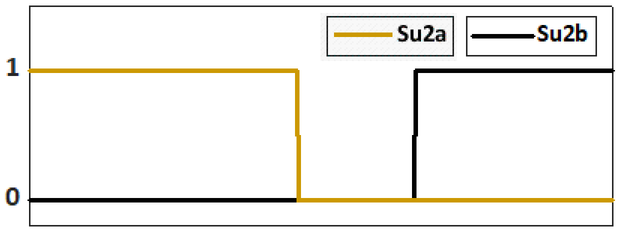
Then consider the same transition but with a negative phase leg output current. When S_{la} changes from high to low, the cell output voltages of the two lower arm cells change from zero to the cell capacitor voltages. The cell output voltages of the two upper arm cells do not change instantly and still equals to the cell capacitor voltages. Then there is a voltage difference in the phase leg, which equals to twice the cell capacitor voltage and is reversely applied to the parasitic inductors in the phase leg and decrease the arm currents in both arms. As soon as this happens, the upper arm current will become negative and it starts to flow through the diode of the main switch in the first upper arm cell, the cell output voltage of the cell changes from the cell output voltage to zero. However, the cell output voltage of the second upper arm cell is still the cell capacitor voltage as S_{u2b} is still high. There is a voltage difference in the phase leg, which equals to one cell capacitor voltage and is reversely applied to the parasitic inductors in the phase leg and decrease the arm currents in both arms. After the first upper arm cell turns on and before S_{u2b} changes from high to low, the first upper arm cell capacitor is bypassed while the second upper arm cell capacitor is still connected into the arm. During this period, the upper arm decreases from zero and remains negative, the second cell capacitor is discharged by the negative arm current while the first cell capacitor voltage remains constant. The cell capacitor voltage in the cell with the delayed gate signals will decrease, and the longer the delay is, the more the capacitor voltage will decrease.

During the delayed period, the upper arm current deceases from zero, the lower arm current decreases from a positive value, which equals to the magnitude of the phase leg output current. Because of the low parasitic inductance value, the currents change fast. However, even if S_{u2b} is delayed for a very long time, the arm currents will not decrease infinitely. When the lower arm current decreases and changes polarity from positive to negative, the lower arm current starts to commute to the diodes of the main switches in the lower arm cells, and the cell output voltages of the lower arm cells start to decrease, and the decrease of two arm currents will slow down. There is a resonance between the device output capacitors in the lower arm and the parasitic inductor in the lower arm. As a result, the lower arm current oscillates around 0, the output voltage of each lower arm cell oscillates around half of the cell capacitor voltage. In the upper arm, the cell output voltage of the first cell is zero, the cell output voltage of the second cell is the cell capacitor voltage. Therefore, the total cell output voltages in the phase leg oscillates around twice the cell capacitor voltage, which means it oscillates around the converter dc bus voltage. The arm currents will not keep decreasing. Then the upper arm current stays negative, with the magnitude around the magnitude of the phase leg output current.

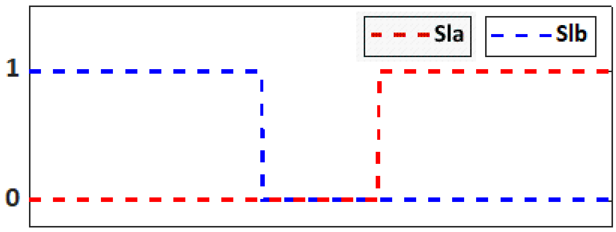
Then consider the other switching transition. Fig. 3-18 shows the gate signals in a phase leg during a switching transition when the cells turn off in the upper arm, the cells turn on in the lower arm, while the two gate signals for the second cell in the upper arm are slightly delayed compared to the gate signals for the other three cells.



(a) Gate signals for the first cell in the upper arm



(b) Gate signals for the second cell in the upper arm



(c) Gate signals for the two cells in the lower arm

Fig. 3-18 Gate signals in a phase leg with turn-off delay in the upper arm.

Firstly, consider the case when the phase leg output current is positive. When S_{u1a} changes from high to low, the cell output voltage of the first upper arm cell changes from zero to the cell capacitor voltage. The cell output voltages of the other three cell do not change instantly. There is a voltage difference in the phase leg, which equals to one cell capacitor voltage and is reversely applied to the parasitic inductors in the phase leg and decreases the arm currents in both arms. As soon as this happens, the lower arm current will become negative and it starts to flow through the diode of the main switches in the two lower arm cells, the cell output voltages of the two cells change from the cell output voltage to zero. However, the cell output voltage of the second upper arm cell is still zero as S_{u2a} is still high. After S_{u1a} changes from high to low and before S_{u2a} changes from high to low, the first upper arm cell capacitor is connected into the arm while the second upper arm cell capacitor is bypassed. During this period, the upper arm decreases from a positive value, which equals to the magnitude of the phase leg output current. The first cell capacitor is charged by the positive arm current while the second cell capacitor voltage remains constant. The cell capacitor voltage in the cell without the delayed gate signals will increase, and the longer the delay is, the more the capacitor voltage will increase.

After S_{u1a} changes from high to low and before S_{u2a} changes from high to low, there is a resonance between the device output capacitors in the lower arm and the parasitic inductor in the lower arm. As a result, the lower arm current oscillates around 0, the output voltage of each lower arm cells oscillates around half of the cell capacitor voltage. In the upper arm, the cell output voltage of the first cell is the cell capacitor voltage, the cell output voltage of the second cell is zero. The total cell output voltages in the phase leg oscillates around the converter dc bus voltage. Then the upper arm current stays positive, with the magnitude around the magnitude of the phase leg output current.

Then consider the same transition but with a negative phase leg output current. When S_{u1b} changes from low to high, the cell output voltage of the first upper arm cell changes from zero to the cell capacitor voltage. At the same time, S_{la} changes from low to high, the cell output voltages of the two lower arm cell changes from the cell capacitor voltages to zero. The cell output voltage of the second upper arm cell does not change instantly and still equals to zero. Then there is a voltage difference in the phase leg, which equals to one cell capacitor voltage and is applied to the parasitic inductors in the phase leg and increase the arm currents in both arms.

The cell output voltage of the second upper arm cell will change from zero to the cell capacitor voltage when S_{u2b} changes from low to high, or when the upper arm current change polarity from negative to positive, whichever happens first. If S_{u2b} changes from low to high first, after S_{u1b} changes and before S_{u2b} changes, the first upper arm cell capacitor is connected into the arm while the second upper arm cell capacitor is bypassed. During this period, the upper arm increases from a negative value, which equals to the magnitude of the phase leg output current, the first cell capacitor is discharged by the negative arm current while the second cell capacitor voltage remains constant. The cell capacitor voltage in the cell without the delayed gate signals will decrease.

However, if S_{u2b} is delayed for a very long time, the change in the upper arm current decides when the second upper arm cell turns off. After the first upper arm cell turns off and before the second upper arm cell turns off, the upper arm current increases from a negative value to a positive value. Therefore, the impact of delays on the cell capacitor voltages is not clear. In addition, a longer delay will not have larger impact of the cell capacitor voltages.

The above analyzes can be applied to the lower arm in the same way, as long as the polarity of the arm current is used.

As a summary, during a turn-on transition with a positive arm current, the gate signal delays do not change the cell capacitor voltages much; during a turn-on transition with a negative arm current, the cell capacitor voltage in the cell with delayed gate signals will decrease and will decrease more with a longer delay; during a turn-off transition with a positive arm current, the cell capacitor voltage in the cell without the delayed gate signals will increase and will increase more with a longer delay; during a turn-off transition with a negative arm current, the impact of gate signal delays on the cell capacitor voltages is not clear.

To mitigate the impact of gate signal delays on the cell capacitor voltage balancing, the control signals need to have high accuracy and need to be well synchronized, all control and driving circuits need to be very consistent with each other.

3.4 Control of ICBT-based Converters

A two-level control method is proposed for ICBT-based converters to generate desired outputs and regulate cell capacitor voltages.

3.4.1 Converter Output Control

As series-connected ICBT-cells operate as an equivalently high-voltage switching device, at the converter level, the ICBT-based converter can be controlled in similar ways as the traditional two-level converter. The duty ratio of the phase leg can be calculated by either an open-loop control, or a closed-loop voltage or current control that regulates the converter output voltage or current. Then the duty ratios of the upper arm cells are the same as the duty ratio of the phase leg, while the duty ratios of the lower arm cells are the complementary duty ratio of the phase leg.

3.4.2 Cell Capacitor Voltage Control

As analyzed in Section 3.3, the existence of parasitic capacitors and the difference among gate signal are two factors that may interrupt the cell capacitor voltage balance. In addition, the switching devices always slightly different characteristics, which is another main cause of the unbalance. The voltage unbalance keeps accumulating on the cell capacitors. Although the main factors of unbalance are identified and corresponding mitigation methods can be applied, a closed-loop cell capacitor is essential to ensure the cell capacitor voltage balance.

In a converter arm consisted of series-connected ICBT cells, the sum of the cell capacitor voltages in each arm is decided by the converter dc bus voltage and the voltage drop on the parasitic passive components in the phase leg, as shown in Section 3.2.1. Therefore, the capacitor voltage control can be achieved by controlling the capacitor voltage difference instead of controlling each capacitor voltage individually. Specifically, only the voltage difference within an arm needs to be controlled.

In an ICBT cell, the cell capacitor voltage does not change when the cell is in the on state as the capacitor is bypassed. For the cells in the same arm, the cell capacitor voltage difference does not change when they are all in the off state as the capacitors share the same current. The cell capacitor voltage difference is only possible to change during the switching transients.

The impact of gate signal delays on the cell capacitor voltage balancing can be utilized to control the voltage difference no matter what causes the unbalance. Applying delays to gate signals to some of the series-connected ICBT cells may force the cells to switch at different instants, and force the cell capacitors to have different currents for short periods of time during the transitions. As a result, the cell capacitor voltage difference can be changed.

Based on the analyses in Section 3.3.2, when the arm current is positive, delays during the turn-on transitions do not change the cell capacitor voltages mush, delays during the turn-off transitions increase the cell capacitor voltage in the cell without the gate signals delays. Therefore, when the arm current is positive, turn-off delays should be applied to the cell with a higher cell capacitor voltage. When the arm current is negative, delays during the turn-on transition decrease the cell capacitor voltage in the cell with the gate signal delays; delays during the turn-off transition may increase or decrease the cell capacitor voltage in the cell with the delays. Therefore, when the arm current is positive, turn-off delays should be applied to the cell with a higher cell capacitor voltage

For either arm current polarity, the applied delays relatively decrease the cell capacitor voltage in the cell with gate signal delays. During the delayed period, one cell capacitor is bypassed while the other cell capacitor in the arm is charged or discharged by the arm current. The magnitude of the arm current change quickly, but changes around the magnitude of the phase leg output current if the delay duration is long. Therefore, assuming the delays are applied to the second cell in the arm, the cell capacitor voltage difference changes by:

$$\Delta\left(V_{c,1} - V_{c,2}\right) \approx \frac{I_o \times t_d}{C} \tag{3-25}$$

Where $V_{c,1}$ is the cell capacitor voltage of the first cell in the arm, $V_{c,2}$ is the cell capacitor voltage of the second cell in the arm, $(V_{c,1} - V_{c,2})$ is the cell capacitor voltage difference between the two cell capacitors, $\Delta(V_{c,1} - V_{c,2})$ is the change of the cell capacitor voltage difference after one switching transition, I_o is the phase leg output current, t_d is the delay time between the gate signals of the two cells, C is cell capacitor capacitance value. However, as the arm current changes quickly, the accuracy of the estimated capacitor voltage change depends on the delay time, parasitic impedances and the converter operation conditions.

The converter-level control sends the same duty ratio value to all the cells in the same arm. Then at each cell, the capacitor voltage control is calculated to potentially apply turn-on or turn-off delays according to the sensed cell capacitor voltage and the arm current polarity, the latter could be decided based on the phase output current polarity and the cell location.

The two arms operate complementarily and have different arm current polarities. Therefore, the turn-off transition with a negative arm current of one arm and the turn-on transition with a positive arm current of the opposite arm is the same transition. To avoid the delays in opposite arms affect each other, the two arms are alternatively allowed to apply delays to adjust the cell capacitor voltage difference.

This capacitor voltage control method can work with either current polarity, works in the same way in either the upper arm or the lower arm, and works in similar ways regardless of the number of cells in the arm. Depending on how the delay values are calculated, the cell capacitor voltage control may work independently at each cell. The delay value of one cell may be calculated without any information of the other cells, or with minimum information of the other cells. Increasing the number of cells in the arm does not significantly increase the complexity of the control.

More details about the cell capacitor voltage control and its implementation are presented in Section 3.5.4 and 3.5.5.

3.5 Experimental Results

A modular Medium Voltage converter is used as the test bed for the ICBT operation and control, with the specifications shown in Tab. 3-7. The converter has identical power cells, which are built with 10 kV, 40 A XHV9 SiC MOSFET modules from Wolfspeed. The converter has two phase legs, which are built by connecting multiple power cells together. The design and construction of the converter are the results of teamwork. The converter design details are shown in [168]-[171].

Because of the modularity, each cell is verified first after built, and the converter is tested with one cell per arm first, then with increasing number of cells.

Tab. 3-7 Specification of the modular MV converter.

Parameter	Value
DC Bus Voltage	24.0 kV
Number of Cells per Arm	4
Cell Capacitor Voltage	6.0 kV
Cell Capacitance	32.5 µF
Switching Frequency	10 kHz

3.5.1 Testing of Power Cells

Pump-back test is conducted to verify the performance of the power cells at the rated voltage and current during the continuous operation. Two half-bridge power cells are used in as the two test units the test. The dc buses of them are connected together to a voltage source, the output terminals of them are connected through a load inductor. The bus voltage is set by adjusting the output voltage of the voltage source, and the output current is controlled by adjusting the gating signals of the switches. Usually, the gate signals in one unit are generated by an open-loop control to achieve a desired output voltage, while the gate signals in the other unit are generated by a closed-loop current control to achieve a desired output current [172]-[174]. During the test, the rated power is circulating between two test units while the voltage source only provides the total losses of the setup.

There are four switching states depending on which two switches conduct current, as shown in Fig. 3-19. During State I, the dc bus voltage is applied on the load inductor, increasing the output current. During State III, the dc bus voltage is reversely applied on the load inductor, decreasing the output current. During State II and State IV, the current flows through the inductor, as well as either two top switches or two bottom switches. The output current decreases slightly because of losses.

As the output current only changes significantly in State I and III, the time durations of these two switching states are controlled to regulate the output current to be as desired. The output current could have a variety of different profiles and different control methods could be used. In this study, two operation modes and their corresponding control algorithms are explored.

In the dc operating mode, each cell has a dc input voltage and a dc output voltage. The output current is a dc current with the ripple within each switching cycle.

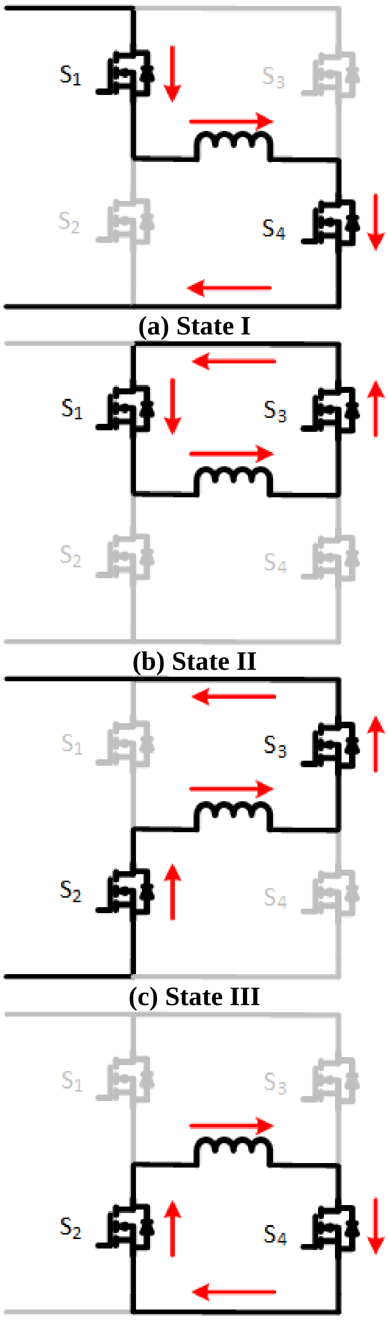


Fig. 3-19 Switching states in the power cell pump-back test.

The duty ratio of S_1, the top switch in the first phase leg, is set to be:

$$d_{1,dc} = 0.5 \tag{3-26}$$

The turn-on of the S_3, the top switch in the second phase leg is set to have a small fixed delay, for example, 1% of a switching cycle, compared to the turn-on of S_1. The turn-off of S_3 also has a delay compared to the turn-off of S_1. The turn-off delay is calculated by the closed-loop current control to regulate the output current to be the desired value. The two bottom switches operate complementarily with the two top switches respectively.

In the ac operating mode, each cell has a dc input voltage and an ac output voltage with a dc offset. The output current is an ac current repeating every output line cycle.

The duty ratio of S_1, the top switch in the first phase leg, is set to be:

$$d_{1,ac} = 0.5 + m \times \sin(\omega t) \tag{3-27}$$

Where $d_{1,ac}$ is the duty ratio of the top switch in the first phase leg in the ac operation, m is the modulation index, ω is the angular frequency.

The duty ratio of S_3 has a small difference compared to S_1, which is calculated by the closed-loop current control to regulate the output current to be the desired value.

All sixteen power cells in the converter are tested in the power cell pump-back test and in both the dc and ac operation modes. One power cell and its key components are shown in Fig. 3-20.

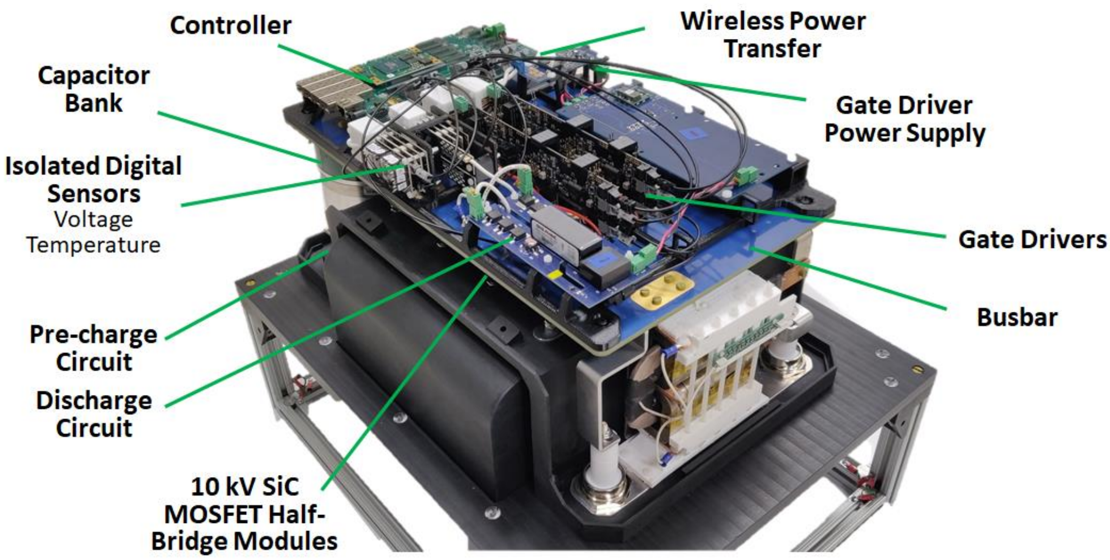
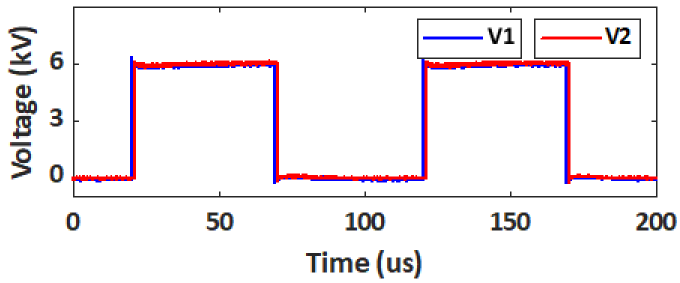
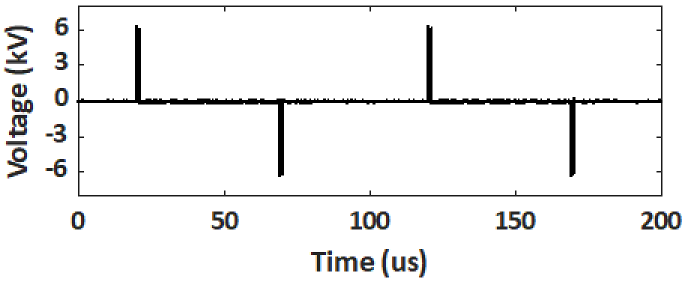


Fig. 3-20 One power cell with 10 kV SiC MOSFET modules.

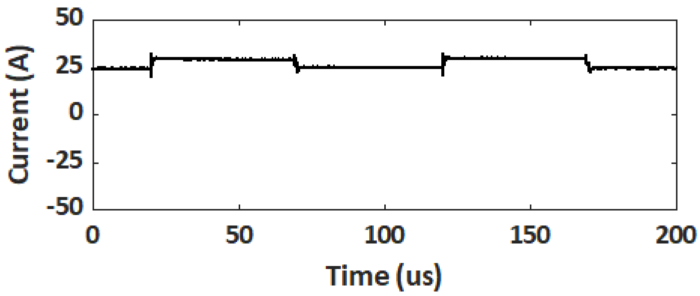
The typical experimental results in the dc operation are shown for two switching cycles in Fig. 3-21. The dc bus voltage is set to be 6 kV, the output current is controlled to be 28 A.



(a) Output voltages



(b) Load voltage



(c) Load current

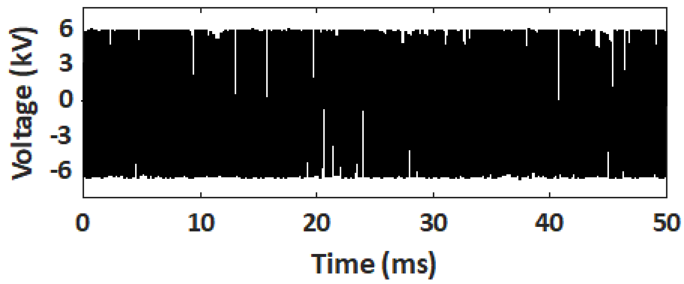
Fig. 3-21 Power cell pump-back test results: dc operation mode.

Fig. 3-21(a) shows the output voltages of the two phase legs. The output of each phase leg switches between 0 and 6 kV. The output voltage of the second phase leg has slightly delays at both transitions.

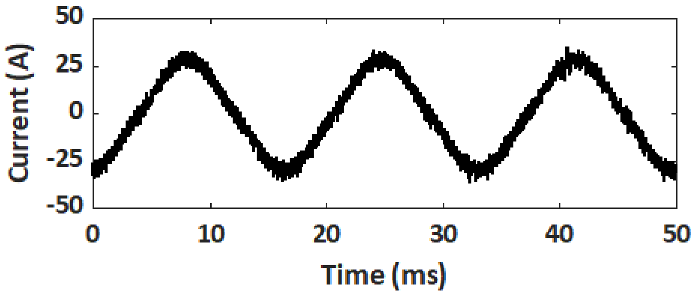
Fig. 3-21(b) shows the load inductor voltage, which is the difference of the two phase leg output voltages. It has a short positive pulse and a short negative pulse per switching cycle. The magnitude of the pulses is 6 kV.

Fig. 3-21(c) shows the load inductor current with an average value of 28 A. The current increases quickly when the load inductor voltage is positive, decreases quickly when the load inductor voltage is negative, and decrease slowly when the load inductor voltage is around zero.

The typical experimental results in the ac operation are shown for three line cycles in Fig. 3-22. The dc bus voltage is set to be 6 kV, the output current is controlled to be 20 Arms.



(a) Load voltage



(b) Load current

Fig. 3-22 Power cell pump-back test results: ac operation mode.

Fig. 3-22(a) shows the load inductor voltage, which is the difference of the two phase leg output voltages. It has short positive pulses and short negative pulses. The magnitude of the pulses is 6 kV. Fig. 3-22(b) shows the load inductor current with a rms value of 20 A.

Depending on the intended operation condition, the output voltage and current of the power cell can be controlled in more ways. For example, the current through a cell in an MMC contains both dc component and ac component. Therefore, a pump-back test with an output current containing both dc component and ac component could be useful.

3.5.2 Testing of a Modular Converter

The pump-back test is conducted for the phase legs to verify the performance of the converter during the continuous operation. Two ICBT-based phase legs consisting of one or more ICBT cells per arm are used. The two phase legs are connected together to a voltage source, the output terminals of them are connected through a load inductor. The output current control during the phase leg pump-back test is the same as the power cell pump-back test.

For medium voltage, high power, modular converters like ICBT-based converters, the energy internally stored in cell capacitors needs to be carefully dealt with. A state machine is defined for the converter, in addition to the control algorithm, to ensure the safe operation and correct functions of the converter. The state machine and the state transitions are shown in Fig. 3-23.

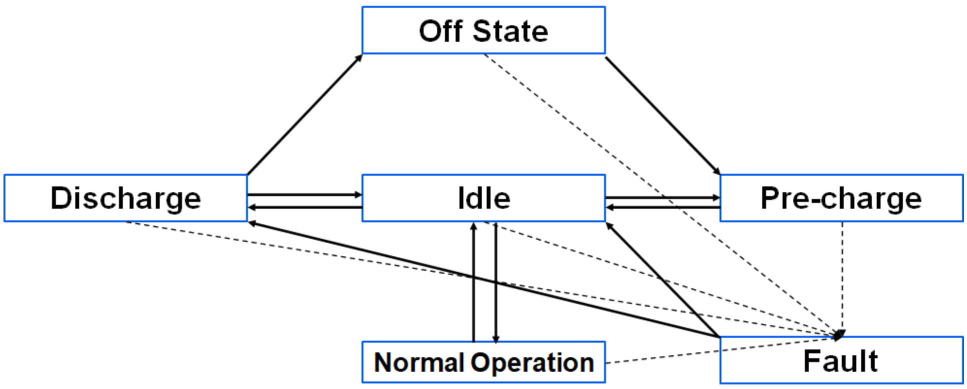


Fig. 3-23 Converter operation state machine.

There is a local controller in each cell and a main controller for the converter. The main controller connects to a computer and receives commands from it. The state is decided in the main controller and then sent to the local controllers. The local controllers act according to the state.

The converter is in the off state at the beginning of a test or the end of a test. All cell capacitors are discharged, all switching devices are turned off, all pre-charge circuits are off, all discharge circuits are on. All auxiliary circuits are operating, all the communication is operating, all hardware and software initializations are finished, and the converter is ready to be energized.

The converter will transit to the pre-charge state from the off state if it receives a “start pre-charge” command. During the pre-charge state, all switching devices are turned off, all discharge circuits are off. The pre-charge circuits charge the cell capacitors to the desired value. Each local controller turns on and off the pre-charge circuit in the cell using a hysteresis control, based on the sensing feedback of the voltage sensor.

The converter will transit to the idle state from the pre-charge state if it receives a “stop pre-charge” command. The idle state is a buffer state. During this state, all switching devices are turned off, all pre-charge circuits are off, are discharge circuits are off. All cell capacitors maintain the voltages.

The converter will transit to the normal operation state from the idle state if it receives a “start operation” command. During this state, all switching devices are switching according to the control algorithm. All pre-charge circuits are off, all discharge circuits are off.

The converter will transit to the idle state from the normal operation state if it receives a “stop operation” command. This is the buffer state and capacitors remain charged.

The converter will transit to the discharge state from the idle state if it receives a “start discharge” command. During the discharge state, all switching devices are turned off, all pre-charge circuits are off, all discharge circuits are on. The cell capacitors are discharged through the resistors in the discharge circuits.

The converter will transit to the off state from the discharge state if all the cell capacitors are fully discharged. The converter is de-energized other than the low-voltage auxiliary circuits.

The converter may enter the fault state from any other states if any kind of fault is detected in the system. During the fault state, all switching devices are turned off, all pre-charge circuits are off, all discharge circuits are off. The fault type and fault location are detected by controllers, summarized in the main controller, sent to the computer, and displayed on the user interface.

The converter will transit to the idle state from the fault state if it receives a “clear fault” command and the previously detected faults no longer exist. Then the converter is ready to enter other states. If the faults still exist, the converter is only allowed to transit to the discharge state from the fault state if it receives a “start discharge” command. All cell capacitors will be discharged, and the faults can be further examined.

Different fault scenarios are considered. The device over-current fault is detected by gate drivers during the normal operation state. The phase leg over-current fault is detected by the main controller based on the sensing results from the phase leg current sensor during all converter states. The cell capacitor over-voltage and under-voltage faults are detected by local controllers and the main controller based on the sensing results from voltage sensors during all converter states. Device over-temperature is detected by local controllers based on the sensing results from temperature sensors during all converter states. Communication error is detected by the main controller, local controllers, gate drivers during all converter states.

The converter experimental results are shown in the following sections. The two phase legs in the converter operate in the same way with the exception of different current polarities. The results from one phase leg will be shown in each set of results.

3.5.3 Experimental Results with One Cell per Arm

Four cells are connected to form a converter with two phase legs, one cell per arm. The converter setup with one cell per arm is shown in Fig. 3-24. The four cells from left to right are the lower arm cell in the first phase leg, the upper arm cell in the first phase leg, the lower arm cell in the second phase leg, the upper arm cell in the second phase leg. A temporary converter dc bus is used and is located on top of the second phase leg. The dc voltage source is located to the right of the converter, which connects to the converter dc bus and then to the cells. The load inductor is located to the left of the converter, and connects to the output terminals of the two phase legs.

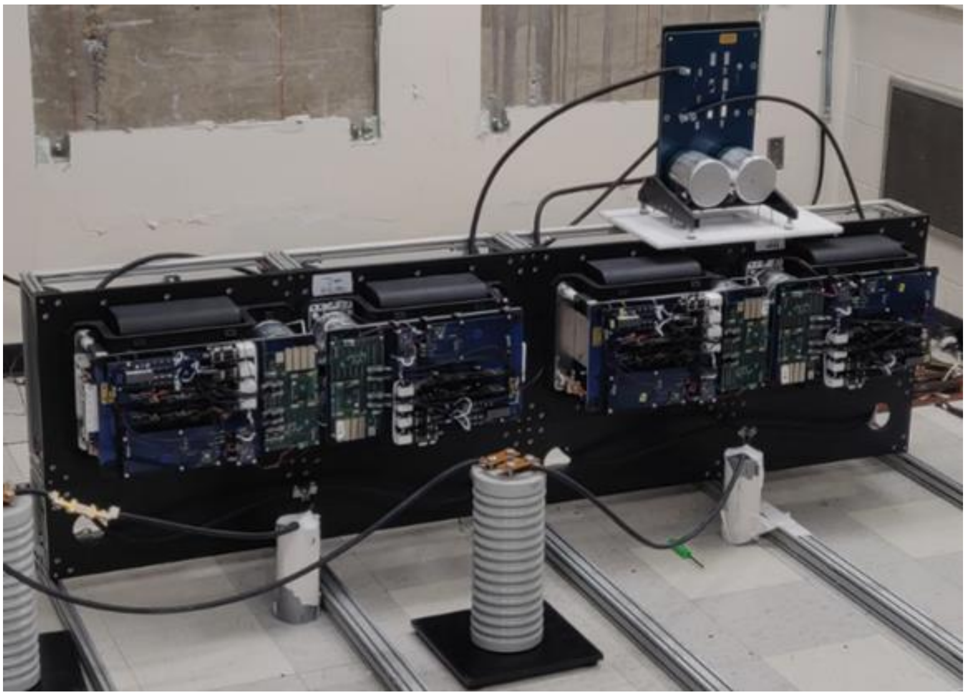
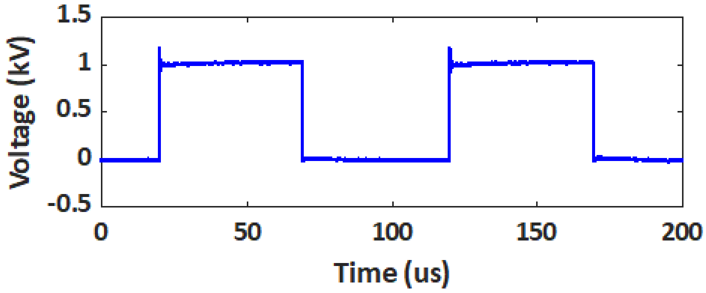
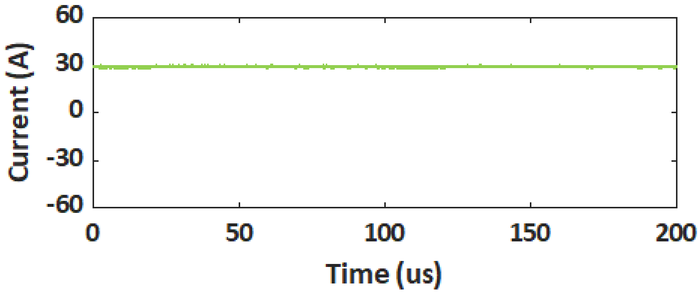


Fig. 3-24 Converter setup with one cell per arm.

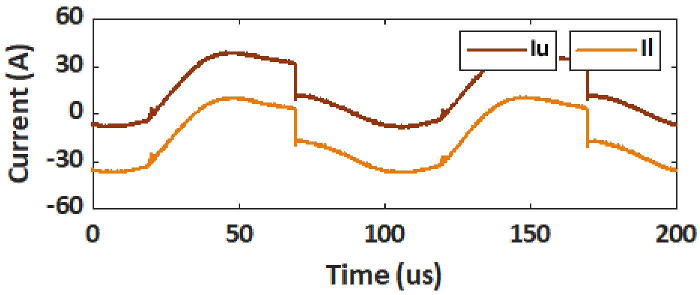
The converter is first tested at a lower than rated voltage. The experimental results at 1 kV dc bus voltage and 28 A dc output current are shown for two switching cycles in Fig. 3-25. The switching frequency is 10 kHz for all the tests.



(a) Cell output voltage of the lower arm cell



(b) Phase leg output current



(c) Arm currents

Fig. 3-25 Experimental results with one cell per arm at 1 kV, 28 A dc.

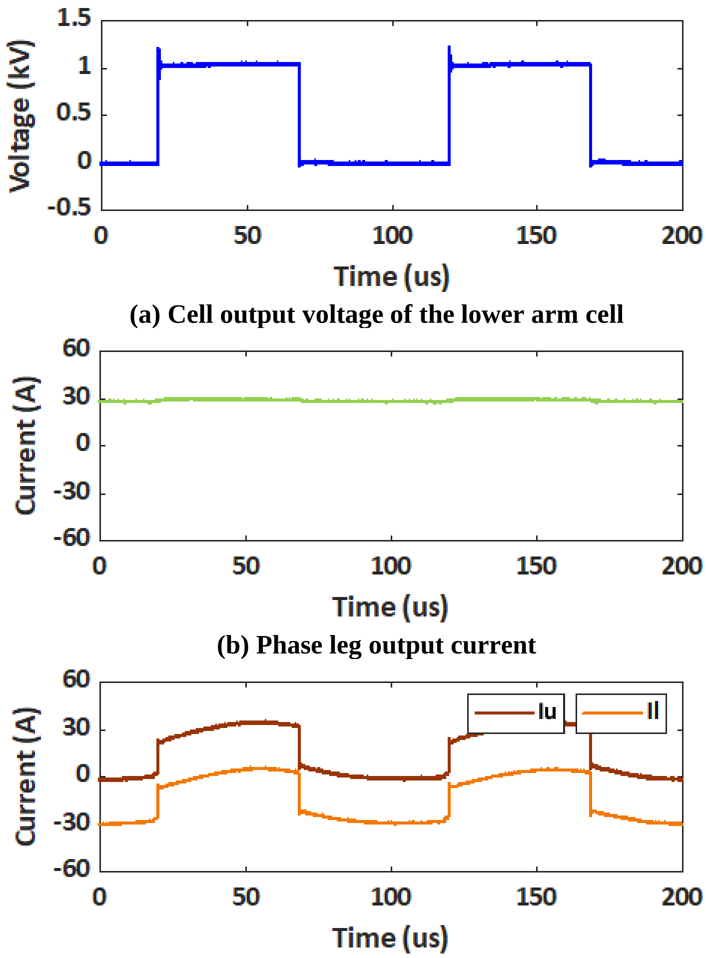
Fig. 3-25(a) shows the output voltage of the cell in the lower arm. It switches between zero and the converter dc bus voltage, 1 kV. Fig. 3-25(b) shows the phase leg output current with an average value of 28 A. Fig. 3-25(c) shows the two arm currents.

With the temporary converter dc bus and the long cables connecting the bus and the cells, the parasitic inductance is estimated to be around 3 μH per arm. Therefore, the resonance in a switching state is more significant than desired. The maximum arm current magnitude is 39.8

A, which is 33% higher than the maximum magnitude of the phase leg current. The high current magnitudes and the slow change rates of the arm currents lead to increased losses.

Based on the analyses in Section 3.2.4, one solution to reduce the current resonance magnitudes is to reduce the parasitic arm inductance value, which is achieved later with the designed converter dc bus. Based on the analyses in Section 3.2.5, another solution is to apply optimal gate signals, which includes delays in the gate signals for opposite arms.

The experimental results at 1 kV dc bus voltage and 28 A dc output current with optimal gate signals are shown for two switching cycles in Fig. 3-26.



(a) Cell output voltage of the lower arm cell

(b) Phase leg output current

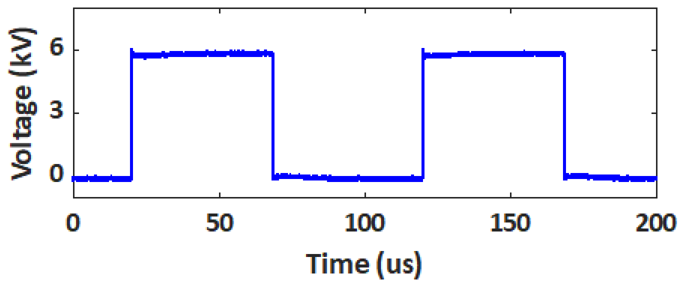
(c) Arm currents

Fig. 3-26 Experimental results with one cell per arm at 1 kV, 28 A dc with optimal gate signals.

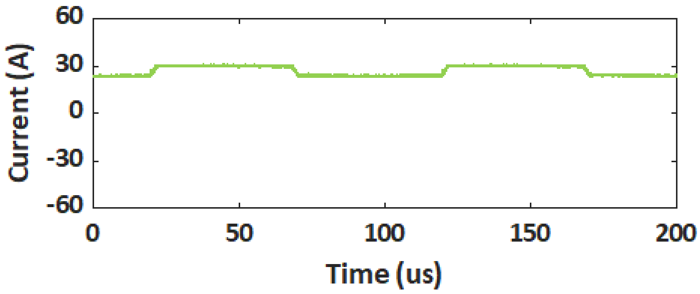
With the optimal gate signals, the cell output voltage and the phase leg output current do not change, the arm currents are controlled to change quickly during the transitions. The current resonance magnitudes largely reduce. The maximum arm current magnitude reduces to 35.5 A, which is 17% higher than the maximum magnitude of the phase leg current. The shapes of the arm currents are much closer to the ideal square wave. When the lower arm cell output voltage is zero, the lower arm current approximately equals to the reversed output current, the upper arm current is around zero, the lower arm conducts the output current while the upper arm blocks the bus voltage. When the lower arm cell output voltage is the cell capacitor voltage, the lower arm current is around zero, the upper arm current approximately equals to the output current, the lower arm blocks the bus voltage while the upper arm conducts the output current.

Comparing the results in Fig. 3-25(c) and Fig. 3-26(c), it can be observed that even without the optimal gate signals, the arm currents change quickly during the second transition. During this transition, the current commutation starts when S_{ua} and S_{lb} are turned off. However, the main device in the upper arm S_{ua} turns off with the device current having the magnitude around the phase leg output current magnitude, the auxiliary device in the lower arm S_{lb} turns off with the device current being around zero. Therefore, the switching speed of S_{lb} is much slower compared to S_{ua}, leading to an inherent delay. There is a delay between the change of the two cells output voltages even without applying delays to the gate signals for the two cells.

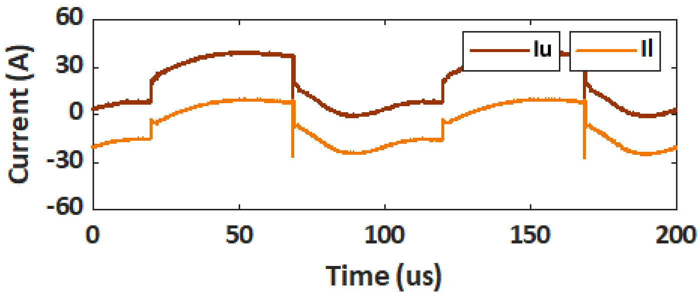
The experimental results at 6 kV dc bus voltage and 28 A dc output current with optimal gate signals are shown for two switching cycles in Fig. 3-27. The output voltage of the cell in the lower arm switches between zero and the converter dc bus voltage, 6 kV.



(a) Cell output voltage of the lower arm cell



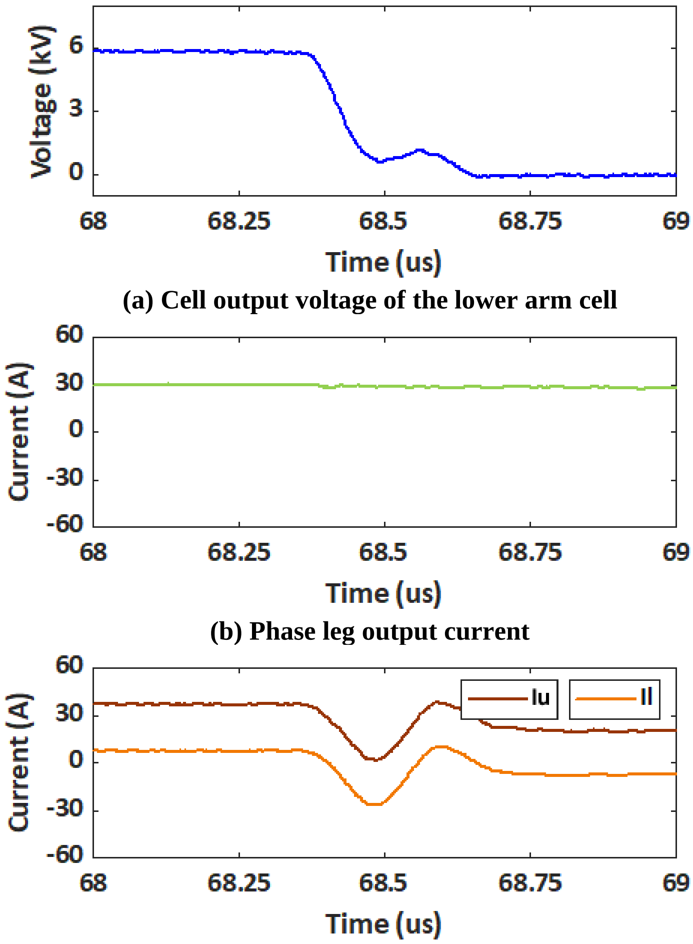
(b) Phase leg output current



(c) Arm currents

Fig. 3-27 Experimental results with one cell per arm at 6 kV, 28 A dc with optimal gate signals.

The controlled fast current changes can be observed at all switching transitions. The shapes of the arm currents are acceptable but not as good compared to the results at 1 kV. There are two reasons. The first one is that it is harder to apply the delays accurately at a higher voltage, as the required delay time is reversely proportional to the dc bus voltage, as shown in Equation (3-24). The second reason is that at higher voltage, the switching transients are longer, and there is significant resonance between the device output capacitors and the parasitic arm inductor., The zoomed-in results for the second switching transition are shown in Fig. 3-28.



(a) Cell output voltage of the lower arm cell

(b) Phase leg output current

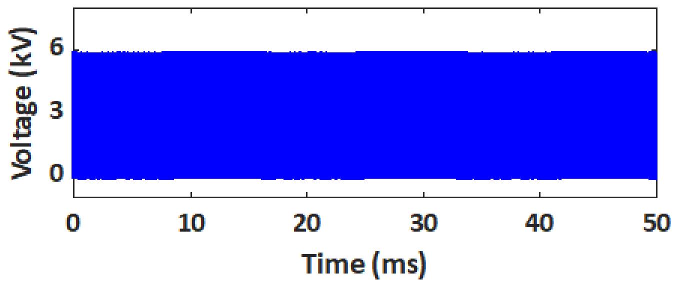
(c) Arm currents

Fig. 3-28 One switching transition with one cell per arm at 6 kV, 28 A dc.

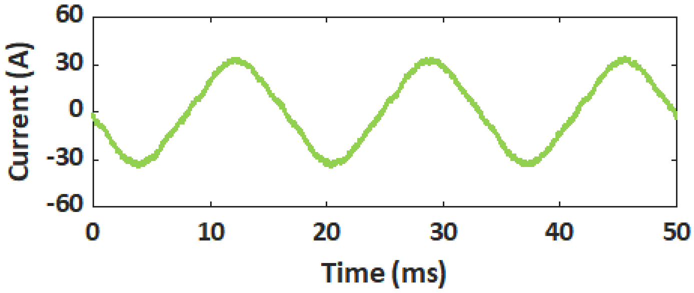
During the transition, the upper arm cell turns off, the lower arm cell turns on. S_{ua} and S_{lb} are turned off. Because the device current difference, S_{ua} turns off faster than S_{lb}. The cell output voltage in the upper arm changes faster, the rising of the cell output voltage decreases both arm currents. However, the changes in the magnitude and the polarity of the upper arm current affect the cell output voltage in the upper arm. The arm currents have uncontrolled fast changes during the transition.

The experimental results at 6 kV dc bus voltage and 22 A ac output current with optimal gate signals are shown for three line cycles in Fig. 3-29. The output line frequency is 60 Hz.

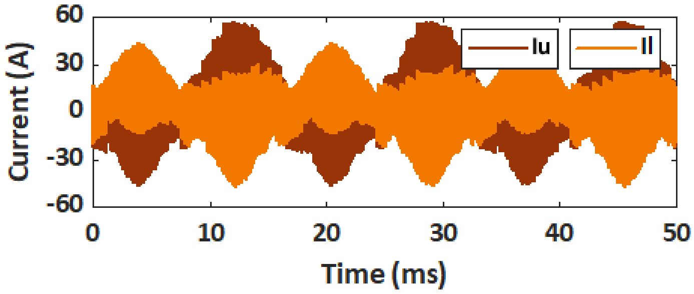
The output voltage of the cell in the lower arm switches between zero and 6 kV. The magnitudes of the arm currents roughly follow the magnitude of the phase leg output current but are higher.



(a) Cell output voltage of the lower arm cell



(b) Phase leg output current



(c) Arm currents

Fig. 3-29 Experimental results with one cell per arm at 6 kV, 22 A ac with optimal gate signals.

It is difficult to directly measure the cell capacitor voltages with probes in the setup. However, with the lower arm cell output voltage measurement, the cell capacitor voltage can be extracted by taking the cell output voltage value when the cell is off. The average value of the cell output voltage near the end of the off state is used for each switching cycle. The extracted cell capacitor voltage in the lower arm is shown for three line cycles Fig. 3-30. The peak-to-peak voltage ripple is less than 20 V. The cell capacitor voltage is in opposite phase compared to the phase leg output current, which matches Equation (3-13).

The experimental results with one cell per arm verify the operation principle analyzed in Section 3.2.1, the impact of high parasitic arm inductances analyzed in Section 3.2.4, and the mitigation with optimal gate signals analyzed in Section 3.2.5.

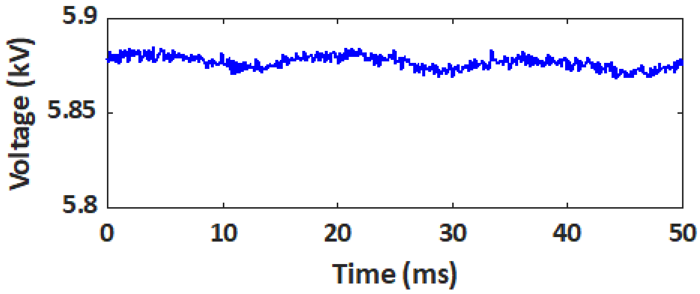


Fig. 3-30 Cell capacitor voltage in the lower arm with one cell per arm at 6 kV, 22 A ac.

3.5.4 Experimental Results with Two Cells per Arm

Four more cells are connected on top of the previous four cells to form a converter with two cells per arm. The converter setup is shown in Fig. 3-31.

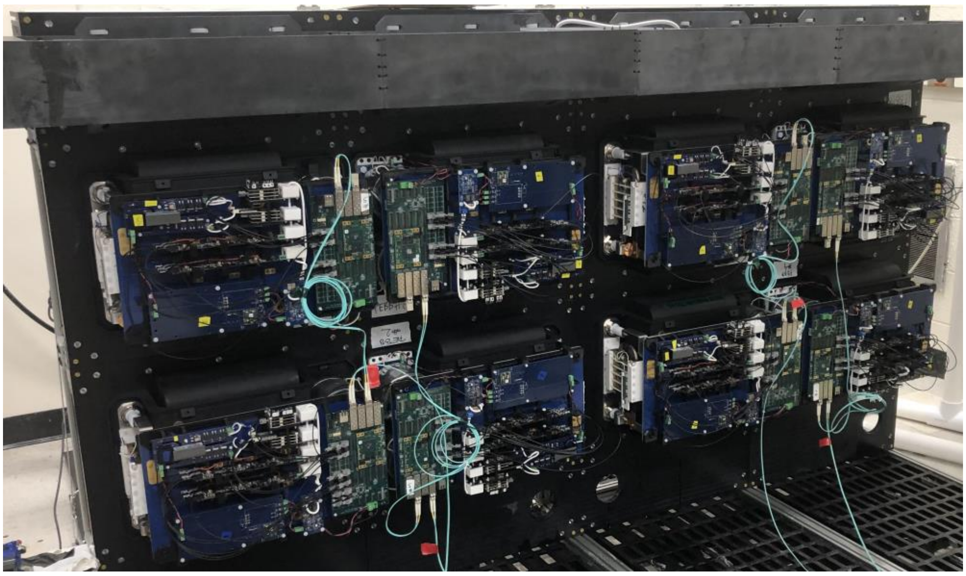


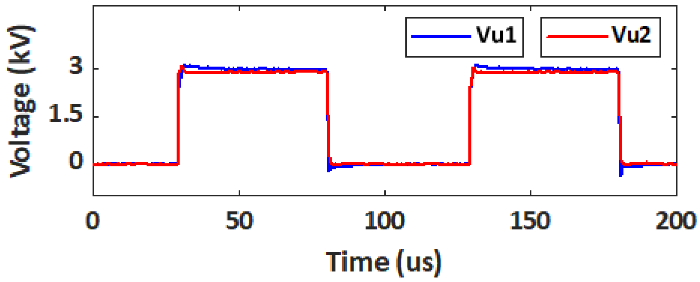
Fig. 3-31 Converter setup with two cells per arm.

Each two vertically connected cells form a converter arm. Within each arm, the cell on the top connects to the converter dc bus, the cell at the bottom connects to the phase leg output terminal.

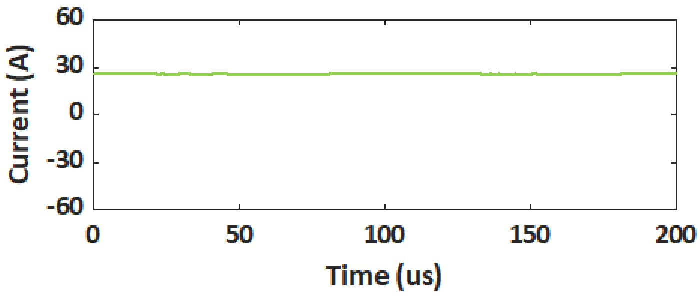
The designed converter dc bus is placed on top of the cells. The total capacitance is 2.2 μF. With this dc bus, the lengths of the cables connecting the cells to the bus are largely reduced. The parasitic arm inductances are reduced.

The converter is first tested at a lower than rated voltage to safely evaluate the cell capacitor voltage balance. The experimental results at 6 kV dc bus voltage and 25 A dc output current are shown for two switching cycles in Fig. 3-32. The phase leg output current control is implemented while the cell capacitor voltage control is not. Each two cells in the same arm are controlled to operate synchronously. There are not delays between the arms in opposite arms either.

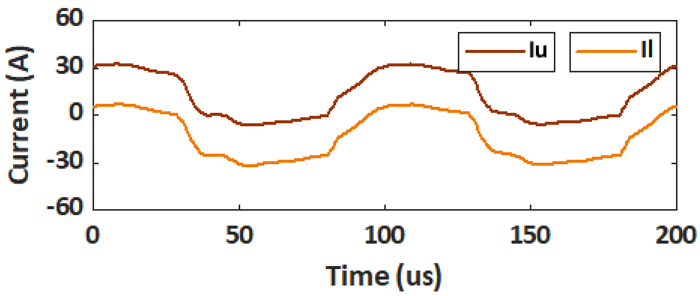
Fig. 3-32(a) shows the output voltages of the two cells in the upper arm. Each cell output voltage switches between zero and 3 kV, half of the converter dc bus voltage. Fig. 3-32(b) shows the phase leg output current with an average value of 25 A. Fig. 3-32(c) shows the two arm currents. There are no controlled fast changes during the switching transitions as no delays are applied to the cells in opposite arms. The cell output voltages and arm currents are similar compared to the results with one cell per arm. Having two cells per arm reduces the voltage stress for each cell.



(a) Cell output voltage of the upper arm cells



(b) Phase leg output current



(c) Arm currents

Fig. 3-32 Experimental results with two cells per arm at 6 kV, 25 A dc without cell capacitor voltage control.

Fig. 3-33 shows the extracted cell capacitor voltages in the upper arm for five seconds. Without the cell capacitor voltage control, the capacitor voltage difference increases by 0.11 kV after five seconds.

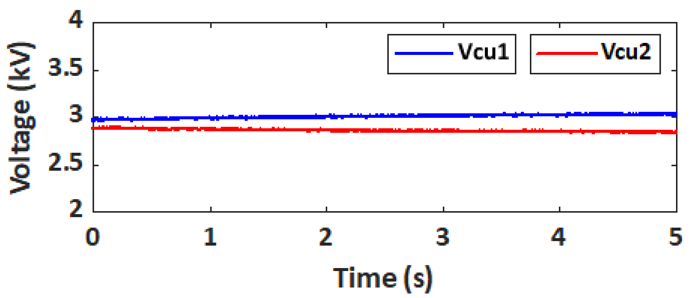
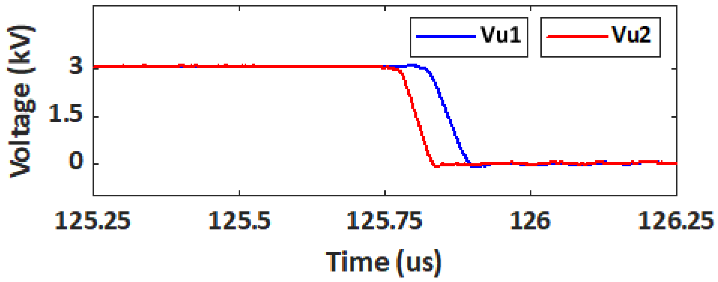


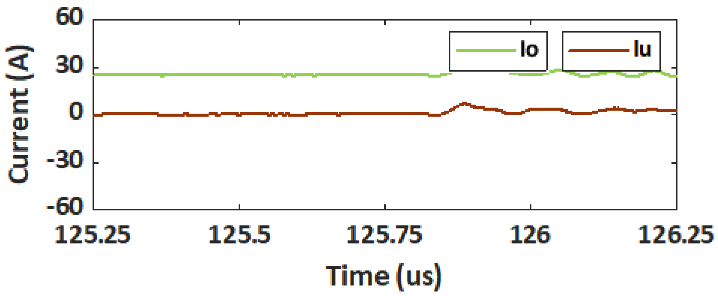
Fig. 3-33 Cell capacitor voltages in the upper arm with two cells per arm at 6 kV, 25 A dc without cell capacitor voltage control.

Then fixed delays are applied to verify their impacts on the cell capacitor voltages. All the tests are conducted at 6 kV dc bus voltage and 25 A dc output current.

Firstly, turn-on delays are applied to the first upper arm cells when the upper arm current is positive. The zoomed-in results for the switching transition are shown in Fig. 3-34.



(a) Cell output voltage of the upper arm cells



(b) Output current and upper arm current

Fig. 3-34 Turn-on transition with delays and a positive arm current in the upper arm.

During the turn-on transition of the upper arm cells, the first cell is delayed for around 50 ns compared to the second cell. During this transition, the upper arm current is around zero. Fig. 3-35 shows the extracted cell capacitor voltages in the upper arm for five seconds.

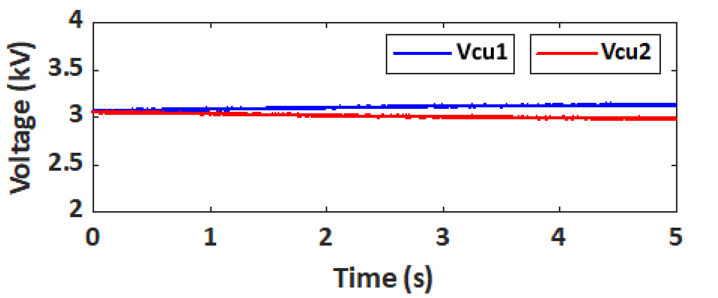
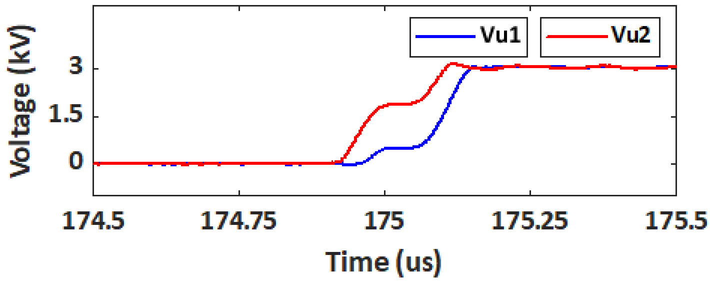


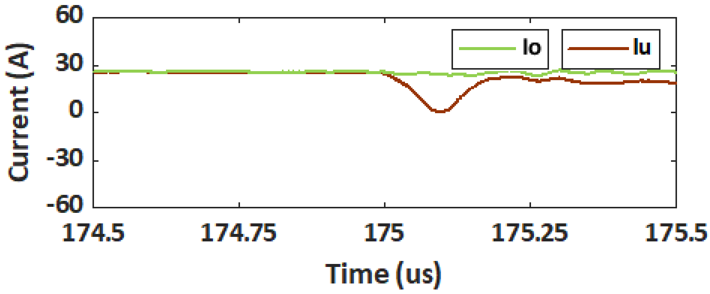
Fig. 3-35 Cell capacitor voltages in the upper arm with fixed turn-on delays and a positive arm current.

With the fixed turn-on delays, the capacitor voltage difference increases by 0.15 kV after five seconds.

Then turn-off delays are applied to the first upper arm cells when the upper arm current is positive. The zoomed-in results for the switching transition are shown in Fig. 3-36.



(a) Cell output voltage of the upper arm cells



(b) Output current and upper arm current

Fig. 3-36 Turn-off transition with delays and a positive arm current in the upper arm.

During the turn-off transition of the upper arm cells, the first cell is delayed for around 50 ns compared to the second cell. During this transition, the upper arm current is positive. Therefore, the second cell capacitor is charged more than the first cell capacitor. Fig. 3-37 shows the extracted cell capacitor voltages in the upper arm for five seconds.

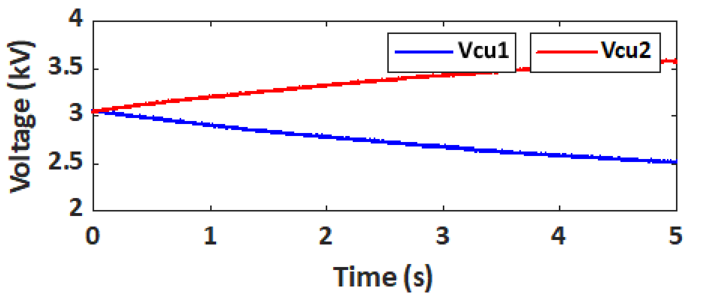
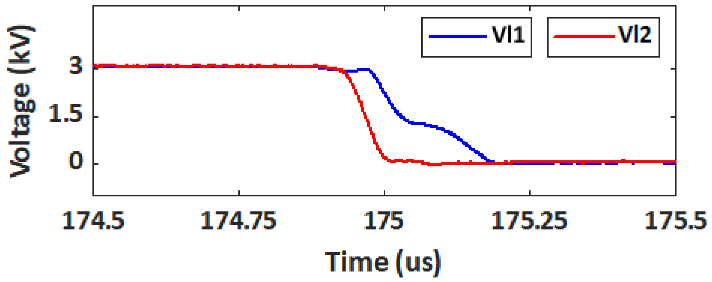


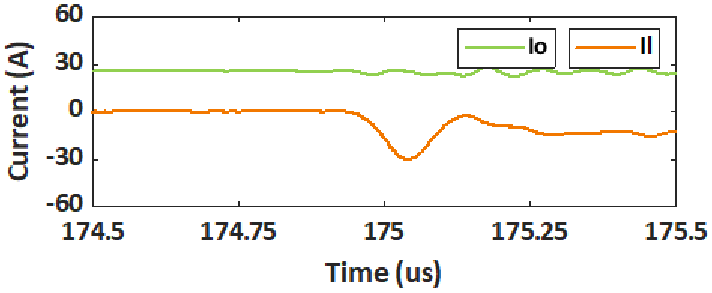
Fig. 3-37 Cell capacitor voltages in the upper arm with fixed turn-off delays and a positive arm current.

With the fixed turn-off delays, the capacitor voltage difference decreases by 1.06 kV after five seconds.

Then turn-on delays are applied to the first lower arm cells when the lower arm current is negative. The zoomed-in results for the switching transition are shown in Fig. 3-38.



(a) Cell output voltage of the upper arm cells



(b) Output current and upper arm current

Fig. 3-38 Turn-on transition with delays and a negative arm current in the lower arm.

During the turn-on transition of the lower arm cells, the first cell is delayed for around 50 ns compared to the second cell. During this transition, the lower arm current is negative. Therefore, the first cell capacitor is discharged more than the second cell capacitor. Fig. 3-39 shows the extracted cell capacitor voltages in the lower arm for five seconds.

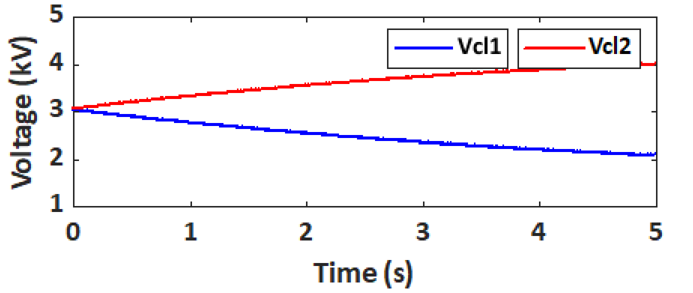
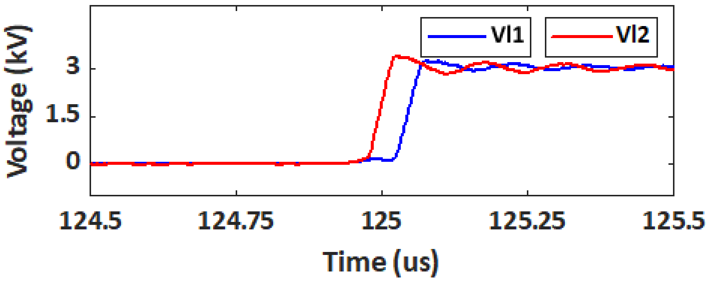


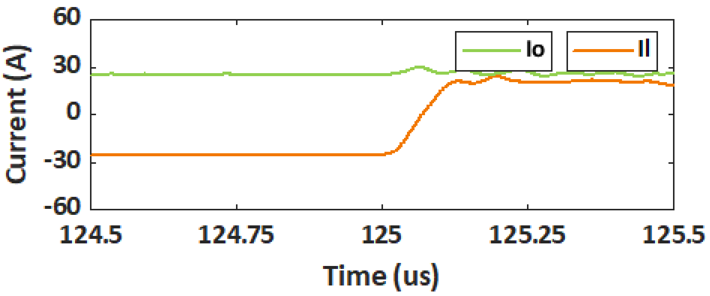
Fig. 3-39 Cell capacitor voltages in the lower arm with fixed turn-on delays and a negative arm current.

With the fixed turn-on delays, the capacitor voltage difference decreases by 1.90 kV after five seconds.

Then turn-off delays are applied to the first lower arm cells when the lower arm current is negative. The zoomed-in results for the switching transition are shown in Fig. 3-40.



(a) Cell output voltage of the upper arm cells



(b) Output current and upper arm current

Fig. 3-40 Turn-off transition with delays and a negative arm current in the lower arm.

During the turn-off transition of the lower arm cells, the first cell is delayed for around 50 ns compared to the second cell. During this transition, the lower arm current increases from a negative value to a positive value. In this particular case, the lower arm current is negative for longer duration. Therefore, the second cell capacitor is discharged more than the first cell capacitor. Fig. 3-41 shows the extracted cell capacitor voltages in the lower arm for five seconds.

With the fixed turn-on delays, the capacitor voltage difference increases by 0.87 kV after five seconds. However, the change of the voltage difference will not increase with a longer delay period.

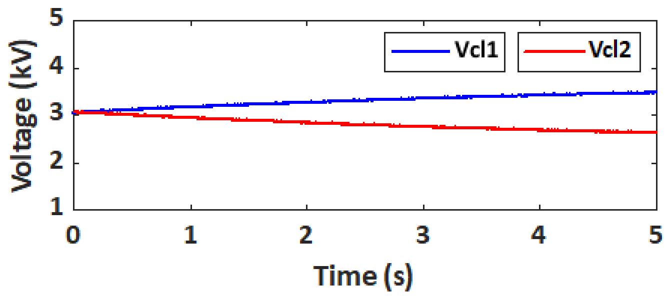
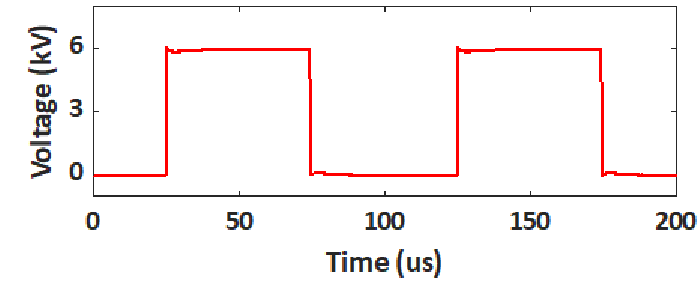


Fig. 3-41 Cell capacitor voltages in the lower arm with fixed turn-off delays and a negative arm current.

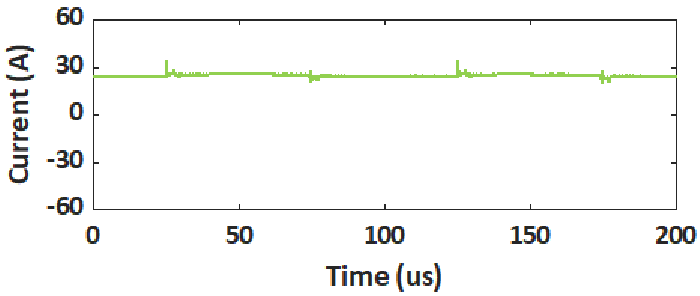
After verifying the impact of gate signals delays on the cell capacitor voltages, the closed-loop cell capacitor voltage control is implemented. The average cell capacitor voltage of each arm is used as the reference for the cell capacitor voltage control. For each cell, the difference between the cell capacitor voltage and the reference voltage is the input for a PI regulator to calculate the desired delay value. Then at each arm, the smaller value of the two cells is subtracted from the two delay values of the two cells. Therefore, one cell has delayed gate signals while the signals for the other cell do not have delays. The upper arm cells and lower arm cells are allowed to apply delay alternatively and it changes every ten switching cycles. Finally, the delays are applied to either the turn-on commands or turn-off commands depending on the phase leg output current polarity and the cell location.

The experimental results at 12 kV dc bus voltage and 25 A dc output current with cell capacitor voltage control are shown for two switching cycles in Fig. 3-42. Fig. 3-42(a) shows the output voltage of the second lower arm cell. It switches between zero and 6 kV, half of the converter dc bus voltage. The cell output voltages and arm currents are similar compared to the results with one cell per arm. Having two cells per arm enables the converter to double the voltage rating and operate with a 12 kV dc bus.

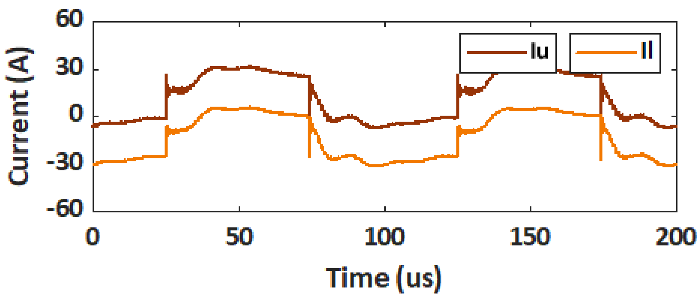
Because of insulation concerns, the output voltages of the other cells are not measured. All the cell capacitor voltages are measured by the voltage sensors in the cells, summarized in the main controller, sent to the computer, displayed on the user interface, and saved through the user interface. The four cell capacitors in the phase leg measured by the voltage sensors are shown in Fig. 3-43. The maximum voltage ripple at a cell capacitor is around 5 V, which is 0.08 % of the rated voltage. The maximum instant voltage difference between two cell capacitors in the same arm is around 3 V, which is 0.05 % of the rated voltage.



(a) Cell output voltage of the second lower arm cell

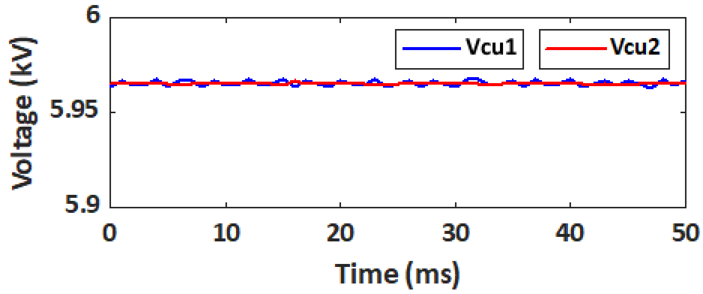


(b) Phase leg output current

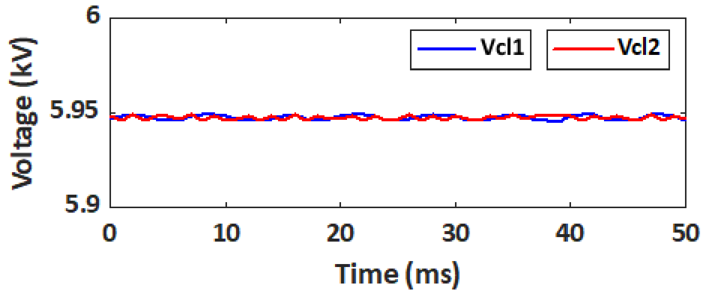


(c) Arm currents

Fig. 3-42 Experimental results with two cells per arm at 12 kV, 25 A dc with cell capacitor voltage control.



(a) Capacitor voltages in the upper arm

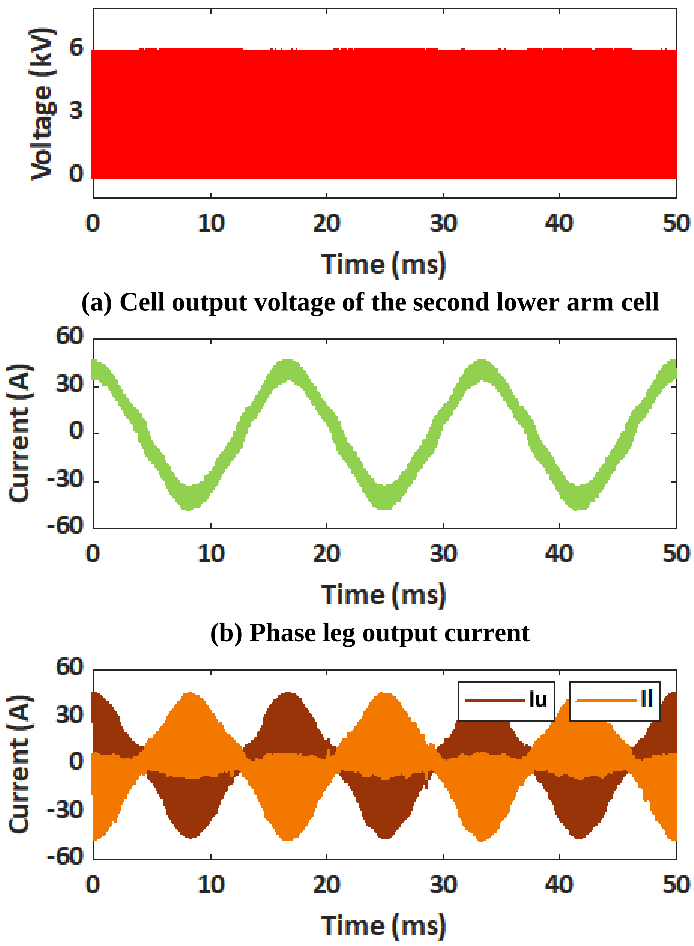


(b) Capacitor voltages in the lower arm

Fig. 3-43 Cell capacitor voltages measured by sensors with two cell per arm at 12 kV, 25 A dc with cell capacitor voltage control.

The experimental results at 12 kV dc bus voltage and 25 A ac output current with cell capacitor voltage control are shown for three line cycles in Fig. 3-44. The output voltage of the second cell in the lower arm switches between zero and 6 kV. The magnitudes of the arm currents approximately follow the magnitude of the phase leg output current.

The four cell capacitors in the phase leg measured by the voltage sensors are shown in Fig. 3-45. The upper arm cell capacitor voltages are in phase compared to the phase leg output current, the lower arm cell capacitor voltages are in opposite phase compared to the phase leg output current. The maximum voltage ripple at a cell capacitor is around 16 V, which is 0.27 % of the rated voltage. The maximum instant voltage difference between two cell capacitors in the same arm is around 6 V, which is 0.10 % of the rated voltage.



(a) Cell output voltage of the second lower arm cell

(b) Phase leg output current

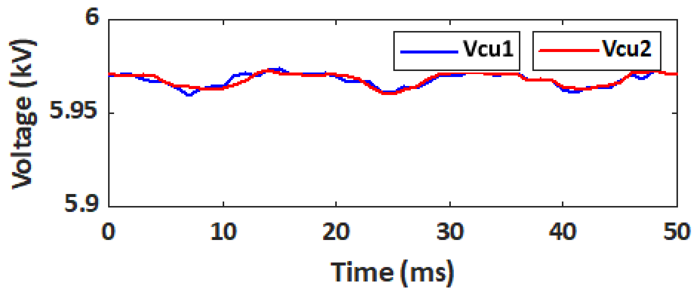
(c) Arm currents

Fig. 3-44 Experimental results with two cells per arm at 12 kV, 25 A ac with cell capacitor voltage control.

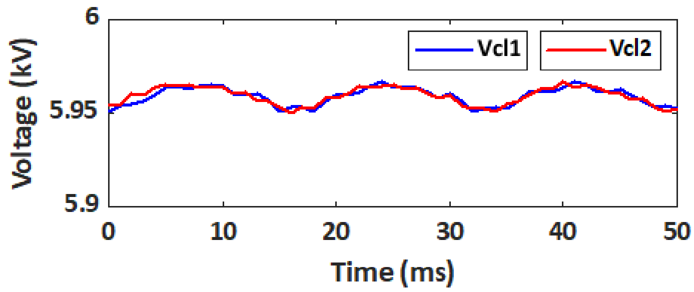
The experimental results with two cell per arm verify the impact of gate signal delays on the cell capacitor voltages analyzed in Section 3.3.2, and the effectiveness of the cell capacitor voltage control proposed in Section 3.4.2.

3.5.5 Experimental Results with Three Cells per Arm

Four more cells are connected on top of the previous eight cells to form a converter with three cells per arm. The converter setup is shown in Fig. 3-46.



(a) Capacitor voltages in the upper arm



(b) Capacitor voltages in the lower arm

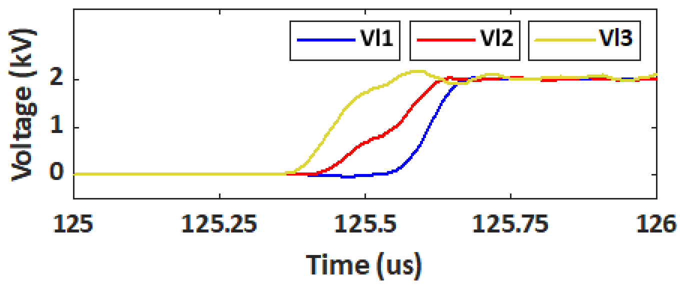
Fig. 3-45 Cell capacitor voltages measured by sensors with two cell per arm at 12 kV, 25 A ac with cell capacitor voltage control.

Fig. 3-46 Converter setup with three cells per arm.

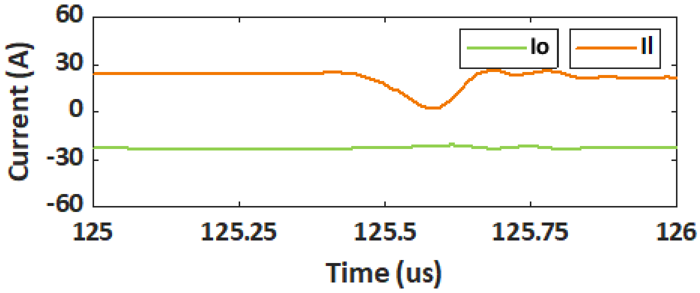
Each three vertically connected cells form a converter arm. Within each arm, the cell on the top connects to the converter dc bus, the cell at the bottom connects to the phase leg output terminal.

Similar with when having two cells per arm, fixed delays are applied to verify their impacts on the cell capacitor voltages. All the tests are conducted with the dc bus voltage being 6 kV and the magnitude of the output current being 25 A. Only the results of the two types of delays which are used in the closed-loop cell capacitor voltage control are shown.

Firstly, turn-off delays are applied in the lower arm when the lower arm current is positive. The zoomed-in results for the switching transition are shown in Fig. 3-47.



(a) Cell output voltage of the upper arm cells



(b) Output current and upper arm current

Fig. 3-47 Turn-off transition with delays and a positive arm current in the lower arm.

During the turn-off transition of the lower arm cells, the first cell is delayed for around 100 ns, the second cell is delayed for around 50 ns, both compared to the third cell. During this transition, the lower arm current is positive. Therefore, the third cell capacitor is charged the most, the first cell capacitor is charged the least. Fig. 3-48 shows the extracted cell capacitor voltages in the lower arm for five seconds.

With the fixed turn-off delays, the first cell capacitor voltage decreases by 0.76 kV, the third cell capacitor voltage increases by 0.75 kV.

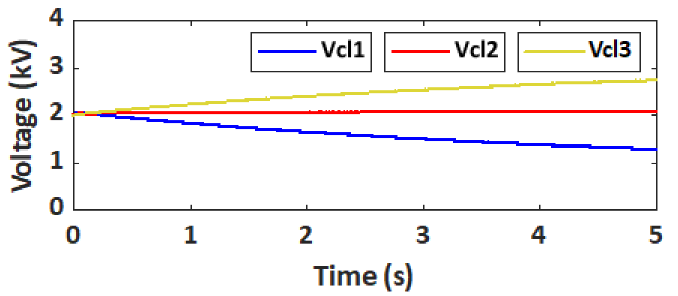
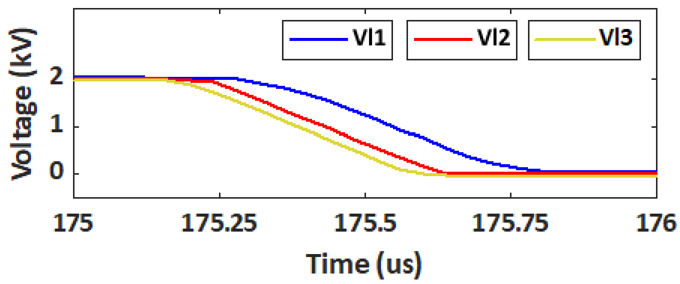
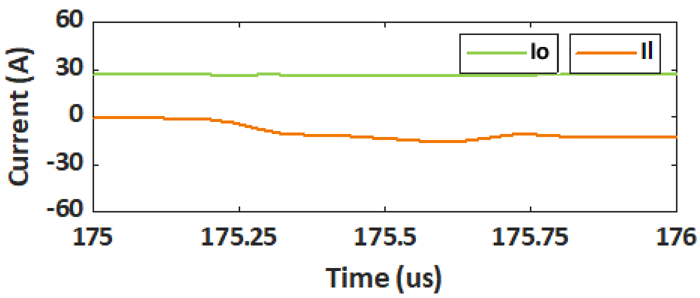


Fig. 3-48 Cell capacitor voltages in the lower arm with fixed turn-off delays and a positive arm current.

Then turn-on delays are applied in the lower arm when the lower arm current is negative. The zoomed-in results for the switching transition are shown in Fig. 3-49.



(a) Cell output voltage of the upper arm cells



(b) Output current and upper arm current

Fig. 3-49 Turn-on transition with delays and a negative arm current in the lower arm.

During the turn-on transition of the lower arm cells, the first cell is delayed for around 100 ns, the second cell is delayed for around 50 ns, both compared to the third cell. During this transition, the lower arm current is negative. Therefore, the first cell capacitor is discharged the most, the third cell capacitor is discharged the least. Fig. 3-50 shows the extracted cell capacitor voltages in the lower arm for five seconds.

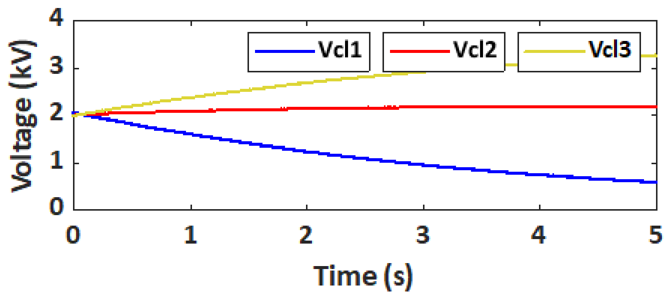


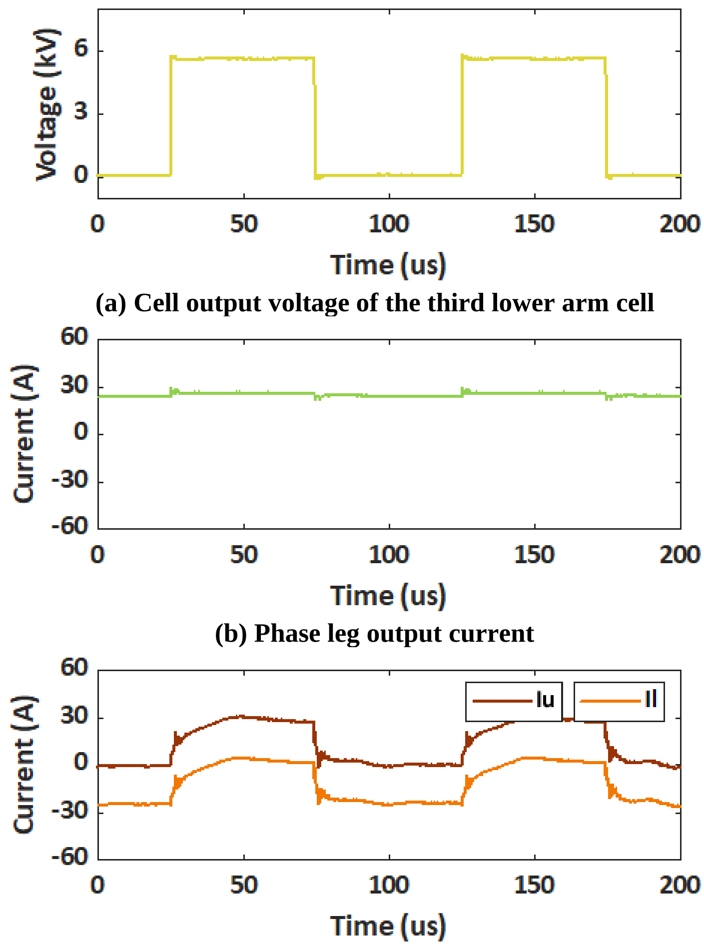
Fig. 3-50 Cell capacitor voltages in the lower arm with fixed turn-on delays and a negative arm current.

With the fixed turn-on delays, the first cell capacitor voltage decreases by 1.45 kV, the third cell capacitor voltage increases by 1.28 kV.

After verifying the impact of gate signals delays on the cell capacitor voltages, the cell capacitor voltage control is implemented in the same way. The average cell capacitor voltage of each arm is used as the reference for the cell capacitor voltage control. For each cell, a PI regulator calculates the desired delay value. The smallest value of the three delay values in each arm is subtracted from the three delay values to remove the delays in one cell while the other two cells may have delays.

The experimental results at 16.5 kV dc bus voltage and 25 A dc output current with cell capacitor voltage control are shown for two switching cycles in Fig. 3-51. Fig. 3-51(a) shows the output voltage of the third lower arm cell. It switches between zero and 5.5 kV, one third of the converter dc bus voltage. The cell output voltages and arm currents are similar compared to the results with one cell per arm and the results with two cells per arm. Having three cells per arm enables the converter to further increase the voltage rating.

The six cell capacitors in the phase leg measured by the voltage sensors are shown in Fig. 3-52. The maximum voltage ripple at a cell capacitor is around 2 V, which is 0.04 % of the rated voltage. The maximum instant voltage difference between two cell capacitors in the same arm is around 1.5 V, which is 0.03 % of the rated voltage.



(a) Cell output voltage of the third lower arm cell

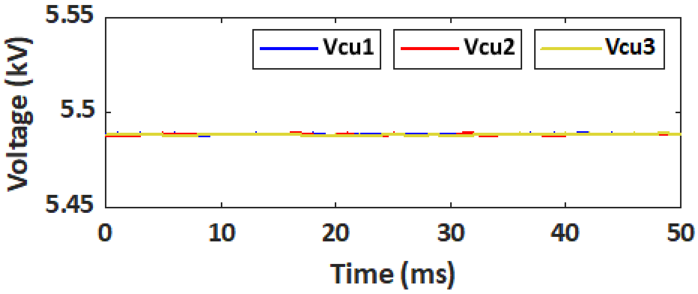
(b) Phase leg output current

(c) Arm currents

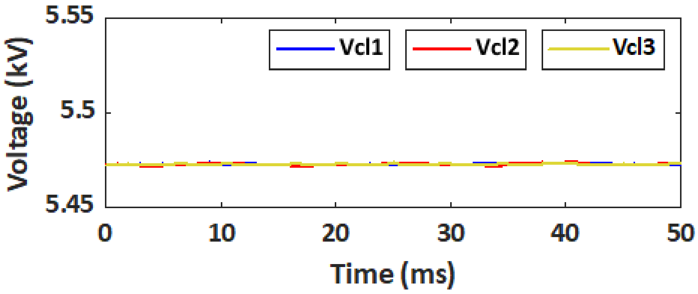
Fig. 3-51 Experimental results with three cells per arm at 16.5 kV, 25 A dc.

The experimental results at 12 kV dc bus voltage and 25 A ac output current with cell capacitor voltage control are shown for three line cycles in Fig. 3-53.

The output voltage of the third cell in the lower arm switches between zero and 5.5 kV. The magnitudes of the arm currents approximately follow the magnitude of the phase leg output current.

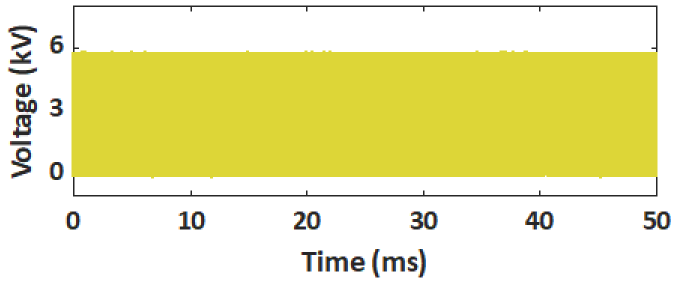


(a) Capacitor voltages in the upper arm

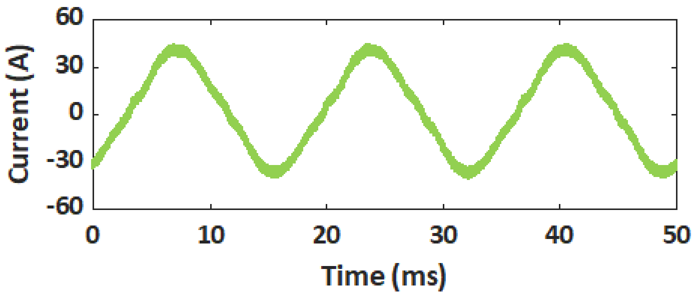


(b) Capacitor voltages in the lower arm

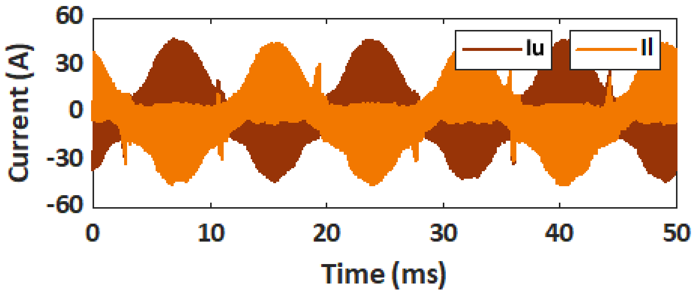
Fig. 3-52 Cell capacitor voltages measured by sensors with three cell per arm at 16.5 kV, 25 A dc.



(a) Cell output voltage of the third lower arm cell



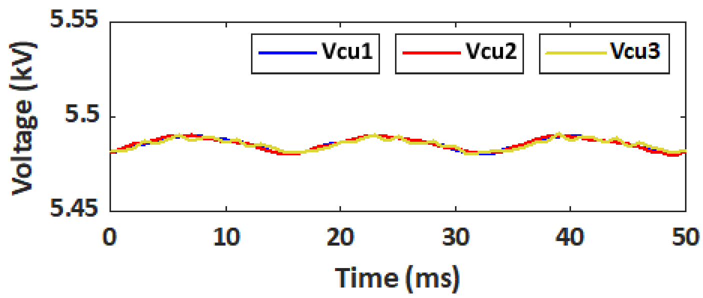
(b) Phase leg output current



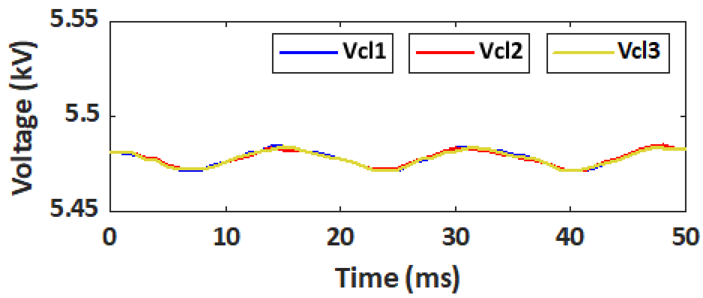
(c) Arm currents

Fig. 3-53 Experimental results with three cells per arm at 16.5 kV, 25 A ac.

The six cell capacitors in the phase leg measured by the voltage sensors are shown in Fig. 3-54. The upper arm cell capacitor voltages are in phase compared to the phase leg output current, the lower arm cell capacitor voltages are in opposite phase compared to the phase leg output current. The maximum voltage ripple at a cell capacitor is around 14 V, which is 0.23 % of the rated voltage. The maximum instant voltage difference between two cell capacitors in the same arm is around 3 V, which is 0.05 % of the rated voltage.



(a) Capacitor voltages in the upper arm

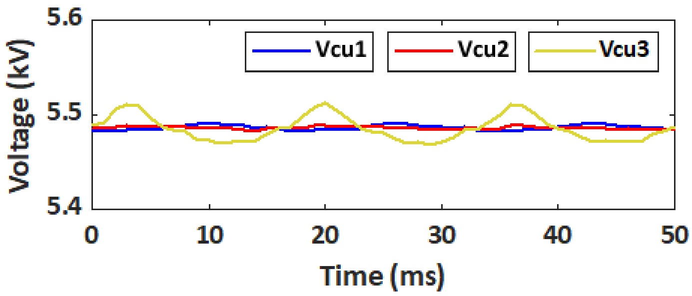


(b) Capacitor voltages in the lower arm

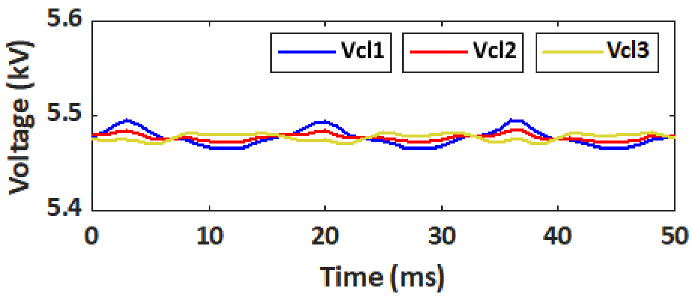
Fig. 3-54 Cell capacitor voltages measured by sensors with three cell per arm at 16.5 kV, 25 A ac.

Although the results shown in Fig. 3-29, Fig. 3-30, Fig. 3-44, Fig. 3-45, Fig. 3-53, Fig. 3-54 are with an ac output current, the output voltage of each phase leg is always around half of the dc bus voltage. A more realistic case is that the phase leg output voltage includes a significant ac component. The largely varying duty ratios of the cells affect both the operation of the ICBT cells and the effectiveness of the cell capacitor voltage control.

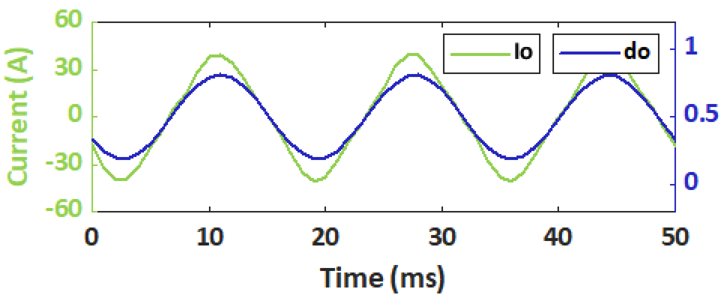
The six cell capacitors in the phase leg, the output current and output duty ratio with a 0.8 modulation index and different power factors are shown in Fig. 3-55 - Fig. 3-58. Although the cell capacitor voltages change with the power factor, the maximum voltage ripple at a cell capacitor is around 61 V, which is 1.22 % of the rated voltage; the maximum instant voltage difference between two cell capacitors in the same arm is around 33 V, which is 0.66 % of the rated voltage.



(a) Capacitor voltages in the upper arm



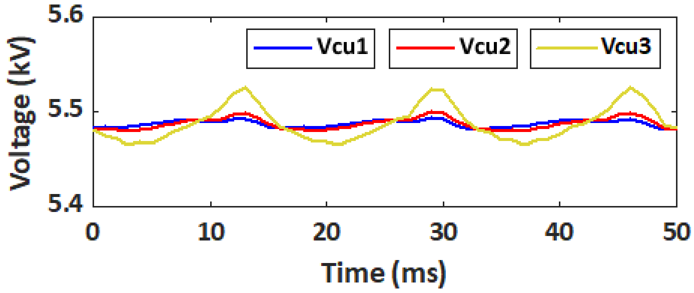
(b) Capacitor voltages in the lower arm



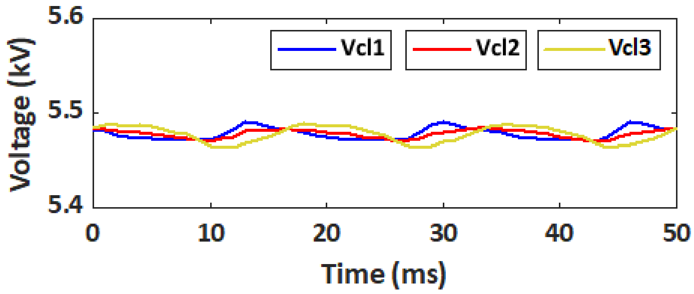
(c) Phase leg output current and output duty ratio

Fig. 3-55 Experiment results with three cell per arm at 16.5 kV, 25 A ac, $\theta = 0°$.

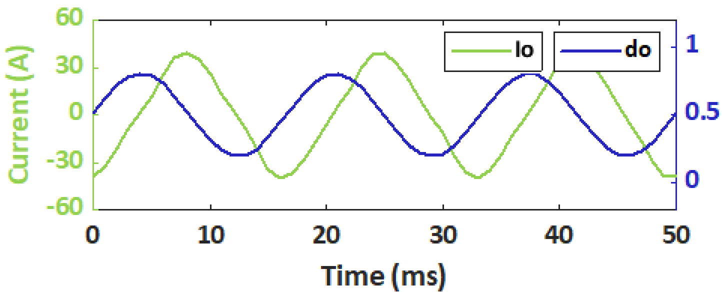
The experimental results with three cell per arm verify the impact of gate signal delays on the cell capacitor voltages analyzed in Section 3.3.2, and the effectiveness of the cell capacitor voltage control proposed in Section 3.4.2. Both are valid regardless of the number of cells per arm.



(a) Capacitor voltages in the upper arm

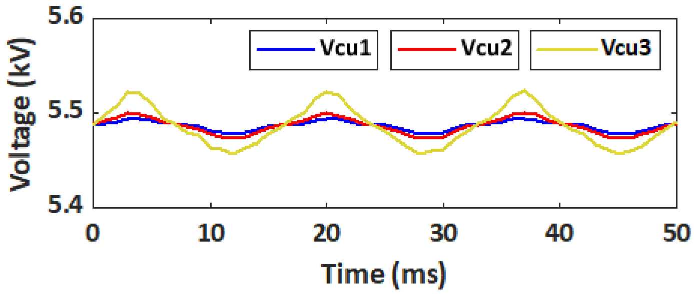


(b) Capacitor voltages in the lower arm

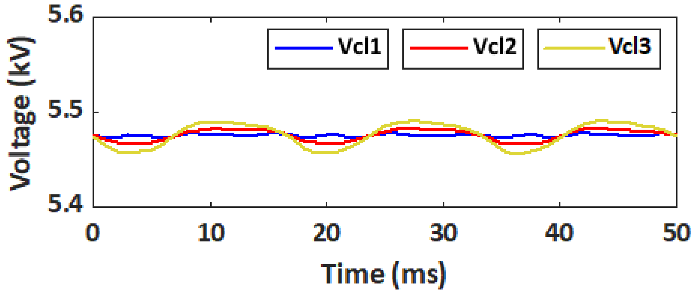


(c) Phase leg output current and output duty ratio

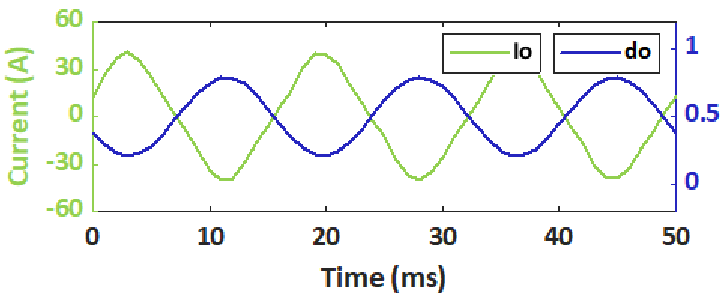
Fig. 3-56 Experiment results with three cell per arm at 16.5 kV, 25 A ac, $\theta = 90°$.



(a) Capacitor voltages in the upper arm

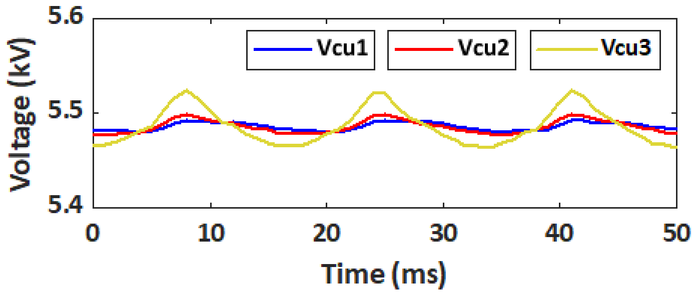


(b) Capacitor voltages in the lower arm

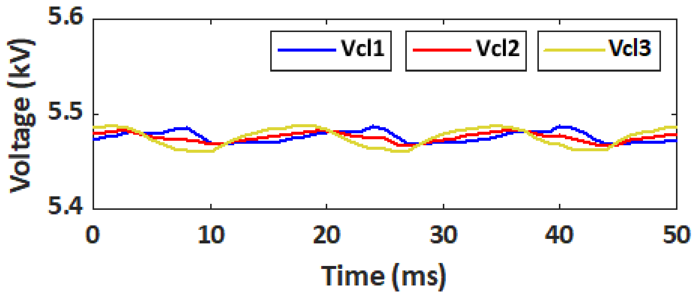


(c) Phase leg output current and output duty ratio

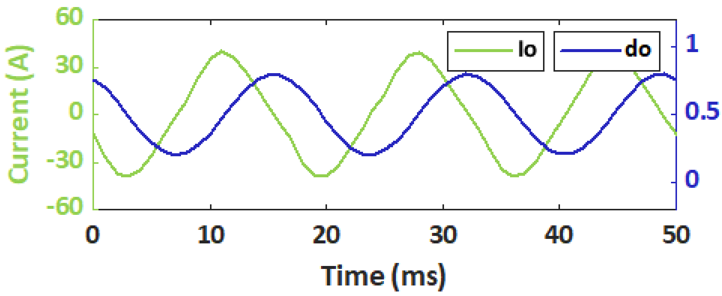
Fig. 3-57 Experiment results with three cell per arm at 16.5 kV, 25 A ac, $\theta = 180°$.



(a) Capacitor voltages in the upper arm



(b) Capacitor voltages in the lower arm



(c) Phase leg output current and output duty ratio

Fig. 3-58 Experiment results with three cell per arm at 16.5 kV, 25 A ac, $\theta = 270°$.

3.6 Summary

The operation principle of ICBT cells and ICBT-based phase legs is analyzed. ICBT-based converters have the structure similar as MMCs, but the operation similar as series-connected switching devices.

Compared to MMCs, ICBT-based converters retain the advantages of devices blocking cell capacitor voltages instead of directly sharing the whole converter dc bus voltage, modularity, and scalability. ICBT cells enable direct power transfer, therefore avoid the issue of large cell capacitor voltage ripples. Without the line frequency dependency on the cell capacitor voltage ripples, ICBT-based converters can operate in both ac and dc operation modes. As no arm inductors are required, the size and loss of the arm inductors are eliminated.

Compared to series-connected switching devices, ICBT-based converters retain the advantage of simple control principle. The cells in the same arm are controlled to operate synchronously, the cells in opposite arms are controlled to operate complimentarily. In this way, an ICBT cell operates as a single switching device, series-connected ICBT cells operate as an equivalently high-voltage device. ICBT-based converters avoid the issue of large and fast-developing voltage unbalance. The voltage unbalance changes much slower and is much easier to control.

Low parasitic inductance in the arm is key to achieve ideal ICBT operation. If the inductance value is not low enough, it will lead to significant current oscillation in the arms, increasing semiconductor losses and cell capacitor voltage offsets. It is more critical with a high switching frequency of SiC MOSFETs. The magnitude of the resonance can be reduced by optimal gate signals that have delays between the signals for the cells in different arms. However, it is preferred to have low parasitic arm inductances other than using the optimal gate signals to have easy control implementation.

The existence of parasitic capacitors is one of the reasons that could affect the capacitor voltage balance. Small currents charge or discharge the parasitic capacitors during the switching transients, causing the cells in the same arm to have different behaviors. The impacts are more significant with the high switching speeds of SiC MOSFETs. The impacts of parasitic capacitors on cell capacitor voltages depend on the load current polarity, switching transition type, and the cell location. Compared to series-connected switches, the voltage unbalance develops much slower among series-connected ICBT cells. The impact of parasitic capacitors can be theoretically eliminated if the heatsinks are not grounded but instead connected to a local reference point in the corresponding cell.

The difference among gate signals is another reason that could affect the capacitor voltage balance. With slightly different gate signals the cells in the same arm may switch at different instants, have different cell capacitor currents and therefore different capacitor voltage. The impacts are more significant with the high switching speeds of SiC MOSFETs. The impacts of the delays on cell capacitor voltages depend on the switching transition type and the arm current polarity. To mitigate the impacts, highly accurate control is required.

Based on the impacts of gate signals delays on cell capacitor voltages, a capacitor voltage control method is proposed to adjust capacitor voltage difference by applying delays to some of the cells. When the arm current is positive, turn-off delays should be applied to the cell with a higher cell capacitor voltage; when the arm current is positive, turn-off delays should be applied to the cell with a higher cell capacitor voltage. A converter level control controls the converter outputs. The proposed converter control method is easy to implement and scalable with different number of cells in the arm.

A modular Medium Voltage converter is used as the test bed for the ICBT operation and control. The converter has identical power cells, which are built with 10 kV, 40 A XHV9 SiC MOSFET modules from Wolfspeed. The converter has two phase legs, which are built by connecting multiple power cells together. With the high voltage SiC MOSFETs, each cell has a higher voltage rating. Less number of cells are required to achieve the same converter voltage rating, and the control can be simpler.

The pump-back test is conducted for both the cells and the phase legs to verify the performance at the rated voltage and current during the continuous operation, without the need for high power source or load. A state machine is defined for the converter, to ensure the safe operation and correct functions of the converter.

The ICBT-based converter is tested with one cell per arm first, then with increasing number of cells. The experimental results with one cell per arm verify the operation principle, the impact of high parasitic arm inductances, and the mitigation with optimal gate signals. The experimental results with two cell per arm and three cells per arm verify the impact of gate signal delays on the cell capacitor voltages, and the effectiveness of the cell capacitor voltage control. With the cell capacitor voltage control, 50% duty ratio and difference number of cells in arm, the maximum cell capacitor voltage ripple at a cell capacitor and the maximum instant voltage difference within an arm are both less than 5 V in the dc operation mode; the maximum cell capacitor voltage ripple at a cell capacitor voltage is less than 20 V, the maximum instant voltage difference within an arm is less than 3 V in the ac operation mode. With three cells per arm and a 0.8 modulation index, the maximum cell capacitor voltage ripple at a cell capacitor voltage is 61 V, the maximum instant voltage difference within an arm is 33 V in the ac operation mode.

Chapter 4. Evaluation and Mitigation of Electromagnetic Interference

In this chapter, the conducted EMI disturbance is evaluated and mitigated in four SiC-based multilevel converters.

4.1 Introduction

EMI is an unintended transfer of electromagnetic energy, which may interfere, corrupt, or damage the operation of the receiving circuit. There are three key elements in this type of energy transfer: the noise source, the noise victim, and the coupling between them [175], [176].

In power electronics converters, the *dv/dt* and *di/dt* at the switching device during the switching transients are the major EMI noise sources [177], [178]. The higher switching speed, higher switching frequency operation, and higher voltage and current ringing of SiC MOSFETs all contribute to increased noise generation from the EMI source [179]. It has been experimentally proved that the EMI noise in SiC-based converters is higher compared with Si-based converters [67], [69], [180]-[182]. As the noise generation from the source is tightly tied to the switching actions, it can be reduced by altering the switching behaviors or patterns of devices. However, that may lead to a tradeoff between the EMI emission and the converter performance, such as the efficiency [68], [180].

Based on how the noise is propagated, the EMI disturbance can be categorized into the conducted EMI and the radiated EMI [183]. In this work only the conducted EMI is studied, which generally ranges from hundreds of kilohertz to tens of megahertz [179]. Altering the impedance of the coupling path, for example by inserting EMI filters, is an effective way to attenuate the EMI disturbance [183]-[185].

Achieving Electromagnetic Compatibility (EMC) is one of the biggest challenges in SiC-based power electronic converters. All components inside the converter must be able to operate without being affected by the noise generated by the converter. At the same time, the EMI emission from the converter must be low enough so that they do not affect the operation of other parts that connect to the converter. There are multiple standards that specify the noise limits from agencies such as the FCC and the CISPR.

Four cases are studied in this chapter. Section 4.2 studies the EMI disturbance at the power input port in a three-level Uninterrupted Power Supply system. Section 4.3 studies the EMI disturbance in the control system in a Modular Multilevel Converter. Section 4.4 studies the EMI disturbance in the auxiliary system in a Modular MV converter. Section 4.5 studies the EMI disturbance in the auxiliary system in a five-level Stacked Multicell Converter. All four converters have SiC MOSFETs as the switching devices. In each case, the conducted EMI disturbance is experimentally evaluated and mitigated.

4.2 EMI Evaluation and Filter Design of a SiC-Based Three-Level Uninterrupted Power Supply

Uninterruptible Power Supply (UPS) systems are power supplies with built-in energy storage systems and are capable of always providing high quality power to critical loads even when the mains input power encounters outage or anomalies. As the UPS systems serve power to critical loads, they must have low EMI emission so that they will not affect the operation of other parts connected to the UPS systems. The International Standard IEC 62040-2 [186] specifies the EMC requirements for UPS systems and is used as the guideline for the evaluation and mitigation in this study.

Like other MV systems, UPS systems can benefit from the use of SiC MOSFETs to achieve higher efficiency and higher power density [60], [61], [187]-[190]. However, the increased EMI emissions must be addressed. In addition, a UPS system may consist of multiple power converter stages, complicating the noise generation and propagation.

4.2.1 UPS System under Study

Online UPS, offline UPS and line-interactive UPS are three main configurations of power electronics UPS systems [191]. The online UPS system [192]-[194] has an inverter stage to always connect to the load regardless of the availability of the mains input power. The dc bus is supported by the rectifier stage if the mains input is available or by the battery if the mains input fails. As the magnitude and frequency of the inverter stage output voltage are independent from those of the rectifier stage input voltage, the online UPS systems are capable of always providing high quality output while experiencing any kind of power line disturbance [191]. The UPS system under evaluation in this study has such an online UPS configuration.

The key specifications of the system are shown in Tab. 4-1. The circuit diagram of the system is shown in Fig. 4-1. The system includes a rectifier stage, an inverter stage, and a bi-directional dc-dc stage. The dc-dc stage connects the dc bus and the battery, charging or discharging the battery. Compared to the traditional online UPS systems with only two back-to-back stages, using the dc-dc stage eliminates the need of line frequency transformers, therefore improves the efficiency and reduces the size and weight [195], [196].

Tab. 4-1 Specification of the UPS system under evaluation.

Parameter	Value
Apparent Power	20 kVA
Mains Line RMS Voltage	480 V
Load Line RMS Voltage	480 V
DC Bus Voltage	800 V
Line Frequency	60 Hz
Switching Frequency	60 kHz

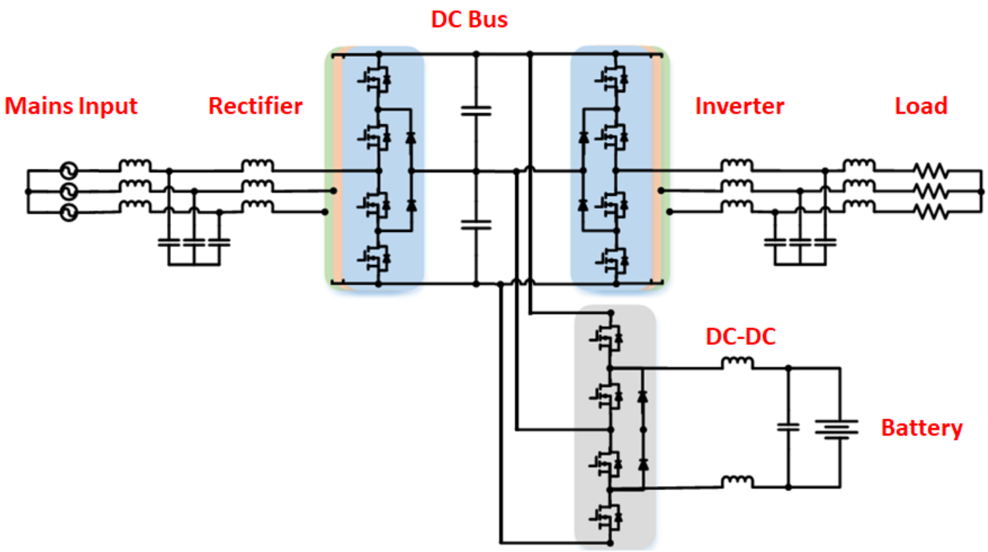


Fig. 4-1 Circuit diagram of the UPS system under evaluation.

The three-level Neutral Point Clamped converter is the topology of both the rectifier stage and the inverter stage. It is shown to have lower losses compared to the two-level converter [188]. It also has lower EMI noise generation compared to the two-level converter. LCL filters are placed before the rectifier stage and after the inverter stage to attenuate the harmonics in input and output currents. The three-level Buck converter is the topology of the dc-dc stage. Compared to the traditional two-level Buck converter, it largely reduces EMI noise generation and facilitates the use of the same three-level SiC MOSFET module [197] for all the three power conversion stages.

A small external gate resistor of 0.05 Ω is used for each gate driving channel to minimize the switching losses. The measured maximum *dv/dt* is 26.4 V/ns and the maximum *di/dt* is 4.14 A/ns [198]. The UPS system including the three conversion stages is shown in Fig. 4-2. The design and construction of the converter are the results of teamwork. The converter design details and experimental results are shown in [198], [199].

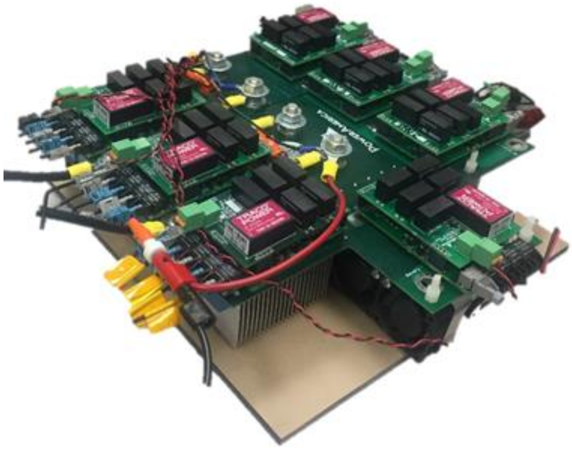


Fig. 4-2 The SiC-based UPS system under evaluation.

4.2.2 EMI Test Environment

Following the specifications in IEC 62040-2, an EMI test environment is established for the conducted EMI emission measurement to minimize the impact of external components on the measurement. The test environment is shown in Fig. 4-3. A 1.8 m × 2.4 m copper plane is used as the ground plane. The UPS system under test is placed on the copper plane with 0.5 m distance to the closest boundary. The ac input power port and the ac output power port are on the opposite sides of the copper plane, connecting to the three-phase ac power supply and to the three-phase resistive loads respectively. To emulate the battery-rack, a load bank with multiple resistors is used and is placed on the copper plane. Three line-impedance-stabilization-network (LISN) units [200] are placed on the copper plane with 0.8 m distance to the UPS system. The LISNs are located at the ac input power port to measure the disturbance voltages of the mains input terminal. The limits of category C3 UPS in the IEC 62040-2 standard are used and are applied to the ac mains input port.

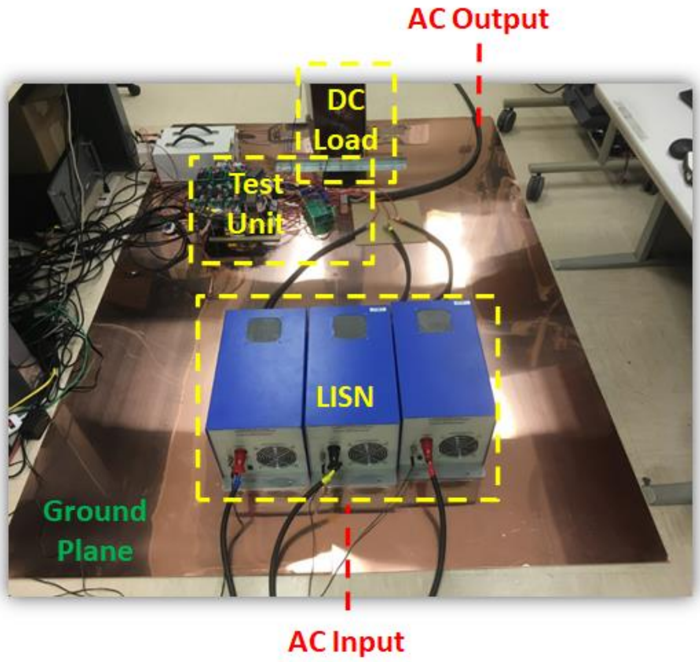


Fig. 4-3 Conducted EMI emission test environment.

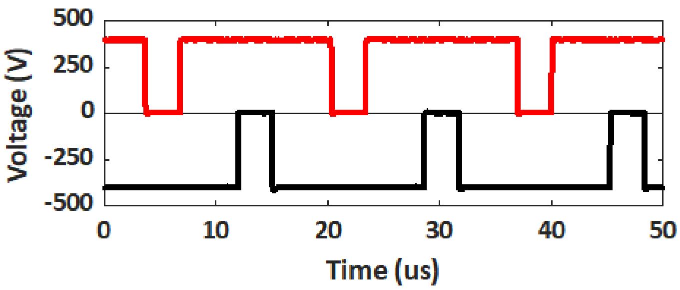
4.2.3 Impact of Modulation Methods

Selective modulation methods can be adopted to reduce the common mode (CM) voltage generation from the power conversion stages.

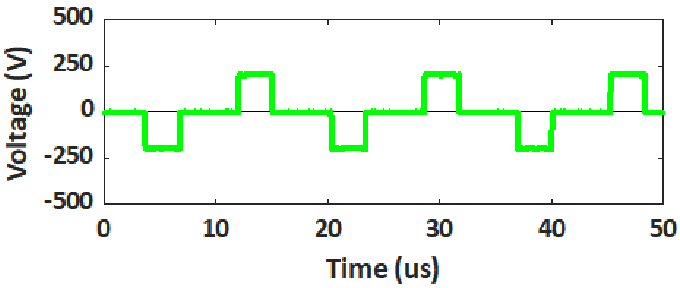
For the three-level dc-dc stage, the CM voltage is defined as the average voltage of the positive and negative output voltages, with the reference to the middle point of the converter dc bus.

$$V_{CM,dc} = \frac{V_{o+} + V_{o-}}{2} \tag{4-1}$$

The top pair of switches and the bottom pair of switches can operate in a 180° phase-shifted pattern or a synchronized pattern [199]. The former is usually preferred because it can reduce the output current ripple. However, the latter is better in terms of EMI emission as it theoretically generates zero CM voltage. Both methods are tested while the UPS system is serving the ac load and charging the battery at the same time. The waveforms of the positive and negative output voltages, the CM voltage of the dc-dc stage using two methods are shown for three switching cycles in Fig. 4-4 and Fig. 4-5. In Fig. 4-4(a) and Fig. 4-5(a), the red waveform represents the positive output voltage, and the black waveform represents the negative output voltage.



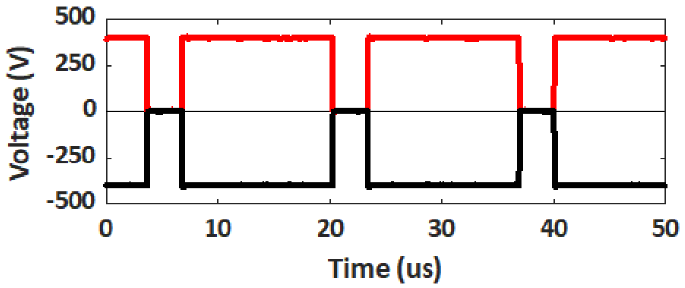
(a) Positive and negative output voltages of the dc-dc stage



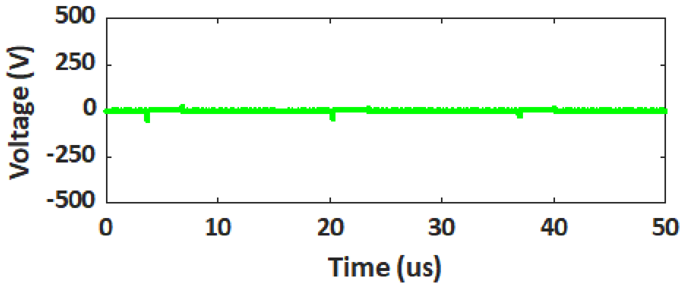
(b) Common mode voltage of the dc-dc stage

Fig. 4-4 Measured voltage waveforms with the phase-shifted operation.

With either modulation method, the positive output voltage switches between the positive half dc bus and zero, the negative output voltage switches between the negative half dc bus and zero. With the phase-shift operation, the CM voltage has one positive pulse and one negative pulse every switching cycle. The magnitude of the CM voltage pulse equals to one quarter of the dc bus voltage. With the synchronized operation, the CM voltage only has short pulses with very low values at switching instants. Although the topology and operation pattern are exactly symmetric even considering dead-time, differences remain among switching devices and components in gate driving circuits, leading to slight mismatches between the top switch pair and the bottom switch pair.



(a) Positive and negative output voltages of the dc-dc stage



(b) Common mode voltage of the dc-dc stage

Fig. 4-5 Measured voltage waveforms with the synchronized operation.

The disturbance voltages of phase a at the ac input port with the two modulation methods are measure and shown in Fig. 4-6.

As can be observed, the emission with the synchronized operation has around 10 dB lower magnitude from 1 MHz to 7 MHz compared with the phase-shifted operation. It is the direct reflection of the reduced CM voltage generated from the dc-dc stage, which propagates to the ac mains input side through the ground.

For the rectifier and inverter stage, the CM voltage is defined as the average voltage of the three phase output voltages, with the reference to the middle point of the converter dc bus.

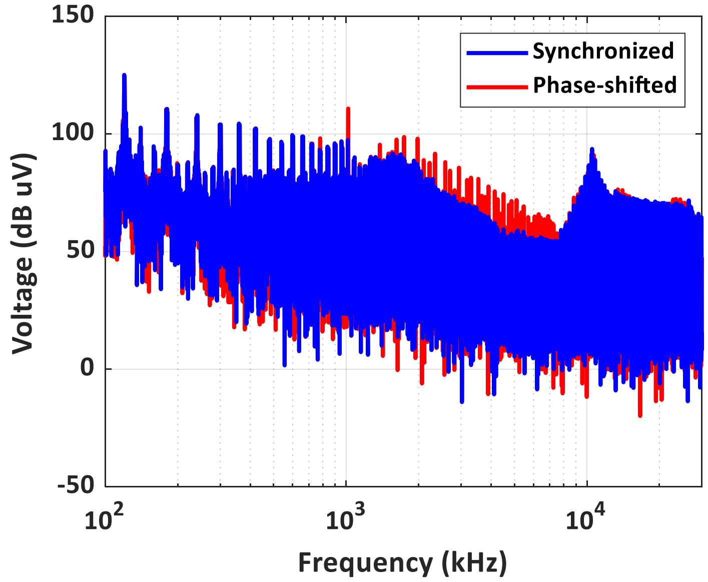


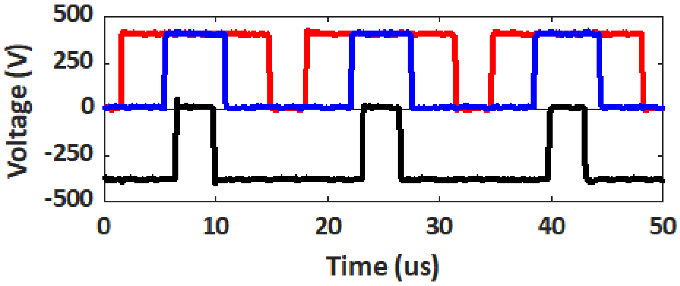
Fig. 4-6 Disturbance voltage with different modulation methods for the dc-dc stage.

$$V_{CM,ac} = \frac{V_{o,a} + V_{o,b} + V_{o,c}}{3} \tag{4-2}$$

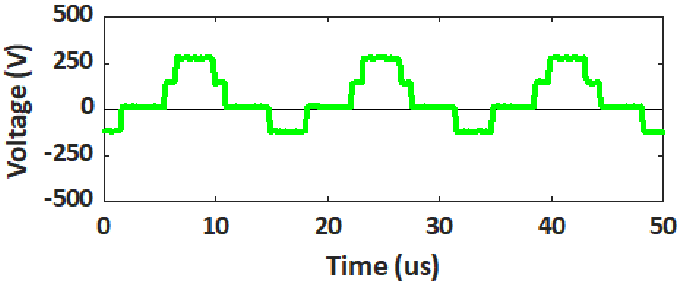
The benefit of a newly developed single common voltage pulse (SCMVP) modulation [201] is explored with the comparison to the traditional center-aligned space vector pulse width modulation (SVPWM) method. Both methods are tested while the UPS system is only serving the ac load. The rectifier stage and the inverter stage have the same modulation method in each test. The waveforms of three-phase output voltages, the CM voltage of the rectifier stage are shown for three switching cycles in Fig. 4-7 and Fig. 4-8. In Fig. 4-7(a) and Fig. 4-8(a), the black waveform represents the output voltage of phase a, the red waveform represents the output voltage of phase b, and the blue waveform represents the output voltage of phase c.

With either modulation method, each phase output voltage switches between the positive half dc bus and zero, or between the negative half dc bus and zero. By cancelling one positive voltage pulse and one negative voltage pulse from two phases, the SCMVP PWM generates only one CM voltage pulse every switching cycle, compared to three pulses of the traditional

SVPWM method. The peak value of the CM voltage pulse is also halved from one third of the dc bus voltage to one sixth of the dc bus voltage.

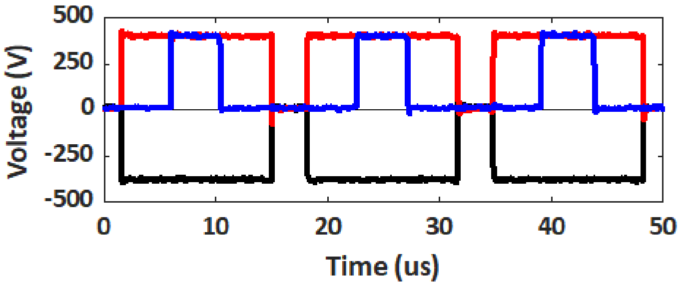


(a) Three-phase output voltages of the rectifier stage

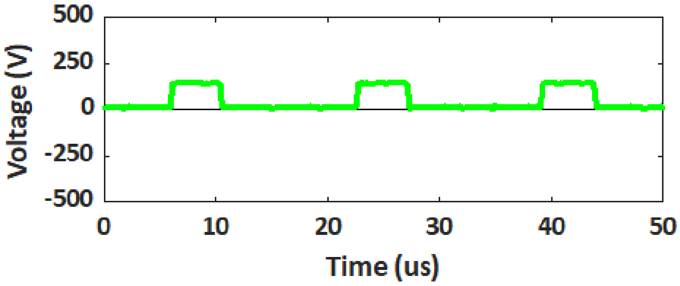


(b) Common mode voltage of the rectifier stage

Fig. 4-7 Measured voltage waveforms with the center-aligned space vector modulation.



(a) Three-phase output voltages of the rectifier stage



(b) Common mode voltage of the rectifier stage

Fig. 4-8 Measured voltage waveforms with the single common mode voltage pulse modulation.

The disturbance voltages of phase a at the ac input port with the two modulation methods are measured while the rectifier stage and the inverter stage are operating, and the dc-dc stage always remains blocked. The disturbance voltages of phase a at the ac input port are shown in Fig. 4-9.

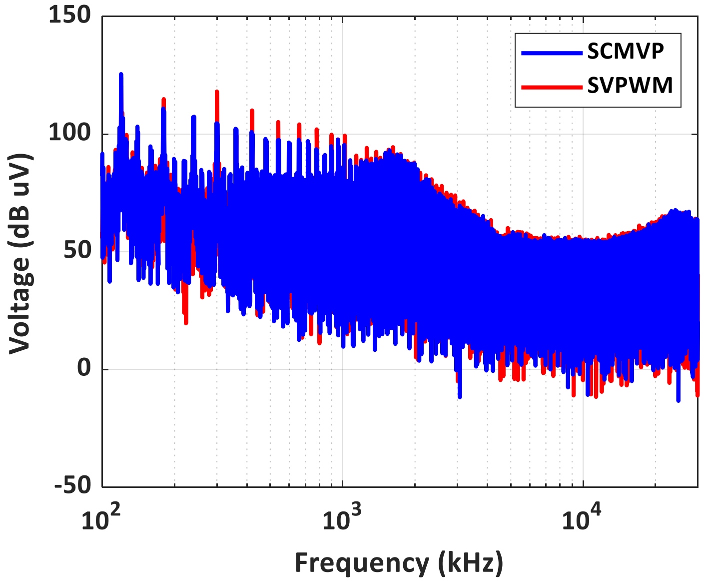


Fig. 4-9 Disturbance voltage with different modulation methods for the rectifier stage and the inverter stage.

As can be observed, the emission with the SCMVP shows 5~15 dB reduction at the multiples of the switching frequency. It is the direct reflection of the reduced CM voltage generated from the rectifier stage and the inverter stage. As the corner frequency of the EMI filter is usually decided by the required attenuation in the low frequency part in the specified frequency range, the above reduction will reduce the EMI filter requirement.

4.2.4 Impact of Operation Modes

The three power conversion stages in the UPS system are involved in the power transfer in different ways depending on the system configuration and the operation mode. As an online UPS system, the inverter stage is always operating to supply the loads. In this study, the EMI emissions in two operation modes are compared. In the normal operation mode, the mains input power is available, and the battery is fully charged. The rectifier and inverter stage are operating while the dc-dc stage remains blocked. In the charging operation mode, the mains input power is available, and the battery is being charged. Three stages are operating at the same time with power flowing from the ac input to both the ac loads and the battery.

The disturbance voltage of phase a at the ac input port is measured while the UPS system is in the normal operation, and then in the charging operation. The rectifier stage remains at the rated full power in both tests. Based on the comparison results of different modulation methods, the SCMVP modulation is applied to the rectifier stage and the inverter stage, the synchronized operation is applied to the dc-dc stage, to reduce the EMI emission. The disturbance voltages of phase a at the ac input port in two operation modes are shown in Fig. 4-10.

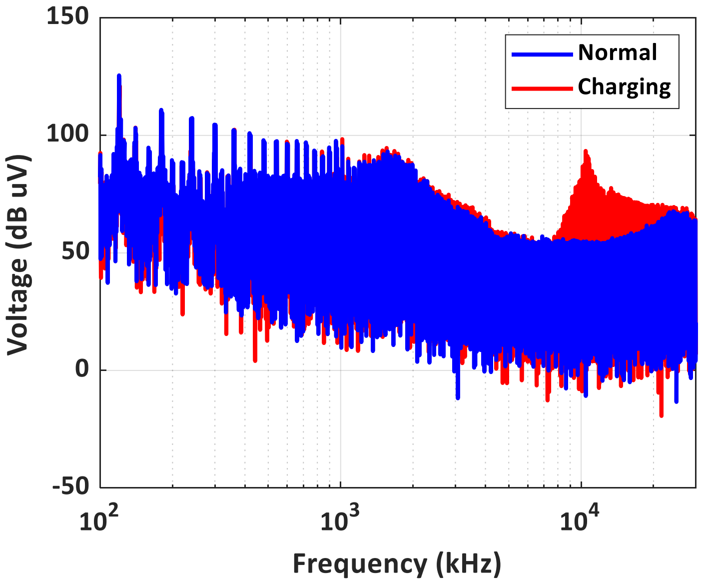


Fig. 4-10 Disturbance voltage with different operation modes.

The disturbance voltage in the charging operation has around 5~30 dB increase from 8 MHz to 25 MHz compared to the normal operation. Although the synchronized operation of dc-dc stage generates little CM voltage, the operation changes the propagation path impedance. The dc-dc stage shows high impedance when blocked in the normal operation but relatively low impedance at high frequencies when operating in the charging operation as a presence of large parasitic capacitors on the battery cabinets. At the frequency range where the impedance has extreme low value, the disturbance voltage of the mains input observes apparent increase in the charging operation. The disturbance voltage of other frequency range is mainly decided by the operation of the rectifier stage and inverter stage.

The impact of power distribution between the inverter stage and the dc-dc stage during the charging operation is also evaluated. The disturbance voltage of phase a at the ac input port is measured when the inverter stage consumes 90 %, then 80 %, of the rated power. The rectifier stage remains at the rated full power in both tests, and the dc-dc stage consumes the rest of the total power. The disturbance voltages of phase a at the ac input port in two operation conditions are shown in Fig. 4-11.

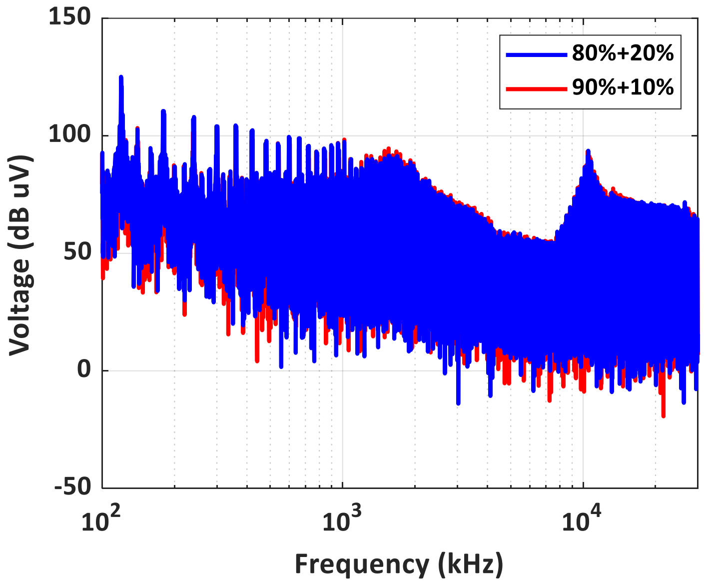


Fig. 4-11 Disturbance voltage with different power distribution.

The two spectrums are very similar, and the difference of the peak values at any frequency is less than 5 dB. While in the charging operation, the propagation paths are always the same, the CM voltage of each power conversion stage always has the same magnitude and fundamental frequency regardless of the power distribution. Although the duty ratios of the output voltages are different with different power distribution, they do not change much. Although the common mode voltages change with the duty ratios of the output voltages, the difference is much smaller compared with the difference when using different modulation methods. Therefore, the impact of power distribution on EMI emission is not significant.

4.2.5 EMI Filter Design

Different operation conditions affect the EMI noise generation from the three power conversion stages, the propagation in the system, and consequently the EMI disturbance at the ac mains input. For a given UPS system, the filters should be designed based on the worst EMI emission among different operation modes, as the operation mode is decided by the required service. However, the UPS systems usually have some freedom to choose the modulation methods. Then the filters can be designed based on the best EMI emission among different modulation methods. Therefore, the filters are designed based on the disturbance voltage measured when the system is operating in the charging mode, with the SCMVP modulation for the rectifier and inverter stage, the synchronized operation for the dc-dc stage. The disturbance voltage of phase a at the ac input port without attenuation is shown in Fig. 4-12. The green solid lines represent the quasi-peak limits in the standard, and the green dashed lines represent the average limits in the standard. Both types of limits range from 150 kHz to 30 MHz.

As the disturbance voltage is higher than the defined limits for most of the frequency range, EMI filters are needed to change the noise path impedance to attenuate the noise. The CM and differential mode (DM) disturbance voltages of phase a at the ac input port are first extracted from the three-phase measurement results, as shown in Fig. 4-13.

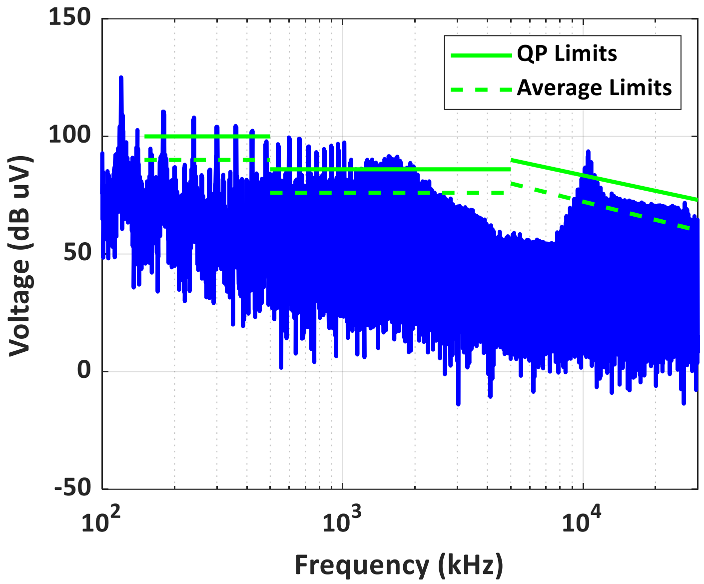
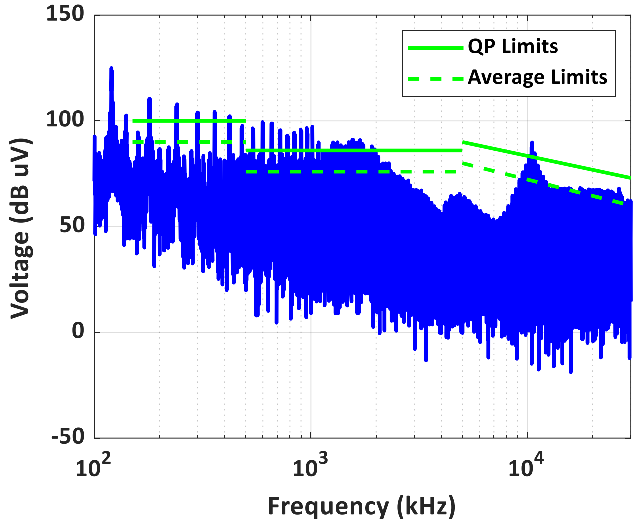


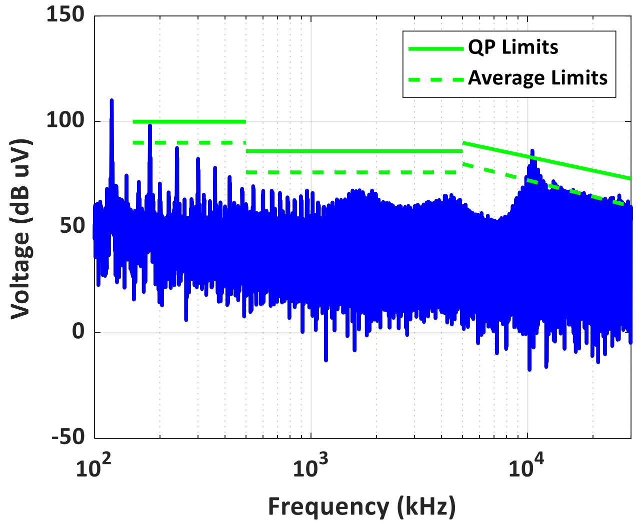
Fig. 4-12 Total disturbance voltage without EMI filters.

CM filters and DM filters are designed according to the CM and DM noise respectively. The DM noise without attenuation is already lower than the limit except around 180 kHz and around 10 MHz while the CM noise is the dominant component. The required attenuations are calculated by subtracting the limits from the unattenuated CM and DM noise. The corner frequency can be calculated based on the required attenuation and the selected topology.

The CM filter is first designed as it needs to provide large attenuation. A three-phase LC filter is used, including a three-phase coupled inductor and three Y-connected capacitors. A nanocrystalline core with the outer diameter of 45 mm is used. Another three-phase LC filter is used as the DM filter. The leakage inductors of the coupled inductor are used as the inductors in the DM filters and three more capacitors are connected. The configuration and the parameters of the filters are shown in Fig. 4-14 and Tab. 4-2.



(a) Common mode component



(b) Differential mode component

Fig. 4-13 Disturbance voltage without EMI filters.

After connecting the CM and DM filters into the system, the disturbance voltage is measured again, as shown in Fig. 4-15. The attenuated disturbance voltage is lower than the quasi-peak limit throughout the whole frequency range. The quasi-peak limit requirement is met. It is also lower than the average limit except around 10 MHz. Because the average disturbance voltage is always the same or lower than the peak disturbance voltage, it can be concluded from Fig. 4-15 that the average disturbance voltage is lower than the average limit except around 10 MHz.

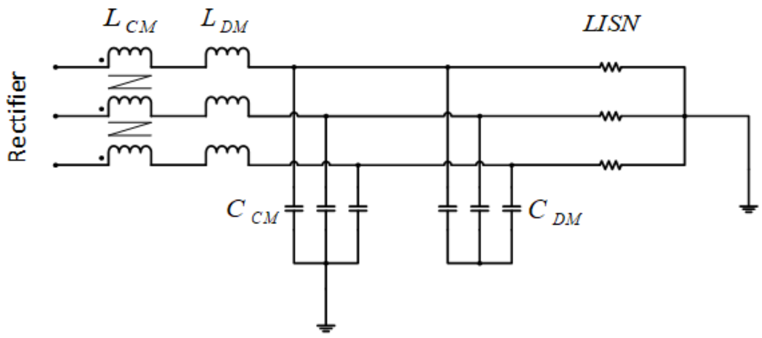


Fig. 4-14 Configuration of the EMI filters.

Tab. 4-2 Parameters of the EMI filters.

Parameter	Value
L_{CM}	923 μH
C_{CM}	330 nF
L_{DM}	0.57 μH
C_{DM}	47 nF

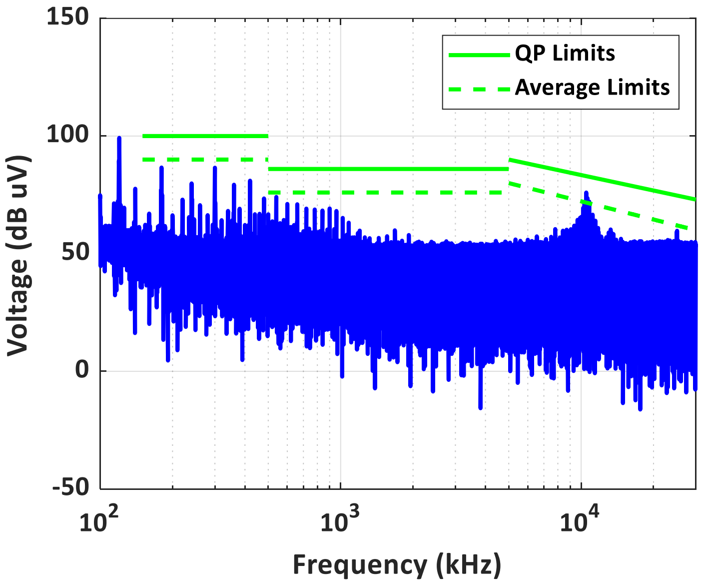


Fig. 4-15 Total disturbance voltage with EMI filters.

Fig. 4-16 shows the measurement using the average detector of the EMC analyzer, which is only used to measure the average disturbance voltage from 10 MHz to 11 MHz to avoid long time duration of the measurement. The results confirms that the average disturbance voltage around 10 MHz meets the average limit. The average limit requirement is met.

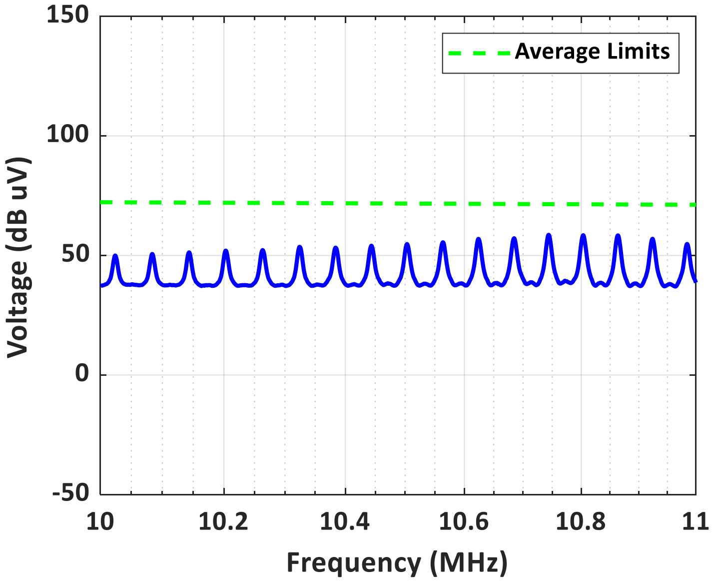


Fig. 4-16 Total average disturbance voltage with EMI filters.

4.3 EMI Evaluation and Mitigation of the Control System in a SiC-Based Modular Multilevel Converter

The idea of Power Electronics Building Blocks (PEBBs) has been proposed [202], [203] and demonstrated [204]-[206] in power electronics conversion systems. Including not only switching devices and passive components but also thermal management components and various auxiliary circuits, a PEBB can be viewed and used as the basic power conversion unit in larger scale systems. Given the modular structure, Modular Multilevel Converter is one of the multilevel topologies than can be easily realized by using PEBBs.

PEBB-based converter can increase its voltage or current rating by connecting more PEBBs in series or in parallel while still utilizing lower rated components and designs in each PEBB. The modularity can also be extended to control implementation [207]-[210]. In a PEBB-based converter, most of the control hardware and computation tasks may be distributed into each PEBB.

However, the EMI emission does not inherent the modularity. The EMI generation and propagation when operating PEBB-based converters could be very different compared to operating a single PEBB alone. Connecting multiple PEBBs in series or in parallel also brings more EMI noise sources and propagation paths comparing to operating with less PEBBs.

PEBB-based converters can benefit from the use of SiC MOSFETs to achieve high efficiency and high power density in MV systems [74], [211]-[213]. However, the use of SiC MOSFETs also brings increased EMI emission. It is well known that the EMI noise at the power ports of the PEBB-converters needs to be contained [214], but the EMI noise at the control ports is sometimes hard to be specified or even completely overlooked.

4.3.1 MMC Prototype under Study

The converter under evaluation is a three-phase MMC prototype. The key specifications of the prototype are shown in Tab. 4-3. The configuration of the converter is shown in Fig. 4-17.

Tab. 4-3 Specification of the MMC under evaluation.

Parameter	Value
Apparent Power	45 kVA
AC Line RMS Voltage	480 V
DC Bus Voltage	1.0 kV
Number of Cell per Arm	1
Cell Capacitor Voltage	1.0 kV
Line Frequency	60 Hz
Switching Frequency	100 kHz

Each PEBB employs a full-bridge (FB) topology and includes two 1.7 kV SiC MOSFET half-bridge modules [215]. A PEBB and its internal components are shown in Fig. 4-18.

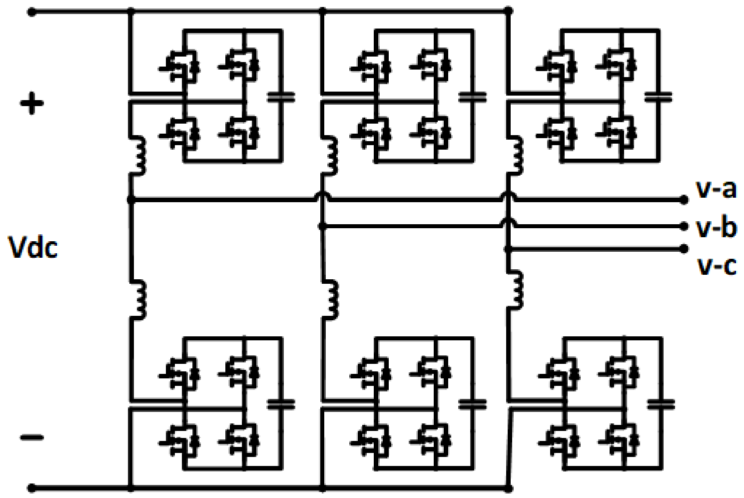


Fig. 4-17 Circuit diagram of the MMC under evaluation.

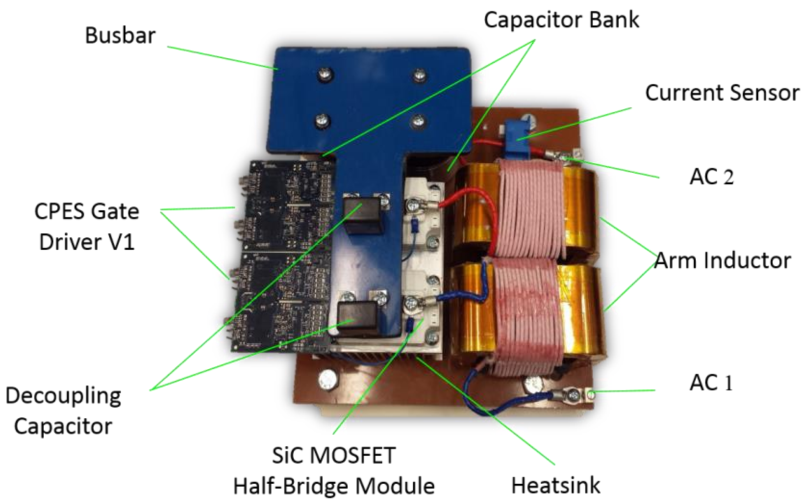


Fig. 4-18 One full-bridge PEBB.

The converter is built by including one PEBB per arm, thus two PEBBs per phase leg, and can be operated as either a three-phase inverter or a three-phase rectifier. The converter prototype is shown in Fig. 4-19.

As the total number of PEBBs in the prototype is only six, a central controller is used instead of a series of distributed controller. The control board and its connections are shown in Fig. 4-20. The power of the control board is provided by a TDK-Lambda 120 Vac to 24 Vdc power supply through a CM choke. The microcontroller on the top side of the board [131] performs the closed-loop calculation and sends out the gate signals. to the CPLD [132] on the board. The CPLD processes the signals and sends out the gating signals.

Fig. 4-19 The SiC-based MMC under evaluation.

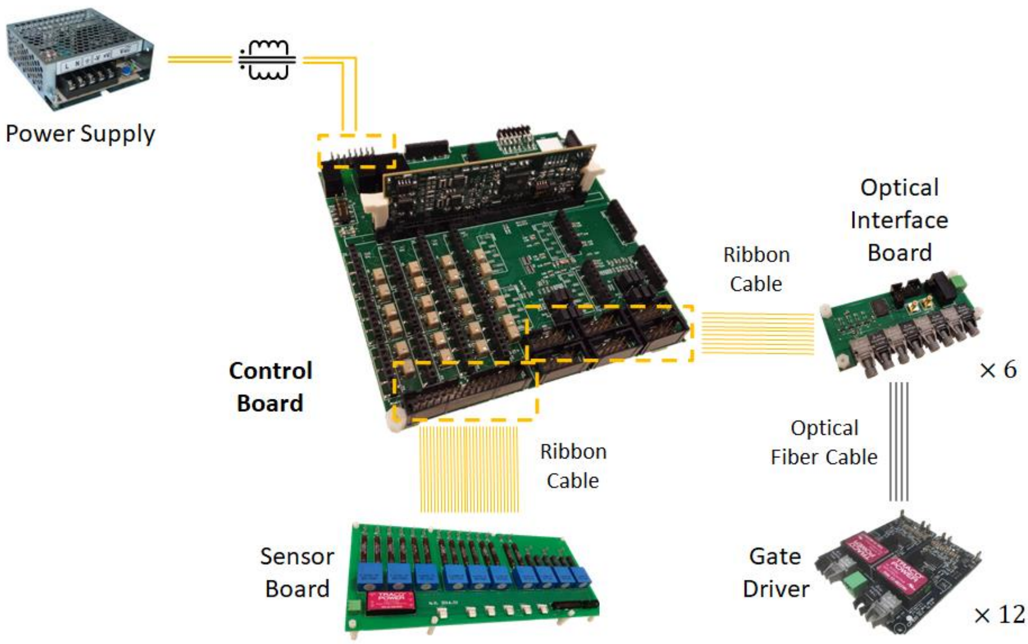


Fig. 4-20 The control board and its connections.

The electrical gate signals are transmitted from the control board to six optical interface boards through ribbon cables. The ribbon cables also transfer power to the optical interface boards. Then the optical gate signals are generated on the boards and transmitted to the gate drivers through optical fiber cables. Using optical gate signals is part of the solutions to ensure the high *dv/dt* immunity of the auxiliary circuit. The control board receives electrical sensing feedback signals of the voltages and currents from a sensor board through ribbon cables.

The power of each gate driver board is provided by the same type of 120 Vac to 24 Vdc power supply. Each PEBB has its own power supply box and another one is used for the control board, so that the noise propagation at the power supply connections is minimized.

LEM closed-loop sensors using the Hall effect are employed to sensor the currents and voltages. The current sensors are localized in each PEBB to sense the arm currents. The voltage sensors are located on a central sensor board, which is shown in Fig. 4-21. The power of the sensor board is provided by the same power supply box which feeds the control board but through another choke. There are ten voltage sensors on the board sensing six cell capacitor voltages, three ac voltages and the dc bus voltage. Each voltage sensor has a pair of twisted high voltage wires connecting to the voltage sensing points. The sensor board also has six groups of wires connecting to the current sensors, providing the power and collecting the sensing signals. Then all the voltage and current sensing signals are transmitted back to the control board through ribbon cables.

Each gate driving channel has a feedback signal indicating whether this channel of driving circuit has detected faults or not. At the same time, each sensing signal is compared to pre-set limits on the control board to check if there is over-voltage or over-current. The CPLD collects all channels of the fault signals and turn off all gating signals if any kind of fault is observed.

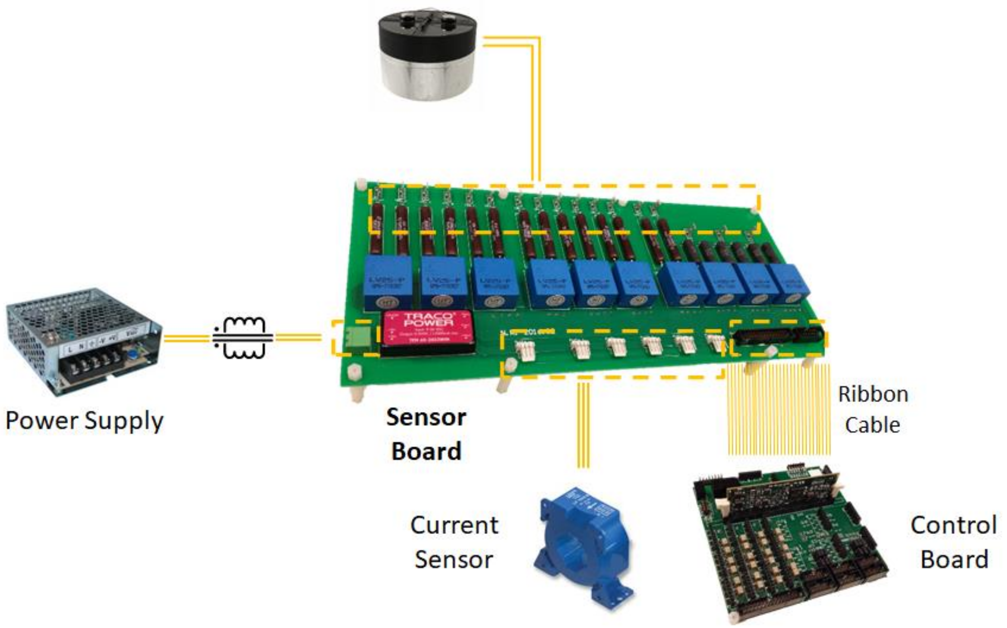
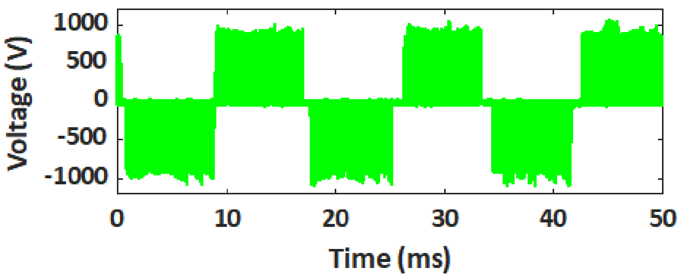


Fig. 4-21 The sensor board and its connections.

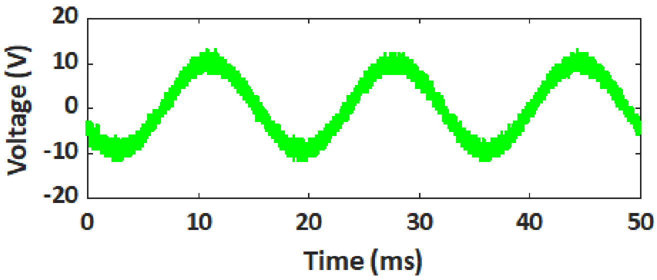
After the PEBBs are built, each of them is first tested as a full-bridge inverter to validate the design. The capacitor is connected to a dc voltage source with 1 kV output voltage. A resistive load is connected between two output terminals of the PEBB through the arm inductors. The output voltage and output current are shown for three line cycles in Fig. 4-22. The output voltage is switching between 1 kV and 0 V or between -1 kV and 0 V. All the PEBBs are verified to be able to operate at the rated voltage of 1 kV.

Then the six individually verified PEBBs are connected together to form the three-phase converter. However, initially the converter could only operate continuously with the dc bus voltage, cell capacitor voltages and ac voltages being half of their respective rated values. When further increasing the voltages, the control board randomly falsely triggers protection. Then all the switching devices are turned off, preventing the continuous operation.

The design and construction of the converter are part of the previous work. The converter design details and experimental results are shown in [216], [217].



(a) Output voltage



(b) Output current

Fig. 4-22 single PEBB full-bridge inverter test results.

4.3.2 EMI Evaluation of the Control System

It is obvious the operation of the control board is affected during the converter tests. To locate the critical EMI propagation paths, total CM currents are measured at different connections in the control system when the inverter is operating at half of the rated voltages. The Tektronix TCP0030A current probe [218] is used, which has a bandwidth greater than 120 MHz and can accurately measure current levels as low as 1 mA.

The optical fiber cables between optical interface boards and gate driver boards have high immunity against EMI noise, and the optical interface boards only have connections to the gate driver boards and to the control board. Therefore, there should be little noise propagated along the ribbon cables between the control board and the optical interface boards as well. The CM current at the power supply connection of the control board is first measured. It is shown for three line cycles in Fig. 4-23. The peak-to-peak value of the CM current is less than 200 mA.

Although it is not conclusive, but the magnitude of the CM current is relatively low. Therefore, the noise is likely mainly from the other connection, from the sensor board to the control board.

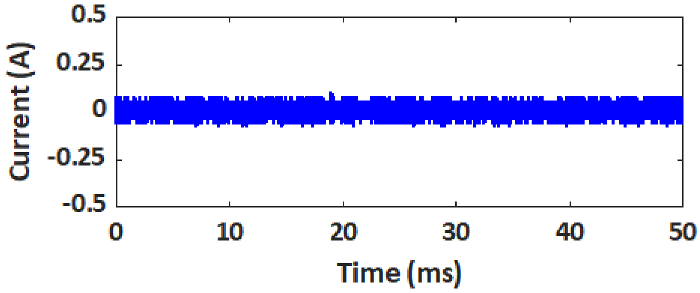
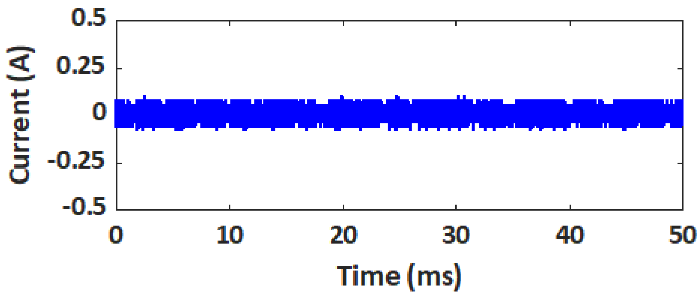


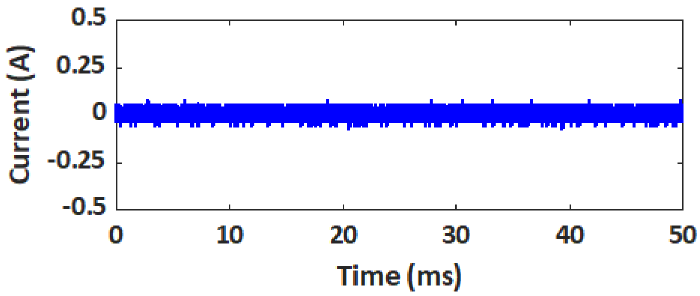
Fig. 4-23 CM current at the power supply connection of the control board.

The CM currents at different paths of the sensor board are measured. Fig. 4-24(a) shows the CM current at the power supply connection, the peak-to-peak value of which is less than 200 mA. Fig. 4-24(b) shows the CM current at the connections between one arm current sensor and the sensor board, the peak-to-peak value of which is less than 200 mA. Fig. 4-24(c) shows the CM current at the connections between one cell capacitor and its corresponding voltage sensor on the sensor board. The peak-to-peak value of the CM current at the voltage sensing path is 860 mA, which is significantly higher than the others. The three currents are shown for three line cycles. It should be noted that the currents shown in Fig. 4-23 and Fig. 4-24 were measured in separate tests and are not aligned with each other. The spectrum of the CM current at the voltage sensing connection is shown in Fig. 4-25. It has high peaks at the multiples of the switching frequency.

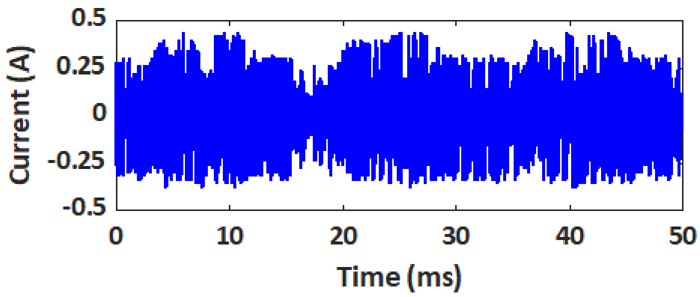
For the cell capacitor voltage sensors, each sensor is used to sense the differential voltage between the positive and negative terminals of the capacitor. However, the voltage potential of the capacitor compared to the voltage potential of another capacitor or to the ground keeps changing with the switching actions of the switching devices.



(a) Power supply connection



(b) Current sensor connection



(c) Voltage sensing connection

Fig. 4-24 CM current at different paths of the sensor board.

One full-bridge PEBB and its two pair of complementary gate signals are shown in Fig. 4-26. The CM voltage of the cell capacitor voltage is the average voltage of the positive and negative terminal voltage potentials of the cell capacitor, with the reference to the converter negative dc bus.

$$V_{c,CM} = \frac{V_{c,+} + V_{c,-}}{2} \tag{4-3}$$

For a cell in the upper arm, the CM voltage of the capacitor equals to:

$$V_{c,CM,u} = \frac{3V_{dc}}{2} - S_{1,u} \times V_{c,u} \tag{4-4}$$

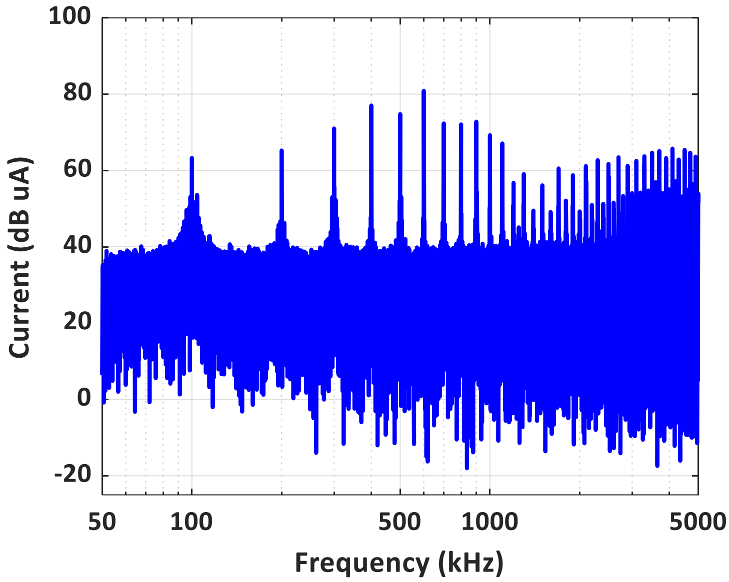


Fig. 4-25 Spectrum of CM current at the voltage sensing connection.

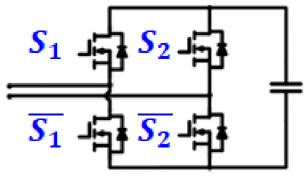


Fig. 4-26 One full-bridge PEBB and its gate signals.

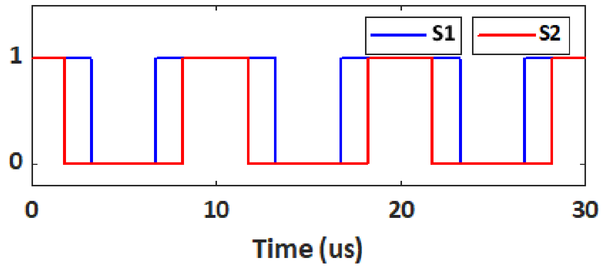
Where $V_{c,CM,u}$ is the CM voltage of a cell capacitor in the upper arm, V_{dc} is the converter dc bus voltage, $S_{1,u}$ is the gate signal for the top switch of the first switch pair in the same PEBB, and $V_{c,u}$ is the cell capacitor voltage in the same PEBB.

For a cell in the lower arm, the CM voltage of the capacitor equals to:

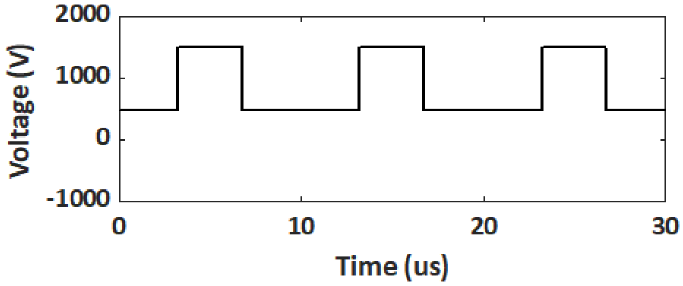
$$V_{c,CM,l} = \frac{V_{dc}}{2} - S_{2,l} \times V_{c,l} \tag{4-5}$$

Where $V_{c,CM,l}$ is the CM voltage of a cell capacitor in the lower arm, $S_{2,l}$ is the gate signal for the top switch of the second switch pair in the same PEBB, and $V_{c,l}$ is the cell capacitor voltage in the same PEBB.

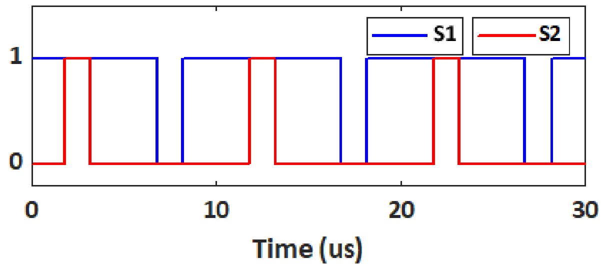
As the capacitor voltage has an average value which equals to the converter dc bus voltage, and a low frequency ripple much lower than the average value, the CM voltage of the upper arm cell capacitor approximately equals to either $\frac{3V_{dc}}{2}$ or $\frac{V_{dc}}{2}$, the CM voltage of the lower arm cell capacitor approximately equals to either $\frac{V_{dc}}{2}$ or $-\frac{V_{dc}}{2}$. Simulated gate signals and cell capacitor CM voltages are shown for three switching cycles in Fig. 4-27.



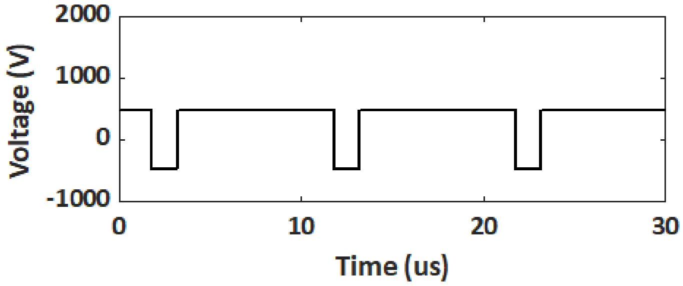
(a) Gate signal in the upper arm



(b) Cell capacitor common mode voltage in the upper arm



(c) Gate signal in the lower arm



(d) Cell capacitor common mode voltage in the lower arm

Fig. 4-27 Simulated gate signals and cell capacitor common mode voltages.

The CM voltage of each cell capacitor changes with the switching actions of one pair of the devices in the same PEBB. It changes at the same frequency, which is 100 kHz, and the same speed as the device drain-to-source voltage, which is dependent on the device voltage and current values, and could be as high as 20 V/ns with the test conditions.

However, the circuit diagram shown in Fig. 4-17 is only a general and simplified one. As can be seen in Fig. 4-18, each arm inductor in the circuit diagram is split into two actual inductors, and they are located at the two different output terminals of the PEBB. A more accurate circuit diagram with split arm inductors is shown in Fig. 4-28.

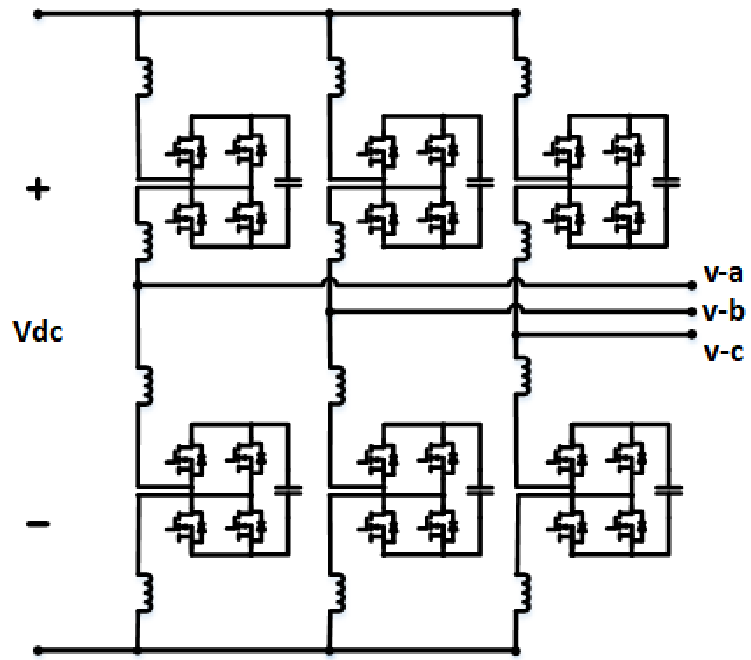


Fig. 4-28 Circuit diagram of the MMC under evaluation with split arm inductors.

With the inductors located between the PEBBs and the converter positive or negative bus, the voltages across the inductors will affect the cell capacitor CM voltages. The sum of the four inductor voltages is the difference between the converter bus voltage and the total cell output voltages. The total inductor voltage equals to:

$$V_{ind,totall} = V_{dc} - \left(S_{1,u} - S_{2,u}\right) \times V_{c,u} - \left(S_{1,l} - S_{2,l}\right) \times V_{c,l} \tag{4-6}$$

The average value of the total inductor voltage in a line cycle is zero, but the instant value is not zero.

All the arm inductors are designed and built in the same way. Each two inductors in the same arm share the same current and should share the same voltage.

The arm inductors in opposite arms do not share the same current or voltage, the difference of them contributes to the changes in the current or voltage in the ac lines. The inductance in each output line is 1.5 mH, which is larger than the inductance in each arm, which is 1.0 mH. In addition, the voltage change corresponding to the ac component is applied on arm inductors across different phase legs and the ac line inductors. Therefore, it can be approximated that all the four inductors in the same phase leg share the same voltage.

Then the cell capacitor CM voltages approximately equal to:

$$V_{c,CM,u} \approx \frac{3V_{dc}}{2} - S_{1,u} \times V_{c,u} - \frac{V_{ind,totall}}{4} \tag{4-7}$$

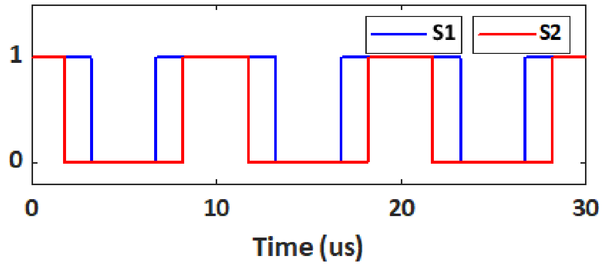
$$V_{c,CM,l} \approx \frac{V_{dc}}{2} - S_{2,l} \times V_{c,l} + \frac{V_{ind,totall}}{4} \tag{4-8}$$

Further ignoring the low frequency ripples on the cell capacitor voltages, the cell capacitor CM voltages approximately equal to:

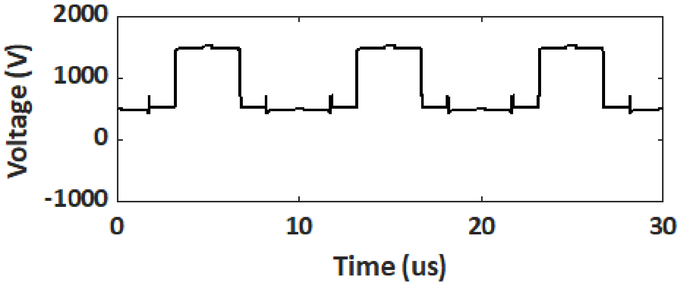
$$V_{c,CM,u} \approx \frac{5 - 3S_{1,u} - S_{2,u} + S_{1,l} - S_{2,l}}{4} \times V_{dc} \tag{4-9}$$

$$V_{c,CM,l} \approx \frac{3 - S_{1,u} + S_{2,u} - S_{1,l} - 3S_{2,l}}{4} \times V_{dc} \tag{4-10}$$

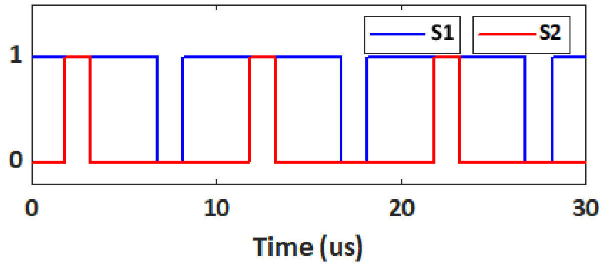
The simulation model is run again with the split arm inductors. Simulated gate signals and cell capacitor CM voltages are shown for three switching cycles in Fig. 4-29.



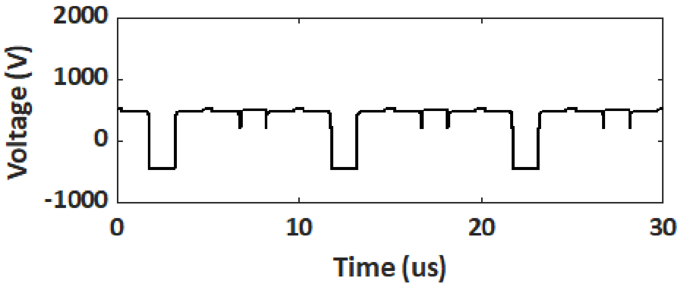
(a) Gate signals in the upper arm



(b) Cell capacitor common mode voltage in the upper arm



(c) Gate signals in the lower arm



(d) Cell capacitor common mode voltage in the lower arm

Fig. 4-29 Simulated gate signals and cell capacitor common mode voltages.

Compared to the results in Fig. 4-27, the first switch pair in the upper arm still plays the major role in determining the cell capacitor CM voltage in the upper arm, the second switch pair in the lower arm still plays the major role in determining the cell capacitor CM voltage in the lower arm. However, with the split arm inductors, the other switch pairs in the same phase leg contribute to the additional short pulses in the cell capacitor CM voltages, with the magnitude of around one quarter of the converter dc bus voltage. In addition, there are even more changes with smaller magnitude, which are the results of the switching actions of the devices in the other phase legs.

For the selected Hall-effect voltage sensors, the primary side connects to the sensed capacitor through two series-connected resistors; the secondary side operates as a current source and connects to a measuring resistor. The voltage across the measuring resistor is connected to the control board for Analog-Digital-Conversion (ADC) and protection. The measuring resistors of different channels are grounded to the control board ground through small resistors. There is also a coupling capacitor between the primary side and the secondary side of the voltage sensor with a capacitance value at the order of 10 pF.

Therefore, each cell capacitor and its sensing circuit form a branch in terms of EMI noise generation and propagation. CM currents are generated as a result of the fast and frequent CM voltage changes and the coupling capacitors. Furthermore, according to Equation (4-9) and (4-10), some of the switching actions lead to opposite changes in cell capacitor CM voltages. Some CM current components may circulate between different sensing channels. Although the sensing circuit is designed to measure the differential voltages of the cell capacitors, the actual voltages at the control board inputs also includes CM components, which may affect the original ADC or protection functions.

In the single cell full-bridge inverter test, the capacitor voltage is measured for monitoring purpose. As the capacitor is directly connected to the dc source, the voltage sensing is not exposed to the fast CM voltage change. However, in the converter three-phase inverter test and three-phase rectifier test, there are CM voltages as analyzed and simulated above. The control system is not able to maintain the designed function with the noises.

If more cells are built and connected in this PEBB-based converter, the CM voltages will be more complicated as they depend on more switching actions of the other cells.

4.3.3 EMI Mitigation of the Control System

The EMI noise generation in the voltage sensing paths is directly related to the switching actions of the switching devices. Therefore, it is hard to reduce the noise source without sacrificing the performance of the converter. Then the propagation paths or the impedances of the paths need to be changed to reduce the EMI impact to the control system operation. With this prototype, the easiest way is to add chokes at the voltage sensing paths. Toroidal powder cores are used as the cores of the chokes. The chocks are placed between each cell capacitor and the corresponding voltage sensor. The CM current at the same voltage sensing connection is measured again when the inverter is operating with half of the rated voltages, as shown in Fig. 4-30.

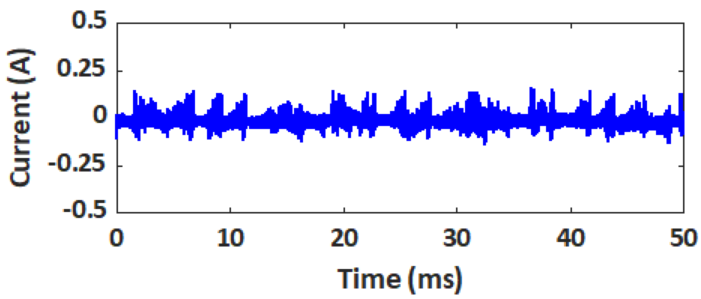
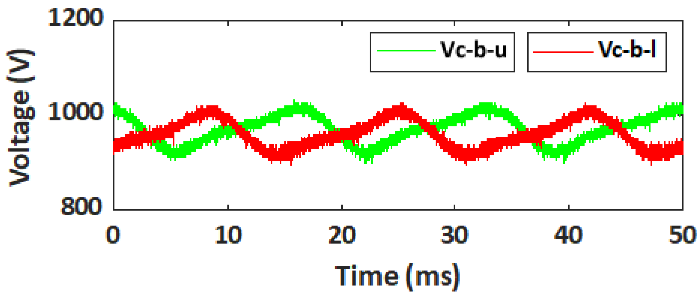


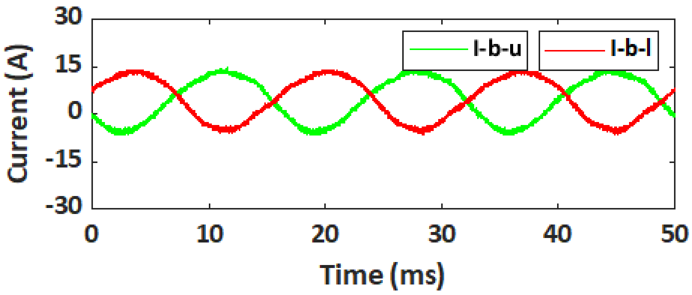
Fig. 4-30 Attenuated CM current at the voltage sensing connection of the sensor board.

The currents in Fig. 4-24(c) and Fig. 4-30 are not aligned with each other. The peak-to-peak value of the CM current is 320 mA, which is 63% lower compared to the result in Fig. 4-24(c).

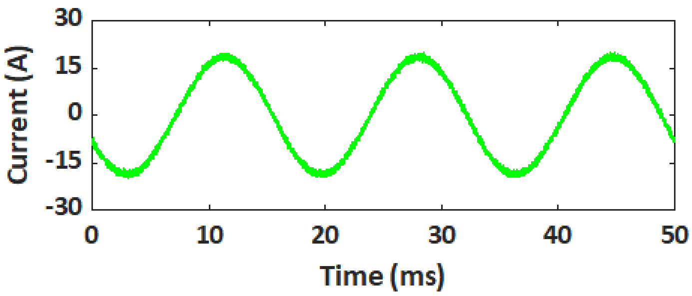
Then the voltages of the inverter are increased to the rated value. The converter is able to continuously operate without any falsely triggered protection. Two cell capacitor voltages, two arm currents and the ac output current of phase b during inverter operation at rated voltages are shown in Fig. 4-31.



(a) Cell capacitor voltages of phase b



(b) Arm currents of phase b



(c) AC output current of phase b

Fig. 4-31 Converter inverter operation test results.

4.4 EMI Evaluation and Mitigation of the Auxiliary System in a SiC-Based Modular Medium Voltage Converter

The modular MV converter with three ICBT cells per arm shown in Section 3.5.5 is studied.

4.4.1 EMI Evaluation of the Voltage Sensing Circuit

Similar as the modular converter in Section 4.3, the cell capacitor voltages need to be measured for the closed-loop control. However, the configuration of the sensing circuit is significantly changed to improve the EMC.

An isolated digital voltage sensor is implemented in each cell. It has an RC voltage divider circuit, the input of which is connected to the cell capacitor, the output of which is located in the middle of the series-connected resistors and capacitors. The output of the voltage divider circuit is connected to a signal conditioning circuit and then an ADC chip and then an FPGA chip, all powered by an isolated power supply [219]. The primary side of the power supply is connected to the middle point of the cell capacitor in the cell. Therefore, the potentials of all the circuits inside the voltage sensor is the same as the potential of the middle point of the cell capacitor. During the converter operation, the CM voltage of the cell capacitor has fast and frequency changes, but theoretically there is no CM voltage change across the voltage sensor. With this configuration, the EMI noise source is minimized.

The ADC is conducted in the voltage sensor and the result is sent to the FPGA. Then the FPGA sends out the ADC results to the local controller inside the cell through optical fiber cables. As the optical fiber cables have high immunity against EMI noise, the noise propagation is minimized.

4.4.2 EMI Evaluation of the Auxiliary Power System

The auxiliary power of each cell is provided by a Wireless Power Transfer (WPT). The negative terminal of the primary side of each WPT is connected to the ground. The negative terminal of the secondary side of each WPT is connected to the middle point of the cell capacitor. The voltage across a WPT equals to the CM voltage of the cell capacitor, which experiences fast and frequent CM voltages changes during the converter operation. With three cells per arm and ignoring the cell capacitor voltage ripple, the CM voltages of the three cell capacitors in the upper arm equal to:

$$V_{c,CM,u1} \approx \frac{7 - 2S_{u1}}{6} \times V_{dc} \tag{4-11}$$

$$V_{c,CM,u2} \approx \frac{7 - 2S_{u1} - 2S_{u2}}{6} \times V_{dc} \tag{4-12}$$

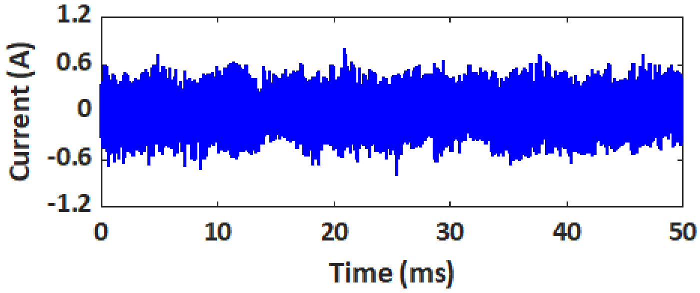
$$V_{c,CM,u3} \approx \frac{7 - 2S_{u1} - 2S_{u2} - 2S_{u3}}{6} \times V_{dc} \tag{4-13}$$

Where $V_{c,CM,u1}$ is the CM voltage of the cell capacitor in the first upper arm cell, S_{u1} is the gate signal for the main switch in the first upper arm cell, V_{dc} is the converter dc bus voltage, $V_{c,CM,u2}$ is the CM voltage of the cell capacitor in the second upper arm cell, S_{u2} is the gate signal for the main switch in the second upper arm cell, $V_{c,CM,u3}$ is the CM voltage of the cell capacitor in the third upper arm cell, S_{u3} is the gate signal for the main switch in the third upper arm cell.

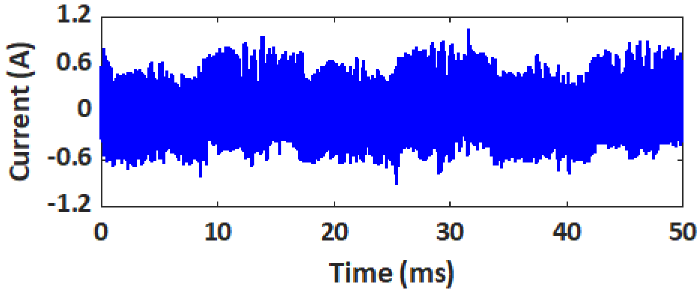
The CM voltage of the first cell only changes with the switching actions of the first cell. The CM voltage of the second cell changes with the switching actions of both the first and the second cell. The CM voltage of the third cell changes with the switching actions of all the three cells in the upper arm.

In the ICBT operation, the three cells in the upper arm approximately operate at the same time, with the difference decided by the cell capacitor voltage control. Therefore, the CM voltage change of the second cell is approximately twice, the CM voltage change of the third cell is approximately three times, both compared to the first cell.

The CM currents are measured at the inputs of the primary sides of the WPTs of the second cell and the third cell in the upper arm while the converter is operating at 12 kV and 25 A rms ac output current, as shown in Fig. 4-32. The spectrums of the two currents are shown in Fig. 4-33. It can be observed that the CM current at the third cell is higher.



(a) Second upper arm cell



(b) Third upper arm cell

Fig. 4-32 CM current at the input of the primary side of WPT.

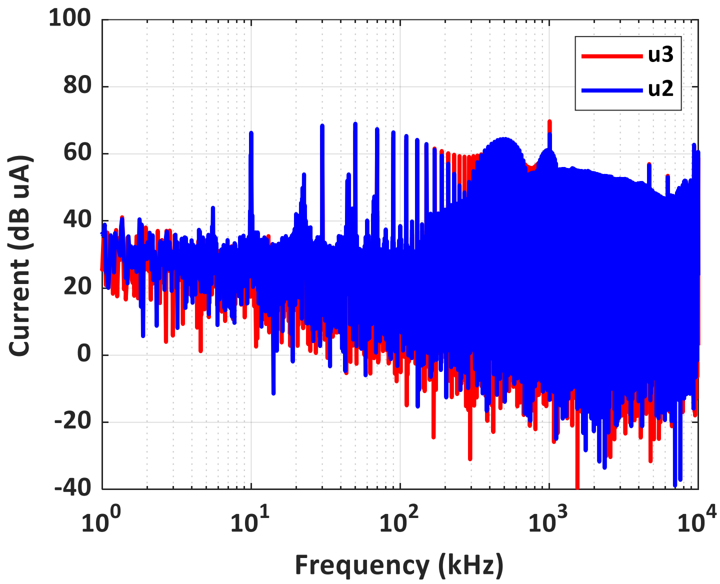


Fig. 4-33 Spectrums of CM currents at the input of the primary side of WPT.

4.4.3 EMI Mitigation of the Auxiliary Power System

The high CM current through the WPT may affect the correct function of the WPT, putting the auxiliary circuits in the cell in danger. There are two types of solutions to mitigate it.

The first solution is to increase the impedance of the propagation path, for example by adding CM chokes at the input of the primary side of the WPT. The attenuated CM current at the input of the primary side of WPT at the third upper arm cell is shown in Fig. 4-34. The spectrum comparison is shown in Fig. 4-35. It can be observed that the CM current is effectively attenuated.

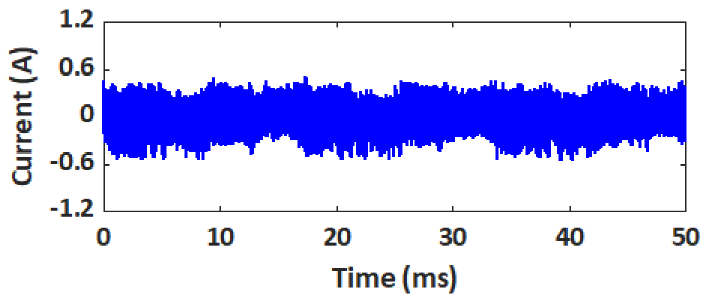


Fig. 4-34 Attenuated CM current at the input of the primary side of WPT at the third upper arm cell.

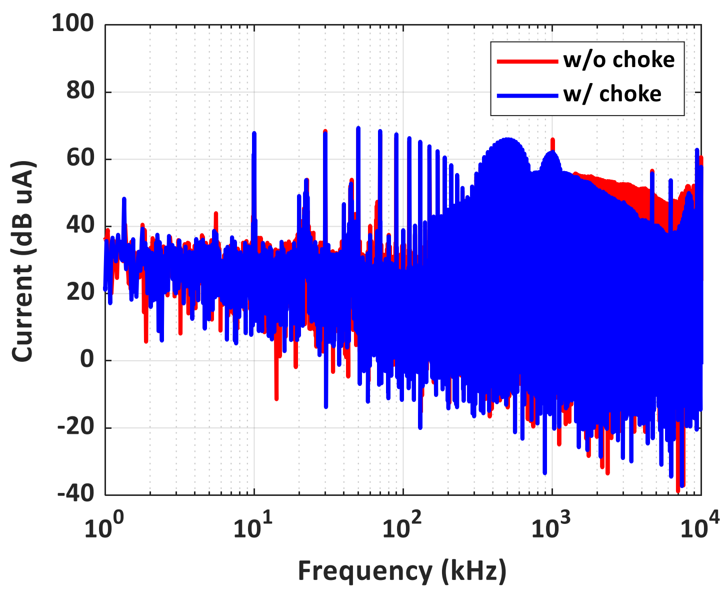
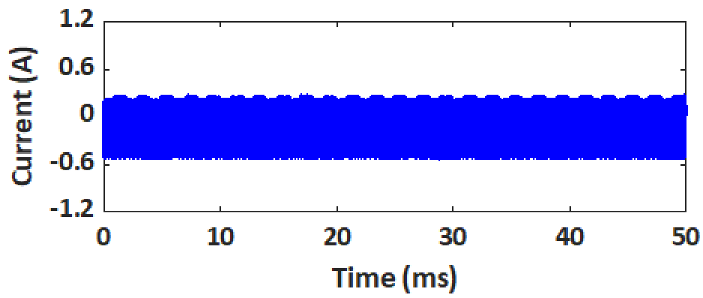
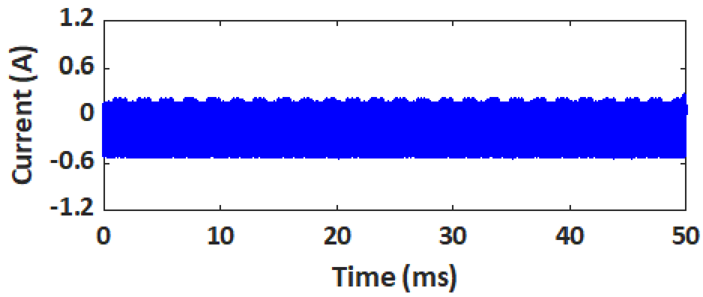


Fig. 4-35 Spectrums of CM currents at the input of the primary side of WPT at the third upper arm cell.

Another solution is to change the switching pattern of the cells, for example by applying additional delays to the gate signals for different cells. The CM current is measured at the third upper arm cell while the converter is operating at 12 kV and 25 A dc output current, using only the delays calculated by the cell capacitor voltage control first, then with 200 ns minimum delay between the gate signals for any two cells, as shown in Fig. 4-36. At each switching transition, the gate signals of one cell do not have any delay; the gate signals of another cell have at least 200 ns delays, and the gate signals of the other cell have at least 200 ns additional delays. The spectrum comparison is shown in Fig. 4-37. It can be observed that the CM current is effectively attenuated.



(a) Without minimum delay



(b) With 200 ns minimum delay

Fig. 4-36 Attenuated CM current at the input of the primary side of WPT at the third upper arm cell.

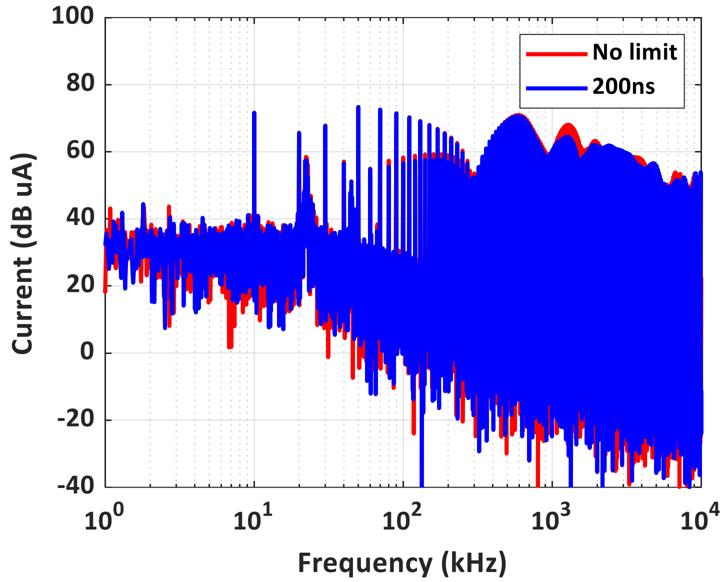


Fig. 4-37 Spectrums of CM currents at the input of the primary side of WPT at the third upper arm cell.

4.5 EMI Evaluation of the Auxiliary System in a SiC-Based Five-Level Stacked Multicell Converter

In this section, the conducted EMI disturbance in the auxiliary system in the designed five-level SMC prototype, which is descripted in Chapter 2, is studied to determine the best auxiliary system configuration to reduce the EMI susceptibility.

4.5.1 SMC Prototype under Study

The converter design details and experimental results are shown in Chapter 2.

During the tests, the input of the power circuit of the inverter prototype is connected to a high-voltage dc voltage source, the output voltage of which is 750 V; the input of the auxiliary circuit of the inverter prototype is connected to a benchtop low-voltage power supply, the output voltage of which is 24 V. The auxiliary input provides the power for the gate driving circuits for the switching devices and the power for the output current sensors.

The same control board used in Section 4.3 is used for the control calculation and it sends out the electrical gate signals to the inverter board. The control board is powered by the same benchtop low-voltage power supply.

4.5.2 EMI Evaluation in the Auxiliary System

With the aforementioned configuration, the CM current at the power supply connection of the control board is measured when the inverter is operating while the dc bus voltage is 200 V, and the output frequency is 3000 Hz. All the CM currents shown in this section are measured with the same test condition. The measured CM current is shown for one line cycle in Fig. 4-38. The peak-to-peak value of the CM current is 260 mA.

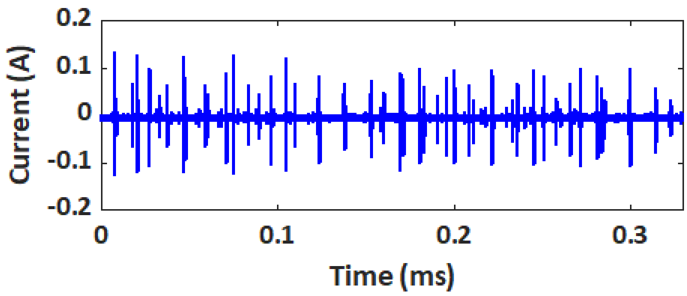


Fig. 4-38 CM current at the power supply connection of the control board.

To suppress the conducted EMI at the control board, two isolated power supplies [221] are connected in series and are connected between the output of benchtop power supply and the input of the control board. The CM current is measured again and is shown in Fig. 4-39. The peak-to-peak value of the CM current is reduced to 200 mA.

To further suppress the conducted EMI at the control board, digital isolators [222] are connected between the control board and the inverter board. The gate signals from the control board are sent to the primary side of the digital isolators, and then the isolated gate signals are sent from the secondary side of the digital isolators to the inverter board. The CM current at the power supply connection of the control board is measured again and is shown in Fig. 4-40. The peak-to-peak value of the CM current is reduced to 184 mA.

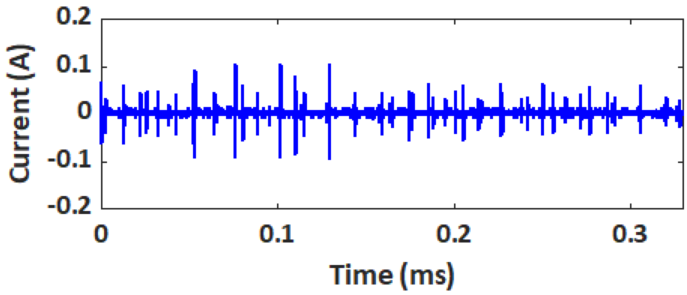


Fig. 4-39 CM current at the power supply connection of the control board with isolated power supplies.

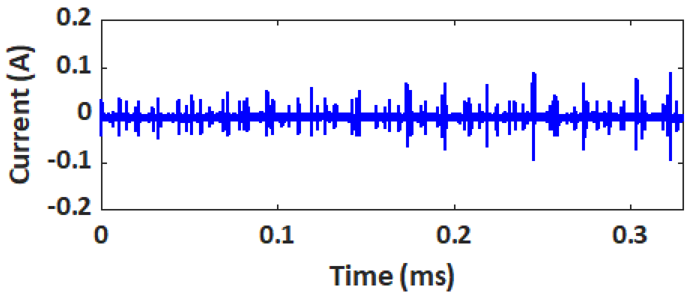
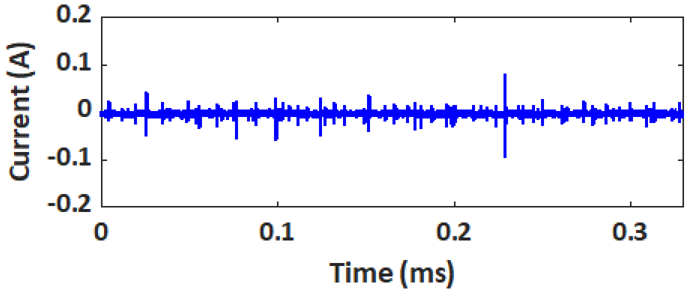


Fig. 4-40 CM current at the power supply connection of the control board with isolated power supplies and digital isolators.

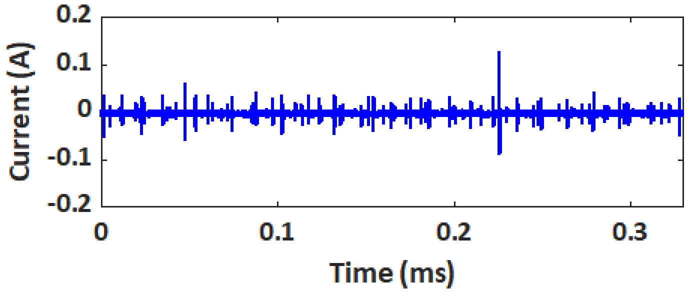
The CM currents in Fig. 4-38, Fig. 4-39, Fig. 4-40 were measured in separate tests and may not be aligned with each other. However, the effectiveness of the isolated power supplies and digital isolators on suppressing the conducted EMI disturbance through the control board can be clearly observed.

At the same time, the CM current at the power supply connection of the inverter board is measured with the second and the third configuration. The measured CM current is shown for one line cycle in Fig. 4-41.

The peak-to-peak value of the CM current is 176 mA with isolated power supplies at the control board, and 218 mA with isolated power supplies and digital isolators at the control board. Although the additional digital isolators further reduce the CM current at the control board, they increase the CM current at the inverter board.



(a) With isolated power supplies at the control board



(b) With isolated power supplies and digital isolators at the control board

Fig. 4-41 CM current at the power supply connection of the inverter board.

In the prototype, the current sensing feedback signals are not connected back to the control board. Therefore, the gate driving circuits for the switching devices, as well as the associated signal paths and auxiliary power paths, are the main EMI noise sources and propagation paths.

For each driving circuit, the voltage potential of the source terminal of the switching device compared to the converter negative dc bus changes with the switching states of the phase leg. The seven used switching states of a five-level SMC phase leg is shown in Tab. 2-5. The switching device source terminal voltage potentials compared to the converter negative dc bus for all the devices at all switching states are listed in Tab. 4-4 and Tab. 4-5.

As can be observed, the device source terminal voltage potentials change with the switching actions of the switching devices. However, the relationship is quite different for different switches. The source terminal voltage potential of the inner cell bottom switch S_{1-2} is constant. The source terminal voltage potentials of the inner cell middle switches $\overline{S_{1-1}}$, $\overline{S_{1-2}}$ are the same, and they only change with the states of the inner cell bottom switching pair. But the source terminal voltage potentials of the other switches are dependent on the states of multiple switch pairs.

Tab. 4-4 Switching device source terminal voltage potentials in an inner cell of a five-level SMC phase leg.

Switching Sates	S_{1-1}	$\overline{S_{1-1}}$	S_{1-2}	$\overline{S_{1-2}}$
1	V_{dc}	$V_{dc}/2$	0	$V_{dc}/2$
2	V_{dc}	$V_{dc}/2$	0	$V_{dc}/2$
3	$3V_{dc}/4$	$V_{dc}/2$	0	$V_{dc}/2$
4	$3V_{dc}/4$	$V_{dc}/2$	0	$V_{dc}/2$
5	$3V_{dc}/4$	$V_{dc}/2$	0	$V_{dc}/2$
6	$V_{dc}/2$	$V_{dc}/4$	0	$V_{dc}/4$
7	$V_{dc}/2$	$V_{dc}/4$	0	$V_{dc}/4$

Tab. 4-5 Switching device source terminal voltage potentials in an outer cell of a five-level SMC phase leg.

Switching Sates	S_{2-1}	$\overline{S_{2-1}}$	S_{2-2}	$\overline{S_{2-2}}$
1	V_{dc}	$3V_{dc}/4$	$V_{dc}/2$	$3V_{dc}/4$
2	$3V_{dc}/4$	$3V_{dc}/4$	$V_{dc}/2$	$3V_{dc}/4$
3	$3V_{dc}/4$	$V_{dc}/2$	$V_{dc}/4$	$V_{dc}/2$
4	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/4$	$V_{dc}/2$
5	$V_{dc}/4$	$V_{dc}/4$	$V_{dc}/4$	$V_{dc}/4$
6	$V_{dc}/4$	$V_{dc}/4$	0	$V_{dc}/4$
7	0	0	0	0

In the designed prototype, before adding digital isolators, the electrical gate signals on the primary sides of the gate driver chips [223] all share the same ground, which is the ground of the control board. Then the fast and frequent voltage change on the secondary sides of the gate driver chips introduce CM currents through the coupling capacitors of the gate driver chips, and to the control board, as measured in Fig. 4-38, Fig. 4-39, and Fig. 4-40.

Another type of propagation paths is through the isolated power supplies [224] for the driving circuits. Like the gate driver chips, the primary sides of the isolated power supplies share the same ground, which is the negative rail of the benchtop power supply; the voltages on the secondary sides change with the source terminal voltage potentials of the corresponding switches. The fast and frequent voltage changes introduce CM currents through the coupling capacitors of the isolated power supplies, and to the inverter board auxiliary power input connection, as measured in Fig. 4-41.

An equivalent circuit for the CM EMI emission is shown in Fig. 4-42.

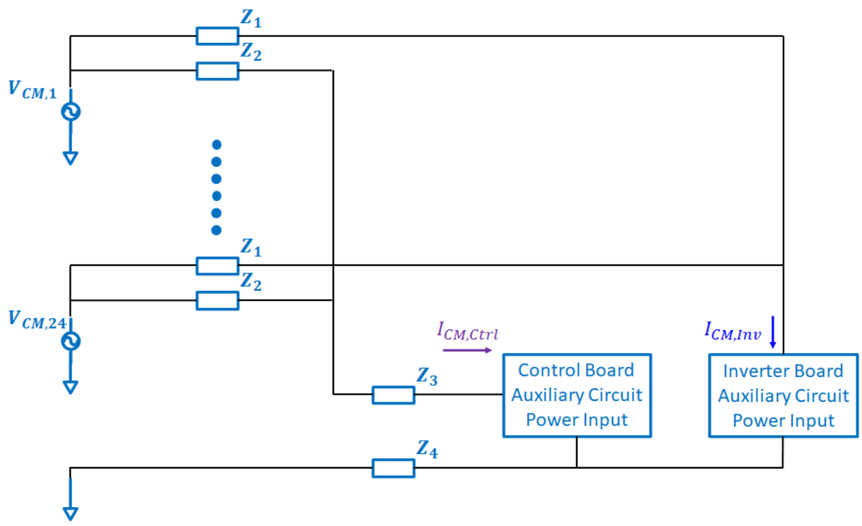


Fig. 4-42 CM EMI emission equivalent circuit for the auxiliary system of the SMC prototype.

There are twenty-four CM voltage sources, corresponding to the twenty-four switching devices in the three-phase prototype. The voltages of the sources may change with the switching states, as listed in Tab. 4-4 and Tab. 4-5. For each CM voltage source, there are two propagation paths: one through the isolated power supply, the impedance of which is represented by Z_1; the other through the gate driver chip, the impedance of which is represented by Z_2. The total CM current through the isolated power supplies is the CM current at the at the power supply connection of the inverter board, as measured in Fig. 4-41. The total CM current through the gate driver chips is the CM current at the power supply connection of the control board, as measured in Fig. 4-38, Fig. 4-39, and Fig. 4-40. When two additional isolated power supplies are connected between the benchtop power supply and the control board, the total impedance of the two isolated power supplies is represented by Z_3. The input voltages to the control board and to the auxiliary circuit of the inverter board can be considered to have the same CM voltage. Z_4 represents the impedances between the benchtop low-voltage power supply output and the high-voltage power supply output, which connects to the converter dc bus. Z_4 is contributed by the impedance of the two power supplies, as well as their input and output connections.

Based on the superposition theorem, it can be concluded that each voltage source contributes to the total CM currents in the same way. The currents can be solved as:

$$I_{CM,Ctrl} = \frac{1}{\frac{(23Z_1 + 24Z_4)}{Z_1}Z_2 + \frac{552Z_1Z_3 + 552Z_1Z_4 + 576Z_3Z_4}{23Z_1}} \times \sum_{i=1}^{24} V_{CM,i} \tag{4-14}$$

$$I_{CM,Inv} = \frac{1}{(23Z_1 + 24Z_4) + \frac{552Z_1Z_4}{23Z_2 + 24Z_3}} \times \sum_{i=1}^{24} V_{CM,i} \tag{4-15}$$

Equation (4-14) describes the total CM current at the power supply connection of the control board. Adding isolated power supplies means adding the impedance of Z_3, adding digital isolators means increasing the impedance of Z_2, both leading to the reduction of the CM current at the control board.

Equation (4-15) describes the total CM current at the power supply connection of the inverter board. Adding digital isolators means increasing the impedance of Z_2, leading to the increase of the CM current at the inverter board.

In the auxiliary circuit, although the signal paths are usually more sensitive and have higher priorities compared to the power paths [225], it is not desired that reducing the CM currents at some paths comes with the price of increasing the CM currents at other paths. Therefore, compared to the original configuration, two series-connected isolated power supplies are added to the power supply connection at the control board, one isolated power supply of the same kind is added to the auxiliary power supply connection at the inverter board. Therefore, the total CM currents at both the control board and the inverter board can be mitigated.

The digital isolators can further reduce the CM currents at the control board. It should be especially effective because it mitigates the CM current at each channel of the propagation path instead of only mitigates the total CM current. However, as discussed in Section 2.4.3, any timing discrepancy in the gate signals may add to the flying capacitor voltage unbalances. The use of digital isolators may contribute to more timing discrepancy in different channels of gate signals. Therefore, the digital isolators are not used.

Like digital isolators, optical transceivers and optical fiber cables can be used to improve the isolation of signals on the control board from the EMI noise sources. It could eliminate the coupling at the signal paths, and is commonly used in SiC-based MV converters. However, the delay of optical transceivers needs to be considered in some of the topologies or operations.

4.6 Summary

The conducted EMI disturbance is evaluated and mitigated in four SiC-based multilevel converters.

In the first case, the focus is on the conducted EMI emission at the ac input of the power circuit in a UPS system. There is a specific way for the measurement and there are specific limits, both defined in the international standard. An EMI test environment is established, and the EMI disturbance is compared with different operation conditions.

Small voltage steps and large number of switching states of multilevel converters topologies provide the flexibility to reduce the CM voltage generation of the rectifier stage, the inverter stage and the dc-dc stage, and consequently the EMI disturbance. Specifically, the synchronized operation of the dc-dc stage reduces the disturbance voltage by around 10 dB from 1 MHz to 7 MHz and the SCMVP modulation of the rectifier and inverter stage reduces the disturbance voltage by 5~15 dB at the multiples of the switching frequency.

Different operation modes could affect noise generation and noise propagation. Specifically, the charging mode, which is identified as the worst case, changes the propagation path impedance. As a result, the disturbance voltage increases by 5~30 dB from 8 MHz to 25 MHz compared to the normal operation, even without any additional CM voltage generation. Different power distribution during the charging mode does not have significant impact.

The designed EMI filters effectively attenuate the disturbance to meet the limits defined in IEC 62040-2.

In the next three cases, the focus is on the conducted EMI emission in different auxiliary ports or paths, instead of the power ports. There are no specifically defined ways for evaluation or specifically defined limits to meet. However, the EMI emission in the auxiliary systems is also critical to ensure the functionalities of the converters, especially in SiC-based converters.

In the second case, the focus is on the conducted EMI emission in the control system in a PEBB-based MMC prototype built with SiC MOSFETs. Each PEBB is individually verified but the converter could not maintain correct functions in high voltage tests.

As suggested by the CM currents measurement, the voltage sensing paths are identified as the critical EMI propagation paths. The EMI noise sources, which are the CM voltages of cell capacitors, change with the switching actions of the switching devices. Each cell capacitor CM voltage is mainly decided by one switch pair in the same PEBB, but is also affected by the other three switch pairs in the same phase leg, and is slightly affected by the other eight switch pairs in different phase legs. CM currents are generated as a result of the fast and frequent CM voltage changes and the coupling capacitors of the voltage sensors. The CM currents, together with other impedances in the digital control system, affect the sensing feedback signals at the control board inputs.

CM chokes are built and placed at the voltage sensing paths. They effectively suppress the CM currents. The converter is able to operate at the rated voltages without falsely triggered protection.

In this PEBB-based multilevel converter, six PEBBs lead to six main EMI noise sources and six critical EMI propagation paths. Each noise source is affected by multiple switch pairs.

Some components in the CM currents circulate within different channels of sources and paths. Therefore, it is more effective to mitigate the EMI emission at each channel instead of mitigating the total EMI emission. Despite the modular structure of the converter, the EMI emission does not inherent the modularity.

In the third case, the focus is on the conducted EMI emission in the control system and in the auxiliary power system in a modular MV converter with ICBT cells.

The configuration of the voltage sensing circuit is significantly changed to minimize the EMI noise generation and minimize the EMI noise propagation.

However, the WPT of the auxiliary systems is exposed to the fast and frequent CM voltage changes of the cell capacitors. The CM voltages of different cell capacitors are different, and could be the dependent on the switching actions of multiple cells. The CM current is effectively attenuated by adding chokes and by applying minimum delays to the cells in the same arm.

In the fourth case, the focus is on the conducted EMI emission in the auxiliary system in a five-level SMC built with SiC MOSFETs.

In this converter prototype, the gate driving circuits, as well as the associated signal paths and auxiliary power paths, are the main EMI noise sources and propagation paths. The device source terminal voltage potentials change with the switching actions of the switching devices. With the large number of switching devices in this five-level converter, the device source terminal voltage potentials of different devices are quite different, and could be dependent on the state of multiple switch pairs.

The voltage changes at the device source terminals introduce CM currents to the control board through the coupling capacitors of the gate driver chips, and may affect the correct functions of the control board. With the original configuration, the EMC completely relies on the isolation performance of the gate driver chips, and the transient immunity of the gate driver chips and the control board. Adding isolated power supplies and digital isolators are both effective ways to suppress the EMI disturbance in the control board.

The voltage changes at the device source terminals also introduce CM currents to the auxiliary power input of the inverter board through the coupling capacitors of the isolated power supplies for the driving circuits.

It is found that when reducing the CM currents at some paths, the CM currents at other paths may increase. Therefore, all propagation paths need to be considered while prioritizing the more sensitive paths.

Chapter 5. Conclusions and Future Work

This works studies the design, control and EMI mitigation of multilevel converters using SiC MOSFETs.

A SiC-based five-level SMC is designed for high-speed motor drive applications. With this design, there is no need for additional filters. The converter output quality is good enough thanks to the high output quality feature of the five-level topology and the high switching frequency capability of SiC MOSFETs. The voltage reflection over-voltage is low enough thanks to the small voltage steps of the five-level topology. Therefore, the design not only achieves a high efficiency of the inverter, but also eliminates the losses and sizes of the filters.

SiC MOSFETs provide high switching frequency operation and low losses. The potential problems of SiC MOSFETs are mitigated in different ways. Both the high switching speed and high switching frequency of SiC MOSFETs increase the magnitude of the voltage reflection over-voltage. It is mitigated by the small voltage steps of five-level topology. Then the layout is designed while minimizing driving loops, minimizing commutation loops, and minimizing coupling between power circuits and auxiliary circuits.

Although different five-level topologies have the same output voltages, some of them have long commutation loops while the others only have short commutation loops. The long commutation loops should be avoided when using SiC MOSFETs and should be considered during the topology selection. The capacitor voltage natural balancing is a common feature in multilevel converters, but its performance is found to be not good with the non-idealities in the converter and the high frequency operation of SiC MOSFETs. Highly accurate control or a closed-loop capacitor control is required.

Then the operation and control of converters with ICBT cells are studied. ICBT-based converters have the structure similar as MMCs, but the operation similar as series-connected switching devices. Compared to MMCs, ICBT-based converters retain the advantages of devices blocking cell capacitor voltages, modularity, and scalability. ICBT cells enable direct power transfer, therefore avoid the issue of large cell capacitor voltage ripples, and can operate in both ac and dc operation modes. The size and loss of the arm inductors are eliminated in ICBT-based converters. Compared to series-connected switching devices, ICBT-based converters retain the advantage of simple control principle. An ICBT cell operates as a single switching device, series-connected ICBT cells operate as an equivalently high-voltage device. ICBT-based converters avoid the issue of large voltage unbalance. The voltage unbalance develops much slower and is much easier to control.

Low parasitic inductance in the arm is key to achieve ideal ICBT operation. If the inductance value is not low enough, it will lead to significant current oscillation in the arms, increasing semiconductor losses and cell capacitor voltage offsets. It is more critical with a high switching frequency of SiC MOSFETs.

The existence of parasitic capacitors and the difference among gate signal are two factors that may interrupt the cell capacitor voltage balance. Their impacts are both more significant with the high switching speeds of SiC MOSFETs. The parasitic capacitors around the device terminal not only contribute to the EMI emission, but also contribute to cell capacitor voltage unbalance. Both factors should be mitigated but a closed-loop control is required.

A two-level control method is proposed for ICBT-based converters to generate desired outputs and regulate cell capacitor voltages. It is easy to implement and scalable with different number of cells in the arm.

The operation and control of ICBT-based converters are experimentally verified with a modular MV converter built with 10 kV SiC MOSFETs. The number of cells is less and the control is simpler with the high voltage of SiC MOSFETs. The ICBT-based converters are verified to achieve low cell capacitor voltage ripples and excellent voltage balance in Medium Voltage high power applications in both dc and ac operation modes.

The conducted EMI disturbance in four SiC-based multilevel converters are studied. The EMI disturbances at the power circuit and at the auxiliary circuit are both critical to ensure the desired functions of the converters. With large number of switching devices and capacitors, both the noise generation and propagation are complex in multilevel converters, which brings both opportunities and challenges.

In the first case, the focus is on the conducted EMI emission at the ac input of the power circuit in a UPS system. Small voltage steps and large number of switching states of multilevel converters topologies provide the flexibility to reduce the CM voltage generation of the rectifier stage, the inverter stage, and the dc-dc stage, and consequently the EMI disturbance. The EMI disturbance can be reduced by reducing the noise source, through topology selection and modulation method selection, and by increasing the impedance of the propagation path, through EMI filters. The noise disturbance can also be affected by the converter operation modes or conditions.

In the next three cases, the focus is on the conducted EMI emission in different auxiliary ports or paths. The CM voltage changes of the switching devices or capacitors are the main noise sources. The larger number of switching devices and capacitors in the multilevel converters leads to large number of noise sources and propagation paths Moreover, different noise sources could have very different profiles, and each noise source could be affected by the actions of multiple switch pairs.

The signal and power circuits for the gate driving and sensing are the main coupling paths in the auxiliary circuits. It is found that some components in the CM currents circulate within different channels of sources and paths. Therefore, it is more effective to mitigate the EMI emission at each channel instead of mitigating the total EMI emission. It is found that when reducing the CM currents at some paths, the CM currents at other paths may increase. Therefore, all propagation paths need to be considered while prioritizing the more sensitive paths.

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