Bidirectional DC-DC Power Converter
Design Optimization, Modeling and Control

by

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ABSTRACT

In order to increase the power density, the discontinuous conducting mode (DCM) and small inductance is adopted for high power bidirectional dc-dc converter. The DCM related current ripple is minimized with multiphase interleaved operation. The turn-off loss caused by the DCM induced high peak current is reduced by snubber capacitor. The energy stored in the capacitor needs to be discharged before device is turned on. A complementary gating signal control scheme is employed to turn on the non-active switch helping discharge the capacitor and diverting the current into the anti-paralleled diode of the active switch. This realizes the zero voltage resonant transition (ZVRT) of main switches. This scheme also eliminates the parasitic ringing in inductor current.

This work proposes an inductance and snubber capacitor optimization methodology. The inductor volume index and the inductor valley current are suggested as the optimization method for small volume and the realization of ZVRT. The proposed capacitance optimization method is based on a series of experiments for minimum overall switching loss. According to the suggested design optimization, a high power density hardware prototype is constructed and tested. The experimental results are provided, and the proposed design approach is verified.

In this dissertation, a general-purposed power stage model is proposed based on complementary gating signal control scheme and derived with space-state averaging method. The model features a third-order system, from which a second-order model with resistive load on one side can be derived and a first-order model with a voltage source on both sides can be derived. This model sets up a basis for the unified controller design and optimization. The Δ-type model of coupled inductor is introduced and simplified to

provide a more clearly physical meaning for design and dynamic analysis. These models have been validated by the Simplis ac analysis simulation.

For power flow control, a unified controller concept is proposed based on the derived general-purposed power stage model. The proposed unified controller enables smooth bidirectional current flow. Controller is implemented with digital signal processing (DSP) for experimental verification. The inductor current is selected as feedback signal in resistive load, and the output current is selected as feedback signal in battery load.

Load step and power flow step control tests are conducted for resistive load and battery load separately. The results indicate that the selected sensing signal can produce an accurate and fast enough feedback signal. Experimental results show that the transition between charging and discharging is very smooth, and there is no overshoot or undershoot transient. It presents a seamless transition for bidirectional current flow. The smooth transition should be attributed to the use of the complementary gating signal control scheme and the proposed unified controller. System simulations are made, and the results are provided. The test results have a good agreement with system simulation results, and the unified controller performs as expected.

To my parents

Xuewen Zhang and Baoshan Chen

To my husband and son

Hongfang Wang and Tyler Wang

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Chapter 1 Introduction

1.1 Background

The bidirectional dc-dc converter along with energy storage has become a promising option for many power related systems, including hybrid vehicle [1], fuel cell vehicle, renewable energy system and so forth. It not only reduces the cost and improves efficiency, but also improves the performance of the system.

In the electric vehicle applications, an auxiliary energy storage battery absorbs the regenerated energy fed back by the electric machine. In addition, bidirectional dc-dc converter shown in Figure 1.1 is also required to draw power from the auxiliary battery to boost the high-voltage bus during vehicle starting, accelerate and hill climbing [1]. With its ability to reverse the direction of the current flow, and thereby power, the bi-directional dc-dc converters are being increasingly used to achieve power transfer between two dc power sources in either direction.

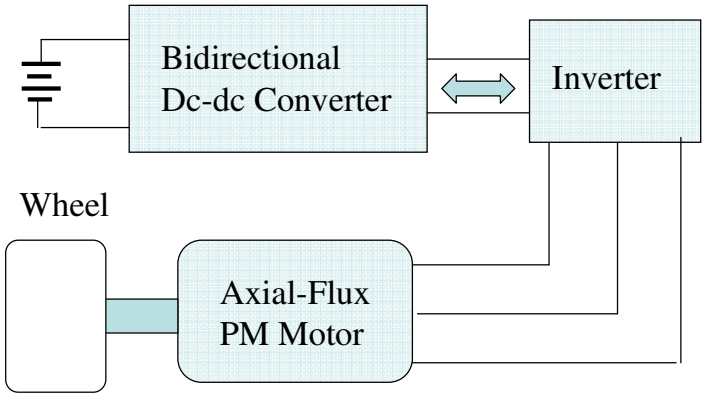


Figure 1.1 Bidirectional dc-dc converter in energy regenerative system

In renewable energy applications, the multiple-input bidirectional dc-dc converter can be used to combine different types of energy sources [2-8]. Figure 1.2 shows a fuel cell based system for domestic applications [2]. The multi-input bidirectional dc-dc converter is the core that interconnects power sources and storage elements and manages the power

flow [5]. This bidirectional dc-dc converter features galvanic isolation between the load and the fuel cell, bidirectional power flow, capability to match different voltage levels [9], fast response to the transient load demand, etc.

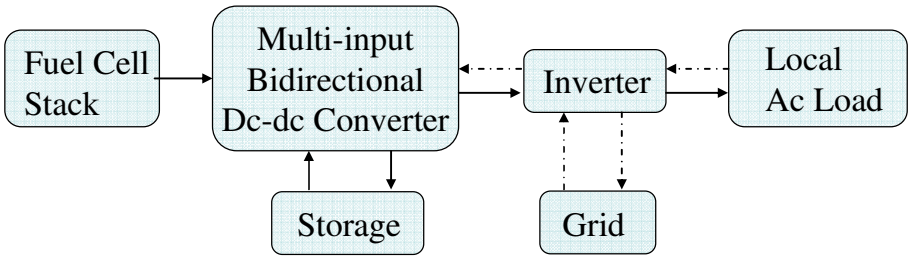


Figure 1.2 A fuel cell system for domestic applications

Recently, clean energy resources such as photovoltaic arrays and wind turbines have been exploited for developing renewable electric power generation systems. The bidirectional dc-dc converter is often used to transfer the solar energy to the capacitive energy source during the sunny time, while to deliver energy to the load when the dc bus voltage is low [9]. A photovoltaic power system with bidirectional converter is shown in Figure 1.3. The bidirectional dc-dc converter is regulated by the solar array photovoltaic level, thus to maintain a stable load bus voltage and make fully usage of the solar array and the storage battery.

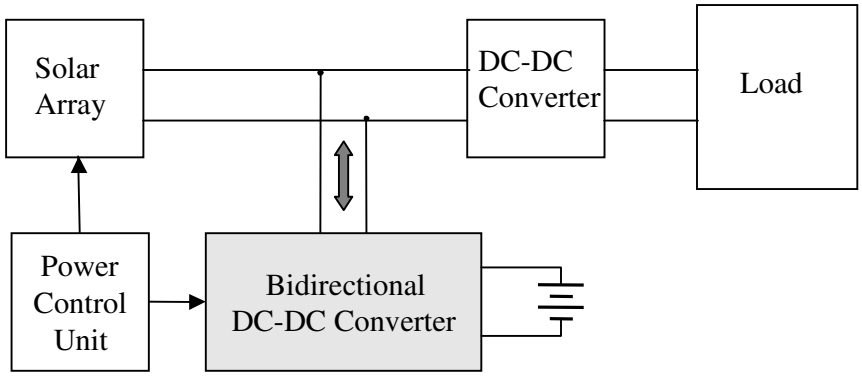


Figure 1.3 Bidirectional dc-dc converter in solar cell photovoltaic power system

In this dissertation, a background description and review of the state-of-the-art bidirectional dc-dc converters are presented firstly to define this work and its novelty. Then, the challenges will be identified related to the design and control issues in the

present non-isolated bidirectional dc-dc power converter. The improved system is proposed with the advantages of high efficiency, simple circuit and low cost. The detailed design and operation considerations are analyzed and described. A unified power stage model is investigated and developed. A novel unified controller is proposed and digitally implemented with the digital signal processor (DSP). The proposed controller provides a freely power flow control in both directions. Simulation results from the proposed circuit are given to verify the operation principles. A laboratory prototype is also implemented and tested to demonstrate its bidirectional power smooth flow capability.

1.2 State-of-the-art Bidirectional DC-DC Converters

1.2.1 Introduction to Bidirectional DC-DC Converters

Most of the existing bidirectional dc-dc converters fall into the generic circuit structure illustrated in Figure 1.4, which is characterized by a current fed or voltage fed on one side [10]-[14]. Based on the placement of the auxiliary energy storage, the bidirectional dc-dc converter can be categorized into buck and boost type. The buck type is to have energy storage placed on the high voltage side, and the boost type is to have it placed on the low voltage side.

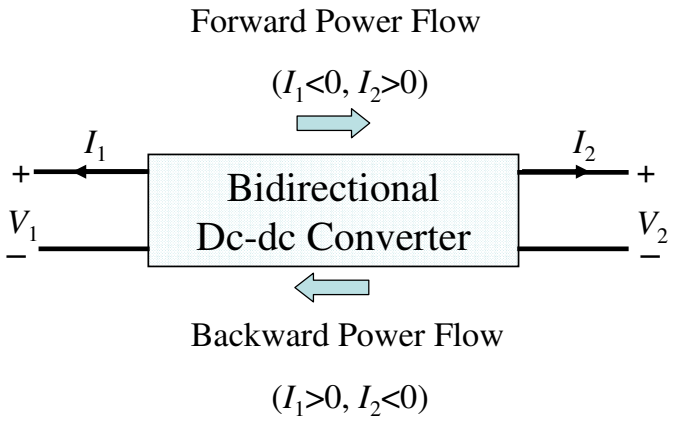


Figure 1.4 Illustration of bidirectional power flow

To realize the double sided power flow in bidirectional dc-dc converters, the switch cell should carry the current on both directions. It is usually implemented with a

unidirectional semiconductor power switch such as power MOSFET (Metal-Oxide-Semiconductor-Field-Effect-Transistor) or IGBT (Insulated Gate Bipolar Transistor) in parallel with a diode, because the double sided current flow power switch is not available. For the buck and boost dc-dc type converters, the bidirectional power flow is realized by replacing the switch and diode with the double sided current switch cell shown in Figure 1.5 [12].

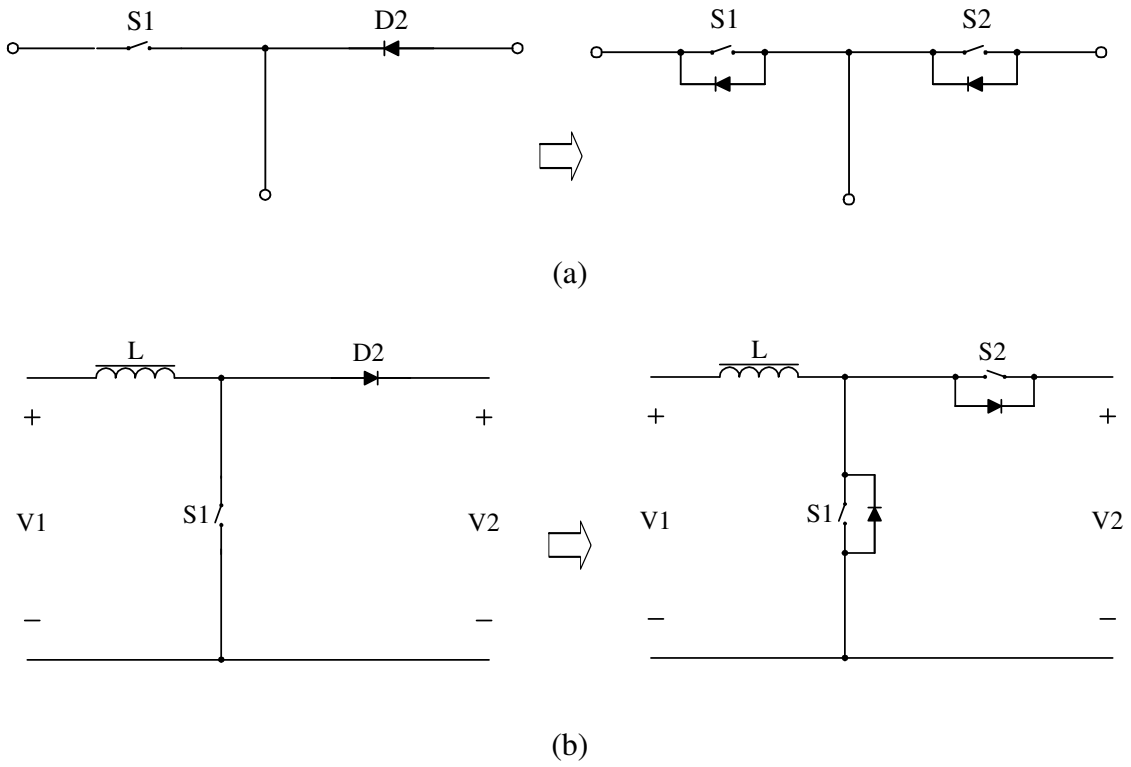


Figure 1.5 Switch cell in bidirectional dc-dc converter

Numerous topologies for possible implementation as bidirectional dc-dc converters have been reported so far [15-37]. Basically they are divided into two types, non-isolated and isolated converters, meeting different application requirements.

1.2.2 Non-isolated Bidirectional DC-DC Converters

In the transformer-less non-isolated power conversion systems, the boost type and buck type dc-dc converter are chosen usually.

The high frequency transformer based system is an attractive one to obtain isolation between the source and load sides. But from the viewpoint of improving the efficiency, size, weight and cost, the transformer-less type is much more attractive. Thus, in the high power or spacecraft power system applications [7, 17, 20, 39-47], where weight or size is the main concern, the transformer-less type is more attractive in high power applications.

The basic non-isolated bidirectional dc-dc converter topology shown in Figure 1.6 is the combination of a step-up stage together with a step-down stage connected in anti-parallel [45]. For the motor drive operations the converter step-up stage is used to step up the battery voltage and control the inverter input. The vehicle regenerative braking is accomplished by using the converter step-down stage, which gives a path for the braking current and allows the recovery of the vehicle energy in the battery.

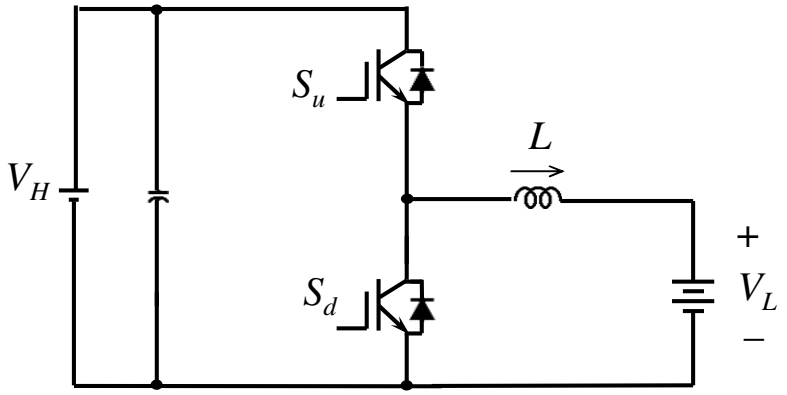


Figure 1.6 Basic bidirectional dc-dc converter with buck and boost structure

For the present high power density bidirectional dc-dc converter, to increase its power density, multiphase current interleaving technology with minimized inductance has been found in high power applications [38, 42]. It is reported that multiphase converter circuits have shown the advantage of less device current stress and better efficiency. A three-phase bidirectional dc-dc converter is shown in Figure 1.7, where the phase switch is controlled with 120-degree phase shift from each other. The ripple on the total current will become relatively small, so a small capacitance is enough in both low and high sides for acceptable voltage ripple.

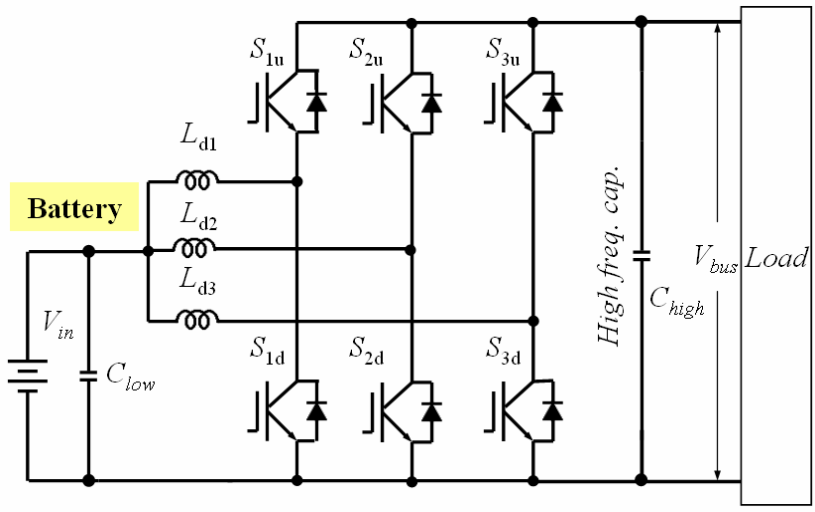


Figure 1.7 A high power density non-isolated interleaved bidirectional dc-dc converter

1.2.3 Isolated Bidirectional DC-DC Converters

In the bidirectional dc-dc converters, isolation is normally provided by a transformer. The added transformer implies additional cost and losses [1]. However, since transformer can isolate the two voltage sources and provide the impedance matching between them, it is an alternative in those kinds of applications. As a current source, inductance is normally needed in between. For the isolated bidirectional dc-dc converters, sub-topology can be a full-bridge, a half-bridge, a push-pull circuit, or their variations [25, 27-30].

One kind of isolated bidirectional dc-dc converter is based on the half-bridge in the primary side and on the current fed push-pull in the secondary of a high frequency isolation transformer [48]. The converter operation is described for both modes; in the presence of dc bus the battery is being charged, and in the absence of the dc bus the battery supplies power. This converter is well suited for battery charging and discharging circuits in dc uninterruptible power supply (UPS). Advantages of this proposed converter topology include galvanic isolation between the two dc sources using a single transformer, low parts count with the use of same power components for power flow in either direction.

The dual active bridge dc-dc converter with a voltage-fed bridge on each side of the isolation transformer operates utilization of the leakage inductance of the transformer as

the main energy storing and transferring element to deliver bidirectional flow power [23], [49-50].

In summary, for the isolated bidirectional dc-dc converter, the operation of the circuit involves the utilization of the leakage inductance of the transformer as the main energy storing and transferring element. The half-bridge based topologies have been developed so far to reduce the device count and increase efficiency [3, 28, 31, 49]. However a voltage imbalance exists between the two split capacitors, thus an additional control circuit to eliminate the voltage imbalance problem is required. The full-bridge bidirectional dc-dc converter shown in Figure 1.8 is considered one of the best choices. However, this system has a complicated configuration, high cost and large size.

1.2.4 Soft-switching Techniques in Bidirectional DC-DC Converters

The efficiency is one of the needed performances for many bidirectional dc-dc converter applications. To improve the efficiency many advanced power conversion techniques such as resonant and soft-switching can be implemented in the power stage [6, 12-13, 38-39, 42, 44, 52-73].

A bidirectional dual full-bridge dc-dc converter has been developed with a unified soft switching scheme and soft start capability shown in Figure 1.8 [71]. The bridge on one side, preferably the lower voltage side, is current-fed, while that on the other side is voltage fed. A simple voltage clamp branch, which is composed of an active switch with its anti-paralleled diode and a capacitive energy storage element in series, is placed across the current-fed bridge to limit transient voltage across the current-fed bridge and realize zero-voltage-switching in boost mode operation, while achieving hybrid zero-voltage zero-current switching (ZVZCS) for the voltage-fed bridge in buck mode operation. In buck mode operation, the voltage-fed bridge is controlled by the well-known phase shift pulse width modulation (PWM). The clamping branch is activated only briefly each time after an on duty cycle is executed and the on-time of the clamp switch is just long enough to reset the transformer leakage current to zero and achieve ZVZCS operation even under maximum load current.

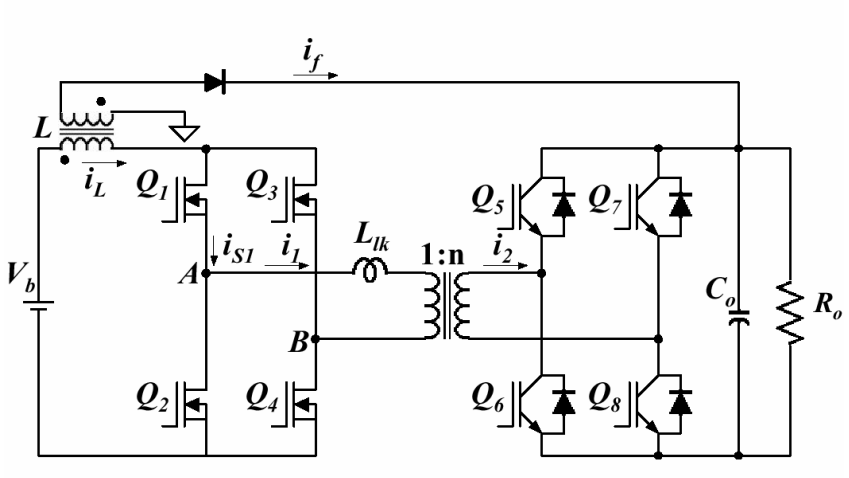


Figure 1.8 A bidirectional full-bridge dc-dc converter with unified soft- switching scheme

1.3 State-of-the-art Bidirectional DC-DC Converter Modeling and Control

(1) Traditional Method without Mode Transition Consideration

Many controller schemes have been discussed for bidirectional dc-dc converter applications. Most designs follow the unidirectional dc-dc controller methodology [41, 43, 45, 74] because there are different circuits topological changes and associated operating principles involved in the two power flow directions. Normally, two independent controllers are needed for battery charging and discharging respectively [45, 92]. No mode transition discussion has been addressed since the power management is normally not included in the design. More efforts are needed for smooth mode transition. Otherwise the transition will cause large current or voltage stress on device, which will be mentioned in Chapter 5.

One example of dealing with smooth mode transition is shown in Figure 1.9 [43]. This is a regulated bus system for the spacecraft power system application. The major effort in this system is to study the trajectories of the system operating point, which are determined according to the stability nature of the equilibrium points for the optimum performance and stability of the system. This type of study tends to complicate the design and reduce the system reliability.

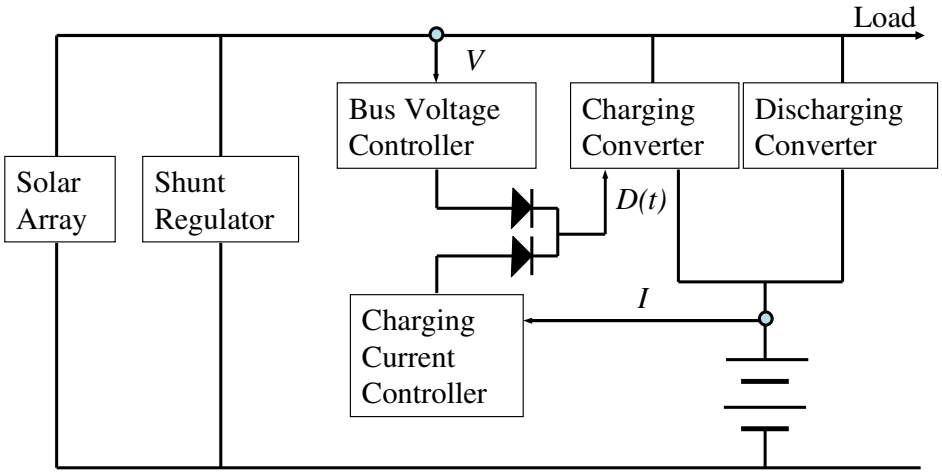


Figure 1.9 Block diagram of regulated bus system

For example, the starting operation point is from point A in Figure 1.10 for sunlight to eclipse transition. As illumination level decreases, the solar array current decreases. The shunt regulator current then decreases to regulate the bus voltage. As soon as the shunt current reaches zero, bus voltage drops rapidly. This is the dead band mode. According to the preset value, the bus voltage will be regulated by the battery discharger. Between the equilibrium points C and D, there is a dead band, which is to avoid undesired overlapping operation. Transient behavior during the dead band mode depends on the circuit parameters including bus capacitor, cable inductance and the transconductance gain of the battery discharger. The preset bus voltage value is needed to trigger the battery discharger for bus voltage regulation. Plus the transient behavior is sensitive to circuit parameters. It is not easy to predict.

(2) Bidirectional DC-DC Power Stage Modeling and Control

Some researchers [31, 51, 72] developed a switch frequency-dependable average method to estimate the system performance at different switching frequencies. This is an extended state-space averaging model and is developed to predict large- and small-signal characteristics of the converter in either direction power flow. The model is especially designed for isolated one.

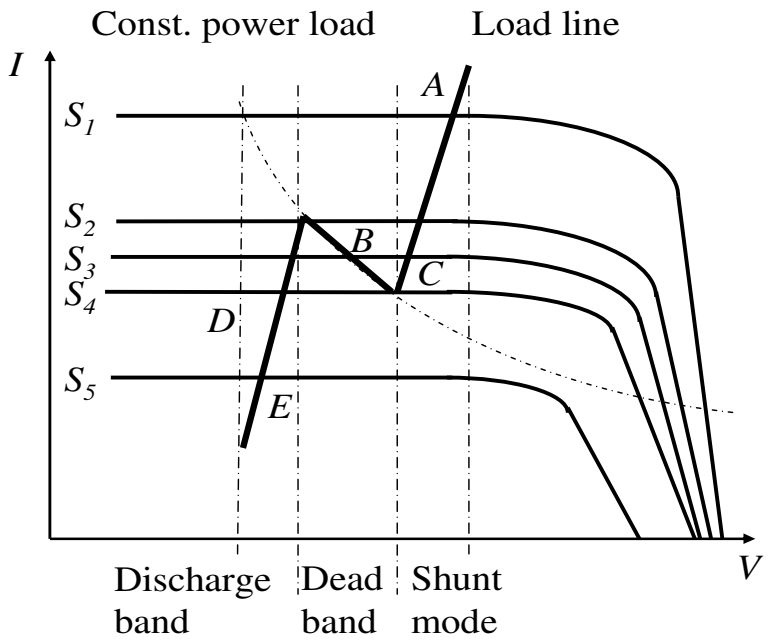


Figure 1.10 Graphical analysis of sunlight to eclipse transition

A digital controller was built after non-linear dynamic model of the converter was derived using a state space averaging method in [8, 75]. Although it utilized the simplified power stage model with the traditional modeling approach, it did claim to handle seamless bidirectional operation. In fact, to design a seamless bidirectional power flow control, more generalized power stage model is needed.

Based on ref [43], an analog current-injection-control in multiphase was implemented in [44, 65, 76, 93]. One error amplifier was used for the spacecraft bus voltage regulation with internal peak current mode control. After careful analysis of the feature of the two modes (bus voltage regulation mode with charging and discharging mode), a sub-optimal controller was proposed for the regulation of the two mode operations. It was expected to reduce the overall system weight. Since the application was focused on the spacecraft power system, no more average current control for both directions was addressed.

1.4 Research Challenges and Proposed Solutions

1.4.1 DCM Operation Related Issues

The non-isolated, multiphase bidirectional dc-dc power converter has been selected to achieve high power density in this dissertation. Usually, to increase the power density, the design adopts small inductor with multiphase to operate in discontinuous conduction mode (DCM). The problem with DCM operation as shown in Figure 1.11 is the related parasitic ringing caused by the inductor and the device output capacitance during current turn-off condition, resulting poor efficiency and significant EMI noises [41]. The disadvantages related to the DCM are: (a) inductor voltage parasitic ringing, (b) hard switching turn-off and increased turn-off loss.

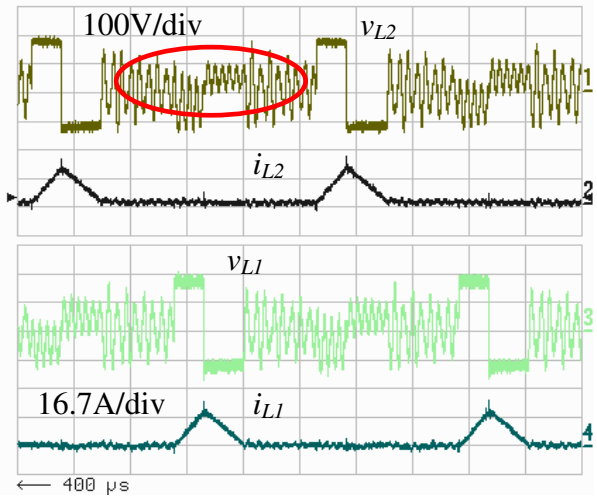


Figure 1.11 Inductor voltage parasitic ringing at DCM operation

The novel technique is to add a lossless snubber capacitor across each switch [38] for soft turn-off and to use complementary gating signal control scheme to realize ZVRT for soft turn-on, thus achieving both soft turn-on and -off. This means after fully discharging the snubber capacitor energy the originally non-active switch diverts the current into the anti-paralleled diode of the active switch so that the main switch can turn on under zero-voltage condition. The detailed discussion of the scheme will be presented in chapter 2.

1.4.2 Power Stage Design and Optimization Related Challenges

Although the lossless capacitor snubber can be added across the switch for soft turn-off, it requires certain amount of energy stored in the inductor to discharge the capacitor energy before device is turned on. The questions are how much inductor current is needed, and how the zero-voltage condition can be guaranteed. The high temperature and high power inductor is also difficult to come by. This dissertation intends to answer these questions through theoretical derivation and empirical data.

1.4.3 General-purposed Power Stage Model Challenges

Power stage model is the basis of the theoretical analysis which leads to the unified controller design and optimization. Normally, transfer function of unidirectional power flow is well known. For bidirectional dc-dc converter, the power stage circuit not only allows the power flow in both directions, but also covers all different operating modes. In another words, different modes can be derived from this model. Thus their fundamental relationship between different operating modes can be established and analyzed. The question is what the bidirectional power stage circuit model can be used.

A power stage with two voltage sources, one on high side and another on low side, is proposed and three energy components, including two capacitors and one inductor, are employed.

1.4.4 Mode Transitions Related Issues in Bidirectional DC-DC Converter

The power flow smooth transition control of the bidirectional dc-dc converter is also quite challenged. Normally, three operating modes are required in inverter charger [75].

(a) wide range output voltage regulator for boost discharging mode

(b) wide range current regulation for buck charging mode

(c) wide range voltage regulation for absorb and float charging mode

Each mode requires a set of control parameters to ensure stability [43]. For electric vehicle, the power management also needs boost power discharging mode. During startup or acceleration, much power from the battery is needed for the motor driving. The power flow control may be employed for bidirectional dc-dc converter. Considering the

relatively constant bus voltage, power flow control also means current flow control. Therefore current regulator is needed for discharging mode. After such short time of large power consumption, the battery usually needs to be charged for the future power needs. Thus current regulator is also needed for battery charging modes. These two modes have different operation points and it is hard to generate a simple logic to realize smooth transition.

A complex decision process is quite difficult to be implemented with hardware. The proposed effort is to use a high-end digital signal processor for all the controller implementation and mode transition control. The digital solution will also help the current sharing between the modules to improve the dynamic performance, which has to be dealt with by peak current injection control (CIC) [44, 73] in analog system.

Unified controller is proposed to generate only one command instead of separate commands at the same time. When there is a demand of quick power flow from the system control unit, the battery can provide required power to the inverter. Once the vehicle reaches the steady speed, the energy management can switch to charge the battery immediately. The energy management can switch from discharging mode to battery charging mode immediately without the need of any intermediate mode. This unified controller is not a compromised design result and it is a design based on theoretical analysis of the generalized power stage model.

If the transition between these modes is fast and smooth enough to guarantee energy effectively transfer without causing system instability, this will improve the vehicle performance and save more effort for operation point selection.

1.5 Research Objectives and Outline

The research objectives are list as follows.

- Design an efficient bidirectional dc-dc converter and optimize the power stage components.
- Establish a general-purposed power stage model and the coupled inductor model.

- Design and implement a unified digital controller used for smooth bidirectional power flow control.
- Test with smooth bidirectional power flow control to validate the power stage modeling and the unified controller design.

The dissertation consists of six chapters, which are organized as follows.

Chapter 1 gives the detailed introduction of the research background. The main concern is the efficiency and reliability of bidirectional dc-dc converter. The various technologies, which can be involved to improve the efficiency in bidirectional dc-dc converter, are described and investigated. Soft-switching technology and the power stage topologies are the main contributions to the high-efficiency improvement. For high power electric vehicle application, the non-isolated multiphase interleaved bidirectional dc-dc is especially preferred for its high efficiency and low cost. There are many operating modes. The smooth mode transition between them and bidirectional power flow control are the basic requirements. At last, the research objectives are proposed.

In Chapter 2, characteristics and the operating principle of the non-isolated power stage with zero voltage resonant transition (ZVRT) soft-switching technology are depicted. The power stage inductance affects the inductor valley current, which is related to the realization of ZVRT, and the inductor peak current, which is related with volume index. Their relationship is discussed and the inductance is therefore optimized for both small volume to increase power density and ZVRT realization. The core material features are compared carefully for less core loss. The snubber capacitor, which is also the resonant capacitor, is selected at minimum overall switching loss through a series of experiments. The system power flow experiments are presented to verify the design results.

In Chapter 3, a general-purposed power stage averaged model is theoretically and systematically established, which is the foundation for unified controller design and optimization. The large signal dc model and small signal ac model expressions under different conditions are derived and discussed. For two voltage sources application, a simplified first-order ac model is given. The model is verified by the comparison of

Simplis simulation and the mathematic derivation. The coupled inductor is adopted to further improve the efficiency, and its model is also derived and validated.

In Chapter 4, a unified controller is designed based on the model set up in Chapter 3. It is expected to have the linear system characteristics and lead to smooth mode transition. Two possible sensing feedback signals, inductor current i_L and output current i_o are investigated in detailed. The designed unified controller is digitally implemented and the related design issues are discussed. Load step tests are conducted and the tests results are provided. Simulation results are also given and compared with experimental results.

In Chapter 5, a series of load step and bidirectional power flow control step experiments are presented and the related simulations are carried out for resistive load and battery load respectively. The related conditions and results for both simulation and experiment are provided. Both simulation and experiment results show that the smooth mode transition is achieved and unified controller works as expected. The steady and smooth mode transition is credited to the generalized power stage topology modeling and the sequent unified controller design and application.

In Chapter 6, conclusions and the future work are summarized.

Chapter 2 Power Stage Design and Optimization

2.1 Introduction

A typical non-isolated bidirectional dc-dc converter technology is to combine a buck converter and a boost converter in a half-bridge configuration. In order to achieve high power density, the converter can be designed to operate in discontinuous conducting mode (DCM) such that the passive inductor can be minimized. The DCM operation introduces a large current ripple, so it is necessary to interleave multiple phases to cancel the high-frequency switching current ripple [77, 78]. In this regard, a 36-phase interleaved converter has been reported in [79]. It is also possible to reduce the ripple with a coupled inductor approach [80]. Another major advantage of the DCM operation is zero turn-on loss and thus low diode reverse recovery loss. However, the DCM operation largely increases turn-off loss because the main switch is turned off at twice the load current or higher. This is the major negative side effect of the inductor size reduction. It also causes inductor current parasitic ringing [41] because the inductor tends to oscillate with the device output capacitance during device turn-off period. The efficiency can be suffered with all these side effects induced by the DCM.

Although the lossless capacitor snubber can be added across the switch for soft turn-off, it requires certain amount of energy stored in the inductor to discharge the capacitor energy before device is turned on. The question is how the zero-voltage condition can be achieved. The section 2.2 intends to answer the question with the use of a complementary gating signal control scheme to turn on the originally non-active switch and to divert the current into the anti-paralleled diode of the active switch so that the main switch can be turned on under zero-voltage condition. The soft switching operation can be considered a zero-voltage resonant transition (ZVRT) [20, 81, 82] switching technology. Thus both soft switching turn-on and -off are achieved. Because of the continuation of this diverted current, the inductor current parasitic ringing also disappears.

To realize ZVRT, inductance should be greater than a certain boundary value. Section 2.3.1 proposes a theoretical derivation method to optimize this value. When the insulated-gate-bipolar-transistor (IGBT) is used as the switching device, the lossless snubber cannot totally eliminate the turn-off loss because there is a tail current. A large-size snubber capacitor does not guarantee minimum loss because it requires large initial inductor current to discharge. Thus it is non-trivial to design the component values and switching timing such that the zero-voltage soft switching can be achieved while the turn-off loss is minimized. There is a design tradeoff between the turn-off loss and the inductor peak current. Section 2.3.3 suggests the optimization of capacitance selection through a series of hardware experiments to ensure the overall power loss is minimized under complementary DCM operating condition. To verify the proposed approach, a 100 kW hardware prototype has been constructed and tested, which will be covered in section 2.4. Experimental results are provided in section 2.5 to verify the proposed design approach.

2.2 Power Stage Topology and Operation Principle

2.2.1 Power Stage Topology

Figure 2.1 shows the proposed soft-switching bidirectional dc-dc circuit topology. A battery pack or other energy source such as ultra-capacitor is placed on the low-voltage side, and a primary energy source such as fuel cell or generator-set is placed on the high-voltage DC bus, which also contains a high-frequency capacitor as the energy buffer. The high-voltage DC bus also serves as the main power bus that provides power output to the main load which is typically an inverter motor drive for vehicle applications. The bidirectional dc-dc converter is placed in between low-voltage and high-voltage sources to allow energy transfer. In many applications such as vehicles and stationary power, the battery pack or energy storage handles quick start-up before the primary source is warmed up. Also during transient load conditions, the energy storage supplements the power for the generator output. This is considered as the “boost mode.” When the energy stored in battery or energy storage element is low, and the high side bus has excess

energy, the converter can then be operated in "buck mode" to charge the low side auxiliary energy storage.

In Figure 2.1, IGBT switches S_{1u}-S_{3u} and S_{1d}-S_{3d} serve as the main switches for either buck mode or boost mode. Each switch has its own anti-paralleled diode which is carrying current during free-wheeling period. Each switch is paralleled with a lossless snubber capacitor. Three inductors L_{d1}-L_{d3} can be used as the boost inductor under boost mode operation or low-pass filter inductor under buck mode operation. Capacitor C_{low} and C_{high} serve as the smoothing energy buffer. With interleaved inductor currents, the ripple current going into these capacitors is minimized.

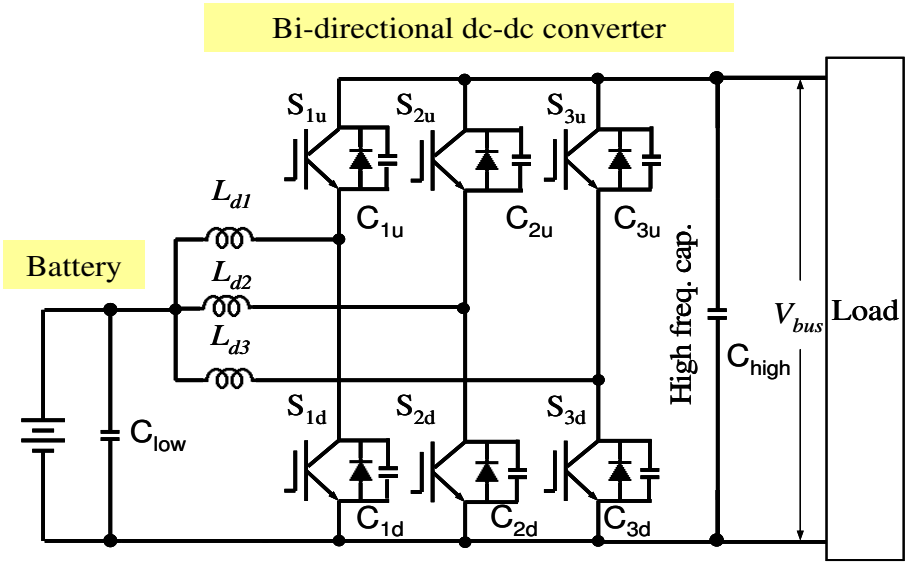


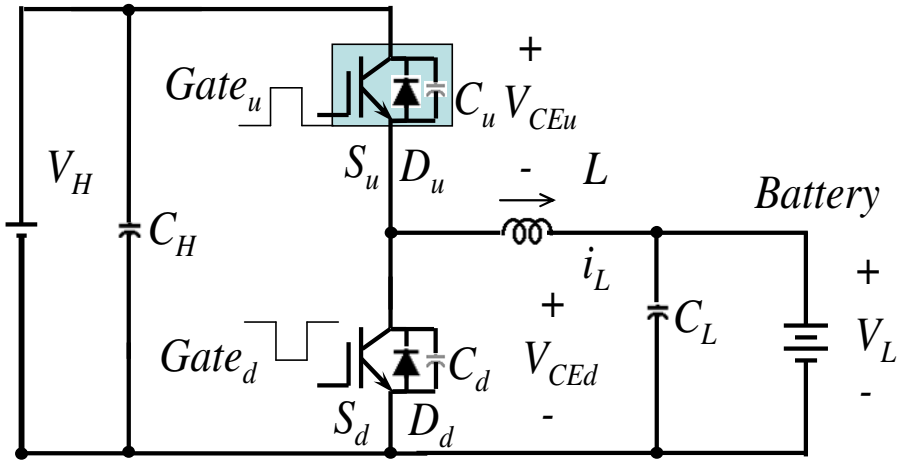
Figure 2.1 Circuit diagram of three phases interleaved synchronous mode zero-voltage switching bidirectional dc-dc converter

2.2.2 Circuit Operation Principle

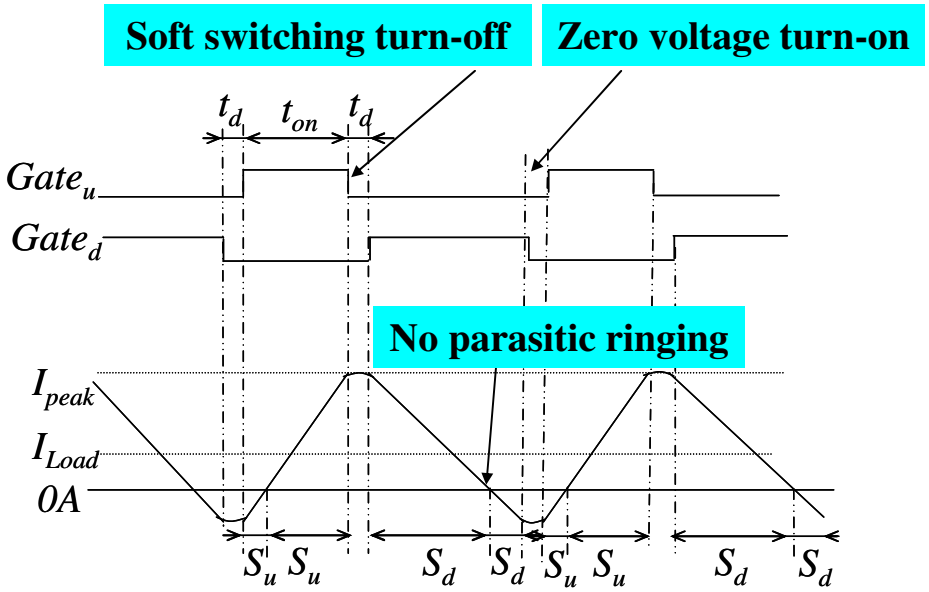
Figure 2.2 shows the proposed complimentary gating control for one phase-leg operation. The inductor current, rather then operating in a traditional DCM condition, goes from positive to negative direction and then swings back to positive. Using the upper switch S_u as the main switch for buck mode operation, lower switch S_d becomes the auxiliary switch.

Initially when the main gate signal $Gate_u$ is on, switch S_u conducts, and the low-side battery is charged. During the dead time t_d, all switches are turned off, so the inductor current i_L will charge C_u and discharge C_d. The device voltage charge and discharge rates are slowed down, and the turn-off loss is reduced. After they are fully charged and discharged, which means the V_{CEd} becomes zero, diode D_d will take over the inductor current. Auxiliary switch S_d is gated on under zero-voltage condition because diode D_d is carrying the freewheeling current. With the voltage V_L against the inductor the current continuously decreases until it passes through zero and changes its direction. At this time, the current will go through the auxiliary switch S_d. It is easily noted that the diode turns off naturally without having reverse recovery loss. The parasitic ring is also fully avoided.

The auxiliary switch S_d creates a negative current, which helps charge C_d and discharge C_u when S_d is turned off into the dead time period. After C_u is fully discharged, the voltage across the main switch V_{CEu} becomes zero, diode D_u will carry the inductor negative current. Then the main switch S_u is turned on at zero-voltage condition. Thus both upper and lower switches are all turned on at zero voltages. After the upper diode conducts, the voltage difference between high side bus voltage V_H and battery voltage V_L will apply across the inductor L, and the inductor current i_L will increase until it passes through zero and changes into positive direction, and the main switch S_u naturally takes over the current.



(a) Circuit diagram for buck mode single phase



(b) Gate signal and inductor current waveform

Figure 2.2 Buck mode operation with complementary gating signal control

The benefits of complementary control ZVRT are noticed in twofold. One is less heat sinking requirement and the other is that a higher switching frequency can be implemented for further reduction of the inductor size. The major additions are the need for the complementary gate signal and the added snubber capacitors that may introduce some tail current during turn-off condition.

2.3 Circuit Parameters Optimization

2.3.1 Inductance Selection

The inductor design has a significant impact on the system performances, such as the realization of complementary control ZVRT soft switching, device switching loss, system volume, inductor power loss etc. It is necessary to optimize the inductance with all the design considerations.

The relationship between inductor peak current I_{peak}, minimum current I_{min}, and inductor RMS current I_{RMS} can be expressed in (2.1)-(2.5), where T_s is the switching period, I_{load} is load current, P is the load power and ΔI is the inductor current ripple.

$$\Delta I = \frac{1}{2} \cdot \frac{V_{in} - V_o}{L} \cdot \frac{V_o}{V_{in}} \cdot T_s \tag{2.1}$$

$$I_{Load} = \frac{P}{V_o} \tag{2.2}$$

$$I_{peak} = I_{Load} + \Delta I \tag{2.3}$$

$$I_{\min} = I_{Load} - \Delta I \tag{2.4}$$

$$I_{rms} = \sqrt{I_{Load}{}^2 + \frac{\Delta I^2}{3}} \tag{2.5}$$

The optimization of the inductor design should satisfy the following conditions: (a) zero-voltage switching condition under all operating conditions and (b) lowest volume.

(1) Realization of ZVRT Soft Switching

From the above-described operation, it is found that the realization of gate signal complementary control ZVRT soft switching depends on the emergence of inductor negative current, which can be acquired by limiting inductance to be less than the value L_{cr} expressed in (2.6). This inductance allows the converter operating under the boundary condition between DCM and CCM.

$$L_{cr} = \frac{1}{2} \cdot \frac{V_{in} - V_o}{P} \cdot \frac{V_o{}^2}{V_{in}} \cdot T_s \tag{2.6}$$

Figure 2.3 shows the inductor peak current I_{peak} and minimum current $I_{\min}$ as a function of inductance in single phase leg at input voltage V_{in} of 700 V, output voltage V_{o} of 200-300 V, switching frequency f_{sw} of 25 kHz and the maximum power P of 33.3 kW (=100 kW/3). Figure 2.3, it can be seen that to get a negative current for all the load conditions the inductance must be less than 17.14 μH. This boundary condition falls at buck mode heavy load (output voltage V_{o}=200 V) point. Figure 2.3 also shows that the inductor peak

current I_{peak} will increase with the decrease of the inductance value. To ensure the operation point below the selected IGBT rating of 400 A, the inductance had better be larger than 13.5 µH, whose peak current is close to 380 A. Therefore, the desirable inductance is selected within 13.5-17.14 µH.

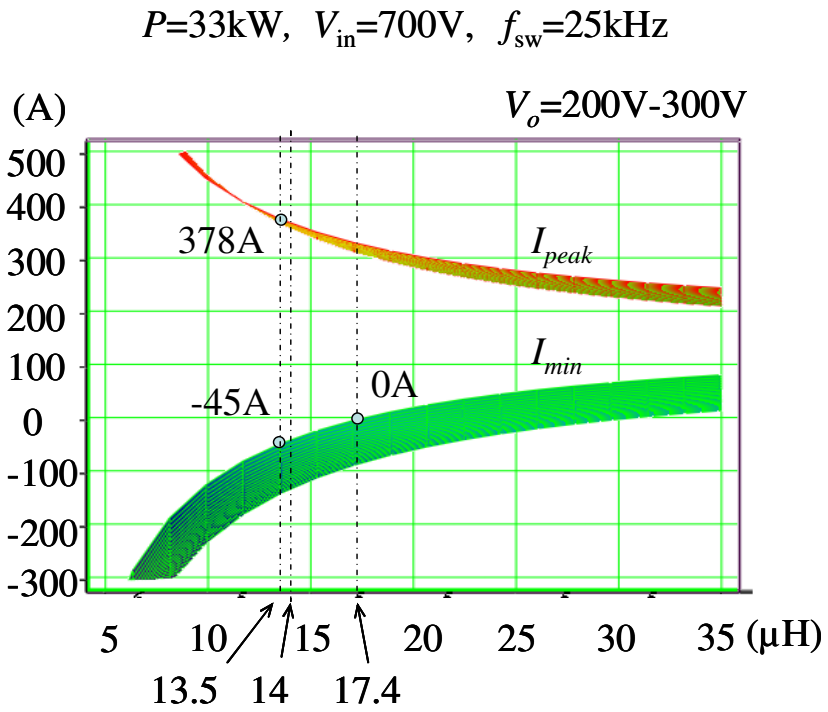


Figure 2.3 Inductor current vs. inductance

(2) Inductor Volume Index

The inductor volume can be represented by the volume index, which is $L{\cdot}I_{peak}^2$. According to equation (2.1)-(2.3), the volume index as a function of inductance is shown in Figure 2.4. The minimum volume area is at 17.14 µH. Further reduction of the inductance will result in larger inductor volume, which implies there is no significant benefit to use smaller inductance from the volume point of view. For inductance between 13.5µH and 17.14 µH, the volume almost makes no difference.

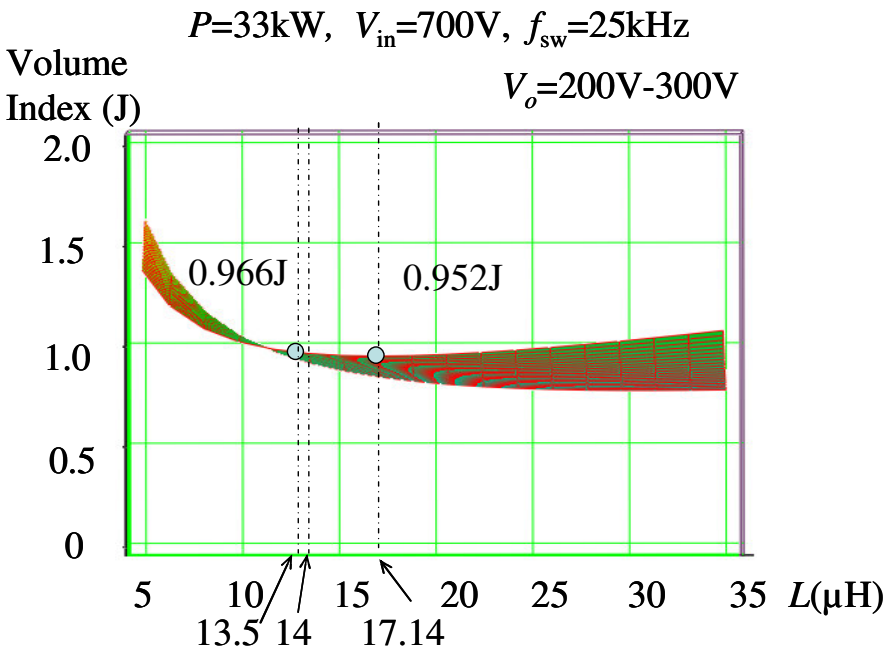


Figure 2.4 Volume index as a function of inductance

2.3.2 Inductor Power Loss Consideration

Inductor core materials influence the core power loss a lot for the same ripple frequency. Table 2.1 is the comparison of different core materials power loss at B=½B_{sat} and f=25 kHz.

Table 2.1 Different core materials performance comparison

	Finemet cut_off	Finemet no cut off core	Fe-Al-Si powder core	Ferrite core	Fe based amorphous
B_{sat} (T)	1.26	1.26	1	0.5	1.56
Max temp. (°C)	150	150	200	125	150
Loss (W/cm^3) f=25kHz, B=0.5B_{sat}	1.033	0.147	4.54	0.173	3.9

Here Finemet is the material which is being formed with fine crystal grains. Note that the Finemet no-cut core is only suitable for transformer applications not the inductor application here. Finemet cut-off core can be used for inductor, since an adjustable air gap can be developed between the two cut-off cores.

The overall comparison results show that the Finemet cut-off core and ferrite core have relative less power loss when flux density B is at half of individual saturation value B_{sat}. The product of operating flux density B, number of turns N and core area A is as shown in (2.7) and under the required inductance value L, such as 14 μH, and certain maximum current I_{pk}, it is fixed. Even though ferrite has less power loss at $½B_{sat}$ condition, its low saturation flux density B_{sat} may result in lower operating flux density and therefore higher area, which means relatively higher volume. The increased core area increases core loss, since the core loss is proportional to the core volume.

$$N \cdot B \cdot A = L \cdot I_{pk} \tag{2.7}$$

Finemet cut-off core is preferred because its higher saturation flux density provides higher energy storage capability and thus smaller inductor volume. High saturation flux density can also avoid core saturation during transient or startup when a large transient current spike is likely to occur. More importantly it helps reduce the air gap and the related gap loss. Another advantage is its higher performance stability in high temperature operation, which is essential for this special application. So Finemet cut-off core is selected for this high power and high temperature application.

2.3.3 Snubber Capacitor Optimization

(1) Snubber Capacitor Selection Consideration

In general, a larger capacitance allows more reduction on turn-off loss, but it may introduce more turn-on loss. Thus the design trade-off is to minimize total turn-on and -off losses. It is easy to understand that if the inductor stored energy is greater than the capacitor energy storage ability and capacitor voltage can be fully discharged during dead time period, there will be no extra turn on loss. The snubber design can be simply done with charge balance of Cv^2 and $½ Li^2$ shown in (2.8).

$$C \cdot v^2 = \frac{1}{2} \cdot L \cdot i^2 \tag{2.8}$$

Here v is capacitor voltage and i is inductor current.

This argument may prompt the use of small capacitance or total elimination of snubber capacitor, which is good for power MOSFET. But with significant IGBT tail current, the simple charge balance is insufficient to minimize the switching loss. In order to ensure minimum loss, a series of experiments were conducted to check the turn-on and turn-off losses under hard- and soft-switching conditions.

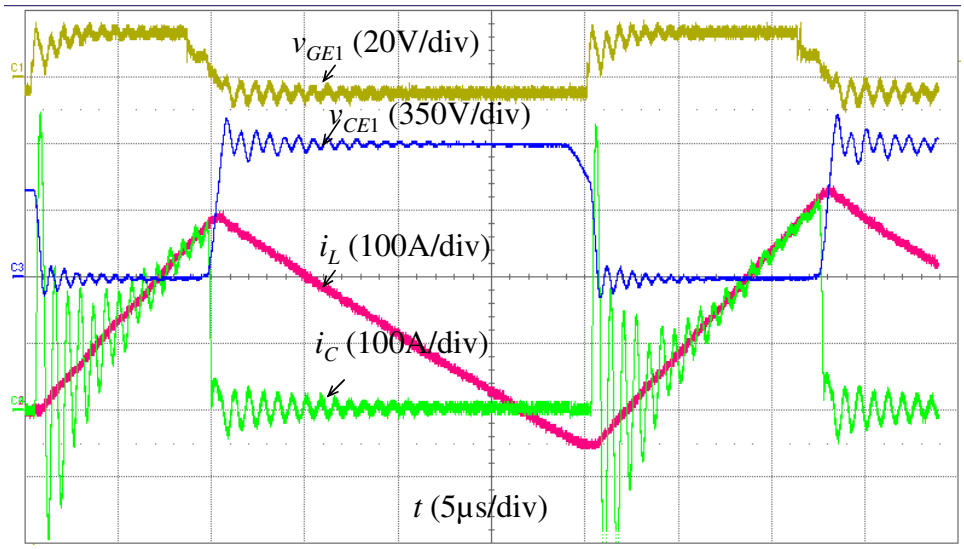
(2) Pulse Experimental Results with Various Capacitances

Using the circuit shown in Figure 2.2 (a) with the selected 14 μH inductance, different capacitances are tested with a pulse tester. The pulse tester produces a double-pulse train, similar to the gate signals shown in Figure 2.2 (b), with each pulse width varying in tenths of micro seconds to establish the inductor current. The double-pulse train repeats every second, and thus a small current sense transformer can be inserted to the device screw terminal without going into saturation. The device voltage and current during switching can be monitored with a high bandwidth oscilloscope and the switching turn-on and -off energies can then be calculated.

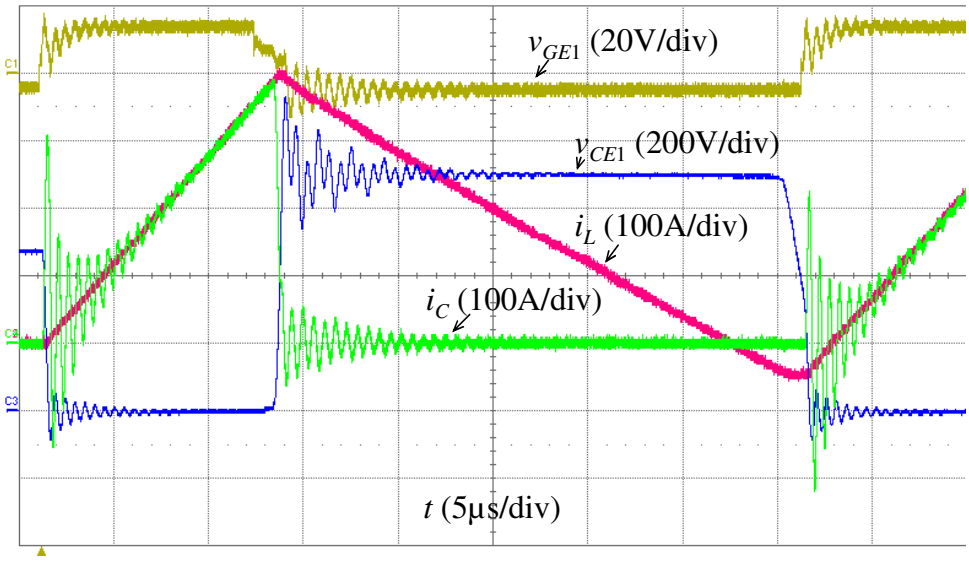
A total of five cases were tested for snubber capacitor optimization: (1) C = 0.14 μF, (2) C = 0.1 μF, (3) C = 0.068 μF, (4) C = 0.033 μF, and (5) C = 0. Figure 2.5 shows measured voltage and current waveforms with snubber capacitor equal to 0.14 μF, 0.068 μF, and 0.033 μF, respectively. The waveforms indicate that the smaller capacitance value, the larger overlap area of v_{CE} and i_c during turn-off, which means larger turn-off loss. They also indicate that the smaller capacitance value, the easier it is for the capacitor voltage to be discharged for zero-voltage turn on. However, the capacitance with which the capacitor voltage is just fully discharged does not necessarily lead to overall highest efficiency. The overall highest efficiency falls at capacitance of 0.068 μF.

No parasitic ringing appears in inductor current, which is as expected. For the switch current, there are some high-frequency noises induced by parasitic inductance during turn-on even if the capacitor energy is fully discharged. These noises are not avoidable because of the inserted current sense transformer. The parasitic ringing can be largely

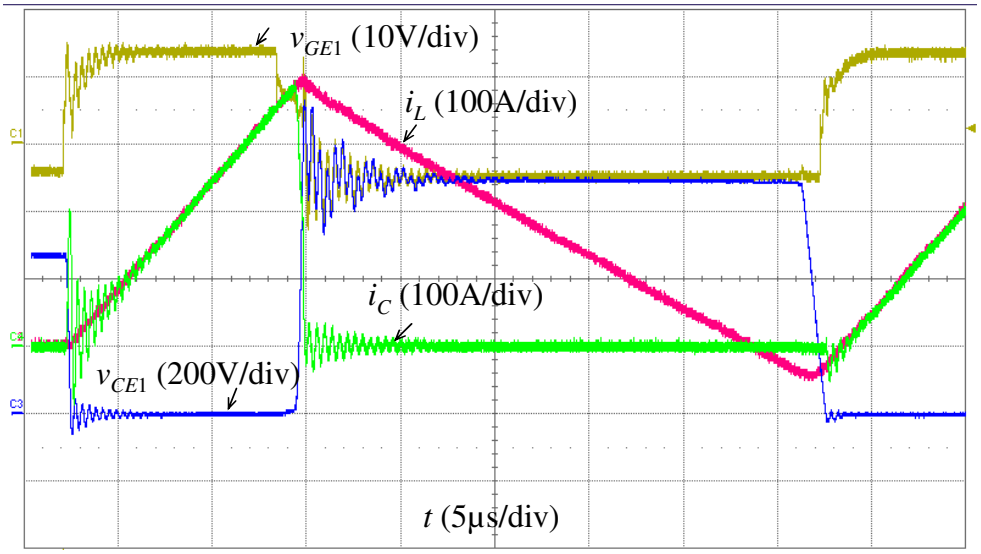
reduced or even eliminated when the current sensor is removed, which can be seen in the later section describing overall system level test results. Notice that the device current well agrees with the inductor current during turn-on, and the measurement result allows accurate estimation of the switching energy.



(a) C = 0.14 μF



(b) C = 0.068 μF



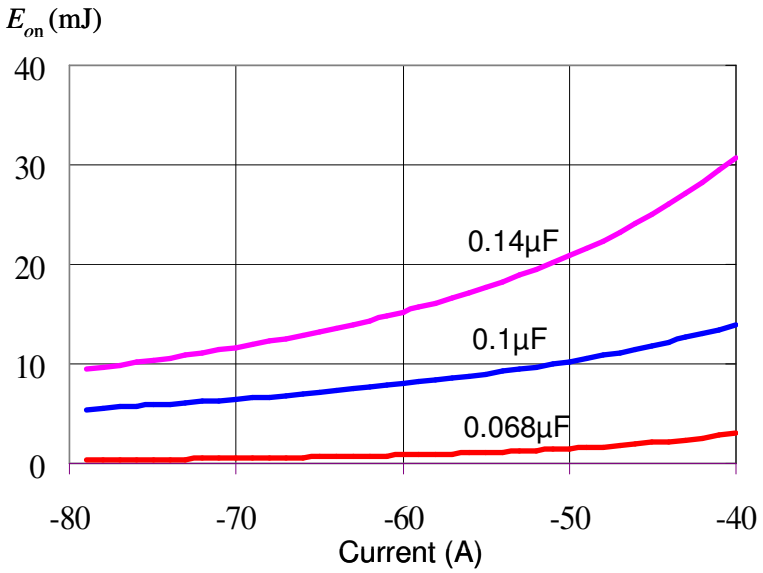
(c) C = 0.033 μF

Figure 2.5 One phase-leg buck mode test result

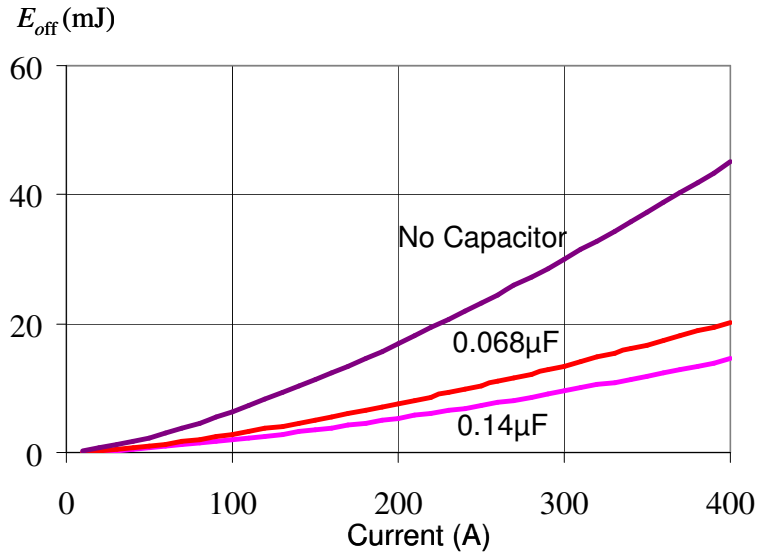
(V_{dc} = 700 V, L=14 μH, dead time=2.5 μs)

(3) Capacitance Optimization with Experimental Results

The results of turn-on losses under (a) C = 0.14 μF, (b) C = 0.1 μF, and (c) C = 0.068 μF are plotted in Figure 2.6(a), and turn-off losses under (a) C = 0.14 μF, (b) C = 0.068 μF, and (c) C = 0 are plotted in Figure 2.6 (b). To plot the curves, each capacitor was tested under more than three current conditions, and the results were curve-fitted into the follow the equations E_{off}=mI^n and E_{on}=hI^k [83, 84]. The basic approach of obtaining m, n, h, and k, is to measure switching energies under two current conditions and take the ratio in between to find these parameters respectively. It is always a good practice to take more than three measurement points and check the calculated parameters to see if the proected switching energies fit with additional measurements.



(a) Turn-on energy vs. current



(b) Turn-off energy vs. current

Figure 2.6 Turn-on and turn-off energy vs. current with various capacitance values

(L=14 μH, heavy load, V_{CE}=700 V, f=25 kHz, dead time=2.5 μs)

With the measured turn-on and -off losses, the capacitor selection can be optimized under the worst case with which the inductor peak current is 370 A and minimum current is –40 A. The curves in Figure 2.7 show the switching loss P_{sw}, P_{on}, P_{off} and switching energy E_{sw}, E_{on}, E_{off} as a function of capacitance value. Here P_{sw} is the sum of P_{on} and P_{off} and E_{sw} is the sum of E_{on} and E_{off}. From the results, it is noticed that the turn-off loss

decreases fast with capacitance value of less than 0.075 μF and there is no obvious improvement with larger capacitance value. While the turn-on loss increases slowly with capacitance value of less than 0.068 μF and increases fast with larger capacitance value. Thus the overall minimum power loss is found at the capacitance of 0.068 μF. Compared with no capacitor snubber case, the total switching power loss is reduced by 50%.

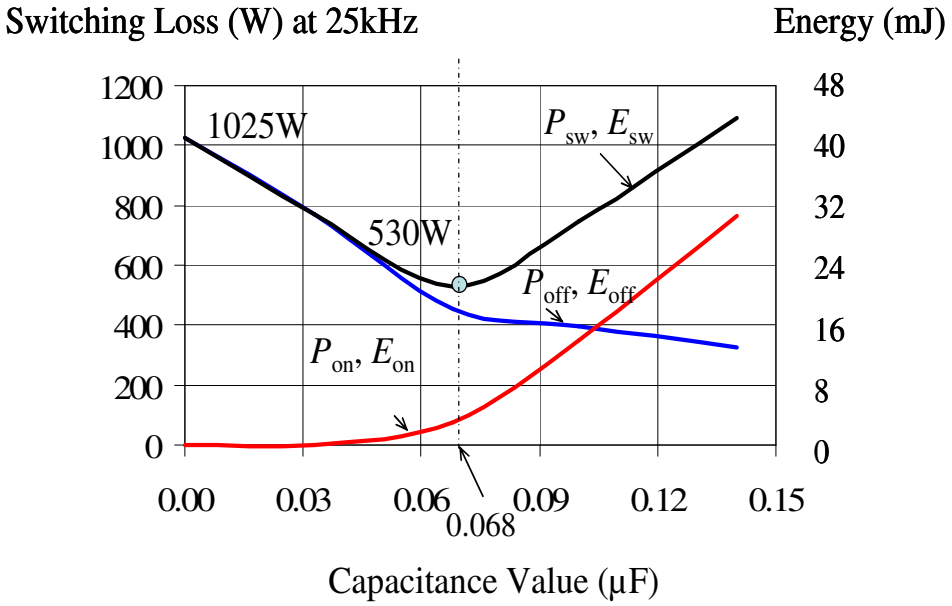


Figure 2.7 IGBT switching loss and energy vs. capacitance

(*L*=14 μH, heavy load, V_{CE}=700 V, *f*=25 kHz, dead time=2.5 μs)

2.4 Bidirectional Power Flow Experimental Verification

2.4.1 Bidirectional DC-DC Power Converter Prototype

Using the above designed parameters, a 100 kW soft-switching bidirectional dc-dc converter prototype has been built. Figure 2.8 shows the photograph of the power stage prototype. The total volume is 16.65 L with the dimension of 37 cm × 30 cm × 15 cm. The gate drives and DSP boards are interfaced with optical fibers, and the sensor signals are transmitted with current sources to minimize the effect of noise interference.

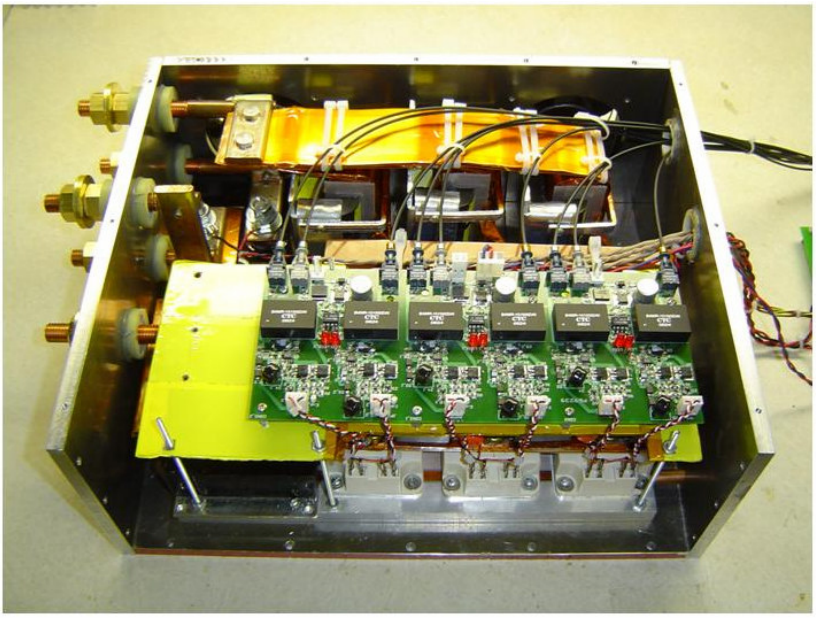
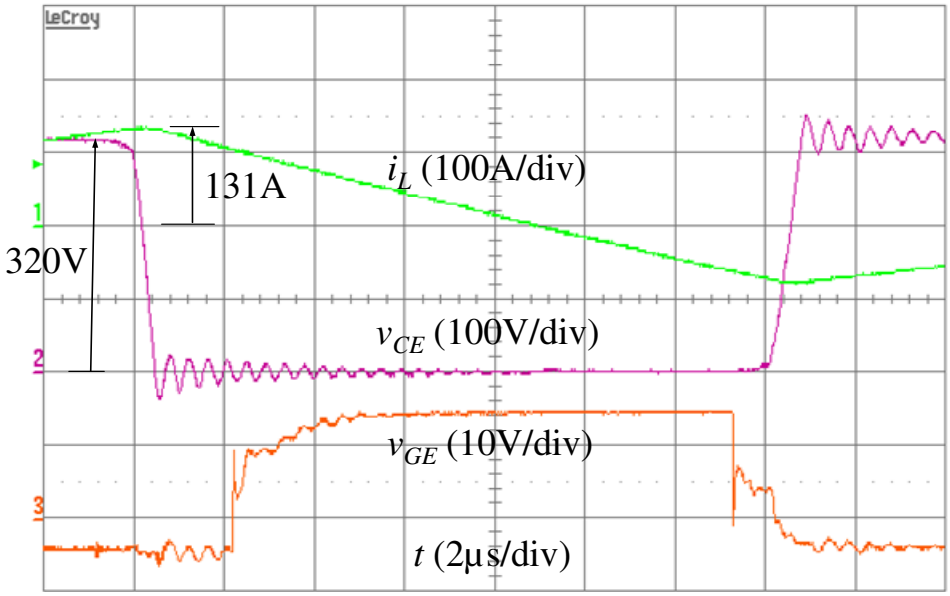


Figure 2.8 100 kW soft-switching high power bidirectional dc-dc converter prototype

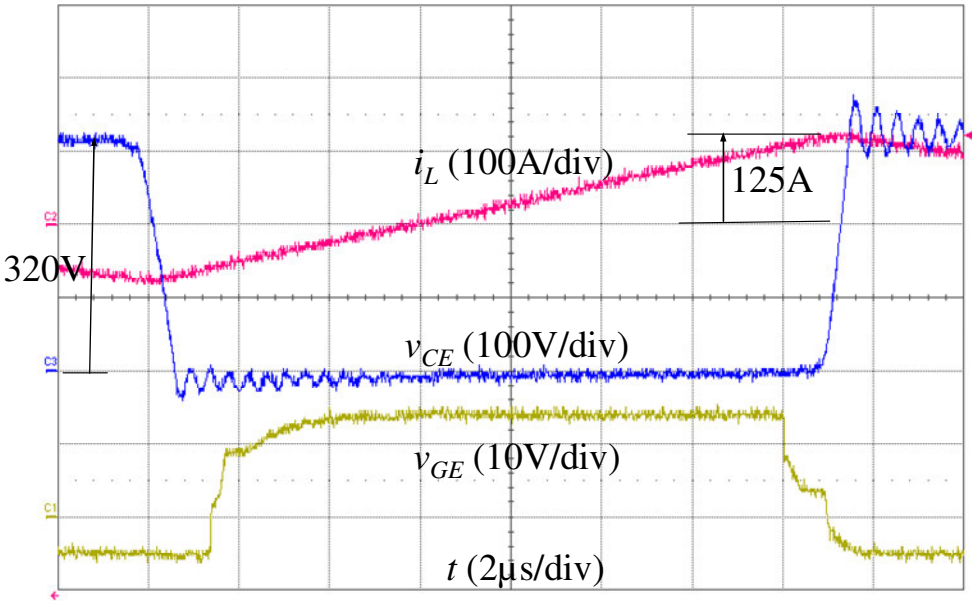
2.4.2 Bidirectional Power Flow Tests

The entire system with three-phase interleaved operation has been tested under both buck and boost mode conditions. The maximum load was tested at the rated 100 kW. Figure 2.9 shows the waveforms for lower device gate voltage v_{GE}, lower device voltage v_{CE} and inductor current i_L at 320 V high-side, 200 V low-side voltage, 13 kW output under 25-kHz switching condition with Figure 2.9(a) showing buck mode and Figure 2.9 (b) showing boost mode. At this relatively light-load condition, the difference between positive and negative current swings is small. Using equation (2.1)-(2.4), the calculated results under the nominal test condition are: current ripple ΔI = 103 A, per phase load current I_{Load} = 22 A, positive peak inductor current I_{peak} = 125 A, and negative peak inductor current I_{min} = –81 A. The experimental currents under buck and boost modes are not identical due to different load resistances connected to different voltage levels. The experimental results in boost mode agree with the calculation almost perfectly. A small difference in between was found in buck mode due to load setting and measurement

errors. Nevertheless, the theoretical derivation was well proven with the experimental results.



(a) Buck mode operation



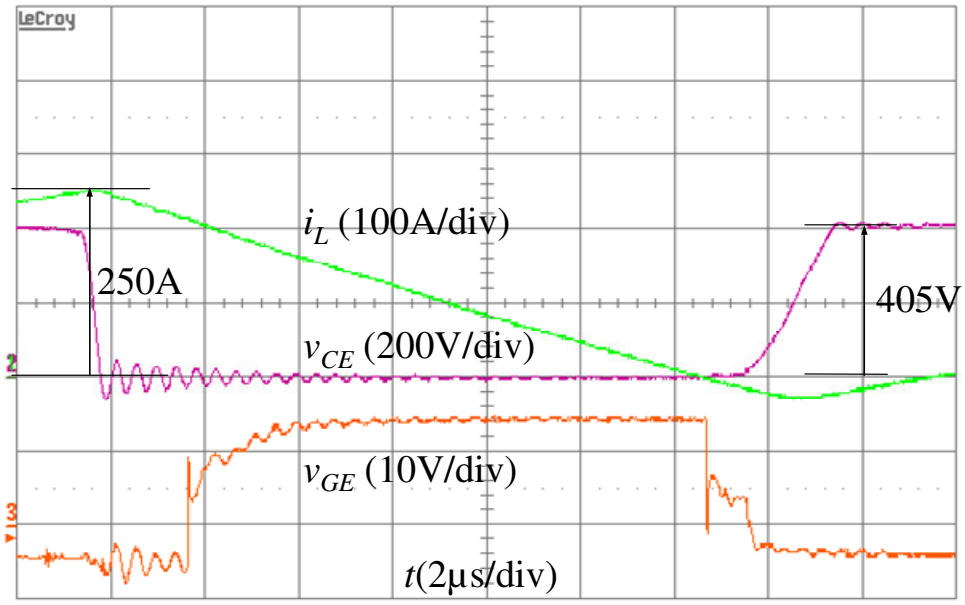
(b) Boost mode operation

Figure 2.9 Measured waveforms for device gate voltage v_{GE}, device voltage v_{CE} and inductor current i_L at 320 V input voltage, 200 V output voltage, and 13 kW output power

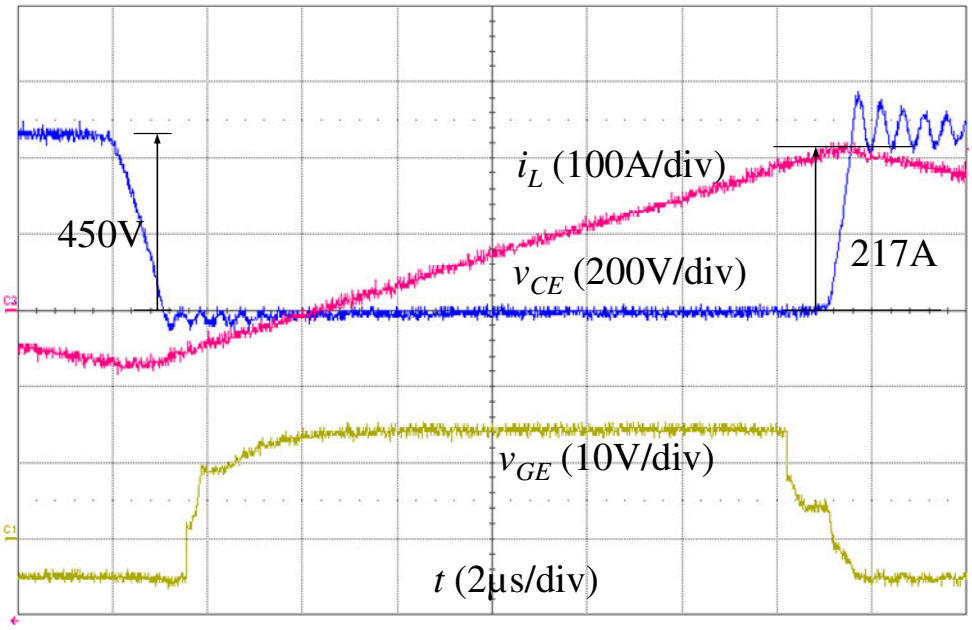
Figure 2.10 shows the tested waveforms for lower device gate voltage v_{GE}, lower device voltage v_{CE} and inductor current i_L at heavy load conditions with Figure 2.10 (a) showing buck mode running at 405 V input voltage, 240 V output voltage, 80 kW load and Figure 2.10 (b) showing boost mode running at 300 V input, 450 V output, 100 kW load conditions. The total peak-to-peak current swings are 280 A and 286 A, respectively. The average per phase inductor currents is 110 A and 72 A, and the two peak currents are 250 A and 217 A, respectively. Again, the experimental results agree with theoretical derivation very well.

From buck mode operation shown in Figure 2.9 (a) and Figure 2.10 (a), it can be seen that before the lower switch turns on, the inductor current reaches the maximum. When turning off the upper switch, the inductor current discharges the lower switch capacitance, and the lower switch voltage v_{CE} drops to zero after resonance with current flowing in the lower diode. The lower switch gate voltage v_{GE} apparently turns on at a clear zero-voltage condition. After lower switch turns on, the inductor current rises to zero and becomes positive. After the lower switch turns off at this positive current, the snubber capacitor across the upper switch turns discharges, and the upper diode then conducts to allow the upper switch to be turned on at zero voltage condition. The voltage and current waveforms are much cleaner than those shown in Figure 2.5 because the current sense transformer is removed.

From boost mode operation shown in Figure 2.9 (b) and Figure 2.10 (b), it can be seen that the initially upper switch is on, and the inductor current is negative. Under heavy load condition, the upper switch current is small but is sufficiently large to discharge the lower switch capacitance and create zero-voltage condition, so the lower switch turns on without loss.



(a) buck mode: 405 V input, 240 V output, 80 kW load

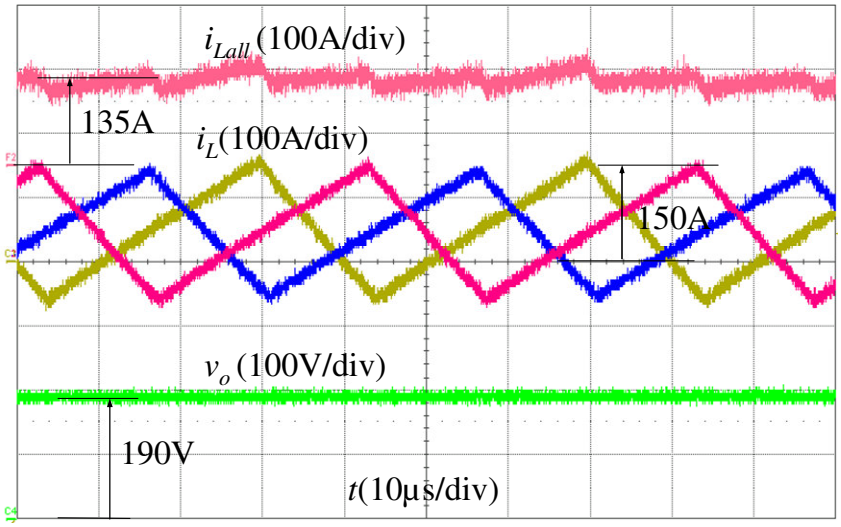


(b) boose mode: 300V input, 450V output

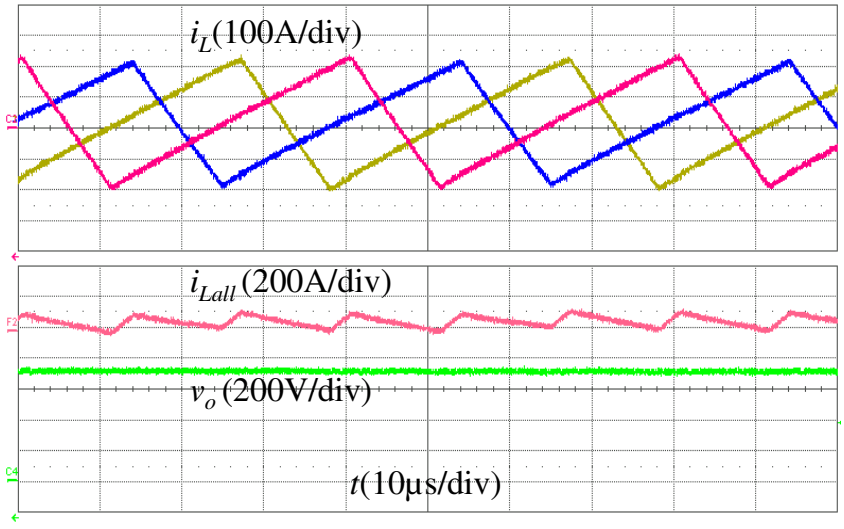
Figure 2.10 Measured waveforms for device gate voltages and inductor current at 100 kW load conditions

2.4.3 Three Phase Interleaved Control Test

The three phase interleaved inductor current waveforms are shown in Figure 2.11 with (a) showing buck mode running at 320 V input, 190 V output, 25 kW load, and (b) showing boost mode running at 210 V input, 700 V output, 21 kW load.



(a) buck mode



(b) boost mode

Figure 2.11 Three phase interleaved indcutor current i_L, overall current i_{Lall} and output voltage v_O waveforms

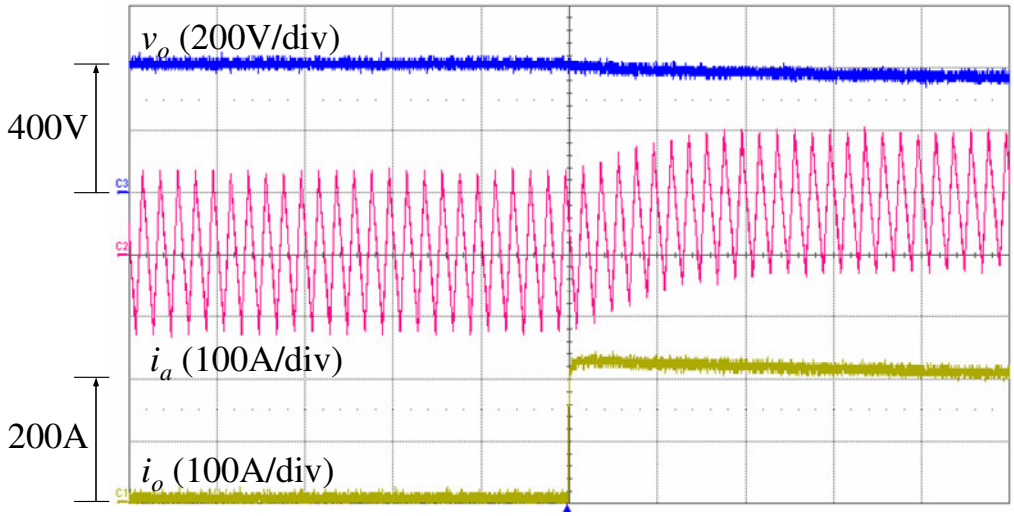
The interleaved scheme reduces the output current ripple and therefore relieves the current stress on both high- and low-side capacitors, which are all high-frequency film capacitors. Note that the output voltage ripple is negligible even with a small value of capacitances used in the circuit. The low side is a 200 μF, 500 V capacitor, and the high side is a 70 μF, 800 V capacitor.

2.4.4 System Open Loop Dynamics Test

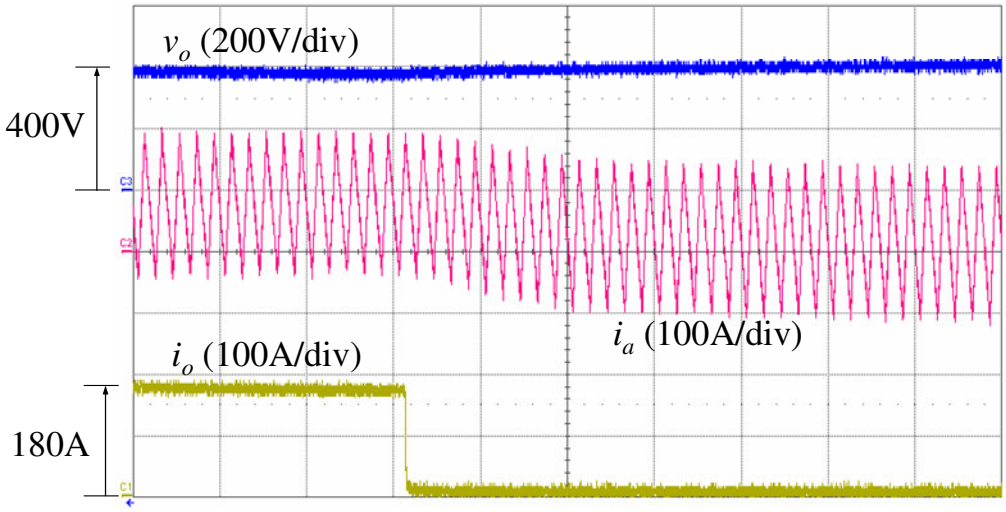
Since the inductor current continuously flows, the transient response of this type of converter operation is quite smooth. The converter can operate from no load to full load or vice versa without significant output voltage fluctuation. Figure 2.12 shows the experimental output voltage and current and inductor current waveforms under boost mode operation. In Figure 2.12 (a), the output load is initially zero, an 80 kW load is added closing a contactor. Even with open-loop control, the output voltage does not show appreciate drop. In Figure 2.12 (b), the output load is initially 72 kW and turned off to zero by opening the contactor. The output voltage does not show appreciable increase.

2.5 Power Loss Analysis and Efficiency Measurement

Major losses of a dc-dc converter come from device conduction, switching and inductor. According to datasheets, the main switching device conduction voltage drop characteristic can be approximated as a first-order equation: $v_{ce} = 0.75 + 0.003 i_{sw}$, where v_{ce} is a fixed voltage device drop and i_{sw} is the device current. Similarly, the anti-paralleled diode has a conduction voltage drop characteristic of $v_{ak} = 1 + 0.0016 i_d$, where v_{ak} is a fixed diode voltage drop, and i_d is the diode current. With 0.068 μF as the snubber capacitor, the switching loss parameters at V_{test}=700 V test condition were found to be: h=451, k=–3.23, and m=4.24×10^{-6}, n=1.414. Figure 2.6 shows the switching energies as a function of the current. Note that the E_{on} occurs only when the current is too small to discharge the snubber capacitors. As indicated in Figure 2.6 (a), the turn-on loss is only noticeable when the current is below 40 A.



(a) Load step from no load to 80 kW



(b) Load dump from 72 kW to zero load

Figure 2.12 Transient response of the converter under boost mode operation

The inductor current has a nearly constant peak-to-peak swing at a given bus voltage and duty cycle. Its positive peak and negative peak vary with the load condition. Under no-load condition, the positive peak equals the negative peak. Thus the main devices conduct significant current even under no load condition. Equations (2.1)-(2.5) express how to calculate the inductor positive peak I_{peak} and negative peak I_{min}. These two

currents can be used to calculate the main device conduction and switching losses. Using buck mode as the example, the upper and lower switches rms currents can be expressed as

$$I_{sw-upper} = I_{peak} \cdot \sqrt{\frac{D}{3}} \tag{2.9}$$

$$I_{sw-lower} = I_{\min} \cdot \sqrt{\frac{1-D}{3}} \tag{2.10}$$

Similarly the diode rms currents can be expressed as

$$I_{d-upper} = I_{\min} \cdot \sqrt{\frac{1-D}{3}} \tag{2.11}$$

$$I_{d-lower} = I_{peak} \cdot \sqrt{\frac{D}{3}} \tag{2.12}$$

The total switch and diode rms currents can be found from the sum of upper and lower device currents, i.e., $I_{sw} = I_{sw\text{-}upper} + I_{sw\text{-}lower}$ and $I_d = I_{d\text{-}upper} + I_{d\text{-}lower}$, and the device conduction losses and switching losses can be found as

Switch conduction:

$$P_{sw\text{-}con} = I_{sw}\,(0.75+0.003I_{sw}) \tag{2.13}$$

Diode conduction:

$$P_{d\text{-}con} = I_d\,(1+0.0016I_d) \tag{2.14}$$

Turn-on switching:

$$P_{on} = h(I_{peak}^{\ k} + I_{min}^{\ k}) f_s\, V_{dc}/V_{test} \tag{2.15}$$

Turn-off switching:

$$P_{off} = m(I_{peak}^{\ n} + I_{min}^{\ n})\, f_s\, V_{dc}/V_{test} \tag{2.16}$$

Figure 2.13 shows the comparison of experimental efficiencies and analytical results under buck mode test condition of 450 V input and 280 V output. The efficiency peaks at

the designed maximum power condition and tapers down in light load conditions. Both calculated and experimental peak efficiencies are found to be around 98%.

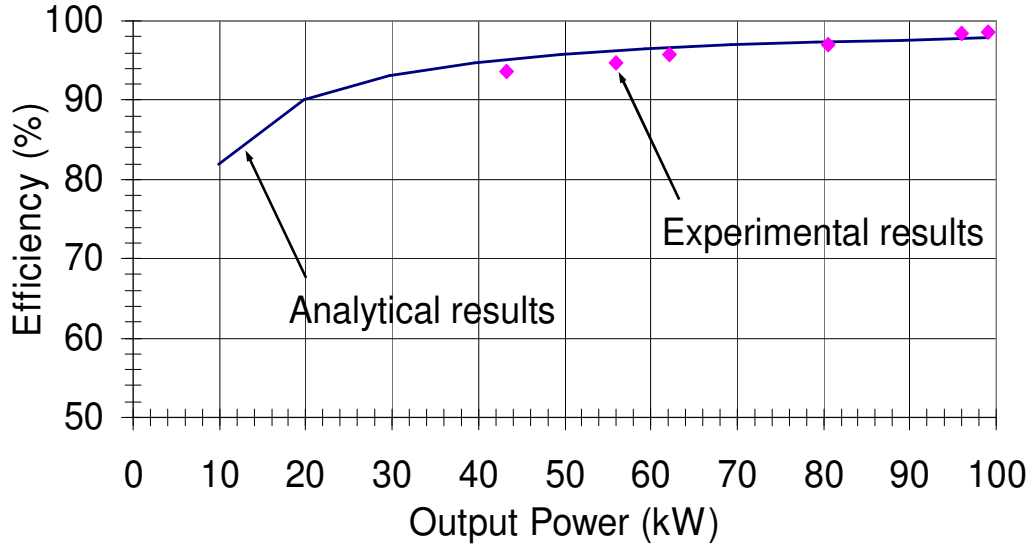


Figure 2.13 Comparison of experimental and calculated efficiencies at 450 V input and 280 V output condition

The light load efficiency suffers because the devices and inductor constantly conduct the current. The component losses are relatively constant throughout the entire power range. The calculated component losses at the full load condition are found as follows.

Switch conduction: $P_{sw\text{-}con} = 480$ W

Diode conduction: $P_{d\text{-}con} = 384$ W

Turn-on switching: $P_{on} = 0$

Turn-off switching: $P_{off} = 588$ W

Inductor loss: $P_L = 698$ W

With a total of 2.15 kW power loss, the most dominant one is the conduction loss including both switch and diode. Together with switch conduction and switching losses, the total device loss is about two-third of the total converter loss, and the remaining one third is in the inductor. Further efficiency improvement may be realized by reducing the conduction loss with higher current rated devices.

2.6 Summary

This chapter describes circuit component optimization technique to achieve significant switching loss reduction for a multiphase interleaved complementary switching type bidirectional dc-dc converter. The design optimization has been applied to a 100-kW bidirectional dc-dc converter and verified with extensive experiments. A full load efficiency of 98% is achieved, which allows high power density packaging for special applications such as high-power hybrid and fuel cell vehicles. The main features of the proposed design can be summarized as follows.

- Zero-voltage switching and thus high efficiency at heavy load conditions
- Interleaving phase-leg currents to eliminate the ripple current going into the sensitive voltage source
- Compact inductor size with discontinuous conduction mode operation
- Compact bus capacitor size with ripple cancellation

Overall, the proposed switching scheme and design approach for the soft-switched bidirectional dc-dc converter not only has size advantage, but also allows significant reduction on switching loss and noise.

Chapter 3 Power Stage Modeling

3.1 Introduction

The design and optimization of power stage circuit parameters were shown in chapter 2. In this chapter, the power stage modeling will be described. A general-purposed power stage circuit model is proposed in section 3.2. Circuit parameters are introduced. After the modeling assumptions are made in section 3.3, the bidirectional dc-dc power stage model is derived with the state-space averaging method in section 3.4. The derived model is validated by comparing between control-to-inductor current transfer function from the Simplis simulation results and the derived mathematical model. The general-purposed power stage model can be used under different operating modes.

A coupled-inductor scheme is introduced for improvement of power stage design to reduce the core loss. It is necessary to model the coupled inductor and provide a simplified model for the system controller design. In section 3.5, detailed analysis of the power stage with coupled inductors is given. The simplified coupled inductor model is provided and again verified by Simplis ac analysis simulation.

3.2 General-purposed Power Stage Circuit Model

For the controller design purpose, a multiphase interleaved converter can be simplified into a single-phase version. It is noted that the phase number only affects the equivalent inductance in simplified model and does not influence the derivation of the power stage circuit model. In this chapter, four-phase interleaved converter shown in Figure 3.1 is cited as an example. The derived model can be extended to any multiple phases converter applications. The single-phase equivalent circuit is shown in Figure 3.2. There are two dc sources including high side bus voltage source V_H and low side battery source V_L representing both voltage sources of the bidirectional dc-dc converter. With two voltage sources, the averaged inductor current i_L or averaged output current i_o can flow in both

directions, instead of flowing only in one direction in one voltage source application. Resistor R_1 represents either high-side source internal resistance in charging and discharging modes or load in boost resistive load application. Resistor R_2 represents either low-side source internal resistance for both charging and discharging modes or load in buck resistive load application. Capacitor C_H and C_L indicate the bus capacitor bank and the output capacitor at battery side respectively. Two active switches, Q_1 and Q_2, are controlled by complementary gating control signal $Gate_1$ and $Gate_2$ separately.

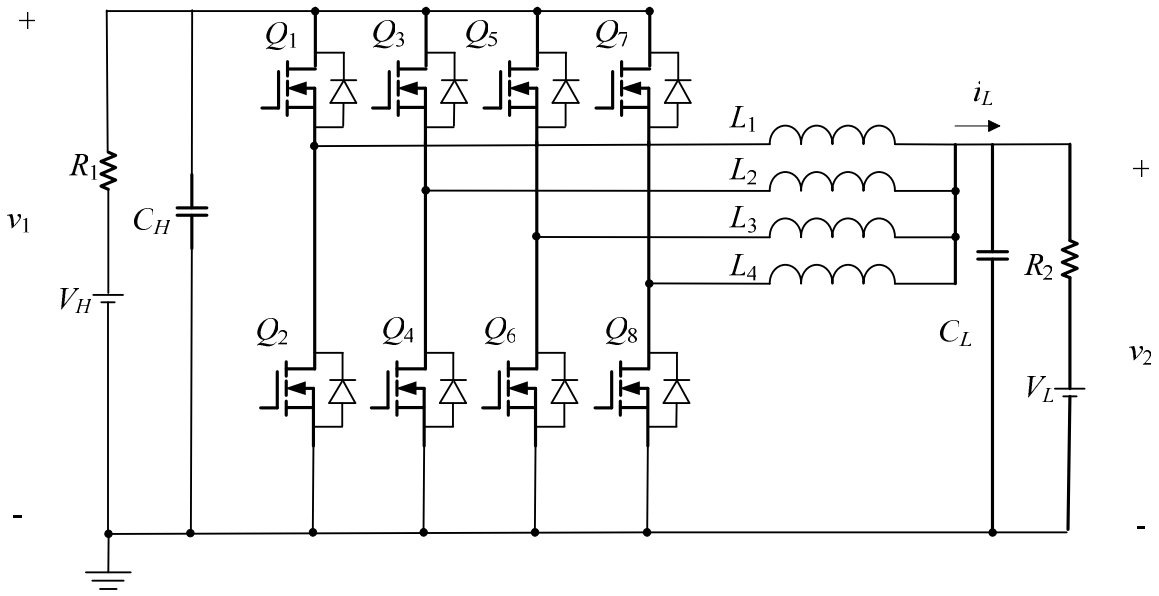


Figure 3.1 Four phases interleaving bidirectional dc-dc converter

For phase number n, the equivalent inductance L is each phase inductance L_1 divided by n. The upper switch Q_1 is the control switch. Inductor parasitic resistance R_{lP} and MOSFET turn-on resistance R_{dson} are also involved in the model, since they are a critical factor for this application. There are three energy storage components: input capacitor C_H, output capacitor C_L and inductor L.

With this circuit model, the derived power plant can be used for battery charging and discharging modes or boost resistive load and buck resistive load applications, since all these cases can employ the same equivalent circuit.

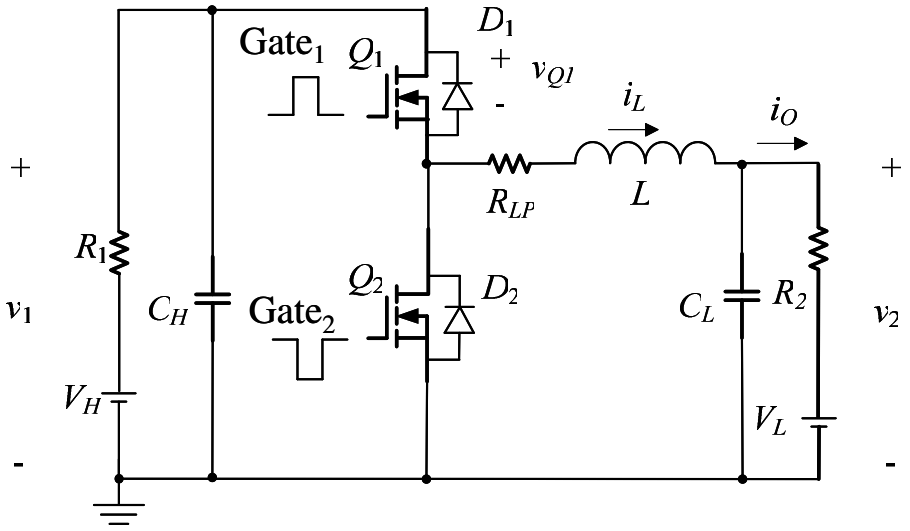


Figure 3.2 Circuit diagram of bidirectional dc-dc single phase

3.3 Model Assumptions

State-space averaging method is employed for the modeling of the bidirectional dc-dc converter with the following assumptions.

(1) Balanced Current among Four Phases

In high power applications, the current unbalanced among phases will not be as high as that in low power applications provided an evenly distributed inductance design and less parasitic power stage layout. The interleaving inductor total current i_{Lall} waveforms of four phases are shown in Figure 3.3.

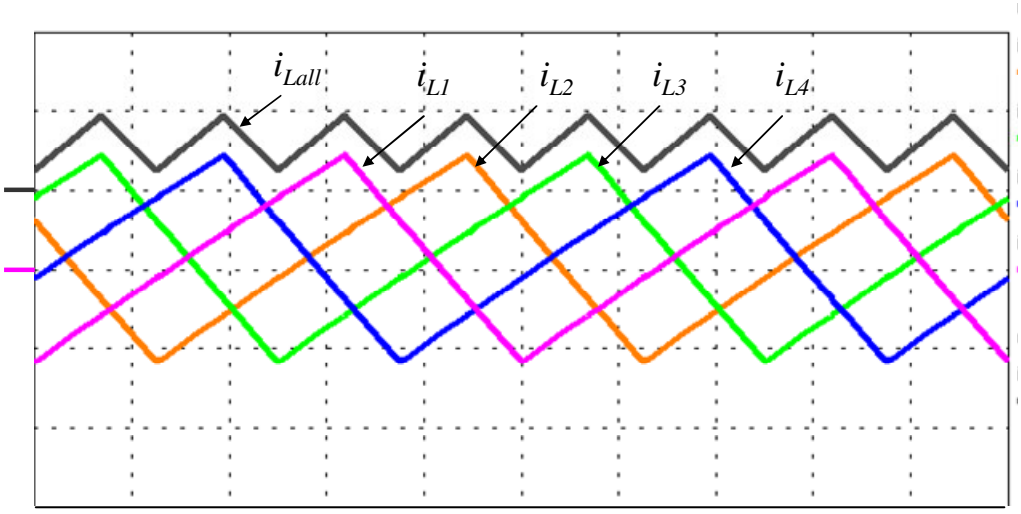


Figure 3.3 Inductor current and total i_L current i_L-all waveform

(2) Small Ripple Assumption

From Figure 3.3, the individual inductor current ripple is relatively large. In such a case, the use of state-space averaging modeling method becomes a question.

In order to get an answer, a series simulation was carried out. A small amplitude ac signal ΔD with perturbation frequency f_{pur} is injected into the duty cycle D. With this duty cycle $D+\Delta D$ control, comparison between switch model and average model of outputs V_o is made. The comparison between switch model and average model of the inductor current i_L is made as well. The average model is the traditional model which is described in ref [90].

Table 3.1 shows the simulation conditions for buck switch model and average model. There are two simulation cases including case 1 and case 2 with two different perturbation frequencies of 2.5 kHz and 100 Hz respectively. Figure 3.4 shows the simulation results of case 1. Figure 3.5 is the simulation result of case 2. It is noted that under the simulation conditions the averaged model follows the middle line of switch model.

Table 3.1 Buck switch model and averaged model simulation conditions

	System parameters						*Perturbation parameters*	
Case	V_H	V_L	L	C	f_s	D	f_{pur}	ΔD
1	280V	0	25μH/4	150 μF	25 kHz	0.63	2.5 kHz	0.01
2	280V	0	25μH/4	150 μF	25 kHz	0.63	100 Hz	0.01

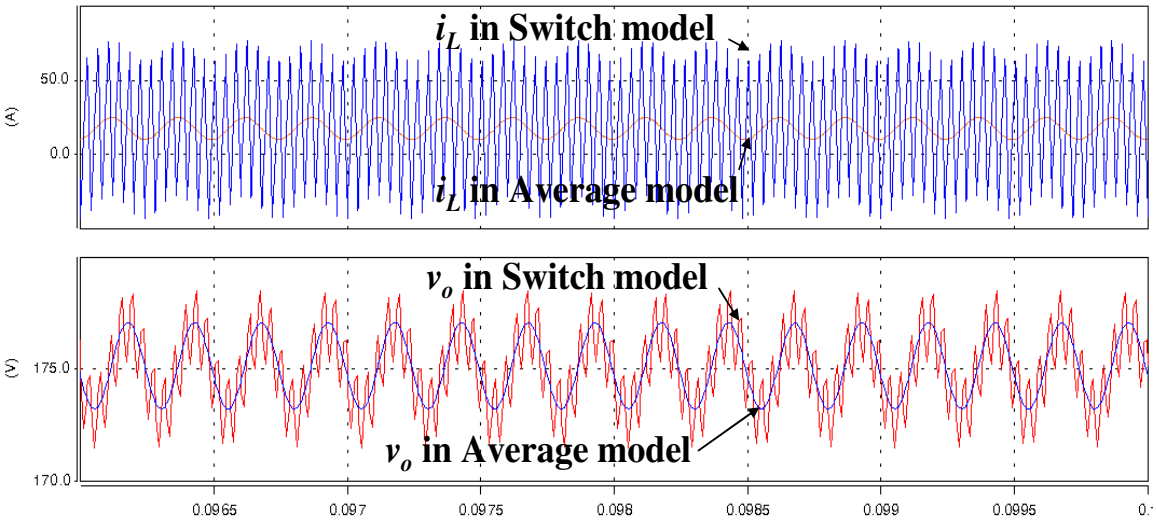


Figure 3.4 Case 1 simulation results of switch model and averaged model for buck mode

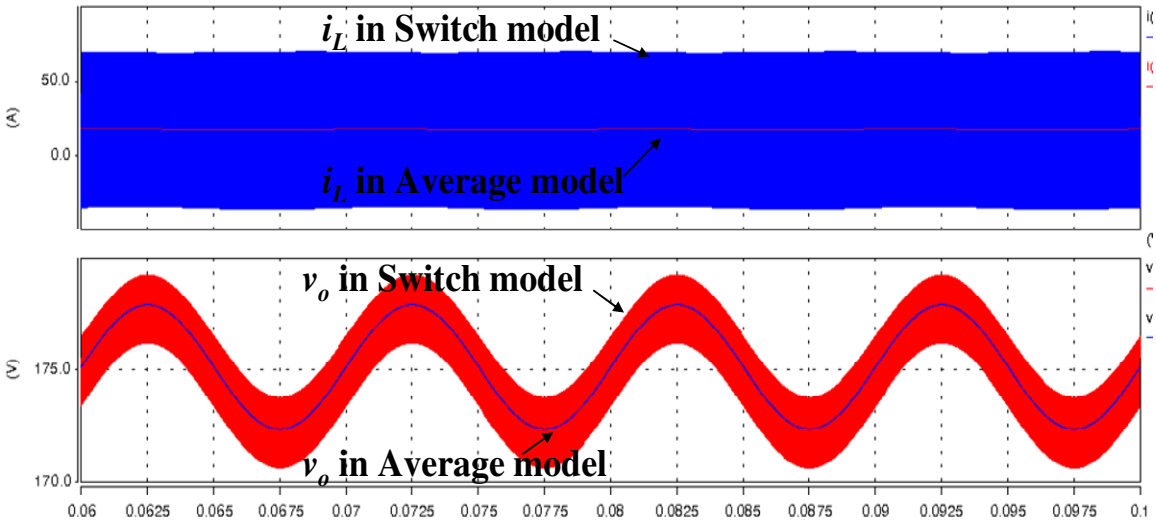


Figure 3.5 Case 2 simulation results of switch model and averaged model for buck mode

Using the same procedure, a boost-mode simulation is made under the conditions shown in Table 3.2. There are two simulation cases including case 1 and case 2 with two different perturbation frequency of 2.5 kHz and 100 Hz respectively. Figure 3.6 is the simulation results of case 1. Figure 3.7 is the simulation result of case 2.

Table 3.2 Boost switch model and averaged model simulation conditions

	System parameters						*Perturbation parameters*	
Case	V_H	V_L	L	C	f_s	D	f_{pur}	ΔD
1	0V	120V	25μH/4	150 μF	25 kHz	0.657	2.5 kHz	0.01
2	0V	120V	25μH/4	150 μF	25 kHz	0.657	100Hz	0.01

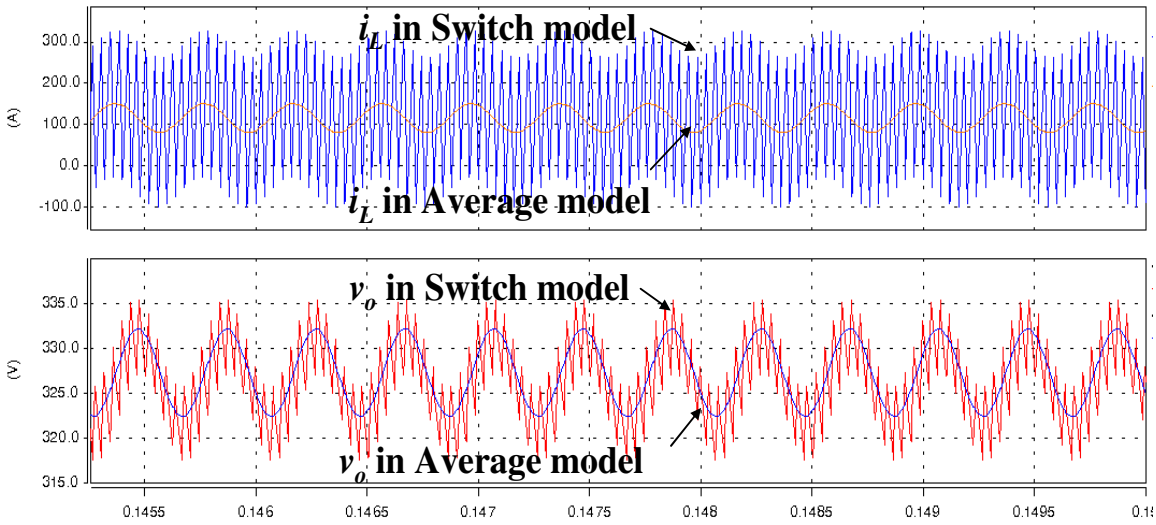


Figure 3.6 Case 1 simulation results of switch model and averaged model for boost mode

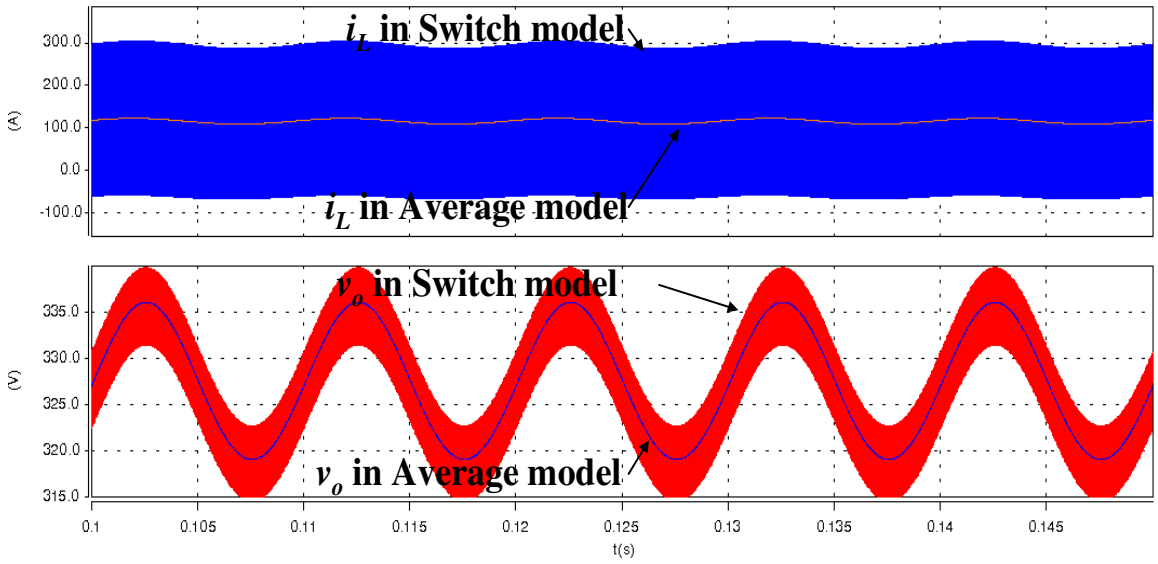


Figure 3.7 Case 2 simulation results of switch model and averaged model for boost mode

The comparisons show that the small ripple assumption can be used in this modeling as long as low perturbation frequency is kept.

(3) Negligible Dead-Time Effect

Since the dead-time t_d is 1μs, which is less than 4 percent of switching period T_{sw}, the dead time effect is ignored to highlight the system stability related design method. So does the soft-switching period which occurs during the dead time.

(4) Identical Device Conduction Voltage Drop in Different Power Flow Directions

The device conduction voltage drop is only a fraction of the dc bus voltage, and the variation among devices is another fraction of the device conduction voltage drop. Thus the conduction voltage drop variation in different power flow directions can be easily neglected.

3.4 Bidirectional DC-DC Power Stage Modeling

3.4.1 State-space Averaged Model

From the discussion in chapter 2 and the above assumptions, it can be seen that no matter which operating modes, either battery charging mode or discharging mode, there are always two subintervals t_{on} and t_{off} as shown in Figure 3.8. In the first subinterval, when the switch Q_1 is on, and Q_2 is off, the converter equivalent circuit can be represented in Figure 3.9.

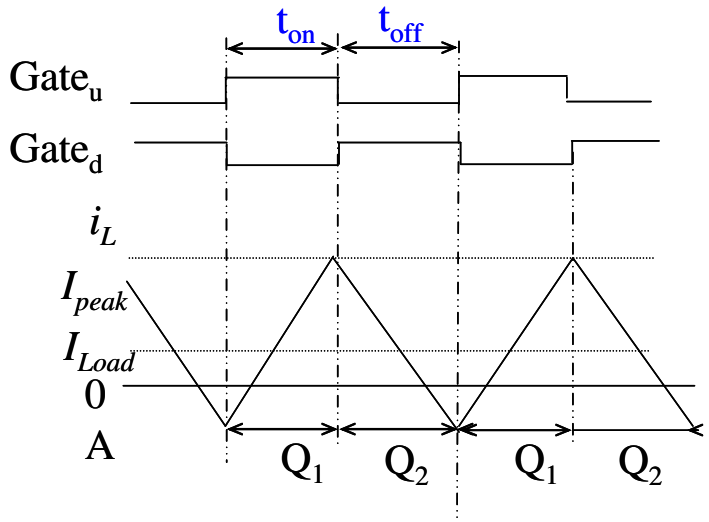


Figure 3.8 Complementary gating signal control

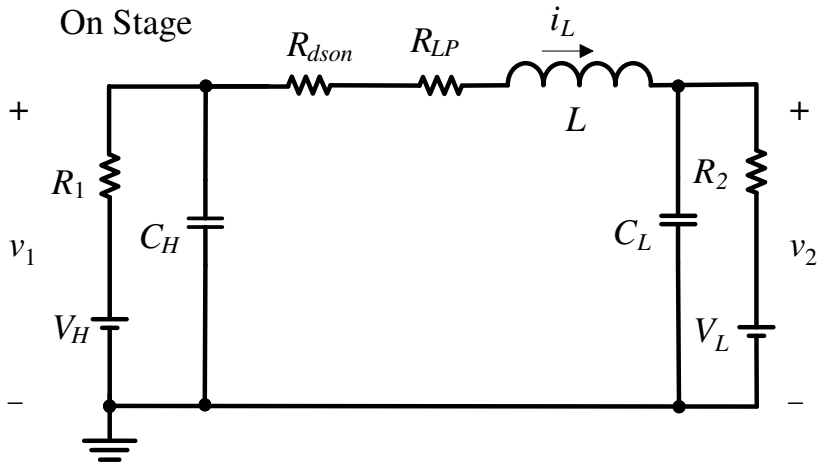


Figure 3.9 First subinterval during t_{on}

There are three energy storage components, inductor current i_L, low side capacitor voltage v_2 and high side capacitor voltage v_1. Inductor voltage across the inductor L is given by (3.1) and the capacitor current is given by (3.2).

$$L\frac{di_L}{dt}+i_L\cdot(R_{dson}+R_{LP})=v_1-v_2 \tag{3.1}$$

$$\begin{cases} C_H\dfrac{dv_1}{dt}=-(i_L+\dfrac{v_1-V_H}{R_1}) \\ C_L\dfrac{dv_2}{dt}=i_L-\dfrac{v_2-V_L}{R_1} \end{cases} \tag{3.2}$$

In the second subinterval, when the switch Q_1 is off, and Q_2 is on, the converter equivalent circuit can be represented in Figure 3.10.

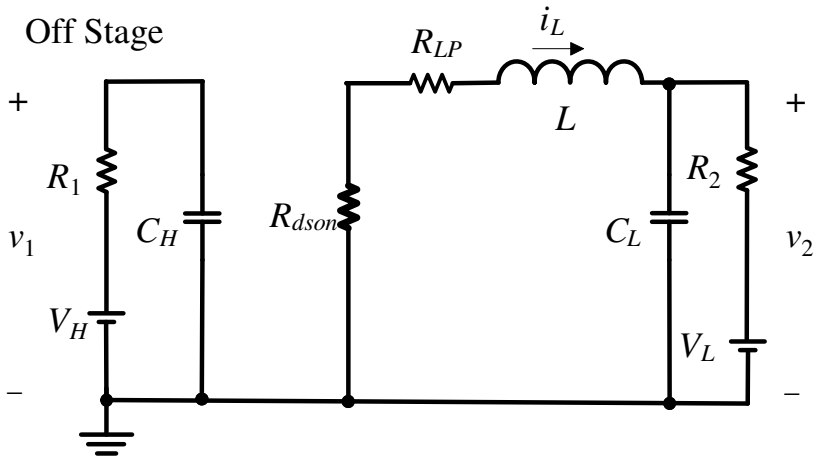


Figure 3.10 Second subinterval during t_{off}

The voltage across the inductor L is given by equation (3.3) and the capacitor current is given by (3.4).

$$L\frac{di_L}{dt}+i_L\cdot(R_{dson}+R_{LP})=-v_2 \tag{3.3}$$

$$\begin{cases} C_H \dfrac{dv_1}{dt} = -\dfrac{v_1 - V_H}{R_1} \\ C_L \dfrac{dv_2}{dt} = i_L - \dfrac{v_2 - V_L}{R_1} \end{cases} \tag{3.4}$$

State-space averaging equations are derived in (3.5).

$$\begin{cases} L\dfrac{d\bar{i}_L}{dt} = D(\bar{v}_1 - \bar{v}_2) - \bar{i}_L \cdot (R_{dson} + R_{LP}) + D'(-\bar{v}_2) \\ C_H \dfrac{d\bar{v}_1}{dt} = -D(\bar{i}_L + \dfrac{\bar{v}_1 - V_H}{R_1}) - D' \dfrac{\bar{v}_1 - V_H}{R_1} \\ C_L \dfrac{d\bar{v}_2}{dt} = \bar{i}_L - \dfrac{\bar{v}_2 - V_L}{R_2} \end{cases} \tag{3.5}$$

Finally, a general averaging model are derived in a group equations (3.6).

$$\begin{cases} L\dfrac{d\bar{i}_L}{dt} = \bar{d}\bar{v}_1 - \bar{v}_2 - \bar{i}_L \cdot (R_{dson} + R_{LP}) \\ C_H \dfrac{d\bar{v}_1}{dt} = -\bar{d}\bar{i}_L - \dfrac{\bar{v}_1 - V_H}{R_1} \\ C_L \dfrac{d\bar{v}_2}{dt} = \bar{i}_L - \dfrac{\bar{v}_2 - V_L}{R_2} \end{cases} \tag{3.6}$$

The state-space averaged dc model that describes the converter in equilibrium is,

$$0 = A \cdot \begin{bmatrix} I_L \\ V_1 \\ V_2 \end{bmatrix} + B \cdot \begin{bmatrix} V_L \\ V_H \end{bmatrix} \tag{3.7}$$

$$A=\begin{bmatrix} -\frac{R_P}{L} & \frac{D}{L} & -\frac{1}{L} \\ -\frac{D}{C_H} & -\frac{1}{R_1 \cdot C_H} & 0 \\ \frac{1}{C_L} & 0 & -\frac{1}{R_2 \cdot C_L} \end{bmatrix}$$

$$B=\begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{R_1 \cdot C_H} \\ \frac{1}{R_2 \cdot C_L} & 0 \end{bmatrix}$$

$R_p=R_{dson}+R_{LP}$

Solving equation (3.7), we can get expressions (3.8)-(3.10).

$$I_L = \frac{D \cdot V_H - V_L}{R_1 \cdot D^2 + R_2 + R_P} \tag{3.8}$$

$$V_1 = \frac{V_H \cdot (R_2 + R_P) + D \cdot R_1 \cdot V_L}{R_1 \cdot D^2 + R_2 + R_P} \tag{3.9}$$

$$V_2 = \frac{D \cdot (V_H \cdot R_2 + D \cdot R_1 \cdot V_L) + R_P \cdot V_L}{R_1 \cdot D^2 + R_2 + R_P} \tag{3.10}$$

The state-space ac state equations that describe the converter in equilibrium can be shown in (3.11).

$$\begin{cases} L\dfrac{d\hat{i}_L}{dt} = (D+\hat{d})(V_1+\hat{v}_1) - (V_2+\hat{v}_2) - (I_L+\hat{i}_L)\cdot(R_{dson}+R_{LP}) \\ C_H\dfrac{d\hat{v}_1}{dt} = -(D+\hat{d})(I_L+\hat{i}_L) - \dfrac{\hat{v}_1 - V_H}{R_1} \\ C_L\dfrac{d\hat{v}_2}{dt} = (I_L+\hat{i}_L) - \dfrac{V_2+\hat{v}_2 - V_L}{R_2} \end{cases} \tag{3.11}$$

By neglecting the higher order items, the control to high-side-voltage transfer function can be obtained in (3.12), the control to low-side-voltage transfer function can be obtained in (3.13), and the control-to-current transfer function can be obtained in (3.14). Equation (3.14) tells us that this is a third-order power stage model.

$$\frac{\hat{v}_1}{\hat{d}} = \frac{-\frac{D}{C_H}\cdot\frac{\hat{i}_L}{\hat{d}} - \frac{1}{C_H}\cdot I_L}{s + \frac{1}{C_H \cdot R_1}} \tag{3.12}$$

$$\frac{\hat{v}_2}{\hat{d}} = \frac{\frac{1}{C_L}}{s + \frac{1}{C_L \cdot R_2}} \cdot \frac{\hat{i}_L}{\hat{d}} \tag{3.13}$$

$$G_{id} = \frac{\hat{i}_L}{\hat{d}} = \frac{(s + \frac{1}{C_H \cdot R_1}) \cdot (s + \frac{1}{C_L \cdot R_2}) \cdot \frac{V_1}{L} - \frac{D \cdot I_L}{C_H \cdot L} \cdot (s + \frac{1}{C_L \cdot R_2})}{(s + \frac{R_p}{L}) \cdot (s + \frac{1}{C_H \cdot R_1}) \cdot (s + \frac{1}{C_L \cdot R_2}) + \frac{D^2 \cdot (s + \frac{1}{C_L \cdot R_2})}{L \cdot C_H} + \frac{(s + \frac{1}{C_H \cdot R_1})}{L \cdot C_L}} \tag{3.14}$$

3.4.2 Model Verification

The above third-order general-purposed model is verified with Simplis™ simulation software, which calculates the frequency response by frequency sweep, similar to real hardware frequency response analyzer producing gain and phase plots without having to derive averaged models [94].

(1) Model Verification at Frequency Domain Case 1

In the simulation, two voltage sources V_H and V_L are provided on both sides. Simulation circuit topology and the circuit components are shown in Figure 3.11. The related parameters include the equivalent inductance L_{equ}, inductance parasitic resistance R_{Lequ}, battery internal resistance R_2 and low side filter capacitor C_L. Their values are indicated in Table 3.3.

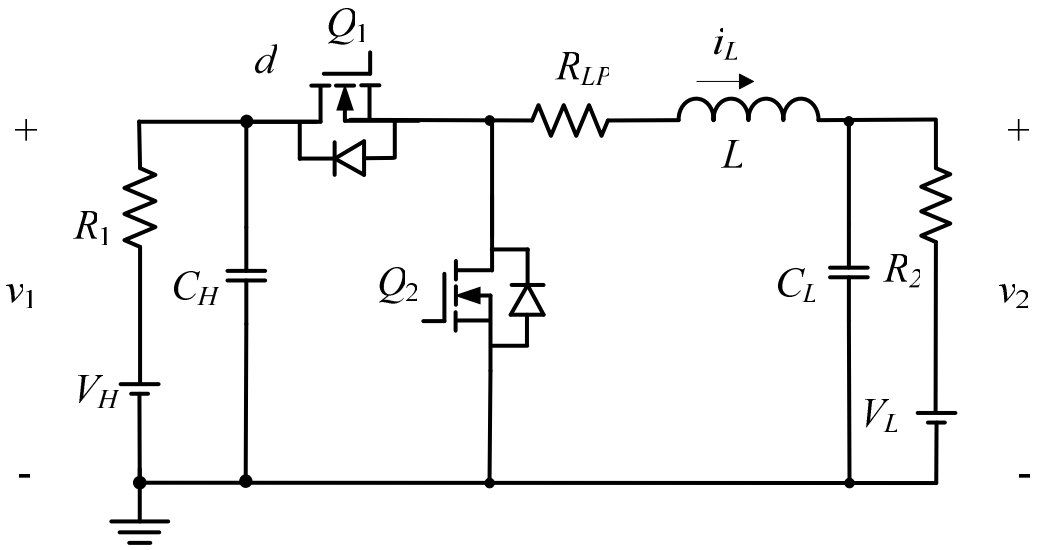


Figure 3.11 Circuit used for model verification

Table 3.3 Simulation parameters for model verification case 1

n	V_H (V)	V_L (V)	D	L_{equ} (μ H)	C_L (μ F)	f_{sw} (kHz)	R_{dson} ($m\Omega$)	R_2 (m Ω)	R_{Lequ} (m Ω)
2	233	115	0.64	5.125	150	20	8.7	30	8.8

Ac analysis of control-to-inductor current is made and the Bode plot of this transfer function is extracted. The Bode plot data from the Simplis simulation is put into Mathcad file and compared with that of derived averaged model. In Figure 3.12, the blue curve is Simplis simulation result and the red one is obtained from Mathcad using the derived averaged model. It is noticed that at the switching frequency, both gain and phase have a little glitch in simulation result, whereas the derived model does not have. Except at this switching frequency and its multiples, the simulated result well agrees that of the derived general-purposed power stage averaged model.

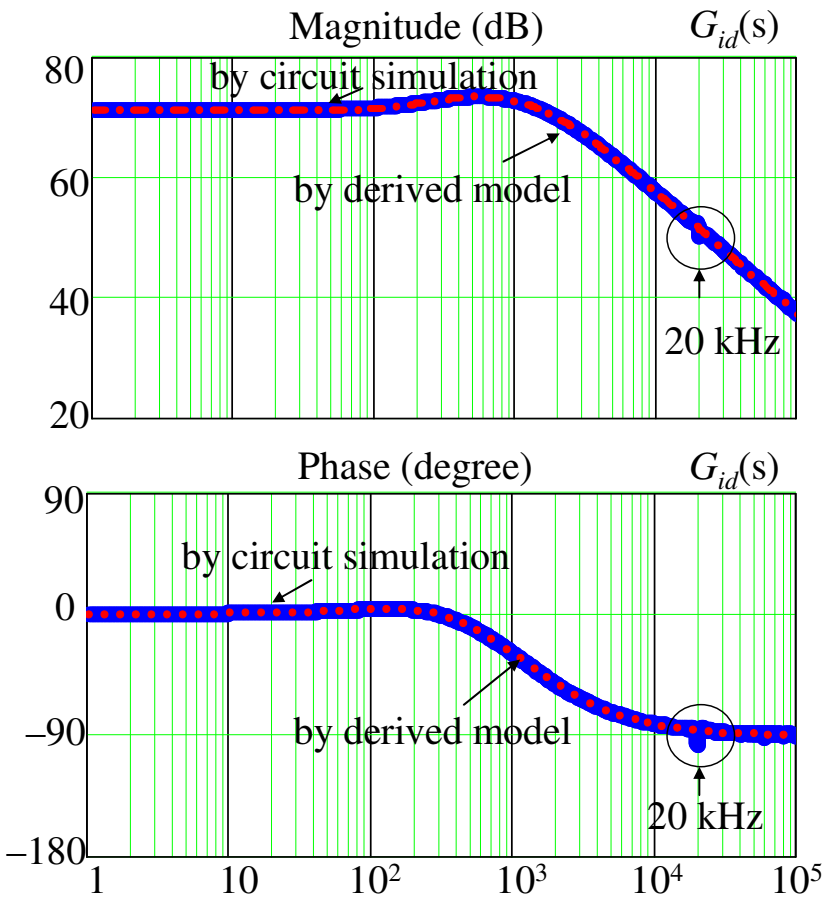


Figure 3.12 Derived averaged model verification for case 1

(blue-Simplis simulation curve, red-Mathcad derived averaged model)

(2) Model Verification at Frequency Domain Case 2

In Figure 3.12, the blue curve is Simplis simulation result and the red one is obtained from Mathcad derived averaged model. For the same reason as in (1), there is a noticeable glitch in both gain and phase of simulation result, whereas derived model does not have.

Table 3.4 Simulation parameters for model verification case 2

n	V_H (V)	V_L (V)	D	L_{equ} (μ H)	C_L (μ F)	f_{sw} (kHz)	R_{dson} (m Ω)	R_{Lequ} (m Ω)	R_1 (Ω)	R_2 (Ω)
2	233	115	0.45	10.25	150	20	8.7	8.8	1	1.1

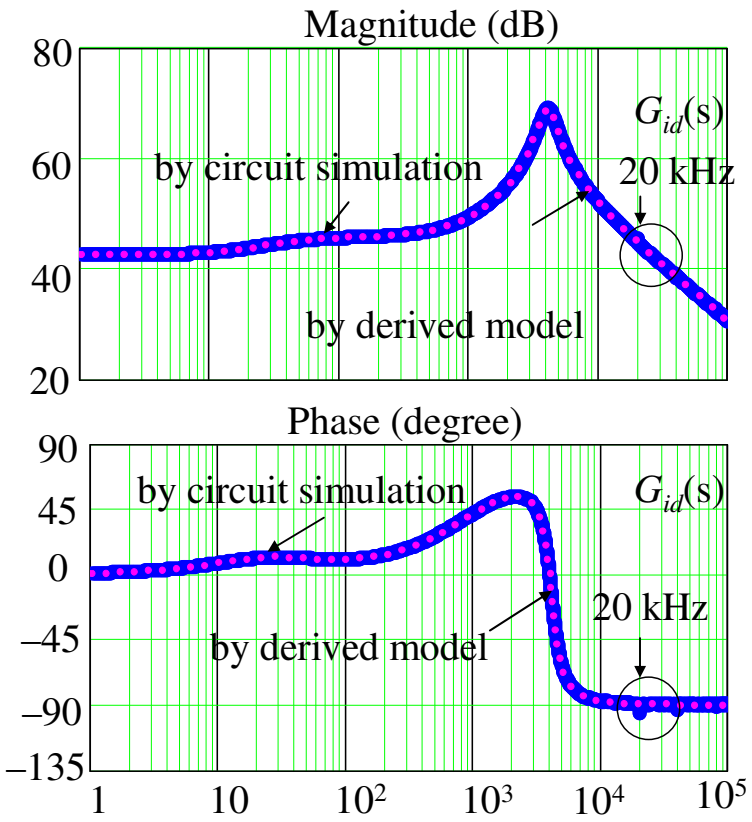


Figure 3.13 Derived model verification for case 2

(blue-Simplis simulation curve, red-Mathcad derived averaged model)

(3) Model Verification at Time Domain

The system time-domain simulation of switching model is compared with the averaged model. Figure 3.14 shows the comparison results where the output current i_o and inductor current i_L using both models. The inductor current i_L with averaged model follows its counterpart of switching model, so does the output current i_o. The agreement indicates that the averaged model can be used for the real system time domain performance analysis.

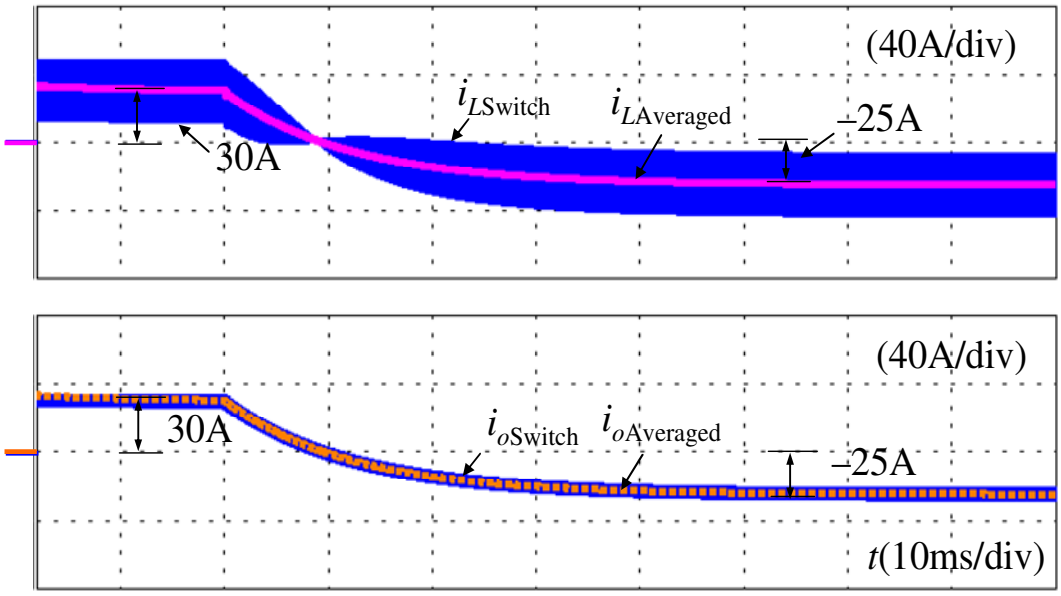


Figure 3.14 Averaged model and switch model simulation waveforms of inductor current i_L and output current i_o

3.4.3 Model Discussion

(1) Current Flow Direction Control

Equation (3.14) suggests that this is a third-order system, since there are three energy storage components including C_H, C_L and L. With this ac model, the relationships between high-side bus voltage v_1, low-side battery voltage v_2, inductor current i_L and duty cycle d are obtained. Since the buck charging and boost discharging current modes share the same power plant transfer function, they can share a unified controller. The defined inductor averaged current i_L reference flow direction is the same as the battery charging power flow direction. In Figure 3.15, it can be seen that the current flow direction of I_L only depends on the relationship between control duty cycle D and zero current duty cycle D_o, which is defined in (3.15). To charge the battery, inductor averaged current I_L should be greater than 0. According to (3.8), correspondingly duty cycle D should be adjusted to be greater than D_o. To discharge the battery, inductor averaged current I_L should be less than 0. Correspondingly, duty cycle D should be adjusted to be less than

D_o. The duty cycle can control the current flow direction. Inductor average current I_L is the same as the output current I_o, so the sign of I_o also can represent the current flow direction.

$$D_o = V_L / V_H \tag{3.15}$$

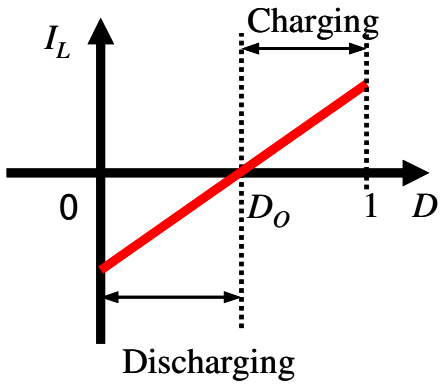


Figure 3.15 Duty cycle *D* versus inductor averaged current I_L

(2) Buck Mode with Resistive Load Converter Model

When the low side voltage V_L is zero, R_2 is treated as a resistive load and R_1 is negligible, the model derived in (3.14) behaves like a standard second-order buck converter model as shown in Figure 3.16.

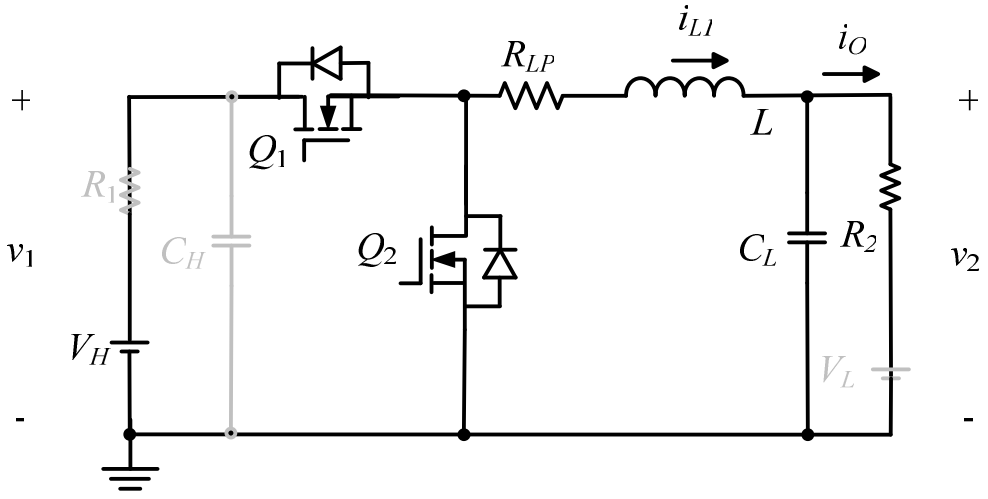


Figure 3.16 Buck mode with resistive load converter equivalent circuit

The state-space equations are shown in (3.16) -(3.19).

$$G_{id}(s)=\frac{\hat{i}_L}{\hat{d}}=\frac{(s+\frac{1}{C_L\cdot R_2})\cdot\frac{V_H}{L}}{(s+\frac{R_p}{L})\cdot(s+\frac{1}{C_L\cdot R_2})+\frac{1}{L\cdot C_L}} \tag{3.16}$$

$$I_L=\frac{D\cdot V_H}{R_2+R_P} \tag{3.17}$$

$$V_2=\frac{D\cdot V_H\cdot R_2}{R_2+R_P} \tag{3.18}$$

$$V_1=V_H \tag{3.19}$$

Duty cycle D_o here becomes zero due to zero value of low side voltage V_L. Duty cycle D is always greater than D_o, since D varies between zero and one. Therefore averaged inductor current is always greater than zero. So in (3.17), inductor averaged current I_L is always positive, which indicates the unidirectional current flow in buck mode.

(3) Boost Mode with Resistive Load

For boost resistive load, R_1 indicates a resistive load, where V_H does not exist. Battery internal resistance R_2 is as small as tens of mΩ, which means R_2 and C_L are negligible. At low frequency of less than kHz, the equivalent circuit is simplified into the one shown in Figure 3.17, which behaves like a second order system.

When the high-side voltage V_H is zero, R_1 is treated as a resistive load and R_2 is negligible, (3.14) is simplified into a standard second-order boost converter model. The state-space equations are shown in (3.20) -(3.23).

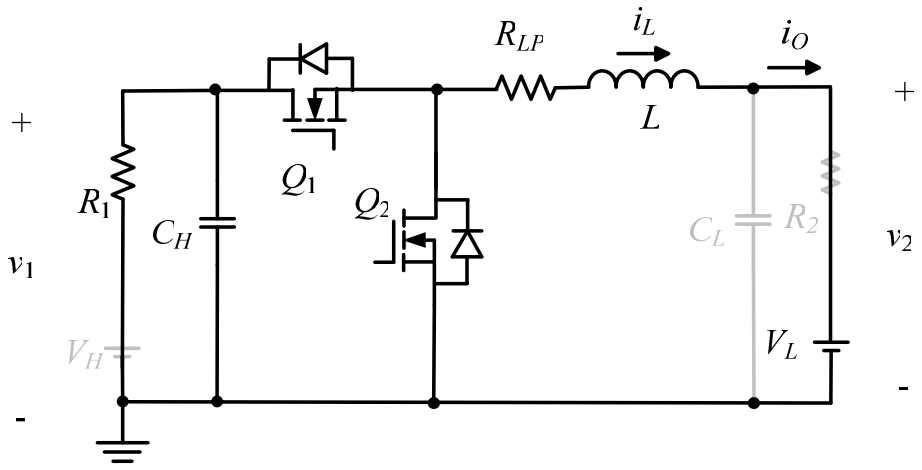


Figure 3.17 Boost mode with resistive load equivalent circuit

$$G_{id}(s)=\frac{\hat{i}_L}{\hat{d}}=\frac{(s+\frac{1}{C_H\cdot R_1})\cdot\frac{V_1}{L}-\frac{D\cdot I_L}{C_H\cdot L}}{(s+\frac{R_p}{L})\cdot(s+\frac{1}{C_H\cdot R_1})+\frac{D^2}{L\cdot C_H}} \tag{3.20}$$

$$I_L=\frac{-V_L}{R_1\cdot D^2+R_P} \tag{3.21}$$

$$V_1=\frac{D\cdot R_1\cdot V_L}{R_1\cdot D^2+R_P} \tag{3.22}$$

$$V_2=V_L \tag{3.23}$$

Duty cycle D_o here becomes infinite value due to zero value of high side voltage V_H. Duty cycle D is not always less than D_o, since D varies between zero and one. Therefore averaged inductor current is always less than zero. So in (3.21), inductor averaged current I_L is always negative, which indicates the unidirectional current flow in boost mode.

(4) Battery Load Converter

Normally battery internal resistance R_2 is as small as tens of mΩ, which is negligible because its voltage is much smaller than the voltage sources. The battery on the low side is also a strong voltage source. On the high side, there is a large capacitor bank C_H, if the

high side is treated as a voltage source, the equivalent third-order circuit can be simplified as the one shown in Figure 3.18. With only one inductor current as the state variable, the system behaves like a first-order system.

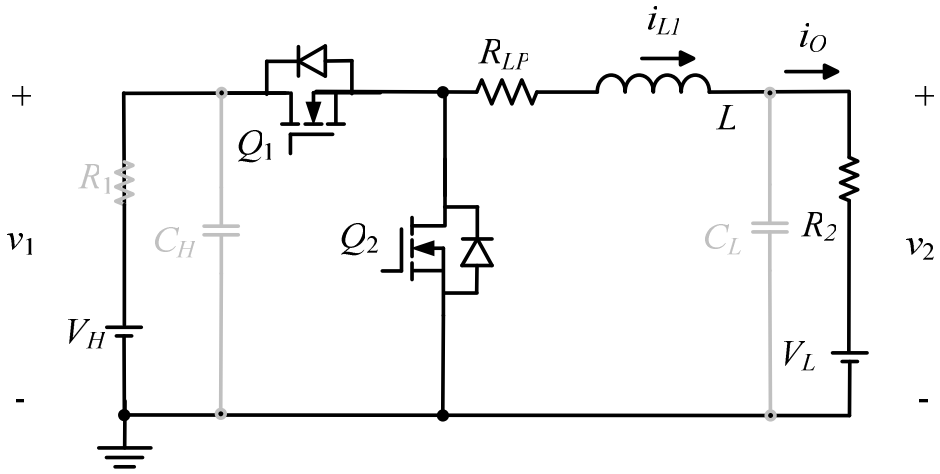


Figure 3.18 Battery load charging and discharging mode equivalent circuit

The state-space dc equations are shown in (3.24) and (3.25).

$$I_L = \frac{D \cdot V_H - V_L}{R_P + R_2} \tag{3.24}$$

$$G_{id}(s) = \frac{\hat{i}_L}{\hat{d}} = \frac{V_H}{L \cdot s + R_p + R_2} \tag{3.25}$$

Equation (3.24) shows that inductor steady-state averaged current I_L is affected only by system parameters R_P, R_2, V_H, V_L and the control variable D. In real application, R_P and R_2 are very small, so I_L will be very sensitive to the control signal D. From (3.25), it is noticed that control to inductor current transfer function G_{id} is not only related with V_H and battery internal resistance R_2, but also with system parasitic resistance R_P. In high power application, R_P is not negligible. For example, inductor parasitic resistance R_{lP} is as high as 36 mΩ and MOSFET APTM50AM17F conduction resistance R_{dson} is as high as 35-mΩ at high temperature condition. For four phases, the R_P is 18 mΩ (=(35+36) mΩ/4). This value is comparable with the battery resistance R_2, which varies from several μΩ to

several mΩ. Neglecting R_P will affect controller design. This equation has nothing to do with I_L, which allows the bidirectional current flow share exactly the same control-to-inductor current transfer function expression G_{id}(s). This essentially guarantees the current flow control transition smoothly.

3.4.4 Circuit Parameters in Different Modes

The general-purposed model can represent the models under different conditions including buck mode with resistive load, boost mode with resistive load and battery load charging and discharging modes. The parameters in different modes are summarized in Table 3.5. If all the circuit parameters are not negligible, the system model will be the third-order model.

Table 3.5 Parameters in different operation modes

Third order system	V_H	V_L	R_1	R_2	C_H	C_L
Buck mode with resistive load	V_H	0	0	R_2	0	C_L
Boost mode with resistive load	0	V_L	R_1	0	C_H	0
Battery load charging and discharging mode	V_H	V_L	0	R_2	0	0

3.5 Coupled Inductor Modeling

3.5.1 Coupled Inductor Introduction

Coupled inductor is introduced to reduce the core loss by flux ripple cancellation in the coupled inductor center leg. Inductor L_1 and L_2 are coupled together and L_3 and L_4 are coupled together as shown in Figure 3.19.

Figure 3.20 shows the complete timing diagram of four phase switches with duty cycle defined in buck mode. There are eight gate signals, Q_1-Q_8. The four gate signal pairs of Q_1-Q_2, Q_3-Q_4, Q_5-Q_6 and Q_7-Q_8 are complementary controlled. There are 90 degree phase shift between the four pairs.

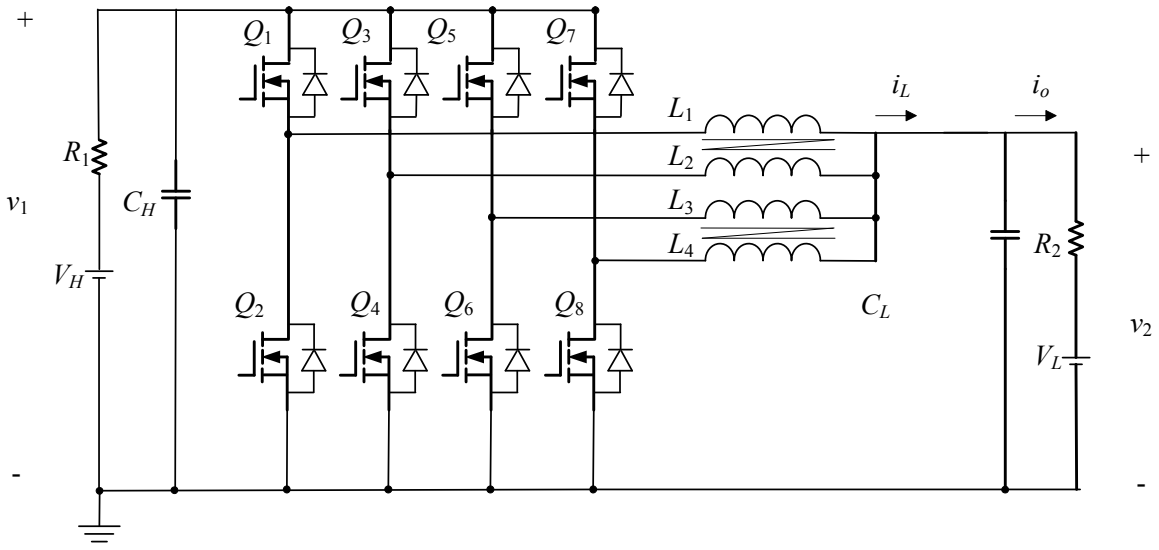


Figure 3.19 Four phases interleaved bidirectional converter with coupled inductors

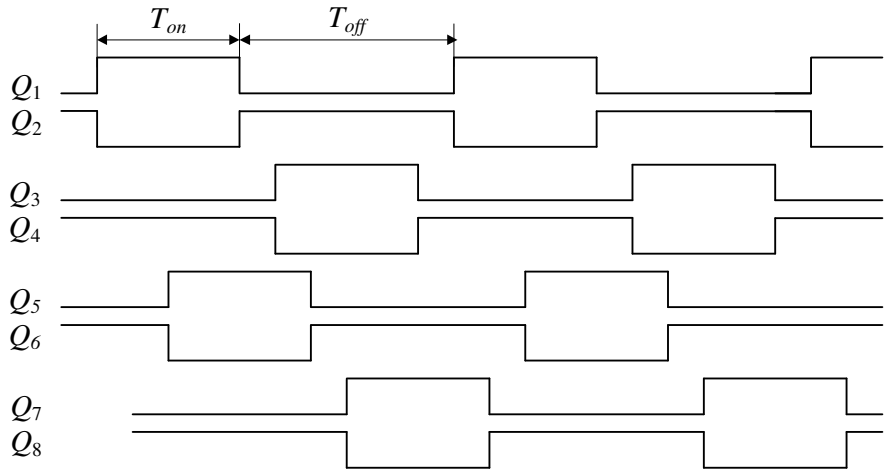


Figure 3.20 Timing diagram of the 4-phase bidirectional dc-dc converter with duty cycle defined in buck mode

3.5.2 Coupled Inductor State-space Modeling

To modeling the power stage, the inductance value is an important parameter for both controller design and inductor value selection.

One set of coupled inductor at duty cycle D<0.5 is cited as an example for the modeling analysis. Figure 3.21 is one leg duty cycle D and the other leg's is also D. They are 180 degree phase shift with each other. Each leg has two switches which are controlled by complementary gate signals.

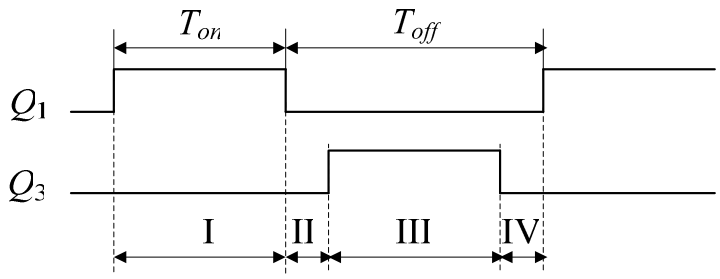


Figure 3.21 Control signal for coupled inductor

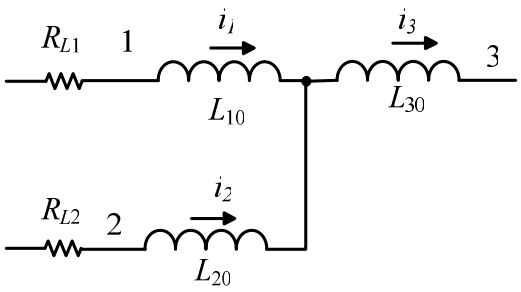
The coupled inductor equivalent circuit Y type model is shown Figure 3.22 (a). According to circuit principle, equivalent circuit Δ type model in Figure 3.22 (b) can also be used.

The inductance relationship between these two models is as follows.

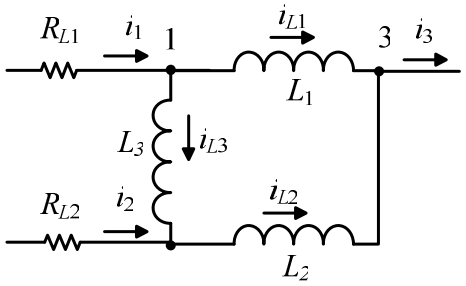
$$\begin{aligned} L_{10} &= L - M \\ L_{20} &= L - M \\ L_{30} &= M \end{aligned} \tag{3.26}$$

$$\begin{aligned} L_1 &= L + M \\ L_2 &= L + M \\ L_3 &= \frac{L^2 - M^2}{M} \end{aligned} \tag{3.27}$$

Where L is the inductance for one leg of coupled inductor and M is the mutual inductance. They can be defined by measurement of Y type model.



(a) Y type model



(b) Δ type model

Figure 3.22 Coupled inductor Y type and Δ type model

Based on the individual period, equivalent circuits are shown in Figure 3.23, Figure 3.24,

Figure 3.25 and Figure 3.26 respectively. The defined direction for inductor L_1 current i_{L1}, inductor L_2 current i_{L2}, and inductor L_3 current i_{L3} are depicted in Figure 3.22.

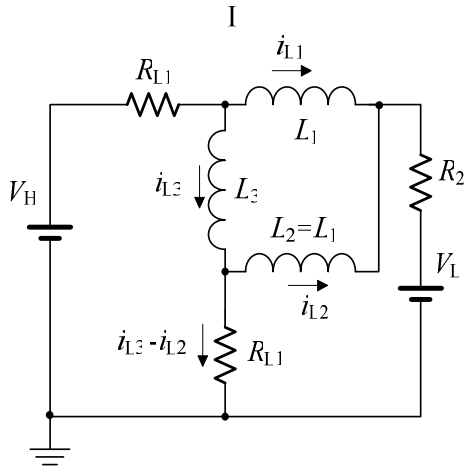


Figure 3.23 Phase I equivalent circuit

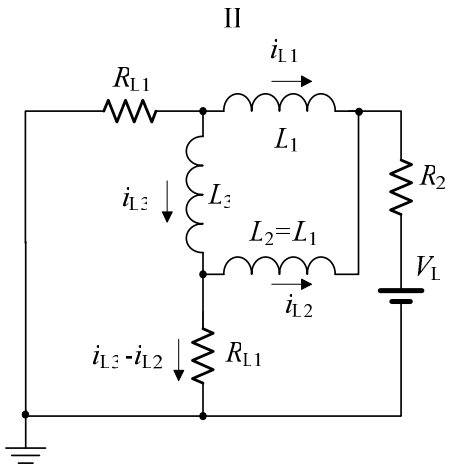


Figure 3.24 Phase II equivalent circuit

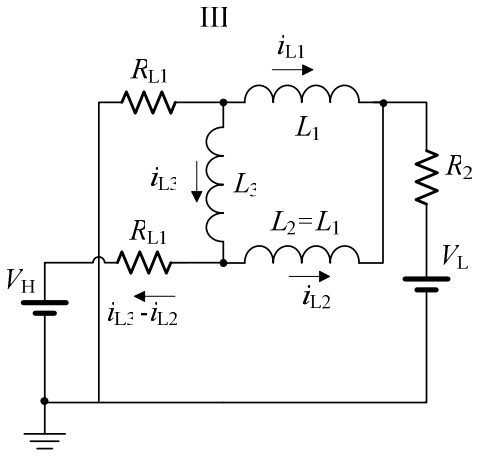


Figure 3.25 Phase III equivalent circuit

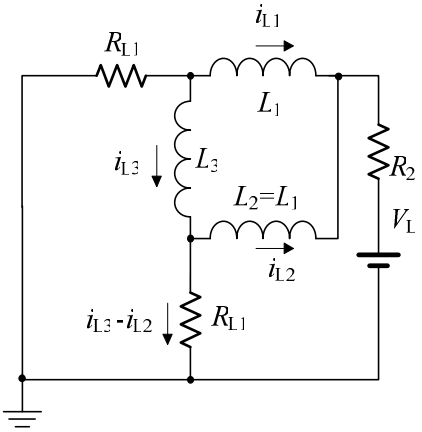


Figure 3.26 Phase IV equivalent circuit

(1) Phase I Equivalent Circuit and State-space State Equations

The state-space state equations for period I, where T is DT_{sw} is as shown in (3.28).

$$\begin{cases} V_H - V_L - (i_{L1} + i_{L3}) \cdot R_{L1} - R_2 \cdot (i_{L1} + i_{L2}) = L_1 \dfrac{di_{L1}}{dt} \\ V_H - (i_{L3} - i_{L2}) \cdot R_{L1} - (i_{L1} + i_{L3}) \cdot R_{L1} = L_3 \dfrac{di_{L3}}{dt} \\ (i_{L3} - i_{L2}) \cdot R_{L1} - V_L - (i_{L2} + i_{L1}) \cdot R_2 = L_1 \dfrac{di_{L2}}{dt} \end{cases} \tag{3.28}$$

(2) Phase II Equivalent Circuit and State-space State Equations

The state equations for period II, where $T = 0.5\ (1 - \mathrm{D})T_{sw,}$ is shown in (3.29).

$$\begin{cases} -V_L - (i_{L1} + i_{L3}) \cdot R_{L1} - R_2 \cdot (i_{L1} + i_{L2}) = L_1 \dfrac{di_{L1}}{dt} \\ -(i_{L3} - i_{L2}) \cdot R_{L1} - (i_{L1} + i_{L3}) \cdot R_{L1} = L_3 \dfrac{di_{L3}}{dt} \\ (i_{L3} - i_{L2}) \cdot R_{L1} - V_L - (i_{L2} + i_{L1}) \cdot R_2 = L_1 \dfrac{di_{L2}}{dt} \end{cases} \tag{3.29}$$

(3) Phase III Equivalent Circuit and State-space State Equations

The state equations for period III, where T is $DT_{sw,}$ is shown in (3.30).

$$\begin{cases} -V_L - (i_{L1} + i_{L3}) \cdot R_{L1} - R_2 \cdot (i_{L1} + i_{L2}) = L_1 \dfrac{di_{L1}}{dt} \\ -V_H - (i_{L3} - i_{L2}) \cdot R_{L1} - (i_{L1} + i_{L3}) \cdot R_{L1} = L_3 \dfrac{di_{L3}}{dt} \\ (i_{L3} - i_{L2}) \cdot R_{L1} + V_H - V_L - (i_{L2} + i_{L1}) \cdot R_2 = L_1 \dfrac{di_{L2}}{dt} \end{cases} \tag{3.30}$$

(4) Phase IV Equivalent Circuit and State-space State Equations

The state equations for period IV, where T is $0.5(1\text{-}D)T_{sw}$ is shown in (3.31).

$$\begin{cases} -V_L-(i_{L1}+i_{L3})\cdot R_{L1}-R_2\cdot(i_{L1}+i_{L2})=L_1\dfrac{di_{L1}}{dt} \\ -(i_{L3}-i_{L2})\cdot R_{L1}-(i_{L1}+i_{L3})\cdot R_{L1}=L_3\dfrac{di_{L3}}{dt} \\ (i_{L3}-i_{L2})\cdot R_{L1}-V_L-(i_{L2}+i_{L1})\cdot R_2=L_1\dfrac{di_{L2}}{dt} \end{cases} \tag{3.31}$$

Applying average method, the state-space averaging equation is summarized in (3.32) .

$$\begin{cases} DV_H-V_L-(R_{L1}+R_2)\cdot\overline{i_{L1}}-R_2\cdot\overline{i_{L2}}-R_{L1}\cdot\overline{i_{L3}}=L_1\dfrac{d\overline{i_{L1}}}{dt} \\ (\overline{i_{L1}}-\overline{i_{L2}}+2\overline{i_{L3}})\cdot R_{L1}=-L_3\dfrac{d\overline{i_{L3}}}{dt} \\ DV_H-V_L-R_2\cdot\overline{i_{L1}}-(R_{L1}+R_2)\cdot\overline{i_{L2}}+\overline{i_{L3}}\cdot R_{L1}=L_1\dfrac{d\overline{i_{L2}}}{dt} \end{cases} \tag{3.32}$$

The state equations of the DC model are shown in (3.33).

$$\begin{cases} DV_H-V_L-(R_{L1}+R_2)\cdot I_{L1}-R_2\cdot I_{L2}-R_{L1}\cdot I_{L3}=0 \\ (I_{L1}-I_{L2}+2I_{L3})\cdot R_{L1}=0 \\ DV_H-V_L-R_2\cdot I_{L1}-(R_{L1}+R_2)\cdot I_{L2}+I_{L3}\cdot R_{L1}=0 \end{cases} \tag{3.33}$$

Equations (3.33)can be further derived in (3.34) and (3.35).

$$I_{L1}=I_{L2}=\frac{DV_H-V_L}{R_2+R_{L1}/2} \tag{3.34}$$

$$I_{L3}=0 \tag{3.35}$$

The state equations of the ac model are,

$$\begin{cases} \hat{d}\cdot V_H - (R_{L1}+R_2)\cdot \hat{i}_{L1} - R_2\cdot \hat{i}_{L2} - R_{L1}\cdot \hat{i}_{L3} = L_1 \dfrac{d\hat{i}_{L1}}{dt} \\ (\hat{i}_{L1} - \hat{i}_{L2} + 2\hat{i}_{L3})\cdot R_{L1} = -L_3 \dfrac{d\hat{i}_{L3}}{dt} \\ \hat{d}\cdot V_H - R_2\cdot \hat{i}_{L1} - (R_{L1}+R_2)\cdot \hat{i}_{L2} + R_{L1}\cdot \hat{i}_{L3} = L_1 \dfrac{d\hat{i}_{L2}}{dt} \end{cases} \tag{3.36}$$

Equation (3.36) can be further derived into (3.37).

$$\frac{\hat{i}_{L1}+\hat{i}_{L2}}{\hat{d}} = 2\cdot\frac{\hat{i}_{L1}}{\hat{d}} = \frac{V_H}{L_{equ}\cdot s + R_2 + R_{Lequ}} \tag{3.37}$$

$$\hat{i}_{L3} = 0 \tag{3.38}$$

Where L_{equ}=1/2L_1 and R_{Lequ}=1/2R_L.

3.5.3 Model Verification

Simulations are made for both coupled inductor Δ type model as shown in Figure 3.27 and the simplified mode as shown in Figure 3.11.

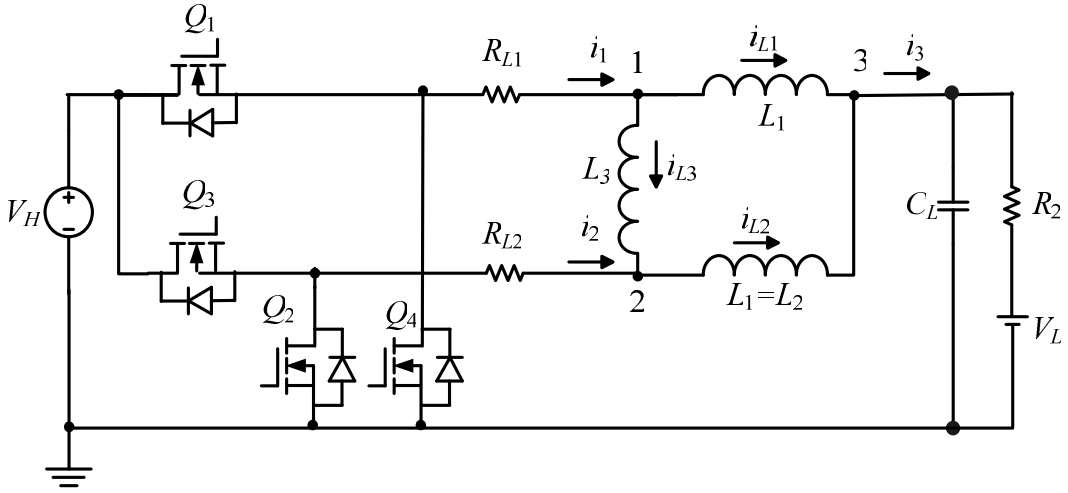


Figure 3.27 Coupled inductor Δ type model

Simulation result in Figure 3.28 indicates that the control-to-inductor current transfer function Bode plots of these two models agree with each other, which means the simplified equivalent inductance can represent real coupled inductor model for accurate dynamic performance analysis. This is also verified by reference [87]. The simulation parameters used here are listed in Table 3.6.

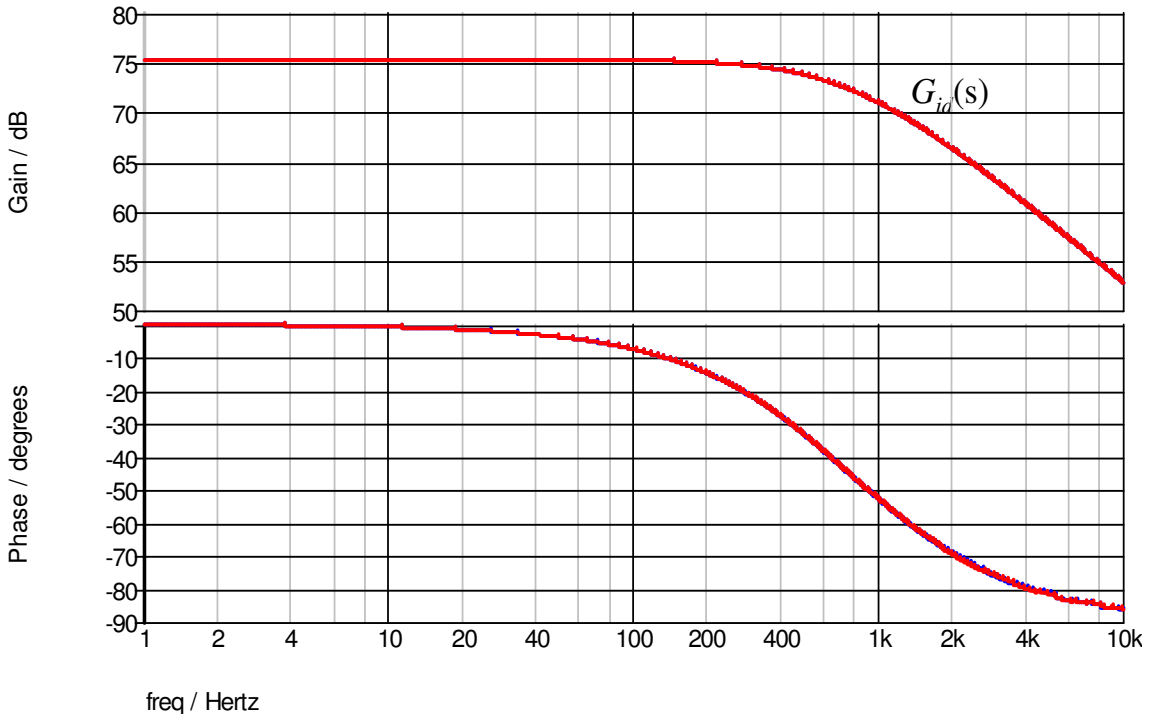


Figure 3.28 Bode plots of control-to-inductor current for coupled inductor Δ type model and simplified model

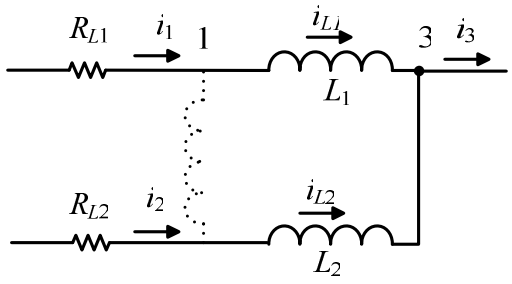
Table 3.6 Simulation parameters for coupled inductor model verification

n	V_H (V)	V_L (V)	L_1=L_2 (μH)	L_3 (μH)	L_{equ} (μH)	C_L (μF)	f_{sw} (kHz)	R_{dson} (mΩ)	R_2 (mΩ)	R_{l1}=R_{L2} (mΩ)	R_{Lequ} (mΩ)
2	280	120	20.5	–91	10.25	150	20	0	30	36	18

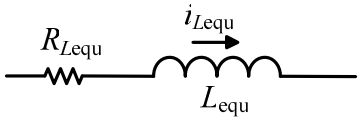
3.5.4 Model Discussion

(1) Equivalent Coupled Inductor Model

Equation (3.35) indicates that Δ-type coupled inductor current i_{L3} in the DC model I_{L3} is equal to zero, which means equivalently there is no voltage drop between DC voltage at point 1 and point 2. Equation (3.38) describes that ac current i_{L3} is equal to zero. This means the voltage second applied on inductor L_3 for each switching period is balanced naturally. Since the positive volt-second applied on the L_3 is equal to the negative volt-second applied on L_3, it is reasonable. Summarily speaking, the inductor L_3 does not exist, so circuit in Figure 3.22 (b) can be equivalent to circuit shown in Figure 3.29 (a) and be further simplified to circuit Figure 3.29 (b).



(a) Equivalent model



(b) Simplified model

Figure 3.29 Coupled inductor model

The coupled inductor equivalent value L_{equ} is L_1 or L_2 divided by 2 as shown in(3.37). Here L_1 is 20.5μH, therefore L_{equ} is 10.25μH. The equivalent parasitic inductor resistance R_{Lequ} in (3.37) is inductor resistance R_L of 36 mΩ divided by 2, which is 18 mΩ.

(2) Equivalent Circuit for Two Pairs of Coupled Inductor Interleaving Controlled

For four-phases interleave-controlled bidirectional converter, the equivalent inductor is the coupled inductor value L_1 divided by the phase number n, which is four here. The equivalent inductance is 5.125 μH, where L_1 is 20.5 μH.

3.6 Summary

A third-order general-purposed power stage averaged model for the bidirectional dc-dc converter is proposed and developed, since the bidirectional power plants share the same equivalent circuit. The model contains a voltage source on both high- and low-sides and three passive energy storage components. It is considered as a general-purposed model. If both ends are constant voltage sources, the complete model becomes a first-order system. If one of the voltage sources is replaced with a resistive load, the transfer function becomes a second-order system.

This general-purposed power stage averaged model makes it possible to design and optimize a unified controller for bidirectional current flow control and smooth mode transition, instead of compromising two controllers.

The Δ-type equivalent circuit clearly shows physical meaning of the coupled inductor. The dynamic and steady-state current of the paralleled-branch inductance i_{L3} and I_{L3} are zero, which indicates that the inductance L_3 can be eliminated from the averaged sense point of view. Thus, the overall equivalent coupled inductor model is the individual inductance, L_1 or L_2, divided by 2, where L_1 and L_2 equal to the self inductance plus the mutual inductance, or $L+M$. Such a simplified equivalent coupled inductor model allows coupled inductor design and frequency domain analysis for controller design.

The proposed general-purposed power stage and the coupled inductor equivalent models have been verified by Simplis ac analysis simulation.

Chapter 4 Unified Controller Design, Digital Implementation and Resistive Load Tests

4.1 Introduction

The analog implementation is difficult to synchronize multiple phases PWM signals and generate precise PWM duty cycle because of the different performance of the discrete components. Digital controller is preferred to generate multiphase interleaved gate signals. It has good noise immunization, which is important in high power application. In addition, the analog implementation tends to have difficulties in mode transition, because the error amplifier of the preferred mode can be saturated during the transition [44]. Digital controller can be easily set to reduce or avoid the delay out of the saturation in the transition. With accurate digital control and relatively high parasitic resistance in high power application, current in each phase can be easily balanced. Thus the digital controller is adopted and implemented in the proposed effort.

Using the general-purposed power stage models proposed in chapter 3, a unified controller design methodology will be described in this chapter. The basic concept of a unified controller is proposed and explained in section 4.2. With the general-purposed third-order transfer functions $G_{id}(s)$ derived in section 3.4.1, the unified controller can be developed and used to control either resistive load or bidirectional charging. In the initial tests, a resistive load is employed. The system filter design will be discussed in section 4.3.2, and the delay effect on the system transfer function will be discussed in section 4.3.3. Based on these design considerations, the design approach of the unified controller $C_i(s)$ under resistive load conditions will be described in 4.4. After the unified controller $C_i(s)$ is discretized into $C_i(z)$ in section 4.5, a digital controller implementation will be described in section 4.6. The proposed unified controller has been tested, and the simulation and test results will be provided in section 4.7. Section 4.8 will summarize the unified controller design and implementation.

4.2 System Structure and Unified Controller

4.2.1 System Structure

The system diagram is shown in Figure 4.1. The control feedback current i_o is sensed from the power stage and fed back through RC filter to the control circuit. The signal after filter is compared with reference I^*, and the error signal is regulated by the controller. After a certain system delay, the PWM duty cycle is generated by the controller and sent out to the gate drive boards to obtain all gate signals G_1-G_8 for a total of eight switches. The gate signals will drive the power MOSFET Q_1-Q_8 to producing the desired output power.

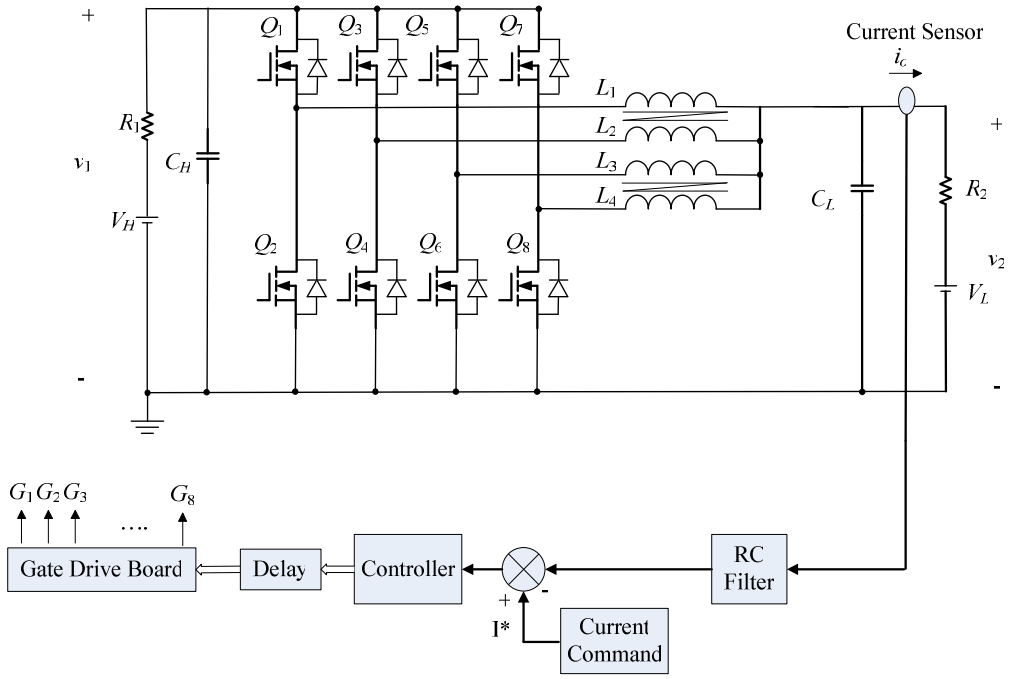


Figure 4.1 System Structure

4.2.2 Unified Controller Concept

In order to simplify the controller and at the same time stabilize the system during the mode transition, a unified controller is proposed. A current mode controller is cited as an example. Figure 4.2 shows that traditional way of two separate controllers: buck and

boost controllers. The reference currents I_{L1}* and I_{L2}* are provided by the power management command separately. The mode switch between two different modes is manipulated by a power management command.

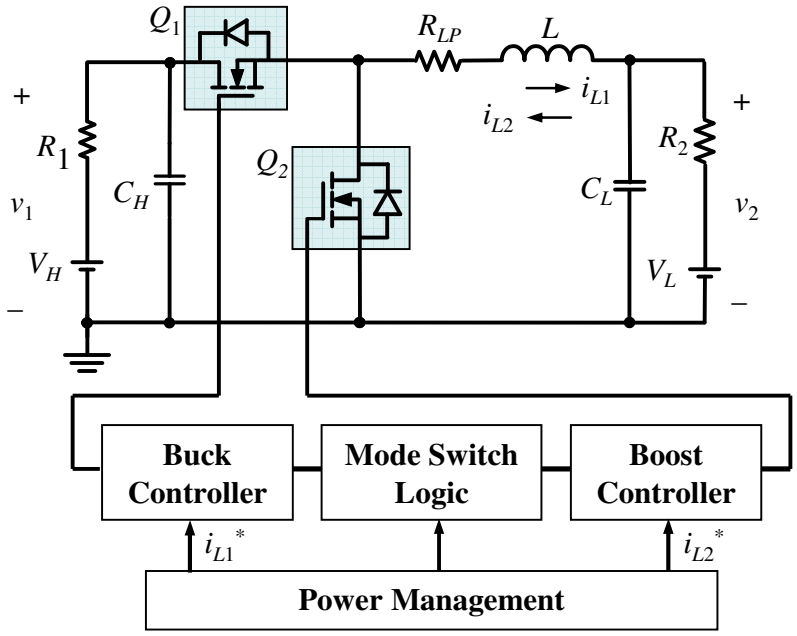


Figure 4.2 Separate controllers controlled power stage

These two controllers can be merged into one with complementary switching, as shown in Figure 4.3. Instead of individual controllers for each mode shown in Figure 4.2, a unified controller is realized. Different current flow directions represent different modes. The control signal shown in Figure 4.4 (a) and (b) indicate that if the buck mode charging current is set to be positive boost mode discharging current will be negative. In this way, the charging and discharging mode is naturally controlled only by a reference current I_L^* setting in positive and negative values respectively instead of forcefully by the power management logic. This essentially avoids the severe transient during the mode change.

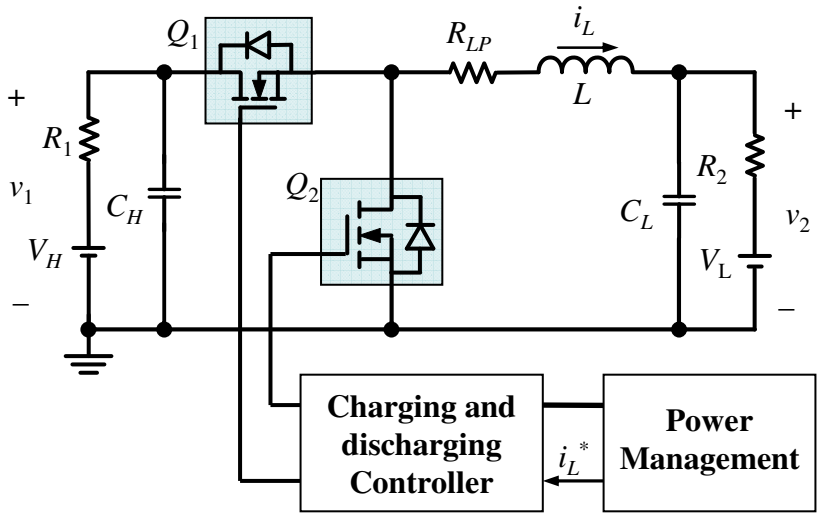


Figure 4.3 Unified controller controlled power stage

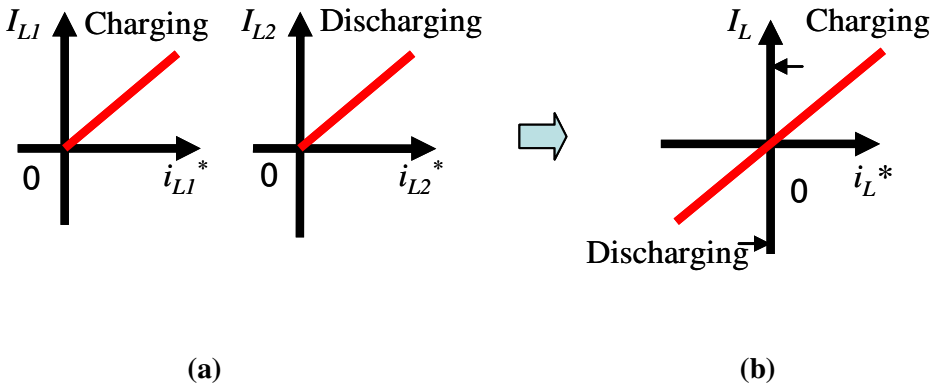


Figure 4.4 Separate controller and unified controller

(a) Control signal in separate controllers (b) Control signal in unified controller

4.3 Controller Design Considerations

4.3.1 Current Sensing Point Discussion

To control the averaged current, there are two possible sensing points. One is the inductor current i_L sensing point, and the other is the output current i_o sensing point, as shown in Figure 4.5. The selection of the sensing point will affect the controller design

and performance. This section will show the effective feedback signal for averaged current mode control for different load conditions.

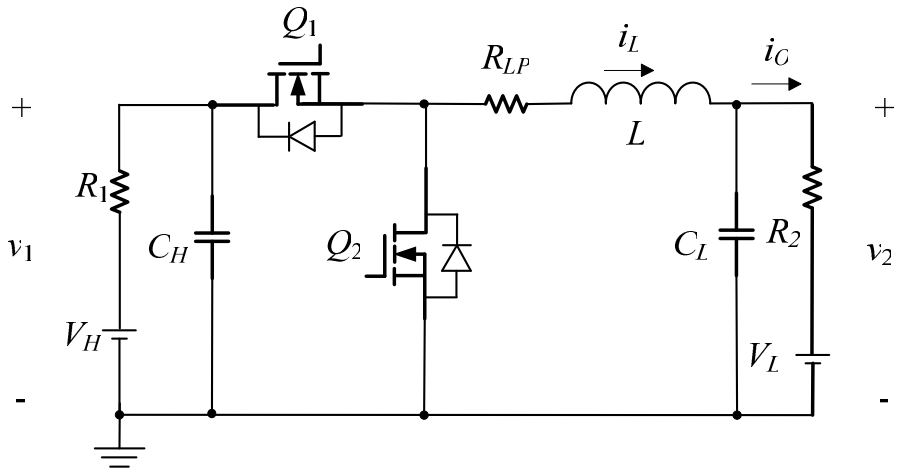


Figure 4.5 Two different current sensing points for inductor current i_L and output current i_o

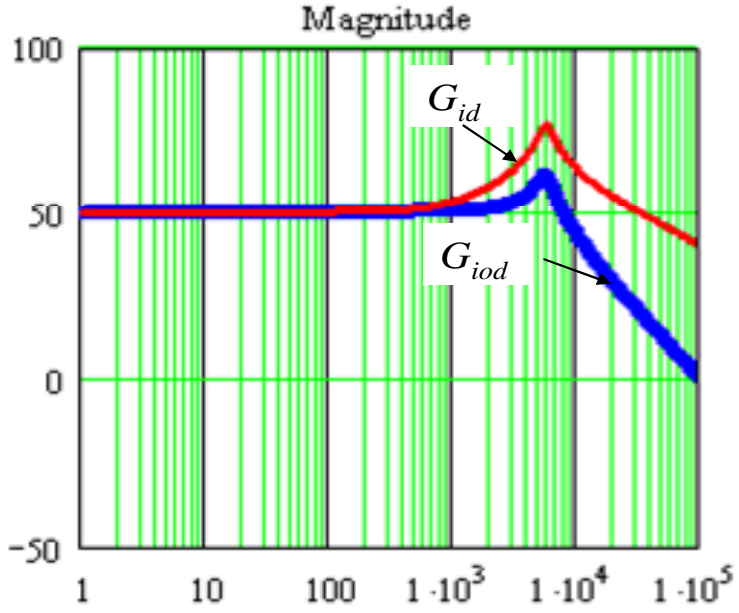
(1) Power Plant Transfer Functions $G_{id}(s)$ and $G_{iod}(s)$

Control-to-inductor current transfer functions $G_{id}(s)$ for different modes are discussed in section 3.4.3. For buck resistive load, transfer function $G_{id}(s)$ in (3.16) can be expressed in (4.1). Control-to-output current transfer function $G_{iod}(s)$ is expressed in(4.2).

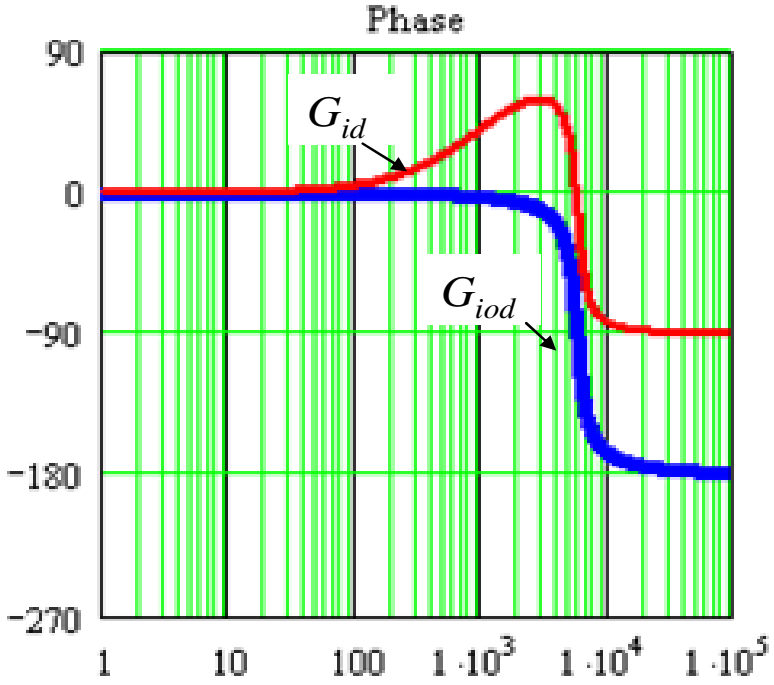
$$G_{id}(s) = \frac{V_H \cdot (C_L \cdot R_2 \cdot s + 1)}{L \cdot s + R_P + R_2 + R_2 \cdot C_L \cdot s \cdot (L \cdot s + R_P)} \tag{4.1}$$

$$G_{iod}(s) = G_{id}(s) \cdot \frac{1}{C_L \cdot R_2 \cdot s + 1} = \frac{V_H}{L \cdot s + R_P + R_2 + R_2 \cdot C_L \cdot s \cdot (L \cdot s + R_P)} \tag{4.2}$$

Figure 4.6 shows the Bode plots of two transfer functions $G_{id}(s)$ and $G_{iod}(s)$. The specification for these two Bode plots is listed in Table 4.1.



(a)



(b)

Figure 4.6. Bode plots of the two sensing current i_L and i_o versus control signal d

Control-to-output current G_{iod}(s) differs from the control-to-inductor current transfer function G_{id}(s) with a low-pass filter consisting of R_2 ·and C_L. In other words, G_{iod}(s) has

an additional pole as compared to G_{id}(s). The larger load resistor R_2, the slower response G_{iod}(s) will present. However, that does not always mean the use of inductor current i_L has more advantage than output current i_o as averaged current feedback signal. Section 4.3.2 will show another aspect of the two sensing points.

Table 4.1 Specification for Figure 4.6

Lable	V_H=V_1 (V)	R_2(Ω)	R_P(Ω)	C_L(μF)	L(μH)
G_{id}	350	1.5	0.018	150	5.1
G_{iod}	350	1.5	0.018	150	5.1

(2) Current Ripple Effect

Figure 4.7 indicates that the current ripples at the two different sensing points are significantly different. At average current of 23 A, inductor total current i_L has around 17 A peak-to-peak current ripple, whereas the output current i_o is a very straight and clean. The inductor ripple needs to be filtered out by the subsequent analog RC(s) filter and digital BF(s) filter.

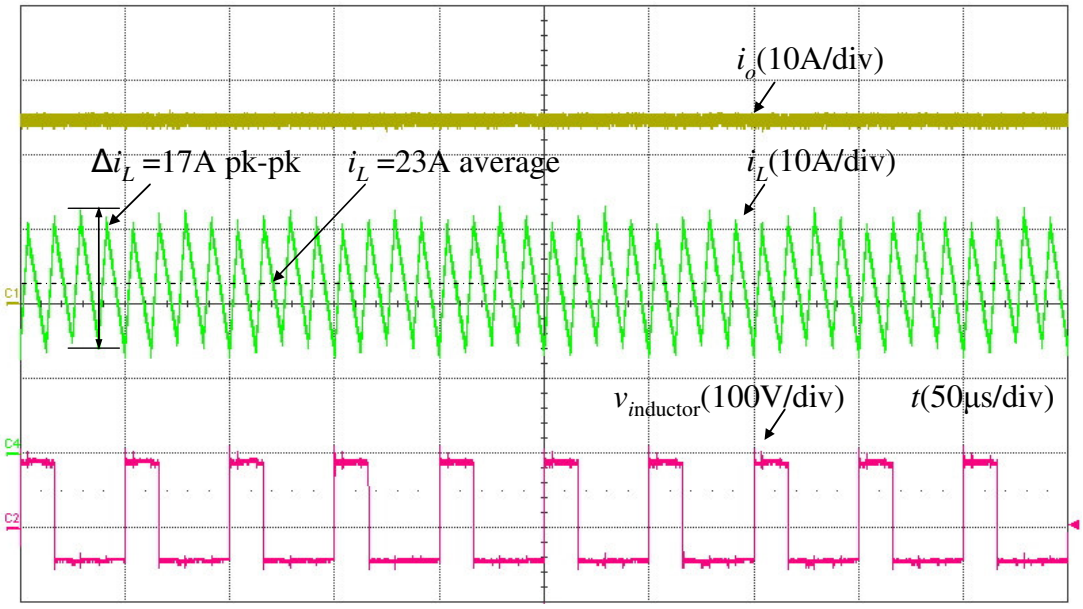


Figure 4.7 Different current sensing points

(3) Discussion

In our original test, resistive load is employed, so the delay caused by the R_2-C_L filter is long. The control-to-output current i_o has much lower frequency response than inductor current i_L, which affects the system feedback loop response. Therefore, sensing inductor current i_L is a good choice. The high current ripple can be filtered out with a proper filter, which provides enough attenuation and at the same time maintains frequency response as high as possible. The filter design will be discussed in section 4.3.2.

4.3.2 Filter Design

Figure 4.7 indicates inductor total current I_L has large ripples. Inductor current ripple frequency of four phases interleaving waveform has four times of the switching frequency, but the asymmetry of the inductance among four phases makes switching frequency component still exist. Therefore, a filter with low cut-off frequency is needed to effectively eliminate the ripple. The cut-off frequency should be lower than the switching frequency,

(1) Analog *RC(s)* Filter

A 2nd order RC(s) filter expressed in equation (4.3) is designed and applied. It not only eliminates the large ripple, but also works as an analog anti-alias filter for 20 kHz sampling frequency. The crossover frequency f_c is 5.3 kHz, which is low enough to reduce the higher frequency ripple.

$$RC(s) = \frac{1}{(1+\frac{s}{2\cdot\pi\cdot f_c})^2} \tag{4.3}$$

The *RC*(s) filter is a 2nd order KRC filter. The structure is shown in Figure 4.8.

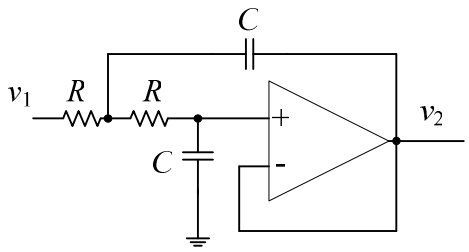


Figure 4.8 A KRC 2nd order filter

(2) Digital Filter BF(s)

A certain physical distance exists from the feedback point to the DSP A/D even if it is minimized purposely. Software filter *BF*(s) is designed to filter out the relatively high frequency noise pick-up on the path from analog filter *RC(s)* to A/D sampling. Here cutoff frequency f_c of 8 kHz indicated in equation (4.4) is selected.

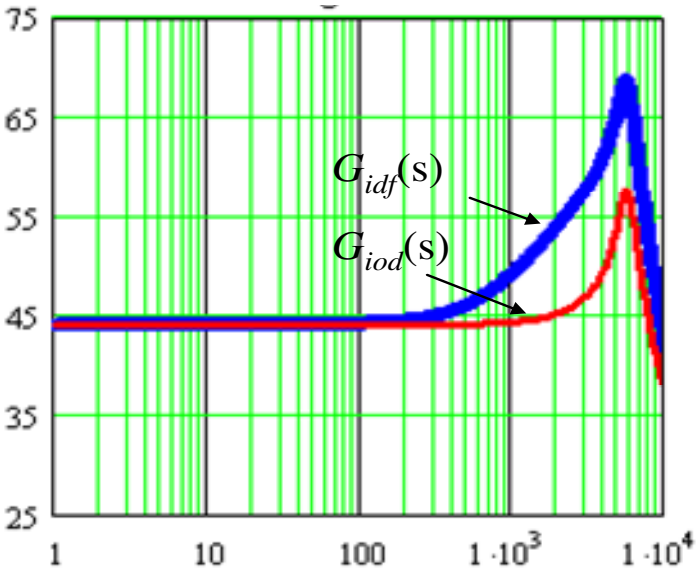
$$BF(s) = \frac{1}{1 + 1.414 \cdot \frac{s}{2 \cdot \pi \cdot f_c} + \left(\frac{s}{2 \cdot \pi \cdot f_c} \right)^2} \tag{4.4}$$

(3) Transfer Function Comparison for Different Sensing Points

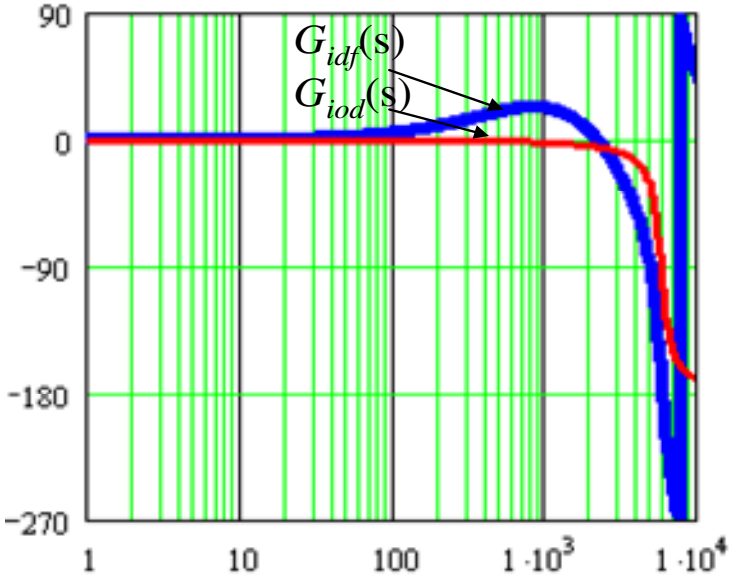
As discussed in section 4.3.1, for resistive load, since inductor current i_L has much faster response, it is a good feedback sensing signal. The large ripple in inductor current i_L can be filtered out by analog filter *RC*(s) with a cutoff frequency of 5.3 kHz and by digital filter *BF*(s) with a cutoff frequency of 8 kHz. The transfer function including the filter is expressed in (4.5). The control-to-output current transfer function G_{iod}(s) is expressed in (4.6). Compared with sensing point of output current i_o, G_{idf}(s) has less phase lag than G_{iod}(s) within the frequency range of 100 Hz to 2 kHz as shown in Figure 4.9. That is understandable. If resistive load R_2 is larger, the delay caused by output is longer. In this case, inductor current i_L as feedback signal has better performance.

$$G_{idf}(s) = G_{id}(s) \cdot RC(s) \cdot BF(s) \tag{4.5}$$

$$G_{iod}(s) = G_{id}(s) \cdot \frac{1}{C_L \cdot R_2 \cdot s + 1} \tag{4.6}$$



(a) Magnitude



(b) Phase

Figure 4.9 Bode plots of control-to-inductor current and control-to-output current for resistive load

4.3.3 System Delay Effect

The whole system is digitally implemented, which will be discussed in Chapter 5. The sampling and computational delays with digital control are unavoidable and should be considered in the controller design. There are three types of delay.

(1) ADC Sampling Delay E_1(s)

First one is ADC sampling delay, which is as small as in sub-micro second range and can be ignored.

(2) Computation Delay E_2(s)

The second delay is caused by computation time E_2(s), which affects the system frequency response and should be considered in the design. The best way to avoid this unfavorable effect is to get it as short as possible. From Figure 4.10[91], it is noticed that the value after the ADC sampling and filter enters into the interrupt service routine (ISR) in the middle of PWM period. This value will be processed to produce the PWM duty cycle within the second half PWM switching cycle. The produced PWM duty cycle will be effective in the following PWM period. In this implementation, delay time, as indicated in Figure 4.10, is equal to half of the PWM switching period T_{sw}.

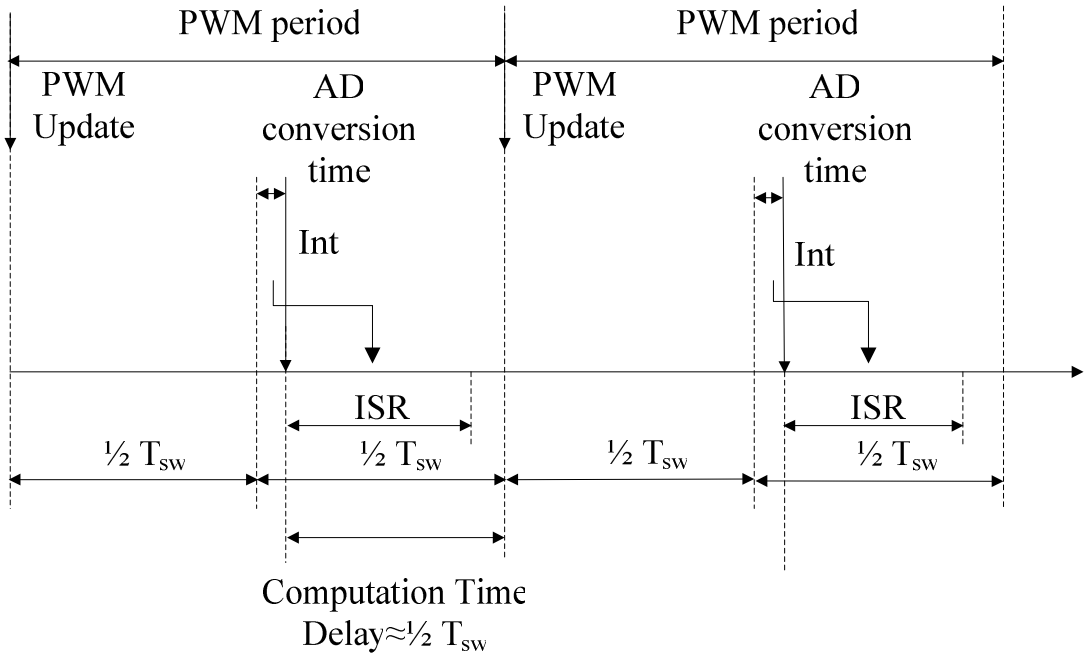


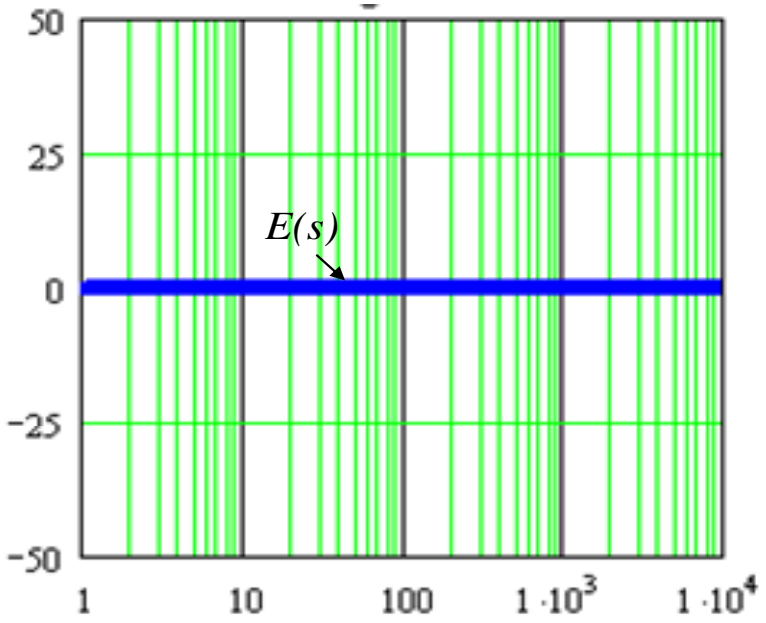
Figure 4.10 Computation time delay $E_2(s)$ explanation

(3) PWM Modulator Sampling Delay $E_3(s)$

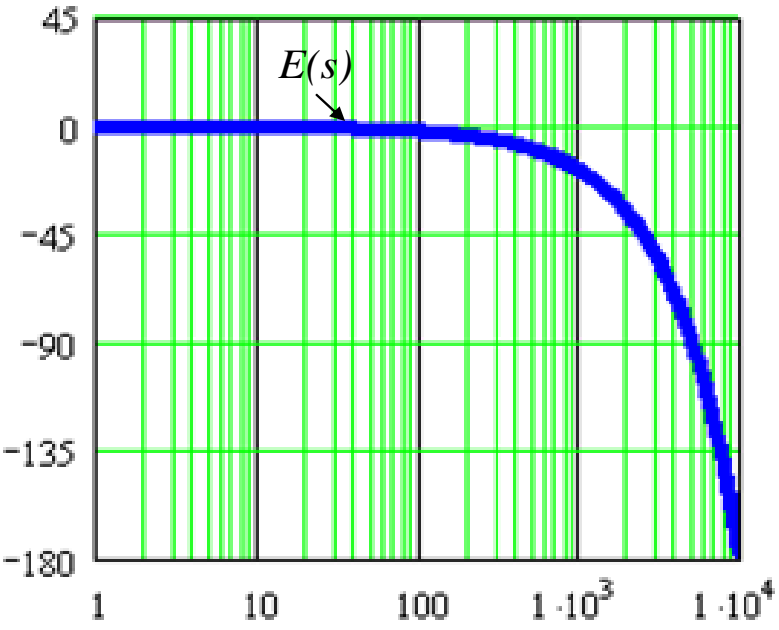
The last delay is PWM modulator uniform sampling delay $E_3(s)$. It is related with duty cycle, so it is hard to accurately predict. For average sense, it is half of PWM switching period T_{sw}.

The transfer function of total delay effect is expressed in (4.7). Its Bode plot is shown in Figure 4.11. With the PWM switching frequency of 20 kHz, the delay causes 18 degree phase lag at frequency of 1 kHz.

$$E(s) = E_2(s) \cdot E_3(s) = e^{-0.5 \cdot T_{sw} \cdot s} \cdot e^{-0.5 \cdot T_{sw} \cdot s} = e^{-T_{sw} \cdot s} \tag{4.7}$$



(a) Effect on gain



(b) Effect on phase

Figure 4.11 Delay effect versus frequency

4.4 Unified Controller C_i(s) Design for Resistive Load

An averaged current mode controller for resistive load will be designed and tested to verify the modeling and the unified controller concept.

4.4.1 Loop Gain Transfer Function Ti(s)

The above discussion indicates that for resistive load, the control loop gain T_i(s) of the system includes control-to-inductor current i_L transfer function G_{id}(s), analog filter RC(s), digital filter BF(s), system delay effect E(s) and controller C_i(s). The expression is given in (4.8). System control block diagram is shown in Figure 4.12.

$$T_i(s) = G_{id}(s) \cdot RC(s) \cdot BF(s) \cdot E(s) \cdot C_i(s) \tag{4.8}$$

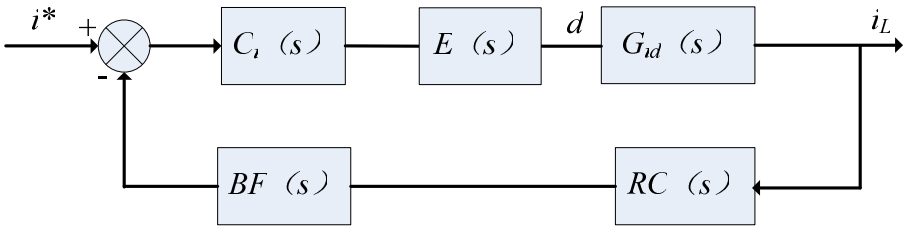


Figure 4.12 System control block diagram for resistive load

4.4.2 Resistive Load Control-to-inductor Current Transfer Function G_{id}(s)

The design conditions are shown in Table 4.1. Each phase inductor value is 25 μH. For four phases, the equivalent inductor value is 25 μH divided by 4, which is 6.25 μH.

Table 4.2 Test parameters

n	L (μH)	C_H (mF)	C_L(mF)	f_{sw} (kHz)	R_{dson} (mΩ)	R_{lP}(mΩ)
4	25/4	7.2	7.2	20	35	36

The buck and boost test conditions are shown in Table 4.3 and Table 4.4 respectively. Their test conditions include input voltage V_H for buck mode or V_L for boost mode, inductor reference current I^*, output voltage V_2 for buck mode or V_1 for boost mode, resistor load R_2 for buck mode or R_1 for boost mode and output power P_o. It should be noticed that a positive current setting is given for charging mode and negative current setting is given for discharging mode.

Table 4.3 Resistive load buck mode test conditions

Case No.	$V_H=V_1$ (V)	V_L(V)	V_2 (V)	I^* (A)	R_2(Ω)	R_1(Ω)	P_o(kW)
1	250	0	150	50	3	0	7.5
2	250	0	75	50	1.5	0	3.75

Table 4.4 Resistive load boost mode test conditions

Case No.	V_H (V)	$V_L=V_2$(V)	V_1 (V)	I^* (A)	R_2(Ω)	R_1(Ω)	P_o(W)
3	0	60	81	-12	0	9	720
4	0	60	114	-12	0	18	720

Control-to-inductor current transfer function Bode plots G_{id}(s) for four cases are shown in Figure 4.13. Transfer function for buck mode is similar to that for boost mode.

4.4.3 Controller Structure

According to the transfer function, the controller structure in (4.9) is selected. An integrator is added to get high dc gain and a pole ω_{p1} is added to render the loop gain run across the 0 dB with 20 dB/decade slope, which allows enough phase margins to be developed after crossover frequency. Two zeros ω_{z1} and ω_{z2} are expected to increase the phase margin around the crossover frequency.

$$C_i(s) = \frac{C_0 \cdot (1+\frac{s}{\varpi_{z1}}) \cdot (1+\frac{s}{\varpi_{z2}})}{s \cdot (1+\frac{s}{\varpi_{p1}})} \tag{4.9}$$

where ω_{z1}=400·2π, ω_{z2}=700·2π , ω_{p1}=30·2π, C_0=3.276.

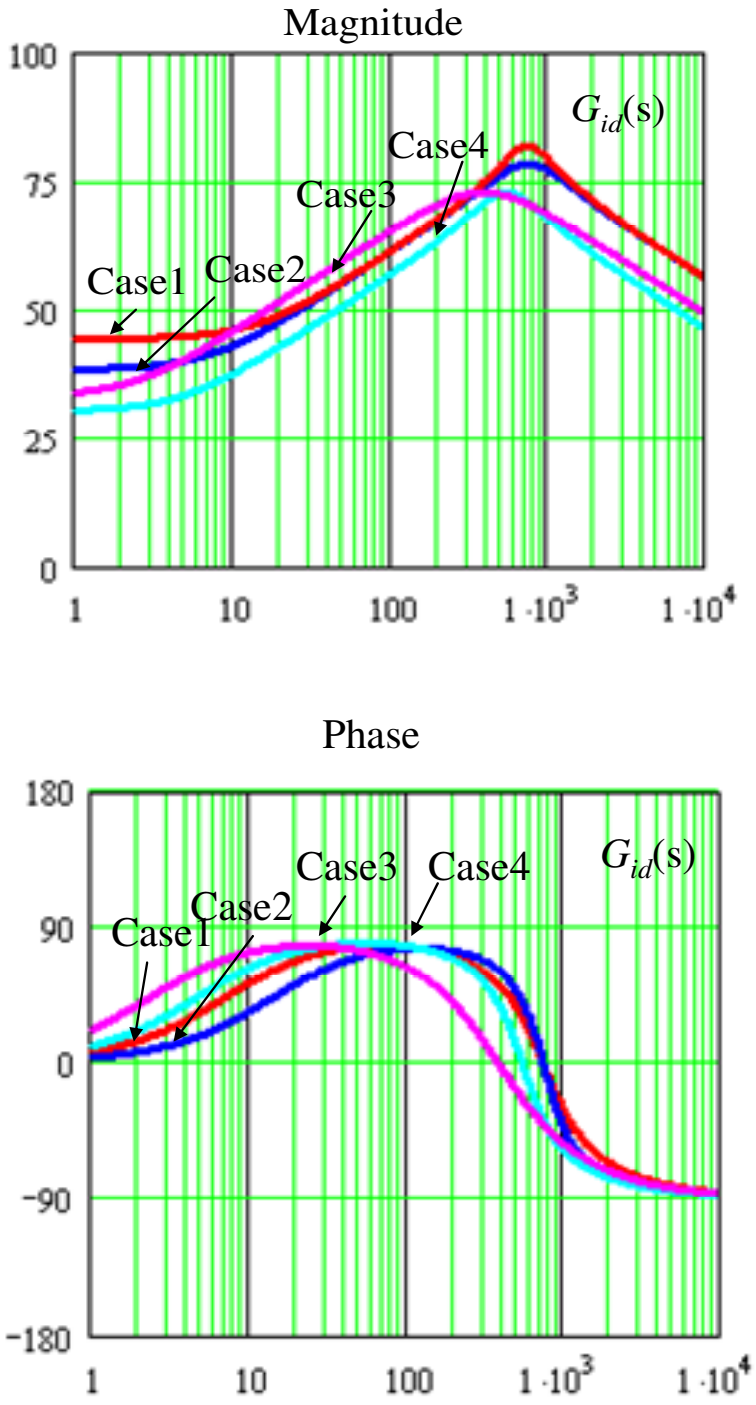


Figure 4.13 Bode plots of control-to-inductor current G_{id}(s) for resistive load

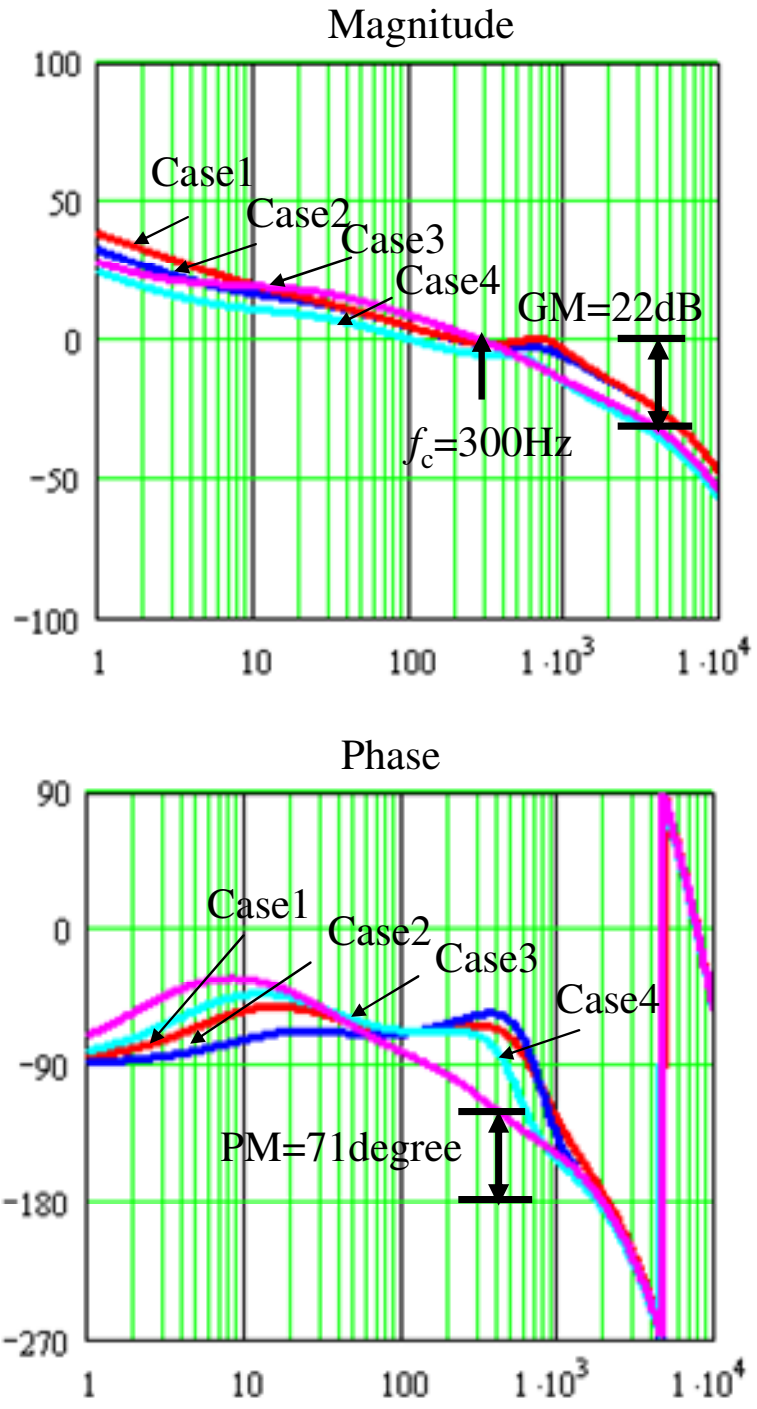


Figure 4.14 Bode plots of current loop gain T_i(s) for resistive load

4.4.4 Design Results

Case No.3 has most phase lag among the group, so it is the worst case. Controller design is based on this case and is verified by the other cases. The Bode plots of the loop gain T_i(s) are as shown in Figure 4.14. The design results are shown in Table 4.5. The worst case No.3 has the least phase margin of 72 degree and crossover frequency f_c of 105 Hz.

Table 4.5 Design results

Case Number	Phase Margin PM(degree)	Gain Margin GM(dB)	Crossover frequency f_c (Hz)
1	115	15.6	210
2	119	13.7	220
3	71.7	22.4	300
4	113	23.5	105

4.5 Digital Controller

4.5.1 Digital Controller Introduction

DSP controller with the core chip DSP TMS320F2808 is developed. Four enhanced PWM modules (ePWM) are involved for interleaved-control gate signals for the four-phase bidirectional dc-dc converter. The clock frequency can be as high as 100 MHz, so the PWM frequency of 20 kHz can be precisely controlled. ADC conversion rate can be as fast as 200 ns with a frequency of 5MSPS (meg samples per second). The PWM trip-zone (TZ) function is utilized to protect the system from the failure caused by major short circuits or over-current conditions.

As discussed previously, the originally designed controller, C_i(s), is for resistive load application and an alternatively designed controller, C_{io}(s), which will be discussed in

Chapter 5, is for battery load application. Here C_i(s) is cited as an example to explain how the controller is digitally implemented.

4.5.2 Unified Controller Discretization

The controller C_i(s) obtained above has a structure shown in (4.10). Tustin method is used for z-transformation because it preserves stability and minimum-phase for both gain and phase properties of the controller below 1/10 of the sampling frequency [88]. With the Tustin bilinear transformation method, the following (4.12) is derived with sampling time T_{sa} of 50 μs.

$$C_i(s) = \frac{C_0 \cdot (1+\frac{s}{\varpi_{z1}}) \cdot (1+\frac{s}{\varpi_{z2}})}{s \cdot (1+\frac{s}{\varpi_{p1}})} \tag{4.10}$$

Where ω_{z1}=400·2π, ω_{z2}=700·2π , ω_{p1}=30·2π, C_0=3.276.

$$s = \frac{2}{T_{sa}} \cdot \frac{z-1}{z+1} \tag{4.11}$$

$$C_i(z) = \frac{b_2 \cdot z^{-2} + b_1 \cdot z^{-1} + b_0}{-a_2 \cdot z^{-2} - a_1 \cdot z^{-1} + 1} \tag{4.12}$$

Where b_0= 0.000065692731219, b_1= –0.000110434470553, b_2= 0.000046378772, a_1= 1.990619426948309, a_2= –0.990619426948309.

With Matlab, the difference caused by the transformation mapping can be easily predicted. For example, substituting (4.11) for z in (4.10) with the sample frequency T_{sa} of the controller, we can get its ω-transform. Comparison between this transform and (4.10), which is shown in Figure 4.15, clearly tells us there is only 6.13 degree phase delay at half sample frequency (here is 10 kHz) after the bilinear transformation and there is no significant gain difference.

$$z = \exp(j \cdot \omega \cdot T_{sa}) \tag{4.13}$$

Where T_{sa}=50 μs.

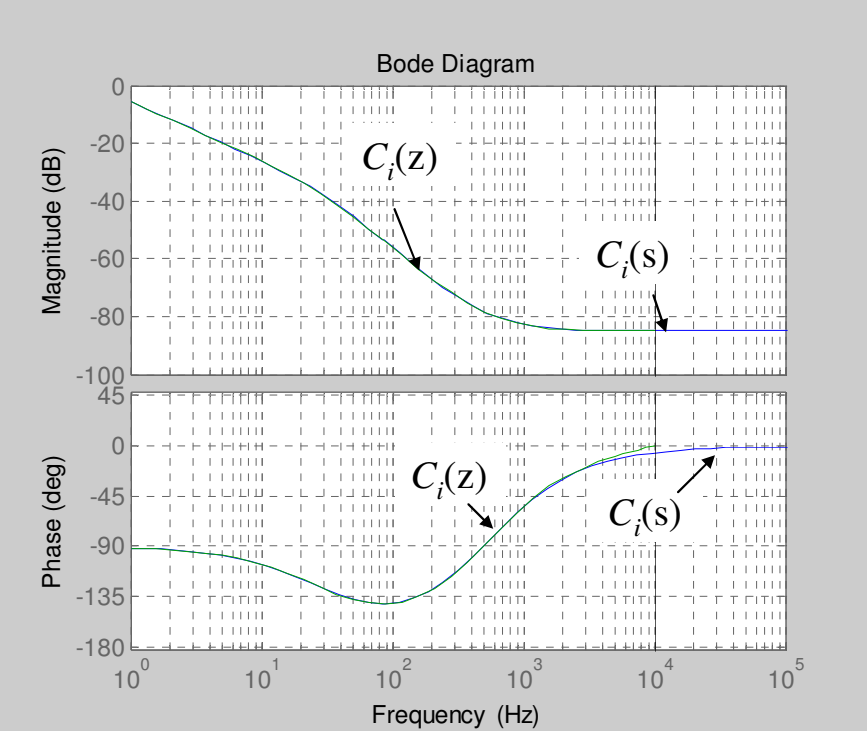


Figure 4.15 Bode plot of ω-transform comparison with that of s-transform

4.6 Digital Controller C_i(z) Implementation

4.6.1 Digital Controller Development

(1) Digital Implementation

Equation (4.12) can be expressed in discrete-time domain (4.14).

$$y(n) = x(n) \cdot b_0 + x(n-1) \cdot b_1 + x(n-2) \cdot b_2 - a_1 \cdot y(n-1) - a_2 \cdot y(n-2) \tag{4.14}$$

Shown in Figure 4.16 is the signal flow graph for this controller. This is direct form I structure. The error signal $x(n)$ is calculated and the output signal $y(n)$ is the sum of the

$b_0 \cdot x(n)$, $b_1 x(n-1)$, $b_2 \cdot x(n-2)$, $(-a_1) \cdot y(n-1)$ and $(-a_2) \cdot y(n-2)$, where b_0, b_1, b_2, a_1, a_2 are given in (4.12).

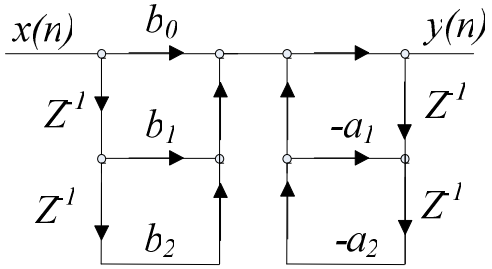


Figure 4.16 Direct form I realization of C_i(z) controller

(2) Quantization of Controller Coefficients

In order to implement a filter and a controller on a digital signal processor, the filter or controller coefficients must be converted into certain word length binary form. This conversion leads to movements in the pole and zero locations and therefore a change in the frequency response of the filter. This is quantization effect.

Different IQ means the different resolution. For an IQ keeps 12-bit resolution will matches the A-to-D sampling. It gives more dynamic range but less resolution than a higher bit condition. The instability caused by quantization will appear. There is a tradeoff between the enough dynamic range and resolution. With numerical stability consideration, IQ-22 is selected. The corresponding coefficients are changed to the following values: b_0= 0.0000656, b_1= –0.0001104, b_2= 0.0000464, a_1= 1.9906194, a_2= –0.9906194.

To check the resolution of the quantized coefficients, with the same principle as in section 4.5.2, Equation (4.13) is substituted for z in (4.12) and coefficients are replaced by its corresponding quantized value, therefore z-transform is mapped back to ω-transform. This transfer function is compared with the transfer function in (4.10). Figure 4.17 shows the comparison result. The two curves agree each other, meaning the quantized coefficient has enough resolution to provide expected frequency response.

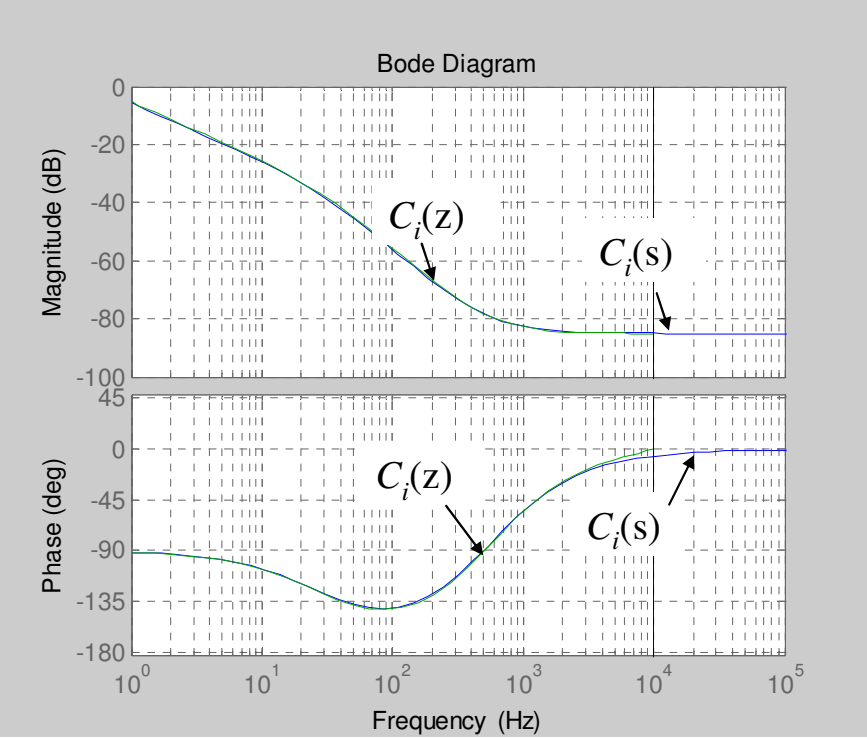


Figure 4.17 Quantization effect on the controller transfer function C_i(z)

4.6.2 Programming Flow Chart

Since high frequency ripples, such as 80 kHz and 20 kHz, exist in the inductor current i_L sensing feedback signal, the sampling frequency should be higher than 20 kHz PWM switching frequency. Multiple time bases are needed, which means one clock is for PWM switching frequency control and the other clock is for ADC sampling frequency control. They are synchronized by built-in synchronization logic. The timing of the two clocks and their relationship are illustrated in Figure 4.18. Considering the ripple frequency, 200 kHz ADC sampling frequency is chosen.

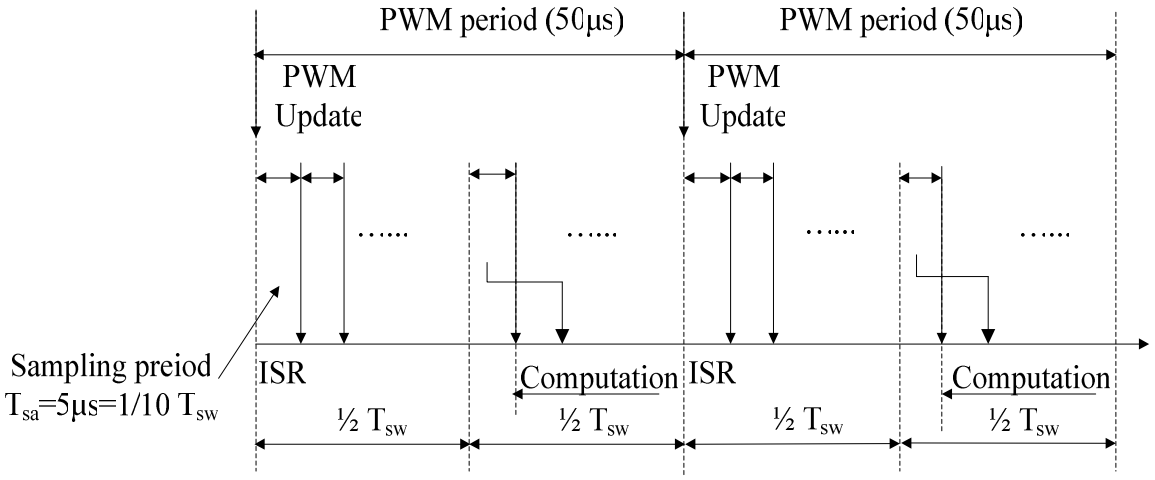


Figure 4.18 ADC sampling period and PWM period for resistive load

As indicated in Figure 4.19, the program is made up of two sections. One is the main program, and the other is the ADC interrupt routine program. In the main program, the initial conditions are setup at the main routine. Following it, a background program processes the controller. The controller produces a PWM duty cycle value, which will be uploaded at the beginning of the next PWM period. During the background calculation, ADC sampling happened periodically. Whenever ADC sampling completes, the interrupt vector will direct the program to the interrupt service routine (ISR) and computes the digital filter $BF(s)$ with the sampled value to filter out the high frequency ripple. The sampled value will not be involved in the controller calculation until the middle of each PWM period. This is controlled by the setting of Flag. For each PWM period is equivalent to ten of sampling periods, after five sampling periods, it comes to the middle of the PWM period, which is characterized by the setting of Flag. It is noted that the controller computation should be done within this half PWM period. This keeps the computational delay $E_2(s)$ as short as half PWM period T_{sw}.

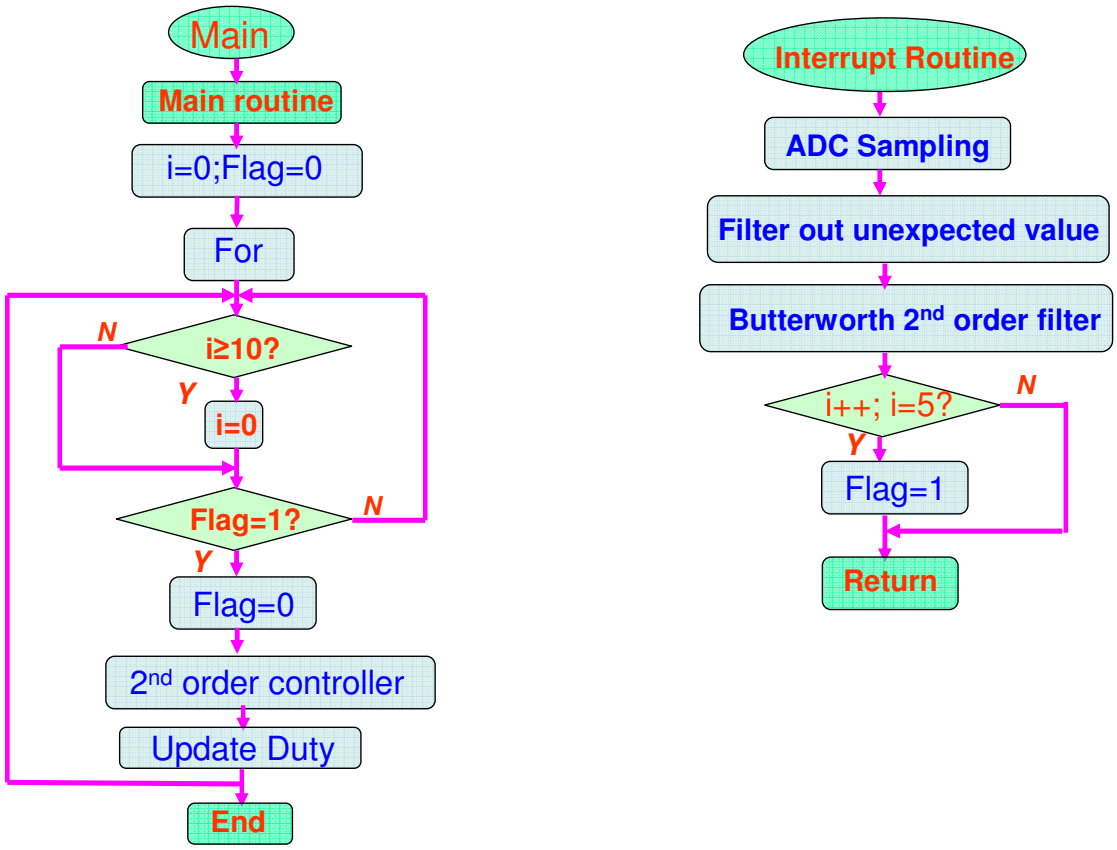


Figure 4.19 Flow chart of the DSP program for resistive load

4.7 Unified Controller for Resistive Load Step Test Results

Figure 4.20 shows the hardware test setup. MOSFET modules are sitting on the heat sink. Gate drive board is on the top of power modules, and on top of gate drive board is the DSP controller board. The total current i_L is sensed and fed back to the DSP board. Four Finemet-based inductors are connected to each respective module. It is noted that the total current i_L, instead of i_o, is used as the feedback signal for the initial test.

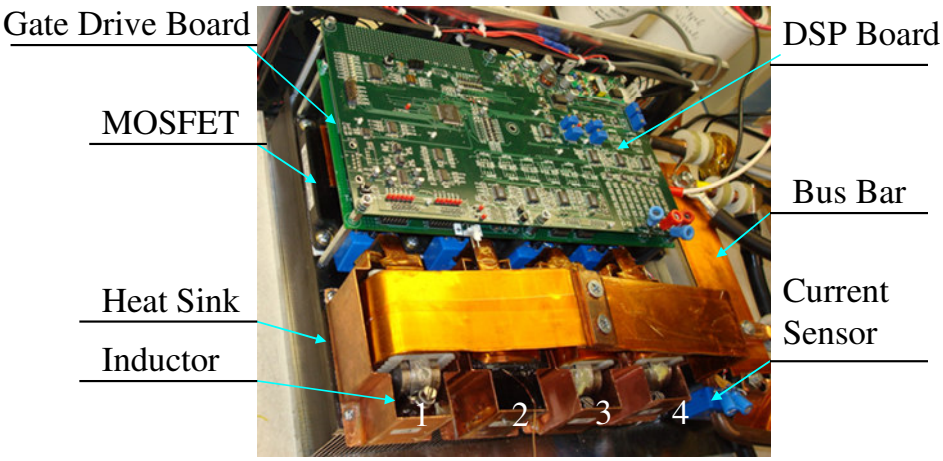
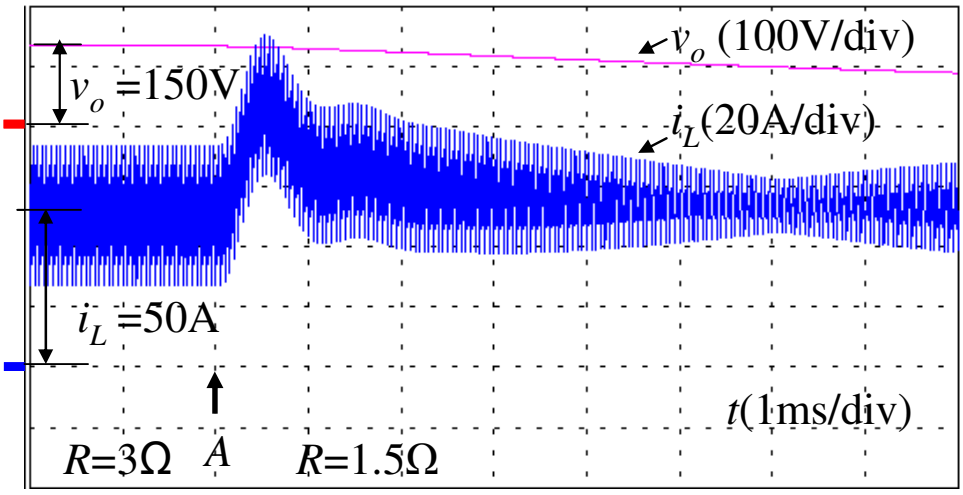


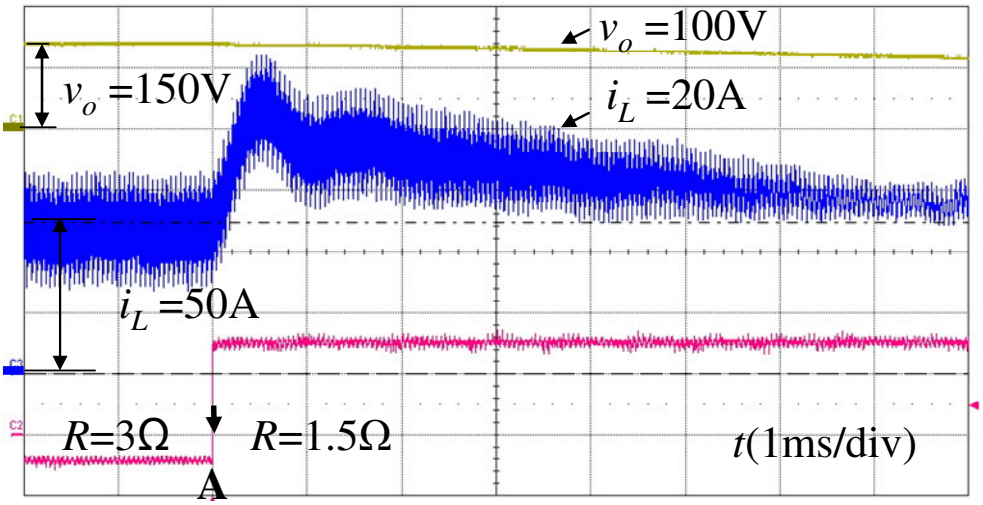
Figure 4.20 Test setup for 4-phase bidirectional dc-dc converter

4.7.1 Resistive Load Buck Mode Step Test Results

Figure 4.21 (a) and (b) show the buck constant current mode load step-up simulation and experimental results, respectively. Large current ripple is found since the sensing point i_L is before low-side capacitor C_L. Before point A, an averaged current of 50 A is regulated. At point A, load resistance changes from 3 Ω into 1.5 Ω. The inductor current increases immediately and is fed back to controller. Finally, before the current increases further, the controller regulates the inductor averaged current back to 50 A. Figure 4.22(a) and (b) show the buck constant current mode load step-down simulation and experimental results, respectively. The averaged current is 50A. Contrary to the load step-up, at point A, load resistance changes from 1.5 Ω to 3 Ω. The current decreases immediately and is fed back to controller. The controller regulates the inductor averaged current back to 50 A.

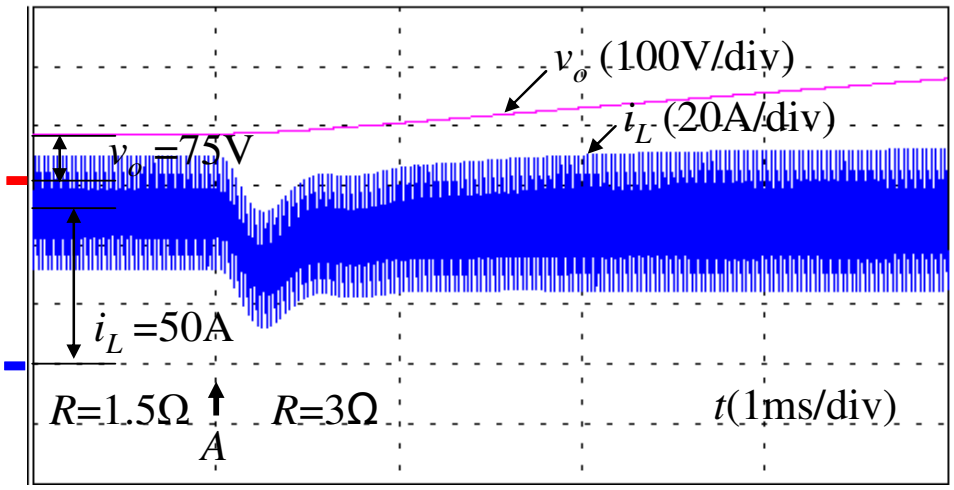


(a) Buck load step-up simulation result

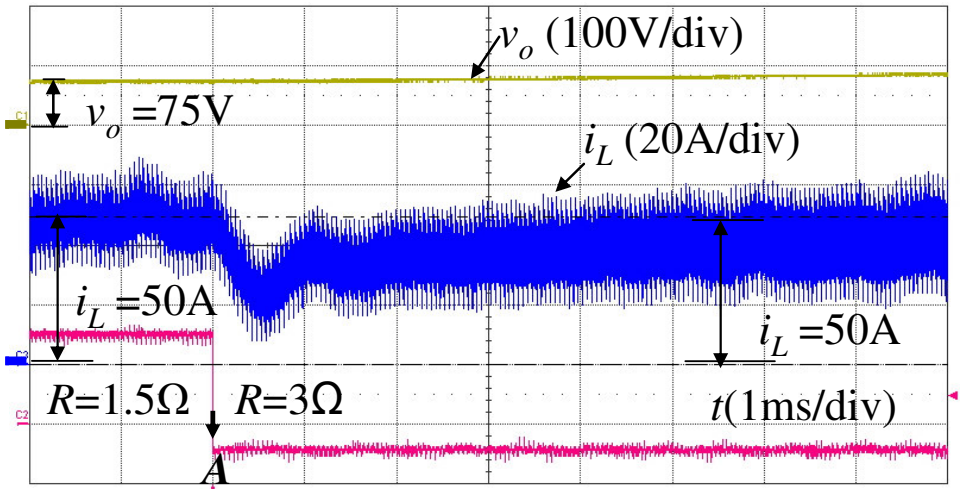


(b) Buck load step-up experimental result

Figure 4.21 Buck load step-up simulation and test results



(a) Buck load step-down simulation result



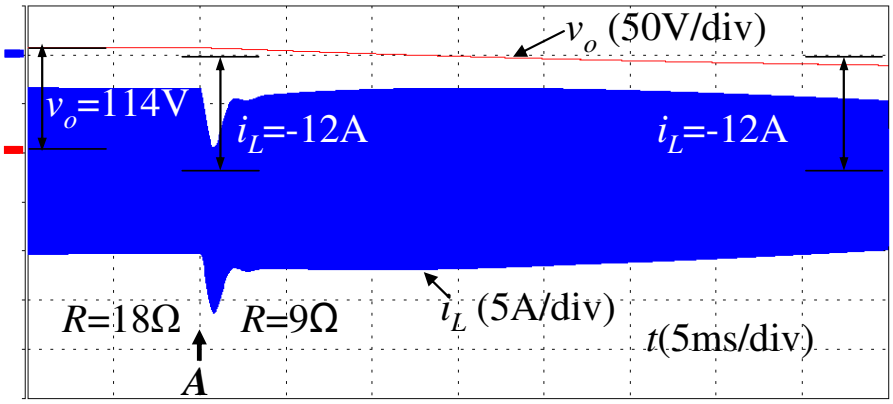
(b) Buck load step-down experimental result

Figure 4.22 Buck load dump-down simulation and test results

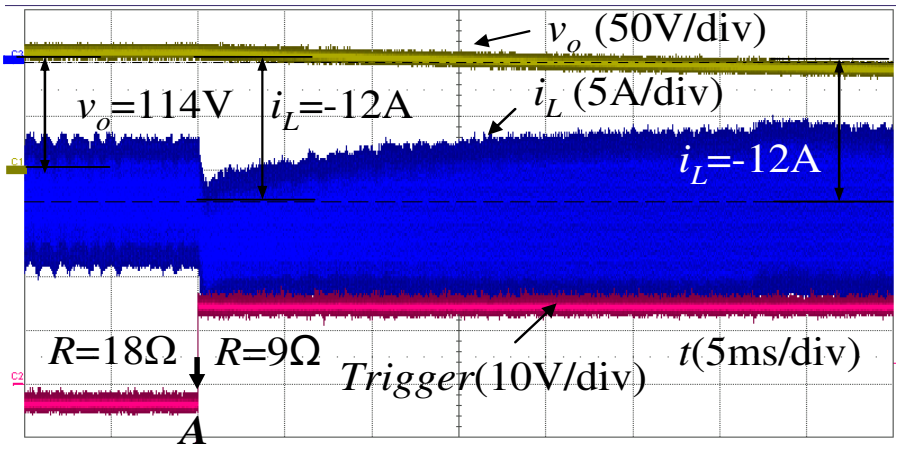
4.7.2 Resistive Load Boost Mode Step Test Results

Boost constant current mode load step-up simulation and experimental results are shown in Figure 4.23 (a) and (b), respectively. Due to the opposite current reference direction, for load step-up the current goes to more negative value instead of going to positive value. Before point A, an averaged current of –12 A is regulated. At point A, the

load resistance changes from 18Ω into 9Ω. The current increases immediately and is fed back to controller. Finally, before the current increases further, the controller regulates the inductor averaged current back to –12 A. Figure 4.24 (a) and (b) show the boost constant current mode load step-down simulation and experimental results, respectively. The averaged current is –12 A. Contrary to the load step-up, at point A, load resistance changes from 9 Ω to 18 Ω. Current decreases immediately and is fed back to controller. The controller regulated the inductor averaged current back to –12 A. A significant current ripple presents due to inconsistent inductor values among 4 phases. However experimental results match with simulation results very well.

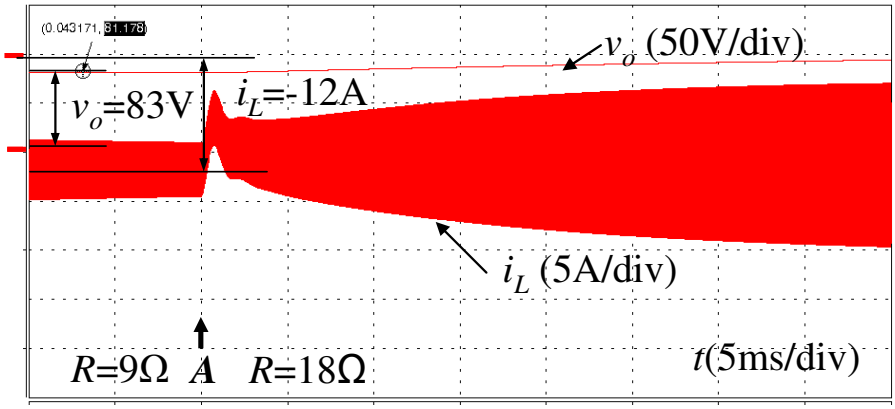


(a) Boost load step-up simulation test result

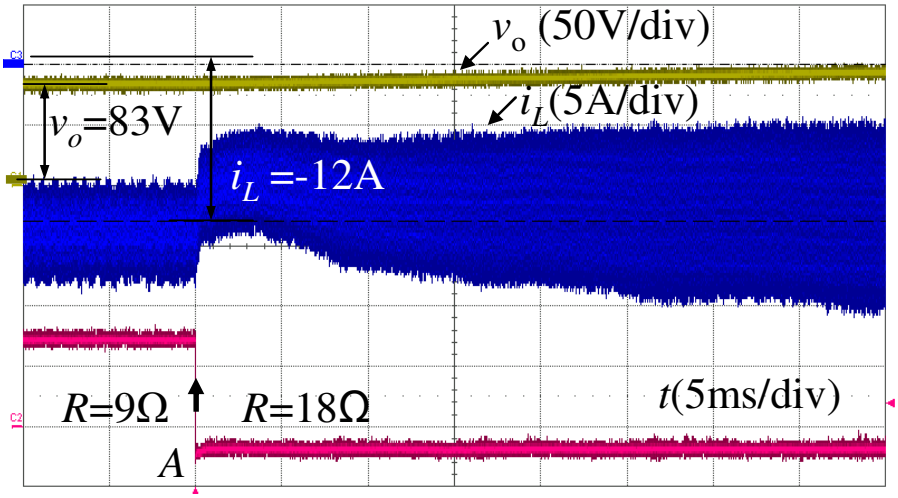


(b) Boost load step-up experimental result

Figure 4.23 Boost load step-up simulation and test results



(a) Boost load step-down simulation result



(b) Boost load step-down experimental result

Figure 4.24 Boost load step-down simulation and test results

4.8 Summary

Unified controller concept is proposed. The proposed unified controller is developed to be applicable for both resistive load buck and boost modes, instead of two controllers for the two modes. Unified controller is designed based on a second-order model, which is derived from the general-purposed third-order power stage model for resistive load condition.

Detailed analysis of the sensing feedback signal, filter design consideration, and delay effect on the digitally implemented system has been provided. In this resistive load, sensing feedback signal at inductor current i_L is believed to have better response than with the output current i_o. Delay effects, which include ADC sampling delay, computation delay and PWM modulation sampling delay, are analyzed and quantified. The entire system frequency response is obtained.

The proposed unified controller is designed and then implemented with a digital control system. The complete system has been simulated with a circuit simulator and verified with hardware experiments. Both simulation and experimental results show that the proposed unified controller performs well in a high power bidirectional dc-dc converter. Stable operation is verified with load step-up tests under both buck charging and boost discharging modes with resistive load. The results indicate that the derived model is valid and can be used for the unified controller design to achieve constant current charging and discharging.

Chapter 5 Bidirectional DC-DC Current Flow Control Experiments

5.1 Introduction

As mentioned in chapter 4, the third-order general-purposed power stage model was applied in resistive load, which has only one voltage source on one of the two ends, and the model can be simplified into a second-order system. Step-load tests verify that the unified controller can be used in both buck mode and boost mode. The sign of current setting I^* can control the power flow direction, which was demonstrated in chapter 4.

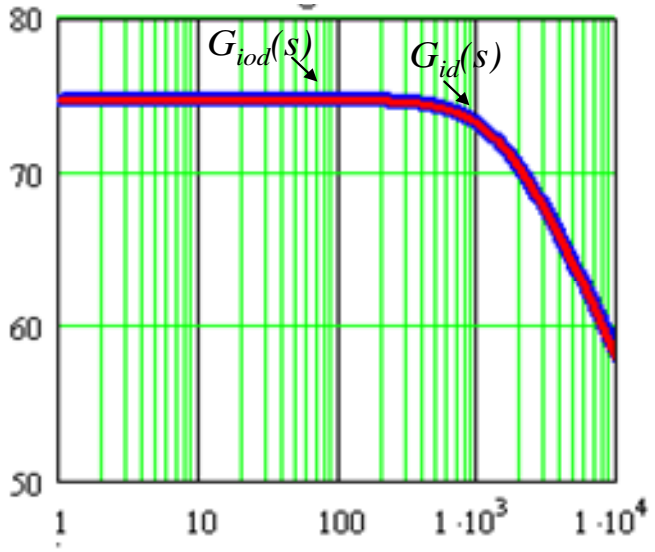
In this chapter, the third order power stage model is applied to a battery load, which has voltage sources on both ends, and the model can be simplified into a first-order system within the interested load range. The unified controller will be applied in the battery load to realize bidirectional current flow control. Investigation on the two possible current sensing points shows the output current i_o, instead of inductor current i_L, has advantage as the sensing signal for battery load. A unified controller $C_{io}(s)$ for bidirectional dc-dc converter test is designed and optimized in section 5.2. Digital implementation and power stage prototype is introduced in section 5.3 and section 5.4 respectively. Unidirectional and bidirectional power flow control tests are conducted, and the simulation results are provided in section 5.5.

5.2 Unified Controller $C_{io}(s)$ Design for Battery Load

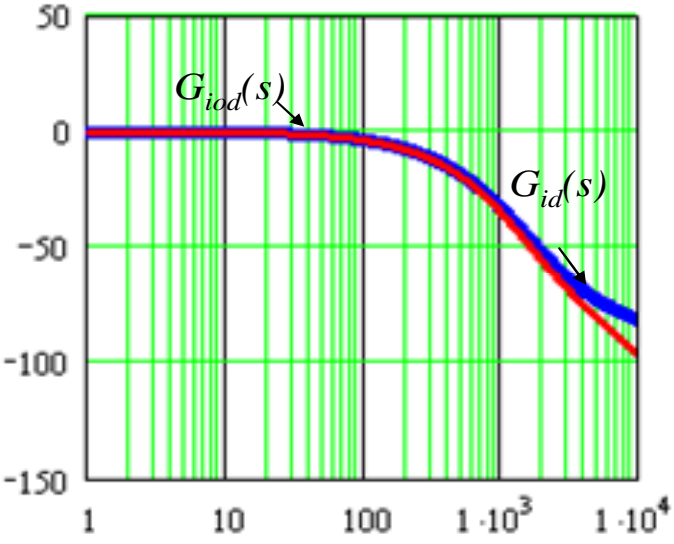
5.2.1 Current Feedback Sensing Signal for Battery Load

For resistive loads described in chapter 4.3, the use of inductor current as feedback signal for the control-to-inductor current transfer function $G_{id}(s)$ works well in the control system design. However, for the battery load condition, the use of output current as feedback signal for the control-to-output current transfer function $G_{iod}(s)$ is a better choice. The Bode plots of two transfer functions shown in Figure 5.1 are close to each

other when frequency is less than 3 kHz. Since in a battery load, the equivalent resistance, which is battery internal resistance, is as small as tens of mΩ, the delay caused by the R_2-C_L is not significant. Thus, sensing point of inductor current i_L brings some benefits from the response point of view. Whereas, the output current i_o sensing point has advantage of small ripple, which releases the stress both on the analog filter and digital filter during the feedback loop.



(a) Magnitude



(b) Phase

Figure 5.1 Bode plots of battery load with different feedback sensing signal i_L and i_o

For the battery load, since the output current i_o has less ripple and fast enough response, only an analog filter RC_1(s) with a cutoff frequency of 10.6 kHz is needed.

5.2.2 Loop Gain Transfer Function T_{io}(s)

For battery load, the total loop gain T_{io}(s) composes system delay E(s) and controller C_{io}(s), including control-to-output current transfer function G_{iod}(s) analog filter RC_1(s) as pointed out in section 5.2.1. The system delay E(s) was described in chapter 4. The system loop gain expression is indicated in (5.1). The system control block is shown in Figure 5.2.

$$T_{io}(s) = G_{iod}(s) \cdot RC_1(s) \cdot E(s) \cdot C_{io}(s) = G_{plant} \cdot C_{io}(s) \tag{5.1}$$

where $G_{plant} = G_{iod}(s) \cdot RC_1(s) \cdot E(s)$.

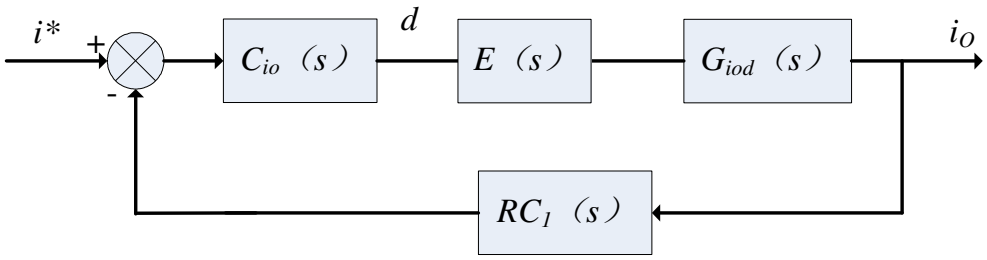


Figure 5.2 System control block diagram for battery load

5.2.3 Battery Load Control-to-output Current Transfer Function G_{iod}(s)

(1) Control-to-output Transfer Function G_{iod}(s)

Equation (4.2) indicates that resistance R_2 affects the location of two poles of the control-to-output current transfer function G_{iod}(s). When the resistance is high, two poles

merge together. When R_2 is less than 0.1 Ω, the two poles split into two separate poles. One goes to low frequency, and the other goes to high frequency as shown in Figure 5.3.

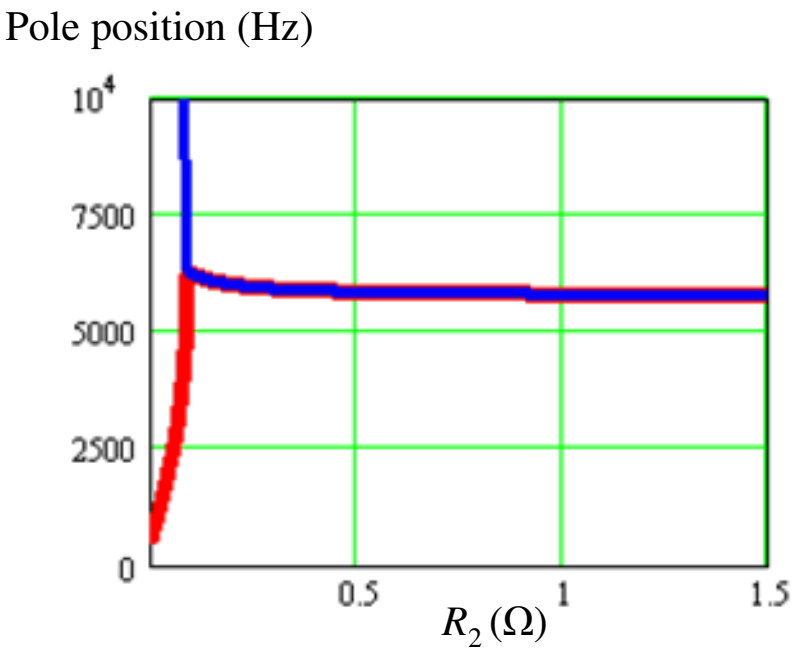
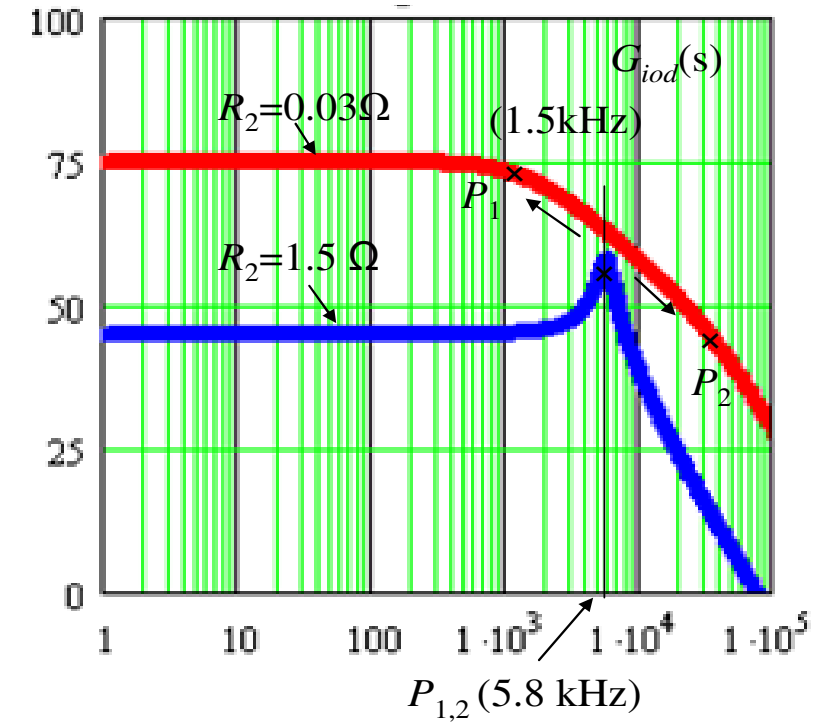


Figure 5.3 Resistance R_2 effect on pole positions

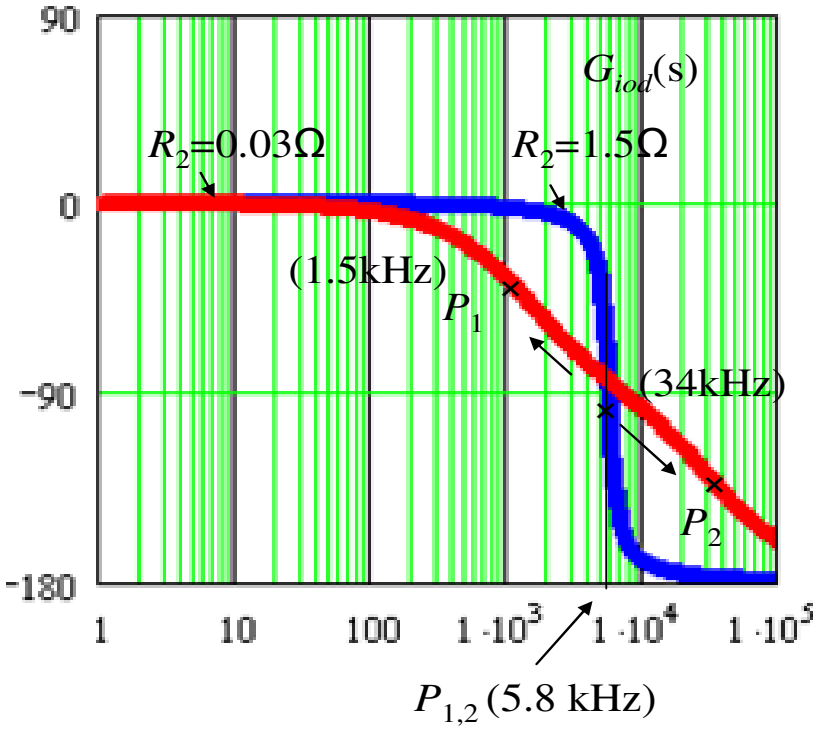
The control-to-output current transfer functions for different resistor R_2 are shown in Figure 5.4. When R_2 is 0.03 Ω, the transfer shows a low frequency pole at 1.5 kHz and a high-frequency pole at 34 kHz. With the 1.5-kHz pole dominating low-frequency response, the transfer function behaves like a first-order system. When R_2 is 1.5 Ω, the transfer function presents a double-pole at 5.8 kHz. With a small R_1, the third pole is located at the frequency higher than 100 kHz, which is not shown in the frequency-domain plots.

Table 5.1 Bidirectional battery load design conditions

Case No.	V_H (V)	V_L (V)	L (μH)	C_H (mF)	C_L (μF)	R_2(Ω)	R_1(mΩ)
1	350	115	20.5/4	7.2	150	0.03	10
2	240	115	20.5/4	7.2	150	1.5	10



(a) Magnitude



(b) Phase

Figure 5.4 Resistance R_2 effect on control-to-output current transfer function G_{iod}(s)

(2) DC Gain of Control-to-Output Current Transfer Function G_{iod}(s)

Equation (4.2) indicates that the dc gain of control-to-output current transfer function G_{iod}(s) will increase with the increase of high side voltage V_H and will decrease with the increase of resistance R_2. The worst case should be the one with highest dc gain, which means the one with highest high-side voltage V_H and lowest resistance R_2. The different cases are shown in Table 5.1. Case No.1 is the worst case, based on which the controller is designed to get enough phase margin, gain margin and high enough crossover frequency f_c. After the controller design, the performances of all the other cases are checked.

5.2.4 Controller Structure

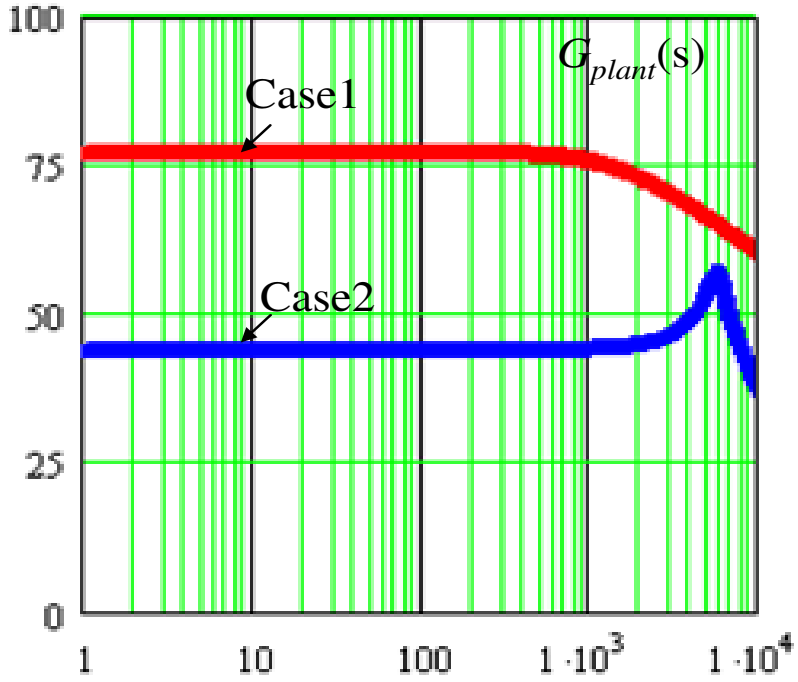
For frequencies less than 3 kHz, the G_{plant} has a relative constant gain as indicated in The controller type II PI controller is selected, and equation is shown in (5.2). Figure 5.5, so a type II PI controller is sufficient to achieve the desired control response.

$$C_{io}(s) = k_p + \frac{k_i}{s} \tag{5.2}$$

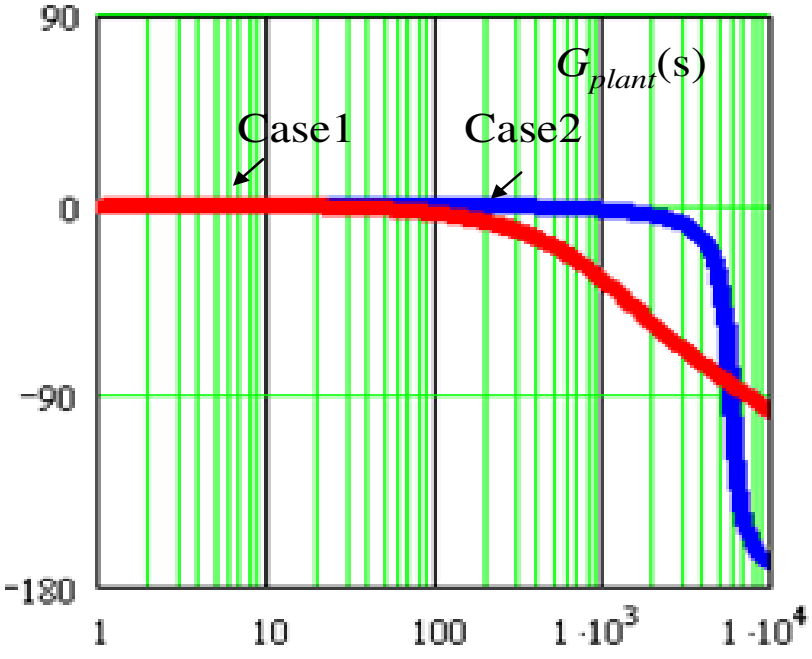
where k_p=0.4 and k_i=6.36943e-6.

5.2.5 Design Results

With the controller expressed in (5.2), loop gain T_{io}(s) transfer function is drawn in Figure 5.6. The design result is shown in Table 5.2. It is noted that case 1 has less phase margin but higher crossover frequency or bandwidth than case 2.

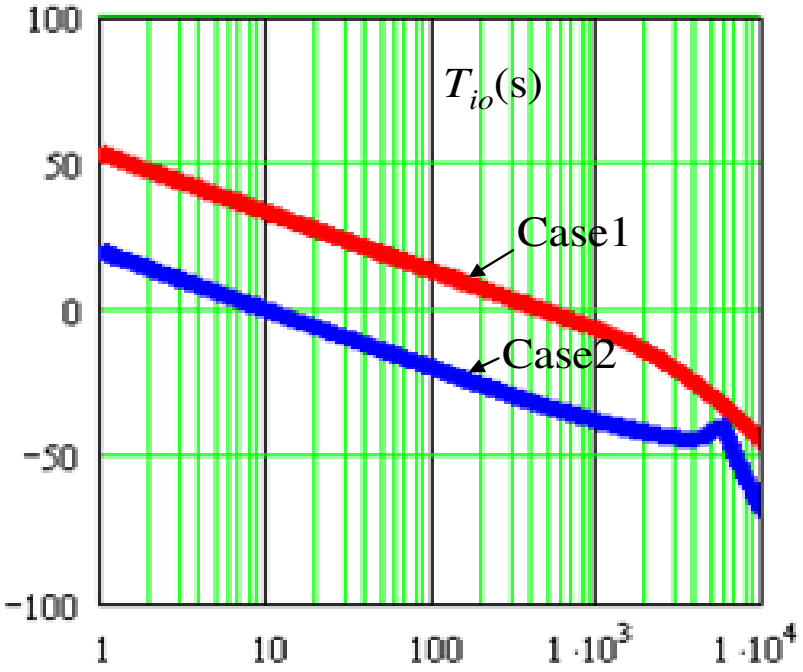


(a) Magnitude

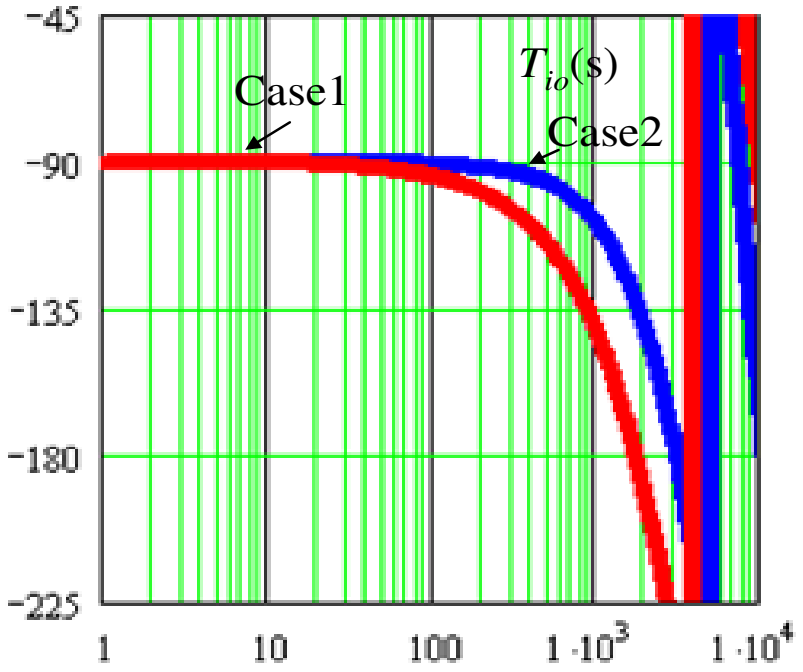


(b) Phase

Figure 5.5 Bode plots of power plant transfer function G_{plant}(s)



(a) Magnitude



(b) Phase

Figure 5.6 Bode plots of control loop gain transfer functions T_{io}(s)

Table 5.2 Design results

Case Number	Phase Margin PM(degree)	Gain Margin GM (dB)	Crossover frequency f_c (Hz)
1	68	13	480
2	90	44	10

5.3 Digital Controller C_{io}(z) Implementation

5.3.1 Controller Discretization and Digital Implementation

The controller parameter coefficients are discretized. The controller discrete time domain expression is indicated in (5.3).

$$y(n) = x(n) \cdot b_0 + x(n-1) \cdot b_1 - a_1 \cdot y(n-1) \tag{5.3}$$

Here a_1= –1, b_0=0.000073662 and b_1= –0.00053662. They are the discretized coefficients. Signal flow graph of the type II controller is shown in Figure 5.7.

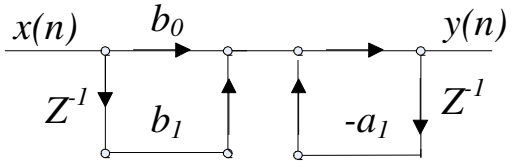


Figure 5.7 Direct form structure I realization of C_{io}(s)

5.3.2 Flow Chart for Battery Load

For the battery load, output current sensing signal is clean, therefore digital filter is not needed, which releases the burden of ADC sampling frequency requirement. The ADC sampling frequency can be as low as PWM switching frequency. The related system event sequence is depicted in Figure 5.8. ADC sampling is triggered by the PWM middle

period point. Upon the end of ADC conversion, interrupt service routine is activated and the controller will be calculated. Finally, PWM duty cycle is achieved within this half of PWM period. When it comes to the next PWM period, this duty cycle will be executed.

Correspondingly, the DSP program flow chart is quite simple and can be described in Figure 5.9.

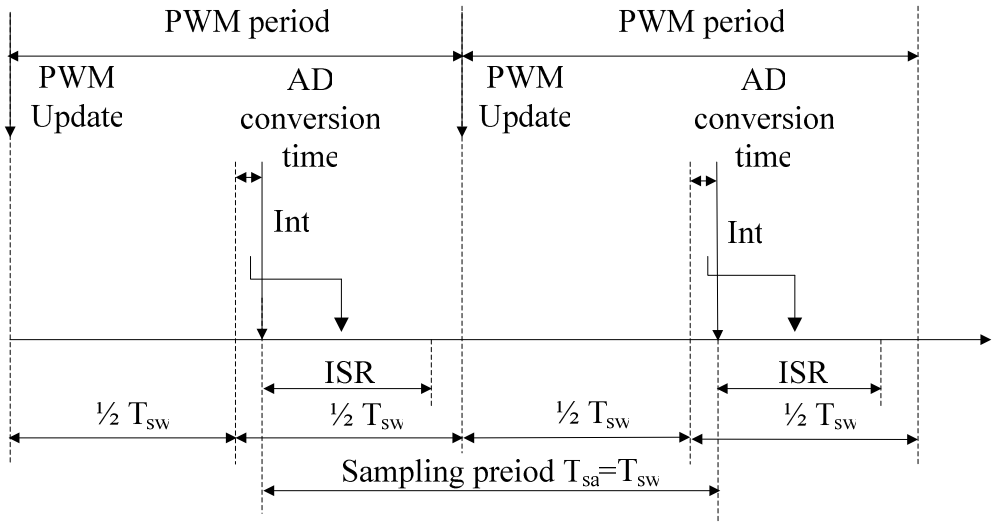


Figure 5.8 ADC sampling period and PWM period for battery load

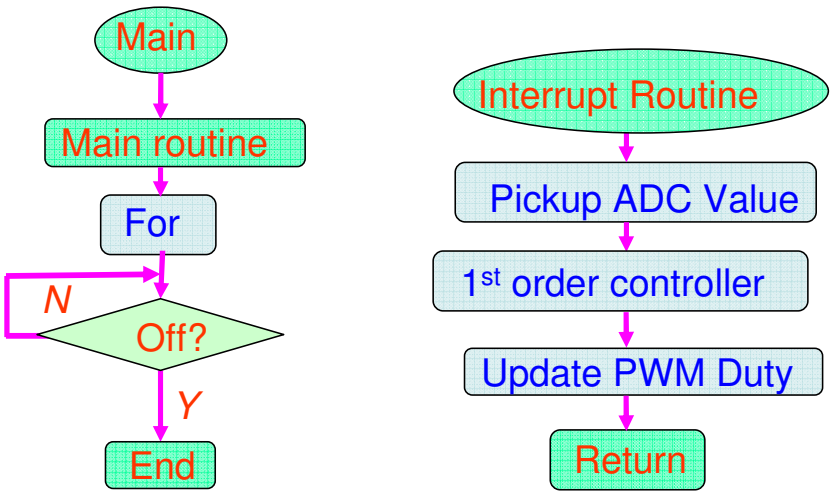


Figure 5.9 Flow chart of the DSP program for battery load

5.4 Power Stage Prototype

It is demonstrated by the tests in chapter 4 that the unified controller regulates both buck resistive load and boost resistive load step. With the voltage source on both sides, the unidirectional and bidirectional current flow control tests will be described in this section.

In this system, the output current i_o acts as feedback signal instead of inductor current i_L. Unidirectional current flow control step tests are first conducted for both buck and boost modes. The bidirectional current flow control step tests are then conducted to demonstrate the effectiveness of the unified controller.

The bidirectional dc-dc power stage prototype is shown in Figure 5.10. It consists of four phase legs of MOSFET modules, two sets of coupled inductors, high- and low-side capacitors, heat sink, a gate drive board and a DSP digital control board. The size of it is 29 Liter (0.4 m×0.36 m×0.2 m). Three fans are used for air cooling. A LEM Hall sensor is put after the output capacitor to measure the total output current. The cable on two ends will go to resistive load, power supply or battery. The related control block is shown in Figure 4.4 (chapter 4). The power stage parameters used in the following tests are listed in Table 3.6.

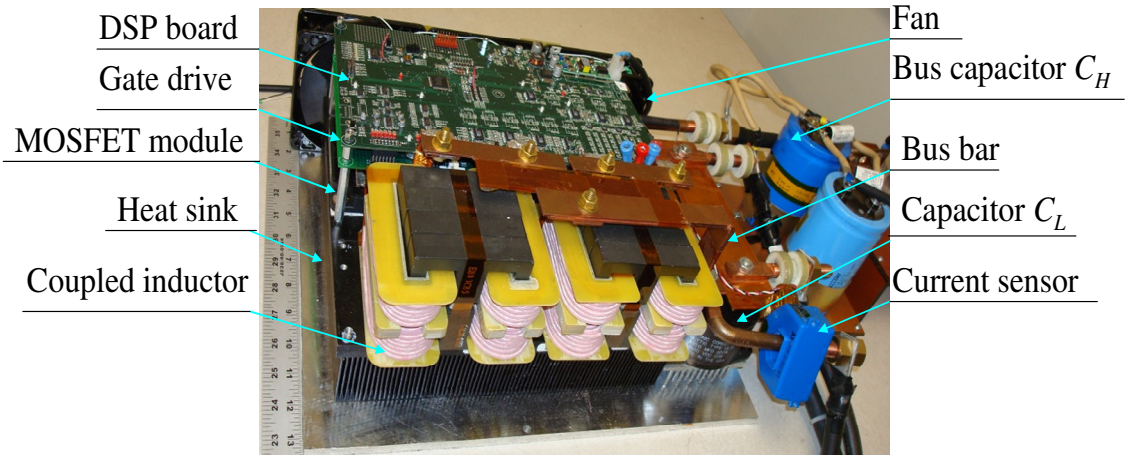


Figure 5.10 Power stage prototype

The simulation schematic is shown in Figure 5.11. There are four phases, including four individual inductances. The inductance is the coupled inductor equivalent inductance value 20.5 μH, which is derived in section 3.5.

Table 5.3 Power stage parameters used in simulation and test

n	MOSFET	L_1-L_4 (μH)	C_H (mF)	C_L (μF)	f_{sw} (kHz)	R_{dson} (mΩ)	R_{l1}-R_{L4} (mΩ)
4	APTM50AM17F	20.5	7.2	150	20	35	36

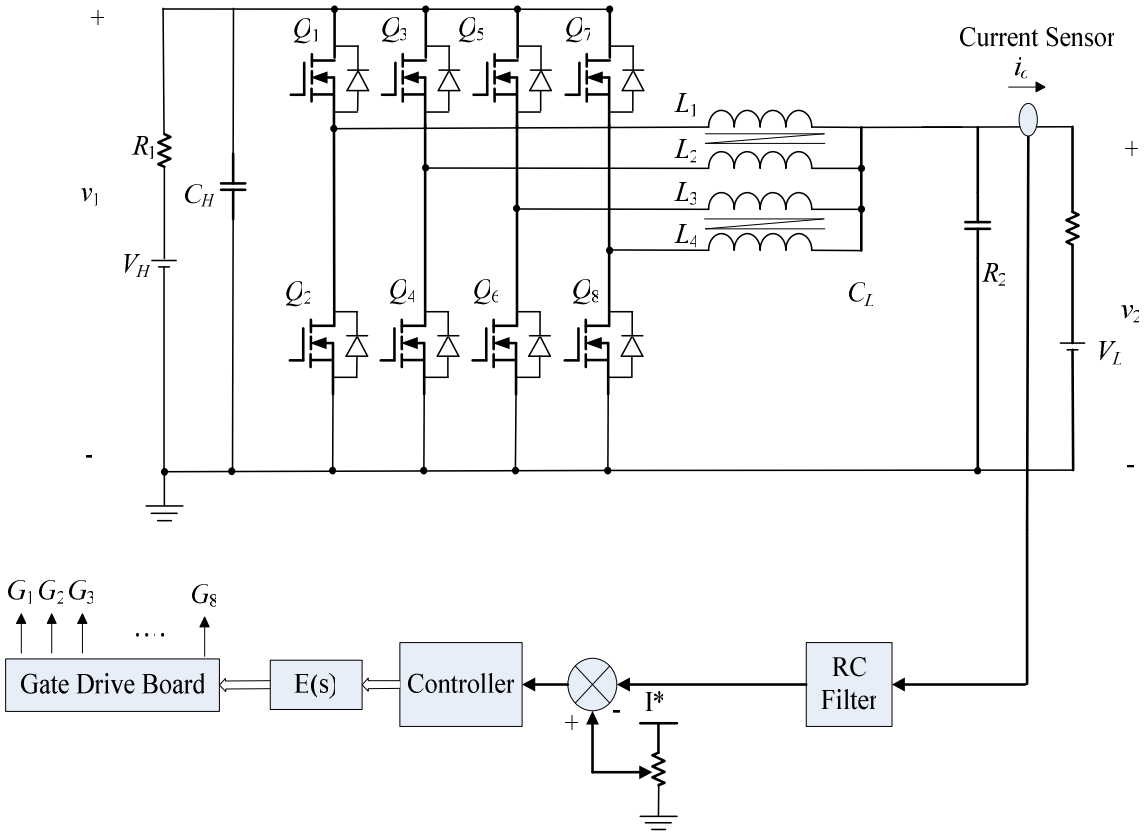


Figure 5.11 Bidirectional dc-dc converter simulation schematic

5.5 Unified Controller for Current Flow Control Step Tests

Unidirectional current flow step tests for both buck and boost mode is conducted under resistive load condition first.

5.5.1 Unidirectional Current Flow Step Tests

(1) Current Flow Step Up Control under Buck Mode

The parameters in Table 5.4 are chosen for buck mode with resistive load test.

Table 5.4 Buck mode test parameters

No.	V_H=V_1 (V)	V_L(V)	V_2 (V)	I^* (A)	R_2(Ω)	R_1(Ω)	P_o(kW)
1	260	0	45	10	4.5	0	0.45
2	260	0	113	25	4.5	0	2.83

A high side voltage V_H of 260 V and resistance of 4.5 Ω are applied. Reference current I^* is changed from 10 A to 25 A. Both simulation and tests result waveforms are captured as shown in Figure 5.12 and in Figure 5.13 respectively.

Before point A, a reference current I^* of 25 A is given and the output current io is stabilized at 25 A. The inductor current i_L is averaged at 25 A as well. At point A, the reference current I^* is commanded from 25 A to 10 A. After this, a gradually and steadily change from 25 A to 10 A in output current io can be observed both in Figure 5.12 and Figure 5.13, so does voltage v_2, with the change from 113 V to 45 V. The overall transition takes about 100 ms. Although the control bandwidth can be controlled by adjusting the controller parameters, such a control response is satisfactory for a high-power system as long as it is stable, and the steady state error in output current i_o is not noticeable. The simulation and test results show a very good agreement, which means the controller works as expected and the system feature can be predicted through simulation.

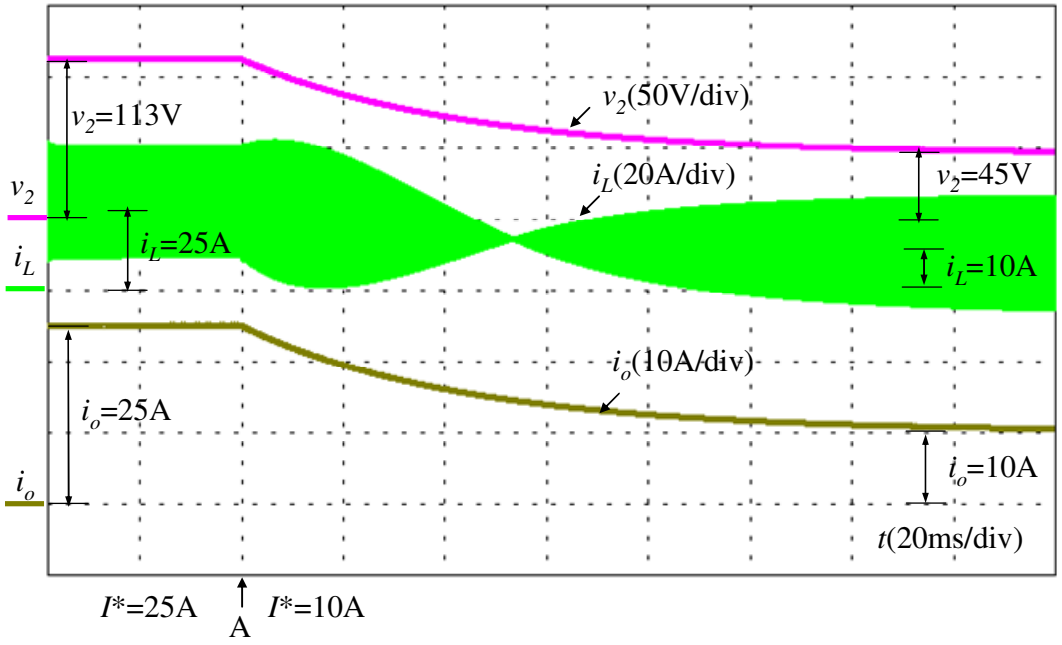


Figure 5.12 Simulation results of current flow step down control for buck mode

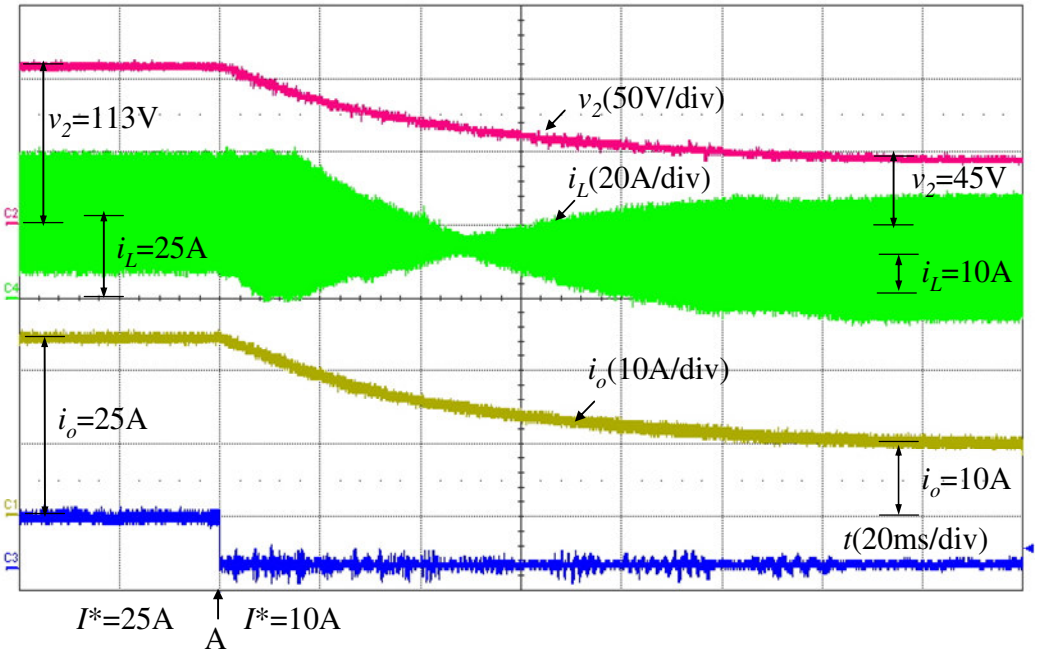


Figure 5.13 Test results of current flow step down control for buck resistive load

(2) Current Flow Step Up Control for Boost Mode

Parameters in Table 5.5 are chosen for boost mode with resistive load test. A low-side voltage V_L of 20 V and resistive load of 18 Ω are applied. Reference current I^* is changed from –14 A to –5 A. Here the boost mode current is defined with negative signs to that refer to reversed current flow. Both simulation and test waveforms are captured as shown in Figure 5.14 and in Figure 5.15 respectively.

Table 5.5 Boost mode test parameters

No.	V_H(V)	V_L=V_2 (V)	V_1 (V)	I^* (A)	R_1(Ω)	R_2(Ω)	P_o(kW)
1	0	20	40	–5	18	0	–0.1
2	0	20	67	–14	18	0	–0.28

A low-side voltage V_L of 20 V and resistive load of 18 Ω are applied. Reference current I^* is changed from –5 A to –14 A. Both simulation and test results are captured as shown in Figure 5.14 and Figure 5.15, respectively.

Before point A, a reference current I^* of –5 A is given, and the output current i_o is stabilized at –5 A. The inductor current i_L is averaged at –5 A as well. At point A, a sudden step down change in reference current I^* of –5A to –14 A is introduced. After this, a gradually and steadily change from –5 A to –14 A in output current i_o can be observed both in Figure 5.14 and Figure 5.15. The corresponding voltage v_1 are changed from 40 V to 67 V. The overall transition takes more than 160ms. Such a response is satisfactory for a high-power battery-based system as long as it is stable and the steady state output current i_o error is unnoticeable. The simulation and test results show very good agreement, which means the controller works as expected and the system feature can be predicted through simulation.

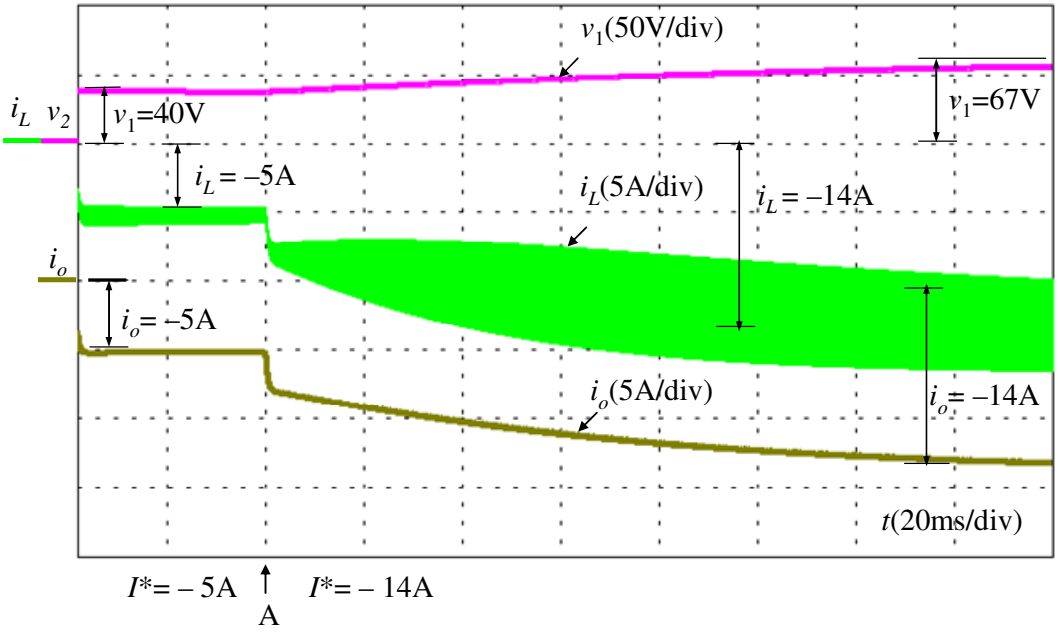


Figure 5.14 Simulation results of boost resistive load current flow step up control

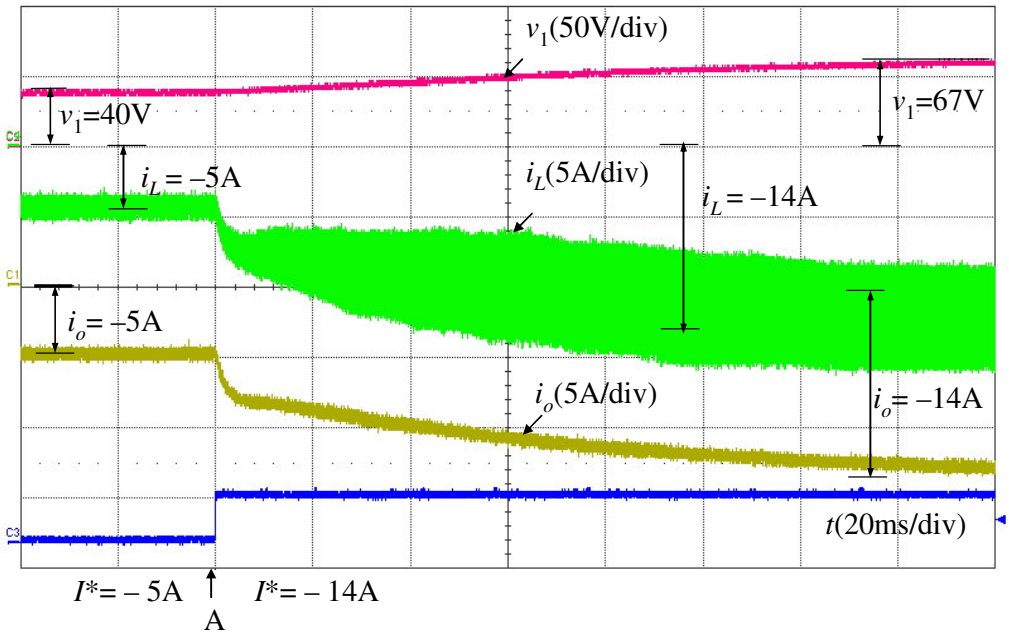


Figure 5.15 Test results of boost resistive load current flow step up control

5.5.2 Traditional Bidirectional Current Flow Control Simulation

To compare the traditional separate controllers with the proposed unified controller, a simulation for the traditional separate controllers [45] is conducted first to show the mode transition behavior.

In bidirectional dc-dc converter, the mode transition for current mode control or voltage mode controller is needed in electrical vehicle application. For example, when there is a demand of quick power flow from the load, the battery can switch from battery charging mode to discharging mode immediately. With buck and boost separate controllers, the mode transition can cause dramatic duty cycle change which will result in a severe jump on inductor current i_L, output current i_o and output voltage v_2. Under the condition shown in Table 5.6, the mode transition with different controllers is simulated. The definitions of the parameters are indicated in Figure 4.2 and the simulation results waveforms are shown in Figure 5.16.

Table 5.6 Mode transition simulation parameters

State	V_H (V)	V_L(V)	R_2(Ω)	I^* (A)	P_o(kW)
1	240	115	1.5	30	4.80
2	240	115	1.5	–30	–3.45

At state-1 period, the converter output charging current is a constant of 30 A. Here only the duty cycle of buck controller d_{buck} is effective and duty cycle of boost controller d_{boost} is ineffective and is holding a minimum duty of 0, since the output current i_o now is regulated by buck controller of 30 A. At point A, the current reference is changed to –30 A, and the converter becomes in boost mode operation, or state-2 period. The duty cycle d_{boost} becomes effective, and d_{buck} becomes ineffective. From Figure 5.16, it is noticed that it takes 8 ms for the controller to get out of the saturation. After another 35 ms, the controller regulates the output current i_o to be –30 A. During this period, low side voltage v_2 drops from 160 V to –125 V, output current i_o drops from the regulated value of 30 A to as low as –160 A and inductor current i_L varies from 450 A to –800 A. This kind of

severe transient during the mode transition period increases both device voltage and current stresses significantly.

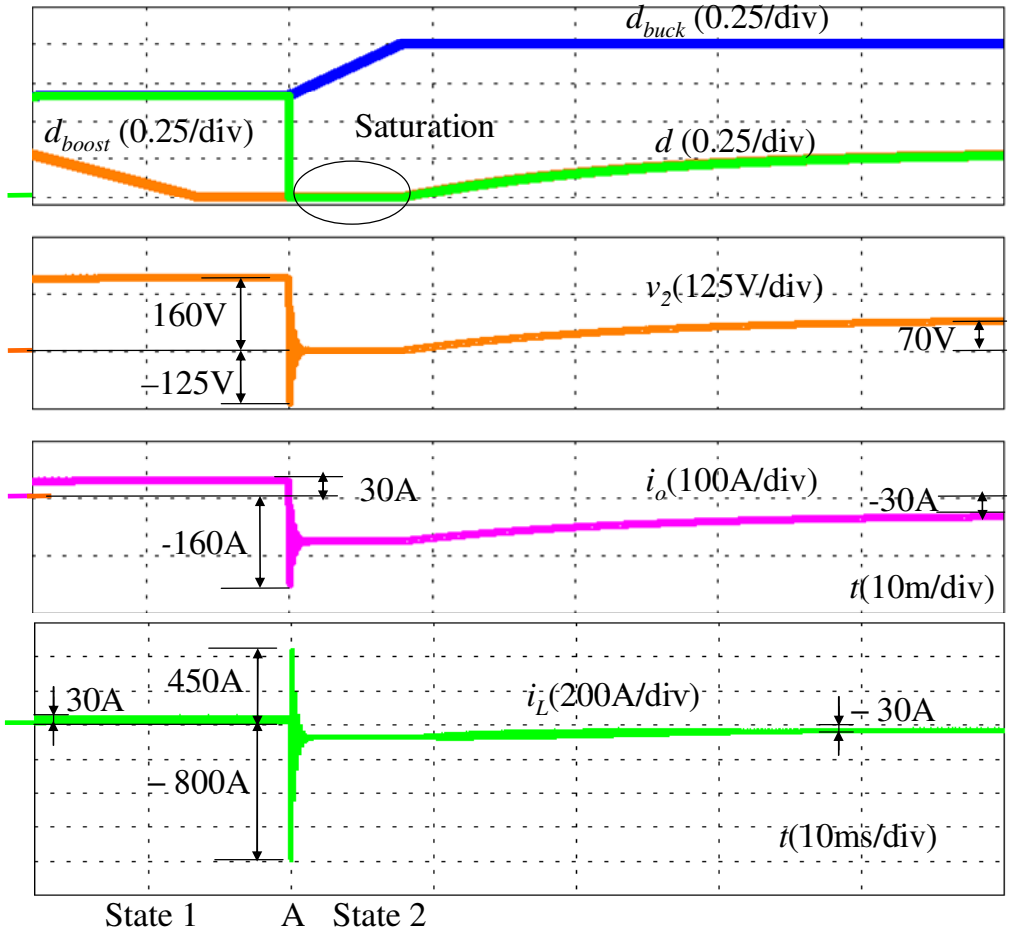


Figure 5.16 Mode transition simulation waveforms of duty cycle d, output current i_o and inductor current i_L

The duty cycle change between the mode transition as shown in Figure 5.16 is severe, which results in the huge current spike.

5.5.3 Bidirectional Current Flow Control Test

A unified controller is applied to bidirectional current flow control test. The two main switches are complementarily controlled by a common duty. Single control duty, by which the power flow can be easily controlled, is generated by the unified controller.

(1) Bidirectional Current Flow Control Test System Setup

Setup shown in Figure 5.17 is used for bidirectional current flow control test, which helps reduce the huge inrush current during the battery connection. The high-side voltage source V_H is constantly charged with a dc power supply V_1. When the voltage between two terminals of switch S_1, which is measured by meter V_{m3}, is close to zero, S_1 can be turned on to connect the $Battery_1$ to the test circuit. The same arrangement is also applied to the low-side connection. When the voltage between two terminals of the switch S_2, which is measured by meter V_{m4}, are close to zero, S_2 can be turned on to connect the $Battery_2$ to the test circuit. A resistor R_2 is connected in series with $Battery_2$ to protect the battery from over current. Meter V_{m1} and V_{m2} are used for monitoring the high-side voltage and low-side voltage, respectively. The direction of the output current i_o flow is defined as positive under buck-mode charging condition.

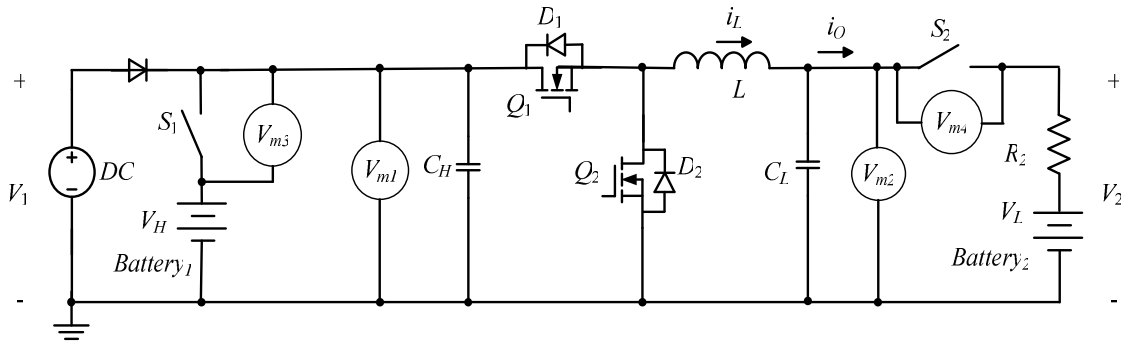


Figure 5.17 System test setup for bidirectional current flow control

Table 5.7 is the test parameters used in bidirectional current flow control. Based on the two battery current capability, the charging current is set to be 30 A and the discharging current is set to be –25 A. The related power levels are –2.88 kW and 4.44 kW respectively, where negative sign means the power is coming out from $Battery_2$.

Table 5.7 Test parameters used in bidirectional current flow control

No.	V_H(V)	V_L(V)	I^* (A)	R_1(mΩ)	R_2(Ω)	P_o(kW)
1	233	115	30	10	1.1	4.44
2	233	115	–25	10	1.1	–2.88

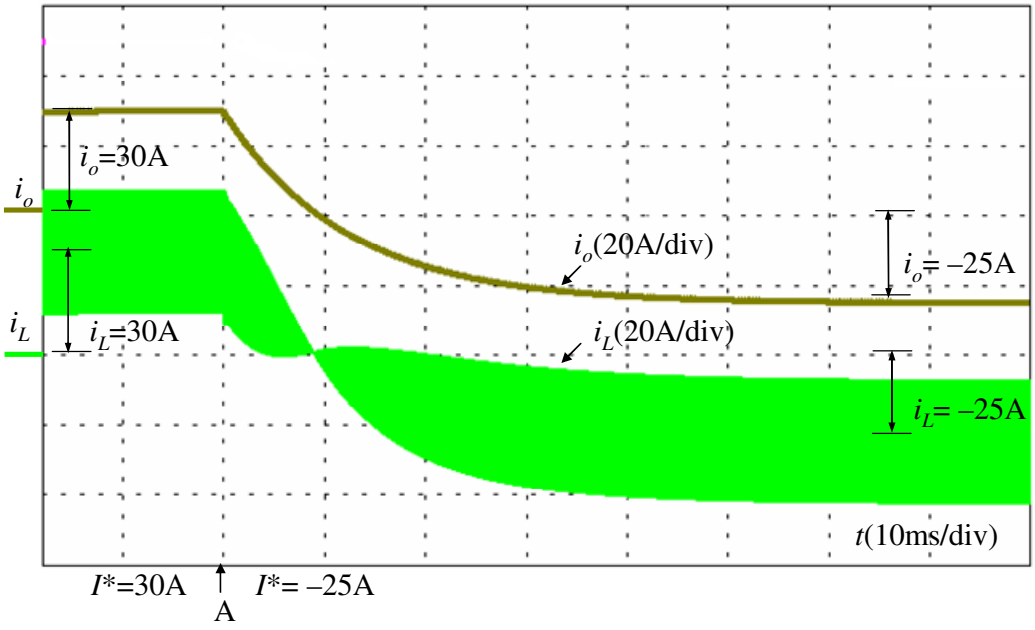


Figure 5.18 Simulation result of bidirectional current flow step down control

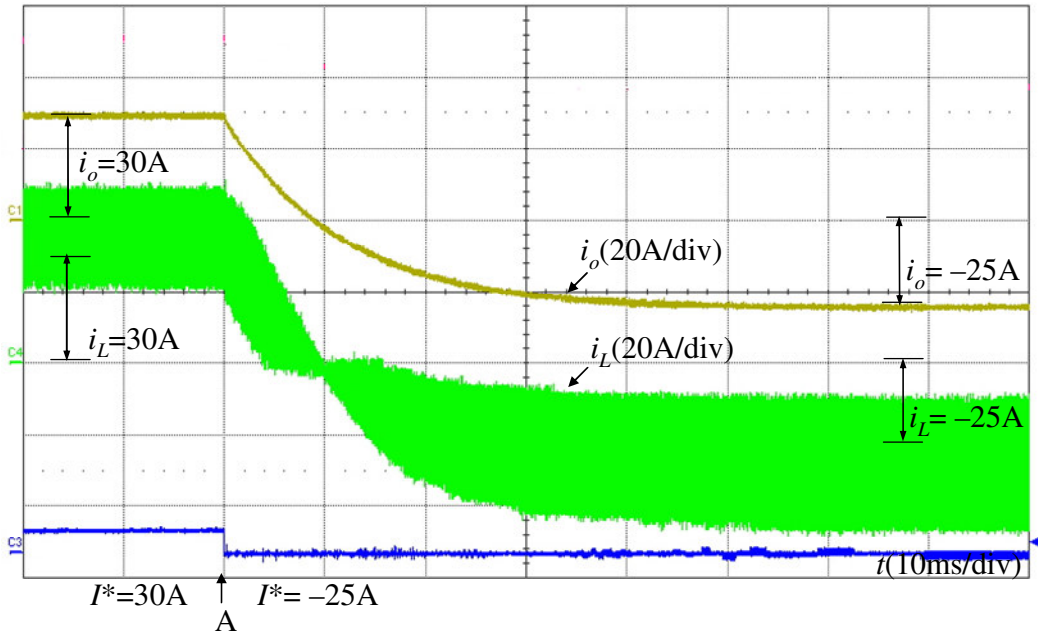


Figure 5.19 Test result of bidirectional current flow step down control

(2) Bidirectional Current Flow Control Test Results

The parameters, including high-side voltage V_H of 233 V, low-side voltage V_L of 115 V and a resistive load of 1.1 Ω, are applied. Reference current I^* is changed from 30 A to –25 A. Both simulation and tested waveforms are captured as shown in Figure 5.18 and Figure 5.19 respectively.

Before point A, a reference current I^* of 30 A is given and the output current io is stabilized at 30 A. The inductor current i_L is averaged at 30 A as well. At point A, a sudden step down change in reference current I^* of 30 A to –25 A is introduced. After this, a gradually and steadily change from 30 A to –25 A in output current i_o can be observed both in Figure 5.18 and Figure 5.19. The overall transition takes less than 40 ms, and the steady state error in output current i_o for both positive and negative current flow is unnoticeable, which means the unified controller accurately regulates both charging and discharging current flow. The regulation is smooth and controllable. The simulation and test results show a very good agreement, which means the controller works as expected and the system feature can be predicted through simulation. The zoom-in test result waveform is shown in the Figure 5.20.

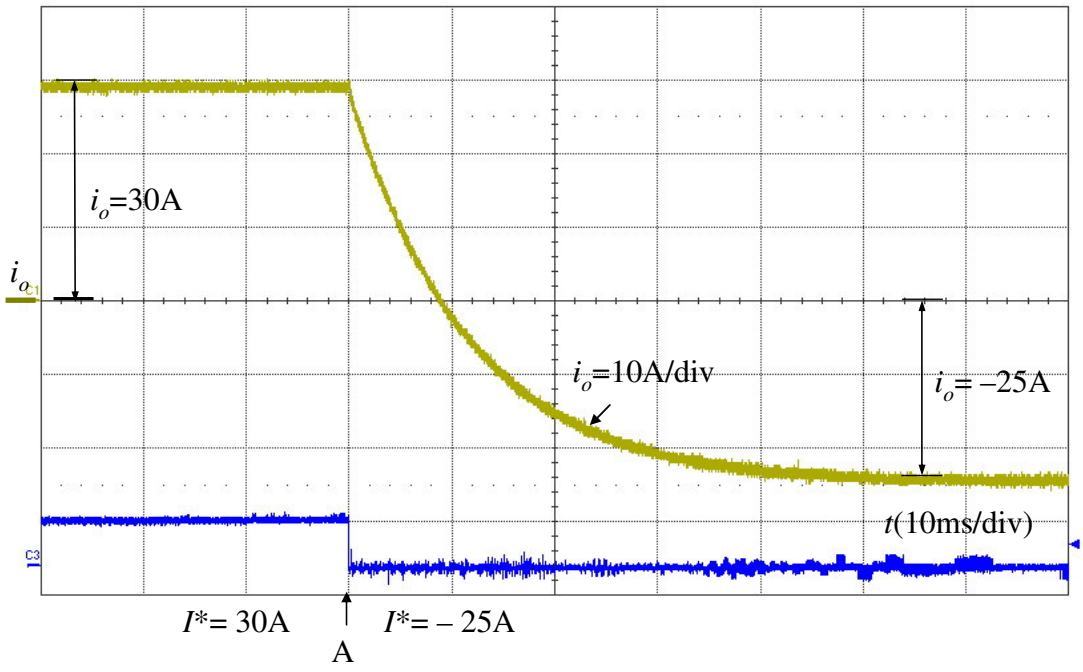


Figure 5.20 Test result of bidirectional current flow step down control

(3) Test Results Discussion

The simulation result of duty cycle during the mode transition is shown in Figure 5.21. As compared to the duty cycle shown in Figure 5.16, the duty cycle changes smoothly without severe change. Although the reference signal change is a step signal, the response is filtered out by the type II controller, and thus the duty cycle is changed smoothly. This smooth change of duty cycle leads to smooth current flow during mode transition, and the severe transient obtained with the separated controllers is no longer present.

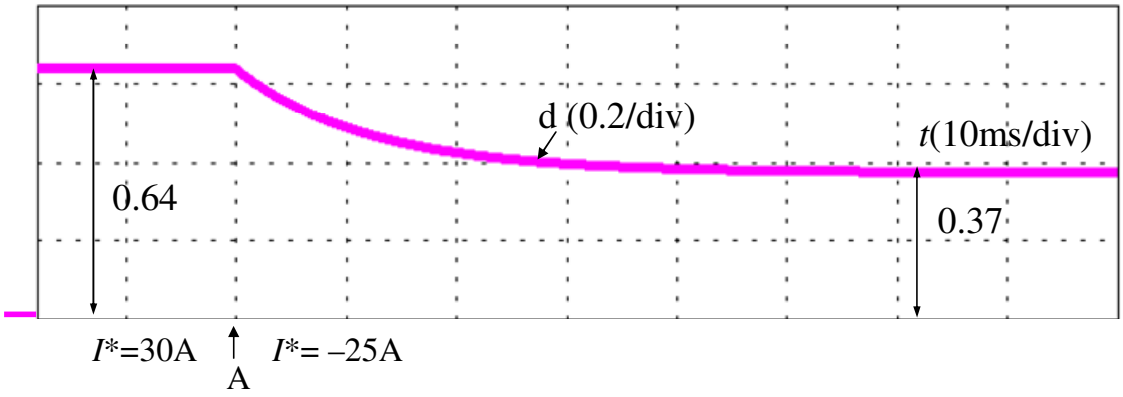


Figure 5.21 Simulation result of bidirectional dc-dc current flow step down control

5.6 Summary

At low frequencies for battery load, the control-to-output current transfer function can be simplified as first-order system which is the same as the control-to-inductor current model derived in chapter 3. After analysis of the sensing feedback signal, filter consideration and delay effect, a unified controller for battery load is designed and applied to the system bidirectional power flow control test.

Compared with the mode transition controlled by separate controllers, the transition controlled by proposed unified controller is smooth and fast enough. The proposed unified controller concept essentially contributes to the smooth transition. Further analysis indicates that the behaviors of their duty cycle are different. The unified controller precisely regulates the error and generates smooth and gradual change duty cycle, while the separate controllers have an abrupt duty cycle change during the mode

transition period, which results in a jump in both voltage and current waveforms and therefore more stresses in device.

The complete system has been simulated with a circuit simulator and verified with hardware experiments. Both simulation and experiment results show that the proposed unified controller performs well in bidirectional power flow control. This proves that the established general-purposed power stage model is valid and the unified controller works as expected with smooth transition during transient power flow reversal. Simulation results and experiment results show a very good agreement. The simulation can be used to predict the system features.

Chapter 6 Conclusions

6.1 Summary

This dissertation introduces the complementary gate signal control to get high power efficiency and improve the discontinuous conduction mode operation EMI noise. On the basis of this control scheme, a third-order general-purposed model of a bidirectional dc-dc converter for battery charging is proposed, developed and investigated. A unified controller, which results in smooth mode transition, is designed based on the general-purposed model. The following conclusions are drawn from the work.

(1) Complementary gating signal control is proposed and its performance is verified by the realization of ZVRT turn-on soft switching. This scheme eliminates parasitic ringing of the inductor current caused by the interaction between the inductor and device output capacitor. Based on this scheme, power stage components are optimized with the proposed methods as follows.

- Inductor volume index is introduced to evaluate the volume. The methodology of optimization is suggested to minimize volume and at the same time to realize ZVRT. Comparison of different materials performance shows that in the high power high temperature application the nanocrystalline-material FINEMET has relatively less core loss, and especially it has higher performance at high temperature.
- A design trade-off exists for the optimization of snubber capacitor. A series of experiments were conducted to determine the capacitance based on the minimum overall device switching loss condition.

With the optimized design, a 100 kW hardware prototype has been constructed and tested. A full-load efficiency of 98% is achieved, which allows high power density packaging for special applications.

(2) A general-purposed third-order model is proposed for the complementary-switching bidirectional dc-dc power stage. The model features two voltage sources on

both high- and low-sides and three energy stored components including one high-side capacitor, one low-side capacitor and one inductor. This general-purposed averaged model has following features.

- The averaged current flow direction is controlled by duty cycle of the main switch. For positive current flow, the duty cycle should be larger than the ratio of low-side and high-side voltage sources. For negative current flow, duty cycle should be smaller than the ratio of low-side and high-side voltage sources.
- This model can be used in the resistive load. In this case, the generalized third-order model behaves like a second-order power stage model which is the same as the conventional dc-dc buck or boost converter model.
- This model can be used in the battery load. In this case, the third-order model behaves like a first-order power stage model because the capacitor is short-circuited.

The Simplis ac analysis simulation is used to validate the model. The time-domain simulation results for the switching model and the averaged model show good agreement.

(3) A coupled inductor Δ-type model is introduced and further simplified. The state-space averaged model analysis indicates that the equivalent coupled inductor model is the self inductance L plus the mutual inductance M divided by two. This model helps the coupled inductor value selection. The model has been verified by Simplis simulation and used for the controller design. The final tests validate the coupled inductor simplified model accuracy.

(4) A unified controller concept is proposed for both buck charging and boost discharging modes based on the derived power stage model. The unified controller controls the power flow direction. The duty cycle during the mode transition changes gradually. The following conclusions are arrived with the controller design and test results.

- The unified controller is designed with the use of the general-purposed third order model, which contain both battery and resistive loads. The stability is ensured under the worst-case condition, which tends to have higher dc gain and less phase margin.

- The unified controller has been digitally implemented with DSP and demonstrated equal current sharing for multiphase operation and avoided duty cycle saturation.
- The designed controller is applied to unidirectional resistive load power flow and bidirectional battery load power flow tests. During the mode transition, a smooth and stable power flow is achieved.
- The complete system has been simulated with a circuit simulator and verified with hardware experiments. Both simulation and experimental results show very good agreement, which indicates that the unified controller performs well in bidirectional power flow control.

As a conclusion, the general-purposed power stage model provides theoretical basis for different operation modes. The proposed unified controller, based on the general-purposed power stage model, achieves a smooth and stable mode transition.

6.2 Future Work

(1) The bidirectional current flow control naturally has smoothly mode transition because of the unified power stage model and the adopted unified controller, but for all the other mode transitions a certain control scheme is needed to develop and further investigated. The other mode transitions include transition between current mode battery charging and voltage mode battery charging control, transition between voltage mode battery charging and bus system voltage mode discharging, and transition between current mode battery discharging and voltage mode discharging.

(2) Research on the power management strategy is needed to incorporate with the mode transitions control scheme.

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