Multi-Kilovolt Gallium Nitride Power Transistors

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ABSTRACT

Power semiconductor device, as a significant contributor to power electronics industry, plays an indispensable role in energy conversion applications including electric vehicles, data centers, consumer electronics, power grids, etc. The evolution of power semiconductor materials has progressed from traditional silicon (Si) to wide-bandgap materials including silicon carbide (SiC) and gallium nitride (GaN). Benefitting from the wide bandgap, high electron mobility and good thermal conductivity of GaN, GaN-based power devices can achieve fast switching speed, high breakdown voltage, and small on-resistance. They have been deployed in numerous power electronics applications, outperforming the Si and SiC counterparts. Nevertheless, despite their inherent advantages, the commercialization of GaN devices, particularly high-electron-mobility transistors (HEMTs), has predominantly been confined to the low-voltage domain of typically below 650 volts. This limitation blocks GaN HEMTs for medium- and high-voltage applications such as electric vehicles, renewable energy processing, and power grids, which have a total market size over USD$15 billion.

The challenge for GaN HEMTs to reach high-voltage applications arises primarily from the highly non-uniform electric field (E-field) distribution within the device structure, predisposing the device to premature breakdown and limiting its operational voltage range. Consequently, the quest for higher voltage capabilities in GaN HEMTs requires the fundamental understanding and effective mitigation of this non-uniform E-field distribution.

In this work, the p-type GaN-based Reduced Surface Field (RESURF) structure is proposed to balance the net charge in the two-dimensional-electron gas (2DEG) channel in GaN HEMT. This design enables a uniform distribution of E-field, enabling the voltage upscaling in GaN HEMT up to 10,000 V (i.e., 10 kV), which is the milestone voltage class in unipolar power devices for high-power applications.

The first part of this thesis introduces the history, background and mechanism of power semiconductor devices and provides solid reasons for GaN as a competitive participant in power electronics industry. It covers a basic introduction about GaN HEMT devices and their commercialization status and states the challenges GaN HEMTs are facing when dealing with mass production. An innovative RESURF structure is introduced to overcome the existing trade-off between on-resistance and breakdown voltage, and to achieve superior overall performance that would be beneficial for GaN HEMT to upscale the voltage classes.

Secondly, the development of a 10 kV unidirectional GaN HEMTs is discussed in detail. An optimized fabrication process flow, including etching, metal deposition, contact formation and dielectric passivation, is established. The RESURF structure is formed through a two-step chlorine-based etching process, with an innovative introduction of

sulfur hexafluoride (SF6) that enables a self-termination etch stop onto the AlGaN surface without damage to the 2DEG channel beneath. A controlled slow etch recipe has been developed as well, aiming for large-scale manufacturing with improved yields. A detailed analysis of the on-state and off-state I-V characterization of devices with various RESURF thickness and length provides an insight into the device breakdown mechanism, which has been verified with physics-based technology computer-aided design (TCAD) simulation.

The third part of this work demonstrates a 3.3-kV monolithic bidirectional switch (MBDS), which a novel device concept that can significantly simplify the circuit design in alternative current (AC) power conversion. A symmetrical p-GaN junction termination extension (JTE) design is proposed for electric field management, and the lateral conduction of this GaN-based MBDS enables a state-of-the-art high-voltage bidirectional switch with low on-resistance, achieving considerable performance advantage compared to the conventional bidirectional switch implemented by discrete devices.

In summary, this research work covers the design, fabrication, characterization, simulation, and breakdown mechanism analysis of GaN-based unidirectional and bidirectional transistors for multi-kilovolt power conversion applications. The extended p-GaN configuration (RESURF for unidirectional devices and JTE for bidirectional devices) offers a spatially-distributed E-field management, enhancing the breakdown voltage scaling capability of GaN HEMTs to exploit the full material advantages of GaN.

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GENERAL AUDIENCE ABSTRACT

Power semiconductor device, as a significant contributor to power electronics industry, plays an indispensable role in energy conversion applications including electric vehicles, data centers, consumer electronics, power grids. The evolution of power semiconductor materials has progressed from traditional silicon (Si) to wide-bandgap materials including silicon carbide (SiC) and gallium nitride (GaN). Benefitting from the wide bandgap, high electron mobility, and good thermal conductivity of GaN, GaN-based power devices can achieve fast switching speed, high breakdown voltage and small on-resistance. They have been deployed in numerous power electronics applications, outperforming the Si and SiC counterparts. Nevertheless, despite their inherent advantages, the commercialization of GaN devices, particularly high-electron-mobility transistors (HEMTs), has predominantly been confined to the low-voltage domain of typically below 650 volts. This limitation prevents GaN HEMTs from the entry into several critical markets such as renewable energy processing and power grids.

In this work, an innovative Reduced Surface Field (RESURF) structure is proposed to enable a uniform distribution of electric field inside the device structure, which would be particularly advantageous for voltage upscaling in GaN HEMTs. This device design enables the demonstration of high-voltage GaN HEMTs up to 10,000 V, the milestone volage class for power devices in medium- and high-voltage applications.

The first part of this thesis introduces the history, background, and physics of power semiconductor devices and provides solid reason for GaN as a competitive participant in power electronics industry.

Secondly, the development of a 10-kV unidirectional GaN HEMTs is discussed in detail. An optimized fabrication process flow, including etching, metal deposition, contact formation and dielectric passivation, is provided. The breakdown mechanism is also unveiled, which will be verified with physics-based device simulations in future works.

The third part of this work demonstrates a 3.3-kV monolithic bidirectional switch (MBDS), a novel device concept for alternative current (AC) power conversion. A symmetrical p-GaN junction termination extension (JTE) design is proposed for electric field management, achieving the highest voltage reported among the MBDS devices. This device can facilitate the development of new circuit topologies in AC power conversion.

In summary, this research work covers the design, fabrication, characterization, simulation, and breakdown mechanism analysis of GaN-based unidirectional and bidirectional transistors, achieving an unprecedented breakdown voltage upscaling capability in GaN HEMTs. The p-GaN configuration (RESURF for unidirectional devices and JTE for bidirectional devices) offers a spatially-distributed electric field management, enhancing the breakdown voltage scaling capability of GaN HEMTs to exploit the full material advantages of GaN.

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1 Chapter 1: Introduction

1.1 Power semiconductor devices: background and physics

1.1.1 Background

With a growing global market of over $43 billion and forecasted market of ~$59 billion by 2032 [1], power semiconductor devices are used as solid-state switches, regulating power system by controlling the current flow through semiconductor materials. As the essential components in power electronics industry, power semiconductor devices varying in voltage, current, power and frequency ratings enables efficient power conversion in various applications including but not limited to lighting, electric vehicles, data centers, electric grid, etc. Low-voltage devices (<600 V) are usually utilized in data centers and consumer electronics; medium-voltage (600V~3.3 kV) devices are mainly used for electric vehicles, photovoltaic system and motor control; high-voltage (3.3 kV ~ >10 kV) devices are usually used for applications such as marine, railway and power grid.

1.1.2 Physics

Ideal power semiconductor devices should be capable of infinite current conduction, infinite voltage blocking, infinite fast switching with zero power loss. The design of practical unipolar power devices aims to achieve low on-state resistance (R_{on}), high breakdown voltage (BV), and low switching loss, as these metrics concurrently determine the efficiency, frequency, and power density of a given power electronic systems.

In static condition, the trade-off between R_{on} and BV stages a key challenge that hinders further development in power semiconductor devices. In semiconductor materials, a lightly doped thick drift region enables higher electric field (E-field) in non-punch through (E-field does not crash into the n+ region) cases. Figure 1–1 illustrates the electric-field distribution for a p+/n-/n+ junction under reverse bias:

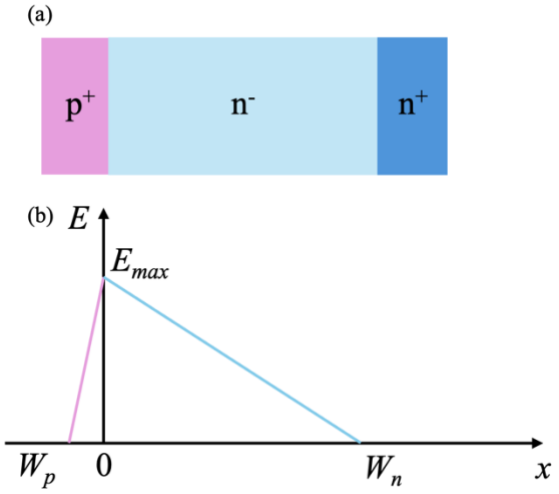

Figure 1–1 (a) Example of a p+/n-/n+ structure. (b) Corresponding E-field distribution of the structure under certain reverse bias.

The peak E-field E_{max} could be derived from the Gauss's law and written as:

$$E_{max} = \frac{qN_D W_N}{\varepsilon} \quad (1)$$

Where q is electron charge, N_D is the doping concentration of n- layer, W_N is the depletion width, and ε is the permittivity of the semiconductor material. Breakdown happens when E_{max} reaches the critical E-field of specific materials (E_c) and could be written as:

$$BV = \frac{\varepsilon E_C^2}{2qN_D} \quad (2)$$

in which q, N_D, ε and E_C are described as above. It could be recognized from equation BV that lighter doping level (lower N_D) is preferred to realize high E_{max} and BV.

On the other hand, the specific on-resistance is determined by carrier concentration and mobility, which is given by:

$$R_{on,sp} = \frac{W_N}{qN_D\mu} \quad (3)$$

In which μ is the mobility of the semiconductor material. To maximize current flow, $R_{on,sp}$ could be reduced with heavier doping (larger N_D) and thinner drift region (smaller W_N), which leads to lower conduction losses.

The Baliga's figure of merit (BFOM) was brought into consideration when evaluating the performance of specific semiconductor devices by relating the $R_{on,sp}$ and BV with the following equation by combining Eq. (2) and (3):

$$R_{on,sp} = \frac{4BV^2}{\varepsilon\mu E_C^3} \quad (4)$$

1.1.3 Materials

Silicon (Si), Silicon Carbide (SiC) and Gallium Nitride (GaN) are the three key materials that have been commercialized to produce power semiconductor devices. On the horizon, Gallium oxide (Ga_2O_3) The material-dependent parameter BFOM limit for Si, SiC, GaN and Ga_2O_3 is calculated with parameters given in Table 1-1 and shown in Figure 1–2 below:

Table 1-1 Critical parameters of materials and corresponding Baliga's figure of merit.

Material	**Electron mobility [cm^2/Vs]**	**Critical E-field [MV/cm]**	**Bandgap [eV]**	**BFOM [relative to Si]**
Si	1350	0.3	1.1	1
SiC	900	3.0	3.3	545
GaN	2000	3.3	3.4	1434
Ga_2O_3	200	8	4.8	2846

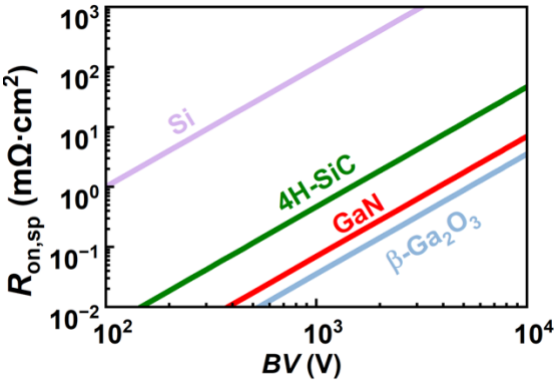

Figure 1–2 Theoretical limit of breakdown voltage vs. $R_{on,sp}$ for Si, 4H-SiC, GaN and Ga_2O_3.

It should be noted that although Si has a relatively low BFOM and the research on power electronic devices has gradually moved from Si to GaN and SiC, Si device still accounts for the largest market share of power semiconductor devices market, targeting for consumer electronics, automotive, communication infrastructure, etc. SiC and GaN devices are both the second largest participants, owing to the faster switching speed and higher power density. Ultra-wide-bandgap materials such as Ga_2O_3 are growing rapidly and are considered as promising participants in next-generation power applications.

1.2 GaN power devices: history, advantage, application, commercial status

1.2.1 Gallium Nitride material

As shown in Table 1-1, Si has the lowest bandgap E_g, which leads to a critical field 10 times smaller than wide-bandgap (WBG) materials such as GaN and SiC. In the past few decades, WBG materials have been extensively studied and researched, and have reached mass production and commercialization.

Gallium Nitride (GaN), a well-known III-V compound semiconductor material, has emerged as a frontrunner in power semiconductor device industry, featuring a remarkable balance of high breakdown voltage, fast switching speed, and small on-resistance. Compared with Si counterparts, GaN possesses an electron mobility of 2000 cm^2/Vs in the two-dimensional electron gas (2DEG) and a critical E-field as high as 3.3 MV/cm, about 10X higher than Si. Initially explored for optoelectronic applications such as LEDs and lasers, GaN has made its solid path into power electronics industry for its superior properties and good stability even under extreme conditions. The high critical E-field enables GaN devices to achieve high blocking voltage with compact device design, while the high electron mobility provides GaN the high current density and low specific on-resistance that can ultimately translate into the capability to reach high switching frequency.

GaN can be grown on diverse substrates including Si, SiC, Sapphire and GaN depending on specific requirements for quality, cost, scalability and integrity. Homogeneous GaN substrates minimize the lattice mismatch between GaN epi layer and the substrate and thus provides the optimal overall performances, but the cost and scalability issue make it less competitive in commercial market currently. GaN-on-Si is the most economical choice in producing GaN based devices and the ability to integrate with existing Si CMOS technologies makes it attractive to low-voltage rating large-scale production, but the large lattice mismatch between GaN and Si leads to severe defects that

may result in wafer arcing and cracking. GaN-on-Sapphire is also economically adopted in GaN market, especially for LEDs and lasers, but the poor thermal conductivity of Sapphire brings in heat dissipation challenge, which makes it more difficult for high-power applications. SiC has the second low lattice mismatch with GaN, but the high cost also hinders its participation in commercial GaN market.

1.2.2 History and mechanism of GaN HEMT

The concept of HEMT was first proposed in 1980s by Japanese physicist Takashi Mimura based on gallium arsenide (GaAs) MOSFET [2]. Research on GaN-based HEMTs originate in 1993 by Khan [3]. An example of prototype GaN HEMT is shown in Figure 1–3 (a). It incorporates a heterojunction between two materials with different bandgaps to form a channel that does not require impurity doping. The AlGaN/GaN heterojunction creates a 2DEG at the interface due to a combined effect of spontaneous polarization and strong piezoelectric polarization. The 2DEG confines a high concentration of sheet charge at the interface that forms a conductive channel with an electron mobility of as high as up to 2000 cm^2/Vs and a charge concentration of up to 10^{13} cm^{-2} range. This highly conductive 2DEG channel allows GaN HEMT to operate at high switching speed with very low on-resistance and power loss, which makes it desirable for applications like radio frequency (RF) amplifiers, electric vehicles (EVs), and data centers.

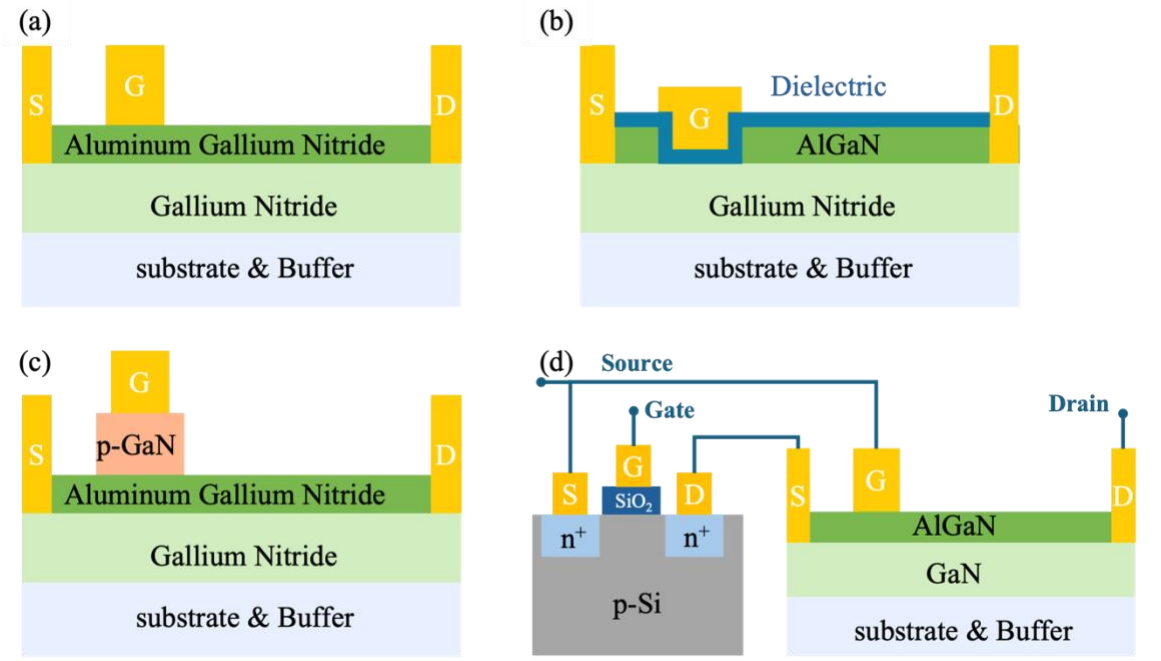

Figure 1–3 (a) Normally-on GaN HEMT. (b) Recessed MIS gate GaN HEMT. (c) p-GaN HEMT. (d) Cascode E-mode GaN HEMT.

Based on the conduction state at gate bias $V_G = 0\ V$, GaN HEMT could be classified into two types, normally-off or enhancement-mode (E-mode), and normally-on or depletion-mode (D-mode). Basic AlGaN/GaN heterojunction HEMT could conduct current even under no gate bias, since the Fermi level crosses the conduction band of the band diagram, as shown in Figure 1–4 (a) and is referred as D-mode. In practical power applications, it is preferrable that current conduction could be controlled through applying positive gate voltage, and therefore research efforts have been made to realize E-mode GaN HEMTs. Several techniques that have been developed and commonly adopted are

summarized in Figure 1–3. On the basis of Figure 1–3(a), Figure 1–3 (b) achieves E-mode by etching the AlGaN under the gate to impair the 2DEG channel. Silicon nitride could also be adopted to realize a MIS gate for the GaN HEMT to rebuild the conduction channel when applying positive gate bias. Figure 1–3 (c) realizes E-mode through growing an additional p-GaN layer during the epitaxial growth, and this p-GaN under the gate could lift-up the conduction band, therefore resulting in E-mode of the GaN HEMTs, as shown in Figure 1–4 (b) band diagram. Another widely-adopted technique in commercial GaN power devices is the cascode structure shown in Figure 1–3 (d), in which the D-mode GaN HEMT is connected in series with an E-mode Silicon MOSFET such that the gate control is through the Si-MOS instead of the normally-on GaN HEMT.

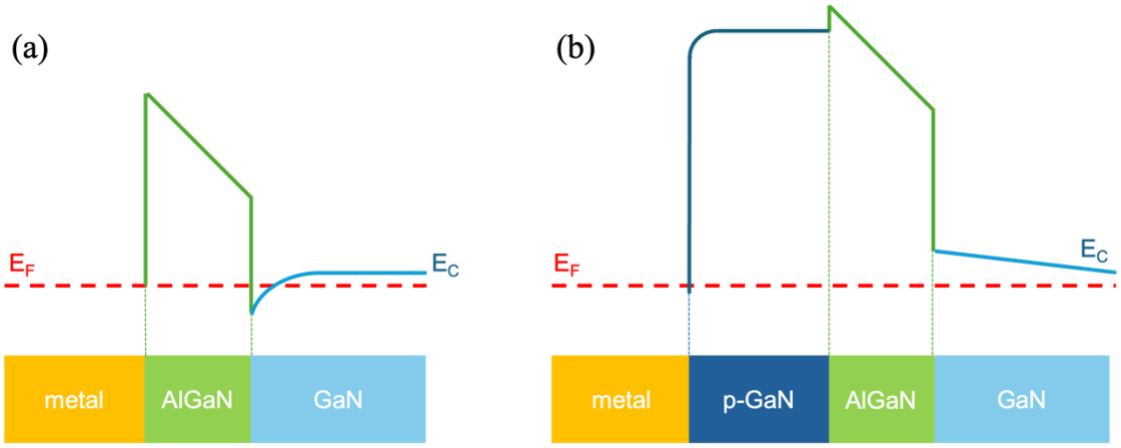

Figure 1–4 Band diagram of normally-on AlGaN/GaN HEMT (a) and normally-off p-GaN/AlGaN/GaN HEMT (b) at zero gate bias.

1.2.3 Commercialization of GaN HEMT

To date, GaN HEMTs have been commercialized in low- and mid-voltage classes from 15 V to 900 V with a targeted market of over $1.25 billion by 2027 [4]. Figure 1–5 provides a summary for current and voltage ratings of commercial and pre-commercial GaN HEMTs from various vendors [5]. Most commercial GaN HEMTs fall below 650 V ratings with various current ratings, while mid-voltage and high-voltage classes still lack competitive participants. Major vendors include Infineon, EPC, Transphorm, GaN Systems, Innoscience, Navitas and Texas Instruments, while more vendors are emerging and entering GaN power electronics market.

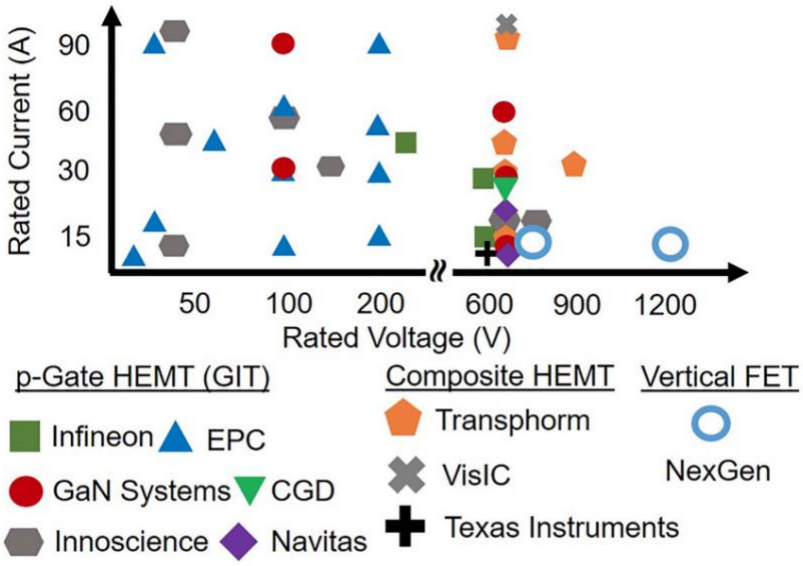

Figure 1–5 Current and voltage ratings of commercial and precommercial GaN devices from various vendors. Figure from [5].

1.3 Challenge and motivation

To enhance the competitiveness of GaN power devices and expand their application spaces, several critical requirements must be taken into consideration:

1) Performance-wise, the trade-offs between off-state blocking capability, on-resistance, and switching speed need to be further improved. The trade-off between breakdown voltage (*BV*) and on-resistance has been a persistent target in optimization of power devices; the performance of current GaN devices is still far from the material limits. Bidirectional devices are also desired to improve circuit performance and reduce device counts in many AC power conversions.

2) Thermal management-wise, improvement can be pursued from the material-based thermal conductivity and the packaging solutions that affect heat dissipation paths [6], [7]. Due to the high cost of GaN-on-GaN homogeneous wafer, most commercial GaN devices are fabricated on heterogeneous epitaxial wafer, and the substrate material also affects thermal managements, which needs to be carefully considered.

3) Reliability-wise, GaN HEMTs face many unique stability, reliability, and robustness challenges [5], [8], [9]. For example, robust gate design ensures stable gate operation, protecting the device from overvoltage and potential degradation and has been extensively studied. Note that reliable high-temperature measurements have been reported on GaN-based transistors, but there remain many gaps on the device switching lifetime under high-temperature, overvoltage, and overcurrent operations.

4) Production- and application-wise, there are still issues centering around the scalable manufacturing, monolithic integration and circuit application. To improve the cost-effectiveness and ensure high yields, optimizing large-scale fabrication process is necessary, especially the etching processes that set the cornerstone for the entire process. Monolithic integration including on-wafer gate driver and bidirectional operation also represents a trending research interest. The gold-less integration process with Si is also desired.

In addition to the above challenges, a fundamental limitation of current GaN HEMTs is the relatively low voltage rating, mostly below 650 V. While vertical GaN devices with unique avalanche capability have demonstrated outstanding reverse-blocking characteristics [10], lateral GaN transistors offer superior integration-capability and scalability, making them preferable solution for power electronics industry. This limitation arises primarily from the highly non-uniform electric field (E-field) distribution within the device structure, predisposing the device to premature breakdown and limiting its operational voltage range. Consequently, the quest for higher voltage capabilities in GaN HEMTs requires the fundamental understanding and effective mitigation of the non-uniform E-field distribution. For this, innovations in device architecture are essential.

In this work, we explore the deployment of the p-GaN based Reduced Surface Field (RESURF) structure to balance the net charge in the 2DEG channel in GaN HEMT to enable a uniform distribution of E-field, which would be particularly advantageous for voltage upscaling in GaN HEMT. Based on this core idea, we develop new device structures with different form factors and apply them into unidirectional and bidirectional GaN HEMTs, experimentally demonstrating the capabilities to upscale the voltage class of GaN HEMTs to 10 kV with superior performance than the Si and SiC counterpart. The device design, fabrication, and characterization are presented comprehensively in this thesis.

1.4 Dissertation outline

Chapter 1 provides an overview of power semiconductor devices, including their historical background, operation mechanisms, and some principal participants in the market. The remaining of this chapter focuses on a comprehensive introduction about GaN power devices, including history, advantages, applications, and current commercialization status, followed by an outline of the challenges and motivations for this research.

Chapter 2 explores the design, fabrication, characterization and breakdown mechanism analysis of a 10-kV unidirectional p-GaN RESURF HEMT. This chapter commences with an investigation of state-of-the-art high-voltage GaN transistors designs, followed by a novel design that enables the upscaling of breakdown voltage to over 10-kV regime. Structures with varying RESURF thicknesses and lengths are included in the breakdown mechanism study, which will be verified by physics-based simulation.

Chapter 3 builds upon the p-GaN design presented in previous chapters and showcases the first demonstration of a 3.3-kV monolithic bidirectional switch. The design, fabrication and characterization are included, and a detailed characterization setup for two forward operation modes and off-state operation are outlined. Mechanism studies and simulation results are provided as well.

Chapter 4 summarizes the work above and proposes several potential research avenues for future works.

2 Chapter 2: 10-kV unidirectional p-GaN RESURF transistors

2.1 State-of-the-art 5-kV+ devices

Although most commercial GaN HEMTs have been confined to <1200 V regime, GaN transistors with higher breakdown voltage have been widely studied, and several over 5 kV cases have been realized through varying techniques. Over 10-kV GaN HEMT was firstly demonstrated in 2009 with the poly-AlN passivation between the gate and the drain [11], but the very high $R_{on,sp}$ of 186 mΩ·cm^2 and the D-mode operation make the device less competitive than similarly-rated SiC MOSFET. Recently, state-of-the-art 10-kV GaN HEMT has been successfully demonstrated on multi-channel GaN-on-Sapphire wafer with a low $R_{on,sp}$ of 40 mΩ·cm^2 [12]. Table 2-1 summarizes state-of-the-art high-voltage GaN HEMTs, featuring their gate design and operation mode (enhancement or depletion), breakdown voltage, $R_{on,sp}$, and their key design to manage the high E-field. The device that will be discussed in the following sections is also included and marked as this work. The corresponding device structures are presented in Figure 2–1.

Table 2-1 Comparison and summary of state-of-the-art 5 kV+ high-voltage GaN transistors.

Ref	***BV*** **[V]**	**Key design**		**Mode**	$R_{on,sp}$ **[mΩ·cm^2]**
		E-field	**Gate**		
Panasonic[11]	10400	Poly-AlN passivation	GIT	D	186
VT[12]	10700	multichannel	cascode	E	40
PSU[13]	10000	Delta-doping+p-GaN	recessed	E	73.5
PKU[14]	6573	Active passivation	p-GaN	E	33.62
POWDEC[15]	10000	Polarization superjunction	p-GaN	D	78.7
This work	>10000	RESURF	p-GaN	E	66.12

As shown in Figure 2–1 (a) and (b), state-of-the-art over 10-kV devices both utilize the low resistance high conductivity multichannel AlGaN/GaN structure to achieve improved $R_{on,sp}$ performances. However, the e-mode realization becomes a coherent issue for multichannel devices, since the complicated charge conduction mechanism in double- or multi-channel structures requires all channel to be controlled at the same time, or a cascode E-mode MOSFET is required to control the overall on/off. Figure 2–1 (a) adopts the cascode structure to realize the E-mode operation, while Figure 2–1 (b) adopts the recessed p-GaN gate to realize the simultaneous control of the double channel. E-mode was automatically realized in Figure 2–1 (d) with a p-GaN gate, while Figure 2–1 (c) and (e) are both depletion-mode normally-off GaN HEMTs.

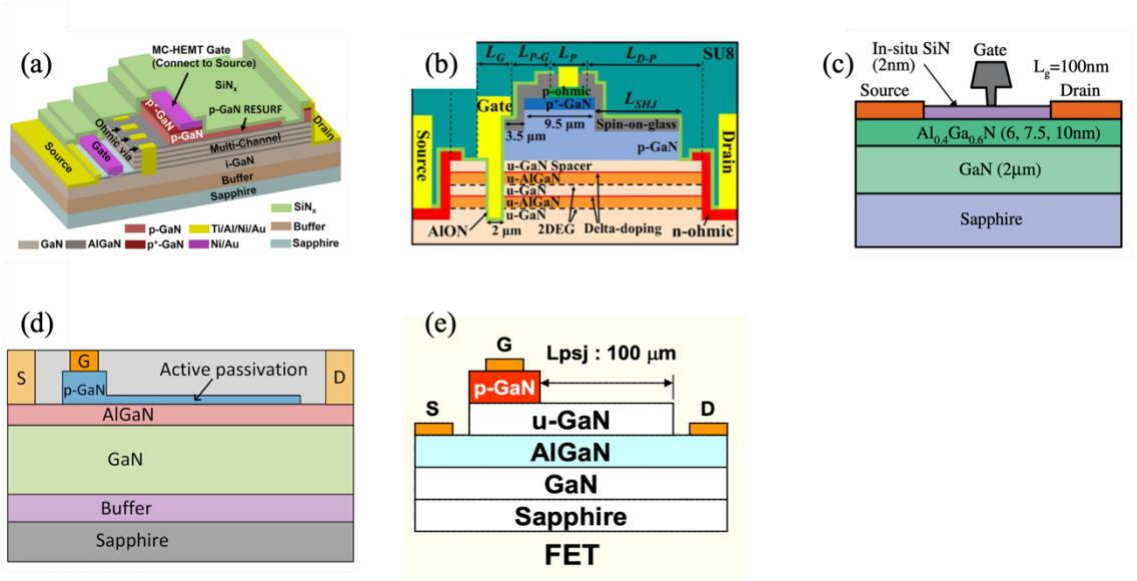

Figure 2–1 (a) Multichannel cascode GaN HEMT[12]. (b) Delta-doped double channel GaN HEMT[13]. (c) Poly-AlN passivation GaN HEMT[11]. (d) Active passivation GaN HEMT[14]. (e) Polarization superjunction GaN HEMT[15].

The most important issue in upscaling breakdown voltage in GaN HEMT is the highly non-uniform electric field (E-field) distribution within the device structure, as discussed in Chapter 1.3. Different approaches are adopted for E-field management. In Figure 2–1 (a) and (d), similar p-GaN RESURF structure is utilized to assist the E-field management between the gate and the drain; Figure 2–1 (b) further integrates delta-doping between AlGaN/GaN double channels to achieve charge balance condition with the p-GaN on top, while natural superjunction and surface passivation are employed in Figure 2–1 (c) and (e), both to suppress the high E-field peak between the gate and the drain.

2.2 Design and fabrication

2.2.1 RESURF: history and physics

RESURF, also known as Reduced Surface Field structure, has been widely used in Si power devices starting from 2000s in lateral MOSFET devices to achieve improved breakdown performances without hindering R_{ON} by manipulating the E-field distribution along the surface [16]. Initial demonstration of RESURF technology involves the

incorporation of an extra vertical p-n junction that supports charge depletion and achieves high *BV*, as shown in Figure 2–2.

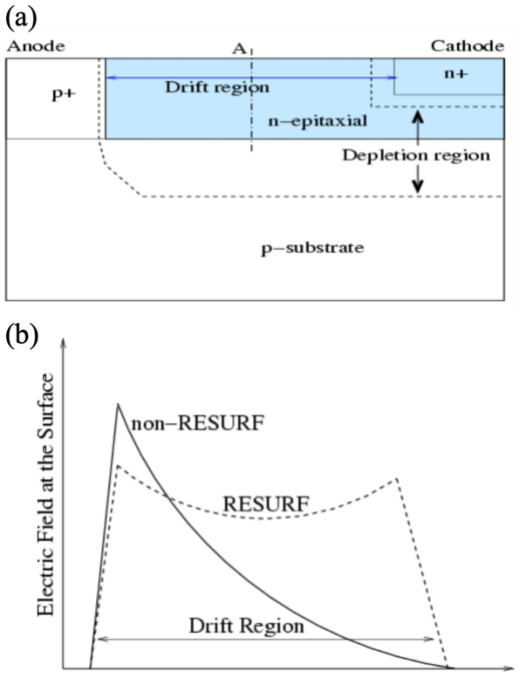

Figure 2–2 (a) Demonstration of lateral RESURF structure. (b) E-field distribution across the surface with and without RESURF. Figures from [17].

2.2.2 RESRUF p-GaN HEMT design

Inspired by the voltage breakthrough by multi-channel (MC) HEMT in our prior work [12], our design utilizes the RESURF structure and integrates it into a common commercial p-GaN/AlGaN/GaN-on-Sapphire wafer, aiming to realize E-mode GaN HEMT with high off-state blocking performance. The 2-D schematics of multichannel MC-HEMT and single-channel p-GaN RESURF HEMT design are presented in Figure 2–3. It could be easily recognized that the gate formation of MC-HEMT is considerably more complicated, necessitating the incorporation of a low-voltage MOSFET with a recessed gate to realize normally-off operation. Our primary goal is to realize E-mode operation without additional complexity on the gate and to allow the device manufacturing based on the established p-GaN HEMT foundry fabrication process.

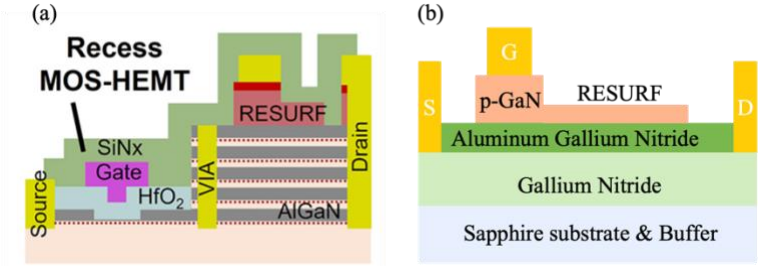

Figure 2–3 (a) Cascode MC-HEMT. Figure from [12]. (b) Schematic of RESURF single-channel p-GaN HEMT design.

2.2.3 Fabrication process

The devices were fabricated on a conventional 2-in GaN-on-Sapphire wafer grown by Enkris Semiconductor, featuring an AlN transition layer, a 1.5 µm carbon-doped GaN buffer, a 200 nm undoped GaN channel, a 15 nm $Al_{0.2}GaN_{0.8}$ barrier layer, and an 80 nm p-GaN cap layer with Mg concentration of ~ 2×10^{19} cm^{-3}. Figure 2–4 (a) depicts a 3-D schematic of designed p-GaN RESURF HEMT featuring $L_G/L_{GS}/L_{GD}$ = 3.5/1.5/25 µm and RESURF length L_{RES}=17 µm, and the corresponding SEM image of fabricated device is shown in Figure 2–4 (b). To accurately understand the doping profile for RESURF design consideration, secondary ion mass spectrometry (SIMS) was carried out and presented in Figure 2–4 (c).

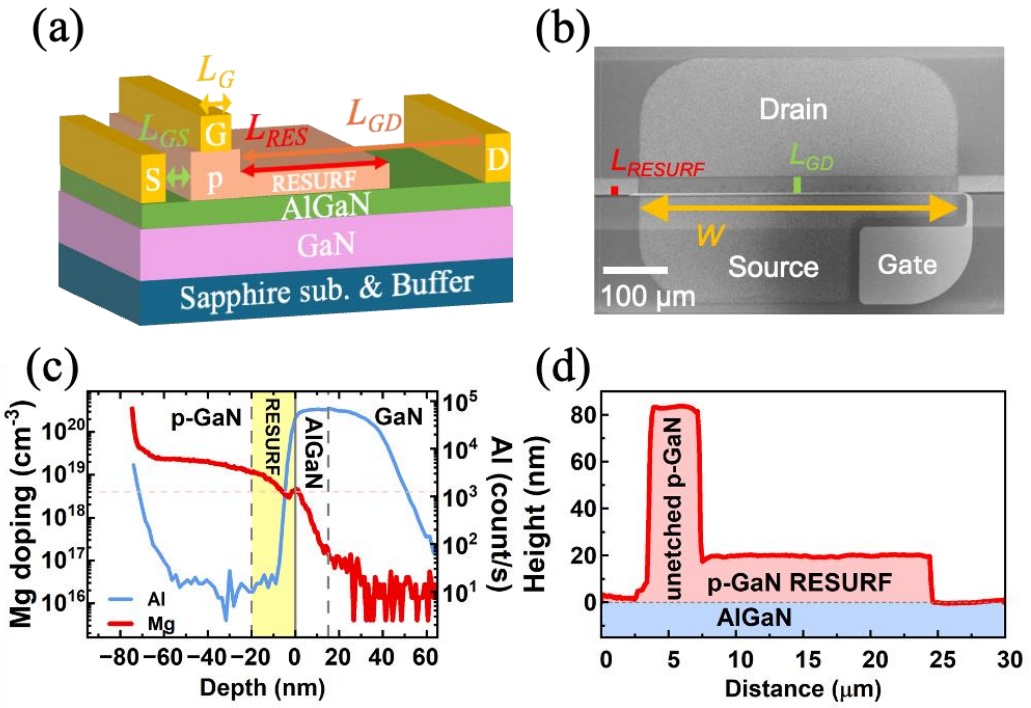

Figure 2–4 (a) Schematic of RESURF p-GaN HEMT. (b) Top-view SEM image of fabricated p-GaN HEMT. (c) SIMS profile for Mg doping and Al concentration of wafer used. (d) AFM height profile of etched sample with t_{RES}= 17 nm.

Device fabrication commenced with a two-step p-GaN etch, starting with a partial etch of ~10-50 nm outside of gate and RESURF region, followed by a self-termination etch with a RESURF thickness defined in the first etch. SF_6 is added in the second etch for an etch stop at the AlGaN surface. Detailed etching information will be provided in later discussions. As shown in Figure 2–4 (d), Atomic Force Microscopy was utilized to verify the height of the RESURF. 25% TMAH and 20:1 BOE rinse were employed to smooth the etched surface after etching. Source and drain ohmic contacts were formed through e-beam evaporated Ti/Al//Ni/Au metal stack of 22/150/55/45 nm, and annealed at 850 ℃ in the N_2 ambient thermal annealing for 30 s, yielding a contact resistance of 1.3 Ω·mm. Following the mesa planar isolation, 50/200-nm Ni/Au was deposited as gate contact metal, which was then annealed in N_2 ambient at 500 ℃ for 5 min. The device was passivated with photoresist for high-voltage measurement.

2.2.4 Two-step etching mask design for RESURF formation

Since dry etching and subsequent inorganic and organic cleaning procedures may introduce damage and contamination to the surface, reducing the etch step is preferred through the fabrication process. Conventional RESURF etch (illustrate in Figure 2–5 (a)) comprises 3-step etching, including removing all p-GaN outside the gate and RESURF area, controlled etch on RESURF, and RESURF termination etch between the RESURF end and the drain (i.e., the etch to create a spacing between RESURF edge and drain). During the 2nd and 3rd etch step, due to photolithography mismatch and anisotropic etching directions, additional undesired etch might be applied to the termination area, potentially leading to damage of the 2DEG channel if the AlGaN layer is damaged. In our 2-step mask design (shown in Figure 2–5 (b)), the 2nd etching step encompasses the termination area up to the source. Consequently, no additional etching will be applied to AlGaN surface once etch stop condition is reached.

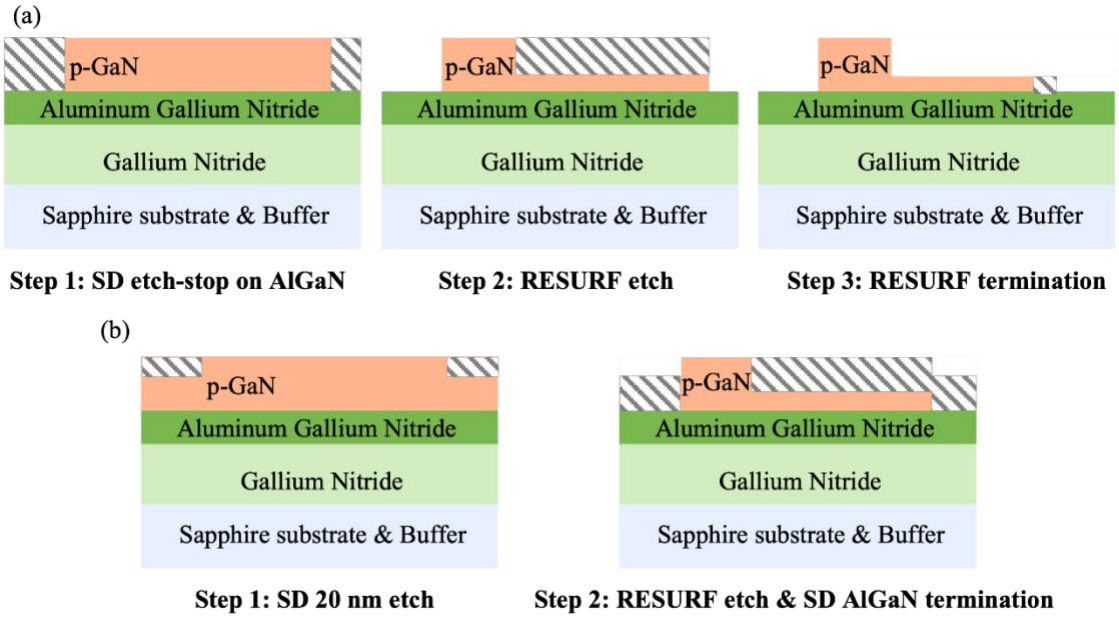

Figure 2–5 (a) Conventional 3-step RESURF etch. (b) 2-step RESURF etch design. Shaded area represents the etching region and depth in each etching step.

2.2.5 Controllable slow p-GaN etch

Given the relatively narrow process window permitted by the initial etch step (etching depth between 15-25 nm), a precise, slow etching recipe with minimal etching damage is essential. Most existing GaN etch recipe employs chlorine-based gases including Cl_2 and BCl_3, which facilitate rapid etch rate but lack precise control. The high doping concentration of p-GaN layer introduces additional challenges to this controlled slow etch, since the highly doped p-GaN is more susceptible to develop micromaskings in pure chlorine-based etch.

A new recipe was developed to achieve a stable and controlled etching rate of 15 nm/min, which enabled the etching time window to reach minutes-range instead of seconds-range for pure chlorine-based etch. The detailed power, pressure, temperature and gas flow parameters are summarized in Table 2-2:

Table 2-2 Controlled slow p-GaN etch recipe parameters.

RF power (W)	ICP power (W)	Pressure (mTorr)	Temperature (°C)	Gas flow (sccm)			
				Cl_2	BCl_3	Ar	C_4F_8
30	300	10	20	5	15	3	20

In this etching recipe, chlorine-based Cl_2 and BCl_3 serve the primary chemical etching function, while Ar is added to remove micromaskings formed during the etch, and C_4F_8 serves as a buffer gas to prevent bird's beak effect that may result in damage of 2DEG channel at the corner where chemical reactions occur with the greatest frequency. Scanning Electron Microscopy (SEM) was carried out after each etching step and the comparison of SEMs for samples subject to conventional Cl_2 etching and new recipe etching is presented in Figure 1–1. It could be clearly recognized that this Ar/ C_4F_8 involved etching recipe not only provides a controlled etching rate, but also minimizes micromasking effects and results in a smoother p-GaN surface after etching.

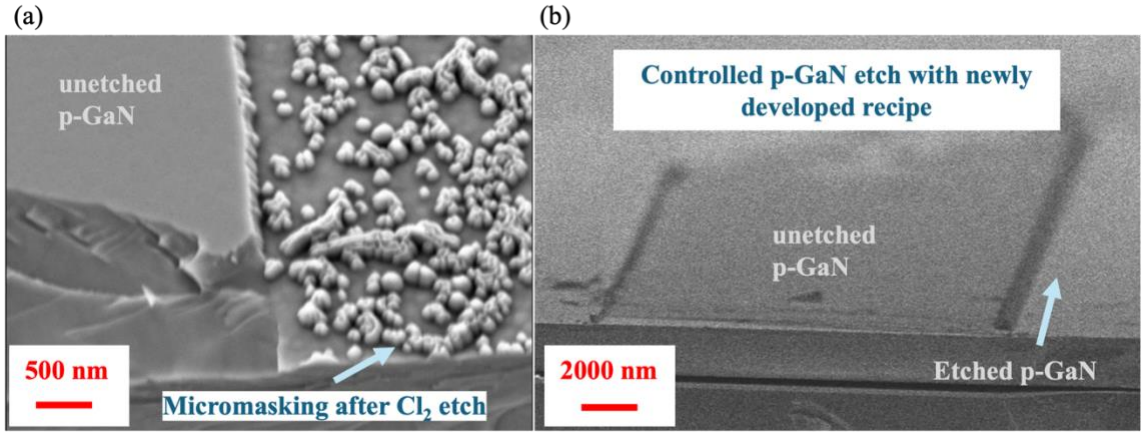

Figure 2–6 SEM image of GaN sample experiencing (a) pure chlorine-based and (b) Ar/C_4F_8 involved etching.

2.2.6 AlGaN/GaN high-selectivity etch

In order to establish a reliable ohmic contact at source/drain region and to avoid punch-through leakage at RESURF termination region, a complete removal of p-GaN without damaging the AlGaN layer beneath is required to protect the 2DEG channel. The Ar/C_4F_8 involved etching recipe above serves the first-step etch perfectly, but the etch rates on GaN and AlGaN are very similar, which makes it difficult to achieve a precise etch stop on the AlGaN surface.

Previously, oxygen (O_2) has been introduced into Chlorine-based GaN etch recipe to achieve etch-stop on AlGaN surface. It was discovered that a carefully tuned $Cl_2/N_2/O_2$ gas mixture combining with low-energy etching power, the etch could automatically stop on AlGaN surface with a negligible etch rate of as low as 0.6 nm/min. The mechanism is that during the dry etching process, oxygen infuses into the AlGaN surface, forming an etching-resistant oxide film (Al,Ga)O_x, which prevents further etching into the AlGaN surface[18].

However, during the oxygen etching process, severe micromasking and birds' beak effect were observed in our highly-doped p-GaN wafer. Additionally, the rapid etch rate of

photoresist in oxygen (approximately 20X faster than p-GaN etch rate) requires a thick photoresist mask, which is unsuitable for feature sizes below 2 μm. The fast etch of PR and resulting unprotected over-etch of p-GaN are shown in Figure 2–7.

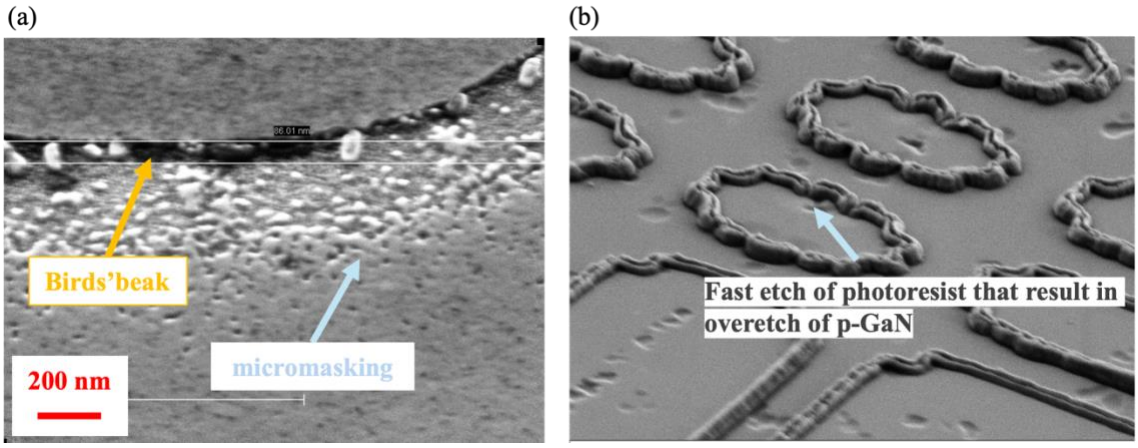

Figure 2–7 Damaged surface after oxygen-involved dry etch.

Given the knowledge base that $(Al,Ga)O_x$ film could serve as the etch stop layer, SF_6 was considered as a substitute for oxygen in self-termination etch recipe, as it can form an etch-resistance layer similar to $(Al,Ga)O_x$. To ensure precise etch-stop on the AlGaN surface, a low etch rate is preferred even with high-selectivity AlGaN/GaN etching recipe. Consequently, a gas mixture of BCl_3/SF_6 is employed to facilitate self-termination p-GaN etch. Detailed etching parameters are provided in Table 2-3.

Table 2-3 High selectivity AlGaN/GaN etch recipe parameters.

RF power (W)	ICP power (W)	Pressure (mTorr)	Temperature (°C)	Gas flow (sccm)		Etch rate (nm/min)	
				SF_6	BCl_3	GaN	AlGaN
60	300	40	20	5	15	22	<1

As documented in previous reports, SF_6, functioning analogously to O_2, reacts with AlGaN surface, forming a $(Al,Ga)F_x$ compound that covers the AlGaN layer and effectively inhibits further etching [19], [20]. Besides, it is also anticipated that the micromasking effect would be reduced because of the non-volatility of SiF_4 side product generated in etching chamber, compared with the SiO_2 byproduct in oxygen-based recipes [19]. It should be noted that compared with slow-etch recipe, selective etch was processed with significantly higher chamber pressure (~5X higher), which was due to the fact that increasing chamber pressure enables a more sufficient interaction between SF_6 and AlGaN surface, thereby improving GaN/AlGaN etching selectivity. Additionally, it has been proven in experiments that fluorine-based selectivity recipe etches photoresist mush slower than oxygen-based recipe, allowing for the usage of thinner photoresist with finer feature sizes.

Scanning electron microscope (SEM) was carried out after each etching step to check the RESURF status. AlGaN and GaN exhibit different colors under Inlens detector, attribute to varying density of electrons reflected from the AlGaN and GaN surface. An

even distribution of dark area is anticipated for AlGaN surface, which is shown in Figure 2–8.

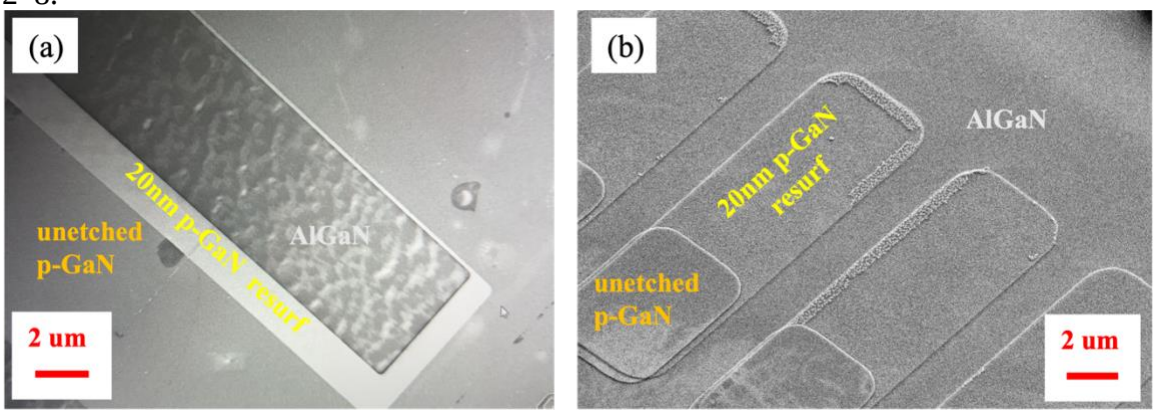

Figure 2–8 SEM image of GaN RESURF structure after 2-step etching.

2.3 Characterization and IV analysis

Electrical characterization was conducted with Keysight B1505A Power Device Analyzer and the ultra-high voltage expander. Devices with RESURF thickness (t_{RES}) ranging from 13 nm to 50 nm were fabricated for performance evaluation under different designs. Two design systems were configured to study the RESURF structure and its corresponding mechanism: 1) fixed RESURF-to-drain distance of 8 µm with varying L_{GD} = 10/15/20/25/30/35 µm; 2) fixed L_{GD} = 25 µm with varying L_{RES} = 4/6/8/12/17 µm. Longer devices with L_{GD} = 100 µm were fabricated using the optimal RESURF thickness of 17 nm to explore the voltage up-scalability of this RESURF p-GaN HEMT design.

2.3.1 On-state I-V characteristics

Figure 2–9 illustrates the on-state transfer characteristics of the two set of devices designed above fabricated on wafer with t_{RES} = 17 nm. The applied drain voltage was maintained at 5 V for both measurements, and all current levels were normalized to current density in mA/mm with device width of 500 µm. All devices exhibit typical transistor behaviors, with similar threshold voltages of approximately 0.5 V extracted at I_D = 10 µA (0.005 mA/mm), as marked in the Figure. The drain current density of all devices ranges from 150 mA/mm to 220 mA/mm, with a gate leakage current of below 10 mA/mm. The RESURF HEMT show a minimum subthreshold swing (*SS*) of 61.35 mV/decade, and a $10^6 \sim 10^8$ current on-off ratio. It should be noted that some devices are subject to fabrication deviations and display different on-off ratios.

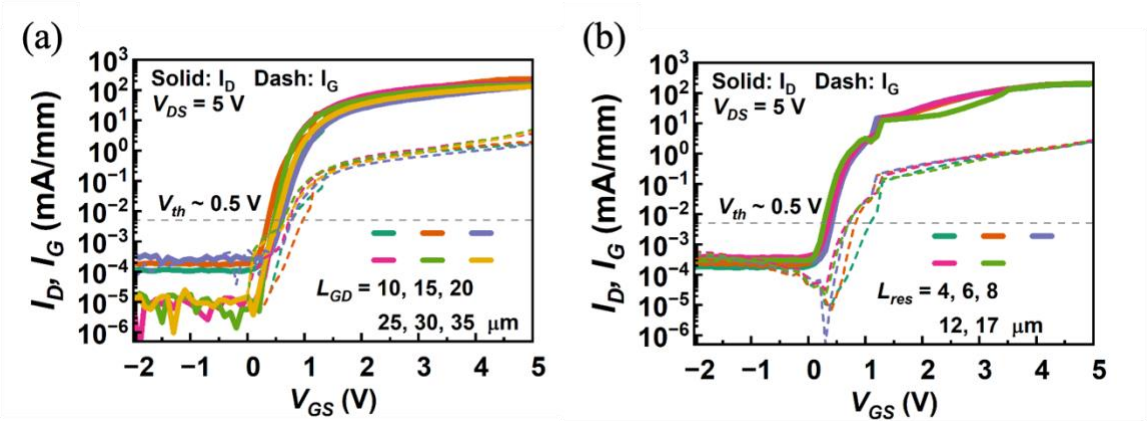

Figure 2–9 Transfer characteristics of fabricated devices with (a) fixed L_{RES}-Drain spacing distance with varying L_{GD} = 10/15/20/25/30/35 µm and (b) fixed L_{GD} = 25 µm with varying L_{RES} = 4/6/8/12/17 µm.

Figure 2–10 represents the output characteristics measured from devices with L_{GD} = 25 µm and L_{RES} = 4 and 17 µm. The linear fit suggests an on-resistance of 18.4 Ω·mm and 20.4 Ω·mm for RESURF lengths of 4 µm and 17 µm, corresponding to a specific on-resistance ($R_{on,sp}$) of 6.07 mΩ·cm^2 and 6.73 mΩ·cm^2, calculated with an L_{SD} of 30 µm and an contact transfer length of 1.5 µm each for the source and drain contact. It could be observed that increasing $R_{on,sp}$ results from the increasing series resistance with longer RESURF, since the depletion of 2DEG channel from p-GaN would increase channel resistance.

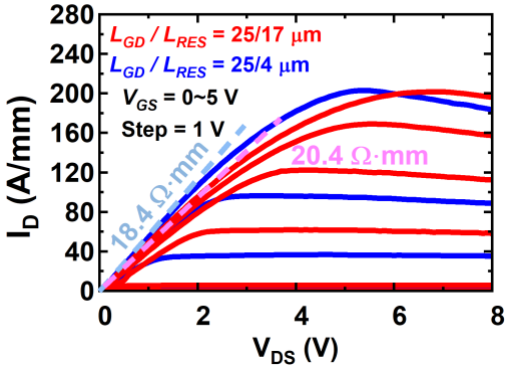

Figure 2–10 Output characteristics of fabricated RESURF HEMT with fixed L_{GD}=25 µm and varying L_{RES} = 4/17 µm.

2.3.2 Off-state I-V characteristics

Figure 2–11 shows the off-state blocking characteristics for devices fabricated on a wafer with a RESURF thickness (t_{RES}) of 17 nm and a fixed RESURF-to-drain distance of 8 µm. Devices with gate-to-drain distances (L_{GD}) of 10, 15, 20, 25, 30, and 35 µm achieved *BV* of 810 V, 1657 V, 2851 V, 3436 V, 4233 V, and 5086 V, respectively. This showcases an excellent *BV* upscaling capability by enlarging the gate-to-drain distances.

Such *BV* upscaling capability is in fact contrary to the classic natural superjunction theory [21], [22]. The natural superjunction theory suggests that the polarization charges in the AlGaN/GaN heterostructure can self-balance, resulting in a net zero charge after the heterostructure is fully depleted. When applying this classic theory to our device, the depleted acceptors in p-GaN will result in considerable net negative charges, which should

result in highly non-uniform E-field and disallow the *BV* to upscale with L_{GD}. In our RESURF HEMT, the linear increase in *BV* with L_{GD} suggests the presence of intrinsic deep donors in AlGaN and/or p-GaN, which is naturally balanced by the net acceptor charges in p-GaN.

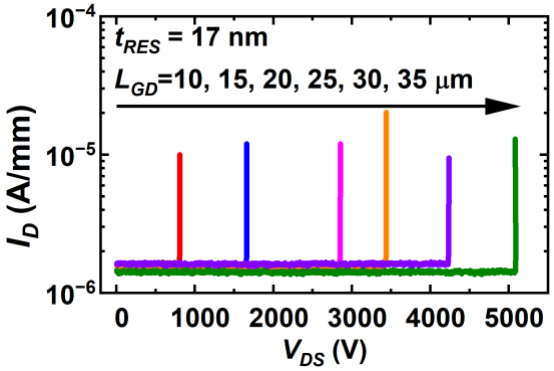

Figure 2–11 Off-state I-V characteristics of devices fabricated on t_{RES} = 17 nm with a fixed RESURF-to-drain distance of 8 µm and various L_{GD} of 10, 15, 20, 25, 30, and 35 µm.

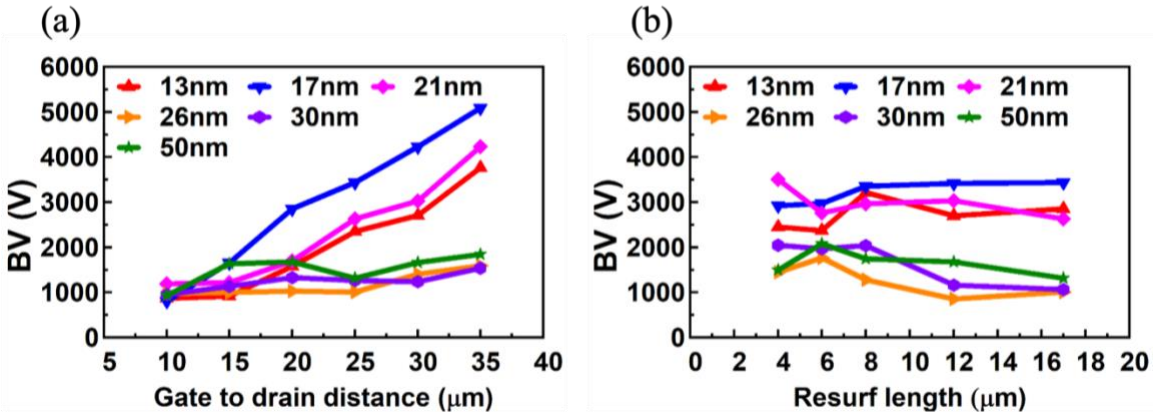

Figure 2–12 (a) *BV* vs. L_{GD} for t_{RES} ranging from 13 to 50 nm. (c) *BV* vs. L_{RES} for t_{RES} ranging from 13 to 50 nm.

Figure 2–12 presents *BV* trend for devices with RESURF thicknesses ranging from 13 to 50 nm. From Figure 2–12 (a), devices with t_{RES} < 21 nm demonstrate scalable *BV* with increasing L_{GD}, whereas excessive RESURF thickness limits *BV* increases, as evidenced by the limited improvement in *BV* in Figure 2–12 (a) with t_{RES} = 26, 30 and 50 nm. This finding suggests an ideal t_{RES} range to achieve optimal *BV* performance. Figure 2–12 (b) presents *BV* results for devices with L_{GD} = 25 µm of varying RESURF lengths and t_{RES} . For t_{RES} < 21 nm, *BV* increases slightly with RESURF length, likely due to improved charge balance between intrinsic donors and acceptors in p-GaN. However, thicker p-GaN layers negatively impact *BV* at longer L_{RES}, as high acceptor concentration leads to charge imbalance and electric field crowding. These findings provide further support for the existence of a RESURF thickness process window in RESURF p-GaN HEMT design; the E-field management could drastically deteriorate for the thicker p-GaN RESURF design due to excess charges.

2.3.3 Over 10-kV RESURF GaN HEMT

The aforementioned breakdown studies suggest that 17 nm represents an optimal RESURF thickness for the current epitaxial structure. Devices with L_{GD} = 50/75/100 µm were fabricated on t_{RES} = 17 nm wafer to investigate the *BV* scalability of RESURF design. Figure 2–13 (a) depicts the output characteristics for fabricated device with L_{GD} = 100 µm and L_{RES} = 30 µm, with an on-resistance extracted to be 50.4 Ω·mm at V_{GS} = 5 V. Figure 2–13 (b) presents a comparison of the transfer characteristics for devices with L_{GD} = 25/100 µm and L_{RES} = 17/30 µm, in which the threshold voltage are both close to 0.5 V. The drain current density for L_{GD} = 25 µm devices is twice higher than L_{GD} = 100 µm device, which is consistent with expectation given the increasing series resistance from the channel resistance increase.

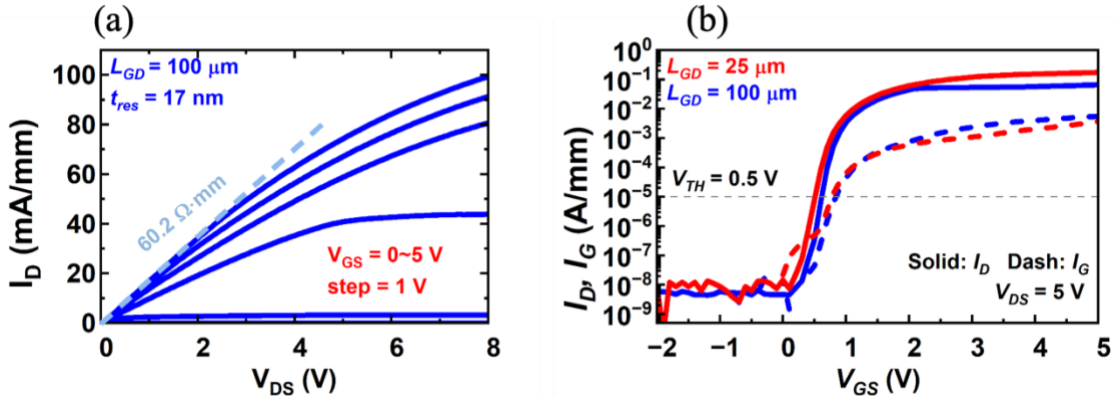

Figure 2–13 (a) Output for device with L_{GD} = 100 µm (b) Transfer characteristics for devices with L_{GD} = 25/100 µm.

Figure 2–14 depict the off-state I-V characteristics of longer devices with over 9 kV breakdown voltage. Five devices have demonstrated *BV* in the range of 9.2 – 10 kV, while two devices have successfully blocked 10-kV, underscoring the high-performance potential of optimized RESURF structures. The drain leakage level remained at a stable nano-ampere level before breakdown, which indicates outstanding off-state blocking capability of RESURF p-GaN HEMT even with longer devices and larger sizes.

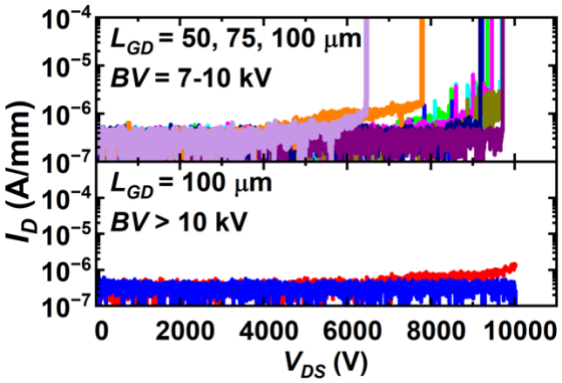

Figure 2–14 Over 9 kV breakdown performance of L_{GD} = 50, 75 and 100 µm devices.

2.4 Benchmark

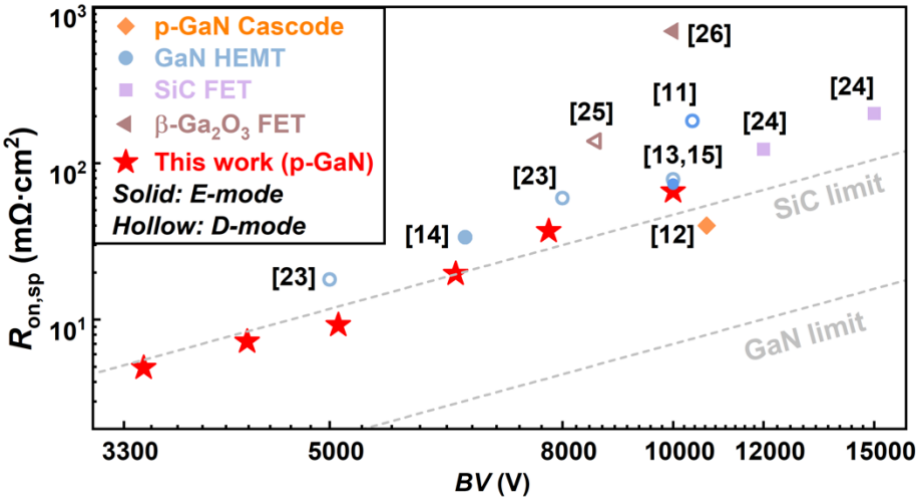

Figure 2–15 Benchmark of $R_{on,sp}$ *vs. BV* for state-of-the-art high voltage GaN transistors .

Figure 2–15 benchmarks the $R_{on,sp}$ *vs. BV* for our device and the state-of-the-art high-voltage GaN HEMT[11], [12], [13], [14], [15], [23], [24], [25], [26]. It should be noted that although our overall performance is inferior to our previous work on cascode MC-HEMT [12], it was fabricated on conventional p-GaN/AlGaN/GaN epitaxial wafer and does not require special multichannel or delta-doped wafer. Furthermore, the fabrication process is considerably simpler, as a normal Ni/Au gate stack with post-gate annealing was employed without any recessed gate and/or special treatment on the p-GaN gate. Our lower-voltage devices have also exhibited outstanding performance in the $R_{on,sp}$ and *BV* trade-off, and have demonstrated promising up-scalability in the higher voltage regimes.

3 Chapter 3: 3.3 kV monolithic bidirectional transistor

3.1 Bidirectional switch: introduction and status

3.1.1 Mechanism

Bidirectional switch (BDS) capable of blocking bipolar voltage in the off-state and conducting current in the on-state in both directions is a crucial component in power electronic industries for AC applications, including current source inverters and matrix inverters [27], [28]. The bidirectional blocking and conduction capability enables an efficient power control, supporting dynamic load conditions without the need of excessive circuit components.

Traditional bidirectional devices are realized through combining discrete devices – for instance, an anti-series connection of two MOSFETs or HEMTs. This design results in at least fourfold increase in chip area, as the on-resistance of each of the two devices needs to be a half of the total R_{on} of the BDS (thereby twice the chip size for each device). This leads to higher cost and device counts.

Monolithic Bidirectional Switches (MBDS) targets to circumvent the area and efficiency penalties of traditional BDS built by discrete devices. The MBDS is fabricated with a single, shared drift region with bidirectional controls, preserving the device compactness by factoring only slightly larger chip size compared with similar unidirectional products.

In the last decade, significant research efforts have been dedicated to the development of MBDS based on SiC MOSFETs [29], [30]and GaN HEMTs[31], [32], [33], [34], [35]. The schematics of SiC MBDS and GaN MBDS are shown in Figure 3–1. As observed from Figure 3–1 (a), SiC MOSFET based MBDS integrate two vertical SiC MOSFET into a lateral device, each in parallel with a Schottky diode to overcome the body diode and enable the dual-direction current-flow through the Schottky diode. However, this device suffers from large $R_{on,sp}$ issue, since the current conduction first flows through two vertical drift-region before deviating into the lateral direction. In comparison, lateral GaN HEMT based MBDS allows current to flow laterally entirely in both directions and only comprise a single drift region, offering improved $R_{on,sp}$ performance.

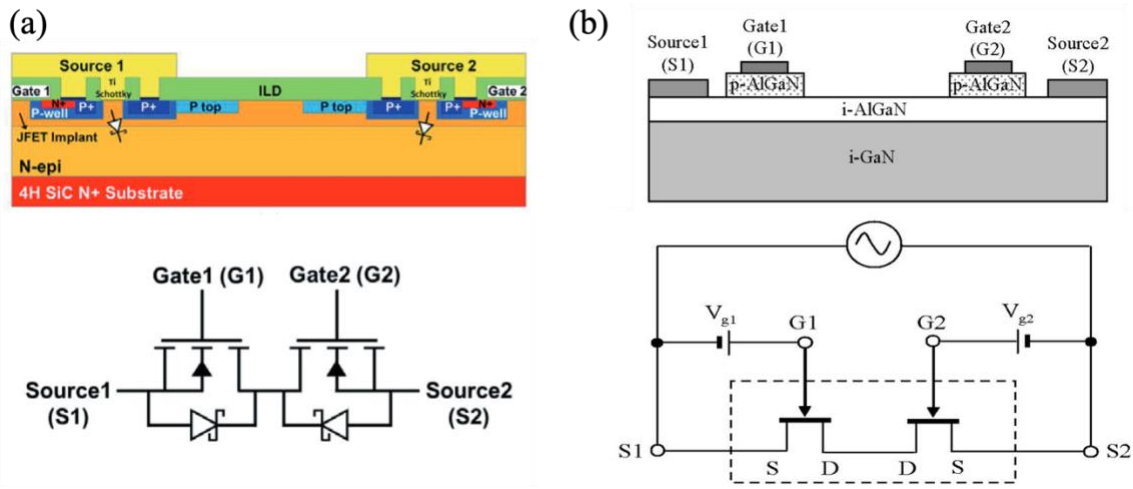

Figure 3–1 Schematic and circuit model of SiC MOSFET-based (a) and GaN HEMT-based (b) MBDS. Figures from [29] and [31].

3.1.2 Industrial development

The development of GaN MBDS has grown fast in the past decade since its first demonstration in 2007 [31]. With a forecasted total market size of $2.5 billion by 2029 for GaN

power devices, GaN MBDS is regarded as a competitive participant for its potential application on electric vehicles, data center and consumer electronics [36]. Leading companies including Infineon have announced nearing-market GaN MBDS available at 40-V, 650-V and 850-V voltage rating [37].

3.2 Design and fabrication

3.2.1 p-GaN JTE design

Despite the rapid progress, the voltage ratings of GaN MBDS devices are still constrained to 600-1200 V, with the reported blocking voltage up to 1500 V [38]. Compared with unidirectional device, MBDS suffers from more challenging E-field management due to the bidirectional blocking requirement. The realization of normally-off operation poses another challenge in the commercialization of GaN MBDS.

Most reported GaN MBDS adopts field-plate structure, which has been widely utilized in commercial unidirectional high-voltage GaN HEMTs. To avoid the complicated fabrication process and high-quality dielectric requirements for the field-plate structure MBDS, here we propose a p-GaN junction termination extension (JTE) design connected to each gate stack for E-field management, inspired the efficacy of using p-GaN-based structures for *BV* upscaling reported in unidirectional GaN devices in Chapter 2. Figure 3–2 presents the schematic of designed p-GaN JET MBDS. This proposed design is not only symmetric, but also constructed on standard p-GaN/AlGaN/GaN epi wafer without any additional requirements for regrowth and/or delta-doping.

Figure 3–2 Schematic of the proposed GaN MBDS with p-GaN JTE

3.2.2 Fabrication process

The epi consists of an AlN layer, a 1.5 μm carbon-doped GaN buffer, a 200 nm undoped GaN channel, a 15 nm $Al_{0.2}Ga_{0.8N}$ barrier, and an 80 nm p-GaN cap layer ([Mg] ~ 2×10^{19} cm^{-3}), all grown on sapphire substrate by Enkris Semiconductor. After p-GaN removal, the sheet resistance (R_{sh}) of is about 450 Ω/sq.

The fabrication commences with two p-GaN etch steps, with the JTE region only subject to the second etch while all other non-gate regions subject to both etches. Detailed etching recipe and steps are described in Chapt.2.2. The first etch employs chlorine gases, while SF_6 is added in the second etch for an etch stop at the AlGaN interface. The JTE thickness (t_{JTE}) is defined by the first etch. Three samples with a t_{JTE} of 10, 20 and 30 nm are fabricated. Figure 3–3(b) shows the surface height profile for an exemplar sample with 20-nm t_{JTE} measured by atomic force microscopy (AFM). After etching, samples are rinsed in a 20:1 BOE solution for 2 minutes. Source and drain Ohmic contacts are formed by Ti/Al/Ni/Au with 850 °C annealing. After device isolation, a gate metal stack of Ni/Au (50/200 nm) is formed, followed by 500 °C annealing in N_2. The device is passivated in a SU-8 resist similar to [12] for high-voltage measurement. Figure 3–3(c) shows the top-view scanning electron microscopy (SEM) image of the fabricated device. S1, G1, G2 and S2 represent Source 1, Gate 1, Gate 2, and Source 2, respectively. On each side, the source-gate length and gate length are 1.5 and 3.5 μm, respectively. The spacing between two gates (L_{G1G2})

is fixed at 19 μm. The JTE length (L_{JTE}) varies from 3 μm, 5 μm, to 7 μm. Similar device without p-GaN JTE is also fabricated.

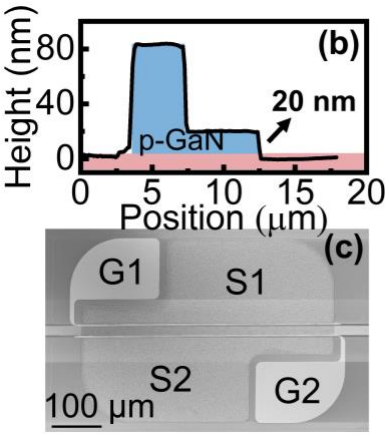

Figure 3–3 AFM height profile of p-GaN gate and JTE and top-view SEM image of the fabricated device.

3.3 Characterization and I-V analysis

3.3.1 On-state I-V: diode mode and transistor mode

The MBDS device characterization requires a synchronous bias modulation at three terminals, G1, G2 and S2. Here we employ a standard transistor test setup with an additional circuit board, on which an isolated power supply is used to provide the bias between the second gate and its neighboring source. The bias schemes for characterizing various operational modes are presented below.

The threshold voltage and operation mode of unidirectional devices with the same design has been verified to be E-mode with V_{th} = 0.5 V in Chapt. 2.3.1. in on-state I-V measurements. To obtain the transistor-mode on-state I-V characteristics for MBDS in one direction (i.e. for G1S1), the 2DEG channel between G2S2 must remain present to guarantee current conduction. Since the devices are designed to be normally-off, the 2DEG under G2 are naturally depleted under V_{G2S2} = 0 V. In order to recover the 2DEG channel, V_{G2S2} was fixed at a positive voltage (V_{G2} remains constantly higher than V_{S2} during the voltage sweep) using the external circuit board and power supply described above.

Figure 3–4(a) shows the forward and reverse output characteristics with one gate swept between 0 and 5 V and the other gate fixed at 2 V higher than the neighboring source. Figure 3–4(b) shows the similar characteristics with the second gate fully turned on by a 5 V bias higher than the neighboring source. The forward (1st quadrant) and reverse (3rd quadrant) characteristics are nearly symmetric with a saturation current density up to 270 mA/mm at V_{G1S1}= V_{G2S2} = 5 V. The R_{on} is calculated to be 17.5 Ω·mm in the 1st quadrant and 16.8 Ω·mm in the 3rd quadrant. The $R_{on,sp}$ is calculated to be 5.6 mΩ·cm² and 5.4 mΩ·cm² using the total device length (29 μm) plus a 3 μm contact transfer length.

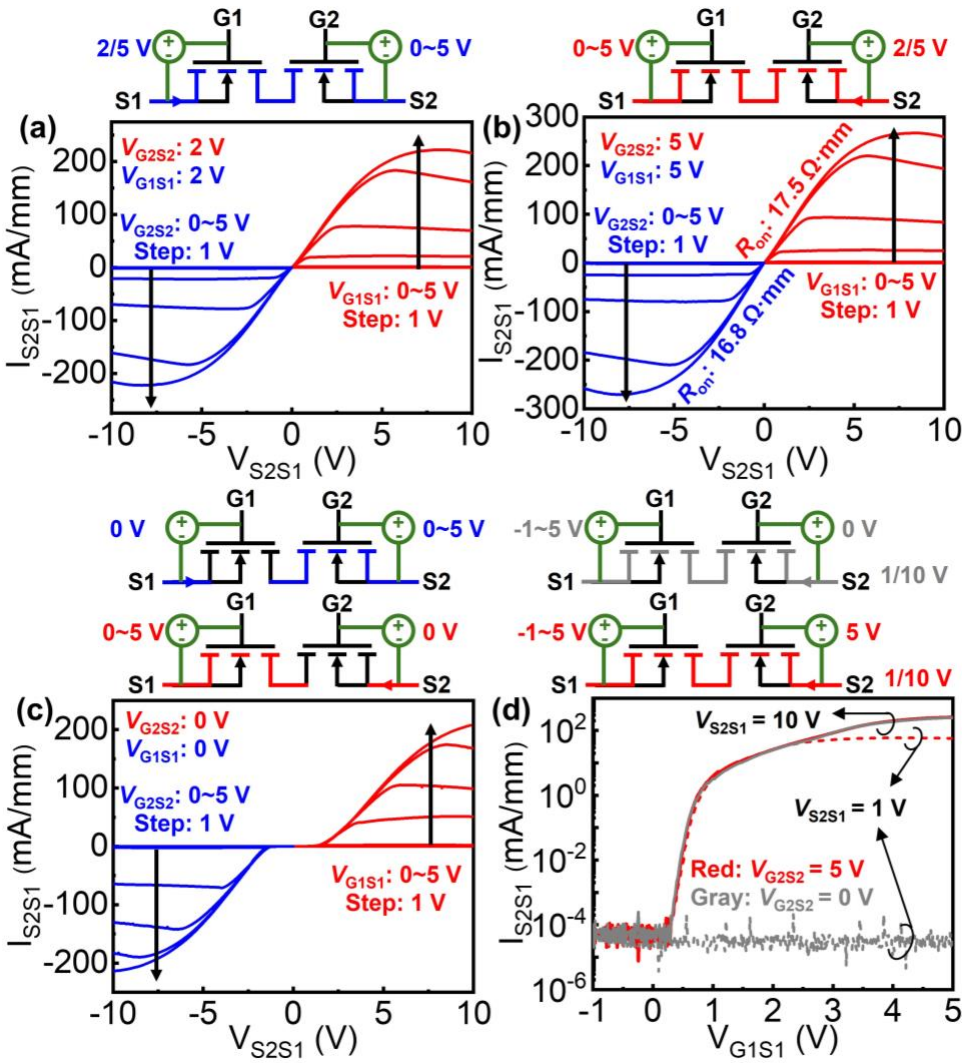

Figure 3–4 Bidirectional output characteristics at (a) V_{G2S2} or V_{G1S1} of 2 V and (b) V_{G2S2} or V_{G1S1} of 5 V (c) Bidirectional output characteristics in the diode mode with V_{G2S2} or V_{G1S1} of 0 V. (d) Transfer I_{S2S1}-V_{G1S1} characteristics at V_{G2S2} = 5 V (red).

An MBDS device can also work in the diode mode when one gate is on and the other gate is off. For an E-mode MBDS, a gate can be turned off by simply shorting it to the neighboring source, which can obviate a gate driver in applications [39]. Figure 3–4 (c) shows the bidirectional diode mode characteristics of the fabricated device with one gate swept from 0 to 5 V and the other gate shorted to the neighboring source. The symmetric characteristics reveal a turn-on voltage of ~1.6 V and a higher R_{on} of 28 Ω·mm.

Figure 3–4(d) shows the transfer characteristics in one direction, while the characteristics in the other direction is nearly identical. Here V_{G1S1} is swept from -1 to 5 V, while V_{G2S2} is fixed at 5 V (red) or 0 V (gray) and V_{S2S1} is fixed at 10 V (solid line) or 1 V (dash line). For V_{G2S2} = 0 V, current conduction is not present at V_{S2S1}= 1 V, as it is below the turn-on voltage of the diode mode. For V_{G2S2} = 5 V, G2 is on, allowing current conduction at V_{S2S1}= 1 V, corresponding to the transistor mode. At V_{S2S1}= 10 V and V_{G2S2}= 5 V, the device shows an on/off ratio of 5×10^6 and a threshold voltage of 0.6 V extracted at I_{S2S1}= 0.1 mA/mm.

3.3.2 Off-state IV

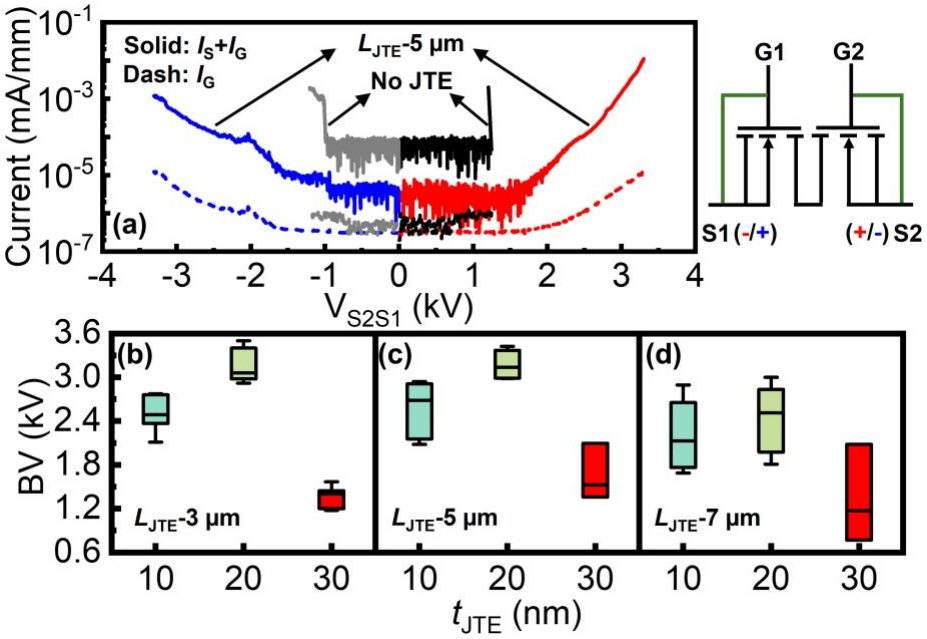

Figure 3–5 (a) Forward and reverse blocking characteristics with and without JTE at $V_{G2S2} = V_{G1S1} = 0$ V. Box plot of destructive *BV* for devices with different t_{JTE} of 10, 20, 30 nm and various L_{JTE} of (b) 3 µm (c) 5 µm, and (d) 7 µm.

Figure 3–5(a) shows the forward and reverse blocking characteristics of the devices with and without JTE. Here G1 is shorted to S1 and G2 shorted to S2. The device without JTE can block 1.2 kV, while the device with t_{JTE} = 20 nm and L_{JTE} = 5 µm can block 3.3 kV in both polarities, resulting in an average lateral *E*-field (E_{avg}) of over 1.73 MV/cm between G1 and G2. This is higher than the usual E_{ave} of ~1 MV/cm in field-plated GaN HEMT [40], showcasing the function of the JTE design. At 3.3 kV, the total leakage current is below 10^{-2} mA/mm with a gate leakage current below 10^{-5} mA/mm in both polarities.

Figure 3–5 (b)-(d) show the box plot of destructive *BV* measured on devices with varying t_{JTE} and L_{JTE}, with 9 devices measured for each type. The highest *BV* is ~3.5 kV. For each L_{JTE}, *BV* elevates when t_{JTE} increases from 10 to 20 nm and significantly drops at t_{JTE} = 30 nm. For devices with different L_{JTE}, the *BV* is generally comparable for L_{JTE}= 3 µm and 5 µm, with the latter being slightly higher, but significantly lower for L_{JTE}= 7 µm.

3.4 Simulation

The physics behind these *BV* results is unveiled by TCAD simulations. Polarization charges are considered along with a deep surface donor (0.9 eV above valence band, concentration 5×10^{13} cm^{-2}). These surface donor states are assumed to arise from the dry-etch induced nitrogen vacancies [41], [42]. Figure 3–6(a)-(c) show the *E*-field distribution in device with various t_{JTE} at a hypothetical blocking voltage of 3 kV. Two *E*-field peaks at the gate edge and JTE edge balances at t_{JTE} = 20 nm. The smaller or larger t_{JTE} induces a higher *E*-field peak at the gate edge or JTE edge, respectively. Fig. 4(d) shows the simulated *E*-field profile along a cutline near the AlGaN/GaN interface as L_{JTE} increases from 3 µm to 7 µm. With a fixed L_{G1G2} =19 µm, a L_{JTE} increase results in a decreased JTE-to-JTE spacing. For a L_{JTE} = 7 µm, the inter-JTE region is only 5 µm, and simulation shows high *E*-field in this region. This may induce the punch through, further leading to an increased leakage current and premature breakdown, which explains the lower *BV*.

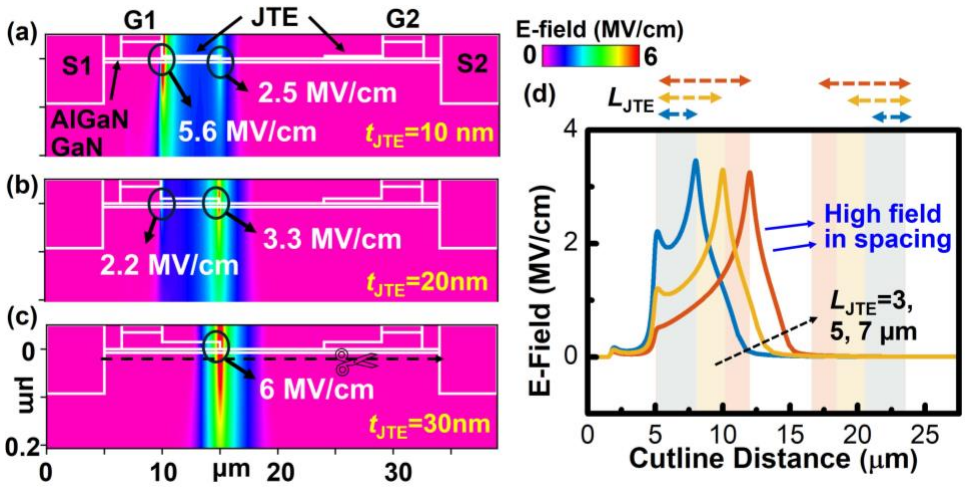

Figure 3–6 Simulated E-field contours under 3000 V blocking condition for t_{JTE} of (a) 10 nm, (b) 20 nm and (c) 30 nm at a fixed L_{JTE} of 5 μm. The peak E-field values are marked. (d) Simulated E-field profile along the cutline shown in (c) for L_{JTE} = 3, 5 and 7 μm with t_{JTE} fixed at 20 nm; the locations of three JTEs are marked in shadow with blue, yellow and orange colors, respectively

3.5 Benchmark

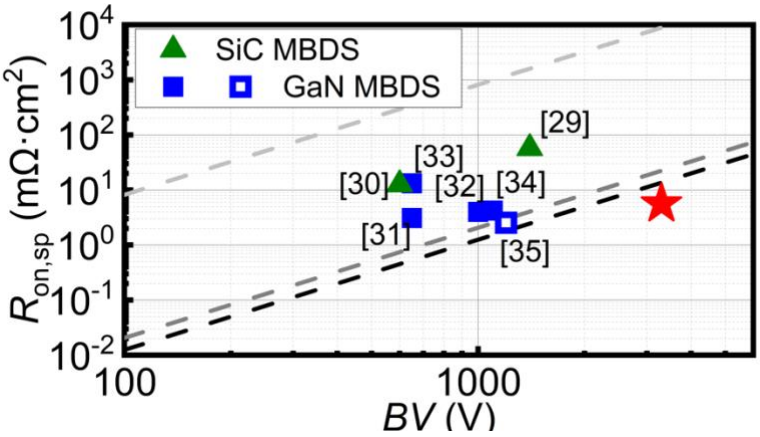

Figure 3–7 Benchmark of the BDS $R_{on,sp}$ *vs. BV* for the GaN MBDS in this work with other GaN and SiC MBDS devices reported in the literature. Dashed lines show the performance limit of BDS devices implemented using discrete Si, SiC and GaN devices. The E-mode/D-mode of each device is also marked.

Figure 3–7 benchmarks the $R_{on,sp}$ versus *BV* for our device and the state-of-the-art MBDSs based on SiC MOSFETs [29], [30]and GaN HEMTs [31], [32], [33], [34], [35]. As a comparison, the $R_{on,sp}$ limit of a BDS realized by two discrete devices is also estimated. For a target R_{on}, each discrete device is $R_{on}/2$, resulting in a 4× area. For GaN HEMT-based BDS, the limit of the BDS $R_{on,sp}$ is about 4× unidirectional limit, which can be written as $R_{on,sp} = 4BV^2R_{sh}/E_{avg}^2$ [43].

Such limit with R_{sh} = 300 Ω/sq and E_{avg} = 1 MV/cm is plotted in Fig. 5. For the Si/SiC-based BDS, due to the large forward voltage drop of the body diode, an additional Schottky barrier diode is often needed to parallel with each MOSFET to lower the 3rd-quad loss, resulting in an 8× area. This renders the BDS $R_{on,sp}$ limit of discrete SiC/Si devices to be ~8 times of the 1-D limit of the respective material, as also plotted in Figure 3–7. The performance of GaN MBDS demonstrated in this work surpasses the practical performance limits of BDS devices implemented by discrete GaN and SiC devices.

4 Chapter 4: Summary and future work

4.1 Summary

This thesis begins with an introduction of power semiconductor devices, focusing on the operation mechanism of semiconductor devices and highlighting the trade-off between on-resistance and breakdown voltage. It brings in some major participating materials including Si, SiC and GaN. GaN-based power devices are introduced in detail in terms of material properties and device structures, as well as their commercialization status. The last section of the first chapter proposes challenges and issues GaN transistors are facing.

In the second and third chapter, a novel p-GaN design is employed for unidirectional and bidirectional GaN-based transistors. With the extended p-GaN design, over 10-kV unidirectional HEMTs and over 3.3-kV monolithic bidirectional switches have been successfully demonstrated. The breakdown mechanisms of bidirectional switch are systematically investigated with physics-based TCAD simulation. Experimental measurements suggest the existence of intrinsic donor in epitaxial layer, balancing the acceptors in p-GaN region and enabling an uniform electric field between the gate and the drain, allowing for an average electric field of over 1.7 MV/cm. The results set a new record in BV and $R_{on,sp}$~BV trade-off in the high voltage GaN HEMT and GaN MBDS devices, suggesting good potential of GaN power devices for multi-kilovolt power electronics.

4.2 Future work

While this work has demonstrated significant progress in GaN-based unidirectional and bidirectional transistors, several research avenues remain open for future exploration to enhance device performances, improve yields and facilitate commercialization of high-voltage GaN power devices.

4.2.1 Large area device demonstration

The realization of large-area devices using the extended p-GaN structure is a critical next step, since large-area devices are essential for scaling current ratings to meet industrial demands. Commercial GaN HEMTs typically utilize interdigitated structures for efficient current handling, which has yet to be implemented with p-GaN RESURF and JTE structured transistors. The two-step etching masks and recipes proposed in this work provides a promising method to achieve precise and reliable fabrication for large-area devices. While the small-area devices demonstrated in this study achieved current ratings of up to 200 mA, further scaling to multi-ampere levels is essential to meet the requirements of industrial applications.

4.2.2 Application-oriented design

To enhance power density and reduce device size, the monolithic integration of GaN transistors with other circuit components on a single wafer is a promising avenue for future research. Designs such as on-wafer half-bridge configurations are particularly relevant for high-efficiency, high-frequency power conversion systems. Additionally, co-integration with gate drivers and passive components could streamline system design, minimize parasitics, and enable compact, high-performance power modules.

4.2.3 Reliability test

Comprehensive reliability studies are essential for understanding failure mechanisms and ensuring long-term device stability under diverse operating conditions. Future work should include high-temperature and ultra-low-temperature testing, as well as dynamic switching evaluations to assess degradation under practical conditions. Innovations in gate dielectric materials and

advanced passivation techniques should also be explored to mitigate degradation mechanisms, such as hot electron effects and surface states, thereby enhancing device robustness and extending operational lifetimes.

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