Optimization of the Process for Semiconductor Device Fabrication in the MicrON 636 Whittemore Cleanroom Facility

by

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(ABSTRACT)

The main objective of this work is to develop and optimize a process for the fabrication of basic semiconductor devices in silicon using the Modu-lab toolset in the MicrON 636 Whittemore cleanroom facility. This toolset is designed to work with four-inch silicon wafers, in a class 10000 cleanroom. Early work on this process produced functioning devices, with low yield and little to no process control. Three aspects of the process were therefore selected for optimization in this work.

The oxidation of the surface of the silicon wafers could not be made to follow models proposed by and accepted in the literature. By carefully changing the airflow in the oxidation furnace module, the uniformity of the oxide layer and the agreement of the growth with models increases to acceptable levels. Also, the effects of redistribution of dopant species due to growth of the oxide layer and the subsequent thermal processing are examined qualitatively.

Phosphorus diffusion in single-crystal silicon has a complex diffusion mechanism involving charged-vacancies, with concentration-dependent diffusion coefficients. It is therefore a complex mathematical problem to model the diffusion of phosphorus from a solid source within the crystal. An empirical model is proposed that accurately predicts the junction depth and sheet resistance of diffused phosphorus layers within the silicon wafer.

Throughout the course of the process it is necessary to monitor the characteristics of the wafers to assure proper conditions. A semiconductor parameter analyzer has been created for this purpose. Our system uses a Keithley model 2400 source meter, Signatone probe station and four-point probe stage, and a PC to measure DC I-V electrical characteristics of materials and devices. The measurements of sheet resistance, as well as device characterization of resistors, p-n junction diodes, and nMOSFETs provides feedback about the accuracy of processing steps, as well as a pedagogical tool for illustrating semiconductor device physics and operation.

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1 Introduction

1.1 Purpose

The purpose of this thesis is to develop and optimize a process to fabricate semiconductor devices in an undergraduate microelectronics facility. While neither a new process nor new theory can be gained from this work, its value lies in the fact that the process was designed around an existing set of low budget tools. To our knowledge, this project is the first of its type, a semiconductor fabrication process designed around the Modu-Lab toolset.

Virginia Polytechnic Institute and State University, under the auspices of the Virginia Microelectronics Consortium (VMEC), the Bradley Department of Electrical and Computer Engineering, and the Materials Science and Engineering Department, has developed an 1,800 ft^2 Class 10,000 cleanroom for teaching the elements of the microchip fabrication process to a multidisciplinary cohort of students from all areas of engineering, science, and even the humanities. The estimated throughput is approximately 500 students per year (about 170 students per semester). The development of our Class 10,000 cleanroom and the operation of our facility are described elsewhere.[1]

The process we have developed follows a manufacturing scheme to fabricate simple devices and simple testable circuits. We design our photolithography masks in AutoCad™ and print them on standard transparencies using a high-resolution Microdry™ printer. This simple mask design and generation procedure allows process flexibility at minimum cost—a complete maskset costs less than a dollar. Further, such simplicity will allow advanced students to design, fabricate, and test wafers using their own masksets. For our introductory class, the mask design includes resistors, p-n junctions, nMOS transistors, and simple circuits, as well as regions for device characterization and analysis. During the processing, students visually inspect and electrically test their wafers to insure the quality of processing. Students can test their wafers and devices using software written in LabView, which permits standard and custom tests. Typically, we measure the sheet resistance after each processing step and we measure I–V curves for each device. The characteristic variables of the processes such as diffusion and oxide growth rates correspond well with literature, thus allowing the students to compare and model their results.

Students taking this laboratory class learn the basics of a complete transistor manufacturing process and develop an appreciation for the processing equipment. This gives them a significant head start towards a career in semiconductor manufacturing or semiconductor related research. The organization and procedures of our process and laboratory have received very favorable comment from industrial representatives who have visited our facilities.

The process developed for this lab is tailored for a specific type of wafer. We use 4-inch (100 mm) diameter, 500 to 550 μm thick, p-type wafers with bulk resistivities between 14 and 22 Ω-cm that were donated to us by Motorola. All tools and times are specific for wafers with these characteristics.

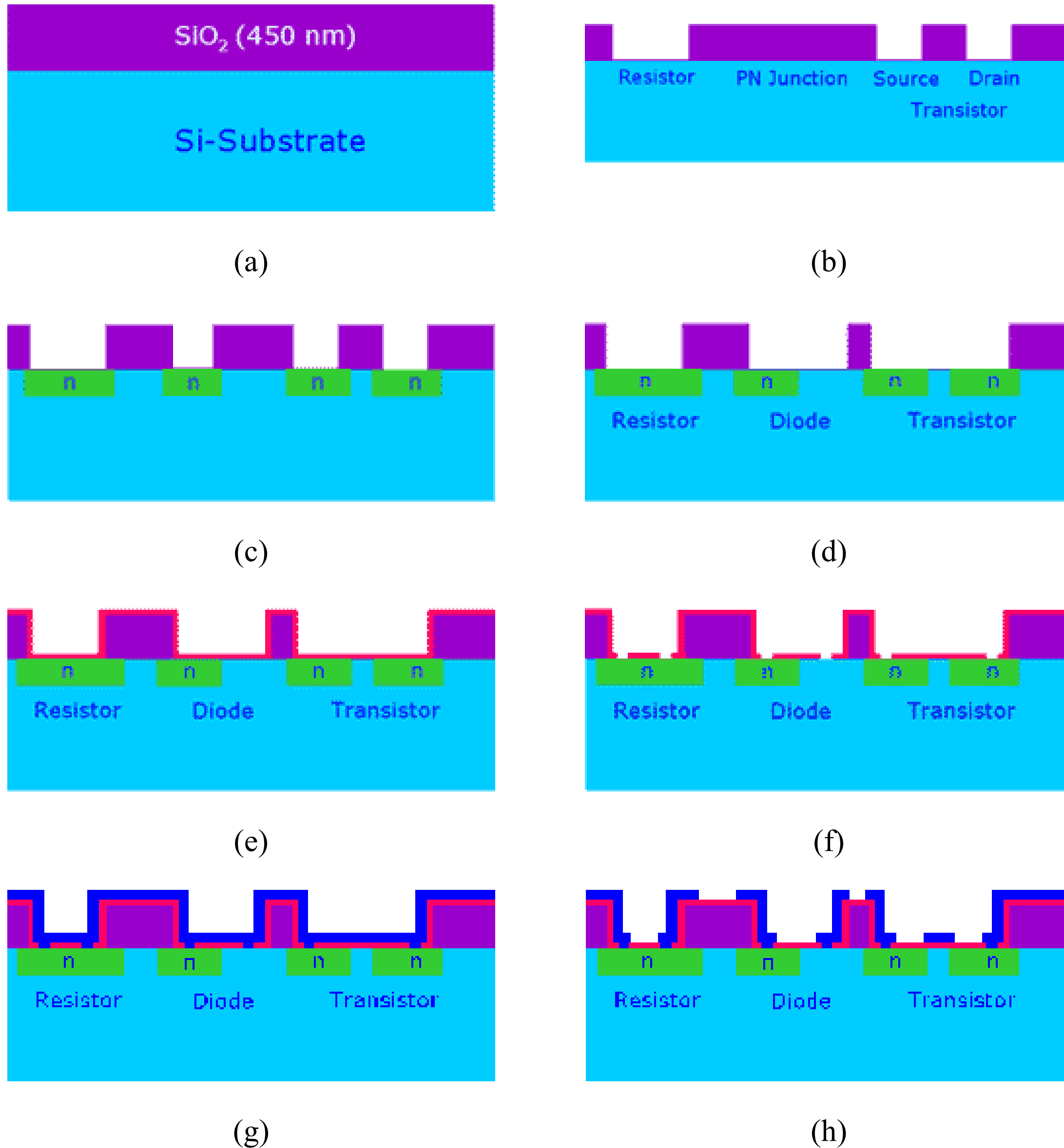


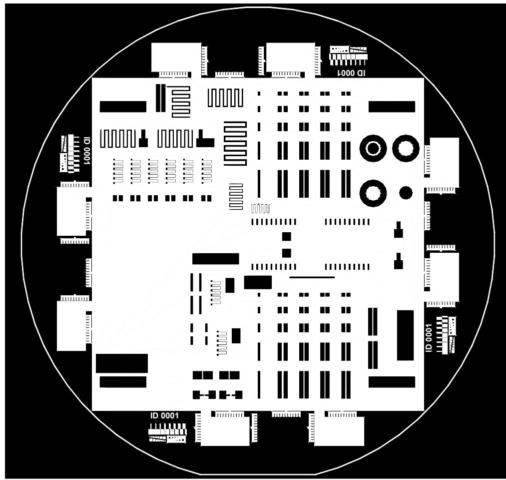
Figure 1.1 Cutaway illustrating each step of the process. (See text for details.)

Wafer fabrication follows a simple nine-step process outlined in the following paragraphs. All processing is carried out using the Modu-Lab series of tools as described elsewhere.[1, 2] Explicit experimental details are given in our laboratory manual.[3] Figure 1.1 displays the eight steps that involve changes to the surface of the wafer. First, the wafer is cleaned with acetone and HF to remove both organic and non-organic materials from the surface. After the wafer is cleaned, and before initial field oxide growth, the

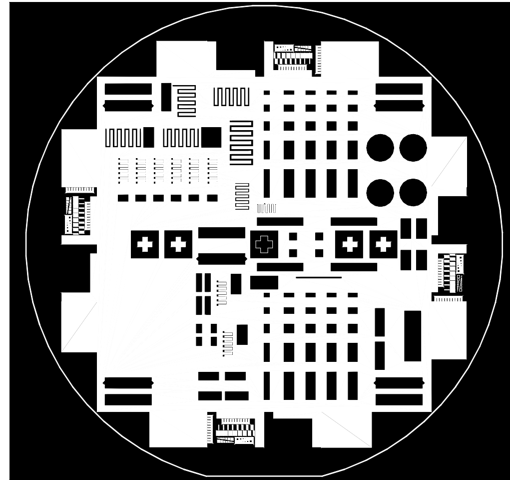
sheet resistance of the wafer is measured. This measurement is used both to familiarize the student with the device characterization module (DCM), and to provide comparative data for future measurements. Following cleaning and measurement, an oxide layer is grown on the wafer under wet conditions (see Figure 1.1(a)) in the oxidation furnace module (OFM). Oxygen entering the furnace is plumbed through a boiler system that heats the water to 98C. The wet oxide grows substantially faster than the dry oxide but is of a lower quality. However, because the only purpose of this layer is to act as a physical barrier against the phosphorus diffusion, it is acceptable. In order to completely block the phosphorus from diffusing through the oxide, the layer must be at least 530 nm thick[4]. Following oxide growth, the thickness is verified using a Filmetrics F20 interferometer.

After the initial field oxide layer has been grown, the first mask (Figure 1.2(a)) is transferred to the wafer at the photolithography module (PM) to allow for chemical patterning of the oxide layer. The oxide is then selectively etched to allow for phosphorus diffusion into the resistors, the n-side of the diodes, and the source and drain of the transistors, as shown in Figure 1.1(b). Using the n-type diffusion furnace module (DFM), the wafer is then doped by heating a solid-state source to 860^0C directly next to the wafer. This source is a ceramic oxide-base material with a gradient distribution of phosphorous pentoxide (P_2O_5) that has been designed to provide a constant effusion of P_2O_5 with time.[5] Wafers are mounted in pairs with the active surfaces facing the source. Up to six pairs of wafers can be doped simultaneously. This predepositon deposits a shallow n-type region with a very high P concentration on the wafer. The source is then removed, and the deposited phosphorus is diffused further into the wafer in the drive-in stage, which consists of baking the wafer at 1100^0C. Figure 1.1(c) shows the wafer with the n-wells diffused into the substrate. Our typical junction depths are 1.5 to 2.0 μm below the surface. The sheet resistance is again measured in a designed test area of the wafer both to verify proper diffusion and to allow for later calculations. Next the field oxide covering the channels of the transistors is removed and a shallow, high quality dry oxide is grown (see Figure 1.1(b) and Figure 1.1(e)) in regions defined by the level 2 mask (Figure 1.2(b)). This dry oxide acts as the capacitive gate for the enhancement MOSFETs. Gate oxides are grown in the OFM at 1000^0C in the same manner as field oxide, except that the oxygen entering the furnace is no longer put through the boiler system. As illustrated in Figure 1.1(f), the gate oxide is patterned using the level 3 mask (Figure 1.2(c)) to create contact holes through which the aluminum metallization can contact the silicon.

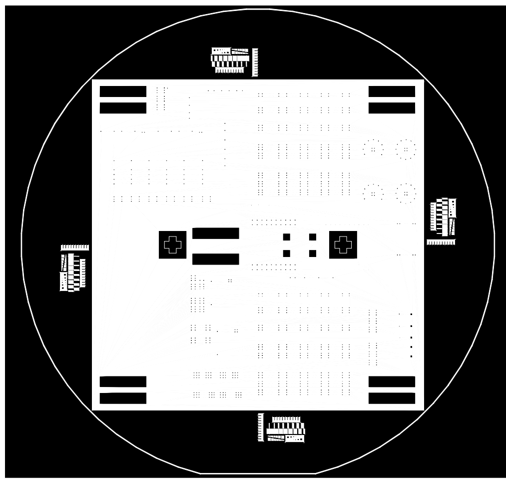
After oxidation and diffusion have been successfully completed and verified on the test module, the aluminum metallizaiton is applied. By means of the PVD metal evaporation system, a thin layer (approximately 200 nm) of aluminum is deposited over the entire surface of the wafer thus electrically connecting the individual devices. The final level 4 mask (Figure 1.2(d)) is then transferred to the wafer and the metal contact pads are isolated (Figure 1.1(h)) using the wet etch module (WEM). At this point, all processes have been completed and the wafer is ready to be tested at the device level as described in the next section.



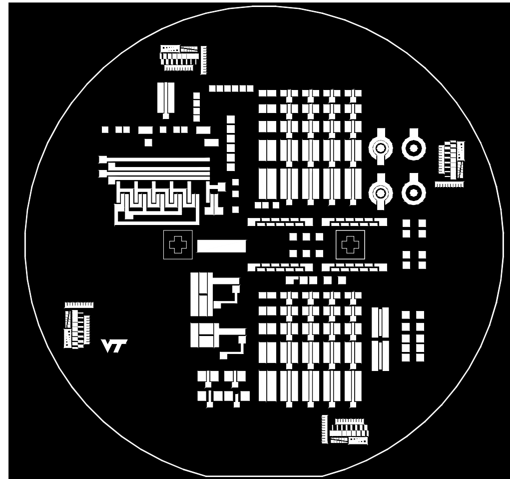
(a) Diffusion Mask



(b) Gate Oxide Etch Mask



(c) Contact Etch Mask



(d) Aluminum Etch Mask

Figure 1.2 Four-layer maskset for process described

The first iteration of the current process yielded poor results with little or no process control[6]. In that work, our objective was to demonstrate for the first time the concept of the Modu-Lab toolset was sound and that devices could indeed be created. The development of the process led to certain problems in understanding some of the critical issues in device fabrication. Later work done in the facility produced a much larger knowledge base on some of these issues such as metallization[7], oxidation[8], and diffusion[9]. Since the results of these experiments did not answer all of the questions raised by earlier work with the toolset, this thesis was proposed to resolve details of the more difficult processing steps in order to optimize the overall yield.

In the following chapters, the necessary developments for oxidation are described in Chapter 2, and for diffusion in Chapter 3, while Chapter 4 describes our development of a new, simplified semiconductor test system. Despite the efforts of previous work, and the work described here, there are several outstanding issues that require additional work before the process used in the Virginia Tech undergraduate process can be described as complete and fully optimized. These issues are described in Chapter 5.

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7 Senior Design Experiments
8 Senior Design Experiments
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2 Thermal Oxidation

2.1 Introduction

In order to create functioning devices in the silicon substrate, there are two important reasons to oxidize the surface of the silicon wafer. The first is to create a physical mask that acts as a barrier to the thermal diffusion of the dopant species. Since the rate of diffusion of the dopant, phosphorus in this case, is much slower in SiO_2 than in single-crystal silicon, a thick oxide layer allows for the creation of a situation in which it is dynamically impossible for the dopant to significantly penetrate the oxide and diffuse into the substrate. By patterning a thermally grown oxide layer through chemical etching, it is possible to allow the dopant to diffuse selectively into the crystal lattice, thereby changing its electrical properties. The second function of an oxide layer is to create a dielectric layer for use in MOS structures. Though there exist other materials that may be used as a dielectric, the virtue of an oxide layer is that it is simple to create. The only tools required are a source of oxygen and a supply of heat.

Our toolset allows for two methods of oxidation, dry oxidation and water-enhanced, or wet, oxidation. The underlying chemical reactions are

$$Si + O_2 \rightarrow SiO_2 \qquad (2.1)$$

And

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \qquad (2.2)$$

As will be shown, although both reactions follow the same general growth equation, the growth rates are substantially different with dry oxide (2.1) growing about one order of magnitude slower than wet oxide (2.2). Most importantly, the electrical properties are substantially different. Wet oxide is entirely adequate for use as a diffusion barrier or field oxide, while the dry oxide has acceptable properties for use as a gate dielectric. Thus, it is critical that for our process to be successful, we must be able to routinely create both wet and dry oxide. Economic considerations required that both be made in the same furnace system, thus resulting in important processing considerations. The two methods have different dynamic and static properties.

The kinetics of both wet and dry oxidation are described by one model[1];

$$X_0(t) = 0.5A[\{1 + \frac{4B}{A^2}(t+\tau)\}^{\frac{1}{2}} - 1] \qquad (2.3)$$

where $X_0(t)$ is the thickness of the oxide layer, t is the time of growth and B, A, and τ are defined by[1]

$$A = \frac{2D}{k_s} \quad (2.4)$$

$$B=2DN_0/M \quad (2.5)$$

$$\tau= X_i^2/B+ X_i /(B/A) \quad (2.6)$$

where D is the diffusion coefficient of oxygen in SiO_2, k_s is the rate constant for the reaction at the Si-SiO_2 interface, N_0 is the concentration of oxidizing species at the oxide surface, M is the number of molecules of the oxidizing species that are incorporated into a unit volume of the resulting oxide, and X_i is the thickness of the initial oxide on the surface of the silicon (~10 to 20 Å).

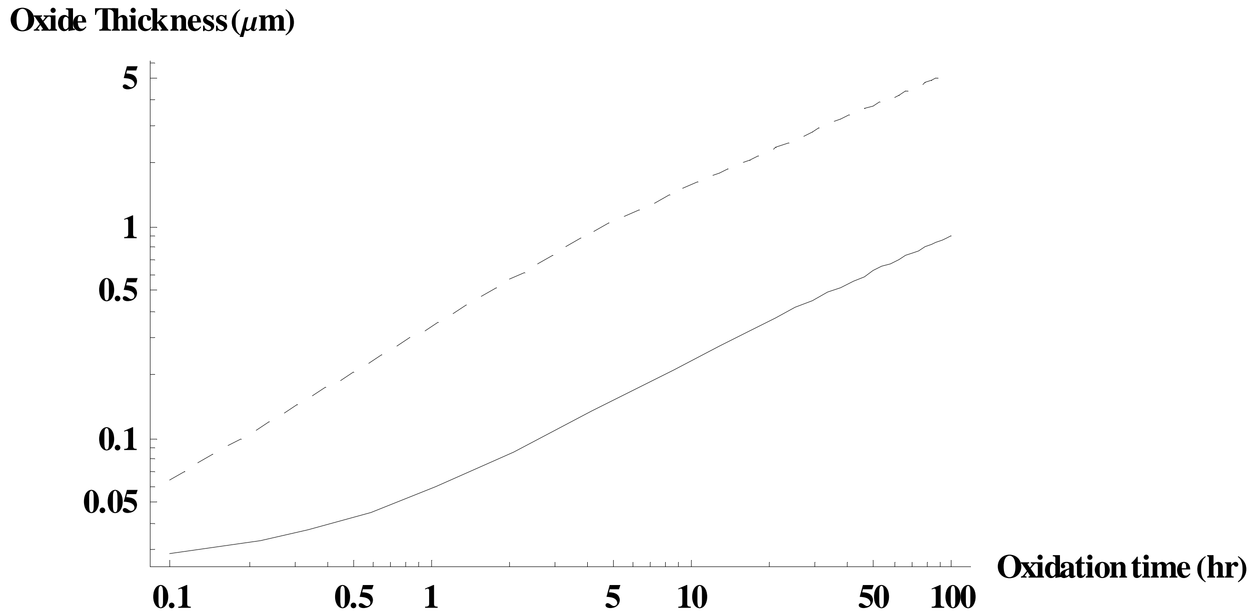

Figure 2.1 Thickness versus time plot for wet and dry oxidation on a (100) single crystal silicon substrate at 1000°C. The dashed line corresponds to water enhanced growth and the solid to dry O_2 growth.

Figure 2.1 shows plots for the thickness of the oxide versus time for each of these methods, at T=1000°C, as predicted from data in Jaeger[1]. It is obvious from this plot that the steam-enhanced method of growth yields a growth rate that is nearly an order of magnitude faster than the simple dry oxidation process.

The uniformity of both the physical masking layer (field oxide) and the dielectric layer (gate oxide) is of great importance in achieving wafers with devices that function similarly across the diameter of the wafer. There are three key effects of oxide nonuniformity that can negatively affect the behavior of devices fabricated on the wafer.

The layer of field oxide that is used as a mask against thermal diffusion must be quite uniform, and in order for the layer to properly mask the surface against later diffusion steps must exceed some minimum thickness through which the diffusant will not have sufficient time to penetrate (see Figure 2.2).

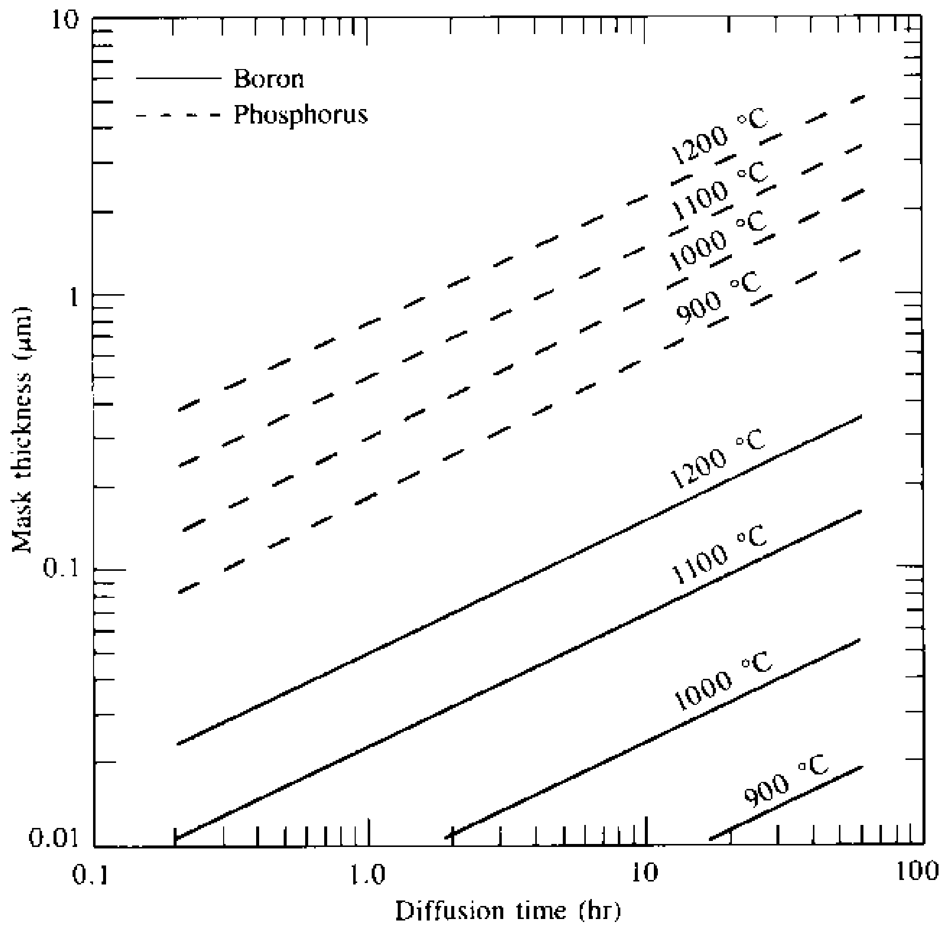

Figure 2.2 Masking Properties of SiO2

The second detrimental affect of a non-uniform oxide layer comes into play in the dielectric layer, or gate oxide. As shall be described in the characterization section of this paper (Chapter 4), the drain current through a MOS structure is inversely proportional to the thickness of the gate oxide. A non-uniform gate oxide layer would therefore result in MOSFET structures that behave quite differently one from the other. By ensuring a consistent thickness in the gate oxide across the wafer, one can eliminate this variable when optimizing other processes, such as thermal diffusion.

That last and most subtle effect of a non-uniform oxide layer is the redistribution of the dopant species near the Si-SiO_2 interface. As the oxidation layer is grown, the impurities near the interface may be incorporated into the oxide layer. A distribution or segregation coefficient, m, is defined by[2]

$$m = \frac{\text{equilibrium concentration of impurity in Silicon}}{\text{impurity concentration in oxide}} \quad (2.7)$$

For boron, m = 0.3, while for phosphorus m = 10. Both elements have low diffusion coefficients in SiO_2.

A value of m greater than 1, with a low diffusion coefficient in SiO_2, results in a rejection of the impurity by the oxide, and a resulting build-up near the surface. An m value less than one, with a low diffusion coefficient in the SiO_2 layer, results in a depletion of the impurity from the surface of the silicon. For this reason, boron tends to be depleted from the silicon surface, while phosphorus builds up. Since the concentration of the dopant affects the electrical properties of the silicon to such a high extent, a small variation in uniformity of the oxide layer will result in dramatic changes in the electrical behavior of devices. The initial oxidation process (field oxide growth) will deplete the boron concentration near the surface. The gate oxidation will increase the phosphorus concentration near the surface, while simultaneously depleting the boron concentration even further. Again, in order for the devices on the wafer to function with some uniformity, the thickness of the oxide must be uniform both across the wafer (to ensure constancy of operation on each wafer) and along the length of the wafer boat (to ensure constancy throughout a group of wafers).

Modeling the redistribution of the boron near the surface is a complex mathematical problem. Although the diffusion of boron in single-crystal silicon is well understood[1], the conditions in the case of oxidation-redistribution are quite difficult to model and to understand. First, the Si-SiO_2 interface is not at a fixed position during the oxidation process. It is well agreed that the oxide layer grows approximately 46% into the substrate, and 54% above the surface[1]. This results in a moving boundary, and one that moves with a non-constant speed, as the growth rate of the oxide layer is not constant with speed (see Figure 2.1). Second, the boron that exists in the wafer will be constantly diffusing down the concentration gradient, changing the flux of boron that can arrive at the Si-SiO_2 interface[2]. Furthermore, during furnace ramp up and ramp down times, the oxide layer does not continue to grow, due to a nitrogen ambient. During the ramp times however, the boron is thermally excited in the crystal lattice, and will redistribute itself along its chemical potential slope. The effects of this dopant redistribution on the behavior of the devices will be discussed again in Chapter 4.

2.2 Apparatus

The oxidation furnace module (OFM) is a PID-controlled, three-zone horizontal quartz tube furnace designed to accommodate 4-in wafers in quartz wafer boats. It has a maximum operating temperature of 1050°C at which temperature it consumes approximately 8 kW. It has an associated gas supply system with two flow meters -- one for high-purity oxygen and one for high-purity nitrogen. Both flow meters are calibrated for 20 psi pressure. Our gas manifold is therefore set to this pressure. We have plumbed the system so that the furnace can be purged with nitrogen while the unit is heating to operating temperature, and then can flow either dry or wet oxygen under controlled conditions. A photograph of the setup used to generate the wet oxygen is shown in Figure 2.3. In this setup, wet oxygen is generated by flowing high-purity oxygen through hot (98°C) DI water.

Figure 2.3 Photo of wet-oxygen generation system

2.3 Oxide Uniformity Procedure

2.3.1 Dry Process

To begin the experiment to test the uniformity of the oxide layer grown under dry conditions, twenty-five wafers were cleaned for two minutes in a 10% buffered oxide etch solution to remove any native oxide or passivation layers. The etching solution is JT Baker B5636. The solution contains both HF and NH_4F, which acts as a buffering agent. Next, the wafers were cleaned with electronic grade acetone and isopropyl alcohol to remove any surface contaminants, such as metals or organics.

In an attempt to assure turbulent gas flow in the furnace, and thus increase the uniformity of the temperature of the gas across the surface of the wafer, two wafer boats were inserted into the tube as baffles[1]. Each baffle wafer boat contained two wafers, one in the first position, and one in the last position. One boat was placed in front of the test wafers, and the other placed behind them, as shown in Figure 2.4

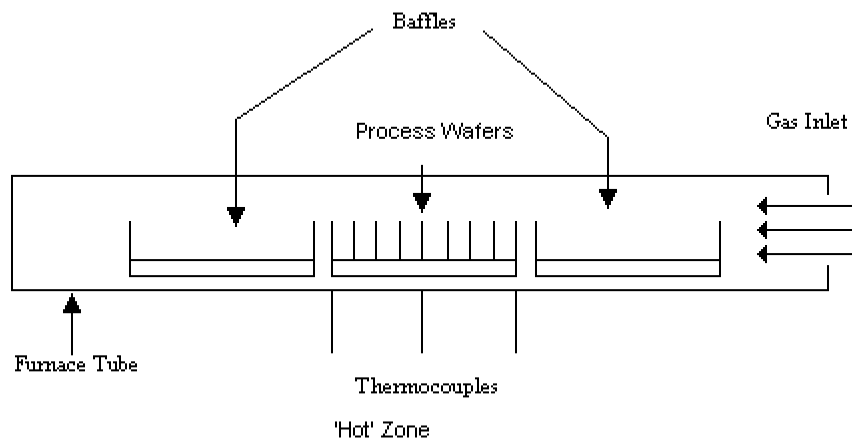

Figure 2.4 Schematic of test wafers and baffle boats inside the quartz furnace tube.

During oxidation, the wafers were loaded into quartz carriers and placed in a furnace at 600°C. The furnace was ramped to 1000°°C under 2 lpm of N_2. As the flowrate is relatively low, the tube is actually only slightly above atmospheric pressure. When the furnace achieved the desired oxidation temperature, the Nitrogen was turned off, and 6 lpm of dry O_2 was flowed into the furnace. The wafers were held at 1000C for 1 hour,

[1] The first iteration of this process did not include baffles[3], and the uniformity of the oxide layers grown was greatly reduced.

then ramped down to 600°C under nitrogen gas. At 600°C, the wafers and carriers were removed from the furnace for characterization. Figure 2.5 shows the thermal cycle of the process with ramp up, hold time, and ramp down.

After the wafers had cooled to room temperature, the thickness was mapped across each wafer, and the results compared between the wafers in the test boat and the baffle boats.

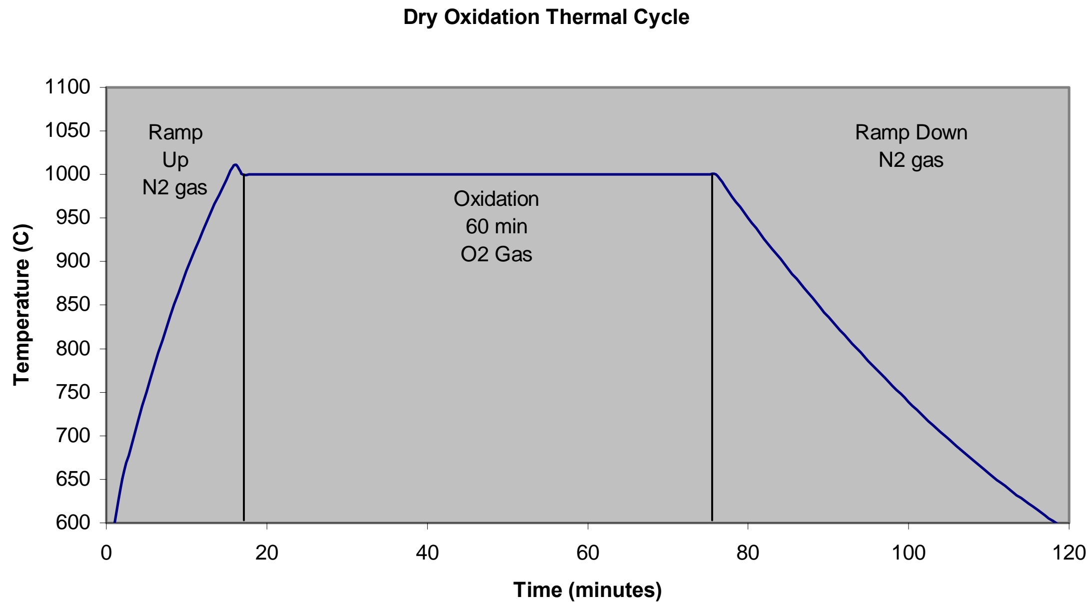

Figure 2.5 Dry Oxidation Thermal Cycle

2.3.2 Wet Oxidation

The process for the wet oxidation is similar to that of the dry oxidation with one key difference. During the wet oxidation, the oxygen gas that is flowed into the system is passed through a bubbler system (see Figure 2.3). The bubbler consists of a flask containing deionized water at 96°C. This bubbler system acts to hydrate the oxygen, and thus dramatically increases the growth rate of the oxide, while simultaneously decreasing the quality of the oxide.

2.4 Oxide Uniformity Results

2.4.1 Wet Oxidation

The conditions for wet oxidation necessitate a good understanding of the flow of the fluid in the furnace tube. Since the water vapor enters the system at 96-100°C and the atmosphere directly surrounding the wafers is at 1000°C, it is crucial that the fluid mixture of water vapor and oxygen be fully mixed. Figure 2.6 shows a typical wafer map measured for a wafer processed for 2.5 hours under wet conditions with no baffles.

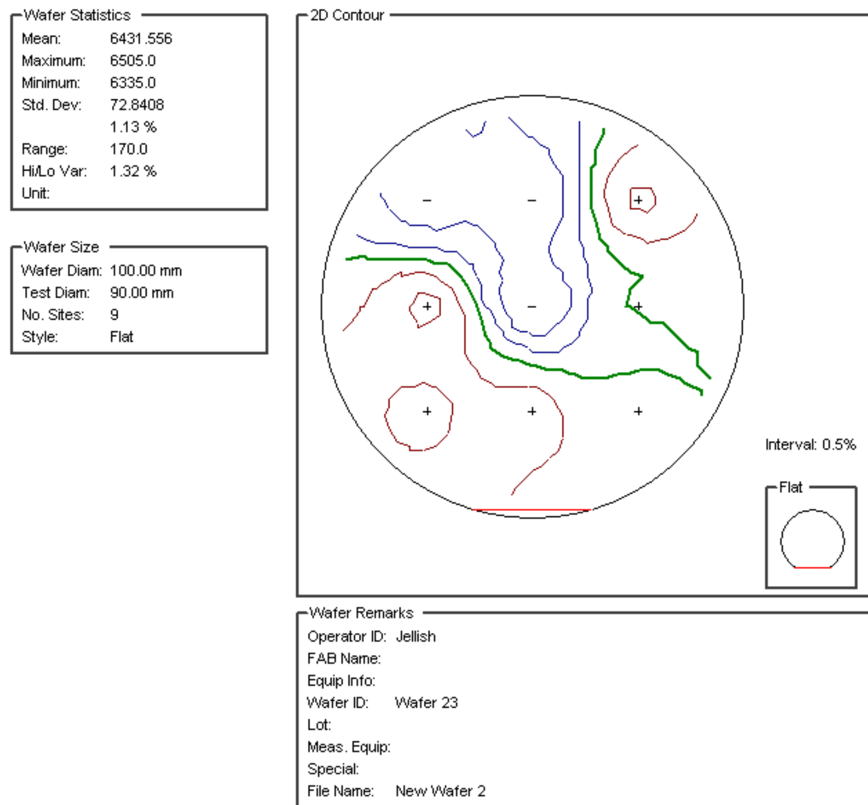

Figure 2.6 Oxide thickness map for a wafer processed with no baffling. Note the standard deviation is 1.13%, and isocontour lines are 0.5% apart. The mean value of the thickness in this sample is 643.2 nm.

The model for wet oxidation (2.3) predicts a thickness of 698.6 nm, which is 8% higher than the mean shown in Figure 2.6 above. We also note from the figure that the standard error of the mean of 9 points is 1.1%. When the baffles are introduced into the system, and the wafer is processed under otherwise identical conditions, the film thickness is increased to 672 nm (only 2.8% less than predicted) while the uniformity is improved to a standard deviation of 0.5%, as shown in Figure 2.7.

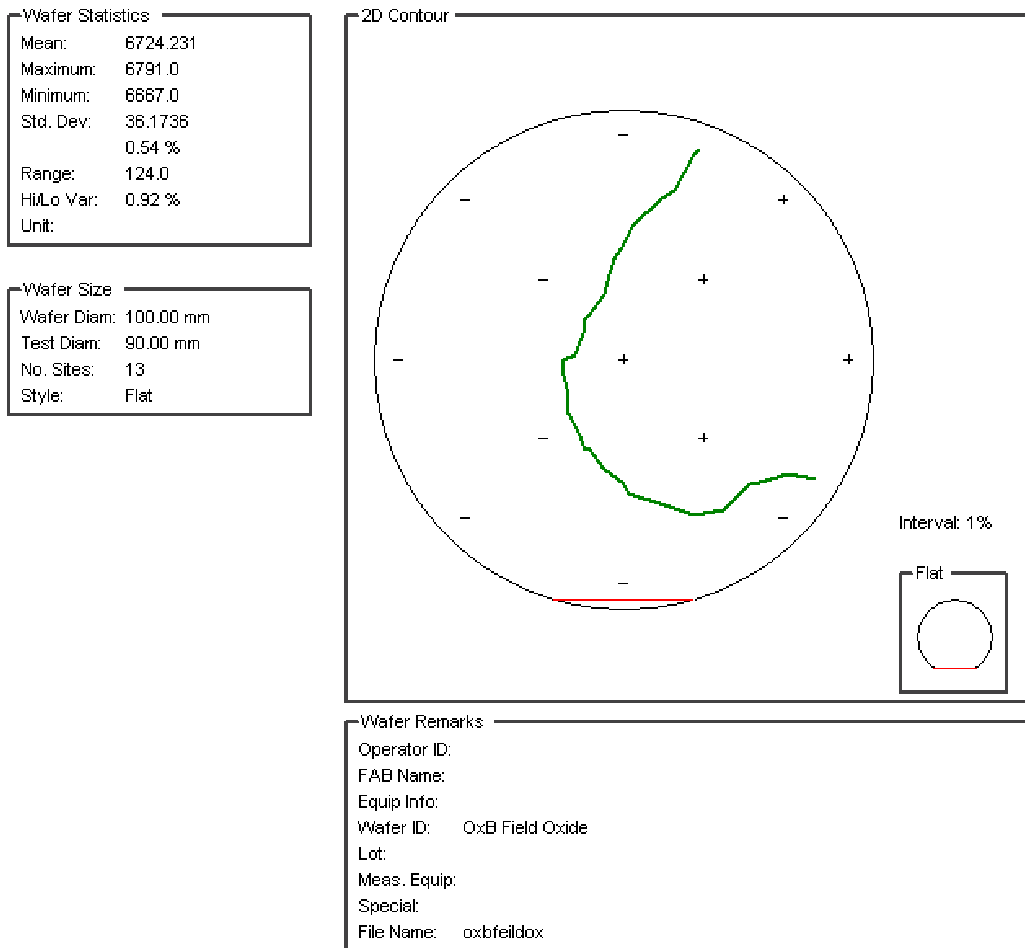

Figure 2.7 Thickness map for a wafer processed with baffles. The mean value is 679.1nm, with a standard deviation of only 0.54%. Note the isocontour lines are in 1% increments.

It is important to note that an additional 4 data points (13 points in all) were measured on this wafer. These additional points are near the outer edges of the wafer as can be seen by comparing Figure 2.6 and Figure 2.7. It would be expected that these outer points would show more variation from the mean than the more central original 9 points. The standard deviation for the central points of Figure 2.7 is 0.3%, a value almost 4 times better than that obtained without baffles.

The results of this study conclusively show that baffles must be used in order to produce the most uniform oxide layers. The resulting oxide layers produced in this manner are entirely satisfactory for our process.

2.4.2 Dry Oxidation

When baffles are used to aid in the creation of turbulence in the atmosphere around the wafers, wet oxidized wafers exhibit very uniform oxide thickness. In the wet oxide test, we did not determine the uniformity of the oxide thickness as a function of position in the wafer boat as small variations from wafer to wafer will have little effect on the process. However, if we are to expect uniform electrical properties from wafer to wafer, it is important that the gate dielectric (gate oxide) not only be uniform across the wafer (device to device variation) but that it also be uniform from wafer to wafer. Figure 2.8 shows a wafer map from the first wafer[2] in lot marked 'process wafers' in Figure 2.4.

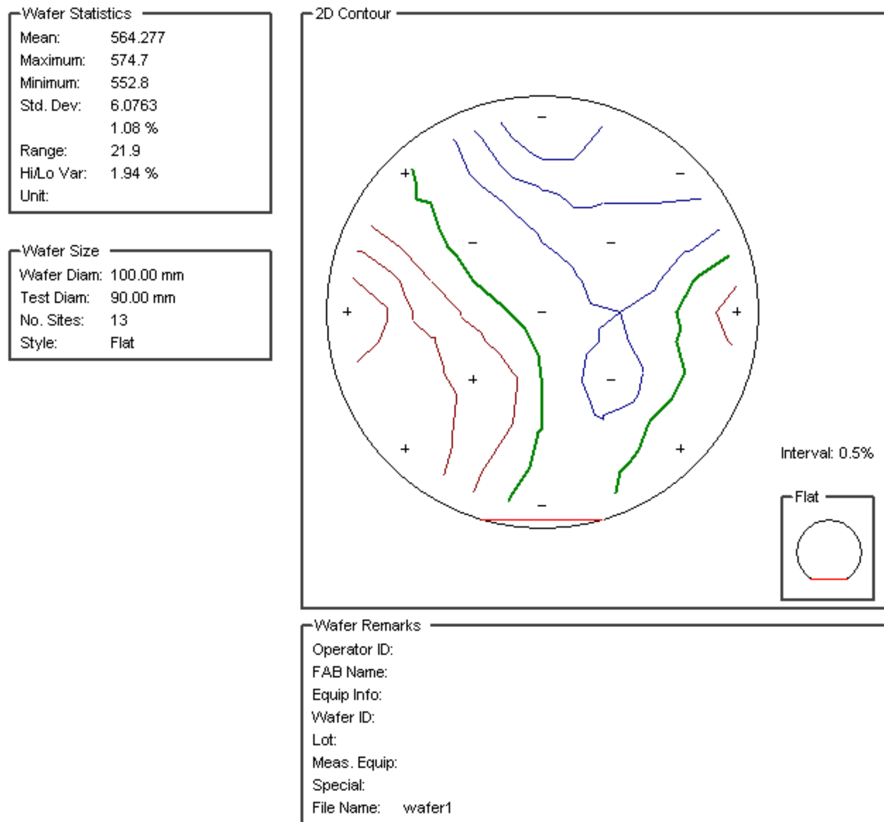

Figure 2.8 Oxide thickness map of wafer 1 processed under dry conditions. The high to low variation of the thickness across the wafer is only 2%. The wafer exhibits an area with a slightly thinner region in the upper right side.

[2] The wafers are numbered 1-n where the first wafer is nearest the oxygen inlet and the nth wafer is furthest from the inlet

Since this wafer has a total high to low variation of only 2% across the entire surface, it can be assumed that the local effects of a variation in gate oxide thickness are quite acceptable for our process. That is to say, the thickness of the gate oxide in each MOS structure can be assumed to be uniform. Also, this implies that MOS structures developed at different locations across the wafer should not see much variation in performance due to different gate thickness.

As the wafers are normally processed in batches, it is important as well that the average thickness from one wafer to the next in the same run be similar. Figure 2.9 shows the average thickness of the oxide on each wafer as a function of wafer position in the wafer boat. The standard deviation of the means of the process wafer set is 0.6%, a value small compared to the 2% standard deviation across the wafer, meaning that all locations come from the same statistical sample. This signifies an unimportant difference between each wafer in the boat. It can therefore be safely assumed that the devices from one wafer to the next will see no important change in electrical behavior due to oxide non-uniformities.

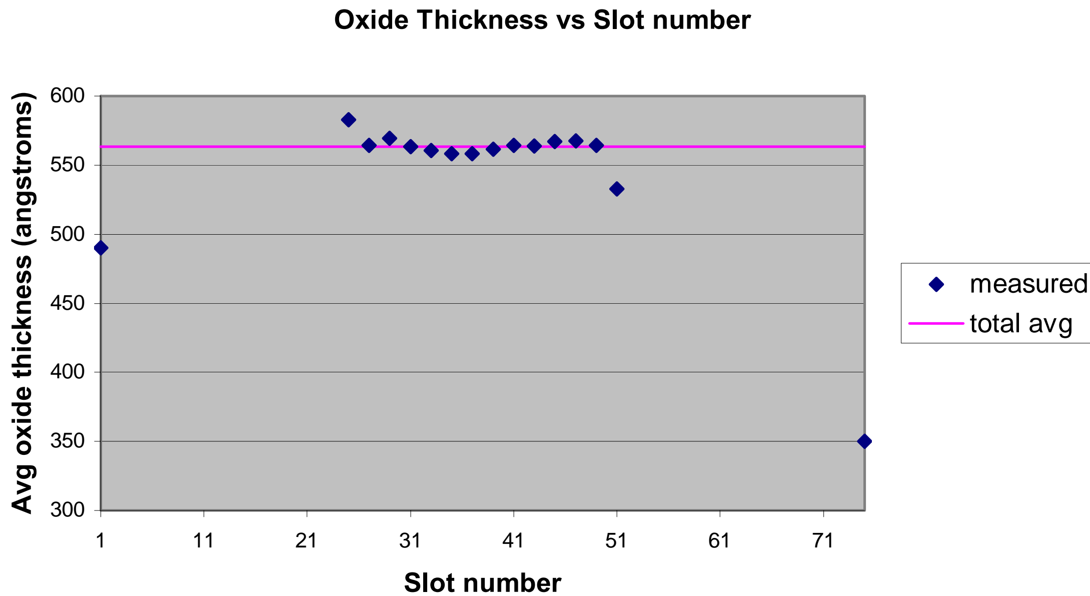

Figure 2.9 Average oxide thickness vs position for test wafers. The standard deviation between the averages is 0.6%.

Though the plot above shows that the wafers have nearly constant average thickness regardless of location in the furnace, a plot of the standard deviations of the thickness with respect to position in the wafer boat shows that the uniformity of the thickness is almost doubled as the wafer is removed in proximity from the gas supply as shown in Figure 2.9. Figure 2.10 shows this trend as experienced in this experiment, a fact that can be seen by the change in standard deviation along the length of the boat.

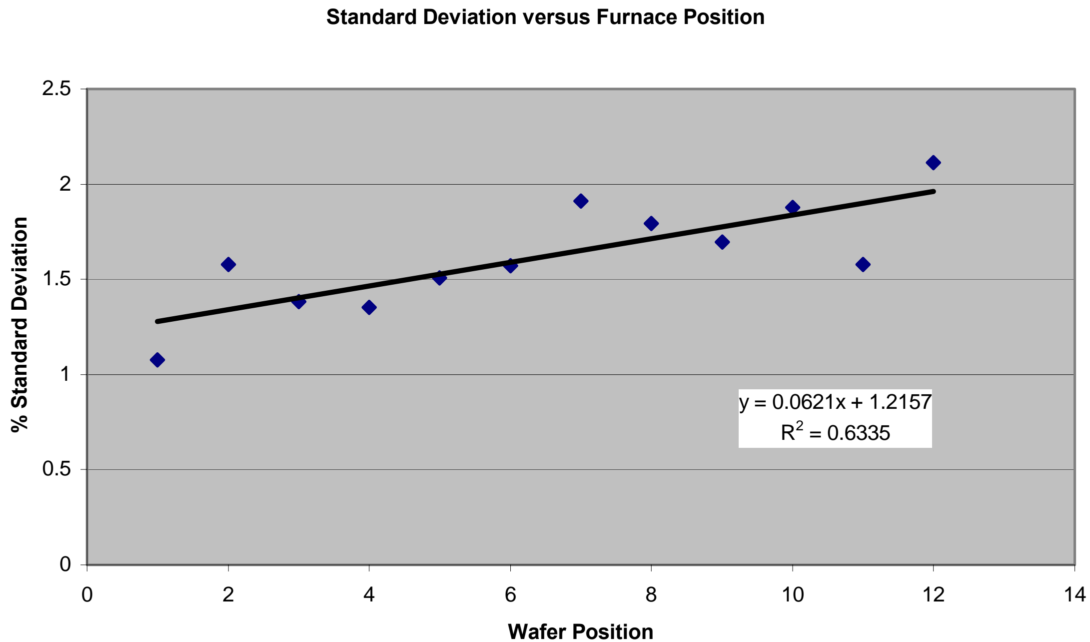

Figure 2.10 Percent standard deviation versus furnace position for wafers processed under dry oxidation conditions.

It is interesting to note the tendency for the oxide to be thinner in the same location on most of the wafers. Figure 2.11 shows a map of the point-by-point average of all of the wafers (25 total) in this process run. From this graph, it can be noted that the upper right portion of the wafers tends to have a thinner oxide layer than the rest of the wafer. The reason for this is still not completely understood, but is assumed to be a problem of gas flow and inadequate wafer baffling.

The average thickness of the oxide grown in this experiment (mean of the means) is 563.6 Å. When the proper temperature and initial conditions are substituted into Equation (2.3), and solved for the thickness, the model predicts a value of 578.4 Å. Thus, the measured data is 2.6% lower than the calculated value. It can therefore be stated that the dry oxide thickness can be very accurately predicted for this toolset. We note that the value predicted here for dry oxidation is slightly higher than the observed value by approximately the same amount as for the wet oxidation.

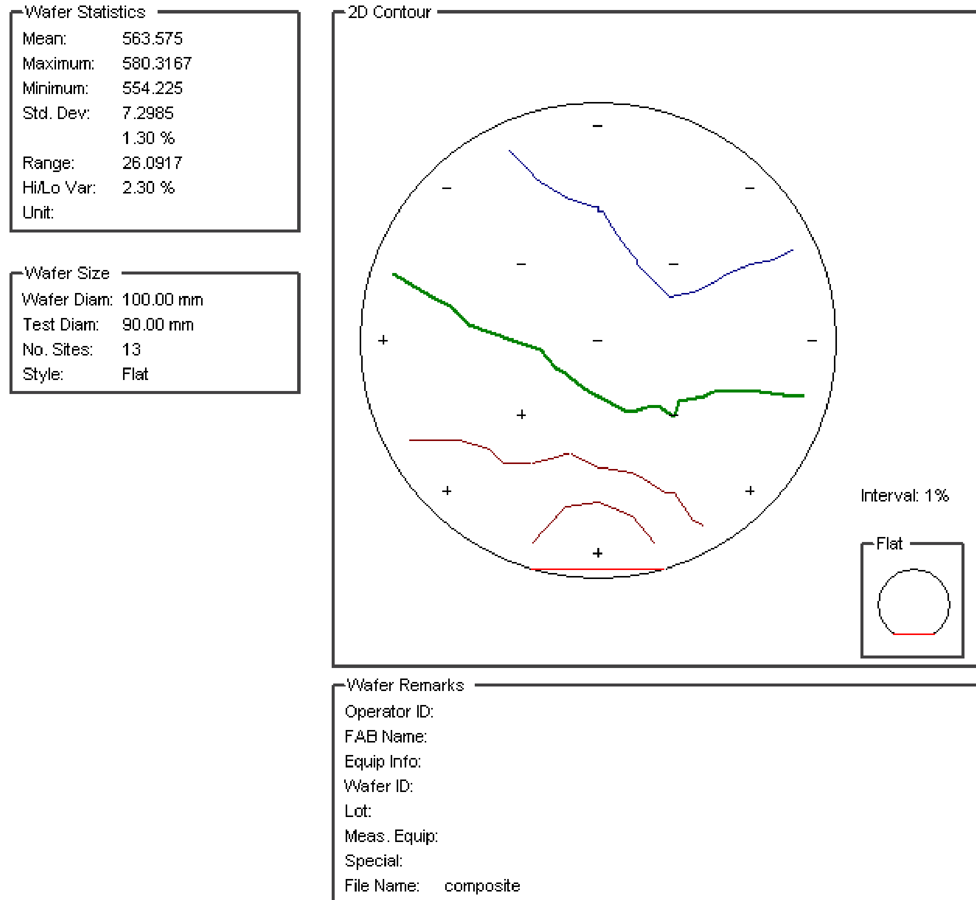

Figure 2.11 Point by point average wafer map of oxide thickness.

2.5 Dopant Redistribution Process

In order to gain a qualitative understanding of the redistribution of the dopants throughout the process, a different experiment needed to be performed. Since the toolset provided has no means of profiling the concentration of the dopants in the wafer, electrical testing was done to measure the sheet resistance of the wafer at certain points in the process. The sheet resistance of the wafer will be strongly affected by a redistribution in dopants near the surface (see Chapter 4 for a further discussion on sheet resistance). Since the current process necessitates both p- and n-type semiconductor materials, two wafers were processed in parallel to examine the redistribution of each of the dopants throughout the entire thermal cycle. Wafer OxA was processed to examine the redistribution of phosphorus, and Wafer OxB that of boron.

2.5.1 Wafer OxA process

The process currently used to create devices includes the following thermal steps: field oxidation; predeposition of dopant; drive-in of that dopant; and gate oxidation. Figure 2.12 shows the entire thermal budget for the process, as well as the points at which the sheet resistance was measured to examine either the effects of oxide growth, thermal cycling, or both.

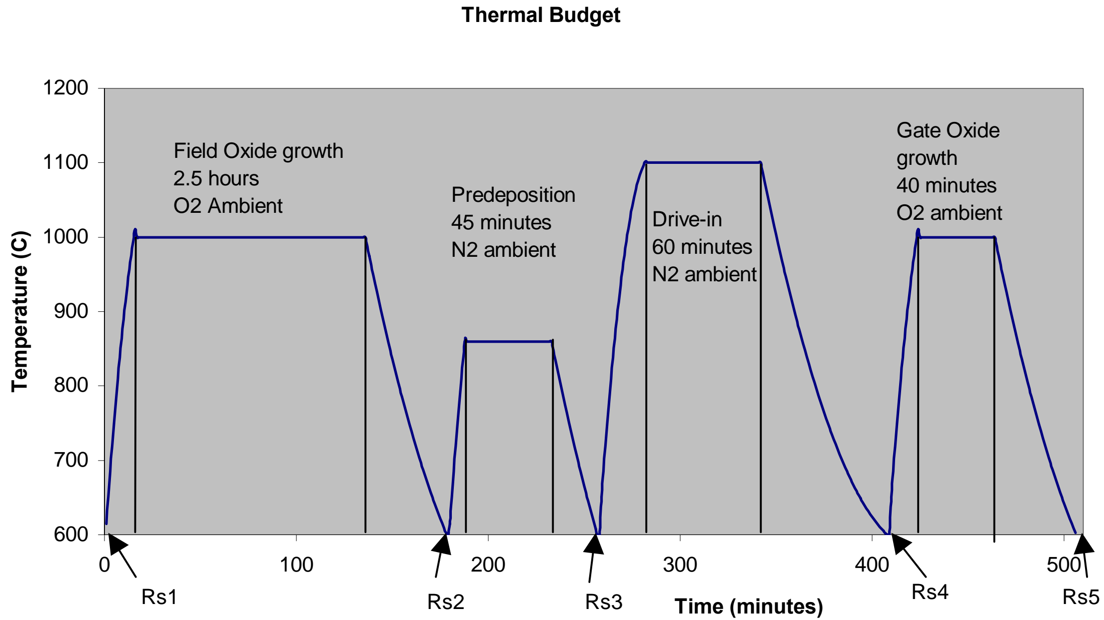

Figure 2.12 Total Thermal Budget of current process with sheet resistance measurement points indicated.

The process is as follows. Before any thermal processing, the wafer is cleaned in an HF etch and the sheet resistance is mapped to log the as-received characteristics of the wafer, Rs_1. The wafer is oxidized at 1000°C under wet O_2 conditions for 150 minutes. After this process, the oxide layer is stripped with an HF etch, and the sheet resistance, Rs_2, is mapped across the entire surface of the wafer. Next, the wafer is thermally cycled to 860°C under N_2 for 45 minutes in direct proximity to a solid source of phosphorus (phosphorosilica glass), and the sheet resistance, Rs_3, is mapped. The predeposition is followed by a 60 minute drive-in at 1100°C under N_2 and another sheet resistance map, Rs_4. Finally, a high quality gate oxide layer is grown on the surface of the silicon at 1000°C under dry O_2 conditions. This oxide is again stripped, and the wafer surface mapped again, Rs_5.

2.5.2 Wafer OxB process

Wafer OxB is processed similarly to Wafer OxA but with a different intent. Wafer OxB was cycled to examine the redistribution of boron, as opposed to phosphorus. The wafer is therefore not doped with phosphorus, but is only thermally cycled as though it were in the regular process flow. Therefore, there are only three sheet resistance measurements performed on wafer OxB. Table 2.1. Points of electrical characterization for determination of dopant redistribution lists the different points in the process flow at which the sheet resistance is measured for each wafer.

Table 2.1. Points of electrical characterization for determination of dopant redistribution

Measurement Designator	Point of Process	Test performed on wafer OxA	Test Performed on wafer OxB
Rs_1	As-received wafer	Yes	Yes
Rs_2	After Field oxidation	Yes	No
Rs_3	After predep	Yes	No
Rs_4	After drive-in	Yes	Yes
Rs_5	After gate oxide	Yes	Yes

By performing this set of experiments it is possible to examine the electrical properties of the substrate at certain key points in the process. More importantly, the final sheet resistance of both the n- and p-type silicon is known at the end of the experiment.

2.5.3 Wafer Characterization

The thickness of the oxide layer grown in either of the methods mentioned above is characterized using a Filmetrics model F20. The basic method of operation is to measure the intensity of light reflected back from the sample at various different wavelengths of light. A model is then made based on the index of refraction of the SiO_2 to determine the thickness of the oxide. A copy of the complete user manual and theory of operation can be found on the Filmetrics web page[4]. The thickness is usually measured at 13 points in a circular pattern, as shown in Figure 2.13. This mapping is done for each of the test wafers, as well as the four baffle wafers. Results are plotted in WaferMap 2.1, a commercially available software program that also computes the mean, maximum value, minimum value, standard deviation, the range and the high to low variation.

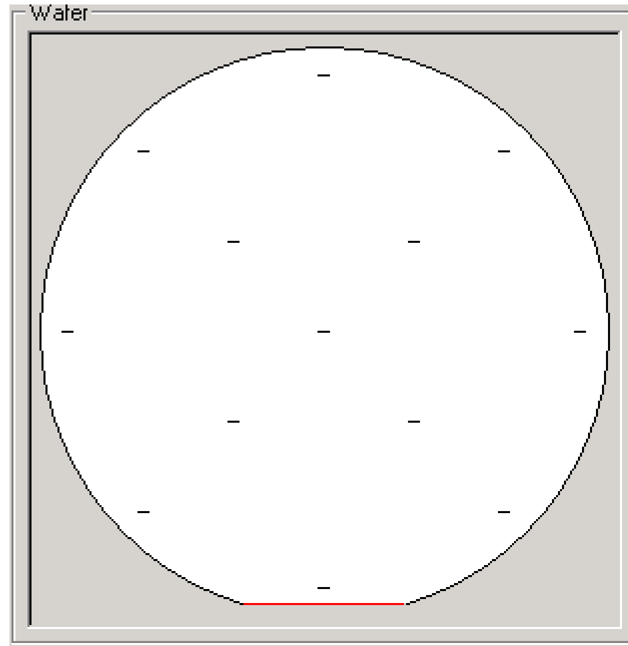

Figure 2.13 Layout of points used to map the oxide grown on the surface of the wafer during experiments.

To examine the redistribution of the dopants near the surface of the SiO_2 interface, the average concentration is measured via a four-point probe sheet resistance measurement. The theory of this characterization technique is described in Chapter 4 of this work. The sheet resistance of each wafer is mapped in the same locations as the oxide thickness map (see Figure 2.13).

2.6 Dopant Redistribution Results

The results of the redistribution experiment are summarized in Table 2.2. This table shows the sheet resistance measurements at each of the points in the experiment.

Table 2.2 Summary of Dopant Redistribution experiment measurements.

Process	Oxide Thickness Grown (nm)	Designation	Wafer OxA	Wafer OxB
Initial Measurement	N/A	Rs_1	744 Ω/□	718 Ω/□
After Field Oxidation	684	Rs_2	1547 Ω/□	N/A
After Predep	0	Rs_3	29.9 Ω/□	N/A
After Drive-in	0	Rs_4	6.6 Ω/□	5941 Ω/□
After Gate Oxidation	54.8	Rs_5	6.6 Ω/□	5100 Ω/□

From the table above, a few key pieces of information can be extracted. The first shows that the initial field oxide growth greatly affects the concentration of boron near the surface of the wafer. The value of the sheet resistance doubles after the growth and removal of the field oxide, as seen by comparing Rs_1 to Rs_2. An increase in the sheet resistance implies a decrease in carriers in the lattice (see Equation (3.14)). Another

expected result is that the thermal cycling done during the diffusion of the n-type dopant into the wafer also allows for further diffusion of boron into the oxide layer. The Rs_4 value of wafer OxB has increased from 718.31 Ω/□ to nearly 6000 Ω/□.

Due to the comparatively short time duration of the dry oxide growth, the redistribution of the dopants is not apparent. A comparison of the Rs_4 and Rs_5 values show little change. Theoretically, the second oxidation step should have further increased the sheet resistance of wafer OxB. However, due to measurement difficulties in high sheet resistance profiling, the sheet resistance values in Table 2.2 cannot be examined quantitatively, but only qualitatively using the four-point probe resistance measurement method. The reasons for the measurement difficulties are: (1) it is difficult to make good electrical contact from the probe to the semiconductor, and (2) the surface leakage current can be comparable to the measurement current[5]. As an example, the percent standard deviation in the Rs_1 measurement of wafer OxB is 10.2% while the percent standard deviation in the Rs_4 measurement of the same wafer is 31.5%. This drastic change in uniformity of conductivity cannot be accounted for in the growth of the field oxide alone, as the field oxide had only a 0.53% standard deviation (see Figure 2.7).

Therefore, we can clearly see that the oxidation process, either wet or dry, can be grown in a method that follows predicted model values. It is also apparent that baffling the wafers can increase the uniformity of the layer grown and is an important aspect of gas and temperature regulation in the furnace system. Finally, it is seen that the growth of the oxide layers has an enormous effect on the electrical characteristics of the dopants, as seen by the dopant redistribution. Furthermore, the lower the sheet resistanceof the material, the greater the variation of electrical properties. This implies that we can grow relatively uniform oxide layers, but some action must be taken in order to compensate for the redistribution of the boron in the near-surface regions of the wafers.

Conclusions for this section and chapter

2.7 References

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[2] Colcaster, R. A., Microelectronics Processing and Device Design, John Wiley & Sons: (1980)
[3] Timmons, C.T., D.T. Gray, and R.W. Hendricks, **Process Development for an Undergraduate Microchip Fabrication Facility**, Proceedings ASEE 2001 Annual Meeting (to be published).
[4] http://www.filmetrics.com
[5] Schroder, D. K., Semiconductor Material and Device Characterization, John Wiley & Sons, Inc., NY, 1990

3 Phosphorus Diffusion

3.1 Background

The single most important processing step for creating semiconductor devices is that of doping the wafer. Single-crystal intrinsic silicon behaves very much like an insulator, but the simple introduction of an element with a different valence band configuration allows for actual semiconducting properties. Ironically, though this process is the most important step in silicon semiconductor device fabrication, it is also the process that is the least understood.

The earliest methods for doping involved classical thermal diffusion from a source into the substrate at elevated temperatures. There are three sources of dopants that are currently available for processing;

- solid source,
- liquid source,
- and gaseous source.

The liquid sources often involve metal-organic chemicals, while the gaseous sources are usually AsH_3 or PH_3 and are extremely toxic as well as pyrophoric. Therefore, we use the solid source for safety purposes in our undergraduate laboratory facility. Of the available solid sources for dopants, phosphorus and boron are ideal because the sources (P_2O_5 and B_2O_3) are relatively safe to handle, non-toxic, and not pyrophoric.

Since silicon is a group IV element, it is usually doped with elements from either group III or group V. Of these elements, phosphorus has one of the more complex diffusion mechanisms. Though the literature proposes several theoretical models for the diffusion of phosphorus into the crystal, there exists no comprehensive theoretical model that accurately predicts the profile of dopants in the lattice of the crystal[1]. These models provide insight into the mechanisms of diffusion and the effects of precipitation of phosphorus on the profile. A bibliographic search of the literature showed that much work was done in the field of thermal diffusion of phosphorus and boron into silicon. However, it appears that research into this field began to wane as the technology for ion implantation began to wax.

The current method for doping silicon used in commercial wafer fabrication plants is that of ion implantation. In this process, excited ions are bombarded into the surface of the silicon crystal. By varying the energy of the ions (200 – 1000 keV) and the beam exposure time , the profile and dose of the wafer can be very accurately controlled. This method is very well understood, and allows for the implantation of well-defined layers, both at the surface and several microns below the surface. While this method yields functioning devices, subsequent thermal processing of the wafer allows for redistribution of the dopants within the lattice. Most commercial fabrication facilities account for the redistribution of dopants mainly through empirical data gathered by destructive testing of the wafers (through SIMS for example). SIMS is an expensive method of characterization, with typical tool prices of close to one million dollars. This is therefore not a practical method of characterization in our facility.

3.2 Distribution of Dopant

3.2.1 Thermodynamics of diffusion

The thermal diffusion of phosphorus in silicon poses significant problems that are still not understood today. Some of the disputed aspects of this diffusion are in the mode of diffusion, the diffusion coefficient, and the effects of precipitation of phosphorus in silicon[2]. In this chapter, we review classical theory and then point out where there are important deviations for phosphorus in silicon.

3.2.1.1 Basic Models for Diffusion

The basic one-dimensional diffusion process follows Fick's first law of diffusion,

$$J = -D\frac{\partial N}{\partial x} \qquad (3.1)$$

where J is the particle flux of the donor or acceptor impurity species, N is the concentration of the impurity, and D is the diffusion coefficient.
Fick's second law of diffusion may be derived using the continuity equation for the particle flux:

$$\partial N/\partial t = -\partial J/\partial x \qquad (3.2)$$

Equation (3.2) states that the rate of increase in concentration with time is equal to the negative of the divergence of the particle flux. In a one-dimensional case, the divergence is equal to the gradient. Combining the above equations yields Fick's second law of diffusion:

$$\partial N/\partial t = D\partial^2 N/\partial x^2 \qquad (3.3)$$

in which the diffusion coefficient has been assumed to be independent of position. In order to solve the above equation, one must employ variable separation or Laplace transform techniques. To solve the equation, one must also assume one of two types of initial conditions for the system. The first boundary condition is referred to as constant-source diffusion, in which the surface concentration of the dopants is held constant throughout the process (the case for a gaseous source). The second boundary condition is called limited-source diffusion, in which a fixed quantity of the dopant species is deposited in a thin layer on the surface of the wafer (e.g. ion implantation). As shall be explained later, the predeposition stage of the process allows for the assumption of either scenario, depending on the processing done just before the drive-in stage.

Under the assumption of a constant surface concentration, the solution to Equation (3.3) is:

$$N(x,t) = N_0 \text{Erfc}(\frac{x}{2\sqrt{Dt}}) \quad (3.4)$$

For a semi-infinite wafer where N_0 is the surface concentration in atoms/cm^3, and D is the diffusion coefficient, given by the Arrhenius relationship

$$D = D_0 e^{(-\frac{E_D}{kT})} \quad (3.5)$$

here D_0 is the diffusion constant, E_D is the activation energy, k is Bolzmann's constant, and T is the temperature in Kelvin.

If the limited supply model is assumed, then the solution to Fick's second law is given by the equation

$$N(x,t) = \frac{Q}{\sqrt{\pi Dt}} e^{-(\frac{x}{2\sqrt{Dt}})^2} \quad (3.6)$$

where Q is the initial dose of impurities within the lattice, and D is given by the same Arrhenius equation as above (Equation (3.5)).

3.2.1.2 Advanced Models

While many of the basic models of diffusion given in the literature assume a substitutional diffusion mechanism, some of the more advanced models assume more complex diffusion mechanisms. The more complex models also take into account the effects of phosphorus precipitation, a concentration dependent diffusion coefficient, and the more complicated concepts of charged vacancies in silicon which lead to ionic attraction and repulsion between the vacancies.

One of the more important works done on the subject of the diffusion of phosphorus in silicon was that done by Fair and Tsai. In this work, the authors report that at high concentrations, the diffusion of phosphorus in silicon produces an impurity atom distribution that differs significantly from either the complementary error function or the Gaussian distributions predicted from Fick's law in the previous section.

It is demonstrated in their work that there are actually three diffusion coefficients for phosphorus in silicon, depending on the concentration. At higher concentrations, the $P^+V^=$ pairs dominate in the P diffusion and P electrical activity. At lower concentrations, the $V^=$ vacancy gives up an electron and results in a P^+V^- charge state. In the 'tail' region of the distribution, the vacancy become a V^+ charge state and actually enhances the diffusion.

An important feature of the diffusion of P in Si is that of electrically active P. Due to the complexities of the diffusion mechanism in the crystal, not all of the phosphorus in the silicon provides electrons as free carriers to the lattice. An empirical expression that describes the relation of carriers to phosphorus atoms in the crystal is given by the equation

$$C_T = n + 2.04E - 41n^3 \qquad (3.7)$$

where C_T is the total phosphorus concentration, and n is the electron concentration in the crystal. A plot of this relationship is shown in Figure 3.1 below.

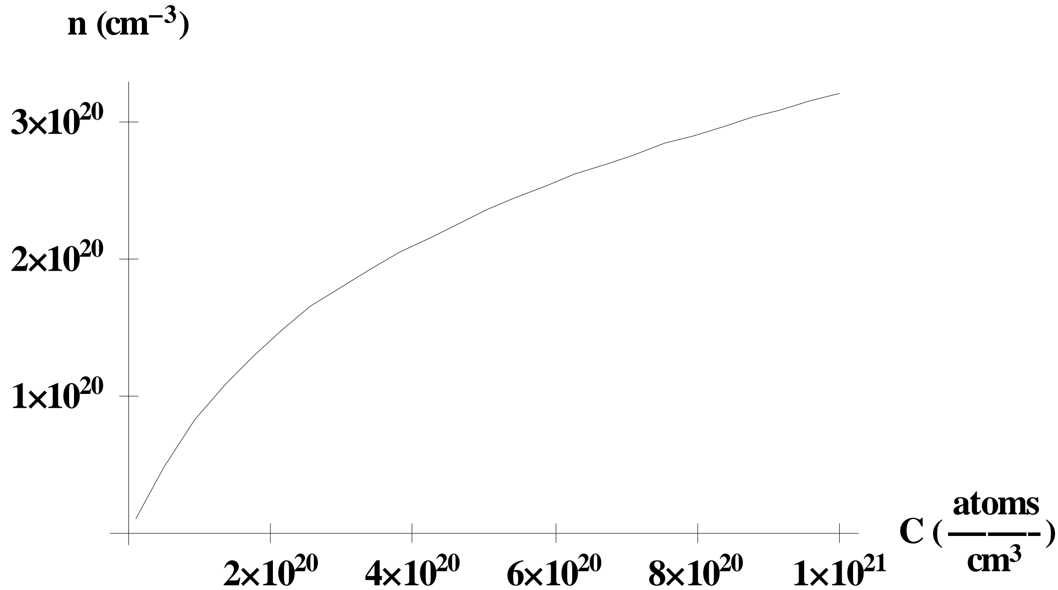

Figure 3.1 Total phosphorus concentration vs. electron concentration in silicon

The significance of Figure 3.1 is that the electrical behavior of the devices must be calculated from the concentrations of carriers, and not from the measured atomic phosphorus profile within the silicon. Since the main method of characterization used in our facility is that of sheet resistance, an understanding of this effect is crucial for process development and control.

Due to the complexities of the diffusion mechanisms of phosphorus in silicon, it is impractical to assume a diffusion coefficient that is constant with respect to the phosphorus concentration. Fair and Tsai reported from their research that the diffusion coefficient has three distinct regions; the 'tail' region, the 'kink' region, and the surface region. An example of the phosphorus diffusivity vs. electron concentration at 1000°C is given in Figure 3.2.

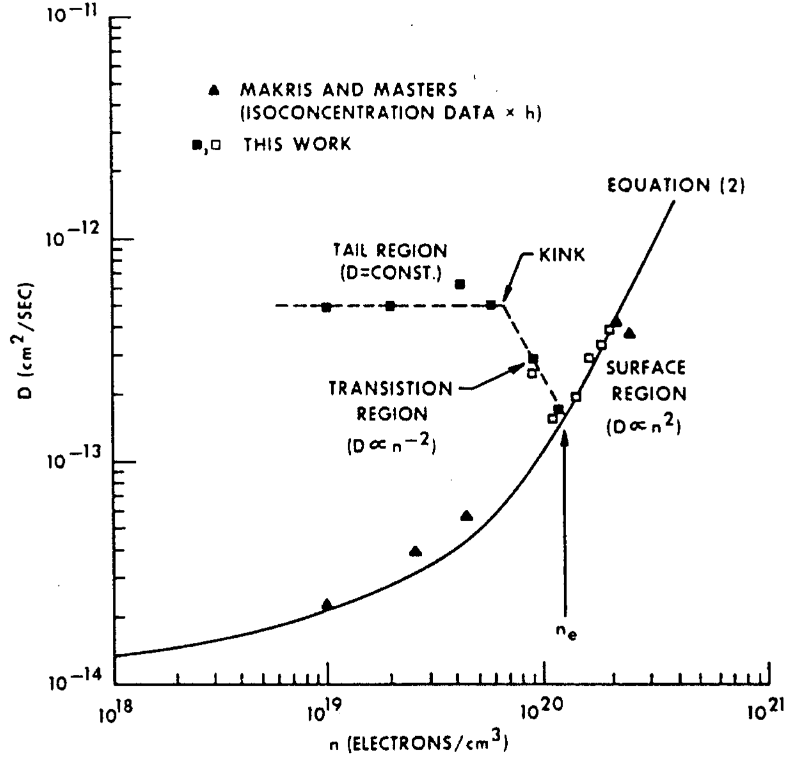

Figure 3.2 Phosphorus diffusivity vs. electron concentration is silicon at 1000°C (from Fair and Tsai[3]).

From their work, Fair and Tsai report a coefficient of diffusion for phosphorus in silicon as

$$D = h[D_i^x + D_i^=(\frac{n}{n_i})^2] \quad (3.8)$$

with

$$h = 1 + \frac{n}{n_i}[(\frac{n}{2n_i})^2 + 1]^{-\frac{1}{2}} \quad (3.9)$$

where n is the electron concentration, n_i is the intrinsic electron concentration and D_i^x and $D_i^=$ are given by the expressions

$$D_i^x = 3.85\exp(\frac{-3.66eV}{kT}) \quad (3.10)$$

$$D_i^= = 44.2\exp(\frac{-4.37eV}{kT}) \quad (3.11)$$

While Eqns. (3.8) through (3.11) can provide for a diffusion coefficient for P in Si, a direct application to the solution of Fick's law is difficult, resulting in a differential equation of the form

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}(D\frac{\partial C}{\partial x}) \quad (3.12)$$

where D is a function of C. A solution to this equation is involved, and is beyond the scope of the material required for an undergraduate teaching facility. An empirical solution for our system is presented for our data in Section 3.4.

3.3 Procedures for Tests

The toolset available in the Whittemore 636 facility allows for a specific form of thermal diffusion, that of solid-source diffusion. The process has two main steps, with several small cleaning steps provided in an attempt to ensure only the diffusion of the desired dopant species – phosphorus.

To begin, any native oxides are removed from the surface of the wafer with a hydrofluoric acid etch. The cleaning is completed with a rinse in isopropyl alcohol and acetone. At this point, any passivation layer and all surface contaminants have been removed from the surface.

The first step is the predeposition step. In this step, the wafer is placed next to a solid source of phosphorus pentoxide (P_2O_5 – Phosplus source from Techniglas) at an elevated temperature. Because of this elevated temperature, the P_2O_5 sources effuse a flux of vaporous P_2O_5 onto the surface of the silicon[3]. This deposited layer then decomposes via the chemical reaction

$$5Si + 2P_2O_5 \rightarrow 5SiO_2 + 4P \qquad (3.13)$$

and the P then diffuses into the substrate, resulting in a shallow, high-concentration layer of phosphorus within the crystal and an oxide layer on the surface. Eighteen wafers were processed in this experiment with different predeposition times and temperatures. Table 3.1 shows the matrix that gives both thermal data and measurement data performed on each wafer for both the predeposition and the drive-in phases of the diffusion.

After the predeposition step, there is a very thin layer of complex phosphosilica glass on the surface of the wafer due to unknown decomposition of both the predeposition and the drive-in steps. This layer can be removed using an HF etch. However, since the layer might provide enough dopant source for the continuous supply model, wafers were processed in parallel. One wafer had the phosphosilica layer removed to allow for a limited-supply assumption, while the other wafer was not etched in order to allow for a continuous supply model.

Following predeposition, half the wafers were etched in HF to remove the oxide. After this etch, the sheet resistance was mapped on all wafers. The wafers were then placed into a furnace at 600°C and ramped to 1100°C, all under dry N_2. At this temperature, the diffusion coefficient is significantly increased (see Equation (3.5)), and the dopant P is allowed to diffuse further into the crystal. After this drive-in step, the wafers were again etched in HF to remove any possible oxidation layers or P_2O_5 layers that might have been deposited during the process. The wafers were then mapped for sheet resistance. A summary of the results of these measurements is given in Table 3.2.

Table 3.1 Matrix for Thermal Diffusion Experiment						
Wafer	Predep Temp (Celsius)	Predep Time (min)	Post predep etch?	Drive-in Temp (Celsius)	Drive-in Time (min)	SIMS measurement?
1A	810	45	Yes	1100	65	No
1B	810	45	No	1100	65	No
2A	810	90	Yes	1100	65	No
2B	810	90	No	1100	65	No
3A	810	180	Yes	1100	65	No
3B	810	180	No	1100	65	No
4A	845	45	Yes	1100	65	No
4B	845	45	No	1100	65	No
5A	845	90	Yes	1100	65	No
5B	845	90	No	1100	65	No
6A	845	180	Yes	1100	65	No
6B	845	180	No	1100	65	No
7A	860	45	Yes	1100	65	Yes
7B	860	45	No	1100	65	Yes
8A	860	90	Yes	1100	65	Yes
8B	860	90	No	1100	65	Yes
9A	860	180	Yes	1100	65	Yes
9B	860	180	No	1100	65	Yes

In order to validate the sheet resistance measurements and to gain a better understanding of the diffusion process, the wafers were sent to Dominion Semiconductor (now Micron Technologies) for further characterization. At Dominion, the wafers were mapped for sheet resistance, and the phosphorus profiles determined by SIMS (secondary ion mass spectroscopy). The SIMS data gave both surface concentrations of phosphorus as well as a profile of the concentration as a function of depth into the crystal. Due to the cost in both man-hours and downtime for the equipment however, it was only possible for six of the wafers to be characterized using SIMS measurements.

3.4 Results and Discussion

The results for the sheet resistance measurements give insight about the profile of the impurity species, though it is impossible to extract the metallurgical junction depth or the surface concentration of the wafer from the Rs measurements alone. The high to low variation is typically 5% for our wafers. Therefore, we believe it is appropriate to compute a single average of the data for each wafer although there is some small, consistent variation between wafers.

Table 3.2 gives a summary of the sheet resistance data of the wafers at the different points in the process (either after the predeposition stage, or after the drive-in stage). These data were verified by comparison to data measured at Dominion Semiconductor (see Appendix A).

Table 3.2 Summary of Sheet Resistance Results for Thermal Diffusion Experiment

Wafer	Post predep Average Ω/□	Post predep % standard deviation	Post drive-in Average Ω/□	Post drive-in % standard deviation
1A	132.65	7.2	58.89	7.3
1B	119.14	3.9	22.25	9.1
2A	69.51	4.0	22.26	17.5
2B	68.35	6.3	11.35	8.4
3A	45.63	2.3	12.47	7.9
3B	46.30	6.2	7.22	6.4
4A	54.74	2.3	13.39	5.0
4B	53.08	3.0	7.21	8.6
5A	36.62	2.6	8.26	8.9
5B	35.39	3.9	4.95	7.9
6A	24.75	1.5	5.47	4.0
6B	24.32	2.3	3.82	3.9
7A	30.47	1.7	6.29	2.8
7B	28.97	2.5	4.07	4.7
8A	21.61	1.6	4.41	3.6
8B	20.97	2.4	3.17	5.1
9A	14.75	1.3	2.95	3.4
9B	14.49	2.0	2.37	4.5

Another interesting phenomena that was observed during the thermal diffusion process was a slightly higher, but reproducible, concentration of dopant at certain points for each wafer. Figure 3.3 shows a typical sheet resistance map performed on the wafers at Virginia Tech. The points of lower resistance all occur at the same location on our wafers. This higher dopant concentration is an effect of subsequent uses of the same quartz wafer boat for many diffusions. While the wafers are being selectively doped with phosphorus, the quartz wafer boats are receiving constant predeposition and drive-in throughout all experimentation and instructional use of the equipment. It is therefore necessary to clean the wafer boats in an HF solution periodically, or to continually change the boats.

Direct comparison with the literature models for diffusion poses several problems in this setup. The first problem deals with the initial dose of phosphorus that has been diffused into or onto the surface of the wafer. The second problem encountered is that of the boundary conditions used to solve Fick's second law of diffusion. The last and most important problem is that of a concentration dependent diffusion coefficient for P in Si, as reported by Fair and Tsai.

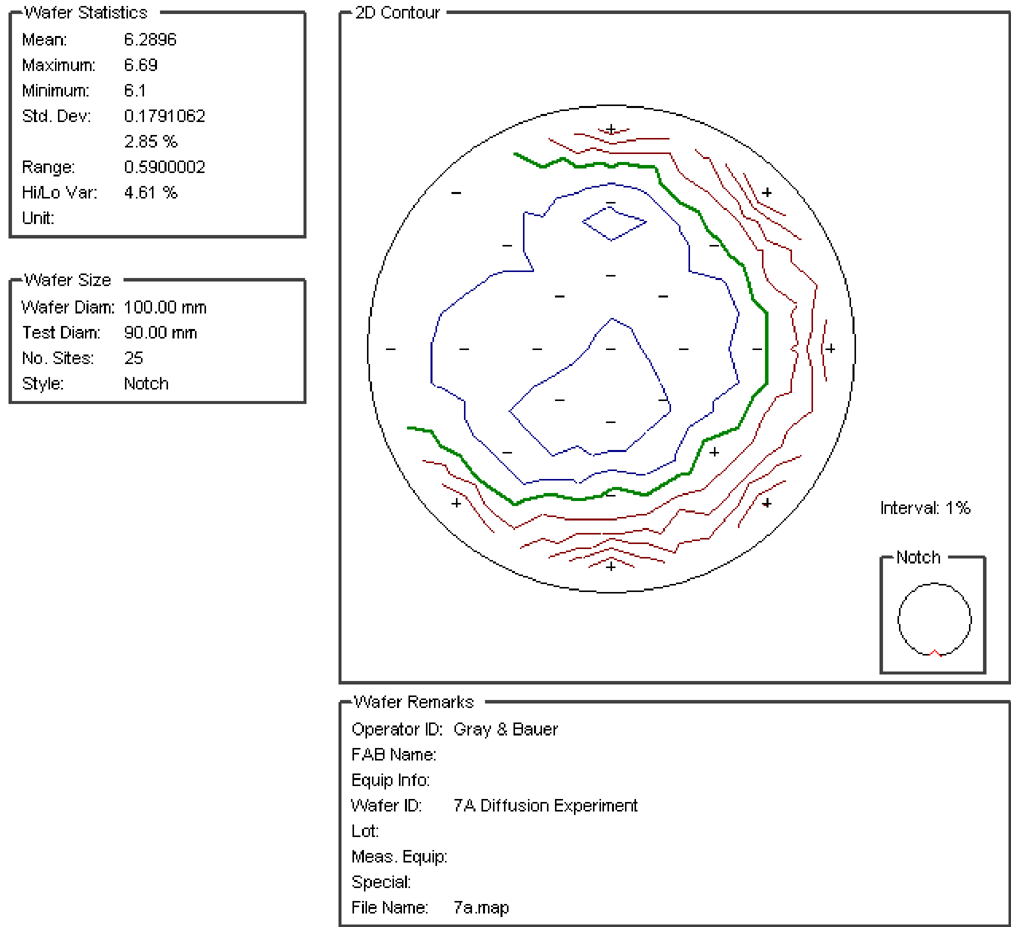

Figure 3.3 Wafer map showing a slight decrease in sheet resistance on one side of the wafer. This decrease can be accounted for by overuse of the quartz wafer boat.

Since the flux of phosphorus from the P_2O_5 solid source is unknown and not easily measured, it is difficult to know whether or not the solid solubility of phosphorus has been reached at the predeposition temperature. Also, since a small amount of the phosphorus diffuses into the crystal during the predeposition stage, there will exist an initial profile in the near-surface area of the wafer. There exist no tools in the Whittemore facility that can measure the surface concentration of the impurity, rendering any characterization of the phosphorus content in the substrate impossible.

However, if one assumes that the solid-solubility has been reached fairly early in the process, it becomes possible to assume a certain dose of phosphorus into the crystal. Since the P_2O_5 sources remain in constant proximity to the silicon wafers and are held at a constant temperature, one can assume a continuous supply model for diffusion, with the surface concentration remaining at that of solid-solubility. For phosphorus in silicon, the solid solubility at 860°C is approximately 3×10^{20} atoms/cc[4]. When these data are

substituted into the continuous-supply model solution to Fick's second law (Equation (3.4)), a profile for the dopant can be assumed to be that shown in Figure 3.4 below, along with the electrically active concentration curve (see Figure 3.1).

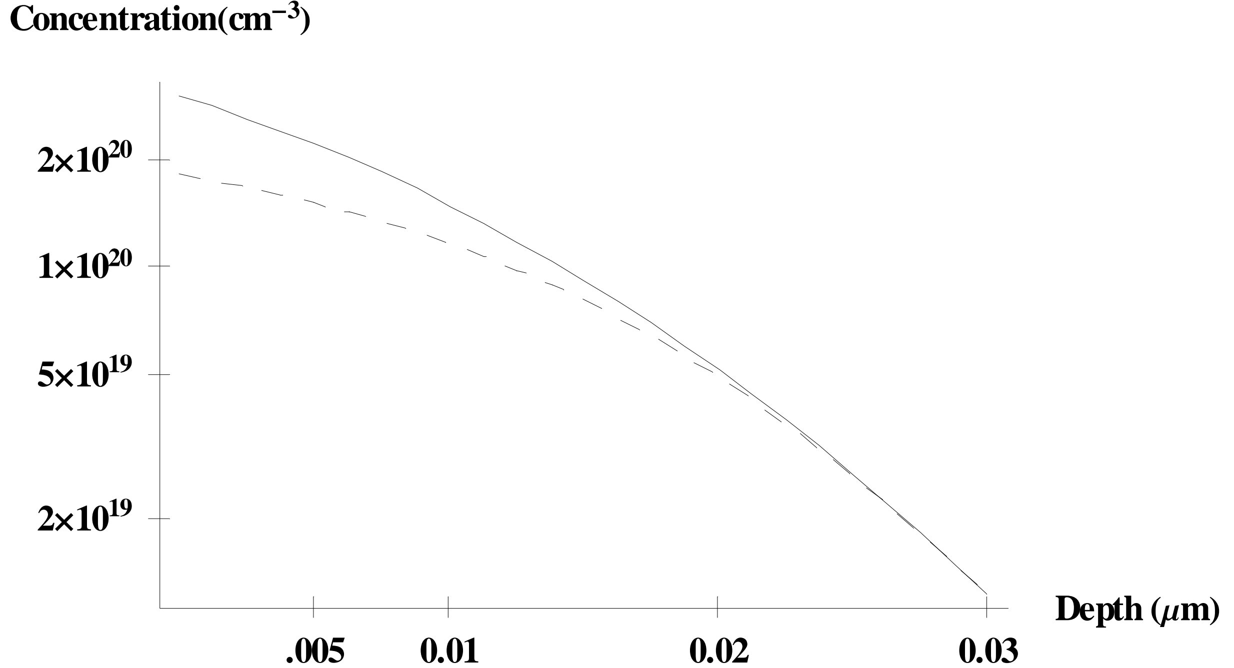

Figure 3.4 Predeposition profile for wafers processed at 860°C for 45 minutes under dry N_2. The integral of this curve is the dose when setting boundary conditions for the drive-in that follow the fixed-supply model. The dashed line corresponds to the electrically active phosphorus profile.

The sheet resistance for a concentration profile is given by

$$R_s = [\int_0^{x_j} q\mu(x)N(x)dx]^{-1} \tag{3.14}$$

where x_j is the metallurgical junction depth, q the charge on an electron, μ(x) is the majority-carrier mobility, and N(x) the net impurity concentration. The value of μ(x) is given by the equation[5]

$$\mu(x) = \mu_{\min} + \frac{\mu_0}{[1+(N(x)/N_{ref})^{\alpha}]} \tag{3.15}$$

where the fit parameters for the mobility are given in Table 3.3.

Table 3.3 Fit Parameters used to determine mobility as a function of concentrationref

Parameter	Value
μ_0 (cm^2/V-s)	1268
μ_{min} (cm^2/V-s)	92
N_{ref} (cm^{-3})	1.3×10^{17}
α	0.91

The junction depth, x_j, is the depth at which the diffusing impurity, phosphorus in this case, is equal to the background concentration of the complementary impurity, boron. At this junction, the silicon acts as intrinsic silicon, since the number of free holes and the number of free electrons is equal. The junction depth x_j can be calculated from

$$x_j = 2\sqrt{Dt\ln(N_0/N_B)} \qquad (3.16a)$$

$$x_j = 2\sqrt{Dt}\,\mathrm{erfc}^{-1}(N_B/N_0) \qquad (3.17b)$$

where D is the diffusivity of the dopant, t is the time of the process, N_0 is the surface concentration and N_B is the background concentration of the wafer. Equation 3.15a applies for the Gaussian distribution while 3.15b is for the complementary error function distribution for diffusion.

When Equation (3.14) above is solved using the curve above for the N(x) values (Figure 3.4), and the proper values for μ, q and x_j, the calculated R_s value is 244 Ω/□. The measured value for the R_s under these conditions has a mean value of 30 Ω/□, a difference of 700%. This model therefore does not adequately describe the predeposition step of the diffusion process.

It is possible to determine the dose of phosphorus that has been diffused into the crystal from the concentration profiles obtained from Dominion Semiconductor. Since one of the wafers has had the surface etched before the drive-in, it can be logically assumed that the drive-in portion of the diffusion process follows the fixed-supply model of diffusion. By that logic, the integral of the profile should give the same value, regardless of the time or temperature of any subsequent processes. When the measured profile for the wafer is integrated, the dose is calculated to be 1.14×10^{16} atoms/cm^2. This dose is to be compared with that calculated from the curve in Figure 3.4 which is only 3.5×10^{14} atoms/cm^2. Clearly more phosphorus has been diffused into the wafer than is predicted by the continuous-supply model with the assumption of a surface concentration equal to the solid-solubility limit at this temperature.

If the profile of phosphorus is recalculated using the dose measured at Dominion Semiconductor, a more accurate representation is given. The surface concentration of phosphorus can be determined from the dose through the equation

$$Q = \int_0^\infty N(x,t)dx = 2N_0\sqrt{Dt/\pi} \qquad (3.18)$$

where Q is the dose of phosphorus in the silicon, N_0 is the surface concentration, D is the diffusion coefficient, and t is the diffusion time. From this equation, the surface

concentration for the wafer under discussion is 9.8×10^{21} atoms/cc. The resulting profile for the predeposition step, and the corrected electrically active profile are shown in Figure 3.5 below.

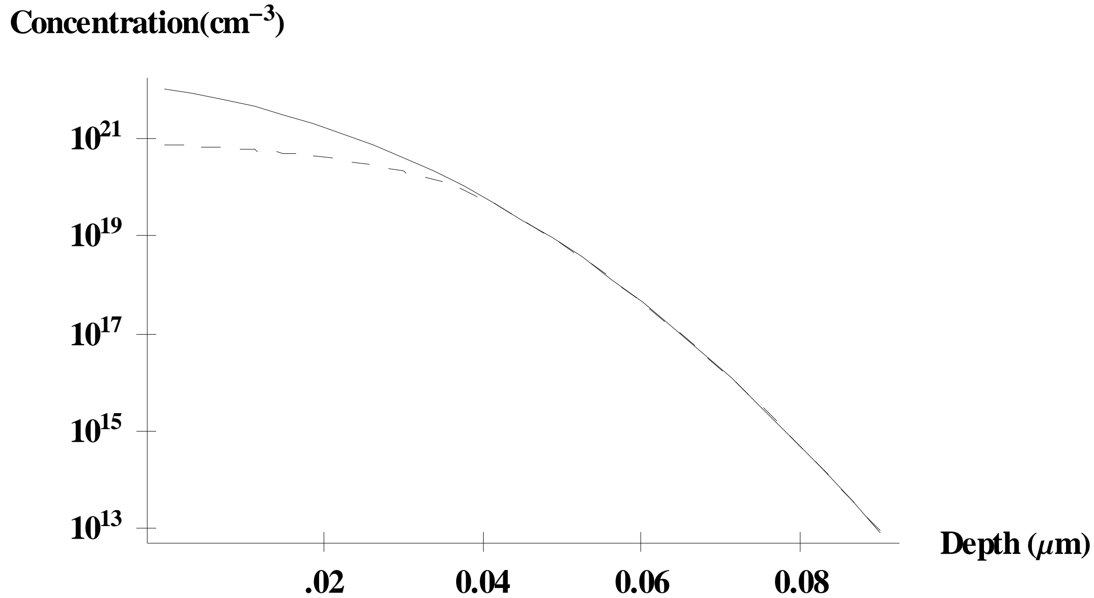

Figure 3.5 Atomic profile and electrically active profile for the predeposition step calculated from the dose measured at Dominion Semiconductor. The solid line represents the total concentration while the dashed curve represents the electrically active concentration.

When the sheet resistance is calculated from the above dashed curve (Figure 3.5), it more closely resembles that measured in the lab. A value of 41 is calculated from the electrically active curve above, compared to 30 measured in the lab. This is a difference of 26%. Fair and Tsai show data that suggests that the diffusion coefficient is much higher for high concentrations of phosphorus than this model assumes (see Figure 3.2). This increased diffusivity will result in (1) more phosphorus in the crystal than predicted, and (2) a decreased sheet resistance. Diffusion models containing a non-constant diffusion coefficient are difficult and involved[6]. Since we are not attempting to numerically solve this problem, but are proposing rather an empirical model for our system, we know that our estimates should underestimate the conductivity, and overestimate the resistance.

The drive-in portion of the diffusion process can also be modeled if one assumes a fixed-supply model. Since no characterization was done of the shallow P_2O_5 layer deposited in the predeposition step, it is not practical to assume an adequate dose for the continuous supply model of diffusion. For this reason, the following analysis will deal solely with the wafer processed under the fixed-supply model. By again using the dose measured at Dominion Semiconductor, and assuming a fixed-supply model, a profile can be generated. A plot of Equation (3.6) assuming D is independent of concentration, and using the dose Q measured at Dominion Semiconductor is shown in Figure 3.6 below.

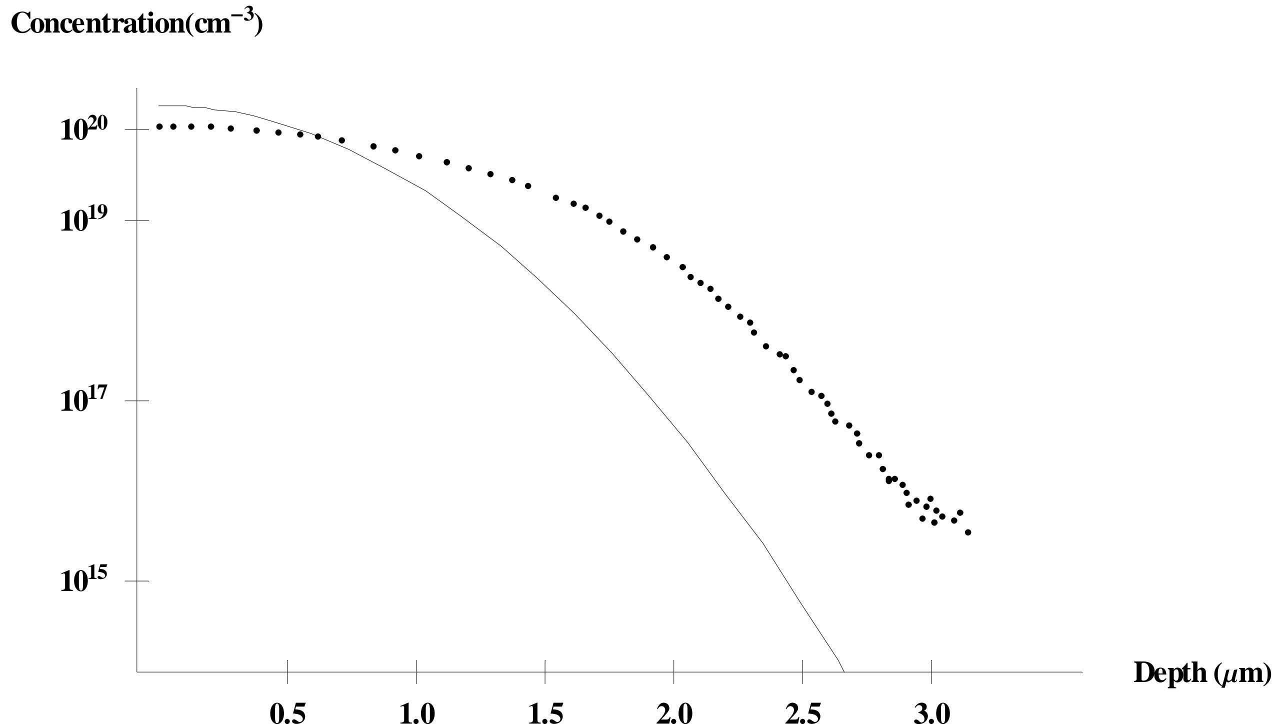

Figure 3.6 Measured profile and calculated profile of phosphorus in the wafer after a 65 minute drive-in at 1100°C using the Arrhenius relationship to determine the diffusion coefficient. The solid line is the curve predicted by the model, while the dotted data points are the data measured at Dominion Semiconductor.

Although the total number of phosphorus atoms in the crystal is the same for the measured and calculated profiles, this model does not accurately portray the dynamics of the diffusion process deep into the wafer. The SIMS data show the material has diffused further into the crystal than this model predicts. The calculated Rs value for the above profile (after having been corrected for electrically active concentration) is 6.9 Ω/□, compared to a 6.3 Ω/□ measured in the lab. The agreement of the resistance values stems form the fact that the resistance is controlled by the near-surface concentration of carriers, and is nearly unaffected by the carriers that are deeper in the crystal.

Since the diffusion coefficient of phosphorus in silicon is not constant with concentration it is understood that this model should have problems in accurately predicting the profile of the phosphorus. For the purposes of modeling our process however, an effective diffusion coefficient was determined by fitting the calculated curve to the measured curve. Since the diffusion coefficient is very sensitive to the activation energy, a small perturbation in activation energy results in a large difference in the diffusion coefficient. The reported value for the activation energy of phosphorus in silicon is given as 3.69 eV. Since the measurement of this energy level is involved and difficult, it can be assumed that the reported value exhibits some error. If this number is varied to 3.62eV (a 2% variation), an effective diffusion coefficient of 5.4×10^{-13} cm^2/sec results. This value of 3.62eV is consistent with that found by French et. al.[7]. Figure 3.7 below shows the measured profile, the calculated profile, and the electrically active profile when the activation energy for the diffusion is set to 3.62eV. This prediction gives a profile that not only matches the electrical behavior measured in the lab, but also gives an accurate x_j value.

The sheet resistance calculated from the electrically active profile in Figure 3.7 below is 6.3 Ω/□, which is the same value measured in the lab.

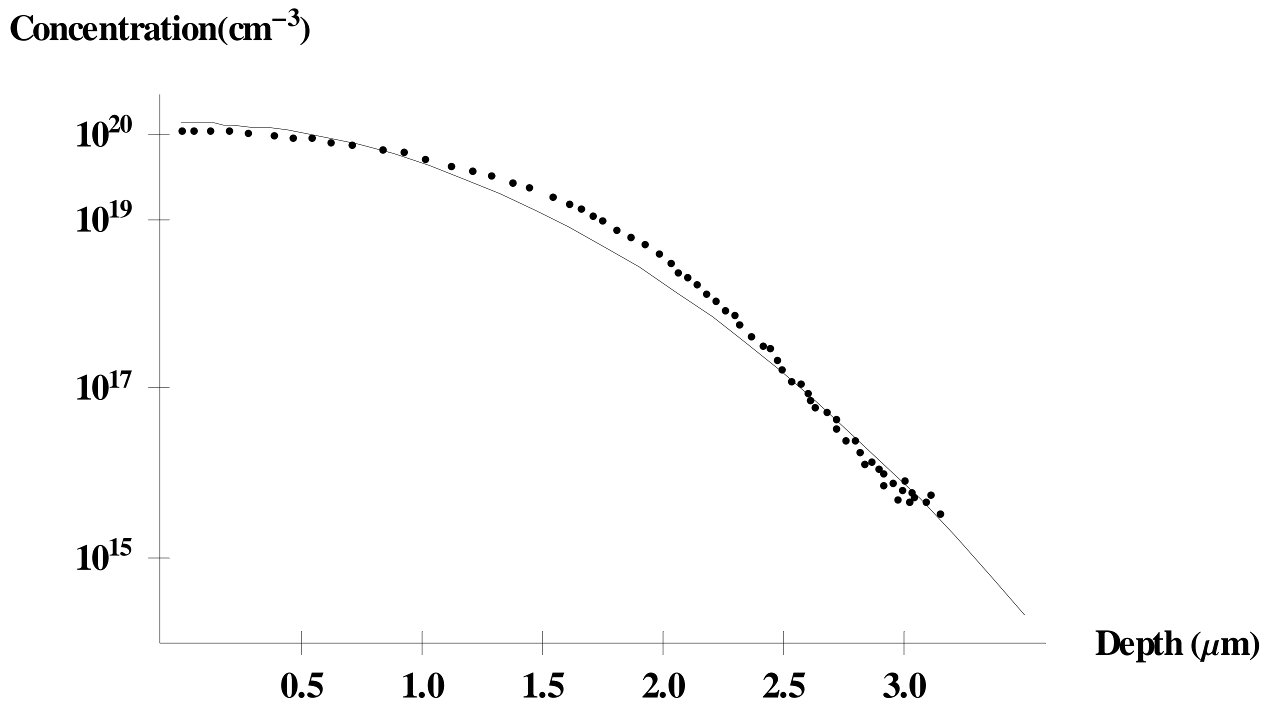

Figure 3.7 Measured, and calculated profiles when $D=D_{eff}=5.4\times10^{-13}$ for a 65 minute drive-in at 1100°C. The dotted data points are those measured at Dominion Semiconductor and the solid curve is the value predicted by the model.

3.5 Empirical Model for Diffusion

When the above analysis is carried out for the three wafers that were measured using SIMS at Dominion Semiconductor, an empirical model for the N_0, Rs, and X_j values can be created.

The first step in the model is to determine the dose of phosphorus diffused into the crystal. An equation that fits empirically the data measured at Dominion is

$$Q = a\left(1 + \frac{be^{(-ct)} - ce^{(-bt)}}{c - b}\right) \qquad (3.19)$$

where Q is the dose, t is the time in minutes of predeposition at 860°C, and a, b, and c were found using TableCurve to be 3.09×10^{16} atoms/cm^2 , 0.033, and 0.033 respectively. Note both b and c are dimensionless. Figure 3.8 below shows the empirical model of atoms/cm^2 versus time at 860°C for our system.

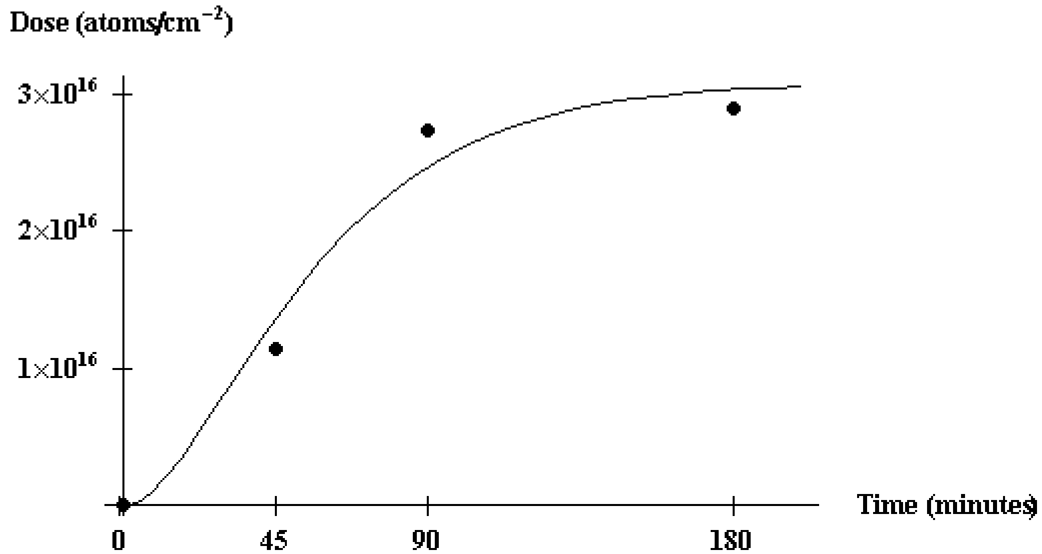

Figure 3.8 Tablecurve fit to measured dose for predeposition times at 860°C

Figure 3.8 suggests that at 860C the maximum dose attainable is 3.09×10^{16} atoms/cm^2. This number is higher than the planar atomic density of silicon 100. However, since some of the phosphorus impingent on the surface will diffuse into the crystal this does not pose a problem to the understanding of the kinetics of the system.

The next step in the modeling is to solve for the surface concentration used in the continuous supply model through Equation (3.18). Using this surface concentration, a profile can be generated for the impurity as a function of depth in the wafer. In order to calculate the sheet resistance from Equation (3.14), it is necessary to correct the profile from atomic concentration to electrically active concentration (Equation (3.7)), and to determine a junction depth. This profile allows for a sheet resistance calculation for the predeposition step (Equation (3.14)). The calculated values for sheet resistance are compared to the measured values in Table 3.4. It is seen that the estimated sheet

resistance and the experimentally observed sheet resistance are generally in good agreement for all experimental conditions studied here.

For the drive-in step, the initial dose value is used rather than the final surface concentration of the predeposition step, providing the wafers are etched before the drive-in step. The procedure for determining the N_0, x_j, and R_s values is the same as for the predeposition step, except for the assumption of a fixed-supply model, and the use of the effective diffusion coefficient, $D_{eff} = 5.4\times10^{-13}$ cm^2/sec. A summary of the data calculated via this model compared to the measured data for the experiment is given in Table 3.4.

Table 3.4 Comparison of empirical model data and measured data for the predeposition at 860C

Time at 860°C (min)	Calculated Dose (atoms/cc)	Calculated Rs after predep	Measured Rs after predep	Calculated Rs after drive-in	Measured Rs after drive-in
45	1.17×10^{16}	40.6	30.5	6.29	6.29
90	2.69×10^{16}	23.7	21.6	3.49	4.41
180	2.95×10^{16}	18.5	14.8	3.29	2.95

3.6 References

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[2] R. B. Fair and J.C.C. Tsai, "A Quantitative Model for the Diffusion of Phosphorus in Silicon and the Emitter Dip Effect," Journal of the Electrochemical Society, 124, 1107-1118 (July, 1977).

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[7] C.S. French, D.P. Belman, D.E. Kardes, and R.W. Hendricks, H**Determination of Junction Depths for Phosphorous Diffused in Silicon**H, Proc. 14th IEEE Biennial University/Government/Industry Microelectronics (UGIM) Symposium held in Richmond, Virginia, June 17-20, 2001.

4 Characterization

4.1 Introduction

A significant component of our laboratory requires that students be able to measure both the sheet resistance of test regions on the wafer during processing and the I–V curves of the simple devices created during the course of the semester. These devices include resistors, pn junction diodes, and nMOSFETs. Commercial semiconductor parameter analyzers (SPAs) are both relatively expensive and far too complex for the level of characterization required for this laboratory. In order to allow such measurements, we have developed a relatively simple and cost effective parameter analysis system.

The purpose of this chapter is to describe this simple, yet automated, system that is built of easily obtainable components and programmed in LabVIEW.

Requirements

To meet the needs of a high-throughput undergraduate laboratory, our semiconductor characterization system must meet several requirements.

(1) It must be relatively inexpensive.
(2) It must be capable of determining
 (a) the sheet resistance of as-received and doped wafers.
 (b) the I–V curves of semiconductor resistors, pn junctions, FETs, and other devices that may be created in the laboratory.
(3) The measurements must be made on devices of dimensions in the range of hundreds of microns
(4) The results generated by the system should compare well with those attained on more sophisticated systems and should be consistent with ASTM standard procedures where applicable.
(5) The time invested by the students to perform the measurements should be low compared to the time spent in analyzing the results of those measurements. This implies that the system must be fully automated.
(6) There must be a simple method for exporting data for inclusion in student laboratory reports. This implies links to a file server since our cleanroom protocols prohibit bringing paper into the cleanroom.
(7) The automation software should be developed in a well-established, simple high-level language that allows for ease of maintenance and modification for future upgrades.

In order to connect the measurement tools and the PC with the semiconductor wafer, the system must be able to interface with both a four-point probe station (for sheet resistance measurements) and with a microprobe station (for device characterization). These two stations must be insensitive to photocurrent generation to ensure proper characterization of the materials and devices.

4.2 System Description

A system that meets these requirements consists of a dedicated four-point probe station for sheet resistance measurements and a wafer probe station with micromanipulators for all I–V measurements. Voltage and current are provided by a voltage-current source module, and data acquisition is via a dedicated PC. The measuring instruments are connected to the PC via a GPIB and all programming is done in LabVIEW 6.1.[1]

Specifically, the system we have developed includes the following components:

- a Signatone model S-304-4 Four Point Probe Station[2] with SP4-62.5-85-TC probe heads. The tungsten carbide (WC) tips are spaced at 0.0625 in.,
- a Signatone model H-150 Hybrid Microprobe Station[3] with six micromanipulator probes,
- a Keithley Instruments model 2400 Series Source Meter[4],
- a National Instruments model SCB-68 shielded I/O connector block[5],
- a National Instruments model 6024E multifunction board[5],
- a National Instruments model PCI-GPIB card,
- a Dell Optiplex G300 PC (550 MHz processor, 128MB memory, 10 GB HD, and Ethernet NIC) with Microsoft Windows 2000 Pro operating system[6],
- a custom-made dark box[7], and
- miscellaneous cabling.

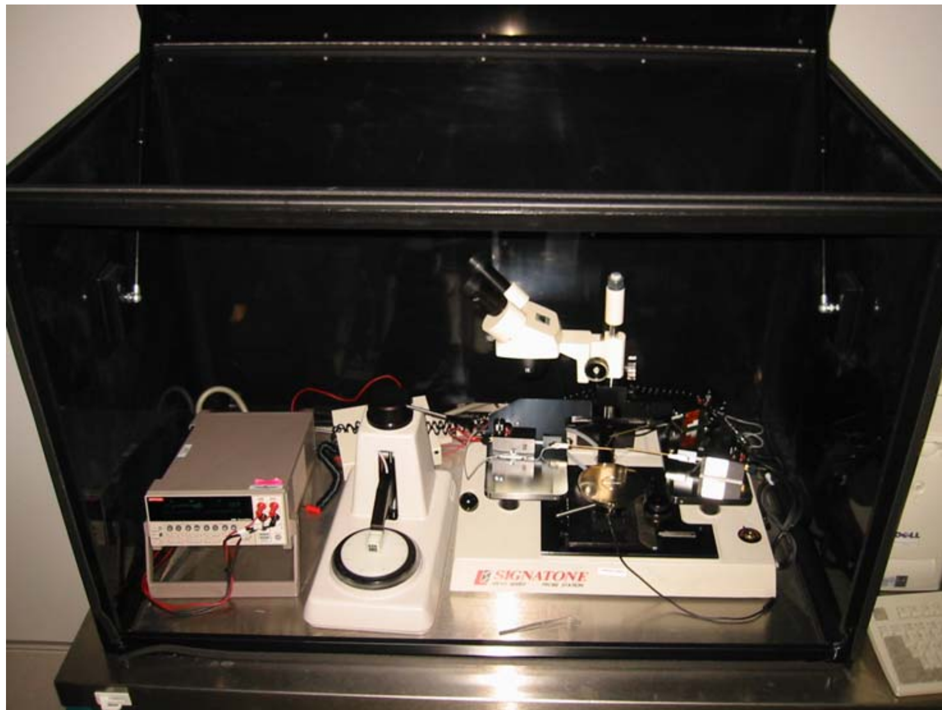
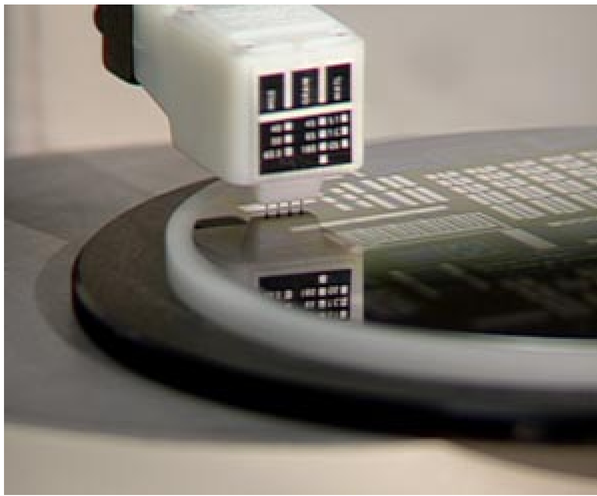
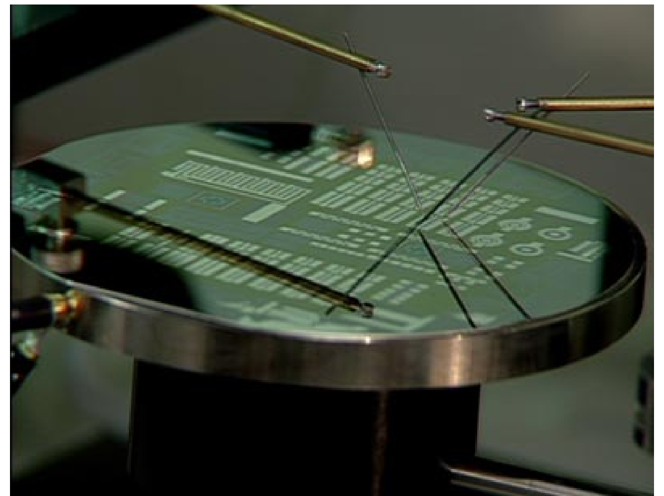


Figure 4.1 Photograph of the Virginia Tech semiconductor characterization system. Components from left to right: Keithley 2400; Signatone S-304; Signatone H-150; and Dell PC.

An important feature of the Keithley 2400 Source Meter is its front and rear panel dual outputs.. This feature allows both the S-304 and the H-150 to be connected simultaneously to the unit although only one may be used at any given time. The wiring of the system is straightforward. The front panel I/O outputs of the 2400 are connected to the outer current probe tips of the S-304 sheet resistance four-point probes, while the front panel 4-wire sense inputs are connected to the inner voltage probe tips. For sheet resistance, the NI 6024E voltage source is unused. In the case of the H-100 microprobe station, the two rear panel 2400 I/O outputs as well as the NI 6024E voltage output are connected to three micromanipulator probe tips that are positioned on the device under test (DUT) as appropriate for the given device and measurement. The signal between the two probe tips connected across the 2400 are read by the 6024E via the SCB-68. The 2400 is controlled by software via the GPIB interface while the 6024E is programmed directly. The software to control the system is described in the next section.



(a)



(b)

Figure 4.2 Photos of DUT (a) in S-304 four-point probe station, and (b) in H-100 microprobe station

As will be shown in the Section 4.5, the photocurrents generated by exposure of our wafers to the fluorescent light of our fabrication facility significantly degrade the quality of our measurements. Thus, we designed a simple dark box that was manufactured for us from black polypropylene.[7] This box has a raisable lid that allows complete access to both Signatone stations but ensures total darkness when the lid is closed.

A photograph of the completed characterization system is shown in Figure 4.1 while typical devices under test are shown in Figure 4.2.

4.3 Software Requirements and Design

The hardware that comprises the system is powerful and capable of performing all the necessary tests required for our laboratory experiments. However, the completion of the several tests required to fully characterize both our process and the resulting devices is tedious (but possible) without automation. Therefore, the system we have developed is controlled by a computer, both to allow for ease of use and to allow for the recording and

analysis of the data gathered in each test. The code that controls the system must be able to easily interface with the hardware, must be capable of allowing some manipulation of test parameters, but not necessarily the actual setup of those tests, and must allow for storage and export of data gathered in the tests in a format that allows for manipulation in other analysis programs (curve fitting software, Microsoft Excel,™ etc.). Since our semiconductor fabrication facility is an evolving laboratory, it is essential that the software be easily modified should the devices or process flow change.

The theory underlying the various tests (sheet resistance for process control and I–V curves of resistors, pn junction diodes, and nMOSFETs) is described in a plethora of texts. We have followed closely the texts by Schroder[8], Neudeck[9], and Pierret[10], plus the relevant ASTM standard procedures[11,12]. The details of our calculations will be given in the following section.

Our pedagogical philosophy is that the characterizations system must automate the acquisition of the data necessary for each measurement, and that it must show the basic I–V characteristics for each measurement. However, it is not essential, as is the case for automated commercial systems such as the Keithley System 86 unit in use in our research facility, that our characterization system be able to perform all of the data manipulation, curve fitting, and parameter extraction operations required for a full analysis of the data. To the contrary, it is an essential part of the student's experience that she be able to perform such analyses manually in software external to the characterization system. As we will demonstrate in the following sections, we have found that all of these analyses can be performed in Microsoft Excel™ although we have found that the availability of a set of statistical macros such as those provided by the ThinkPoint™ Statistics Menu[13] is especially valuable for more advanced students who are required to perform error analyses on the parameters they extract from the system.

There exist many computing languages that could be used to handle both the automated control of the hardware and provide a user-friendly interface. We selected LabVIEW 6.1 as our programming language. LabVIEW is an visual programming language with an excellent drag and drop graphical user interface (GUI) and support for networking and data storage in a relational database management system (RDBMS). As such, it has a lower learning curve than would C++ or many of the other lower level languages. The source code for our program is available from the MicrON WWW site at no cost under the distribution rules of the Free Software Foundation[14] and is available on our website.[15]

We have programmed our characterization system to have a simple GUI that leads the student through the measurements. First, the type of measurement to be performed is selected and the system instructs the student to mount the wafer in the correct station and to position the requisite probes (either 4-point sheet resistance or I–V measurements using micromanipulators) on the location/device to be measured. In the case of I–V measurements, the student is instructed to position either two probes (resistors, pn junctions) or three probes (FETs). The dark box lid is closed and the PC is instructed to proceed.

Our undergraduate facility is one of four major facilities operated by the Center for Microelectronics, Optoelectronics and Nanotechnology (MicrON) at Virginia Tech[16]. The facilities serve several hundred faculty, graduate, and undergraduate researchers.

Access to these facilities and the many instruments contained therein is controlled by a sophisticated laboratory information management system (LIMS)[17]. As part of this system, all users store data acquired in the facilities in personal subdirectories maintained on a dedicated remote file server outside the cleanroom. The semiconductor characterization station described here has been coded so that the students may likewise store all data on the this file server, thus allowing them access to their data for analysis at any time without our having to be concerned with local security issues associated with providing backup of and FTP access to the characterization system PC.

4.4 Applications

At this time, there are four tests that are designed into the characterization system and which are routinely performed in the lab. These are: measurement of the sheet resistance of the wafer following various steps in the processing, I–V characteristics of resistors, I–V characteristics of pn junction diodes, and I–V characteristics of nMOSFETs. More tests can be added when new devices are included in the mask set used by the students. We envision building contact resistance structures, capacitors, BJTs, pMOSFETs, cMOSFETs, and perhaps simple circuits such as ring oscillators in the future. However, for the present we have found that the three devices currently on our mask set provide an excellent introduction to MOS fabrication for our sophomore-level students. In the following paragraphs, we outline each of these measurements and show typical results for our wafers.

4.4.1 Sheet Resistance

The resistivity of a finite slab of a uniformly doped semiconductor wafer, as determined by the four-point probe method with uniformly spaced probes, is[18]

$$\rho = 2\pi s F \frac{V}{I} \tag{4.1}$$

where s is the probe spacing and F is a correction factor for both the effects of the finite size of the sample and the placement of the probes on a finite sample. F is written as the product of three terms

$$F = F_1 F_3 \left[\ln(2) F_2 / \pi \right] \tag{4.2}$$

where F_1 corrects for the sample thickness, F_2 corrects for the sample dimensions, and F_3 corrects for the probe placement. The correction factor F_1 also depends on whether the bottom wafer surface is conducting or non-conducting. Details of the various calculations are reviewed by Schroder.[18] In our case, we have set up the Signatone S-304 using a Teflon insulating disk between the wafer and the sample support, thus validating the use of the non-conducting correction factor. In our case where the sample thickness is small compared to the probe spacing ($t \le s/2$), F_1 is

$$F_1 = \frac{t/s}{2\ln(2)} \tag{4.3}$$

In the case where the lateral dimension of the dimension of the wafer, d, is large compared to the probe spacing ($d \geq 40s$)

$$F_2 = \frac{\pi}{\ln(2)} \qquad (4.4)$$

This is easily the case for measurements made near the center of our uniformly doped 100 mm wafers, but care must be taken for measurements in the special n-wells we have created for determining the effect of n-doping via diffusion.

Again, for measurements made far from the edges of a circular wafer, $F_3 = 1.0$. However, for measurements made in a rectangular doped area, if the distance, d, of the probe is less than 3s from the edge of the well, F_3 is different from unity and depends on the orientation of the probe and whether or not the boundary of the well is conducting or insulating. In our case, our diffused wells are 2.5 mm x 10 mm. We make measurements with the axis of the probe tips parallel to the long dimension of the well. The wells may be considered to have non-conducting edges. For this geometry, $F_3=1.489$. We take care to be sure the measurement is made in the center of the well, and we have created a separate well for each measurement that must be made to monitor the process. In our current wafers, there are three separate wells, one for use after each thermal process.

Combining Eqns. (4.1)–(4.4), for the case where $F_3=1.0$, the resistivity is

$$\rho = \frac{\pi t}{\ln(2)} \frac{V}{I} = 4.532 t \frac{V}{I} \qquad (4.5)$$

Equation (4.5) may be applied directly to our bare wafers of thickness $t = 0.550 \pm 0.050$ mm. However, in our doped wafers where the n-doping ($N_D \approx 10^{19}$/cc) is orders of magnitude greater than the p background doping ($N_A \approx 10^{15}$/cc), the depth of the metallurgical junction, x_j, is only approximately known and there is a strong concentration gradient of the donor doping.[19] In this case, it is traditional to determine the sheet resistance of the material rather than the resistivity. The sheet resistance is an averaged measurement of the number of carriers that are present in a diffused wafer and can be calculated from the dopant profile**.**

$$R_s = \frac{\bar{\rho}}{x_j} = \left[\int_0^{x_j} q \mu N(x) dx \right]^{-1} \qquad (4.6)$$

where q is the charge on the electron, μ is the carrier mobility, and N(x) is the carrier concentration at a depth *x* below the surface[20]. Combining Eqns. (4.5) and (4.6), and using the appropriate F_3 for our diffused wells,

$$R_s = \frac{\bar{\rho}}{x_j} = \left(\frac{\pi}{\ln 2} \right) F_3 \frac{V}{I} = 6.748 \frac{V}{I} \qquad (4.7)$$

for $s \geq t$ where s is the probe spacing and t is the sample thickness.

To make sheet resistance measurements, a small, fixed current is applied to the outer pair of probes and the potential across the inner pair of probes is measured following the ASTM standard procedures. In our apparatus the drive current is swept between lower and upper limits that result in induced voltages of approximately –10mV and 10mV

respectively. Figure 4.3 shows typical results for one of our wafers. The two curves in the figure show the sensitivity of the measurement to light. These curves represent the raw data measured by sweeping a DC current source, and measuring the resulting DC voltage. The starting voltage, ending voltage, number of points to measure, and horizontal correction factor are all user-inputs into the system. The starting and ending voltages are selected in accordance with the ASTM standard procedure. On completion of data acquisition, a regression curve is fitted through the data to determine V/I and the resistivity or the sheet resistance is computed from Eqns. (4.5) or (4.7) as appropriate.

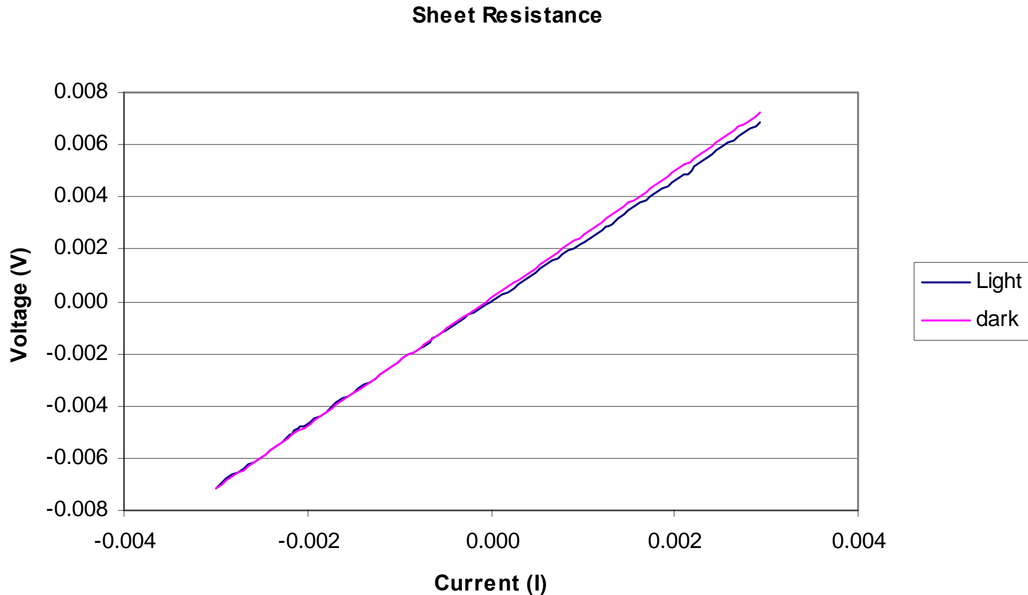


Figure 4.3 Example of R_s data generated by the characterization system and plotted in Microsoft Excel. Note the increase in the current resulting from photogeneration when the sample is measured in the light. The effect of light is to reduce R_s from its correct value by 3%.

A straightforward propagation of errors analysis shows that the estimated standard error of the sheet resistance for the data of Figure 4.3 is approximately 0.005%. This very small value is because of the extremely good fit of the data to Ohm's law ($R^2 = 1.000$). This analysis does not take into account systematic errors resulting from errors in the correction factors F_1, F_2, or F_3, nor does it take into account errors resulting from areal non-uniformity of doping of the wafer on a scale of the size of the spacing of the probe tips. We will shortly show that the latter effect is small.

We have made two important deviations from the ASTM standard procedure. First, rather than measure the voltage at a fixed drive current and then with the current leads reversed, and then averaging the two results, because we have an automated system, we sweep the drive current between the negative and positive values as shown in Figure 4.3 and compute a regression line fit to the data. This is equivalent to performing the average n times, where 2n+1 is the number of data points in the sweep. Second, the ASTM procedure requires that the drive current be determined by placing a standard resistor in

series with the current probes and measuring the voltage drop across it with a 3½ digit voltmeter. In our system, we program the output current, but we read back the actual current output by the 2400 source meter. A simple propagation of error analysis shows that, for the accuracy required of our measurements, this procedure provides excellent results. More importantly, it greatly simplifies the measurements and reduces the cost of the system.

Sheet resistance is measured throughout the course of the wafer fabrication to ensure proper doping, as well as to monitor to some degree the effect of thermal cycling on dopant redistribution. Although in our standard wafers there are only 5 test pads for sheet resistance, as a calibration of this system, we prepared a wafer that was doped over the entire area of its surface. We then measured 25 positions in a appropriate x-y grid and created a contour map of the sheet resistance using Wafer Map 2.1[21]. A typical result is shown in Figure 4.4. The contour spacings are in 1% increments and show that our solid-state diffusion process is remarkably constant over the wafer surface (-2% / +6% from the average). The plots show a slightly higher (5%) doping on one side of the wafer than the other. This has been attributed to contamination of the quartz wafer boat with P due to overuse (see Chapter 3). As a check of our system, the same wafer was measured at Dominion Semiconductor (now Micron Technologies) in Manassas, Virginia using a commercial sheet resistance wafer mapping system with very similar quantitative results as shown in Chapter 3.

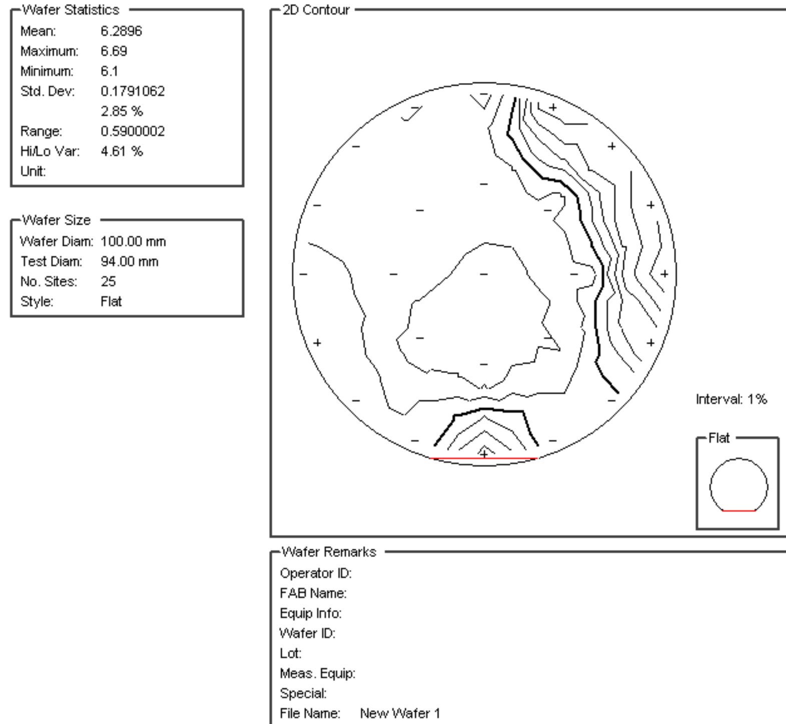


Figure 4.4 Contour map of sheet resistance measurements on a wafer doped with P via a solid-state process over its entire surface. The contour spacings are in 1% increments.

4.4.2 Resistors

On completion of wafer fabrication, the first devices that are characterized are the resistors. Our resistors are made from n-diffused lines ($N_D=10^{17}–10^{19}$/cc) in the p-type substrate ($N_A=10^{14}$/cc). They are created as meanders with multiple metallic pads as shown in Figure 4.5. The objective of this geometry is to allow the students to check the uniformity of long resistors by measuring the resistance between different pads. The resistance between any two pads (numbered 0,1,…,5, respectively) is measured by mounting the wafer on the H-150 microprobe station, positioning one probe on pad 0, and the other probe sequentially on pads 1 through 5.

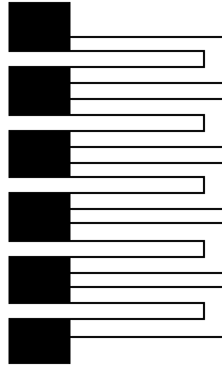


Figure 4.5 Typical layout of a resistor. The black rectangles represent Al measurement contact pads.

The user is requested to input a starting voltage, a stopping voltage, and the number of points to sweep. The system then sweeps the voltage through those values and measures the resulting current. A regression plot of the sensed voltage versus the drive current gives a straight line whose slope is the resistance between the probes. These data are saved for export and further off-line data analysis.

Since the geometry of the resistors is identical for each segment of the meander, if the wafer is uniformly doped over the physical size of the entire resistor, the resistance between each pair of pads should be identical. Therefore, the resistance between the nth pad and the first pad should be given by

$$R_n = \frac{V_n}{I} = R_s n \left(\frac{L}{W} \right) \quad (4.8)$$

where n is the pad number, V_n is the voltage drop between the nth pad and the end pad, L is the path length between any two pads, and W the path width. A typical result of such a regression for a resistor meander is shown in Figure 4.6. For our mask set, the distance between each pair of pads is L/W = 21.4□ (the units of L/W is squares, or □). Using this value and the slope of the regression line of R_n versus n shown in (Figure 4.6), the sheet resistance is found to be 4.29 ± 0.03 Ω/□ obtained from the error analysis in the regression coefficients of R vs. n. This measurement does not take into account the effect of the contact resistance of the aluminum pads or the effect of current spreading under the contacts[22], both of which should be considered for more precise determinations of R_s. The error analysis also assumes no error in L/W. Any such errors would cause a systematic error in R_s.

Wafers currently processed in our lab have only five sheet resistance measurement ports available, which makes it somewhat difficult to determine the level of uniformity across the entire wafer. There will therefore be some disagreement between the actual resistance measured on the device and that calculated by multiplying the area of the resistor by the average sheet resistance of the wafer. The average value of the sheet resistance measured through the sheet resistance ports for the wafer shown in Figure 4.6

is 5.63 Ω/□, a value that is 31% higher than the value determined from the resistors. The discrepancy cannot be explained by non-uniformities in the doping (see Figure 4.4), nor by contact resistance. Examination of the meander under an optical microscope (Figure 4.7) shows that meander paths designed to be 500 μm wide were actually etched to a width of approximately 610 µm. The actual value is 22% wider than the designed value, which explains the variation in the resistor values calculated using the sheet resistance versus those measured directly from the aluminum pads.

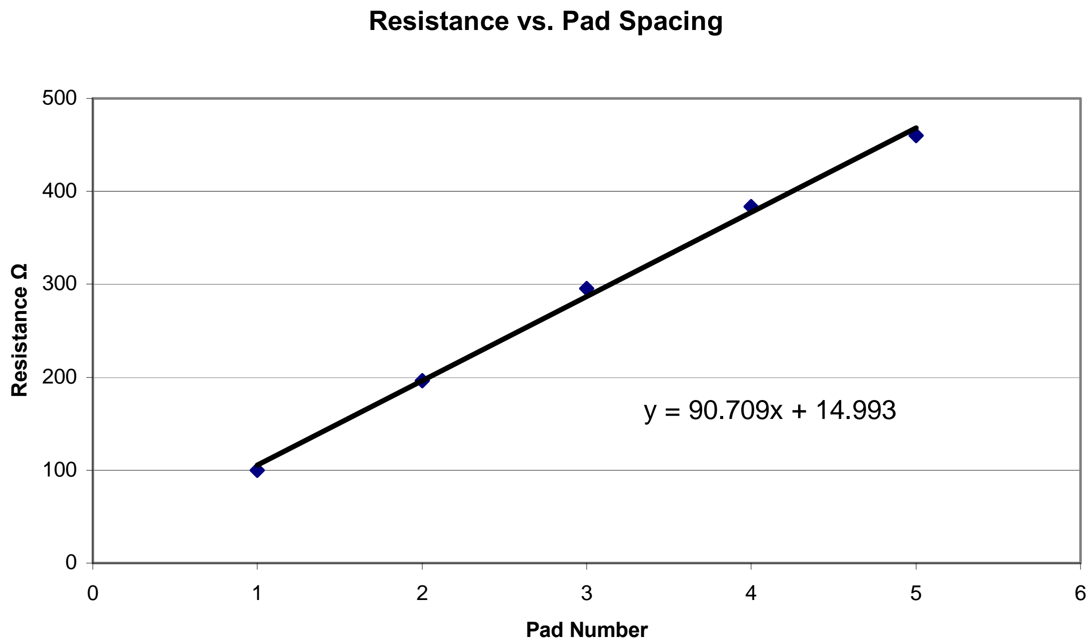


Figure 4.6 Plot of resistance versus pad spacing. The curve is nearly linear with only slight curvature for n = 5. This implies locally uniform doping of the substrate.

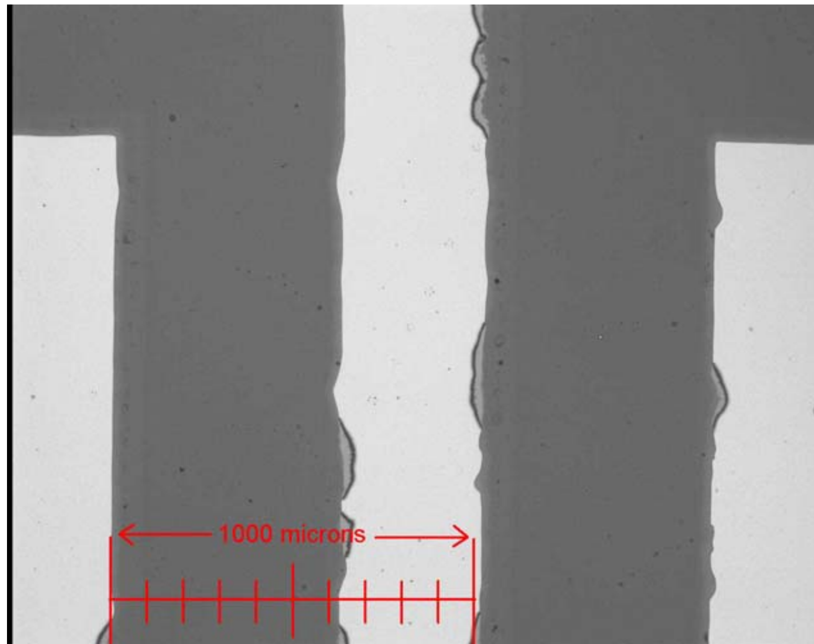


Figure 4.7 Optical micrograph of resistor meander path. The dark area in the photo is the etched channel into which phosphorus was diffused. The actual width of the channel is 610 μm where the designed width was 500 μm.

The variance of the two resistance values (that calculated from sheet resistance versus that measured from the resistor meander) can therefore be taken as a measurement of the amount of over-etch of the oxide layer. This over-etching is a result of either light bending around the mask, poor contact between the mask and the photoresist, or simply too much time in the HF bath.

4.4.3 pn Junctions

The p-n junction devices are constructed by creating an n+ well in the p-type substrate by thermal diffusion. A thin layer of gate oxide (40 nm) is grown over both the p-type substrate and the n-well to provide physical protection. Next, an aluminum contact pad (50 nm) is evaporated on each side of the p-n junction, contacting the silicon through holes that are chemically etched through the oxide. The I–V characteristics of the p-n junctions may therefore be thought of as surface measurements. For this reason, all characterization will follow the analysis of the abrupt junction diode. We have created five different size p-n junctions varying from Z= 1000 µm to 6000 µm. Figure 4.8 shows a typical I–V curve for a diode junction, including both the case in which there is direct light on the diode and the case in which the diode is protected in the dark box. This plot shows a significant photoelectric effect on the measurements. The reverse bias current is raised from –5 µA to –8 µA for light versus dark conditions. There are three characteristics of the p-n junction that are routinely examined by our students using this setup—the reverse breakdown voltage, the ideality factor, and the effect of the bulk semiconductor resistance on the forward current.

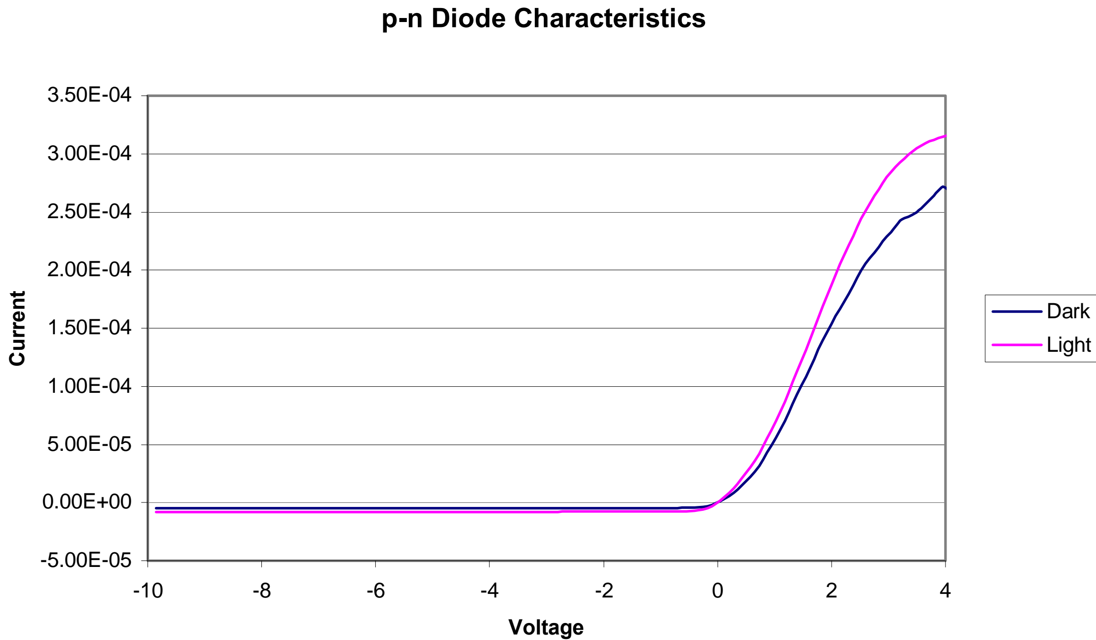


Figure 4.8 Example of Light v Dark for a typical p-n junction diode. Reverse current for light and dark measurements is –8 µA and –5 µA respectively. Also note the difference in slope of the ‘on’ sections of the curves.

4.4.3.1 Reverse Breakdown Voltage

The reverse bias breakdown voltage of the n^+-p junctions created on our wafers is related to the concentration of carriers on the more lightly doped side of the junction. The avalanche breakdown voltage is related to the doping concentration by[23]

$$V_{BR} = \frac{K_s \varepsilon_0 E_{CR}}{2q} \left(\frac{N_A + N_D}{N_A N_D} \right) \tag{4.9}$$

where V_{BR} is the reverse breakdown voltage, E_{CR} is the critical value of electric field, K_S is the relative dielectric constant of the semiconductor, ε_0 is the permittivity of free space, and N_A and N_D are the values of the concentration of acceptors and donors on each side of the junction. The critical value of the electric field, E_{CR}, is a physical constant for a given semiconductor material, and is nearly independent of doping. E_{CR} is about 3×10^5 V/cm for Si[24]. For our wafers, which are lightly doped p substrates with n^+ diffusion doping, Eqn. (4.9) is proportional to $1/N_A$. Substituting the known constants for Si in Eqn. (4.9) and the known acceptor concentration (1×10^{14} /cc), an avalanche breakdown voltage of approximately -1500 V is predicted.

The breakdown characteristics of a p-n junction diode created in our lab are shown in Figure 4.9, from which it is seen that the breakdown voltage occurs at around –140V. This value is substantially lower than that predicted for an ideal device and may be accounted for by the curvature of the edges of the n-wells in our shallow (1.5–2.5 μm) devices.[19] Yang shows that the breakdown voltage is 140 V for devices with a curvature of about 4 μm.[25] It is not possible for us to determine the exact shape of our wells. However, we believe these results to be completely self-consistent.

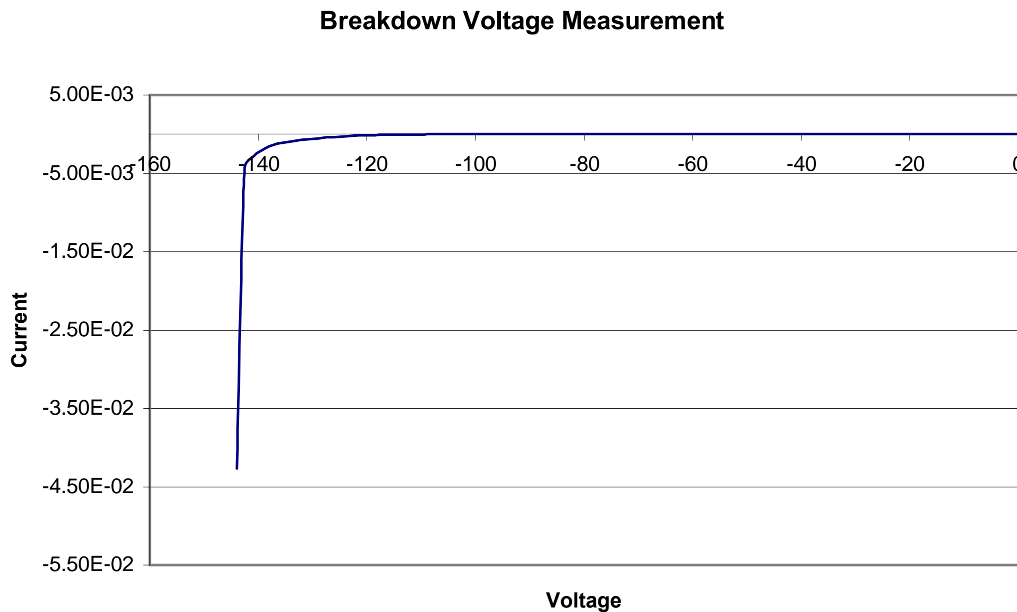


Figure 4.9 Breakdown voltage measurement of a n^+-p junction diode. The plot shows avalanche breakdown at about –140 V.

4.4.3.2 Forward Deviations from Ideality

There are two characteristics of a pn junction that might cause deviations from the ideal when the diode is forward biased. Both the bulk resistance and the ideality factor can affect the properties of the I-V characteristics of the device.

The diode current of a pn junction is usually written as a function of the applied voltage

$$I = I_0\left(e^{qV_d/nkT} - 1\right) \qquad (4.10)$$

where I_0 is the reverse saturation current, q is the charge on the electron, V_d is the diode voltage, n is the ideality factor, k is Boltzmann's constant, and T is the absolute temperature. This expression does not take into account the series resistance of the devices. The series resistance is a function of geometry, material resistance and contact resistance. Taking the series resistance, r_s, into account, we may write the diode voltage as

$$V_d = V - Ir_s \qquad (4.11)$$

where V is the applied voltage to the device.[26] The series resistance term in Eqn. (4.11) accounts for the downward curvature of the data shown in the forward bias region of Figure 4.8.

The conductance of the diode is defined as $g_d = dI/dV$. Using this expression and Eqns. (4.10) and (4.11), it is straightforward to show that

$$\frac{I}{g_d} = \frac{nkT}{q} + Ir_s \qquad (4.12)$$

which is a convenient form for determining the series resistance of the device. When I/g_d (= I dV/dI) is plotted versus I, the resulting curve is a straight line with slope of r_S and intercept of nkT/q. Figure 4.10 is a plot generated from data measured on one of our n^+-p junction diodes. The estimated series resistance of the diode obtained from a regression of I/g_d vs I is 15.37 ± 0.11 kΩ. The R^2 for the regression of the diode in Figure 4.10 is $R^2 = 0.999$. This high series resistance is due to both the contact spacing on the p side of the junction as well as the relatively low doping level of the p-side of the junction. This value is extremely large. Typical pn junction diodes have r_s values of a few ohms. r_s is very high for our devices because the carrier concentration of the p-type is material is so low, and the aluminum contact pads is set so far from the actual junction.

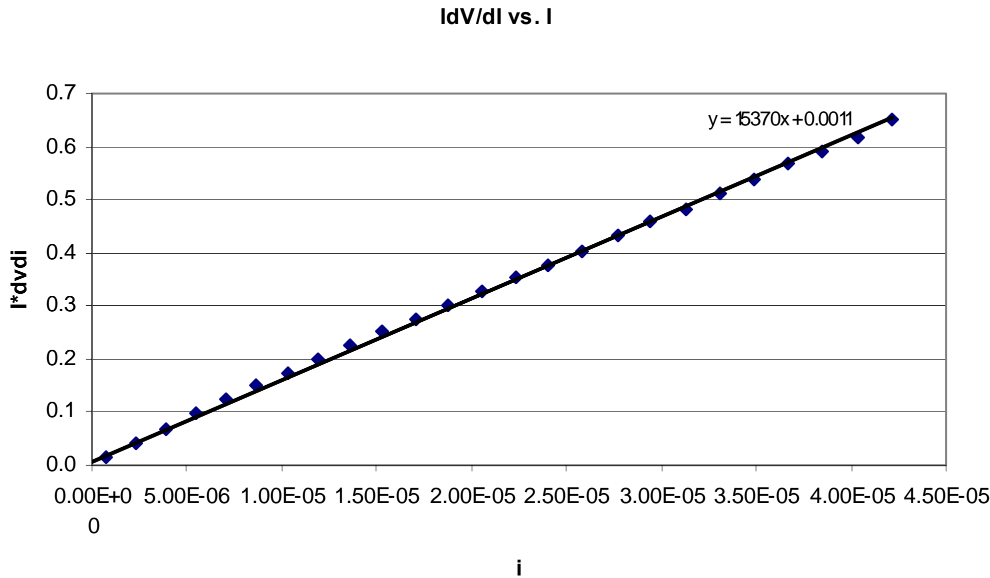


Figure 4.10 Plot of IdV/dI vs. I for a diode. The linear regression fit to the data is also shown.

For these data, we find n = 0.27 ± 0.12. This range does not include the allowed range of $1 \leq n \leq 2$ and is likely due to unidentified systematic errors. Thus we are unable to derive a realistic value for the ideality factor of our diodes due to the very large value of r_s. The only methods possible to reduce this error is either to redesign the maskset to reduce the distance from the aluminum contact pad to the junction or to dope the p side of the junction more heavily.

4.4.4 nMOSFETs

The nMOSFETs created in our process are made by doping two n-type wells in a p-type substrate, growing a 40 nm gate oxide, and evaporating aluminum contacts for the drain, source, and gate, as shown in Figure 4.11. The gate oxide thickness is monitored using a Filmetrics F-20 thin film measurement system.[27] There are 20 FETs on each wafer, with varying channel lengths and widths. The details of this process have been given elsewhere[28]. As described there, channel lengths are between 100 μm and 250 μm. Typical channel widths are 500 μm to 6000 μm.

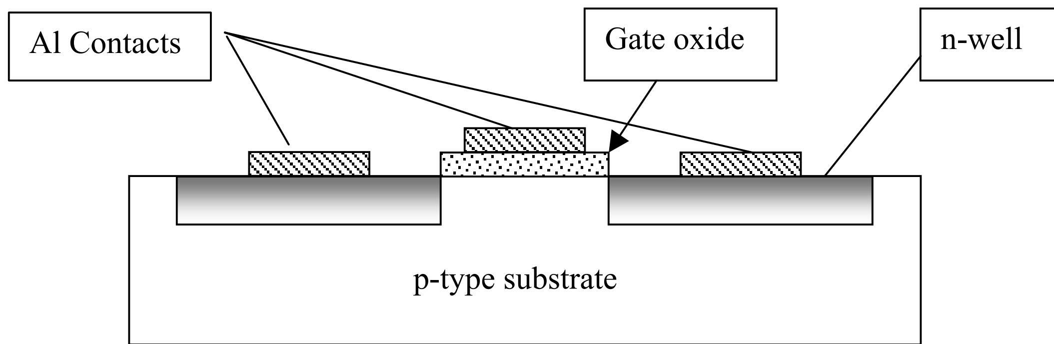


Figure 4.11 Layout of p-channel enhancement MOSFET.

To measure the I–V characteristics of the MOSFETs, a DC voltage is applied to the gate by the NI 6024E while the value of the drain-to-source voltage (V_{DS}) is swept per user defined limits and step values with the Keithley 2400. During this time, the drain current I_D is measured, also with the Keithley 2400. This loop is performed for six user-defined gate voltage values, giving the characteristic curves for the FET, as shown in Figure 4.12. These data are available for export.

Figure 4.12shows that the transistor has characteristics that are close to ideal, and that it is 'off' when the gate voltage (V_{GS}) is zero, i.e. the current is about 32 μA when V_{GS} = 0 V. The fact that the FET behaves as an enhancement mode device implies that the field oxide used as a physical barrier against the thermal diffusion was sufficiently thick so as not to allow leakage of phosphorus into the channel during the diffusion of P in the n-wells.

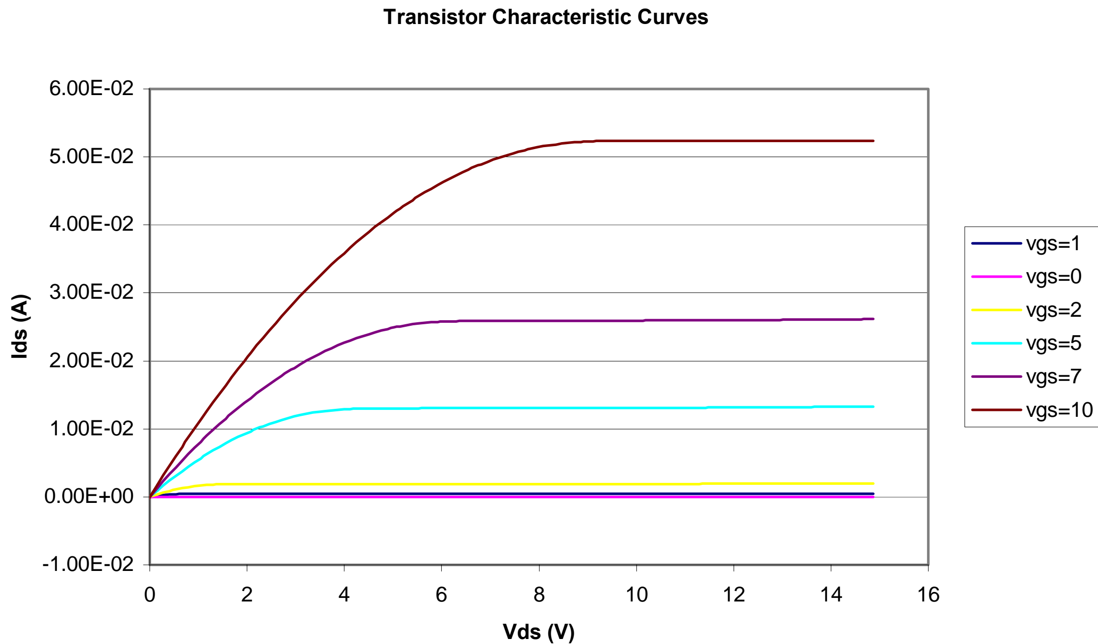


Figure 4.12 Characteristic curves for a MOSFET constructed in the lab. The dimensions of the channel are 250 µm long by 6 mm wide.

Although much can be inferred about the MOSFET fabrication process and operation from the curves shown in Figure 4.12, it is also beneficial to examine the threshold voltage characteristics of the device. In order to measure the threshold voltage of the FET, a small drain voltage is applied and the drain current is measured at each point of a user-defined gate voltage sweep.[12, 29]

The small drain voltage ensures that the device will operate in the linear region during the measurement. Figure 4.13 shows an example of the I–V curve resulting from this measurement for the same device shown in Figure 4.12. To determine the threshold voltage, a line is drawn tangent to the curve at the point of inflection (maximum slope). The point of inflection of this curve, found from the maximum in the derivative of the curve, is at V_{GS} = 1.53 V. The line tangent to the curve at this point, will intercept the x-axis at V_T. The tangent curve is also shown in Figure 4.13. For this particular device, the threshold voltage is 0.24 V. A propagation of error analysis shows that the standard error of V_T is ± 0.003 V for the data shown in Figure 4.13. The very small errors are due to the extremely good fit of the regression curve to the data (R^2 = 1.000). However, the analysis does not include any systematic errors.

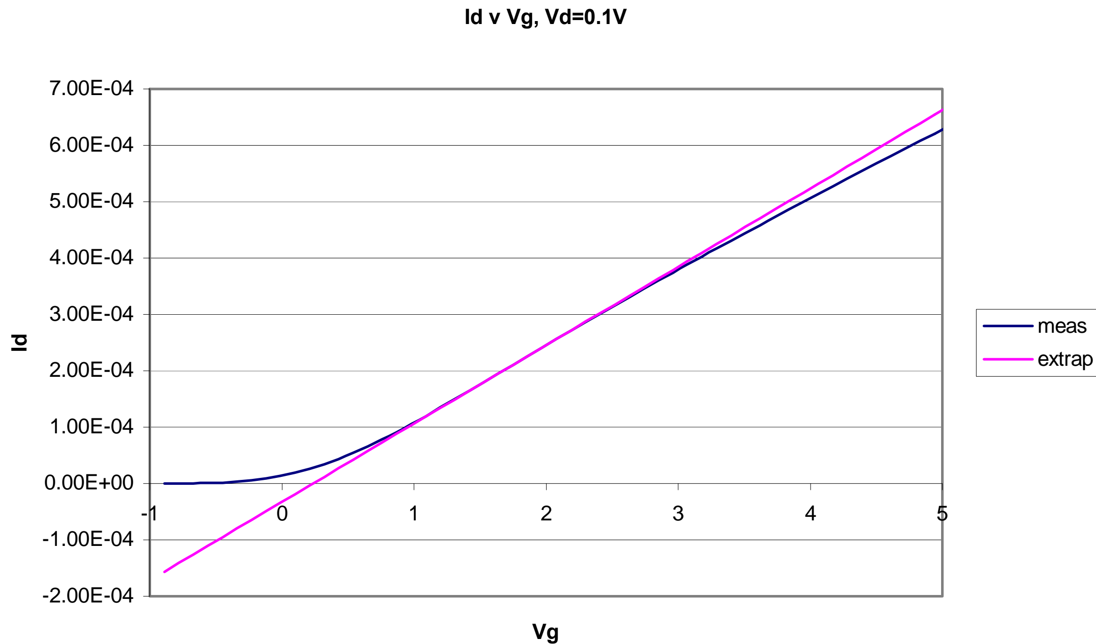


Figure 4.13 Threshold voltage measurement for the device shown in Fig. 11. A line is extrapolated through the point of inflection, tangent to the measured curve. The intercept of the extrapolated line with the x-axis is the threshold voltage, 0.24V.

4.5 Discussion

The semiconductor characterization tool developed here is seen to be capable of a wide range of measurements on simple devices created in our entry-level undergraduate teaching cleanroom. Our objective has to introduce students at an early stage in their scientific careers to the many exciting aspects of semiconductor fabrication and processing.[30] The measurements described here are simple enough to be described to and performed by such students. However, they are also sufficiently sophisticated that senior students taking our laboratory course as a terminal course in their undergraduate education may develop a greater appreciation of details described in more advance electronics courses.

We are exploring several upgrades that could be made to the wafer mask set in order to provide additional simple devices that can illustrate important pedagogical concepts. First, we plan to redesign the diodes to reduce the series resistance of the p-type material. This would allow a more realistic determination of the ideality factor, n. We are also examining ways in which we can create a test pad arrangement to allow students to measure the contact potential of the Al pads.[31] Although too complex for our early students, a determination of the properties of the gate oxide using C–V techniques[32] could be very interesting for more advanced students. We are testing our current wafers using a powerful Keithley System 86 Semiconductor Characterization System that has both a

Model 4200 SPA as well as sophisticated quasi-static and dynamic C–V capabilities. Once we have verified that such measurements make sense on our simple wafers it will be straightforward to add simpler and less sophisticated C–V measurement tools to the system described here.

4.6 References

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5 Recommendations for Future Work

Although this research provides not only a process for the fabrication of devices in the Whittemore facility, it also provides a somewhat optimized process at that. However, there are a multitude of opportunities both for further optimization of the process and for a broader knowledge of the area of semiconductor devices. The following recommendations provide areas of the process that are still not fully characterized. The understanding of these aspects of the process would greatly increase the yield and quality of the devices fabricated in this facility.

1. The current maskset used in this process is a simple four-mask set with 100 micron resolution. Since the completion of the bulk of this research, the possibility for the reduction of the line-wdth to submicron has arisen. The reduction in feature size would allow for more efficient use of the material as well as exploration into the questions that arise with sub-micron feature sizes.

2. Throughout the process of this research, not work was done concerning the p-type doping of the silicon. The MicrON center has the capability to dope the wafers with Boron use the solid-source technique. This doping would allow for the creation of CMOS devices as well as the overall reduction of resistances in diodes and MOSFET structures. As shown in this thesis, the diffusion of materials is often difficult to characterize and model. It is therefore recommended to explore the aspects of boron diffusion into silicon, including the diffusivity and sheet resistance parameters.

3. Although the method of doping has been sufficiently characterized for this set of design tools, no work was done to determine optimum levels of doping for the devices created. It is recommended that research be done in engineering device performance by varying processing parameters to achieve predetermined dopant levels within the crystal.

4. The semiconductor parameter analyzer provdes limited characterization of the silicon. With several small modifications to the software and toolset, a greater set of tests could be achieved. The current system performs a sweep test to measure the sheet resistance of the material while NSTA standards require only a two-point measurement. Changing this test would increase the efficiency of the system. A quick method to gain an understanding of the dopant levels in the near-surface region of the wafer is to measure the C-V properties of well-defined structures. This would eliminate the need for SIMS profiling, which is not possible to perform in our facility Lastly, incorporation of these test results into a database would allow for statistical analysis the process.

6 Vita

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Personal History

Born in Las Vegas Nevada, son of a United States Air Force Officer. Raised mostly in Virginia, with a four year stay in Belgium.

Educational History and Degrees Earned

B.S. in Electrical Engineering earned in 2000
M.S. in Materials Science and Engineering earned in 2002
Ph.D. work to begin in January 2003 in Materials Science and Engineering