Chapter 3. Thermomechanical reliability of the Dimple Array interconnect

3.1 Significance of reliability in solder area array packages

Power electronics devices and modules are prone to harsh environmental conditions during their service time; these include thermal and power cycling, shock and vibration, and corrosion. To answer the question of whether a technique will ultimately be accepted, reliability is one of the most important considerations. Reliability is the ability of a device to fulfill its intended function in terms of a specific period of time. The basic tasks for reliability engineering are to raise the level of understanding of various factors that will affect the reliability of a device, and to improve the service life of the product by giving solutions based on the obtained knowledge. The factors influencing reliability cover a wide range of internal and external factors, such as (to name a few) materials, geometric dimension, defects, processing, load patterns, temperature, etc.

There are two major aspects of reliability in power packaging: die-attach reliability and the interconnect reliability. The die-attach is common to a wide range of power packages, from discrete device package such as SO-8 and TO-247, to power MCMs. The basic function of the die-attach is to conduct heat from the bottom of the chips to the heat sink or the ambient. In many applications, the die-attach also serves as an interconnection between device electrodes, such as the collector and the circuit. Large-area solder bonding is commonly used for the die-attach between device and lead-frame or DBC substrates. Numerous studies of solder-attach fatigue failure due to cycling temperature loads and mechanical loads from the mounting have been reported [99,100,101,102,103,104].

The interconnect reliability of power packages mainly involves wire bond failure [105,106,107,108] or area array solder joint failure. Failure of the wire bond is mainly caused by the local CTE mismatch between aluminum wires and the silicon, although

ultrasonic rubbing may induce cracks in the silicon. The failure in area array solder joints is caused by weak adhesion between the under-bump metallization (UBM), local CTE mismatch between the solder and the silicon, and global CTE mismatch between the interconnect substrate (DBC or copper) and silicon. When a temperature swing is imposed, these CTE mismatches cause a complex state of stresses and strains. Concentration of these stresses and strains results in various failure modes, such as voiding, crack initiation and growth, delamination, and rupture of solder joints.

Trends towards the cost-performance requirement of electronic products have created a growing need for significantly improved thermal performance and package reliability. The conventional controlled collapse bonding (CCB) of flip chip solder joints raises concerns in terms of high stress/strain concentration at the silicon/solder interface. The DAI technology, as stated in previous chapters, has the potential to reduce these stress/strain concentration at this interface, and can thus improve the reliability of the solder joints.

The objectives of the reliability study of the DAI technique are to:

- Define design weaknesses by inducing stress under a variety of operating conditions;
- Obtain failure data under accelerated power or thermal cycling test condition; and
- Analyze failure mechanisms with the aid of FEM analysis.

3.2 Reliability evaluation methods

3.2.1 Thermal cycling test

The thermal cycling test has been standardized by JEDEC (temperature cycling JESD22-A104-B) [109]. This test examines the resistance of components to mechanical stresses induced by alternated high and low temperature extremes. The test is normally conducted in either single- or dual-chamber temperature cycling equipment. In the first choice, the samples are placed inside a stationary chamber, where hot or cold air circulates by a system fan. Depending on the cooling rate required, liquid nitrogen or a boost heater can be used to speed up the cooling or heating process. In the dual-chamber test, one chamber

is kept at a high temperature and the other is kept at the low extreme. Samples are transferred from one chamber to the other to achieve a fast cooling/heating rate. Figure 3.1 shows the temperature cycling profile specified by JEDEC.

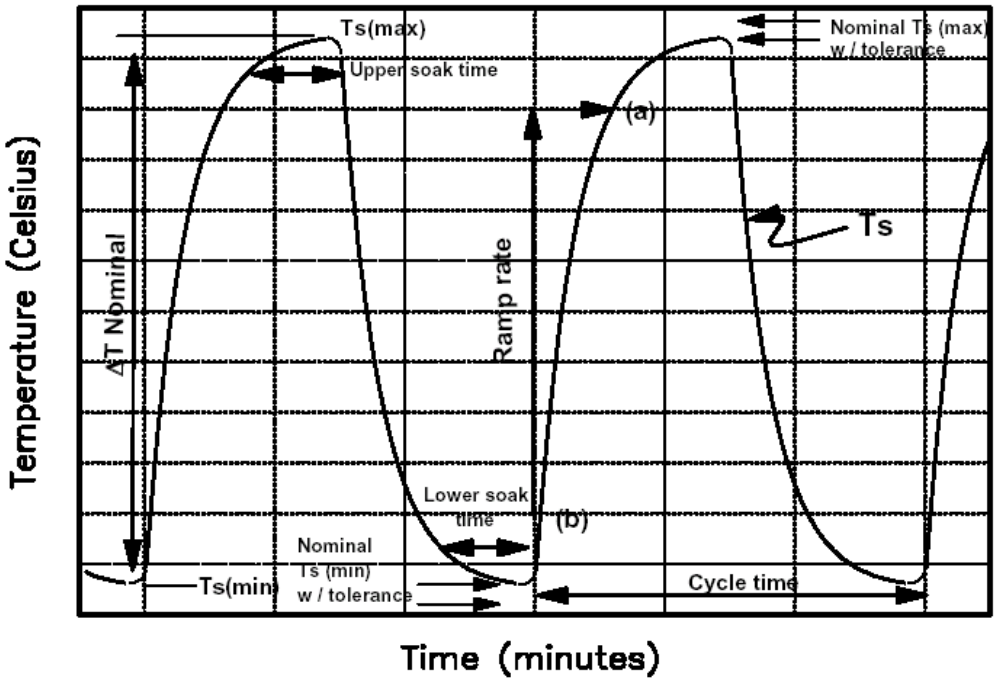


Figure 3.1 Temperature cycling profile specified by JEDEC.

The soak time and cycle time are regulated in a selection of ten test procedures. In this investigation, test procedure B has been used. This procedure describes a test condition from –55^{o}C to 125^{o}C. The soak time has been chosen to be five minutes at temperature extremes with a cycle frequency of one cycle/hour.

3.2.2 Power cycling test

Due to the highly demanding requirement for power module reliability, power cycling capability is seen as one of the most important aspects of reliability performance for applications such as the power train. The definition of power cycling in JEDEC standards (EIA/JESD22-A105-B) is less detailed. Although it is suggested that the devices be alternately cycled five minutes on, five minutes off, much of the research work in industry and universities did not follow this condition. Indeed, the purpose of power cycling is to "simulate worst case conditions encountered in typical applications" [110].

Therefore, due to the difference in the nature of applications, the worst case conditions are different, and thus the parameters of power cycling, including the setup of the heating or cooling method, can be very dissimilar.

Held, et al. [111] carried out a power cycling test using 300A/1200V single-switch IGBT modules. He used three medium temperatures Tm of 60, 80, and 100°C, and a ΔT_j of 30 to 80K. The current load of the test was between 240 and 300A, with ton = 0.6 to 4.8s, and t_{off} between 0.4 and 5s. Water-cooled heat sinks were used, and the failure criterion is a 5% increase of V_{CE}. Figure 3.2 shows the power cycling test circuit used by Held, et al.

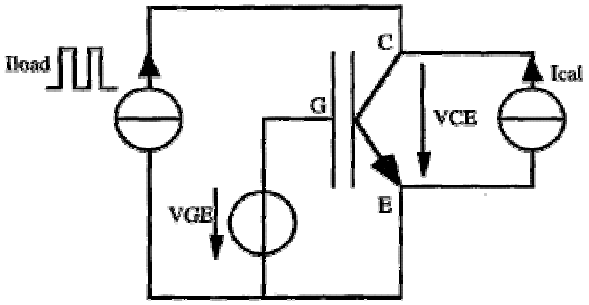


Figure 3.2 Power cycling test circuit for 1200V, 300A single-switch IGBT device.

Morozumi, et al. [103] used a power-on time of two seconds with an 18-second interval. The temperature swing ΔT_j was from 50K to more than 110K. The IGBT modules were mounted on an air-cooled heat sink. V_{GE}, V_{CESAT}, and I_{CES} were monitored. In the work of Hamidi, et al. [105], the power cycling test conditions were: ton = 0.9s, toff = 1.3s, ΔT_j is about 60K, and a maximum junction temperature T_{jmax} of between 105°C and 125°C. The base-plate temperature swing ΔT_c was about 17K and the maximum base-plate temperature T_{cmax} was between 60°C and 80°C. A collector current of 230 to 250A was pushed through the module during the on-state. The failure criteria were a 5% increase of V_{CESAT}, a 20% module thermal resistance, or gate emitter short, whichever occurs first. In his experiment, only the change in V_{CESAT} was observed due to wire bond degradation. In the work of Scheuermann, et al. [112], the power cycling test was performed on SkiM3 modules, and those test conditions are given in Table 3.1.

Table 3.1 Power cycling test parameters used by Scheuermann, et al.

ΔTnom [K]	Tj,min [°C]	Tj,max [°C]	ton [s]	toff [s]	I [A]
110	40	150	≈ 35	≈ 11	80
80	40	120	≈ 23	≈ 5	72
30	85	115	≈ 0,6	≈ 0,7	200

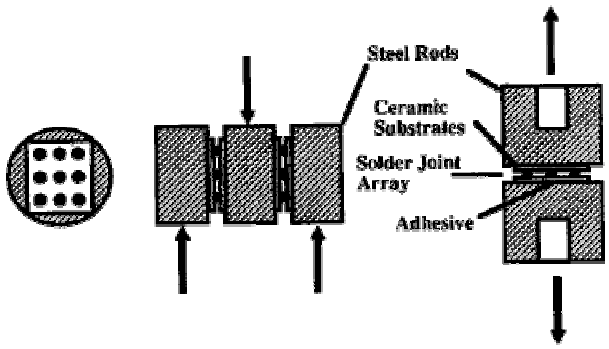
Schuetze, et al. [2,113] used a power cycling test condition of approximately one second/cycle with a failure criterion of a 5% increase of saturation voltage. The three test points for ΔT_j were: 50K, 75K and 125K. In addition to the power cycling test, which activates wire bond lift-off failure, they performed "thermal cycling" that accelerated the failure of solder-attach layer between the DBC substrate and the base plate by alternating the base plate (often referred as the "case") between two temperatures. The thermal cycling cycle time is about two to six minutes with a failure criterion of a 20% increase in thermal resistance. The test conditions for the thermal cycling were: ΔT_j = 80K, with one set of experiments carried out at T_{min} = 20°C and the other set of experiments at T_{max} = 100°C.

It is clearly shown that among the large amount of work in power cycling tests on power modules, the implemented methods differ from one source to the other. Based on the target mechanisms of interest, the power cycle time can be very short, i.e., less than ten seconds for wire bond lift-off failures, or a longer cycle time of a couple of minutes for solder attach failures. There is essentially no standard. It is also interesting to notice that these tests generally use a 5% increase of V_{CESAT} as an indicator of wire bond lift-off, while the 20% increase of thermal resistance is for solder-attach failure.

3.2.3 Mechanical test

Mechanical tests include the shear test, tensile test, twisting test, and mechanical cycling tests (cyclic bending). Mechanical cycling tests are frequently reported because they can simulate the thermal mismatch fatigue [114,115,116]. The three-point and four-point bending tests are two common testing methods in this category. This type of tests offers almost unlimited acceleration in strain and frequency. They are mostly used to study the

reliability of area array solder bumping packages, such as flip chip, BGA on PWB, etc. Cautions in using this method are that the complex behavior of solder at different temperatures is not considered, and that the introduction of alien failure modes causes difficulty in bridging the results with real operating conditions [117]. Figure 3.3 shows the test principles for shear and tensile tests [118].



(a) (b) (c)

Figure 3.3 Mechanical shear and tensile test: (a) test sample; (b) double lap shear configuration; and (c) tensile configuration.

3.3 Failure analysis methods

3.3.1 Scanning acoustic microscopy (SAM)

The SAM is a non-destructive inspection method sensitive to defects beneath the surfaces of packages. A SAM scan sends high-frequency (10MHz to 200MHz) ultrasound waves to the sample. The sound waves are reflected when they encounter layers or interfaces with different acoustic impedances. Therefore, SAM is capable of detecting voids, cracks and delaminations within packages. The percentage of voiding in large area soldering for power modules, for example, can be detected and calculated from SAM scanning. Common scan modes of a scanning acoustic microscope are A, B and C-scans.

With C-SAM (C-mode scanning acoustic microscopy) an ultrasonic transducer alternately sends focused pulses into the samples and receives reflected signals while scanning across the sample. The reflected signals are filtered by an electronic gate to capture features at desired depths according to the time at which the echoes are received.

Images can then be created in tens of seconds by correlating these signals and the positions of the transducer [119]. Figure 3.4 shows an example by He, et al. [120] of C-SAM monitoring of crack initiation and growth in the solder-attach of silicon devices of different sizes on a copper base plate.

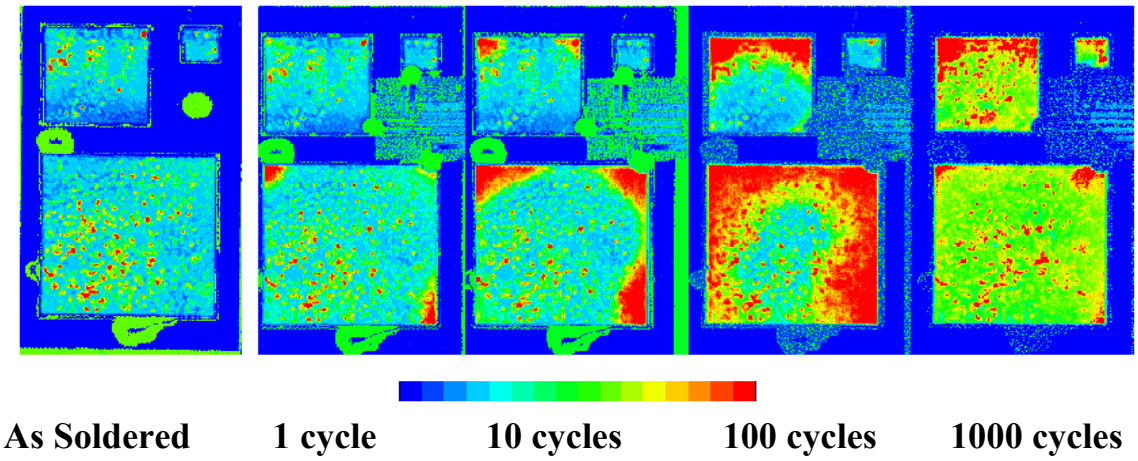


Figure 3.4 C-SAM monitoring of crack evolution in the die-attach of silicon devices.

The conventional acoustic imaging technique can be time-consuming and requires a degree of expertise in obtaining and analyzing results. Tomographic acoustic micro imaging (TAMI™) [121] offers layer-specific information with a much more simplified setup. TAMI provides a C-scan image of each layer, and up to 30 images within one scan. The capability to easily separate the interfaces of complex multilayer packages makes it easy to more clearly understand the failure modes [122]. Figure 3.5 shows the principle of TAMI scanning [122].

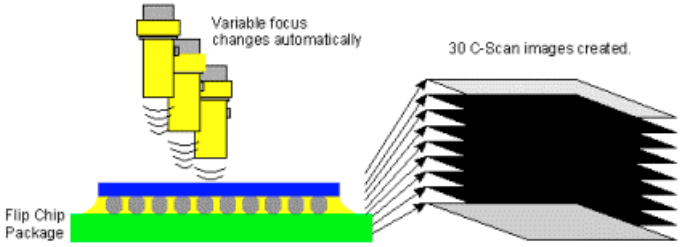
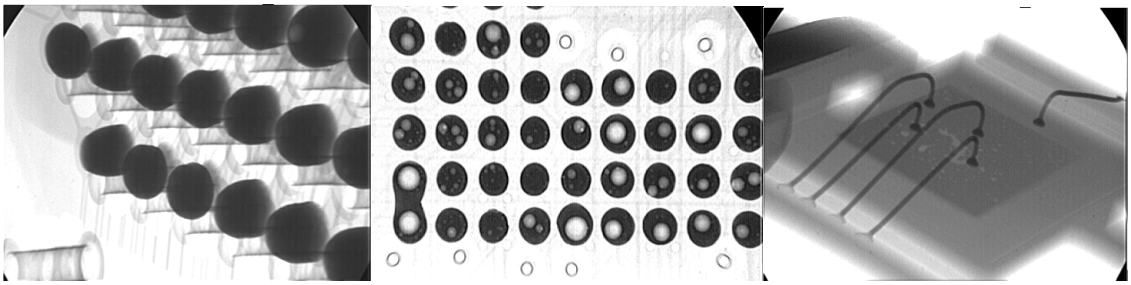


Figure 3.5 TAMI scanning principle
(reprinted with the permission of Sonix Incorporated).

3.3.2 X-ray inspection

X-ray is one of the emerging technologies for non-destructive testing and inspection of encapsulated electronic packages. Quality improvement can be made by accurately detecting flaws and defects such as solder voiding, bridging, solder ball alignment, etc. [123,124,125]. Figure 3.6 (a)-(c) shows the X-ray imaging of BGA array, BGA voiding and bridging, and wire bonds (scales of these photos are not available), respectively.



(a) (b) (c)

Figure 3.6 X-ray inspection of: (a) and (b) BGA packages; and (c) wire bond packages (all photos courtesy of X-Tek).

Having excellent performance in detecting voiding, X-ray inspection does have shortcomings. Conventional X-ray cannot pass through dense materials such as copper and lead. Therefore, in the case of cold solder joints (not connected to chip or board), X-ray is not able to identify the flaws [126].

3.3.3 Metallographic sectioning

Metallography provides a powerful tool for inspecting the microstructure of electronic components and material interfaces. Major steps include sectioning and cutting, mounting, planar grinding, polishing and etching.

Most metallographic samples need to be sectioned to the area of interest using abrasive cutting or diamond wafer cutting. The latter is a better approach for cutting electronic components because it causes less damage to the samples. Next, a mounting operation protects the specimen edge and maintains the integrity of a material's surface features. This step is done by encapsulating the specimen using castable mounting resins (acrylic resins, epoxy resins and polyester resins). Depending on the encapsulation depth of the

site of interest, a second sectioning may be needed. A subsequent planar grinding planarizes the sample cross-sections and exposes the exact area of interest. A sequentially decreasing grit/particle size of the silicon carbide abrasive paper is normally used. For electronic components that have multiple materials with various degrees of hardness, it is recommended that fine abrasives such as 400- or 600-grit SiC be used after sectioning to prevent brittle substrates such as silicon from cracking. A coarser-grit abrasive might produce more damage to the specimen than sectioning. Hard ceramic substrates (such as alumina) should be rough-polished with diamond lapping films to minimize edge rounding. For scanning electron microscopy analysis, polishing of the specimen using diamond or alumina fine powder is usually required. The particle size starts from 5 micron and 1 micron, and can be as fine as 0.1 micron. Ultrasonic cleaning is recommended after every particle-size polishing to thoroughly clean the surface because residual powder from the last polishing step may contaminate the next level of polishing mixtures and cause scratches on the sample surfaces. And last, selective etching can be used to inspect the microstructural features such as grain boundaries and phases. The purpose of etching is to optically enhance these microstructural features. Etching selectively exposes these microstructural features based on composition, stress or crystal structure. The most common technique for etching is selective chemical etching, and numerous formulations have been used over the years [127].

Optical microscopy analysis is often performed after metallographic sectioning of samples. Most solder joint cracking and underfill delamination can be observed by using an optical microscope.

3.3.4 Scanning electron microscopy (SEM)

Modern scanning electron microscopes have resolutions of 40 Å and large depths of focus at magnifications approaching 50,000x [128]. Specimens must be electrically conducting. A beam of electrons is excited from a small tungsten filament. Figure 3.7 shows the interaction of the electron beam and the sample [129]. Either secondary electrons or primary backscattered electrons can be used to extract topographical

information. The backscattered electron scanning mode can also be used to identify phases with elements of different atomic numbers.

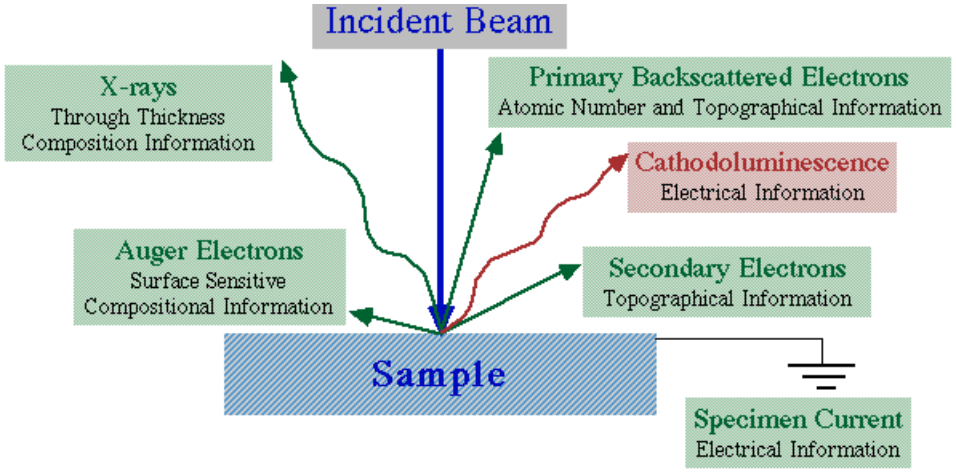


Figure 3.7 Electron/specimen interactions in SEM
(reprinted with permission of Professor Scott Chumbley, Iowa State University).

3.4 Reliability testing and failure analysis of DAI and CCB interconnects

In this research, the reliability of the Dimple Array solder joints is experimentally studied using the thermal cycling test and the power cycling test. Throughout these tests, the Dimple Array solder joints are compared with the CCB solder joints.

3.4.1 Thermal cycling test

The thermal cycling (or temperature cycling) test has been the major accelerated testing method used to study solder joint fatigue. The thermal cycling test accelerates solder joint fatigue through alternating the temperature between cold and hot extremes. Dramatic plastic deformation occurs during the temperature transition, and creep occurs in all stages of the test. Important test parameters include the temperature extremes, cooling and heating rate, and soak/dwell time.

Objectives of the thermal cycling test are to:

1) Collect and compare reliability data of DAI and CCB solder joints; and
2) Investigate failure mechanism for both types of solder joints.

3.4.1.1 Experimental procedure

In order to track fatigue damage such as crack growth, the best approach is to monitor solder joint resistance at intervals of thermal cycling. However, all the solder joints are connected in parallel between the conductive chip metallization and the metal sheet, which renders the change of each individual solder joint immeasurable.

In order to measure individual solder joint resistance, silicon wafers with UBM were solder-bumped to perform this test. The wafer was patterned to have a number of conductive traces. Each trace will connect to a solder joint. Dimpled copper sheets, each of which is dimensioned 8 by 10 mm, are used to connect six conductive traces on the wafer. For CCB solder joints, a flat copper sheet is used. Figure 3.8 shows a schematic of the test sample and the method to measure the resistance of individual solder joints.

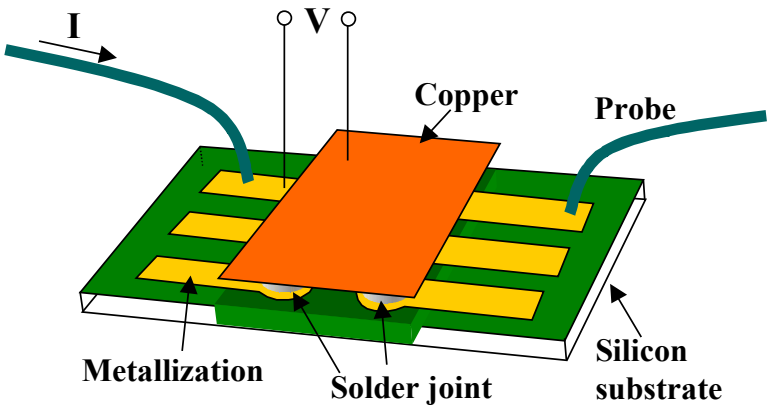


Figure 3.8 Schematic of the resistance measurement for thermal cycling samples.

3.4.1.2 Sample preparation for temperature cycling

Processing of the silicon wafer is carried out as follows: First, a silicon wafer (N type, resistance 1-10ohm-cm) is placed into the sputter chamber. Aluminum is first sputtered onto the wafer to form the base of the metallization. This layer is about 1 μm. Then a vacuum baking is performed using a ceramic electrostatic chuck. This step is crucial because adhesion of the metal to the wafer depends heavily on the quality of the Si/Al adhesion. A phase diagram of Al-Si (Figure 3.9 [130]) shows that an alloying process occurs at 577^{o}C between the Al and the Si. Experiments in this research have indicated that satisfactory adhesion is achieved with a temperature of no more than 300^{o}C and with

a ten-minute annealing duration. Next, Ni/V or titanium (0.1-0.3 μm, 5~15min) and copper (0.5 μm, ~25min) are deposited onto the wafer.

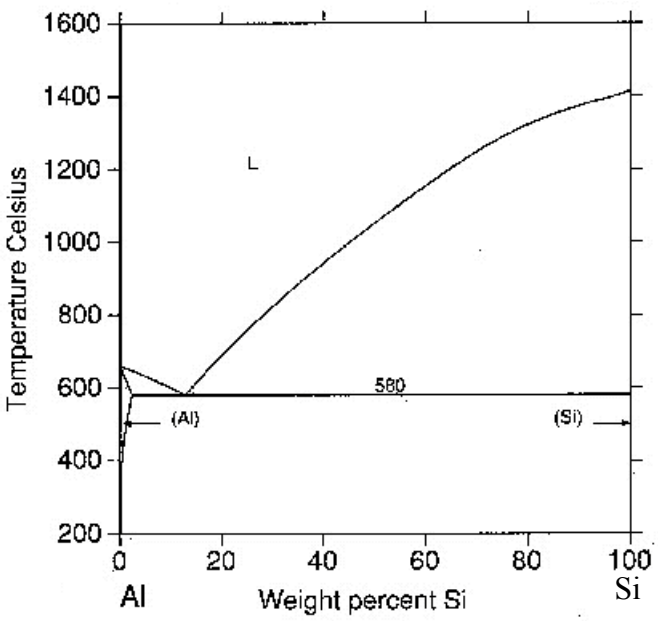


Figure 3.9 Phase diagram of aluminum and silicon.

Patterning of the solderable metal layer is done using the AZ P4400 positive photoresist (from Clariant). After UV light exposure, the photoresist pattern is developed using AZ 400 1:4 diluted developer. The exposed metals are etched using ammonium persulfate, a slow etchant for copper with excellent line-width definition and which is mild enough for most photoresist coatings. After etching, the resist is stripped off using acetone. Last, a thin layer of gold (0.1 μm) is electroless-plated onto the copper traces for improved wettability. For the CCB solder joints, a coating of a solder mask is needed for defining the solder joint opening area (ball-limiting area). A quarter of a metallized wafer is shown in Figure 3.10.

Copper interconnect flex sheets are prepared in 8 x 10 mm^2 format. For DAI samples, the copper sheets are stamped using a set of fixtures to create an array pattern of 2 x 3 dimples. For CCB samples, the ball-limiting region must be defined by using the solder mask to prevent solder ball collapse.

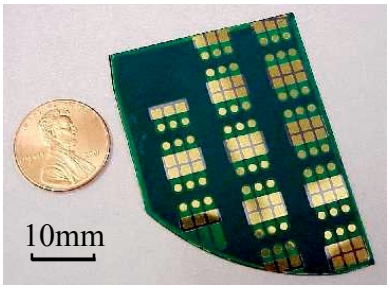


Figure 3.10 Metallized wafer with solderable patterns.

Next, solder paste is screen-printed onto the bond pad using a stainless-steel stencil. Then, the dimpled copper sheets are pick-and-placed onto each location and the wafer is sent to a five-stage belt oven for profiled temperature reflow. Residual flux around the solder joints is cleaned after solder reflow. Figure 3.11 shows a photo of the DAI samples.

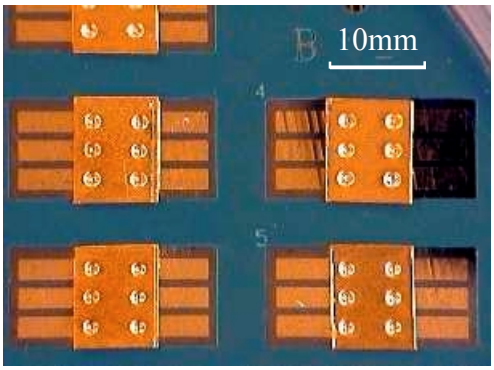


Figure 3.11 Thermal cycling samples.

A summary of test samples for thermal cycling is listed in Table 3.2.

Table 3.2 Summary of thermal cycling test samples.

	Pb37Sn63, no underfill	*Ag3.5Sn96.5, no underfill*
Dimple sample No.	48	21
CCB sample No.	48	42

The test equipment is the Tenney Junior Environmental Test Chamber, Model TUJR with a Watlow 942 controller. Boost heater and boost cooling are included. In this

investigation, JEDEC standard test procedure B has been used. This procedure describes a test condition from –55^{o}C to 125^{o}C. The soak time has been chosen to be five minutes at temperature extremes with a cycle frequency of one cycle/hour. Resistance change of the solder joints was monitored periodically at cycle intervals.

3.4.2 Power cycling test

The power cycling test has been well documented as an effective approach for evaluation of wire bond-related failures in power electronics modules [103,111,112]. A properly configured test procedure can impose a cyclic stress on the bond-to-silicon connection, therefore activating the main failure mechanism of bond wire lifting.

In the area array flip chip package, the source for strains and stresses within the solder joint is the global mismatch between different coefficients of thermal expansion of the copper interconnect and the silicon device, as well as the local mismatch between solder joint, copper interconnect and silicon. The goal of performing a power cycling test on the flip chip packages is to activate the main failure mechanism of solder joint fatigue.

Previous discussion in this chapter (Section 3.2.2) showed that test conditions for power cycling depend heavily on applications and the targeted failure mode. There are no universal/standard power cycling test specifications. Power cycle time can range from less than one second to minutes, and even longer. Although the eutectic tin-lead solder creeps even at room temperature, creep would not occur if the rate of strain or loading is too high [131]. Since the goal is to accelerate the failure mechanism of solder joint fatigue, the cycle time must be long enough that the solder creep contributes to the fatigue damage [132]. In this test, the cycle time is chosen to be one minute.

3.4.2.1 Power testing circuit and assembly

The power testing circuit is shown in Figure 3.12. Power diodes are packaged using either the Dimple Array or the CCB method and are connected in series with a switching device.

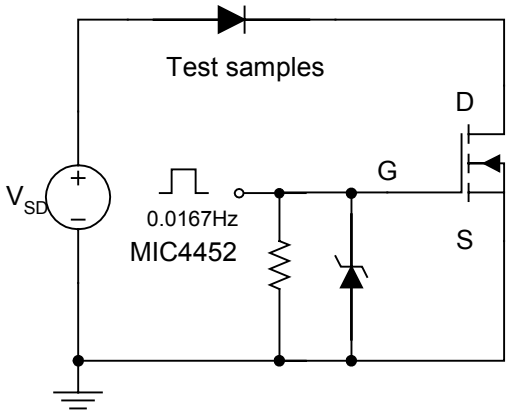
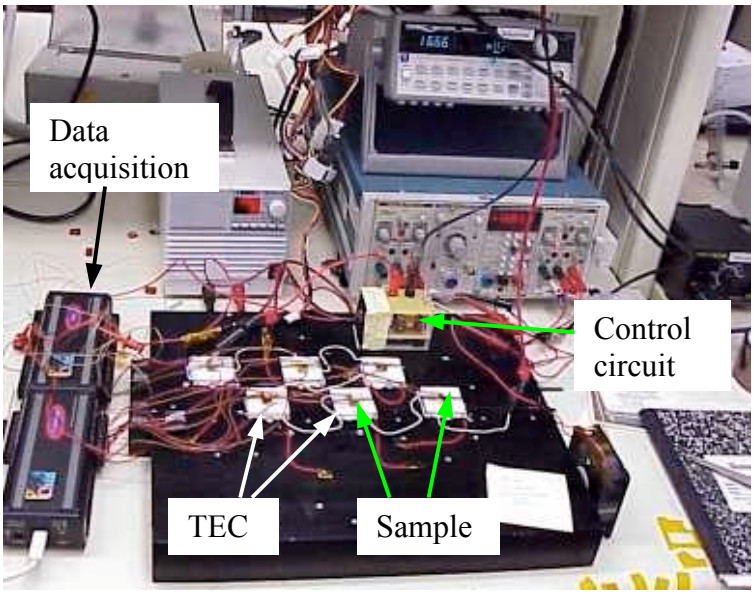


Figure 3.12 Power cycling test circuit.

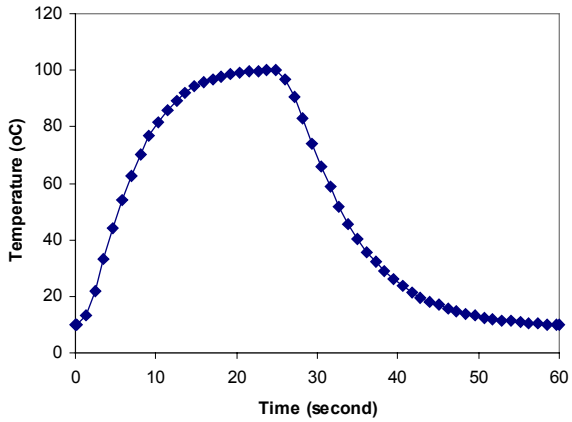
For the switching device, an IRFP044 HEXFET MOSFET is used, which has a current rating of 57A, voltage rating of 60V, and $R_{DS(on)}$ of 0.028Ω. IRFP044 is in a TO-247 package with an insulated mounting hole. In order to drive the IRFP044, a MICREL MIC4452CT non-inverting driver (TO-220) package is used (driving capability of up to 12A (peak) and wide operating range from 4.5V to 18V) to supply gate voltage and gate current through a gate resistor. In the power cycling setup, the input voltage was selected to be 10V for the MIC4452, and the square-wave with a frequency of 0.01667Hz (1 power cycle/min) is generated by a signal generator. The duty cycle is adjusted so that the on-time is 25 seconds and the off-time is 35 seconds, allowing for sufficient cooling of the sample to 10~15^{o}C.

To start the test, a flip chip area array-packaged test chip (power diode) is mounted on a thermal electric cooler (TEC) to provide active cooling of the package. The device is heated rapidly during the power-on period by using the MOSFET to control the flow of current through the device. During the power-off period, the device is cooled rapidly by the TEC. Depending on the current levels passing through the device and the TEC, the maximum and minimum temperatures of the device can be adjusted to a desired value. Once the preferred ΔT is obtained (measured using a thermocouple at the copper interconnect and read through a data-acquisition module), it will not be adjusted even if an increase of the maximum temperature occurs. The advantage of using the TEC is that

for compact flip chip packages it is very effective for cooling the device to below room temperature, therefore imposing a large temperature swing on the solder joints. Throughout the test, the on-voltage drop and the temperature of the device under test are measured in real time. The power cycling setup and a typical power cycling temperature profile are shown in Figure 3.13.



(a)



(b)

Figure 3.13 Power cycling test setup (a) and a typical power cycling temperature profile (b).

The period of a power cycle is 60 seconds, with 25 seconds for power-up and 35 seconds for cooling. The voltage signal measured is actually the diode's forward voltage drop plus

the voltage drop that occurs due to packaging resistance. Failure criteria are a 5% increase in forward voltage drop at rating current or a 20% increase in thermal resistance, whichever occurs first. Measurements must be taken at a constant temperature and at a constant current level, since the forward voltage drop of the test devices has a strong temperature dependency. Temperature dependency of the forward voltage of a typical diode device is shown in Figure 3.14.

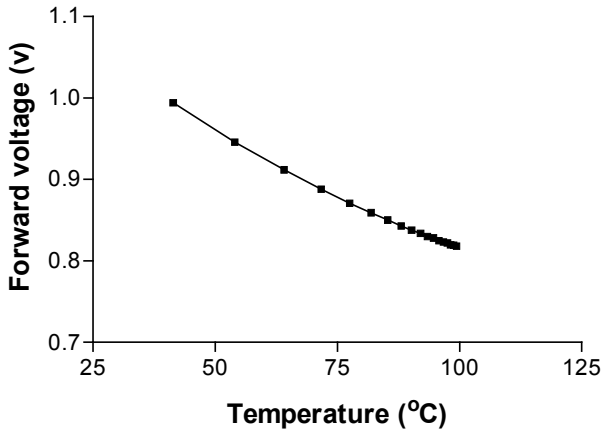


Figure 3.14 Temperature dependency of diode forward voltage.

3.4.2.2 Sample preparation for power cycling test

Since the power cycling test requires the device to have active self-heating, functional silicon dies are used. The IXYS DWEP 35-06 fast recovery epitaxial diodes, 6 x 6 mm sq. in size, and 0.5mm in thickness, are used. These devices have solderable UBM (Al/Ti/Ag) on both sides.

For Dimple Array packages, the processing is relatively easier. The diodes are first solder-attached to alumina DBC substrates using a higher-melting-temperature solder (eutectic tin-silver solder) reflowed at 240°C. Solder paste is screen-printed onto the devices through a stainless steel stencil with a thickness of 10 mil. Square copper sheets, cut at the same size as the silicon devices and laminated to ensure planarity, are then stamped with dimple patterns. The copper dimple sheets are then pick-and-placed on the tops of the silicon/DBC assemblies, which will go through a second reflow process.

For the CCB packages, due to the need for ball-limiting masks, a clean room process is added for both the silicon diode and the copper interconnect. The solder mask is first spin-coated on the devices or copper sheets with a subsequent 40-minute bake at 75^{o}C. Solder openings are then patterned on the devices and copper sheets by a UV exposure lamp. After being developed in a solder mask developer solution, the pieces are rinsed with water and post-baked for ten minutes. Finally, the devices and the copper interconnect sheets are ready for solder bumping. Again, using a stainless steel stencil, eutectic Pb/Sn solder is first screen-printed onto the copper sheets. In order to increase solder volume for a higher standoff height, an additional 30mil-diameter solder ball (still eutectic Pb/Sn) is added onto each pad. The copper sheet is then reflowed at 210^{o}C. Figure 3.15 shows a picture of the reflowed CCB copper interconnect before being attached to the devices.

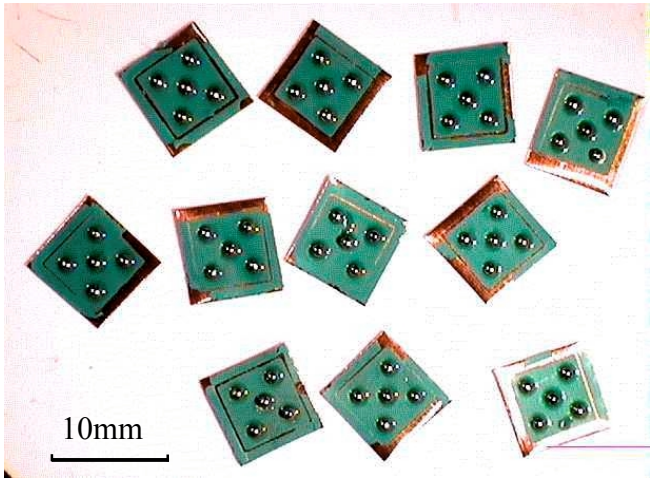


Figure 3.15 CCB copper interconnect with preformed solder balls.

On the device side, the same type of solder is screen-printed to the solder mask-defined pads. The copper interconnects populated with solder bumps are flipped and aligned with the solder paste on the devices. A second reflow completes the CCB process. After assembling both types of packages, some samples are underfilled using Loctite™ 3565 high-performance epoxy.

3.4.3 Failure analysis using metallographic cross-sectioning

Failed samples were metallographically cross-sectioned for optical microscopy and SEM examination. The preparation steps include the following:

- Sample mounting

- Mix Buehler Epoxicure Hardener (20-8132) 36:100 with Buehler Epoxicure Resin (20-8130). Adding a little more hardener can obtain a faster curing.
- Place samples with metal clip supports in the mounting cup.
- Fully stir the mixture but try to minimize air bubbles. Then slowly pour in the epoxy. If observing excessive bubbles, de-air the samples using a vacuum chamber before the cup gets warm.
- Usually it takes six hours or longer to cure the sample.

- Sectioning

- Mount the solid cylinder to a diamond saw.
- With continuous water drops, cut sample near the desired interface.

- Polishing

- Start with 320-grit (34.3 μm), and progress to 400-grit (22 μm), then 600-grit (14.5 μm) sandpaper. Note: No dry polishing, since it may crack the silicon.
- Cloth polishing with 5 micron (Al2O3 powder), 1 micron, 0.5 micron.
- After every fine-polishing step, use the ultrasonic bath to remove residual powders on surfaces.

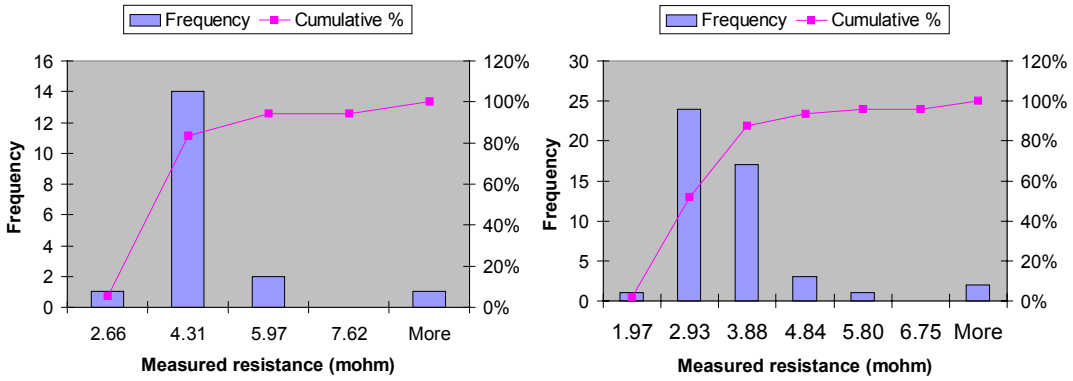
- Final attack etching (only needed to observe solder grain boundary)

- Mix 160 ml water, 40 ml NH_4OH, and 3 drops of 30% H_2O_2.
- Immerse for 30 seconds to one minute.
- Rinse, and air- or N2-dry.

3.5 Thermal cycling test results

3.5.1 Pb37-Sn63 solder

Solder joint integrity has been monitored using the measured resistance value of each joint. Resistance measurement is done using the four-point method. The histograms of the measured zero-cycle resistance for CCB and dimple solder joints are shown in Figure 3.16 (a) and (b), respectively. The zero-cycle resistance of the CCB is mostly around 4.3 mΩ, while for the Dimple Array solder joint it is about 3 mΩ. It must be pointed out that the measured resistance includes the resistance of both the solder joint and the solderable metallization traces on the silicon surface.



(a) (b)

Figure 3.16 Zero-cycle resistance histogram for (a) CCB and (b) DAI solder joints.

Normalized resistance, which is the measured value R divided by the resistance at zero-cycle R_0, can be used to compare the thermal cycling capability of the CCB and the DAI solder joints. Typical normalized resistance R/R_0 versus number of thermal cycles is shown in Figure 3.17. Most CCB solder joints display a drastic resistance increase after only 35 thermal cycles from -55 to 125^{o}C, while the dimple solder joint shows a much slower rate.

In addition, more than 20% of the CCB solder joints were found to have high zero-cycle resistance, although no zero-cycle opening is found.

These data are significantly different from those of the conventional (IC) BGA board-level and flip chips. In those tests, the first failure normally occurs after a few hundred cycles. This is mostly because of the large CTE mismatch between the silicon device and the copper interconnect (13 ppm/K) in contrast to the smaller CTE mismatch in the BGA (ceramic substrate to PCB board is about 7 ppm/K) and the flip chip package (silicon to ceramic substrate: < 5 ppm/K).

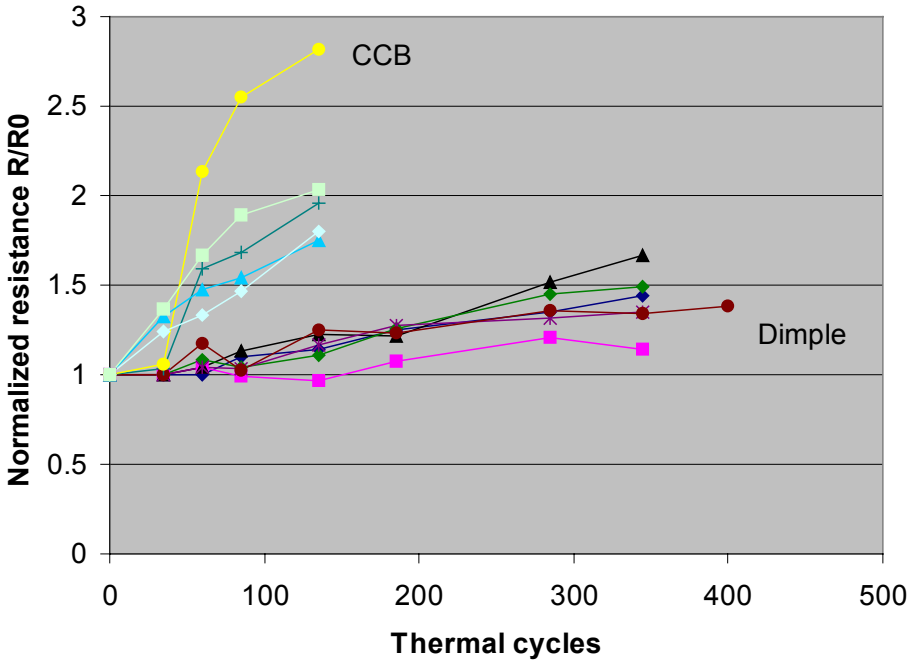


Figure 3.17 Typical normalized resistance R/R_0 versus number of thermal cycles.

Figure 3.18 shows the cumulative fail plot registered by a 20% resistance change. Data points are fit with nonlinear regression, it is the one-phase exponential association method (expressed by equation: $y = y_{\max}(1-\exp(-kx))$). Significantly higher life for Dimple Array solder joints is found as compared with CCB solder joints. If this criterion is taken as the judgement of the time-to-crack initiation, then the mean time of fatigue crack initiation for Dimple Array solder joints is about 110 cycles for this test condition. More than 50% percent of the CCB solder joints were found to have a resistance change of 20% after eight (extrapolated) thermal cycles. About 30% of the CCB solder joints

open circuits after 135 cycles, and roughly 40% of the dimple solder joints open circuits after 345 cycles.

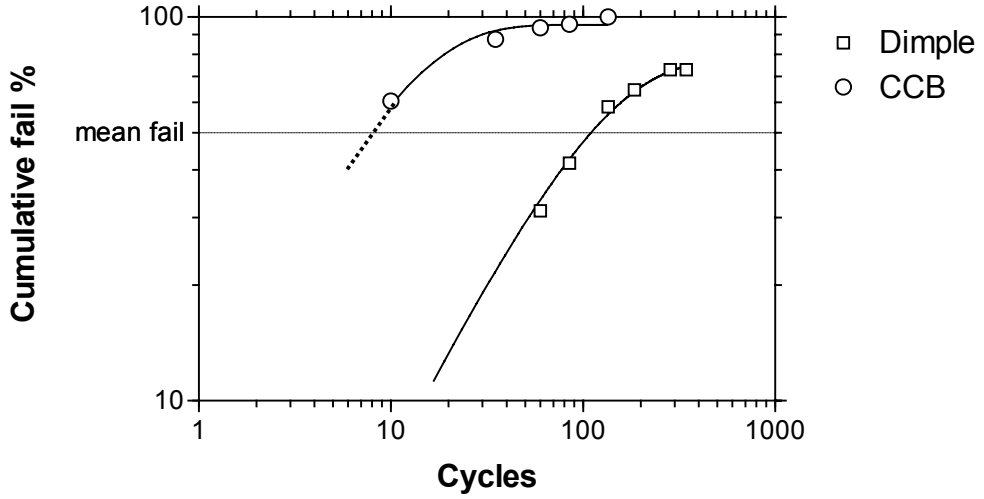


Figure 3.18 Cumulative fails based on a 20% increase in resistance, using Pb37 solder.

The cumulative fail plot of the test samples, based on 50% increase in initial resistance, is shown in Figure 3.19. The mean life-to-fatigue failure for the CCB is 23 cycles, and is about 185 for the Dimple Array solder joint.

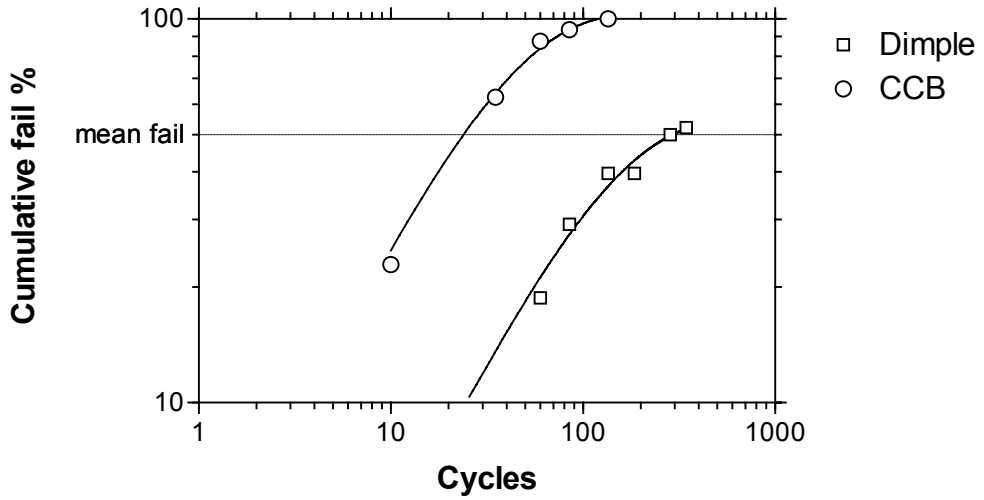
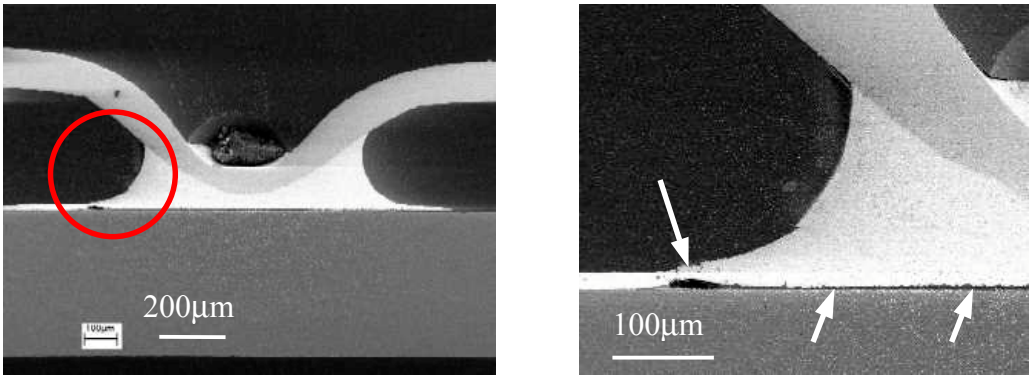


Figure 3.19 Cumulative fails based on a 50% increase in resistance, using Pb37 solder.

In the failed dimple solder joint samples, the solder-to-silicon interfaces show delamination. Figure 3.20 shows a typical failed sample and the enlarged view of the left

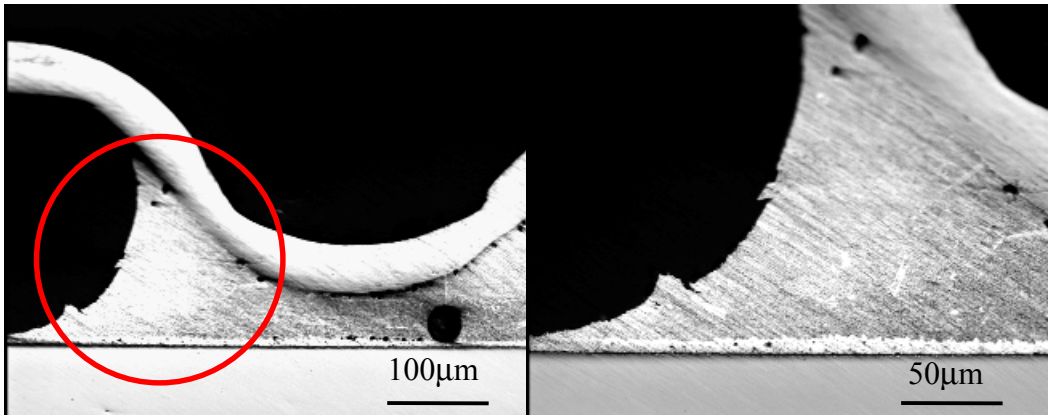
side. The solder joint was measured to be 2.48mΩ at zero cycle; and after 285 cycles it was 3.78 mΩ. Arrows point to the delamination regions.



(a) (b)

Figure 3.20 (a) A dimple solder joint that failed at 285 thermal cycles; and (b) the zoomed-in view of the circled region.

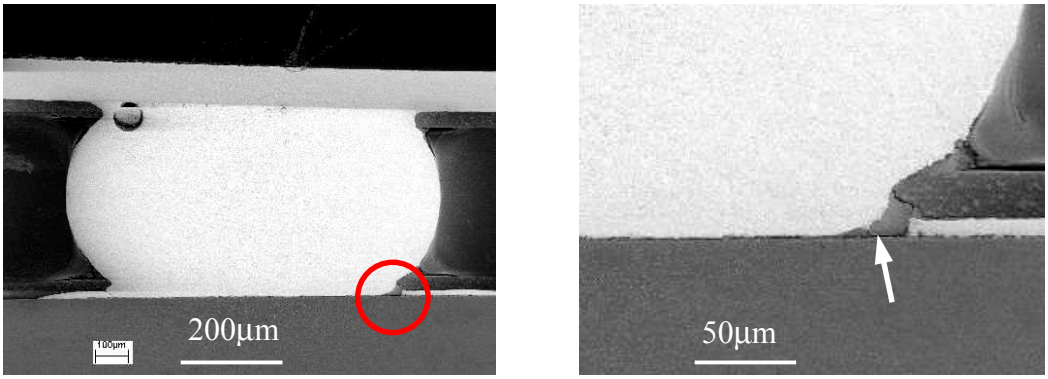
Figure 3.21 shows a dimple solder joint that sustained 400 cycles with little change in measured resistance.



(a) (b)

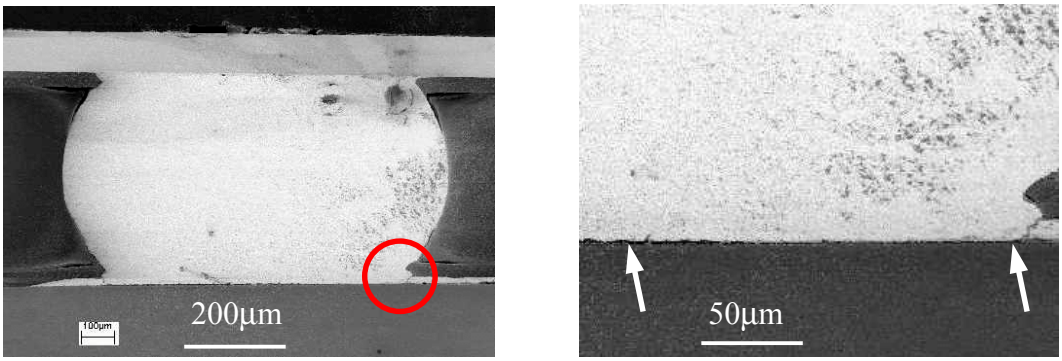
Figure 3.21 (a) A dimple solder joint after 400 thermal cycles; and (b) the zoomed-in view of the circled region.

In the failed CCB solder joints, at both the solder/pad openings and solder-to-silicon interfaces, delaminations were found. Figure 3.22 shows the solder/pad opening and Figure 3.23 shows a typical solder delamination image. The solder/pad opening occurs at the corner of the solder joint, where the stress/strain concentration is highest.



(a) (b)

Figure 3.22 (a) A typical CCB solder joint that was found open at 135 cycles; and (b) the zoomed-in view of the circled region.



(a) (b)

Figure 3.23 (a) A CCB solder joint that failed (50% up) at 135 cycles; and (b) the zoomed-in view of the circled region.

3.5.2 Lead-free Ag3.5-Sn96.5 solder

Lead-free solder Ag3.5-Sn96.5 displays a behavior very different from that of the eutectic Sn-Pb solder. Figure 3.24 shows the typical normalized resistance trend versus the number of thermal cycles for both Dimple and CCB solder joints. Essentially no difference can be identified.

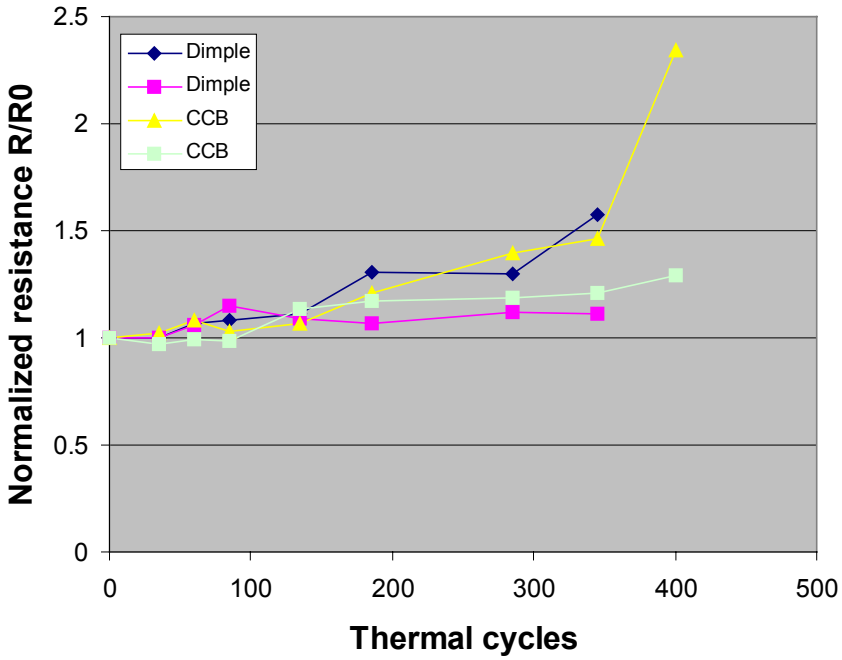


Figure 3.24 Typical resistance change of the Ag3.5-Sn96.5 Dimple and CCB solder joints.

Figure 3.25 shows the cumulative fail in percent for Dimple Array and CCB solder joints, based on a criterion of a 20% increase in resistance. Since the data points do not fit to a simple non-linear regression curve other than polynomial equation, they are connected by a straight line between them. It is shown that the first sign of resistance increase appears at 35 cycles in CCB solder joints, but not until 60 cycles for dimple joints. However, there is essentially no difference in mean failure (50% of samples) for both sets of solder joints. On the other hand, if using a failure criterion of a 50% increase in resistance, the CCB solder joints slightly outperform the dimple solder joints (Figure 3.26).

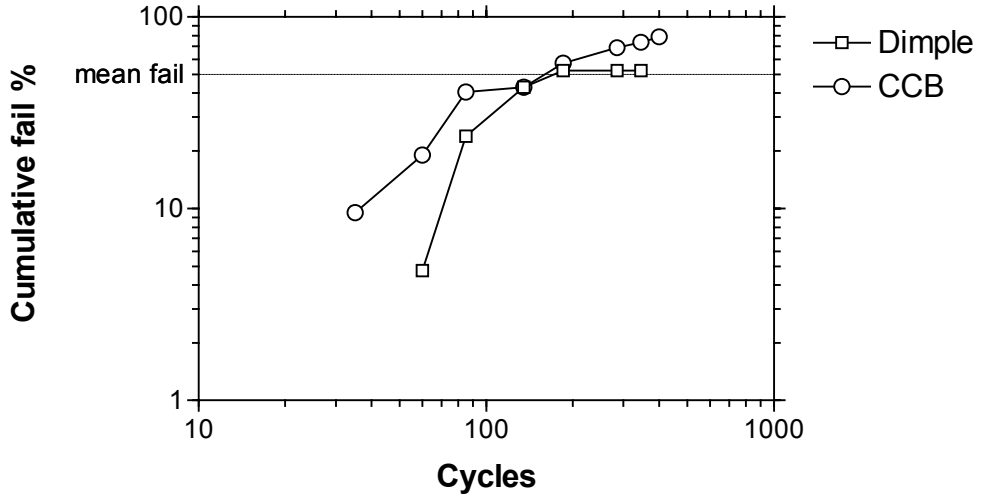


Figure 3.25 Cumulative fails based on a 20% increase in resistance, using Ag3.5-Sn96.5 solder.

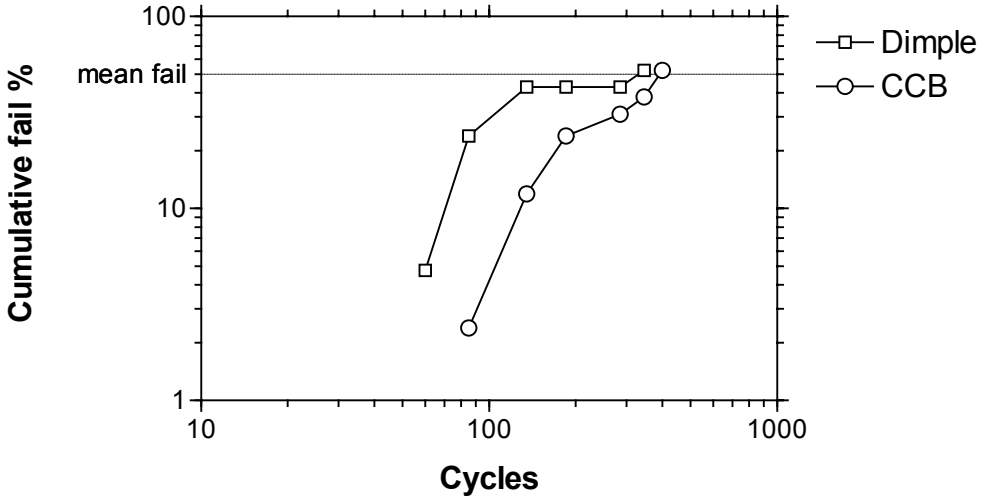
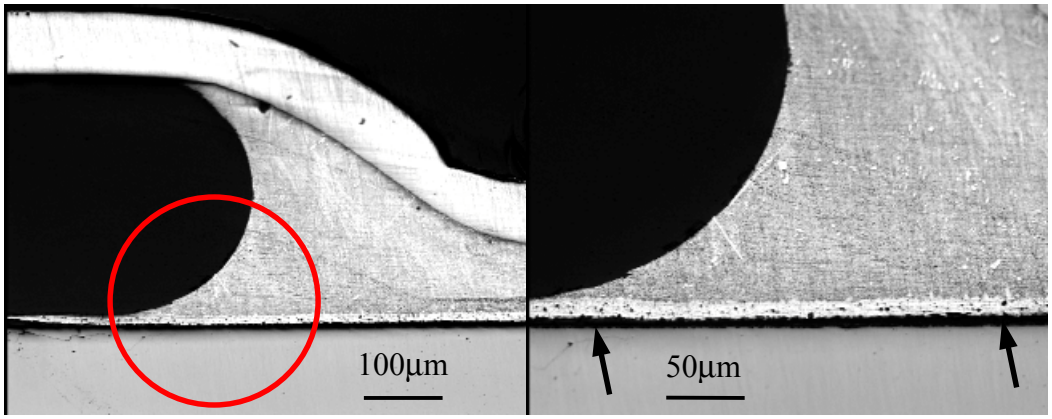


Figure 3.26 Cumulative fails based on a 50% increase in resistance, using Ag3.5-Sn96.5 solder.

Figure 3.27 shows an optical microscopy image of the cross-section of a typical Ag3.5-Sn96.5 dimple solder joint after 345 thermal cycles.



(a) (b)

Figure 3.27 (a) An Ag3.5-Sn96.5 dimple solder joint after 345 thermal cycles; and (b) the zoomed-in view of the circled region.

Figure 3.28 shows a typical Ag3.5-Sn96.5 CCB solder joint after 400 thermal cycles.

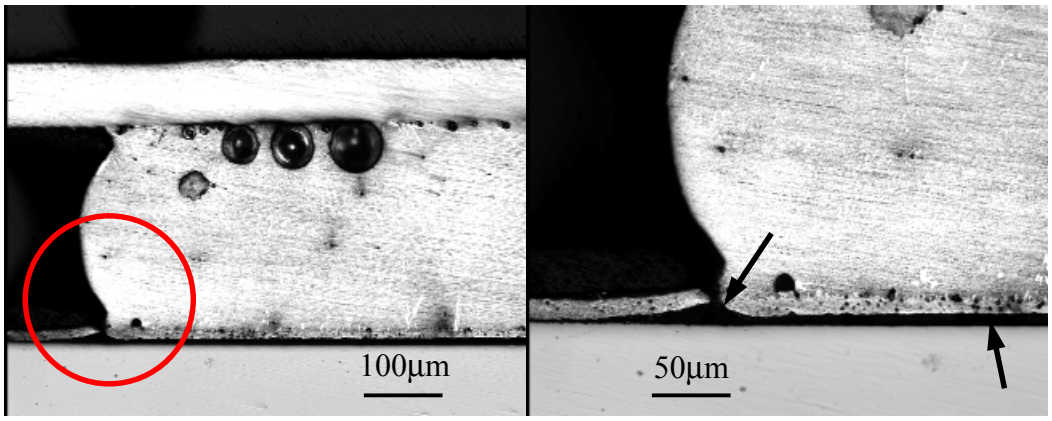


Figure 3.28 (a) Ag3.5-Sn96.5 CCB solder joint after 400 thermal cycles; and (b) the zoomed-in view of the circled region.

A similar failure pattern is seen for both the dimple and the CCB solder joints made using Ag3.5-Sn96.5 solder: delamination of the metallization pad as indicated by the arrows. This is probably due to the high normal stress at the solder/pad interface that exceeded the adhesion strength between the UBM pad and the silicon for non-underfilled samples. In this case, the in-house metallization process needs to be enhanced to meet the adhesion requirement for thermal cycling test.

3.6 Power cycling test results

3.6.1 Non-underfilled samples

- CCB packages

A pronounced change in thermal resistance was found when testing non-underfilled CCB packages. In this situation, the temperature of the package during cooling was stable. What's different is the temperature at the end of heating cycle T_{max}. Figure 3.29 shows the temperature change in T_{max} of a CCB test package without underfill. The onset of the increase in T_{max} was recorded just before the number of power cycles reached 200.

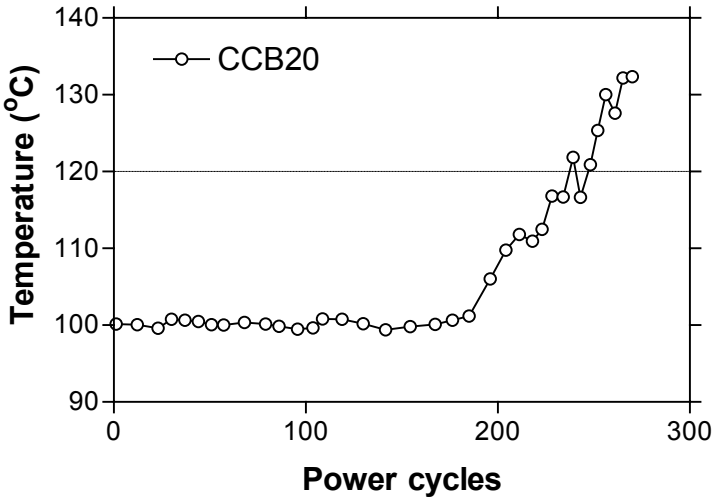


Figure 3.29 Temperature change reflecting an increase in thermal resistance of CCB test samples.

The packages were cross-sectioned for failure analysis after power cycling. It was found that in these CCB samples, the silicon devices were cracked very early in power cycling. Figure 3.30 shows typical cross-sections of the CCB packages. The die-cracking (indicated by arrows), not the solder joint failure, caused the temperature change. This should be mostly induced by the rigid structure of the CCB and the large CTE mismatch between the copper and the silicon.

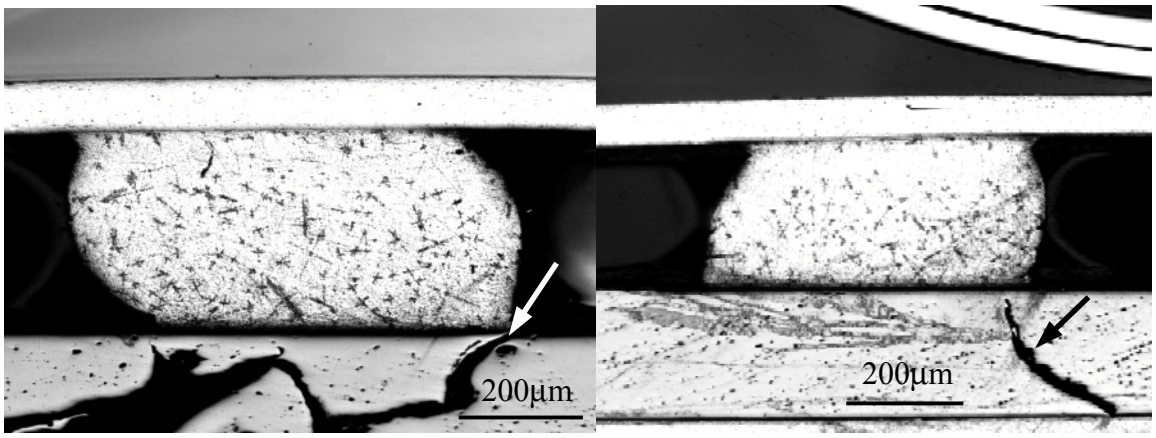
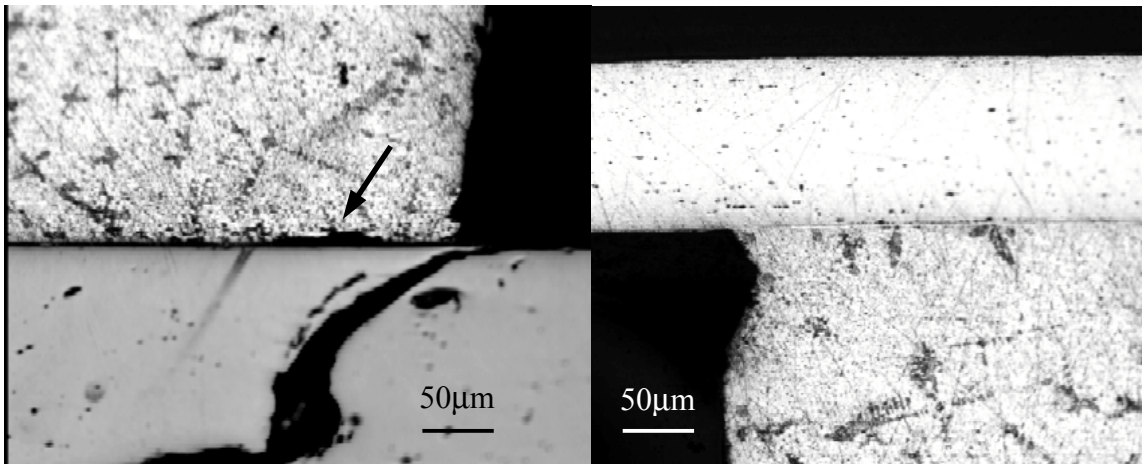


Figure 3.30 Typical cracked CCB solder joints.

Although the solder joints are considered to have no failure in this case, a zoomed-in view over the corner region of the CCB solder joint reveals a crack that just initiated, as shown in Figure 3.31 (a). This crack started from the edge at the silicon/solder interface and is about 100 µm long. It is interesting to note that this happened when the CCB package was only subjected to 280 power cycles. Furthermore, an infant crack appears at the right-hand solder corner.



(a) (b)

Figure 3.31 (a) Just-initiated crack under a 200x microscope;
(b) no crack is found at copper/solder interface.

- Dimple Array packages

For Dimple Array packages, Figure 3.32 shows the typical trend of the temperature at the end of each heating cycle T_{max} versus the number of power cycles. The temperature-

dependency of forward voltage for the non-underfilled DAI packages is shown in Figure 3.33. Both curves are almost flat over the entire range of testing period (~ 2,800 cycles). Since the FEM suggested a time-to-crack-initiation of ~2,000 cycles, the experiment was stopped and samples were cross-sectioned for examination.

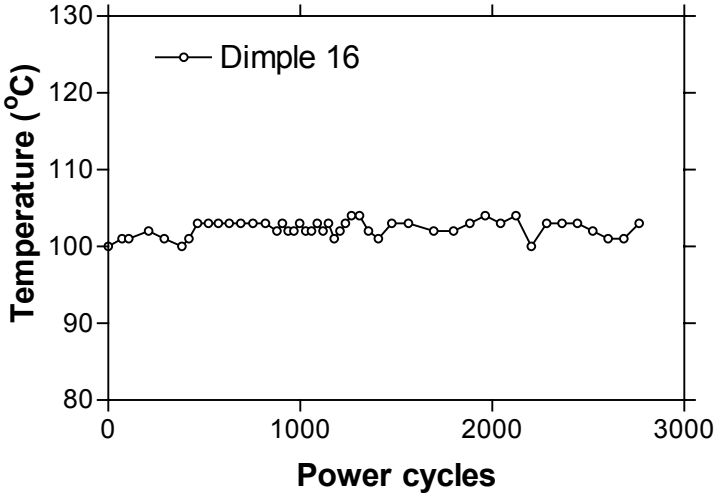


Figure 3.32 Measured package temperature as a function of the number of power cycles.

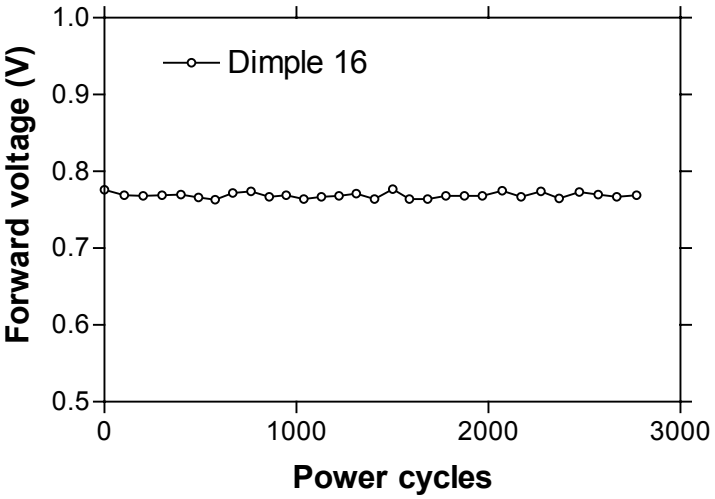


Figure 3.33 Measured package forward voltage as a function of the number of power cycles.

Figure 3.34 shows the cross-section of the solder joint of a non-underfilled dimple package with 2,800 cycles. Surprisingly, although there is no sign of change in forward voltage and thermal resistance, a crack propagating from the edge to the center is clearly seen. This raises questions about the effectiveness of the forward voltage measurement.

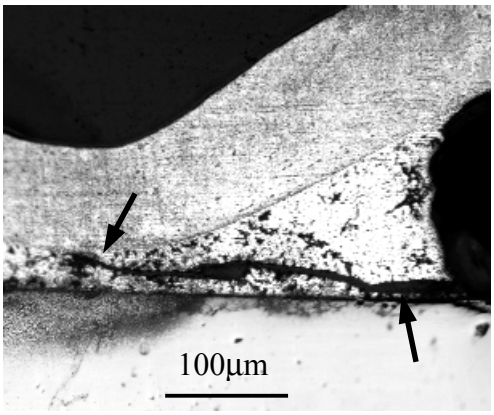


Figure 3.34 A typical failed Dimple Array samples (non-underfilled) at 2,800 power cycles.

The reason that the forward voltage measurement cannot determine the amount of time required for crack initiation and growth is speculated as follows: The measured forward voltage actually consists of a voltage drop due to the device on-resistance, UBM resistance, and solder joint resistance. A typical solder joint used in the Dimple Array package or CCB package has a resistance of less than 1 mΩ. The voltage drop due to the DC conduction of the solder joint is only a small fraction of the typical forward voltage of the device (0.7V ~ 1V). Therefore, slight change in the solder joint will not significantly affect the forward voltage.

3.6.2 Underfilled samples

- CCB

Figure 3.35 shows the measured voltage of the underfilled CCB packages versus the number of power cycles. It is shown in the chart that a large jump in forward voltage, measured at the device-rated current for the CCB solder joints, occurs around 1,600 cycles. The increase of the forward voltage may or may not be due to crack initiation in the solder joints, based on the observation of non-underfilled samples, as discussed in

Section 3.6.1. The final breakdown of the solder joints is characterized by a large change in forward voltage.

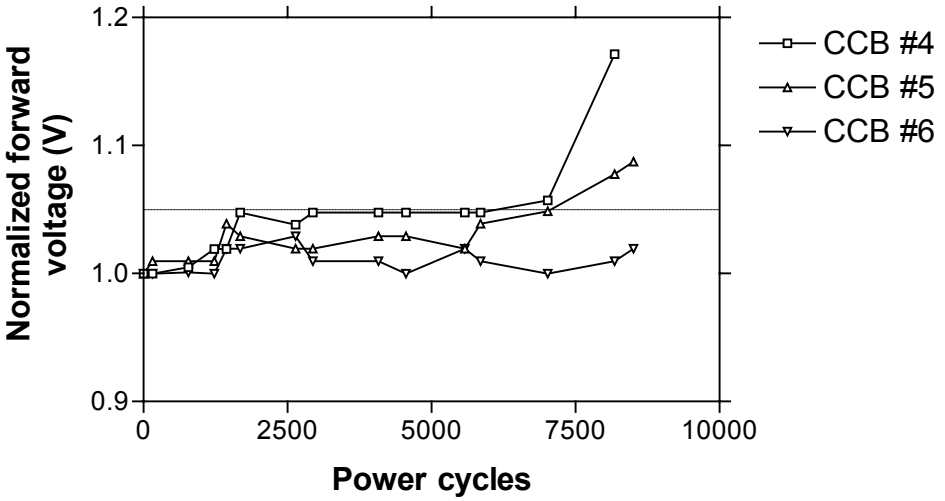


Figure 3.35 Measured voltage as a function of the number of power cycles for underfilled CCB packages.

Figure 3.36 shows a typical CCB solder joint after 4,000 power cycles. Cracks were already developed at the corner of the solder joint on the chip side. An infant crack is found in the solder at both the chip side and the copper side. Figure 3.37 is the enlarged view of the lower left corner of the same solder joint.

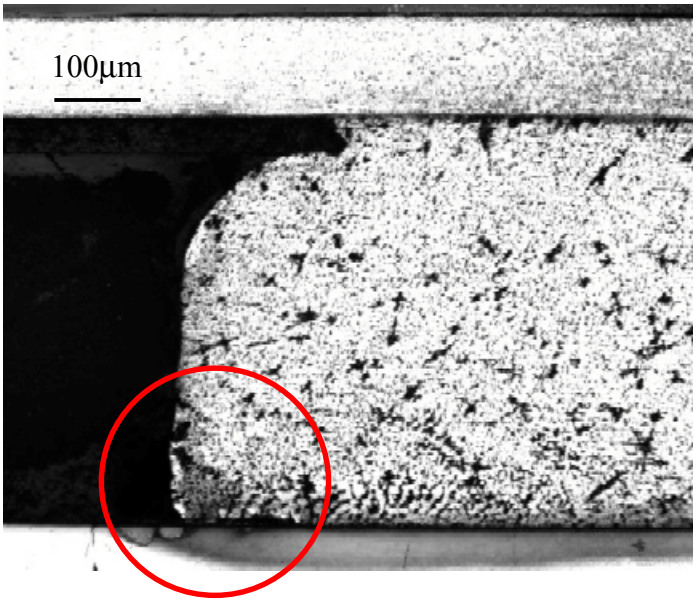


Figure 3.36 A typical CCB solder joint after 4,000 power cycles.

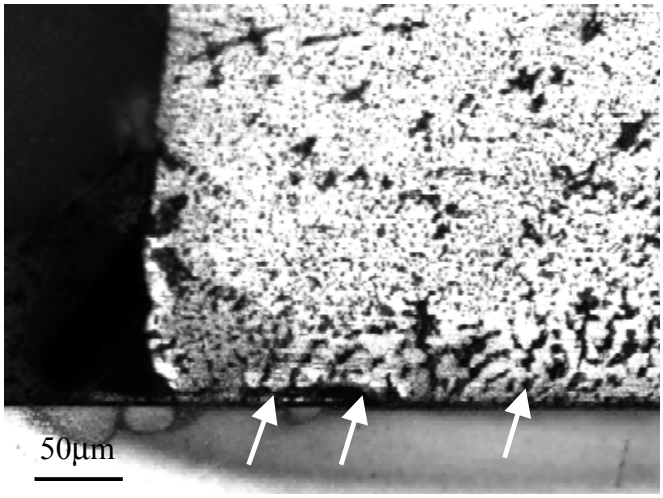


Figure 3.37 A zoomed-in view of the corner crack shown in Figure 3.36.

Figure 3.37 shows the voiding of the solder at the infant crack. Figures 3.38 and 3.39 show another example of the initial voiding and cracking in the solder at both the copper/solder and the device/solder interface in the CCB solder joint, which are pointed by the arrows.

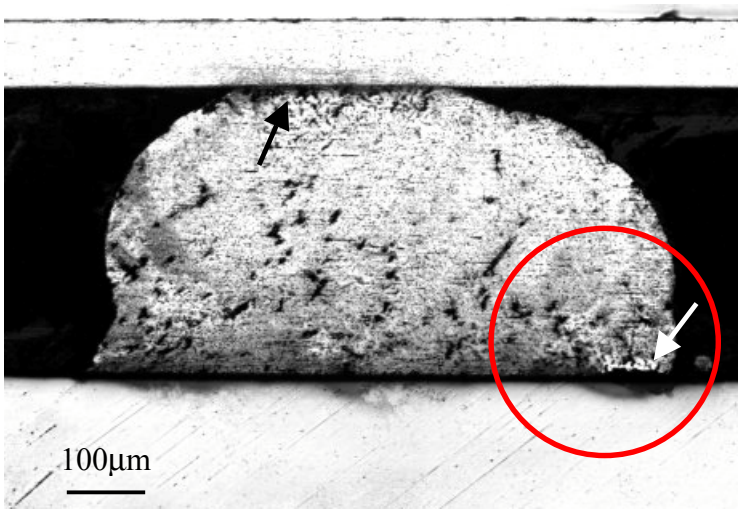


Figure 3.38 A CCB solder joint after 4,000 power cycles also shows voiding at the copper/solder interface (black arrow).

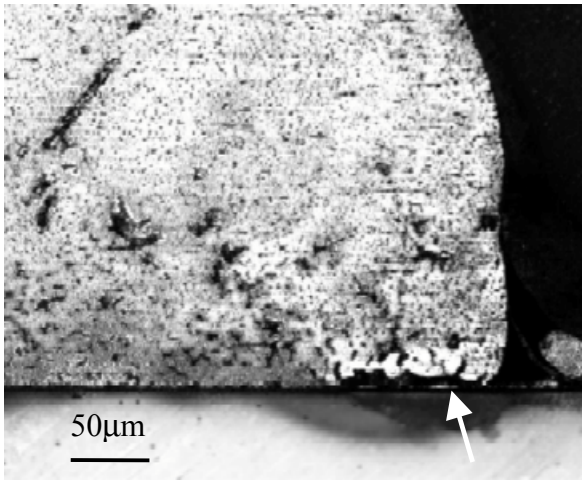
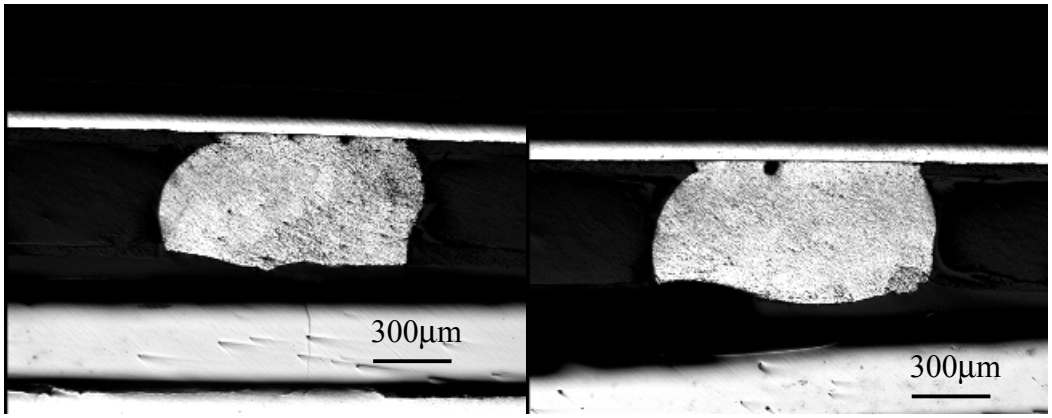


Figure 3.39 A zoomed-in view of the corner crack shown in Figure 3.38.

Figure 3.40 shows the optical microscopy image of CCB solder joints after 8,500 cycles. Significantly wider cracks are observed in the solder joints. The cracks were found to be on the silicon chip side. The copper interconnect looks thinner in the images because of shadows on the curved polishing surface.

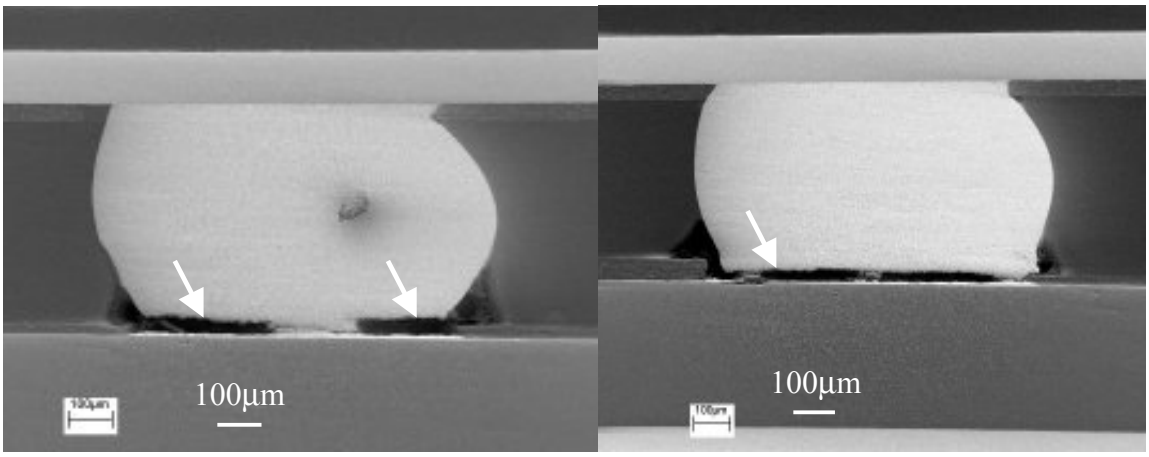


(a) (b)

Figure 3.40 Optical microscopy images of CCB solder joints after 8500 cycles (sample #4,5).

Figure 3.41 shows SEM cross-section images of failed CCB solder joints after 8,500 cycles. Again, the cracks occurred at the solder/silicon interface. Figure 3.41 (a) is a center solder joint and (b) is an edge solder joint. It is clearly shown that for the center

solder joint, cracks approached from both corners, while for the edge solder joint, a single crack cleft through the whole solder joint.



(a) (b)

Figure 3.41 Cross-sections of (a) a center CCB solder joint and (b) an edge CCB solder joint after 8,500 cycles.

- Dimple

Unlike the CCB packages, for the dimple packages, no apparent onset point of forward voltage increase is observed. As shown in Figure 3.42, the forward voltage of the underfilled dimple samples does not display much increase until about 4,000 cycles. After that, the measured forward voltage increases at a faster pace.

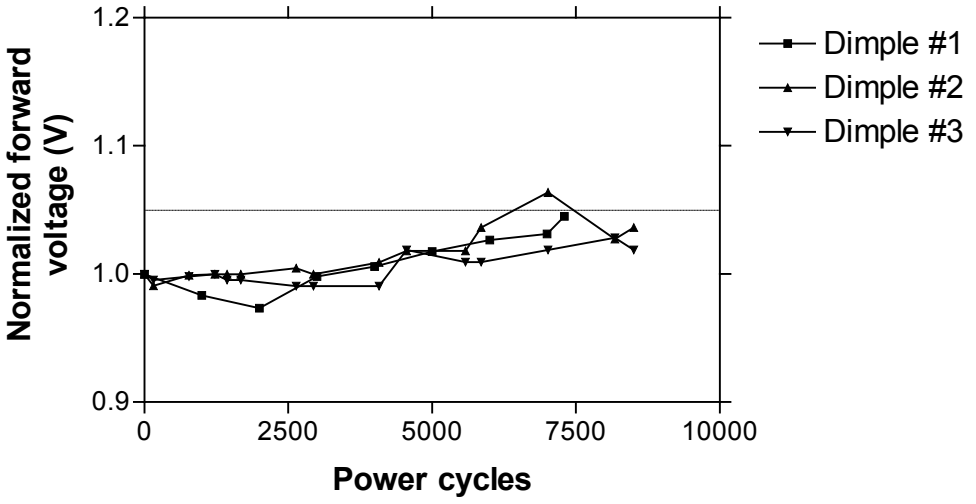
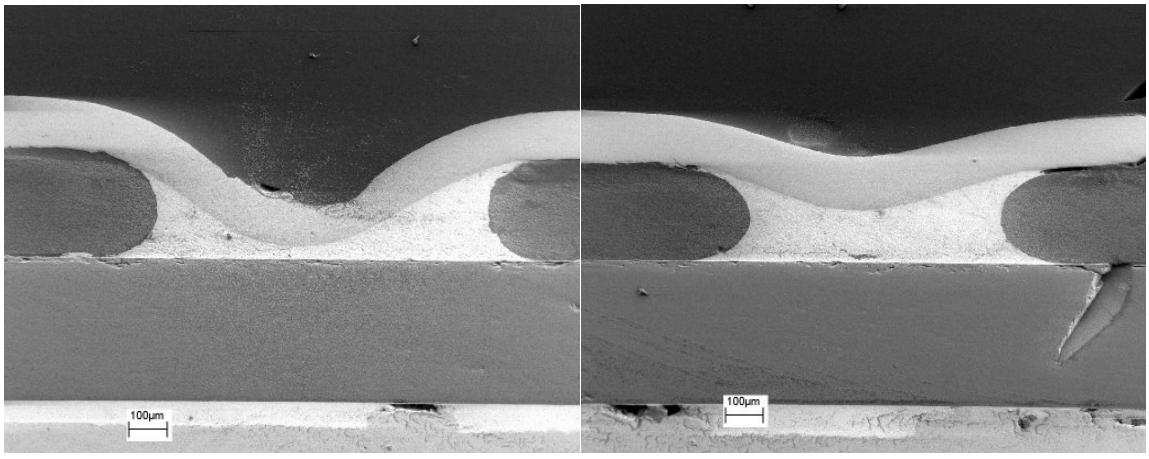


Figure 3.42 Power cycling voltage measurements for underfilled CCB and Dimple packages.

Figure 3.43 (a) shows the cross-section SEM images of an underfilled Dimple Array package after 5,000 power cycles. No cracks were observed. Figure 3.43 (b) is another solder joint that sustained 8,500 power cycles before developing a cracking within the solder joint.



(a) (b)

Figure 3.43 (a) A typical dimple solder joint after 5,000 cycles; (b) a dimple solder joint after 8,500 cycles.

Figure 3.44 shows the cross-section of a Dimple Array solder joint after 12,700 cycles. Solder cracking due to fatigue is seen in this figure. The crack started from the corner at the silicon/solder interface and propagated to the solder/copper interface at the center region, and finally reached the other side of the silicon/solder interface. Another crack growth path is found from the neck of the Dimple Array solder joint. It met the first crack after propagating through the solder joint for about 0.2 mm.

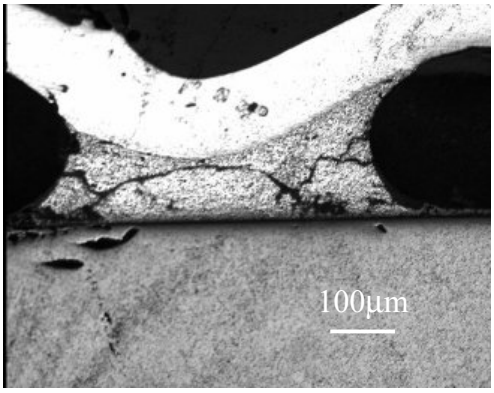


Figure 3.44 Cross-section of a typical dimple solder joint after 12,700 cycles (Sample #9).

3.6.3 Ag3.5-Sn96.5 solder

Performance of the lead-free eutectic silver-tin solder (Ag3.5-Sn96.5) was evaluated. Figure 3.45 shows the trend of forward voltage versus the number of power cycles. Again, not much information can be obtained from this chart due to the insensitivity of the forward voltage to solder cracking.

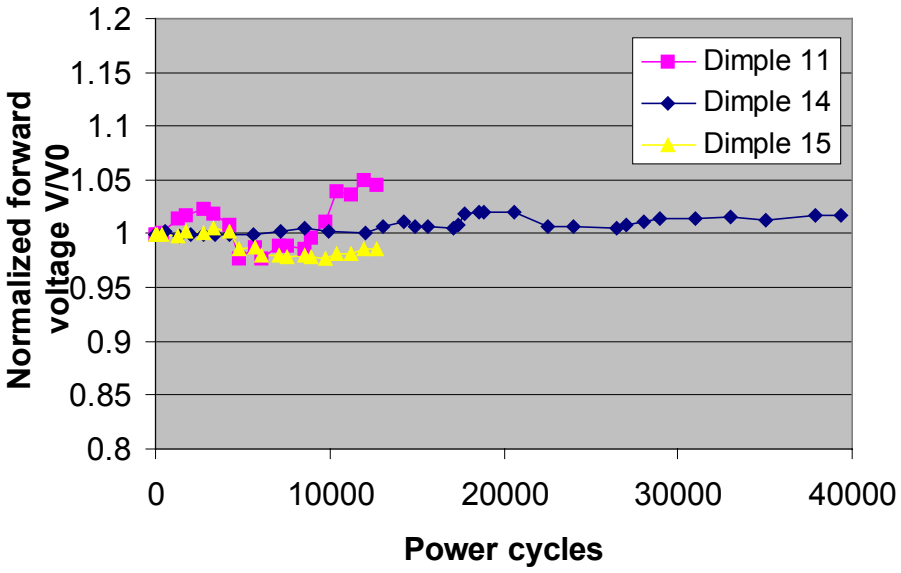


Figure 3.45 Forward voltage versus number of power cycles for Ag3.5-Sn96.5 dimple solder joints.

Figure 3.46 shows an SEM image of the metallographic section of a zero-cycle Ag3.5 DAI sample.

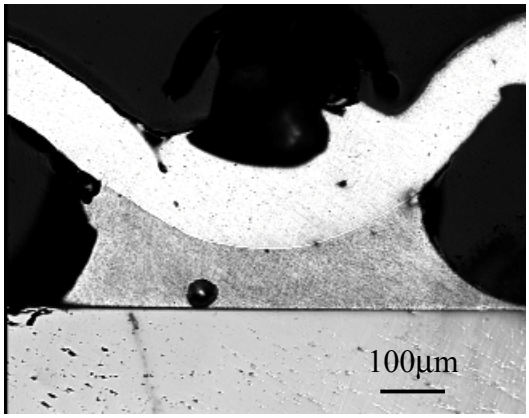


Figure 3.46 A zero-cycle Ag3.5-Sn96.5 dimple solder joint.

Figure 3.47 shows an Ag3.5-Sn96.5 dimple solder joint after 12,700 power cycles (sample #11 from Figure 3.45). The left side of the solder joint is the farther end from the center of the chip. The crack initiated from the left-hand side (silicon/chip interface), propagated the through center (in this solder joint, the standoff height was not maintained during reflow), and penetrated the neck of the right half of the solder joint.

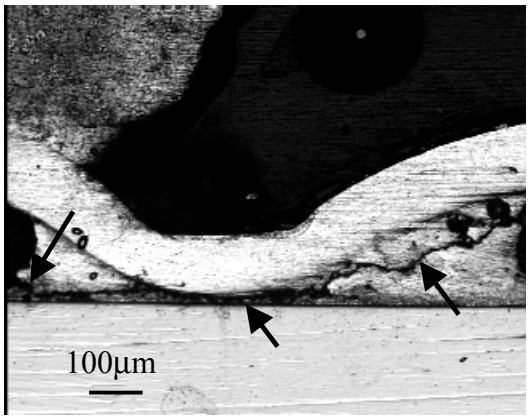


Figure 3.47 Cross-section of a dimple solder joint after 12,700 cycles.

Figure 3.48 shows an SEM image of the metallographic section of an Ag3.5 DAI sample (underfilled) after more than 35,000 power cycles (sample #14). The forward voltage of the sample has not exceeded 5% of the original measurement at the zero-cycle. From the SEM image, it is seen that cracks populate the solder joint, but the whole structure is held in place by the underfill.

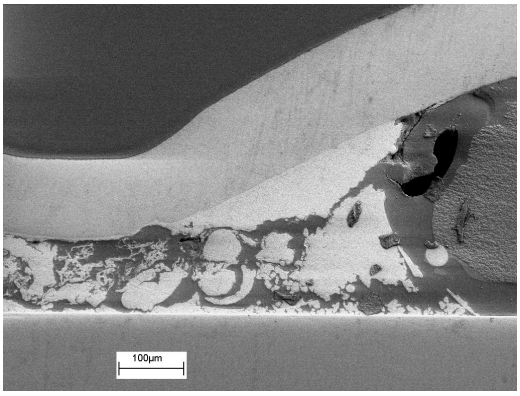


Figure 3.48 An Ag3.5-Sn96.5 dimple solder joint after more than 35,000 power cycles.

3.6.4 C-mode scanning acoustic microscopy

In this study, attempts were made to use SAM to examine the Dimple Array solder joints. The SAM is reported to be effective for non-destructive detection of die-attach voids and delamination. However, it has been unsuccessful in detecting any details of the solder joints of the DAI packages. Figure 3.49 shows an SAM image from a zero-cycle Dimple Array package using a 15 MHz SAM actuator. Though the locations of the five dimple solder joints are clearly represented by the dark regions, the color of these regions indicates either an absence of reflecting signals caused by the curved dimple surface topology or the shadowing effects from the solder. In either case, the solder/silicon or solder/copper interface is not accessible.

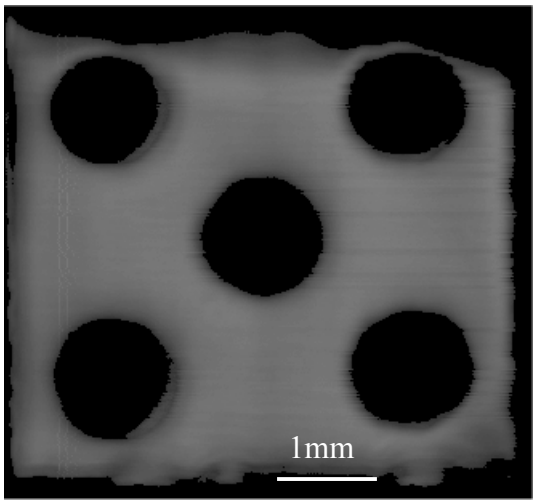
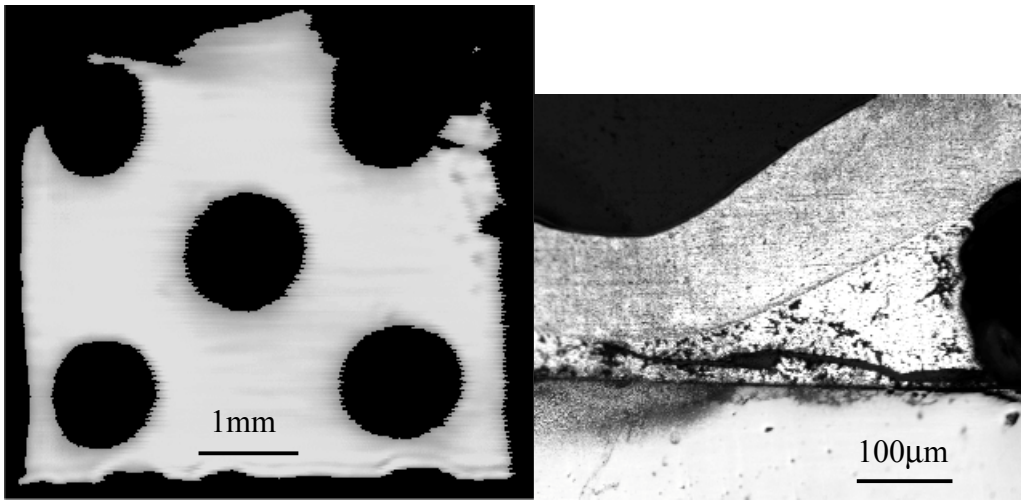


Figure 3.49 C-mode SAM image of a zero-cycle Dimple package.

Figure 3.50 (a) shows SAM scan pictures of the same sample after 2,800 power cycles. The image shows dark color in the dimple regions. The C-SAM was not able to capture the cracking of the DAI sample due to the uneven surface caused by the dimple structure: The ultrasound bounces off of the dimples at such an angle that the transducer is unable to read the pulse echo information [133]. A previously shown (Figure 3.34) metallographic cross-section image of this sample indicating solder joint cracks is shown again in Figure 3.50 (b).



(a) (b)

Figure 3.50 A dimple sample after 2,800 power cycles (#17): (a) C-mode SAM images; and (b) the cross-section view.

Summary

In this chapter, the thermomechanical reliability of the DAI has been evaluated using accelerated testing, including thermal cycling and power cycling. In all tests the CCB packages were used for comparison. The foci of the thermal and power cycling tests are compared in Table 3.3.

Table 3.3 Foci of the thermal cycling and power cycling tests.

Cases	*Thermal cycling*	*Power cycling*
Pb37-Sn63, non-underfilled	**Focus √**	Evaluated
Pb37-Sn63, underfilled		**Focus √**
Ag3.5-Sn96.5, non-underfilled	Evaluated	
Ag3.5-Sn96.5, underfilled (Dimple only)		Evaluated

Figure 3.51 summarizes the thermal cycling results for non-underfilled CCB and dimple solder joints made by Pb37-Sn63 solders. Openings and delaminations were commonly found in failed CCB solder joints at around 135 cycles. In contrast, dimple solder joints apparently last longer, with most delamination failures occurring after 250 cycles. No

opening failures were found, and some dimple solder joints even exhibit no failure at 350 cycles.

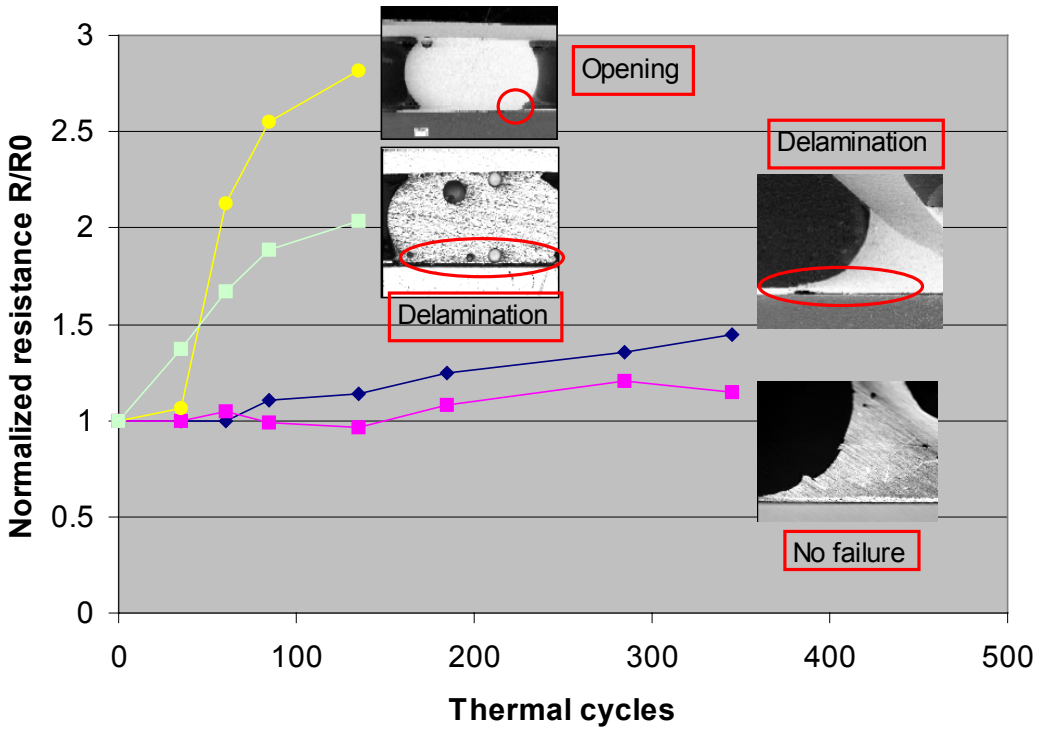


Figure 3.51 Summary of the Pb37-Sn63, non-underfilled samples for thermal cycling test.

The thermal cycling test on non-underfilled Ag3.5-Sn96.5 solder joints suggests a similar reliability for the Dimple and CCB solder joints. Use of the Ag3.5-Sn96.5 solder substantially improves CCB solder joint reliability, while it does not greatly improve dimple solder joint reliability.

Power cycling test results on Pb37-Sn63 underfilled samples are summarized in Figure 3.52. The measured forward voltage can not be relied on to make a judgement as to whether or not a crack initiates in the solder joint, nor can it be used to indicate crack growth. Shown in this figure, the Dimple Array solder joints have less damage than the CCB solder joints for the same power cycling duration. Fatigue cracks in the CCB solder joints are wider and are localized to the device/solder interface, while for the Dimple Array solder joints, the cracks are thin and go through the bulk of the solder.

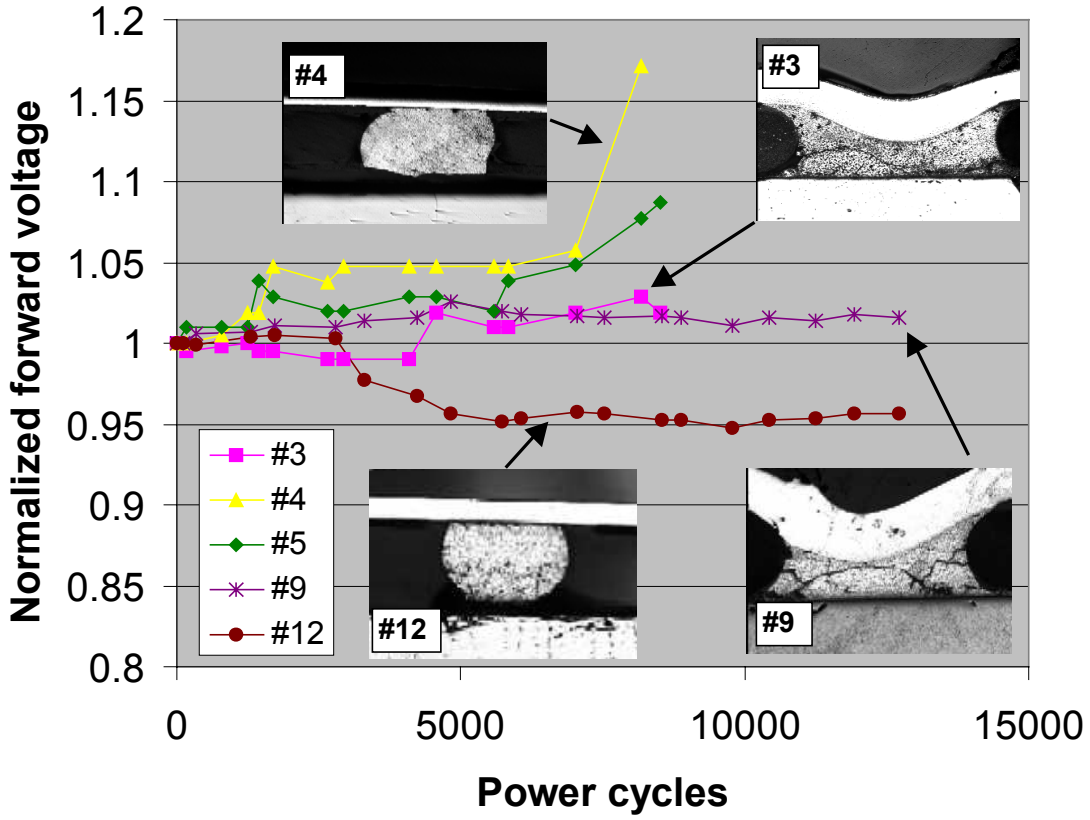


Figure 3.52 Summary of the Pb37-Sn63, underfilled samples for the power cycling test.

The fatigue life of solder joints includes crack initiation, crack growth, and catastrophic failure. However, it has been very difficult to determine the exact time of crack initiation using the forward voltage measurement because only a very small portion of the measured value is contributed by the solder joint voltage drop. Similarly, in testing of the wire bond interconnected modules, one can not make a judgement on when exactly the crack starts to grow. This is a drawback of most power cycling testing methods using forward voltage measurement.

Based on metallographic cross-sectioning examination, power cycling fatigue lives of the underfilled Dimple Array solder joints are generally longer than those of the CCBs.

The next chapter will present numerical analysis of Dimple Array solder joint reliability using the FEM method.