

Modeling and Design of Digital Current-Mode Constant On-time Control

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(ABSTRACT)

This thesis presents the fundamental issues of the digital controlled DC/DC converter. A lot of challenges exist when you introduce the digital control technique into the control of the DC/DC converter, especially with regards to the voltage regulator module. One issue is the limit cycle oscillation problem caused by the quantization effect from the ADC and DPWM of the digital control chip. Another issue is the delay problem coming from the sample-and-hold effect.

In this thesis, the modeling, analysis and design methodology for the constant frequency voltage-mode control is reviewed. A DPWM (Digital Pulse Width Modulator) model is verified in simulation, which shows what effects the digital control brings to the conventional Pulse Width Modulator.

In CPES, the constant on-time control concept is introduced into the digital control of the voltage regulator module. This provides a high resolution of DPWM and allows the digital constant on-time voltage-mode control architecture to be proposed. To limit the oscillation amplitude in the digital control structure, the digital constant on-time current-mode control w/ external ramp is further proposed in CPES. To analyze this structure, a describing function model is proposed for the digital constant on-time current-mode

control, which takes both the sample-hold effect and the quantization effect into consideration. This model clearly shows the stability problem caused by the sample-hold effect in the current loop. Using larger ramp's slope values, this stability issue can be alleviated.

Based on this model, a design methodology is introduced. By properly designing the current loop's ADC resolution and the voltage loop's ADC resolution, the limit cycle oscillation in this structure can be minimized: the digital constant on-time current-mode control will only have the oscillation coming from the sample-hold effect in the current loop, which can be greatly reduced by adding the large slope's external ramp to this structure. Simulation verification for this design methodology is provided to prove the concepts. Based on the proposed model, the compensator design is performed. The motivation for the compensator design is to push the bandwidth while satisfying the stability condition and the dynamic no-limit-cycle oscillation condition. When analyzing the case of one sample per switching cycle, there is a certain amount of delay, which compromises the phase characteristics. Our design also requires a large external ramp because it will reduce the oscillation amplitude in our system. From our model, it is quite obvious that the external ramp must have a slope larger than one time that of inductor current down slope. A slope that is too larger will weaker the phase and limit the bandwidth. When using the normal current-mode compensator, like the 1-pole 1-zero compensator, the phase is dropped too much and the bandwidth will be limited too low. If we use a 2-pole 2-zero compensator, the phase can be boosted. However, in this case, the gain margin requirement from the dynamic no-limit-cycle oscillation condition will make the further improvements on bandwidth impossible. In our design, the one sixth of the switching frequency is achieved.

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Chapter 1 Introduction of Modeling for Digital Controlled DC/DC Converter

1.1. Digital Controlled DC/DC Converter and Its Nonlinear Effects

The circuit diagram of the digital controlled voltage-mode single-phase buck converter is shown in figure 1.1.

The digital controlled buck converter, as shown in Fig. 1.1 has three parts that are different from analog control: an analog-to-digital converter, a digital compensator and a digital pulse-width modulator.

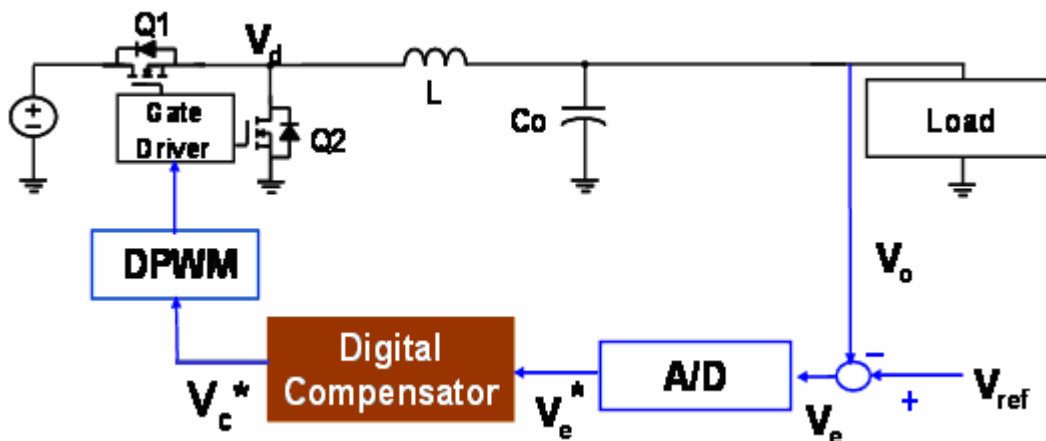


Fig. 1.1 Circuit Diagram of Digital Voltage-Mode Controlled Buck Converter

The analog-to-digital converter (ADC) contains two parameters which are quite important to system performance and control design: the sampling frequency, T_{sample} and the quantization level: ΔV_{ADC} as shown in Fig. 1.2 [19]. Here ΔV_{ADC} is the step size in figure 1.2.

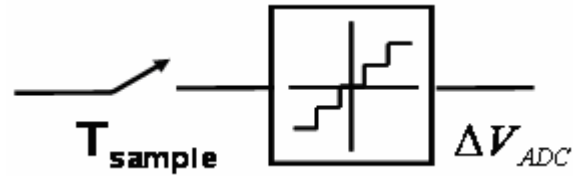
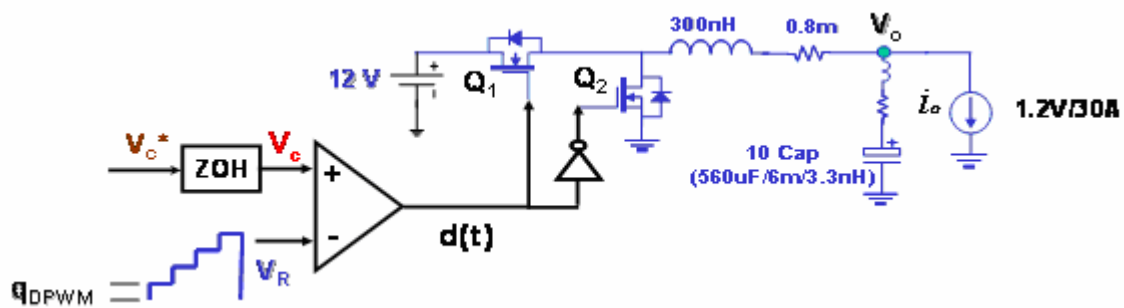
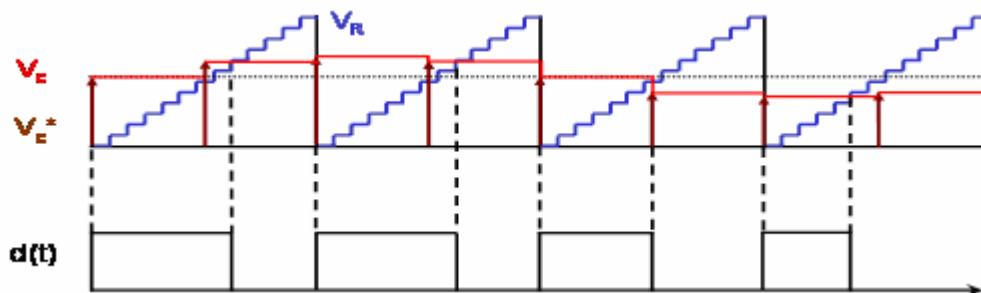


Fig. 1.2 Sampling Frequency and Quantization Level in ADC

Fig. 1.3 shows a typical block diagram and waveform of a Digital pulse-width modulator. From Fig. 1.3 (a), it is quite clear to us that a typical DPWM includes a register to hold the compensator's output, V_c^* and a counter to count the system clock, in order to produce a digital ramp. Because of this register, there is a zero-order-hold block representing its hold effect. Fig. 1.3 (b) shows a typical waveform for a two sampling per switching cycle case. In this case, digital compensator outputs the control signal V_c^* for two times in one switching cycle, and the register holds this value to compare with the digital ramp from the counter. Finally a certain value of the duty cycle is produced to regulate the buck converter [26].



(a) Circuit diagram of Digital PWM



(b) PWM waveform of Digital PWM

Fig. 1.3 Digital Pulse-width Modulator in Constant-Frequency Digital Voltage-Mode Controlled Buck Converter

When comparing the ADC and DPWM to the analog control, it is clear that there are two fundamental effects: one is a sample-hold effect and the other one is a quantization effect. These two nonlinear effects bring the issues and also call for a special methodology to model and design the digital controlled DC/DC converter system.

First, the sample-hold effect brings a delay issue to the digital controlled DC/DC converter. As we know, the delay influences the reaction speed of the DC/DC converter to the perturbation. This issue becomes more stringent in the voltage regulator modulator application [2-3, 30-31]. Second, the quantization effect coming from the ADC and the DPWM will produce a well-known issue: limit cycle oscillation problem [5]. The limit cycle oscillation superimposes on the output voltage switching ripple and, hence makes the total output voltage ripple worse. This becomes more intolerable in VR application, because the maximum allowable range for a steady-state output voltage ripple is quite small. This stringent requirement for an output voltage ripple makes a high resolution of DPWM necessary. A lot of research work has been focused on this issue and several solutions have been proposed.

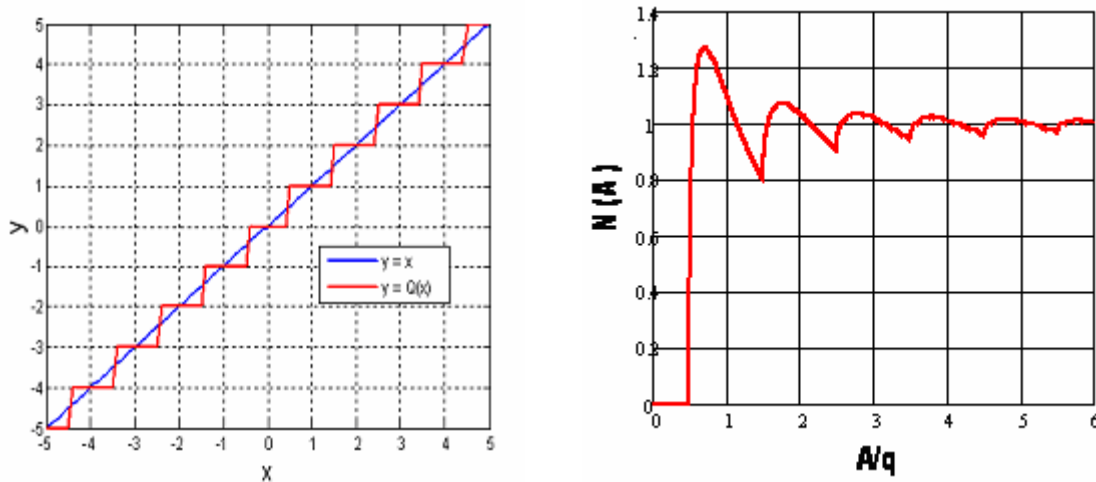
In the second section, the quantization effect modeling will be reviewed and the DC offset issue is illustrated. In the third section, the sample-hold effect modeling is introduced. First a conventional model from textbook is introduced and then a zero-order-hold model in digital controlled DC/DC converter is discussed. Based on the modeling of these two fundamental nonlinear effects of digital control, a DPWM model and also the system model of digital constant-frequency voltage-mode controlled DC/DC converter can be constructed. Based on the loop model, the design guidelines are investigated in forth section.

1.2. Describing Function Model for Quantization Effect

Limit cycle oscillation is a result of the presence of signal amplitude quantizers, which are present in the ADC and DPWM modules in the digital control feedback loop [5, 13]. Especially in voltage-mode control case, the quantization effects of the ADC and the DPWM are in series. The limit cycle oscillation coming from the interaction between these two quantization effects is quite hard to predict, both in its amplitude and in its frequency. This makes the task of controlling the output voltage ripple in certain applications, like the VR application, a big challenge. In order to avoid limit cycle oscillation, literatures [6] has placed much effort on modeling the quantization effect from the ADC and the DPWM, and developing certain no-limit-cycle oscillation design guidelines.

1.2.1. ADC Quantization Modeling

In a typical digital controlled system, the ADC serves as the interface between the analog world and the digital world: it performs two tasks on the signals, which need to be processed in digital control chip, sampling and quantization. Since the quantization is a nonlinear effect, the conventional linear modeling method, state-space averaging model, is not valid to describe its characteristics. The describing function method is a good tool to model nonlinearities, like quantization, saturation, and dead-zone. In literature [19], the describing function model for the round-off quantization is derived and shown in fig. 1.4. In literature [5], the authors argue that because the control law contains an integral term, only limit cycles having a zero dc component can be stable, because the integrator drives the dc component of the error signal to the zero error bin. Since in steady-state the dc bias is driven to zero, and the compensator has a low-pass characteristic, the sinusoidal-input describing function of a round-off quantizer can be used to model the ADC in DC/DC converter application. In literature [6], the same argument is used to apply the textbook's round-off describing function model for ADC.



(a) Round-off quantizer

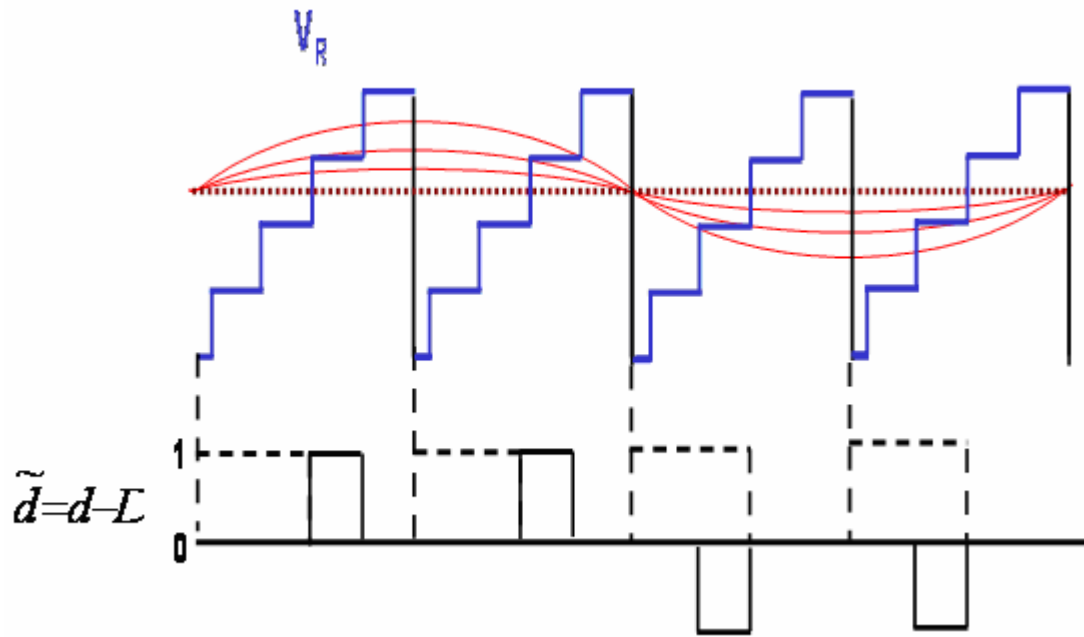
(b) Describing Function of Round-off Quantizer

Fig. 1.4 Describing Function Curve for Round-off Quantization

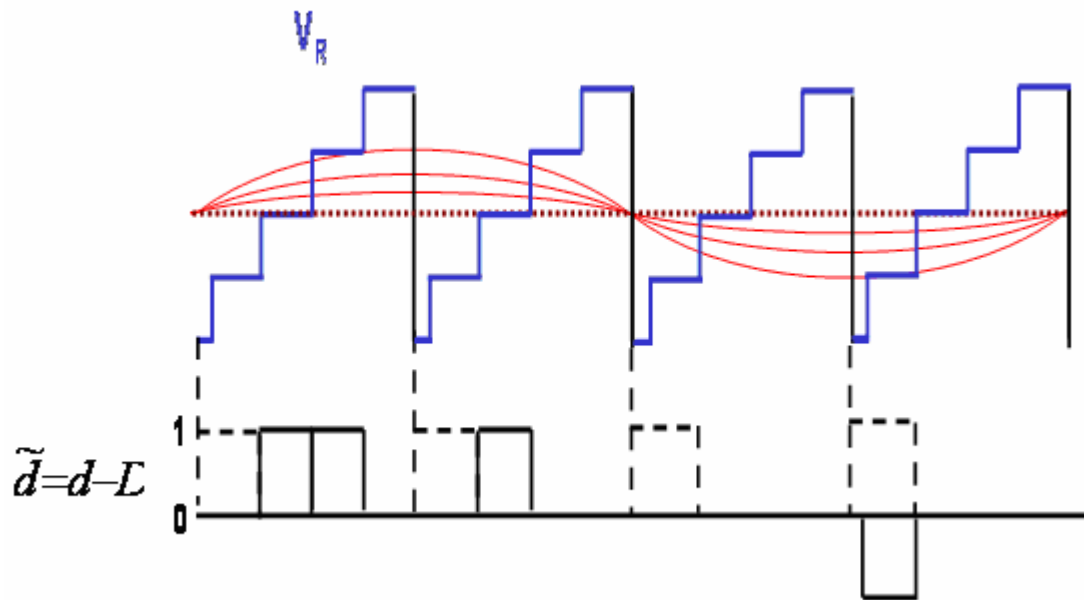
The horizontal axis of this curve is a ratio between the sinusoidal oscillation's amplitude at the input of ADC and the quantization level of that ADC. The vertical axis is the nonlinear gain value, which is the ratio between the sinusoidal oscillation's amplitude at the input of ADC and the same frequency sinusoidal oscillation's amplitude at the output of that ADC. From the curve, we can observe that the maximum value for this gain is $\frac{4}{\pi}$.

1.2.2. DPWM Quantization Modeling

For the quantization effect in DPWM, the literature [6] pointed out that the offset at the input of the DPWM quantizer can be arbitrary, so the round-off quantizers describing function is not enough to model the DPWM quantizer. Figure 1.5 shows the influence of offset.



(a) Offset = 0.0: dotted line at center



(b) Offset = 0.5: dotted line at boundary

Fig. 1.5 Offset Issue in Modeling of DPWM

When comparing the fig. 1.5 (a) and fig. 1.5 (b), one notices that although the V_c perturbation's amplitude is same, but the different DC values (different offset) lead to different duty cycle value. When it comes to deriving the describing function model of DPWM, the different duty cycles, while containing the same V_c perturbation amplitude, will result in a different describing function gain. The definition is shown as:

$$\frac{\tilde{d}}{\tilde{v}_c} = \frac{A_d}{A_c} = DF \cdot F_M \quad (1)$$

In this equation, DF represents the describing function gain due to DPWM quantizer. F_M is related to the height of the digital ramp, which represents the modulation effect and is similar to the analog PWM case. The figure 1.6 gives an illustrative example. In this case, the sampling frequency is assumed to be infinite. If we know the ratio between A_d and A_c and we know F_M , the describing function gain of the DPWM quantizer can be obtained through either derivation or simulation.

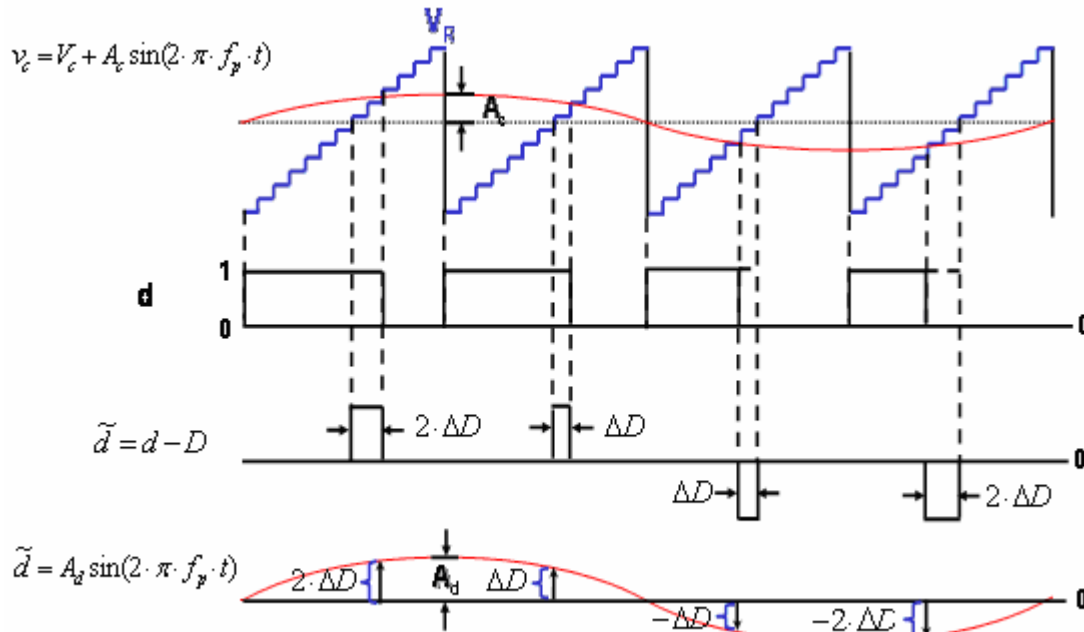


Fig. 1.6 An Illustrative Example to Derive the DPWM Gain

Since a lot of mathematics work is needed to derive the ratio between A_d and A_c and also because it is quite hard to get the analytical results, the simulation method can be applied to help obtain the describing function gain. Figure 1.7 shows the simulation setup.

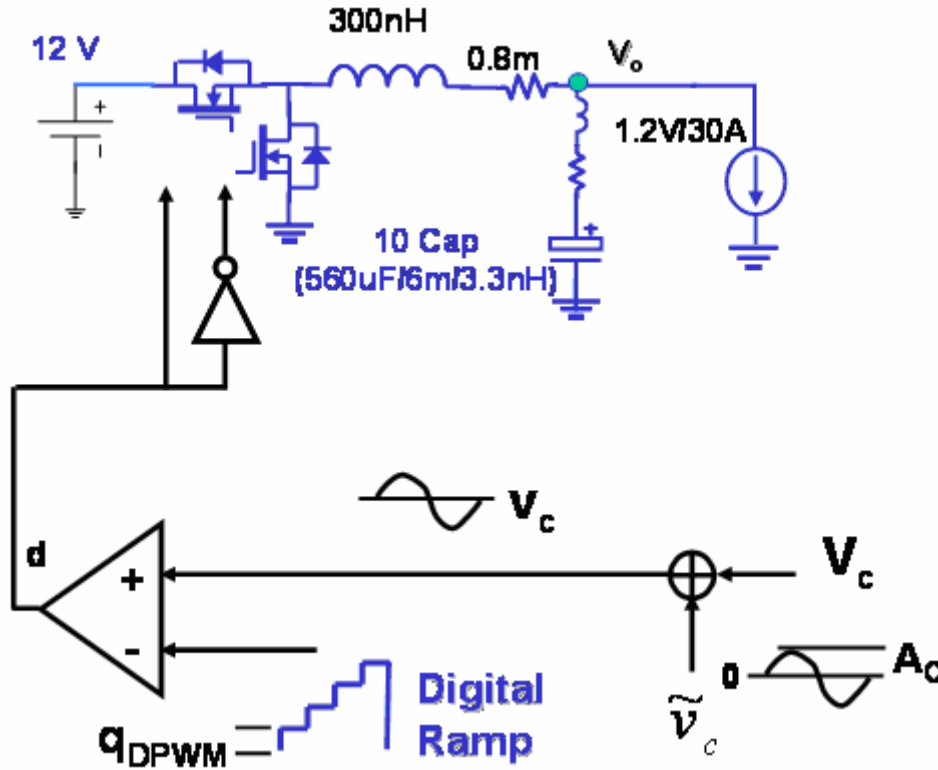
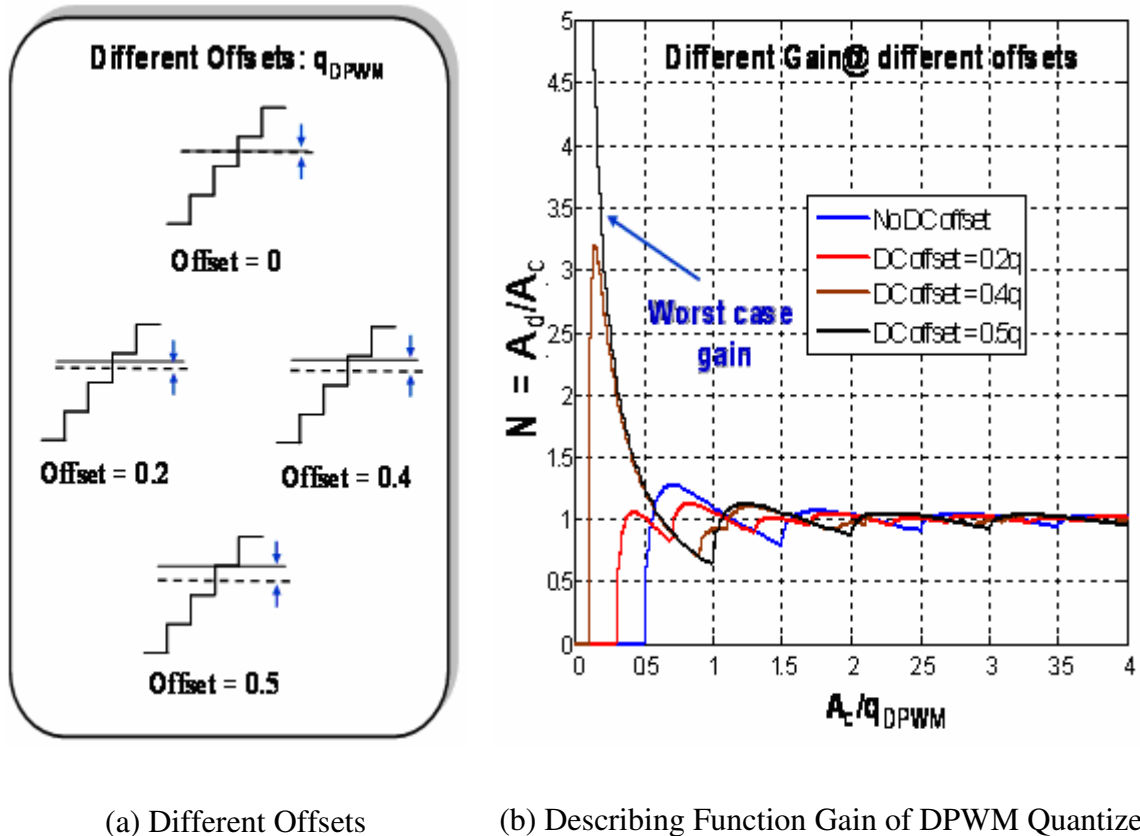


Fig. 1.7 Simulation Setup for Deriving the Describing Function Gain

In this simulation setup, the quantized ramp is compared with the control signal to determine the turn-off edge of the duty cycle. In this simulation, since we focus on the quantization gain, the continuous V_c perturbation is utilized, which is equivalent to the assumption of infinite sampling frequency. The injected V_c has two parts: the steady-state value, as capital V_c and the small variation superimposed on the steady-state value. By changing the amplitude of this small sinusoidal variation and the value of the steady-state V_c , and measuring the duty cycle perturbation's fundamental component, the ratio between A_d and A_c can be obtained and, hence, the describing function gain of DPWM quantizer. Figure 1.8 shows the results.



(a) Different Offsets

(b) Describing Function Gain of DPWM Quantizer

Fig. 1.8 Describing Function Gain of DPWM Quantizer

The resulting describing function gain is quite different from the ADC describing function gain. Because of the different offset, the gain will show quite a big value in the low A_c range. The worst case is to have the offset equal to $0.5q_{DPWM}$; here q_{DPWM} is the step size of DPWM quantizer. In this case, the gain will approach to infinity at very small A_c . Physically, it means that although the perturbation amplitude at the input of DPWM is quite small, but the perturbation amplitude at the duty cycle is constant and the ratio between these two becomes larger. Actually, the perturbation of the duty cycle at this case is normally equal to one step of DPWM resolution, q_{DPWM} .

This characteristic of DPWM quantizer causes a problem in digital controlled DC/DC converter: because of this large gain, even a very small perturbation at the input of DPWM will cause a certain amount of oscillation at the duty cycle and hence at output voltage. The observation that DPWM can contribute an effective gain much larger than 1

has an important consequence in the construction of the system dynamic model and derivation of additional no-limit-cycle conditions [6], which will be covered in section 1.4.

1.3. Modeling for Sample-hold Effect

Since the digital control chip can only process the discrete-time samples of signals, sampling action is necessary to discretize the analog, continuous signal into a discrete-time signal. When the compensator finishes the processing task of those discrete-time signals, the discrete-time control command V_c^* should be compared with the ramp produced by clock, as shown in figure 1.3. In this case, a register is necessary to hold the value of V_c^* and to be able to compare with digital ramp. So there will be a hold function from this register.

Then the ADC's sampling function and the DPWM register's hold function act as a sample-hold function for the whole system.

1.3.1. Classical Model for Sample-hold Effect in digital control

Literature [19] analyzes the typical transfer function for sample and hold and also shows the effect associated with the hold: delay. Later, literature [15] utilizes these kinds of analysis for sample and hold function in the digital controlled DC/DC converter application. To simplify the analysis, the sample and hold can be separated into two mathematical operations: a sampling operation represented by impulse modulation and a hold operation represented as a linear filter. Figure 1.9 shows the symbol or schematic of the ideal sampler and gives a mathematical representation of the process of taking periodic samples.

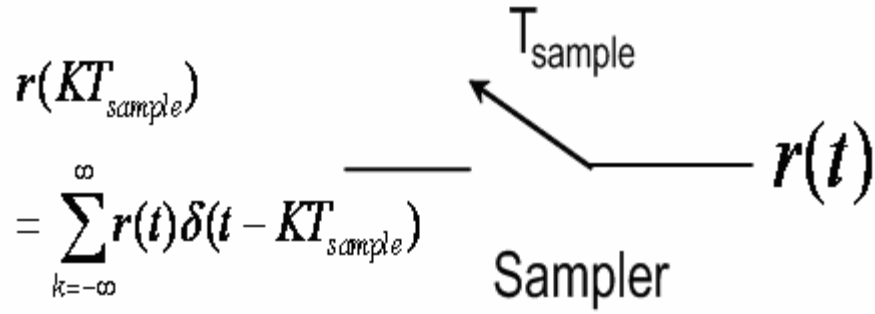


Fig. 1.9 The sampler

From the above figure, it is quite clear that the signal after sampler is a product of the original signal and the train of impulses, $\sum \delta(t - kT_{sample})$. The latter series is periodic and can be represented by a Fourier series:

$$\sum_{k=-\infty}^{\infty} \delta(t - kT_{sample}) = \frac{1}{T_{sample}} \sum_{n=-\infty}^{\infty} e^{j(2\pi n/T_{sample})t} \quad (2)$$

Take the Laplace transform of the output of the mathematical sampler, after a certain mathematical derivation; we can get the result as:

$$R^*(s) = \frac{1}{T_{sample}} \sum_{n=-\infty}^{\infty} R(s - j \cdot n \cdot \omega_{sample}) \quad (3)$$

This equation shows that after the sampler, a never-ending train of sidebands is produced.

Now we need to model the hold operation to complete the description of the physical sample-and-hold. The hold operation can be defined as,

$$r_h(t) = r(kT_{sample}) \quad kT_{sample} \leq t < kT_{sample} + T_{sample}. \quad (4)$$

This extrapolation is a zero-order polynomial, and is called a zero-order hold. The transfer function is designated as ZOH(s),

$$ZOH(s) = \frac{1 - e^{-sT_{sample}}}{s} \quad (5)$$

So we can have the following equation:

$$R_H(s) = R^*(s) \cdot \frac{1 - e^{-sT_{sample}}}{s} = \frac{1}{T_{sample}} \sum_{n=-\infty}^{\infty} R(s - j \cdot n \cdot \omega_{sample}) \cdot \frac{1 - e^{-sT_{sample}}}{s} \quad (6)$$

In the frequency range lower than half of sampling frequency, the following approximate transfer function can be obtained for the sample-and-hold:

$$SH(s) = \frac{1 - e^{-sT_{sample}}}{sT_{sample}} \quad (7)$$

For this transfer function, the delay associated with the hold can be calculated,

$$\delta\phi = -\frac{\omega T_{sample}}{2} \quad (8)$$

1.3.2. Zero-order-hold Model in DPWM

Actually the above classical sample-and-hold model is not valid for the application of the DPWM controlled DC/DC converter; the delay associated with the hold is over-estimated. The reason is that in a previous sample-and-hold modeling, the Pulse Width Modulator's effect is not taken into consideration in deriving the hold transfer function. So when we apply the above transfer function of sample-and-hold into the loop design, the delay is over-estimated in small duty-cycle case. Literature [2-3] develops a more reasonable zero-order hold model for DPWM.

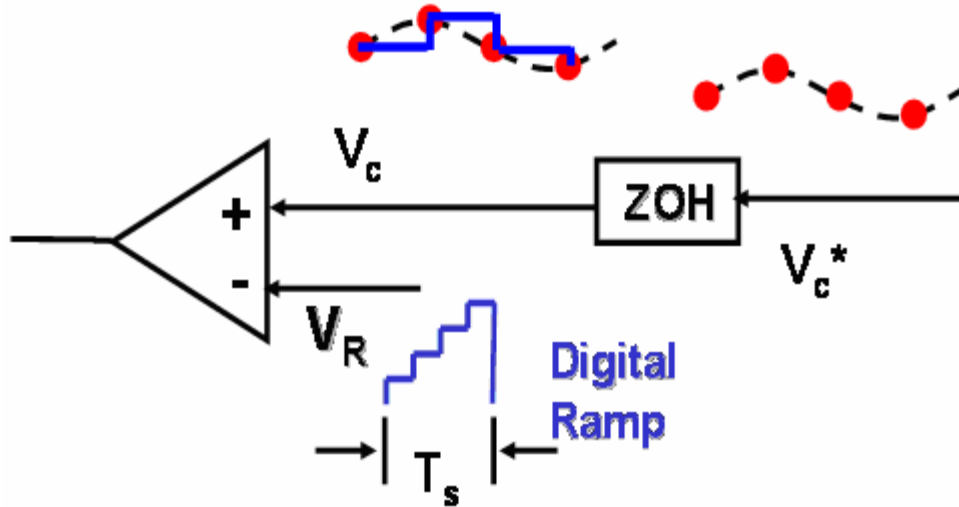


Fig. 1.10 Typical Blocks of Zero-order-hold Effect in DPWM

Figure 1.10 shows the typical waveform for the zero-order-hold effect in digital PWM. The discrete-time signal goes through the zero-order-hold block of DPWM and will give us the piece-wise constant output. Finally, this piece-wise constant control signal is compared with the ramp to determine the duty cycle. A conceptual drawing is shown in figure 1.11. Here the digital ramp is simplified as a continuous ramp in order to ignore the quantization effect at first.

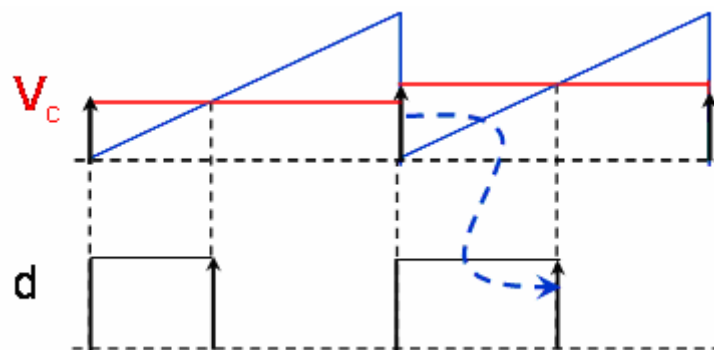


Fig. 1.11 Typical Waveform of Zero-order-hold Effect in DPWM

The associated delay in a steady state can be derived:

$$ZOH(s) = e^{-s(D \cdot T_s)} \quad (9)$$

T_s is the switching frequency in figure 1.11.

In this case, we show the one sample one cycle case; later literature [24] studies the multi-sample one cycle case and gives the zero-order-hold delay equation in that case.

$$ZOH(s) = e^{-s t_d} \quad (10)$$

Here, t_d is a quite complex one as shown,

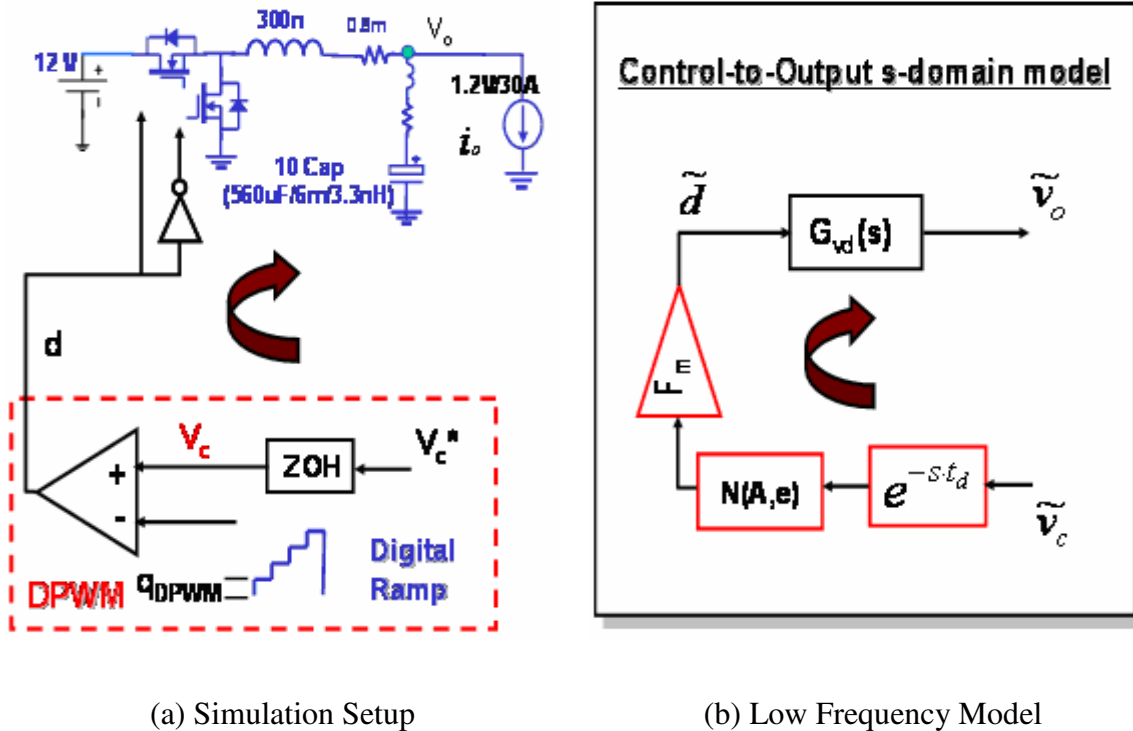
$$t_d = D \cdot T_s - \frac{\text{floor}(N \cdot D)}{N} \cdot T_s \quad (11)$$

1.4. Modeling of Feedback Control

Before we can design the system, the system model will be developed in this subsection.

1.4.1. A DPWM model

Based on the above analysis, a DPWM model can be obtained by combining the zero-order-hold model with the quantizer model into the PWM block.



(a) Simulation Setup

(b) Low Frequency Model

Fig. 1.12 A DPWM Model

As figure 1.12 shows, the DPWM model is separated into three parts to represent three different kinds of effects. The delay term represents the delay, which originated from zero-order-hold effect of the DPWM's register. The nonlinear gain $N(A,e)$ is to model the DPWM's quantizer and the F_m is the modulator gain.

Now we are going to use the simulation to verify this model.

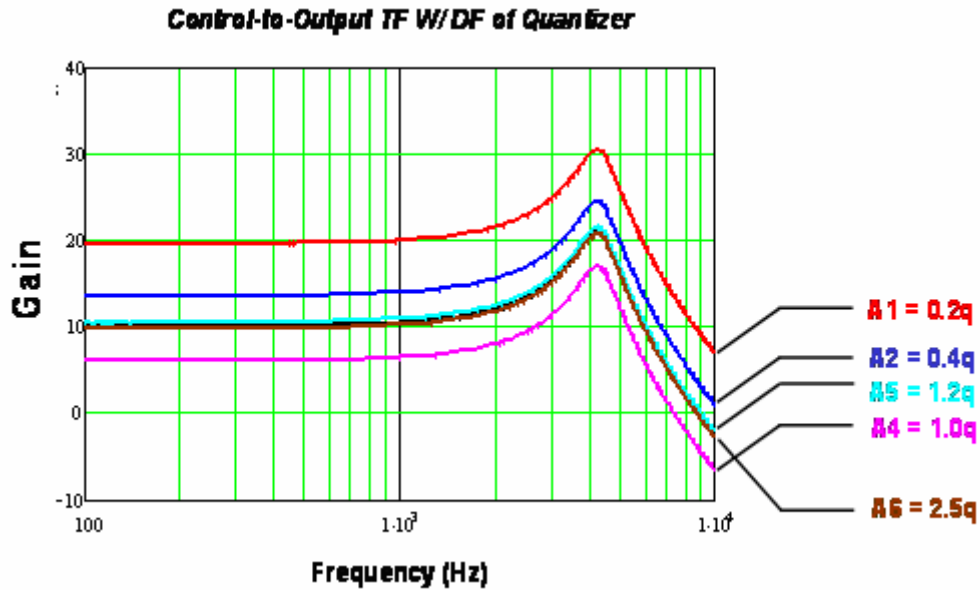


Fig. 1.13 Verification of Quantization Effect ($q = q_{\text{DPWM}}$)

The simulation waveforms for the control-to-out at different oscillation amplitudes are shown in figure. 1.13; here the offset is selected to be 0.5, the worst case. From this simulation, we can see the effect of the nonlinear gain, which is quite different from analog case. The simulation software is PSIM.

Figure 1.14 shows the comparison between the model and simulation waveform. There is one sample in one switching cycle, which basically means the control update's frequency is the same as the switching frequency. In these simulations, we change the switching frequency from 300 kHz to 1 MHz. From this comparison, it is quite clear that this model is valid in up to half of the switching frequency. For the usual power supply design, since the bandwidth is relatively low, as compared to the switching frequency, this low frequency model is good enough.

However, for the multi-phase voltage regulator module application, the preferred bandwidth is quite high. This model is needs to be adjusted to accommodate this stringent requirement. For this high frequency modeling part, literature [16] already discussed it.

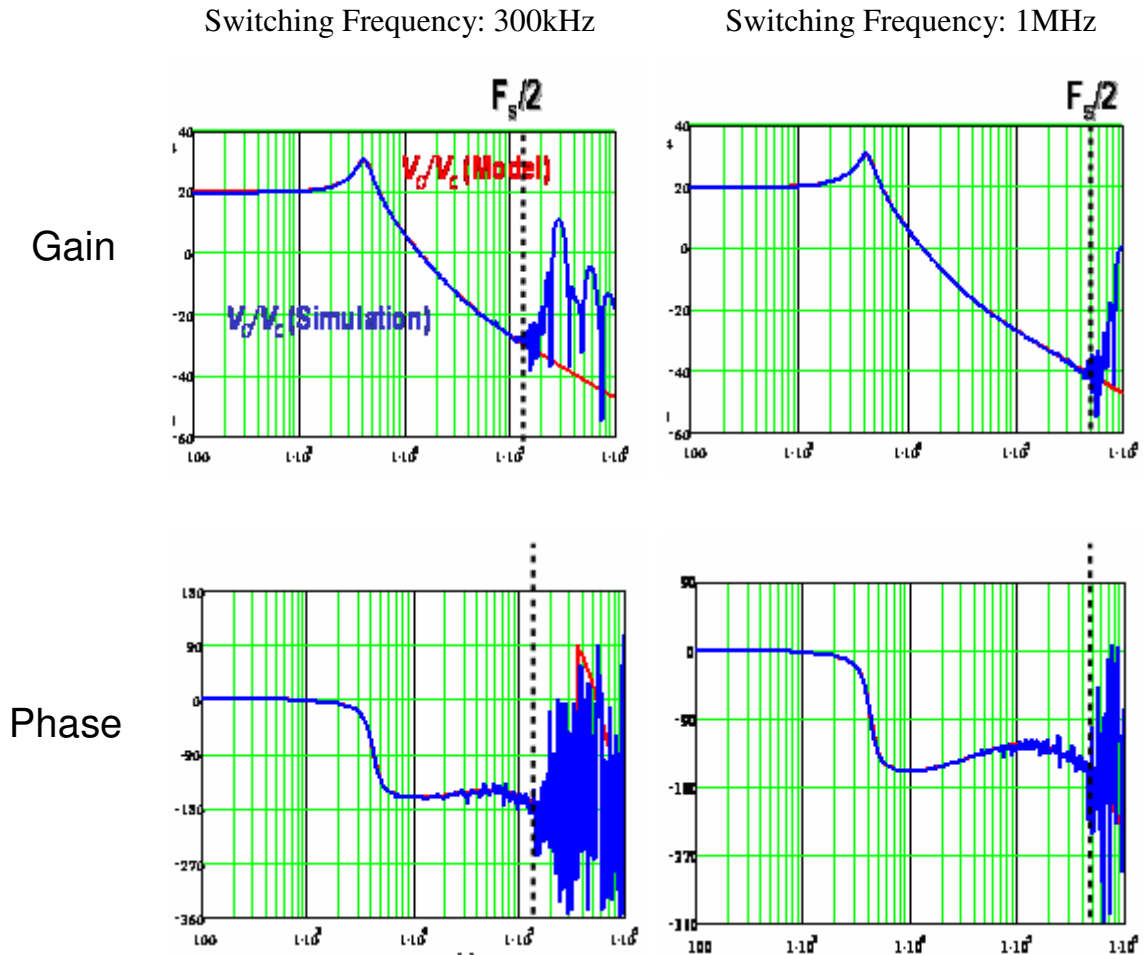


Fig. 1.14 Comparison between Model and Simulation: one sample one cycle

The above simulation focuses on one sample one cycle case. Figure 1.15 verifies the multi-sample one cycle case and shows the similar results. The switching frequency is fixed at 300 kHz and so the model validation is still up to half of switching frequency. By comparing 8 samples in one cycle with the 1 sample in one cycle case, it is quite obvious that there is almost no change in the gain, but the phase is raised a little bit due to the multi-sampling technique. This can help us to push the bandwidth.

However, the more the samples we use, the faster the ADC we need, the higher the compensator's calculation speed, and the higher the cost. This put a big issue for digital control to achieve high bandwidth and fast transient. To alleviate this transient problem,

several companies propose nonlinear methods to help the digital control chip deal with this issue. For example, the Primarion utilizes the ATR to achieve the fast transient [18], while the Silabs uses two set of compensators and multi-sampling techniques [25].

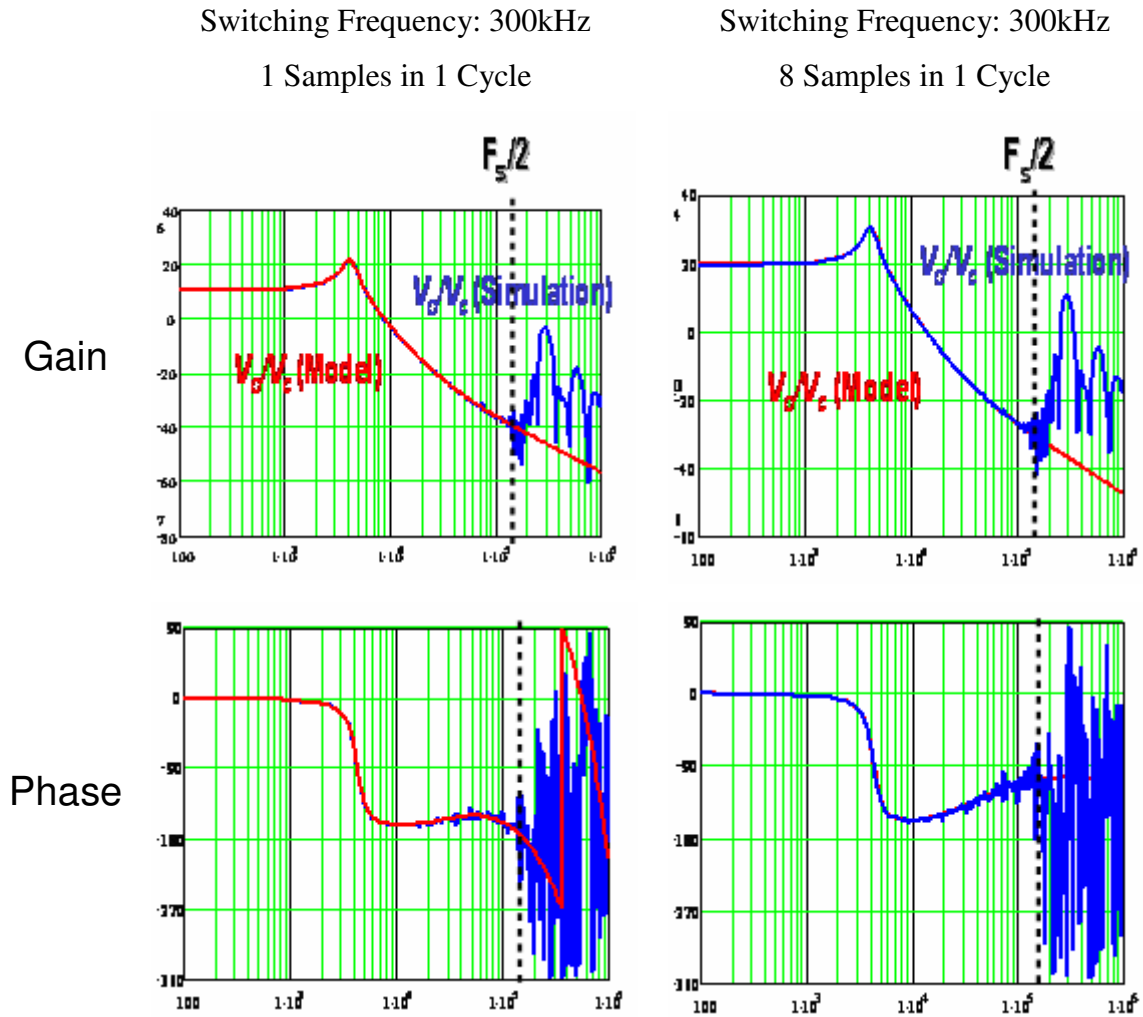


Fig. 1.15 Comparison between Model and Simulation: multi-samples one cycle

1.4.2. An ADC model

Here, we make a simplification to the ADC model. As we know, it has the quantization operation, and the sampling operation, but it also needs a certain amount of conversion time. This time comes between when the ADC gets the command to do the sampling from controller and when the samples of the signals are being sent to the controller.

Normally the amount of delay is quite small for the fast ADC. The ADC's model is composed of three blocks as shown in figure 1.16.

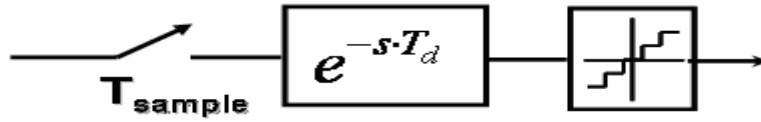
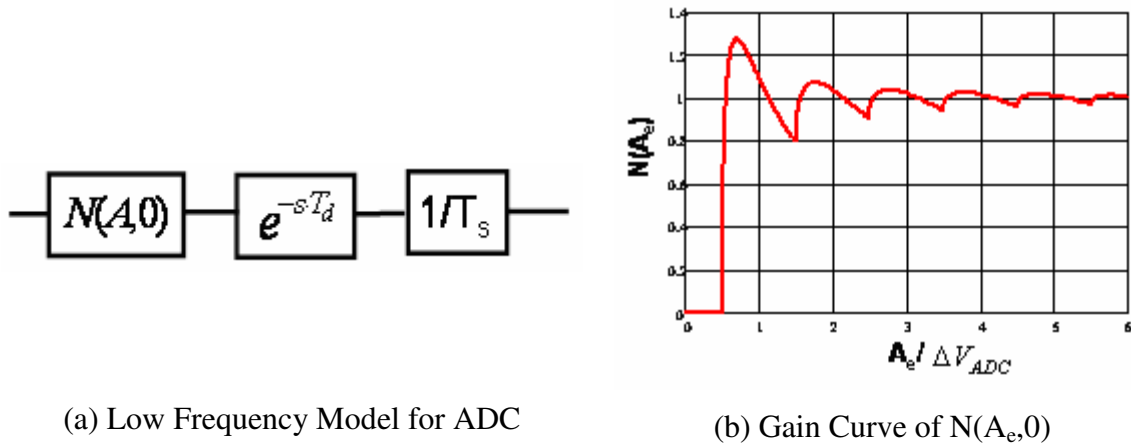


Fig. 1.16 ADC Blocks

From previous analysis, we know that the signal before the sampler and after the sampler has a relation as,

$$R^*(s) = \frac{1}{T} \sum_{n=-\infty}^{\infty} R(s - j \cdot n \cdot \omega_s) \quad (12)$$

This equation describes the aliasing effect caused by the sampling action. Since we are considering a frequency range below half that of the sampling frequency, and also because the power stage and compensator has low-pass characteristics, we can ignore the aliasing effect originates from the sampler. Then the ADC model is reduced to:



(a) Low Frequency Model for ADC

(b) Gain Curve of $N(A_e, 0)$

Fig. 1.17 Low Frequency ADC Model

1.4.3. Loop Model

In previous subsections, we have developed the models for the sample-and-hold effect and also the quantization effect, both for the ADC and the DPWM. So we can construct a loop model for digital voltage-mode constant frequency control.

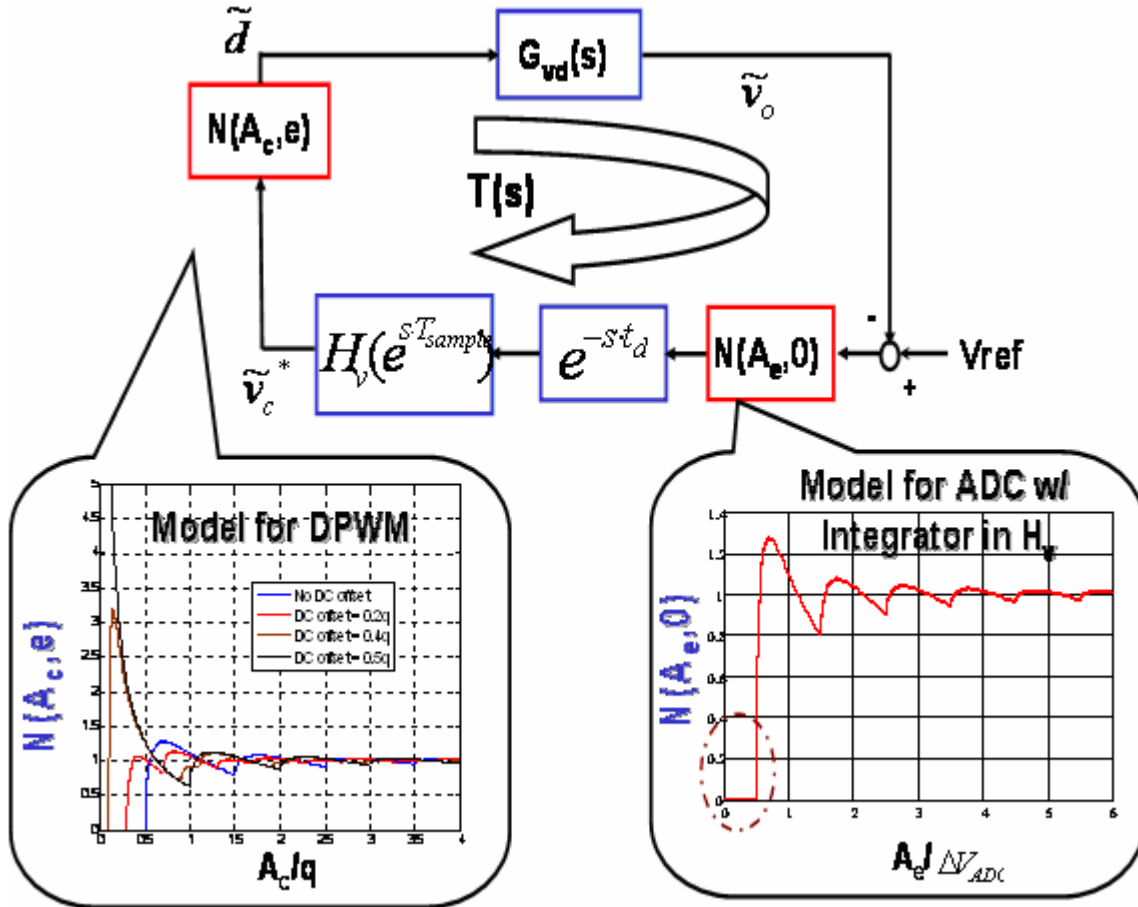


Fig. 1.18 Loop Model ($q = q_{DPWM}$)

Here the delay from both the ADC and the DPWM are integrated into the delay t_d , so the total delay for one sample one cycle case should be:

$$t_d = t_{conv} + t_{cal} + D \cdot T_s \quad (13)$$

Here, t_{conv} is the conversion time of ADC, t_{cal} is the calculation time needed to do the compensation and $D \cdot T_s$ is the delay from the hold function of DPWM. The gain of F_m

and $1/T_s$ is already absorbed by the compensator. The t_{conv} is actually the t_d in previous ADC model.

1.5. Design Methodology for Constant Frequency Digital Voltage-Mode Control

Previously, we reviewed the model for digital control's two effects: sample and hold effect and quantization effect, and also pointed out the issues: the limit cycle oscillation issue caused by quantization effect and the transient issue caused by the delay coming from hold effect. Actually the conversion delay from ADC and the calculation delay from the digital compensator also become an issue for transient. Now in this section, we are going to introduce the design aspects focusing on the first issue, limit cycle oscillation. In this design methodology, the constant frequency voltage-mode control is the study objective, as shown in figure 1.1 and repeated in figure 1.19.

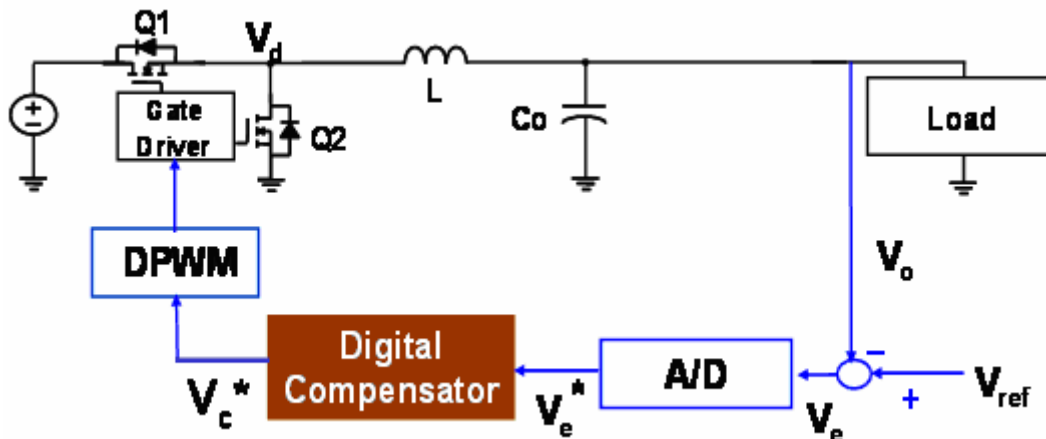


Fig. 1.19 A Constant-Frequency Digital Voltage-Mode Control

About the design for transient, a lot of work has been done, especially in voltage regulator application; the most important indication for fast transient in linear control is the bandwidth. For nonlinear control, one direct thought is to use a linearization method, like the describing function, to get the model for the nonlinear control in frequency

domain. Then a similar concept in linear control can be utilized. Another thought is to use a state trajectory to get time-domain information, like peak value of voltage during transient to help the design.

However, except the issue of transient, the limit cycle oscillation is also a quite important issue in low voltage application. Hence how we design the system to eliminate the limit cycle oscillation becomes quite an important target. In this section, the solution for this issue is reviewed.

Currently, the literature [6] that investigates this issue is the most complete. As shown in figure 1.18, the dynamic model for the system of figure 1.19 is developed, where the two quantizers are replaced by the gain model which is amplitude and offset dependent. Based on the model of in figure 1.18 and the describing functions from the previous section, the existence, frequency and amplitude of a sinusoidal limit-cycle oscillation can be obtained.

Let $T_L(s)$ be the linear part of the loop gain, which does not include the quantizers,

$$T_L(s) = G_{vd}(s) \cdot H_v(e^{sT_{sample}}) \cdot e^{-sT_d} \quad (14)$$

As we know, the describing functions of the quantizers are independent of frequency, and do not introduce a phase shift between the input sinusoidal signal and the fundamental component of the output signal. Therefore, from linear system theory, if a limit-cycle oscillation exists, the oscillation frequency f_x is such that:

$$\angle T_L(j \cdot \omega_x) = -180^\circ \quad (15)$$

Suppose that the amplitude of the signal V_e at the input of the ADC is a . Then at the frequency f_x , the magnitude of the amplitude/offset-dependent system loop gain $T(a, e)$ can be found as follows:

$$\|T(a, e)\| = \frac{v_o}{d} \cdot \frac{d}{v_c} \cdot \frac{v_c}{v_e} \cdot \frac{v_e}{e} \quad (16)$$

Here e is the error between output voltage and reference voltage: $e = V_{ref} - V_o$.

The above equation can be further expressed as,

$$\begin{aligned} \|T(a, e)\| &= \frac{v_o}{d} \cdot \frac{d}{v_c} \cdot \frac{v_c}{v_e} \cdot \frac{v_e}{e} \\ &= \|G_{vd}(j \cdot \omega_x)\| \cdot N_{DPWM} (\|G_c(j \cdot \omega_x)\| \cdot N_{A/D}(a, 0) \cdot a, e) \cdot \|G_c(j \cdot \omega_x)\| \cdot N_{A/D}(a, 0) \end{aligned} \quad (17)$$

If there exists an amplitude a_x and an offset e_x such that

$$\|T(a_x, e_x)\| = 1 \quad (18)$$

And

$$\left. \frac{\partial \|T(a, e_x)\|}{\partial a} \right|_{a=a_x} < 0 \quad (19)$$

A near-sinusoidal limit-cycle oscillation of amplitude a_x and frequency f_x will occur in the system.

Based on above equations, the no-limit-cycle conditions and design guidelines can be formulated.

1.5.1. Static Condition

The DPWM has the resolution problem due to quantization effect; the minimal time slot for on-time and switching cycle is the clock cycle, shown in figure 1.20.

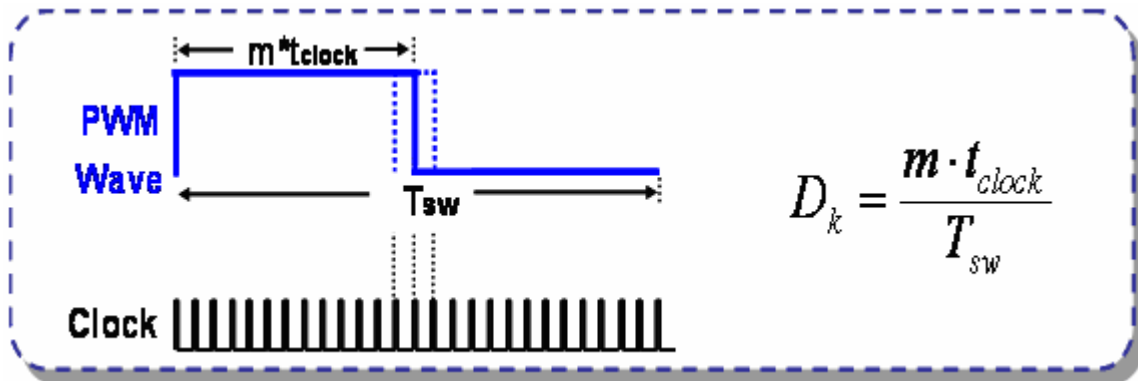


Fig. 1.20 Resolution of Duty Cycle

Then it is quite obvious for us to imagine that for the buck converter, the steady-state output voltage can be a set of discrete values:

$$V_o = D_k \cdot V_{in} = \frac{m \cdot t_{clock}}{T_{sw}} \cdot V_{in} \quad (20)$$

The minimum step change of output voltage is

$$\Delta V_o = \frac{t_{clock}}{T_{sw}} \cdot V_{in} = \frac{1}{n} \cdot V_{in} \quad (21)$$

Here, n is the number of clocks in one switching cycle and m is the number of clocks of on-time. So in the steady-state, the output voltage can only achieve these values and the minimum increment is ΔV_o .

The ADC also has the resolution requirement. If the DPWM resolution is less than the ADC resolution, and there is no DPWM level that maps into the ADC bin corresponding to the reference voltage, then the controller will alternate between the DPWM levels around the ADC bin corresponding to the reference voltage. This is because in a steady-state the controller will attempt to drive V_o to this bin. This bin is referred to as the zero-error bin. Figure 1.21 shows an illustration of two cases [5].

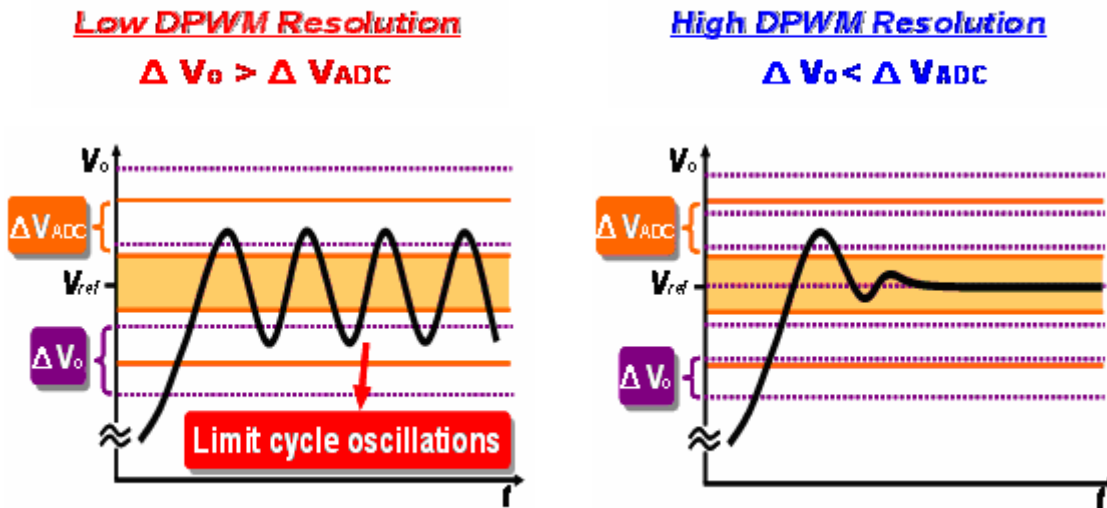


Fig. 1.21 DPWM Resolution's Influence on Limit Cycle Oscillation

From [5] and [6], a necessary no-limit-cycle condition is developed:

$$\Delta V_o = \frac{1}{n} \cdot V_{in} < \Delta V_{ADC} \quad (22)$$

Here, ΔV_{ADC} is the resolution of voltage ADC. In [6], a coefficient is added in this inequality to give some design margin.

This condition is only the necessary condition. If we cannot meet this condition, the limit cycle oscillation is always happening. Later, in the current-mode control case, we develop a corresponding condition for that structure. However, to eliminate the limit cycle oscillation, more efforts should be paid. Literature [6] develops a modeling approach to tackle this issue.

1.5.2. Dynamic Condition

Here the literature [6] will be referred to in this subsection. A dynamic no-limit-cycle condition follows from the previous discussion. Let f_x be a frequency where the following equation is satisfied:

$$\angle T_L(j \cdot \omega_x) = -180^\circ \quad (23)$$

The dynamic no-limit-cycle condition is:

$$\|T(a, e)\| < 1 \quad (24)$$

For all $a > \frac{\Delta V_{ADC}}{2}$ and $0 \leq e \leq \frac{q_{DPWM}}{2}$, where a is the amplitude of the signal at the input of ADC.

This general dynamic no-limit-cycle condition leads to two simple no-limit-cycle conditions in terms of the ADC and the DPWM resolutions, and the converter and compensator parameters.

B.1 The worst-case (infinite) DPWM gain, which occurs for $e = q_{DPWM} / 2$, is canceled by the zero gain of the ADC for signal amplitudes $a < \Delta V_{ADC} / 2$:

$$\frac{4}{\pi} \|G_{vd}(j \cdot \omega_x)\| \cdot q_{DPWM} < \Delta V_{ADC} \quad (25)$$

A very large effective DPWM gain is a result of a very small amplitude signal at the DPWM input around the worst-case offset. In this case, the DPWM output is a square wave of amplitude q_{DPWM} , and $\frac{2}{\pi} \cdot q_{DPWM}$ is the amplitude of the corresponding fundamental component at f_x . The dynamic condition B.1 is the condition that the resulting amplitude a at the ADC input is smaller than $\Delta V_{ADC} / 2$.

Actually from the DPWM gain curve, we can also observe that when the oscillation amplitude at the input of DPWM is quite small, the DPWM gain will become infinite at worst-case offset.

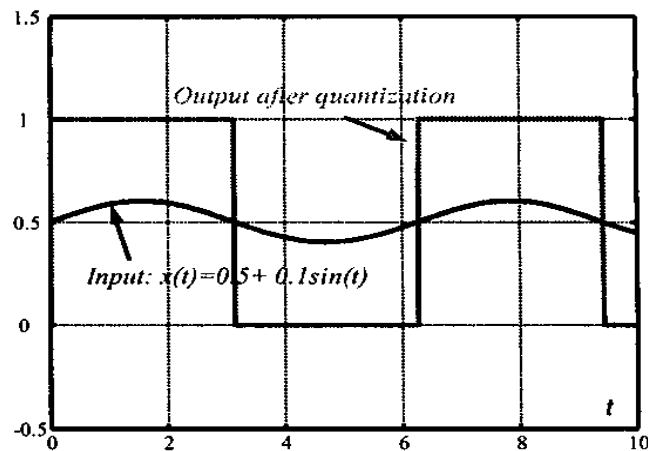


Fig. 1.22 An Illustrative Case of DPWM Large Gain at Worst-case Offset

Figure 1.22 shows an illustrative case about this quite large gain with $q_{DPWM} = 1$. As we can see the offset of the input sinusoidal oscillation is at 0.5, half of DPWM level, which

is the worst case offset. In this case, although the amplitude of input sinusoidal is quite small, 0.1, but the output oscillation of DPWM is a square waveform and the amplitude is one DPWM level, 1.0. So when we calculate the ratio between the input sine wave's amplitude and the output fundamental component's amplitude, the gain should be $\frac{2}{\pi} \cdot 0.5$. If the input sine wave's amplitude becomes smaller and smaller, this gain will increase further.

Since it is not possible to deal with this high gain using the linear compensator, one thought is to tackle this by using the ADC zero gain. The output oscillation of the DPWM will propagate through the power stage and produce output voltage oscillation. If this output voltage oscillation is located in the zero-error bin of the ADC, then the ADC output will be zero, which means the controller will not respond to this oscillation. Hence this oscillation can be avoided. Based on this concept, we need to know the output voltage oscillation due to one DPWM level oscillation at the output of DPWM.

Since we are concerned about the sinusoidal oscillation, the square waveform output of DPWM should be processed with Fourier analysis in order to get the fundamental component. With Fourier analysis, we know that to a square waveform with amplitude one q_{DPWM} as shown in figure 1.22, the amplitude of its fundamental component can be easily obtained:

$$\tilde{v}_d = \frac{2}{\pi} \cdot q_{DPWM} \quad (26)$$

Now this oscillation goes through the power stage and produces the output voltage oscillation, as shown in figure 1.23.

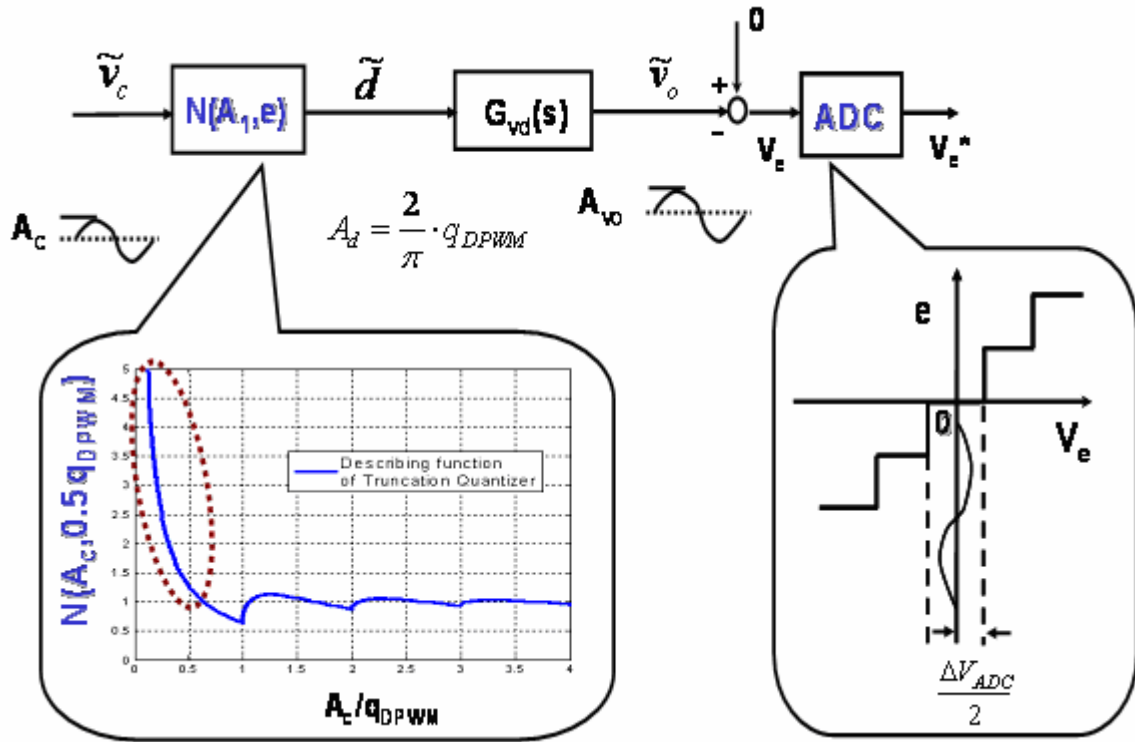


Fig. 1.23 Oscillation Propagation

The output voltage oscillation amplitude should be:

$$\tilde{v}_o = \frac{2}{\pi} \cdot q_{DPWM} \cdot \|G_{vd}(j\omega_x)\| \quad (27)$$

If this output voltage oscillation amplitude is smaller than half of ADC zero-error bin size, then this oscillation can be avoided. So the no-limit-cycle oscillation condition B.1 is produced and repeated here again:

$$\frac{4}{\pi} \|G_{vd}(j \cdot \omega_x)\| \cdot q_{DPWM} < \Delta V_{ADC} \quad (28)$$

B.2 The gain margin GM_L of the linear part of the system is sufficiently high:

$$GM_L > 20 \cdot \log\left(\frac{4}{\pi}\right)^2 = 4.2 \text{ dB} \quad (29)$$

If a signal at the DPWM output oscillates between only two adjacent quantization levels, then the no-limit-cycle condition B.1 applies. If the DPWM output steps over three or

more levels, then the effective DPWM gain cannot be greater than $\frac{4}{\pi}$, for any offset value e . Therefore, under the assumption that the signal at the DPWM output spans over more than two quantization levels, the combined DPWM and ADC gain cannot exceed $(\frac{4}{\pi})^2 = 1.62$, which gives the no-limit-cycle condition B.2.

When the DPWM output steps more than two levels, the input oscillation of DPWM should also become larger than one step. In this case, the gain of the DPWM quantizer will decrease and converge to one and in this gain range, the maximum value is $\frac{4}{\pi}$. Taking the ADC gain maximum value into consideration, we will have a maximum gain incremental equal to the square of $\frac{4}{\pi}$. This gain increase, since it is finite, can be compensated by the digital compensator. The gain margin concept is used for this case as shown in an above no-limit-cycle condition B.2.

The static condition and dynamic condition B.1 clearly indicates the need for a high-resolution DPWM. The condition B.2 has direct implications on the compensator design: the compensator must include an integral action and must result in a sufficiently large gain margin of the linear part. As further pointed out by the literature [6], in all cases, to avoid limit-cycle oscillations, the static condition must be satisfied. In applications with a relatively fast controller, the oscillation frequency f_x is relatively high. In this condition, in addition to the static condition, the condition B.2 must be taken into consideration.

1.6. Thesis Objective and Outline

The DPWM resolution for digital voltage-mode controlled buck converter is as shown:

$$\Delta V_o = \frac{1}{n} \cdot V_{in} = \frac{T_{clock}}{T_{sw}} \cdot V_{in} \quad (30)$$

From the steady-state condition, we know that if ΔV_o is small enough there is more possibility to eliminate the limit cycle oscillation. Based on this thought, many researchers studied methods to make the T_{clock} or the equivalent T_{clock} to be as small as possible. One quite straightforward method is to push the clock frequency to be higher. Literature [12] uses a ring-oscillation instead of a counter to construct the DPWM, hence providing a more fine time slot for T_{clock} . Similarly, the CoPEC proposed the delay-line concept to achieve a similar goal [21]. However, the pure ring-oscillation or pure delay-line structure DPWM gives the problem of high cost and larger silicon area. So the hybrid structure is proposed to make a trade-off between resolution and cost [9].

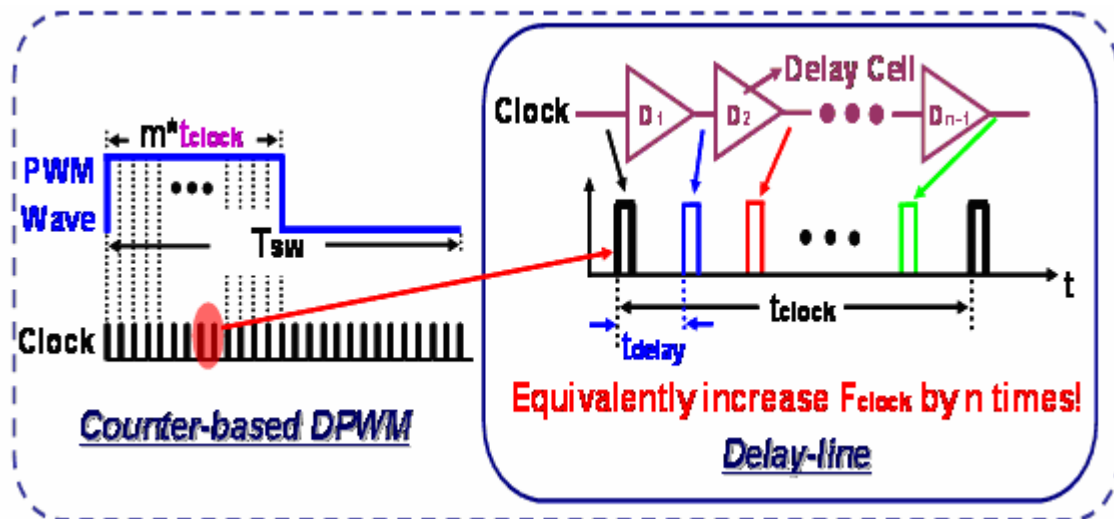


Fig. 1.24 Concept of Hybrid DPWM

Based this hybrid structure, the industry companies, like TI and Primarion, develops their products. However, with high resolution of DPWM, it is not guaranteed that limit cycle

oscillation can be avoided since high resolution only provides the benefits of reducing the possibility of limit cycle oscillation.

Another way of achieving high resolution while alleviate the cost issue is developed in literature [13]. In this literature, the dithering method is proposed to get the high resolution. However, the dither method will introduce the low frequency ripple into the loop, which although is predictable, still makes the system worse. The industry company Silicon Lab utilizes this dithering concept by developing a random dither pattern to alleviate the low frequency ripple problem. But the effect does not seem good enough.

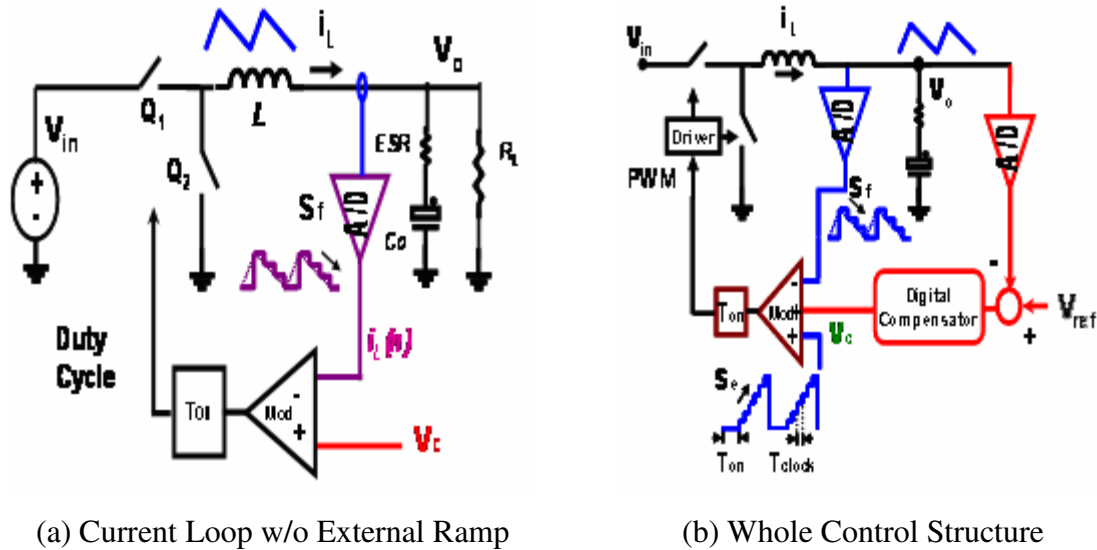
CPES proposes another method to accomplish the high resolution. The constant on-time modulator is introduced into digital control. In constant on-time control, the DPWM resolution can be expressed as:

$$\Delta V_o = \Delta D \cdot V_{in} = \left(\frac{m}{n} - \frac{m}{n+1} \right) \cdot V_{in} = \frac{m}{n \cdot (n+1)} \cdot V_{in} \approx D \cdot \frac{1}{n} \cdot V_{in} \quad (31)$$

When comparing these two resolution equations, we can see that the constant on-time modulator provides smaller ΔV_o , especially when the steady-state duty cycle is quite small.

However, for the single-loop voltage-mode control, although the constant on-time modulator can provide the higher resolution and fine ΔV_o , the limit cycle oscillation amplitude is still hard to predict

Based on this concern, CPES further investigates the current-mode control structure and proposes the digital constant on-time current-mode control [33] as shown in figure 1.28.



(a) Current Loop w/o External Ramp

(b) Whole Control Structure

Fig. 1.25 Digital Constant On-time Current-Mode Control

Based on our study, we find that this kind of digital control structure will provide us the limit of oscillation amplitude in current loop. By proper design of current ADC and voltage ADC, we can achieve this limit function. By further adding the external ramp, we can reduce the oscillation amplitude in current loop and hence on the output voltage. To understand and design this structure is the objective of this thesis.

To fully investigate this structure, a model is developed in chapter 2. This model provides us the design tool for the compensator and also shows some insights on the influence of the external ramp. Simulation verification of the model is provided in this chapter.

In chapter 3, first the limit cycle oscillation issue is studied in the digital constant on-time current-mode control. Then, the steady-state design guideline for current ADC and voltage ADC to satisfy the steady-state no limit-cycle oscillation condition is developed. This aims at minimizing the oscillation in the system. Time-domain simulation shows the validity of this design guideline. Based on the proposed model, the compensator design is performed. The motivation for the compensator design is to push the bandwidth while satisfying the stability condition and the dynamic no-limit-cycle oscillation condition.

Chapter 3 investigates the design of compensator based on the model proposed in chapter 2.

Chapter 4 gives the summary of whole thesis and also the future work.

Chapter 2 Modeling Digital Constant On-time Current-Mode Control

The Previous chapter mentioned the digital current mode constant on-time control structure proposed in CPES. The main benefit of this structure is its ability to limit the oscillation amplitude. However, it is still lacking an analytical tool and a detailed design methodology for it. In this chapter, a model is developed for this structure. The design methodology is studied in chapter 3.

Figure 2.1 shows the system structure for a digital current-mode constant on-time control. This is a two loop structure with two ADCs for inductor current and output voltage. The modulator is the constant on-time modulator. There is an external ramp to help to reduce the limit cycle oscillation.

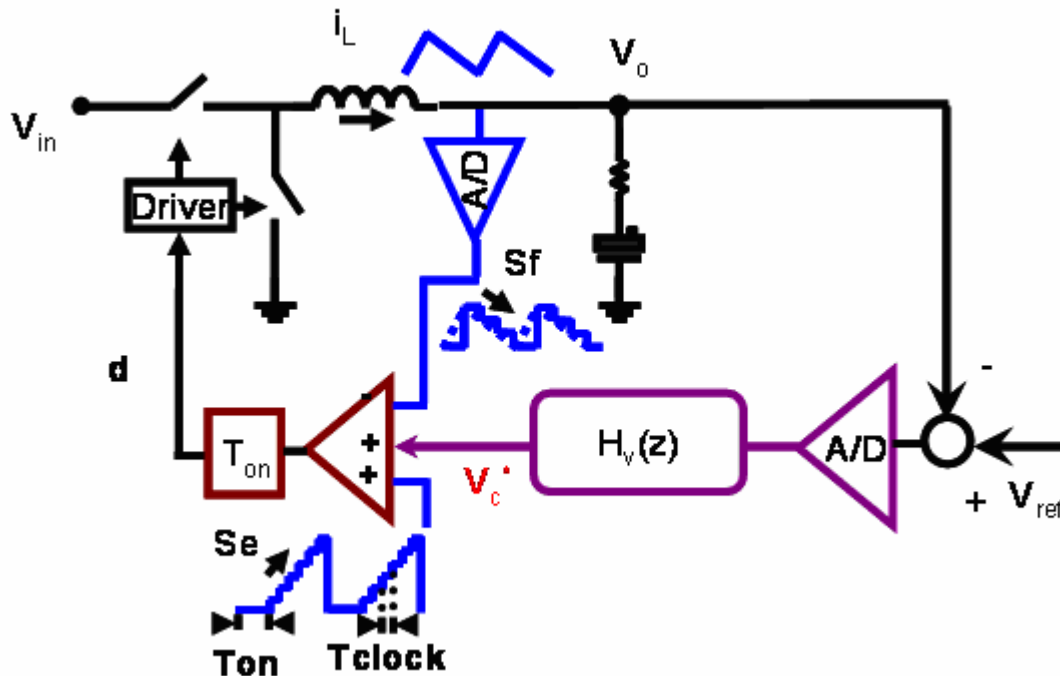


Fig. 2.1 Digital Current-mode Constant On-time Control

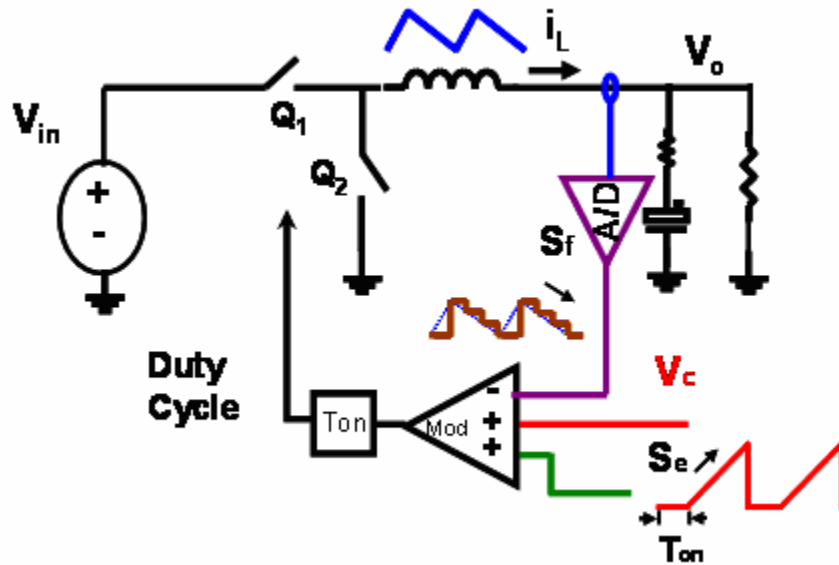
In this structure, we can focus on the current loop at first and develop a model that gives us the small-signal characteristics of control to output voltage, which can be used for compensator design.

In its current-mode cell, there are two origins of quantization effects. One is the quantization effect from the current ADC. Another one is from the clock frequency of the external ramp. Since the clock frequency is quite high and the product of the external ramp's slope and clock cycle is usually smaller than the current ADC's quantization level, it is natural to assume that the quantization effect from the clock frequency can be ignored.

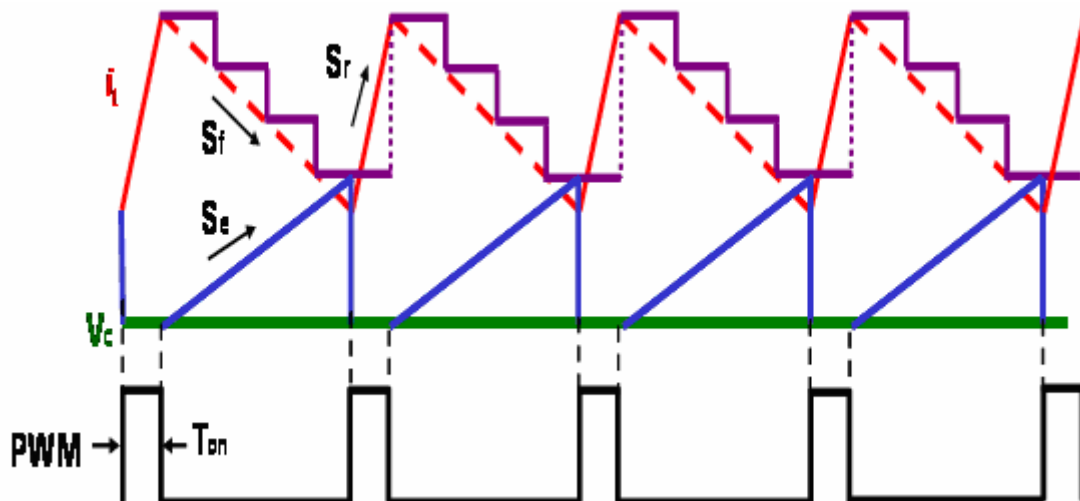
Now after a certain amount of assumptions and simplification, there are only two nonlinear effects related to digital control: the sample-and-hold effect from the current loop ADC and the quantization effect from the current loop ADC. Based on chapter 1's analysis, we know that in modeling the digital controlled DC/DC converter, the sample-and-hold effect and the quantization effect are separately modeled. This methodology will be utilized here.

2.1. Modeling Digital Current-Mode Constant On-time Modulator

In this section, the simplified current cell shown in figure 2.2 will be studied and modeled. And the quantization effect and the sample-and-hold effect will be separately discussed as in chapter 1.



(a) Current-Mode Cell



(b) Typical Waveform

Fig. 2. 2 Digital Current-mode Constant On-time Control: Current Cell

In this control, the sampling mechanism is designed like this: in constant on-time period, there is no sampling signal; while in off-time period, the first sampling signal begins at the end of on-time period, and then samples at a fixed sampling period, which is proportional to switching frequency.

Based on this sampling mechanism, the current waveform is shown in figure 2.2 b. Now we will use the describing function modeling methodology to develop the model for this structure, as shown in figure 2.3.

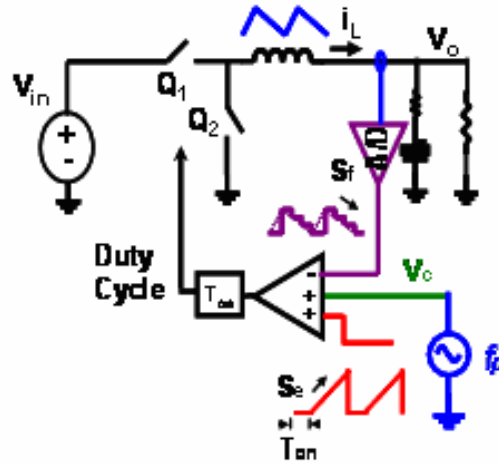


Fig. 2.3 Describing Function Concept to Derive the Model

Assumption: the ramp is continuous in derivation

In this methodology, a sinusoidal perturbation source is superimposed on the steady-state control signal V_c , and the resultant inductor current waveform is being analyzed by the Fourier series to get the fundamental component $i_L(f_p)$. The ratio between the inductor current's fundamental component and the control signal's perturbation is describing function model from control V_c to inductor current i_L :

$$\frac{i_L}{v_c} = \frac{i_L(f_p)}{v_c(f_p)} = DF \quad (32)$$

Here before we derive the model, there are two assumptions.

- (1) In derivation of current cell's model, the fixed input voltage and fixed output voltage is assumed;
- (2) The switching frequency and the perturbation frequency have a relation as:

$$N \cdot f_s = M \cdot f_p \quad (33)$$

Figure 2.4 shows the definition of the waveform for derivation:

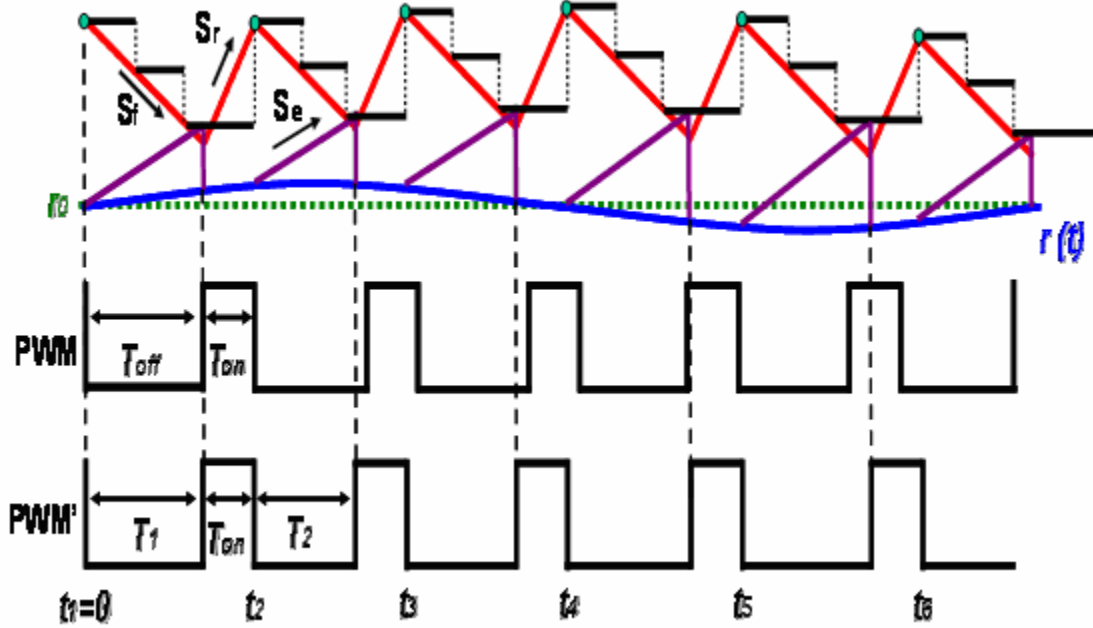


Fig. 2.4 Typical Waveform to Derive the Model

As shown in figure 2.4, the perturbed duty cycle is:

$$r(t) = r_0 + \hat{r} \sin(2\pi f_m \cdot t), \quad \hat{r} \ll r_0, \quad Nf_s = Mf_m \quad (34)$$

Because of this perturbed duty cycle, the off time has a certain amount of perturbation too. Here, PWM denotes the steady-state duty cycle waveform, while the PWM' denotes the perturbed duty cycle waveform, which is also the waveform to be transformed by the Fourier series. As we can see, in steady-state PWM waveform, the off time is also achieving its steady-state value, as T_{off} . While in perturbed PWM waveform, the off time is changed cycle by cycle.

From the assumed time scale, $t_1 = 0$, the first off time is named as T_1 , the second off time is named as T_2 . Following this terminology, and noticing that in small perturbation case the number (N) of sampling cycles in each switching cycle is same, the generalized off-time calculation can be obtained:

$$r(t_{i-1}) + S_e \cdot T_{i-1} - (T_{i-1} - N \cdot T_{sample}) \cdot S_f + S_r \cdot T_{on} = r(t_i) + S_e \cdot T_i + S_f \cdot N \cdot T_{sample} \quad (35)$$

Then we can calculate the off-time perturbation which is caused by the control signal's perturbation. The off-time perturbation is defined as:

$$T_i = T_{off} + \Delta T_i, \quad \Delta T_i \ll T_{off} \quad (36)$$

From the off-time calculation equation, we can have:

$$r(t_{i-1}) + (S_e - S_f) \cdot T_{i-1} + S_r \cdot T_{on} = r(t_i) + S_e \cdot T_i \quad (37)$$

And we also know that:

$$T_{off} = s_n \cdot T_{on} / s_f \quad (38)$$

This is the steady-state condition. Based on the time scale definition in the typical waveform, we have,

$$t_i = (i-1)(T_{on} + T_{off}) + \sum_{k=1}^{i-1} \Delta T_k \quad (39)$$

If we define:

$$m = \frac{S_e - S_f}{S_e} \quad (40)$$

Then when we combine the equations (37), (38), (39), (40), finally we can get the off-time perturbation expression as:

$$\Delta T_i = -\frac{\hat{r}}{S_e} \sin[\pi f_m \cdot (T_{on} + T_{off})] \cdot \left\{ e^{-j\pi f_m (T_{on} + T_{off}) + j2\pi f_m T_{off}} \cdot \frac{m^i - e^{j2\pi f_m i (T_{on} + T_{off})}}{m - e^{j2\pi f_m (T_{on} + T_{off})}} + e^{j\pi f_m (T_{on} + T_{off}) - j2\pi f_m T_{off}} \cdot \frac{m^i - e^{-j2\pi f_m i (T_{on} + T_{off})}}{m - e^{-j2\pi f_m (T_{on} + T_{off})}} \right\} \quad (41)$$

Now from the control signal (v_c) perturbation, we can calculate the off-time perturbation, but our goal is to get the inductor current perturbation's fundamental component. So we apply the Fourier series on the perturbed inductor current waveform:

First, we use a time-domain equation to describe the perturbed inductor current waveform:

$$i_L(t) \Big|_{0 \leq t \leq t_M + T_{off(M)} + T_{on}} = \int_0^t \left[\frac{V_{in}}{L_s} d(t) - \frac{V_o}{L_s} \right] dt + i_{L0} \quad (42)$$

Then the Fourier transform is applied on this inductor current function to get the component at frequency f_p :

$$\begin{aligned} c_m &= \frac{j2\pi f_m}{N\pi} \sum_{i=1}^M \int_{t_i+T_i}^{t_i+T_i+T_{on}} e^{-j2\pi f_m t} dt \cdot \frac{V_{in}}{L \cdot j \cdot 2\pi \cdot f_m} \\ &= \frac{j2\pi f_m}{N\pi} e^{-j2\pi f_m T_{off}} (e^{-j2\pi f_m T_{on}} - 1) \left[\sum_{i=1}^M (e^{-j2\pi f_m (i-1)(T_{on}+T_{off})} \sum_{k=1}^i \Delta T_k) \right] \cdot \frac{V_{in}}{L \cdot j \cdot 2\pi \cdot f_m} \end{aligned} \quad (43)$$

In this equation, we note that there is a term containing the off-time perturbation. Then we substitute the off-time perturbation equation into the Fourier coefficient equation:

$$\frac{i_{L(f_m)}}{v_{c(f_m)}} = \frac{c_m}{\hat{r}} = \frac{1}{s_e \cdot T_s} (e^{-j2\pi f_m T_{on}} - 1) \frac{e^{j2\pi f_m (T_{on}+T_{off})}}{m - e^{j2\pi f_m (T_{on}+T_{off})}} \cdot \frac{V_{in}}{L \cdot j \cdot 2\pi \cdot f_m} \quad (44)$$

Finally, we can get the describing function for the structure shown in figure 2.4 a:

$$\frac{i_L(s)}{v_c(s)} = \frac{1}{S_e \cdot T_s} (e^{-sT_{on}} - 1) \frac{e^{sT_s}}{m - e^{sT_s}} \cdot \frac{V_{in}}{L \cdot s} \quad (45)$$

Here, $T_s = T_{on} + T_{off}$ is the steady-state switching cycle.

The above model is based on the assumption that the input and output voltage is fixed during derivation. If we take these two perturbations into consideration, we will have another two coefficients from the input and output voltage perturbation to inductor current perturbation signal. Please refer to [33] and the results are shown here:

k1 gain (from input voltage perturbation to inductor current perturbation):

$$k_1 = \frac{R_i \cdot \hat{i}_{L,ave}}{\hat{v}_{in}} = S_e \cdot \frac{1}{V_o} \cdot T_{on} + \frac{R_i}{2L_s} T_{on} \quad (46)$$

k2 gain (from output voltage perturbation to inductor current perturbation):

$$k_2 = \frac{R_i \cdot \hat{i}_{L,ave}}{\hat{v}_o} = -\frac{R_i}{2L_s} T_{on} - S_e \cdot \frac{V_{in}}{V_o^2} \cdot T_{on} \quad (47)$$

2.2. Modeling Quantization Effect from Current ADC

Now we finish the describing function model for the digital constant on-time current-mode cell while only considering the sample-and-hold effect. We need to model the quantization effect to complete the whole model.

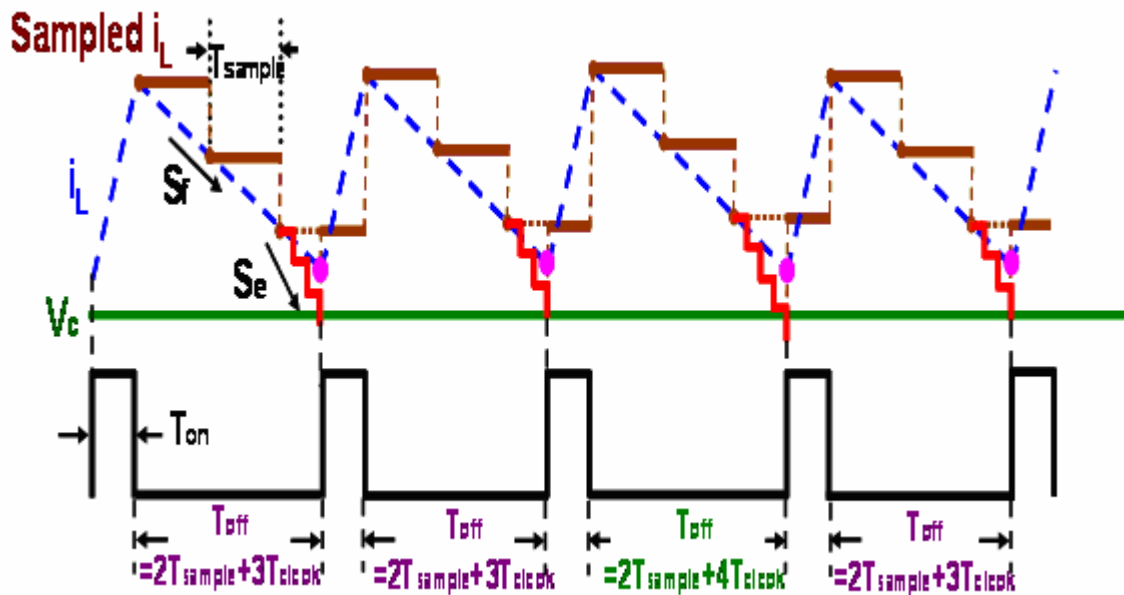


Fig. 2.5 ADC Output Current Waveforms without Quantizer

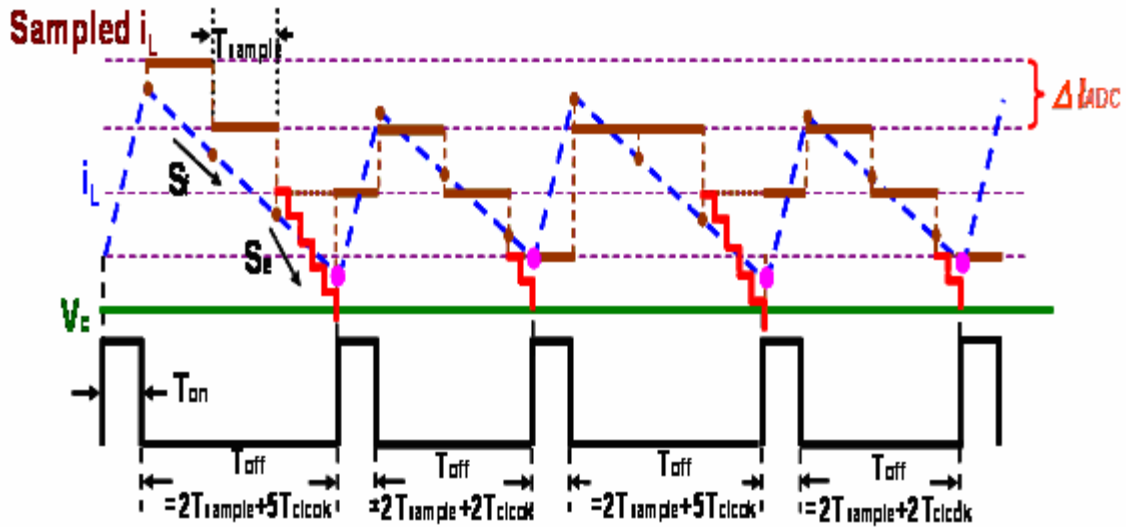


Fig. 2.6 ADC Output Current Waveforms with Quantizer

From the comparison between figure 2.5 and figure 2.6, it is quite clear that due to the quantization effect in ADC, the ADC output current and the DPWM output is a little bit different than the case without quantization, which gives us a certain amount of quantization error. As we discussed in the previous chapter, the quantization model is basically a nonlinear gain inserted into the loop, as shown in figure 1.19. This methodology will be applied in digital constant on-time current-mode control case too.

Here we will use the simulation method to get the describing function gain. The methodology is shown in figure 2.7.

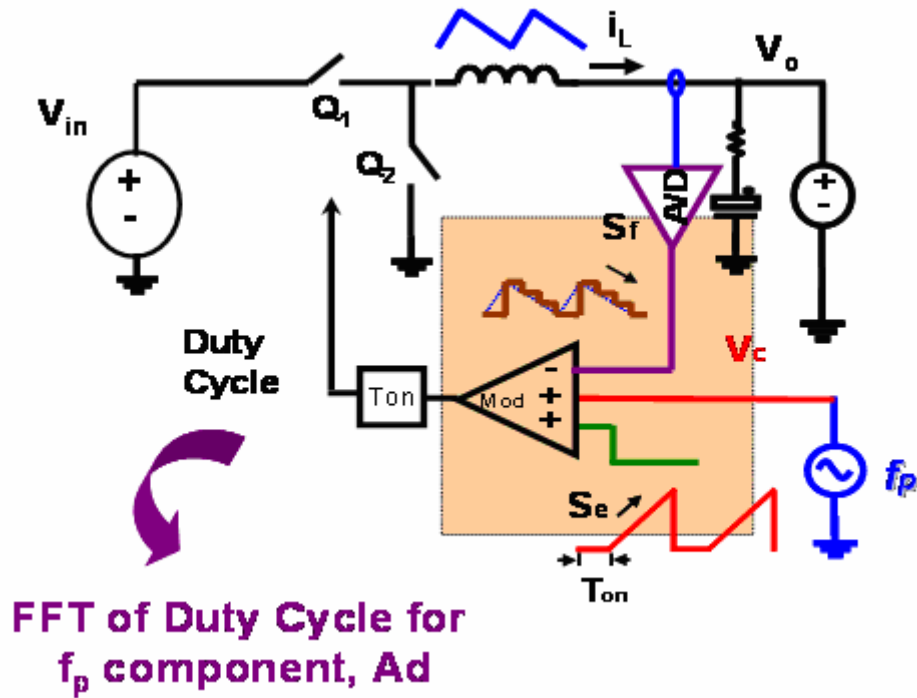


Fig. 2.7 Simulation Setup for Nonlinear Gain of Quantization Effect

The basic concept is to add a perturbation source at control signal v_c , and then apply the FFT on the duty cycle to get the fundamental component's amplitude. Then the nonlinear gain of quantization effect can be gotten from the following equation:

$$\frac{A_d}{A_c} = N(A_c, e_{V_c}) \cdot \left| \frac{1}{S_e \cdot T_s} \cdot (e^{-s \cdot T_{on}} - 1) \frac{e^{s \cdot T_s}}{m - e^{s \cdot T_s}} \right|_{f=f_p} \quad (48)$$

Here the A_d is the duty cycle fundamental component's amplitude and A_c is the perturbation source's amplitude. To obtain the nonlinear gain of quantization effect, this ratio is divided by the gain of previous model at perturbation frequency (f_p).

Figure 2.8 shows the ratio between A_d and A_c from the simulation. Figure 2.9 shows the resultant nonlinear gain $N(A_c, e)$ from the processing:

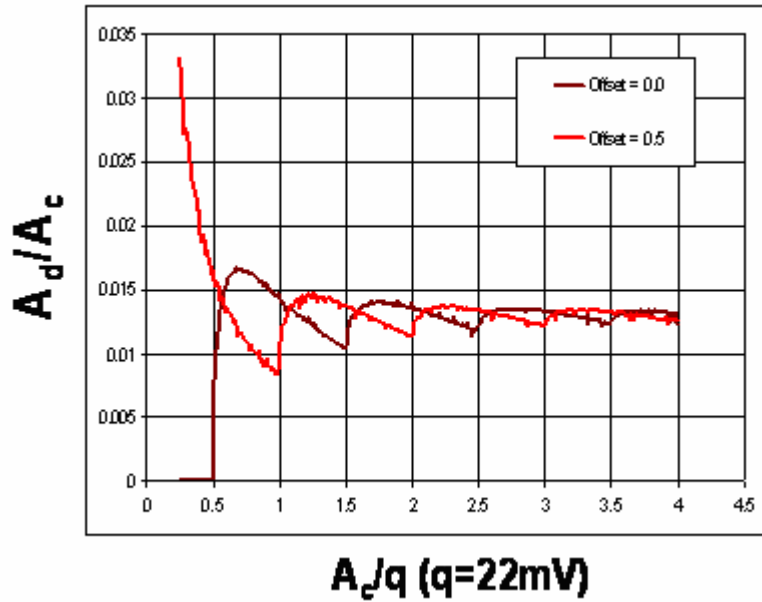


Fig. 2.8 The ratio between A_d and A_c from Simulation

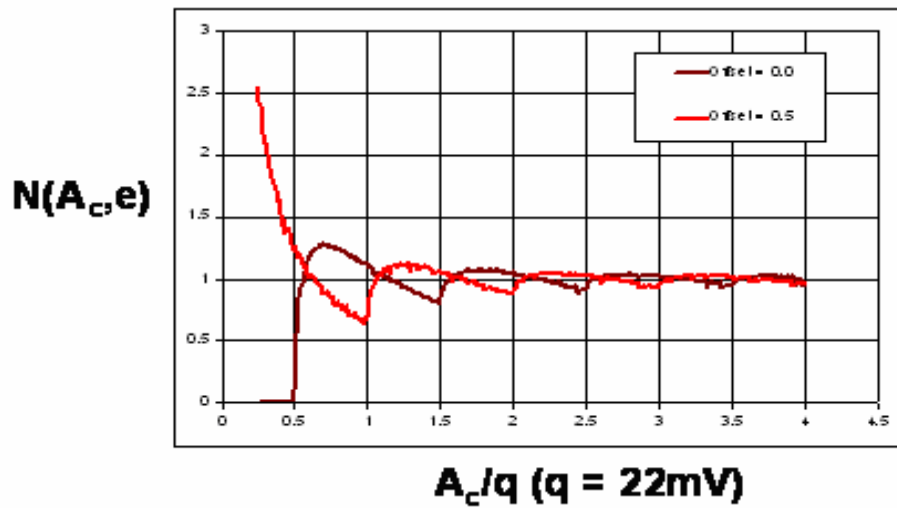


Fig. 2.9 Nonlinear Gain of Quantization Effect

Comparing the nonlinear gain got from simulation and the nonlinear gain previously introduced in chapter 1, we can see that these two are same.

Finally, we can get the whole model for the current-mode cell as:

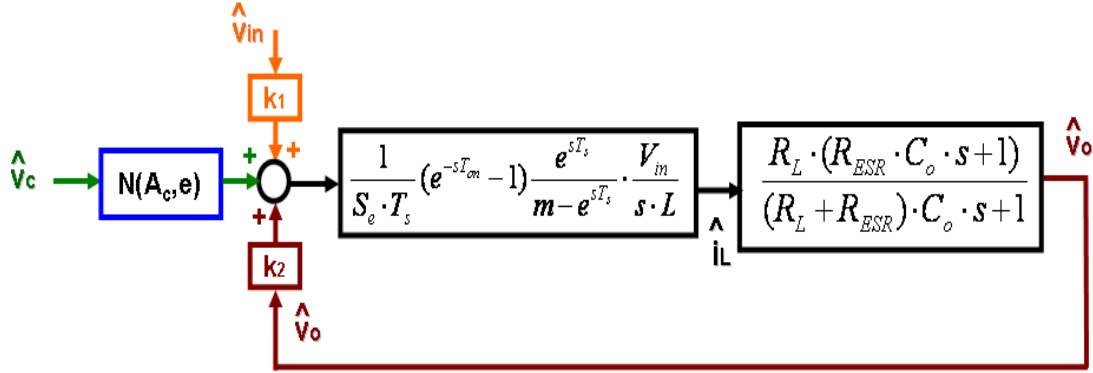


Fig. 2.10 Model Blocks

Here, the nonlinear gain $N(A_c, e)$ is shown in figure 2.9. This is the same as the gain developed in literature [6]. The DF developed for constant on-time modulator with a sample-hold effect taken into consideration is already included in the model from v_c to v_o when ignoring the k_1 and k_2 , repeated here:

$$\frac{i_L(s)}{v_c(s)} = \frac{1}{S_e \cdot T_s} (e^{-sT_{on}} - 1) \frac{e^{sT_s}}{m - e^{sT_s}} \cdot \frac{V_{in}}{L \cdot s} \quad (49)$$

Here, k_1 is the low frequency gain from input voltage perturbation to the inductor current perturbation as shown in equation (46) while k_2 is the low frequency gain from output voltage to the inductor current perturbation. These two gain are used to compensate the assumptions we made during the derivation of describing function model.

2.3. Model Verification by Simulation

2.3.1. Simulation Setup

From figure 2.10, we can see that there are two kinds of describing function models: one is the describing function model for a current-mode constant on-time modulator with sample-hold effect; another one is the describing function model for the quantization effect from the ADC in current-loop. Here the first part of describing function model (DF) is not related to the perturbation source at control signal V_c , while the second part of describing function model $N(A_c, e)$ is the function of the perturbation source. Since the

quantization gain is obtained from simulation, this part is not necessary to be verified in simulation again.

Another point worth mentioning regarding the verification methodology is that in derivation, we assume the fixed input and fixed output voltage, and then get the describing function DF in figure 2.10. So in our verification of control-to-inductor current transfer function, we will fix the input voltage and output voltage. While verifying the control-to-output voltage transfer function, we take the k_2 into consideration and use capacitor branch and resistor load.

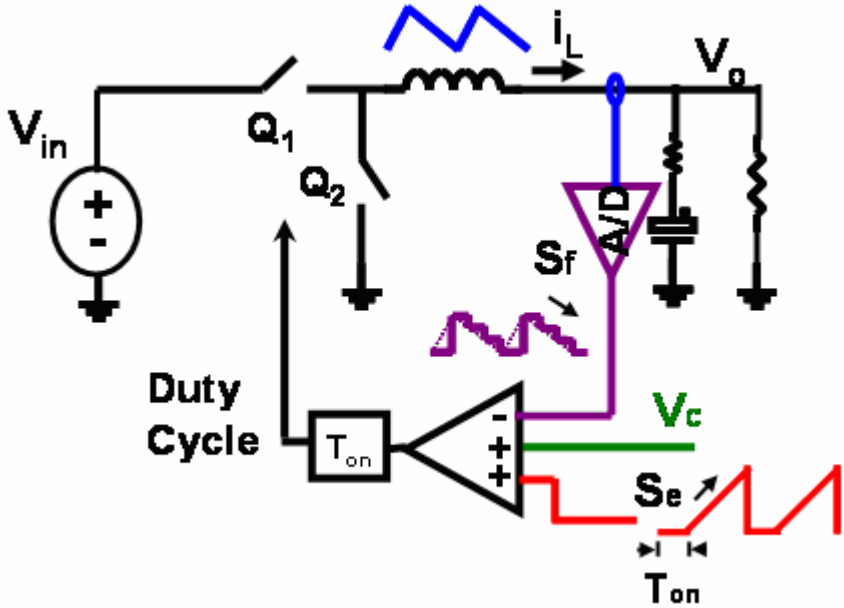
Based on these two considerations, when verifying the digital constant on-time modulator's model DF, we use the SIMPLIS to build a constant on-time modulator circuit with sample-and-hold function block. This simulation setup is equivalent to a digital constant on-time modulator with quantization gain equal to one.

2.3.2. Verification Results

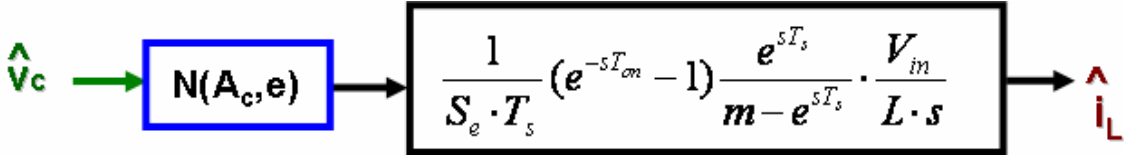
The 1st verification is the verification of the control-to-inductor current transfer function. As we can see from figure 2.9, the quantization gain approaches to one when the control signal v_c 's perturbation amplitude becomes quite large.

As shown in figure 2.11, if we assume the $N(A_c, e)$ to be 1.0, the simulation result, control-to-inductor current, should be mainly composed of the DF' and the V_{in}/L_s transfer function since we fixed the output voltage and input voltage in our simulation setup.

The results are shown in figure 2.12 and figure 2.13.



(a) Current-Cell



(b) Control-to-Inductor current TF

Fig. 2.11 Verifying Control-to-inductor current TF

Here $N(A_c, e)$ is equal to one when V_c 's perturbation amplitude is quite large comparing with current ADC quantization level.

$$\text{Transfer Function: } \frac{\tilde{i}_L}{\tilde{V}_c}$$

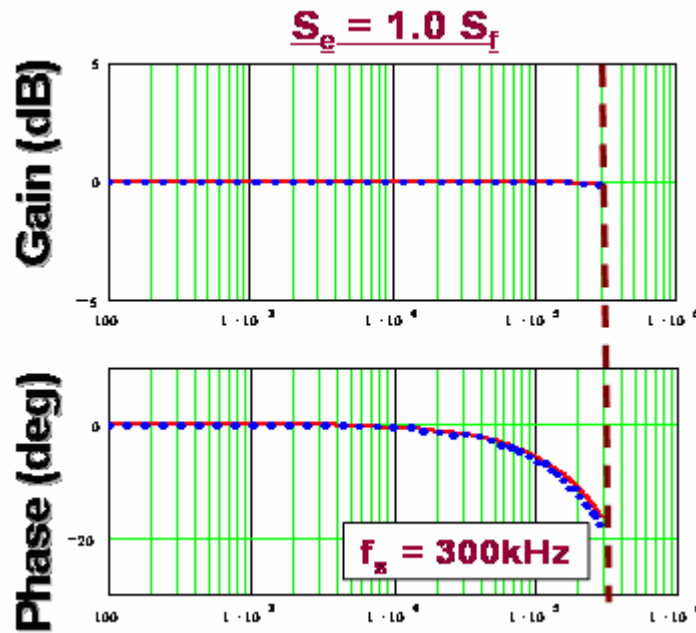


Fig. 2.12 Verification for Control-to-inductor current TF: $S_e = 1.0 S_f$

Red: Model, Blue: Simulation

Figure 2.12 shows the external ramp's slope equal to the inductor current down slope case. As we can see, the simulation matches with the model quite well. Figure 2.13 shows another case: external ramp's slope equals 4 times the inductor current down slope. It is obvious that in that case, the model is still matched with the model quite well.

When the slope of the external ramp becomes larger, both the gain and phase have more and more characteristics of two poles. This is quite reasonable because when the external ramp slope becomes larger and larger, the effect of inductor current ramp becomes diminishes. This causes the control structure to approach the voltage-mode control structure, which has the double-pole characteristics.

Transfer Function: $\frac{\tilde{i}_L}{\tilde{V}_c}$

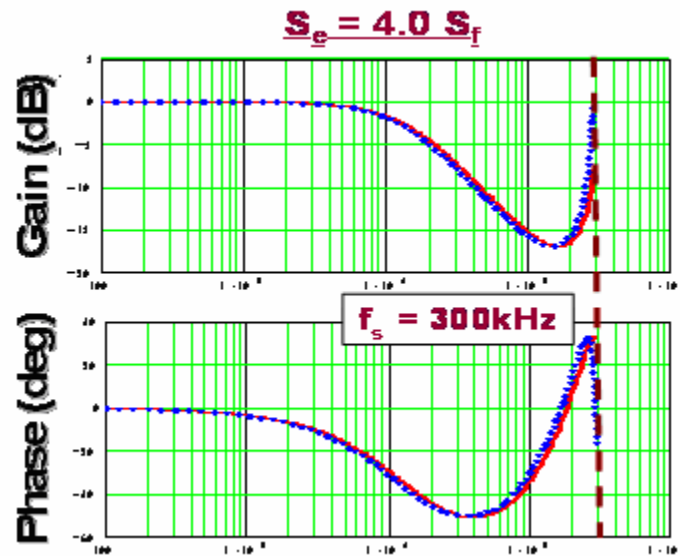


Fig. 2.13 Verification for Control-to-inductor current TF: $S_e = 4.0 S_f$

Red: Model, Blue: Simulation

The control-to-output voltage is also verified in simulation w/o considering the quantization effect. The control-to-output model blocks shown in figure 2.14 and the results are shown in figure 2.15, 2.16 and 2.17. The nonlinear gain is assumed to be 1.0.

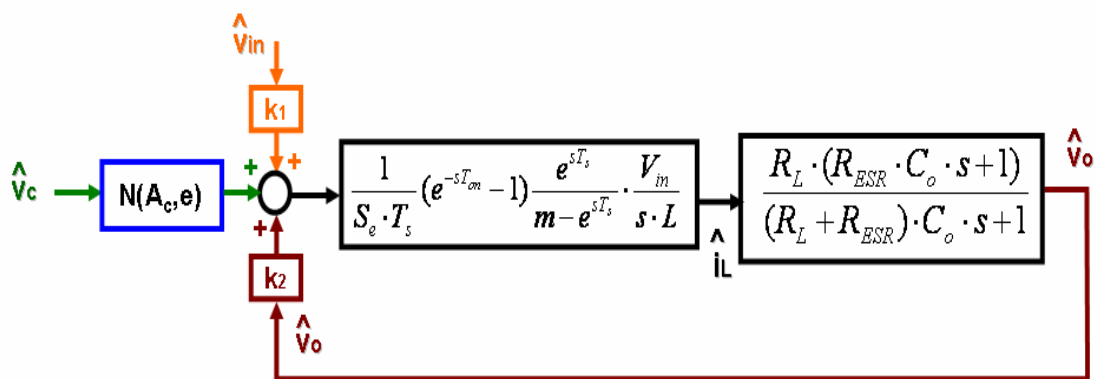


Fig. 2.14 Control-to-output Model Blocks

$$\text{Transfer Function: } \frac{\tilde{V}_o}{\tilde{V}_c}$$

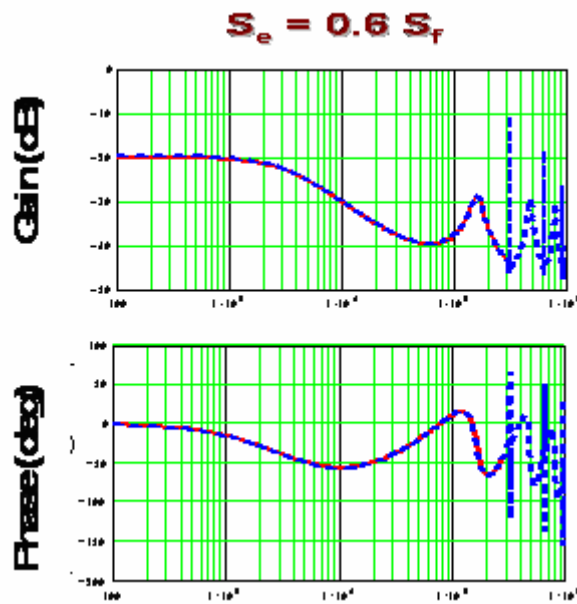


Fig. 2.15 Verification for Control-to-Output Voltage: Red, model; Blue: simulation

$$\text{Transfer Function: } \frac{\tilde{V}_o}{\tilde{V}_c}$$

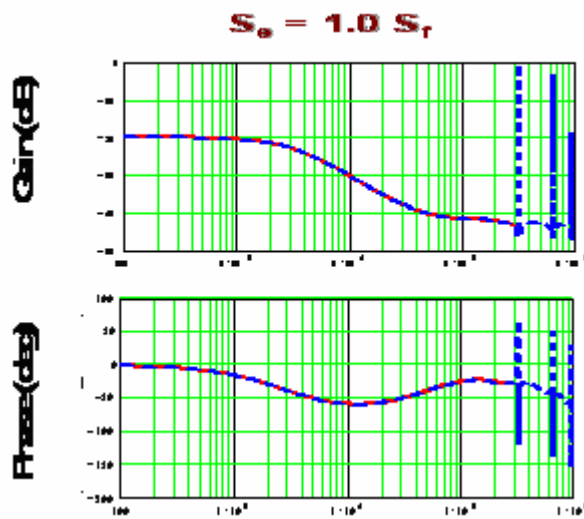


Fig. 2.16 Verification for Control-to-Output Voltage: Red, model; Blue: simulation

$$\text{Transfer Function: } \frac{\tilde{V}_o}{\tilde{V}_c}$$

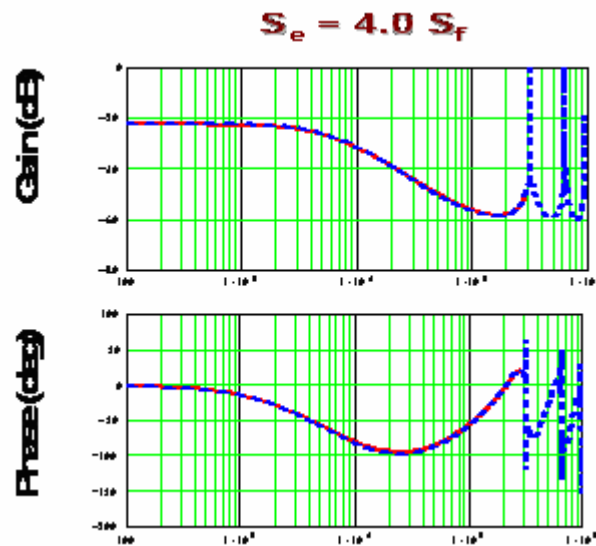


Fig. 2.17 Verification for Control-to-Output Voltage: Red, model; Blue: simulation

Based on the above simulation verification, it is obvious that the model developed in this section is valid and should be useful for design.

All the simulation parameters can be found in the table 3.1 and 3.2.

Chapter 3 Design of Digital Constant On-time Current-Mode Control

In the previous chapters, the digital constant frequency voltage-mode control case is reviewed. The loop model is developed and the design guideline is investigated. Then in chapter 2, the proposed new control structure, digital constant on-time current-mode control, is introduced. Its describing function model is also developed in chapter 2. Designing this structure, however, is still unknown to us. In this chapter, the section 3.1 will discuss the limit cycle oscillation problem in this control structure. Then in section 3.2, a steady-state condition is proposed, which basically gives us a relationship between the current ADC and voltage ADC resolution. With the help of this steady-state condition, the benefits of limiting the current loop oscillation amplitude in one sampling step can be achieved. However this condition is valid under the assumption that the sampling frequency of the current ADC is infinite. When we take the finite sampling into consideration, a quite high sampling frequency is necessary to meet this condition, which will put a big burden on the current loop ADC's cost. Literature [33] proposes an external ramp concept for digital constant on-time current-mode control. By introducing the external ramp into this control structure, we will see two benefits: first, the current ADC's resolution requirement is alleviated; second, the sampling frequency of current loop ADC is greatly reduced. Hence the cost of current loop ADC is decreased significantly.

The circuit diagram of the digital constant on-time current-mode control is shown in figure 3.1. Here, we study the limit cycle oscillation problem from the basic control structure, which is a digital constant on-time current-mode control without an external ramp.

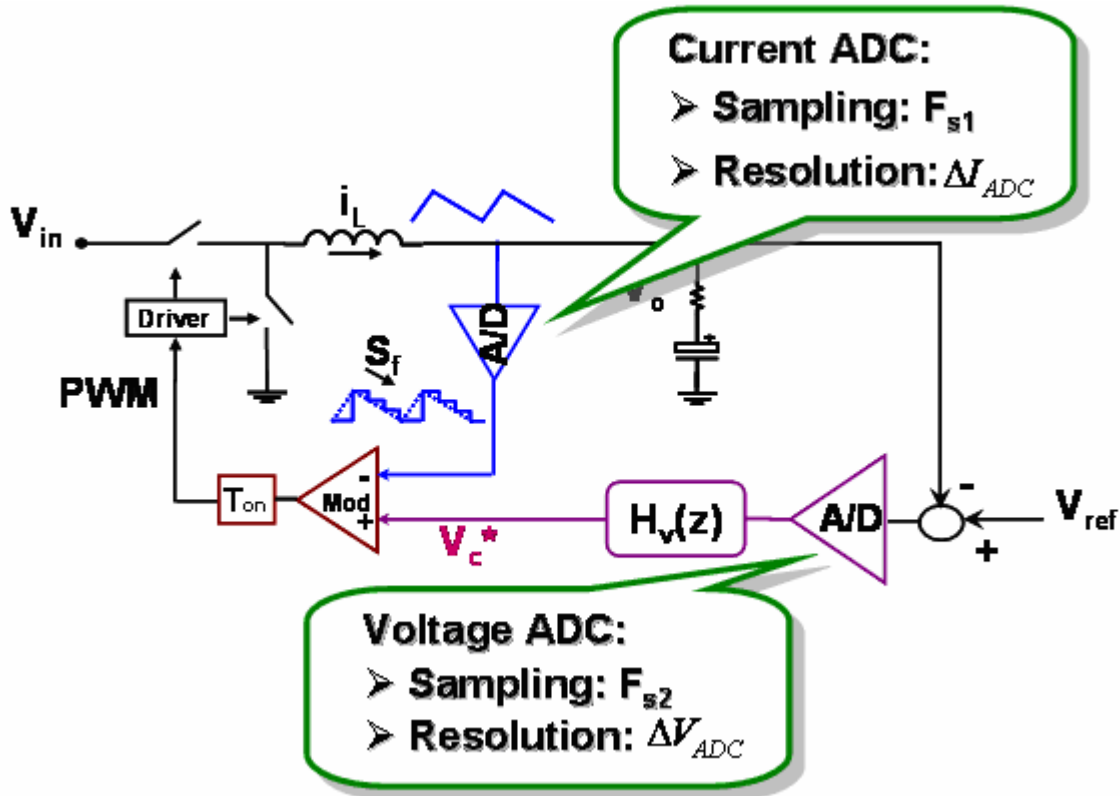


Fig. 3.1 Digital Constant On-time Current-Mode Control

As we show in figure 3.1, there are two ADCs. One is used to digitalize the inductor current and produce a stair case current ramp for the constant on-time modulator. Another one is used to digitalize the feedback output voltage signal (basically the error voltage). In this control structure, from control design point of view, there are three blocks we should design. These two ADCs have their parameters for design: sampling frequency and resolution step. The compensator is another block for design.

It should be pointed out that in this design, the voltage ADC's sampling frequency is assumed to be one sample per switching cycle. In this case, the switching ripple won't be injected into control loop.

In this design stage, the limit cycle oscillation issue is the purpose for the system design, so before we present the design guideline, the limit cycle oscillation issue in the control structure shown in figure 3.1 is investigated in section 3.1.

while the quantization effect is, at first, ignored. The comparison shows that due to the digitalization of current loop, the limit cycle oscillation is introduced into system. How to analyze the oscillation problem in the current loop when we consider both sample-and-hold effect and quantization effect?

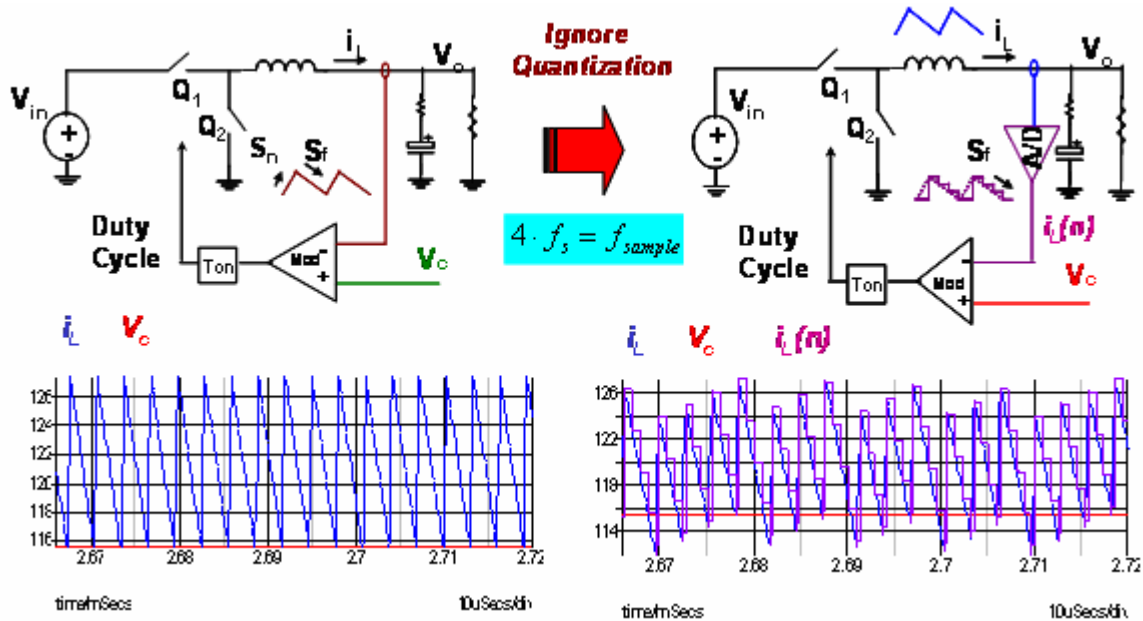


Fig. 3.3 Current Is Oscillating When Introduce the Sample-Hold Effect Into Current Loop

3.1.1. Current Loop Oscillation Analysis w/ Infinite Resolution

In this section, the digital constant on-time current loop w/ the assumption of infinite resolution of current ADC will be analyzed for its oscillation issue, which is equivalent to ignore the quantization effect at first.

With the introduction of the sample-and-hold effect into the constant on-time current loop, the delay associated with the sample-and-hold effect is also taking its effect. When comparing with the analog constant on-time control, it is natural for us to imagine that the turn-on edge of next cycle's on-time pulse will be delayed a little, as shown in figure 3.4.

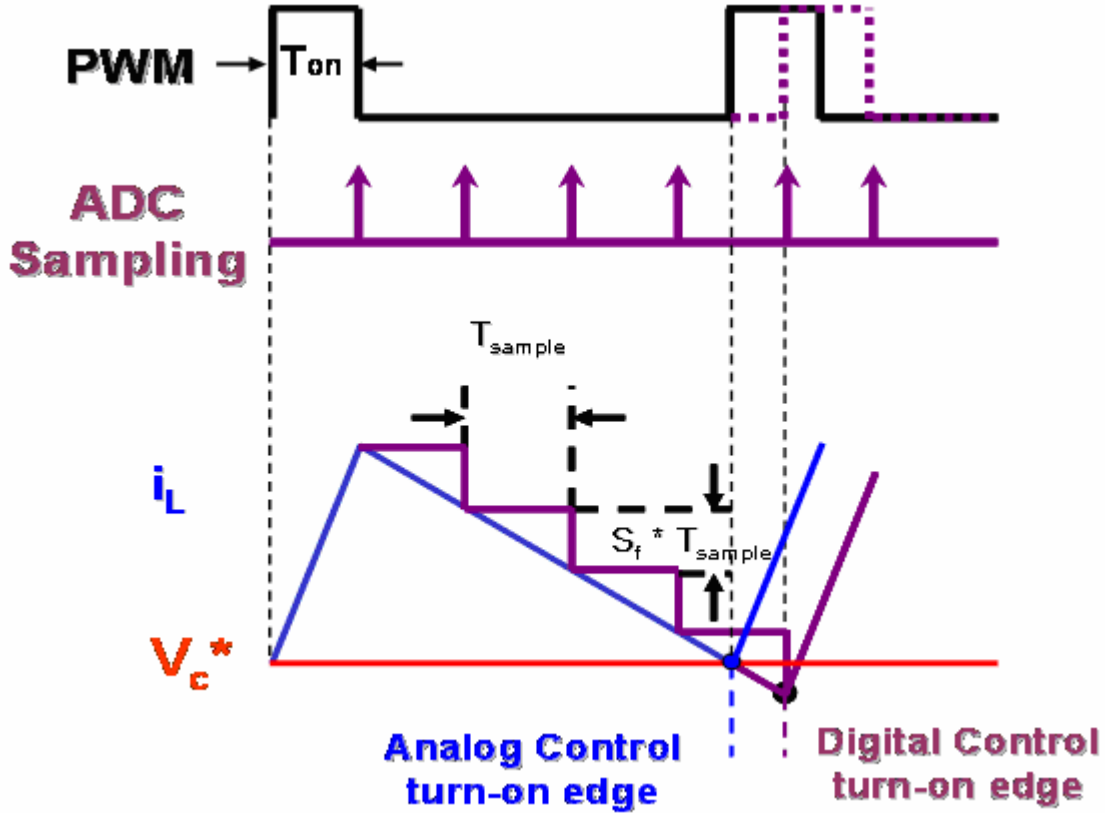


Fig. 3.4 Sample-hold Effect Delay the Turn-on Edge of Next Cycle On-time Pulse

With this kind of sample-hold effect, the current loop is no long stable. This unstable phenomenon can also be viewed from the model developed in chapter 2. In control-to-output transfer function, we see that with the small slope's external ramp, there is a bump on the G_{vc} transfer function. Figure 3.5 shows the limit cycle oscillation in current-loop with only the sample-hold effect being considered. As we can see, since the sample frequency cannot be guaranteed to be the multiple integer times of the frequency corresponding to off-time:

$$F_{sample} \neq N \cdot F_{off} \quad (F_{off} = \frac{1}{T_{off}}) \quad (50)$$

The turn on-edge of the next cycle is different from the previous cycle's turn on-edge, which leads to the oscillation in current loop. This oscillation is inevitable because the sample-hold effect cannot be removed in current loop ADC.

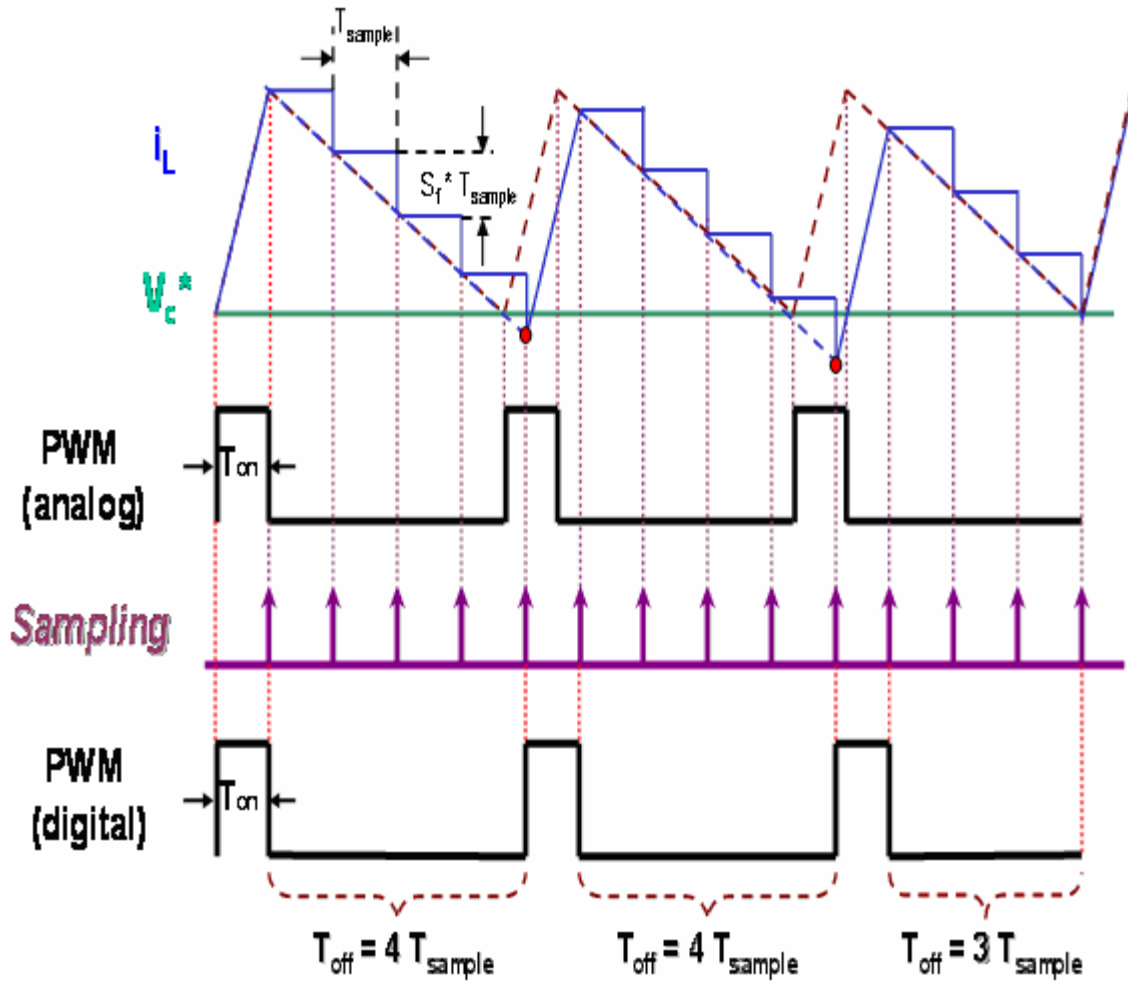
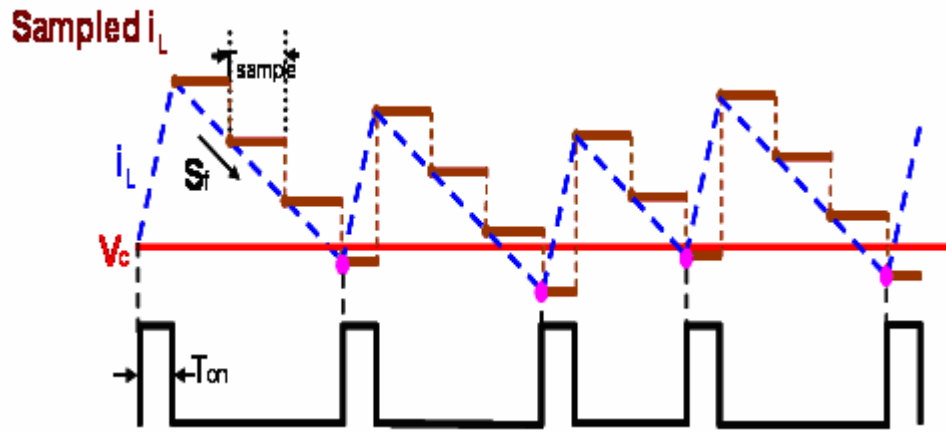
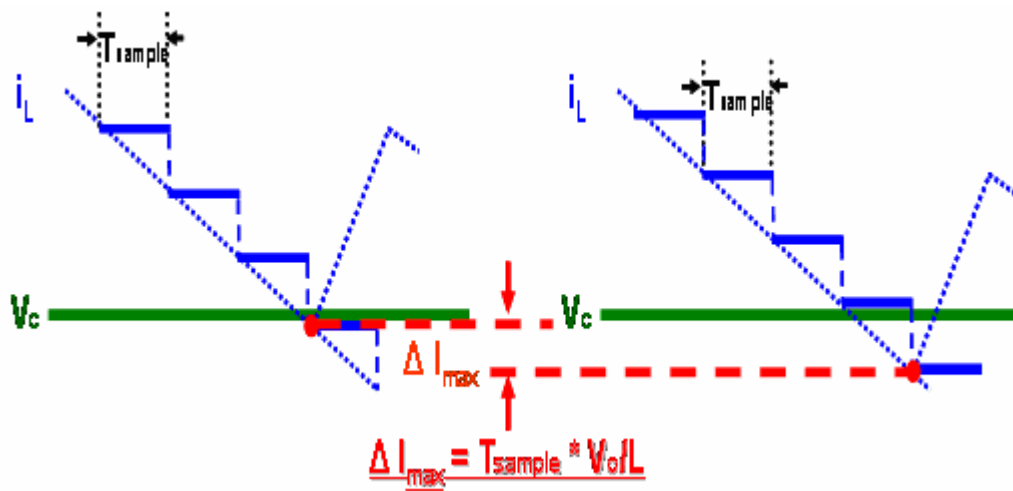


Fig. 3.5 Inductor Current Oscillation: only sample-and-hold effect; v_c is fixed;

However this kind of current oscillation has a quite interesting characteristic: if we ignore the quantization effect from current loop ADC, the oscillation amplitude, although cannot be avoided, is limited to one sampling step. Figure 3.6 shows this limiting characteristic and the maximum amplitude of current oscillation.



(a) Current Oscillation Conceptual Drawing



(b) Oscillation Maximum Amplitude

Fig. 3.6 Current Loop Oscillation Amplitude is Limited

As shown in figure 3.6, the extreme cases are like these: the highest inductor current sampling point is the point almost touching v_c as shown in left side of figure 3.6 (b). The reason is that if the sampling point is a little bit larger than V_c , then it has to wait until next sampling point to turn on the next cycle, which is the right side of figure 3.6 (b). So the maximum oscillation amplitude is:

$$\Delta I_{\max} = T_{\text{sample}} \cdot S_f = T_{\text{sample}} \cdot \frac{V_o}{L} \quad (51)$$

From this equation, we can see that, the limit cycle oscillation in current loop is well limited and there are two ways to decrease this oscillation amplitude: one is to increase sampling frequency; the other one is to decrease the V_o/L value. So in this case, the limit cycle oscillation is well controlled by the system parameters, a great benefit of this structure.

3.1.2. Current Loop Oscillation Analysis w/ Finite Resolution

But to achieve the above characteristic, the limiting benefit, there is an assumption: ignoring the quantization effect in the current ADC. However, the quantization effect exists in both the current ADC and the voltage ADC. The issue will then come out when we consider the quantization effect in the oscillation analysis.

Since the current ADC and voltage ADC both have the quantization effect, to simplify the analysis, we will study its effect step by step. First we consider the quantization effect from the current ADC and assume that the compensator's output is continuous. Figure 3.7 and figure 3.8 show the oscillation problem considering both the sample-hold effect and quantization effect from the current ADC.

First, let's take a look at figure 3.7. The quantized current should be equal or smaller than the v_c , at which time, the next cycle can be turned on. When steady-state average value of v_c is in the middle of two adjacent quantization levels and there is a small perturbation on v_c , the sampled current (the points) should be a little bit less than the steady-state average value of v_c , the pinked dashed line. Next the quantized current is converted to the $k-1$ level, which is smaller than the actual v_c , the red solid curve. So this is the highest possible sampling point for the inductor current, and also the highest turn-on edge for the inductor current.

In another case, when the sampled inductor current value is a little bit higher than steady-state average value of v_c , the pink dashed line, the quantized current becomes k level,

which is always larger than the actual v_c . When this happens, the switch cannot be turned on and the current will further decrease, till the next sampling point of inductor current, which is quantized to $k-1$ level.

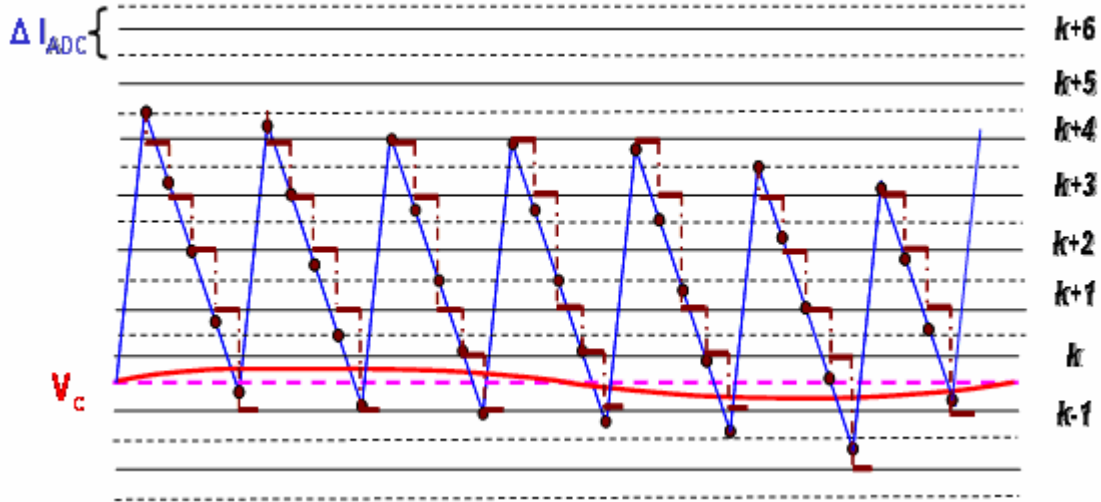


Fig. 3.7 Current Oscillation Considering Both Sample-hold Effect and Quantization Effect:

(Steady-state average value of v_c at middle of Quantization level)

From the above analysis, we can see that the sampled inductor current is needed to compare with the steady-state average value of v_c , the pink dashed line in figure 3.7, instead of the actual v_c , to determine the turn-on edge of next cycle. So this mechanism is same as the case without the quantization effect. Hence, it is quite natural for us to derive the oscillation amplitude in this case:

$$\Delta I_{\max} = T_{\text{sample}} \cdot S_f = T_{\text{sample}} \cdot \frac{V_o}{L} \quad (52)$$

In conclusion, when steady-state average value of v_c is in the middle of two adjacent quantization levels and there is a small perturbation on v_c , this perturbation will not influence the oscillation amplitude, which is equivalent to giving us a zero gain for the small perturbation of v_c .

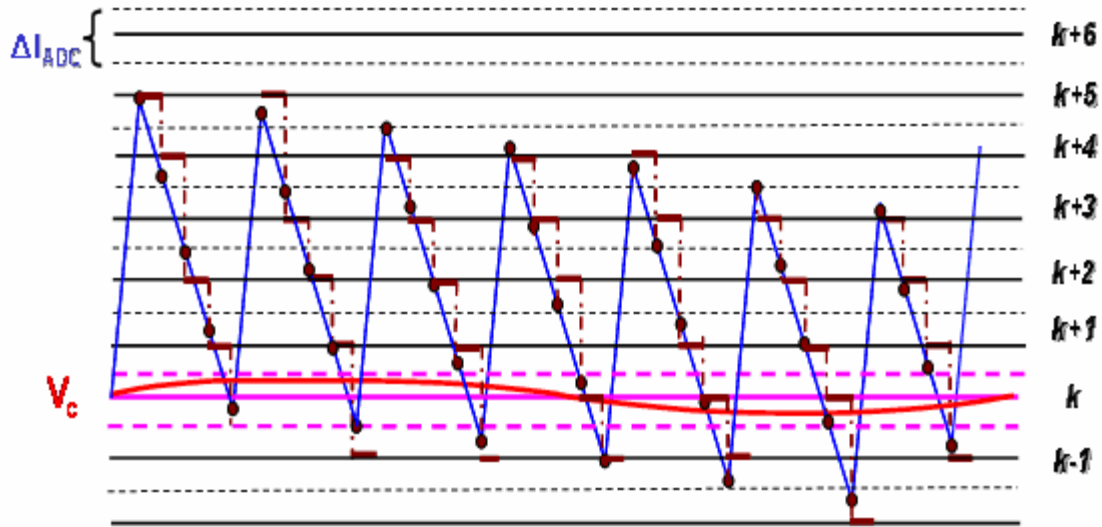


Fig. 3.8 Current Oscillation Considering Both Sample-and-hold Effect and Quantization Effect:

(Steady-state average value of v_c at boundary of Quantization level)

In another case, the steady-state average value of v_c is at a boundary of quantization levels and there is a small perturbation on v_c , referring to figure 3.8. In the positive cycle of the v_c perturbation, if a sampled inductor current is a little bit less than the top pink dashed line, then the sampled inductor current will be quantized to the k level, which is smaller than v_c . The switch is then turned on. However, if the sampled inductor current is a little bit higher than the top pink dashed line, then the turn-on edge has to wait until the next sampling point. So the highest sampling point and also the highest turn-on edge is the point that is a little bit less than the top pink dashed line. This point determines the highest possible value of the inductor current bottom value.

While in the negative half cycle of the v_c perturbation, if the sampled inductor current is a little bit higher than the bottom pink dashed line, the quantized current is still at k level. Unfortunately, in negative half cycle, the k level is always larger than the actual v_c , so the switch cannot be turned on. We have to wait until next sampling point of inductor current to turn on the switch. In this case, we know that the lowest sampling point or the lowest turn-on edge is one sampling cycle lower than the bottom pink dashed line.

Finally, based on the above analysis, we can know that the current oscillation amplitude in this case is:

$$\Delta I_{\max} = T_{\text{sample}} \cdot S_f = T_{\text{sample}} \cdot \frac{V_o}{L} + \Delta I_{\text{ADC}} \quad (53)$$

Here, ΔI_{ADC} is the quantization level of current ADC and also the distance between the top pink dashed line and bottom pink dashed line mentioned in the above analysis and shown in figure 3.8.

Figure 3.9 shows the simulation waveform to prove the above analysis.

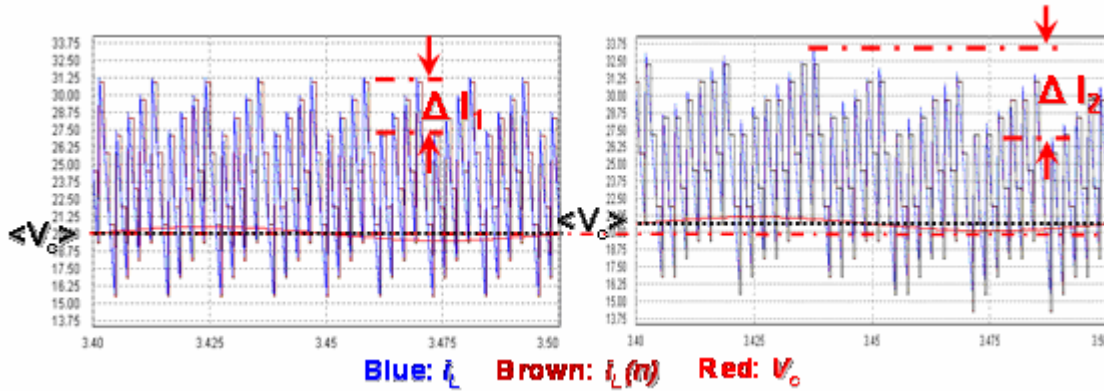


Fig. 3.9 Simulation of Inductor Current Oscillation

Here we have the same v_c perturbation amplitude, the only difference is the average value of v_c . The left one is at the boundary of quantization levels while the right one is at the middle. We can notice from figure 3.9 that the oscillation amplitude of inductor current has a big difference due to the different position of the average value of v_c , which shows the influence of the quantization effect: make the oscillation worse

From the above analysis, we can conclude that in the case of a digital constant on-time current-mode control without an external ramp, the inductor current oscillation is inevitable. If we take the quantization effect from the current ADC into consideration, this oscillation might become worse even though v_c has a very small amount of oscillation.

Then there comes a question: where does the v_c oscillation come from? As we know, if v_c has no oscillation, then the quantization effect in current ADC won't have any trouble.

To answer this question, it should be pointed out that since the current loop has a quantization effect and the voltage feed-back path also has a quantization effect from voltage ADC, these two quantization blocks might cause the limit cycle oscillation in voltage loop, and hence, make the current oscillation worse due to the oscillation from V_c . As we show in figure 3.10, equivalently there are two quantizers: one is the equivalent DPWM; another one is the voltage ADC. When the voltage ADC is in series with the equivalent DPWM, the interaction between these two quantizers might cause the oscillation on v_c .

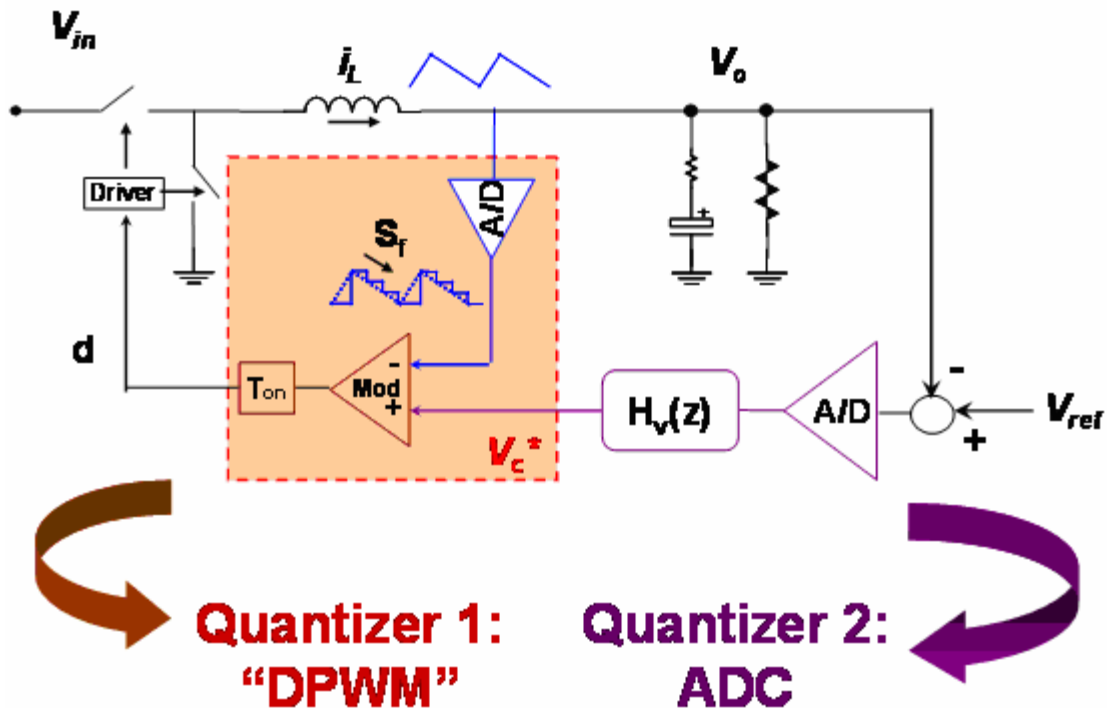


Fig. 3.10 Two Quantizers are in Series

Figure 3.11 shows when these two quantizers are not well designed, the oscillation on the output voltage V_o , the error voltage V_e^* and also the control signal V_c^* .

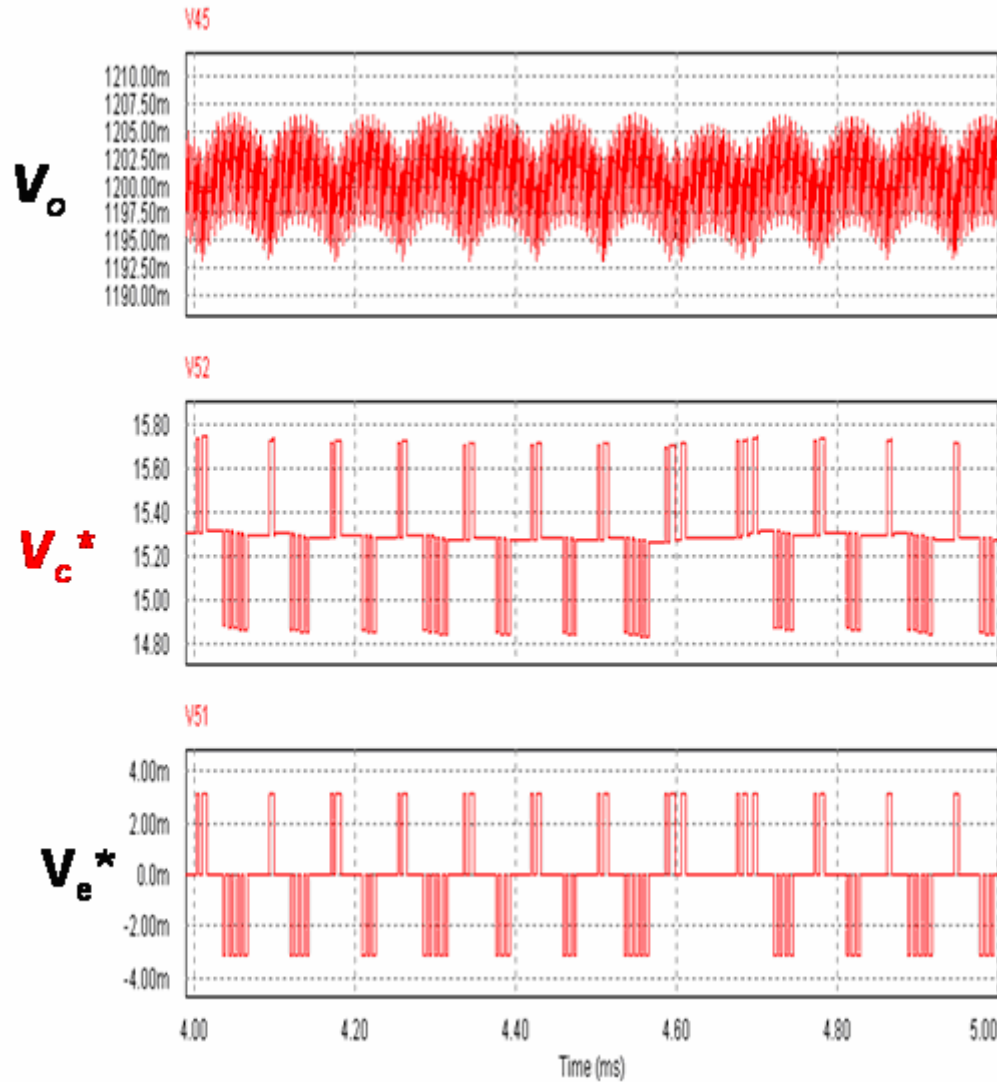


Fig. 3.11 Voltage Loop Oscillation

So in order to limit the current oscillation amplitude into one sampling step, how to design the current ADC and voltage ADC resolutions becomes a quite important issue. The next section will talk about this issue.

3.2. Minimizing the Limit Cycle Oscillation

In the previous section, we investigated the oscillation issue on the digital constant on-time current-mode control.

The quantization effect in the current loop ADC introduces a quantized current in current loop and this quantized current source will further produce a quantized output voltage in steady-state. Since there is a voltage ADC in the feed back path, these two quantization effects might cause the limit cycle oscillation in voltage loop, as in the case of the voltage mode control. In the digital constant on-time current-mode control, the oscillation on v_c will make the current oscillation worse and the limiting function cannot be achieved.

In designing the resolution of these two quantizers, it is quite important for us to possibly limit the current oscillation into one sampling step, and hence, possibly minimize the current oscillation.

To investigate this issue, the external ramp is first removed and the structure shown in figure 3.12 is studied.

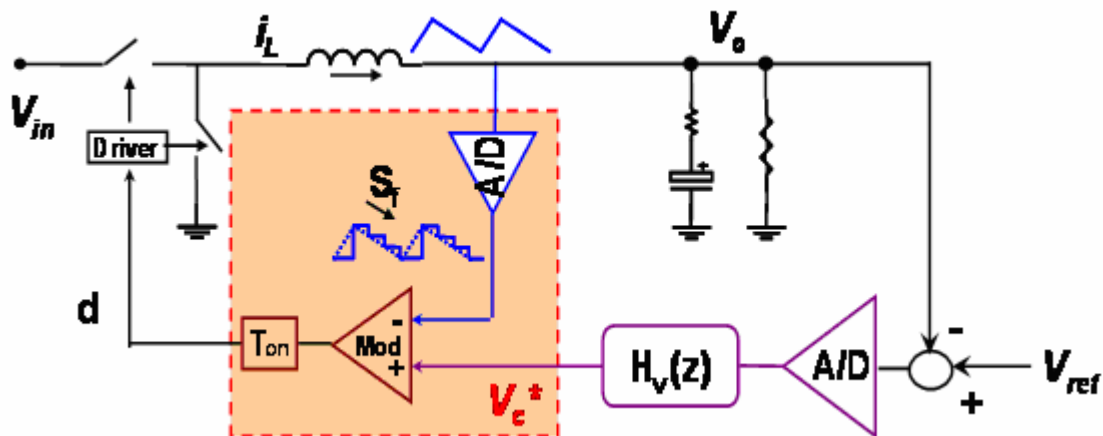


Fig. 3.12 Closed Loop Digital Constant On-time Current Mode Control w/o External Ramp

Previously in the voltage-mode control, we calculated this quantized output voltage as it is shown in figure 3.13.

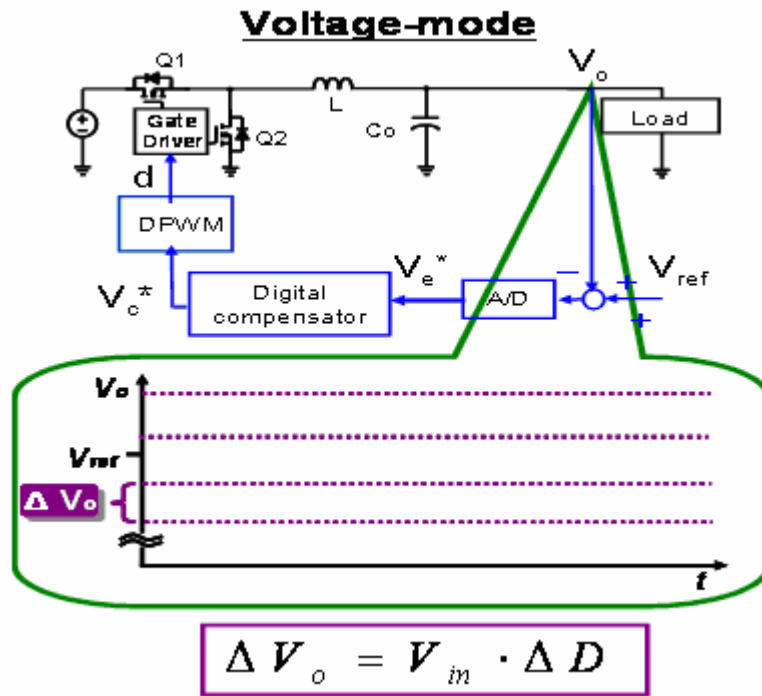


Fig. 3.13 Steady-state Output Voltage Resolution in Voltage-Mode Control Case

If this ΔV_o is smaller than the resolution of voltage ADC, the necessary condition of a no-limit-cycle is satisfied. Following this design concept, in digital constant on-time current-mode control, we will also have a ΔV_o at the output node. But the real issue is how much is this ΔV_o and how should we calculate it?

Before we calculate this ΔV_o , let's review the analog constant on-time current-mode control.

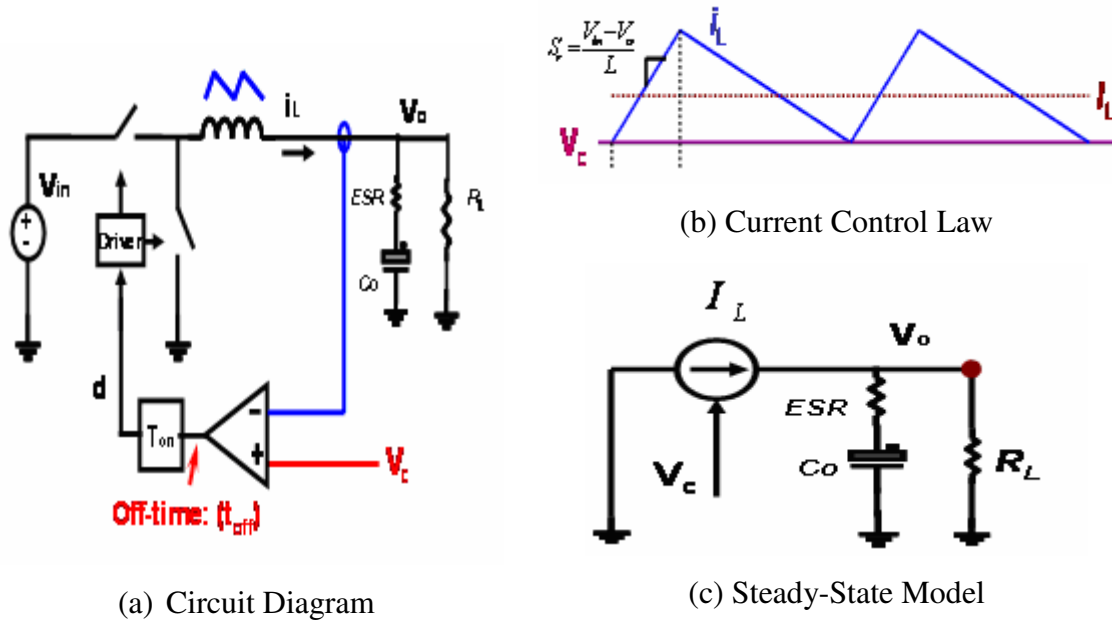


Fig. 3.14 Analog Constant On-time Current-Mode Control

From figure 3.14, we can see that in constant on-time control, the V_c regulates the valley value of inductor current. In steady state, the relation between the valley value and average value of inductor current is fixed; the V_c is also regulating the average value of inductor current. So we can get the steady-state model as shown in figure 3.14 (c).

Based on the above curve, there are two equations we can get.

(1) a relation derived from constant on-time control law in steady-state:

$$I_L = \frac{V_{in} - V_o}{L} \frac{T_{on}}{2} + V_c \quad (54)$$

(2) load characteristic:

$$I_o = \frac{V_o}{R_L} \quad (55)$$

In steady-state, the average value of inductor current should be equal to load current, the following equation should be valid in steady-state:

$$I_L = \frac{V_o}{R_L} = \frac{V_{in} - V_o}{L} \frac{T_{on}}{2} + V_c \quad (56)$$

This steady-state model can also be obtained from the modeling work about analog constant on-time current-mode control [33].

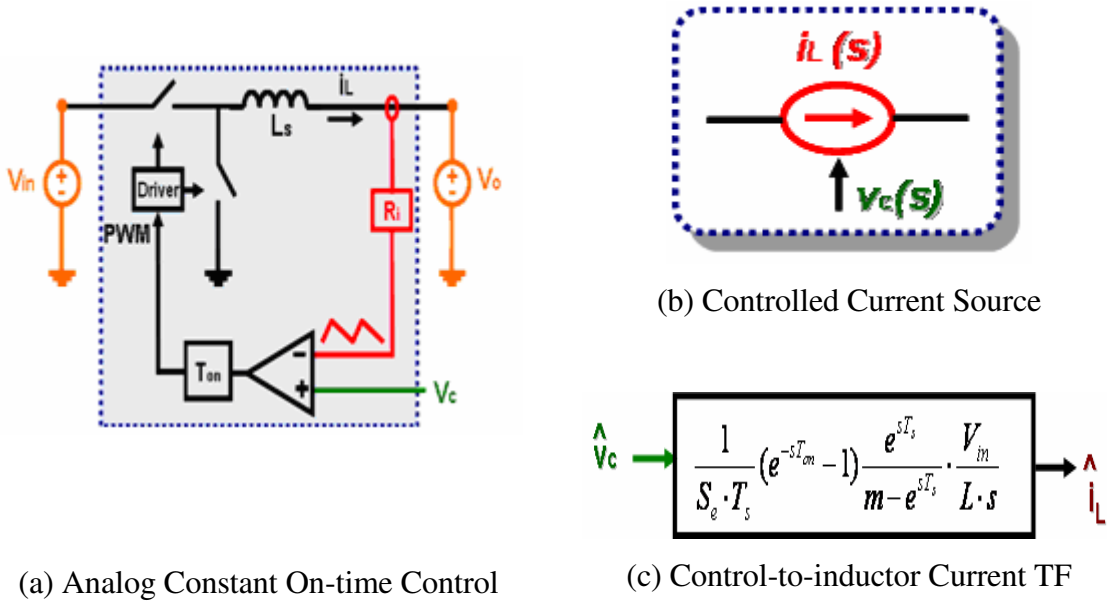


Fig. 3.15 Modeling of Analog Constant On-time Control

From this model, the control-to-inductor current transfer function is:

$$\frac{i_L(s)}{v_c(s)} = DF = \frac{f_s}{s_f} (1 - e^{-sT_{on}}) \cdot \frac{V_{in}}{L_s s} \quad (57)$$

In this model, we can calculate its limit to get the steady-state model ($s=0$):

$$\frac{I_{Lmin}}{V_c} = \lim_{s \rightarrow 0} \frac{i_L(s)}{v_c(s)} = \lim_{s \rightarrow 0} \frac{f_s}{s_f} (1 - e^{-sT_{on}}) \cdot \frac{V_{in}}{L_s s} = 1 \quad (58)$$

Since in constant on-time current-mode control, the control signal V_c is regulating the bottom value of the inductor current, the above I_{Lmin} denotes the bottom value. To get the average value of the inductor current, there is another relation between bottom value and average value needed:

$$I_L = I_{L\min} + \frac{1}{2} \cdot S_n \cdot T_{on} = I_{L\min} + \frac{1}{2} \cdot \frac{V_{in} - V_o}{L} \cdot T_{on} = V_c + \frac{1}{2} \cdot \frac{V_{in} - V_o}{L} \cdot T_{on} \quad (59)$$

The exact same steady-state model can be obtained for average inductor current, as shown in figure 3.14.

While in digital constant on-time current-mode control, the quantization effect from current ADC will quantize the current loop and give us a quantized current source as shown in figure 3.16.

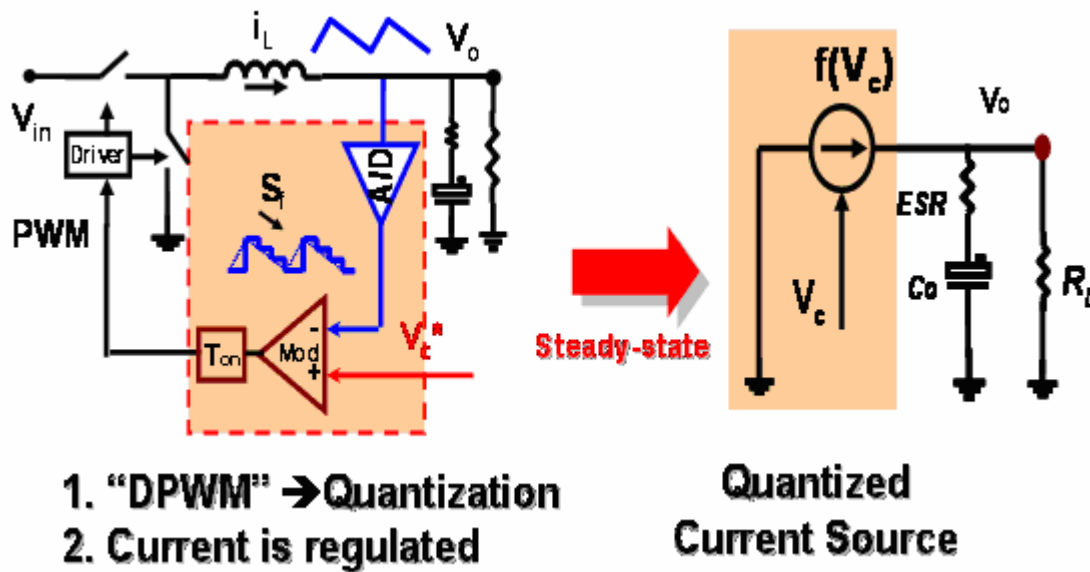


Fig. 3.16 Quantized Current Source

Then if we want to know the ΔV_o , the characteristics of this quantized current source should be clarified. In figure 3.17, a typical current waveform is shown with the assumption of infinite sampling frequency of current ADC.

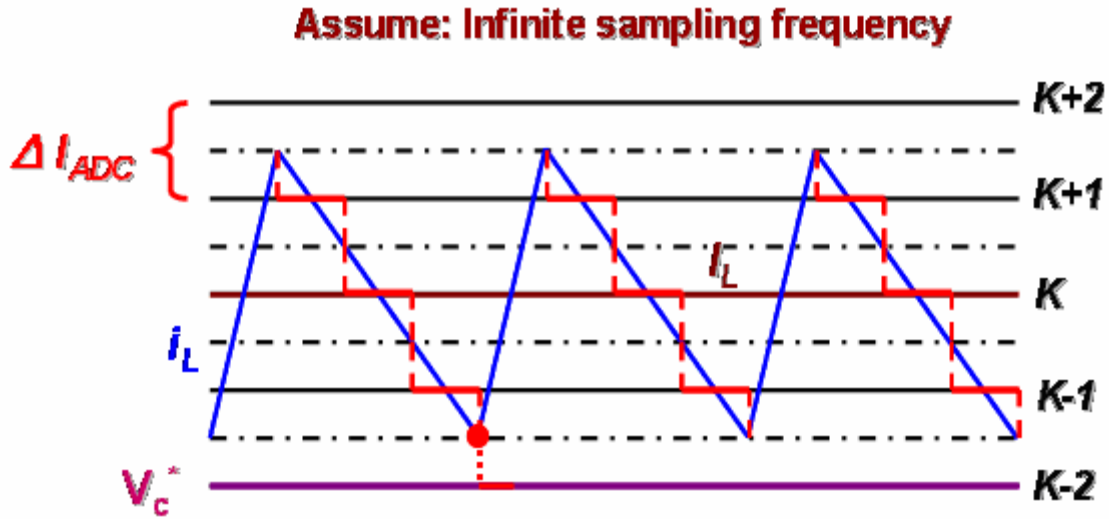


Fig. 3.17 Current Waveform in Digital Constant On-time Control

From figure 3.17, we can see that when the inductor current touches the middle level between $k-1$ and $k-2$, it converts to $k-2$. In this case, V_c^* is at $k-2$, so the converted inductor current is equal to V_c^* , and the switch is turned on at this point.

When V_c^* moves from $k-2$ to $k-1$ and still is less than $k-1$, the inductor current waveform won't change and the shape remains the same. The average inductor current will also stay the same. But if V_c^* is equal to or a little bigger than $k-1$, the inductor current changes. The bottom value moves to the middle level between k and $k-1$. But the average value of the inductor current does not change one step. It will follow the equation (*). So the minimum step of V_c to regulate the inductor current is ΔI_{ADC} , while the minimum step change of the average inductor current is:

$$\Delta I_L = \frac{1}{1 + \frac{R_L \cdot T_{on}}{L \cdot 2}} \cdot \Delta I_{ADC} \quad (60)$$

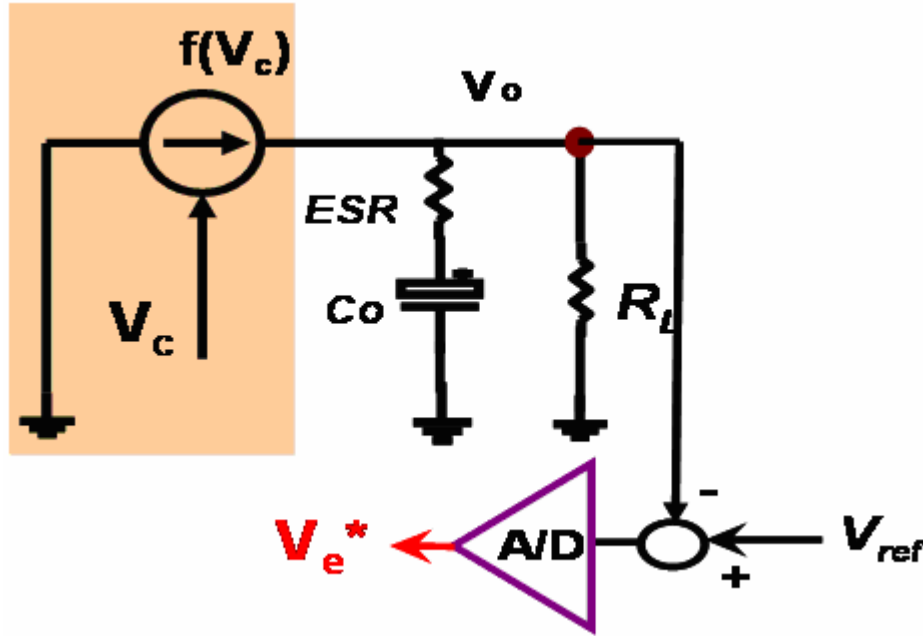


Fig. 3.18 Steady-state Model to Satisfy the Necessary Condition

Since in steady-state the average inductor current goes through the resistor load, the step the change of output voltage can be calculated as:

$$\Delta V_o = \Delta I_L \cdot R_L = \frac{1}{\frac{1}{R_L} + \frac{1}{L} \frac{T_{on}}{2}} \Delta I_{ADC} \quad (61)$$

To satisfy the necessary condition, as shown in figure 3.18, we will have a relation between the current ADC resolution and the voltage ADC resolution, as shown:

$$\Delta V_o = \frac{1}{\frac{1}{R_L} + \frac{1}{L} \frac{T_{on}}{2}} \Delta I_{ADC} < \Delta V_{ADC} \quad (62)$$

To illustrate the concept and also to prove it, a simulation example is provided. The simulation parameters are listed in table 3.1

Table 3.1 System Parameters

I_o (A)	V_o (V)	R_L (Ω)	V_{in} (V)	T_{on} (ns)	L (nH)	ΔV_{ADC} (mV)
20	1.2	0.06	12	333	300	3.125

Based on these parameters, the required current ADC resolution should meet the following condition:

$$\Delta I_{ADC} < \left(\frac{1}{R_L} + \frac{1}{L} \frac{T_{on}}{2} \right) \Delta V_{ADC} = 0.054 A \quad (63)$$

Figure 3.19 and figure 3.20 show two cases with different current ADC resolution designs.

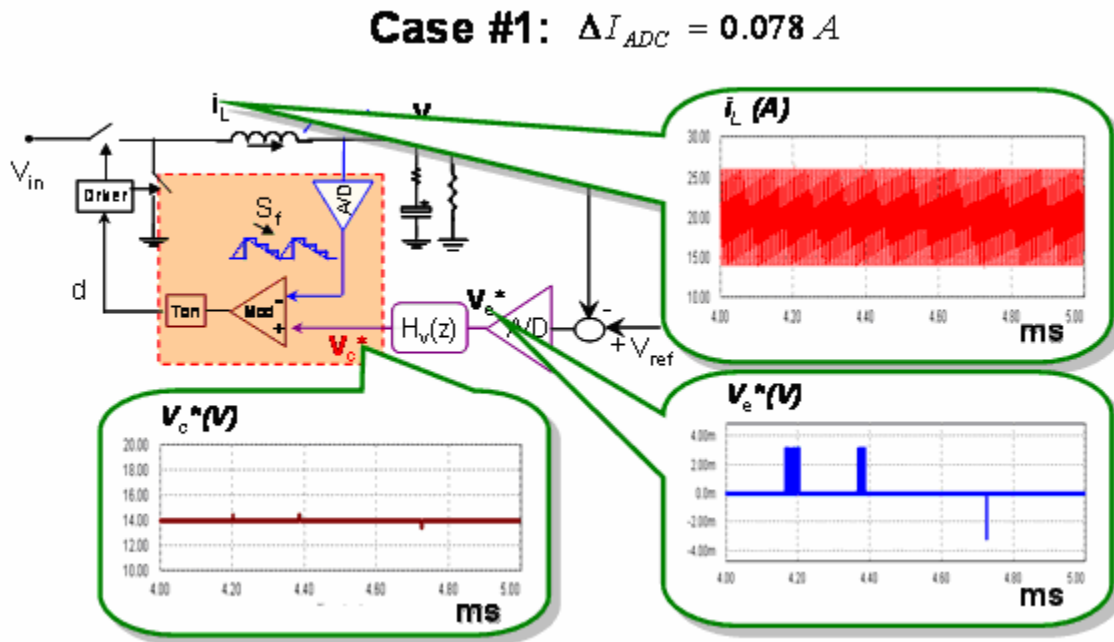


Fig. 3.19 Simulation Case Not Satisfying the Necessary Condition

It is clear that with the assumption of infinite sampling frequency, the design satisfying the necessary condition shows no limit cycle oscillation, while the design not satisfying the necessary condition shows limit cycle oscillation. However, the above simulation is based on the assumption that there is infinite sampling frequency, which is actually not possible in a practical case. If we consider the finite sampling, then the oscillation caused by the sample-and-hold effect of the current ADC will superimpose on this quantized current source. In that case, even if we design the current ADC resolution to satisfy the necessary condition, there are still oscillations.

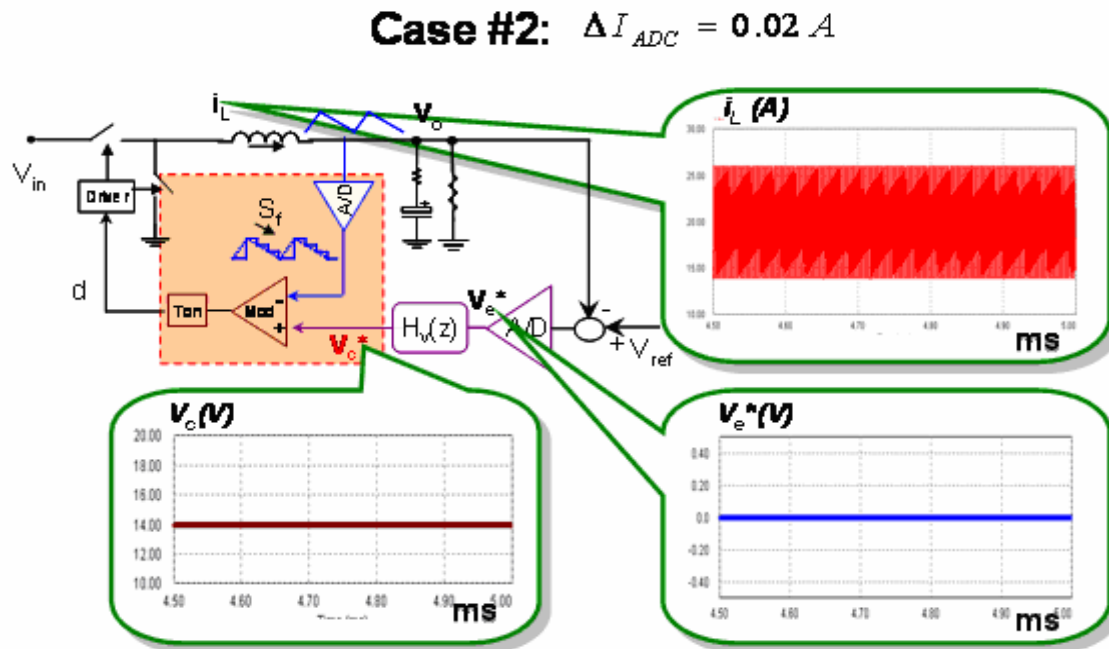


Fig. 3.20 Simulation Case Satisfying the Necessary Condition

Figure 3.21, figure 3.22 and figure 3.23 show the simulation results with the sampling frequency equal to 5 times the switching frequency, 10 times the switching frequency and 15 times the switching frequency.

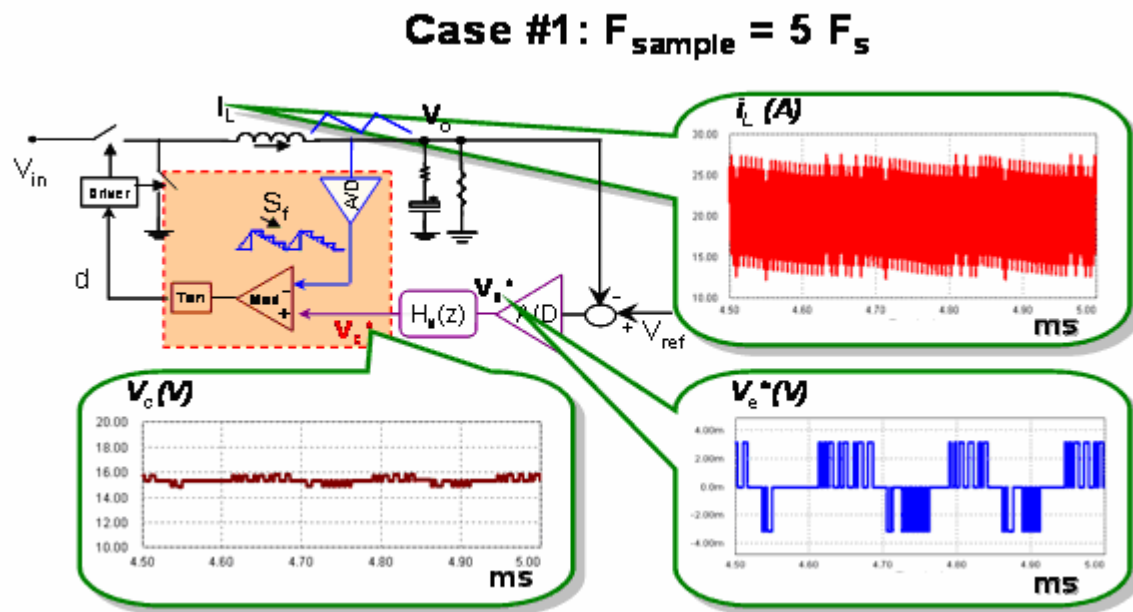
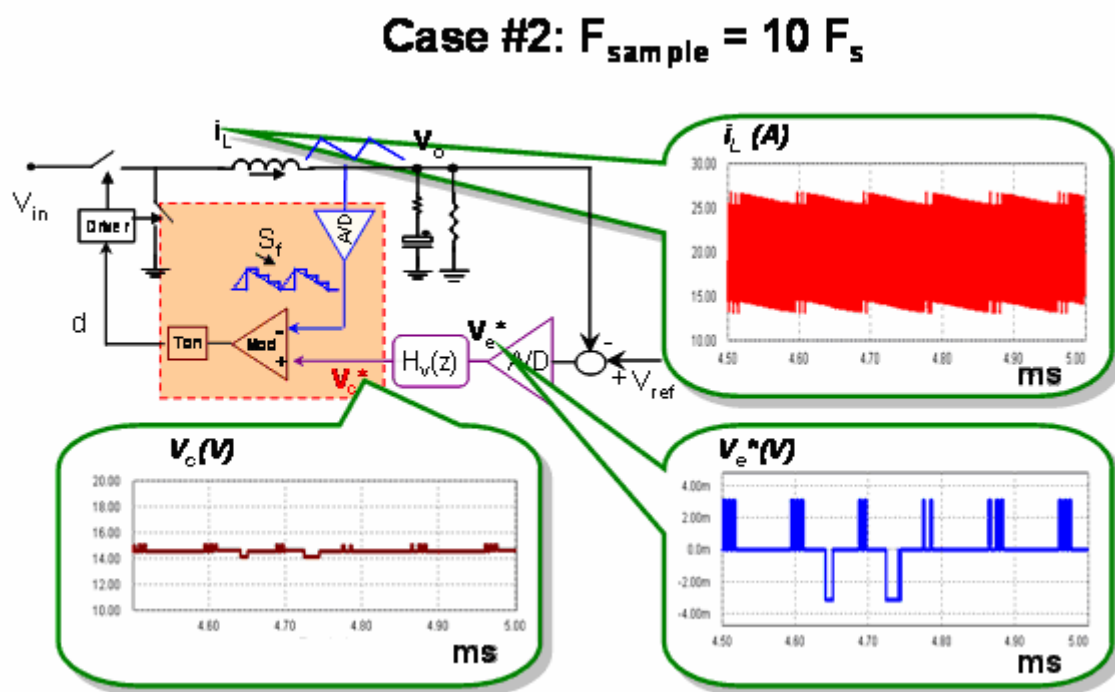
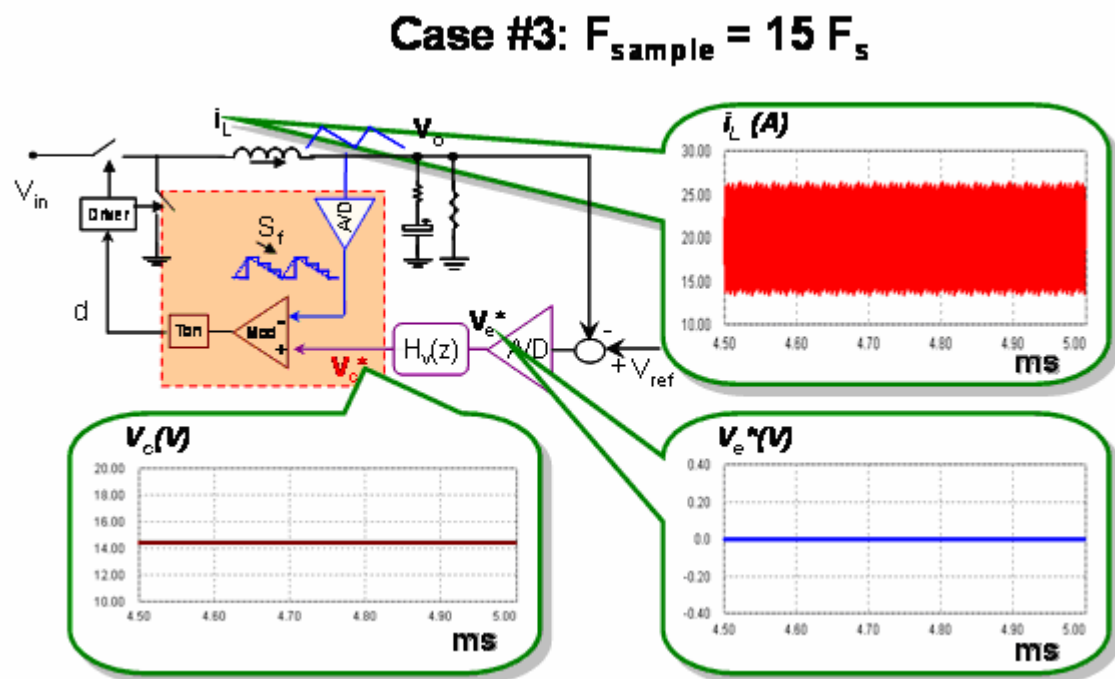


Fig. 3.21 Simulation Case with Finite Sampling Frequency ($F_{sample} = 5 F_s$)

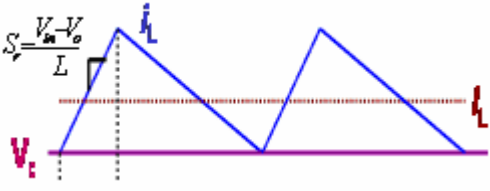
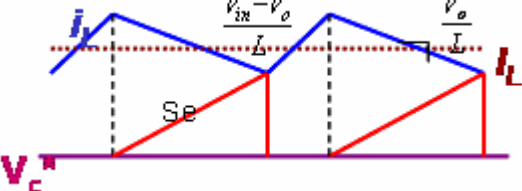
Fig. 3.22 Simulation Case with Finite Sampling Frequency ($F_{\text{sample}} = 10 F_s$)Fig. 3.23 Simulation Case with Finite Sampling Frequency ($F_{\text{sample}} = 15 F_s$)

Comparing figure 3.21~3.23, it is quite clear that when the sampling frequency of current ADC is not high enough (for example, $5 F_s$ or $10 F_s$), the current oscillation is quite big, hence causing the voltage oscillation to be also quite big. This oscillation amplitude will exceed the zero-order bin size of voltage ADC and make the control signal V_c oscillate too, although the current ADC and voltage ADC resolutions meet the necessary condition. But when the sampling frequency of the current ADC is high enough (for example $15 F_s$), the current oscillation is small. In that case, the voltage ADC zero-error-bin can cancel this oscillation and the control signal V_c won't oscillate. So in this case, the only oscillation in the system is caused by the sample-hold effect in current ADC. As we pointed out in the previous section, this oscillation is well limited and the maximum size is one sampling step. Finally we achieve the limiting function of current oscillation. However, the higher sampling frequency puts a big burden on the current ADC, adding to the cost of the system.

In [33], the author proposed the external ramp concept to reduce the sampling frequency. Here we utilize this concept and analyze its benefits.

With external ramp, the above design condition should be changed. The table 3.2 shows a comparison between w/o external ramp and w/ external ramp.

Table 3.2 Comparison Between w/o Ramp and w/ Ramp

	
$I_L = \frac{V_{in} - V_o}{L} \cdot \frac{T_{on}}{2} + V_c$	$I_L = V_c + \frac{V_{in} - V_o}{V_o} \cdot S_e \cdot T_{on} + \frac{V_{in} - V_o}{2 \cdot L} \cdot T_{on}$
$\Delta V_o = \frac{1}{\frac{1}{R_L} + \frac{1}{L} \cdot \frac{T_{on}}{2}} \Delta I_{ADC}$	$\Delta V_o = \frac{1}{\left(\frac{1}{R_L} + \frac{V_{in}}{V_o^2} \cdot S_e \cdot T_{on} + \frac{T_{on}}{2 \cdot L} \right)} \Delta I_{ADC}$
$\frac{1}{\frac{1}{R_L} + \frac{1}{L} \cdot \frac{T_{on}}{2}} \Delta I_{ADC} < \Delta V_{ADC}$	$\frac{1}{\left(\frac{1}{R_L} + \frac{V_{in}}{V_o^2} \cdot S_e \cdot T_{on} + \frac{T_{on}}{2 \cdot L} \right)} \Delta I_{ADC} < \Delta V_{ADC}$

From this comparison, we can see that although the voltage ADC resolution is same, the external ramp reduces the required current ADC resolution. To prove this benefit, we design the two current ADC resolutions: one is without an external ramp and the other one is with an external ramp.

For the case without the external ramp, the current ADC requirement is same as equation (63), repeated in (64):

$$\Delta I_{ADC} < \left(\frac{1}{R_L} + \frac{1}{L} \cdot \frac{T_{on}}{2} \right) \Delta V_{ADC} = 0.054A \quad (64)$$

If we choose 40A as the current ADC conversion range, then 11 bits is preferred to leave a certain design margin:

$$\Delta I_{ADC} = \frac{40}{2^{11}} = 0.0195 \quad (65)$$

However, if we choose an external ramp slope equal to 4 times the inductor current's down slope, then the current ADC requirement becomes:

$$\Delta I_{ADC} < \left(\frac{1}{R_L} + \frac{V_{in}}{V_o^2} \cdot S_e \cdot T_{on} + \frac{T_{on}}{2 \cdot L} \right) \cdot \Delta V_{ADC} = 0.192A \quad (66)$$

In this case, using the same conversion range, 40A, 9-bit is good enough to achieve this resolution requirement. So with the external ramp, the current ADC resolution requirement can be alleviated.

Another benefit of the external ramp is reducing the sampling frequency of current ADC. Figure 3.24 shows a simulation result to illustrate this benefit.

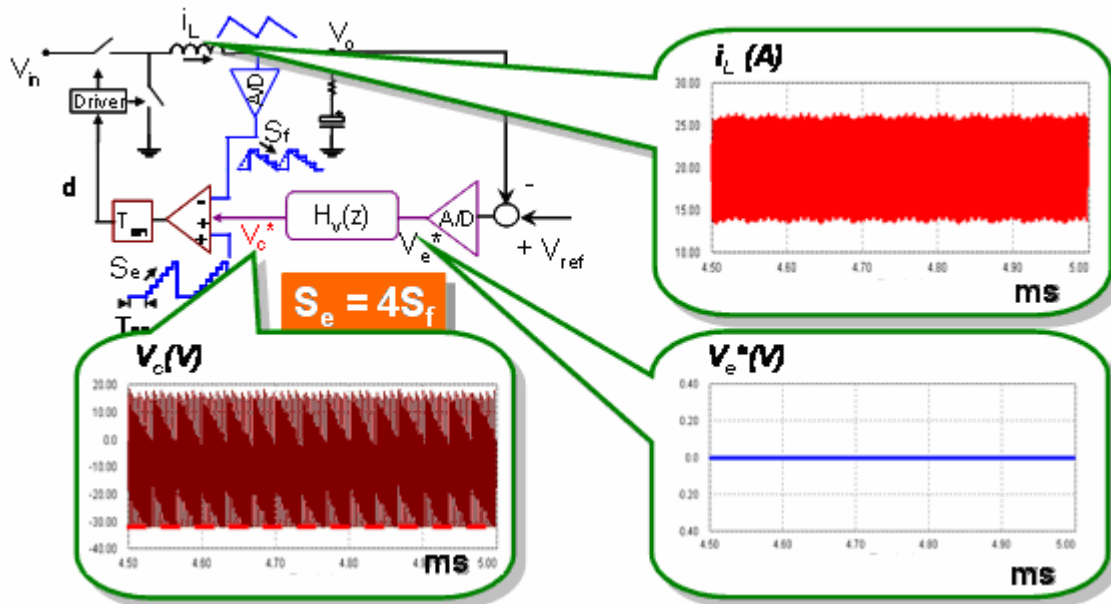


Fig. 3.24 Simulation Case with External Ramp ($S_e = 4 S_f$, $F_{sample} = 3 F_s$)

In this simulation, we use $S_e = 4 S_f$ external ramp and the current ADC sampling frequency is equal to 3 times the switching frequency. The current ADC resolution is as previously designed, 9 bits for 40A. We can see that the error voltage V_e^* is equal to zero and the V_c , the bottom line of external ramp, is flat. Thus, there is no oscillation on the V_c and V_e^* and the limiting function is still achieved.

3.3. Design of Feedback Control

In sections 3.1 and 3.2, the oscillation problem is analyzed and resolutions for two ADCs are also designed. However, how to design the compensator is still an issue for this control structure. In this section, the feedback design of the digital constant on-time current-mode control will be introduced.

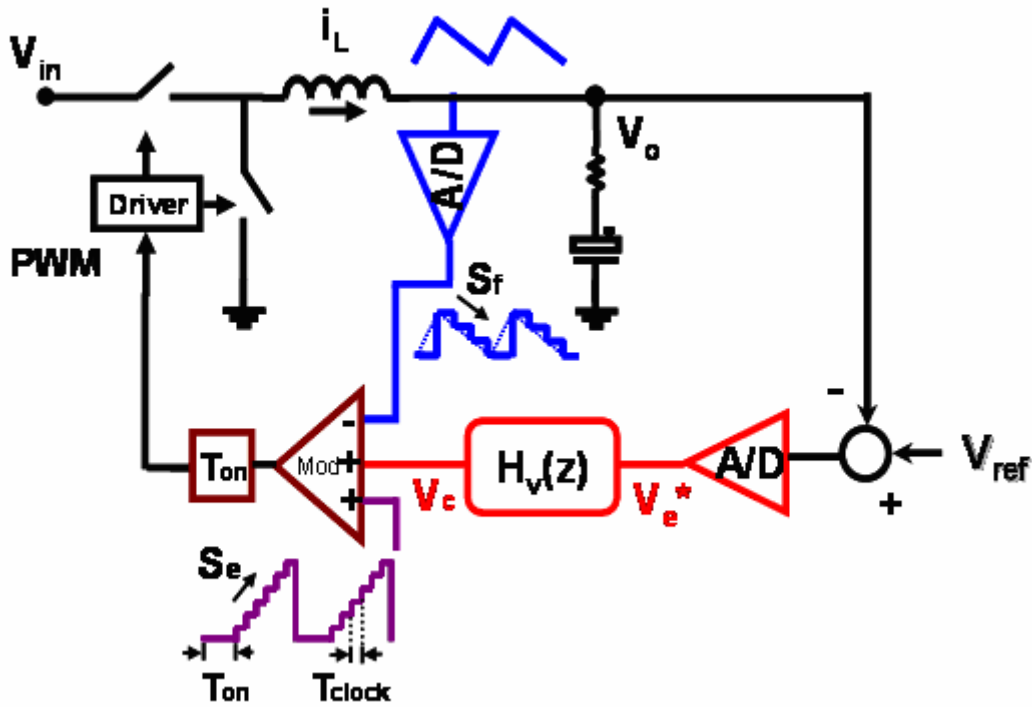


Fig. 3.25 Circuit Blocks of Digital Constant On-time Current-Mode Control

Figure 3.25 shows the system to be designed. Based on the review in the first chapter of this thesis, the digital compensator design should meet the gain margin requirement, as shown in below:

$$GM_L > 20 \cdot \log\left(\frac{4}{\pi}\right)^2 = 4.2dB \quad (67)$$

However, for the common practice of the control design for DC/DC converter, the phase margin is another requirement that must be met for stability. For example,

$$PM_L \geq 60^\circ \quad (68)$$

After satisfies the above two requirements, we can design the compensator to give us enough bandwidth in order to have a reasonable transient.

Based on the above design criteria, let's come back and take a look at the model of the digital constant on-time current-mode control, which developed in chapter 2. The figure 3.26 shows the loop model for the digital constant on-time current-mode control.

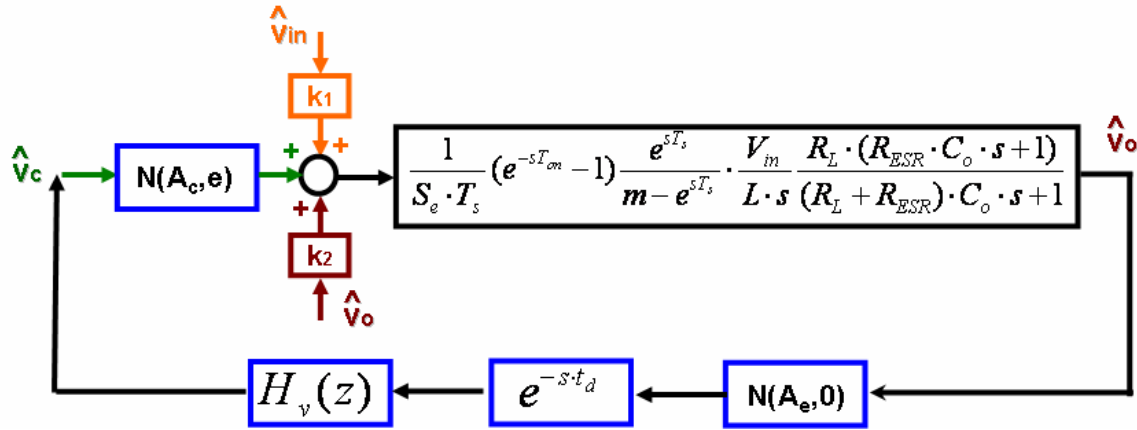


Fig. 3.26 Loop Model of Digital Constant On-time Current-Mode Control

From figure 3.26, it is quite obvious that within the loop, there are two nonlinear gain terms: $N(A_c, e)$ and $N(A_e, 0)$. From chapter 2, we also know that these two nonlinear gains are the same as those in the digital voltage-mode control case. So a similar design guideline from the digital voltage-mode control case can be applied. In the digital constant on-time current-mode control case, the linear part is now defined as:

$$T_L(s) = DF \cdot Z_c(s) \cdot e^{-s \cdot t_d} \cdot H_v(e^{s \cdot T_{sample}}) \quad (69)$$

In this linear part's transfer function, the $Z_c(s)$ is the input impedance of the parallel branches of the output capacitor and the load resistor:

$$Z_c(s) = R_L // \left(ESR + \frac{1}{s \cdot C_o} \right) \quad (70)$$

Before we can design the compensator, the external ramp slope should be determined. From [33], we know that the larger the external ramp slope, the smaller oscillation amplitude. From the section 3.2 analyses, we know that the larger external ramp slope also gives us the benefit of reducing the current loop ADC resolution requirement. So from an oscillation amplitude and resolution point of view, a larger slope is preferred.

However, the larger external ramp will give us trouble, especially when there is a large delay in the loop. For the constant on-time modulator, if we sample the output voltage at the middle of on-time, the delay time can be calculated. Figure 3.27 shows the time delay in digital constant on-time modulator when output voltage samples are taken at the middle of on-time.

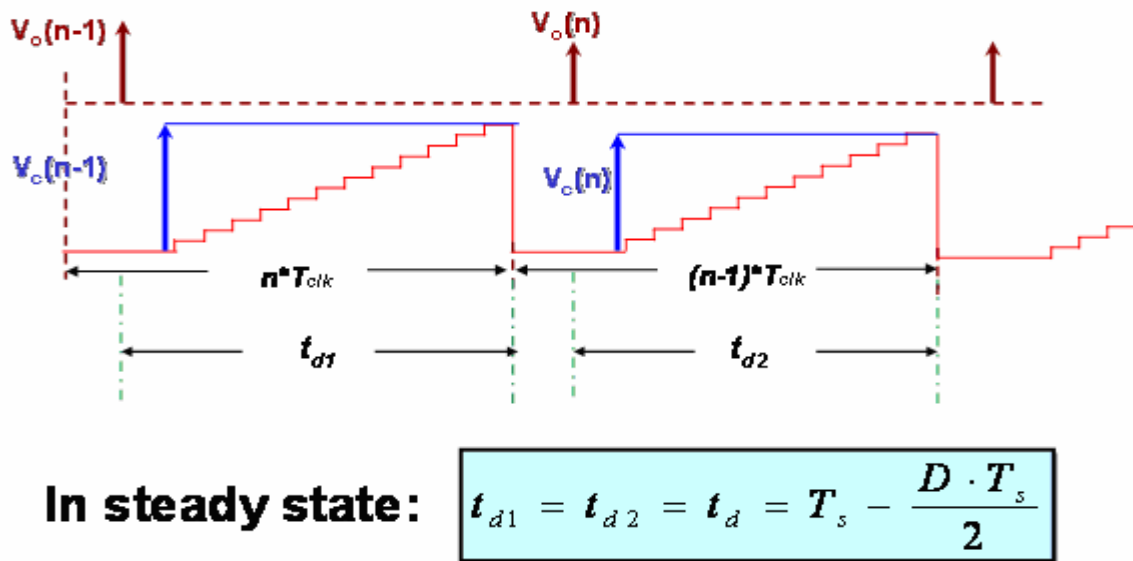


Fig. 3.27 Time Delay in Digital Constant On-time Control

As we can see from figure 3.27, the time delay is:

$$t_d = T_s - \frac{D \cdot T_s}{2} \quad (71)$$

With this amount of time delay, the larger external ramp slope will give us big trouble because the external ramp drops the phase in control-to-output transfer function, as shown in figure 3.28.

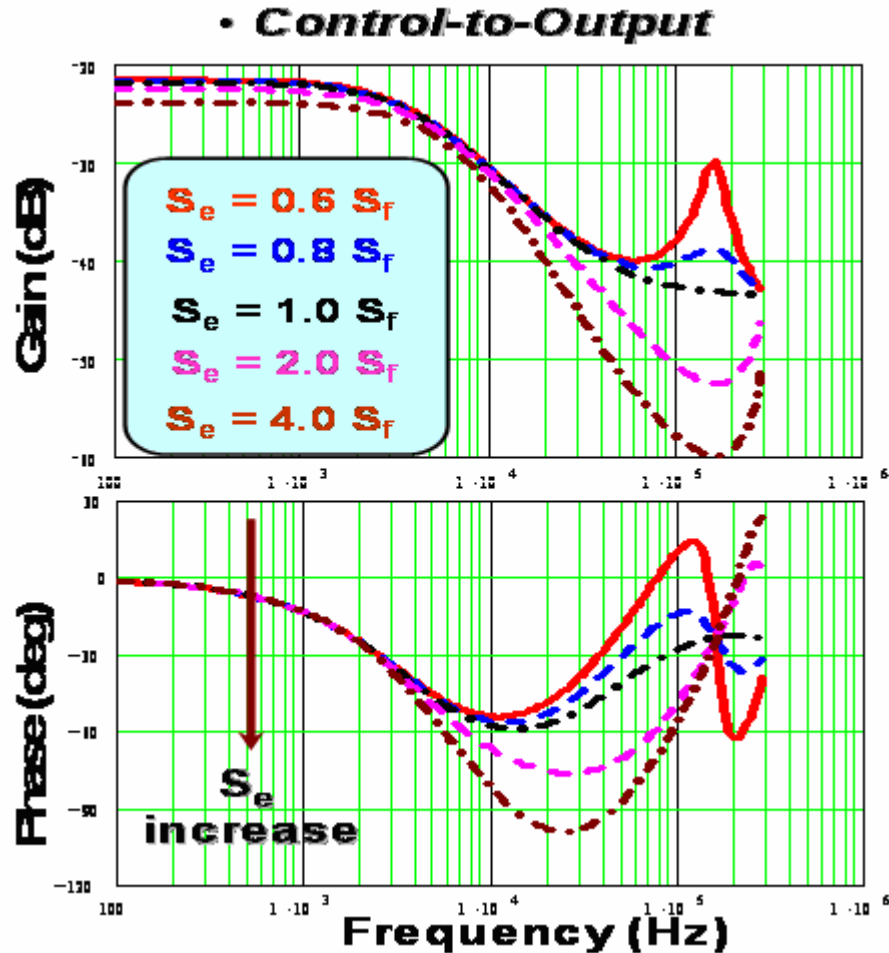


Fig. 3.28 Control-to-output Transfer Function with Different External Ramp Slope

Figure 3.28 shows the control-to-output transfer function without delay time. As we can see that when the external ramp's slope becomes larger, the phase drop of the control-to-output transfer function becomes worse, especially in the frequency range we are interested. If we further take the delay into account, this phase drop will be even worse. So we cannot choose too large external ramp slope. In our design, the $S_e = 4 S_f$ is selected as a trade-off between oscillation amplitude and phase characteristics.

Before we design the compensator, the control-to-output transfer function with delay is shown in figure 3.29.

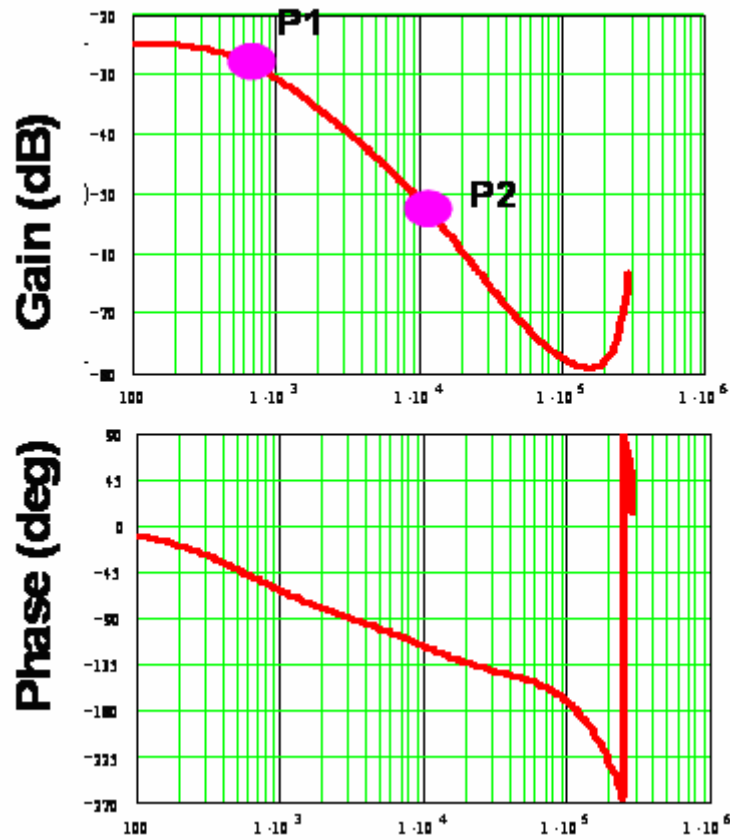


Fig. 3.29 Control-to-output Transfer Function with Time Delay

The transfer function is shown below. From figure 3.29, we can see that there are two separate poles.

$$G_{vc}(s) = DF \cdot \frac{V_{in}}{L \cdot s} \cdot Z_c(s) \cdot e^{-s \cdot t_d} \quad (72)$$

In the first design, the common compensator in current-mode control is utilized. It is a 1-pole 1-zero compensator. The second pole is ignored because in our output voltage sampling mechanism, the output voltage's switching ripple will not be injected into the control loop. So there is no need to use the second pole to attenuate the switching ripple. Figure 3.30 shows two design examples.

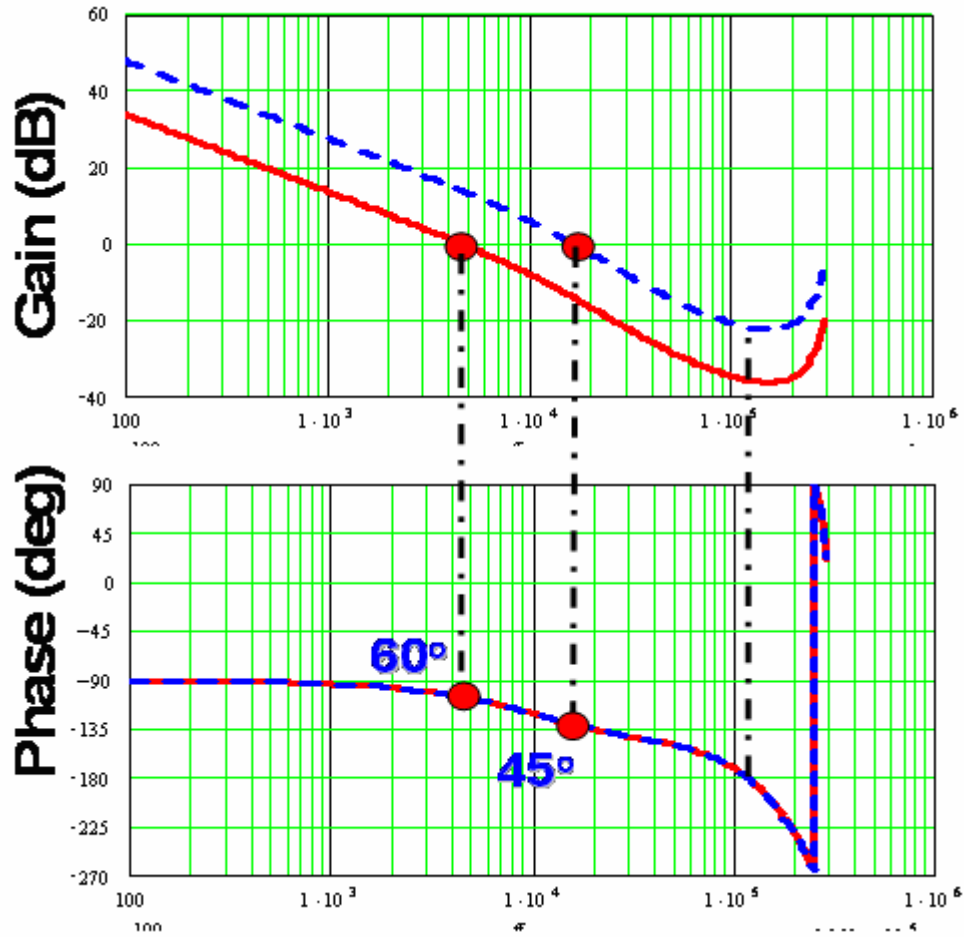


Fig. 3.30 Design Results with 1-Pole 1-Zero Compensator

Here the compensator structure is:

$$H_v(s) = \frac{k}{s} \left(1 + \frac{s}{\omega_z}\right) \quad (73)$$

The zero is used to cancel the first pole and the integrator gain is used to push the bandwidth. In the two cases, the bandwidth is really low. If we push the bandwidth to be a 20th of the switching frequency, 300 kHz, the phase margin is already not enough. But as we can see, the gain margin is quite enough for these two cases. So in this compensator design, the phase margin limits the bandwidth and the bandwidth is too low.

The second design case uses 2-pole 2-zero compensator. The design results are shown in figure 3.31.

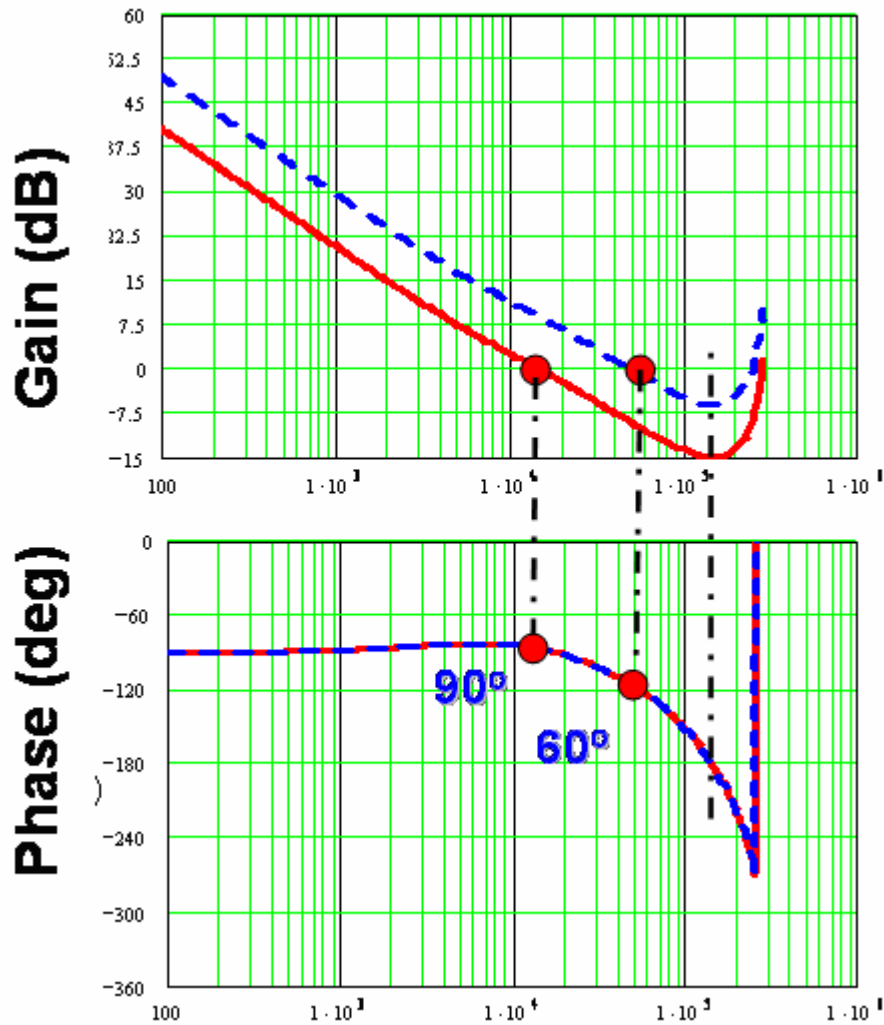


Fig. 3.31 Design Results with 2-Pole 2-Zero Compensator

The compensator structure is:

$$H_v(s) = \frac{k}{s} \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \cdot \left(1 + \frac{s}{\omega_{z2}}\right)}{1 + \frac{s}{\omega_{p1}}} \quad (74)$$

Here, the first zero is still used to cancel the first pole and the second zero is used to push the phase margin. The second pole is used to cancel the ESR zero. The integrator gain is still used to push the bandwidth.

In these two designs, we can see that now the bandwidth is pushed to be one 6th of the switching frequency. The phase margin is still 60 degree. However the gain margin is reduced to be about 7 dB. If we further push the bandwidth, the gain margin will be not enough.

Figure 3.32 and 3.33 show the steady-state simulation waveform for 2-pole 2-zero compensator case. The bandwidths are equal to one 20th of the switching frequency and one 6th of the switching frequency.

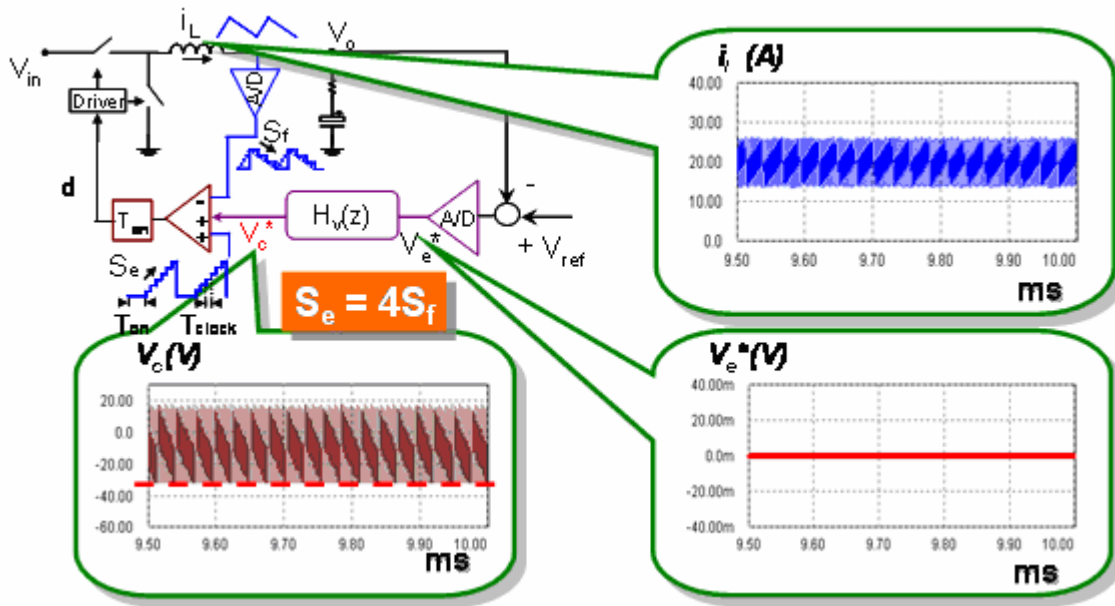


Fig. 3.32 Steady-state Simulation: second design @ BW = Fs/20

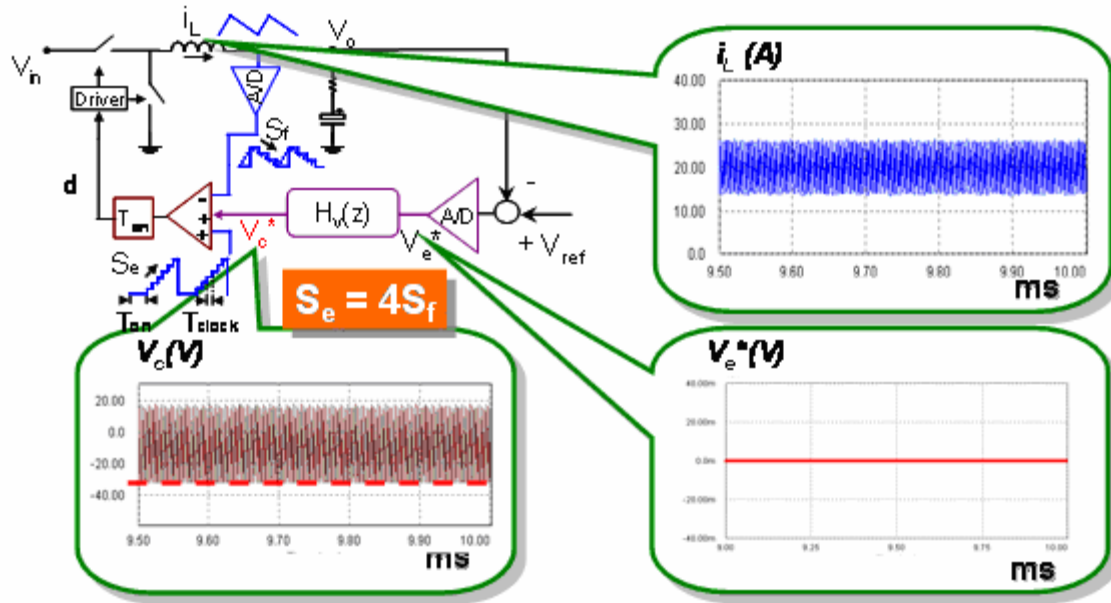


Fig. 3.33 Steady-state Simulation: second design @ $BW = F_s/6$

For both designs, we can see that there is only current loop oscillation; the voltage loop oscillation doesn't exist. Figure 3.34 shows the transient comparison between these two cases to show the validity of bandwidth improvement.

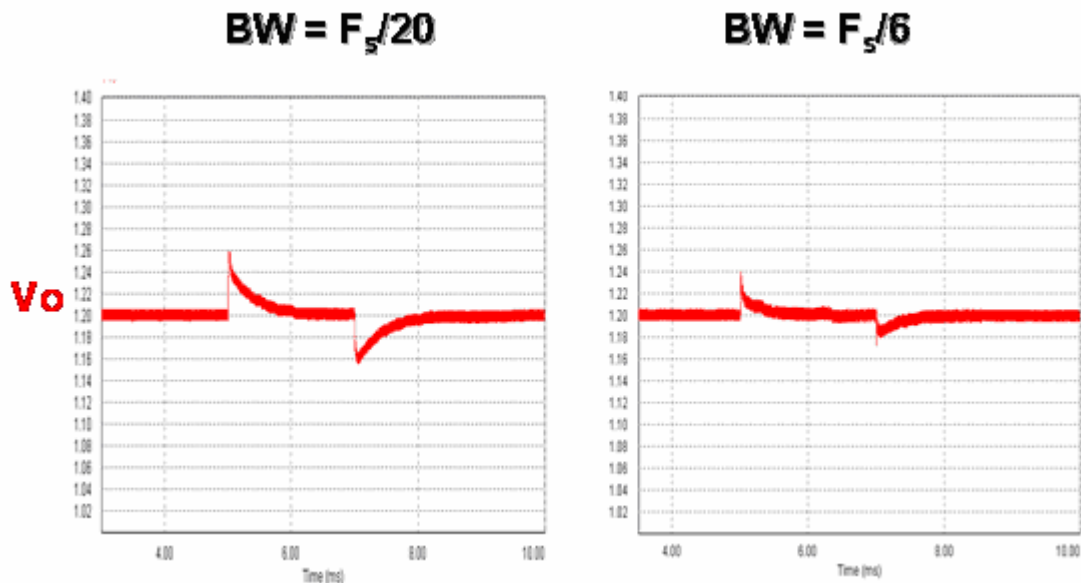


Fig. 3.34 Transient Comparison

In above transient simulation, the load current is stepping down from 20 A to 0 A and back to 20 A. The slew rate of load current is 100A/us.

Chapter 4 Conclusion and Future Work

In this thesis, the topic of modeling and design of digital controlled DC/DC converter is studied.

Digital control is increasing its application in DC/DC converter application. But it also brings some issues to the system. One of these issues is limit cycle oscillation caused by the interaction between DPWM quantization effect and ADC quantization effect. For this issue, a lot of solutions have been developed to reduce or eliminate it.

For the voltage-mode control case, a loop model is reviewed and verified in simulation and also the design guideline. Based on this modeling methodology and design guideline, we studied the digital constant on-time current-mode control structure which is proposed in CPES to reduce the high resolution DPWM requirement.

Firstly, a describing function model is developed for this control structure, which includes the sample-hold effect in current loop ADC. And then, for the quantization effect in current ADC, by extending the similar describing function modeling concept as literature and using the simulation tool, we get the nonlinear gain curve for the quantization effect from current ADC in our control structure. So a complete model is finally built for current loop. Then, simulation is performed to verify this model.

Secondly, to design this control structure, we first analyze the oscillation issue in this structure. Based on our analysis, we find that the digital constant on-time current-mode control structure has a good benefit on its oscillation problem. If we don't consider the quantization effect, the sample-hold effect will give the oscillation in current loop, but this oscillation amplitude is well limited in one sampling step. So if we increase the sampling frequency, we can reduce this oscillation amplitude in a well-controlled manner. However, this oscillation is inevitable. When we consider the quantization effect from

current ADC and voltage ADC, the oscillation might become worse. To possibly minimize the current oscillation amplitude, the quantization effect should be tackled in our design.

To tackle this quantization issue and to minimize this oscillation amplitude, thirdly, the steady-state condition for design of current ADC resolution and voltage ADC resolution is given out. For the structure with external ramp, we find that the external ramp can help us to achieve the steady-state design condition more easily, giving the benefits of both reducing the sampling frequency and number of bits for the current ADC.

In the final chapter, how to design the dynamic response is also taken into consideration: how to achieve the goals of transient response while keeping satisfying the requirements from limit cycle oscillation and stability. We use 2-pole 2-zero compensator to design the loop and achieve the bandwidth at one 6th of switching frequency

One aspect about future work is current sharing. For digital constant on-time current-mode control, we are studying the single-phase case. If we extend it into multi-phase, how to share the current between phases?

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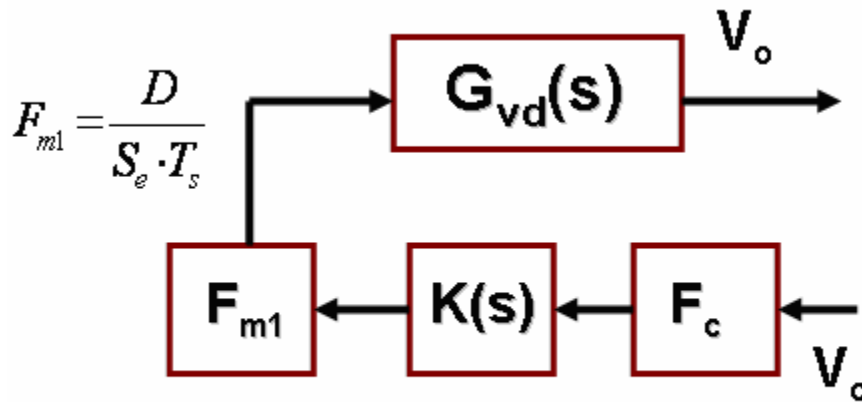
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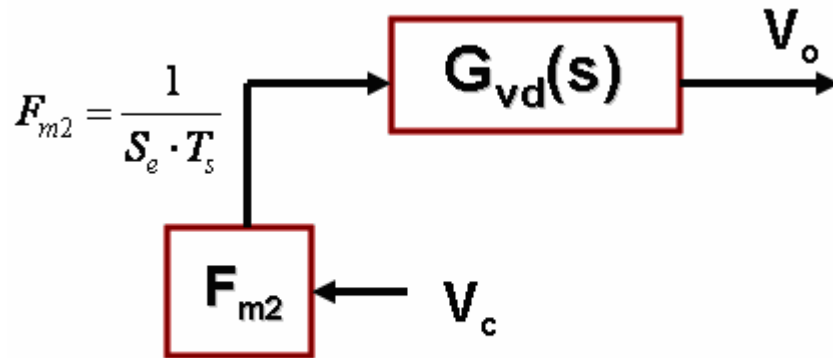
Appendix

A comparison between analog constant on-time modulator with constant frequency modulator is shown in Fig. A. 1. Here (a) is the result of voltage-mode control from literature [37].



Constant on-time

(a) Constant On-time Modulator Model



Constant frequency

(b) Constant Frequency Modulator Model

Fig. A. 1 Constant On-time V.S. Constant Frequency

Fig. A. 2 shows the delay in digital constant on-time modulator.

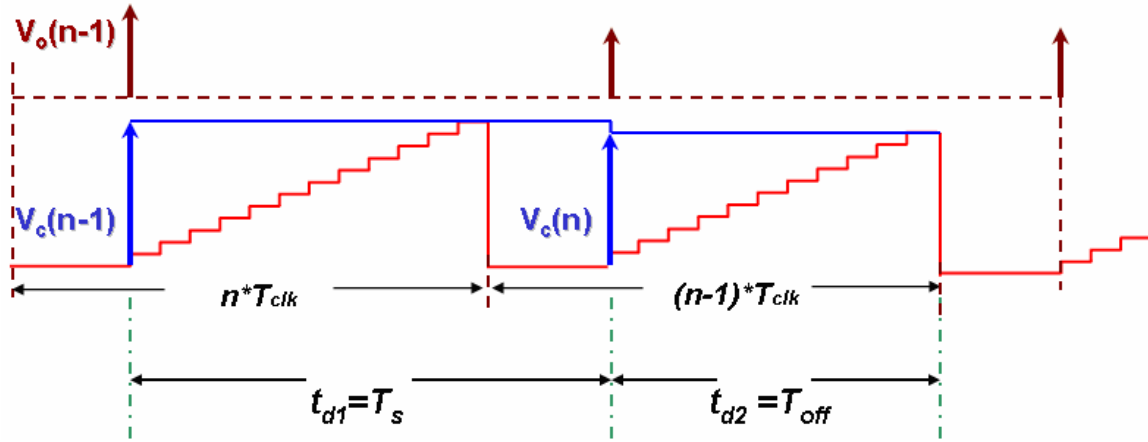


Fig. A. 2 Time-delay Calculation for Digital Constant On-time Modulator

In this figure, the control V_c updating scheme is following the assumption as:

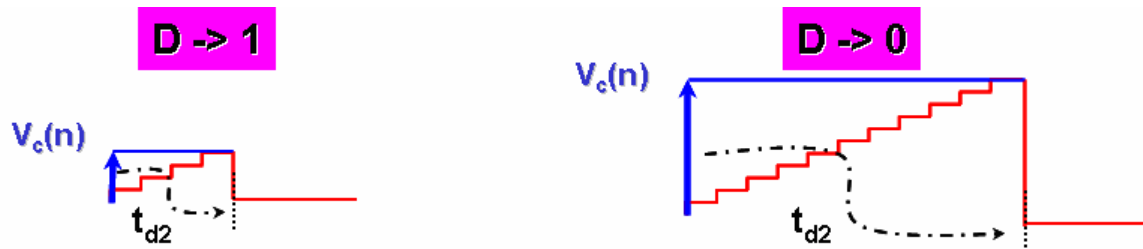


Fig. A. 3 Control Update Scheme Rule

In steady state, the time delay will be:

$$t_d = t_{d1} + t_{d2} = T_s + (1-D) \cdot T_s \quad (\text{A.1})$$

This is a quite large delay when duty cycle is relative small. This conclusion is true for current-mode constant on-time control case if the control V_c is still update at same way as shown in figure A.3.

One solution is using multiple sampling techniques, as shown in figure A.4.

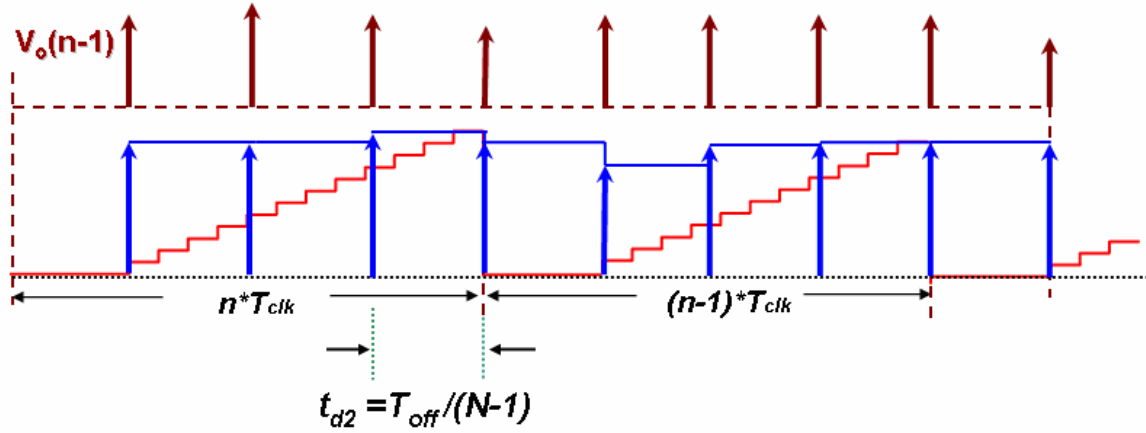


Fig. A. 4 Multiple Sampling Technique To Reduce the Time Delay in Constant On-time Modulator

Here the relation between switching frequency and sampling frequency is as:

$$T_s = (N-1) \cdot T_{sample} + T_{on} \quad (A.2)$$

So the time delay will be reduced to be:

$$t_{cd} = t_{ZOH} - t_{Fc} = \frac{(1-D) \cdot T_s}{N-1} - \frac{(1-D) \cdot T_s}{2} \quad (A.3)$$

The t_{zoh} is the delay associated with zero-order hold in multi-sampling control and t_{Fc} is the delay from analog constant on-time modulator.

Vita

The author, Bin Huang, was born in Ningbo, Zhejiang, China. He received the B. S. degree from Zhejiang University in 2001. From September 2001, he was pursuing his master in Tsinghua University and got his master in July 2004.

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