DEVELOPING MODELING AND SIMULATION METHODOLOGY FOR VIRTUAL PROTOTYPE POWER SUPPLY SYSTEM

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(ABSTRACT)

This dissertation develops a modeling and simulation methodology for design, verification, and testing (DVT) power supply system using a virtual prototype. The virtual prototype is implemented before the hardware prototyping to detect most of the design errors and circuit deficiencies that occur in the later stage of a standard hardware design verification and testing procedure. The design iterations and product cost are reduced significantly by using this approach.

The proposed modeling and simulation methodology consists of four major parts: system partitioning, multi-level modeling of device/function block, hierarchical test sequence, and multi-level simulation. By applying the proposed methodology, the designer can use the virtual prototype effectively by keeping a short simulation CPU time as well as catching most of the design problems.

The proposed virtual prototype DVT procedure is demonstrated by simulating a 5 V power supply system with a main power supply, a bias power supply, and other protection, monitoring circuitry. The total CPU time is about 8 hours for 780 tests that include the basic function test, steady stage analysis, small-signal stability analysis,

large-signal transient analysis, subsystem interaction test, and system interaction test. By comparing the simulation results with the measurements, it shows that the virtual prototype can represent the important behavior of the power supply system accurately. Since the proposed virtual prototype DVT procedure verifies the circuit design with different types of the tests over different line and load conditions, many circuit problems that are not obvious in the original circuit design can be detected by the simulation.

The developed virtual prototype DVT procedure is not only capable of detecting most of the design errors, but also plays an important role in design modifications. This dissertation also demonstrates how to analyze the anomalies of the forward converter with active-clamp reset circuit extensively and facilitate the design and improve the circuit performances by utilizing the virtual prototype. With the help of the virtual prototype, it is the first time that the designer is able to analyze the dynamic behavior of the active-clamp forward converter during large-signal transient and optimize the design correspondingly.

To my parents and husband

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1. INTRODUCTION

With the increasing capabilities of computer software and CPU speeds, simulation is taking an increasingly important role in the circuit design process. Integrating circuit design and test procedures by simulation becomes an inevitable trend in today's highly competitive society [1-7]. By integrating simulation into the design process, a set of simulation tests can verify design concepts and uncover most of the potential design deficiencies before the first prototyping. Consequently, the product cost and time in the circuit design, verification, and testing (DVT) process can be reduced significantly.

Unlike design automation in integrated, especially digital, circuits, the simulation of a power electronic circuit is still a helpful tool, but not a necessary tool, in a circuit design [1-5]. The non-linearity of a power electronic circuit makes it far more sophisticated than an integrated digital circuit, and the simulation of a power supply system is not currently used anywhere in industry as a necessary design process. Today's design and test procedure of a complex power supply system still relies heavily on hardware breadboards and prototypes to do the vast majority of their design and concept verification; as a result, the production cost and time are consumed in this electrical DVT process.

This dissertation proposes a modeling and simulation methodology to develop a simulation procedure for power supply systems, so the conceptual circuit design can be verified, tested and improved before the hardware prototype DVT process to reduce the development cost and shorten the design time.

1.1 Background and motivation

1.1.1 Electrical design, verification, and testing of power supply system

1.1.1.1 Major electrical requirements of power supply system

The block diagram of a complex multi-output custom switching power supply system is shown in Fig. 1.1. There are four main power supplies in the system: three main power supplies (an ac - dc power factor correction circuit, a 5 V forward converter, and a 12 V multi-output forward converter) and a bias power supply. Each power supply has its own control, protection, monitoring, and enable circuits as shown in Fig. 1.1. The output of the PFC circuit provides the input to dc-dc converters; the 5V and 12 V forward converters power the output loads; and the bias power supply provides the power supply needed for control, protection, monitoring, and enable circuits of the system.

The major electrical requirements of a power supply system are shown in Fig. 1.2. It covers the customer specifications and design requirements of the power supply system in different categories, such as input, output, loss and stress, stability, logic signal, protection, start up and shut down. The input requirement includes maximum input current, inrush current, power factor, EMI, and so forth. The output requirement includes load regulation, output ripple voltage, cross-load regulation, and output voltage drift with temperature. The dynamic load response requirement is to verify the system output voltage specification during transient, such as maximum output voltage variants during load changes, output recovery time during transient. The loss and stress requirement includes efficiency, voltage and current stresses of the circuit components. The stability requirement includes crossover frequency, phase margin, and gain margin of the small-signal control loop gain. The logic signal requirement is to verify that all the monitoring signals used for display (e.g. the under-voltage signal) are correct during different circuit operations. The protection requirement is to verify the responses of the protection circuits during abnormal conditions (e.g. over-voltage, over-current, and over-temperature conditions). The start up and shut down requirement is the system's rising time, hold up time, output over/under shoot, and start up and shut down sequence. The hardware tests are limited to measure input and output signals of the system due to the integration of the circuit modules. Most of the tests are for customer specification verification.

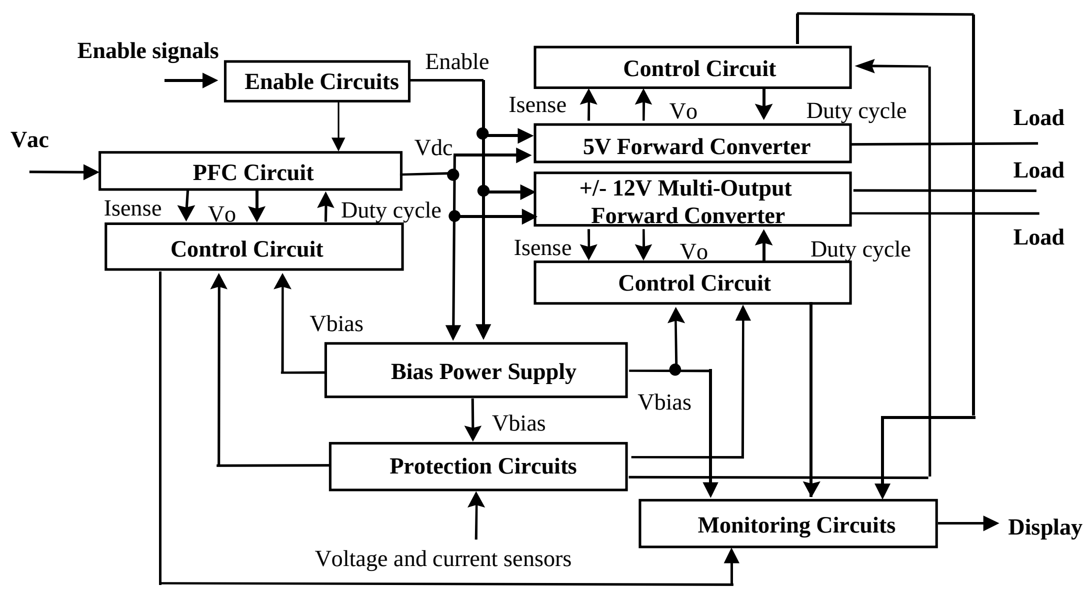


Fig. 1.1. Block diagram of a multi-output power supply system.

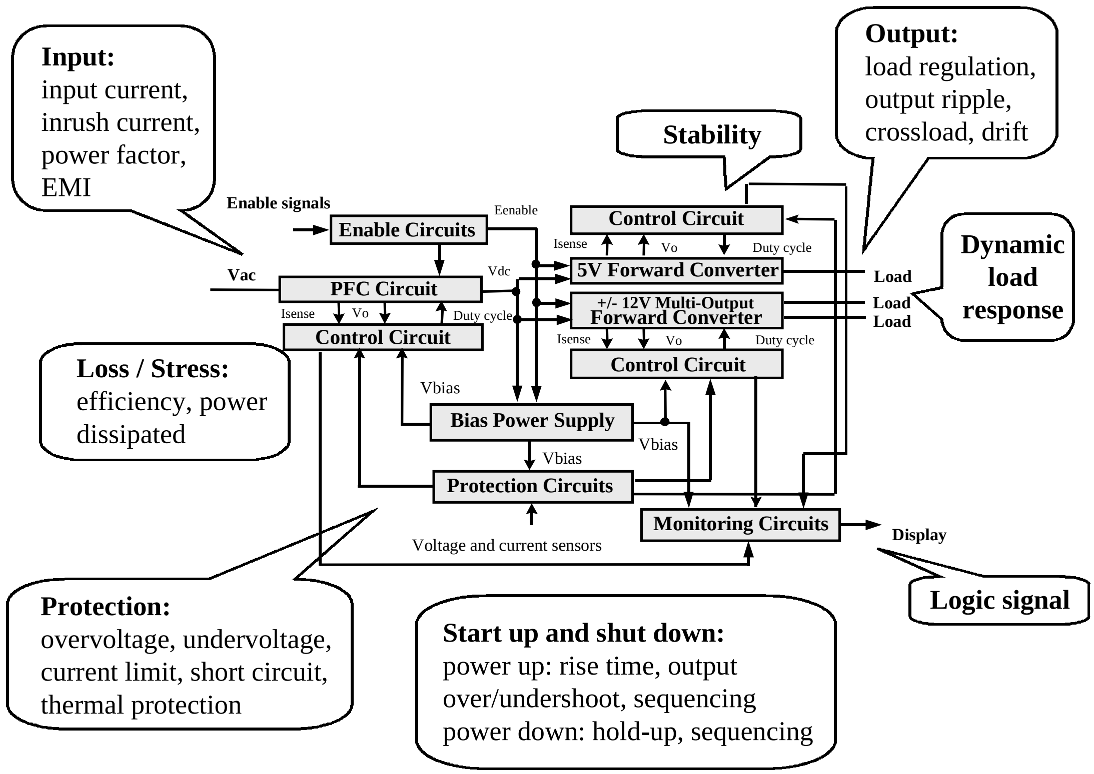


Fig. 1.2. Major electrical requirements in power supply system. The hardware tests are limited to measure input and output signals of the system due to the integration of the circuit modules. Most of the tests are for customer specification verification purpose.

1.1.1.2 Typical product development procedure

A typical product development procedure is shown in Fig. 1.3. After the initial paper design, a prototype is built to verify the design. Any errors found in the prototype test are fed back to the designer who would then have to go thorough another design iteration (i.e. debugging, redesign, even rebuilding the prototypes) to fix the problems. The debugging and prototyping time in the design iterations increase production cost and design time. The errors found in the later stage are more time and cost consuming, especially in the final production stage, as shown in Fig. 1.3.

Fig. 1.4 shows an example of a project development schedule from a company. The whole project development time is ten months, in which three design iterations from March to August take the major part of the whole schedule, as shown in the shaded area of Fig. 1.4. The total number of print wiring board (PWB) changes is six in three iterations, and these PWB changes increase design cost. Each additional design-iteration adds more than two months of the delay time of the product, in addition to the cost for prototyping. Different power supply products could end up with more iterations than the one in the example shown in Fig. 1.4. According to a static analysis from the same company, the worst case for PWB change is 19 with a total number of parts changes of 560 in the past several years. In the whole procedure of a project development, the design iterations increase product cost and time significantly.

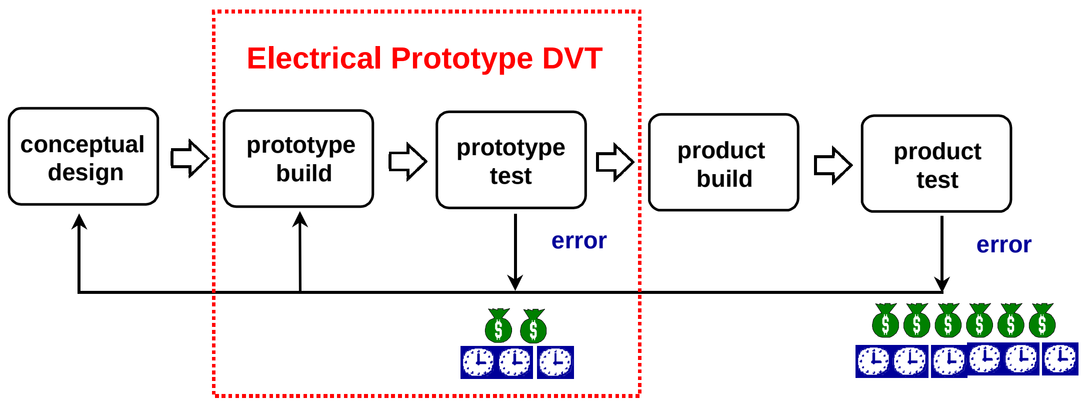


Fig. 1.3. In the typical product development procedure, the designers must rely very heavily on the prototype test to do the vast majority of their design and concept verification. Each design error, especially the one found in the later stage, needs to go through the design iteration, which increases production cost and time.

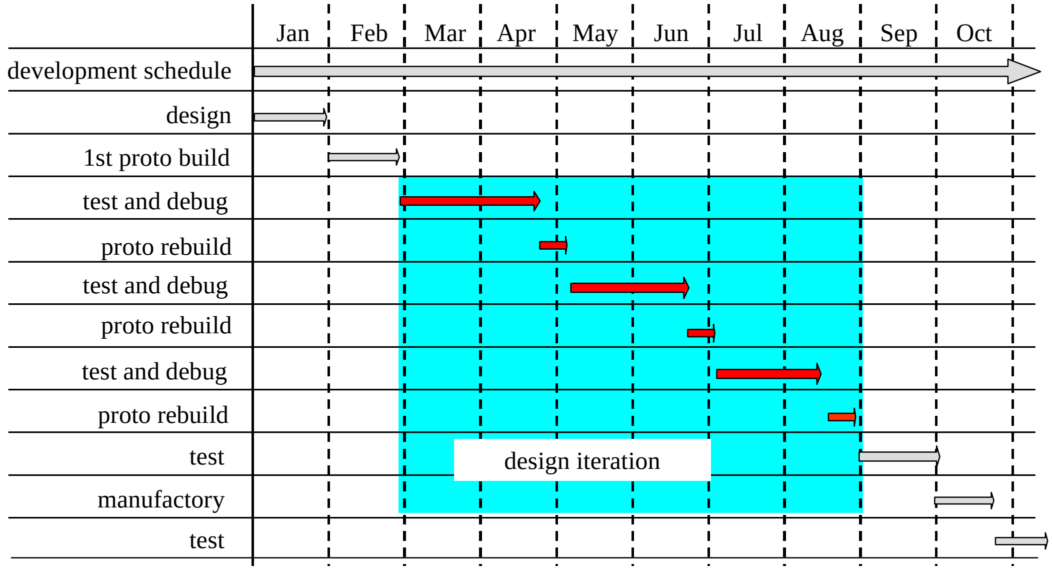


Fig. 1.4. Example of a project development schedule. The shaded area shows additional design cost and time due to design errors and iterations.

1.1.1.3 Error distribution survey of electrical test

Before searching for suitable approaches to reduce the product cost and time, it is very important to know the major types of errors and their distributions in the design process. According to prototype change order (PCO) data, which is collected from fourteen projects in six months from a company, a major circuit-error distribution chart is shown in Fig. 1.5. PWB changes in the chart means prototype rebuilding. The errors requiring PWB changes usually indicate more design cost and time. In Fig. 1.5, different design errors are summarized into ten categories as follows:

Compensator – problems related to control loop design, such as dc gain, phase and gain margin of the control loop. In many circuits, control loop redesign is necessary due to non-ideal characteristics of components such as operational amplifier, optical coupler, and parasitic parameters of the transformer and other components that have not been considered in the initial design.

Tweak protection circuit – problems related to adjustment of threshold voltages and currents in protection and monitoring circuits, such as over-voltage, under-voltage, over-current and current limit circuits. These circuits need to be adjusted to meet customer specifications and have fast and accurate response during abnormal circuit conditions. Due to non-ideal characteristics in a system, such as component tolerances, rising or falling times of IC chips, much time and effort for tweaking is involved in the hardware tests even though these circuits are relatively simple compared with some circuits in the system, such as main converters.

Steady state regulations – problems related to output voltage regulations, such as output voltage not meeting the specifications with certain line and load conditions.

Large-signal transient – problems, such as unstable circuits, exceeding a device's ratings, or output voltage overshoot exceeding the specifications during line or load large-signal transient.

Nonlinear operation – abnormal circuit operation due to non-linearity of components (e.g. excessive diode leakage current at high temperature affecting circuit logic, delay of devices introducing slow response of the system during over-voltage).

Interaction – system interaction problems, such as interaction between bias power supply and control and protection circuits.

Start-up and shut down -- system errors during start-up and shutdown such as wrong timing or sequence (e.g. soft start, hold off time).

Thermal – overheat of devices (which need larger rectifiers or fast FETs to lower temperature) or over-temperature protection.

High frequency noises – circuit problem related to high frequency parasitic parameters, such as EMI or layout (e.g. noise on IC, adding noise reduction caps, moving ground location).

Misc. – miscellaneous errors which are not directly related to design (e.g. mistakes in a document: wrong part number, schematic drawing error, parts change due to cost or bad performance of part, customer specification change).

Among these design errors, system interaction, start-up sequencing, and abnormal operation of a circuit under specific load and line conditions are the most time-consuming errors.

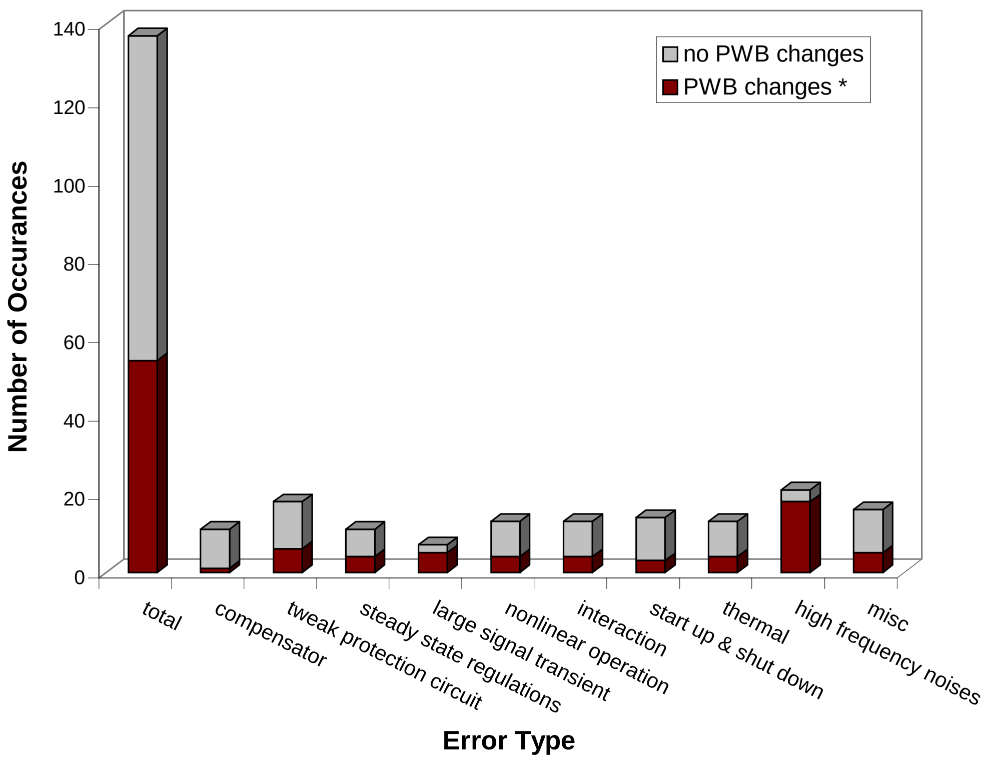


Fig. 1.5 Major circuit error distribution chart for fourteen projects in six months from a company prototype change order (PCO) survey. PWB change in the chart means prototype rebuilding.

1.1.2 Virtual prototype design, verification, and testing of power supply system

1.1.2.1 Introduction of virtual prototype DVT

Fig. 1.6 is the redrawing of the project development schedule in Fig. 1.4. The shaded area shows the additional product cost and time due to the design iterations. These design iterations can be reduced by a set of simulation tests before prototype building. The proposed product development procedure is shown in Fig. 1.7. After the circuit conceptual design, a virtual prototype of the power supply system is built using a simulation tool with adequate models. By running a set of simulation tests in a virtual prototype in this earlier stage, most of the errors found in a later stage in a typical product development procedure can be detected before prototyping. Then, these errors are debugged and fixed in the virtual prototype by computer-aided design. The whole simulation process is called virtual prototype DVT as shown in Fig. 1.7. By integrating the virtual prototype DVT into the typical product development procedure, the errors which used to be found in the electrical prototype test and product test will be reduced; consequently, the design iterations, the product cost and time can be reduced.

Fig. 1.7 shows that the virtual prototype DVT is implemented for three purposes: verifying circuit operations and specifications, detecting most of the design errors before prototyping, providing design information to help the designer debug and fix design errors. The rest of the chapters are going to demonstrate how to fulfill these tasks.

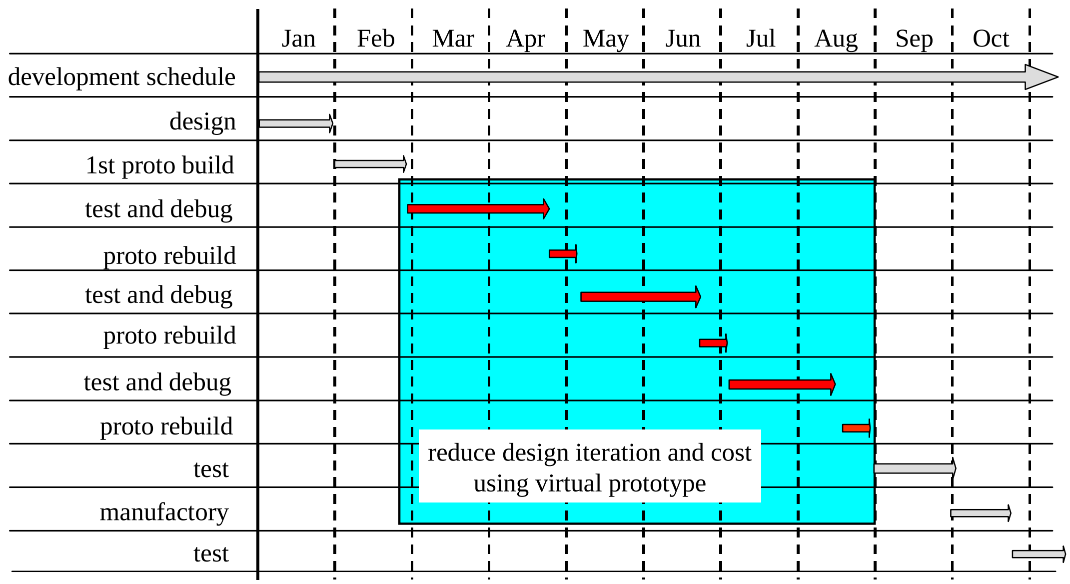


Fig. 1.6. Redrawing of the project development schedule in Fig. 1.4. The virtual prototype DVT intends to reduce design iterations in the shaded area.

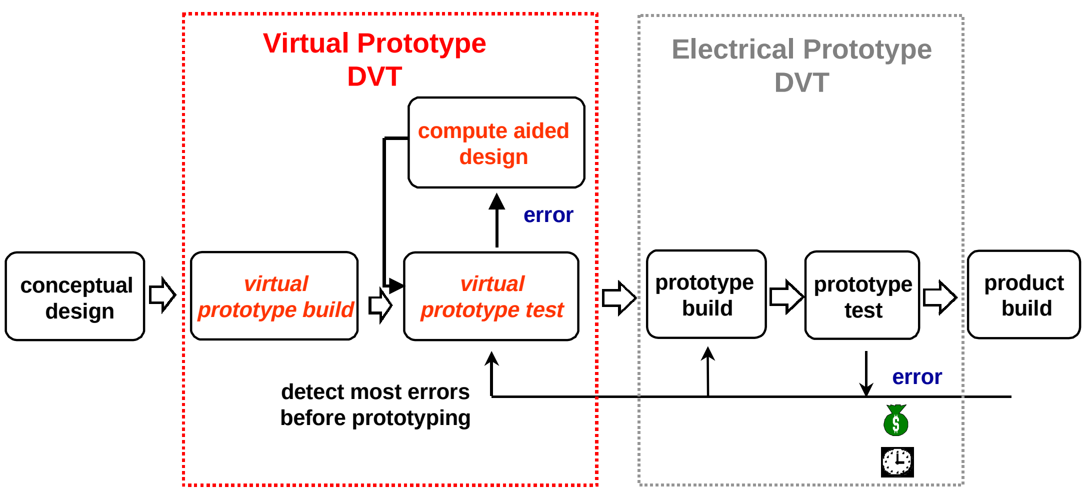


Fig. 1.7 In the proposed product development procedure, most of the design errors can be detected in the virtual prototype test before the first prototyping, so the number of design iterations can be minimized to reduce product cost and time.

1.1.2.2 More comprehensive performance testing / verification via virtual prototype

The virtual prototype has more comprehensive performance testing and verification advantages over the hardware prototype, such as:

The virtual prototype will not be damaged as the hardware prototype when the devices are overstressed or the circuit operates abnormally in some tests (e.g. the short-circuit test).

Unlike the hardware prototype of the power supply system, which is an integrated module, it is easier for the virtual prototype to take out part of the circuit or disable part of the system in order to debug or test system functions.

It is hard to verify the whole system's behavior in the hardware prototype, since the probe points of the prototype are limited in a single test. However, with a virtual prototype, there is more freedom of monitoring points.

It is easier to implement test automation in the virtual prototype than in the hardware prototype, so more operational conditions can be verified in the virtual prototype test to enhance the system stability.

When redesigning or debugging the circuit, the virtual prototype is easier to change component values and modify circuits.

Although the virtual prototype test has these advantages, the hardware prototype test is still necessary due to the limitation of the virtual prototype. For example, it is very hard to implement the virtual prototype in an available general circuit simulation software by considering circuit parasitic parameters due to circuit layout or high frequency noise, and the device or IC chip nonlinear characteristics due to the drift of temperature and time.

In order to minimize the errors in the design iterations, the virtual prototype test should cover the electrical test in a typical procedure as much as possible and implement additional tests when necessary. The major virtual prototype tests of the same system as Fig. 1.1 are shown in Fig. 1.8.

Compared to the electrical test in Fig. 1.2, the virtual prototype test covers most of the electrical tests except those related to EMI, layout, drift, and thermal issues. These uncovered tests are marked in gray italic font in Fig. 1.8. Additional tests are shown in shaded areas in Fig. 1.8, which are used to enhance the system stability.

By integrating the virtual prototype test into the test procedure as shown in Fig. 1.7, we can detect most of the errors found in the electrical test in a typical test procedure. The estimated error-covered area related to the error distribution chart in Fig. 1.5 is shown in Fig. 1.9. The dark areas show the errors that could be detected by the virtual prototype test. Due to the limitation of the virtual prototype, the major problems that cannot be covered are related to EMI, layout, and thermal issues as shown in Fig. 1.9.

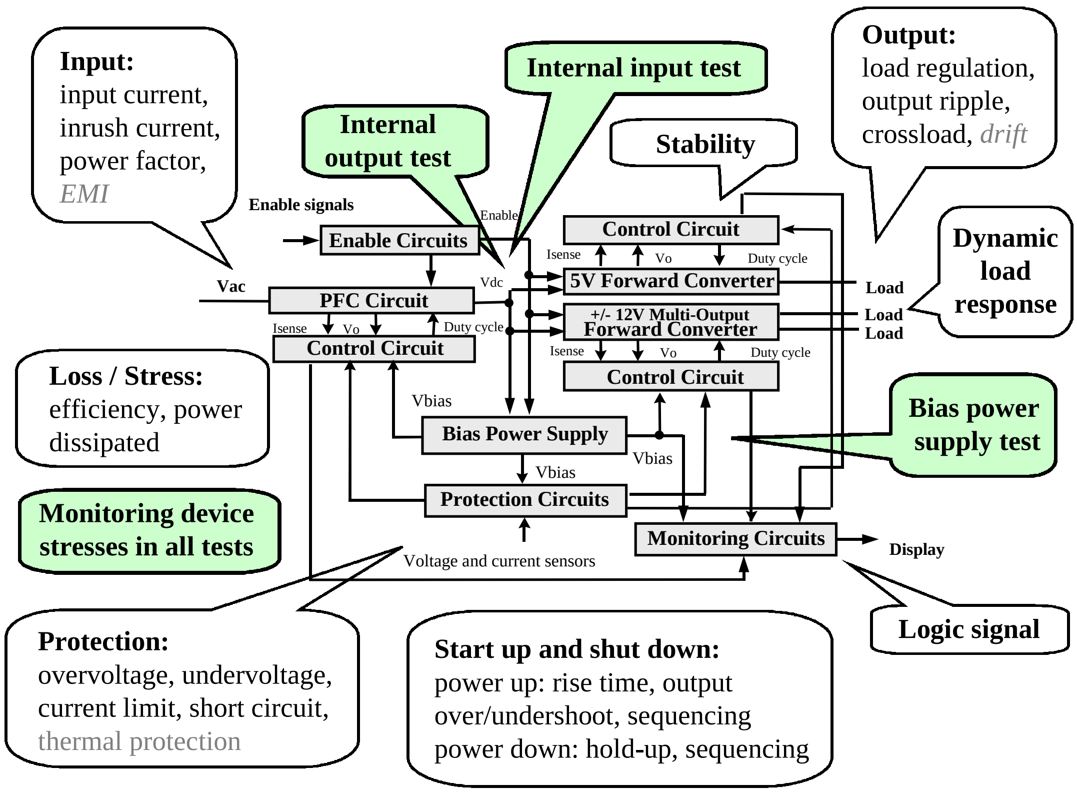


Fig. 1.8. Major tests in the virtual prototype test. Additional tests can be added for stability purposes, which are in shaded areas. However, the virtual prototype test cannot tackle problems related to thermal, EMI, and layout; these tests are shown in gray italic color.

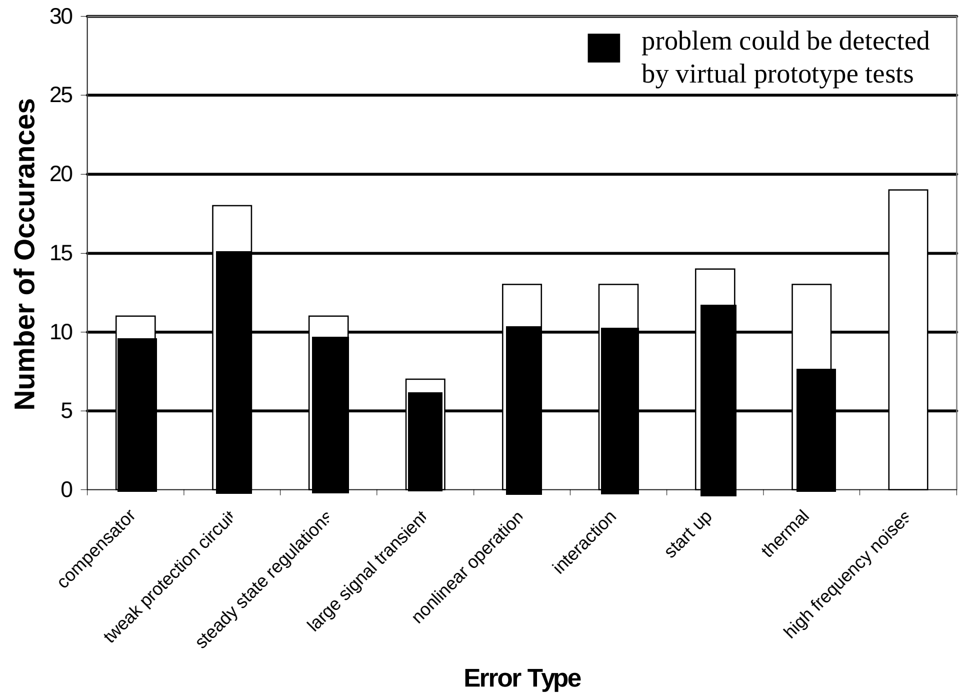


Fig. 1.9. Estimated covered error area of the virtual prototype test. The dark areas show the problems that could be solved by virtual prototyping.

1.1.2.3 Fast algorithm and adequate accuracy for virtual prototype simulation engine

The design errors found in a later stage of a typical electrical test, especially at the product building stage, are usually more time and cost consuming. These errors are often not obvious in the initial design and occur only in some particular operating points. It is very important for a virtual prototype test to cover the whole operating range of the system to find these problems. After finding problems, more simulations are needed to debug and fix the problems and to verify the modified circuit. For a complex power supply system, hundreds to thousands of simulation tests are involved in a complete design process.

In order to implement the virtual prototype test, there are two requirements for the virtual prototype simulation engine. The first requirement is that the virtual prototype should be built on a very fast simulation engine. If it takes several weeks to complete thousands of simulation tests, the virtual prototype test is not a practical approach to be used in a day-to-day design process. The second requirement is that the virtual prototype should represent accurate system behavior so the real problems can be caught in the simulation. A simulation engine for the virtual prototype test is going to be selected based on these criteria.

1.2 Objective and dissertation outline

1.2.1 Objective

Although the concept of the virtual prototype test has been introduced more than a decade ago [1-6] and sounds so promising, simulation has not been used as a routine manner as part of the design process. The major issue is the conflicts between the simulation speed and system accuracy [30-34]. Currently, the simulation role is largely reserved for conceptual feasibility studies, specific problem resolution, and other academic applications.

Most recent studies have focused on trying to simulate one performance aspect of one simplified representation of a real production circuit, the methodology that is effective to simulate the virtual prototype is wholly insufficient. No commercial tool has been designed specially for this purpose. No one has ever demonstrated what must be done in order to make a virtual prototype test detect a high percentage of the latent design errors that exist in a production schematic during the development process with an affordable amount of time and effort.

This dissertation proposes a modeling and simulation methodology and a test procedure to set a frame for the virtual prototype test. The purpose of the simulation is not only to detect a high percentage of the latent design errors existing in a practical power supply system, but also to provide circuit information to help the designer debug and fix design errors.

The multi-level modeling and simulation methodology is demonstrated and verified by simulating practical forward-converter power supply circuits. EMI, circuit layout, and thermal issues are not covered in the dissertation because other special tools are more suitable to tackle these problems. Brute force simulation is used to detect design errors. It will show that by using proposed modeling and simulation methodology, the total CPU time is about 8 hours for 800 tests of a power supply system simulation

1.2.2 Dissertation outline

This dissertation consists of seven chapters.

Chapter 2 proposes a test procedure to implement the virtual prototype test. Current available simulation approaches and their limitations are discussed, and then a modeling and simulation methodology is proposed to provide accurate system behaviors with minimized computational time. The methodology to fulfill the test procedure of the virtual prototype test is discussed in four parts: system partitioning, multi-level modeling, hierarchical test sequence and multi-level simulation. Among the four parts of the methodology, multi-level modeling and multi-level simulation are the two most important parts that are discussed further in later chapters.

Chapter 3 discusses the multi-level modeling approach and key issues in deriving models of a virtual prototype. How to derive models with different model levels is one of the most important issues in a virtual prototype test. An inadequate model will degrade the simulation speed and the accuracy of the system, which are two criteria of the virtual prototype test.

There have been many efforts in developing models for virtual prototype tests. Chapter 3 uses numerous examples to illustrate the modeling approach and contains a full list of the models that have been developed in a power supply system simulation. The purpose of these models is not to ask people to copy the same models exactly, but to provide a reference and a guideline, so people can derive their own models according to different applications, circuits, tests, and interests of circuit behavior.

Chapter 4 demonstrates the multi-level simulation methodology by running the whole virtual prototype test process in several forward-converter power supply systems. The power supply system consists of a forward converter as the main power supply with an over-voltage protect, an over-current protect, an under-voltage detector, and a bias power supply providing all the power for control and protection circuits. The simulation results are compared with measurements to verify the accuracy of the proposed approach. It shows that a virtual prototype test can replace actual prototype tests in simulation by running through all operating points. It also discussed design errors found in the virtual prototype test and how to fix these in simulation.

Some of the design errors cannot be fixed straightforwardly. Chapter 5 demonstrates how the virtual prototype can help debug the problems in the circuit and analyze the circuit when the circuit operation is hard to predict (e.g. due to parasitic parameters of circuit or during dynamic transient). The analysis in this chapter includes dc analysis with parasitic parameters of the circuit and large-signal transient analysis in the forward converter with active-clamp-reset circuits.

Chapter 6 further demonstrates how the virtual prototype can provide the circuit information needed in a design process. A design optimization procedure is provided by creating design curves through virtual prototype simulation in a forward converter with an active-clamp-reset circuit.

Chapter 7 is a summary of the proposed modeling and simulation methodology of the virtual prototype test. Future work is also discussed in this chapter.

2. VIRTUAL PROTOTYPE -- MODELING AND SIMULATION METHODOLOGY

2.1 Review of previous simulation approaches

2.1.1 Schematic-based simulation tools available for power electronics circuits

The development of design automation tools for power electronic circuit analysis and design application has been discussed for more than a decade [1-6]. A number of fundamental methods have been proposed for this purpose. However, progress in developing suitable techniques and tools in power electronics circuits has been much slower than that in the digital and analog IC design area [7]. The non-linearity of the power electronics circuit makes it more difficult to realize the design automation. Among many simulation engines, there are two main development directions for a power electronic simulation: SPICE-like simulation and piecewise linear based simulation. The main work in terms of SPICE-like simulation is to develop accurate large-signal power semiconductor models; in contrast, the piecewise linear based simulation mainly uses ideal switches and a linear algorithm to accelerate the simulation speed.

2.1.1.1 SPICE-like simulation tools

The SPICE-like simulation uses the modified nodal analysis approach [25]. A variable time step integration method is used to solve the circuit equations. The major commercial simulation engines for SPICE-like simulation are SPICE [26] and SABER [87].

The SPICE simulation engine is very popular for general circuit analysis. The major advantages of SPICE-like simulation include the full support of a device library, the capability to describe the relationship between node voltages and branch by nonlinear equations. These advantages make it capable of modeling detailed device characteristics and simulating detailed waveforms. One example of the application is loss analysis and stress calculation [27-29].

However, the necessity of simulation through the details of a switching transition requires small simulation time steps to ensure sufficient numerical accuracy; this translates to long simulation times when analyzing circuit behavior over hundreds or thousands of switching cycles. For example, it is usually time-consuming to reach the steady state of a power converter circuit due to the low frequency characteristics of the output filter. The other disadvantage is that the iterative solution routines used in a SPICE-like simulation engine are most likely to run into convergence problems at the switching points, especially at a large-transient simulation, such as during circuit start-up or at abnormal conditions. It is not suitable to select SPICE-like simulation engines for virtual prototype implementation.

2.1.1.2 Piecewise linear simulation tools

Piecewise-linear-based simulation uses the state variable approach, which is developed especially for switching circuit applications [76]. The major commercial software is SIMPLIS [88].

This approach formulates a set of circuit equations in terms of state variables, which normally are voltages across capacitors and currents through inductors. With the state variable formulation, the switching converter is represented by linear sets of state equations, with one set for each operating mode. Since the set of state equations during one operating mode is linear and time-invariant, it can be solved using linear algebra instead of non-linear integration. For piecewise-linear-based simulation tools, fewer convergence problems occur in the simulation, and the simulation speed is ten to hundred times faster than SPICE-like tools for a long time simulation of a switching circuit [7-12].

In recent years, many nice features have been implemented in SIMPLIS, such as the Periodic Operating Point (POP) analysis and the automated small-signal frequency-domain analyzer. The POP analysis uses a special algorithm to accelerate convergence to the steady-state for a periodic-operation system, so the circuit can reach the steady state faster than a brute force simulation [39]. The automated small-signal frequency-domain analyzer performs the frequency analysis via a time-domain simulation, so there is no need to derive the small signal models [38]. These features make SIMPLIS a good candidate for the virtual prototype test.

However, the piecewise-linear-based simulation engines are developed mainly for simulation using ideal models instead of detail models. There is a limitation to implement control algorithms with nonlinear equations or to derive device models with nonlinear characteristics in this kind of simulation engine. The models in the simulation tool and the capability to derive models are limited compared with SPICE and SABER. Since most of the current applications are for simple design verification, less effort has been made to improve models for more accurate results.

2.1.2 Simulation approaches to reduce simulation time

Based on these simulation engines, several simulation approaches, such as the state-space averaging model simulation approach and the hierarchical simulation approach are developed to accelerate simulation speed and system accuracy.

2.1.2.1 Average model simulation

The average modeling approach was proposed by Middlebrook and Cuk [15-16]. It is based on a state-averaging concept and therefore known as the state-space averaging technique. This approach converts a nonlinear, time-varying, switched circuit into a continuous linear, time-invariant equivalent circuit by averaging state variables during one cycle. An extension of this technique is presented in many papers [17-24]. This method is very useful for the small-signal analysis of a dc/dc converter, and large signal transient analysis. The simulation speed is superior since no switching action is involved. The major disadvantage is that extra effort is needed to derive the average models. The average model simulation is only suitable for some applications, such as circuit operation analysis and small-signal frequency analysis in a SPICE-based simulation engine. It is not suitable for a virtual prototype test since it cannot represent the real system and loses a lot of circuit behaviors related to switching actions, such as transformer reset, device stress, and over-voltage response.

2.1.2.2 Hierarchical simulation

From the above discussion, we know that simulation time can be prohibitively long when hundreds of tests of a complex power supply system are required to complete the virtual prototype test, so it is unrealistic to run all the tests by using SPICE-like simulation. At the same time, simulations using a simplified circuit diagram, an average model, or a simple model in SIMPLIS cannot detect many real-life design errors that take up most of the design cost and time.

In recent years, many studies have discussed these issues and proposed a "hierarchical" or "multilevel" simulation approach [30-34]. This approach combines different tools (e.g. SPICE and SIMPLIS) and different techniques (e.g. large signal model and average model) to analyze the circuit at the various levels of interest. This approach can take advantage of different tools and techniques efficiently and make the simulation very powerful. One of the disadvantages in this approach is that it cannot support all the tools and techniques within one simulation environment. Designers need more efforts to draw the schematics and adjust simulation results in different simulation engines because of the incompatibility of the software tools.

2.2 Concept of virtual prototype DVT

2.2.1 Selection of simulation engine for virtual prototype DVT

The virtual prototype DVT should be implemented in a single simulation engine capable of fast simulation speed and accuracy. The simulation engine is selected first before developing the test procedure for a virtual prototype test. From the previous discussion, we know that although no simulation engine is available for this purpose, the SIMPLIS simulation engine is the best candidate among commercial simulation tools because:

- The simulation speed of SIMPLIS is ten to one hundred times faster than SPICE-like simulation engines for a long-term simulation. There are also fewer convergence problems in a SIMPLIS simulation.

- Most of the simulations in a virtual prototype test need to reach a steady state first before the final test (e.g. load regulation, loss analysis, transient analysis). SIMPLIS uses a special algorithm to find the steady state of a periodic operation circuit, so it further reduces the simulation CPU time from a brute force simulation.

- SIMPLIS can perform the frequency analysis through a time domain simulation. No small-signal model needs to be derived in the whole test process.

A major disadvantage of SIMPLIS is that it uses ideal switches in the simulation, so the detailed waveform during switching transition is ignored. In paper [35], a piecewise linear model for the MOSFET is derived to predict successfully the switching losses in a power supply circuit. It shows that a more accurate simulation is possible with a more complex SIMPLIS model. Since many design errors in a real power supply system cannot be detected by using simple models, many efforts are needed to enhance the characteristics of SIMPLIS models for virtual prototype test purposes. How to implement SIMPLIS models will be discussed in the next chapter. A single simulation engine, SIMPLIS, and a UNIX workstation SPARC 20 are used for the simulation tests in the dissertation.

2.2.2 Improving simulation speed and accuracy via multi-level modeling and simulation approach

In order to detect most of the design errors before the first prototyping, the models used in a simulation should include major characteristics to present the important behavior of the circuit. However, by implementing detailed models in SIMPLIS, the simulation speed could be as slow as the one in a SPICE-like simulation engine. How to implement a multi-level complexity of the virtual prototype to manage the simulation with both interested system behavior and fast simulation time is the major issue in the test process.

2.2.2.1 Multi-level modeling and simulation concepts

First, we need to understand two terms used in the rest of the dissertation: simulation CPU time and simulation time. "Simulation CPU time" means the computational time needed in a simulation; and "simulation time" means the circuit-operating time that a user has defined in a simulation.

A diode with different levels of complexity is used as a simple example to illustrate the relationship between complexity, simulation speed, and the accuracy with which the simulation describes the actual system behavior. Fig. 2.1 shows four ways that the forward voltage and current characteristics of a diode could be modeled, with a detailed physical model, a two-segment model, a three-segment model, and a three-segment with piecewise linear capacitor model.

Very often, the two-segment model is as good as other, more complex models since the diode on-to-off and off-to-on transition time is very short compared with the on time or the off time. When this is true, selecting a two-segment model can give the shortest simulation time without losing the simulation accuracy. A multi-segment model or physical device model may be needed when the device behavior during the transition time is an important factor in predicting the targeted aspect of circuit operation. The selection of the device model with the appropriate level of complexity will depend on the trade-off between the system behavior accuracy and the simulation speed.

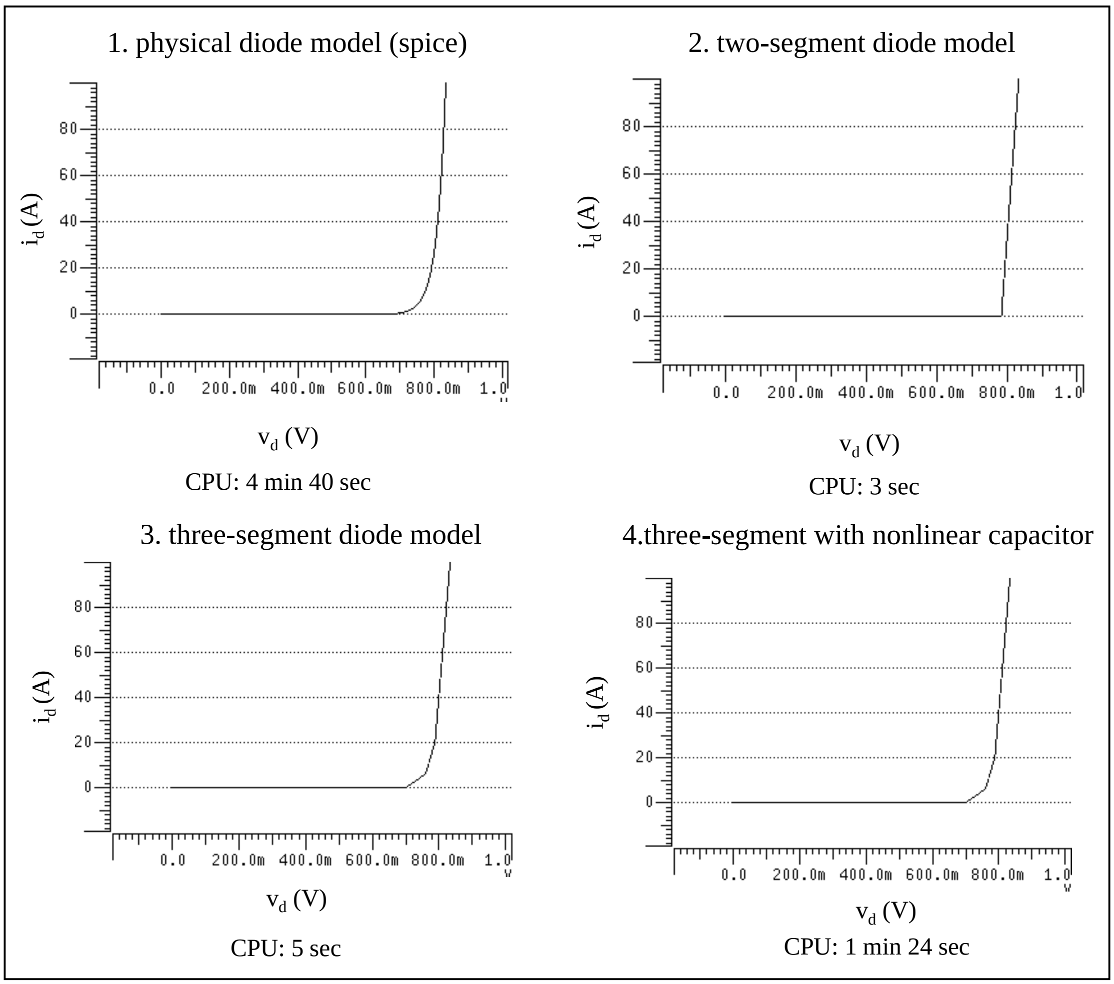


Fig. 2.1 Diode forward voltage drop characteristics of different models: 1. physical diode model. 2. two-segment diode model. 3. three-segment diode model. 4.three-segment model with nonlinear capacitor.

A simple test circuit shown in Fig. 2.2 is used to test the simulation speed and system behavior accuracy with different levels of complexity in the diode model. The initial voltage of the output capacitor is zero. Fig. 2.3 shows the output voltage waveforms, and Fig. 2.4 shows the voltage and current of the freewheeling diode. V_{o1} is the output voltage for a physical diode model; V_{o2}, V_{d2}, and I_{d2} are for the two-segment model; V_{o3}, V_{d3}, and I_{d3} are for the three-segment model; and V_{o4}, V_{d4}, and I_{d4} are for the three-segment model with a piecewise linear capacitor.

The CPU times of the simulation are 4 minutes 40 seconds for the physical device model using SPICE PLUS, 3 seconds for the two-segment model using SIMPLIS, 5 seconds for the three-segment model, and 1 min 24 seconds for the nonlinear capacitor model using SIMPLIS. The simulation waveforms are very close for different complexity diodes in steady state waveforms, and the simulation with the physical diode model takes a longer CPU time because of the complexity of the model and the different mathematical approach of the simulation engine.

As shown in the figure, during transient analysis a simple two-segment diode model may not present the peak voltage value of the output voltage accurately because it cannot present the nonlinear characteristics of a forward voltage drop during the whole load range. Whether a three-segment diode model is needed in this condition depends on the requirements of the simulation. When the discharging of the charge storage of the diode needs to be considered (e.g. in loss analysis and snubber design), a three-segment model with a nonlinear capacitor to present the charge stored in the diode is needed. A diode with multi-level modeling can provide the opportunity to reduce the circuit complexity in a simulation, consequently to minimize the simulation CPU time.

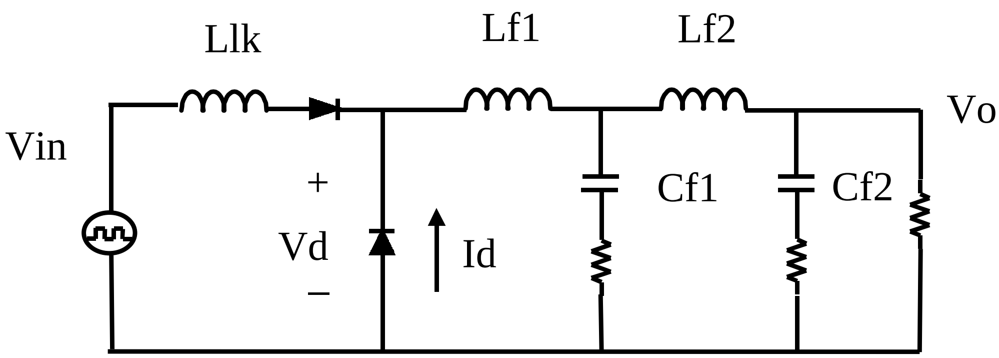


Fig. 2.2 Simple test circuit diagram.

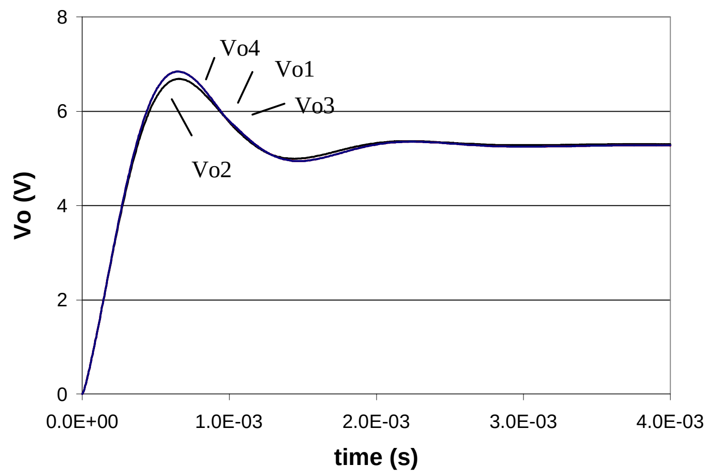
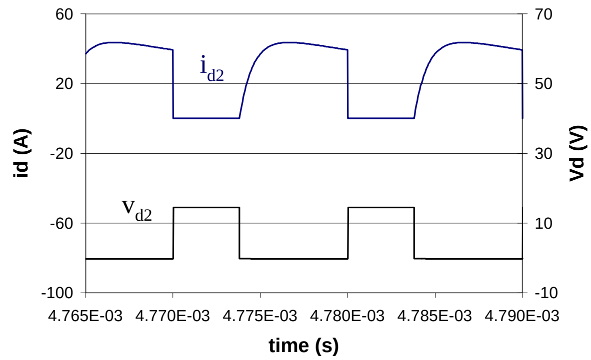
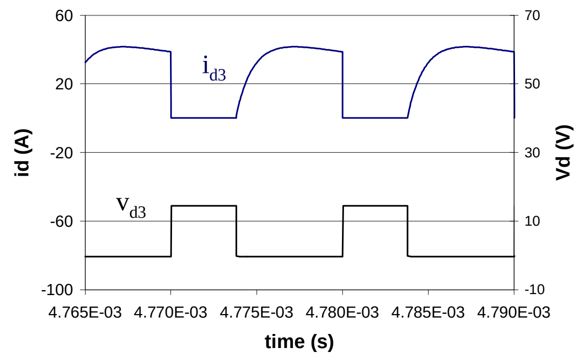


Fig. 2.3 Circuit output voltage waveform comparison between different diode models.

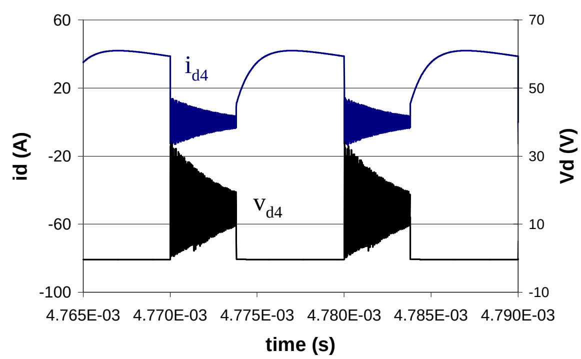
V_{o1} : Output voltage using a physical diode model with SPICE PLUS.
V_{o2}: Output voltage using a two-segment diode model with SIMPLIS
V_{o3}: Output voltage using a three-segment diode model with SIMPLIS
V_{o4}: Output voltage using a three-segment with nonlinear capacitor diode model with SIMPLIS



(a)



(b)



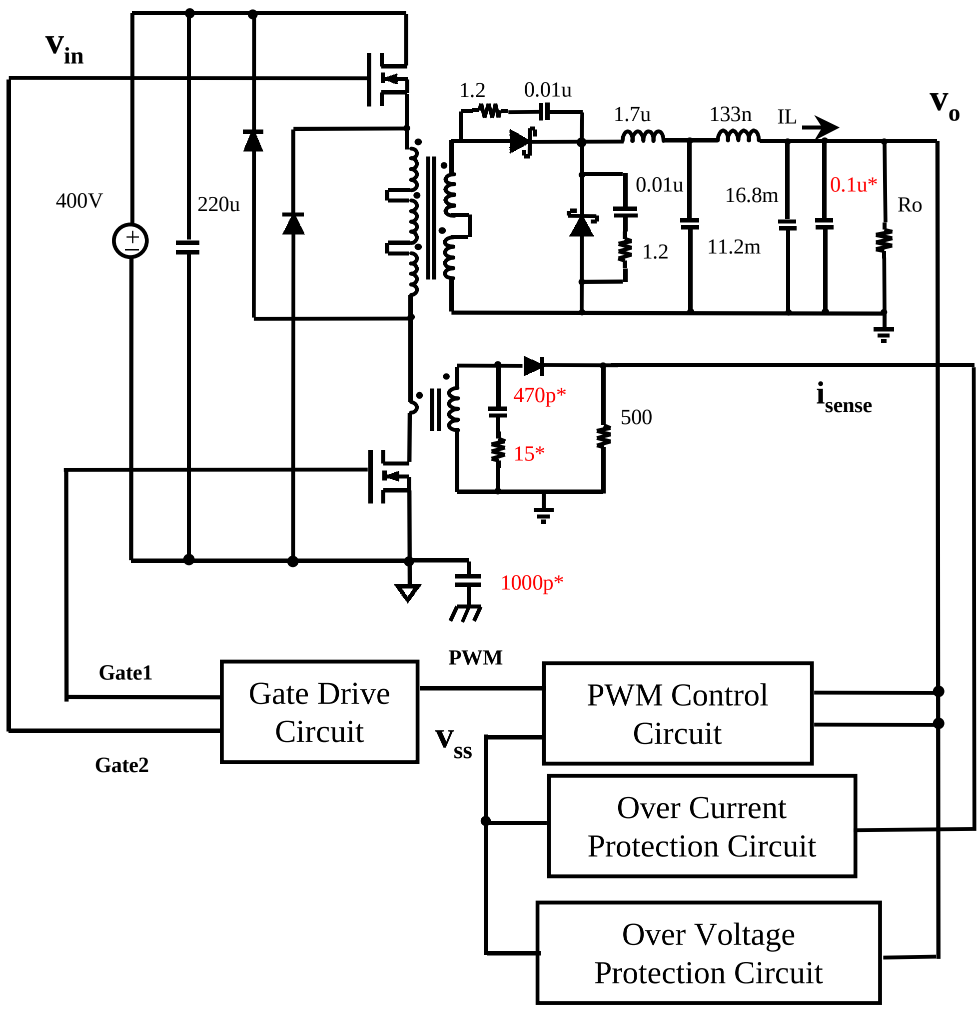
(c)

Fig. 2.4 Circuit diode voltage and current waveforms comparison between different diode models. (a) diode forward-voltage and current with two-segment diode model at steady state. (b) diode forward-voltage and current with three-segment diode model at steady state. (c) diode forward-voltage and current by using three-segment with nonlinear capacitor diode model at steady state.

2.2.2.2 Multi-level modeling of power supply system

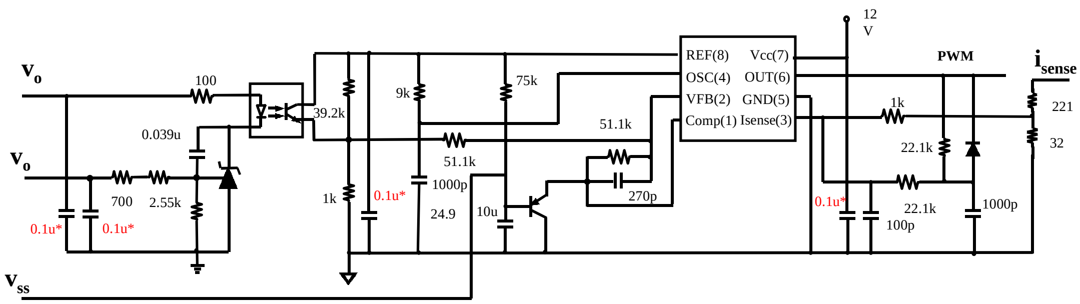
From the previous section, we see that a simpler diode model can reduce the complexity of the circuit schematics in simulation. Actually, there are more approaches to reduce the complexity of a system. A 5 V two-transistor forward converter subsystem shown in Fig. 2.5 is used as an example to show how a different complexity of the circuit affects the simulation speed. The 5 V converter subsystem includes the main power stage, PWM control, gate drive, over-voltage protection, and over-current protection circuits. The components highlighted with an asterisk on values are high frequency noise suppression components.

The 5 V converter subsystem is used to investigate the simulation CPU time for 100 virtual prototype tests. Since, in virtual prototype tests, some tests require more simulation time (e.g. large-signal transient), and some require less simulation time (e.g. loss analysis), for simplicity, we assume that there are 90 long-term tests and 10 short-term tests for 100 tests. Each long-term test needs 5 ms simulation time, and each short-term test needs 100 us simulation time.

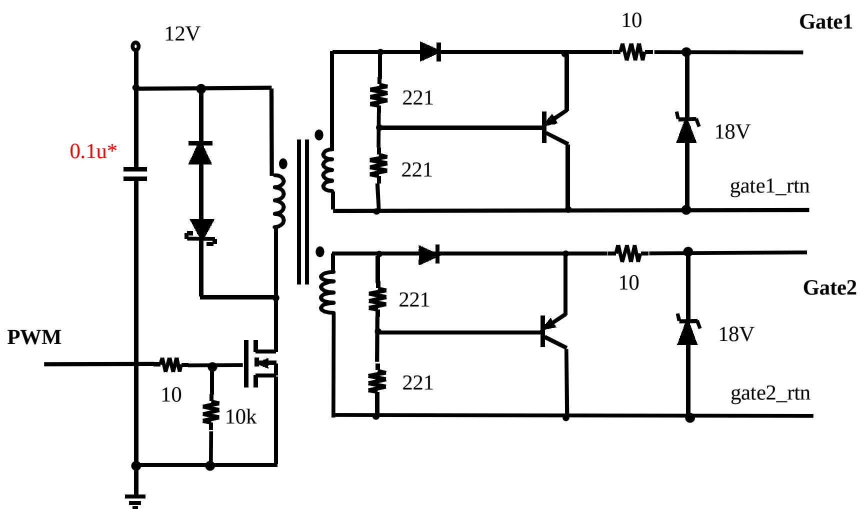


(a) 5 V two-transistor forward converter subsystem

Fig. 2.5. Two-transistor forward converter subsystem circuit

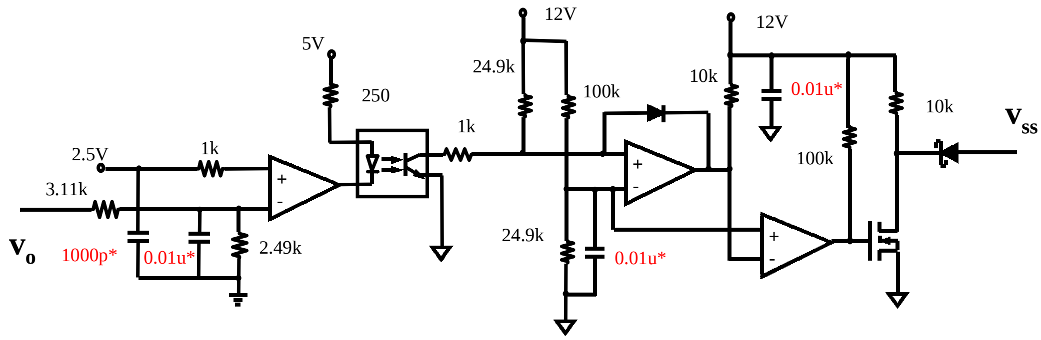


(b) Peak current mode PWM control circuit

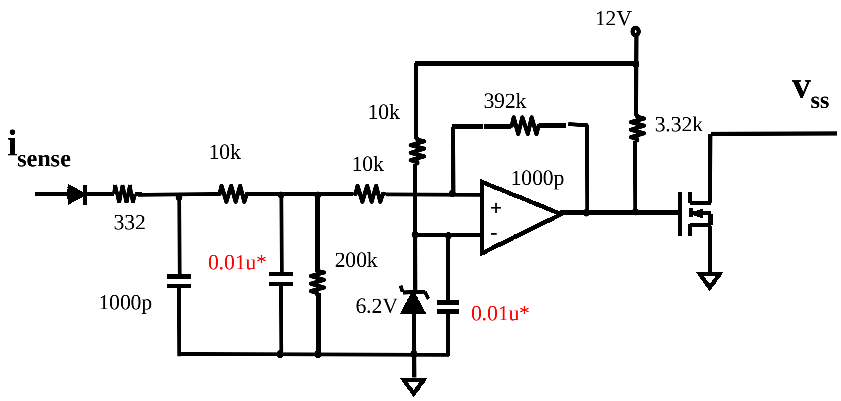


(c) Gate drive circuit

Fig. 2.5. Two-transistor forward converter subsystem circuit (continued).



(d) Over-voltage protection circuit



(e) Over-current protection circuit

Fig. 2.5. Two-transistor forward converter subsystem circuit (continued).

Table 2.1 compares the simulation CPU time with a different system complexity of the 5 V converter subsystem. The complexity of the circuit is reduced from the original schematics by reducing the number of the blocks used in the simulation, changing MOSFET and the gate drive block model complexity, and eliminating high frequency components. Two gate drive block models used in comparison are shown in Fig. 2.6: the simple gate drive block model provides the isolation function of the transformer and the resistance of the gate, and the detail model has detailed circuit schematics. The two MOSFET models used are shown in Fig. 2.7: an ideal switch model and a complex switch model. The complex MOSFET model describes the device behavior in the active region as discussed in [35], while the simple MOSFET model uses an ideal switch with on and off resistance.

From Table 2.1, we can see that for a full production schematic with complex models for gate drive block and MOSFET, the estimated simulation CPU time for 100 tests is more than 25 hours. The actual virtual prototype test could have more than 1000 tests, as we will discuss later, so it will take more than 10 days to complete the whole simulation process which is not practically acceptable. From the data, we see that, although SIMPLIS is very fast for a simplified schematic with simple models, it is necessary to develop simulation methodology to accelerate the simulation speed for a full production schematic in the virtual prototype test.

By reviewing the product schematics, we can see that some high frequency noise suppression components, such as those highlighted with an asterisk (e.g. the high frequency capacitors connected to the power supply of controller chip), exist only to suppress unwanted side effects of high frequency parasitic components. Many of these parasitic components will never appear in the simulation, given our current ability to model and predict their magnitudes. Therefore, in many cases the high frequency noise suppression components may be removed from the production schematic before we send it to the simulation without compromising the simulation accuracy. As shown by comparing rows one and two, eliminating those noise suppression components can speed up the simulation greatly (by more than half in this example).

Table 2.1 Comparison of simulation CPU time of 5 V converter subsystem with different circuit complexity.

Simulation Conditions	CPU with 100 μs simulation time	CPU with 5 ms simulation time	CPU with 100 tests *
Full schematic	4 min 37 sec	16 min 24 sec	25.4 hours
Simplification -- modifying schematic	1 min 48 sec	6 min 36 sec	10.2 hours
Further simplification - eliminating OV and OC protection circuits	44 sec	5 min 32 sec	8.5 hours
Further simplification - using simple gate drive and complex MOSFET	24 sec	3 min 26 sec	1.8 hours **
Further simplification - using simple gate drive and MOSFET	8 sec	1 min 8 sec	

* Assuming 90 long-term tests and 10 short-term tests for 100 virtual prototype tests. Each long-term test needs 5 ms simulation time, and each short-term test needs 100 us simulation time.

** Short-term simulations use the model of row 4, long term simulations use the model of row 5.

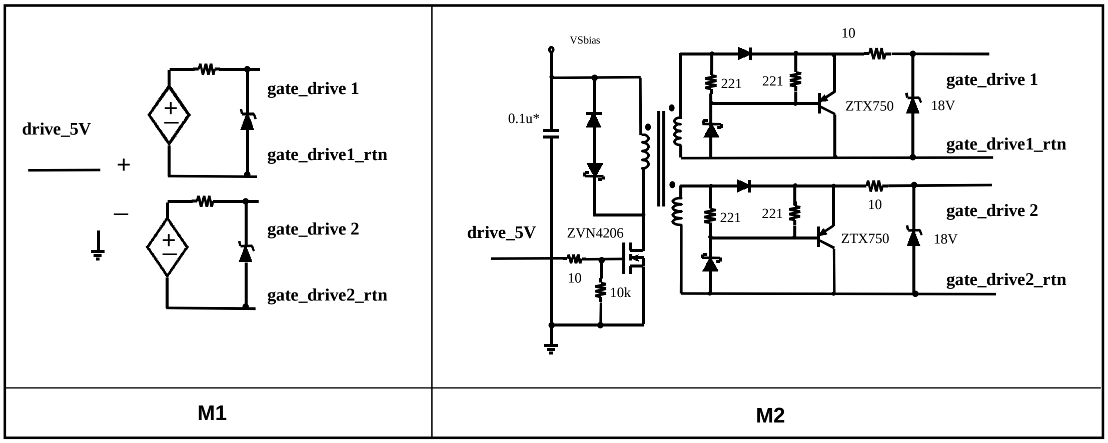


Fig. 2.6. Example of simple gate drive model (M1) and complex gate drive model (M2).

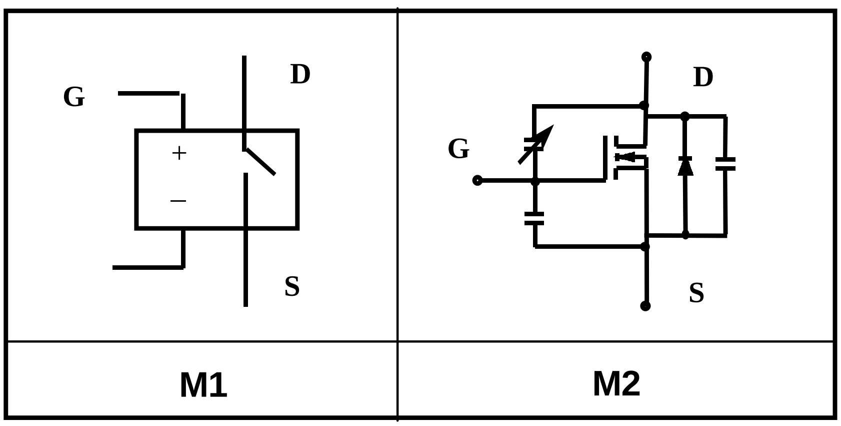


Fig. 2.7. Example of simple gate MOSFET model (M1) and complex MOSFET model (M2).

Row three of Table 2.1 shows a simplification that can be made by eliminating over voltage and over current protection circuits when these two circuits are not involved in simulation (e.g. loss analysis, voltage regulation).

Row four further simplifies the circuit by using a simplified gate drive model shown in Fig. 2.6. It shows that when a detailed gate drive circuit is not necessary, a simplified gate drive circuit can reduce about half of the simulation CPU time.

Row five uses a simplified gate drive in Fig. 2.6 and a simplified MOSFET model in Fig. 2.7. This combination can be used in most of the simulation (e.g. load regulation, large-signal transient), and it reduces the simulation CPU time significantly.

In a virtual prototype test, a complex MOSFET model can be used for loss analysis, which only requires a short term simulation, while most simulations can use a simplified switch model which requires a long term simulation. Row four of Table 2.1 shows the simulation CPU time for 100 tests is 1.8 hours according to this combination.

Table 2.1 shows that the simulation CPU time can vary by more than an order of magnitude depending on the complexity of the models and blocks. It is worthwhile to use simpler models and fewer blocks in a simulation as long as the result is adequate. By judicious selection of model levels, the computational time can be reduced significantly without losing the accuracy of the interested system behavior.

The multilevel modeling and simulation approach is proposed in this chapter, which focuses on selecting the appropriate level of device model complexity (e.g. diode model level) and block complexity (e.g. gate drive block level) for each specific objective. Therefore, the shortest simulation CPU time can be achieved while still accurately simulating the system's behavior.

2.2.3 Overview of proposed simulation methodology and virtual prototype DVT procedure

By using a multilevel modeling and simulation approach, it is possible to develop a simulation approach for a virtual prototype test, such that

- Simulation schematics can be simplified dynamically by taking out or simplifying part of the system, which is not involved in a particular test.
- Simulation is capable of providing different level of details according to the designer's interest by using a different complexity of models.

The proposed virtual prototype DVT procedure is shown in Fig. 2.8. After initial conceptual design, a production schematic is generated. Then the designer identifies the major functions in the circuit (e.g. power stage, over voltage protection) and partitions schematics into function blocks. The process to partition the system into blocks is called system partitioning.

After system partitioning, there are two parallel steps: implementing models and generating a test sequence for the virtual prototype test. The device models are derived first, then the function block models. Since most of the models are implemented with multiple complexity levels, the process to implement models is called multi-level modeling device and function block.

At the same time, a test sequence is generated according to defined function blocks and tests which need to be covered. The test sequence starts from individual block tests and ends with the system interaction tests. This approach is called a hierarchical test sequence.

The last step before a system simulation is to determine the levels of each model used in the simulation and the complexity of the simulation schematics, so the simulation CPU time is minimized. The methodology in this process is called multi-level system simulation.

In the meanwhile, each error detected in the test process will go through the design modification process via design, verification, and testing iterations.

So, there are four major parts of simulation methodology in the virtual prototype test procedure as shown in Fig. 2.8. The methodology which needs to be developed is shown in the shaded area. It consists of four parts: system partitioning, multi-level modeling device/function block, hierarchical test sequence, and multi-level system simulation.

In the procedure, how to define models (multi-level modeling), when to use which model (multi-level simulation), and how to complete the whole virtual prototype test systematically (hierarchical test sequence) are the essential issues in the development of simulation methodology.

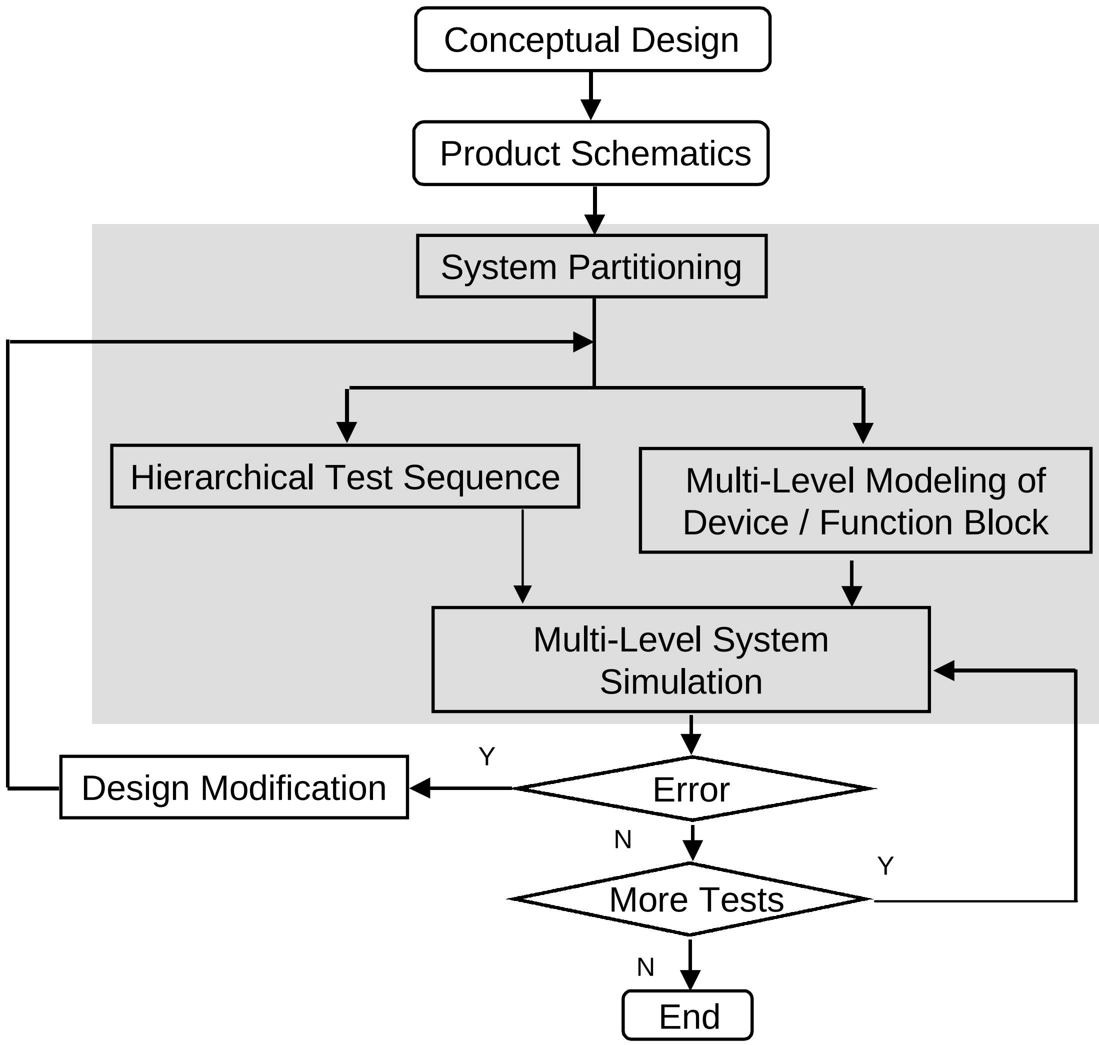


Fig. 2.8. Proposed virtual prototype DVT procedure. The simulation methodology is shown in the shaded area, it includes four parts: system partitioning, multi-level modeling of device and function block, hierarchical test sequence, and multi-level system simulation.

2.3 Development of virtual prototype DVT

A 5 V forward converter power supply system is used as an example to demonstrate how to implement the virtual prototype test. The circuit schematic of a 5 V forward converter power supply is shown in Fig. 2.9.

2.3.1 System partitioning

The 5 V power supply system in Fig. 2.9 includes a main power supply with 5 V output and a bias power supply with two 12 V outputs to provide the primary and secondary bias voltages needed in the circuit operation. From the circuit schematics we know that it is not effective to simulate the whole power system in simulation since it is too time consuming and most of the tests only involve part of the system. It is desirable to partition the circuit schematics into small function blocks, so a new simplified schematic can be generated dynamically for each test. The circuit partitioning consists of four steps: identifying function blocks, defining blocks, partitioning schematics, and simplifying blocks.

2.3.1.1 Functions

The first step is to identify system functions. The 5 V power supply system in Fig. 2.9 includes a main power supply and a bias power supply. The main power supply includes power stage, control, gate drive, over-voltage, under-voltage, and over-current circuits, and the bias power supply includes a bias enable circuit and a bias power supply circuit which provides all the internal power supplies of the main power supply. Besides the basic power convention function in the main converter, the two-transistor forward converter also includes a transformer-reset circuit, and a snubber circuit. The PWM control circuit includes a start-up circuit.

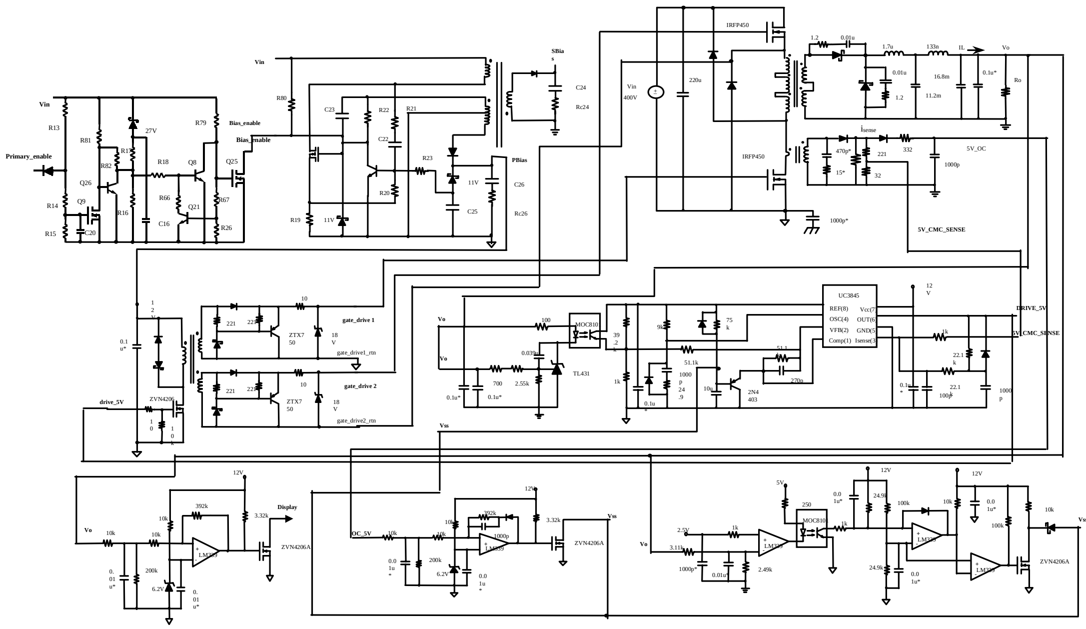


Fig. 2.9 Schematic of a 5V forward converter power supply system. It includes a main power supply (two-transistor forward converter) with 5 V output and a bias power supply (flyback converter) with two 12 V outputs to provide the primary and secondary bias voltages needed in the circuit operation

2.3.1.2 Blocks

How many blocks should we define in the schematic? A block is the smallest unit of the circuit on which we can do a single function test. More blocks mean more different complexity levels of the system, so we have more chance to reduce the simulation CPU time in a single test. For example, the main power converter can be defined as three blocks: power stage, gate drive, and PWM control circuit. This makes the simulation more effective: gate drive can be simplified to a simple model to reduce simulation CPU time significantly as we have shown in the previous section; the control circuit could be replaced by a fix duty cycle circuit in loss analysis, etc.

If there are too many blocks defined, it will increase the complexity of the test procedure when defining multi-level simulation, which we will discuss later. There is no absolute way to define blocks in system schematics. As a rule of thumb, if two blocks are always included in the same tests, or if keeping these two blocks together has no significant difference in simulation CPU time, these two blocks can be defined as one block instead of two. For example, in most of the applications, there is no need to define the main power stage to more blocks, such as primary and secondary blocks.

One way to define the blocks in a 5 V converter power supply system is shown in Fig. 2.10. The blocks include: power stage, PWM control, gate drive, over voltage protection, over current protection, under voltage detector, bias circuit, and bias enable blocks.

2.3.1.3 Schematic partitioning

After defining blocks, the whole schematic can be partitioned into small block schematics. If a SIMPLIS concept schematics interface is used, each partitioned block schematic can be defined as a hierarchical model (i.e. a high level sub-circuit). The other way to do it in automated simulation is to define each component a block property (e.g. the components in a gate drive circuit have gate drive block properties), so a component can be extracted in a particular simulation according to block properties.

The partitioned schematic of the 5 V power supply system is shown in Fig. 2.10. In the dissertation, the simulation schematic will be presented as a block diagram as shown in Fig. 2.11. The interactions among blocks can be seen in the partitioned block diagram.

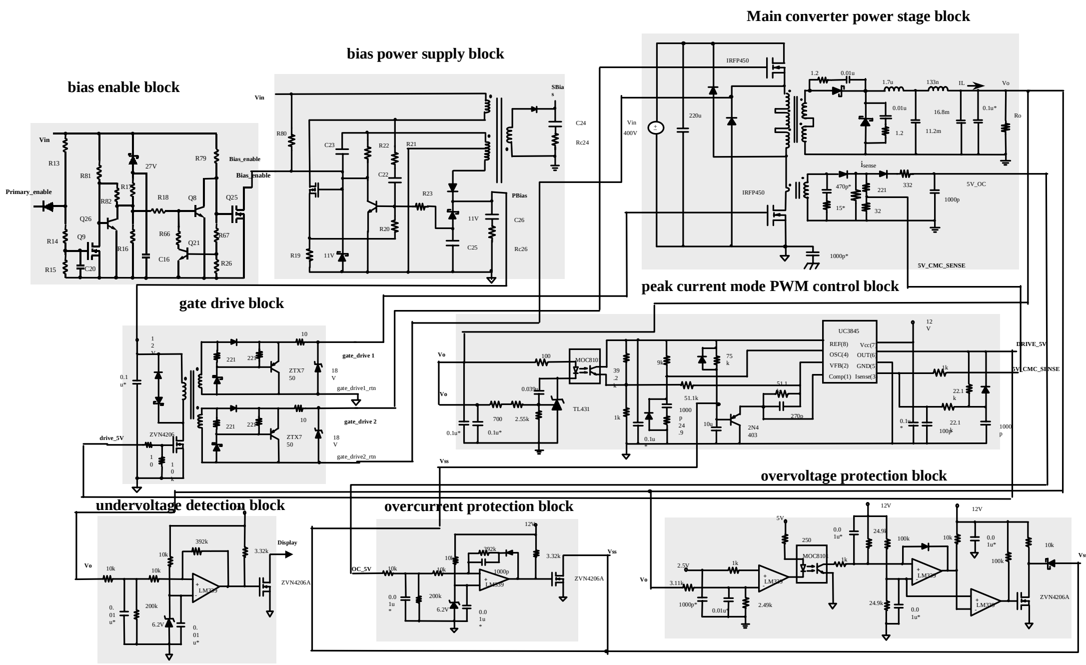


Fig. 2.10 Identify major function blocks in a 5V forward converter power supply system. The main power supply includes power stage, control, gate drive, over-voltage, under-voltage, and over-current circuits, and the bias power supply includes a bias enable circuit and a bias power supply circuit.

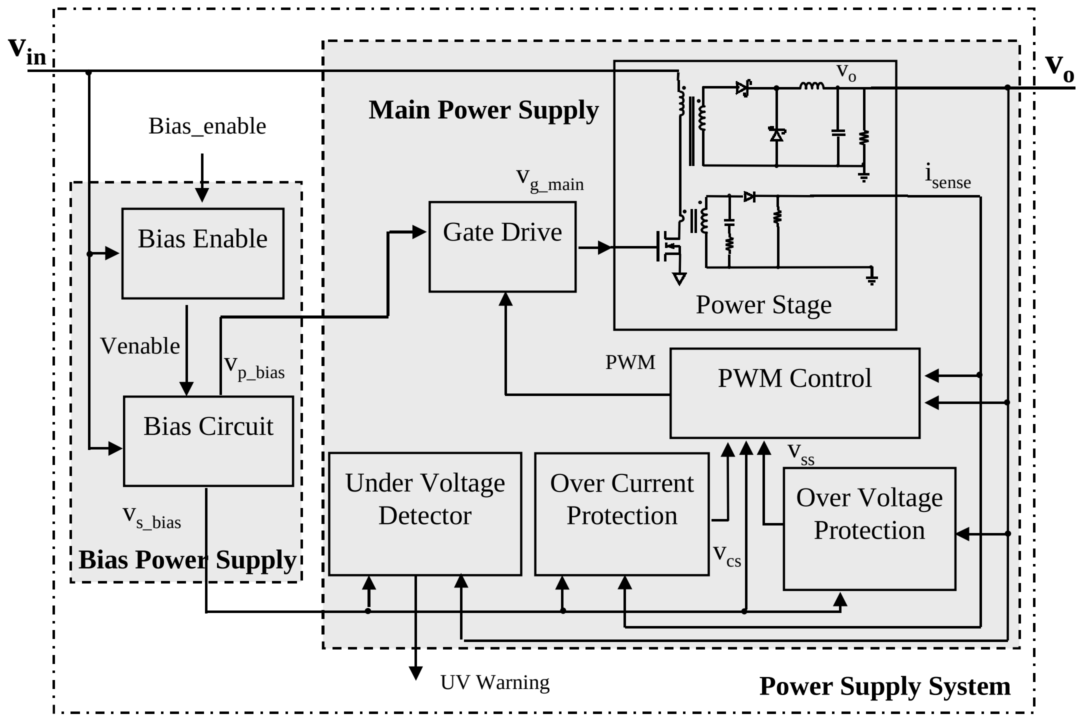


Fig. 2.11. System block diagram of the 5V forward converter power supply system.

2.3.1.4 Block simplification

The simulation speed of SIMPLIS is determined mainly by two factors: the number of L, C, and nonlinear segments, and the smallest time constant, which determines the time, step in each topology (RC, RL). It is important to refine each block schematic before the virtual prototype test in order to avoid unnecessarily reduced simulation speed. The refine block procedure covers two steps:

1. Eliminate the high frequency noise suppression components, such as those highlighted with an asterisk in Fig. 2.5. As we discussed in 2.2.2.1, these components do not provide system behavior interested in tests and usually

have small time-constants, so eliminating these components can accelerate the simulation speed significantly.

2. Reduce L, C, and switches by combining paralleled capacitors, in series inductors, and paralleled switches (MOSFETs, diodes, etc.). This can reduce the number of state variables and the maximum number of possible topologies in the simulation, so as to accelerate the simulation speed.

2.3.2 Multi-level modeling

2.3.2.1 Multilevel modeling of components

There are three types of components in the circuit: passive components, semiconductor devices, and IC chips. The main passive components are: capacitor, inductor, and transformer; the main semiconductor devices are: diode, MOSFET, and bipolar transistor; the IC chips are: comparator, operational amplifier, optical coupler, gate driver, and so forth.

From the previous section 2.2.2.1, we know that a simple piecewise linear model such as the two-segment model can be sufficient most of the time, and a more precise device model such as the diode model with storage charge characteristics can be used if the test requires more accurate system behavior. More diode models may needed in other applications. For example, the off character of a diode (leakage current) is an important character in mag-amp circuits [45], so a diode model with more accurate leakage current characteristics may be needed for that particular application. The total number of model levels needed in each device depends on different applications.

Fig. 2.12 shows the diode models used for testing the 5 V forward converter system shown in Fig. 2.11. A two-segment model and a two-segment with piecewise linear charge capacitor model are suggested. Application examples for the multi-level diode model are summarized in Table 2.2. The selection of other device models follows the same principles illustrated in this example. Fig. 2.13 is an example to show the number of model levels for each component needed in a virtual prototype test of the power supply system shown in Fig. 2.11. The detail about modeling of these components is discussed in the next chapter.

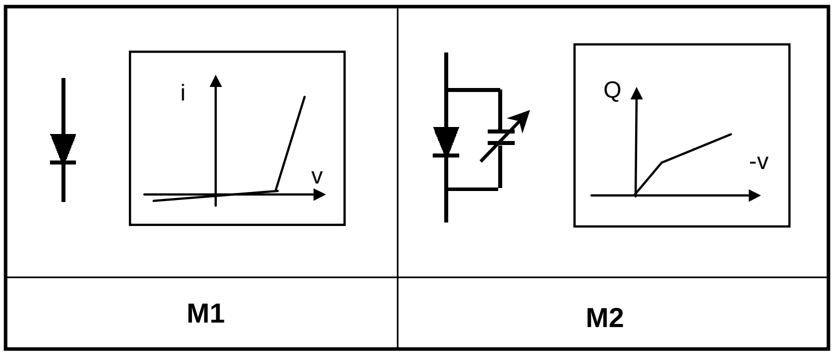


Fig. 2.12. Multi-level models of diode. M1: a two-segment model. M2: a two-segment diode with piecewise linear charge capacitor.

Table 2.2. Application examples of multi-level models of diode.

Model level	Description	Major characteristics	Application example
M1	Two-segment	Basic function: diode on and off characteristics	Steady state analysis
M2	Two-segment with nonlinear capacitor	M1 + Charge storage (on and off transient)	Loss analysis, snubber design

Passive component

name	capacitor	inductor	transformer
total model levels	3	2	4

Semiconductor device

name	diode	MOSFET	bipolar transistor
total model levels	2	4	2

IC chip

name	op amp	comparator	optical coupler	voltage regulator	gate driver
total model levels	1	1	1	1	1

Fig. 2.13. Example of model levels of passive components, semiconductor devices, and IC chips needed in a virtual prototype test of the power supply system shown in Fig. 2.11.

2.3.2.2 Multilevel modeling of blocks

Fig. 2.15 is an example to show the number of model levels for each block needed in a virtual prototype test of the power supply system shown in Fig. 2.11. The detail of modeling of these blocks is discussed in the next chapter.

As an example, the gate drive models are shown in Fig. 2.14. In gate drive models, model level 1 (M1) presents the basic function of the gate drive, M2 has both gate drive and bias supply current, and M3 is a detailed model. Similar to block models, the total numbers of model levels needed in each block depends on different circuits and applications.

From Fig. 2.13, we see that all the IC chips only have one model level, and all the passive components and semiconductor devices are multilevel models. Since the main power stage block and the bias circuit block are main blocks that are composed of these passive components and semiconductor devices, the power stage block and bias circuit block are different to other blocks from the modeling aspect. It is worthwhile to mention that, unlike the gate drive block, the multiple models of power stage block and bias power supply block are determined by model levels of numerous components in the blocks. How to generate multilevel models of these blocks is more related to each specific test instead of a modeling aspect. This will be discussed later in the multi-level simulation section.

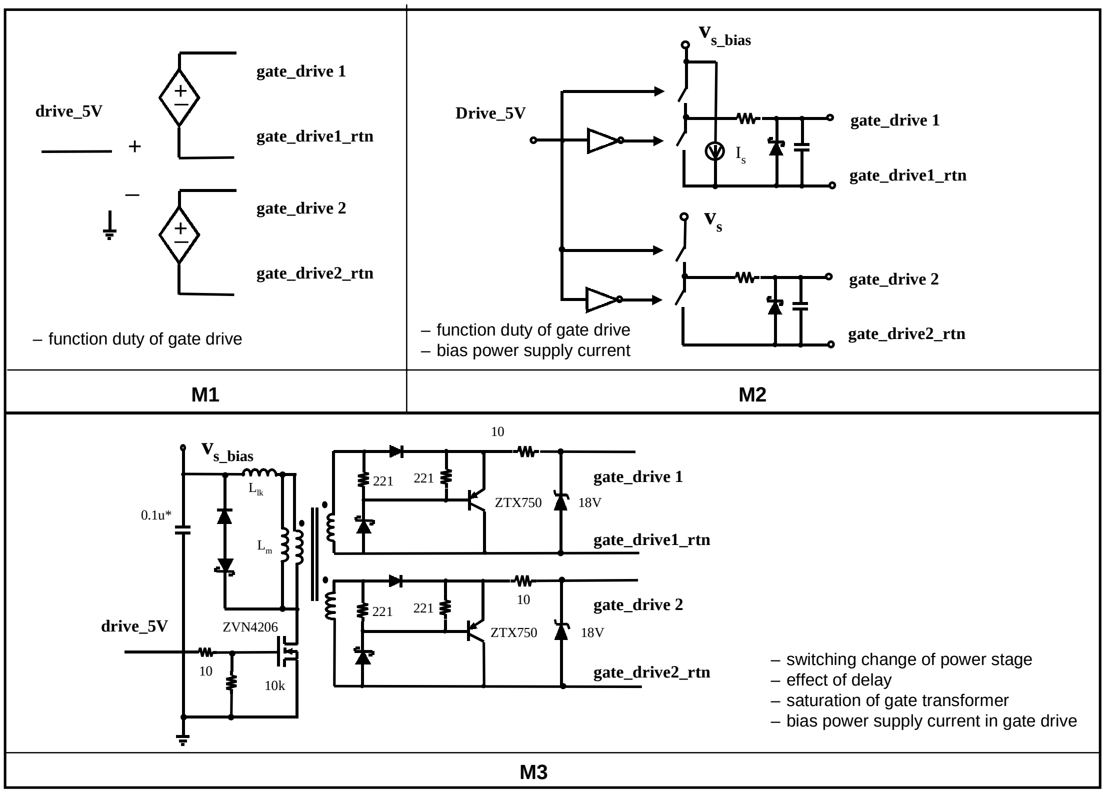


Fig. 2.14 Multi-level models of gate drive block. M1: the basic function of the gate drive. M2: gate drive function and bias supply current. M3: detailed schematic model.

block name	power stage	gate drive	pwm control	OC	OV	UV	bias enable	bias
total model levels	7	3	3	1	1	1	1	3

Fig. 2.15 Example of the model levels of blocks needed in a virtual prototype test in the power supply system shown in Fig. 2.11.

2.3.3 Hierarchical test sequence

Unlike in the hardware prototype DVT, most of the electrical tests are performed on the whole power supply module due to the integration of the prototype. The virtual prototype DVT can have a more thorough and completed test sets for several reasons:

- Simulation can take out or include any part of the schematic, adjust circuit parameters, change components, and change test conditions more conveniently.

- Simulation can monitor any node voltage and branch current in the circuit. For example, the magnetizing current of the main power transformer is an important variable for transformer design verification. It can be monitored easily in simulation while it is rarely measured in the hardware tests.

- Simulation can perform all the tests without damaging the real circuits. Many design errors will not be detected until the circuit burned out devices in the hardware test (e.g. exceeding device stresses, transformer saturation). In a virtual prototype test, no damage is involved and aggressive tests could be done to examine extreme conditions (e.g. in dynamic load transient test, a step load change will exam the circuit performance in an extremely case).

- More operating points can be examined in an automated simulation test system. Only several test points and limited tests are performed in the hardware tests since most of the electrical tests are done manually. In a virtual prototype test, it is possible to implement an automation test system, so it runs the system thoroughly by sweeping the whole operating range, and report errors through exported data analysis.

A hierarchical test sequence is proposed to run all the simulations in the virtual prototype DVT systematically. The proposed test sequence starts from function block tests that involve small circuit units (block) to system interaction tests that involve the whole system. The objective is to verify ultimately the circuit design in a small simulation schematic (e.g. single block test) first, so the simulation with long-term and large simulation schematics can be minimized to reduce simulation CPU time. Fig. 2.16 is an example of the proposed virtual prototype test sequence for the 5 V power supply system shown in Fig. 2.11. The whole test procedure includes six levels of tests: a basic function test, a steady state test, a small-signal stability test, a large-signal transient test, a subsystem interaction test, and a system interaction test. The shaded areas indicate the test sequence, and the first two rows indicate the system structure. In order to make the example more general, the over-voltage protection and over-current protection circuits in Fig. 2.11 are categorized as protection blocks and the under-voltage detect circuit is categorized as a monitoring block.

2.3.3.1 Level 1 -- basic function test

The level 1 test is to verify the basic function of each individual block without considering its interaction with other blocks.

Gate drive test: duty cycle transfer function, transformer saturation, bias current range, and time delay of duty cycle signal.

Power stage test: basic converter function, transformer reset circuit function.

Control circuit test: normal operation of control circuit, output voltage regulation, start-up function, minimum and maximum duty cycle of the control circuit, bias current range.

Protection circuits test: threshold voltages of protection circuits, bias current range.

Monitoring circuit test: threshold voltage, display function, bias current range.

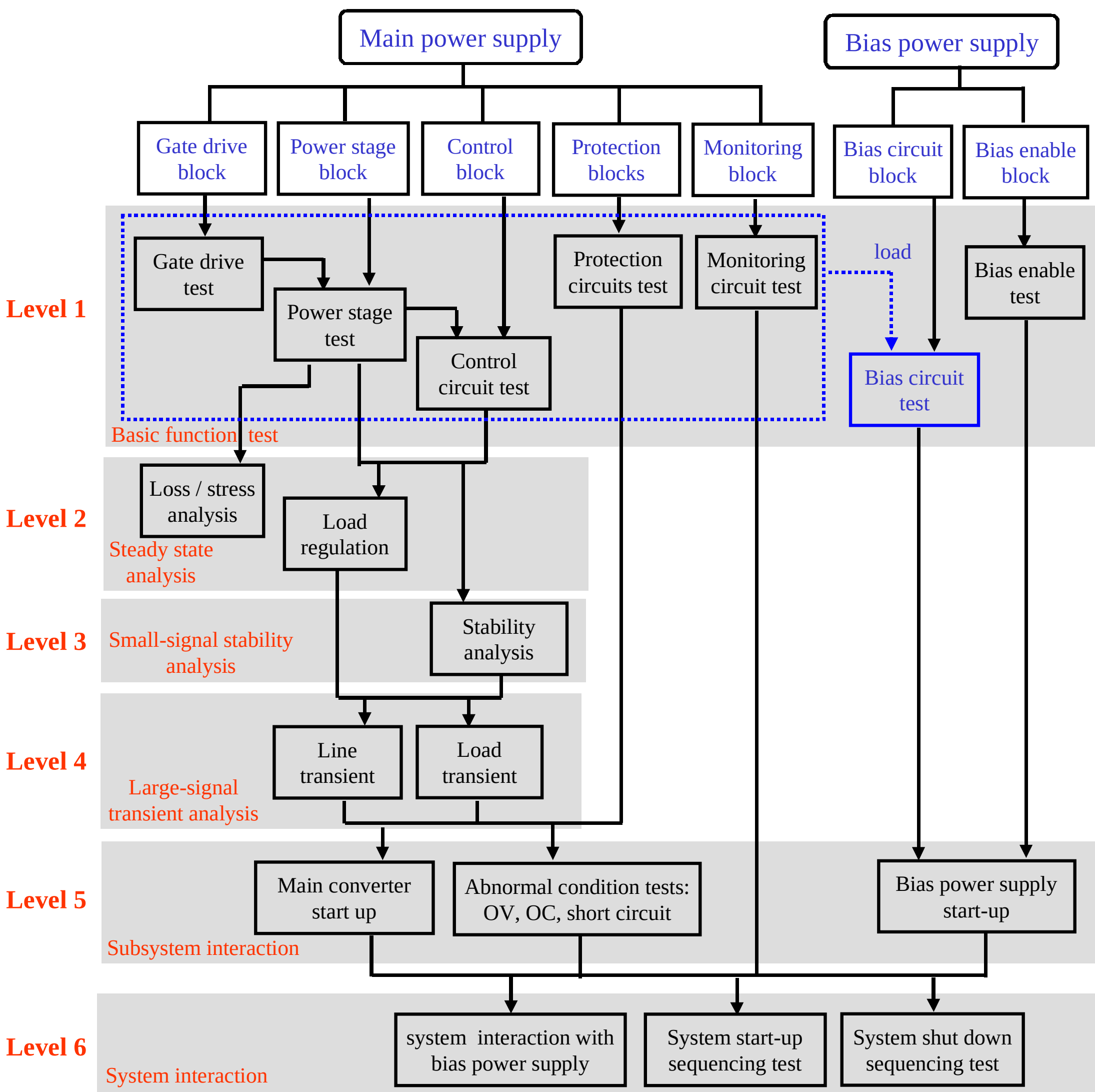


Fig. 2.16. Example of proposed hierarchical test sequence for virtual prototype test. The whole test procedure includes six levels: basic function test, steady state analysis, small-signal stability analysis, large-signal transient analysis, subsystem interaction, and system interaction.

Bias circuit test: the above tests must to be done before the bias circuit test to get the correct load information of the bias circuit (bias current range). Since the bias power circuit is the power supply with simple structure and loose specification, it has similar tests to the main power supply. Some tests may be negligible depending on the detail bias circuit used in different power supply systems.

Bias enable test: threshold enable voltage.

2.3.3.2 Level 2 -- steady state analysis

Since basic operations of the circuit have been verified in level 1, level 2 is going to verify if the design meets static specifications. Following is a list of major parameters tested in simulation.

Loss and stress analysis: power dissipation of main devices, device stresses, transformer saturation in steady state operation, ripple voltage, snubber design.

Load regulation: output voltage over different load and line conditions.

2.3.3.3 Level 3 -- small-signal stability analysis

The level 3 test gets small-signal analysis through time domain simulations.

Stability analysis: phase and gain margins.

2.3.3.4 Level 4 -- large-signal transient analysis

After verifying the circuit operation at steady state and small signal perturbations, level 4 examines circuit operation over the large-signal line and load transients.

Line transient: device stresses, transformer saturation, output voltage regulations (overshoot, undershoot, recovery time).

Load transient: device stresses, transformer saturation, output voltage regulations (overshoot, undershoot, recovery time).

2.3.3.5 Level 5 -- subsystem interaction

Level 5 verifies subsystem response during start-up and abnormal conditions.

Main converter start-up: input current, output voltage overshoot/undershoot, device stresses.

Abnormal condition tests (e.g. OV, OC, and short circuit): output voltage overshoot/undershoot, maximum load current, device stresses, over-voltage protection circuit and over-current protection circuit responses.

Bias power supply start up: input current, output voltage overshoot/undershoot, device stresses.

2.3.3.6 Level 6 -- system interaction

The last level, level 6, is to detect the interactions on the main power supply and the bias power supply.

System interaction with bias power supply: detect interaction problems in steady state.

System start-up sequencing test: output voltage overshoot, start up sequence of control circuit, protection circuits, and monitoring circuit, output voltage rising time, device stresses.

System shut down sequencing test: output voltage overshoot, shut down sequence of control circuit, protection circuits, and monitoring circuit, output voltage hold up time, device stresses.

2.3.4 Multi-level system simulation

After we have partitioned the schematics into blocks, derived multi-level models of circuit components and blocks, and generated a hierarchical test sequence, the last step is to determine the model levels and blocks used in each test. There are three steps to do it:

1. Determine blocks included in the simulation schematics.

2. Determine the model levels of passive components and semiconductor devices of the included blocks (e.g. power stage block).

3. Determine the model levels of other blocks in the simulation schematic (e.g. gate drive block).

We will go through two examples to illustrate the multi-level simulation approach proposed in the virtual prototype test. Fig. 2.17 shows the power stage block diagram of the 5 V forward converter power supply system and Fig. 2.18 is a summary of multi-level models of components in the power stage block.

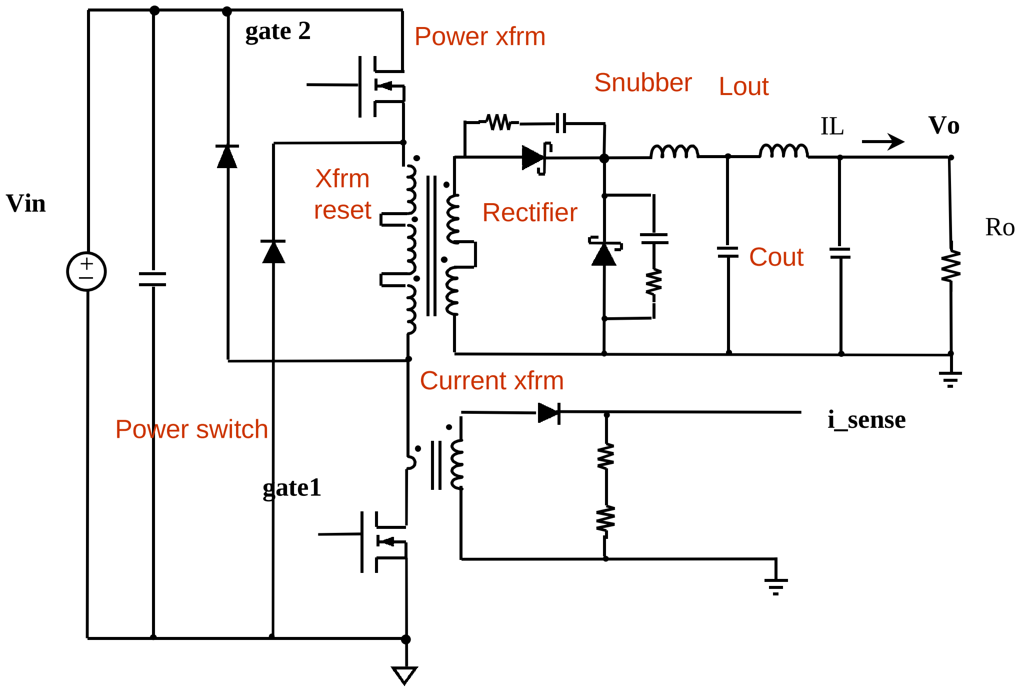


Fig. 2.17. Power stage block circuit diagram of 5 V forward converter power supply system in Fig. 2.11.

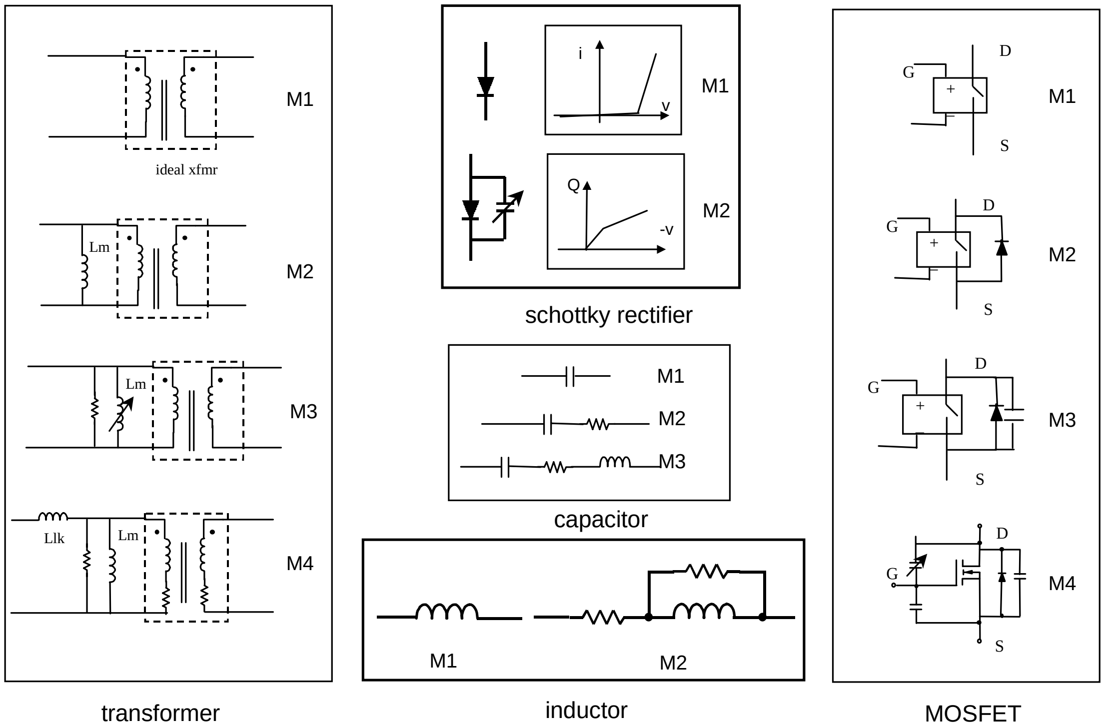


Fig. 2.18. Multi-level models of components in power stage block.

2.3.4.1 Example of multi-level simulation for loss analysis

The first example of multi-level simulation is to calculate power dissipation (loss) of the 5 V power supply system shown in Fig. 2.11. The first step is to determine the models included in the simulation schematics. The blocks selected are shown in Fig. 2.19. Since the over-voltage protection, over-current protection, under-voltage detector, and bias enable blocks do not affect the system's steady state performance, these blocks are eliminated in this simulation.

The second step is to determine model levels of components in the power stage. Consequently, the model complexity of the power stage block is determined. Table 2.3 shows the model of the power stage block for loss analysis. The detail MOSFET mode M4 shown in Fig. 2.18 is selected, since the on and off switching transition determines the switching loss of the MOSFET. Similarly, the rectifier model M2 (with nonlinear charge characteristics) is selected. The snubber circuit is included to eliminate the oscillation of rectifiers. Since the transformer leakage inductance affects the switching speed, M4 model is used. The reset circuit is included to reset the magnetizing inductance. A capacitor model M2 (with ESR) instead of M3 (with ESR and ESL) is selected in the simulation because the effect of ESL in a steady state is negligible. Fig. 2.20 shows the equivalent circuit diagram of the power stage.

The third step is to determine the model levels of other blocks. In the loss analysis, A simple two, 12 V bias voltages model is used for the bias circuit block, a gate drive model M2 shown in Fig. 2.14 is used to get the correct gate resistance. A fixed duty cycle signal is used as a simple PWM control block model.

After these steps, the loss analysis test can be performed by using the simulation schematic generated in the example.

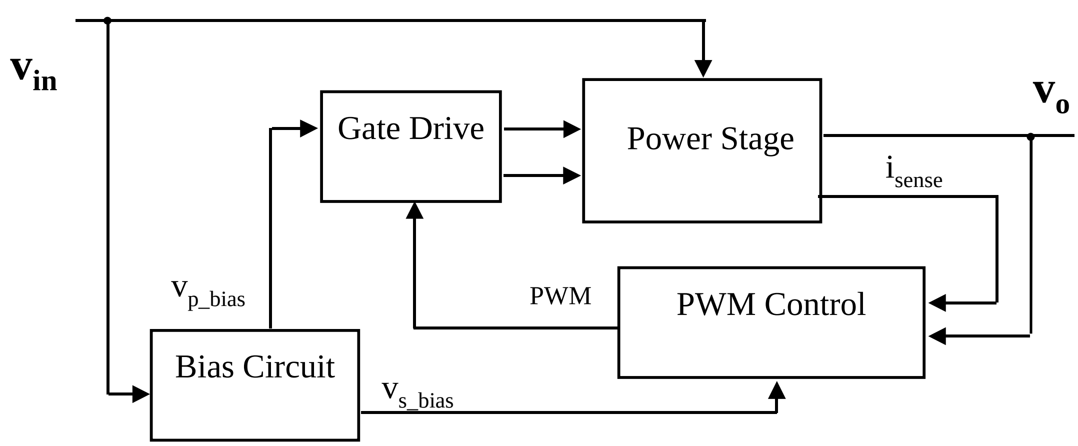


Fig. 2.19 Block diagram of simulation schematic for loss analysis.

Table 2.3. The model of power stage block for loss analysis

Component	Power switch	Power xfrm	Current xfrm	Rectifier	Lout	Cout	Xfrm reset	Snubber
Component level	4	4	2	2	2	2	Y	Y

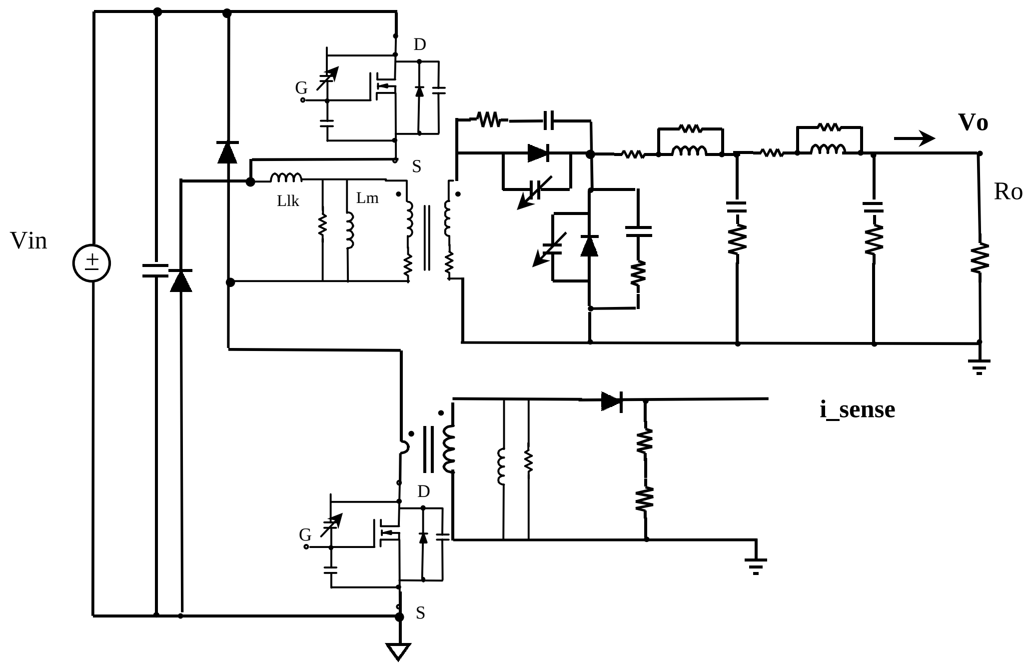


Fig. 2.20. Equivalent power stage circuit diagram for loss analysis.

2.3.4.2 Example of multi-level simulation for short circuit test

The second example of multi-level simulation is a short circuit test of the 5 V power supply system shown in Fig. 2.11. Similar to the first example, the first step is to determine the models included in the simulation schematic. The blocks selected are shown in Fig. 2.21. Since the major purpose of this test is to verify over-current protection, the over-current block is included in the simulation.

Table 2.4 shows the model of the power stage block for a short current test. The switching transition in MOSFET and the rectifier are not important in this test; the simplest switch model and diode model are used. As a sequence, the snubber circuit is not included in the simulation. The transformer model with nonlinear magnetizing inductance is used, since the transformer saturation is monitored. The reset circuit is included to reset the magnetizing inductance. A capacitor mode M3 (with ESR and ESL) is selected in the simulation because the effect of ESL in a fast load transient condition is not negligible. Fig. 2.22 shows the equivalent circuit diagram of the power stage for a short circuit test.

The third step is to determine the model levels of other blocks. In the short circuit test, a simple two, 12 V bias voltages model is used for the bias circuit block, and a gate drive model M1 shown in Fig. 2.14 is used. A detailed PWM control circuit model is used here for the closed loop operation.

From these preceding examples, we see that the simulation schematic with different complexity levels can be determined by identifying the circuit behavior required in each test. More examples will be illustrated later.

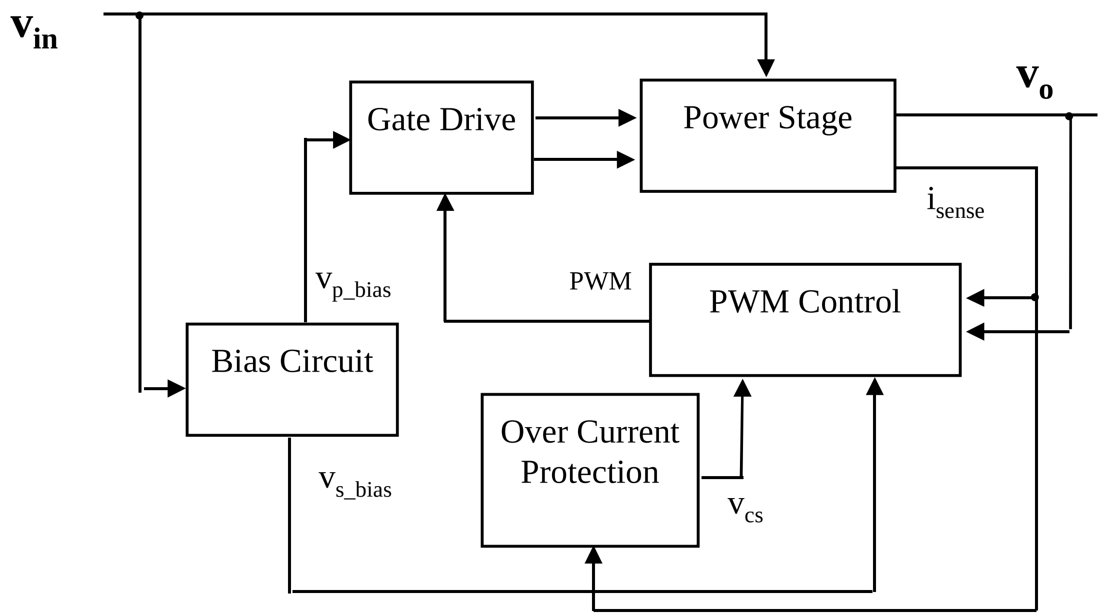


Fig. 2.21 Block diagram of simulation schematics for short circuit test.

Table 2.4. The model of power stage block for short circuit test

Component	Power switch	Power xfrm	Current xfrm	Rectifier	Lout	Cout	Xfrm reset	Snubber
Component level	1	3	1	1	1	3	Y	NA

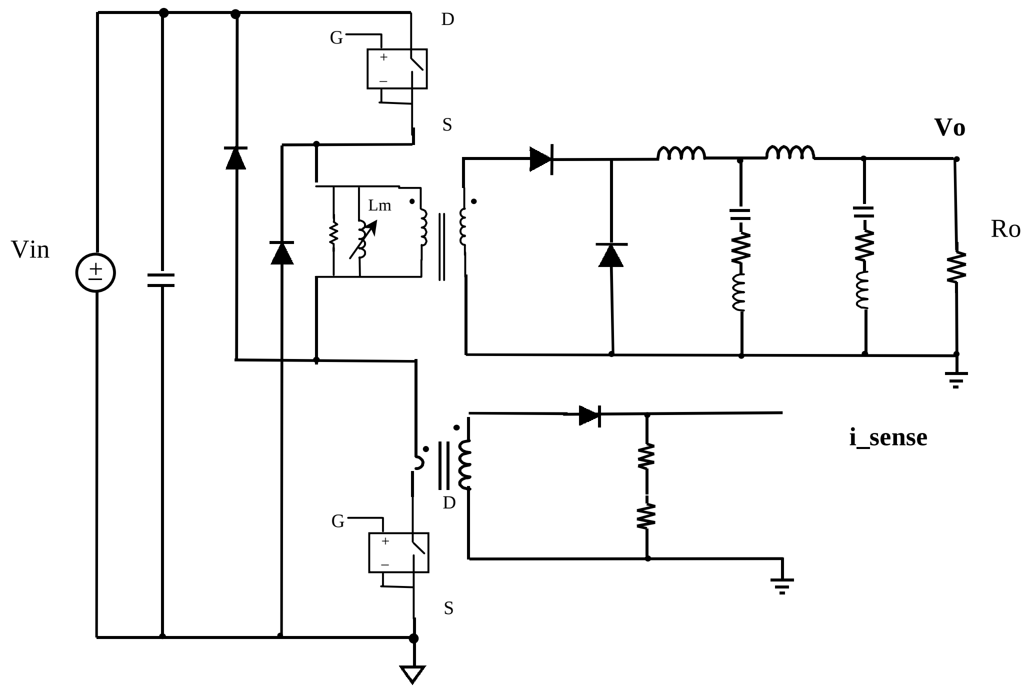


Fig. 2.22. Equivalent power stage circuit diagram for short circuit test.

2.4 Summary

The complexity of the device models and circuits is a key to simulation speed. With large, complex power converter systems, the selection of suitable model levels can affect simulation times significantly. With current simulation practice, the power stage, control circuit, gate drive circuit, and other circuits are often simplified, which results in losing some of the intra-cycle detailed circuit behavior of the real product (e.g. saturation of the devices, time delay of the control circuit due to the device characteristics). In addition, the over-current, over-voltage circuits and bias power supply circuit may be ignored or simulated separately because of the long time transient involved for the whole system; the simulation may even employ an averaged model of the power stage. Although these simulations can be effective when they are used only for understanding the operation of a new circuit, evaluating different topologies, or helping to evaluate certain design parameters, typically, these approaches are not acceptable for virtual prototype test purposes. A more accurately modeled system and a more realistic schematic are needed to detect most of the circuit errors for normal and abnormal conditions.

The multilevel modeling and simulation approach are proposed in this chapter, which focuses on selecting the appropriate level of device model complexity (e.g. diode model level) and block complexity (e.g. gate drive block level) for each specific objective. Therefore, the shortest simulation CPU time can be achieved while still accurately simulating the system's behavior. The multi-level modeling and simulation methodology in the virtual prototype test procedure are composed of four parts:

System partition: identify major functions of the system and partition system into blocks.

Multi-level modeling: identify important characteristics of passive components, semiconductor devices, IC chips, and blocks and create multi-level models for different tests.

Hierarchical test sequence: determine test sequence and condition of virtual prototype tests.

Multi-level simulation: identify important characteristics of the system needed in test (by combining blocks and different levels of models for each particular test) and generate a simulation schematic for each test.

By applying multi-level modeling and simulation methodology in the virtual prototype test, the simulation time and accuracy are improved greatly as shown in Fig. 2.23.

Fig. 2.23 is a comparison among different simulation approaches: SPICE-based simulation, SIMPLIS simulation with simple models, and SIMPLIS simulation with proposed multi-level modeling and simulation approach. The right hand bar chart shows the estimated error percentage that each simulation approach could detect before the first hardware prototyping, and the estimated simulation CPU time for a virtual prototype test with 1000 simulations. It shows that with the proposed simulation approach, the simulation CPU time are reduced significantly while having the highest capability to detect the problems due to the judicious selection of the complexity of the system in each simulation test.

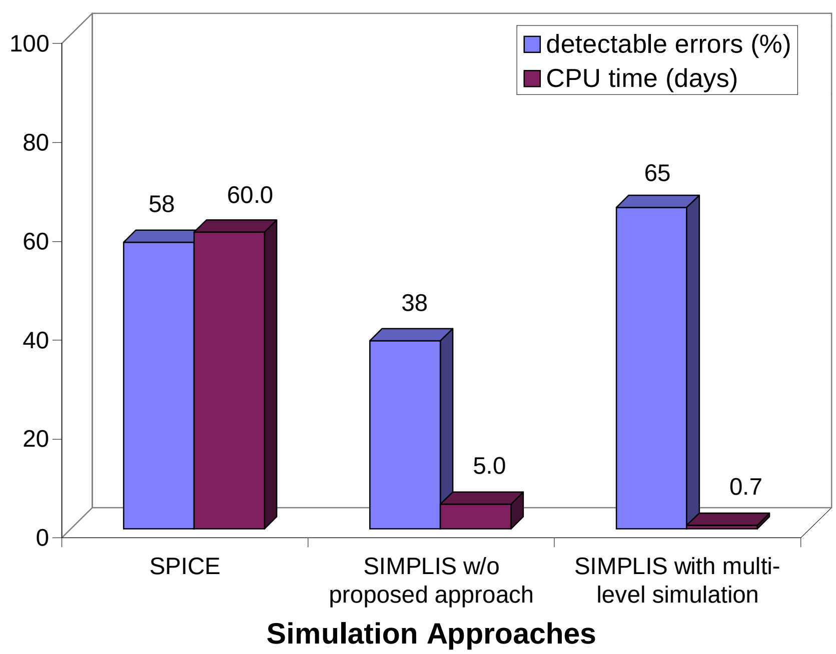


Fig. 2.23. Comparison of estimated detectable error percentage and CPU time for 1000 tests using different simulation approaches. The simulation CPU time and detectable errors are improved significantly by developing a multi-level modeling and simulation approach.

3. MULTI-LEVEL MODELING

The complexity and accuracy of models used in the virtual prototype test will directly affect the simulation speed and the accuracy of the system's behavior. Because the virtual prototype test not only requires a large number of simulation tests, but also requires adequate accuracy in the simulation to represent and detect the design problems in the real circuit, how to model the power supply system is critical to the success of the virtual prototype test.

This chapter will illustrate how to implement multi-level models of the power supply system and discuss major models used in the virtual prototype DVT.

3.1 General rules and consideration

There are numerous models available in different simulations as well as many different ways to derive a model engine [28, 35-36, 47-51]. How can we select or implement an adequate model from so many choices? A diode is used as an example to illustrate the modeling principles for the virtual prototype test.

3.1.1 Identifying derived component characteristics

Before implementing the diode model, the first task is to identify the major characteristics of a diode and understand how each characteristic of the component contributes to different system behavior in a simulation. The basic function of a diode is to pass current in one direction and block it in the opposite direction. The basic function relates to two important characteristics of the diode: forward current vs. forward voltage and reverse current vs. reverse voltage. At high frequency, the parasitic capacitance of the parasitic pn junction becomes significant; it is related to capacitance vs. reverse voltage characteristics in the data sheet. The other characteristic is the diode break down reverse voltage. The major characteristics of a schottky rectifier are shown in Fig. 3.1.

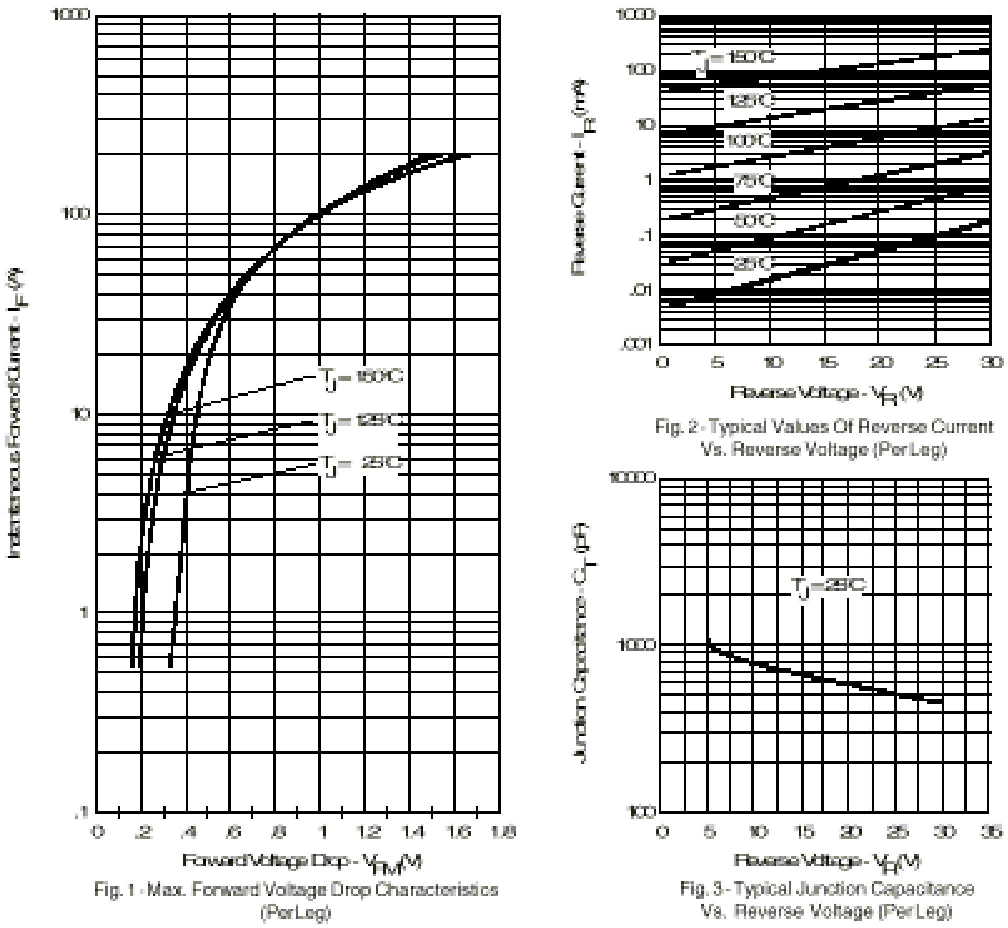


Fig. 3.1. Major characteristics of a schottky rectifier.

3.1.2 Piecewise linear modeling

After identifying the major characteristics of the component, different levels of model can be derived. Fig. 3.2 shows the I-V characteristics of a diode. A piecewise linear resistor is used to implement the I-V characteristics. In order to simplify the discussion, we have two assumptions: the piecewise linear curve passes the original (V_F = 0 V, I_F = 0 A), and the maximum number of the piecewise-linear segments in the model is three to keep the model reasonably simple and to maintain adequate simulation speed. Fig. 3.3 shows several possible approaches to implement the I-V characteristics. The solid lines are actual curves and the dotted lines are piecewise linear approximations. Fig. 3.3(a) is a simple two-segment approximation. Fig. 3.3(b) - Fig. 3.3(d) improves the model by adding an additional segment for a different purpose. Fig. 3.3(b) improves the forward voltage vs. current characteristics in the model, Fig. 3.3(c) improves the reverse voltage vs. current characteristics in the model, and Fig. 3.3(d) adds the break down reverse voltage characteristics.

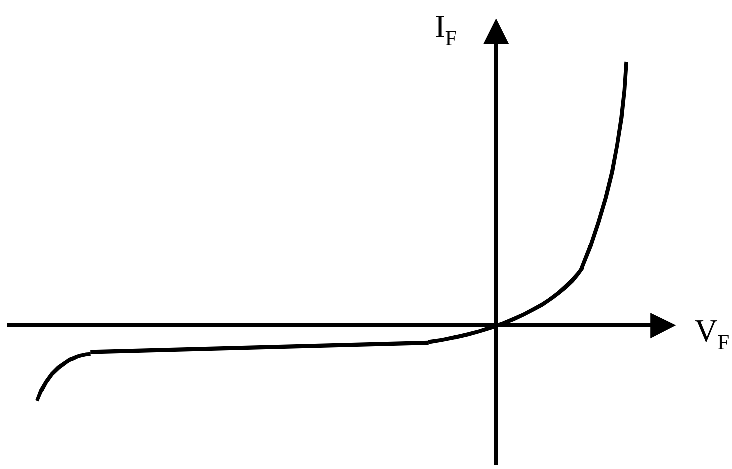


Fig. 3.2. I-V characteristics of a diode.

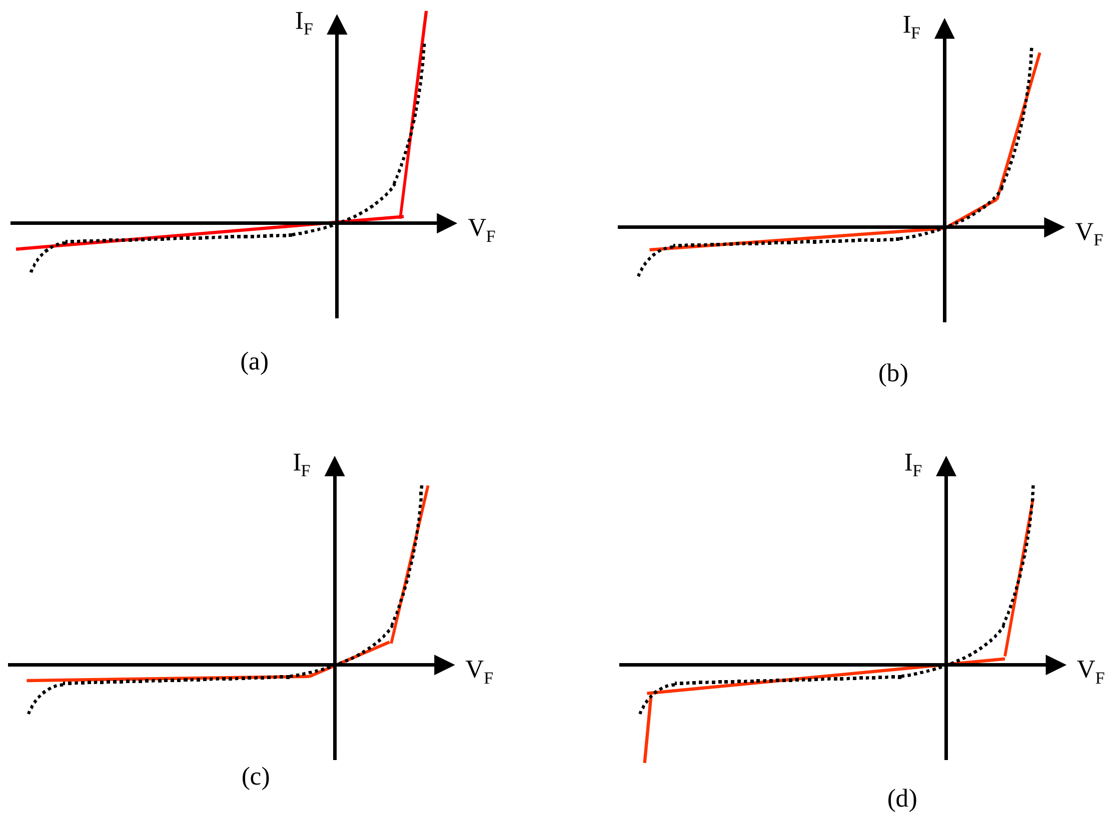


Fig. 3.3. Example of implementation of the I-V characteristics of a diode. The solid lines are actual curves and the dotted lines are piecewise linear approximation. (a) simple two-segment approximation. (b) improved forward voltage vs. current characteristics. (c) improved reverse voltage vs. current characteristics. (d) additional break down reverse voltage feature.

The selection of model levels of I-V characteristics depends on different applications, tests, and designer's preferences, and is a trade off between simulation speed and accuracy as well. In Fig. 3.3, (a) has fast simulation speed and is accurate enough for most of the applications, (b) has a more accurate circuit behavior during transient, (c) is used when the leakage current is an important parameter in circuit operation (e.g. in a mag-amp post regulator [45]), and (d) is used in a zener diode.

Similarly, the voltage-dependent capacitance characteristic of the pn junction (solid line of Fig. 3.4(a)) can be implemented by a piecewise linear capacitor. The piecewise linear capacitance in SIMPLIS is described by the charge vs. voltage characteristics as shown in the solid line of Fig. 3.4(b). The total topologies of the diode model are the product of segments of the I-V curve and the segments of the Q-R curve. A two-segment approximation as shown in the dotted line of Fig. 3.4(b) is suggested to reduce the complexity of the whole diode model. The corresponding capacitance vs. voltage curve is shown in the dotted line of Fig. 3.4(a). The voltage-dependent capacitance characteristic of the pn junction is included in a diode model when the simulation requires circuit detail waveform at high frequency (e.g. loss analysis, snubber design).

For the whole power supply system, there are a lot of components which need to be implemented in a virtual prototype test, and each component could have many model levels. To simplify the virtual prototype test procedure, the total levels for each component should be minimized.

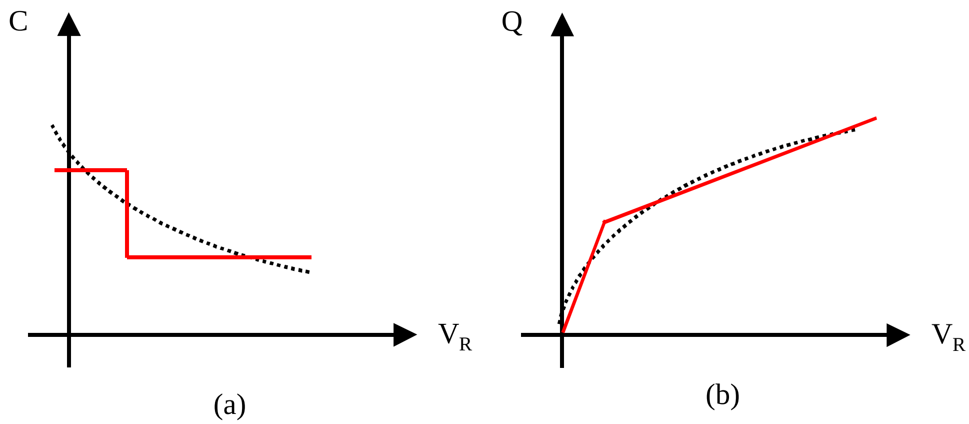


Fig. 3.4. The voltage-dependent capacitance of the pn junction (solid line of (a)) is implemented by a piecewise linear capacitor in SIMPLIS. The piecewise linear capacitance in SIMPLIS is described by the charge vs. voltage characteristic as shown in the solid line of (b). A two-segment approximation is suggested as shown as dotted lines in (a) and (b) correspondingly.

3.1.3 Selecting adequate parameter values for the model

The selection of model parameter values is also very important in a virtual prototype test. An adequate parameter value could improve the accuracy of the simulation without extra complexity in the model. We will illustrate the principle by selecting the parameter value of a simple two-segment rectifier model.

A two-segment diode is often called an ideal diode. It is modeled to have an infinitely or extremely small on resistance and an infinitely or extremely large off resistance as shown in Fig. 3.5(a). Little accuracy is lost by this assumption when the purpose of the simulation is to understand circuit operation. For example, simulating a buck converter by using an ideal diode and an ideal switch still provides the correct operation of the buck circuit and shows that the duty cycle is a function of output voltage and input voltage. However, this is not the case in the virtual prototype test.

The virtual prototype simulation needs to represent more reality of a hardware prototype. The duty cycle is not only a function of output voltage and input voltage, but also a function of load current due to the current dependent of the forward voltage drop of the diode and switch. With the same model structure, an adequate on resistance of the rectifier provides more circuit information than the one with an "ideal" on resistance.

Fig. 3.5(b) shows one possible way to select parameter values for a two-segment rectifier diode model. Point 1 and point 2 determine the on resistance of the diode, while Point 3 and point 4 determine the off resistance of the diode. Point 1 is selected at full load or maximum load to provide a more accurate result at extreme conditions; point 2 is selected so the on resistance curve fits the I-V curve as closely as possible. Point 3 is at the origin, and point 4 is selected at 75% of the break down voltage point, since in hardware design, the designer considers that the diode reverse voltage should not exceed 75% of the break down voltage in our case.

There is no fixed way to select parameter models. The model is adequate as long as it presents the most important characteristics of the circuit. An example of how to derive a rectifier model is provided in the appendix in a MATLAB file format. For small signal diode models, it is not necessary to derive a new model every time when simulating a new power supply system. Several general diodes with fixed parameters can be stored in a device library for reusing these derived models. For a large signal diode, such as a shottky rectifier, a dynamic library (model with variable parameters) is recommended, since the model parameters could change corresponding to different applications and design concerns. The parameters can be calculated easily by inserting device data from a data sheet or measurement by using a MATLAB file.

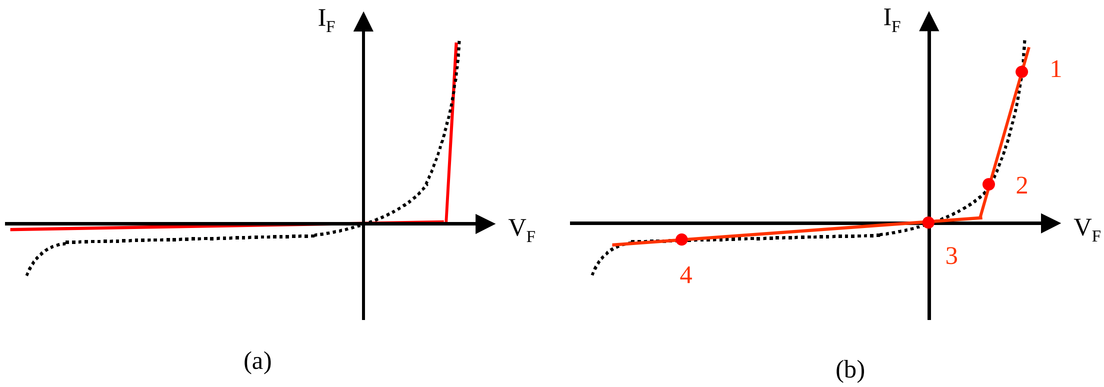


Fig. 3.5. Select parameter values of a two-segment diode. (a) an ideal model with extremely small on resistance and extremely large off resistance. (b) a proposed model in the virtual prototype test, in which point 1 and point 2 determine the on resistance, point 3 and point 4 determine the off resistance.

3.1.4 Understanding the limitation of the model

The components of the analog circuit, especially in a power electronics circuit, show a large extent of non-linearity. No matter how good the model is, it is almost impossible to be "equal" to the real components. Therefore, it is important to know the assumptions made when each model is derived, and beware of the limitation or accuracy of the simulation when some assumptions do not hold.

3.2 Modeling of circuit components

There are two types of models in a virtual prototype: the circuit component model and the function block model. In this section, we will first discuss the circuit component models. The circuit component models are discussed in three categories: passive components, semiconductor devices, and IC chips.

Fig. 3.6 is a redrawing of the 5 V forward converter power supply system discussed in chapter 2. Fig. 3.7 shows multi-level models of components, devices, and IC chips for the virtual prototype test of a power supply system. The shaded models mean all or part of the original SIMPLIS models are used in the tests. We will discuss each category in the following sections.

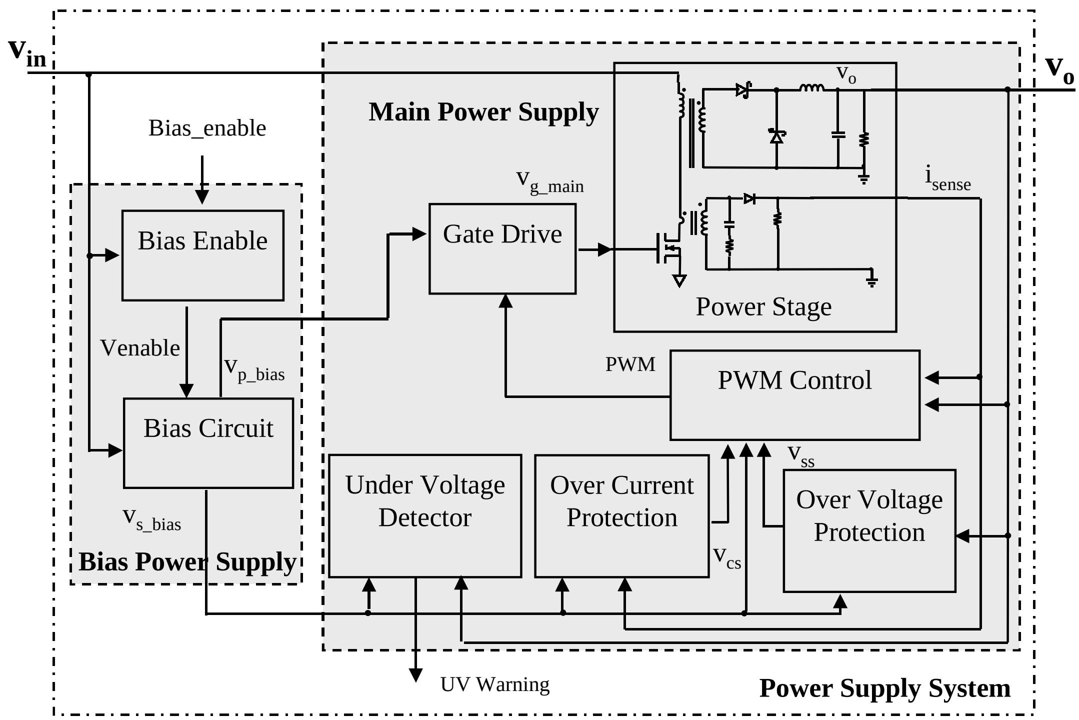


Fig. 3.6. Redrawing of circuit block diagram of the 5 V power supply system.

Passive component

name	capacitor	inductor	transformer
total model levels	3	2	4

Semiconductor device

name	diode	MOSFET	bipolar transistor
total model levels	2	4	2

IC chip

name	op amp	comparator	optical coupler	voltage regulator	gate driver
total model levels	1	1	1	1	1

Fig. 3.7. Multi-level models of passive components, semiconductor devices, and IC chips for the virtual prototype test of a power supply system in chapter 2. Shaded models mean all or part of SIMPLIS models are used in the tests.

3.2.1 Modeling of passive components

3.2.1.1 Models of passive components

In order to simulate the power supply subsystem using the multiple level complexity modeling approach, the selection of the model level complexity is very important. An understanding of the effect of each parasitic parameter in the components is one of the keys to success. Major components include the capacitor, inductor, and transformer as shown in Fig. 3.8, Fig. 3.9, and Fig. 3.10. SIMPLIS models for the capacitor and inductor are used. Transformer models are implemented by parameters Lm and Llk instead of core information in SIMPLIS (core material, AL value, and so forth).

3.2.1.2 Effect of parasitics -- an example

A study of the effect of each parasitic parameter of an output capacitor is presented here to demonstrate the approach used to determine models with different levels of complexity. Capacitor model level 2 and level 3 are compared in the simulation to study the effect of the parasitic parameters.

A simplified circuit diagram of the secondary side of the power converter with a two-stage output filter is shown in Fig. 3.12. The major parasitic parameters of a capacitor are the equivalent series inductance (ESL) and the equivalent series resistance (ESR) as shown in the figure. In Fig. 3.12, Vo is the voltage across the output capacitor. For a power converter with constant current load, the waveform of the output capacitor voltage with parasitic parameters is shown in Fig. 3.13. It shows that a capacitor model without ESL could be used in this condition.

Fig. 3.14 shows the simulated waveform of the output voltage following a change in load current from 90A to 80A at a 10A/us rate of change. A level 2 capacitor model and a level 3 capacitor model are used for each of the two capacitors in the output filter. The measurement is not available because of the limited current step ratio of the load equipment in the laboratory. The measurement is expected to have the same waveform as in the simulation. From the simulation result, we can see that in order to predict the voltage across the output capacitor, the most complex capacitor model needs to be used in the simulation.

According to the study of the capacitor during different tests, the multi-level model of the capacitor can be summarized as in Table 3.1.

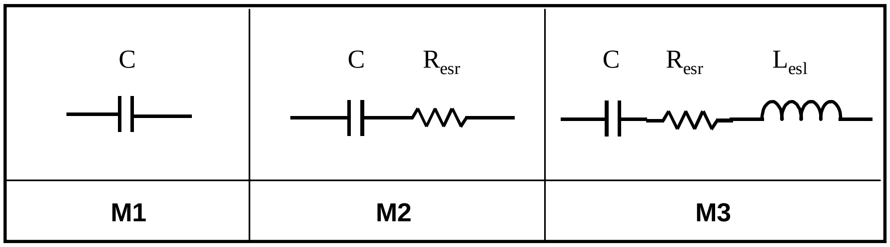


Fig. 3.8. Capacitor models. C: capacitance; R_{esr}: ESR; L_{esl}: ESL.

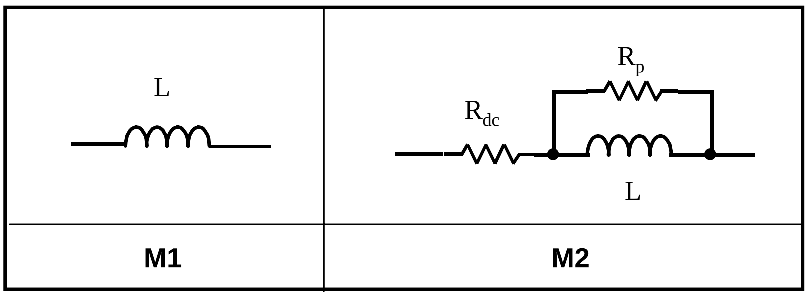


Fig. 3.9. Inductor models. L: inductance; R_{dc}: winding dc resistance; R_p: core loss resistance.

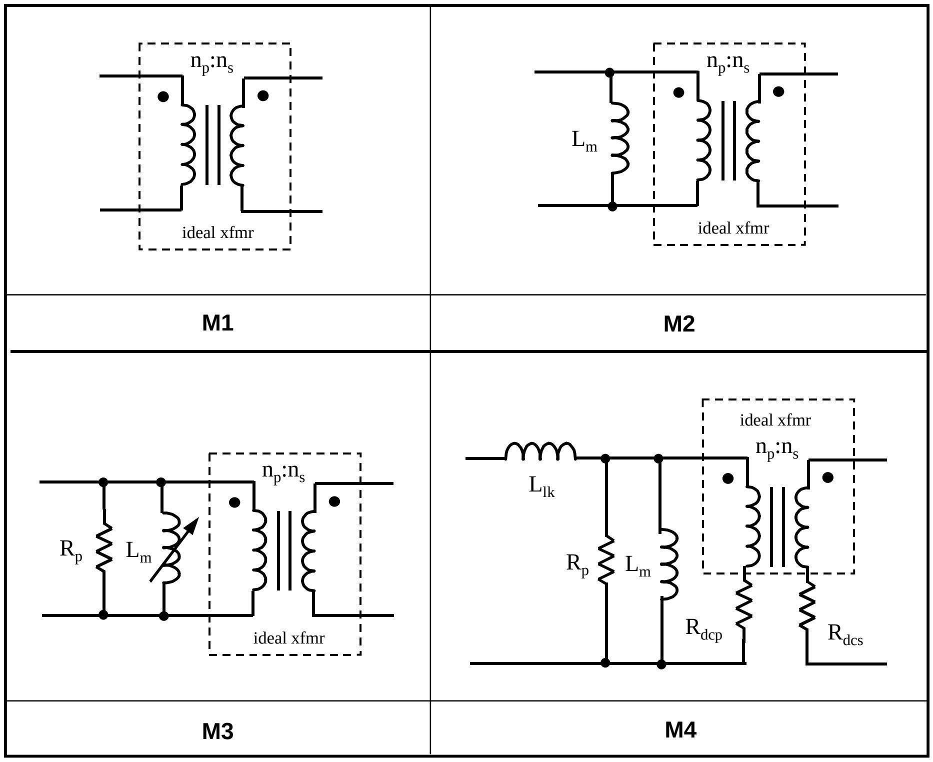


Fig. 3.10. Transformer models. L_m: magnetizing inductance; L_{lk}: leakage inductance; R_{dcp}, R_{dcs}: winding dc resistance; R_p: core loss resistance

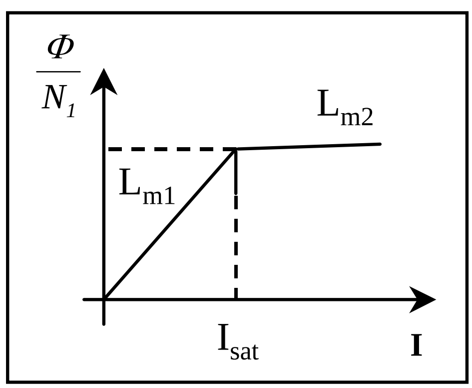


Fig. 3.11 L_m characteristics in M3 of Fig. 3.10.

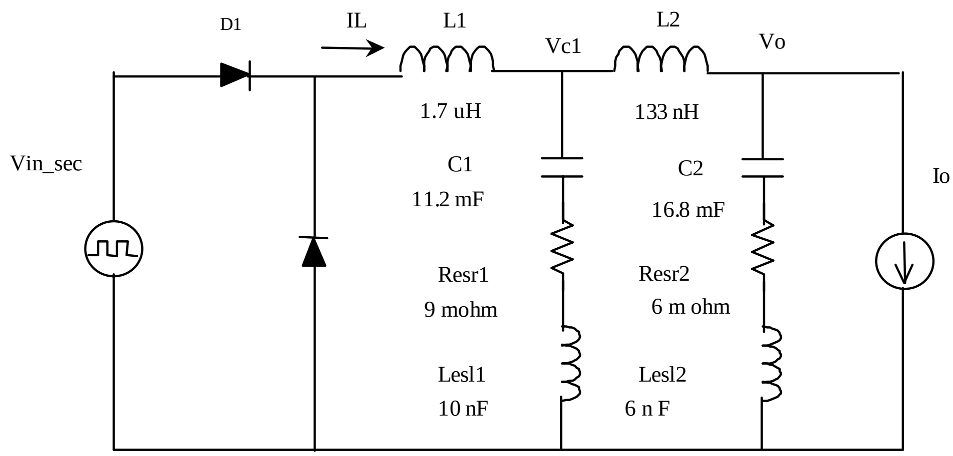
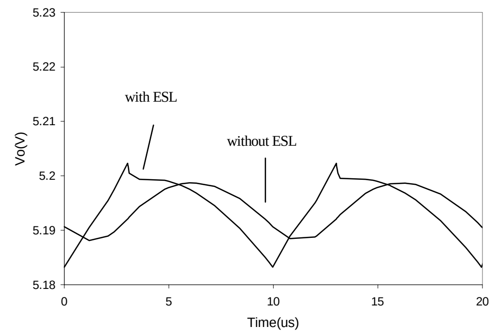
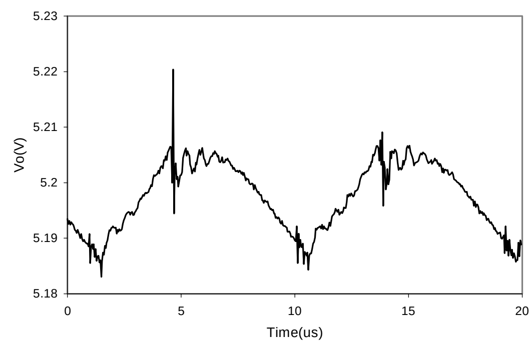


Fig. 3.12. Simplified circuit diagram of the secondary side of the power converter with a two-stage output filter.



(a) Simulation results of Vo.



(b) Measurement of Vo

Fig. 3.13 Output voltage of the second stage of the tow-stage output filter.

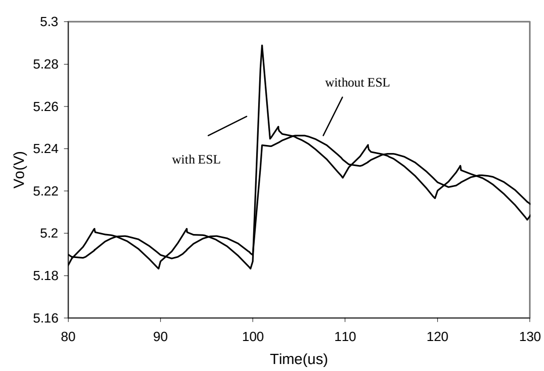


Fig. 3.14 Output voltage waveforms when the load step changes from 90A to 80A with 10A/us rate.

Table 3.1. Application example for multi-level models of the capacitor.

Model level	Description	Application example
M1	Capacitor	Capacitor in compensation network
M2	Capacitor with ESR	Output capacitor for steady state analysis
M3	Capacitor with ESR and ESL	Output capacitor during fast load transient or high frequency operation

3.2.2 Modeling of semiconductor devices

3.2.2.1 Models of semiconductor devices

The major semiconductor devices include the diode, MOSFETs, and bipolar transistors. The simplest model usually only has on and off characteristics to present the basic function of the device, and a detailed model includes the on or off transient behavior, which is especially important for loss analysis, snubber design, and so on. The multi-level models are shown in Fig. 3.15- Fig. 3.21.

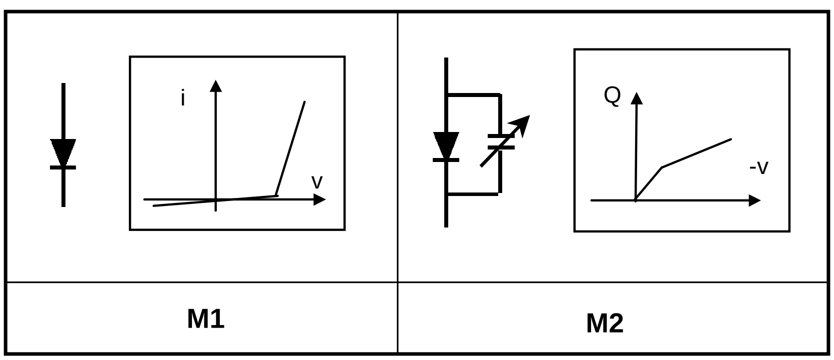


Fig. 3.15. Diode models.

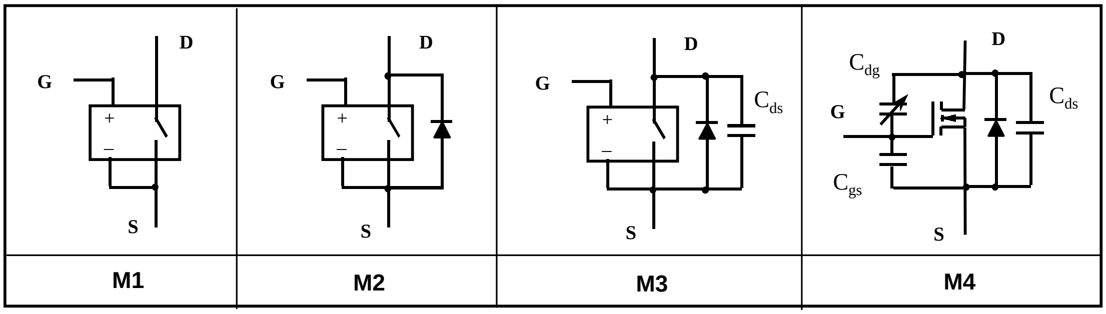


Fig. 3.16. N MOSFET models.

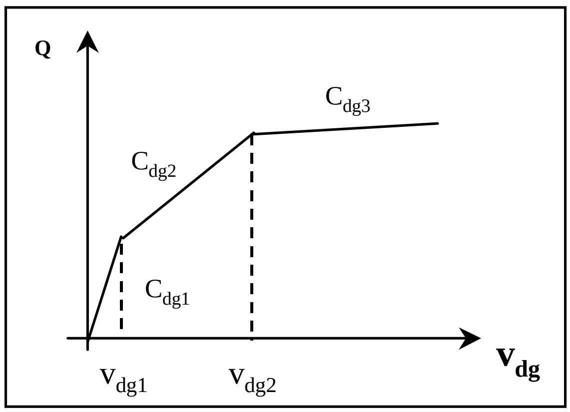


Fig. 3.17. C_{dg} characteristics in M4 of N MOSFET models.

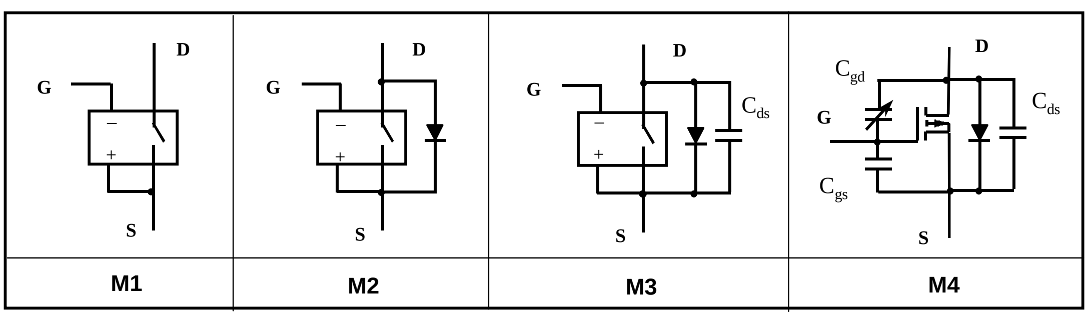


Fig. 3.18. P MOSFET models.

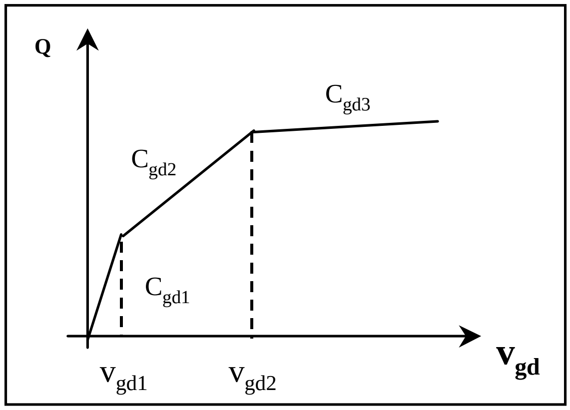


Fig. 3.19. C_{gd} characteristics in M4 of P MOSFET models.

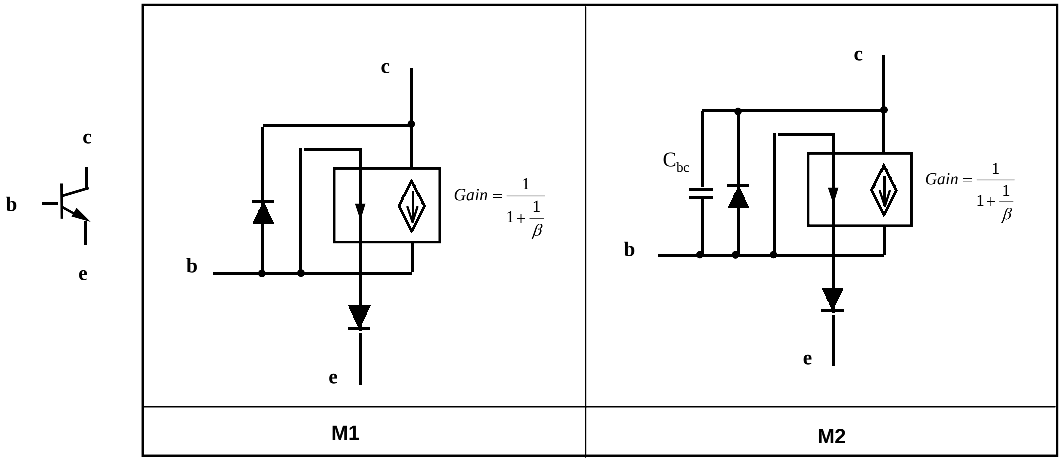


Fig. 3.20. NPN bipolar transistor model.

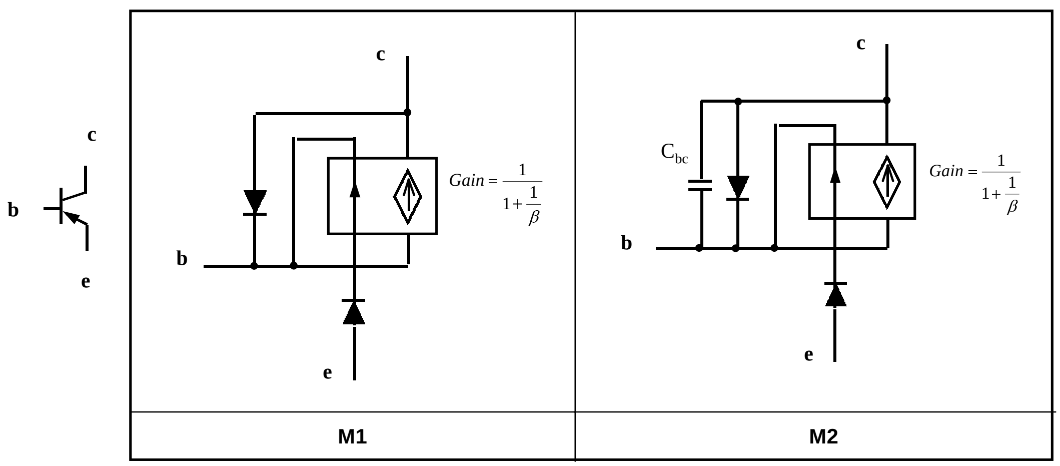


Fig. 3.21. PNP bipolar transistor model.

3.2.2.2 Modeling of MOSFET

Fig. 3.16 shows the multi-level models of a N MOSFET. Similar to the diode model, we can summarize the major applications for different levels of model in Table 3.2.

Table 3.2. Application example for multi-level models of MOSFET.

Model level	Description	Application example
M1	Ideal switch	Main switch for system level simulation
M2	Ideal switch + body diode	Active-clamp switch
M3	M3 + Cds	ZVS of main switch
M4	FET with on and off transient characteristics	Loss analysis, snubber design

M4 model as shown in Fig. 3.22 can present the on and off transient of the MOSFET [35]. It is implemented by a FET model as shown in Fig. 3.23 and charges of the MOSFET. The equivalent MOSFET model for on, off, and active states are shown in Fig. 3.24. The current Ci during active stage is:

$$C_i(t) = g_m \cdot (V_{gs}(t) - V_{th}) \tag{3.1}$$

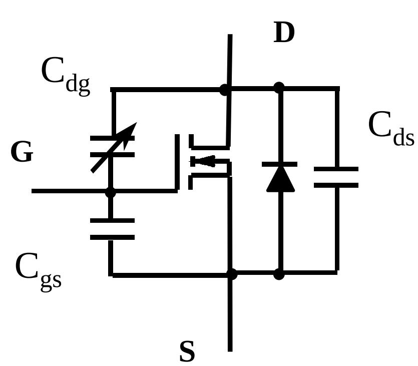


Fig. 3.22. Basic structure of MOSFET model (M4).

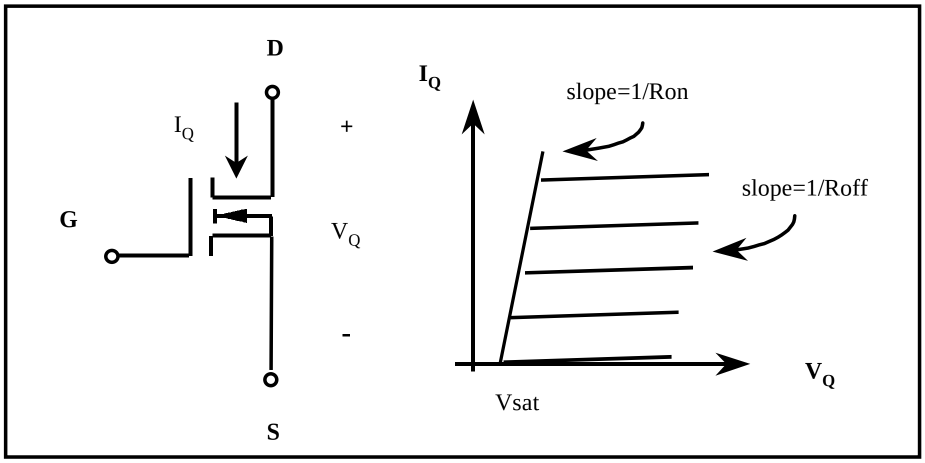


Fig. 3.23. Major characters of the FET model.

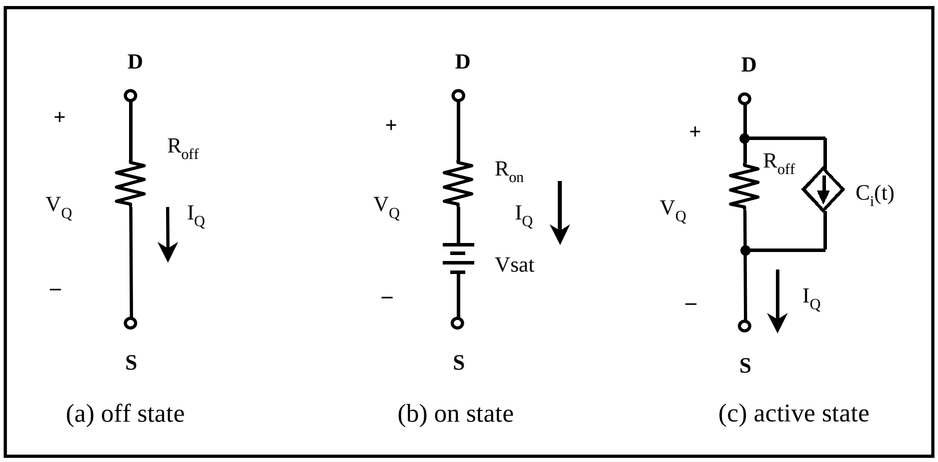


Fig. 3.24. Equivalent MOSFET model for on, off, and active states.

3.2.3 Modeling of IC chips

3.2.3.1 Models of IC chips

Modeling of IC chips is more complex because there are many characteristics for each chip and a chip could be very complex, such as a controller chip.

Major IC chips in the circuit include the operational amplifier, comparator, optical coupler, gate driver, voltage regulator, and different controller chips which are combinations of basic IC chips and will not be discussed here. Most of the IC chips are modeled as behavior models to simplify the circuit and accelerate the simulation. It is especially important to identify the characteristics needed in each test, since an IC chip model could be very simple or very complex in order to present the characteristics required.

To accelerate the simulation speed without losing the accuracy of the system, multi-level models are needed for each IC chip. How can we implement multi-level models of IC chips when the models in the current library are not sufficient? This section will use an operational amplifier to demonstrate a general approach to implement models.

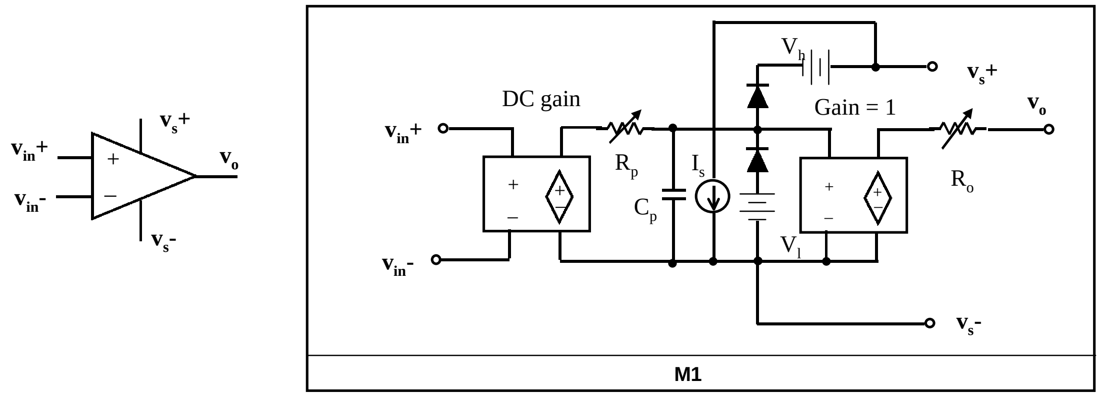


Fig. 3.25. Operational amplifier model.

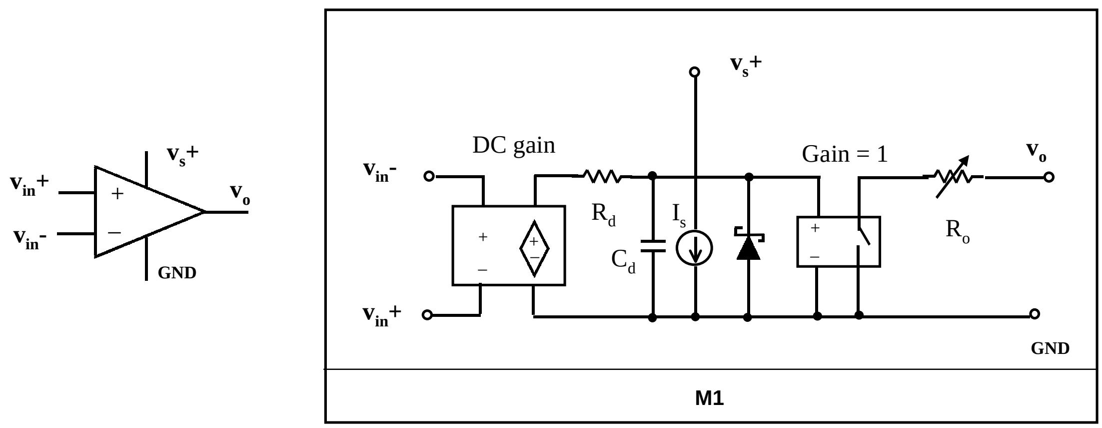


Fig. 3.26. Comparator model.

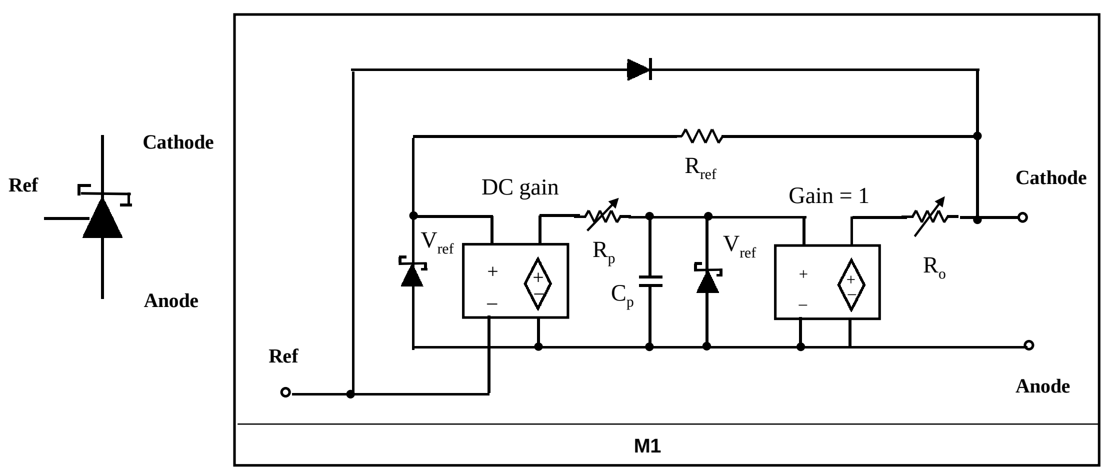


Fig. 3.27. Voltage regulator TL431 model.

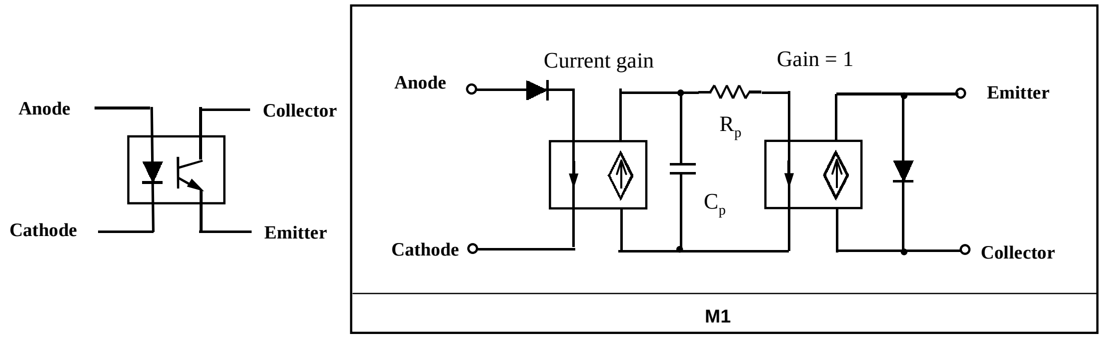


Fig. 3.28. Optical coupler model.

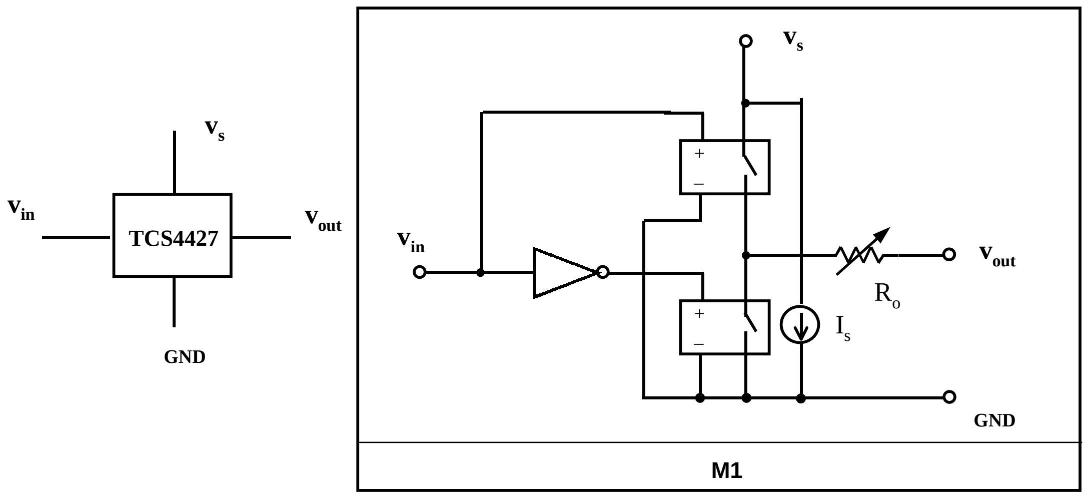


Fig. 3.29. Gate driver TSC4427 model.

3.2.3.2 Modeling of operational amplifier

An operational amplifier consists of transistors, resistors and capacitors, and can be modeled at the device level. It can also be modeled at the behavioral level in terms of its two-port characteristics: the input impedance, the output impedance, and the voltage gain. All of these quantities are tabulated as functions of frequency in the data sheets from various manufacturers. A behavioral model can be synthesized in terms of resistors, inductors, capacitors, and controlled sources almost independently of the actual components inside the operational amplifier [36]. The modeling procedure is described as follows.

An ideal operational amplifier with infinite input impedance, zero output impedance, near infinite dc gain, and output voltage clamping as shown in Fig. 3.30(a) is used to study circuit topologies or different control schemes. However, this ideal model is not suitable to be used in the virtual prototype test. An improved operational amplifier model with low frequency pole characteristic is shown in Fig. 3.30(b).

Fig. 3.30(c) shows a further improved version of the operational amplifier model with input impedance, output impedance, output slew rate, and output sourcing and sinking capabilities. This model can be used in most of the simulations since it presents the adequate "delay" behavior in control or protection circuits.

When a tolerance analysis of threshold voltage in a protection circuit is needed, the bias and offset current and bias voltage of the operational amplifier could be modeled as shown in Fig. 3.30(d). A bias power supply current is also modeled in Fig. 3.30(d).

Does that mean that we need four models for an operational amplifier? The level one will not be used since a test either requires a level 2 (for threshold voltage) or the delay or control is needed. Level 4 only adds a current source, which will not increase the complexity of the circuit much, so we will reduce the total model levels of the operational amplifier to two levels. Since the tolerance analysis will not be discussed in this dissertation, only one level is used in the simulation as shown in Fig. 3.25.

The model has an output impedance Ro, two clamp diodes, Dh and Dl, which clamp the output to the power supply of pin 3 and 4, respectively. Rp and Cp are used to create op amp open-loop low-frequency pole, Rp also limits the maximum current capability of the op-amp to present slew rate characteristic, and Is is the static supply current of the IC chip.

Data of the LM358 are used to create the corresponding operational amplifier model. The comparisons of the derived model to the data sheet with major characteristics are shown in Fig. 3.31 and Fig. 3.32. The model's characteristics match the data sheet very well. The parameters in the model can be determined easily from the data sheet.

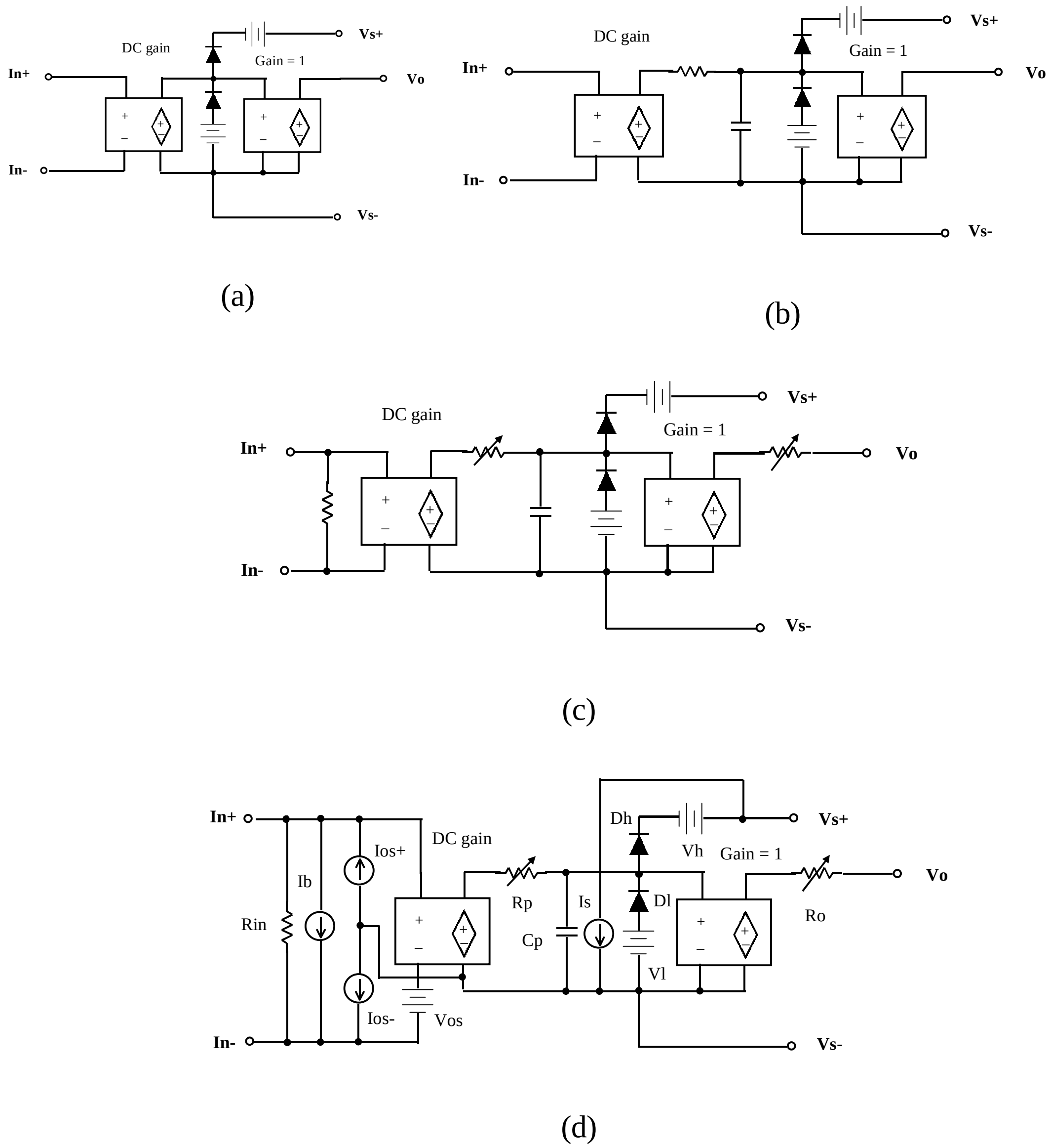
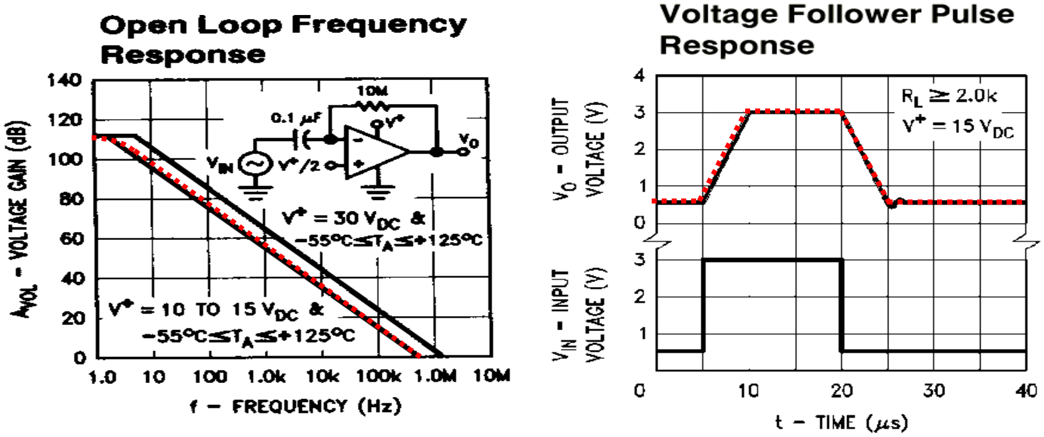
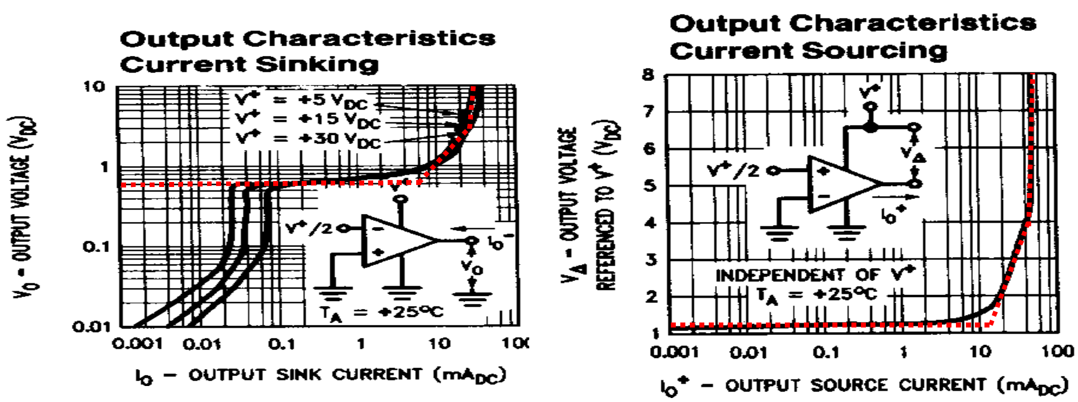


Fig. 3.30. Derivation of operational amplifier. (a)ideal operational model. (b) improved model with low frequency pole. (c) improved model with slew rate, output sourcing and sinking capability. (d) improved model with bias current, offset voltage and curent of input pins, and power supply current.



(a) (b)

Fig. 3.31. Comparison of open loop frequency response and slew rate of the operational amplifier LM358 with data sheet. Dotted lines are simulation results. Solid lines are from the data sheet.

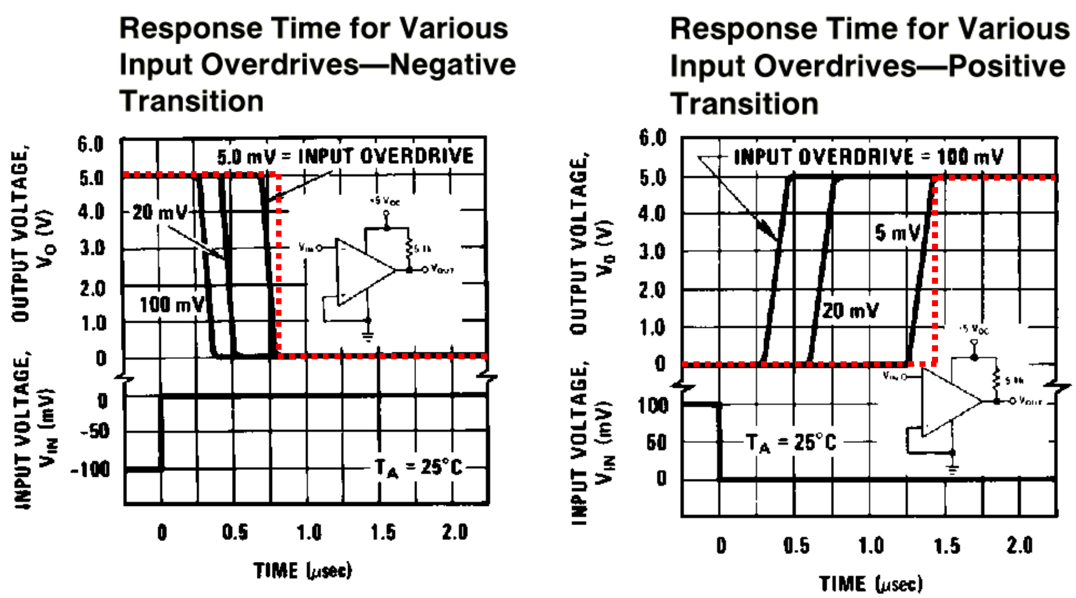


(a) (b)

Fig. 3.32. Comparison of output characters of the operational amplifier LM358 with data sheet. Dotted lines are simulation results. Solid lines are from the data sheet.

3.2.3.3 Modeling of comparator

Data of the LM339 is used to build the corresponding comparator model. Since the major difference between an op amp and a comparator is the comparator's open collector output and faster response characteristics, the model of the comparator is different from the previous op amp model. Fig. 3.26 is the LM339 model schematic. The open collector output characteristic is modeled by a switch to set proper on and off resistance. The comparator does not have a slew rate feature; the delay time of the output is set as in the data sheet of "response time for various input overdrives, both negative and positive transition." The parameters can be settled in the model by adjusting the value of R, C, and the voltage controlled switch parameters. Fig. 3.33 and Fig. 3.34 show the comparison of the waveforms from the simulation results and the data sheet; the results match the data sheet very well.



(a) (b)

Fig. 3.33. Comparison of the response time delay of the comparator LM339 with the data sheet. Dotted lines are simulation results. Solid lines are from the data sheet.

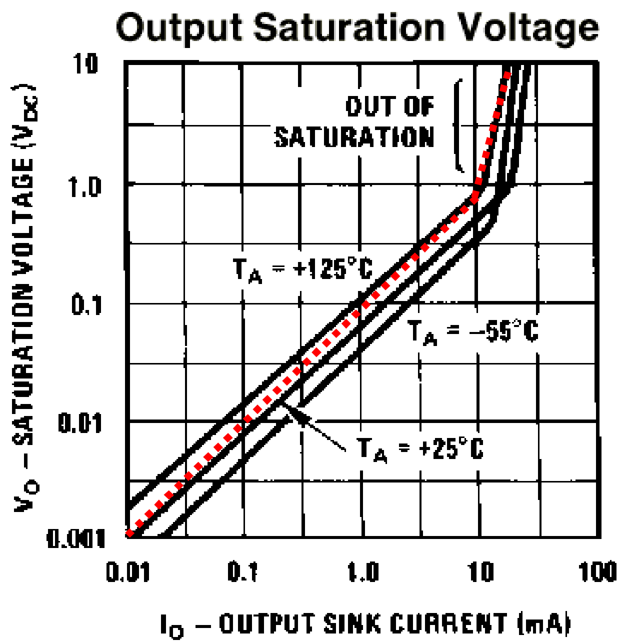


Fig. 3.34 Comparison of output characters of the comparator LM339 with the data sheet. Dotted lines are simulation results. Solid lines are from the data sheet.

3.3 *Modeling of function blocks*

3.3.1 Models of function blocks

Since the complexity of the device models and subcircuits is a key to simulation speed, with large, complex power converter subsystems, the selection of suitable model levels can affect simulation time significantly. Similar to the generation of multi-level models of devices, components, and IC chips, the multi-level modeling of function blocks follows the same procedure.

According to the function of each block, the blocks of power supply systems as shown in Fig. 3.6 can be defined as six categories: the main power stage, the gate drive circuit, the control circuit, protection circuits, the bias power supply, and other monitoring circuits. Each block could have more than one level when necessary. The models could be varied according to different systems and applications. Here we use the system in Fig. 3.6 as an example to demonstrate the levels. Fig. 3.35 is an example of the model levels of blocks needed in a virtual prototype test in the power supply system.

block name	power stage	gate drive	pwm control	OC	OV	UV	bias enable	bias
total model levles	7	3	3	1	1	1	1	3

Fig. 3.35 Example of model levels of blocks needed in a virtual prototype test in the power supply system shown in Fig. 3.6.

3.3.2 Main converter

Main converter models are more dependent on the specific tests. We are going to discuss them in the next chapters.

3.3.3 Gate drive

The gate drive models are shown as in Fig. 3.36. There are three different levels: M1 presents the basic function of the gate drive, M2 has both the basic function of the gate drive and the bias supply current, and M3 is a detailed model.

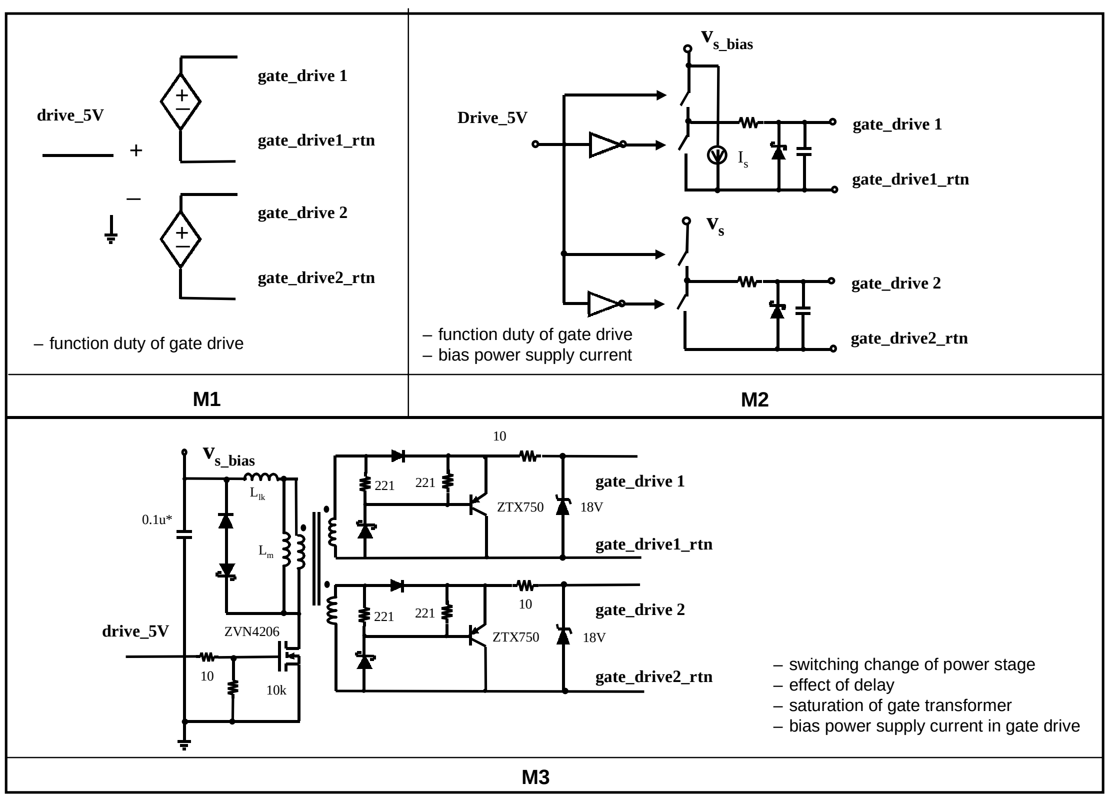


Fig. 3.36 Multi-level modeling of the gate drive block.

3.3.4 Control circuit

The control block has four levels, as shown in Fig. 3.37. M1 has a fixed duty cycle signal, M2 has a control loop function but no start-up characteristics, and M3 is a detailed model with start-up characteristics. An additional block to represent the minimum duty cycle and maximum duty cycle in a real circuit is implemented in the control block as shown in Fig. 3.38.

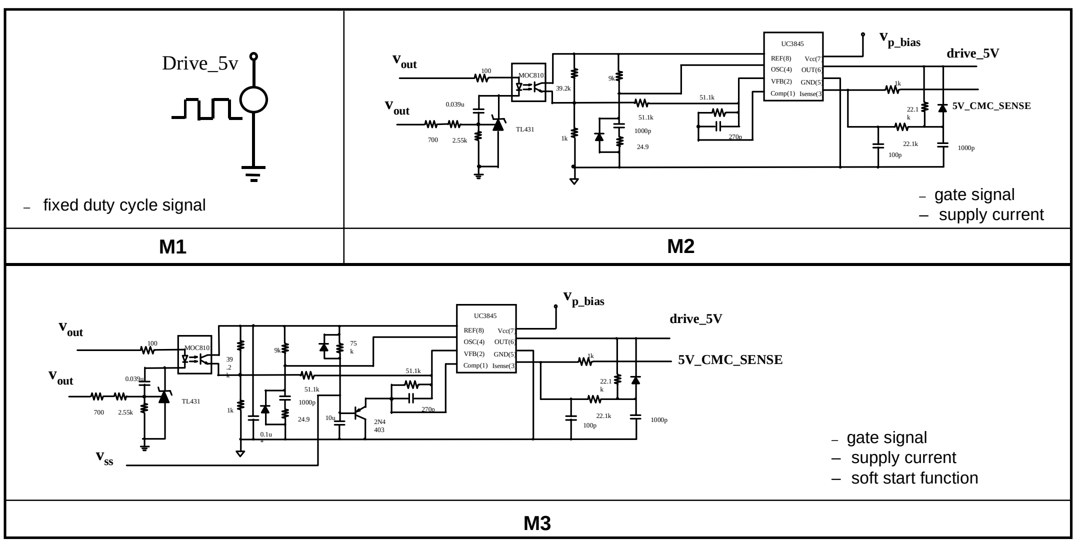


Fig. 3.37 Multi-level modeling of the control block.

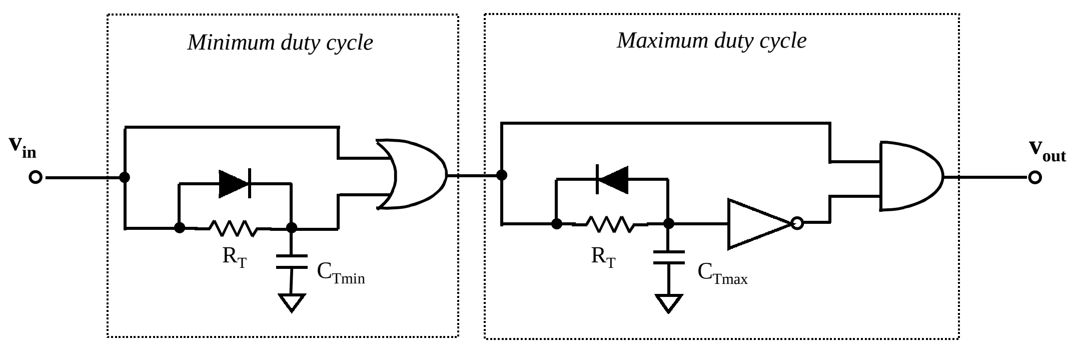


Fig. 3.38 Implementation of minimum duty cycle and maximum duty cycle in the control block.

3.3.5 Protection and monitoring circuits

This type of circuit includes over-voltage, over-current, under-voltage, over-temperature, and enable circuits. Only a detailed model is needed in the simulation.

3.3.6 Bias power supply

A bias power supply has three levels, as shown in Fig. 3.39. M1 is used for the ideal supply voltage, M2 is a detailed model without leakage inductance of the transformer, and M3 is a detailed model with leakage inductance of the transformer.

How to select different models in different tests will be discussed in the next chapter.

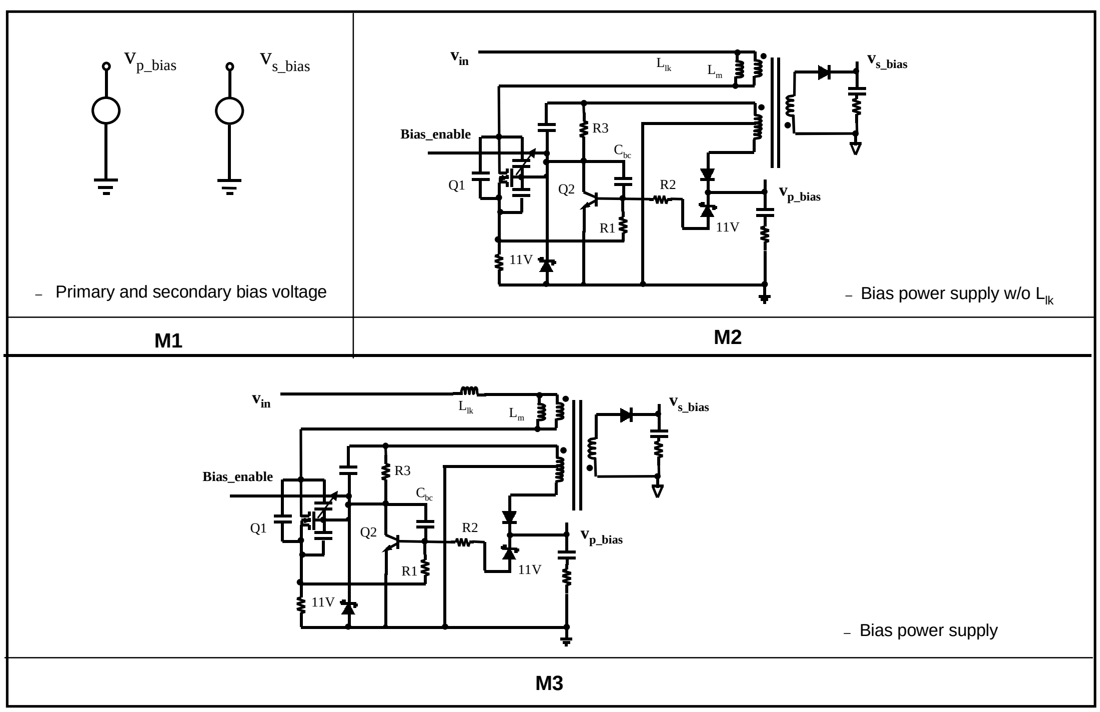


Fig. 3.39 Multi-level modeling of the bias power supply block.

3.4 Summary

The complexity and accuracy of models used in the virtual prototype test will affect the simulation speed and the accuracy of the system behavior directly. This chapter introduces the principle to make models for the virtual prototype test and illustrates a modeling approach to implement multi-level models of the power supply system. Two types of models have been discussed: the circuit component models and block models.

4. USING VIRTUAL PROTOTYPE FOR DESIGN, VERIFICATION, AND TESTING

4.1 Introduction

4.1.1 Overview of 5 V forward converter power supply system

This chapter demonstrates the proposed virtual prototype DVT procedure by simulating a 5 V, 150 W power supply system. The power supply system comprised of multiple dc/dc converters operating at different switching frequencies is illustrated in Fig. 4.1. The main power supply includes a power stage, control circuit, gate drive, over-voltage protection, over-current protection, and under-voltage detector circuits. A bias power supply, which provides the internal bias voltages needed by the main power supply, includes a bias circuit and bias enable circuit.

The power supply block diagram is the same as what we have discussed in previous chapters. Although the main power supply uses a forward converter with an active-clamp reset circuit instead of a two-transistor forward converter circuit, the previous discussion is general enough to apply to this circuit. The forward converter with active-clamp reset circuit is selected here because the circuit has many interesting design issues and challenges that we can explore in the process of the virtual prototype test. The peak current mode control is used for the forward converter circuit.

The bias power supply uses a self-oscillating flyback converter with two outputs. This example is chosen because of the unusually high degree of interaction between these two switching power supplies. Problems associated with interactions of this type are very difficult to predict at the paper design stage. A simulation capability that enables the designer to detect these problems before building a first prototype would be very valuable in reducing the design cycle time.

The circuit specification of the power supply system is: input voltage 36 - 72 V, output voltage 5 V, main power supply switching frequency 500 kHz, output power 150 W. The bias power supply is designed to operate at megahertz.

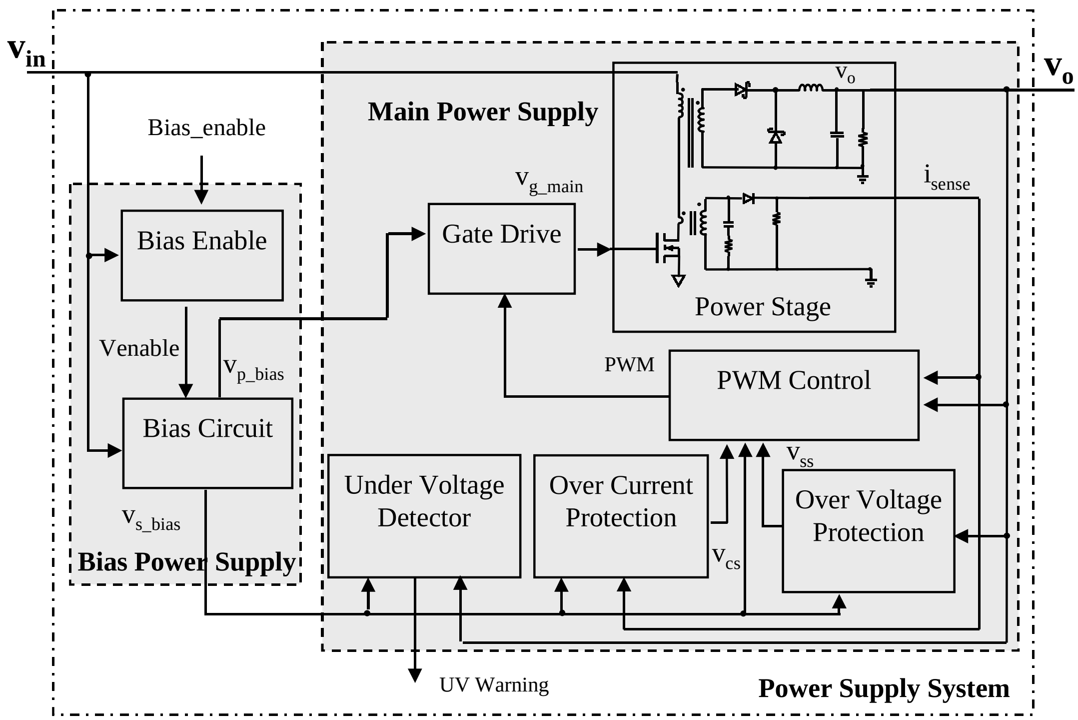


Fig. 4.1. Circuit block diagram of a 5 V power supply system.

4.1.2 Principle of operation of forward converter with active-clamp reset circuit

The performance of the forward converter is strongly dependent on the transformer-reset method. Generally, it has been established that the active-clamp reset approach offers a better performance than the other reset approaches because it allows the operation of the converter with a maximum duty cycle well above 50%, with a minimum stress on the semiconductor components [55]. In fact, due to a large maximum duty cycle, the turns ratio of the transformer can be increased, which decreases the conduction loss on the primary side and allows the selection of the secondary-side rectifiers with a lower breakdown rating, and, consequently, a lower forward-voltage drop. In addition, the active-clamp-reset method recycles the magnetizing energy of the core, as opposed to the other methods (the RCD-clamp method, for example) that dissipate this energy. As a result, the conversion efficiency of the forward converter with the active-clamp reset can be higher than that of the same topology with the other reset schemes. Also, the active-clamp reset approach results in the optimal use of the transformer core, since the core is excited symmetrically in the first and third quadrants of the B-H plane. However, the active-clamp-reset method requires an extra switch with the associated drive and a resonant capacitor (i.e. it increases the complexity and the cost of the power stage). Nevertheless, this method seems indispensable in achieving the optimum performance of the forward-converter topology.

The forward converter power-stage with the active-clamp reset is shown in Fig. 4.2. The reset circuit consists of auxiliary switch S_2 and clamp-capacitor C_c. To simplify the analysis of the operation, it is assumed that the inductance of output-filter inductor L_f is large so that the output filter can be represented by constant-current source I_o. In addition, it is assumed that all semiconductors are ideal. It should be noted that the transformer is modeled as a parallel connection of magnetizing inductance Lm and the ideal transformer with the turns-ratio $n = \frac{N_p}{N_s}$ as shown in Fig. 4.3. To further facilitate the explanation of the operation, Fig. 4.3 shows the topological stages of the simplified circuit during a switching cycle, whereas Fig. 4.4 shows the essential waveforms.

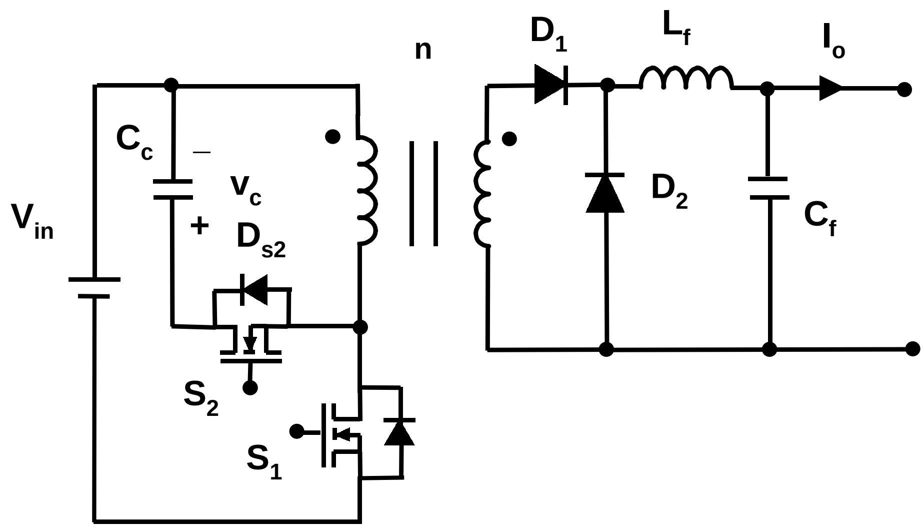
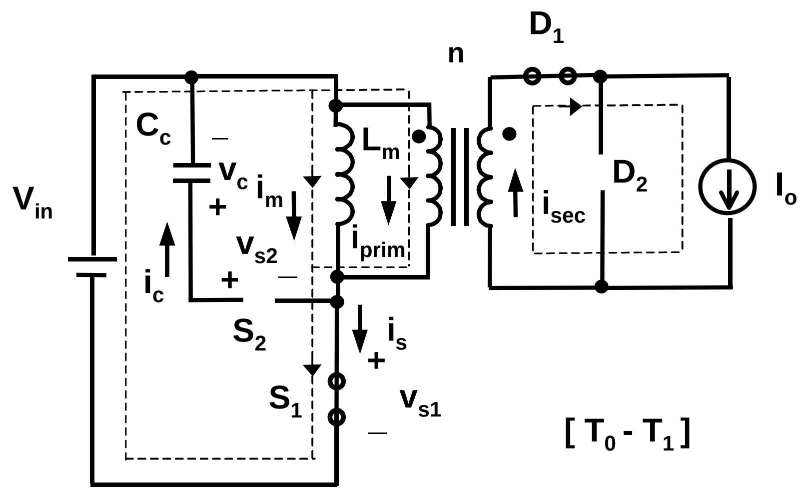
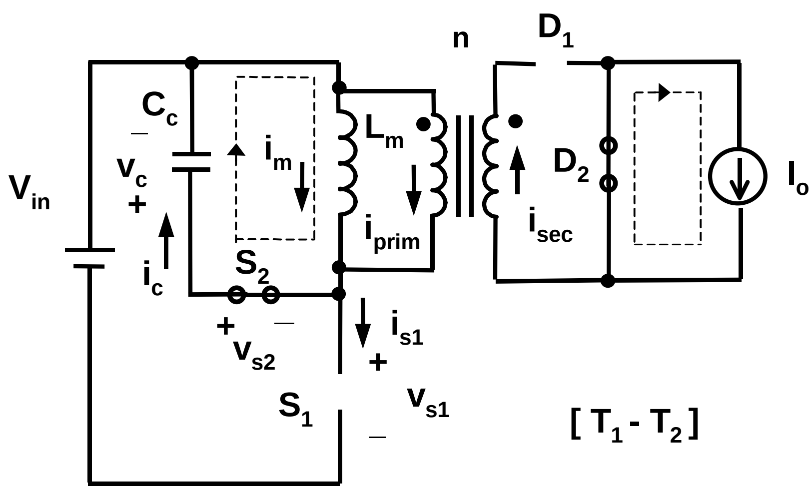


Fig. 4.2. Forward converter power-stage with the active-clamp reset.



(a)



(b)

Fig. 4.3. Circuit operation diagrams of the simplified active-clamp forward converter. (a) [T_0-T_1] interval. (b) [T_1-T_2] interval.

Since, in this analysis, ideal switches with zero switching times are assumed, a complementary gate-drive signals without a dead time are used as shown in Fig. 4.4. Because of the true complementary gate-drives, the circuit has only two topological stages as shown in Fig. 4.3.

During the interval [T_0-T_1], when main switch S_1 is on, the corresponding topological stage is shown in Fig. 4.3(a). During this stage, output current I_o flows through the secondary winding inducing primary current, $i_{prim} = \frac{I_o}{n}$. At the same time, because a constant positive input voltage V_{in} is connected across the primary of the transformer, magnetizing current i_m increases with a constant slope. During the on time of the switch, switch current i_{s1} is given by the sum of primary current i_{prim} and magnetizing current $i_{m,}$ as shown in Fig. 4.4.

When main switch S_1 is turned off at $t = T_1$, output current is instantaneously commutated from rectifier D_1 to freewheeling rectifier D_2, because the leakage inductance of the transformer is neglected, as shown in Fig. 4.3 (b). At the same time, magnetizing current i_m is commutated from main switch S_1 to the anti-parallel diode of the auxiliary switch S_2. Since S_2 is turned on at $t = T_1$ while its anti-parallel diode is conducting (i.e. while the voltage across it is zero), switch S_2 is turned on under a zero-voltage-switching (ZVS) condition. There is no additional turn-on loss at this instant. Due to a negative voltage v_c across the primary winding of the transformer, i_m decreases. If clamp voltage v_c is assumed constant (i.e. if the clamp capacitor capacitance is large), the down-slope of i_m is constant as shown in Fig. 4.4.

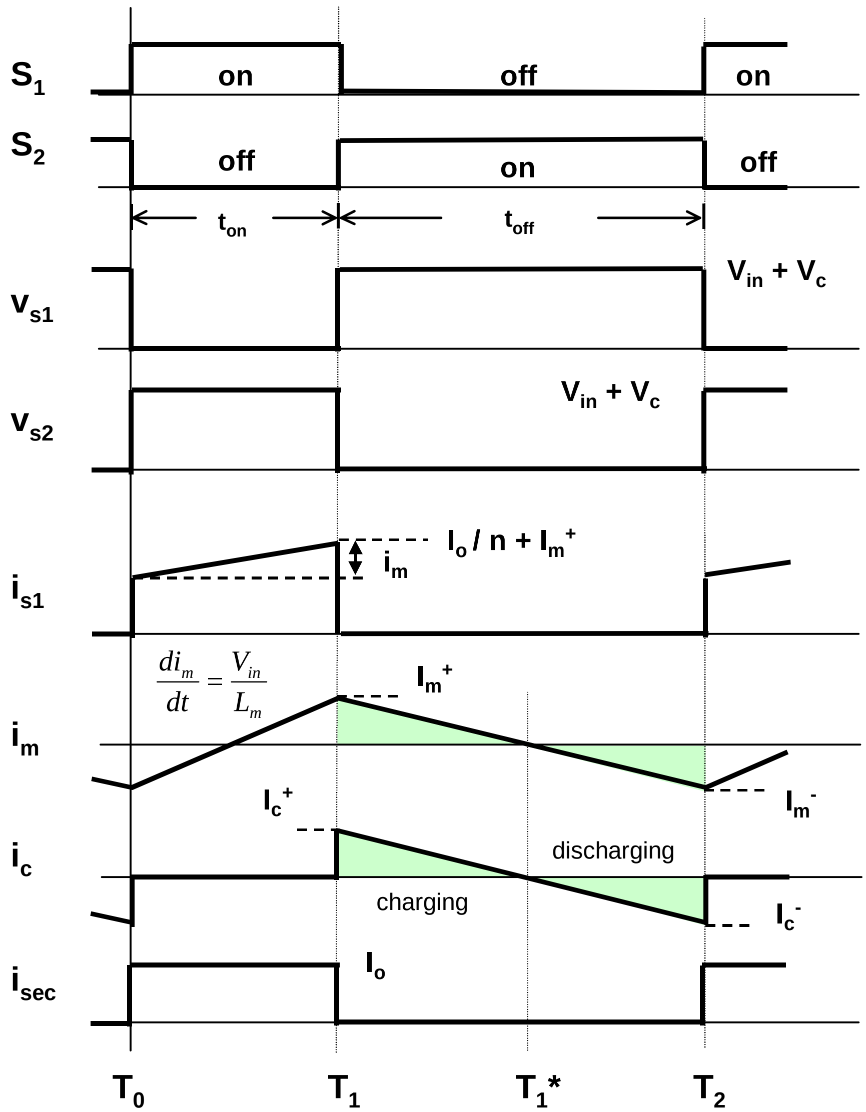


Fig. 4.4. Key waveforms of the circuit operation of the simplified forward converter with the active-clamp reset.

After i_m reaches zero at $t = T_1^*$, it continues to flow in the negative direction through the transistor (channel) of the closed auxiliary switch S_2. This topological stage ends when auxiliary switch S_2 is turned off and main switch S_1 is turned on at $t = T_2$, initiating a new switching cycle.

From the flux-balance requirement of the transformer core, it follows that

$$V_{in} \cdot t_{on} = V_c \cdot t_{off} \tag{4.1}$$

Clamp voltage V_c is given by

$$V_c = \frac{D}{1 - D} \cdot V_{in} \tag{4.2}$$

where, t_{on} is the on time of main switch S_1, t_{off} is the off time of S_1, $D = \frac{t_{on}}{T_s}$ is the duty cycle of S_1, and T_s is the switching period.

From the charge-balance requirement of the clamp capacitor, it follows that

$$I_c^+ = I_c^- \tag{4.3}$$

where $I_c^+ = i_c(t_1)$ and $I_c^- = i_c(t_2)$, as shown in Fig. 4.4.

Since, during the off-time, main switch S_1 is off, $i_c = i_m$, it also follows that

$$I_m^+ = I_m^- \tag{4.4}$$

where $I_m^+ = i_m(t_1)$ and $I_m^- = i_m(t_2)$.

Therefore, the dc component of the magnetizing current of the circuit in Fig. 4.2 is equal to zero.

4.1.3 Principle of operation of bias power supply

Fig. 4.5 shows the bias power supply circuit diagram. The bias power supply is a self-oscillating flyback converter with two outputs. One of the outputs provides the power system primary-side bias voltage and the other provides the power system secondary-side bias voltage. Since the converter operates as a self-oscillating circuit, it has a variable switching frequency, which is a function of the input voltage and the load.

The self-oscillating flyback converter of Fig. 4.5 operates at the critical boundary between the continuous and discontinuous conduction modes. Fig. 4.6 shows the ideal operating waveforms when the effect of the charging currents of the gate drive circuit is ignored. During the on time of the power switch Q1, the primary magnetizing current i_m increases linearly. The initiation of the turn-off signal to the power switch Q1 is controlled by a transistor, Q2. For most of the conversion cycle, the voltage at the base of Q2 is less than that required to turn on Q2. Under these conditions, the base voltage of Q2 is the weighted average (by the ratio of R1 and R2) of the voltage v_{R4} and v_{err}. The FET Q1 turns off when the transistor Q2 turns on and pulls the gate signal below the threshold voltage. At a given operating point, the error voltage v_{err} essentially is fixed. Consequently, the power switch Q1 will turn off when the current sensor voltage v_{R4} rises high enough so that the voltage at the base of Q2 is sufficiently forward biased so as to begin to discharge the gate of Q1. The next turn-on action of Q1 will occur when the magnetizing current reaches zero and the primary side voltage of the transformer collapses towards zero. This causes a regenerative signal to be applied to the gate of Q1 through the winding n3 of the bias supply transformer. This signal pulls the gate voltage high to once again turn on the power switch Q1.

The bias converter is regulated by feedback from the primary-side bias voltage v_{p_bias}. As the primary bias voltage v_{p_bias} increases, the error voltage v_{err} also increases. A larger voltage across v_{err} will increase the voltage across the base of transistor Q2.

This will cause Q2 to turn on with a smaller peak current sensor voltage, v_{R4}. Since the magnetizing current will reach a lower current level with a smaller current sensor voltage, less energy is transferred to the output. The output voltage will be reduced and regulated to the desired voltage.

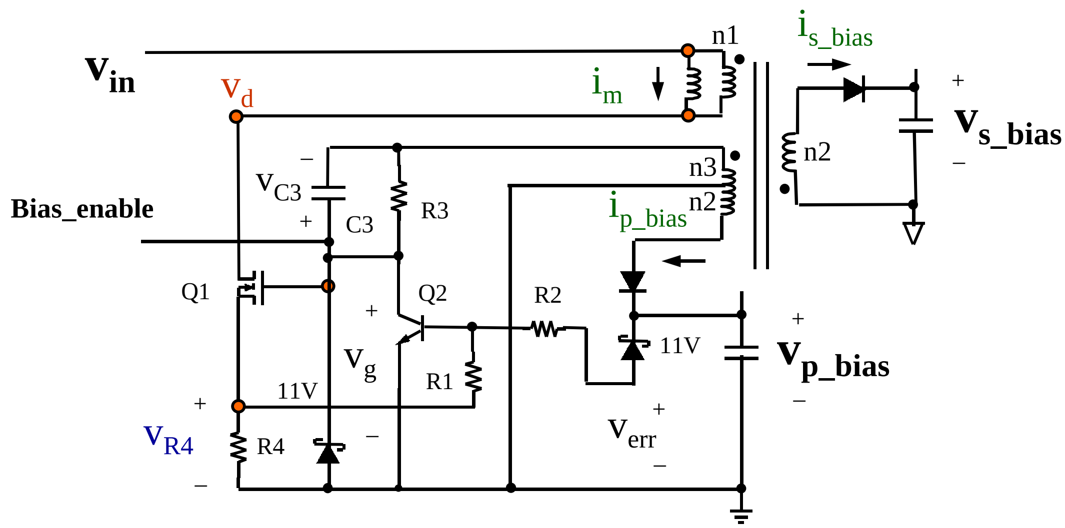


Fig. 4.5. Simplified circuit diagram of the self-oscillating flyback bias power supply.

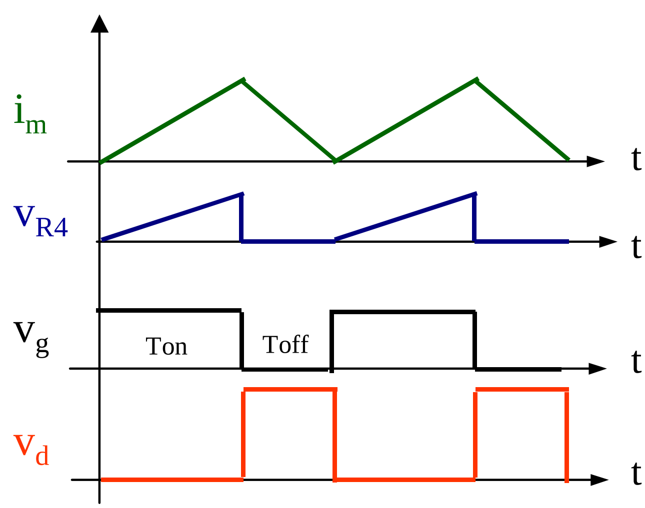


Fig. 4.6. Operation waveforms of the flyback converter in the ideal operation.

4.1.4 Overview of the virtual prototype DVT process

4.1.4.1 Multi-level modeling of main power stage

Fig. 4.7 is the power stage circuit diagram of the 5 V forward converter with an active-clamp reset circuit. The simulation schematics with different complexity levels can be determined by identifying the circuit behavior required in each test. The detail of each level will be discussed in following sections. Table 4.1 is the summary of the component level of the power stage block for the virtual prototype DVT with the component levels of the circuit defined in chapter 3. From Table 4.1 we see that there are a total of seven different models of the power stage used in the simulation and the number of model levels varies on different applications. The model level of the power stage is on a simple to complex order.

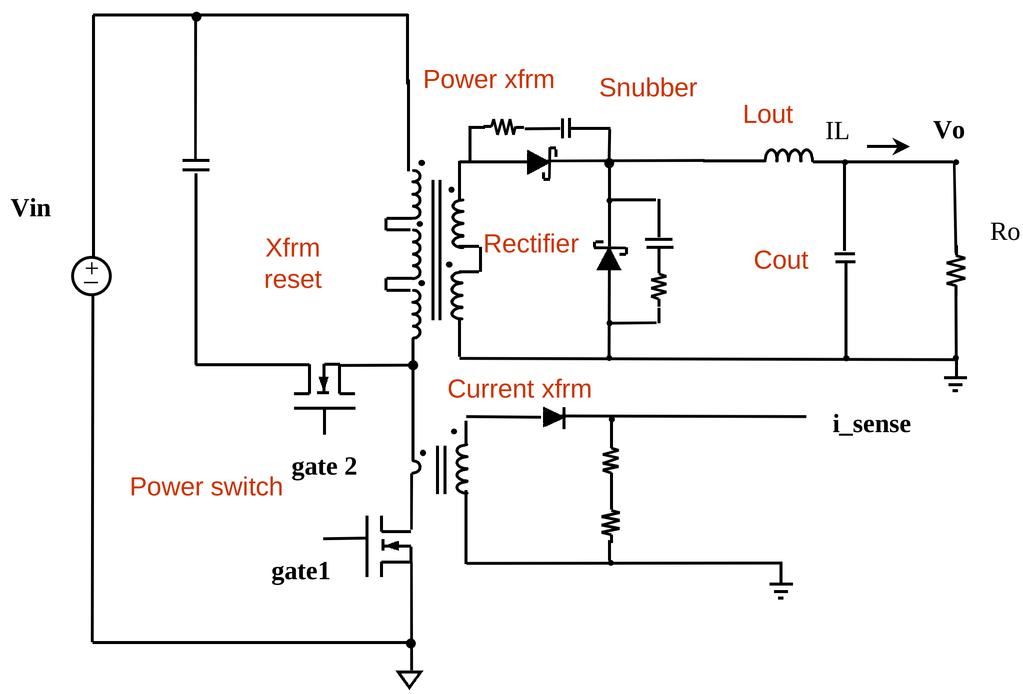


Fig. 4.7. The power stage circuit diagram of the 5 V forward converter with active-clamp reset circuit.

Table 4.1. Summary of the component levels of the power stage block for the virtual prototype test.

		Component level							
Model number	Test type example	Power switch	Power xfrm	Current xfrm	Rectifier	Lout	Cout	Reset	Snubber
M1	System interaction	1	1	1	1	1	2	N	N
M2	Load regulation, Stability analysis	2	2	1	1	1	2	Y	N
M3	Line transient, Main power supply start-up	2	3	1	1	1	2	Y	N
M4	Load transient	2	3	1	1	1	3	Y	N
M5	Control test	2	2	4	1	1	2	Y	N
M6	Power stage test	2	2	2	1	1	2	Y	Y
M7	Loss analysis	4	4	2	2	2	2	Y	Y

4.1.4.2 Multi-level simulation of power supply system

The virtual prototype DVT procedure of the 5 V forward converter is the same as in chapter 2, which is redrawn in Fig. 4.8. The whole procedure will be discussed through six levels in this chapter as shown in Fig. 4.8. After defining the model numbers of the power stage, we can also summarize the complexity levels of the simulation schematics. The definitions of other function block levels are similar to the ones in chapter 3. Table 4.2 is the summary of a multi-level simulation test table for all the virtual prototype tests. We will discuss each test in this chapter.

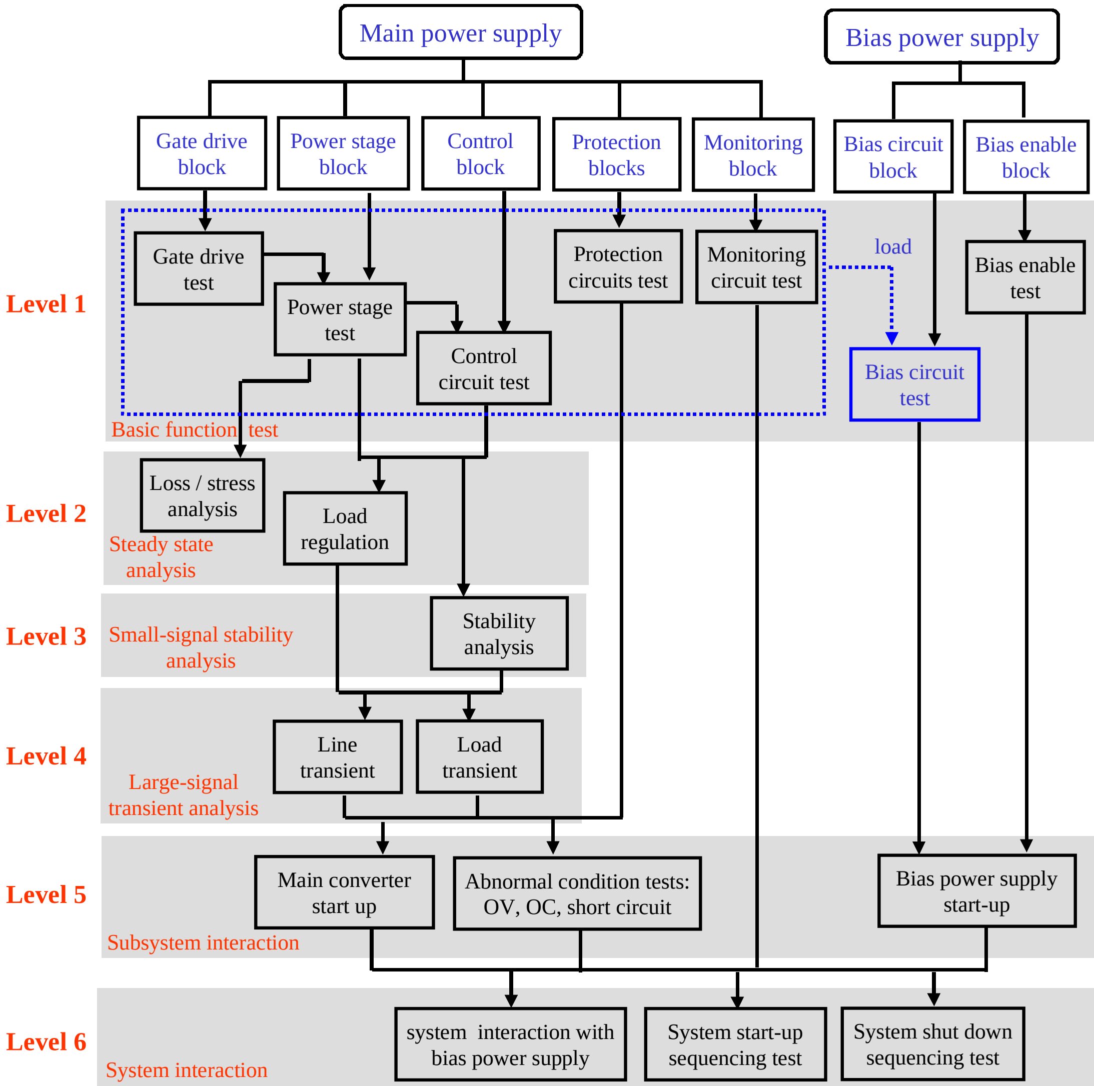


Fig. 4.8. Virtual prototype DVT flow chart.

Table 4.2. Summary of the multi-level simulation test table of the virtual prototype test.

simulation level	test name	power stage	gate drive	pwm control	OC	OV	UV	bias enable	bias
	(total modle levles)	7	3	3	1	1	1	1	3
Level 1	gate drive test		3	1				1	
	power stage test	6	1	1					
	control circuit test	5	1	3				1	
	protection circuits test:								
	OV circuit test				1			1	
	OC circuit test					1		1	
	monitoring circuits test: UV circuit test						1	1	
	bias block test:								
	bias power supply stress							3	
	bias power supply load							2	
	regulation							2	
	bias line transient							2	
	enable circuit test								1
Level 2	main converter loss	7	2	1				1	
	load regulation	2	1	2				1	
Level 3	stability analysis	2	1	2				1	
Level 4	line transient	3	1	2				1	
	load transient	4	1	2				1	
Level 5	main coverter start up	3	1	3	1	1		1	
	abnormal test:								
	OV test	2	1	2	1	1		1	
	OC test	2	1	2	1	1		1	
	short circuti test	3	1	2	1	1		1	
Level 6	main and bias converter interaction	1	2	3				3	
	system startup sequence	1	1	3	1	1	1	2	1
	system shut down sequence	1	1	3	1	1	1	2	1

4.2 Level 1 -- basic function test

The first level of simulation is the basic function test. The main purpose of the basic function test is to verify the fundamental operations of each individual block, so the problems related to single blocks can be caught before a more complex or time-consuming test in later levels.

4.2.1 Main power supply basic function test

Because the tests in this level are relatively simple, we will not go through each test in detail. The complexity level of the test circuit, simulation CPU time, and the test condition are summarized in the appendix.

4.2.1.1 Gate drive test

Normally, no individual test of the gate drive is used in a hardware test. However, gate drive tests can be added in the virtual prototype test to search for any possible design problems through all operating points. A periodic pulse signal is applied to replace the control circuit, and two capacitors with Cgs value of MOSFET in the main power stage are added to the outputs of the gate drive circuit. A detail transformer model (M4) is used. A series of gate drive tests are performed by varying the duty cycle from minimum to maximum range.

The gate drive test is to verify the basic gate drive function, check the transformer saturation, record the delay of the gate drive signal, and record the average bias current needed for the gate drive block.

4.2.1.2 Main power stage test

The main task in the main power stage test is to verify the forward converter operation and the reset of the main transformer (i.e. the operation of active-clamp reset circuit). The component level of the power stage block is M6, as shown in Table 4.1.

Although a simple rectifier model is used in this test, the snubber is included in the simulation to check the side-effect of the design. The input voltage and duty cycle are varied as a set to keep the output voltage at roughly 5 V. The ripple of output voltage is verified to adjust the output filter design. The final condition of all the state variables are saved for loss analysis in the next level simulation.

4.2.1.3 Control circuit test

The control circuit test is to verify the control circuit operation, switching frequency, start-up circuit operation, the maximum duty cycle, the minimum duty cycle, and the saturation or current bias of the current sense transformer. The component level of the power stage block is M5, as shown in Table 4.1. The bias current needed in the control block is recorded in the test. The final state variable values can be used as the initial condition for the load regulation test.

4.2.1.4 Protection and monitoring blocks test

The protection and monitoring block tests are very straightforward. The tasks are to verify the basic operation of circuits, find threshold voltages, and record the bias current needed in the test.

4.2.2 Bias power supply basic function test

4.2.2.1 Bias circuit test

The bias circuit is a unique power supply, which differs from the main power supply. The major function of the bias circuit is to provide the bias voltage for the main power supply system. The test is to verify that the bias can guarantee the normal operation of the system under different conditions. No restrictive specifications are provided from a customer specification point of view. Although it also has tests similar to the main power supply (e.g. load regulation, loss analysis, and transient response), the tests are focused mainly on finding possible system interactions issues. The routine tests are trivial and not going to be discussed here; the circuit operations related to interaction issues are discussed later in the system interaction section.

4.2.2.2 Bias enable block test

Similar to protection circuits, the bias enable test is used to verify the basic operation of the circuit and find the threshold voltages of the enable signals.

4.2.3 Summary of the basic function test

Table 4.3 is the summary of test conditions and CPU times for the basic function test of the main power supply and Table 4.4 is the summary of test conditions and CPU times for the basic function test of the bias power supply. The test conditions cover the proposed operating points which need to be tested. More test points can be added between each point listed in the table.

In the rest of the dissertation, the notations of the table are:

Vmin: minimum input voltage of the whole system operation (30 V in the example)

Vl: minimum normal input voltage of specification (32 V)

Vnorm: nominal input voltage

Vh: highest normal input voltage (72 V)

Vmax: highest operation voltage (80 V)

Imin: minimum load of the whole system operation (0 A)

Idcm: load in dcm operation (1 A)

Iccm: load in ccm operation but closed to dcm boundary (3 A)

25%*Ifull: 25% full load (7.5 A)

In: nominal load (15 A)

Ifull: full load (30 A)

Imax: maximum load (38 A)

Ib_norm: bias current at normal condition

Ib_max: maximum bias current

Ib_min: minimum bias current

The duty cycle notation is similar to input voltage.

Vsense low to high (2): sense voltage from low to high and high to low (extend to similar notations in the table).

Table 4.3. Summary of test conditions and CPU times for the basic function test of the main power supply

Test type		Test condition			Simu time (s)	Total number of tests	CPU time (min)
		Vin	Io	Other			
Gate drive		--	--	Dmin - Dmax (7)	10 u	7	0.14
Power stage		Vmin, Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh,Vmax (7)	Imin, Idcm, 25%*Ifull, 50%*Ifull, 75%*Ifull, Ifull, Imax (7)	Duty cycle: corresponding to Vin (7)	100 u	49	4.9
Control		Same as above	Same as above	--	5 m	49	49
Protection circutis	OV	--	--	Vsense low - high (2)	1 m	2	0.06
	OC	--	--	Isense low - high (2)	1 m	2	0.06
Monitoring circuit: UV		--	--	Vsense low - high (2)	1 m	2	0.06
Total		--	--	--	--	111	54.48

Table 4.4. Summary of test conditions and CPU times for the basic function test of the bias power supply

Test type		Test condition			Simu time (s)	Total number of tests	CPU time (min)
		Vin	Io	Other			
Bias circuit	Load regulation	Vmin, Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh,Vmax (7)	Imin	Ib_norm, Ib_max	2 m	14	9.8
			In	Ib_norm, Ib_max	50 u	14	0.98
	Stress analysis	Vmin, Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh,Vmax (7)	Imin	Ib_norm, Ib_max	2 m	14	19.6
			In	Ib_norm, Ib_max	50 u	14	1.96
	Line transient	Vl toVnorm (2), Vnorm to Vh (2), Vl to Vh (2)	Imin	Ib_norm, Ib_max	3 m	12	12
			In	Ib_norm, Ib_max	1 m	12	9
	Load transient	Vl, Vnorm, Vh	--	Ib_min to Ib_norm (2), Ib_n to Ib_max (2), Ib_min to Ib_max (2)	1 m	18	13.5
Total		--	--	--	--	98	66.84

4.3 Level 2 -- steady state analysis

4.3.1 Loss/stress analysis

In a hardware test, the circuit efficiency is obtained by measuring the input power and output power; the power loss distribution on each component cannot be obtained from the measurement. The device overstresses are not known until the circuit board is burned out. In the virtual prototype test, the power loss of each component can be calculated through simulation and the maximum voltage and current of each component are compared with the device rating, so the stress problem in the design can be caught before the first prototyping. The transformer magnetizing current is also inspected to check the transformer saturation, magnetic bias, and flux walking.

The component level of the power stage block is M7, as shown in Table 4.1. The loss/stress analysis is to calculate the loss distributed in the main devices, estimate the efficiency, verify snubber design, check transformer saturation and steady state stresses of components, and measure the output voltage ripple. Similar to the example in chapter 2, a simplified gate drive (M2) is used to provide the gate resistance, and a pulse signal is used to replace the control circuit (M1). The model levels of the function blocks for loss analysis is shown in Table 4.2. The circuit initial conditions are obtained from the power stage block test in order to reduce the simulation time.

4.3.1.1 Loss and stress curves

The loss/stress analysis uses the parameter values of the circuit components according to worst cases (e.g. on-resistance of the device uses the values at 125^{o}C in the example). The real circuit is expected to have less losses in devices and a higher efficiency.

The efficiency of the main power converter under different load is shown in Fig. 4.9. The dotted lines are measurement and the solid lines are simulation results. The loss curves of major semiconductor devices over the whole operation area with different line and load conditions are shown in Fig. 4.10. Fig. 4.10(a) is the power loss of main switches. Fig. 4.10(b) is the power loss of the auxiliary switch. Fig. 4.10(c) is the power loss of the forward schottky diode (rectifier 1). Fig. 4.10(d) is the power loss of the free wheeling schottky diode (rectifier 2).

The maximum voltage and current of the major semiconductor devices are shown in Fig. 4.11. Fig. 4.11 compares the device voltage and current stresses to device voltage and current ratings. The stress values of the devices are obtained by simulation the circuit under a series of line and load conditions. In the figure, the maximum currents of the main switch and auxiliary switch refer to rms currents, and the maximum currents of the rectifiers refer to average currents.

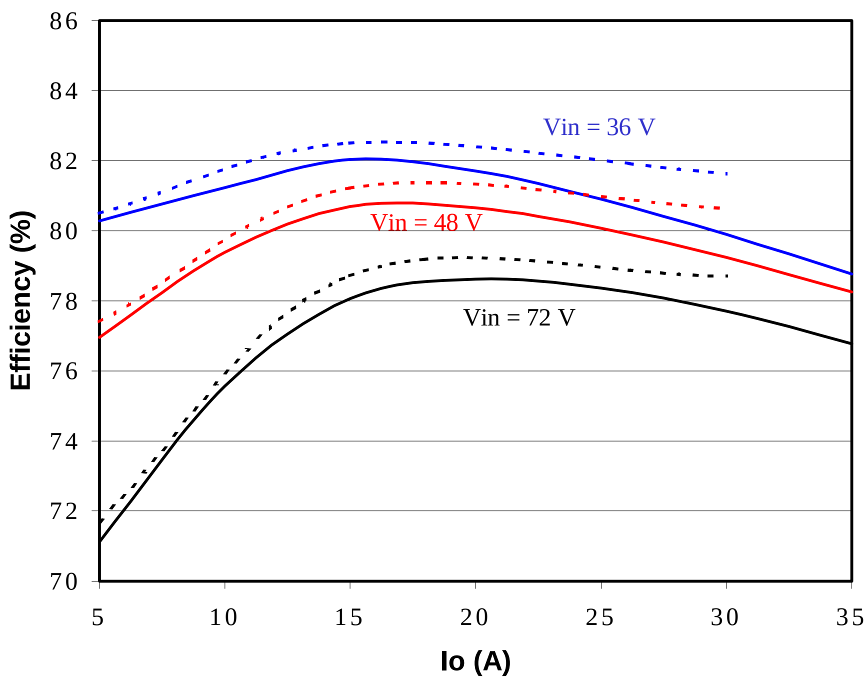


Fig. 4.9. The efficiency of the main power converter under different line and load conditions. Solid lines are simulations and dotted lines are measurements.

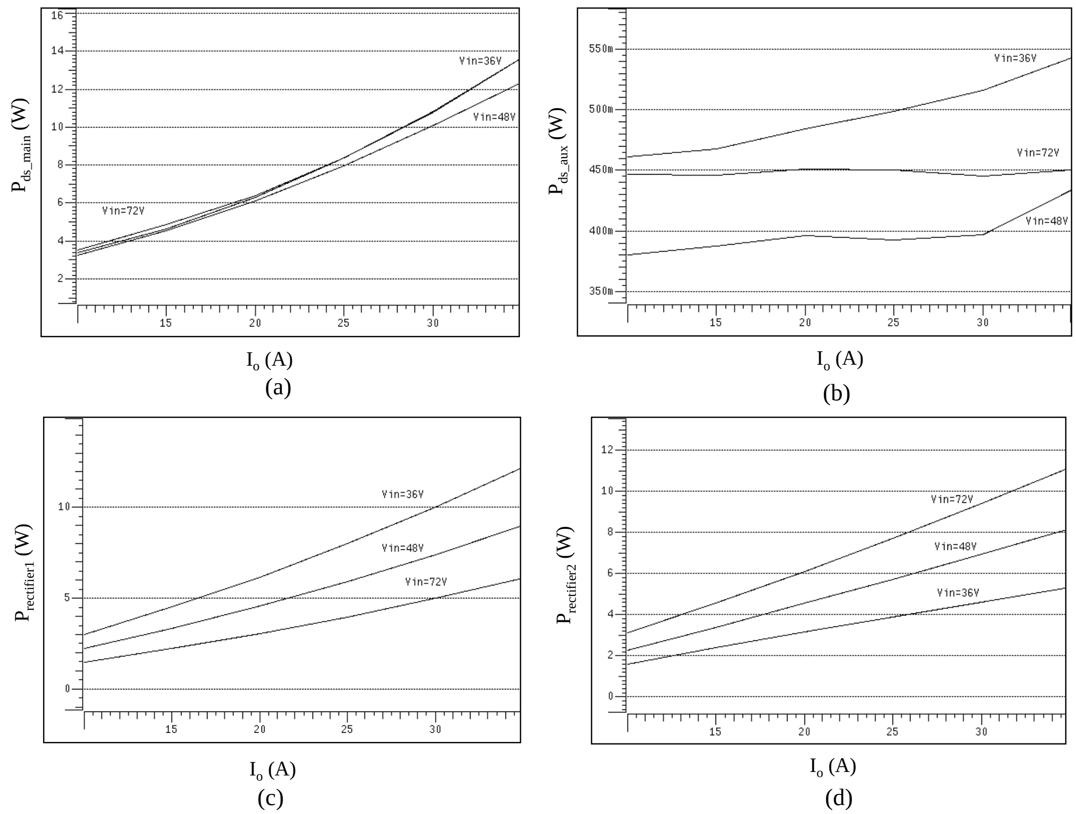


Fig. 4.10 The loss curves of major semiconductor devices. (a) main switches. (b) auxiliary switch. (c) the forward schottky diode (rectifier 1). (d) the free wheeling schottky diode (rectifier 2).

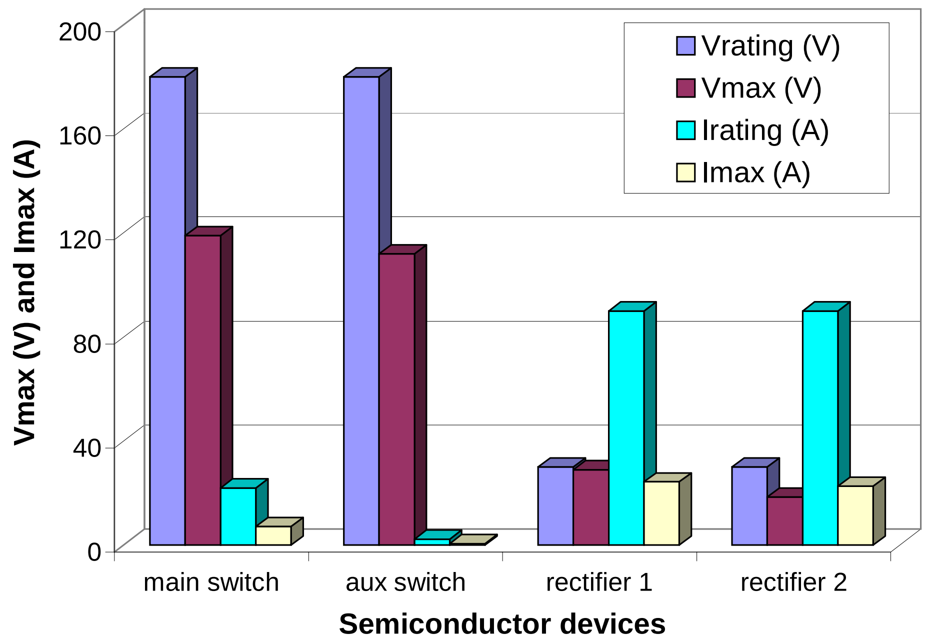


Fig. 4.11. Comparison of device voltage and current stresses to device voltage and current ratings. In the figure, the maximum currents of the main switch and auxiliary switch refer to rms currents, and the maximum currents of the rectifiers refer to average currents.

4.3.1.2 DC bias of the magnetizing current in transformer

In loss/stress analysis, the transformer design is verified by measuring the magnetizing current. Fig. 4.12 shows the average magnetizing current of the power transformer under whole-circuit operating conditions. The shaded area shows that the circuit loses ZVT operation of the active-clamp switching due to the dc bias of the magnetizing current of the transformer at heavy load. The circuit waveforms at Vin = 48 V, Io = 30 A are shown in Fig. 4.13.

It is worth mentioning that the dc bias of the magnetizing does not appear in the power stage block test, so the dc bias is related to the additional parasitic parameters in the loss analysis. By comparing the different complexities of the power stage model in

M6 and M7 of Table 4.1, the leakage inductance of the transformer and the device parasitic capacitance are two possible parasitic parameters that inducing the dc bias. In the next chapter, we will show from the circuit analysis that the dc bias of the magnetizing current is caused by the leakage inductance of the transformer and the parasitic capacitances of MOSFET, the transformer, and diodes.

The problem could be fixed by increasing the core size. A better solution is to redesign the circuit. After further study of the circuit design in the next two chapters, we see that the problem can be fixed by reducing the leakage inductance of the transformer, as shown in Fig. 4.14. The detail design procedure is discussed in later chapters.

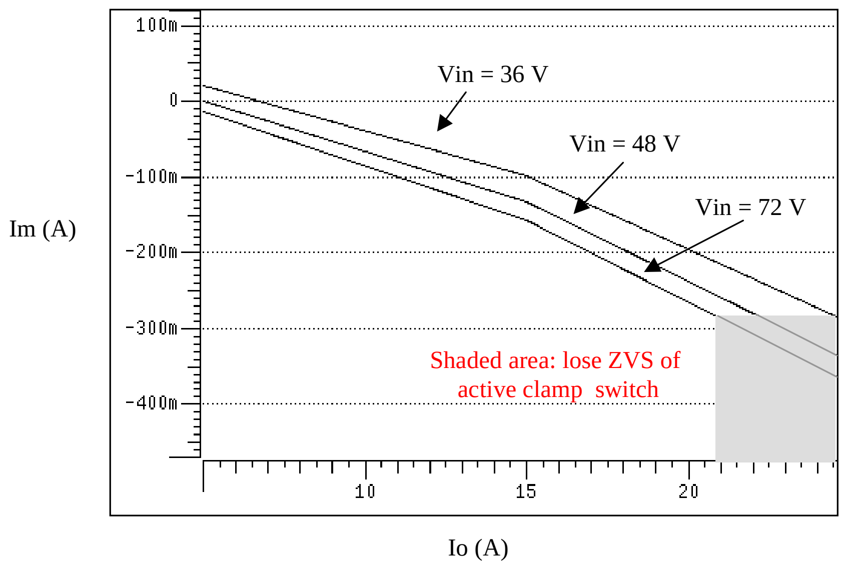


Fig. 4.12. Average magnetizing current vs. lines and loads. It shows that when the circuit operates in the shaded area, ZVS of the active clamp switch is lost due to a large biased negative magnetizing current.

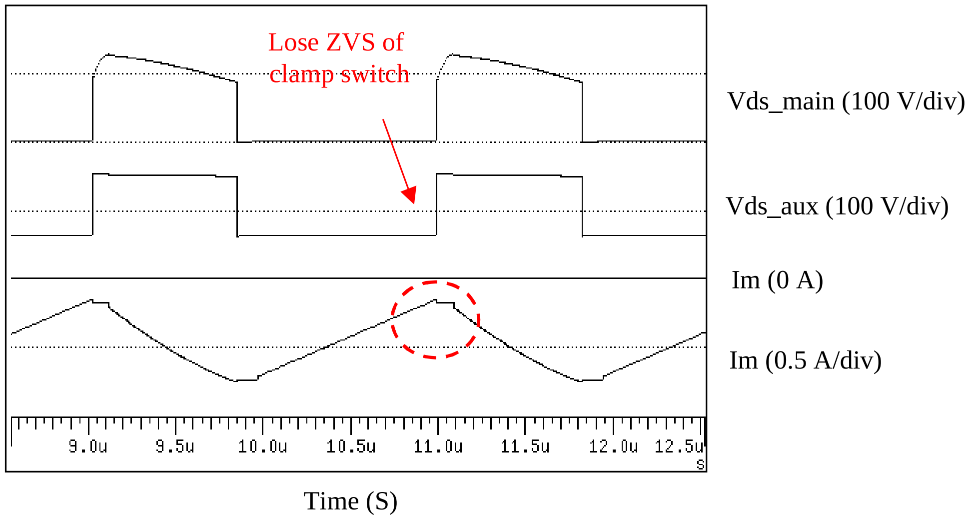


Fig. 4.13. There is a dc bias of the magnetizing current in a steady state operation. At heavy load, the dc bias of the magnetizing current is always negative. The circuit loses ZVS of the active clamp switch.

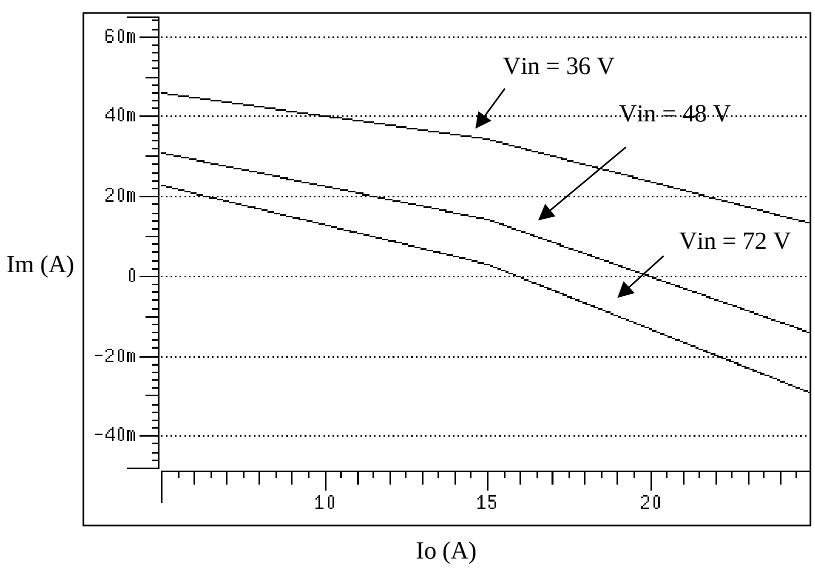


Fig. 4.14. The problem is fixed by redesigning the transformer into a smaller leakage inductance.

4.3.2 Load regulation

The component level of the power stage block is M2, as shown in Table 4.1. A simple gate drive circuit (M1) and a control circuit without start-up (M2) are used in the simulation. The circuit initial conditions can be obtained from the control block to reduce the simulation time.

4.3.2.1 Verify circuit behavior with different loads

In order to get accurate behavior for the system, the virtual prototype should present the right circuit behavior over different loads. The steady state waveforms of the main switch drain to source voltage and output voltage at Vin = 48 V, Io = 15 A is show in Fig. 4.15. Fig. 4.15(a) is the simulation result, and Fig. 4.15(b) is the measurement. The spike of output voltage is due to the ESL of the output capacitor. Since the main task of the load regulation is to measure the average output voltage, and since the ESL will not affect the average value of the output voltage, the ESL is not included in the simulation. It is relatively simple to get an accurate result for nominal operation conditions, but when the circuit operates at no load or light load conditions, some parameters of the models are critical for an accurate waveform.

Fig. 4.16 shows the simulation waveform at a light load condition when no delay of the control block is modeled in the virtual prototype. The circuit has a small duty cycle in each switching cycle and shows a similar behavior as in a heavy load condition. Fig. 4.17 shows the waveform of the measurement. As seen in Fig. 4.17, the control circuit skips several switching cycles due to the delay of the controller chip and MOSFET (about 300 nS) which introduces a minimum duty cycle. After implementing a minimum duty cycle block in the control circuit as we discussed in the previous chapter, the simulation shows a similar behavior as in the measurement. The simulation result is shown in Fig. 4.18(a). The repeated cycle lengh can be adjusted by changing the leakage current of the rectifier diodes as shown in Fig. 4.18(b). It also shows that the leakage current of the rectifier diodes will affect the system behavior in a light load condition.

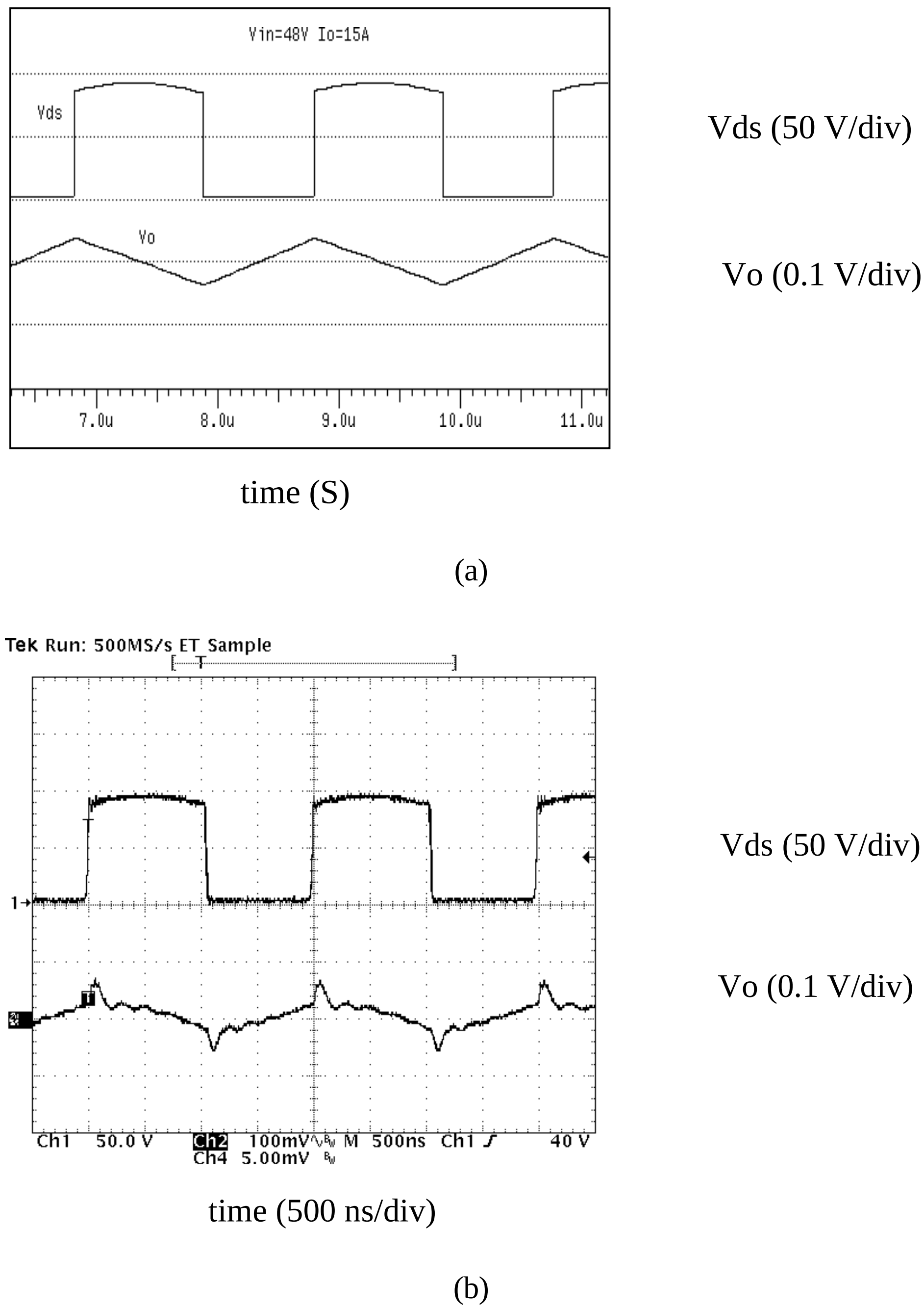


Fig. 4.15 Steady state waveform at Vin = 48 V, Io = 15 A. (a) simulation. (b) measurement

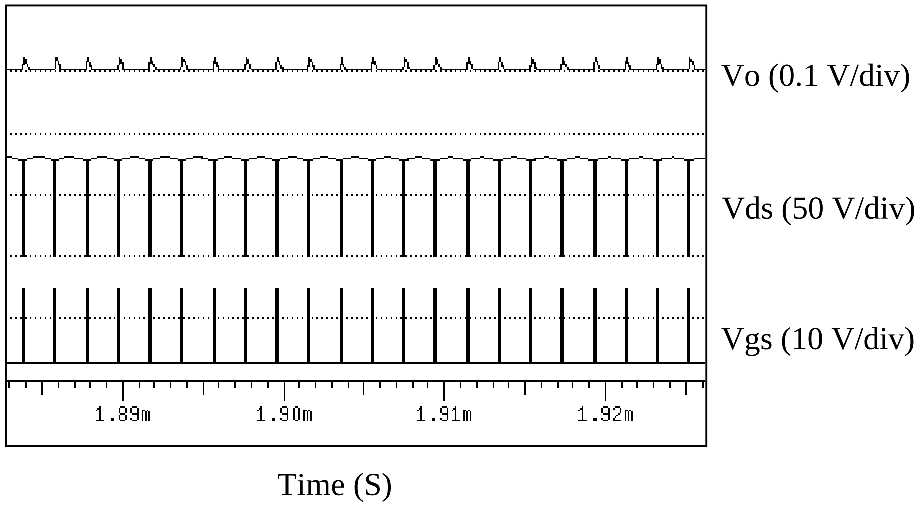


Fig. 4.16. Circuit waveforms when the minimum duty cycle function in the control block is not modeled. Simulation condition: Vin = 72 V, Io = 0.05 A.

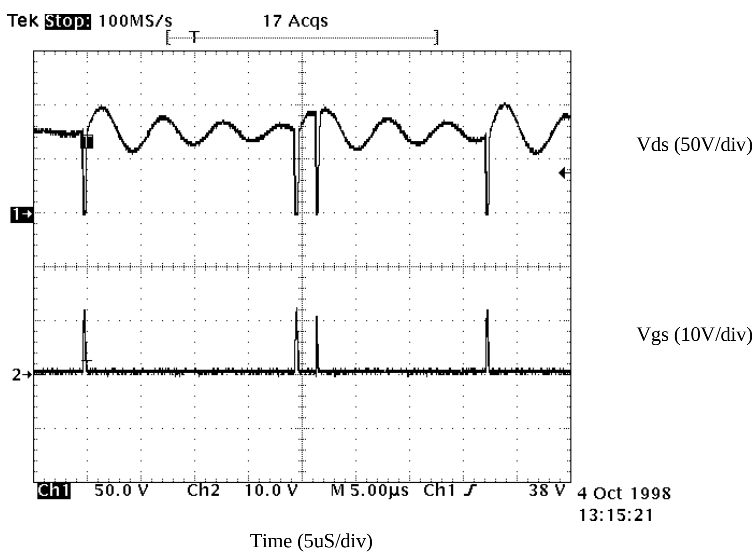
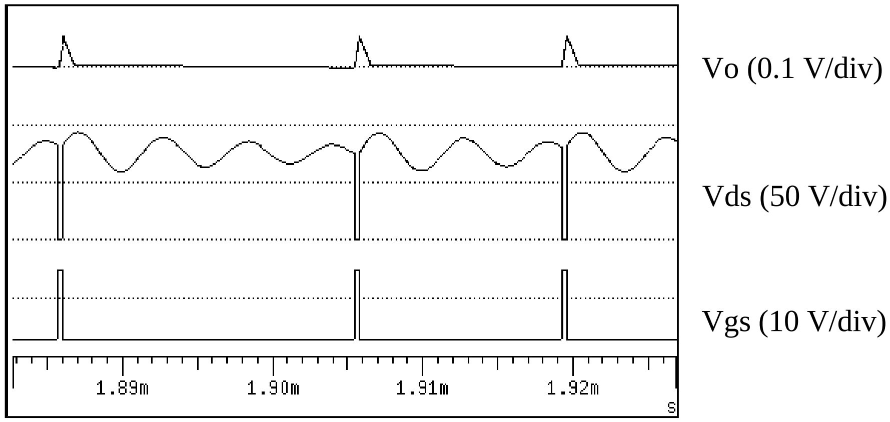
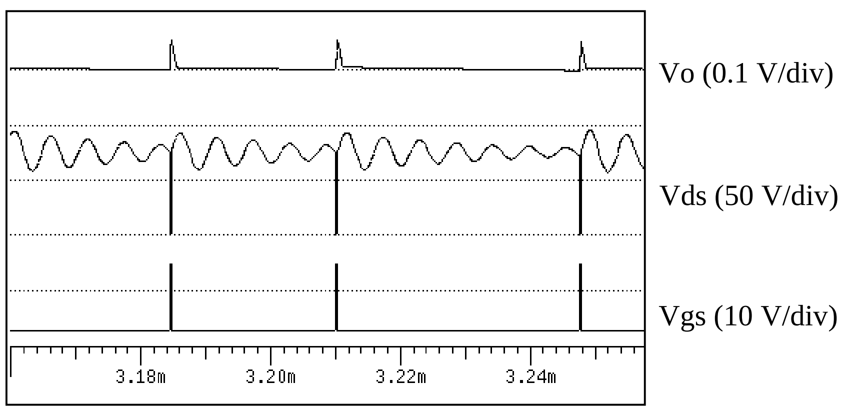


Fig. 4.17 Measurement shows different circuit behavior compared with Fig. 4.16. Vin = 72 V, Io = 0.05 A.



Time (S)

(a)



Time (S)

(b)

Fig. 4.18. Simulation results after a minimum duty cycle function is implemented in the control block. The circuit operates at no load and Vin = 72 V. (a) with adequate leakage current in the rectifier diode model. (b) with smaller leakage current in the rectifier diode model.

4.3.2.2 Load regulation curve

Load regulation is verified by sweeping the input voltage and load by the whole operational range. The simulation results are shown in Fig. 4.19. The measurement of the circuit shows a constant 4.976V due to the limitation of the meter reading.

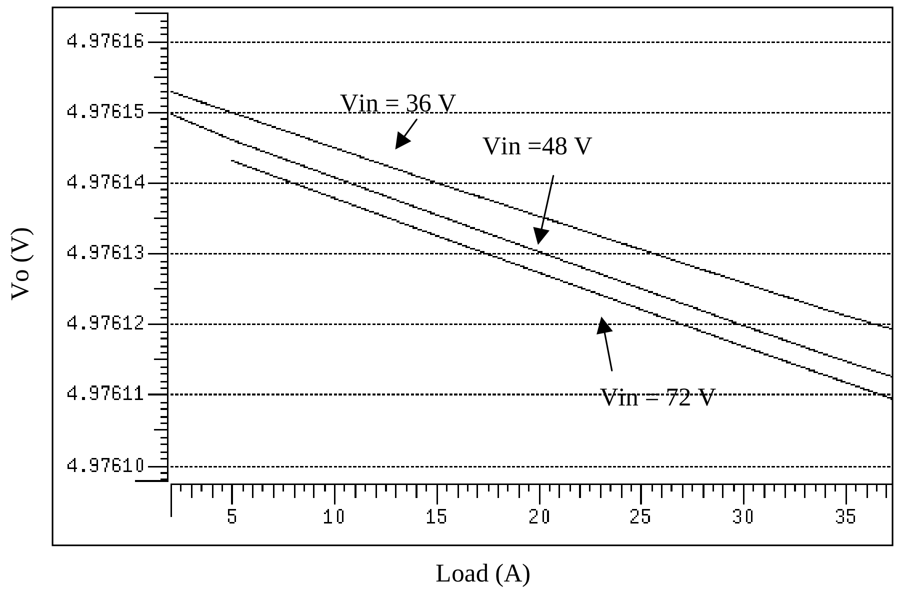


Fig. 4.19 Simulation results of the load regulation (experimental shows output voltage regulated at 4.976 V due to the limitation of the meter reading).

4.3.3 Summary of steady state analysis

Table 4.5 is the summary of the test conditions and CPU times for the steady state test of the main power supply

Table 4.5. Summary of test conditions and CPU times for the steady state test

Test type	Test condition			Simu time (s)	Total number of tests	CPU time (min)
	Vin	Io	Other			
Loss / stress analysis	Vmin, Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh,Vmax (7)	Imin, Idcm, 25%*Ifull, 50%*Ifull, 75%*Ifull, Ifull, Imax (7)	Dmin - Dmax (7)	10 u	49	9.8
Load regulation	Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh (5)	Imin, Idcm, 25%*Ifull, 50%*Ifull, 75%*Ifull, Ifull, Imax (7)	--	20 u	35	0.7
Total	--	--	--	--	84	10.5

4.4 Level 3 -- small signal stability analysis

4.4.1 Small signal test

SIMPLIS simulates the small signal transfer function by running a series of time domain simulations with different frequencies of small signal perturbations [38]; this is very close to a hardware measurement from the impedance analyzer. No small signal model needs to be derived in the test procedure. The circuit stability can be verified according to the crossover frequency and the phase margin of the loop gain. A 50 degree phase margin usually is required in circuit design. The stability of the circuit is verified by running the whole operational range of the input voltages and loads. The component level of the power stage block is M2, as shown in Table 4.1.

Fig. 4.20 is the comparison of simulation and measurement for a small-signal loop gain of the active-clamp forward converter at Vin = 48 V and Io = 15 A. The dotted line is the measurement and the solid line is the simulation. These two results match very well.

Fig. 4.21 shows the crossover frequency and phase margin of the active-clamp forward converter over the whole circuit operation range. It shows that the loop gain is independent of the load current in the simulation. Even though the circuit has a phase margin larger than 50 degrees under most of the operating points, the shaded area in the table shows that the phase margin is -20 degrees at the low line condition.

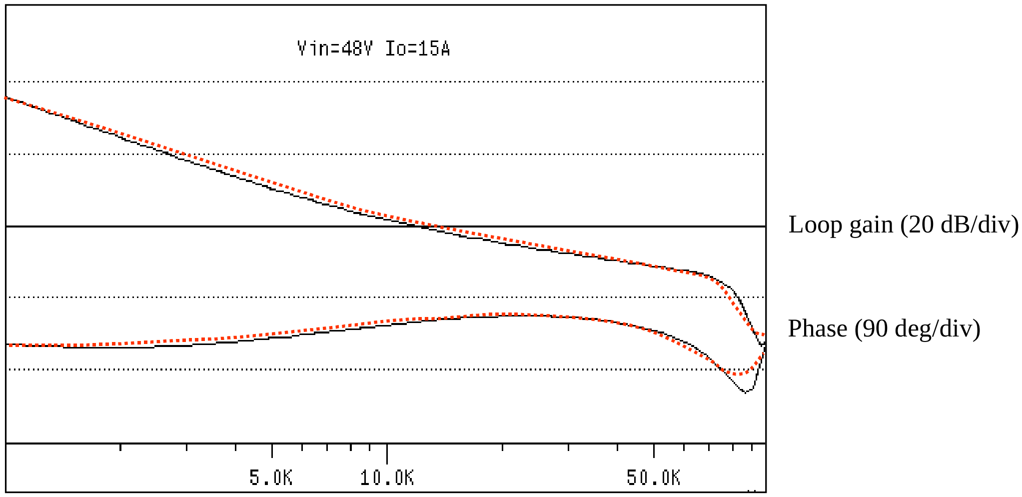
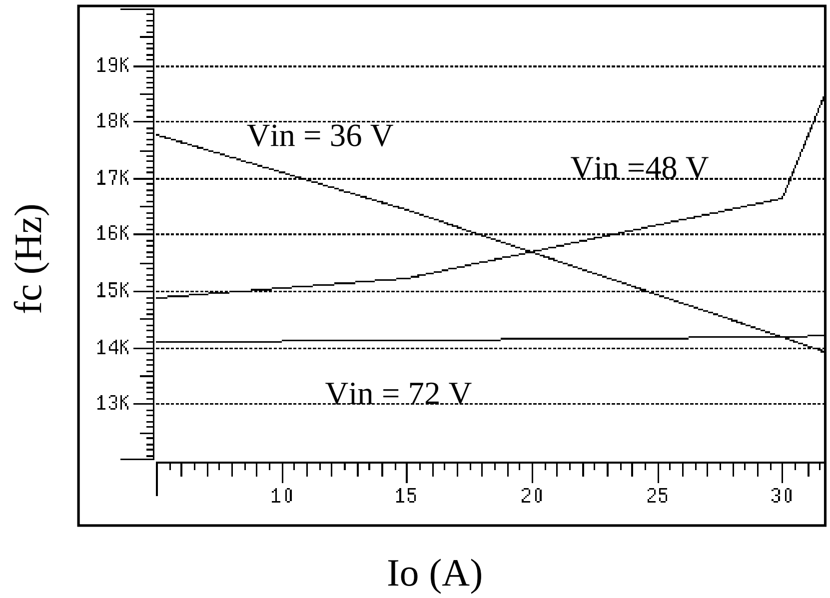
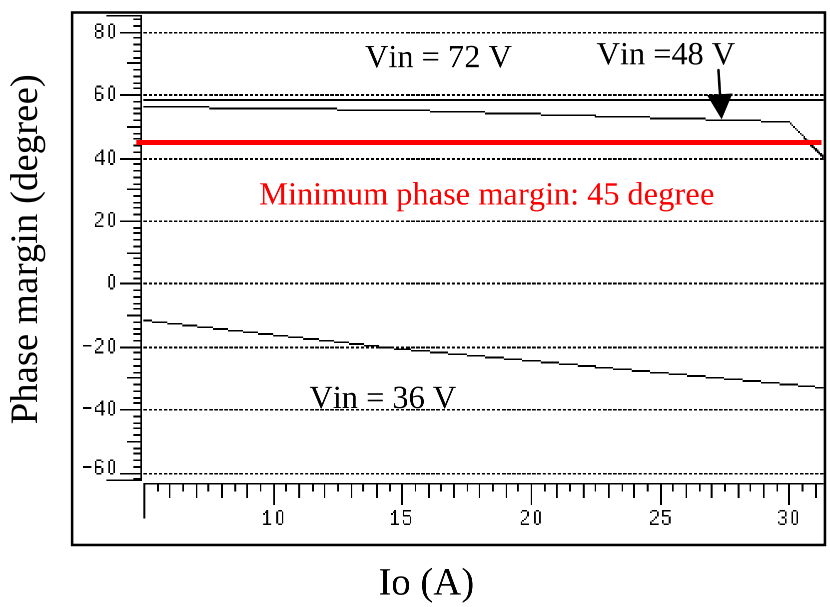


Fig. 4.20 Comparison of simulation and measurement for the loop gain and phase of the forward converter with the active-clamp reset circuit at Vin = 48 V, Io = 15 A. Dotted line: measurement, solid line: simulation.



(a)



(b)

Fig. 4.21. Crossover frequency and phase margin of the active-clamp forward converter over load and line ranges. (a) crossover frequency. (b). phase margin.

4.4.2 Design modification of control loop

The loop gain of the active-clamp circuit at Vin = 36 V is shown in Fig. 4.22. We can see that there is an additional pole and a zero around the crossover frequency, and this reduces the phase margin of the loop gain.

Fig. 4.23 shows the loop gain of the circuit with different input voltages. It shows that the active-clamp reset circuit introduces an additional pair of moving pole and zero in the loop gain. Studies show that the frequencies of the moving pole and zero are a function of the resonant frequency of the active-clamp circuit [62, 64, 67]. The resonant frequency of the reset circuit is

$$f_o = \frac{d'}{2 \cdot \pi \cdot \sqrt{L_m \cdot C_s}} \,. \tag{4.5}$$

This is a function of the duty cycle, the magnetizing inductance L_m and the clamp capacitance C_c. In order to eliminate the interaction of the additional pole and zero to the control loop design, the crossover frequency of the loop gain should be designed far below the smallest resonant frequency of the active-clamp circuit. The smallest resonant frequency happens at the lowest line at Vin = 36 V, which has the largest duty cycle.

The problem is fixed by redesigning the resonant frequency of the active-clamp circuit to a higher frequency. Fig. 4.22 shows the simulation result after redesigning the circuit. When the crossover frequency of the loop gain is smaller than the resonant frequency, the crossover frequency and phase of the loop gain is independent of the active-clamp circuit as shown in the figure.

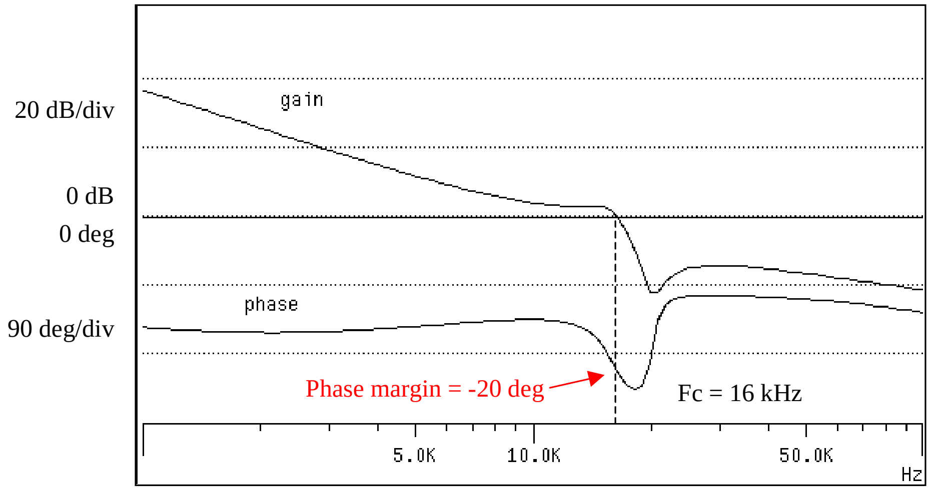


Fig. 4.22. The simulation shows the circuit has a small phase margin at low line. Vin = 36V.

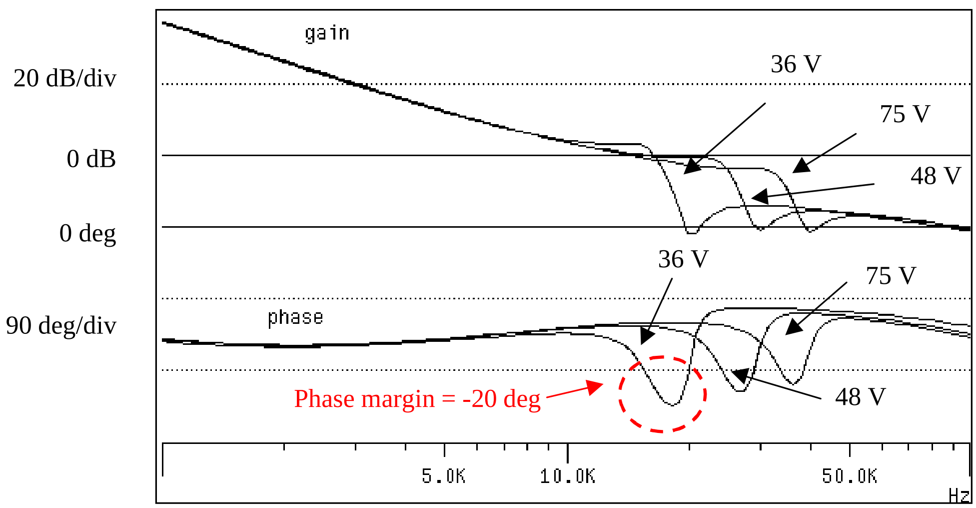


Fig. 4.23. The small signal loop gain waveforms with different input voltages. The active-clamp circuit introduces an additional pole and a zero at the resonant frequency of the reset circuit, which is a function of the duty cycle, L_m and C_s.

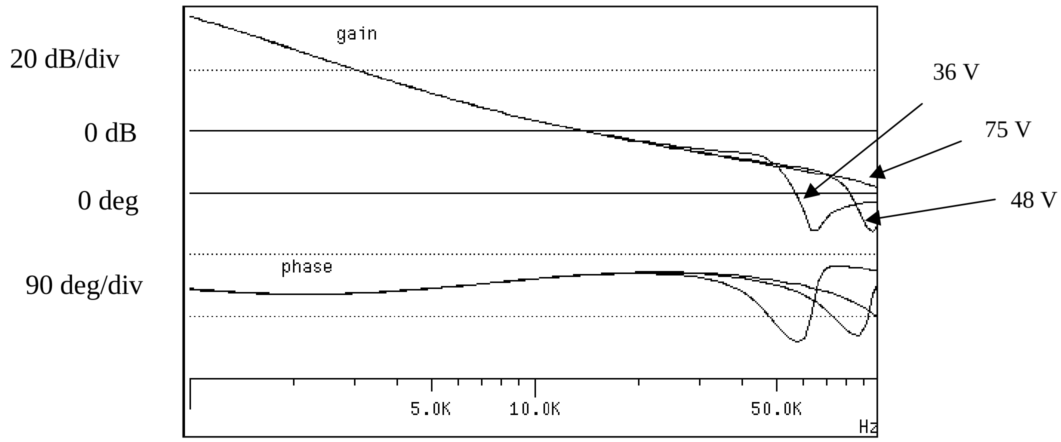


Fig. 4.24 Redesign the circuit by moving the resonant frequency to a higher frequency. The crossover frequency and the phase of the loop gain are independent of the active-clamp circuit.

4.4.3 Summary of small-signal stability analysis

The summary of test conditions and CPU times for the stability test is shown in Table 4.6.

Table 4.6. Summary of test conditions and CPU times for the stability test

Test type	Test condition			Simu freq (Hz)	Total number of tests	CPU time (min)
	Vin	Io	Other			
Stability test	Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh (5)	Iccm, 25%*Ifull, 50%*Ifull, 75%*Ifull, Ifull (5)		100 - 100 k	25	5
Total	--	--	--	--	25	5

4.5 Level 4 -- large-signal transient analysis

In the hardware test, the large-signal transient test is used mainly to verify the customer specifications, such as output voltage recovery time and output voltage overshoot during a specific load change. In the virtual prototype test, more tests can be done to cover different circuit operating conditions, so circuit stability problems, device overstress or failure under special conditions can be detected before hardware prototyping.

4.5.1 Line transient

Most of the time, no line transient test is required in the hardware test. The input voltage rising rate is usually slow due to the input filter of the circuit, so it has less problems than the load transient which could have a much faster slew rate at normal conditions. However, in abnormal conditions (such as a rush input current or failure of the input filter), a fast line transient could affect the circuit operation if the circuit is not well designed. If a circuit can tolerate step changes of the input voltages and loads, then the circuit will have fewer problems under undesirable conditions. The robust design of the circuit will also have less chance to have a recall from the product, which will increase the product cost and time significantly.

The component level of the power stage block is M3, as shown in Table 4.1. A transformer with nonlinear saturation characteristics is selected (M3) to present accurate system behavior in case the transformer is saturated during the transient.

The line transient test runs the circuit through different input voltages, loads, and input voltage rising rates. Fig. 4.25 shows the output voltage v_o and the main switch drain to source voltage v_{ds_main} waveforms during a line step change 36 V - 72 V. The main switch voltage v_{ds} shows a large peak during the transient which is much larger than the ripple voltage. The peak is because of the charge unbalance of the clamp capacitor of the active-clamp-reset circuit during the transient; details will be discussed in the next chapter. The worst condition happens when the input has step changes from low line to high line, as in Fig. 4.25. The transient is independent of load for most of the cases. From Fig. 4.25 we see that the circuit does not have problems during the line transient.

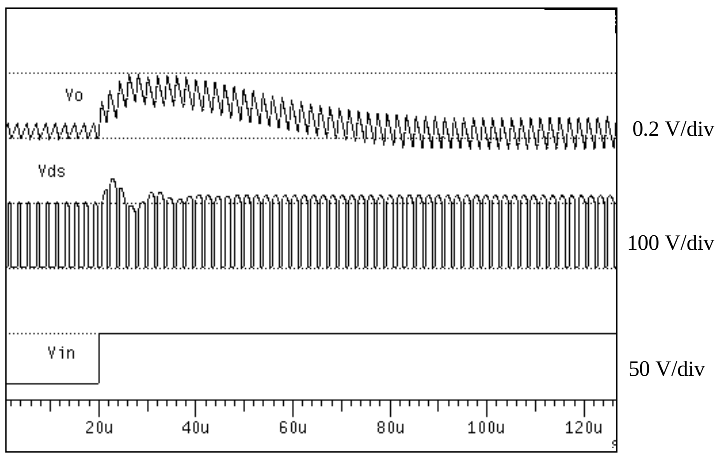
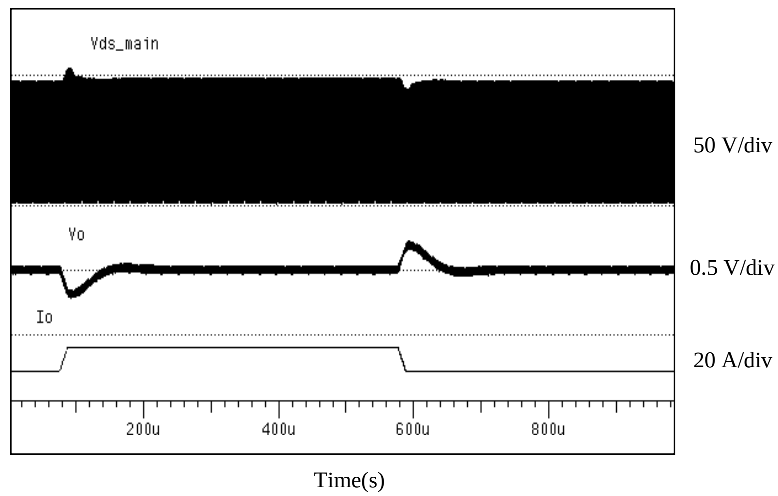


Fig. 4.25. Simulation waveform with input voltage step changes from 32 V to 72 V, and Io = 15 A.

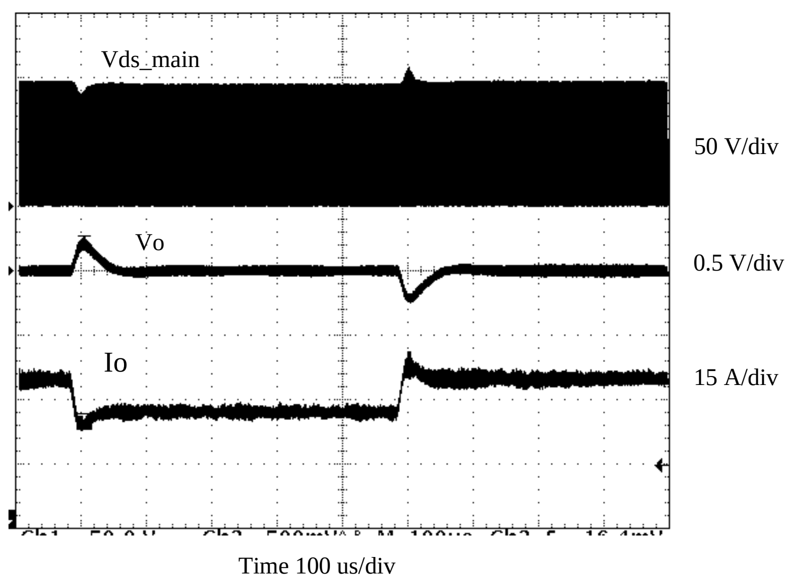
4.5.2 Load transient

Similar to the line transient, the load transient test runs the circuit through different input voltages, loads, and load voltage rising rates. The component level of the power stage block is M4, as shown in Table 4.1. A transformer with nonlinear saturation characteristics is selected (M3) to present accurate system behavior in case the transformer is saturated during the transient, and a capacitor model with ESL is used to present the possible spike during a fast load transient, as discussed in the previous chapter.

Fig. 4.25 shows the output voltage v_o and the main switch drain to source voltage v_{ds_main} waveforms during a load step change from 22.5 A to 30 A and 30 A to 22.5 A. The input voltage is 48 V, and the load change slew rate is 0.625 A/us. Fig. 4.27 shows the zoomed-in waveforms of Fig. 4.25. It shows that the virtual prototype test can represent accurate behavior in the transient response.



(a)



(b)

Fig. 4.26. Circuit transient response waveforms when load steps up from 22.5 A to 30 A and down from 30 A to 22.5 A at Vin = 48 V. The load change slew rate is 0.625 A/us in the simulation. (a) simulation (b) measurement.

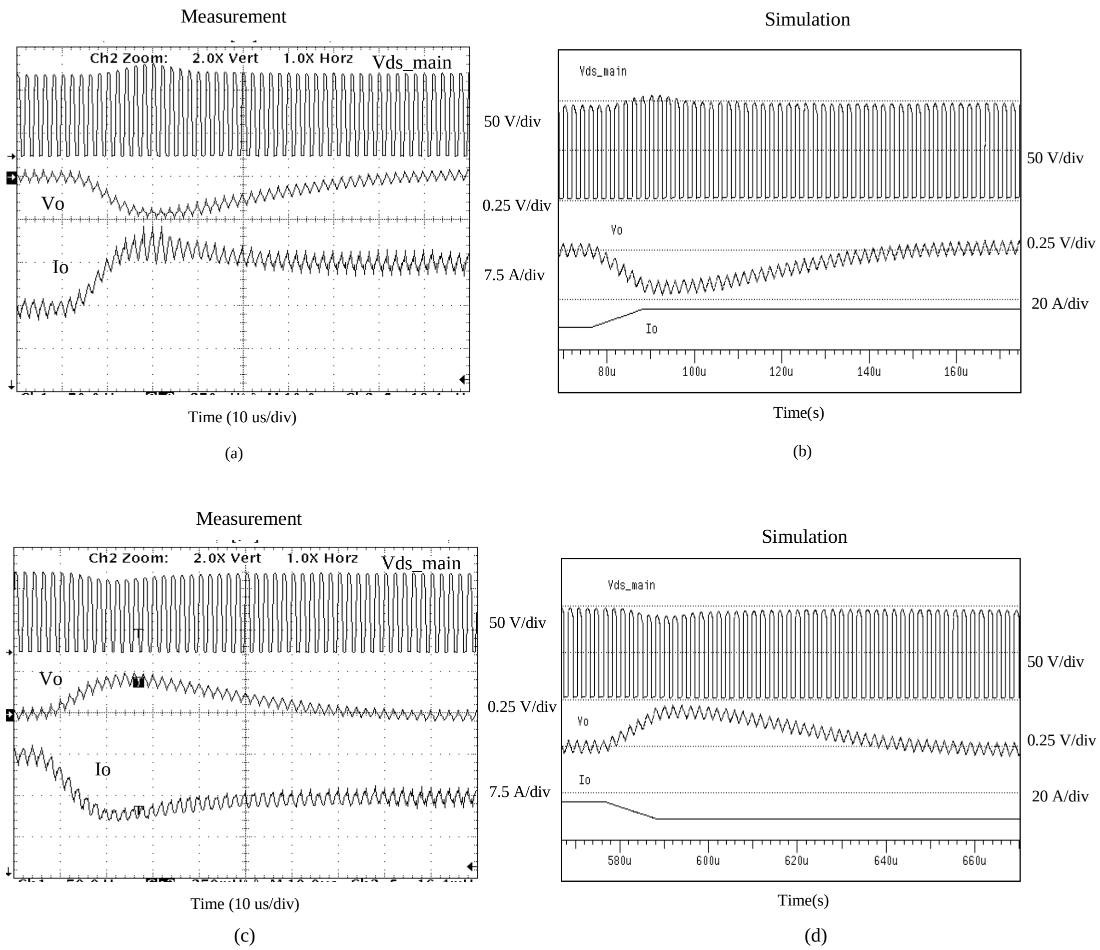


Fig. 4.27. Zoomed-in view of the circuit transient response waveforms of Fig. 4.26. (a) measurement of load change from 22.5 A to 30 A. (b) simulation of load change from 22.5 A to 30 A. (c) measurement of load change from 30 A to 22.5 A. (b) simulation of load change from 30 A to 22.5 A.

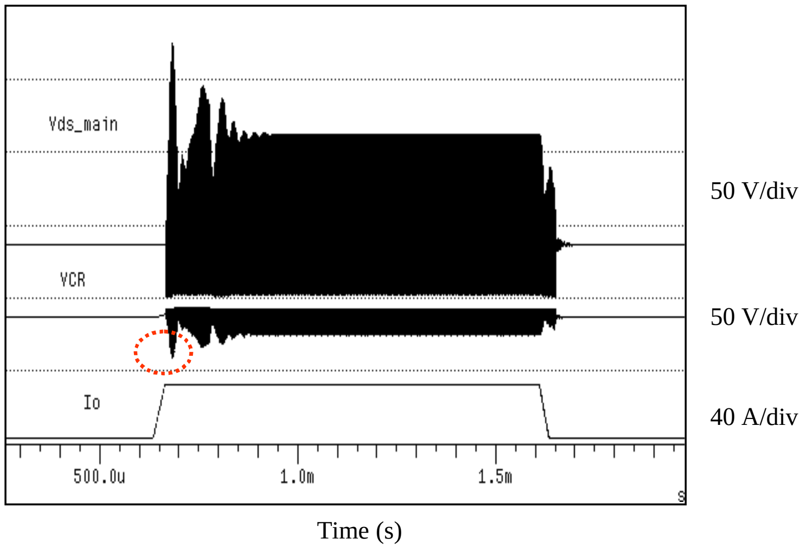
4.5.3 Design problems in large-signal transient

The same as in the line transient, the main switch voltage V_{ds} shows a large peak voltage during the transient, which is much larger than the ripple voltage. From the simulation, it shows that the largest peak occurs when the circuit has a large load transient from no load to full load at low line. Under this condition, the reverse voltage of the forward rectifier in the forward converter is 34 V, which exceeds the break down voltage rating (30 V), as shown in Fig. 4.28. Fig. 4.28 shows the large-signal response waveforms at Vin = 36 V, Io from no load to full load to no load transient. The load step slew rate is 1 A/us. Fig. 4.28(a) is the simulation result, and Fig. 4.28(b) is the measurement. The dotted circle shows that the rectifier voltage V_{CR} exceeds the device rating at the beginning of no load to full load transient.

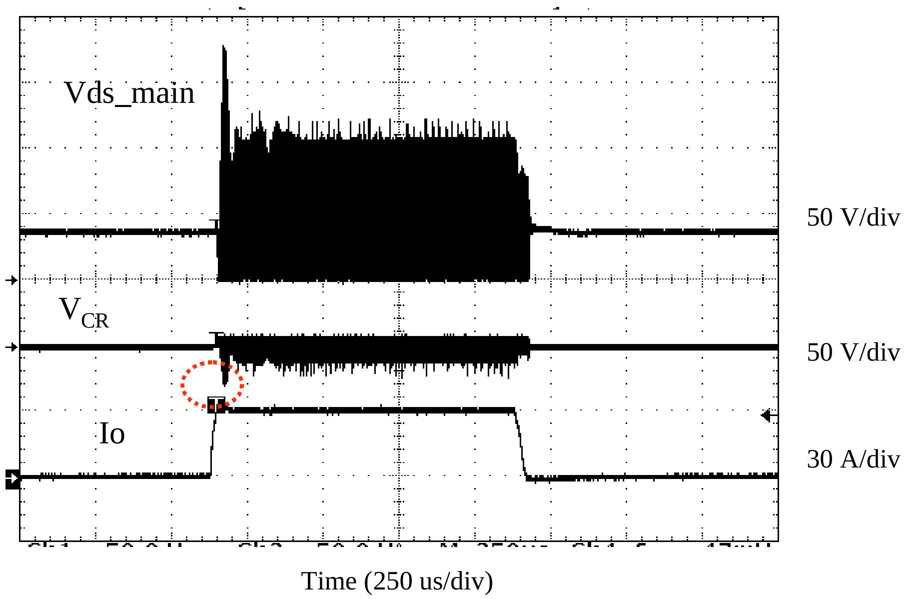
Fig. 4.29 shows a zoomed-in waveform of Fig. 4.28 for no load to full load to no load transient. Fig. 4.29(a) is the measured waveform of no load to full load transient. Fig. 4.29(b) is the simulated waveform of no load to full load transient. Fig. 4.29(c) is the measured waveform of full load to no load transient. Fig. 4.29(d) is the simulated waveform of full load to no load transient. Comparing the measurement and simulation, it shows that the virtual prototype can predict the dynamic behavior of the system very well.

The simulation also shows that there is a transformer saturation problem during no load to full load transient as in Fig. 4.30. These problems are all related to the active-clamp reset circuit. Although it is possible to adjust the circuit parameters by trials and errors to fix the problems, the problem's solution is not straightforward. It may require a lot of time and effort but still not come out as a robust circuit, since these parameters are not independent parameters and involve different circuit design issues.

In the next two chapters, we will focus on discussing the design issues related to the active-clamp circuit and demonstrate how to use the virtual prototype simulation to help in design.



(a)



(b)

Fig. 4.28 Large-signal response waveforms at Vin = 36 V, Io from no load to full load to no load transient. Load step slew rate is 1 A/us. (a) simulation. (b) measurement. The dotted circle shows that the rectifier voltage V_{CR} exceeds the device rating.

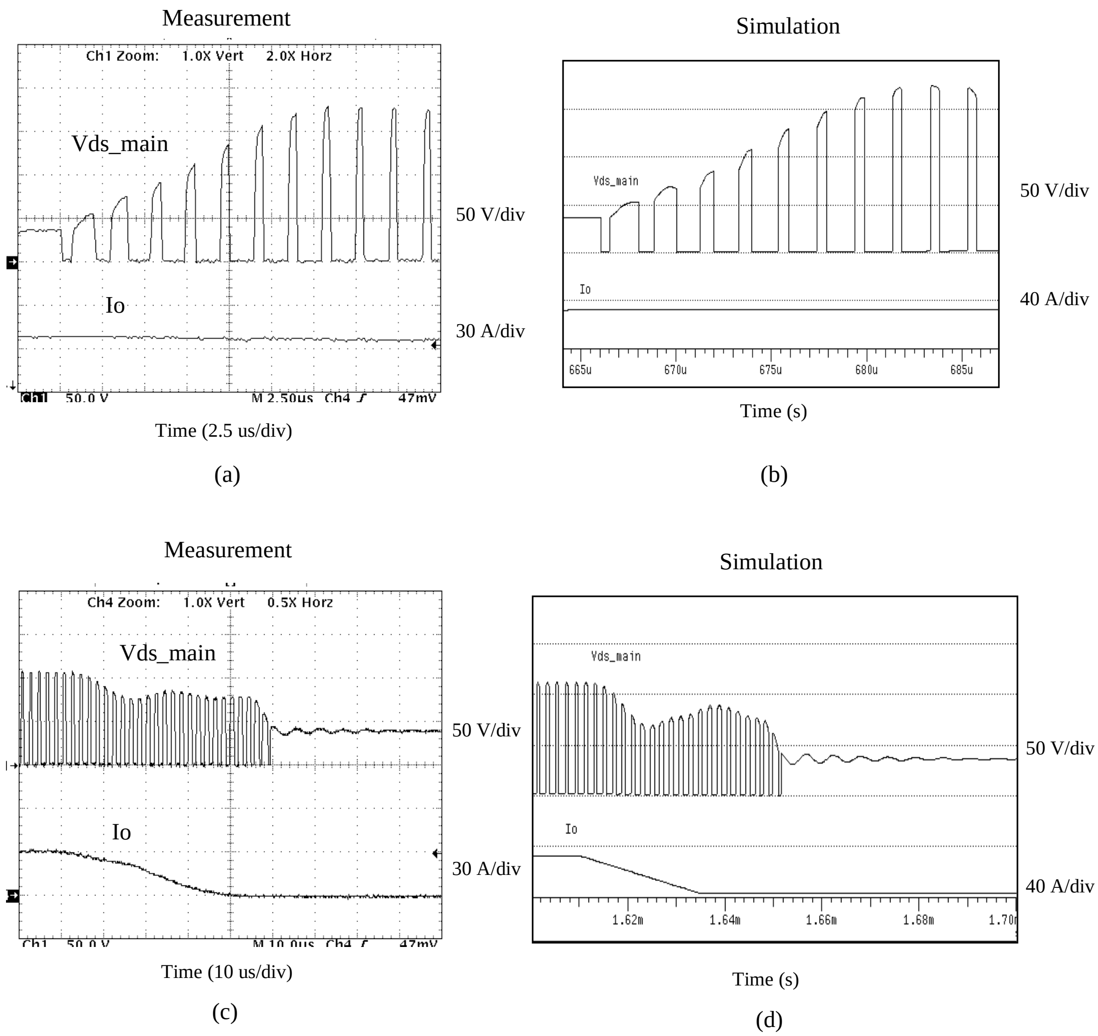


Fig. 4.29. Zoomed in waveform of Fig. 4.28 for no load to full load to no load transient. (a) measured waveform of no load to full load transient. (b) simulated waveform of no load to full load transient. (c) measured waveform of full load to no load transient. (d) simulated waveform of full load to no load transient. Comparing the measurement and simulation, it shows that the virtual prototype can predict the dynamic behavior of the system very well.

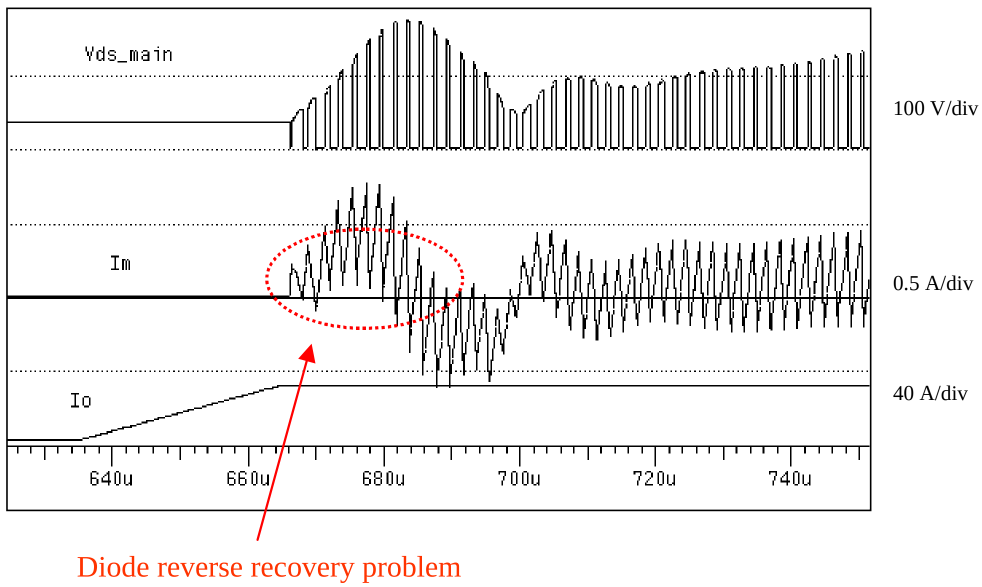


Fig. 4.30 The simulation shows there is a diode reverse recovery problem during no load to full load transient at Vin = 36 V.

4.5.4 Summary of large-signal transient analysis

The summary of the test conditions and CPU times for the transient analysis is shown in Table 4.7.

Table 4.7. Summary of test conditions and CPU times for the transient analysis

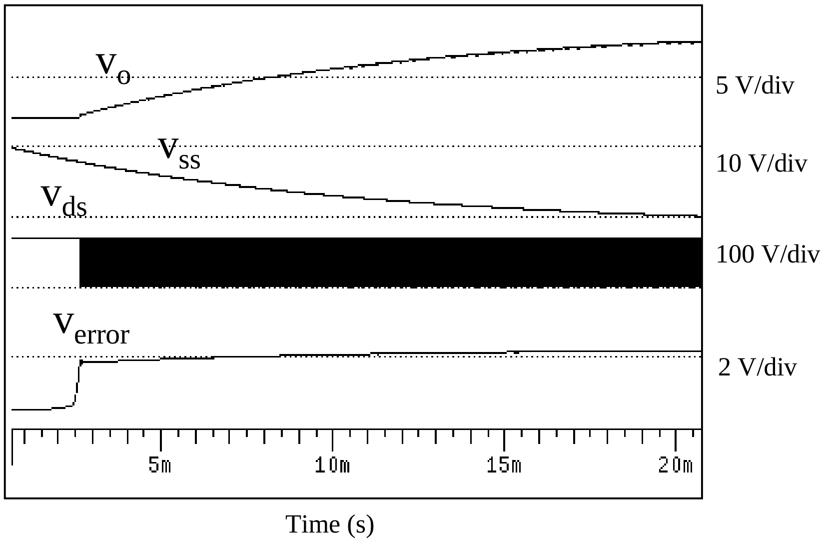
Test type	Test condition			Simu time (s)	Total number of tests	CPU time (min)
	Vin	Io	Other			
Line transient	Vl to Vnorm (2), Vnorm to Vh (2), Vl to Vh (2)	Imin, Idcm, 25%*Ifull, 50%*Ifull, 75%*Ifull, Ifull (6)	Different slew rates of input step change (3)	0.5 m	108	30.24
Load transient	Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh (5)	Imin to 25%*Ifull (2), 25%*Ifull to 50%*Ifull (2), 50%*Ifull to 75%*Ifull (2), 75%*Ifull to Ifull (2), Imin to 50%*Ifull (2), 50%*Ifull to Ifull (2), Imin to Ifull (2)	Different slew rates of load step change (3)	0.5 m	210	63
Total	--	--	--	--	336	98.28

4.6 Level 5 -- subsystem interaction

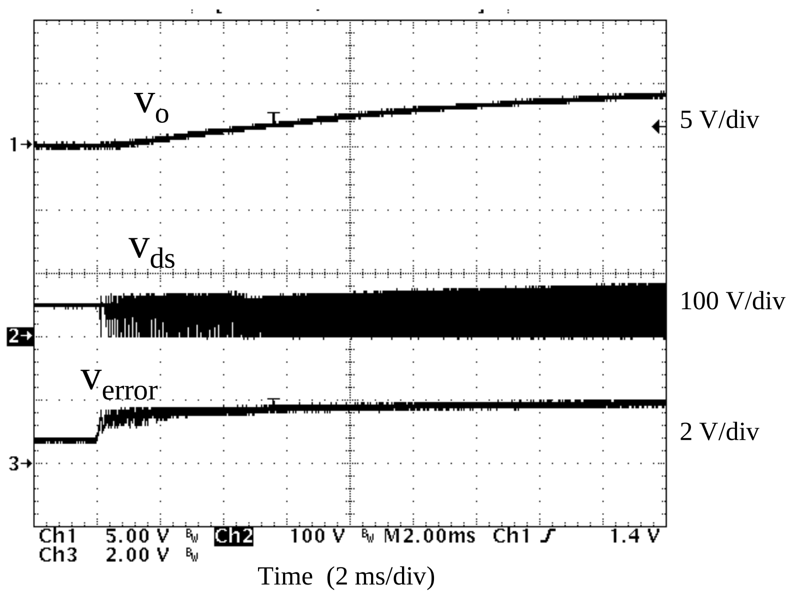
As we can see from the hierarchical test sequence table of Fig. 4.8, the subsystem interaction test will involve most of the blocks in a subsystem. Protection circuits, such as over-voltage and over-current protection circuits, are simulated with the main converter to verify the prompt reaction of the circuit under abnormal conditions.

4.6.1 Main power supply start-up

The start-up test is used to verify the device stresses of the power supply during start-up, the output voltage overshoot/undershoot, the input current, and the rising time of the output voltage. The component level of the power stage block is M3, as shown in Table 4.1. The detail control circuit which includes the start-up circuit (M3), OV, and OC blocks are included in the simulation. Fig. 4.31 shows the start-up waveforms of the main power supply. Fig. 4.31(a) is the simulation result, and Fig. 4.31(b) is the measurement. The input voltage of the simulation is 48 V, and the load is at 2 A. This shows that the rising time of the output voltage of the main power supply is about 20 mS. The simulation matches the measurement very well.



(a)



(b)

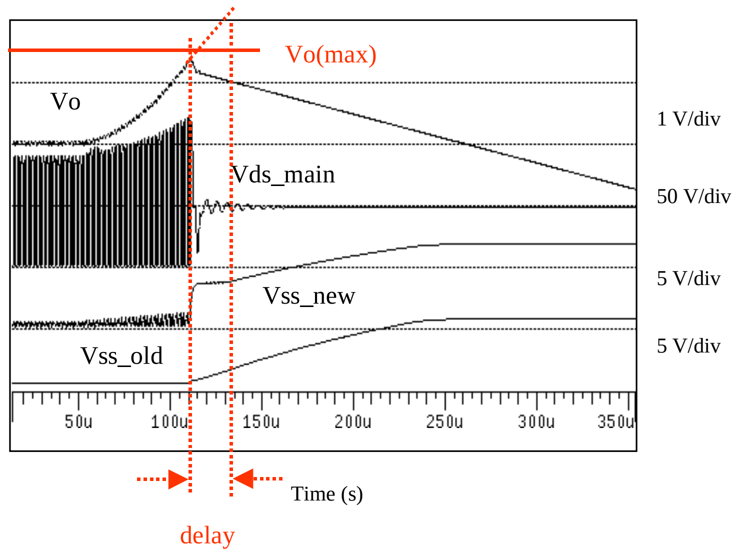
Fig. 4.31 Verification of the start-up of the main power supply at Vin = 48 V and Io = 2 A. (a) simulation. (b) measurement.

4.6.2 Abnormal condition test

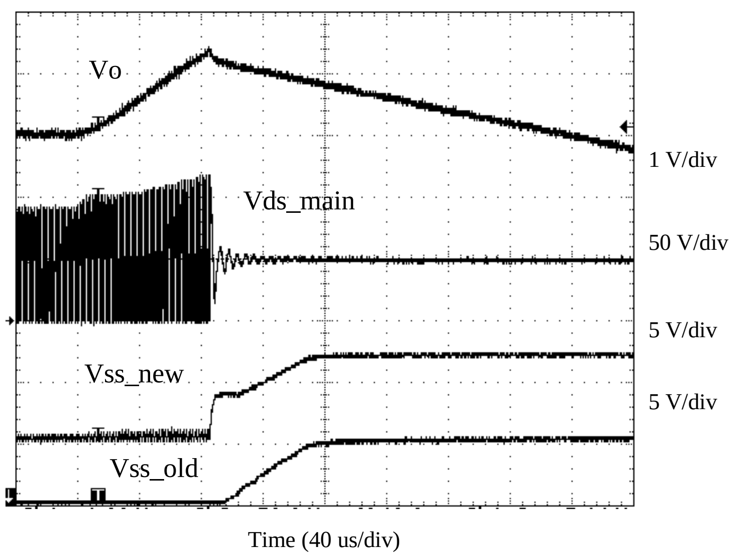
4.6.2.1 Over-voltage test

The component level of the power stage block for the over-voltage test is M3, as shown in Table 4.1. The control block without a start-up circuit (M2) is used in the simulation. The major purpose of the start-up test is to verify the system reaction to over voltage. The modeling of delays in protection and control circuits is critical for the accuracy of the system behavior in this type of test.

The over-voltage test is performed by disconnecting the sensed output voltage during the test. Fig. 4.32 shows the circuit waveform of the over-voltage test. Fig. 4.32(a) is the simulation waveforms, and Fig. 4.32(b) is the measurement. Vss_old is the control signal in the original circuit to shut down the power stage when the sensed voltage exceeds the threshold voltage. There is an additional 0.6 V overshoot of the output voltage due to the delay of the over-voltage circuit in the original design; this makes the maximum voltage of the power supply exceed the maximum voltage specification. By redesigning the circuit with less delay in the protection circuit, the problem is solved. The new control design has a signal Vss_new as shown in Fig. 4.32. It is worthwhile to mention that the major delay of the over-voltage protection circuit is from the slew rate of the operational amplifier, so it is critical to add this characteristic in the IC chip model.



(a)



(b)

Fig. 4.32 Over-voltage test waveform. With the old circuit design, the delay of the over-voltage circuit introduces an additional 0.6V voltage overshoot. It makes the maximum voltage of the power supply exceed the maximum voltage specification.

4.6.2.2 *Over-current test*

Similar to the over-voltage test, the component level of the power stage block is M3, as shown in Table 4.1. The over-current test is performed by increasing the load source, as shown in Fig. 4.33. In this figure, I_L is the inductor current, V_{SS} is the soft start capacitor voltage, and V_O is the output voltage. The over-current protection circuit acts when the inductor current reaches approximately 38 A.

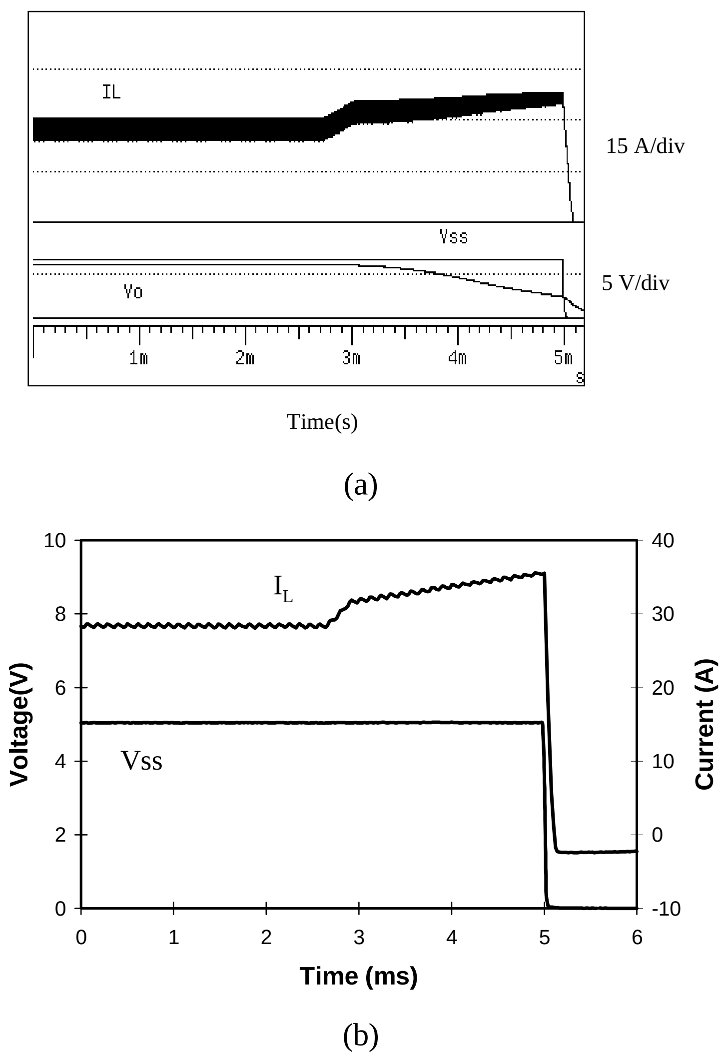


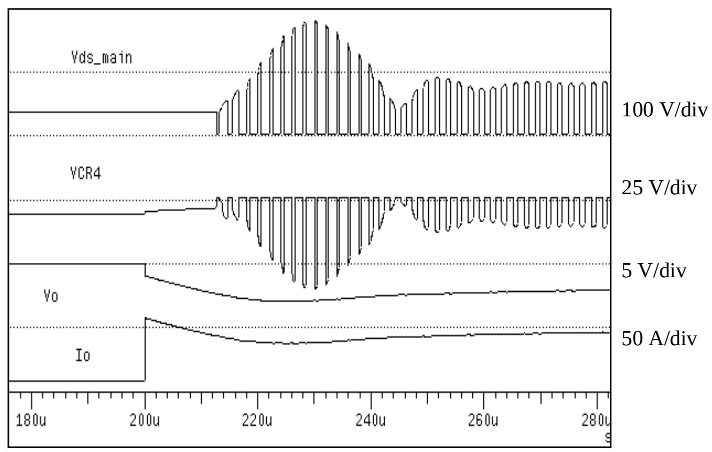
Fig. 4.33 Simulation and measurement waveforms of inductor current and soft start capacitor voltage during the over-current test. (a) simulation. (b) measurement.

4.6.2.3 Short circuit test

The component level of the power stage block for short circuit test is M4, as shown in Table 4.1. Fig. 4.34 shows the short circuit test waveform at Vin = 36 V, Io = 0 A. Fig. 4.34(a) is the simulation result, and Fig. 4.34(b) is the measurement. The load is not the same in the simulation and the measurement due to the non-linearity of the short circuit of the load source in the measurement. The simulation can predict the peak of the main switch drain to the source voltage and the rectifier voltage. The peak voltage of the rectifier in the short circuit test is -32 V in the simulation, which exceeds the rectifier rating and the peak voltage of the rectifier in the measurement is about -30 V.

Fig. 4.35 shows the magnetizing current I_m in the same short circuit test. Similar to the previous load transient test, the magnetizing current of the transformer stays positive for a short period as the marked area in the figure, which will cause the diode reverse recovery problem in the circuit.

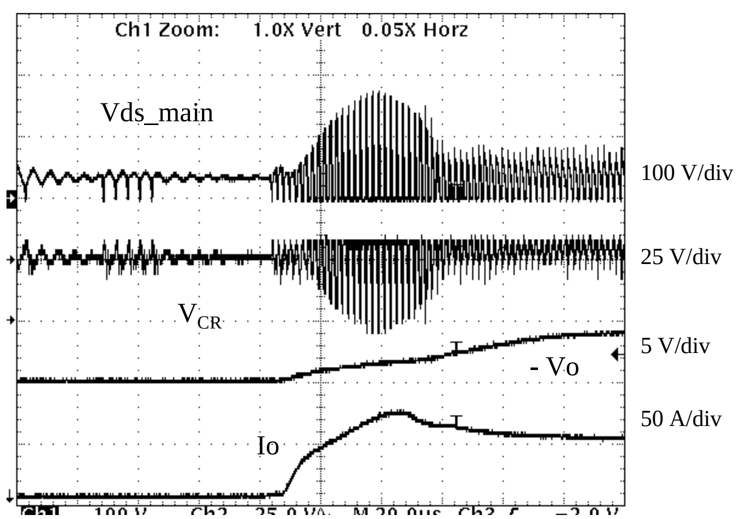
Simulation



Time (s)

(a)

Measurement



Time (20 us/div)

(b)

Fig. 4.34 Short circuit test waveform at Vin = 36 V, Io = 0 A. (a) simulation. (b) measurement.

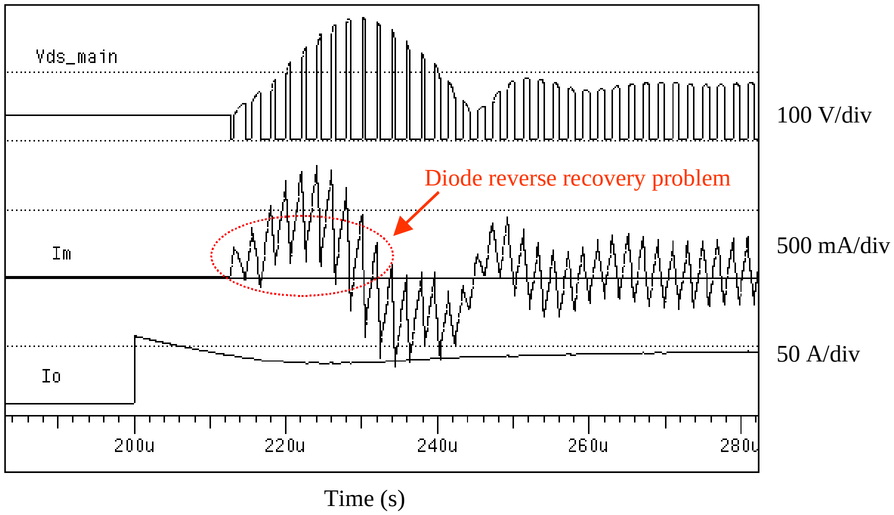


Fig. 4.35. Short circuit test at Vin = 36 V, Io = 0 A. The marked area shows diode reverse recovery problem of the active-clamp circuit due to a positive magnetizing current in a short period.

4.6.3 Summary of subsystem interaction

The test conditions and CPU times for the subsystem interaction test is shown in Table 4.8.

Table 4.8. Summary of test conditions and CPU times for the subsystem interaction test.

Test type		Test condition			Simu time (s)	Total number of tests	CPU time (min)
		Vin	Io	Other			
Main power supply start-up		Vl, Vnorm, Vh (3)	Imin, 50%*Ifull, Ifull (3)		35 m	9	72
Abnormal condition test	OV test	Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh (5)	Imin, Idcm, 25%*Ifull, 50%*Ifull, 75%*Ifull, Ifull (6)		0.5 m	30	15
	OC test	Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh (5)	Imin, Idcm, 25%*Ifull, 50%*Ifull, 75%*Ifull, Ifull (6)		0.5 m	30	15
	Short circuit test	Vl, (Vl+Vnorm)/2, Vnorm, (Vnorm+Vh)/2, Vh (5)	Imin, Idcm, 25%*Ifull, 50%*Ifull, 75%*Ifull, Ifull (6)		0.5 m	30	15
Total		--	--	--	--	99	117

4.7 Level 6 -- system interaction

The system interactions of the bias power supply and the main converter are potentially far more complex than the interactions between dc-to-dc converters connected in parallel or cascade. The interactions between the bias power supply and the main power supply involve all the functional blocks of the entire power supply system.

Often the design of the bias power supply is assumed trivial, since it consumes very little power and usually does not have strict specifications in terms of output voltage regulation and dynamic performance. However, as we can see from Fig. 4.1, these two converters in the complex power supply system are highly interactive. In particular, different operating conditions of the main power supply affect the bias current drawn by the control and protection circuitry of the main power supply. These line and load changes of the bias power supply will in turn affect the bias voltages of the main power supply. As we shall show, many of the potential problems resulting from this interaction are exceedingly difficult to predict analytically and often are very costly to detect and solve using hardware tests.

In recent years, many efforts have been made to develop simulation methodologies to help design and detect problems of the power converter [1-6, 27-43, 46-47, 52-54]. The contents of these papers cover issues such as general simulation approaches [1-6], multi-level modeling for accelerating simulation speed [30-34], inspection of system interaction of cascaded converters [41-42], loss estimation by using simulation [28, 35], and start-up transient analysis of the converter [52-54]. However, no literature has been presented so far on how to use simulation to verify the detailed design of a complex power supply system. The simulation of two converters with different switching frequencies is so time-consuming that the study of the interactions of these two converters usually is reserved for hardware testing.

This section proposes a simulation approach that can explore the interaction of the complex power supply system efficiently. By carefully de-coupling the two converters while including the important characteristics of each converter in the simulation, the simulation CPU time is reduced to a practical range. The objective of the section is to verify the methodology by using measured data from an actual power supply system illustrated in Fig. 4.1. Moreover, it also shows how to look for solutions when detecting the potential problems.

The main power converter of Fig. 4.1 operates at a switching frequency of 500 kHz, while the bias power supply operates at a variable switching frequency in the megahertz region. This section shows that the proposed simulation approach can verify important aspects of the power supply system design effectively. The performance of the bias power supply over the whole load range, the interactions of the bias power supply and the main power supply during large-signal transients, and the start-up sequencing of the power supply system are discussed in this section. We confirm the validity of the simulations by comparing critical waveforms with lab measurements.

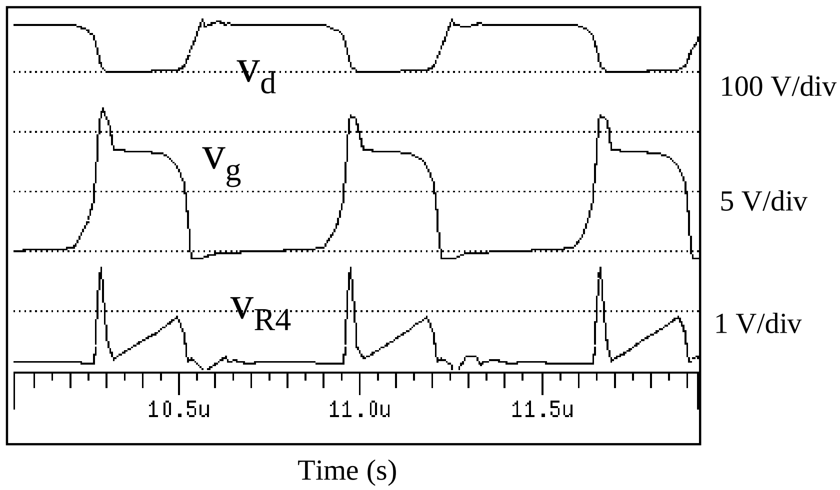
4.7.1 Bias circuit tests

This section will discuss the bias circuit tests that relate to interaction discussions.

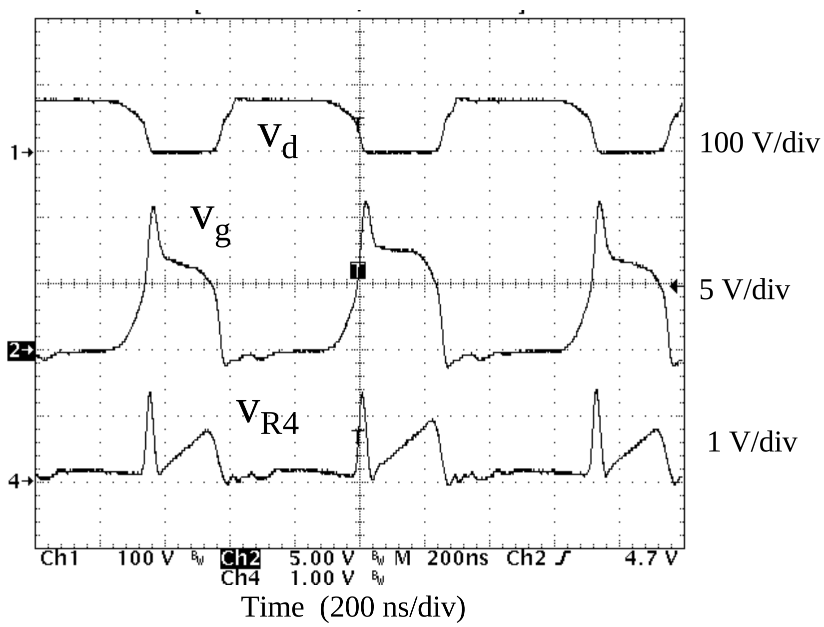
4.7.1.1 Verification of steady state performance of the bias circuit

The actual circuit operation differs from the ideal flyback circuit because of the magnitude of the gate drive current that is coupled to the primary through the transformer winding n3. The turn-on of Q2 draws an additional current from the gate drive circuit and this additional current is reflected in the primary current, thus generating a higher current spike during the turn-on of the power switch Q1.

Fig. 4.36(a) shows the steady state simulation waveform of the bias power supply with V_{in} = 48 V, I_{p_bias} = 80 mA, and I_{s_bias} = 40 mA, in which I_{p_bias} is the primary bias load current, and I_{s_bias} is the secondary bias load current. The waveforms shown in Fig. 4.36(a) are the drain voltage v_d of the power switch Q1, the gate voltage v_g, and the current sensor voltage v_{R4}. Fig. 4.36(b) shows the measurement of the circuit under the same operating conditions. The simulation shows very close agreement with the measurement. Both the simulation and measurement waveforms show a high spike voltage on v_{R4} at turn-on.



(a)



(b)

Fig. 4.36. Steady state waveforms of the bias power supply at V_{in} = 48 V, I_{p_bias} = 80 mA, and I_{s_bias} = 40 mA. Simulation and measurement shows a high spike at the switch on instant in the bias power supply in steady state. (a) simulation. (b) measurement.

4.7.1.2 De-coupling the bias from the main power supply

The bias power supply has two outputs. The self-oscillating mechanism causes the conversion frequency of the bias power supply to vary as a function of line and load. It is important to understand the nature and range of load variation for both the primary and secondary outputs of the bias power supply.

4.7.1.2.1 Estimate the load range of the secondary bias power supply

The secondary bias power supply provides the internal bias current for control, over-voltage protection, under-voltage protection, and over-current protection circuits of the main power supply. The bias supply current is monitored during the simulation for each of these circuit blocks. Table 9 shows that the total estimated load range of the secondary bias power supply is 35 - 45 mA dc. Only the main converter is needed in the simulation to obtain these estimates.

Table 9 Estimated secondary bias power supply currents from the previous simulation.

Block name	Control	OV	OC	UV	Total
Normal bias supply current (mA)	28	3	2	2	35
Maximum bias supply current (mA)	32	5	3	3	43

4.7.1.2.2 Estimate the load of primary bias power supply and its interaction with the secondary bias power supply

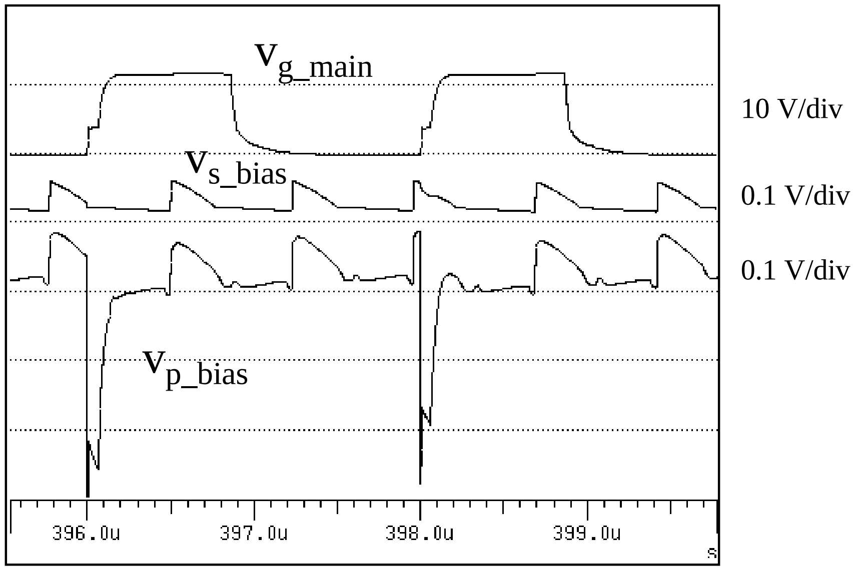
The primary bias power supply powers the gate drive circuit of the main power supply. In order to reduce the simulation time, the load on the primary bias supply is represented by the gate drive of the main converter driving a MOSFET model. The complete power stage of the main power supply is not used in the simulation. The load on the secondary bias is represented by a constant resistance. Fig. 4.37(a) shows the simulation waveforms of the gate signal of the MOSFET model v_{g_main}, the secondary bias voltage v_{s_bias}, and the primary bias voltage v_{p_bias}. The corresponding lab measurements are shown in Fig. 4.37(b). The load on v_{P_bias} of the gate drive current of the main converter is a pulsating current. The interaction between these two power supplies along with the dynamic cross regulation of the bias power supply can be observed in both Fig. 4.37(a) and 5(b).

We conclude that since the ripple on the secondary bias voltage caused by the pulsing load on the primary bias is less than 50 mV, it is not necessary in subsequent simulations to use a pulsing current model for the primary bias load. A constant current model can be used. From the simulation and measured data, the average primary bias current is 80 mA at full load.

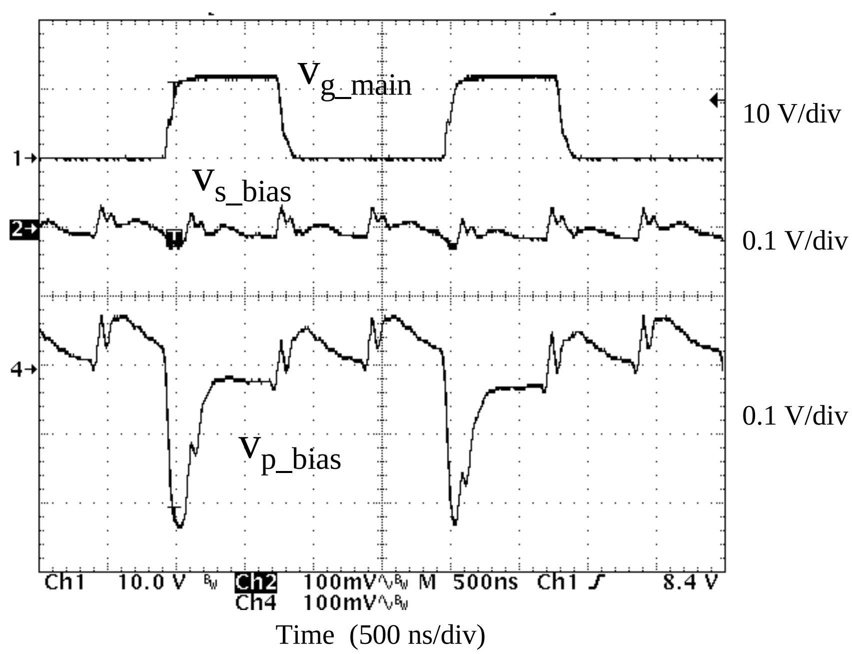
It was observed that when the main converter operates at high line and no load, the main converter will skip several switching cycles to regulate its output voltage. Under these conditions, the average load current on the primary bias is extremely small. Next, we examine what is required to simulate this type of interaction accurately.

4.7.1.3 Design verification of the operating characteristics of the bias power supply

Previous analysis shows that the load of the bias power supply can be simplified to different constant loads. The load of the primary bias is 80 mA except when the main converter is under high line, no load conditions such that the primary bias load is near 0 mA. The load of the secondary bias is typically 40 mA and could vary over the range of 35 – 45 mA. First, we will characterize the bias supply operation under extremely light load conditions. Next we will find the worst case large signal transient condition.



(a)



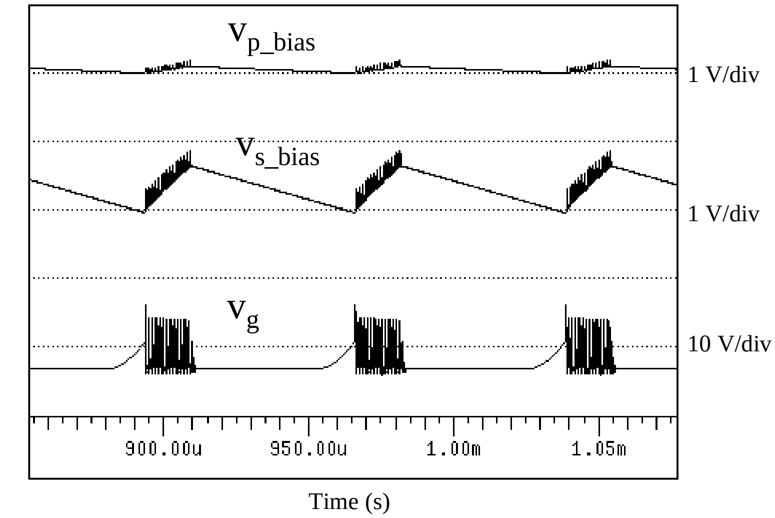
(b)

Fig. 4.37. Effect of the pulsating gate-drive current of the main power supply on the bias power supply. (a) simulation. (b) measurement.

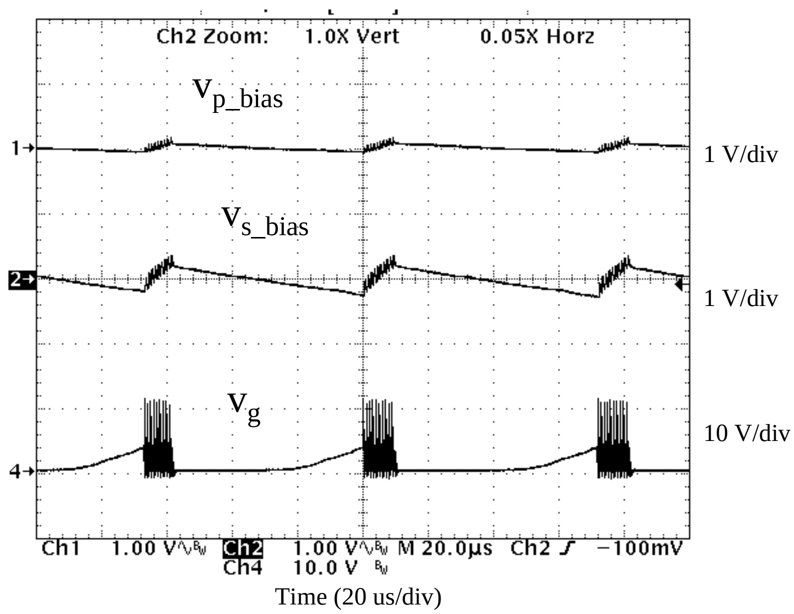
4.7.1.3.1 Characterize extremely light load operation

Under the extreme conditions where the main power supply is at high line and no load, the bias power supply operates with a sub-harmonic oscillation as shown in Fig. 4.38 and Fig. 4.39. Fig. 4.38(a) and Fig. 4.39(a) are the simulation results and Fig. 4.38(b) and Fig. 4.39(b) show the lab measurements. It is interesting to note that the bias supply behavior is sensitive to the parasitic base collector capacitance of Q2. We measured two different printed circuit board layouts, and the difference can be seen by comparing Fig. 4.38(b) and Fig. 4.39(b). The simulation can reproduce both circuit behaviors by adjusting the parasitic capacitance +/-25%.

It is important to find the sensitivity of the main power supply to this ripple on the secondary bias supply. First, we need to look for other possible sources of interaction before we discuss the interaction with the bias power supply and the main power supply.

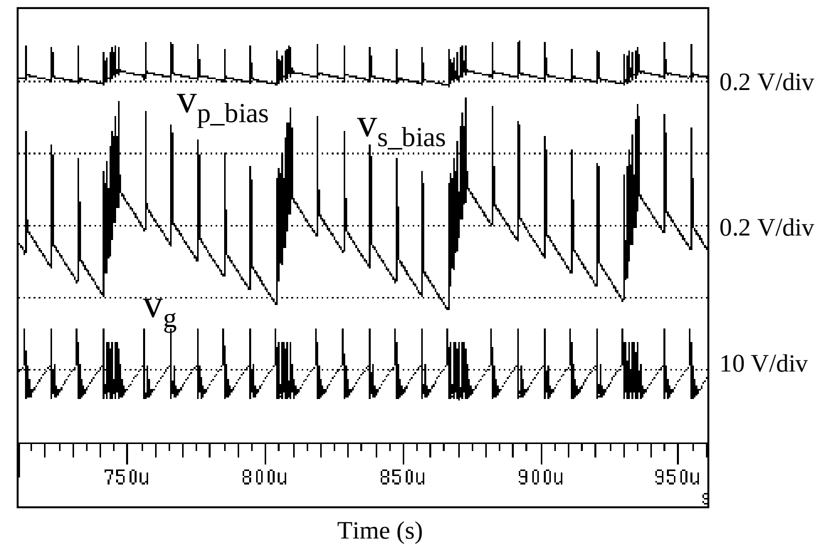


(a)

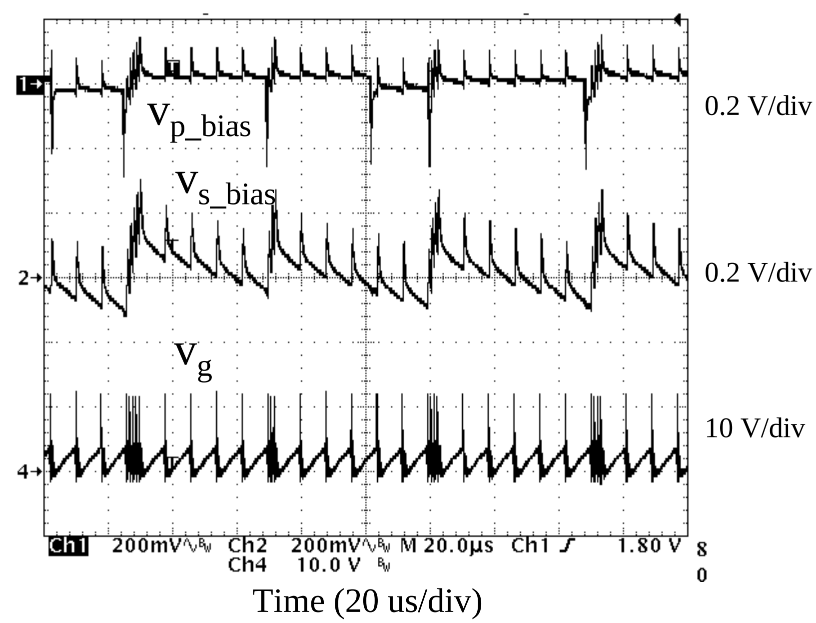


(b)

Fig. 4.38. Output voltage of the primary and secondary bias power supply at V_{in} = 75 V, I_{p_bias} = 2 mA, and I_{s_bias} = 40 mA. (a) simulation. (b) measurement.



(a)



(b)

Fig. 4.39. Output voltage of the primary and secondary bias power supply with a different printed circuit board layout at V_{in} = 72 V, I_{p_bias} = 2 mA, and I_{s_bias} = 40 mA. (a) simulation. (b) measurement.

4.7.1.3.2 Investigate large-signal transient response of the bias power supply

In order to predict the interaction of the bias power supply with the power supply system during transients, the first step is to find the worst scenario of the bias voltage response during line and load step changes. Large signal transients include load step changes from 35 mA - 45 mA and 45 mA to 35 mA with different line voltages, and line voltage step changes with different load conditions. By simulating the circuit under these load and line conditions, the simulation results show that the largest variation of the secondary bias power supply output occurs at a line change from 36 - 72V with I_{p_bias} = 80 mA and I_{s_bias} = 40 mA which is shown in Fig. 4.40.

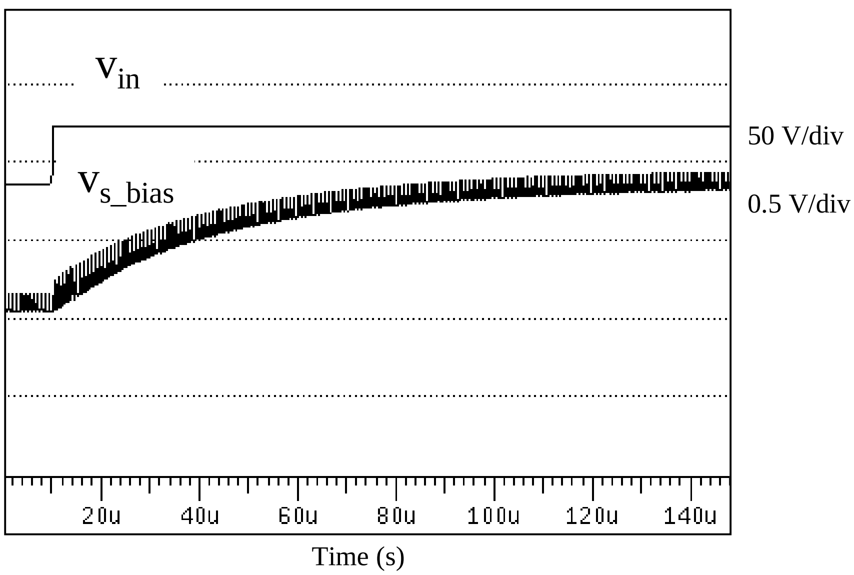


Fig. 4.40. Load transient response of the bias power supply with a line step change of 36 - 72 V, I_{p_bias} = 80 mA, and I_{s_bias} = 40 mA.

4.7.2 Interaction of bias power supply with the power supply system

The component level of the power stage block for system interaction tests is M1, as shown in Table 4.1. The active-clamp-reset circuit is not used in the simulation. Most of the components in the power stage block use the simplest model levels.

4.7.2.1 Interaction of the bias power supply and the main converter due to variation of secondary bias voltage

In the previous section, we see that when the main power supply operates at high line and no load condition, there is a low frequency ripple voltage on the secondary bias power supply. It is very important to study the sensitivity of the main power supply to this ripple voltage. A saw-toothed signal is used to emulate the secondary bias power supply ripple to reduce the simulation CPU time. The simulation conditions are V_{in} = 72 V, I_{p_bias} = 2 mA, and I_{s_bias} = 40 mA.

By varying the ripple value of this saw-tooth, we can explore the sensitivity of the main power supply to this ripple. Simulation testing on an early development version of this circuit shows that the main power supply was sensitive to the ripple on v_{s_bias} when the ripple is larger than 2 V as illustrated in Fig. 4.41. The output voltage of the main converter v_o, the inverting input voltage v_{inv} and the output voltage v_{error} of the error amplifier, and the voltage of the soft start v_{ss} are defined in Fig. 4.42 where we see the simplified control and soft-start circuit diagram of the main power supply. All the voltages are referenced to the ground in Fig. 4.42. The soft-start circuit is designed to pull the inverting pin of the error amplifier to a high voltage to limit the rising rate of the duty cycle during start up. However, the ripple of the bias supply voltage v_{s_bias} could couple through C103 and Q101 when the ripple is too large. This could induce a low frequency noise in the output voltage of the error amplifier, and thus the output voltage of the main converter. In the lab, the largest ripple of the secondary bias voltage is less than 1 V, which is below the critical condition. However, using the simulation, we found that the ripple could be larger than 2 V when the parasitic base collector capacitance of Q2 is 50% smaller than the present value in the actual circuit. The sensitivity of the main power supply to the secondary bias voltage ripple can be reduced by redesigning the bypass resistor, R_b, in the soft-start circuit to reject the higher ripple of the secondary bias voltage. The simulation is shown in Fig. 4.43 to verify the design. The low frequency output ripple of the main power converter is eliminated.

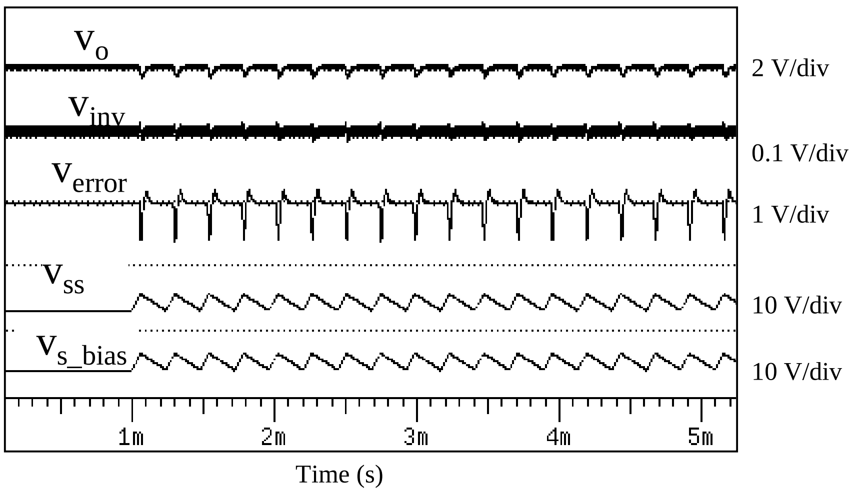


Fig. 4.41. Output voltage of the main converter carries low frequency ripple due to the output ripple of the secondary bias voltage.

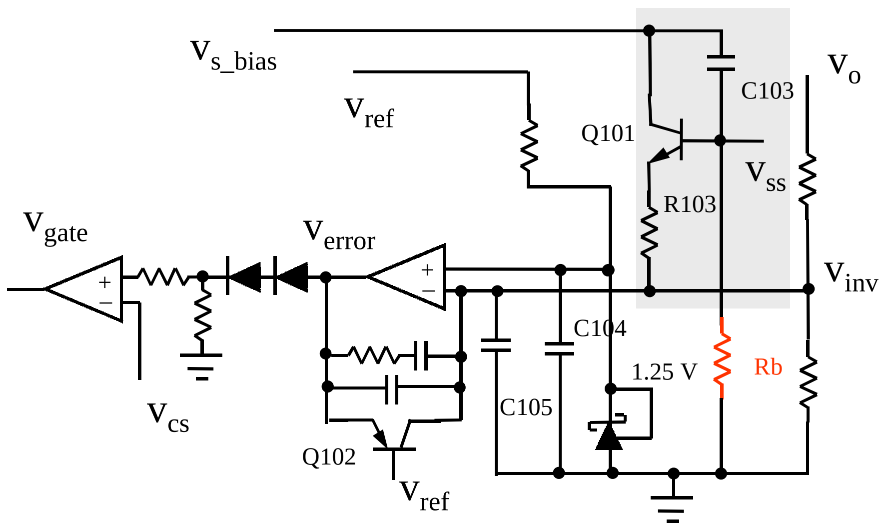


Fig. 4.42 Simplified control and soft-start circuit diagram.

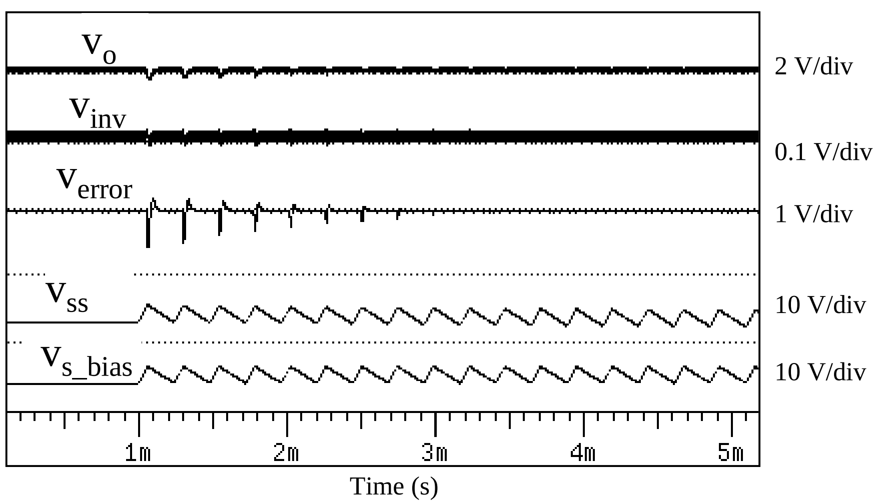


Fig. 4.43. Eliminate the low frequency output ripple of the main converter by redesigning the resistor R_b in the soft-start circuit.

4.7.2.2 Power supply interactions during large-signal transients

Large-signal transient analysis shows that the worst case transient response of the bias voltage happens during a line step from 36V to 72V when I_{p_bias} = 80 mA and I_{s_bias} = 40 mA. A voltage source with a step change from 12 V to 13 V and rising rate 60 us/V is used to represent the worst case of the dynamic response in the bias power supply. The sensitivity of an early development version of the main power supply is shown in Fig. 4.44. The main output voltage v_o shows a 30 mV dip due to the secondary bias voltage variations during the line transient.

Similar to the previous section about the ripple voltage of the secondary bias, this problem can be solved by adjusting the bypass resistor R_b in the soft-start circuit. The simulation waveforms after adjusting the resistor R_b are shown in Fig. 4.45. The output variation of the main power converter is eliminated.

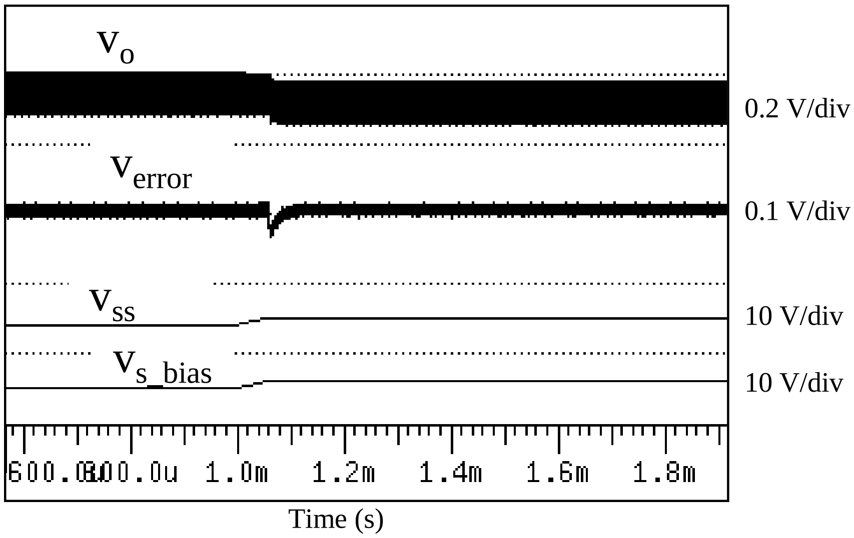


Fig. 4.44. The output voltage of the main converter has a 30 mV voltage dip due to the dynamic response of the bias power supply during line transient.

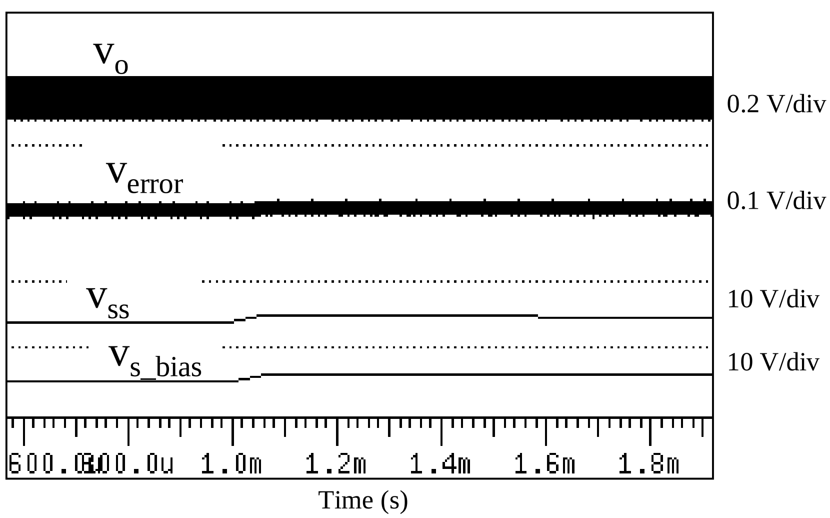


Fig. 4.45. Eliminate the interaction of the bias power supply with the main power supply during transient by adjusting the bypass resistor R_b in the soft-start circuit.

4.7.3 System start up sequence

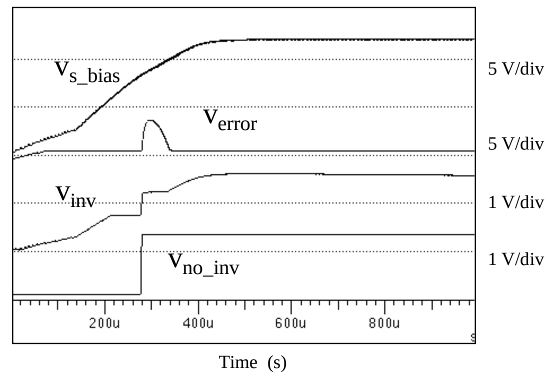
Since the system start-up usually requires a long-term simulation, it is wise to reduce unnecessary system complexity before simulation. The simulation methodology is to de-couple the main power supply and the bias power supply without losing the behavior of the power supply system. The simulation procedure is to split the whole start-up test into two intervals. The first interval is the period before the output of the main converter begins rising, the second interval is the period after the bias power supply approaches a steady state and all the control and protection circuits are operating normally.

Before the output voltage of the main power supply starts up, the main power stage is inactive, so it can be eliminated in the simulation. The gate drive signal of the main power supply is monitored to verify the inactive state of the main power stage. All the output signals of the control circuits are monitored to verify the correct sequence during the system start-up. The simulation period for the first interval is 2 mS and the CPU time is 4 minutes.

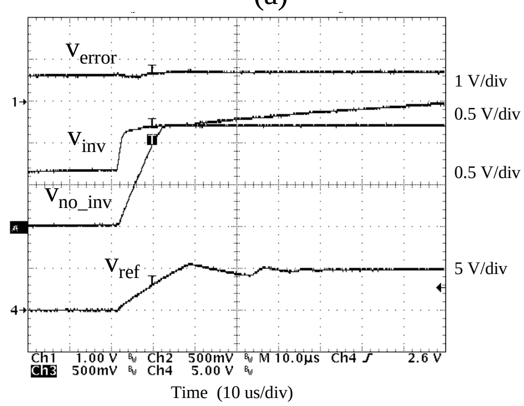
Fig. 4.46(a) shows the simulation waveforms of the control circuit signals of the main power supply as the entire power system starts up. The output voltage of the error amplifier V_{error} shows a "bump" during the bias voltage ramp-up. This is because the voltage of the non-inverting pin of the error amplifier v_{no_inv} is larger than the voltage of the inverting pin v_{inv} during the "bump" period. This "bump" could possibly turn on the main converter for a short period during start-up. However, the measurement in Fig. 4.46(b) does not show any "bump" during the bias voltage ramp-up period. By comparing the simulation and the measurement, we find that V_{inv} ramps up at a slower rate in the actual circuit because the PWM reference voltage of the controller chip rises rather slowly. The slew rate of the PWM reference voltage of the controller chip needs to be modeled in order to capture this behavior. This also shows that it is important to control the relative timing of the v_{inv} and v_{no_inv} signals during start-up. To confirm this understanding, in Fig. 4.46(c), we added a capacitor across the inverting pin of the error amplifier to slow its slew rate.

The second interval of the test starts after the secondary bias power supply reaches a steady state and all the control and protection circuits start to operate normally. The bias power supply can then be replaced by a constant voltage source in this test. The main power supply is included in the test to verify the control and protection circuits design during the main power supply start-up. This test is covered in the main power supply start-up test.

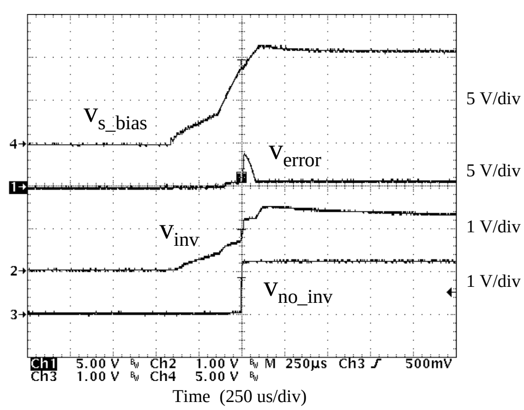
It is important to mention that the CPU time is about 100 minutes if both power supplies are included in the whole system start-up test. Even if the simulation CPU time is not critical for a single simulation, in practice, many simulation iterations are needed for design verification. Using the proposed procedure can reduce the simulation time dramatically.



(a)



(b)



(c)

Fig. 4.46 Verification of start-up sequence of the power supply system before the output voltage of the main power supply starts up. (a) simulation waveforms. (b) measurement. (c) verification of the circuit sensitivity to the timing of the input pins of the error amplifier during start-up.

4.7.4 System shut down sequence

The system shut down test is very straightforward. The component level of the power stage block for the shut down test is M1 as shown in Table 4.1 We will not discuss it in detail.

4.7.5 Summary of system interaction

Table 4.10 is the summary of test conditions and CPU times for the system interaction test of the main power supply.

Table 4.10. Summary of test conditions and CPU times for the system interaction test

Test type	Test condition			Simu time (s)	Total number of tests	CPU time (min)
	Vin	Io	Other			
System interaction with bias power supply	Vnorm	--	--	--	5	10
System start-up sequence	Vl, Vnorm, Vh (3)	Imin, 50%*Ifull, Ifull, (3)	--	3 m	9	45
System shut down sequence	Vl, Vnorm, Vh (3)	Imin, 50%*Ifull, Ifull, (3)	--	20 m	9	54
Total	--	--	--	--	23	109

4.8 Summary

This chapter demonstrates the virtual prototype test procedure to verify both the component and the system level performance of a complex power supply design. The simulation capability illustrated in this chapter can enable a designer to detect design problems before building a first prototype contributing to a significant reduction in the design cycle time. Fig. 4.47 is the summary of virtual prototype test numbers and simulation CPU time. For total 776 test, the simulation CPU time is 7.7 hours.

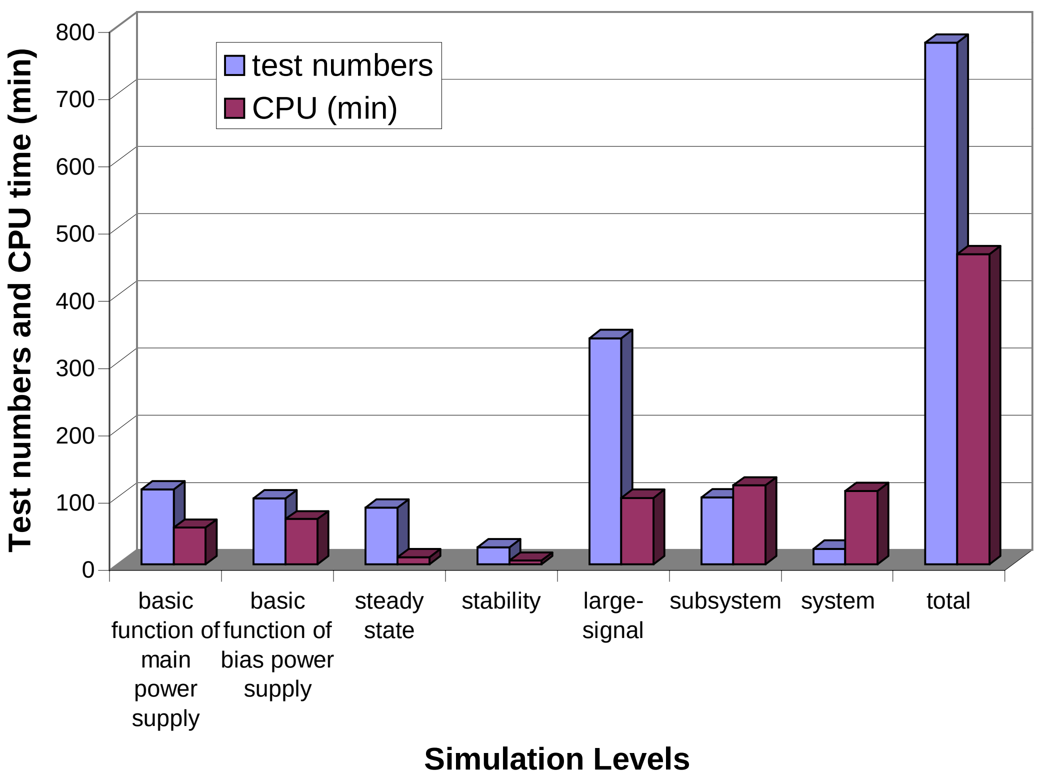


Fig. 4.47. Summary of virtual prototype DVT total number of tests and simulation CPU time.

5. ANALYSIS OF ANOMALIES OF THE ACTIVE-CLAMP FORWARD CONVERTER WITH THE AID OF VIRTUAL PROTOTYPE

5.1 Introduction

In previous chapter, several problems are detected which related to the active-clamp reset circuit of the forward converter. Since one parameter change in active-clamp reset circuit affects many responses of the circuit, it is very time consuming to adjust the circuit parameters to fix problems in each test and make trials and errors to verify all the other test. A better solution is to understand and predict the possible problems of the circuit and design the circuit with considering of all the design issues.

The virtual prototype developed in previous chapters can change parameter values in the circuit and run a series of simulations in a short simulation CPU time. This shows more advantages in analyzing, debugging, and redesigning the circuit compared to the hardware prototype as follows:

- It is easier to simulate any part of the circuit and vary any parameter values in circuit topologies using simulation. Comparing the differences of the simulation results among these changes can help us to understand the circuit and find the solution to solve the problems.

- Most of the times, the analytical equations of the circuit is very hard to derive, simulation can get the characteristic curves of a circuit easily and provide the information needed in a design.

In this chapter and next chapter, we will demonstrate how to analyze and design the active-clamp-reset circuit in the forward converter with the aid of virtual prototype simulation. From previous simulation, it shows that there are several design problems in the active-clamp reset circuit: a large dc bias of the magnetizing current of the power transformer causes the loss of ZVT in active-clamp switch; the interaction of the reset circuit to forward converter reduces the phase margin of small signal loop gain; and the resonant of the magnetizing current and clamp capacitor causes a high peak of the output voltage of the main switch during transient and abnormal conditions. We will analysis these anomalies of the active-clamp forward converter in this chapter and propose a design guideline to solve these problems in the next chapter.

5.2 Effect of component parasitics to steady state behavior

A number of papers have discussed design issues relate to the active clamp reset mechanism [55-69]. The negative dc bias of the magnetizing current in the active clamp circuit has been observed and mentioned in the literature [56]. However, no detailed analysis and explicit equations have been provided in the paper. It is very important to estimate the dc bias of the magnetizing current before the prototyping, so that the dc bias can be considered in the original transformer design.

In this section, we all show that there is a positive or a negative dc bias of the magnetizing current of the transformer in the circuit due to the parasitic capacitance, C_s, and the leakage inductance, L_{lk}. This dc bias could saturate the transformer, cause diode reverse recovery problem, and make the active clamp switch lose zero voltage turn-on. This paper will analyze the dc operation of the active clamp circuit with the parasitic parameters L_{lk} and C_s, and derive the numerical equations of the dc bias to verify the observation in the simulation. The design guideline regarding the dc bias of the transformer will be discussed in the next chapter. It is the first time that a numerical equation of the dc bias of the magnetizing current has been provided.

5.2.1 Simulation observations

From previous simulation, we found that the dc bias of the magnetizing current was not shown in the power stage test (Fig. 5.1), but shown in the loss analysis test as in Fig. 5.2. Comparing the simulation schematics, we found the major differences in these two tests are the capacitance of the devices and the leakage inductance of the transformer is included in loss analysis test.

We will simulate the circuit by including each individual parasitic parameter separately to see the effect of each parameter. Fig. 5.3 shows the simulation waveform with the parasitic capacitances included in the schematics and Fig. 5.4 shows the simulation waveform with the leakage inductance of the transformer included in the schematics. The circuit condition is at nominal: Vin = 48 V and Io = 15 A. We see that the parasitic capacitances introduce a positive dc bias of the magnetizing current, while the leakage inductance of the transformer introduces a negative dc bias of the magnetizing current. Comparing with the simulation with both parameters in the simulation as in Fig. 5.2, we see that the bias of the magnetizing current is closed to the sum of each bias value.

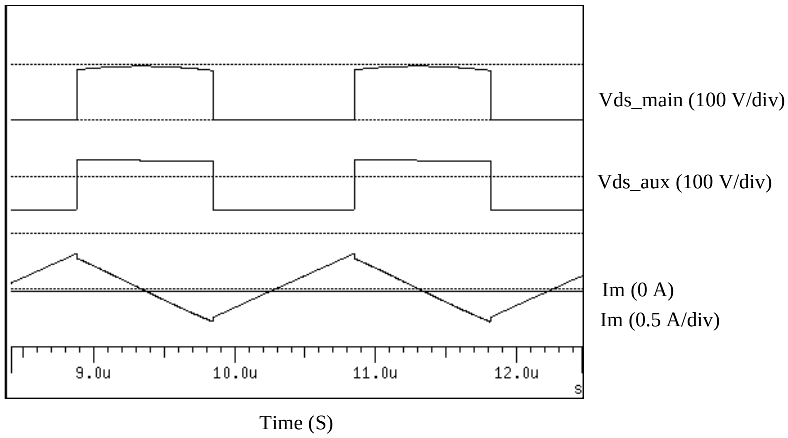


Fig. 5.1 Simulation of the power stage test without parasitic parameters of devices and transformer does not show the dc bias of the magnetizing current of the transformer.

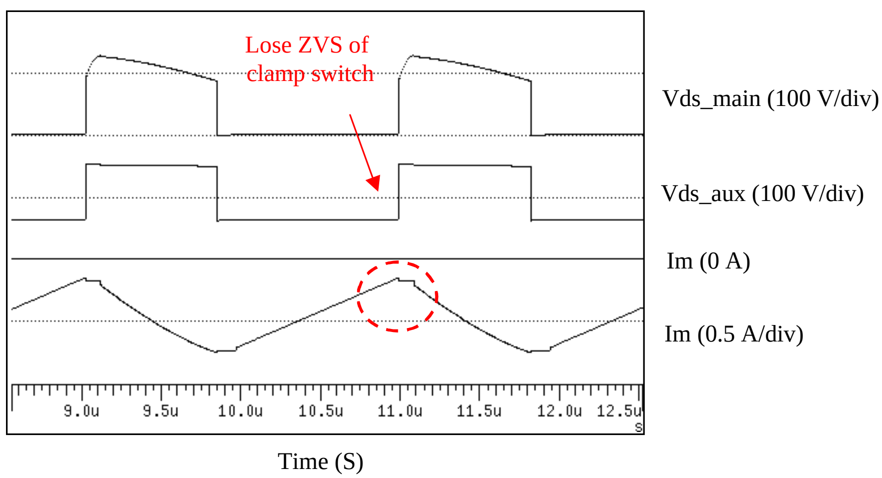


Fig. 5.2. With the leakage inductance of the transformer and parasitic capacitances of devices, there is a dc bias of the magnetizing current in steady state operation. The circuit loses ZVS of active clamp switch as shown in the figure.

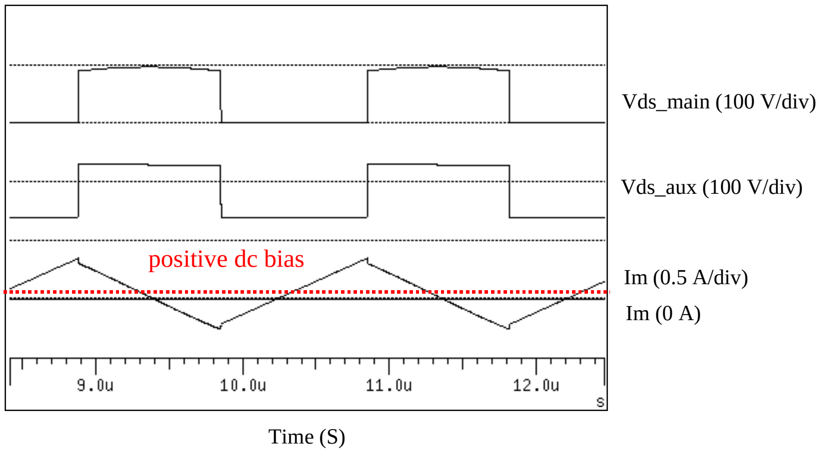


Fig. 5.3 simulation waveform with parasitic capacitances has a positive dc bias of the magnetizing current of the transformer.

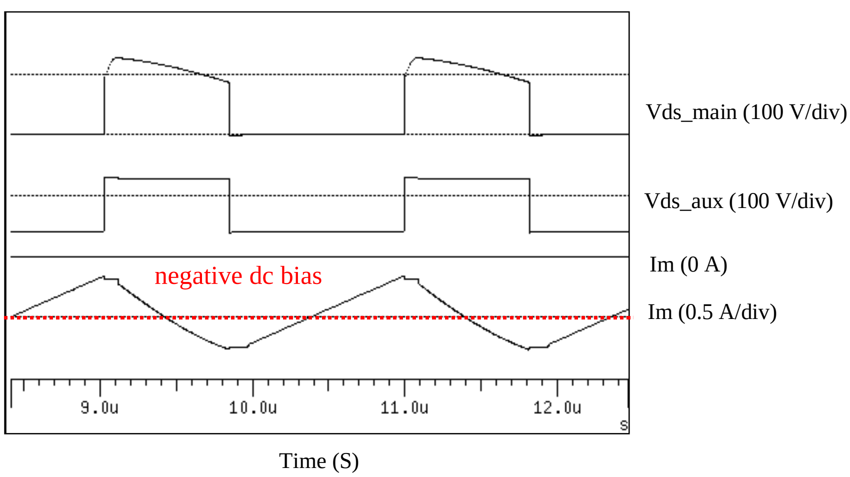


Fig. 5.4 Simulation waveform with leakage inductance capacitances has a negative dc bias of the magnetizing current of the transformer.

Fig. 5.5 shows the bias magnetizing current curves with different input voltages, loads, and the parasitic capacitances, C_s. The parasitic capacitances introduce a positive dc bias of the magnetizing current. The worst case of the positive dc bias occurs at low line and large C_s, the load has no effect of the dc bias in this condition.

Fig. 5.6 shows the dc bias magnetizing current curves with input voltage, loads, and the leakage inductance, L_{lk}. The leakage inductance introduces a negative dc bias of the magnetizing current. The worst case of the negative dc bias occurs at full load and large L_{lk}, the input voltage has no effect of the dc bias in this condition.

If the observation is correct, we can use simulation to provide design curves and generate a design procedure according to these simulation curves. First we will analyze the circuit operation to verify the observations in the simulation.

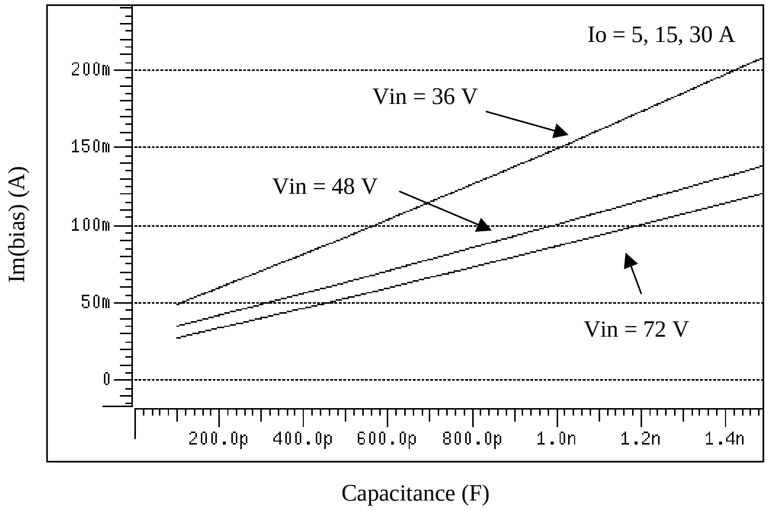


Fig. 5.5. The parasitic capacitances introduce a positive dc bias of the magnetizing current. Load has no effect of the dc bias.

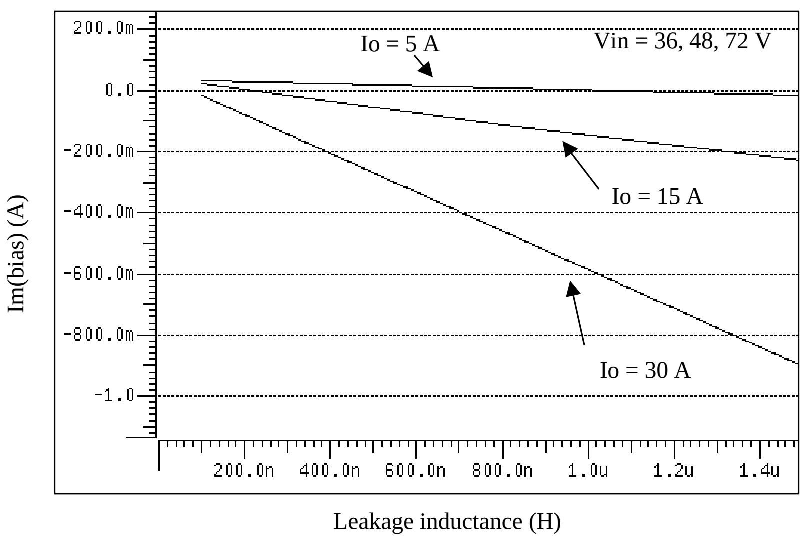


Fig. 5.6. The leakage inductance introduces a negative dc bias of the magnetizing current. The input voltage has no effect of the dc bias.

5.2.2 Analysis of the effect of the parasitic capacitance and the leakage inductance of the transformer

5.2.2.1 Design issues

As described in the previous section, the average magnetizing current i_m over one switching cycle is zero in an ideal circuit. However, there is a positive or negative dc bias of the transformer magnetizing current in steady state when the parasitic capacitance C_s, and the leakage inductance of the transformer L_{lk} are considered. The circuit diagram is shown in Fig. 5.7, in which C_s is the total equivalent parasitic capacitance of the main switch, S_1, active clamp switch, S_2, and the transformer, and L_{lk} is the leakage inductance of the transformer.

In this section, we will show that the amplitude of the dc bias of the magnetizing current is a function of C_s, L_{lk}, input voltage, and load. The positive dc bias is due to the extra energy stored in the parasitic capacitance, and the negative dc bias is due to the extra energy stored in the leakage inductance of the transformer. A large positive dc bias could saturate the transformer core or have diode reverse recovery problem; and a large negative dc bias could saturate the transformer core or lose ZVS of the active-clamp switch as shown in Fig. 5.8. This section is going to explain the dc bias phenomenon and derive the explicit equation of the dc bias of the magnetizing current, so that the problem related to the dc bias current can be considered in the original transformer design.

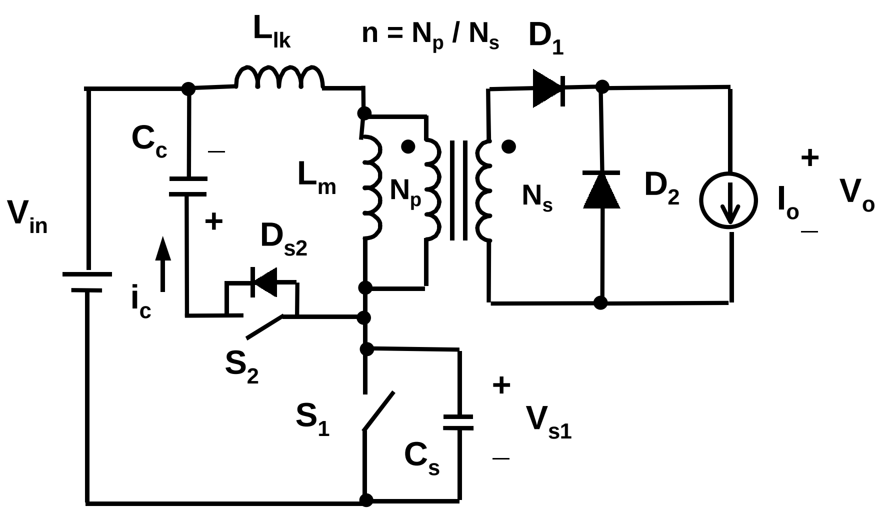


Fig. 5.7. Circuit diagram of the active-clamp forward converter with the equivalent parasitic capacitance C_s and the leakage inductance of the transformer L_{lk}.

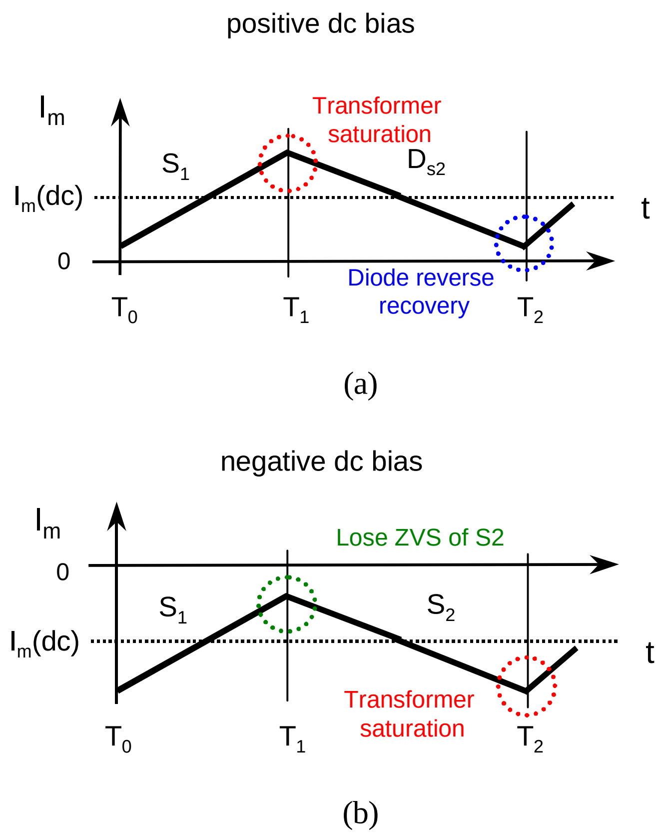


Fig. 5.8. Problems due to the dc bias of the magnetizing current of the transformer. (a) a large positive dc bias could saturate the transformer core or have diode reverse recovery problem. (b) a large negative dc bias could saturate the transformer core or lose ZVS of the active-clamp switch turn-on.

5.2.2.2 Positive dc bias of the magnetizing current

Fig. 5.9 shows the steady state operation waveforms of the active-clamp forward converter with a positive dc bias of the magnetizing current. The positive dc bias of the magnetizing current happens when the energy stored in the leakage inductance L_{lk} is less than the energy stored in the parasitic capacitance C_s. Because of the parasitic capacitance and the leakage inductance, the operation of the circuit in Fig. 5.7 is slightly different than the one we discussed in chpater 4. The difference can be seen after main switch S_1 is turned off. There are six stages during a switching cycle.

Stage 1 [T_0 - T_1]: After the main switch S_1 is turned on at t = T_0, the output current I_o flows through rectifier D_1, inducing a current in the primary winding of the transformer. L_m is charged by input voltage V_{in}. As a result, the main switch current i_{s1} during this interval is given by

$$i_{s1} = i_m + \frac{I_o}{n}. \tag{5.1}$$

This topological stage ends at t = T_1, when the main switch S_1 is turned off.

Stage 2 [T_1 - T_2]: After the main switch S_1 is turned off at T_1, capacitor C_s is charged by the reflected load current in the primary winding, $\frac{I_o}{n}$. This stage ends when v_{s1} reaches the input voltage V_{in} at T_2.

Stage 3 [T_2 - T_3]: After v_{s1} reaches V_{in}, the secondary voltage becomes equal to zero, and the transformer is shorted. Since the current in rectifier D_1 cannot be reduced to zero immediately due to the leakage inductance, D_1 and D_2 are simultaneously conducting during this period. The leakage inductance i_{lk} starts to resonate with C_s. This stage terminates at t = T_3, when the current in D_1 decreases to zero and the leakage inductance current i_{lk} becomes equal to the magnetizing current i_m. During this stage, the magnetizing current keeps constant since the primary and the secondary of the transformer are shorted.

Stage 4 [T_3 - T_4]: At T_3, D_1 disconnects, and the transformer is an open circuit. Since the energy stored in C_s is larger than the energy in L_{lk}, C_s has not been charged to $V_{in} + V_c$ at T_3. L_m and L_{lk} continue to resonate with C_s until $v_{s1} = V_{in} + V_c$ at T_4.

Stage 5 [T_4 - T_4^*]: At T_4, current in the leakage inductance and the magnetizing inductance continues to flow through the anti-parallel diode of switch S_2 and clamp capacitor C_c. Due to a negative voltage V_c across the magnetizing inductance, i_m decreases. If capacitance C_c is assumed large so that the ripple of the clamp voltage V_c is small compared to the dc component, the downslope of i_m is constant. This stage ends, when i_m reaches zero at t = T_4^*. The active clamp switch, S_2, can be turned on anytime during this period with ZVS.

Stage 6 [T_4^* - T_5]: When the current in the anti-parallel diode of switch S_2 reaches zero at T_4^*, the active clamp switch S_2 starts to conduct. The magnetizing current, $i_{m,}$ will continue to flow in the opposite direction through S_2. This stage ends at t = T_5, when switch S_2 is turned off.

According to the charge balance, the shaded area of i_c during [T_4 - T_4^*] interval is equal to the one during [T_4^* - T_5] interval as shown in Fig. 5.9, i.e. $i_c^+ = i_c^-$. The magnetizing current i_m follows the charge current i_c during [T_4 - T_5] interval, but during [T_3–T_4] interval, C_s is charged by i_m and i_{lk}. Since $L_m >> L_{lk}$, L_{lk} is neglected. The additional variation of i_m in this period induces additional magnetizing current, i.e., $I_m^+ > I_m^-$, where, $I_m^+ = i_m(t_3)$ and $I_m^- = i_m(t_5)$.

In order to maintain the flux balance, there is a positive dc bias of the magnetizing current in the transformer as shown in Fig. 5.9. If the dc bias of the magnetizing current is too large, I_m^- is positive during the whole switching cycle, the magnetizing current is still conducting through the anti-parallel diode of the active-clamp switch S_2 when the main switch S_1 is turned on. As a result, there is a large diode reverse recovery current conducting through diode D_{s2} to the main switch, S_1, which could damage the semiconductor devices.

According to the energy balance during [T_2 - T_5],

$$\begin{aligned}&\frac{1}{2}\cdot L_{lk}\cdot i_{lk}(t_2)^2+\frac{1}{2}\cdot L_m\cdot i_m(t_2)^2-\frac{1}{2}\cdot\left(L_{lk}+L_m\right)\cdot i_m(t_5)^2\\&=\frac{1}{2}\cdot C_S\cdot\left(v_s(t_5)-V_{in}\right)^2-\frac{1}{2}\cdot C_S\cdot\left(v_s(t_2)-V_{in}\right)^2\end{aligned},\qquad(5.2)$$

where

$$i_{lk}(t_2)=\frac{I_o}{n}+i_m(t_2)\qquad(5.3)$$

$$i_m(t_2)=i_m(t_3)=I_m{}^{+}\qquad(5.4)$$

$$i_m(t_5)=I_m{}^{-}\qquad(5.5)$$

$$v_s(t_2)=V_{in}\qquad(5.6)$$

$$v_s(t_5)=V_{in}+V_c\qquad(5.7)$$

When $\frac{I_o}{n} >> i_m$, we can simplify (5.2) to:

$$\frac{1}{2}\cdot L_m\cdot\left(I_m{}^{+}\right)^2-\frac{1}{2}\cdot L_m\cdot\left(I_m{}^{-}\right)^2\approx\frac{1}{2}\cdot C_S\cdot V_c{}^2-\frac{1}{2}\cdot L_{lk}\cdot\left(\frac{I_o}{n}\right)^2\qquad(5.8)$$

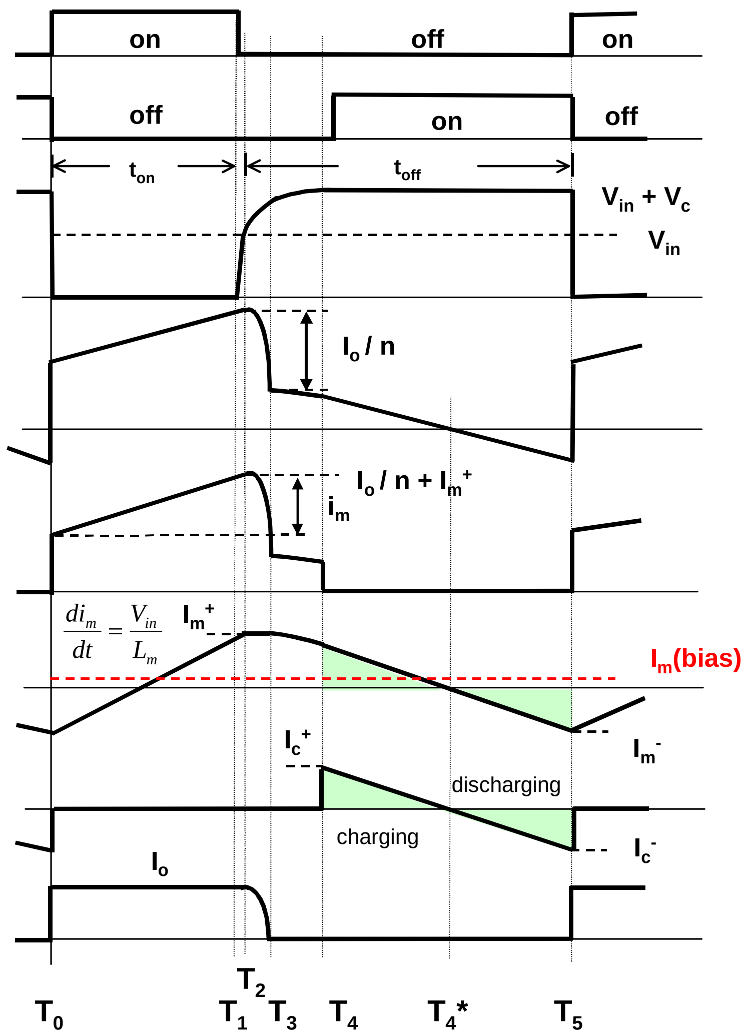


Fig. 5.9. Circuit operation waveforms with positive dc bias of the magnetizing current.

5.2.2.3 Negative dc bias of the magnetizing current

Fig. 5.10 shows the steady state operation waveforms of the active-clamp forward converter with a negative dc bias of the magnetizing current. The negative dc bias of the magnetizing current happens when the energy stored in the leakage inductance L_{lk} is larger than that in the parasitic capacitance C_s. There are six stages during a switching cycle, in which stages 1, 2, 5, and 6 are the same as in the positive dc-bias current case. Only stage 3 and 4 are different, which are [T_2 - T_3] and [T_3 - T_4] intervals.

Stage 3 [T_2 - T_3]: After main switch S_1 is turned off and v_{s1} reaches V_{in} at T2, the secondary voltage becomes equal to zero, and the transformer is shorted. Since the current in the rectifier diode D_1 cannot be reduced to zero immediately due to the leakage inductance of the transformer, D_1 and D_2 are simultaneously conducting during this period. The leakage inductance i_{lk} resonates with C_s until C_s is charged to $V_{in} + V_c$ at T_3.

Since the energy stored in L_{lk} is larger than the energy in C_s, the leakage inductance current i_{lk} is larger than the magnetizing current i_m at T_3. During this stage, the magnetizing current keeps constant since the primary and the secondary of the transformer are shorted.

Stage 4 [T_3 - T_4]: At T_3, current in the leakage inductance, which is larger than the magnetizing current, continues to flow through the anti-parallel diode of switch S_2 and resonate with the clamp capacitor C_c. D_1 and D_2 are still simultaneously conducting during this stage, and the magnetizing current keeps constant since the primary and the secondary of the transformer are shorted. This stage terminates at $t = T_4$, when the leakage current i_{lk} is equal to the magnetizing current i_m. At T_4, D_1 disconnects, and the transformer is an open circuit. At the next stage, L_m and L_{lk} start to resonate with C_c, which is the same as discussed in the positive dc-bias current case.

According to the charge balance, the shaded area of i_c during $[T_3 - T_4^*]$ interval is equal to $[T_4^* - T_5]$ as shown in Fig. 5.10. During $[T_3 - T_4]$, C_c is charged by leakage inductance i_{lk}. The magnetizing current i_m only follows i_c during $[T_4 - T_5]$, the two shaded area of i_m is not equal. i.e., $I_m^+ < I_m^-$, where $I_m^+ = i_m(t_4)$ and $I_m^- = i_m(t_5)$. In order to maintain the flux balance, there is a negative dc bias of the magnetizing current in the transformer as shown in Fig. 5.10.

If the dc bias of the magnetizing current is too large, I_m^+ is negative when v_{s1} reaches $V_{in} + V_c$ at T_2. As a result, the current flows through the active-clamp switch, S_2, instead of the anti-parallel diode when S_1 is turned off and S_2 is turned on. In this condition, S_2 is turned on with hard switching, that increase the loss of the circuit.

According to the energy balance during $[T_2 - T_5]$,

$$\begin{aligned}&\frac{1}{2}\cdot L_{lk}\cdot i_{lk}(t_2)^2+\frac{1}{2}\cdot L_m\cdot i_m(t_2)^2-\frac{1}{2}\cdot\left(L_{lk}+L_m\right)\cdot i_m(t_5)^2\\&=\frac{1}{2}\cdot C_S\cdot\left(v_s(t_5)-V_{in}\right)^2-\frac{1}{2}\cdot C_S\cdot\left(v_s(t_2)-V_{in}\right)^2\end{aligned}, \tag{5.9}$$

where

$$i_{lk}(t_2)=\frac{I_o}{n}+i_m(t_2) \tag{5.10}$$

$$i_m(t_2)=i_m(t_3)=i_m(t_4)=I_m^+ \tag{5.11}$$

$$i_m(t_5)=I_m^- \tag{5.12}$$

$$v_s(t_2)=V_{in} \tag{5.13}$$

$$v_s(t_5)=V_{in}+V_c \tag{5.14}$$

When $\frac{I_o}{n} >> i_m$, we can simplify (5.9) to:

$$\frac{1}{2} \cdot L_m \cdot \left(I_m^{\ +}\right)^2 - \frac{1}{2} \cdot L_m \cdot \left(I_m^{\ -}\right)^2 \approx \frac{1}{2} \cdot C_S \cdot V_c^{\ 2} - \frac{1}{2} \cdot L_{lk} \cdot \left(\frac{I_o}{n}\right)^2 \tag{5.15}$$

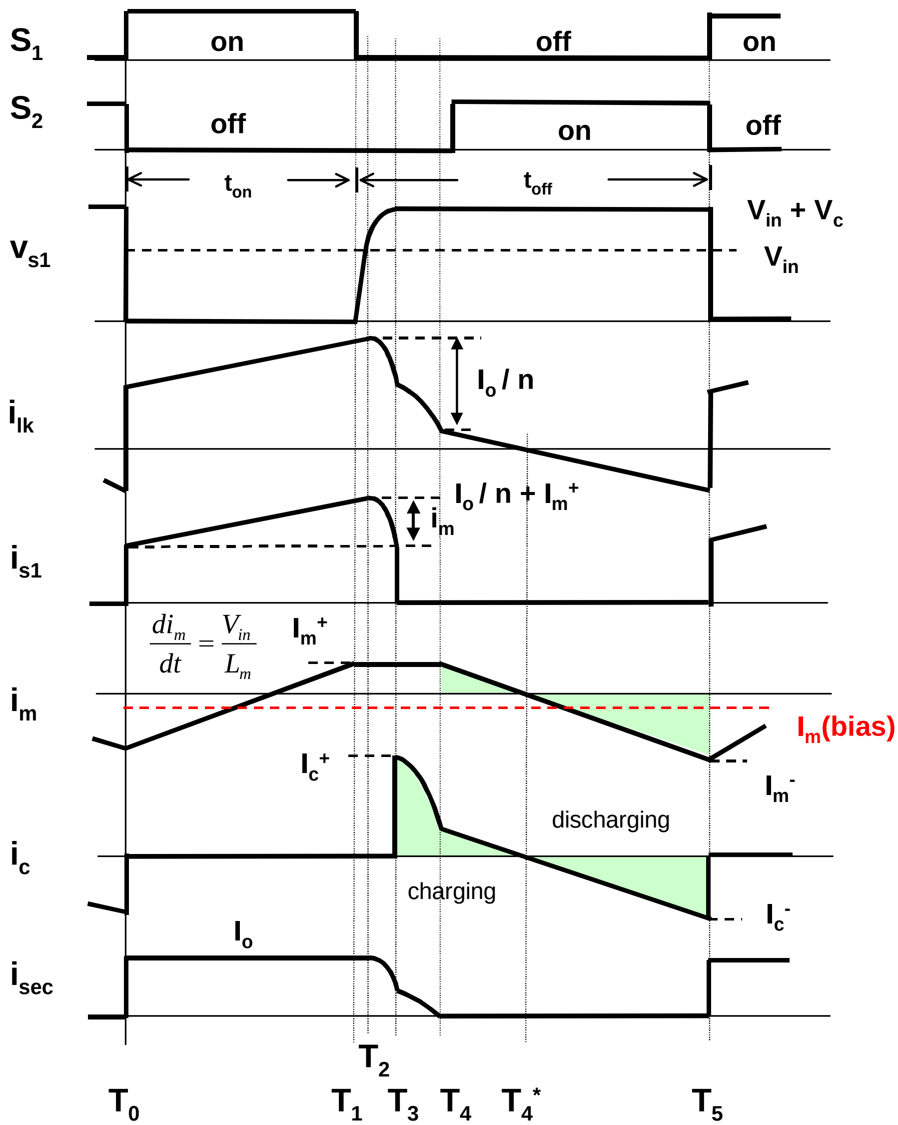


Fig. 5.10. Circuit operation waveforms of the negative dc bias of the magnetizing current.

5.2.3 Derivation of the dc bias of the magnetizing current

According to the energy balance equations (5.8) and (5.15), for both the positive and the negative dc-bias current, we get:

$$\frac{1}{2}\cdot L_m\cdot\left(I_m^{+}\right)^2-\frac{1}{2}\cdot L_m\cdot\left(I_m^{-}\right)^2=\frac{1}{2}\cdot C_S\cdot V_c^{2}-\frac{1}{2}\cdot L_{lk}\cdot\left(\frac{I_o}{n}\right)^2 \tag{5.16}$$

This equation can also be written as

$$\frac{1}{2}\cdot L_m\cdot\left(I_m^{+}+I_m^{-}\right)\cdot\left(I_m^{+}-I_m^{-}\right)=\frac{1}{2}\cdot C_S\cdot V_c^{2}-\frac{1}{2}\cdot L_{lk}\cdot\left(\frac{I_o}{n}\right)^2 \tag{5.17}$$

Since [T_1-T_2] interval is very short, the peak to peak magnetizing current can be approximated by

$$I_m(pp)=I_m^{+}-I_m^{-}=\frac{V_{in}\cdot D\cdot T_s}{L_m} \tag{5.18}$$

Let

$$I_m(bias)=\frac{1}{2}\cdot\left(I_m^{+}+I_m^{-}\right) \tag{5.19}$$

$$E_{Cs}=\frac{1}{2}\cdot C_s\cdot V_c^{2} \tag{5.20}$$

$$E_{Llk}=\frac{1}{2}\cdot L_{lk}\cdot\left(\frac{I_o}{n}\right)^2 \tag{5.21}$$

where I_m(bias) is the dc bias of the magnetizing current, E_{cs} is the energy stored in the parasitic capacitance C_s, and E_{Llk} is the energy stored in the leakage inductance L_{lk}.

Replacing (5.17) with (5.18) - (5.21), the dc bias of the magnetizing current can be written as

$$I_m(bias) = \frac{E_{Cs} - E_{Llk}}{V_{in} \cdot D \cdot T_s} \tag{5.22}$$

In addition, the maximum magnetizing current is:

$$I_m(\max) = |I_m(bias)| + \frac{1}{2} \cdot I_m(pp) = \frac{|E_{Cs} - E_{Llk}|}{V_{in} \cdot D \cdot T_s} + \frac{V_{in} \cdot D \cdot T_s}{2 \cdot L_m} \tag{5.23}$$

The terms in the equations are defined as in Fig. 5.11. Fig. 5.12 shows the simulation and calculation results of the dc bias of the magnetizing current under different input voltage and load conditions. The circuit specification is: V_{in} = 100 - 400 V, V_o = 5 V, I_o = 0 - 20 A with L_{lk} = 5 uH and C_s = 600 pF. The simulated curves are dotted lines and the calculated curves are solid lines. The results match very well. Fig. 5.12 shows that the negative dc bias is more severe than the positive dc bias, due to the range of the parameter values. The negative bias magnetizing current is the major concern in an practical circuit design.

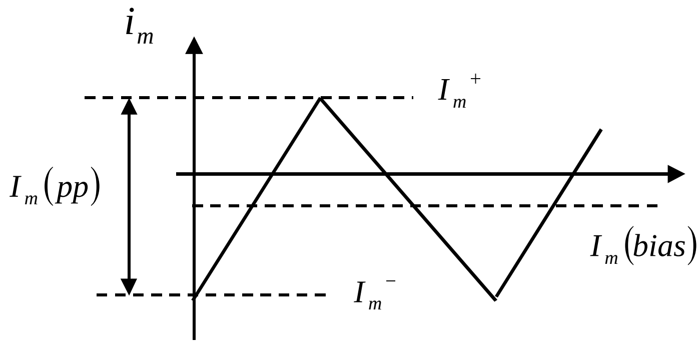


Fig. 5.11. Definition of the terms in the bias magnetizing current equations.

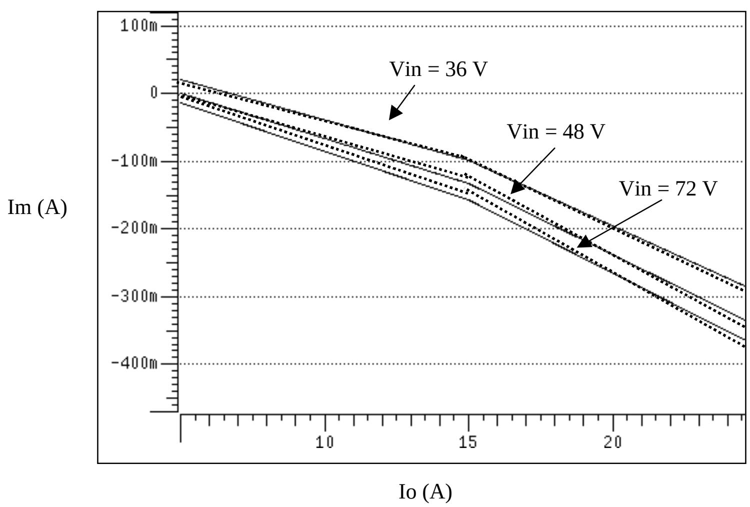


Fig. 5.12. Simulated and calculated dc bias curves with different loads and input voltages when L_{lk} = 0.8 uH and C_s = 100 pF. Solid lines: simulation. Dotted lines: calculation.

5.3 Effect of active clamp reset circuit to large signal transients

5.3.1 Simulation observations

From previous virtual prototype DVT, several problems detected are related to the dynamic responses of the active-clamp-reset circuit in large signal transients. It shows that there could be a large peak switch voltage and magnetizing current which is much larger then the ones in steady state in large-signal transient and circuit abnormal conditions. These dynamic behaviors could cause switch voltage stress, transformer saturation, or diode of the active clamp switch reverse recovery problems. The transient waveforms during load change and short circuit test are redrawn in Fig. 5.13 - Fig. 5.16. The solution to these problems is not obvious from simulation observation, we will analyze the transient behavior of the circuit before the design modifications.

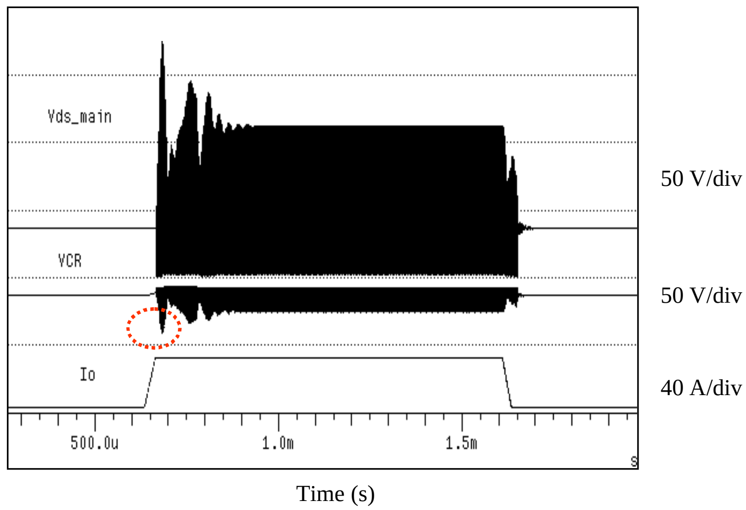


Fig. 5.13 Large-signal response waveforms at Vin = 36 V, Io from no load to full load to no load transient. Load step slew rate is 1 A/us. V_{CR} exceeds the device rating.

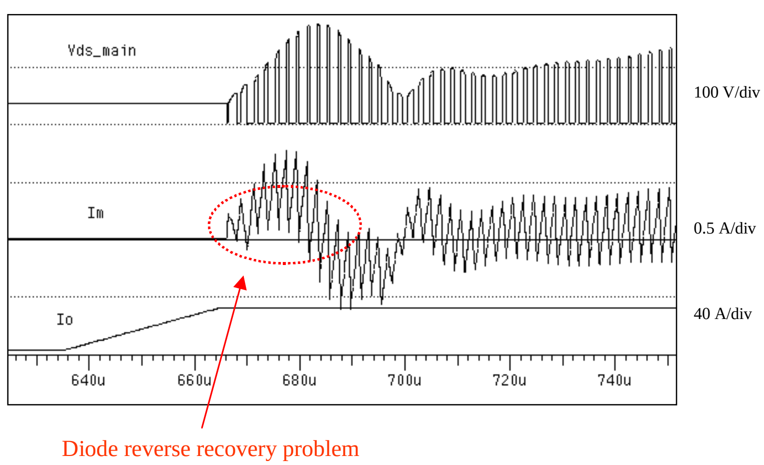


Fig. 5.14 Simulation shows there is a diode reverse recovery problem during no load to full load transient at Vin = 36 V.

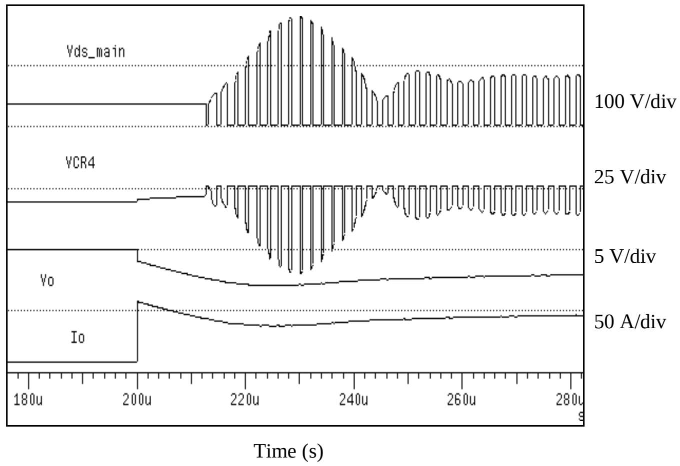


Fig. 5.15 Short circuit test waveform at Vin = 36 V, Io = 0 A.

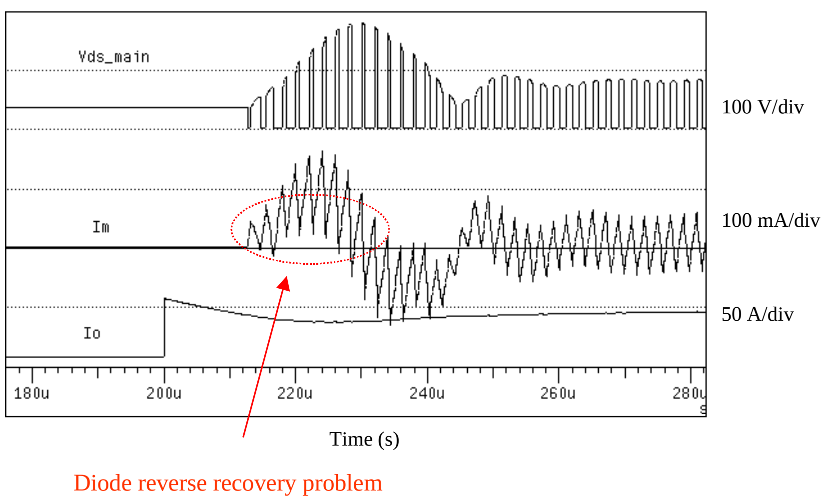


Fig. 5.16. Short circuit test at Vin = 36 V, Io = 0 A. The marked area shows diode reverse recovery problem of the active-clamp circuit due to a positive magnetizing current in a short period.

5.3.2 Design issues

In order to solve the circuit problems in large-signal transient, we need to understand the dynamic behavior of the circuit. Since a forward converter with current mode control has more non-linear characteristics than the one with voltage feedback control, we will start from a simple case, i.e., an active-clamp forward converter with voltage mode control. The simplified circuit diagram of the forward converter with the active-clamp reset with voltage feedback control is shown in Fig. 5.17. The active-clamp-reset circuit consists of the series connection of auxiliary switch S_2 and clamp capacitor C_C. It should be noted that transformer in Fig. 5.17 is shown as a parallel connection of the magnetizing inductance L_M and the ideal transformer with a turns-ratio $n = \frac{N_P}{N_S}$.

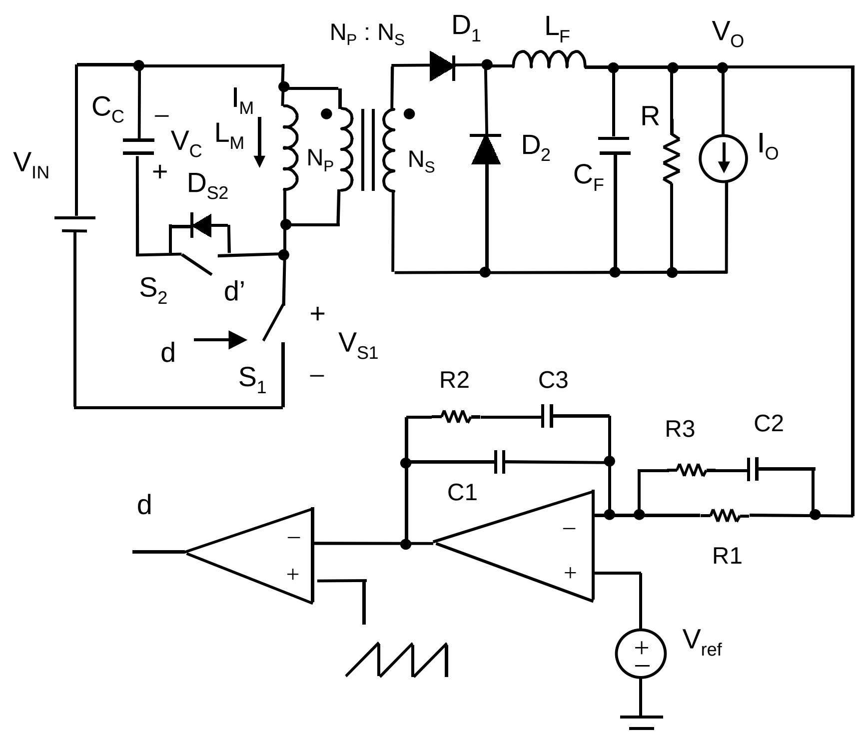


Fig. 5.17. Circuit diagram of active-clamp forward converter with voltage feedback control.

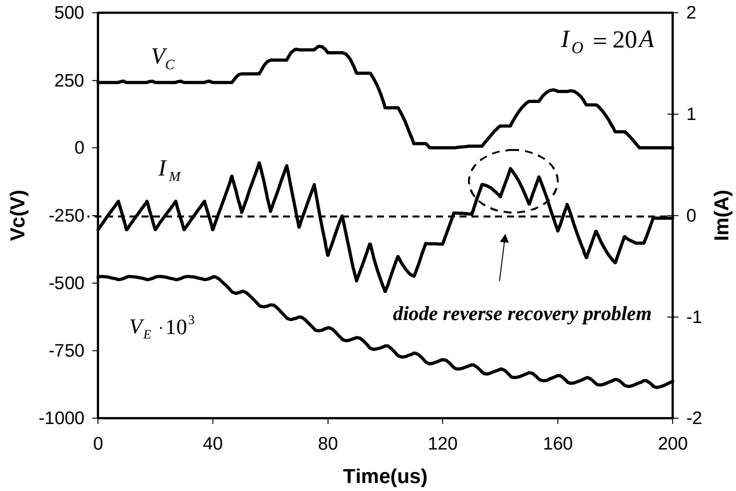
To illustrate the behavior of the forward converter with active-clamp reset, Fig. 5.18 shows the simulation results of the circuit in Fig. 5.17 with output-voltage feedback control during large-signal transients. Fig. 5.18(a) shows clamp-capacitor voltage V_C, magnetizing current of the transformer I_M, and output voltage of the error amplifier V_E during an input-voltage transient from 100 V to 200 V. Fig. 5.18(b) shows the same waveforms during a load transient from 18 A to 20 A. The circuit parameters are: L_M=2.5 mH, C_C=22 nF, maximum duty cycle D_{max}=0.7, switching frequency f_s=100 kHz, and control loop crossover frequency f_c=3.6 kHz.

As can be seen from Fig. 5.18(a) and (b), the peak voltage of the clamp voltage and magnetizing current during transients are much larger than the ripple voltage and current in steady state. Therefore, for a proper design of the circuit, it is very important to understand the circuit performance and predict the maximum stresses of the components during large-signal transients.

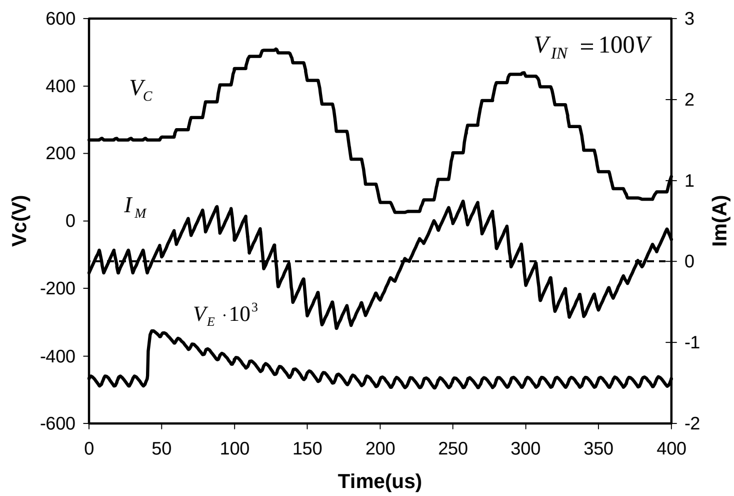
Specifically, before the input-voltage transient, the converter in Fig. 5.18(a) operates with a large duty cycle and with a balanced flux in the core so that $V_{IN} \cdot D = V_C \cdot (1-D)$. Since after the line change, the duty cycle and the clamp-capacitor voltage V_C does not change instantaneously, the volt-second product becomes unbalanced, i.e., $V_{IN} \cdot D > V_C \cdot (1-D)$. As a result, the magnetizing current of the transformer starts increasing after the input-voltage change. The increased magnetizing energy charges the clamp capacitor, increasing the clamp-capacitor voltage. This transition continues until V_C becomes large enough so that the volt-second product becomes $V_{IN} \cdot D < V_C \cdot (1-D)$, and the magnetizing current of the transformer starts to decrease. The described clamp-capacitor voltage increase and the subsequent decrease after the transient can be seen as an oscillatory response of the resonant circuit consisting of the clamp capacitor and the magnetizing inductance of the transformer. Similar resonant behavior during load transient can be observed in Fig. 5.18(b).

If the forward converter circuit with the active-clamp reset is not correctly designed, the peak clamp-capacitor voltage and magnetizing current during input-voltage and load transients may cause an excessive voltage stress on the primary switch and/or saturation of the core of the transformer. Yet another problem that may happen during transients is that the body diode of auxiliary switch S_2 may conduct due to a positive magnetizing current at the instant when main switch S_1 is turned on, as indicated in Fig. 5.18(a). If the auxiliary-switch body diode is conducting when the main switch S_1 is turned on, a slow reverse-recovery of the body diode may cause the failure of the circuit because of the low-impedance current path through the clamp capacitor, the auxiliary-switch body diode, and the main switch.

One approach to eliminate this problem is to connect a Schottky diode in series with the auxiliary switch to block the conduction of the body diode, and then to connect a fast-recovery anti-parallel diode around the series connection of the Schottky and the auxiliary switch [56]. The other approach is to design an active-clamp circuit, so that the magnetizing current is always negative at the instant main switch S_1 is turned on.



(a)



(b)

Fig. 5.18. Simulation results of large-signal transients of the forward converter with the active-clamp reset and output-voltage feedback control: (a) input-voltage step change from 100 V to 200 V; (b) load step change from 18 A to 20 A.

5.3.3 Large-signal analysis using state trajectory

State trajectory analysis is a very effectively tool for large-signal transient analysis [70-75]. We will first derive the stage trajectory equations for active-clamp circuit.

Fig. 5.19(a) and Fig. 5.19(b) are the simplified circuit diagrams during main switch S_1 turn-on and turn-off period, respectively. The state equations of v_c and i_m during S_1 on the period, Fig. 5.19(a), are

$$C_C \cdot \frac{dv_c}{dt} = 0\,, \tag{5.24}$$

$$L_M \cdot \frac{di_m}{dt} = V_{in}\,. \tag{5.25}$$

By solving (5.24) and (5.25), the state trajectory during the on time of S_1 can be described as

$$v_c(t) = v_c(t_0), \tag{5.26}$$

$$i_m(t) = \frac{V_{in}}{L_M} \cdot t + i_m(t_0), \tag{5.27}$$

where $v_c(t_0)$ is the initial value of the clamp-capacitor voltage and $i_m(t_0)$ is the initial value of the magnetizing current of the transformer at the main-switch-on instant. The state trajectory during this period is a line parallel to i_m axis with a constant v_c, as shown in Fig. 5.20.

During the off period, Fig. 5.19(b), the state equations of v_c and i_m are

$$C_C \cdot \frac{dv_c}{dt} = i_m\,, \tag{5.28}$$

$$L_M \cdot \frac{di_m}{dt} = -v_c \,. \tag{5.29}$$

By solving (5.28) and (5.29), the state trajectory during the off time of S_1 can be described as

$$v_c(t) = r \cdot \cos[\alpha - \omega_o(t) \cdot t], \tag{5.30}$$

$$i_m(t) \cdot Z_O = r \cdot \sin[\alpha - \omega_o(t) \cdot t], \tag{5.31}$$

$$v_c(t)^2 + [i_m(t) \cdot Z_o]^2 = r^2 \,, \tag{5.32}$$

where,

$$r = \sqrt{v_c(t_1)^2 + i_m(t_1)^2 \cdot Z_o^{\;2}} \,, \tag{5.33}$$

$$\alpha = \tan^{-1}\left(\frac{i_m(t_1) \cdot Z_o}{v_c(t_1)}\right), \tag{5.34}$$

$$\omega_o = \frac{1}{\sqrt{L_M \cdot C_C}} \;, \tag{5.35}$$

$$Z_o = \sqrt{\frac{L_M}{C_C}} \;, \tag{5.36}$$

$v_c(t_1)$ is the initial value of the clamp-capacitor voltage, and $i_m(t_1)$ is the initial value of the magnetizing current of the transformer at the turn-off instant of main switch S_1. The state trajectory during this period is shown in Fig. 5.20.

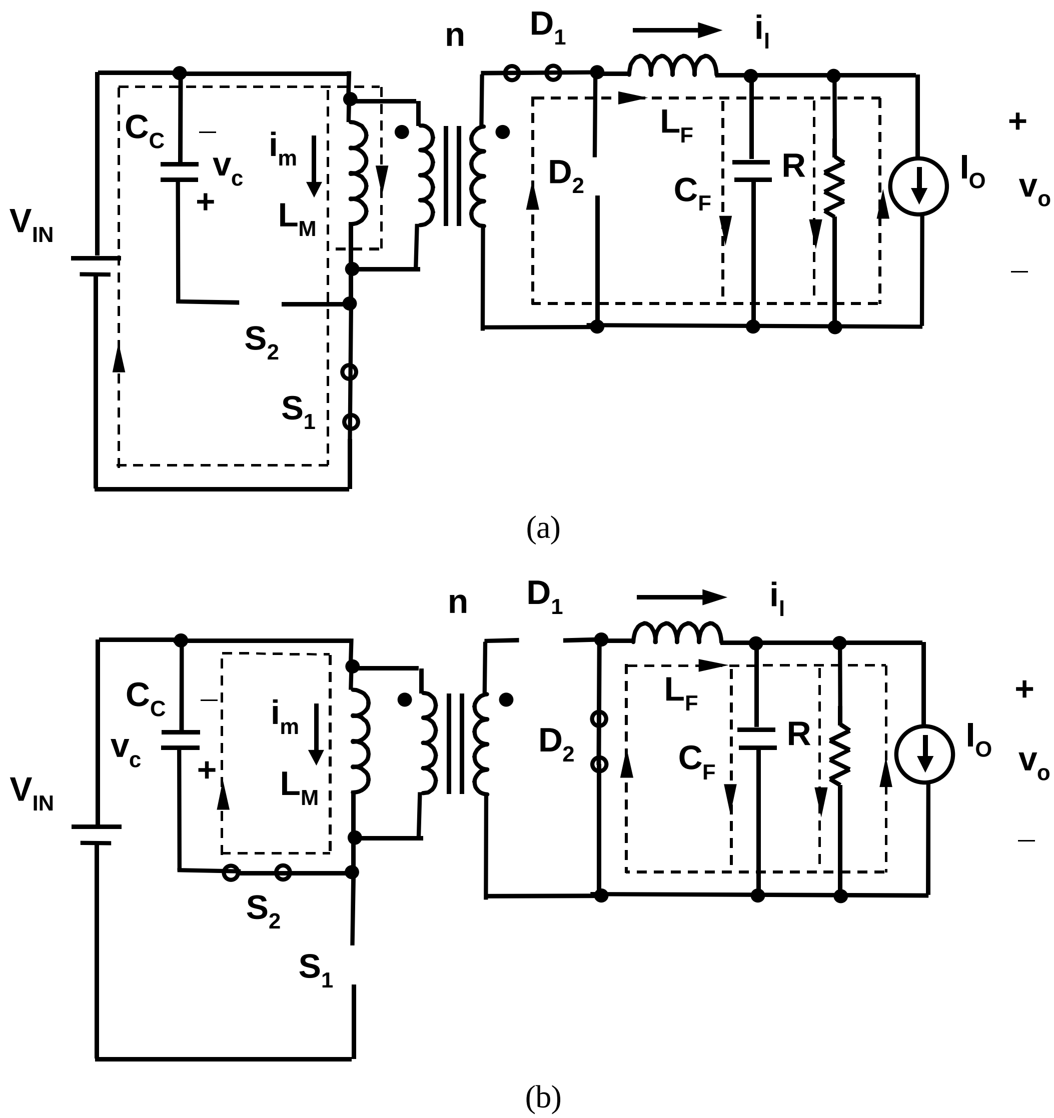


Fig. 5.19 Simplified circuit diagrams: (a) during the on period of main switch; (b) during the off period of main switch.

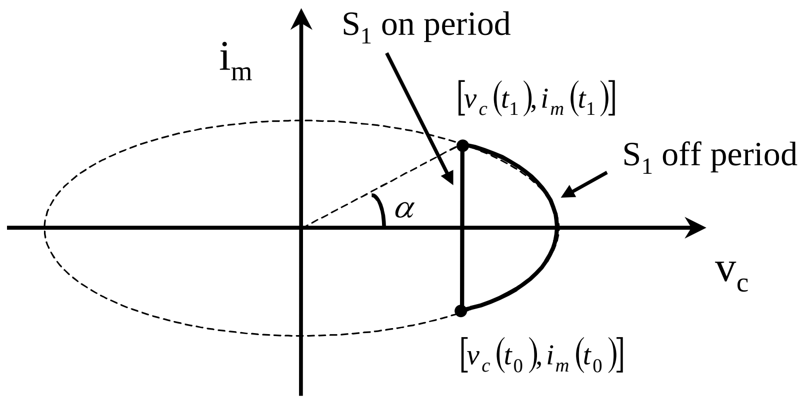
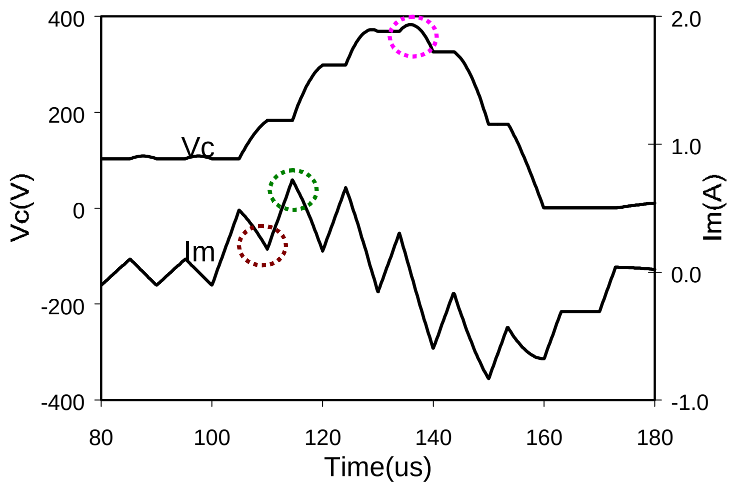


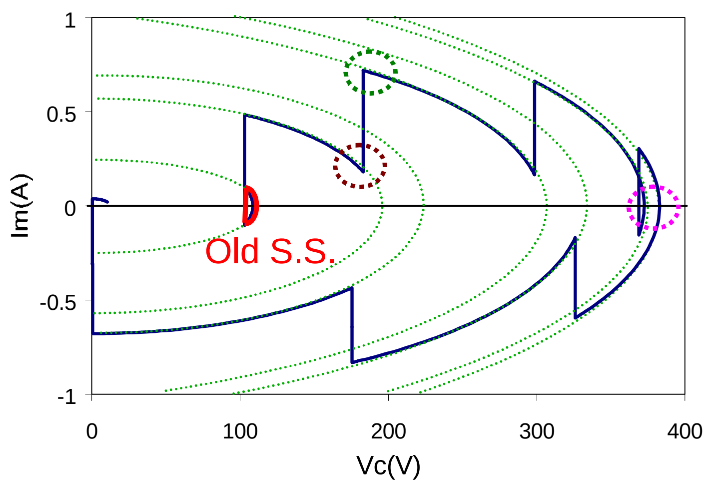
Fig. 5.20. The state trajectory of the active-clamp reset circuit in steady state.

5.3.4 Study of the effect of design parameters in voltage feedback control

In steady state, the state trajectory of the active-clamp reset circuit is in a closed circle, while in large-signal transient, the trajectory is connected by many uncompleted circles. Fig. 5.21(a) shows the time domain waveform of the magnetizing current of the transformer and the clamp capacitor voltage and Fig. 5.21(b) is the same waveform in v_c-I_m state trajectory plane. The dotted cycle in each figure shows the correspondent point, which could cause the problem in the circuit. The small cycle of Fig. 5.21(b) at old steady state (SS) point is the steady state trajectory, it is much smaller than the dynamic trajectory in the figure. So the circuit stress during large-signal transient is much worse than in the steady state.



(a)



(b)

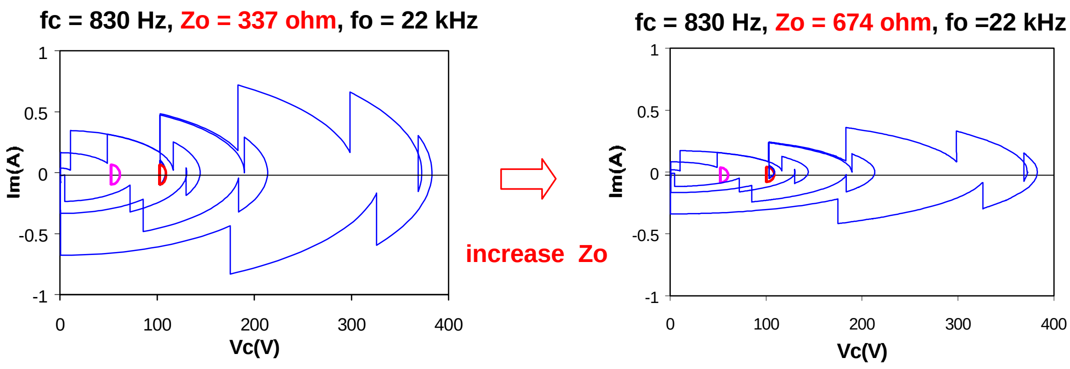
Fig. 5.21. Comparison of time domain simulation waveforms with state trajectory during large-signal transient. (a) time domain simulation. (b) state trajectory.

From previous analysis, we know that the state trajectory is a function of character impedance and resonant frequency of the L_m-C_s network. Since the dynamic behavior is also determined by the whole system response during the transient, the state trajectory is also a function of control bandwidth. Similar to dc analysis, we can change each individual parameter separately in order to understand the effect of each parameter during the dynamic transient.

Fig. 5.22 shows the effect of character impedance of the resonant network. Fig. 5.22(a) shows the original circuit transient waveform with crossover frequency f_c = 830 Hz, character impedance Z_o = 337 ohm, and resonant frequency f_o = 22 kHz. Two small close cycle represent the old steady state and the new steady state, it is much smaller than the dynamic trajectory during transient. Fig. 5.22(b) keeps the same f_c and f_o, and double the character impedance Z_o. It shows that larger Z_o has smaller current stresses and the same voltage stress from the figure.

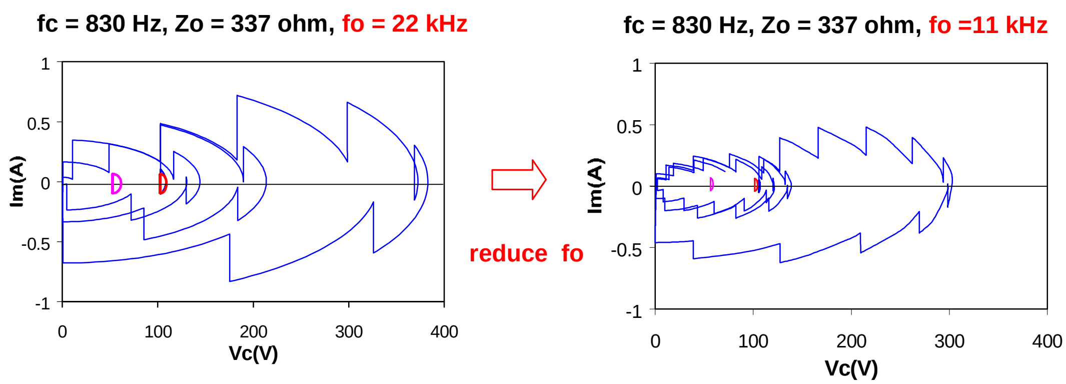
Fig. 5.23 shows the effect of the resonant frequency of the network, f_o. The resonant frequency is reduced to half from Fig. 5.23(a) to Fig. 5.23(b). It shows that smaller f_o has smaller current stresses and the voltage stress.

Fig. 5.24(a) and (b) shows the effect of bandwidth of the close loop control, f_c, during line transient. Fig. 5.24(c) and (d) shows the effect of bandwidth of the close loop control, f_c, during load transient. The bandwidth of the control is increased from 830 Hz to 12 KHz in both cases. It shows that in line transient, a larger f_c has smaller current stresses and the voltage stress; while in load transient, a smaller f_c has smaller current stresses and the voltage stress.



(a) (b)

Fig. 5.22 Effect of character impedance of the resonant network, Z_o. Larger Z_o has smaller current stresses and the same voltage stress.



(a) (b)

Fig. 5.23. Effect of resonant frequency of the network, f_o. Smaller f_o has smaller current stresses and the voltage stress.

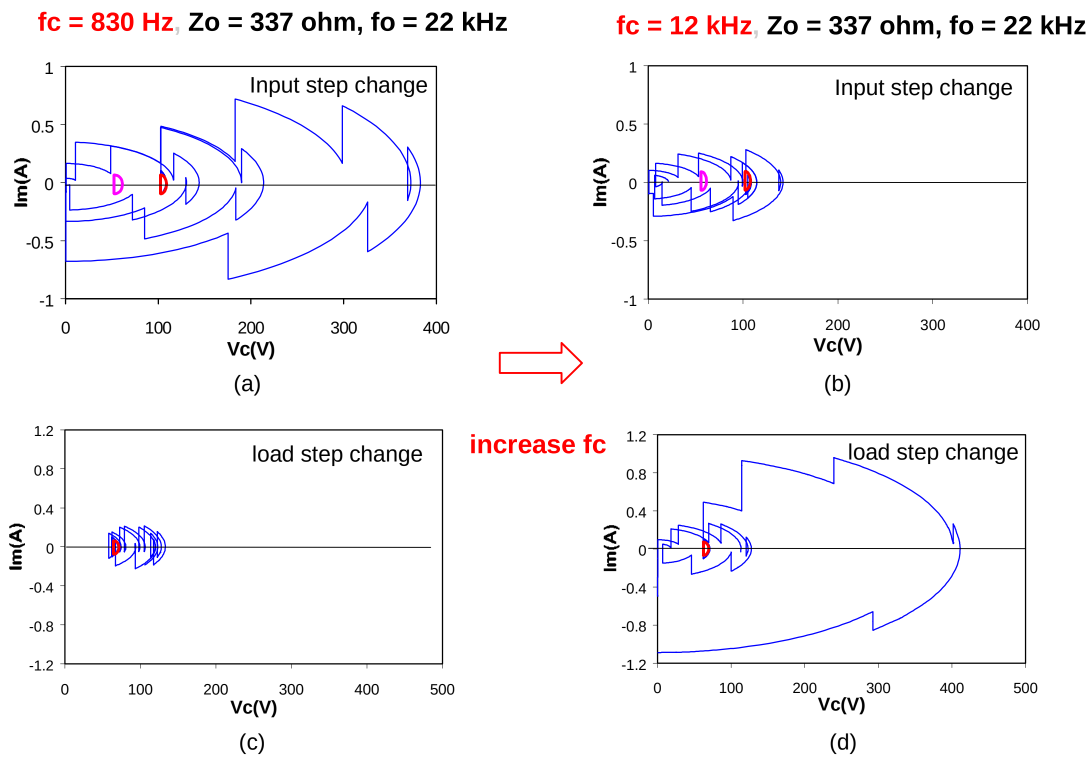


Fig. 5.24. Effect of bandwidth of the close loop control, f_c. In line transient, a larger f_c has smaller current stresses and the voltage stress; in load transient, a smaller f_c has smaller current stresses and the voltage stress

Table 5.1 shows the design trade off according to simulation observations. In order to have a smaller current stress, we prefer a larger magnetizing inductance. But a larger magnetizing inductance has a smaller ripple current, which means a larger possibility to have diode reverse recovery problem. Increasing the clamp capacitor reduces the clamp capacitor voltage but at the same time, it increases the magnetizing current of the transformer. The bandwidth of the control is most confusing. It has an opposite effect in load and line transients. None of the parameter gives the circuit a perfect solution, how to make the trade off when selecting these design parameters? The simulation cannot give us a straightforward answer.

The solid line in Fig. 5.25 shows the state trajectory of the active-clamp reset circuit during the same input-voltage transient as in Fig. 5.18(a). The state trajectory starts with a closed cycle as described in Fig. 5.20. The dashed line in Fig. 5.25 is generated by connecting all the average points in each switching period. The averaged state trajectory shows a much simple waveform than the one in the state trajectory. The averaged state trajectory presents the dynamic behavior of the state variable in a simple form by ignoring the ripple information, which can be easily considered after the analysis.

Table 5.1. Design trade off is very hard to make according to simulation waveform observation.

Condition	Lm	Cc	fc
Larger Zo	↑	↓	
Smaller fo	↑	↑	
Diode reverse recovery	↓		
Line change			↑
Load change			↓
Design trade-off	?	?	?

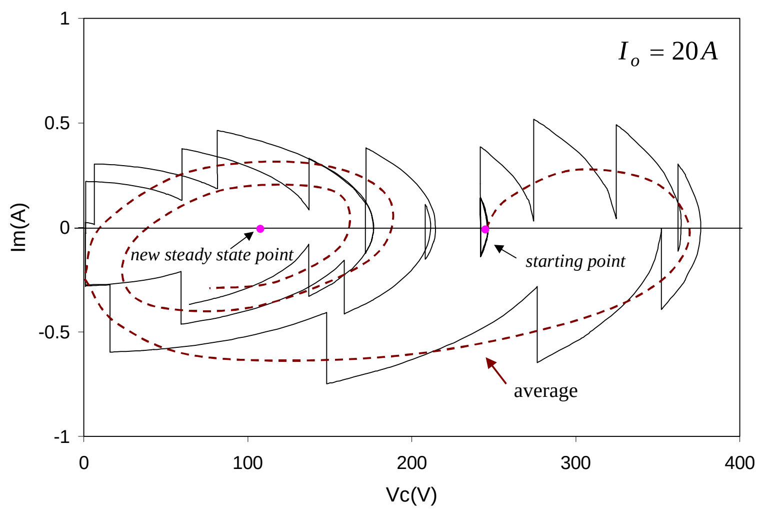


Fig. 5.25 The state trajectory of the active-clamp reset circuit during input-voltage step from 100 V to 200 V transient.

5.3.5 Duty cycle equations during step input-voltage and load transients

Since the transient behavior of the active-clamp reset circuit depends on the speed of the control and the characteristics of the resonant circuit, we will first derive the duty cycle equations during line and load transient.

As can be seen from Fig. 5.18(a) and Fig. 5.18(b), the clamp voltage and magnetizing current transient waveforms show a resonant behavior with superimposed high switching-frequency ripples. Usually the resonant frequency is at least one magnitude smaller than the switching frequency in order to obtain a small ripple voltage of the clamp capacitor in steady state. Therefore, to simplify the analysis, the switching frequency ripples are ignored in the following analysis. However, the clamp voltage and magnetizing current ripples can be easily added into the results obtained by the simplified model later. As an illustration, Fig. 5.25 shows the relationship between state trajectory (solid line) and average state trajectory (dashed line).

5.3.5.1 Average model of the active-clamp forward converter

From Fig. 5.19(a) and Fig. 5.19(b), by ignoring the high switching frequency ripples, the average model of the active-clamp forward converter can be written as

$$C_F \cdot \frac{dv_o}{dt} = i_l + I_o - \frac{v_o}{R}, \tag{5.37}$$

$$L_F \cdot \frac{di_l}{dt} = \frac{d \cdot V_{in}}{n} - v_o, \tag{5.38}$$

$$L_M \cdot \frac{di_m}{dt} = d \cdot V_{in} - d' v_c, \tag{5.39}$$

$$C_C \cdot \frac{dv_c}{dt} = d' \cdot i_m, \tag{5.40}$$

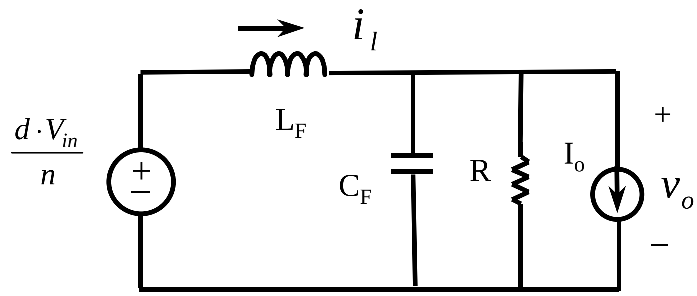
where d is the duty cycle of main switch and d'=1-d.

Equations (5.39) and (5.40) can be rewritten as

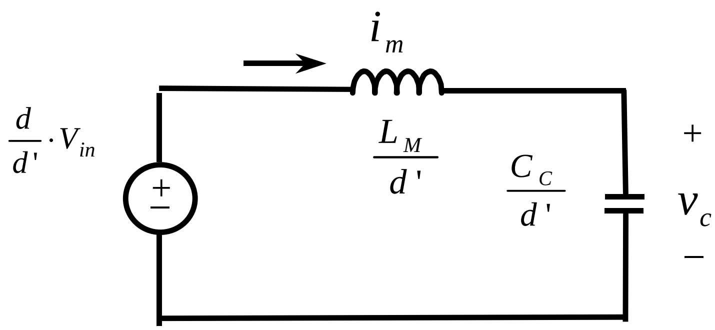
$$\left(\frac{L_m}{d'}\right)\cdot\frac{di_m}{dt}=\frac{d}{d'}\cdot V_{in}-v_c\,, \tag{5.41}$$

$$\left(\frac{C_c}{d'}\right)\cdot\frac{dv_c}{dt}=i_m\,. \tag{5.42}$$

According to (5.37)-(5.42), the average model of the forward converter power stage and the active-clamp reset circuit can be drawn as in Fig. 5.26(a) and Fig. 5.26(b), respectively. As can be seen from Fig. 5.26, the forward converter power stage and the active-clamp reset circuit are only coupled through the duty cycle. For the step input-voltage and load changes, the forward converter power stage represents a linear system. However, the average active-clamp reset circuit is nonlinear with respect to the duty cycle.



(a)



(b)

Fig. 5.26 The average model of the active-clamp forward converter:
(a) average model of the forward converter power stage;
(b) average model of the active-clamp reset circuit.

5.3.5.2 Duty cycle equations of forward converter with voltage feedback control during line and load changes

To further study the transient behavior of the active-clamp circuit, it is necessary to know the duty cycle dependence during input-voltage and load changes. Assuming that the input-voltage perturbation is limited to a step change, and

$$\begin{aligned} V_{in\_new} &= V_{in\_old} + \Delta v_{in} \\ I_{o\_new} &= I_{o\_old} + \Delta i_o \\ D_{new} &= D_{old} + \Delta d \\ V_{o\_new} &= V_{o\_old} + \Delta v_o \end{aligned} \quad , \tag{5.43}$$

where Δv_{in} and Δi_o are the perturbations and Δd and Δv_o are the corresponding changes.

The perturbations of (5.43) yield

$$\Delta v_o = G_d \cdot \Delta d + G_v \cdot \Delta v_{in} + Z_o \cdot \Delta i_o \,, \tag{5.44}$$

where,

$$G_v = \frac{\Delta v_o}{\Delta v_{in}} = \frac{\dfrac{D_{old}}{n}}{1 + s \cdot \dfrac{L_F}{R} + s^2 \cdot L_F \cdot C_F} \quad , \tag{5.45}$$

$$Z_o = \frac{\Delta v_o}{\Delta i_o} = \frac{s \cdot L}{1 + s \cdot \dfrac{L}{R} + s^2 \cdot L \cdot C} \quad , \tag{5.46}$$

$$G_d = \frac{\Delta v_o}{\Delta d} = \frac{\dfrac{V_{in\_new}}{n}}{1 + s \cdot \dfrac{L_F}{R} + s^2 \cdot L_F \cdot C_F} \quad . \tag{5.47}$$

Assuming the transfer function of control loop compensator is A(s), the loop gain is $T(s) = A(s) \cdot G_d(s)$ as shown in the closed-loop block diagram of the forward converter in Fig. 5.27. According to Fig. 5.27, the closed loop equations are

$$\frac{\Delta d}{\Delta v_{in}}\Big| close = \frac{\Delta d}{\Delta v_o} \cdot \frac{\Delta v_o}{\Delta v_{in}} = -\frac{D_{old}}{V_{in\_new}} \cdot \frac{T(s)}{1 + T(s)} \,, \tag{5.48}$$

$$\frac{\Delta d}{\Delta i_o}\Big|close = \frac{\Delta d}{\Delta v_o}\cdot\frac{\Delta v_o}{\Delta i_o} = -\frac{s\cdot L_F\cdot n}{V_{in\_new}}\cdot\frac{T(s)}{1+T(s)}, \tag{5.49}$$

where, D_{old} is the duty cycle before perturbation, and V_{in_new} is the input voltage after the line step change.

Generally, neglecting the ESR zero of output-filter capacitor C_F, the optimal compensation of the output-voltage feedback control loop requires the transfer function of the compensator in the form

$$A(s) = \frac{A_{dc}}{s}\cdot\frac{(1+s/\omega_{z1})\cdot(1+s/\omega_{z2})}{(1+s/\omega_p)}, \tag{5.50}$$

where, compensator zeroes ω_{z1} and ω_{z2} are placed to cancel two poles in G_d transfer function, i.e., ω_{z1} and ω_{z2} are close to $\frac{1}{\sqrt{L_F\cdot C_F}}$, and ω_p is placed at a frequency between crossover frequency ω_c and switching frequency ω_s.

Since when T>>1, $\frac{T}{1+T}\approx 1$, and when T<<1, $\frac{T}{1+T}\approx T$. The $\frac{T}{1+T}$ transfer function becomes

$$\frac{T}{1+T} = \frac{1}{(1+s/\omega_c)\cdot(1+s/\omega_p)}, \tag{5.51}$$

as shown in Fig. 5.28.

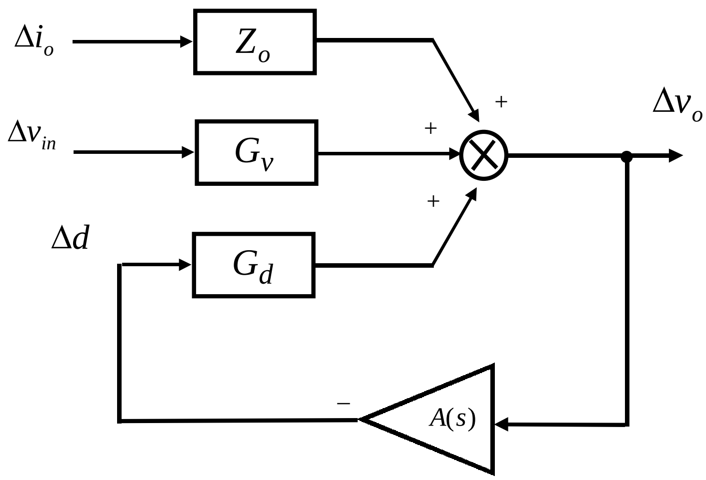


Fig. 5.27 Forward converter closed loop block diagram.

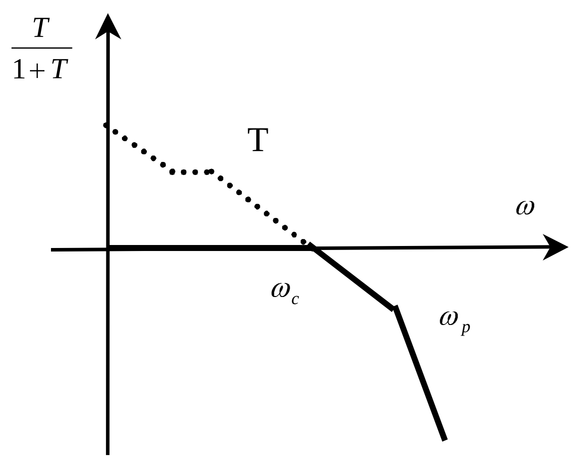


Fig. 5.28 T/(1+T) Bode plot.

Substituting (5.51) into (5.48) and (5.49), the closed-loop transfer functions are

$$\frac{\Delta d}{\Delta v_{in}}\Big|_{close} = -\frac{D_{old}}{V_{in\_new}} \cdot \frac{1}{(1+s/\omega_c)\cdot(1+s/\omega_p)}, \tag{5.52}$$

$$\frac{\Delta d}{\Delta i_o}\Big|_{close} = -\frac{s\cdot L_F \cdot n}{V_{in\_new}} \cdot \frac{1}{(1+s/\omega_c)\cdot(1+s/\omega_p)}. \tag{5.53}$$

Therefore, from (5.52), for a step input voltage change, the time domain equation for the duty cycle can be written as

$$d(t) = D_{old} + (D_{new} - D_{old})\cdot\left(1 - \frac{\omega_p}{\omega_p - \omega_c} e^{-\omega_c \cdot t} + \frac{\omega_c}{\omega_p - \omega_c} e^{-\omega_p \cdot t}\right) \tag{5.54}$$

Because generally ω_p is selected so that $\omega_p >> \omega_c$, (5.54) can be simplified to

$$d(t) = D_{old} + (D_{new} - D_{old})\cdot\left(1 - e^{-\omega_c \cdot t}\right). \tag{5.55}$$

Similarly, from Eq. (5.53), under the same assumptions, the time domain equation for the duty cycle during a step load change can be obtained as

$$d(t) = D_{old} - \frac{n\cdot\omega_c\cdot L_F}{V_{in}}\cdot\Delta I_o\cdot e^{-\omega_c \cdot t}. \tag{5.56}$$

5.3.6 Proposed average state trajectory analysis approach

5.3.6.1 Average state trajectory equations

From Fig. 5.26, it can be seen that the average model of the active-clamp reset circuit is a nonlinear system whose parameters are the functions of the duty cycle. At the same time, the duty cycle is independent of the parameters of the L_M-C_C resonant network, i.e., it is decoupled from the state variables, v_c and i_m. In addition, since the duty cycle does not change during each switching period, the average model in Fig.

5.26(b) can be considered linear during each switching period with input voltage fixed at $\frac{d}{d} \cdot V_{in}$, magnetizing inductance $\frac{L_M}{d'}$, and clamp capacitance $\frac{C_C}{d'}$.

By solving (5.41) and (5.42), the state trajectory equations during each switching period are

$$v_c(t) = r(0) \cdot \cos[\alpha(0) - \omega_o \cdot t] + v_{center}\,, \tag{5.57}$$

$$i_m(t) \cdot Z_O = r(0) \cdot \sin[\alpha(0) - \omega_o \cdot t], \tag{5.58}$$

where,

$$v_{center} = \frac{d}{d'} \cdot Vin\,, \tag{5.59}$$

$$r(0) = \sqrt{[v_c(0) - v_{center}(0)]^2 + i_m(0)^2 \cdot Z_O{}^2}\,, \tag{5.60}$$

$$\alpha(0) = \tan^{-1}\left(\frac{i_m(0) \cdot Z_O}{v_c(0) - v_{center}}\right). \tag{5.61}$$

In (5.57) - (5.61), $v_C(0)$ is the initial average voltage of the clamp capacitor and $i_m(0)$ is the initial average magnetizing current of the transformer at the main switch on instant. $\omega_o = \frac{d'}{\sqrt{L_M \cdot C_C}}$ is the resonant frequency of L_M-C_C resonant network, and $Z_O = \sqrt{\frac{L_M}{C_C}}$ is the characteristic impedance of the resonant network.

By combining (5.57) and (5.58), the state trajectory equation can be written as

$$[v_c(t) - v_{center}]^2 + [i_m(t) \cdot Z_O]^2 = r(0)^2 \tag{5.62}$$

It is an eclipse with center (v_{center}, 0) in the $v_c - i_m$ state plane, and a circle in the $v_c - i_m \cdot Z_O$ state plane. The dynamic equilibrium point, v_{center}, is the center of the state trajectory and is a function of the duty cycle and the input voltage. The average state trajectory is shown in Fig. 5.29 with the solid line.

Because the duty cycle is a slow varying compared with a switching period, the duty cycle d(t) changes gradually during transient. Consequently, it can be assumed that the average state trajectory movement is a continuous movement with moving center $v_{center}(t)$ described by equations (5.57)-(5.62), where all quantities dependent on duty cycle are functions of time.

Similarly, one can analyze the average state trajectory in the presence of resistive loss R_M which represents a sum of the switch on resistance and the core loss of the transformer. The normalized average state trajectory with damping is shown in Fig. 5.29 with a dashed line. v_{center} is the spiral point of the state trajectory and the damping of the trajectory is $e^{-\frac{R_M}{2 \cdot L_M} \cdot t}$.

Since time constant in the damping term is usually very large when no external damping circuit is used, the effect of the damping does not have a significant impact on peak values of state variables in the transient analysis. The rest of the section will analyze the circuit's transient behavior without a damping effect.

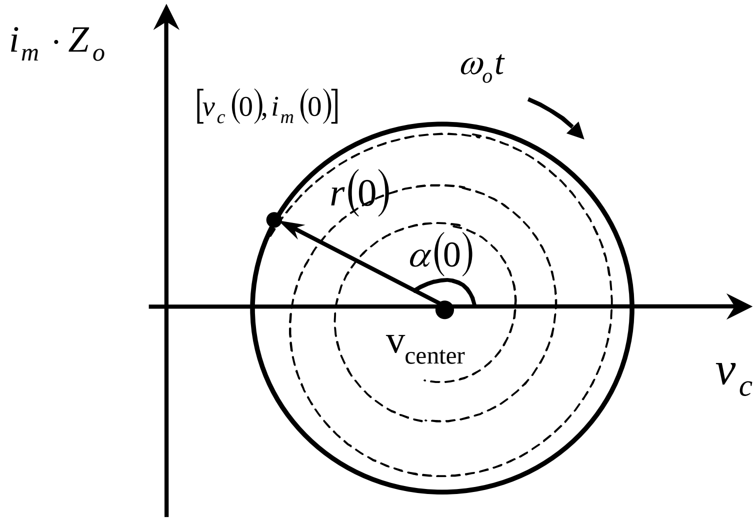


Fig. 5.29. Average state trajectory without damping (solid line); with damping (dashed line).

5.3.6.2 Movement of the average state trajectory during line transient

Before the input-voltage step change from V_{in_old} to V_{in_new}, the average state trajectory is a single point in the $v_c - i_m \cdot Z_o$ state plane with duty cycle d=D_{old}, initial average clamp-capacitor voltage $v_c(0) = \frac{D_{old}}{D_{old}'} \cdot V_{in\_old}$, and the average magnetizing current of the transformer $i_m(0) = 0$. Since immediately after an input-voltage step change, the duty cycle cannot change instantaneously, the trajectory center after the change is $v_{center}(0) = \frac{D_{old}}{D_{old}'} \cdot V_{in\_new}$ and the average state trajectory follows the circle described in (5.62) with the center [$v_{center}(0)$, 0] and radius $r(0) = |v_{center}(0) - v_c(0)|$.

When the converter operates with the control loop open, i.e., has a fixed duty cycle, d does not change. Consequently, v_{center} and r do not change, and the state trajectory is a fixed circle as shown in Fig. 5.30. However, when the forward converter has an output-voltage feedback control, the duty cycle changes gradually from D_{old} to D_{new} as described in (5.55) so the center of the circle moves from $v_{center}(0)$ to $v_{c\_new} = \frac{D_{new}}{D_{new}'} \cdot V_{in\_new}$, which is the new steady state value of the clamp-capacitor voltage. The trajectory movement is illustrated in Fig. 5.31.

Fig. 5.31(a) and Fig. 5.31(b) are the state trajectories during input-voltage from 200 V to 300 V transient with a bandwidth f_c=3 kHz and f_c=20 kHz, respectively. Both state trajectories follow the open loop circle (dashed line) at the beginning of the transient. Since v_{center} moves faster in Fig. 5.31(b) due to a higher bandwidth, the state trajectory in Fig. 5.31(b) takes less time to move to the new steady state, and it results in a lower peak voltage of the switch and a lower peak magnetizing current (smaller thick solid-line circle).

Fig. 5.31(c) and Fig. 5.31(d) are the state trajectories during input-voltage from 300 V to 200 V transient with a bandwidth f_c=3 kHz and f_c=20 kHz, respectively.

Similar state trajectory movements can be observed. As can be seen from Fig. 5.31, the worst case (largest thick solid-line circle) happens when the input-voltage steps from low to high, and the bandwidth is lowest.

The resonant frequency of the active-clamp circuit plays an important role, since the state trajectory is determined by two movements, the state trajectory center movement, whose speed is controlled by the bandwidth f_c; and the resonant movement, whose speed is determined by the resonant frequency f_o. Fig. 5.32 shows the calculated maximum values of v_c and i_m as functions of f_o/f_c. For the same bandwidth, a lower resonant frequency has a smaller peak clamp-capacitor voltage and peak magnetizing current.

The peak voltage of the main switch and the magnetizing current of the transformer can be calculated by adding the ripple as

$$i_m(peak) = i_{m\_ave}(\max) + \frac{1}{2} \cdot \frac{V_{in} \cdot D \cdot T_s}{L_M} \tag{5.63}$$

$$v_{s1}(peak) = V_{in\_new} + v_{c\_ave}(\max) + \frac{1}{2} \cdot \frac{1}{8} \cdot \frac{D' \cdot n \cdot V_o \cdot T_s^2}{L_M \cdot C_C} \tag{5.64}$$

5.3.6.3 Movement of the average state trajectory during load transient

Before a load step change, the average state trajectory is a single point in the $v_c - i_m \cdot Z_o$ state plane with duty cycle d=D_{old}, initial average clamp-capacitor voltage $v_c(0) = \frac{D_{old}}{D_{old}'} \cdot V_{in}$ and the average magnetizing current of the transformer $i_m(0) = 0$. According to (5.56), at the moment of a step load change, the duty cycle changes for

$$\Delta d = -\frac{n \cdot \omega_c \cdot L_F}{V_{in}} \cdot \Delta I_o, \tag{5.65}$$

so that the initial trajectory center is

$$v_{center}(0) = \frac{D_{old} + \Delta d}{D_{old}' - \Delta d} \cdot V_{in} . \qquad (5.66)$$

The average state trajectory follows the circle described in (5.62) with circle center at [$v_{center}(0)$, 0] and radius $r(0) = |v_{center}(0) - v_c(0)|$.

Because of the output-voltage feedback control, the duty cycle returns gradually to D_{old} as described in (5.56). Therefore, the center of the circle moves from $v_{center}(0)$ to $v_c(0)$, which is the original steady state value of the clamp-capacitor voltage, as illustrated in Fig. 5.33.

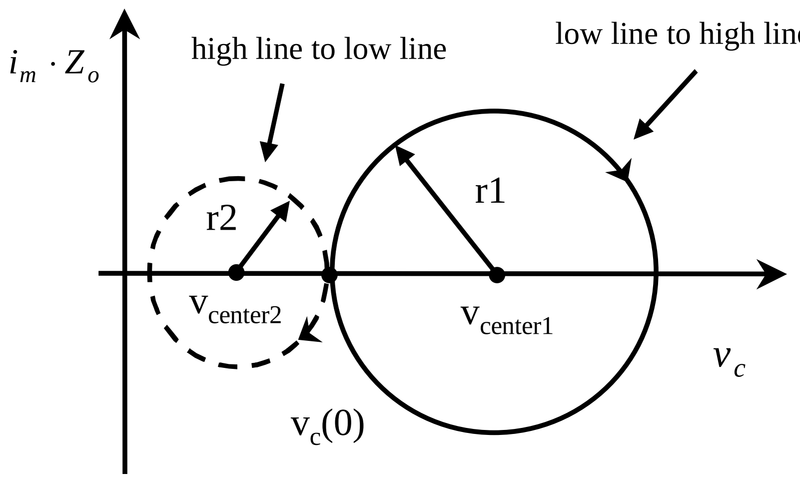
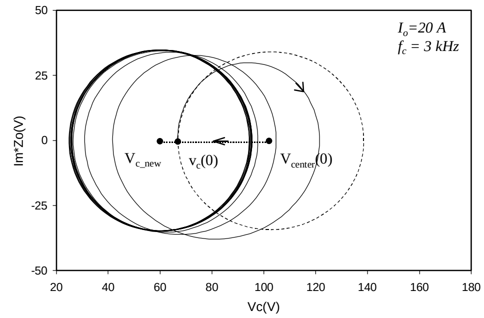
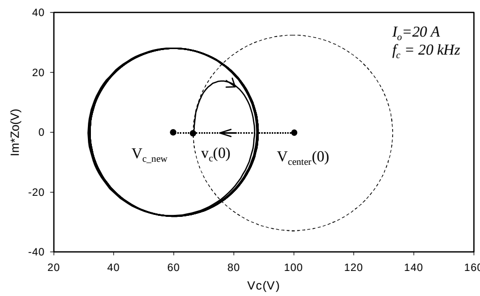


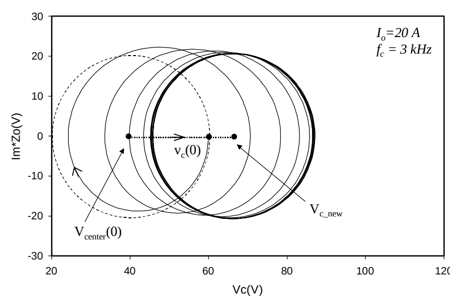
Fig. 5.30. Open-loop state trajectories during input step changes.



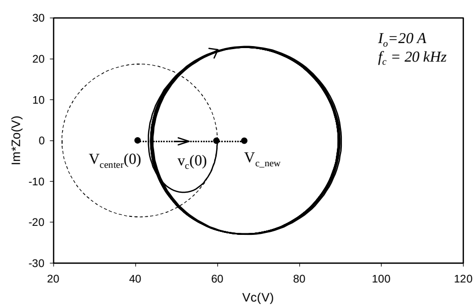
(a)



(b)



(c)



(d)

Fig. 5.31. Closed-loop average state trajectories with different bandwidths and input step changes: (a)-(b) input-voltage step from 200 V to 300 V; (c)-(d) input-voltage step from 300 V to 200 V.

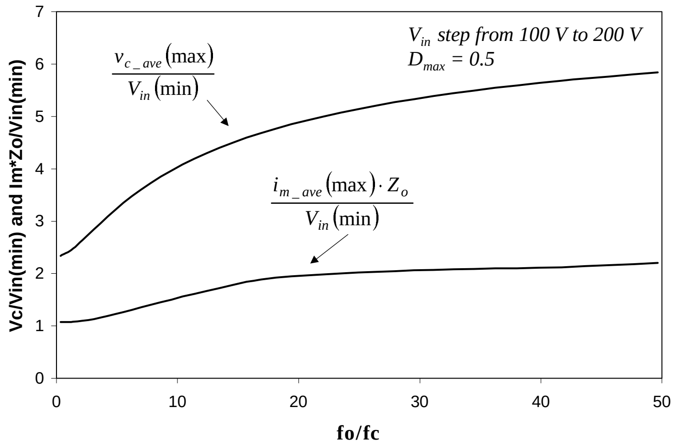
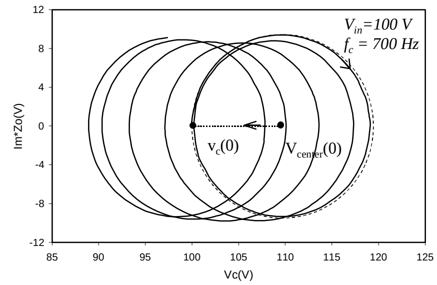


Fig. 5.32 The maximum average values of v_c and i_m are functions of f_o/f_c.

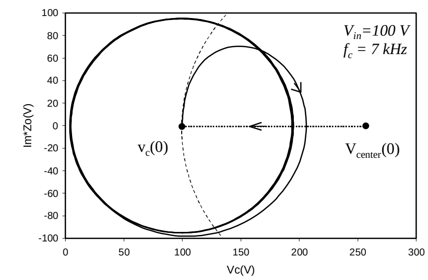
Fig. 5.33(a) and Fig. 5.33(b) are the state trajectories during a step load change from 18 A to 20 A with a bandwidth of f_c=3 kHz and f_c=20 kHz, respectively. Both state trajectories follow the open loop circle (dashed line) at the beginning of the transient. Since v_{center} moves faster in Fig. 5.33(b) due to a higher bandwidth, the state trajectory in Fig. 5.33(b) takes less time to move to the new steady state. It should be noted that according to (5.56), the circuit with higher control bandwidth has a larger initial duty cycle jump. As a result, the initial radius r(0) is much larger for the high bandwidth case. This is opposite to the case of a step input-voltage change, where the circuit with a higher bandwidth control experiences a larger maximum clamp-capacitor voltage and magnetizing current.

Fig. 5.33(c) and Fig. 5.33(d) show the state trajectories during a step load change from 20 A to 18 A with a bandwidth f_c=3 kHz and f_c=20 kHz, respectively. As can be seen from Fig. 5.33, the maximum transient voltage stress of the switch and the maximum transient magnetizing current occur for a positive step load changing with a high bandwidth. For the same bandwidth, a lower resonant frequency has a smaller peak clamp-capacitor voltage and peak magnetizing current.

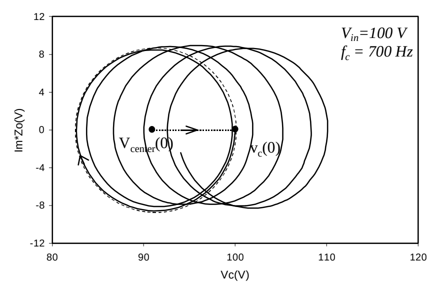
In addition, the minimum input-voltage condition exhibits the largest clamp-capacitor voltage and the magnetizing current transient since $v_{center}(0)$ is the largest due to the smallest d'. A smaller output-filter inductance helps to reduce the duty cycle change during transients and reduces the peak voltage and the magnetizing current.



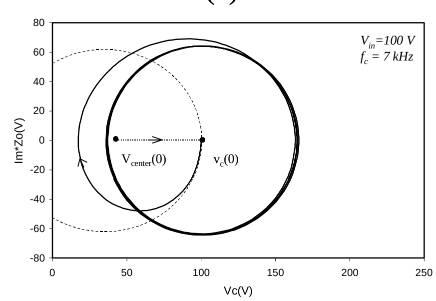
(a)



(b)



(c)



(d)

Fig. 5.33. Closed-loop average state trajectories with different control bandwidths and load step changes: (a)-(b) load current step from 18 A to 20 A; (c)-(d) load current step from 20 A to 18 A.

5.3.7 Experimental verification of average state trajectory approach

In order to verify the averaged state trajectory analysis approach, a circuit board of a 100W, 5V forward converter with active clamp reset circuit is build to verify the predicted trajectory. The circuit parameters are shown in Fig. 5.34. The input voltage range of the circuit is 40-100 V and the maximum duty cycle is 0.7.

Fig. 5.35 shows the experimental waveforms of the clamp capacitor, V_C, and the magnetizing current, I_M with an input step change from 50 to 75 V and load 10A. Fig. 5.36 shows the averaged state trajectories of calculated (dashed line) and measured (solid line) V_C and I_M. The measured V_C and I_M reach the new steady state faster due to the damping in the real circuit. It shows that the analysis predicts the dynamics of clamp capacitor voltage and the magnetizing current very well during the line transient. The model without damping is used for the worst case scenario.

Fig. 5.37 shows the experimental waveforms of the clamp capacitor, V_C, and the magnetizing current, I_M with a load step change from 10 to 15 A and input voltage 50 V. Fig. 5.38 shows the averaged state trajectories of calculated (dashed line) and measured (solid line) V_C and I_M. The measured V_C and I_M reach the new steady state faster due to the damping in the real circuit. It shows that the analysis also predicts the dynamics of clamp capacitor voltage and the magnetizing current very well during the load transient. The model without damping is used for the worst case scenario.

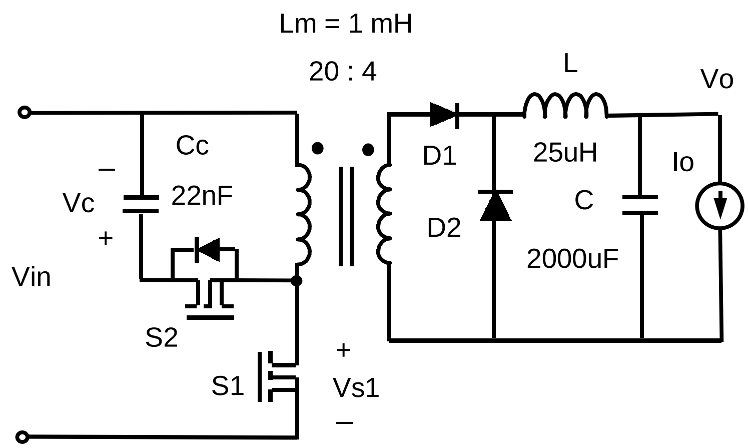
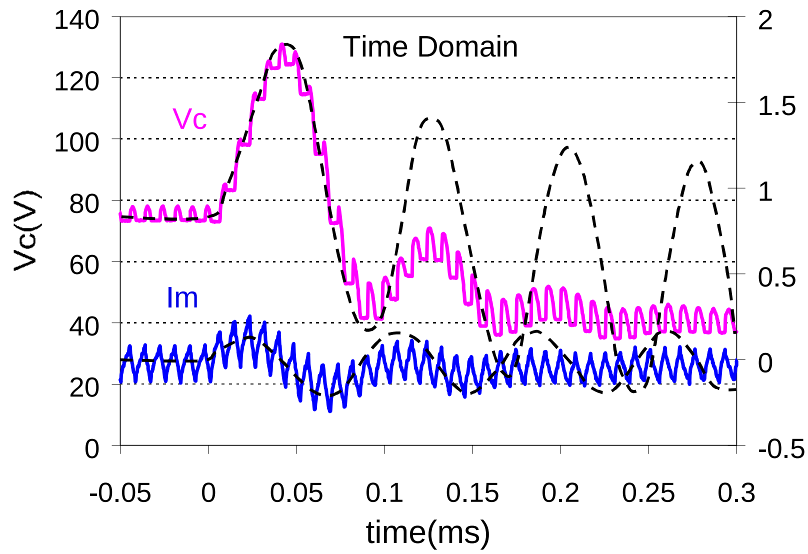
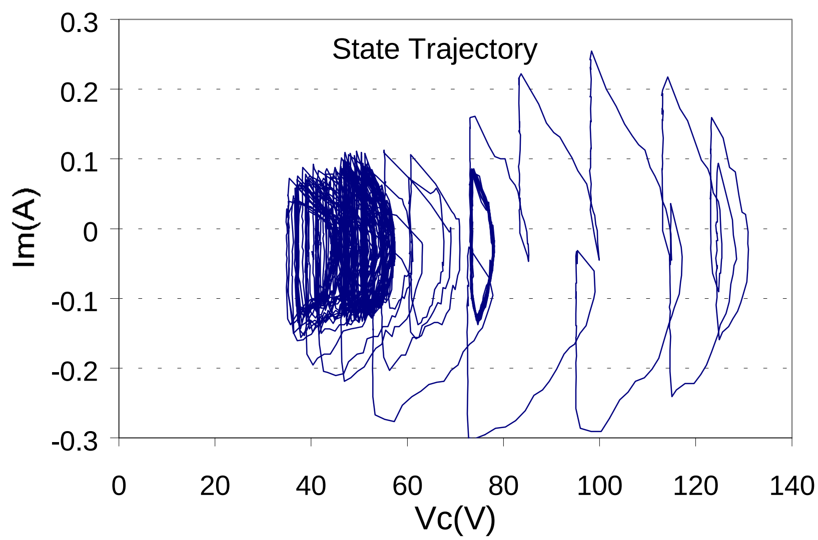


Fig. 5.34 Experimental circuit diagram



(a)



(b)

Fig. 5.35 Experimental waveforms with an input step change from 50 V to 75 V: (a) time domain waveforms of clamp capacitor voltage and magnetizing current; (b) same transient waveforms in V_C-I_M state plane.

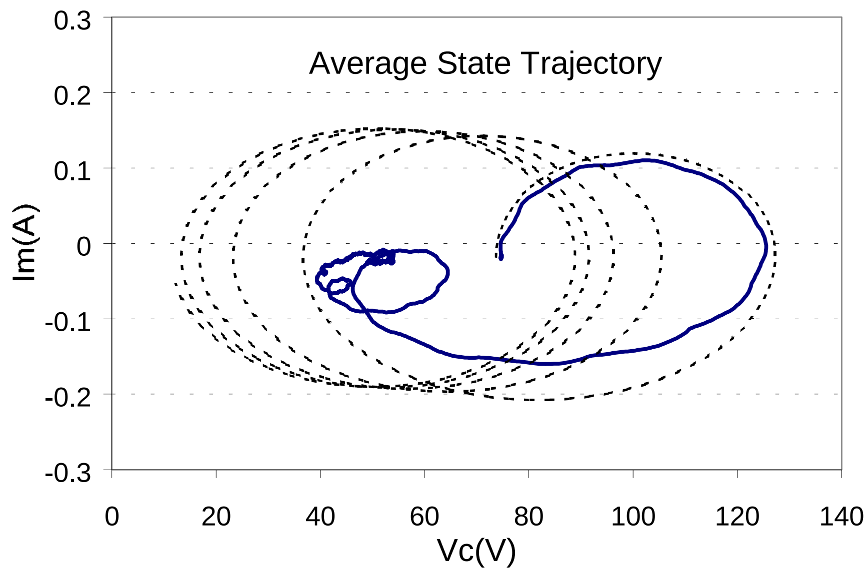
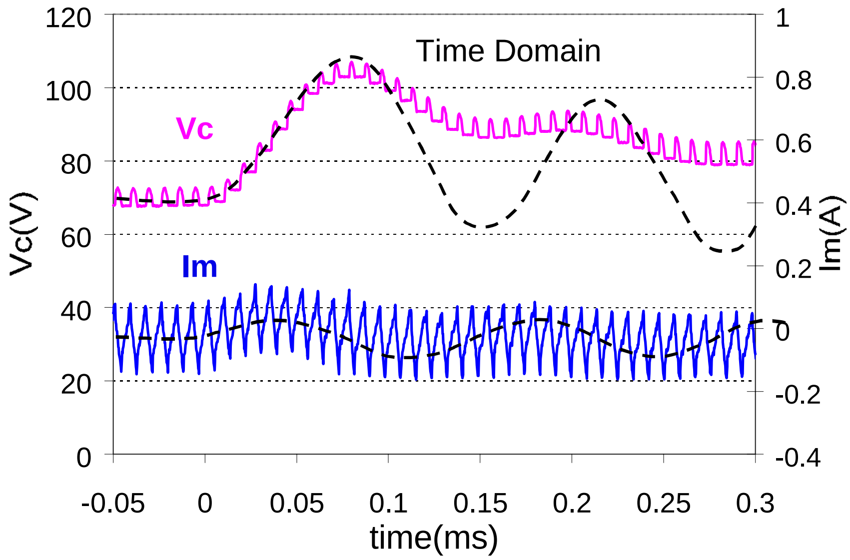
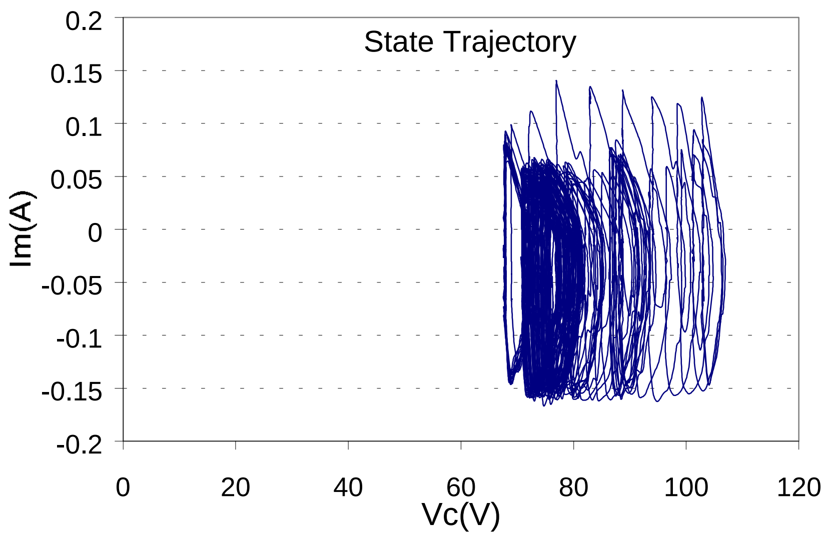


Fig. 5.36 Comparison of averaged state trajectories of calculated and measured V_C and I_M during 50 – 75 V line transient. Dashed line, calculation; solid line, measurement.



(a)



(b)

Fig. 5.37 Experimental waveforms with a load step change from 10 A to 15 A: (a) time domain waveforms of clamp capacitor voltage and magnetizing current; (b) same transient waveforms in V_C-I_M state plane.

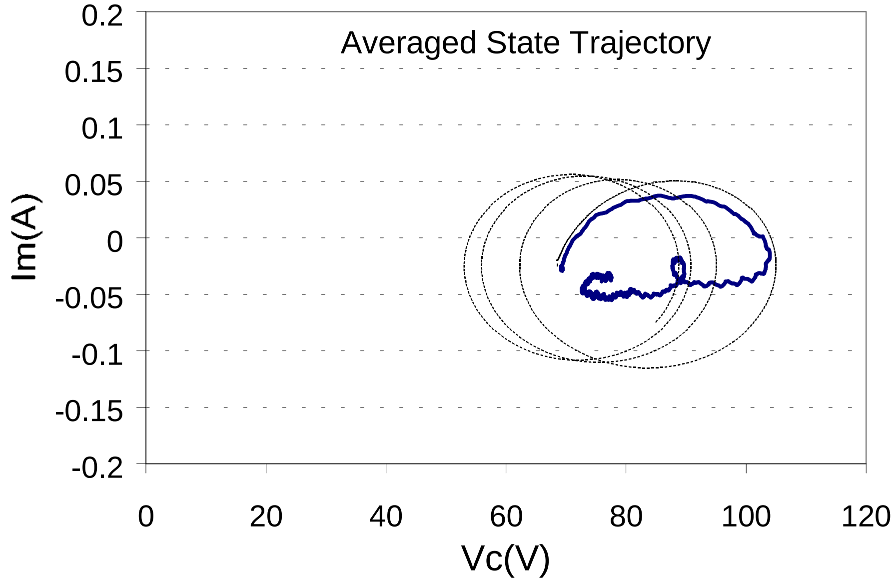


Fig. 5.38 Comparison of averaged state trajectories of calculated and measured V_C and I_M during 10 – 15 A load transient. Dashed line, calculation; solid line, measurement.

5.4 Summary

The dc analysis of the forward converter with active-clamp reset circuit is discussed in this chapter. It shows that the parasitic capacitances of the devices (main switch, active clamp switch, and the parasitic capacitance of the transformer) introduce a positive bias magnetizing current of the power transformer in steady state. And the leakage inductance of the transformer introduces a negative bias magnetizing current of the power transformer in steady state.

A large positive dc bias of the magnetizing current could cause the diode reverse recovery problem of the circuit and a large negative dc bias could cause the active-clamp switch loss the ZVT on operation. The numerical equations of the bias magnetizing current are derived to verify the simulation observations.

The large-signal performance of the active-clamp-reset circuit is very important in a robust circuit design. During large-signal transient, the charge unbalance of the active-clamp capacitor could cause a resonant of the reset network. Consequently, it could cause a large peak of the switch voltage and magnetizing current of the power transformer. The large peak of the switch voltages and the transformer magnetizing current could overstress the devices, saturate the transformer, and cause the diode reverse recovery problem.

An average state trajectory approach is proposed to analyze the response of the active-clamp circuit and predict the dynamic trace during the large-signal transients. The average state trajectory approach is demonstrated by predicting and calculating the dynamic performance of the active-clamp-reset circuit with output-voltage feedback control during line and load transients. A circuit board is build to verify the average state trajectory approach. The analysis results match the experimental results very well during line and load transients. It is shown from the analysis that control bandwidth is also a design parameter besides the magnetizing inductance of the transformer and the active-clamp-capacitor.

6. DESIGN OPTIMIZATION OF THE ACTIVE-CLAMP FORWARD CONVERTER USING VIRTUAL PROTOTYPE DVT

6.1 Introduction

From previous large-signal analysis of the forward converter with active-clamp reset circuit, we see that the average state trajectory can clearly show the dynamic movement of the active-clamp circuit during different line and load conditions. There are two movements are involved in the average state trajectory: the movement of the resonant network which is a function of the magnetizing inductance and clamp capacitance, and the movement of the state trajectory center, which is a function of duty cycle. Due to the input voltage or load change, the circuit moves from an old steady state to a new steady state (for load transient, it will move back to the original steady state) by these two movement as shown in Fig. 6.1. For a forward converter with a fixed active-clamp reset circuit (i.e. L_m and C_c are fixed), the whole trajectory is determined by the movement of the steady state center, which is a function of the duty cycle.

Fig. 6.1 illustrates the average state trajectory of the circuit during a line transient. The original steady state point is 0, then the center moves from 0 to 1, 2, 3, 4 during the transient, and 4 is the new steady state point. We can predict the dynamic movement of the circuit as long as we understand the duty cycle movement during the large-signal transient. We can see that the far the center moves away from the original point, the larger the clamp voltage and magnetizing current could be. The largest voltage and current stresses of the circuit can be measured by $\Delta v_{c\_center}(\max)$, as shown in Fig. 6.1.

From average state trajectory analysis, we can predict the worst case scenario in the transient, so the circuit can be designed according to these worst conditions.

Previous chapter shows that it is possible to derive the duty cycle equations in voltage feedback control, so the average state trajectory can be obtained by enter simple duty cycle equations in a numerical analysis tool, such as Matlab. Since the final goal of the analysis is to solve the large-signal transient design problems in the 5V power supply system discussed in the chapter 4, where an active-clamp forward converter with current mode control is applied, we will further extend the analysis result and provide the design procedure for current mode control circuit. In the following analysis, it will show that the average state trajectory can not be obtained by some simple equations because the non-linearity of circuit in the current-mode control. This chapter is going to demonstrate how the average state trajectory analysis and the virtual prototype simulation tool facility solving the design problems related to active-clamp reset circuit. At the end, the virtual prototype DVT process is repeated to verify the design.

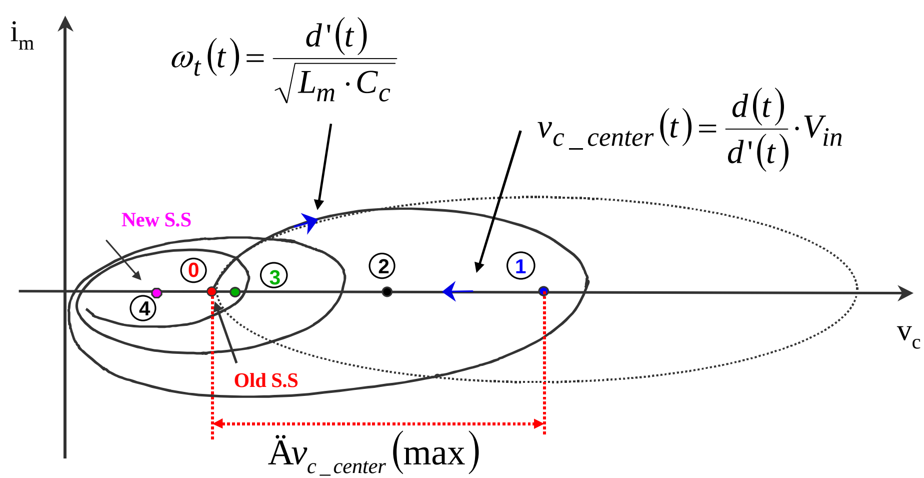


Fig. 6.1. There are two movements involved in the average state trajectory: the movement of the resonant network and the movement of the state trajectory center, which is a function of the duty cycle.

6.2 Dynamic performances of the active-clamp reset circuit with peak current mode control

Since the 5 V forward converter of the power supply system we tested has peak current mode control, we will extend the study of the average state trajectory with voltage mode control to the one with current mode control in this section. At first, we will study the duty cycle equations in current mode control. In voltage model control, the forward converter with active-clamp reset circuit can be de-coupled into two independent circuits: the simple forward converter circuit and an active-clamp reset circuit. With the assumption that the magnetizing current is much smaller than the load current reflected to the primary, so the control of the forward converter is independent of the reset circuit, and the reset circuit in related to main forward converter by duty cycle in voltage feedback control.

In current mode control, since the sensed current is the sum of the load current and the magnetizing current, the active-clamp reset circuit could have interactions with the main forward converter [67]. If we design the circuit such that the resonant frequency of the reset circuit is much larger than the crossover frequency of the forward converter and the load current is much larger than the magnetizing current, the circuit can be de-coupled into two independent circuits as in the voltage feedback control.

6.2.1 Average model of the forward converter with peak current mode control

Fig. 6.2 shows a simplified forward converter circuit diagram with peak current mode control. The circuit is simplified to a buck converter by eliminating the primary circuit and moving the primary input voltage into an equivalent voltage source on the secondary. We define the slope of the sensed current ramp is S_n, the slope of the external ramp is S_e, and the modulator gain for the model is F_m, duty cycle is d, the current sensor gain is R_i, where

$$S_n = \frac{\frac{V_{in}}{n} - V_o}{L}. \tag{6.1}$$

From Fig. 6.3, we can see

$$V_c - S_e \cdot d \cdot T_s = \left(I + \frac{S_n \cdot d \cdot T_s}{2} \right) \cdot R_i\,, \tag{6.2}$$

Simplify (6.2), we get

$$\left(S_e + \frac{\frac{V_{in}}{n} - V_o}{2 \cdot L} \cdot R_i \right) \cdot d \cdot T_s = V_c - I \cdot R_i\,. \tag{6.3}$$

If we define

$$F_m = \frac{1}{\left(S_e + \frac{\frac{V_{in}}{n} - V_o}{2 \cdot L} \cdot R_i \right) \cdot T_s}\,, \tag{6.4}$$

then

$$d = F_m \cdot (V_c - I \cdot R_i) \tag{6.5}$$

From (6.4), we can see that when the input voltage Vin has a sudden change, Fm will change immediately before the voltage compensation responses, the circuit has an additional feed-forward from input voltage compared with a voltage mode control circuit. Also, when the load has a sudden change, the change of the output voltage will cause Fm to change immediately, which is an addition feed-forward from output voltage.

Since Fm changes under line and load transients, (6.5) is a nonlinear equation. The duty cycle is determined by three terms: modulator gain, output voltage of the error amplifier, and the sensed inductor current. We have to understand the transient response of each term in order to predict the dynamic performances of the circuit.

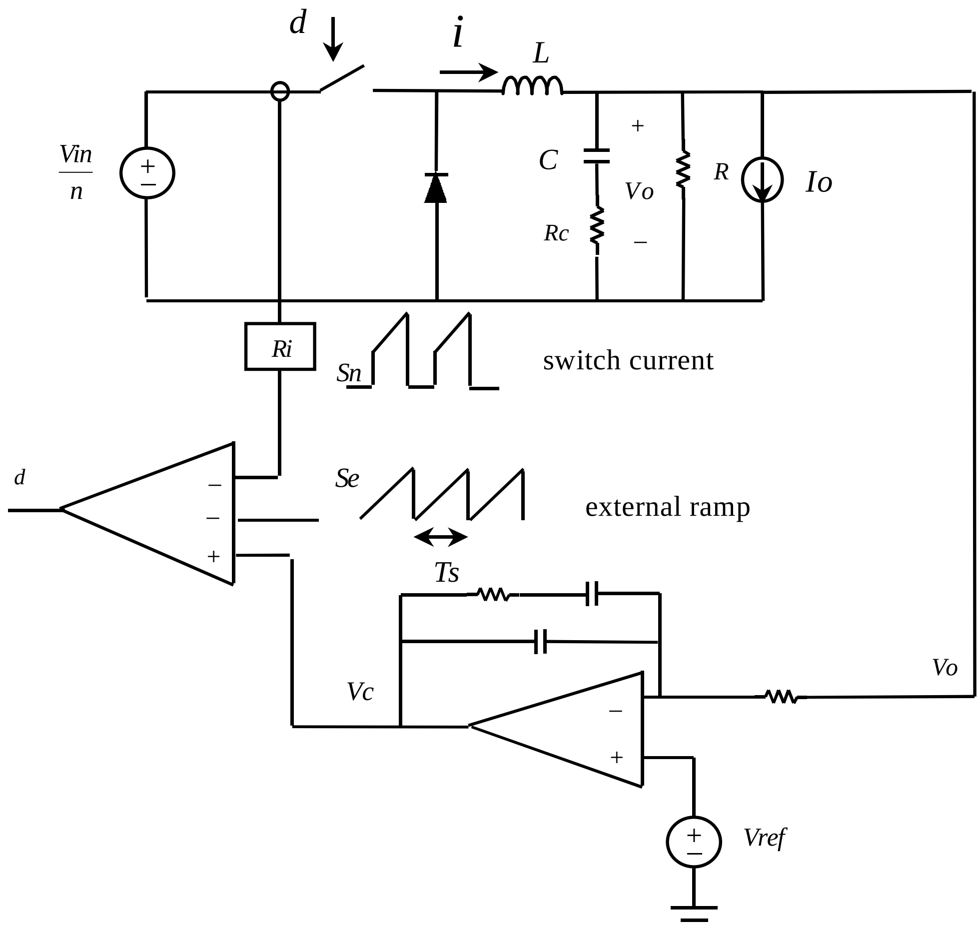


Fig. 6.2. Simplified forward converter circuit diagram with peak current mode control.

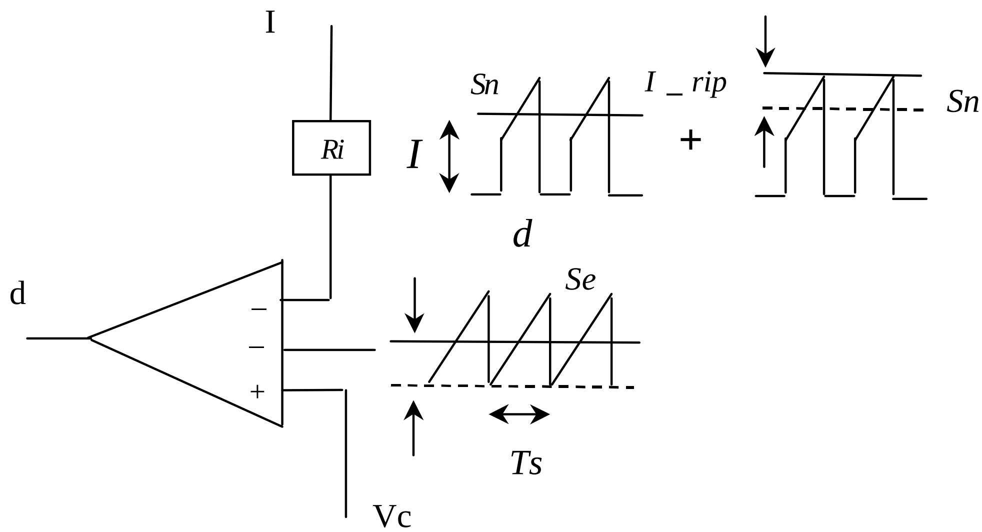


Fig. 6.3. Circuit diagram for deriving duty cycle equations.

6.2.2 Circuit dynamic performances under line transient

As in (6.5), the duty cycle is a function of F_m, i, and v_c, since (6.5) is a nonlinear equation, we can not derive the explicit equations of the duty cycle during large-signal transient. We will study the transient responses of each individual term under small perturbations, and predict the duty cycle large-signal behavior correspondingly.

6.2.2.1 Dynamics of the control v_c under small perturbation of the input voltage

Fig. 6.4 shows converter average model circuit diagram. Similar to the voltage loop derivation in the previous chapter, we can derive control to input voltage equation from following steps:

$$\frac{\Delta v_c}{\Delta v_{in}} = \frac{\Delta v_c}{\Delta v_o} \cdot \frac{\Delta v_o}{\Delta v_{in}} \tag{6.6}$$

T_v is the voltage loop gain with current loop closed, so

$$\frac{\Delta v_c}{\Delta v_{in}}\Big|_{close} = -\frac{T_v}{\dfrac{\Delta v_o}{\Delta v_c}} \cdot \frac{\dfrac{\Delta v_o}{\Delta v_{in}}}{1+T_v} = \frac{\dfrac{\Delta v_o}{\Delta v_{in}}}{\dfrac{\Delta v_o}{\Delta v_c}} \cdot \frac{T_v}{1+T_v} \tag{6.7}$$

$$\frac{\Delta v_c}{\Delta v_{in}}\Big|_{close} = -\frac{R}{R_i} \cdot \frac{\dfrac{L}{R \cdot T_s} + \left(D' \cdot m_c - \dfrac{1}{2}\right)}{D \cdot \left[m_c \cdot D' - \left(1 - \dfrac{D}{2}\right)\right]} \cdot \frac{T_v}{1+T_v} \tag{6.8}$$

where

$$m_c = 1 + \frac{S_e}{S_n} \tag{6.9}$$

The detailed derivations of the small-signal transfer functions with current mode control can be found in [80-86]. If we define the crossover frequency of the closed loop gain is ω_c as shown in Fig. 6.5, then

$$\frac{\Delta v_c}{\Delta v_{in}}\Big|_{close} = -k_v \cdot \frac{1}{1 + s/\omega_c} \tag{6.10}$$

$$\Delta v_c(t) = -k_v \cdot \left(1 - e^{-\omega_c \cdot t}\right) \cdot \Delta v_{in} \tag{6.11}$$

where,

$$k_v = \frac{R}{R_i} \cdot \frac{\dfrac{L}{R \cdot T_s} + \left(D' \cdot m_c - \dfrac{1}{2}\right)}{D \cdot \left[m_c \cdot D' - \left(1 - \dfrac{D}{2}\right)\right]} \tag{6.12}$$

Since k_v is a constant for a specific circuit, the small-signal response of the error voltage, v_c, is a function of the control bandwidth, ω_c, and is a first order function.

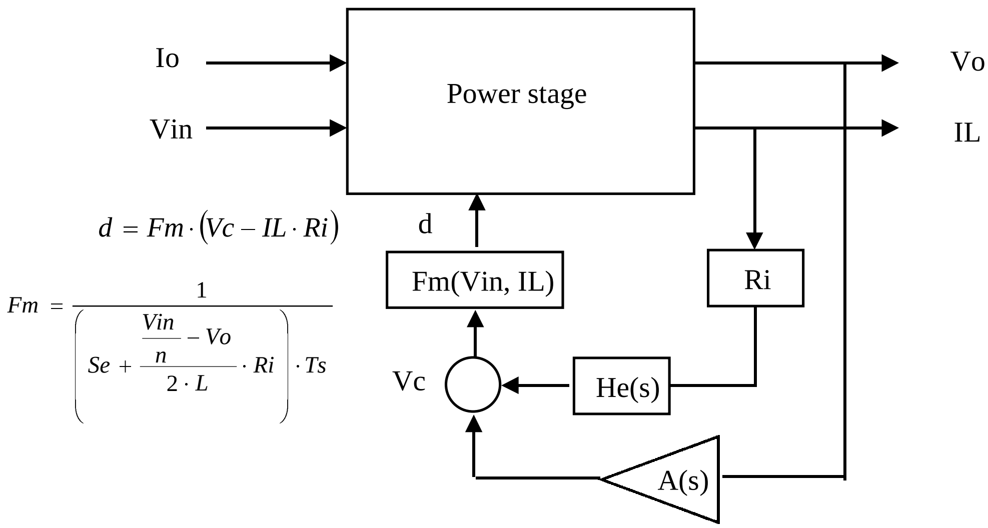


Fig. 6.4 Simplified average model circuit diagram.

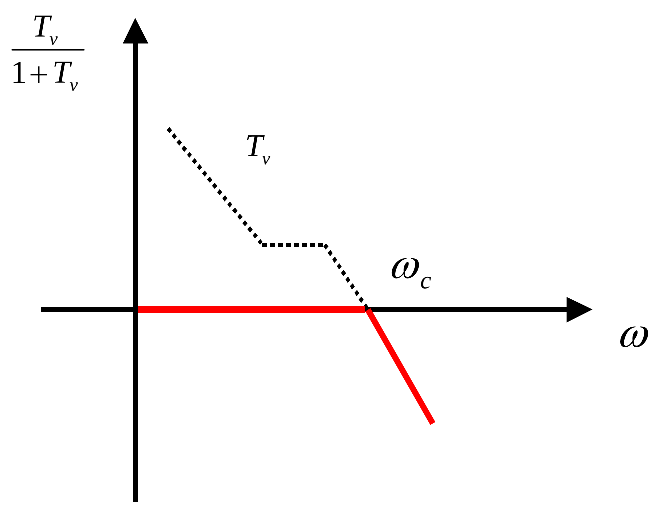


Fig. 6.5 Bode plot of $\frac{T_v}{1+T_v}$. T_v is the loop gain when current loop is closed.

6.2.2.2 Dynamics of the inductor current i_l under small perturbation of the input voltage

From Fig. 6.4, we get:

$$I_L = I_o + \frac{S \cdot C}{1 + S \cdot R_c \cdot C} \cdot V_o \tag{6.13}$$

$$\frac{\Delta i_l}{\Delta v_{in}} = \frac{S \cdot C}{1 + S \cdot R_c \cdot C} \cdot \frac{\Delta v_o}{\Delta v_{in}} \tag{6.14}$$

$$\frac{\Delta v_o}{\Delta v_{in}}\Big|_{close} = \frac{D \cdot \left[m_c \cdot D' - \left(1 - \frac{D}{2}\right)\right]}{\frac{L}{R \cdot T_s} + \left(D' \cdot m_c - \frac{1}{2}\right)} \cdot F_p(S) \cdot F_h(S) \cdot \frac{1}{1 + T_v} \tag{6.15}$$

where,

$$F_p(S) = \frac{1 + S \cdot C \cdot R_c}{1 + \frac{S}{\omega_p}} \tag{6.16}$$

$$\omega_p = \frac{1}{C \cdot R} + \frac{T_s}{L \cdot C} \cdot (m_c \cdot D' - 0.5) \tag{6.17}$$

$$F_h(S) = \frac{1}{1 + \frac{S}{\omega_n \cdot Q_p} + \frac{S^2}{\omega_n^2}} \tag{6.18}$$

$$Q_p = \frac{1}{\pi \cdot (m_c \cdot D' - 0.5)} \tag{6.19}$$

The transfer function, $F_p(S)$, gives the dominant low-frequency characteristics of the system and the transfer function, $F_h(S)$, shows the effects of the sampling action on the system.

Equation (6.15) can be written as:

$$\frac{\Delta i_L}{\Delta v_{in}}\Big|_{close}=\frac{D\cdot\left[m_c\cdot D'-\left(1-\frac{D}{2}\right)\right]}{\frac{L}{R\cdot T_s}+\left(D'\cdot m_c-\frac{1}{2}\right)}\cdot F_h(S)\cdot\frac{1}{1+T_v}\cdot\frac{S\cdot C}{1+\frac{S}{\omega_p}} \tag{6.20}$$

Since ω_p is a low frequency pole, assume:

$$\omega_p<\omega_c \tag{6.21}$$

$$\frac{\Delta i_L}{\Delta v_{in}}\Big|_{close}=k_i\cdot\frac{s/\omega_c}{1+s/\omega_c} \tag{6.22}$$

$$\Delta i_L(t)=k_i\cdot e^{-\omega_c\cdot t}\cdot\Delta v_{in} \tag{6.23}$$

in which,

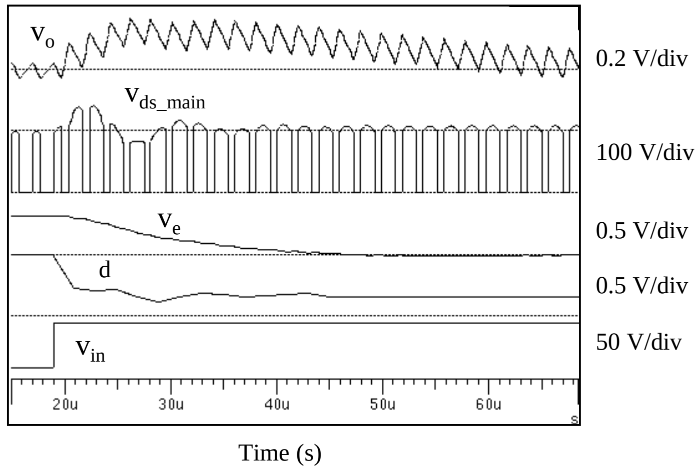
$$k_i=\frac{D\cdot\left[m_c\cdot D'-\left(1-\frac{D}{2}\right)\right]}{\frac{L}{R\cdot T_s}+\left(D'\cdot m_c-\frac{1}{2}\right)} \tag{6.24}$$

Since k_i is a constant for a specific circuit, the small-signal response of the inductor current, i_L, is a function of the control bandwidth, ω_c, and is a first order function.

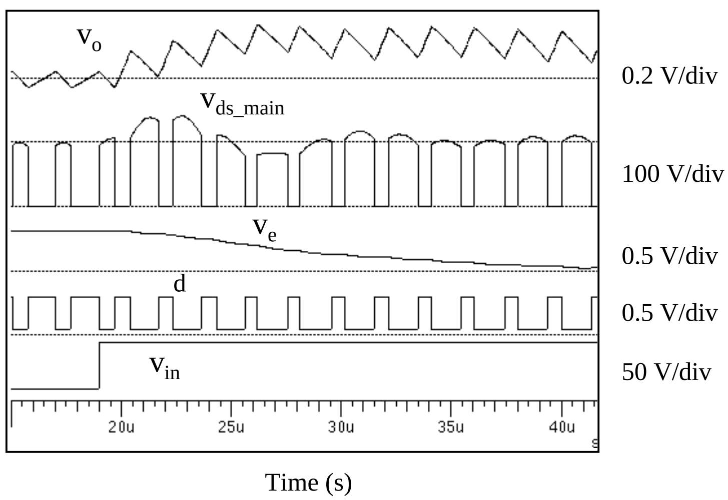
6.2.2.3 Dynamics of the duty cycle under line transient

Since V_o's change is not significant compared to V_{in}'s during line transient, F_m is basically a function of V_{in}. For an input voltage from low to high, Vin increases, so Fm decreases. v_c and i_l are both first order functions of crossover frequency as in (6.10) and (6.18). Compared with the change of v_c and I_l in this case, change of the F_m dominants the duty cycle function as we called voltage feed-forward mechanism. The duty cycle decreases instantaneously because of the feed-forward control.

Fig. 6.6 shows the circuit response waveform during line step change from 36 V to 72 V, Io = 15 A. The crossover frequency of the circuit is fc = 13.7 kHz. The peak voltage of the main switch during transient is not significant compared with the transient we discussed in voltage control mode. Fig. 6.6(a) shows that averaged duty cycle waveform and Fig. 6.6(b) is a zoomed in of Fig. 6.6(a) with original duty cycle waveform. Both figures show that the duty cycle changes immediately after the next cycle of line change due to the input voltage feed-forward mechanism.



(a)



(b)

Fig. 6.6. Circuit transient response during line step change from 36 V to 72 V, Io = 15 A. fc = 13.7 kHz. (a) averaged duty cycle waveform. (b) zoomed in of figure (a) with original duty cycle waveform. Both figures show that the duty cycle changes immediately after the next cycle of line change due to the input voltage feed-forward mechanism.

6.2.2.4 Dynamics of the state trajectories under line transient

Fig. 6.7 is the same transient as in Fig. 6.6. Vin 36 - 72 V, Io = 15 A. Fig. 6.7(a) is the time domain L_m and C_c waveform. Fig. 6.7(b) is the state trajectory waveform. Fig. 6.7(c) is the average state trajectory waveform. From Fig. 6.7(c) we see that the average state trajectory does not move too far to the right side compared to the one in the voltage mode control.

Fig. 6.8 is a study of the effect of f_c to circuit response. It shows that the reducing of f_c does not have a significant effect in line transient response as in voltage mode control due to the feed-forward control. In the figure, Vin is from 36 to 72V, Io is 15 A. Fig. 6.8(a) is the time domain waveform with f_c = 13.7 kHz. The peak voltage of main switch is 132 V. Fig. 6.8(b) is the time domain waveform with f_c = 3 kHz. The peak voltage of main switch is 132 V. Fig. 6.8(c) is the average stage trajectory with f_c = 13.7 kHz. Fig. 6.8(d) is the average stage trajectory with f_c = 3 kHz. Fig. 6.8(c) and (d) does not show significant differences in trajectory movement

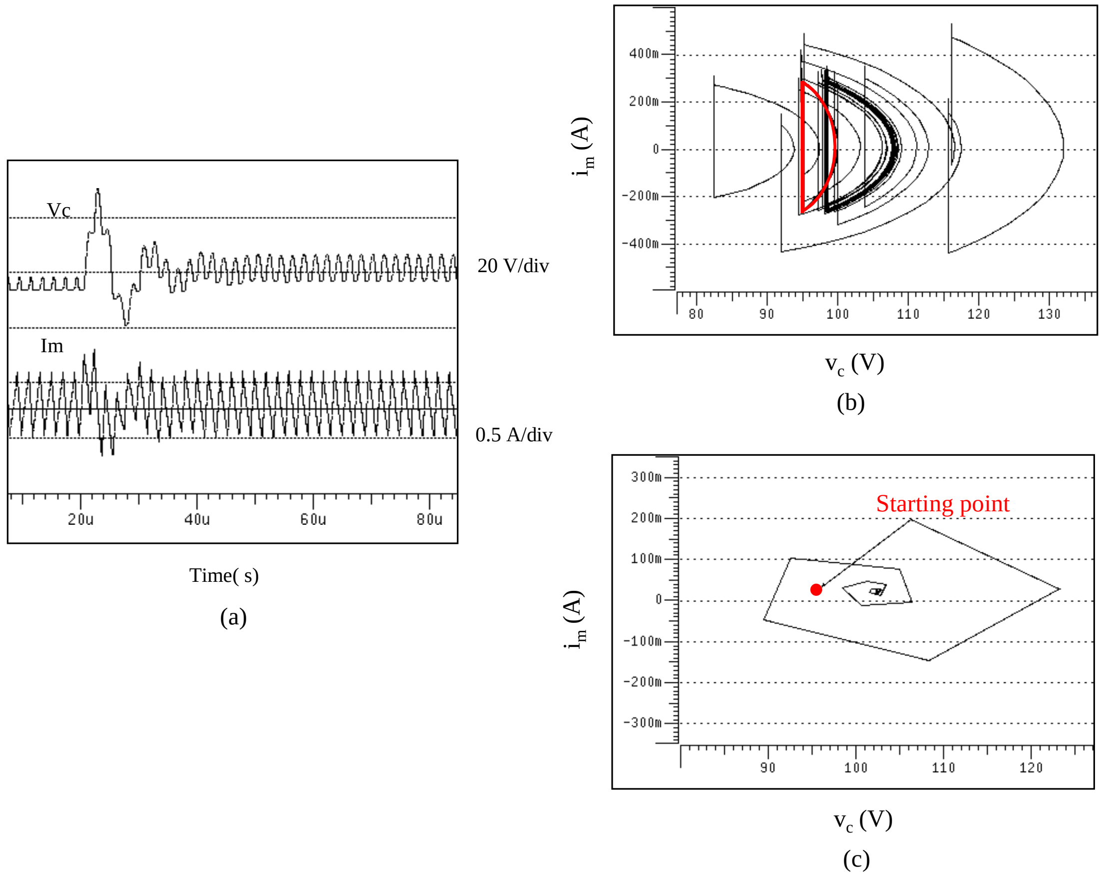


Fig. 6.7. Same transient as in Fig. 6.6. Vin 36 - 72 V, Io = 15 A. (a) time domain L_m and C_c waveform. (b) state trajectory waveform. (c) average state trajectory waveform.

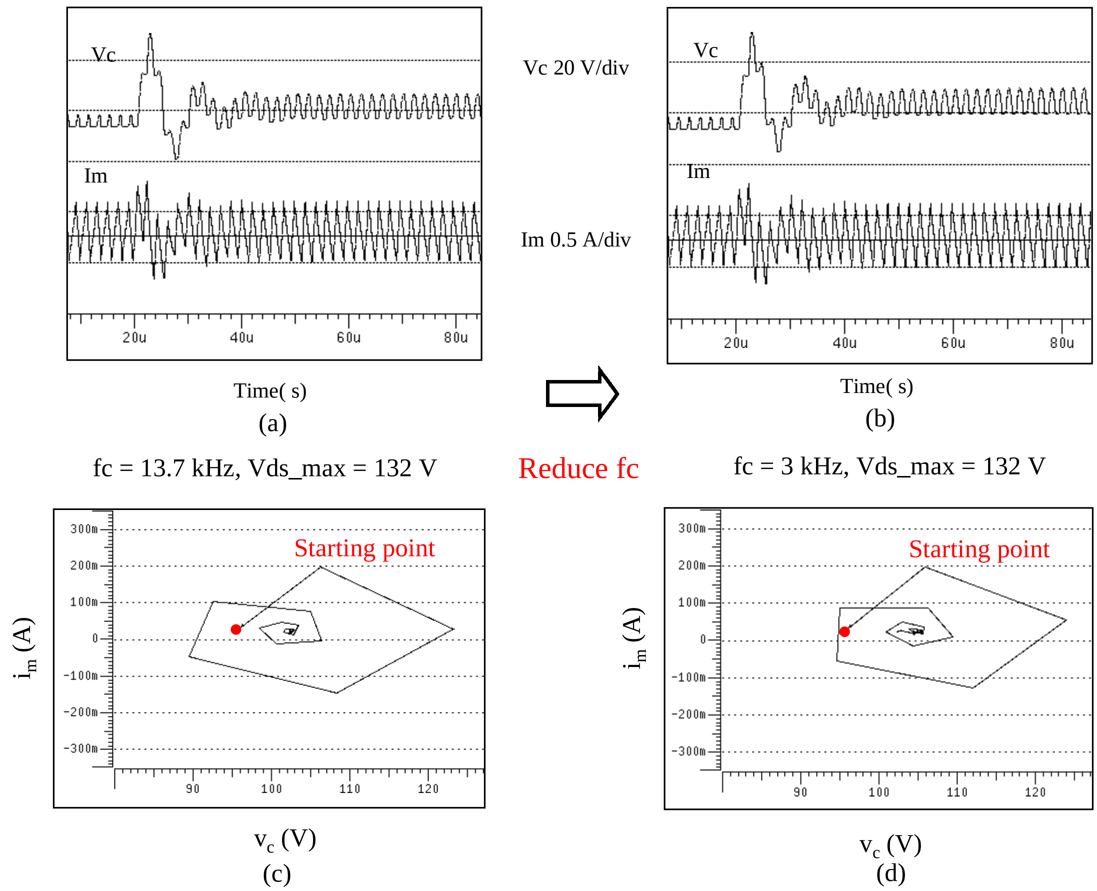


Fig. 6.8 Reducing f_c does not have a significant effect in line transient response as in voltage mode control due to the feed-forward control. Vin from 36 - 72 V, Io = 15 A. (a) time domain waveform with f_c = 13.7 kHz. The peak voltage of main switch is 132 V. (b) time domain waveform with f_c = 3 kHz. The peak voltage of main switch is 132 V. (c) average stage trajectory with f_c = 13.7 kHz. (d) average stage trajectory with f_c = 3 kHz. (c) and (d) does not show significant differences in trajectory movement.

6.2.3 Comparison of line transient dynamics with voltage and current mode control

From previous analysis, we see in voltage mode control, $\Delta v_{c\_center}(\max)$ as shown in Fig. 6.1 is

$$\Delta v_{c\_center}(\max) = \frac{D_{\max}}{D_{\max}'} \cdot \Delta V_{in} \tag{6.25}$$

and the worst case of voltage mode control happens at

- minimum line (maximum duty cycle)
- input step change from low to high
- low bandwidth and high resonant frequency of reset circuit.

In current mode control, due to the feed-forward mechanism, $\Delta v_{c\_center}(\max)$ is reduced significantly when line from low to high.

$$\Delta v_{c\_center}(\max) = \frac{D_{feed\_forward}}{D_{feed\_forward}'} \cdot V_{in}(new) - \frac{D_{\max}}{D_{\max}'} \cdot V_{in}(old) \tag{6.26}$$

Where V_{in}(old) is the input voltage before the step change, V_{in}(new) is the input voltage after the step change, and $D_{feed\_forward}$ is the duty cycle immediately after the input step change due to the feed-forward mechanism.

If we define the feed-forward mechanism gain

$$k_f = \frac{S_e + \dfrac{\dfrac{V_{in}(new)}{n} - V_o}{2 \cdot L} \cdot R_i}{S_e + \dfrac{\dfrac{V_{in}(old)}{n} - V_o}{2 \cdot L} \cdot R_i}, \tag{6.27}$$

then

$$D_{feed\_forward} = \frac{D_{\max}}{k_f} \tag{6.28}$$

Since k_f >1 when the input voltage steps from low to high, the duty cycle is reduced immediately.

Fig. 6.9 compares the transient response of the active-clamp circuit with current and voltage mode control. Both circuit is designed with the same bandwidth, f_c = 14 kHz. Fig. 6.9(a) is the transient waveforms with current mode control. Fig. 6.9(b) is the transient waveforms with voltage mode control. Fig. 6.9(c) is the average state trajectory in current mode control. Fig. 6.9(d) is the average state trajectory in voltage mode control. The worst case of the line transient in current mode control happens at V_{in} from 36 V to 72 V transient at full load as shown in Fig. 6.9(a), there is no design problems in line transient

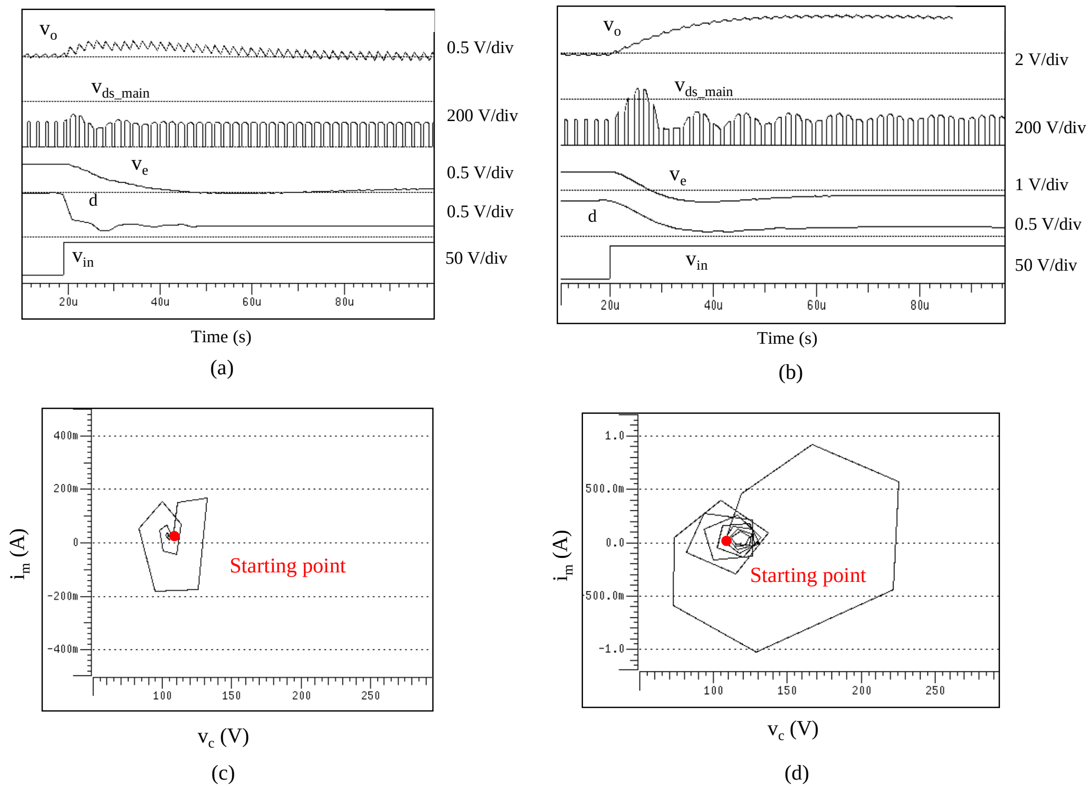


Fig. 6.9. Comparison of transient response of the active-clamp circuit with current and voltage mode control. Simulation condition: V_{in} from 36 to 72 V, I_o = 30 A. Both circuit has f_c = 14 kHz. (a) transient waveforms with current mode control. (b) transient waveforms with voltage mode control. (c) average state trajectory in current mode control. (d) average state trajectory in voltage mode control.

6.2.4 Circuit dynamic performances under load transient

6.2.4.1 Dynamics of the control v_c under small perturbation of the load

Similar to input transient derivations, we can derive the control to load equation from following steps:

$$\frac{\Delta v_c}{\Delta i_o} = \frac{\Delta v_c}{\Delta v_o} \cdot \frac{\Delta v_o}{\Delta i_o} \tag{6.29}$$

If T_v is the loop gain with current loop closed, then

$$\frac{\Delta v_c}{\Delta i_o}\Big|_{close} = -\frac{T_v}{\frac{\Delta v_o}{\Delta v_c}} \cdot \frac{\frac{\Delta v_o}{\Delta i_o}}{1+T_v} = \frac{\frac{\Delta v_o}{\Delta i_o}}{\frac{\Delta v_o}{\Delta v_c}} \cdot \frac{T_v}{1+T_v} \tag{6.30}$$

$$\frac{\Delta v_c}{\Delta i_o}\Big|_{close} = \frac{R_i}{F_h(s)} \cdot \frac{T_v}{1+T_v} \tag{6.31}$$

If the crossover frequency of the closed loop gain is ω_c, then

$$\frac{\Delta v_c}{\Delta i_o}\Big|_{close} = R_i \cdot \frac{1}{1+s/\omega_c} \tag{6.32}$$

$$\Delta v_c(t) \approx R_i \cdot \left(1-e^{-\omega_c \cdot t}\right) \cdot \Delta i_o \tag{6.33}$$

So similar to line transient, the small-signal response of the error voltage, v_c, is a function of the control bandwidth, ω_c, and is a first order function.

6.2.4.2 Dynamics of the inductor current i_l under small perturbation of the load

From Fig. 6.4 we get:

$$I_L = I_o + \frac{S \cdot C}{1+S \cdot R_c \cdot C} \cdot V_o \tag{6.34}$$

$$\frac{\Delta i_l}{\Delta i_o} = 1 + \frac{S \cdot C}{1 + S \cdot R_c \cdot C} \cdot \frac{\Delta v_o}{\Delta i_o} \tag{6.35}$$

$$\frac{\Delta v_o}{\Delta i_o}\Big|_{close} = \frac{R}{1 + \frac{R \cdot T_s}{L} \cdot \left(D' \cdot m_c - \frac{1}{2} \right)} \cdot F_p(S) \cdot \frac{1}{1 + T_v} \tag{6.36}$$

$$\frac{\Delta i_L}{\Delta i_o}\Big|_{close} = 1 - \frac{R}{1 + \frac{R \cdot T_s}{L} \cdot \left(D' \cdot m_c - \frac{1}{2} \right)} \cdot \frac{1}{1 + T_v} \cdot \frac{s \cdot C}{1 + \frac{s}{\omega_p}} \tag{6.37}$$

$$\frac{\Delta i_L}{\Delta i_o}\Big|_{close} = 1 - \frac{s}{s + \omega_c} \cdot \frac{s}{s + \omega_p} \tag{6.38}$$

$$\Delta i_L(t) = \left(1 - \frac{\omega_c}{\omega_c - \omega_p} \cdot e^{-\omega_c \cdot t} + \frac{\omega_p}{\omega_c - \omega_p} \cdot e^{-\omega_p \cdot t} \right) \cdot \Delta i_o \tag{6.39}$$

Since ω_p is a low frequency pole, the system response will first be affected by control bandwidth, ω_c. The small-signal response of the inductor current, i_L, is close to the function of the control bandwidth, ω_c, and is a first order function.

6.2.4.3 *Dynamics of the duty cycle under load transient*

Since V_{in} does not change during load transient, F_m is basically a function of V_o. For a load step change from low to high, V_o decreases, so Fm decreases. v_c and i_l are both first order functions of crossover frequency as in (6.26) and (6.33). The duty cycle equation is:

$$\Delta d(t) = F_m \cdot R_i \cdot \left(\frac{\omega_p}{\omega_c - \omega_p} \cdot \left(e^{-\omega_c \cdot t} - e^{-\omega_p \cdot t} \right) \right) \cdot \Delta i_o \tag{6.40}$$

When V_o's change is not significant, the change of the F_m does not dominants the duty cycle function, this happens in most of the case due to the specification of the output voltage.

Fig. 6.10 shows the circuit response waveform during the load step change from 15 A to 30 A, Vin = 36 V. The crossover frequency of the circuit is fc = 13.7 kHz. The first rising of the duty cycle is mainly determine by crossover frequency of the control loop and it is a first order system.

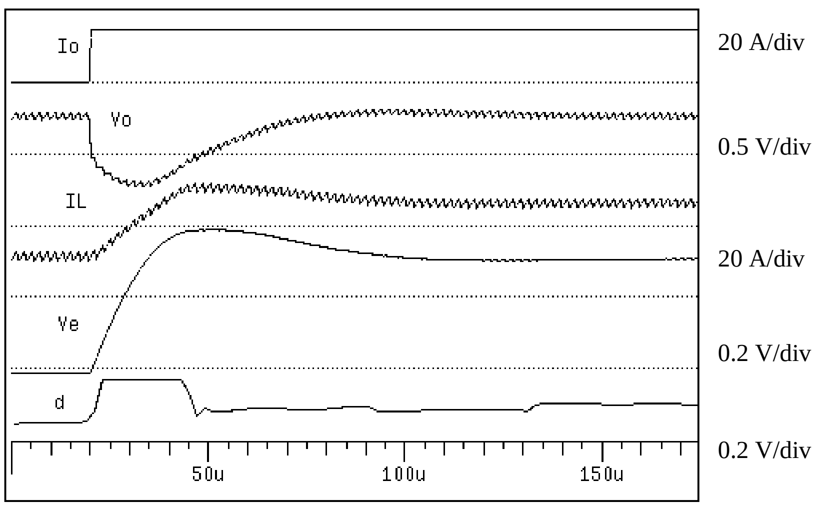


Fig. 6.10 Transient response waveform during load step chagne from 15 A to 30 A, Vin = 36 V. f_c = 13.7 kHz.

6.2.4.4 Dynamics of the state trajectories under load transient

Fig. 6.11 has the same load transient condition as Fig. 6.10. The additional output voltage-feedback due to the change of F_m doesn't have significant effect. Fig. 6.11(a) is the time domain L_m and C_c waveform. Fig. 6.11(b) is the state trajectory waveform. Fig. 6.11(c) is the drain to source voltage of the main switch . Fig. 6.11(d) is the average state trajectory waveform. From Fig. 6.11(d) we see that the average state trajectory moves far to right side compared to that in the line transient. The possible circuit design problems are marked by the dotted cycle as in Fig. 6.11.

Fig. 6.12 is a study of the effect of f_c in load transient. It shows that the reducing of f_c decreases the voltage stress of the main switch. In the figure, Vin is 36 V, Io is from 15 A - 30 A. Fig. 6.12(a) is the time domain waveform with f_c = 13.7 kHz. The peak voltage of main switch is 184 V. Fig. 6.12(b) is the time domain waveform with f_c = 8.2 kHz. The peak voltage of main switch is 131 V. The main switch voltage stress is reduced significantly by reducing the control loop bandwidth.

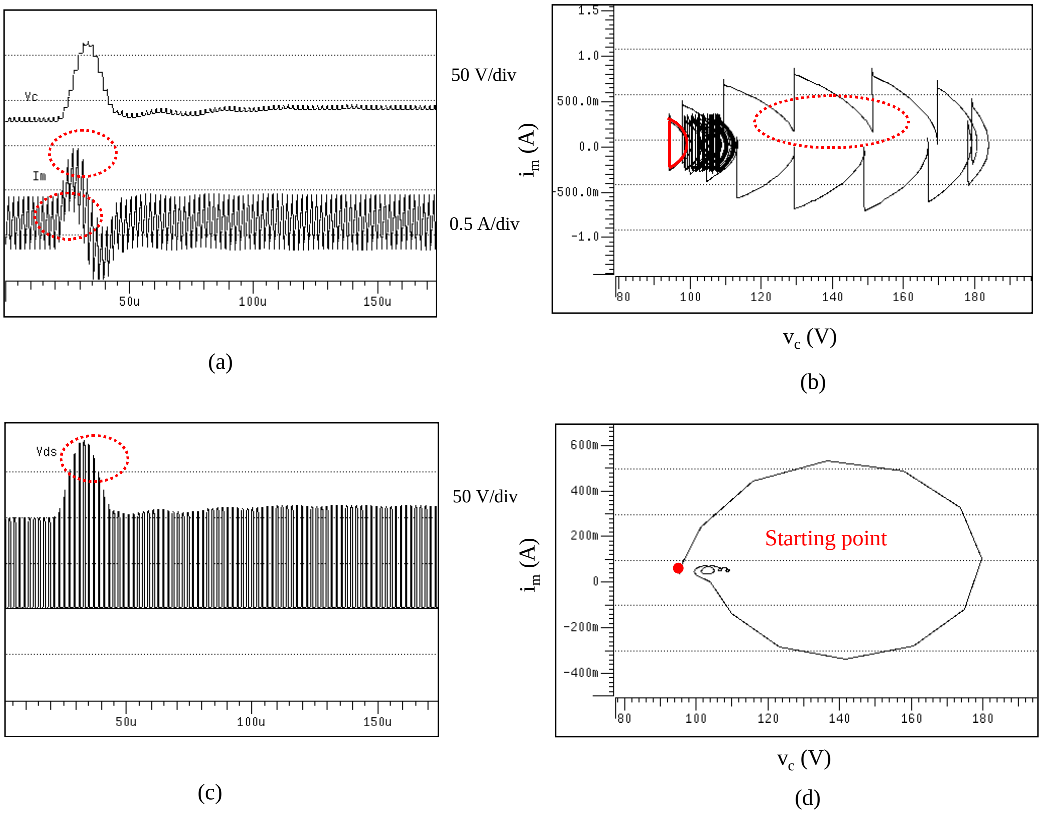


Fig. 6.11. Io from 15 A to 30 A, Vin = 36 V. f_c = 13.7 kHz. (a) the time domain L_m and C_c waveform. (b) the state trajectory waveform. (c) the main switch drain to source voltage. (d) the average state trajectory waveform. The circuit problems are shown in dotted cycles.

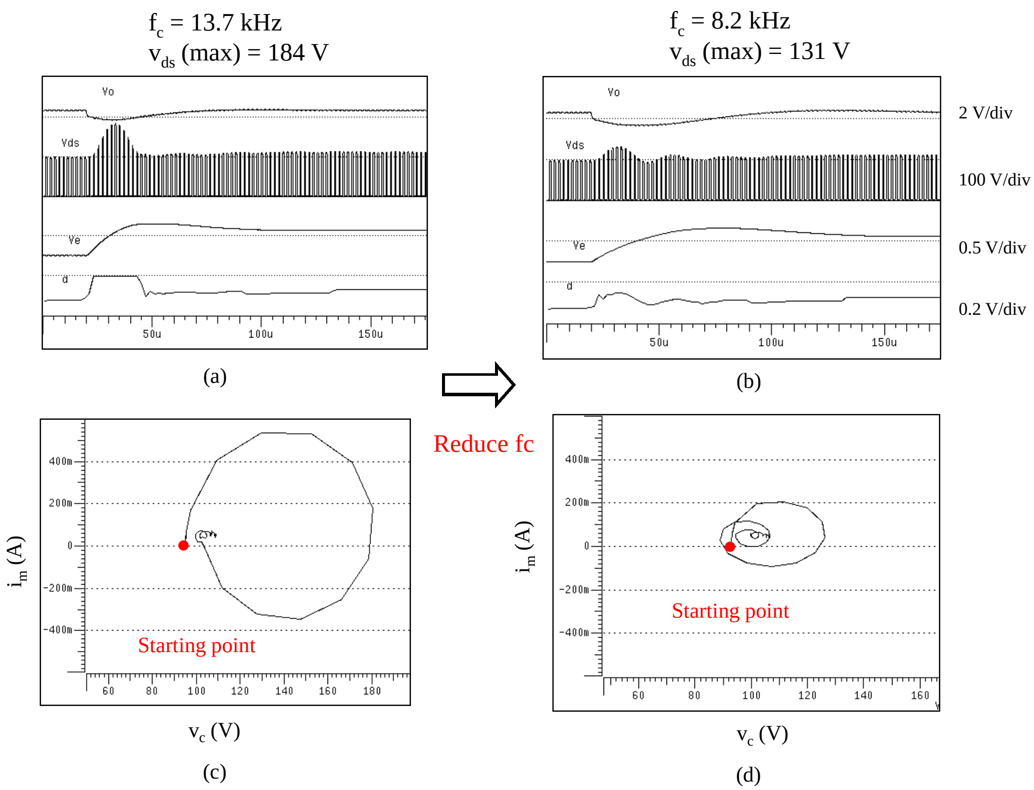


Fig. 6.12. Effect of fc in load transient. (a) the time domain waveform with f_c = 13.7 kHz. The peak voltage of main switch is 184 V. (b) the time domain waveform with f_c = 8.2 kHz. The peak voltage of main switch is 131 V. The main switch voltage stress is reduced by reducing the control loop bandwidth significantly. (c) average state trajectory with f_c = 13.7 kHz. (d) average state trajectory with f_c = 8.2 kHz.

6.2.5 Comparison of load transient dynamics with voltage and current mode control

As shown in Fig. 6.1, $v_{c\_center}(t)$ is

$$v_{c\_center}(t) = \frac{d(t)}{d(t)'} \cdot V_{in} \tag{6.41}$$

The worst case in load transient happens when duty cycle has the largest jump at the beginning of the transient. Similar to voltage mode control, in current mode control, the duty cycle jump is a function of first order system:

$$\Delta d(t) = F_m \cdot R_i \cdot \left(\frac{\omega_p}{\omega_c - \omega_p} \cdot \left(e^{-\omega_c \cdot t} - e^{-\omega_p \cdot t} \right) \right) \cdot \Delta i_o \tag{6.42}$$

Fig. 6.13 shows the transient waveforms of the active-clamp circuit during load transient in both voltage mode (a) and current mode (b) control. The simulation condition is Vin = 36 V, Io from 15 A to 30 A. Fig. 6.13(c) is the average state trajectory in current mode control and Fig. 6.13(d) is the average state trajectory in voltage mode control. Even the load transient response are not exactly the same in both cases, circuit has large voltage and current stresses and could have problems as shown in Fig. 6.11. The worst case happens at

- minimum line
- load step change from low to high
- high bandwidth.

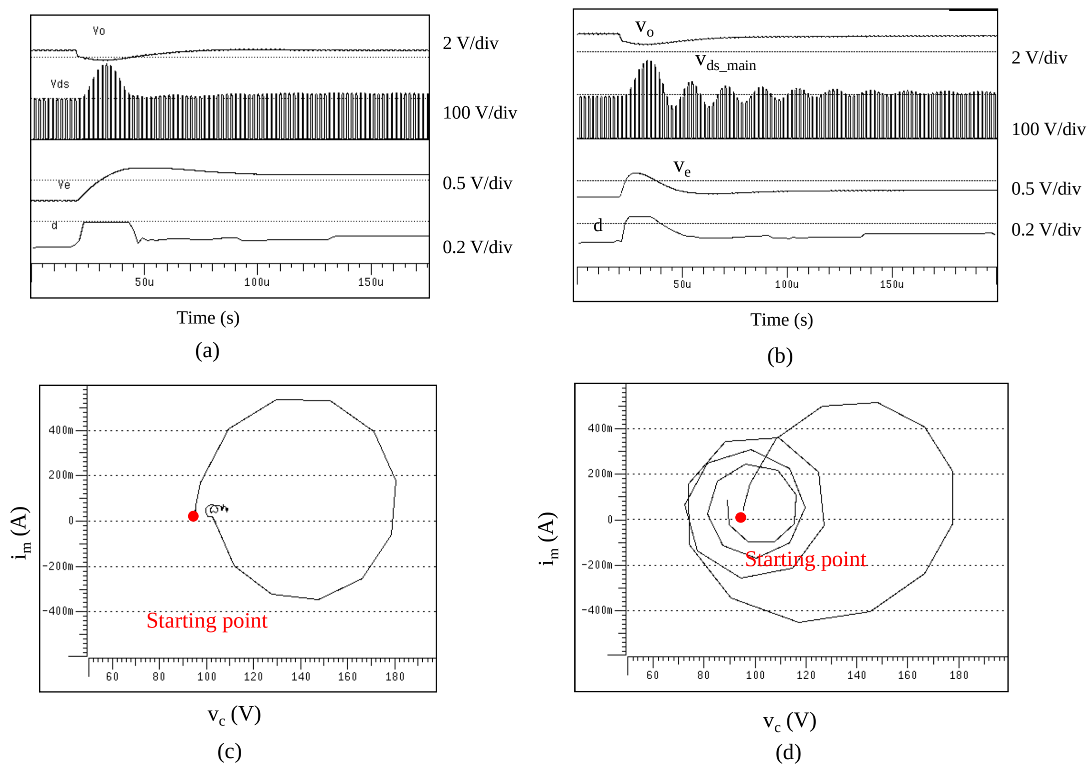


Fig. 6.13. Line transient response of the active-clamp circuit in (a) voltage mode and (b) current mode control. (c) is the average state trajectory in current mode control and (d) is in voltage mode control. It shows that even the transient responses in current mode control and voltage mode control are different, both transients have large voltage and current stresses and could cause circuit problems.

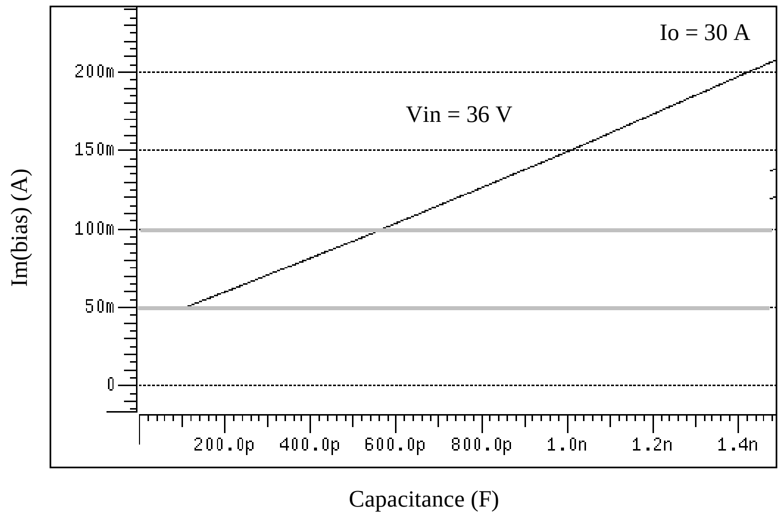
6.3 Design considerations of the power transformer at steady state operations

As we discussed in the previous chapters, the parasitic capacitances and the leakage inductance of the transformer cause a positive or negative dc bias of the magnetizing current of the transformer. This dc bias could cause the transformer saturation, the diode reverse recovery problem (with a large positive dc bias), and the active-clamp switch to lose ZVS turn-on (with a large negative dc bias). It is very important to have an adequate transformer design to avoid these problems.

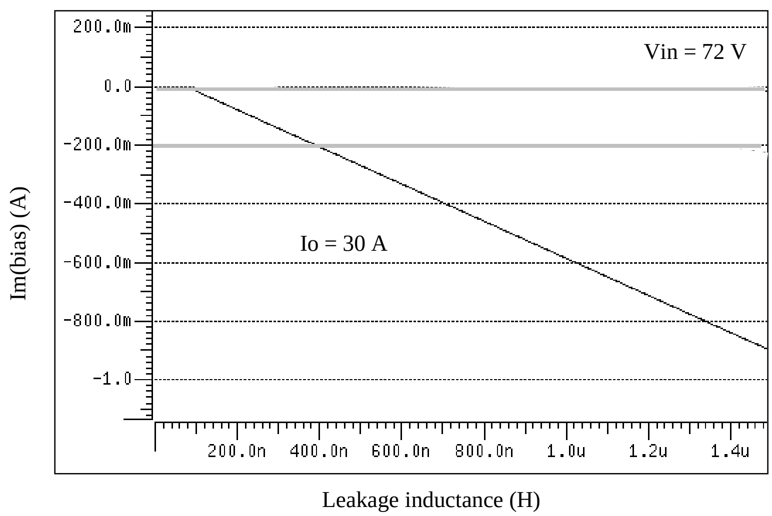
This section shows how to take into account the effect of the dc bias of the magnetizing current in the transformer design with the aid of simulated design curves. The circuit specifications and the parameters of the 5 V forward converter power supply system are: V_{in} = 36 - 72 V, I_o = 0 - 30 A, transformer turns, N_p = 4 and N_s = 1, switching frequency F_s = 500 kHz, and the equivalent parasitic capacitance C_s = 200 pF.

6.3.1 Generating design curves of the maximum dc magnetizing current

The maximum positive dc bias of the magnetizing current occurs at low line full load with maximum duty cycle; and is a function of the parasitic capacitance; the maximum negative dc bias of the magnetizing current occurs at high line full load, and is a function of the leakage inductance. The design curves can be obtained by simulating the virtual prototype with different parameter values as shown in Fig. 6.14. Fig. 6.14(a) shows the maximum positive dc bias vs. parasitic capacitance at low line full load, and Fig. 6.14(b) shows the maximum negative dc bias vs. leakage inductance at the high line and full load.



(a)

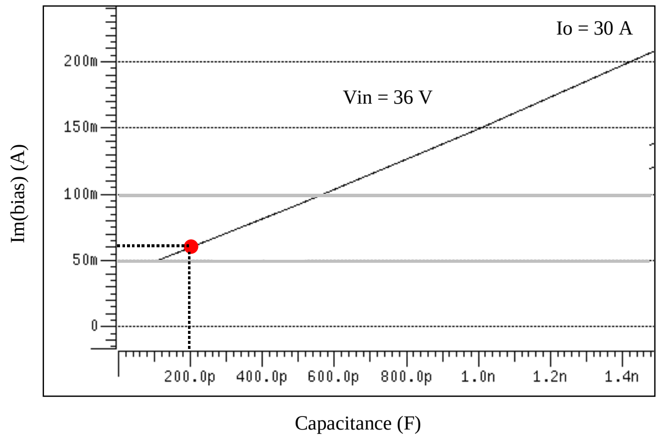


(b)

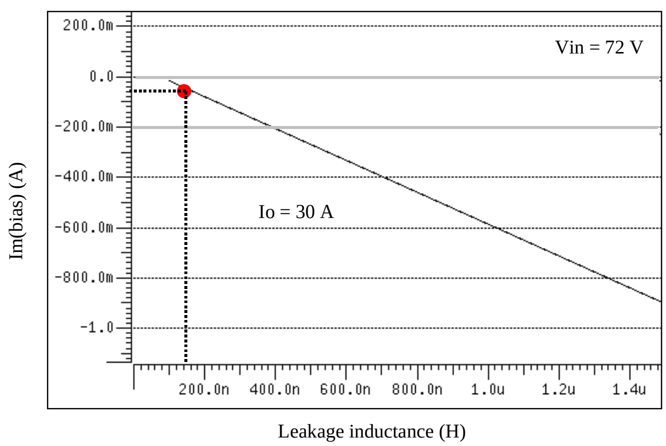
Fig. 6.14. The design curves of the maximum dc bias of the magnetizing current. (a) the maximum positive dc bias with different parasitic capacitances. (b) the maximum negative dc bias with different leakage inductances.

6.3.2 Estimating the maximum dc bias of the magnetizing current

The equivalent parasitic capacitance C_s is 200 pF, so the maximum positive dc bias of the magnetizing current is 60 mA as shown in Fig. 6.15(a); the estimated leakage inductance L_{lk} is 150 nH, so the maximum negative dc bias is 60 mA as shown in Fig. 6.15(b). The maximum dc bias in absolute value, $\max(|I_m(bias)|)$, is 60 mA.



(a)



(b)

Fig. 6.15. The estimated maximum dc bias of the magnetizing current. (a) the maximum positive dc bias with C_s = 200 pF. (b) the maximum negative dc bias with L_{lk} = 150 nH.

6.3.3 Verifying the transformer non-saturation

The definitions of the flux terms in magnetic equations are shown in Fig. 6.16. The flux bias of the transformer core due to the parasitic capacitance and the leakage inductance is:

$$B_{bias} = \mu \cdot \frac{N_p \cdot \max(|I_m(bias)|)}{l_e} \tag{6.43}$$

where $\max(|I_{m\_dc}|)$ is the maximum dc bias current, N_p is the primary winding turns, and l_e is the magnetic path length. The condition for the transformer core has non-saturation is

$$\frac{1}{2} \cdot B_{pp} + B_{bias} < B_{sat} \tag{6.44}$$

where the flux swing,

$$B_{pp} = \frac{V_{in} \cdot \Delta t}{N_p \cdot A_e}, \tag{6.45}$$

in which, A_e is the effective cross sectional area of the core.

If the criterion in (6.38) is not satisfied, the transformer has to be redesigned. One of the possible solutions is to reduce μ by increasing the air gap.

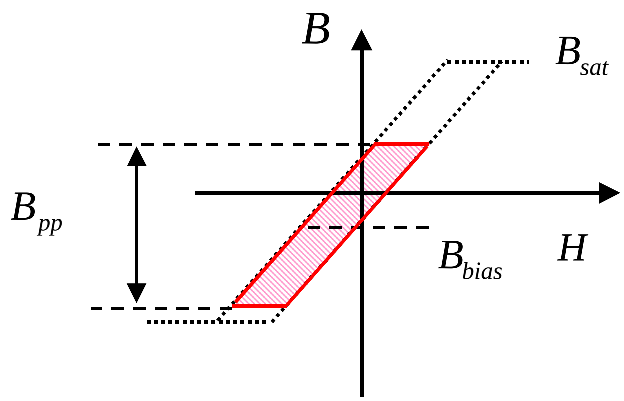


Fig. 6.16 Definition of the flux terms in magnetic equations.

6.3.4 Verifying the proper operation of the active-clamp circuit at steady state.

The condition for the circuit has no diode reverse recovery problem and has ZVS turn-on of the active-clamp switch is:

$$I_m(pp) > 2 \cdot \max(|I_{m\_dc}|). \tag{6.46}$$

So the criterion of the magnetizing inductance is:

$$L_m < \frac{V_{in} \cdot \Delta t}{2 \cdot |I_{m\_dc}|} \tag{6.47}$$

where,

$$L_m = \frac{\mu \cdot N_p{}^2 \cdot A_e}{l_e} \tag{6.48}$$

If the criterion in (6.42) is not satisfied, the transformer has to be redesigned. One of the possible solutions is to reduce μ by increasing the air gap. It is worth to mention that additional design consideration is recommended for the large-signal transient behavior of the active-clamp reset circuit [69], which will be discussed in the following section.

6.4 Design consideration to minimize voltage/current stresses during large-signal transient

6.4.1 Design issues of the active-clamp circuit

As we discussed in the previous chapters, there are several design issues in active-clamp circuit, especially during large-signal transient. Fig. 6.17 shows the load transient waveforms of the active-clamp circuit. The maximum voltage of the main switch and the maximum magnetizing current of the transformer are much larger than that at steady state. These could cause circuit problems such as voltage stresses, transformer saturation, and the diode reverse recovery problem which are marked as dotted circles in Fig. 6.17. Besides large-signal transient problems, circuit could have stability problem due to the interaction of the resonant network of the active-clamp-reset circuit. Fig. 6.18 shows small-signal transfer function of the loop gain. The phase margin of the loop gain at crossover frequency is negative due to the additional pole in the active-clamp-reset circuit near resonant frequency.

This section will demonstrate how to use virtual prototype to provide design information and optimize the design parameters related to these design issues. The design parameters discussed here are the magnetizing inductance of the transformer L_m, the clamp capacitance C_c, the control bandwidth f_c, and the maximum duty cycle limit Dmax. The circuit has input voltage 36 - 72 V, full load 30 A. The duty cycle limit of the controller chip is 0.75. The control bandwidth of the current circuit design is 14 kHz. The design process focuses on solving the potential problems in the circuit: voltage stress of the main switch, transformer core saturation, diode reverse recovery of the active-clamp switch, small-signal instability due to the active-clamp circuit.

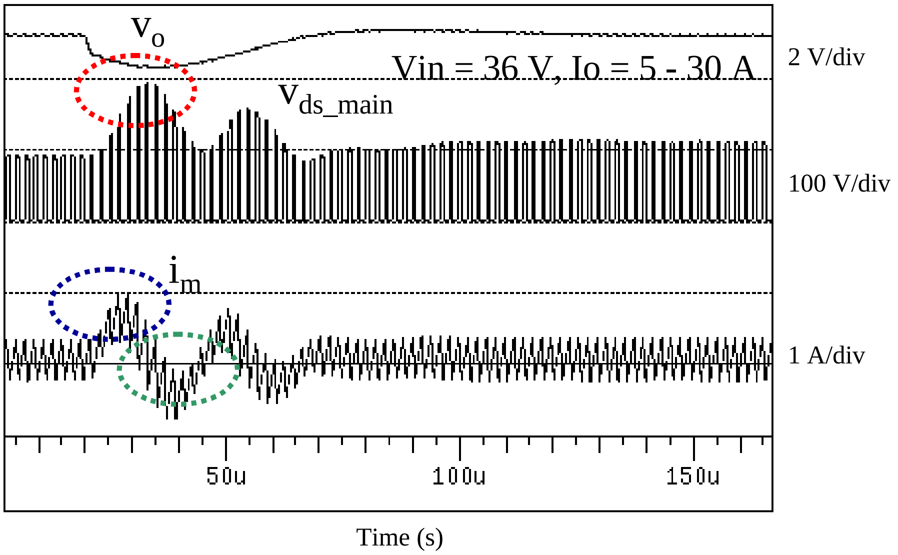


Fig. 6.17 Active-clamp circuit problems during large-signal transient.

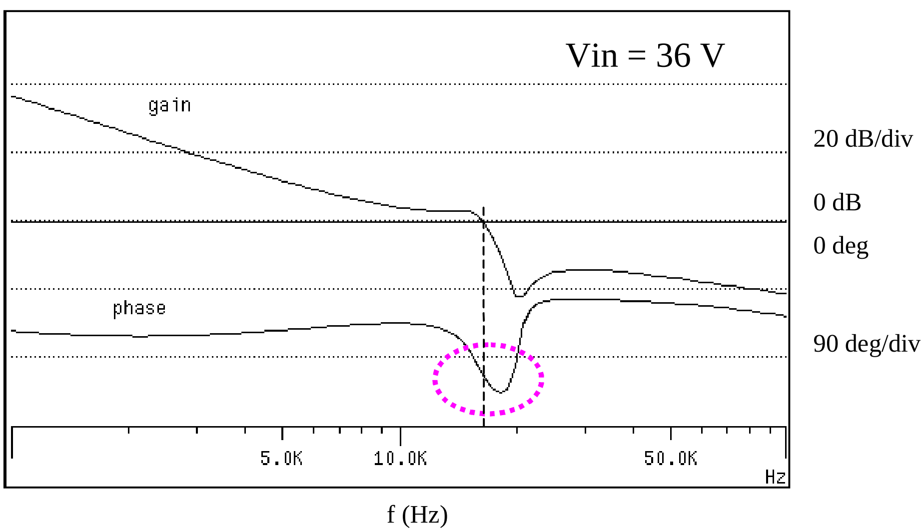


Fig. 6.18 Stability problem due to the resonant network of the active-clamp reset circuit.

6.4.2 Normalization

The normalized peak voltage and peak current values will be used in the design curve. The normalized switch voltage is $\frac{V_s}{V_{in}(\min)}$ and the normalized magnetizing current is $\frac{i_m \cdot Z_o}{V_{in}(\min)}$. The x axis uses f_o as a parameter. Where, V_{in}(min) is the minimum voltage of the circuit, in this circuit example, it is 36 V, f_o is the resonant frequency of the active-clamp circuit, and Z_o is the character impedance.

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_m \cdot C_c}} \tag{6.49}$$

$$Z_o = \sqrt{\frac{L_m}{C_c}} \tag{6.50}$$

6.4.3 Design constraints

There are four design criteria: the voltage stress of the main switch, transformer saturation, reverse recovery problem of the body diode of the active clamp switch, and the small-signal stability problem. For each design criterion, we can draw a forbidden area in the design curve.

6.4.3.1 Design constraint 1: switch voltage stress

Voltage stress: V_s(peak) < V_s (rating)

Where, V_s(peak) is the peak voltage during the transient, V_s(rating) is the device voltage rating of the main switch. If we use nominal curves in the design, the design constraint of the voltage rating is shown as the shaded area in Fig. 6.19.

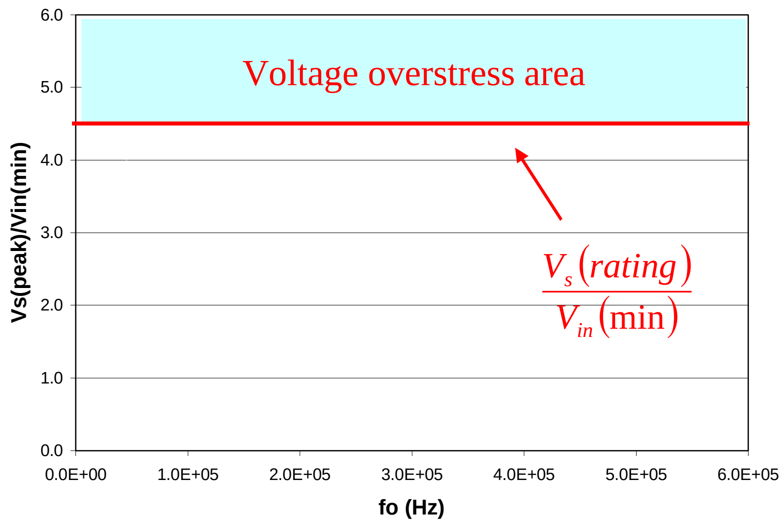


Fig. 6.19. Voltage overstress area in design curve.

6.4.3.2 Design constraint 2: small signal stability

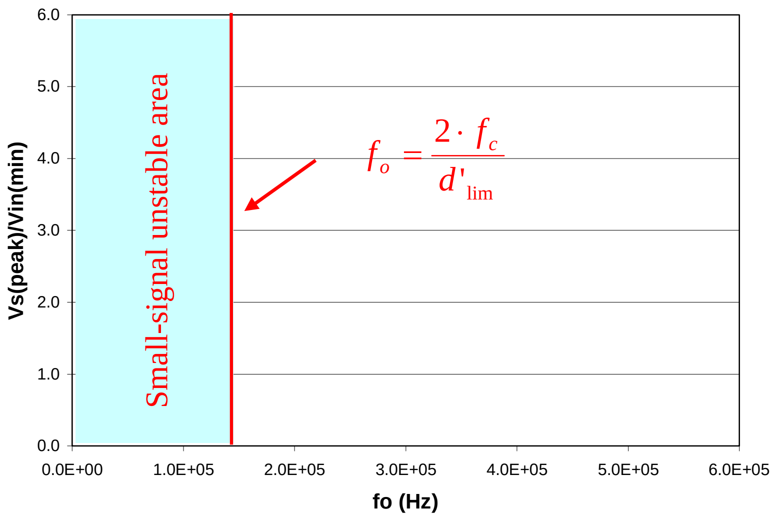
The resonant frequency of the active-clamp circuit should meet the following equation to have a stable system and not affect the phase margin.

$$d'_{\lim} \cdot f_o > 2 \cdot f_c \tag{6.51}$$

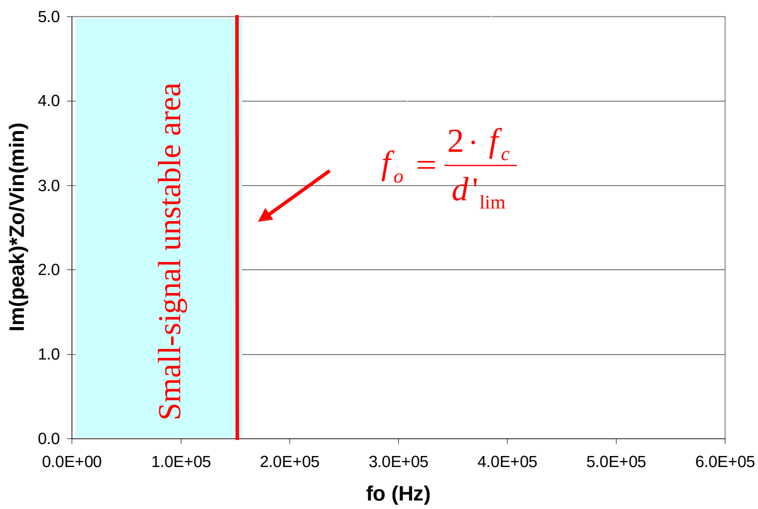
where $d'_{\lim}$ is the duty cycle limit value of the controller chip, f_c is the control bandwidth. So small-signal stable condition is:

$$f_o > \frac{2 \cdot f_c}{d'_{\lim}} \tag{6.52}$$

The design constraints for the small signal stability are shown as the shade areas in Fig. 6.20(a) and (b).



(a)



(b)

Fig. 6.20. Small signal unstable area in design curves. (a) peak switch voltage curve. (b) peak magnetizing current curve.

6.4.3.3 *Design constraint 3: transformer saturation*

Fig. 6.21 shows the relation between flux and magnetizing current, where, A_e is the effective cross sectional area of the core, Lm is the magnetizing current. From Fig. 6.21, we can get:

$$i_m(sat) = \frac{B_{sat} \cdot A_e \cdot N_p}{L_m} \tag{6.53}$$

We can rewrite saturating magnetizing current into:

$$i_m(sat) = \frac{B_{sat} \cdot A_e \cdot N_p \cdot 2 \cdot \pi \cdot f_o}{Z_o} \tag{6.54}$$

The design constraint for transformer saturation is:

$$\frac{i_m(peak) \cdot Z_o}{V_{in}(\min)} < \frac{B_{sat} \cdot A_e \cdot N_p \cdot 2 \cdot \pi \cdot f_o}{V_{in}(\min)} \tag{6.55}$$

The design constraint for the transformer saturation is shown as shaded area in Fig. 6.22. It is a straight line in the normalized design curve.

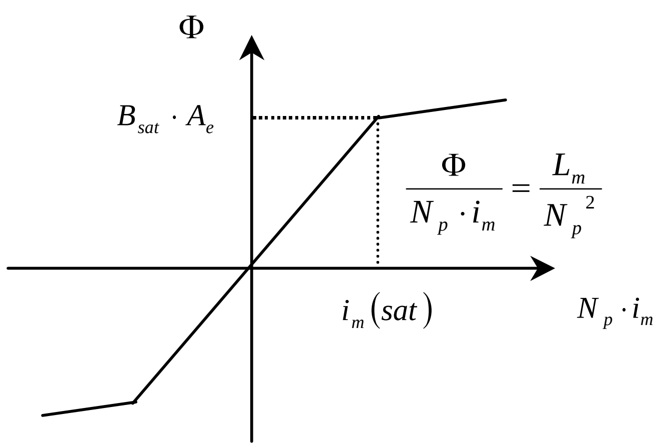


Fig. 6.21. Relation of saturation flux to the saturation magnetizing current.

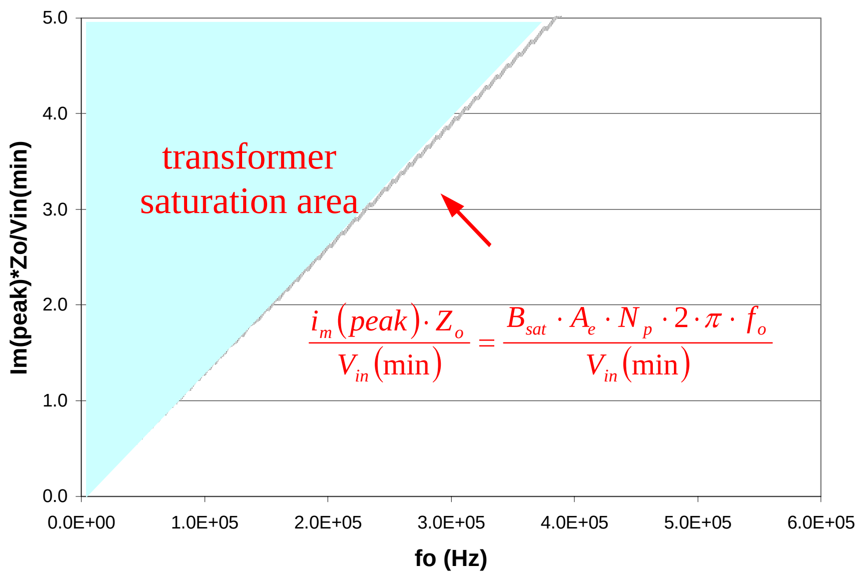


Fig. 6.22 Transformer saturation area.

6.4.3.4 Design constraint 4: diode reverse recovery problem

$$i_m(peak) < i_m(ripple) \tag{6.56}$$

where,

$$i_m(ripple) = \frac{V_{in}\cdot D\cdot T_s}{L_m} = \frac{n\cdot V_o\cdot T_s}{L_m} \tag{6.57}$$

Similar to peak magnetizing current, the ripple current can be written as:

$$\frac{i_m(ripple)\cdot Z_o}{V_{in}(\min)} = \frac{n\cdot V_o\cdot 2\cdot\pi\cdot f_o}{f_s\cdot V_{in}(\min)} \tag{6.58}$$

The diode reverse recovery problem area is shown as in Fig. 6.23. It is a straight line in the normalized design curve.

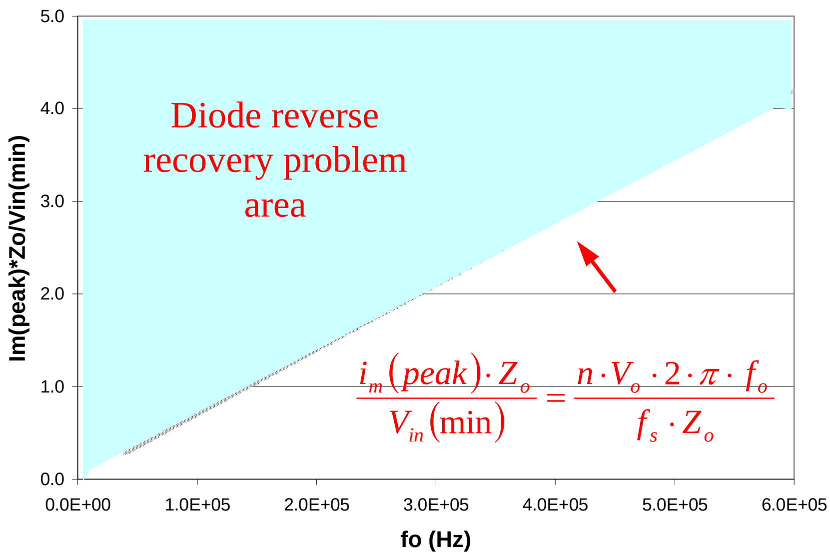
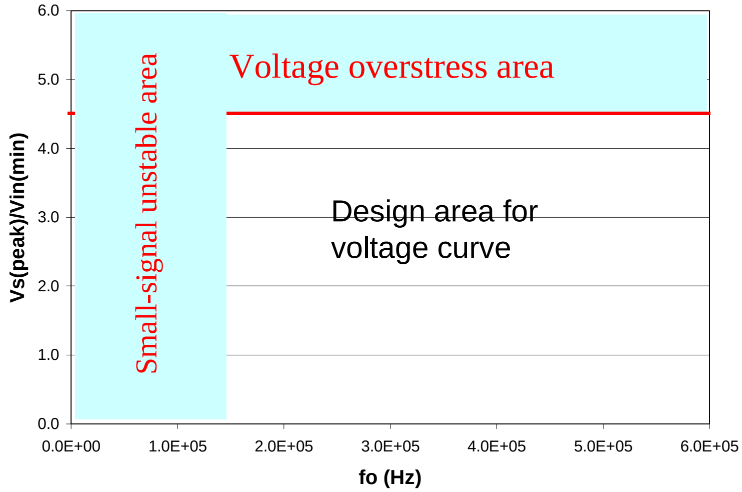


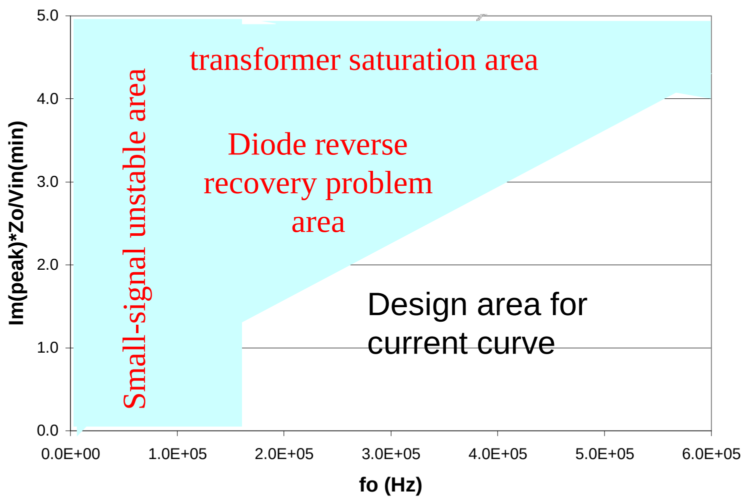
Fig. 6.23. The diode reverse recovery problem area.

6.4.3.5 *Feasible operating regions for the switch voltage and magnetizing current*

According to four design constraints, we can draw the feasible operating regions for voltage and magnetizing current as shown in Fig. 6.24.



(a)



(b)

Fig. 6.24 Feasible operating regions for voltage and magnetizing current. (a) design area for normalized switch voltage curve. (b) design area for normalized magnetizing current curve.

6.4.4 Generating design curves

For the fixed control bandwidth and maximum duty cycle limit, we can generate a set of design curves of the maximum peak voltage and magnetizing current by varying parameters L_m and C_c. Since line transient is not a problem in current mode control, we will generate design curves according to the worst conditions in load transient. From previous analysis, we know that the worst case happens at low line and load from low to high transient. In this example, Vin is 36 V, and Io changes from 0 A to 30 A.

A set of design curves is generated by varying L_m and C_c values with a fixed control bandwidth, 14 kHz, and maximum duty cycle limit, 0.75. Each single simulation generates one point in the voltage design curve and one point in the magnetizing current curve. The normalized design curve for peak voltage and magnetizing current are shown in Fig. 6.25 and Fig. 6.26, respectively. There are 7 simulation points (with different C_c values) for each Lm and the total number of simulations to generate a set of curves in Fig. 6.25 and Fig. 6.26 are 35. The total simulation CPU time is only 9 minutes by using proposed simulation and modeling approach.

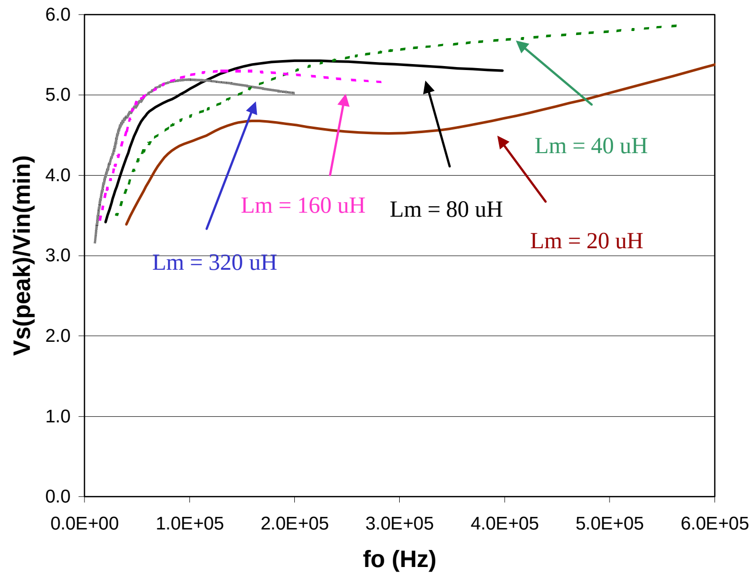


Fig. 6.25 Normalized peak switch voltage vs. f_o curve.

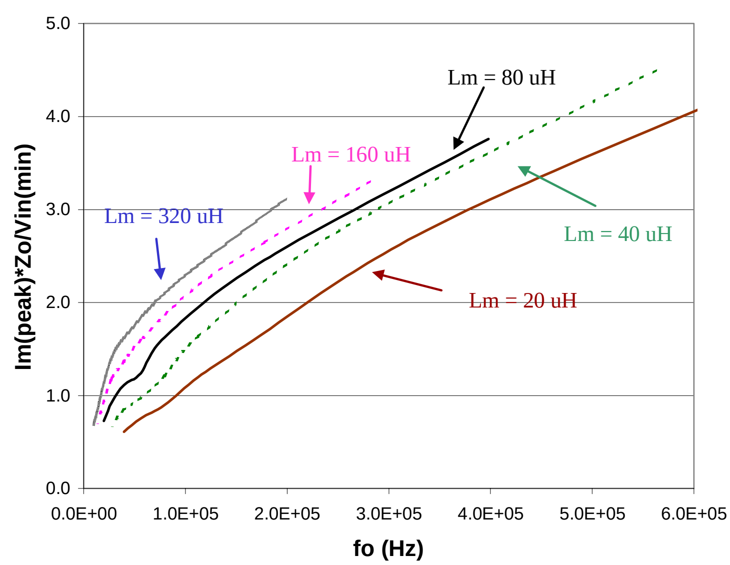


Fig. 6.26 Normalized peak magnetizing current vs. f_o curve.

6.4.5 Determine the feasible Lm and Cc to meet the design constraints

After we generate the design curves with design constraints, the feasible L_m and C_c to meet all the design criteria can be easily determined. We will use the main converter in the power supply system discussed in the chapter 4 as an example to demonstrate how to use design curves to redesign the active-clamp circuit parameters and solve the previous design problems.

Assuming the device rating of the main switch is 180 V, so the normalized boundary of the voltage stress is 5 when V_{in}(min) = 36 V. When the control bandwidth, f_c = 14 kHz, and maximum duty cycle limit, d_{lim} = 0.75, the boundary of the resonant frequency for small-signal stability is 112 kHz. The feasible L_m and C_c can be determined by three steps.

1. Find the desired parameter ranges for f_o and L_m in peak-voltage design curves.

Fig. 6.27 is the peak-voltage design curves with f_c 14 kHz and d_{lim} 0.75. These is a big dot in Fig. 6.27, which corresponds to the original design, L_m = 80 uH and C_c = 0.01 uF. The maximum voltage is about 200 V, which exceeds the 180 V voltage rating of the switch.

The dotted lines covered area is the desired design area to meet voltage stress limitation and small signal stable criterion in the normalized peak switch voltage vs. f_o curves. We can see that only the curve at L_m = 20 uH meets the constraints when f_o is at 112 kHz to 480 k Hz range.

2. Within the defined ranges for f_o and L_m in step 1, we can find the desired ranges for f_o and L_m that also meet the magnetizing current constraints.

Fig. 6.28 is the peak magnetizing-current design curves with f_c 14 kHz and d_{lim} 0.75. These is a big dot in Fig. 6.28, which corresponds to the original design, L_m = 80 uH and C_c = 0.01 uF. It shows that the original design has diode reverse recovery problem and is at the boundary of the transformer saturation.

Fig. 6.28 shows that there are no feasible parameters available within the desired areas from step1. It also means that there is no feasible L_m and C_c can meet all the design constraints in the previous circuit condition.

We need to change the design parameters and repeat the design iterations. There are several ways to do it (e.g. loosing design constraints, changing control bandwidth or maximum duty cycle limit) and these approaches will be discussed in the next section: design trade off.

3. If we find the desired ranges for f_o and L_m from step 1 and 2, C_c can be calculated by

$$C_c = \frac{1}{(2 \cdot \pi \cdot f_o)^2 \cdot L_m} \tag{6.59}$$

Within the desired parameter range, a smaller f_o, thus a smaller C_c usually is preferred to reduce the voltage and current stresses.

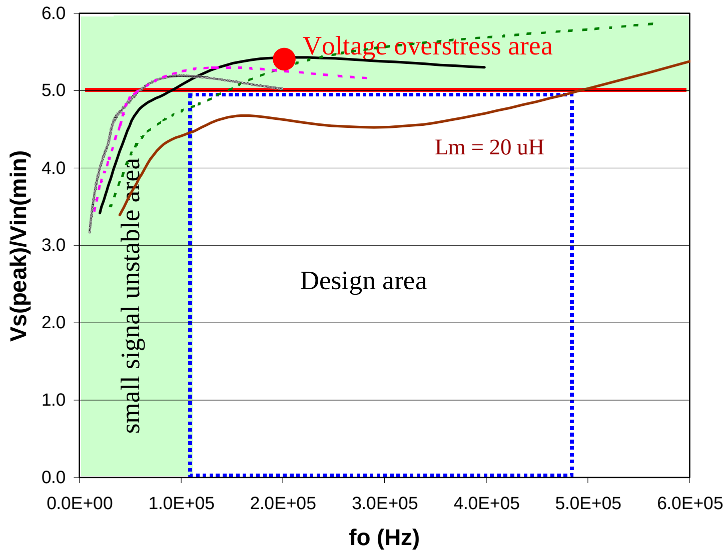


Fig. 6.27 The dotted lines cover the desired design area to meet voltage stress limitation and small signal stable criterion in the normalized peak switch voltage vs. f_o curves.

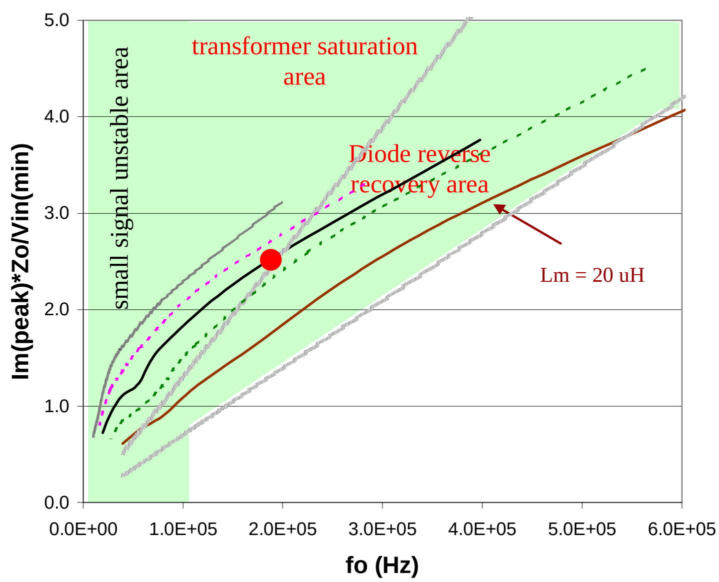


Fig. 6.28 Find design area to meet transformer criteria in normalized peak magnetizing current vs. f_o curve.

6.4.6 Design trade-off

If there is no adequate parameters of L_m and C_c that can meet all the design criteria, the other design parameters have to be changed. After changing circuit parameter values, we can repeat the design iterations from step 1 to 3.

Previous example shows that there is no adequate L_m and C_c to meet all the design criteria. There are several design trade-off to solve the problem.

Design trade-off 1: increasing device rating.

From Fig. 6.27 and Fig. 6.28, we see that if we do not restrict the device voltage rating, there is a small area in Fig. 6.28 which can meet all the design criteria. The design result will be L_m = 20 uH and C_c smaller than 6 nF. The additional disadvantage is the high ripple current of the magnetizing current due to a small L_m.

It is worthwhile to mention that a too small magnetizing inductance could have a very high ripple of the magnetizing current which will increase the loss of the circuit and may affect the main converter operation if the ripple of the magnetizing current is not negligible to the reflected load.

Fig. 6.29 shows load transient waveforms with original circuit design at Vin = 36 V, load step change from 0 to 30 A. The circuit parameters are L_m = 80 uH, C_c = 0.01 uF, f_c = 14 kHz, and d_{lim} = 0.75. The peak voltage value is 195 V and there is diode recovery problem during the transient.

Fig. 6.30 shows load transient waveforms with magnetizing inductance reduced from 80 uH to 20 uH at the same transient condition. The peak voltage value is still high, but there is no diode recovery problem during the transient. The ripple magnetizing current is very high in the circuit.

Dlim = 0.75, Fc = 14 kHz Lm = 80 uH, Vs = 195 V

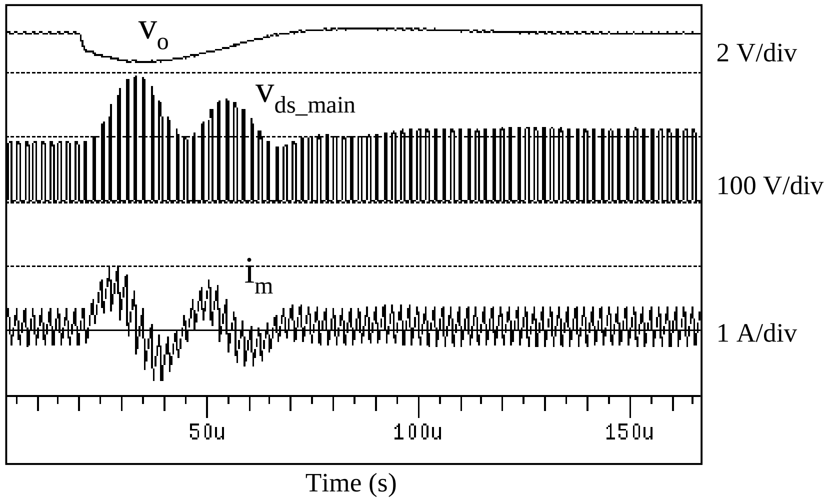


Fig. 6.29. Load transient waveforms with original circuit design at V_{in} = 36 V, load step change from 0 to 30 A.

Dlim = 0.75, Fc = 14 kHz, Lm = 20 uH, Vs = 191 V

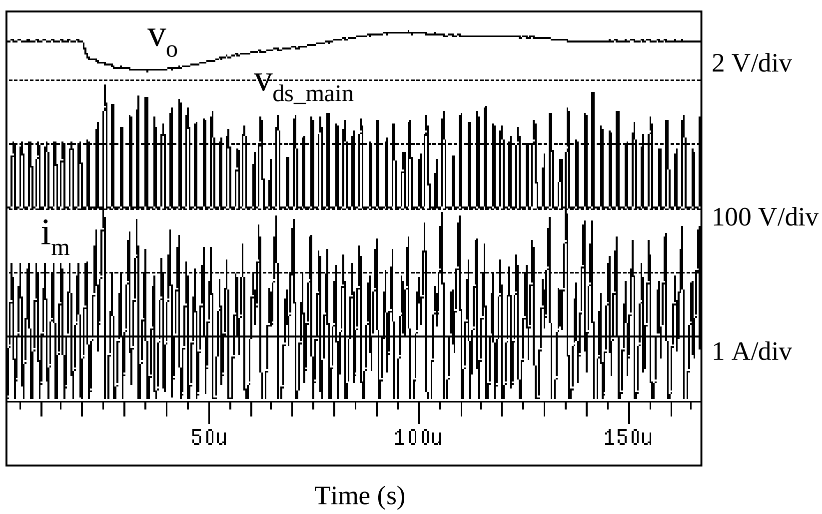


Fig. 6.30. Load transient waveforms with reduced magnetizing inductance L_m = 20 uH at V_{in} = 36 V, load step change from 0 to 30 A.

Design trade-off 2: getting rid of the constraint of the body diode reverse recovery.

From Fig. 6.28, we see that the diode reverse recover constraint is the hardest one to meet in the parameter design. The design is much easier to meet other criteria without this constraint. This can be done by connecting a Schottky diode in series with the auxiliary switch to block the conduction of the body diode, and then to connect a fast-recovery anti-parallel diode around the series connection of the Schottky and the auxiliary switch [56]. The disadvantage is the additional components to increase the cost of the circuit.

Design trade-off 3: decreasing control bandwidth.

From previous analysis, we know that a smaller bandwidth can reduce the peak voltage and current during load transients. The disadvantage is a slower recovery from transient in the output voltage of the main converter.

Fig. 6.31 and Fig. 6.32 shows the normalized voltage and magnetizing current design curves with reduced control bandwidth. The f_c is reduced from 14 kHz to 8 kHz. The design result is L_m = 40 uH, C_c is less than 0.013 uF. In the figure, it shows that a smaller C_c, thus a larger f_o, has a larger voltage stress but less current stress and more design margin without saturation and diode reverse recovery problem.

Fig. 6.33 shows load transient waveforms with bandwidth reduced from 14 kHz to 8.2 kHz, and magnetizing inductance reduced from 80 uH to 40 uH at the same transient condition. The peak voltage value is reduced from 195 V to 153 V, and there is no diode recovery problem during the transient. However, the output voltage transient response is little bit slower than the original design.

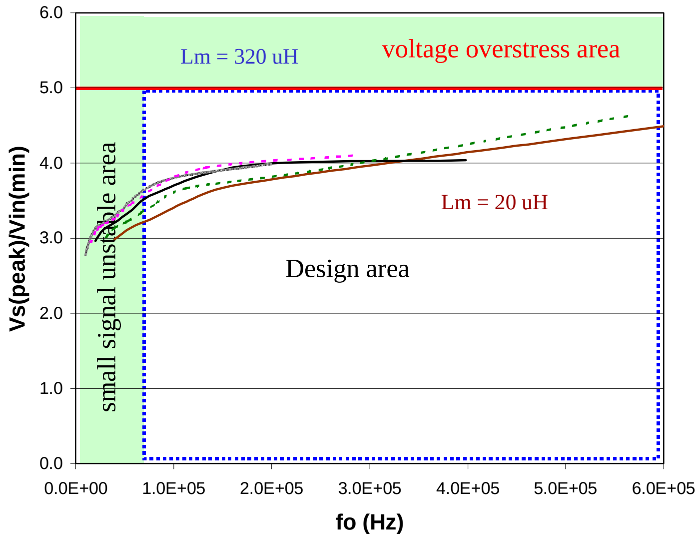


Fig. 6.31 Normalized voltage design curve with reduced control bandwidth. The f_c is reduced from 14 kHz to 8 kHz. The design area to meet voltage stress limitation and small signal stable criteria is shown in the dotted line.

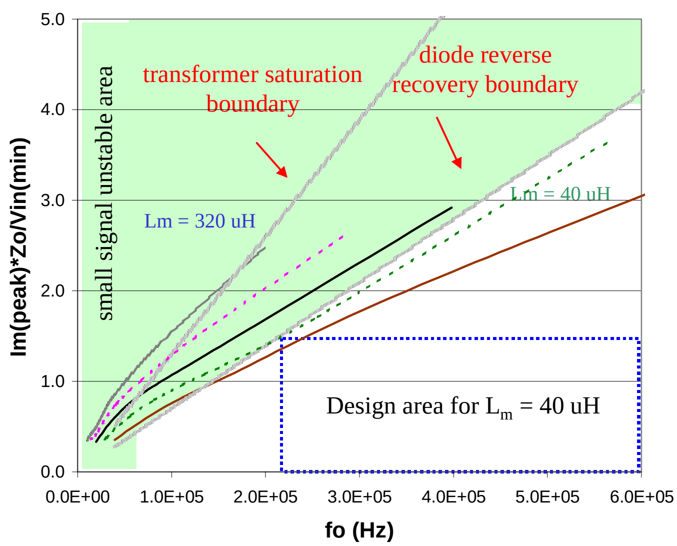


Fig. 6.32 Normalized magnetizing current design curve with reduced control bandwidth. The f_c is reduced from 14 kHz to 8 kHz. The design area without transformer saturation and diode reverse recovery problem shows in the dotted area.

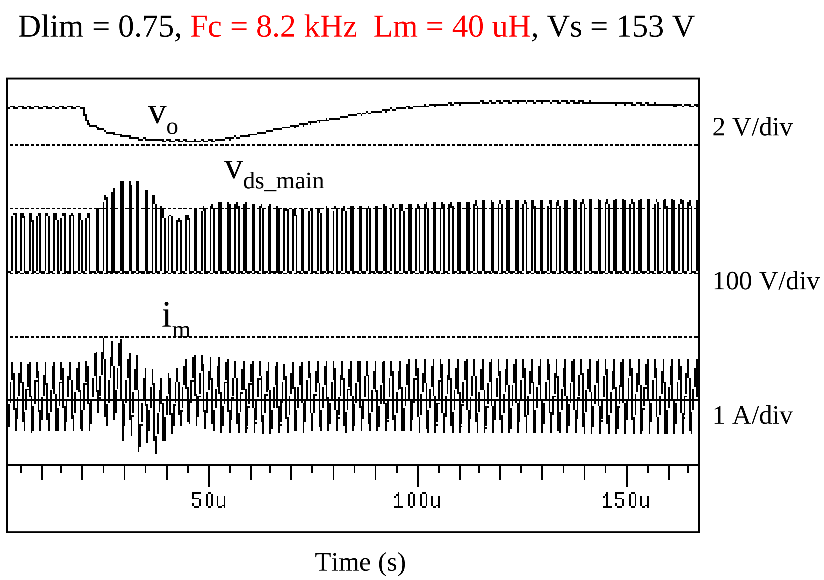


Fig. 6.33. Load transient waveforms with reduced bandwidth f_c = 8.2 kHz at V_{in} = 36 V, load step change from 0 to 30 A.

Design trade-off 4: reducing maximum duty cycle limit value.

The voltage and current stresses can also be reduced by reducing the maximum duty cycle limit value. Similar to solution 3, the disadvantage is a slower recovery from transient in the output voltage of the main converter.

Fig. 6.34 and Fig. 6.35 shows the normalized voltage design curve with reduced maximum duty cycle limit. The maximum duty cycle limit is reduced from 0.75 to 0.7. The design result is L_m = 40 uH, C_c is less than 0.011 uF. Similar to the precious case, a smaller C_c has a larger voltage stress, but less current stress and more design margin without saturation and diode reverse recovery problem.

Fig. 6.33 shows load transient waveforms with maximum duty cycle limit reduced from 0.75 to 0.7, and the magnetizing inductance reduced from 80 uH to 40 uH at the same transient condition. The peak voltage value is reduced from 195 V to 141 V, and there is no diode recovery problem during the transient.

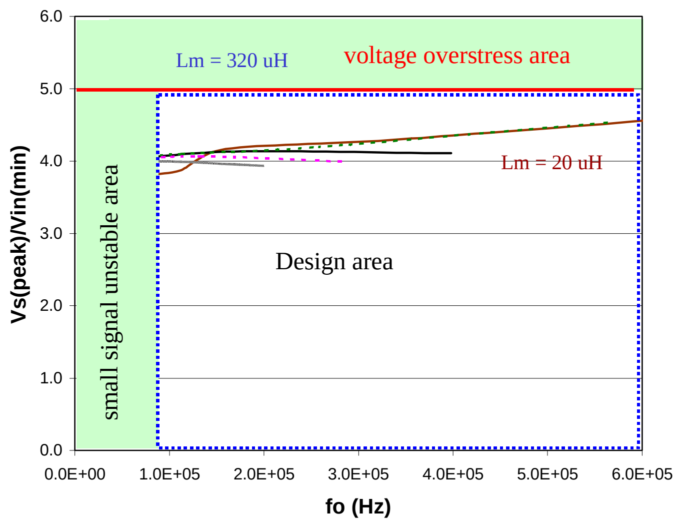


Fig. 6.34 Normalized voltage design curve reduced maximum duty cycle limit. The Dlim is reduced from 0.75 to 0.7. The design area to meet voltage stress limitation and small signal stable criteria is shown in the dotted area.

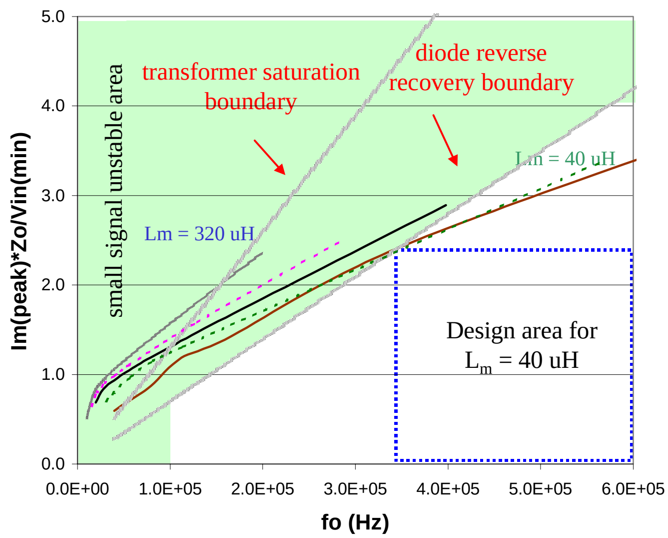


Fig. 6.35 Normalized magnetizing current design curve with reduced maximum duty cycle limit. The Dlim is reduced from 0.75 to 0.7. The design area without transformer saturation and diode reverse recovery problem shows in the dotted line.

Dlim = 0.7, Fc = 14 kHz Lm = 40 uH, Vs = 141 V

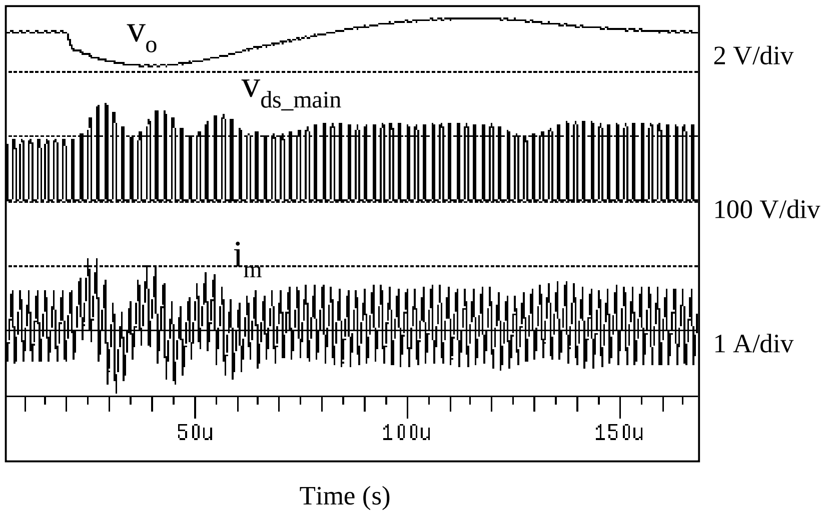


Fig. 6.36. Load transient waveforms with reduced maximum duty cycle limit d_{lim} = 0.7 at V_{in} = 36 V, load step change from 0 to 30 A.

6.5 Validation of the design by virtual prototype test

Virtual prototype DVT process is repeated after the circuit design modification. The following are comparisons between the original circuit problems and the circuit behavior after the design modification. The circuit parameters are modified by reducing the maximum duty cycle limit from 0.75 to 0.7 and magnetizing inductance from 80 uH to 40 uH. The clamp capacitance is 0.01 uF.

6.5.1 DC performance

Fig. 6.37 shows design verification of dc bias of magnetizing current of transformer. The dc bias of the magnetizing current does not shown any problems since the magnetizing current ripple is about 800 mA .

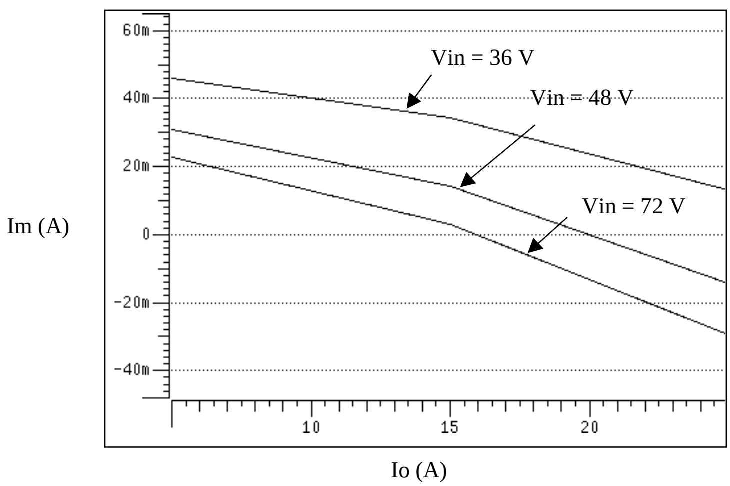


Fig. 6.37. Design verification of dc bias of magnetizing current of transformer at steady state.

6.5.2 Small signal performance

Fig. 6.38 shows the design verification of the small signal analysis at worst case condition. The resonant frequency of the active-clamp circuit has been pushed far enough and does not interfere with the crossover frequency of the loop gain.

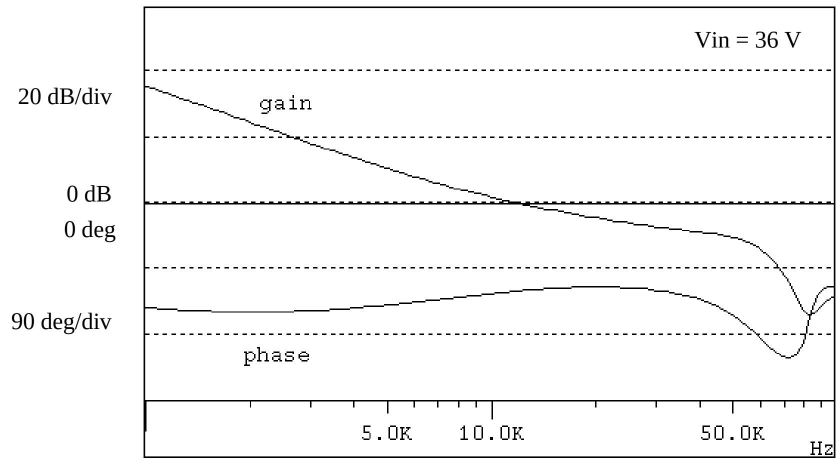
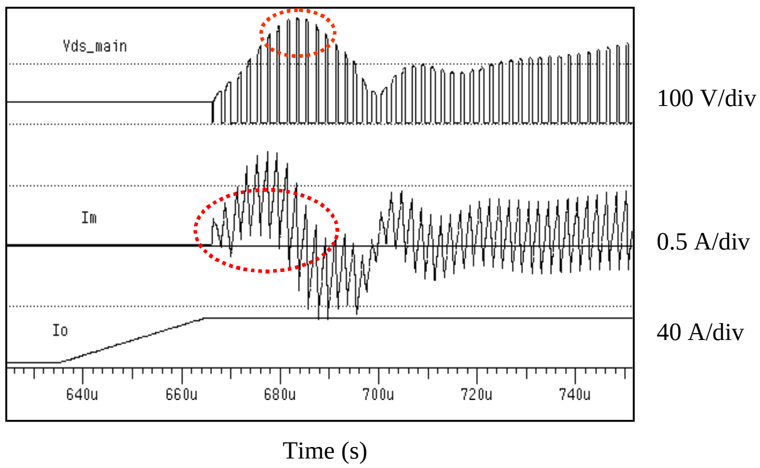


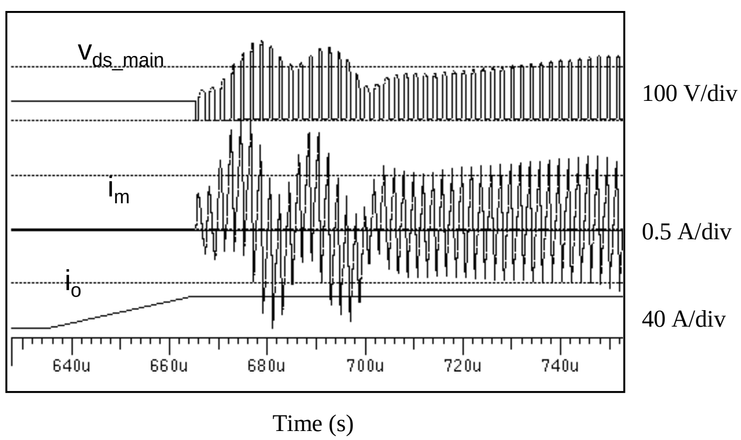
Fig. 6.38 Design verification of the small signal analysis.

6.5.3 Large-signal transient

Fig. 6.39 shows the design verification of the large-signal transient analysis with worst case: Vin = 36 V, Io = 0 to 30 A. Fig. 6.39(a) shows the waveforms with original design. Fig. 6.39(b) shows the waveforms after design modification. The original circuit problems during large-signal transient are solved.



(a)

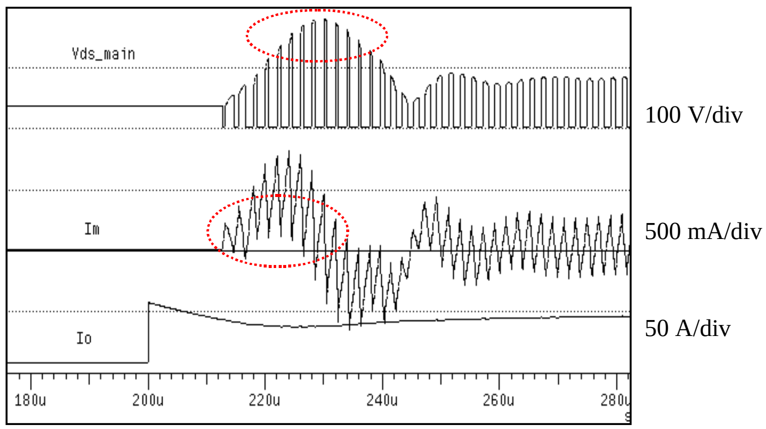


(b)

Fig. 6.39 Design verification of the large-signal transient analysis with worst case: Vin = 36 V, Io = 0 to 30 A. (a) waveforms with original design. (b) waveforms after design modification.

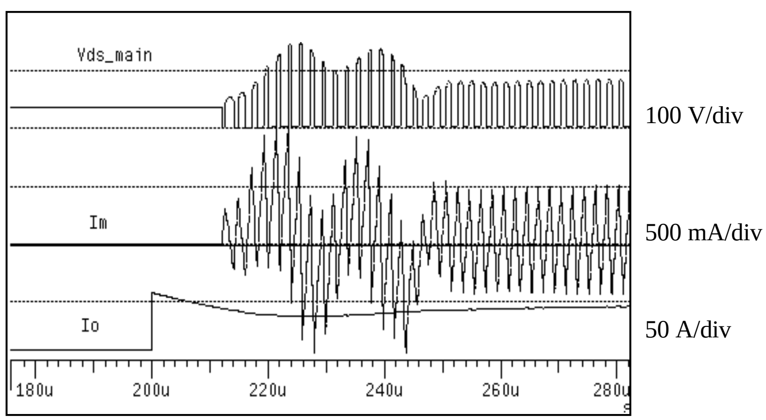
6.5.4 Abnormal conditions

Fig. 6.40 shows the design verification of the short circuit test: Vin = 36 V, Io = 0 A. Fig. 6.40(a) is the waveforms with original design. Fig. 6.40(b) is the waveforms after design modification. The original circuit problems during abnormal conditions are solved.



Time (s)

(a)



Time (s)

(b)

Fig. 6.40 Design verification of the short circuit test: Vin = 36 V, Io = 0 A. (a) waveforms with original design. (b) waveforms after design modification.

6.6 Summary

The dynamic responses of the active-clamp forward converter circuit with peak current mode control under line and load transients are discussed. A design procedure is provided to solve these design issues. The circuit performances of the power supply system design are improved by redesign the active-clamp reset circuit. The virtual prototype DVT is processed to verify the design. It is the first time that with the aid of the virtual prototype, we are able to optimize the circuit design of the active-clamp forward converter for large-signal transient behaviors.

7. CONCLUSIONS

Today's design and test procedure of a complex power supply system is very expensive and time consuming because the designers must rely very heavily on hardware breadboards and prototypes to do the vast majority of their design and concept verification. A virtual prototype that implemented by simulation software is implemented in this dissertation, so that a set of systematic simulation tests can be added before the first hardware prototyping to verify the design concepts and uncover most of the potential design deficiencies. By detecting most of the errors before the hardware test, this virtual prototype DVT procedure can reduce design iterations significantly. Consequently, it can shorten product time to market and reduce design errors and the resulting costs of delays, changes, rework, and other quality problems.

This dissertation implements the virtual prototype by developing simulation methodology for a practical power supply system. A multi-level modeling and multi-level simulation methodology is proposed and verified by detailed simulations for a forward-converter power supply system. The multilevel modeling and simulation approach focuses on selecting the appropriate level of device models and function blocks for each specific objective, therefore, the shortest simulation CPU time can be achieved while still simulating the system behavior accurately.

The multi-level modeling and simulation methodology in virtual prototype test procedure is composed of four parts: circuit partition, multi-level modeling, hierarchical test sequence, and multi-level simulation. By applying multi-level modeling and simulation methodology in virtual prototype test, the simulation time and accuracy are improved significantly. It shows that for a practical 5 V forward converter power supply system, it took less than 8 hours to finish about 800 tests for a complete virtual prototype test. The virtual prototype DVT procedure covers different system tests that include the basic function test, steady stage analysis, small-signal stability analysis, large-signal transient analysis, subsystem interaction test, and system interaction test.

The dissertation also demonstrates how to debug and solve the circuit design problems by the aid of virtual prototype. The anomalies of the active-clamp forward converter are well known for a decade, but there is no effective way to analyze and predict these problems so far. The problems related to the large-signal transients of the circuit are very hard to be considered in a design procedure. The analysis and design of the active-clamp reset circuit with considering the dynamic performances show great challenge because of the non-linearity of system behavior.

With the help of the virtual prototype, it is the first time that we are able to analyze the dynamic behavior of the active-clamp forward converter and provide a design optimization procedure to obviate these circuit problems. The average-state-trajectory approach is proposed in the dissertation and verified by circuit measurements. It shows the proposed state-trajectory approach can predict the dynamic behavior of the reset circuit in both voltage feedback control and current mode control circuits during input voltage and load transients.

A design procedure for active-clamp reset circuit is proposed by using computer generated design curves. Finally, the 5 V power supply system is verified by repeating the virtual prototype DVT test with the new design parameters. It shows that the problems related to active-clamp circuit are solved by using this proposed design procedure.

This dissertation focuses on verifying the circuit performance at a nominal condition, i.e., at a specific temperature with nominal component values. Due to the fast simulation speed of the virtual prototype DVT, this methodology can be applied to a system that requires more simulation tasks (e.g. simulation with different temperatures, tolerance analysis).

The proposed modeling and simulation methodology is to set a guideline or a frame for the virtual prototype test. The complexity levels of models and simulation schematics are flexible in terms of capable to vary for different applications or different preferences of designers. Since most of the models, test sequences, the levels of simulations are very general and can be used for different power supply systems, it is very easy for other people to justify his own model levels and test sequences according to different applications and preferences. The best way to implement the virtual prototype DVT is to use an automation test system, so that all the tests can be fulfilled and the circuit problems can be recorded in an automated simulation runs.

Appendix A Dynamic Library Work Sheet Example (Mathcad file)

General approach for creating rectifier diode model

Principle:

1. Select leakage current at 125 C
2. Select forward voltage drop at 125 C
3. Assume two segment model. When V = 0V, I = 0A
3. Need three points in data sheet to generate model. Proposed point
   leakage current at 75% break down voltage
   forward voltage at 1A
   forward voltage at maximum or full load
4. Adjust parameter values If there are n diodes in parallel.

Define units:

$uA \equiv 10^{-6} \cdot A$

$nC \equiv 10^{-9} \cdot C$

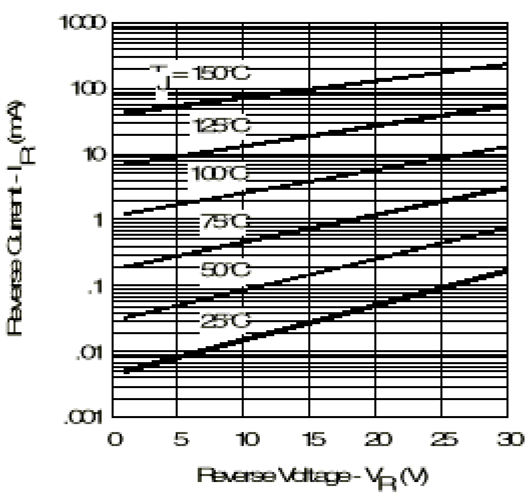
Example: 32CTQ030 rectifier

Major characteristics of 32CTQ030 rectifier:

From data sheet:

Major Ratings and Characteristics

Characteristics	32CTQ030	Units
$I_{F(AV)}$ Rectangular waveform	30	A
V_{RRM}	30	V
I_{FSM} @ tp = 5 μs sine	900	A
V_F @ 15 Apk, T_J = 125°C (per leg)	0.40	V
T_J	-55 to 150	°C



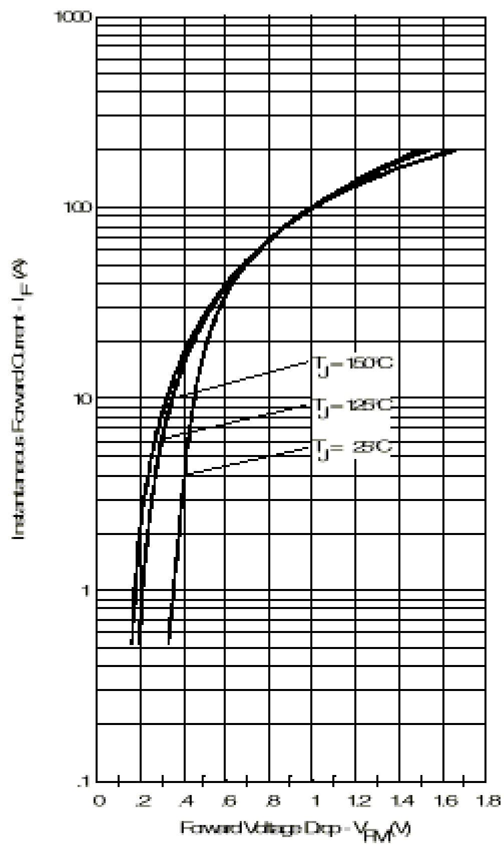
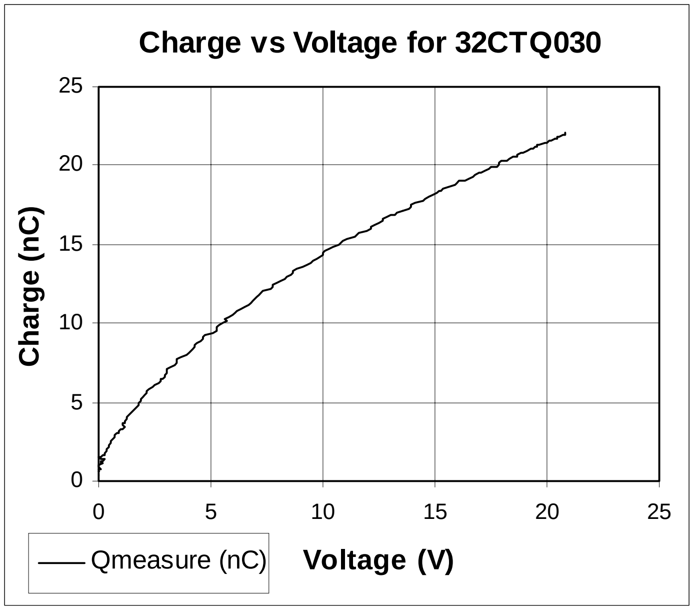


Fig. 1 - Max. Forward Voltage Drop Characteristics

From measurement:



Circuit specification: maximum current 50 A three rectifier in parallel

$Imax := 50 \cdot A$

$n := 3$

Calculate diode parameters:

1. Select three points in forward current vs. forward voltage fro data sheet:

Break down voltage is 30 V, leakage current at 75% break down voltage is 35 mA in data sheet:

$Vb := 30 \cdot V$

$Vr := -0.75 \cdot Vb \qquad Vr = -22.5 \, V$

$Ir := -15 \cdot mA$

Maximum forward current in each rectifier:

$$If\_max := \frac{50 \cdot A}{n} \qquad If\_max = 16.667 \, A$$

Get forward voltage drop at 1 A and 17 A from data sheet:

$$Vf1 := 0.2 \cdot V \qquad If1 := 1 \cdot A$$

$$Vf2 := 0.42 \cdot V \qquad If2 := 17 \cdot A$$

2. Calculate turn on and off resistances:

$$Roff := \frac{Vr}{Ir} \qquad Roff = 1.5 \cdot 10^{3} \; \circ ohm$$

$$Ron := \frac{Vf2 - Vf1}{If2 - If1} \qquad Ron = 0.014 \circ ohm$$

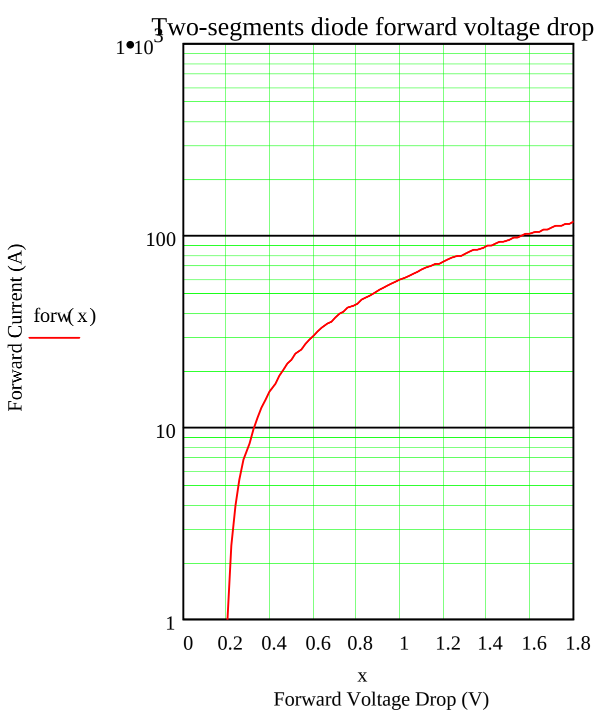
3. Calculate intersection of two segments:

$$leak(x) := \frac{x}{Roff}$$

$$forw(x) := \frac{x - Vf1}{Ron} + If1$$

4. Verification (model valid for If < 17 A):

$$x := 0 \cdot V, 0.02 \cdot V .. 2 \cdot V$$



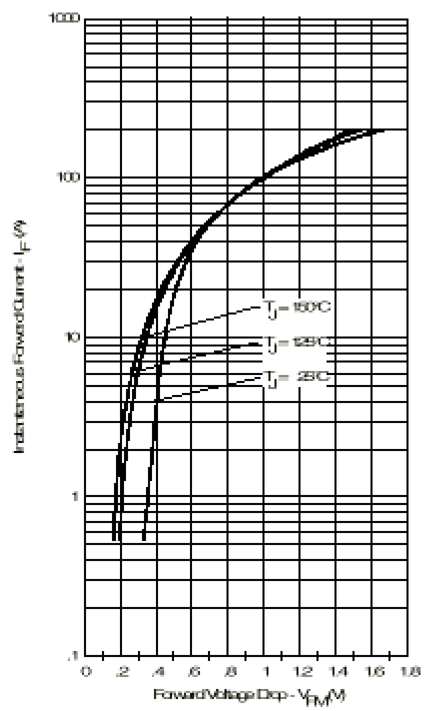
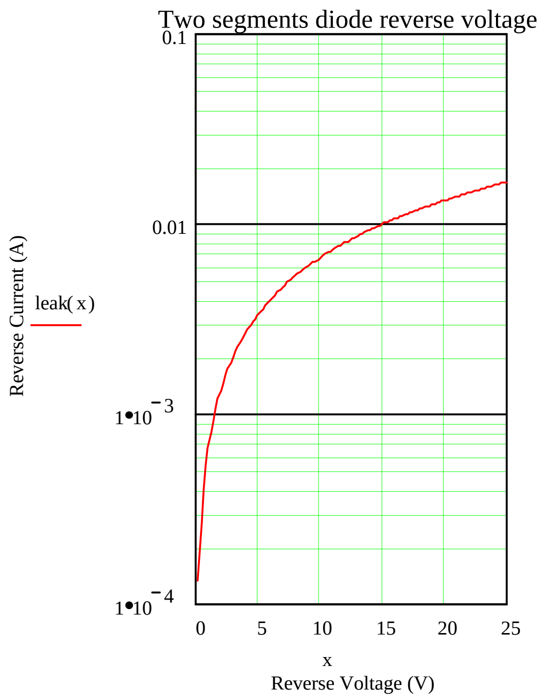
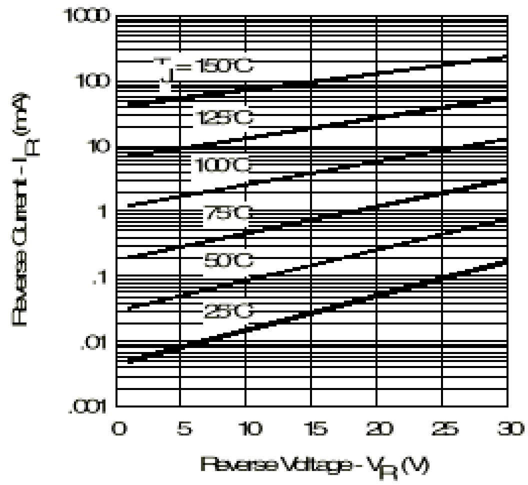


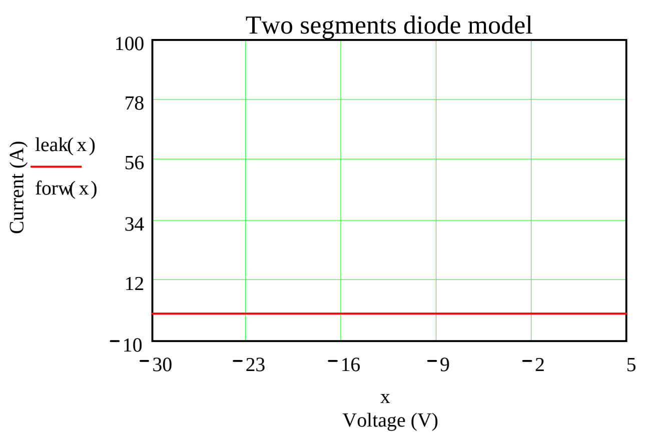
Fig. 1 - Max. Forward Voltage Drop Characteristics

$x := 0 \cdot V, 0.2 \cdot V .. 25 \cdot V$





$x := -30 \cdot V .. 5 \cdot V$



Find knee forward voltage:

Knee voltage initial guess: $x := 0.3 \cdot V$

Given

$leak(x) = forw(x)$

$Vknee := find(x)$ $\qquad Vknee = 0.186 \cdot V$

$Iknee := forw(Vknee)$ $\qquad Iknee = 1.242 \cdot 10^{-4} \cdot A$

Calculate charge parameters:

1. Select three points of charge vs. reverse voltage from measureme

$Vq0 := 0 \cdot V \qquad Q0 := 0 \cdot C$

$Vq1 := 5 \cdot V \qquad Q1 := 10.5 \cdot nC$

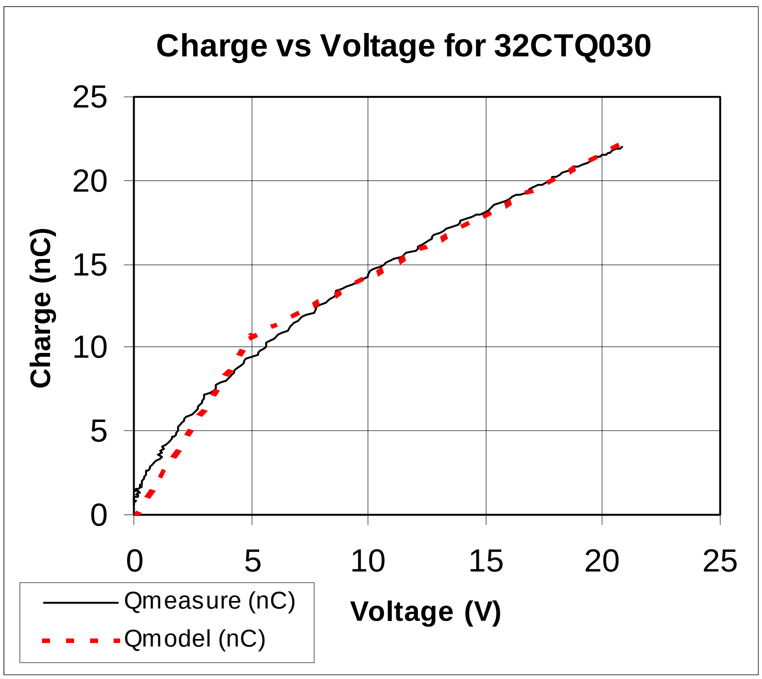
$Vq2 := 21 \cdot V \qquad Q2 := 22.4 \cdot nC$

2. Calculate two-segment capacitor values:

$$C1 := \frac{Q1 - Q0}{Vq1 - Vq0} \qquad C1 = 2.1 \cdot 10^{-9} \; \cdot F$$

$$C2 := \frac{Q2 - Q1}{Vq2 - Vq1} \qquad C2 = 7.437 \cdot 10^{-10} \; \cdot F$$

3. Verification:



Summary of rectifier model (three paralleled) parameters:

Level 1:

Piecewise linear resistor parameters:

$V0\_n := Vr$	$I0\_n := n \cdot Ir$
$V1\_n := n \cdot Vknee$	$I1\_n := n \cdot Iknee$
$V2\_n := n \cdot Vf1$	$I2\_n := n \cdot If1$
$V0\_n = -22.5 \cdot V$	$I0\_n = -0.045 \cdot A$
$V1\_n = 0.559 \cdot V$	$I1\_n = 3.725 \cdot 10^{-4} \cdot A$
$V2\_n = 0.6 \cdot V$	$I2\_n = 3 \cdot A$

Level 2:

Piecewise linear capacitor parameters (in addition to piecewise linear resistor in level 1):

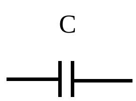
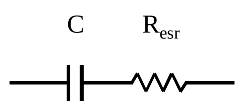
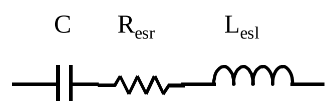
$Vq0\_n := Vq0$	$Q0\_n := n \cdot Q0$
$Vq1\_n := Vq1$	$Q1\_n := n \cdot Q1$
$Vq2\_n := Vq2$	$Q2\_n := n \cdot Q2$
$Vq0\_n = \cdot V$	$Q0\_n = \cdot nC$
$Vq1\_n = \cdot V$	$Q1\_n = \cdot nC$
$Vq2\_n = \cdot V$	$Q2\_n = \cdot nC$

Appendix B Device Model Library

B.1. Passive components

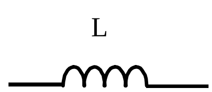
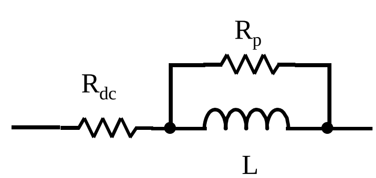
Capacitor

C: capacitance; R_{esr}: ESR; L_{esl}: ESL

		
M1	**M2**	**M3**

Inductor

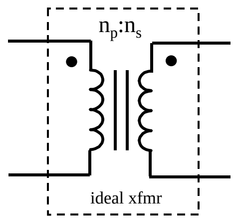
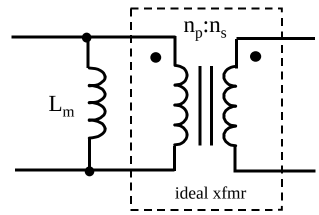
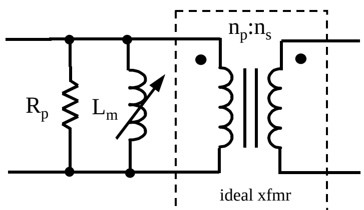
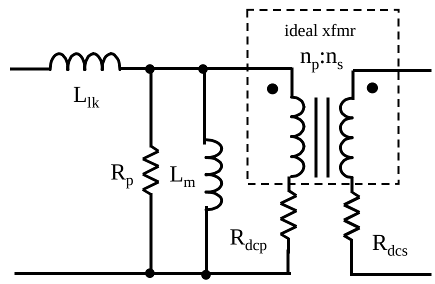
L: inductance; R_{dc}: winding dc resistance; R_p: core loss resistance.

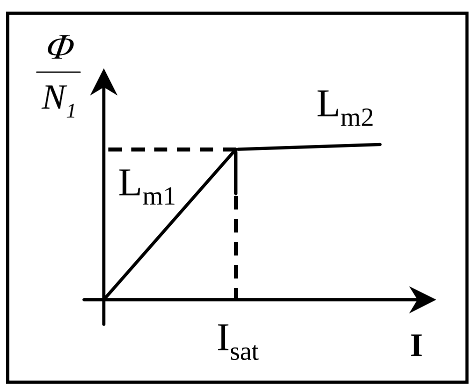
	
M1	**M2**

Transformer

L_m: magnetizing inductance; L_{lk}: leakage inductance

R_{dcp}, R_{dcs}: winding dc resistance; R_p: core loss resistance

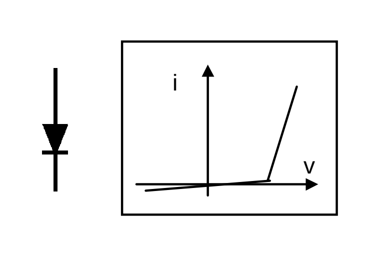
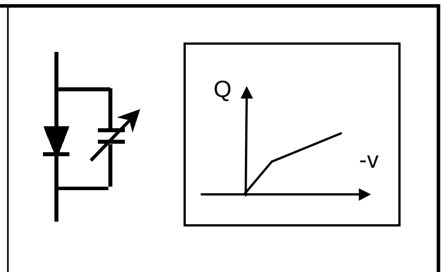
	
M1	**M2**
	
M3	**M4**



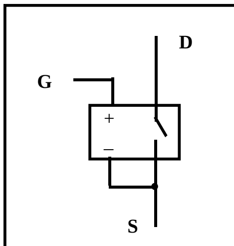
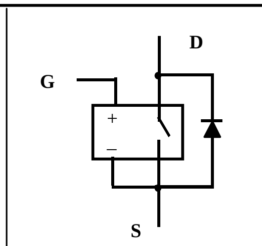
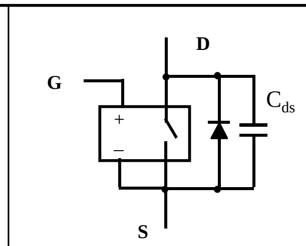
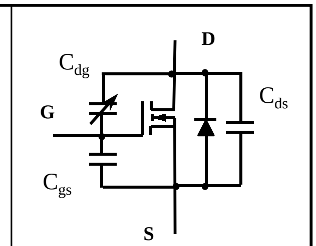
L_m characteristics in M3 of transforer

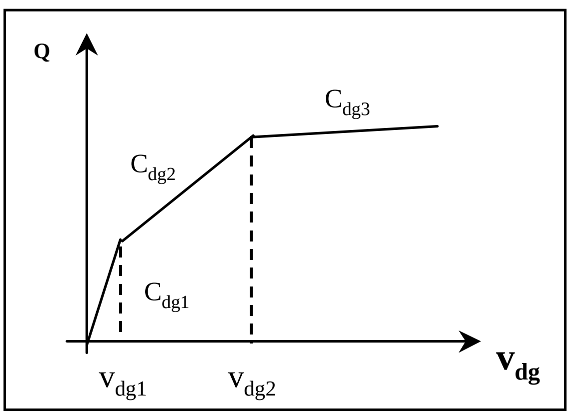
B.2. Semiconductor devices

Diode

	
M1	**M2**

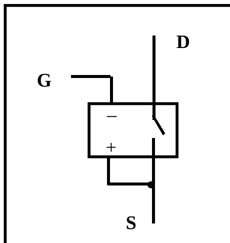
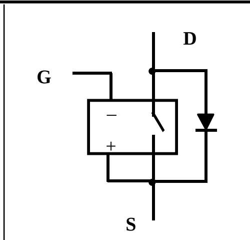
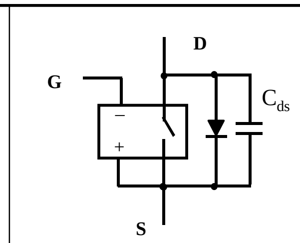
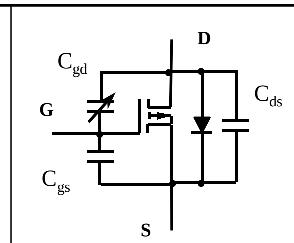
N MOSFET

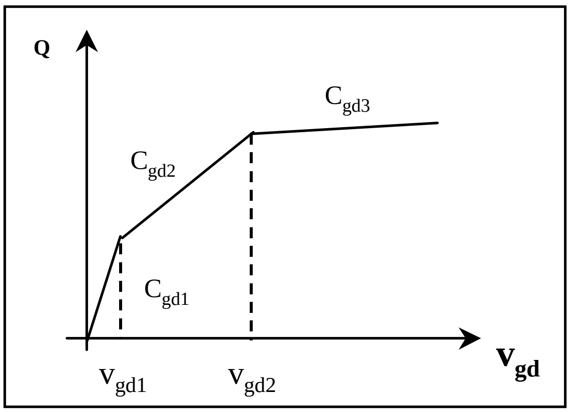
			
M1	**M2**	**M3**	**M4**



C_{dg} characteristics in M4 of N MOSFET

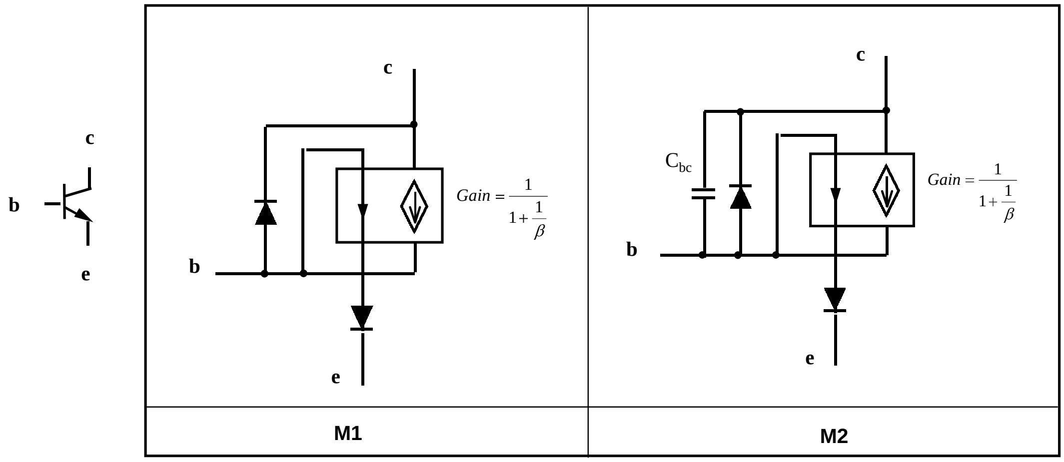
P MOSFET

			
M1	**M2**	**M3**	**M4**

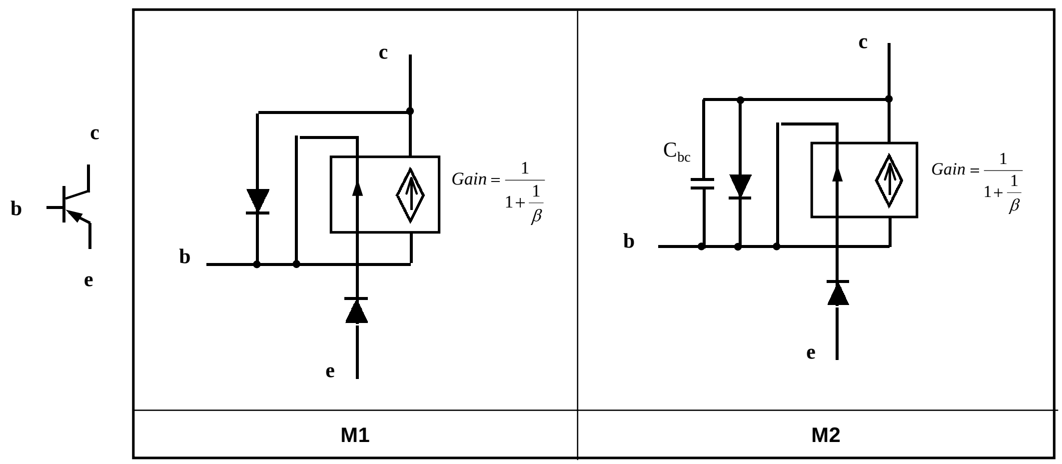


C_{gd} characteristics in M4 of P MOSFET

NPN bipolar transistor



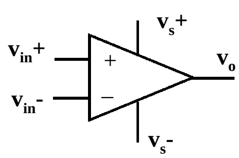
PNP bipolar transistor

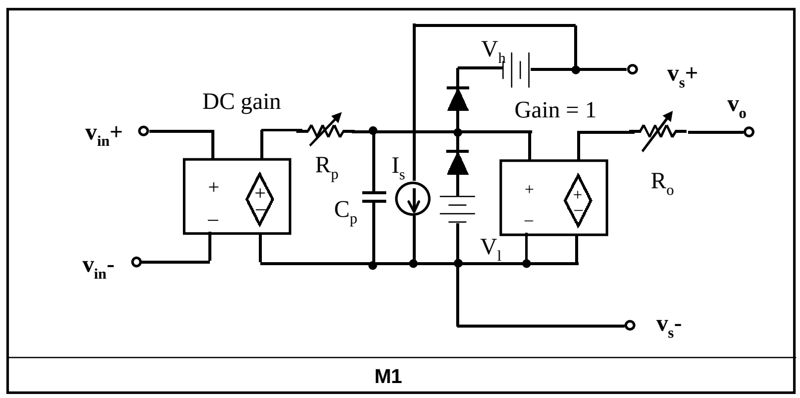


B.3. IC chips

Operational amplifier

R_{in}: input resistance
R_o: output resistance
R_p, C_p: low frequence pole
V_h: maximum output voltage limiter
V_l: minimum output voltage limiter
I_s: static power supply current



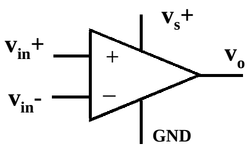


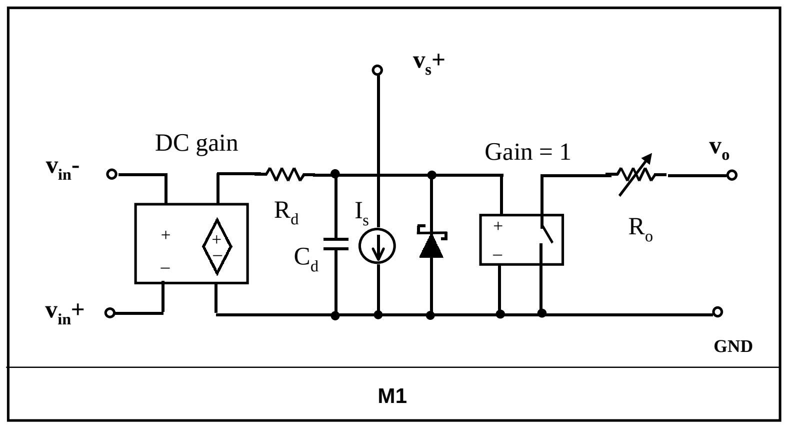
Comparator

R_o: output resistance

R_d, C_d: delay time constant

I_s: static power supply current

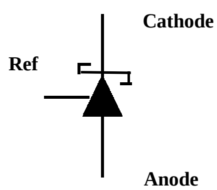


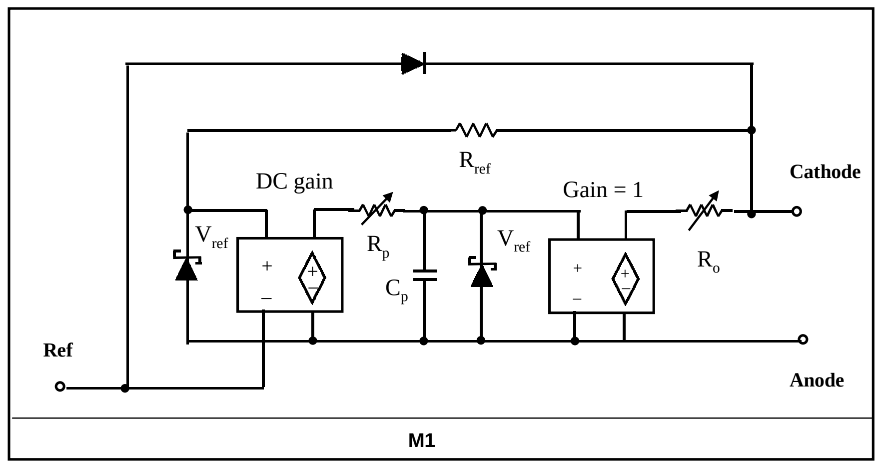


Voltage regulator TL431

R_o: output resistance
R_p, C_p: low frequence pole R and C

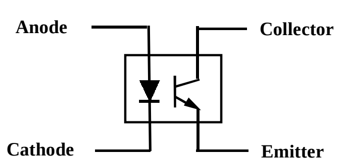
V_{ref}: reference voltage

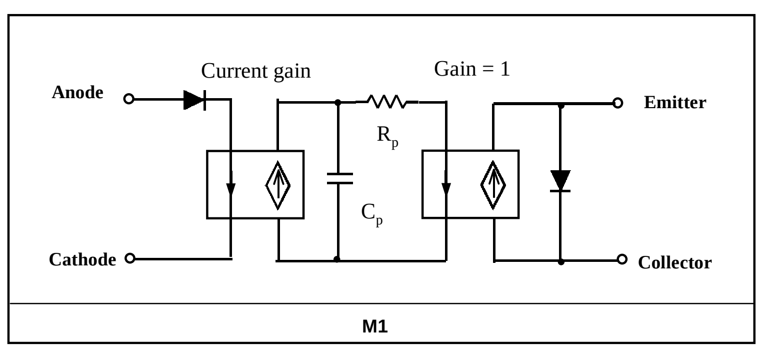




Optical coupler MOC8101

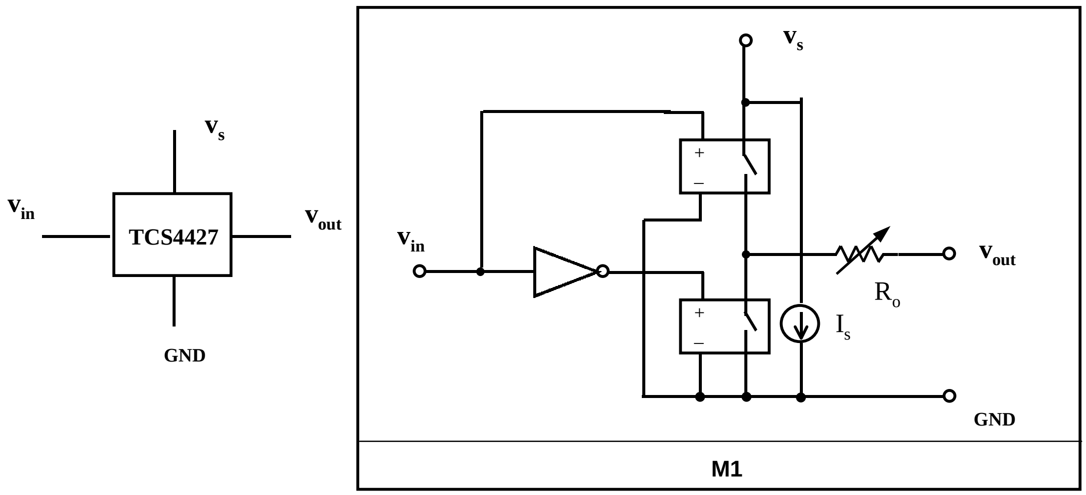
R_p, C_p: low frequence pole R and C





Gate driver TSC4427

I_S: static power supply current



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Vita

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