DESIGN AND ANALYSES OF A DIMPLE ARRAY INTERCONNECT TECHNIQUE FOR POWER ELECTRONICS PACKAGING

by

Sihua Wen

Dissertation submitted to the faculty of
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Materials Science & Engineering

Dr. Guo-Quan Lu, Chair
Dr. J. Daan van Wyk
Dr. Douglas J. Nelson
Dr. Dušan Borojević
Dr. Carlos Suchicital
Dr. Louis Guido

August 2002
Blacksburg, Virginia

Keywords: flexible circuit, flex, assembly, converter, BGA

Design and Analyses of A Dimple Array interconnect Technique for Power Electronics Packaging

Sihua Wen
Advisor: Dr. Guo-Quan Lu
Materials Science and Engineering Department &
Center for Power Electronics Systems
Virginia Polytechnic Institute and State University

Abstract

This research developed a novel, non-wire bond semiconductor interconnect technology, termed the Dimple Array interconnect (DAI), with significantly improved electrical, thermal and mechanical characteristics for power electronics applications. In the DAI structure, electrical connections onto the devices are achieved by solder bumps formed between the silicon device and arrays of dimples stamped on a metal sheet flex.

This research first presents the design of the materials, electrical and thermal performance, reliability, and the fabrication process of the DAI. It was found that due to the use of solder material, the current handling capability and thermal management of Dimple Array interconnected devices are significantly better than those using wire bonds. In addition, the shorter and wider solder joints reduce parasitics, which is a serious problem in wire bond interconnects. The proposed fabrication process of the DAI is simpler than other developing integrated power packaging technologies, such as flip chip and deposited metallization integration. DAI was successfully demonstrated in a half-bridge power electronics module with much improved electrical characteristics.

The study then focuses on the thermomechanical reliability of Dimple Array packages as compared to conventional controlled collapse bonding (CCB) flip chip packages. Experimental approaches, such as power cycling and temperature cycling tests, and numerical simulation with the help of finite element analysis (FEA) were used. The thermal cycling test shows that dimple solder joints display an eightfold reliability improvement over the

conventional CCB solder joints. The power cycling test showed that the measured forward voltage can not reliably reflect the integrity of the solder joint interconnect. However, from metallographic cross-section images of these samples, it was concluded that the DAI solder joints are more reliable than the CCB solder joints under power cycling conditions. FEA results showed excellent correlation with experiments in predicting that the Dimple Array solder joints are more fatigue-resistant due to a reduced stress/strain concentration. Furthermore, failure mechanisms were explored using the mapped stress/strain distribution within the models. It was found that the CCB solder joint has a highly localized strain concentration at the device/solder interface, while strains are more uniformly distributed over the whole Dimple Array solder joint.

Keywords: solder bumping, Dimple Array, power, packaging, modeling, FEM, reliability, thermomechanical, accelerated testing, flip chip, area array packaging

ACKNOWLEDGMENTS

I would like to express my sincere thanks to my advisor, Dr. Guo-Quan Lu, for his guidance, time and efforts on my behalf. I could not have finished on time if he had not been trying to suppress his flexible supervision, which could effectively counteract my strong motivation to graduate.

I am indebted to my other committee members, Dr. J. Daan van Wyk, Dr. Douglas J. Nelson, Dr. Dusan Borojevic, Dr. Carlos Suchicital and Dr. Louis Guido, for agreeing to serve on my committee and offering me thoughtful advice and guidance.

I am grateful to all my packaging research group fellows, Jess Calata, Shatil Haque, Xingsheng Liu, Jinggang Wang, Zhenxian Liang, Robert Fielder, Guofeng Bai, Zhiye Zhang, Xingdan Li, and Kelly Stinson-Bagby, and lab managers Dan Huff and Bob Martin, for their great friendship and help.

I owe sincere thanks to Dengming Peng and Wei Dong for their tremendous help to me when I first came to Blacksburg. I would like to thank my other CPES friends, Rengang Chen, Bo Yang, Kaiwei Yao, Qun Zhao, Lingyin Zhao, Jinghai Zhao, Li Ma, Nick Sun, Jinghong Guo, Yuancheng Ren, Yu Meng, Zhou Chen, Yin Liu, Yong Li, Zhenxue Xu, Bin Zhang, Xigen Zhou, Francisco Canales, Seung-Yo Lee, and Pieter Wolmarans, for their friendship and help. They have made my life at CPES more enjoyable. In addition, thanks to Johan Strydom for distracting me whenever possible as a colleague and former roommate.

I would like to thank Jan Doran, Amy Hill, and David Berry in the Materials Science Department for advising and assisting me. I would like to thank Trish Rose, Teresa Shaw, Elizabeth Tranter, Lesli Farmer, Mike King, Steve Chen, and all of the other CPES staff. They make our work here at CPES possible.

None of this would have been possible without the constant support of my family; them I thank the most of all.

The research was sponsored by the Office of Naval Research. This work made use of ERC Shared Facilities supported by the National Science Foundation under Award Number EEC-9731677.

TABLE OF CONTENTS

List of Figures ix
List of Tables xvii

Chapter 1. Introduction 1
1.1 Significance of first-level interconnections for power semiconductor devices and modules 2
1.2 Current interconnect technologies for packaging of power electronics devices and modules 3
1.2.1 Wire bonding 3
1.2.2 Pressure pack 5
1.2.3 Deposited metallization 7
1.2.4 Area array interconnect 10
1.2.5 Flip chip in power packaging 12
1.2.6 Performance of first-level interconnects 17
1.3 Motivation for developing the Dimple Array interconnect 19
1.3.1 Issues with the wire bond interconnect 19
1.3.2 Issues with the conventional controlled collapse flip chip interconnection 20
1.3.3 Dimple Array interconnect — an alternative area array solder bumping technology 21
1.3.4 Advantages of the Dimple Array interconnect technique 22
1.4 Objectives and outline of this thesis 25
1.5 Original contributions 27
1.6 Publications and patents 28

Chapter 2. Design and development of the Dimple Array interconnect 30
2.1 Prior arts of dimpled structures in microelectronic assemblies 30
2.2 Investigation of the DAI for power semiconductor devices and modules 35
2.2.1 Current handling capability 36
2.2.2 Thermal 37
2.2.3 Parasitics 39
2.2.4 Interconnect materials 40
2.2.5 Solder alloy systems 42
2.2.6 Shape design 45
2.3 Design of the Dimple Array solder joints for improved reliability 48
2.3.1 Documented approaches for improving solder joint reliability 49

2.3.2 Design of the DAI reliability 57
2.4 Process development of the Dimple Array interconnected devices 63
2.4.1 Chip-level UBM processing 63
2.4.2 Dimple flex interconnect fabrication 65
2.4.3 Dimple area array bumping and assembly 67
2.4.4 Underfill 68
2.4.5 Dimple Array interconnected power switching stage module integration 70
2.4.6 Process complexity evaluation 71
2.5 Implementation of the Dimple Array interconnect approach on a half-bridge power IGBT module 73
2.5.1 Existing power module packaging technology 73
2.5.2 Dimple Array module layout design and fabrication 74
2.5.3 Electrical performance of the Dimple Array module 76
Summary 78

Chapter 3. Thermomechanical reliability of the Dimple Array interconnect 80
3.1 Significance of reliability in solder area array packages 80
3.2 Reliability evaluation methods 81
3.2.1 Thermal cycling test 81
3.2.2 Power cycling test 82
3.2.3 Mechanical test 84
3.3 Failure analysis methods 85
3.3.1 Scanning acoustic microscopy (SAM) 85
3.3.2 X-ray inspection 87
3.3.3 Metallographic sectioning 87
3.3.4 Scanning electron microscopy (SEM) 88
3.4 Reliability testing and failure analysis of DAI and CCB interconnects 89
3.4.1 Thermal cycling test 89
3.4.2 Power cycling test 93
3.4.3 Failure analysis using metallographic cross-sectioning 98
3.5 Thermal cycling test results 99
3.5.1 Pb37-Sn63 solder 99
3.5.2 Lead-free Ag3.5-Sn96.5 solder 103
3.6 Power cycling test results 107
3.6.1 Non-underfilled samples 107
3.6.2 Underfilled samples 110
3.6.3 Ag3.5-Sn96.5 solder 116

3.6.4 C-mode scanning acoustic microscopy 118
Summary 119

Chapter 4. Numerical analysis using finite element simulation 122
4.1 Introduction to numerical analysis 122
4.2 Capabilities and challenges of modern finite element modeling approach 125
4.3 Existing solder joint fatigue life prediction models 125
4.3.1 Plastic strain-based models 126
4.3.2 Creep strain-based models 128
4.3.3 Energy-based models 129
4.4 Documented FEM analysis of area array packages 130
4.4.1 FEM analysis of CBGA and CCGA by IBM 131
4.4.2 FEM modeling of enhanced standoff height solder joints 133
4.4.3 FEM modeling of underfill effects 137
4.5 FEM modeling of the thermal fatigue of DAI and CCB solder joints 138
4.5.1 Material models 138
4.5.2 Modeling process 146
4.6 FEM modeling results 152
4.6.1 Thermal cycling 152
4.6.2 Power cycling 159
4.7 Discussions 162
4.7.1 DBC and die-attach effects 162
4.7.2 Correlation between FEM and experiments 163
4.7.3 Discussion of various modeling issues 167
Summary 176

Chapter 5. Future applications of the Dimple Array interconnect 178
5.1 Discrete power package 178
5.1.1 Conceptual CAD design 178
5.1.2 Fabrication of the DAI TO-247 package 179
5.1.3 Thermal modeling and discussion 179
5.2 Packaging of FTO 181
5.2.1 Available packaging schemes 181
5.2.2 Processing 182
5.2.3 Thermal considerations for FTO packaging 184

Chapter 6. Summary and conclusions 186

6.1 Design and development of the Dimple Array interconnect.....186
6.2 Thermomechanical reliability of the Dimple Array interconnect.....187
6.3 Numerical analysis using finite element simulation 189
References 191
VITA..... 201

LIST OF FIGURES

Figure 1.1 Technology roadmap of IR's board-level discrete power packages (courtesy of International Rectifier). 1

Figure 1.2 Opened-up view of a TO-247 MOSFET package. 4

Figure 1.3 Wire bond power modules and schematic of interconnect hierarchy: (a) EUPEC MCM package (courtesy of EUPEC); (b) inside of a power module; and (c) power module components. 4

Figure 1.4 Ball bond (a); and wedge bond (b) and (c) (magnifications were estimated). 5

Figure 1.5 Aluminum wedge bonding machine step sequence (1-6) (reprinted with permission of Kluwer Academic Publishers). 6

Figure 1.6 Evolution of pressure pack packaging. 6

Figure 1.7 Construction of a press-pack GTO (courtesy of ABB): (a) cross-section schematic of press-pack GTO; and (b) GTO housing and GTO devices. 7

Figure 1.8 ABB IGCT 5SHY 35L4503 (courtesy of ABB). 7

Figure 1.9 Cross-section view of GE POL module structure.....8

Figure 1.10 Photograph of a POL module fabricated at Virginia Tech. 9

Figure 1.11 Cross-section schematic of the Embedded Power technology. 9

Figure 1.12 Processing flowchart of the embedded power stage. 10

Figure 1.13 Embedded Power IPEM prototype. 10

Figure 1.14 Applications of flip chips: (a) flip chip BGA structure (courtesy of Oki Electric Industry Co. Ltd); and (b) V-groove fiber alignment using reflowed Au-Sn solder bumps (courtesy of Karl Suss). 11

Figure 1.15 Fairchild's bottomless SO-8 package using solder bump technology (reprinted with permission of Power Electronics Technology). 13

Figure 1.16 Fairchild's MOSFET BGA (courtesy of Fairchild Semiconductor). 14

Figure 1.17 An SEM image of IR's FlipFET (courtesy of IR). 15

Figure 1.18 Flip chip power packaging developed at CPES: (a) schematic of D^2BGA; and (b) chip scale power package.....15

Figure 1.19 DirectFET™ package (courtesy of IR): (a) cross-section of DirectFET soldered to PCB; and (b) comparison of current conduction paths. 16

Figure 1.20 Schematics of ThinPak cross-section and three-dimensional view (courtesy of SPCO).....17

Figure 1.21 Wire bond failures: (a) photograph shows electrical overstress indicated by fusing of three parallel wirebonds of a power transistor (courtesy of Motorola); (b) wire bond heel crack, overbonded (courtesy of Motorola); and (c) wire bond fatigue crack (magnifications were estimated).....20
Figure 1.22 Stress/strain concentration at CCB solder joints. 21
Figure 1.23 The Dimple Array interconnect (a); and the wire bond interconnections (b). 22
Figure 1.24 Structures of (a) the Dimple Array interconnect; and (b) the controlled collapse bonding. 23
Figure 2.1 US Patent 6,284,563: compliant microelectronic assemblies. 30
Figure 2.2 US Patent application 2001/0041370: A method for fabricating a semiconductor package with a heat sink. 31
Figure 2.3 US Patent application 2001/0045643: A stress-relief structure for the semiconductor package. 31
Figure 2.4 US Patent 5,110,761, method to form top contact for non-flat semiconductor devices: (a) flat metal lead interconnection; (b) and (c) dimpled metal lead interconnection. 32
Figure 2.5 US Patent application 2001/0028109: A method for area array flip chip bonding. 33
Figure 2.6 Metallographic images of Powermite® packages (a) flat copper strap; and (b) dimpled copper strap. 34
Figure 2.7 Artistic view of the Dimple Array interconnected package.....35
Figure 2.8 Infrared microscopy image of the temperature distribution of a power transistor interconnected by wire bonds. 36
Figure 2.9 Comparison of contact geometry of wire bond and flip chip interconnects. 37
Figure 2.10 Conventional wire bond SOIC-8 (top) and the FLMP SOIC-8 package (bottom) (reprinted with permission of Rajeev Joshi, Fairchild Semiconductor). 38
Figure 2.11 Comparison of the electrical and thermal resistance of individual wire bond, flip chip solder joint and the Dimple Array solder joint. 39
Figure 2.12 Inductance (a) and resistance (b) of some lead frame materials as a function of frequency (reprinted with permission of Kluwer Academic Publishers).....42
Figure 2.13 Phase diagrams of some solder alloy systems. 43
Figure 2.14 FEM model of IBM's ceramic column grid array interconnection with coated solder columns. 44
Figure 2.15 Shape parameters of the Dimple Array solder joint. 46
Figure 2.16 BGA solder joints shape prediction using Surface Evolver: (a) barrel shape solder joint and (b) hourglass shape solder joint. 47

Figure 2.17 Dimple solder joint shape evolution as predicted by Surface Evolver. 48
Figure 2.18 A first-order estimation of the fatigue life of solder joints. 48
Figure 2.19 IBM's BGA and column grid array. 49
Figure 2.20 Fatigue of 50mil solder columns subjected to –55/125^{o}C thermal cycles. 50
Figure 2.21 Double-bump structure in Motorola's wafer-level chip scale package (courtesy of Motorola, magnification was estimated). 51
Figure 2.22 Motorola's wafer-level chip scale packaging processing (courtesy of Motorola). 51
Figure 2.23 S3-Diepack schematics. 52
Figure 2.24 Failure modes of the conventional WLCSP (a) and the S3-Diepacks (b). 53
Figure 2.25 Comparison of flip chip structures: (a) CCB; and (b) SST solder joints. 53
Figure 2.26 Backside clip attachment of Mechatronics power packages from Motorola. 54
Figure 2.27 Fatigue failure modes for PCSB (a) and a conventional BGA solder joint (b). 56
Figure 2.28 Accumulated fatigue failure rate of PCSBs and conventional BGA solder joints. 56
Figure 2.29 Nokia's polymer core bump (a) and transfusion bonding process (b) (reprinted with permission of Chip Scale Review). 57
Figure 2.30 Schematics of C4 solder joint: (a) 3D sketch; and (b) sections before and after thermal displacement. 59
Figure 2.31 Sample flex substrate and the construct of a single-sided flex circuit (courtesy of Allflex, Inc). 60
Figure 2.32 Test vehicle design for measuring resistance change during thermal cycling: (a) dimple copper flex pattern; and (b) CAD layout showing four underlying devices. 60
Figure 2.33 Effects of dimple height on solder joint shape. 61
Figure 2.34 Proposed UBM structure for the Dimple Array solder bumping. 64
Figure 2.35 A fixture used to stamp the dimple flex. 66
Figure 2.36 Fabrication of the dimple flex using stamping fixtures: (a) stamping process; and (b) top view of a stamped dimple copper flex. 67
Figure 2.37 Process flow of the Dimple Array solder bumping. 68
Figure 2.38 Conventional underfill-flow process. 69
Figure 2.39 Underfilled power device with Dimple Array interconnects. 69
Figure 2.40 Schematic of Dimple Array interconnect and integrated DAI power switching stage module. 70
Figure 2.41 Flowchart for manufacturing various power modules: (a) wire bond; (b) flip-chip; (c) deposit-metallization; and (d) DAI modules. 72

Figure 2.42 Circuit diagram of half-bridge power IGBT module (shaded region) and its drive circuit. 73
Figure 2.43 Cross-sections of the conventional package (a) and the improved package (b). 74
Figure 2.44 Top views of (a) the conventional package and (b) the improved package 74
Figure 2.45 The circuit layout design of the Dimple Array interconnected module. 75
Figure 2.46 A demonstration half-bridge IGBT module (a) and a close-up look (b). 75
Figure 2.47 A second-phase prototype module. 76
Figure 2.48 Power module test circuits: (a) for the low-side switch; (b) inductor charging path (thick line); and (c) inductor discharging path (thick line). 76
Figure 2.49 Power stage switching characteristics at 600V and 50A: (a) turn-on; and (b) turn-off. 77
Figure 2.50 Switching energy comparison of the commercial wire bond module and the Dimple Array module. 78
Figure 3.1 Temperature cycling profile specified by JEDEC. 82
Figure 3.2 Power cycling test circuit for 1200V, 300A single-switch IGBT device. 83
Figure 3.3 Mechanical shear and tensile test: (a) test sample; (b) double lap shear configuration; and (c) tensile configuration. 85
Figure 3.4 C-SAM monitoring of crack evolution in the die-attach of silicon devices. 86
Figure 3.5 TAMI scanning principle (reprinted with the permission of Sonix Incorporated). 86
Figure 3.6 X-ray inspection of: (a) and (b) BGA packages; and (c) wire bond packages (all photos courtesy of X-Tek). 87
Figure 3.7 Electron/specimen interactions in SEM (reprinted with permission of Professor Scott Chumbley, Iowa State University). 89
Figure 3.8 Schematic of the resistance measurement for thermal cycling samples. 90
Figure 3.9 Phase diagram of aluminum and silicon. 91
Figure 3.10 Metallized wafer with solderable patterns. 92
Figure 3.11 Thermal cycling samples. 92
Figure 3.12 Power cycling test circuit. 94
Figure 3.13 Power cycling test setup (a) and a typical power cycling temperature profile (b). 95
Figure 3.14 Temperature dependency of diode forward voltage 96
Figure 3.15 CCB copper interconnect with preformed solder balls. 97
Figure 3.16 Zero-cycle resistance histogram for (a) CCB and (b) DAI solder joints. 99
Figure 3.17 Typical normalized resistance R/R_0 versus number of thermal cycles. 100
Figure 3.18 Cumulative fails based on a 20% increase in resistance, using Pb37 solder. 101

Figure 3.19 Cumulative fails based on a 50% increase in resistance, using Pb37 solder. 101
Figure 3.20 (a) A dimple solder joint that failed at 285 thermal cycles; and (b) the zoomed-in view of the circled region. 102
Figure 3.21 (a) A dimple solder joint after 400 thermal cycles; and (b) the zoomed-in view of the circled region. 102
Figure 3.22 (a) A typical CCB solder joint that was found open at 135 cycles; and (b) the zoomed-in view of the circled region. 103
Figure 3.23 (a) A CCB solder joint that failed (50% up) at 135 cycles; and (b) the zoomed-in view of the circled region. 103
Figure 3.24 Typical resistance change of the Ag3.5-Sn96.5 Dimple and CCB solder joints. 104
Figure 3.25 Cumulative fails based on a 20% increase in resistance, using Ag3.5-Sn96.5 solder. 105
Figure 3.26 Cumulative fails based on a 50% increase in resistance, using Ag3.5-Sn96.5 solder. 105
Figure 3.27 (a) An Ag3.5-Sn96.5 dimple solder joint after 345 thermal cycles; and (b) the zoomed-in view of the circled region. 106
Figure 3.28 (a) Ag3.5-Sn96.5 CCB solder joint after 400 thermal cycles; and (b) the zoomed-in view of the circled region. 106
Figure 3.29 Temperature change reflecting an increase in thermal resistance of CCB test samples. 107
Figure 3.30 Typical cracked CCB solder joints. 108
Figure 3.31 (a) Just-initiated crack under a 200x microscope; (b) no crack is found at copper/solder interface. 108
Figure 3.32 Measured package temperature as a function of the number of power cycles. 109
Figure 3.33 Measured package forward voltage as a function of the number of power cycles. . 109
Figure 3.34 A typical failed Dimple Array samples (non-underfilled) at 2,800 power cycles. .. 110
Figure 3.35 Measured voltage as a function of the number of power cycles for underfilled CCB packages. 111
Figure 3.36 A typical CCB solder joint after 4,000 power cycles. 111
Figure 3.37 A zoomed-in view of the corner crack shown in Figure 3.36. 112
Figure 3.38 A CCB solder joint after 4,000 power cycles also shows voiding at the copper/solder interface (black arrow)..... 112
Figure 3.39 A zoomed-in view of the corner crack shown in Figure 3.38. 113
Figure 3.40 Optical microscopy images of CCB solder joints after 8500 cycles (sample #4,5). 113

Figure 3.41 Cross-sections of (a) a center CCB solder joint and (b) an edge CCB solder joint after 8,500 cycles. 114
Figure 3.42 Power cycling voltage measurements for underfilled CCB and Dimple packages. 114
Figure 3.43 (a) A typical dimple solder joint after 5,000 cycles; (b) a dimple solder joint after 8,500 cycles. 115
Figure 3.44 Cross-section of a typical dimple solder joint after 12,700 cycles (Sample #9). 115
Figure 3.45 Forward voltage versus number of power cycles for Ag3.5-Sn96.5 dimple solder joints. 116
Figure 3.46 A zero-cycle Ag3.5-Sn96.5 dimple solder joint. 116
Figure 3.47 Cross-section of a dimple solder joint after 12,700 cycles. 117
Figure 3.48 An Ag3.5-Sn96.5 dimple solder joint after more than 35,000 power cycles. 117
Figure 3.49 C-mode SAM image of a zero-cycle Dimple package. 118
Figure 3.50 A dimple sample after 2,800 power cycles (#17): (a) C-mode SAM images; and (b) the cross-section view..... 119
Figure 3.51 Summary of the Pb37-Sn63, non-underfilled samples for thermal cycling test. 120
Figure 3.52 Summary of the Pb37-Sn63, underfilled samples for the power cycling test. 121
Figure 4.1 Schematic of a C4/CBGA assembly. 131
Figure 4.2 Finite element models of the CBGA. 132
Figure 4.3 Equivalent inelastic strain of various solder fillets. 132
Figure 4.4 Finite element model of CCGA assembly: (a) overall model; (b) a solder column; and (c) a deformed solder column. 133
Figure 4.5 FEM mesh of a WLCSP with stacked balls. 134
Figure 4.6 Lifetime prediction for various WLCSP and flip chip designs. 135
Figure 4.7 Schematic of the thermal fatigue fracture mechanism in the Pb-5Sn alloy: (a) formation mechanism of Laird-type striation; (b) formation mechanism of the Pb alloy striation; and (c) estimation of the direction of crack propagation and slip plane. 136
Figure 4.8 Thermal fatigue life of CCB microsolder joints. 136
Figure 4.9 Package deformation at 125^{o}C without (a) and with (b) underfill. 137
Figure 4.10 Total strain versus life equation (reprinted with permission of L. T. Nguyen). 139
Figure 4.11 Steady-state creep strain rate of the Pb37-Sn63 solder (a) and the Ag3.5-Sn96.5 solder (b) as a function of stress at various temperatures. 145
Figure 4.12 Plastic properties of (a) the eutectic Pb-Sn solder and (b) the eutectic Ag-Sn solder. 146

Figure 4.13 Sample modeling process using the dimple solder joint and copper interconnect: (a) base geometry; (b) surface mesh; (c) solder joint mesh obtained from sweep of the surface mesh; and (d) copper interconnect mesh. 147
Figure 4.14 FEM models: (a) CCB package not showing Cu; (b) full CCB package; (c) DAI package not showing Cu; and (d) full DAI package. 149
Figure 4.15 Power cycling test sample: (a) Dimple Array package and (b) CCB package. 150
Figure 4.16 FEM models for (a) the DAI and (b) the CCB. 151
Figure 4.17 Deformation of the Dimple Array package at the cold extreme (-55^{o}C), 30x magnification. 152
Figure 4.18 CEEQ contour of the DAI after the initial cooling stage. 153
Figure 4.19 Von Mises stress distribution in (a) CCB models and (b) DAI models (Chip center is marked with circle on the left side). 154
Figure 4.20 CCB solder joints strain contours: (a) PEEQ and (b) CEEQ (the chip center is to the left). 155
Figure 4.21 DAI solder joints strain contours: (a) PEEQ and (b) CEEQ (the chip center is to the left). 155
Figure 4.22 Stress components at the weakest locations in solder joints; cold extreme. 156
Figure 4.23 Strain components at weakest locations in solder joints; cold extreme. 157
Figure 4.24 Equivalent inelastic strain (CEEQ and PEEQ) histories in solder joints. 158
Figure 4.25 Shear stress-strain hysteresis loops of the CCB and dimple solder joints. 159
Figure 4.26 Von Mises stress contours in the dimple solder joints at the cold extreme. 159
Figure 4.27 Von Mises stress contours in the CCB solder joints at the cold extreme. 160
Figure 4.28 Equivalent inelastic strain histories for power cycling. 161
Figure 4.29 Total accumulative equivalent plastic strain for first four cycles: (a) DAI and (b) CCB solder joint. 161
Figure 4.30 Normal stresses S22 at the solder/device interface for (a) CCB and (b) DAI. 165
Figure 4.31 Correlation: (a) optical microscopy image of a DAI joint (12,700 cycles); and (b) the FEM predicted inelastic strain distribution. 166
Figure 4.32 Correlation: (a) SEM image of a CCB joint (8,500 cycles); and (b) the FEM predicted inelastic strain distribution. 166
Figure 4.33 History of the eutectic DAI solder joint: (a) Mises stress; (b) strain; and (c) temperature 167
Figure 4.34 Temperature profile (top) and von Mises stress (bottom) for a case study that considers residual stress (a) and omits residual stress (b). 169

Figure 4.35 Effects of underfill materials: (a) DAI and (b) CCB solder joint. 170
Figure 4.36 FEM comparison of Ag3.5-Sn96.5 solder and Pb37-Sn63 solder under power cycling conditions. 172
Figure 4.37 Comparison of the creep strain rates of constrained solder (such as in the solder joint). 173
Figure 4.38 Two dimple shapes: (a) the original and (b) a flat-bottom-dimple interconnect. 174
Figure 4.39 Stress contours: (a) the original and (b) the flat-bottom-dimple solder joint. 174
Figure 4.40 Comparison of the inelastic strain range in the weakest sites of the original and the flat-bottom-shaped dimple solder joints. 175
Figure 5.1 (a) Artistic view of the Dimple Array TO-247 discrete MOSFET package; and (b) the wire bond TO-247 discrete MOSFET package, top molding not shown. 178
Figure 5.2 Fabrication flowchart for the DAI TO-247 MOSFET. 179
Figure 5.3 Thermal performance of TO-247 power packages: wire bond (a) and DAI (b) (Graphs courtesy of Dr. Tao Lin, Math Dept. at Virginia Tech)..... 180
Figure 5.4 FTO device structure..... 181
Figure 5.5 Various approaches for FTO packaging: (a) ThinPak; (b) press pack; (c) wire bond; and (d) solder area array. 182
Figure 5.6 FTO packaging process using dimple area array bumping. 183
Figure 5.7 Prototype FTO package (a) and simulation model (b). 184
Figure 5.8 Transient thermal impedance for wire bond model (a) and Dimple Array bumping FTO model (b). 184
Figure 6.1 Summary of the Pb37-Sn63, non-underfilled samples for the thermal cycling test. . 188
Figure 6.2 Summary of the Pb37-Sn63, underfilled samples for the power cycling test. 189

LIST OF TABLES

Table 1.1 Wire bonding processes. 5
Table 1.2 Flip chip packaging in power electronics applications. 13
Table 1.3 Pros and cons of various power packaging technologies 18
Table 1.4 Comparison of wire bonding and flip chip bonding. 23
Table 2.1 Dimpled structures in US patents and patent applications. 34
Table 2.2 Properties for various interconnect materials. 40
Table 2.3 Properties of some solder materials. 45
Table 2.4 Properties of some underfill materials. 55
Table 2.5 Properties of LOCTITE 3565 underfill. 62
Table 2.6 Various UBM deposition processes. 64
Table 2.7 Typical UBM systems and their applicable processing techniques. 64
Table 2.8 UBM system for the Dimple Array solder bumping. 65
Table 3.1 Power cycling test parameters used by Scheuermann, et al. 84
Table 3.2 Summary of thermal cycling test samples. 92
Table 3.3 Foci of the thermal cycling and power cycling tests. 119
Table 4.1 Capabilities and limitations of FEM. 126
Table 4.2 Material properties used in the FEM analysis. 144
Table 4.3 Visco-plastic properties of eutectic solders. 145
Table 4.4 Comparison of the equivalent creep, plastic and total inelastic strain per cycle. 162
Table 4.5 Strain ranges and the maximum stress at the cold extreme for the no-DBC case and the with-DBC case. 162
Table 4.6 FEM predictions and experimental results for thermal cycling. 164
Table 4.7 Prediction of crack initiation time using FEM. 165