SMALL-SIGNAL ANALYSIS AND DESIGN OF A DISTRIBUTED POWER SYSTEM

by

Lucian R. Lewis II

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APPROVED:

Fred C. Lee
Dr. Fred C. Lee, Co-chairman

Bo H. Cho
Dr. Bo H. Cho, Co-chairman

Dr. Vatche Vorperian

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(ABSTRACT)

A small-signal analysis of a two-stage distributed power system is performed. Although the distributed power system is composed of conventional PWM converters, the analysis methods can be extended to systems using other converter topologies. The analysis focuses on two important features of a two-stage distributed power system: parallel power modules and cascaded regulators.

The small-signal characteristics of parallel module regulators are analyzed, and an expression for the loop-gain of a parallel-module system is obtained. It is found that a parallel module system can be configured so that the loop-gain of the system is independent of the number of modules.

The effects of placing switching regulators in cascade are analyzed. Of primary concern is the effect of the second stage's dynamic impedance on the first stage's control loops. It is found that the negative dynamic resistance of the second stage gives rise to right-half-plane poles in the opened-loop gains of the first stage. Fundamental loop-gain analysis is used to determine that stability of the system. It is found that the first stage of a cascaded regulator system must satisfy additional design constraints in order to be stable while driving a negative dynamic resistance.

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Chapter 1

INTRODUCTION

It is common practice to use a centralized approach to power system solutions for computer and other VLSI systems. Such a power system typically consists of a single, high-power, remotely-located regulator that is connected to its load through a long bus-bar distribution network. This approach faces serious problems in meeting the requirements of future systems. As the size of CMOS VLSI circuitry shrinks, logic supply voltages drop and power levels increase, leading to requirements for hundreds or thousands of amps of current at voltages of five volts or less. The stress placed on power switches by such currents may greatly reduce the reliability of the power system. Another important problem results from the dynamic nature of VLSI loads. Because CMOS gates only consume power during transitions between logical states, CMOS circuitry requires the power system to accommodate very large and rapid changes in load demand. The inductance associated with a long distribution bus prevents the centralized power system from responding fast enough to large changes in load current [1]. In addition, power distribution cables are lossy and degrade system efficiency. As a solution, a distributed approach may be used to improve the power system's ability to respond to VLSI loads as well as improve its reliability.

A distributed power system (DPS) may employ one or two stages of switching power conversion. In a single-conversion architecture DPS, AC or rectified AC would be distributed to multiple off-line switching regulator modules operating in parallel. In a dual-conversion-architecture DPS, two stages of parallel-module switching regulators are used. The first stage (the line conditioner) converts off-line power to an intermediate DC voltage, which is distributed throughout the system to the second stage (load converters). The load converters may be located in slots near the logic cards or on the logic cards themselves. Both types of distributed power systems use parallel power modules to lower component strosses and provide fault tolerance through the use of redundant modules. Also, both approaches allow the power supply to be located much closer to its load than a centralized power system, allowing improvements in response time and distribution efficiency. A comparison between distributed power system approaches shows that while the single stage architecture has inherently higher efficiency and results in a simpler system than the two-stage configuration, its suffers from the need to distribute prime input power throughout the entire system Because of the wide input voltage ranges, and EMI and high voltage isolation requirements for interfacing with prime power do not lend themselves to high power densities, a single stage approach is probably not feasible if on-card regulation is required. For these and other reasons [1], a two stage architecture was chosen for this study.

Most of the research related to distributed power systems has concentrated on methods of achieving the high power densities necessary for single card or on-board operation, while relatively little work has been directed at system-level considerations. In order to help fill this gap, a research project was sponsored by the IBM Systems Integration Division in Manassas, Virginia. The purpose of the project was to study the modeling, analysis and design of a dual-conversion architecture DPS using both small-signal analysis and time-domain simulation. Because the goals of the project were related to system level considerations, well-known PWM converter topologies were used, allowing concentration upon system-level phenomena. While the details of the analysis presented in the following thesis are applicable only to the topologies considered, the analysis approach should remain valid for systems us-

ing other converter types as well. Fig. 1.1 shows a block diagram of the two-stage DPS. Further details about the present DPS hardware will be presented as needed in the following text. Details concerning the choice of system configuration and circuit topologies are discussed in reference [1].

This thesis demonstrates the use of small-signal analysis methods and computer simulation in the analysis and design of a dual-conversion architecture DPS. Although this thesis considers only buck-derived PWM converters, the approach to the modeling and analysis of the DPS may be readily adapted to other circuit topologies. Chapter 2 briefly discusses the modeling of the DPS, which is covered in detail in reference [2]. Chapter 3 discusses the analysis and design of parallel module switching regulators, using the load converter as a design example. The analysis and design of cascaded switching regulators is considered in Chapter 4. Primary concern is given to the modeling, analysis and design of the line conditioner in the cascaded configuration. Analysis methods and design guidelines which consider the negative-resistance characteristic of the load converters' input impedance are presented for the line conditioner. The design of a filter for the intermediate bus is also discussed. Summary and conclusions are presented in Chapter 5.

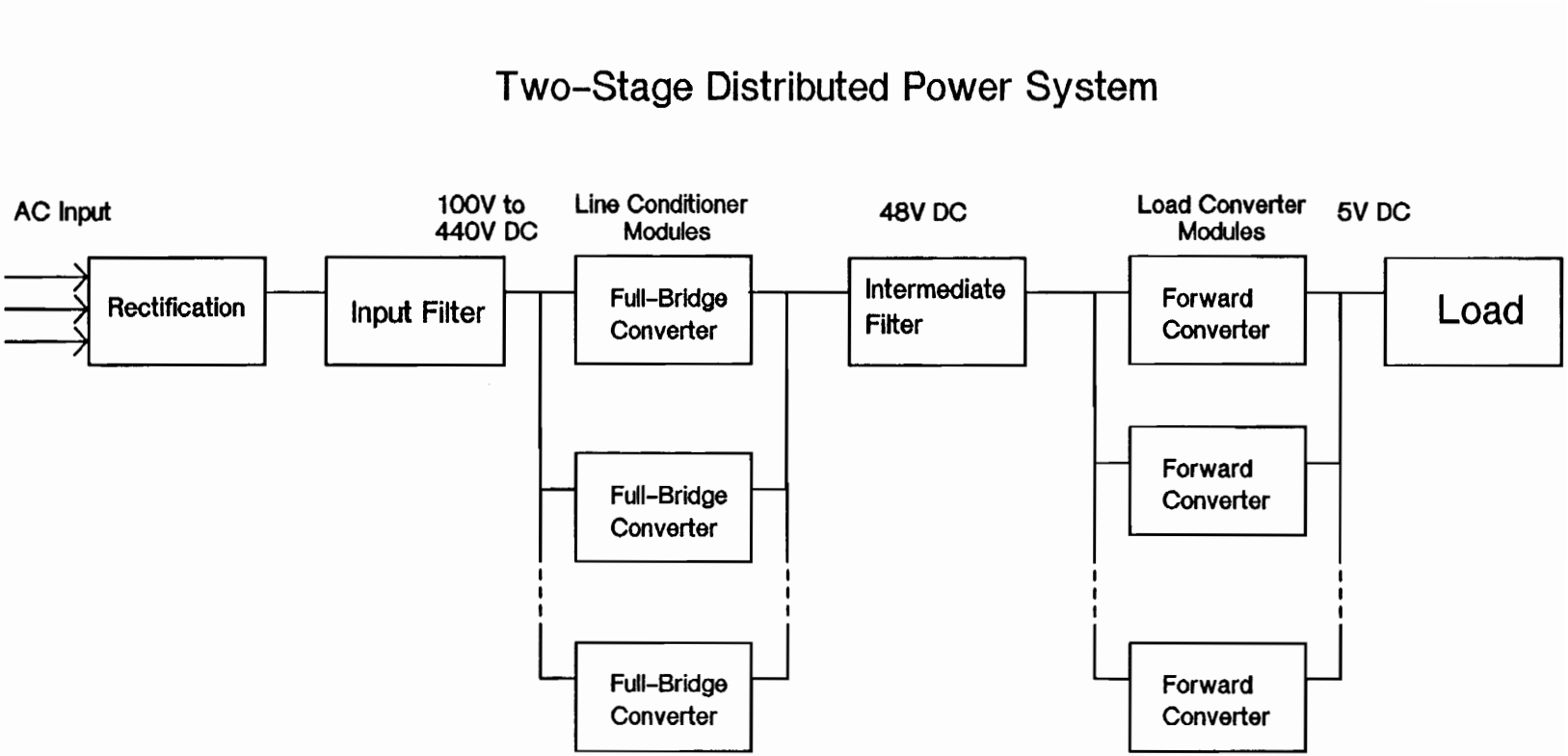


Figure 1.1. Block Diagram of Two-Stage DPS

Chapter 2

MODELING APPROACH FOR THE DISTRIBUTED POWER SYSTEM

Even a moderately-sized DPS with parallel-module switching power converters and associated circuitry is a complex, high-order system. Modelling such a large system with individual circuit elements requires a great deal of effort and results in a model that cannot be modified easily if the system configuration should change. By modeling the system at the component level (i.e. power stage, input filter, load, etc.), changes in system configuration may be handled with relative ease. Analysis and design of a high-order system poses an intractable problem if the system is considered in its entirety. It is therefore desirable to model the system so it can be analyzed and designed at the component level (i.e. a switching regulator). This requires a computer simulation model of the system that is modular, allowing components and subsystems to be simulated either individually or as a part of the full system. In order to achieve modularity, each component must be treated as an unterminated, multi-port network, because the source and load characteristics seen by a given component are determined by its place within the full system.

Each component is modeled by writing the state and output variables as functions of input variables and component parameters. The selection of input and output variables at each port must result in a set of components with a compatible interconnection scheme.

A switching regulator is modeled with three functional blocks: the power stage, feedback compensation and the pulse-width modulator (see Fig. 2.1). To maximize the flexibility of the switching regulator modeling, each functional block is modeled as an independent unterminated module, allowing a variety of switching regulators to be modeled by connecting the appropriate blocks from a pre-stored model library. Due to its discrete and nonlinear nature, the power stage requires different models for time-domain simulation and small-signal analysis. Two feedback blocks model the sensing and compensation circuitry of the voltage and current control-loops. A detailed circuit model that accounts for op-amp limitations was used for the voltage-loop compensator. For a current-injection-controlled (CIC) regulator, the current feedback circuit is modeled by a constant gain. The PWM block generates the switch ON / OFF command from the current and voltage feedback signals and an internally-generated

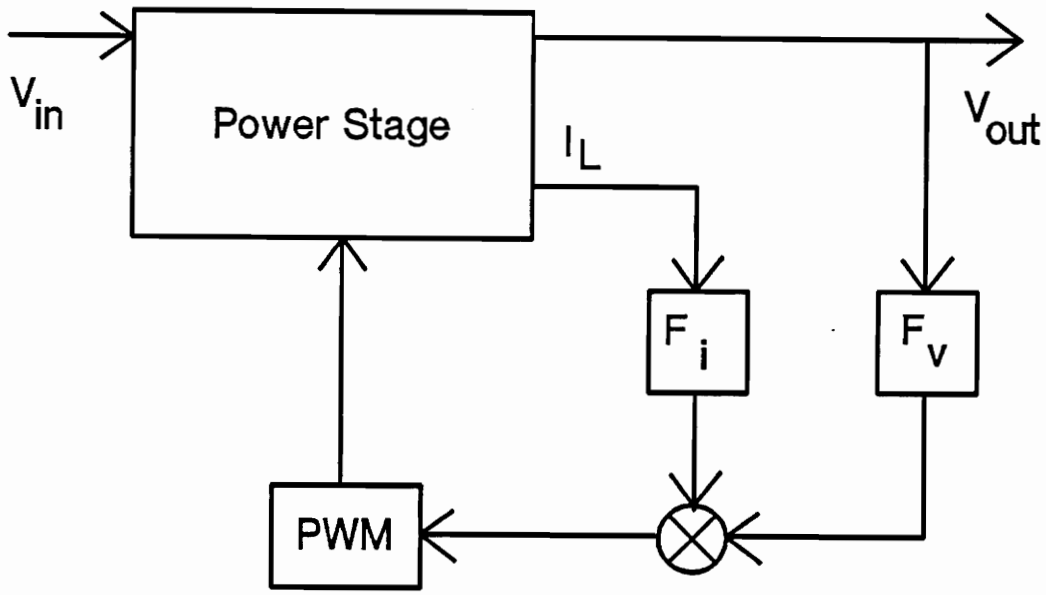


Figure 2.1. Block Diagram of General Switching Regulator Model

ramp. comparisons are used to analyze the DPS. The PWM block also includes protection and control functions such as soft start, peak current protection, and duty cycle limiting. Due to its nonlinear nature, the PWM block also requires different models for time-domain and small-signal analysis.

The Boeing Computer Services program, EASY5, allows the use of a modular modeling approach, and has been successfully adapted to electrical power systems as described in references [2],[3] and [4]. The models used for both time and frequency-domain simulation for this system are described in detail in reference [2].

Chapter 3

SMALL-SIGNAL ANALYSIS AND DESIGN OF PARALLEL POWER MODULES

As discussed in Chapter 2, parallel power modules will be used in distributed power systems for reasons of increased reliability, flexibility and higher performance. Parallel-module switching regulators will almost certainly employ current-mode control to achieve a stable, high performance system. Since the design of current-mode-controlled switching regulators is basic to the material presented in this thesis, it will be discussed briefly for single regulators in the following section.

3.1 Current-Mode Control of Switching Regulators

A single-loop-controlled switching converter is regulated by sensing the converter's output voltage and comparing this voltage with a preset reference to generate an error signal. After passing through some compensation circuitry, this error signal is compared with a ramp waveform to generate a pulse-width-modulated (PWM) control signal for the power switch. The basic elements of a single-loop controlled forward converter are shown in Fig. 3.1. While the single-loop scheme is relatively easy to analyze and design, it can be difficult to obtain designs which provide good stability and high performance. Obtaining satisfactory results is especially difficult for boost and flyback converters. In order to improve both the stability and small-signal performance characteristics of switching regulators, a two-state-variable control scheme utilizing the output-filter inductor current, in addition to the capacitor voltage, may be used. In this scheme, the ac (ripple) portion of the inductor current is used in place of the artificially-generated ramp found in the single-loop control scheme. A multi-loop-controlled forward converter is shown in Fig. 3.2. An early form of multi-loop control was developed for NASA's standardized-control-module (SCM) project. The SCM implementation of multi-loop control obtains the inductor current waveform by sensing the voltage applied to the inductor core and integrating it to reproduce the ac portion of the waveform. The SCM control has a

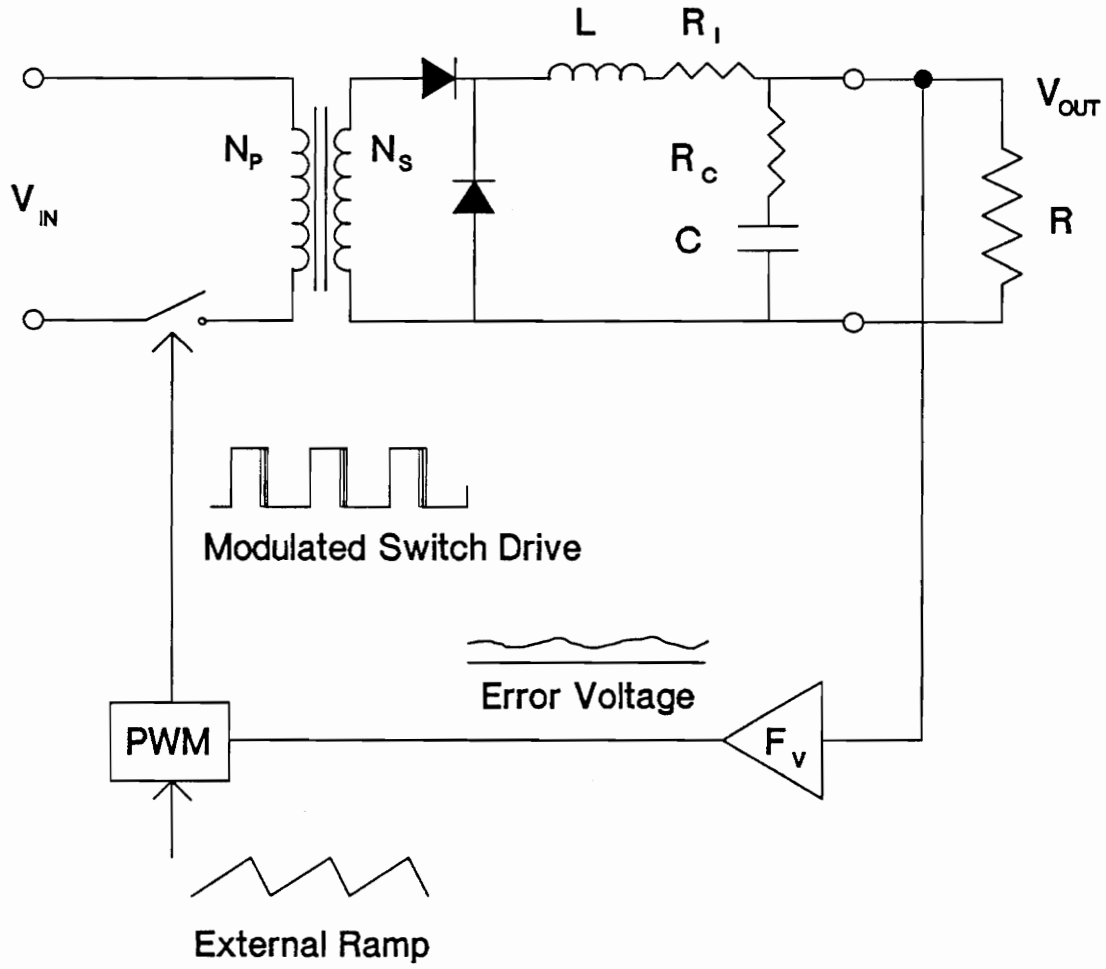


Figure 3.1. Single Loop Control Scheme

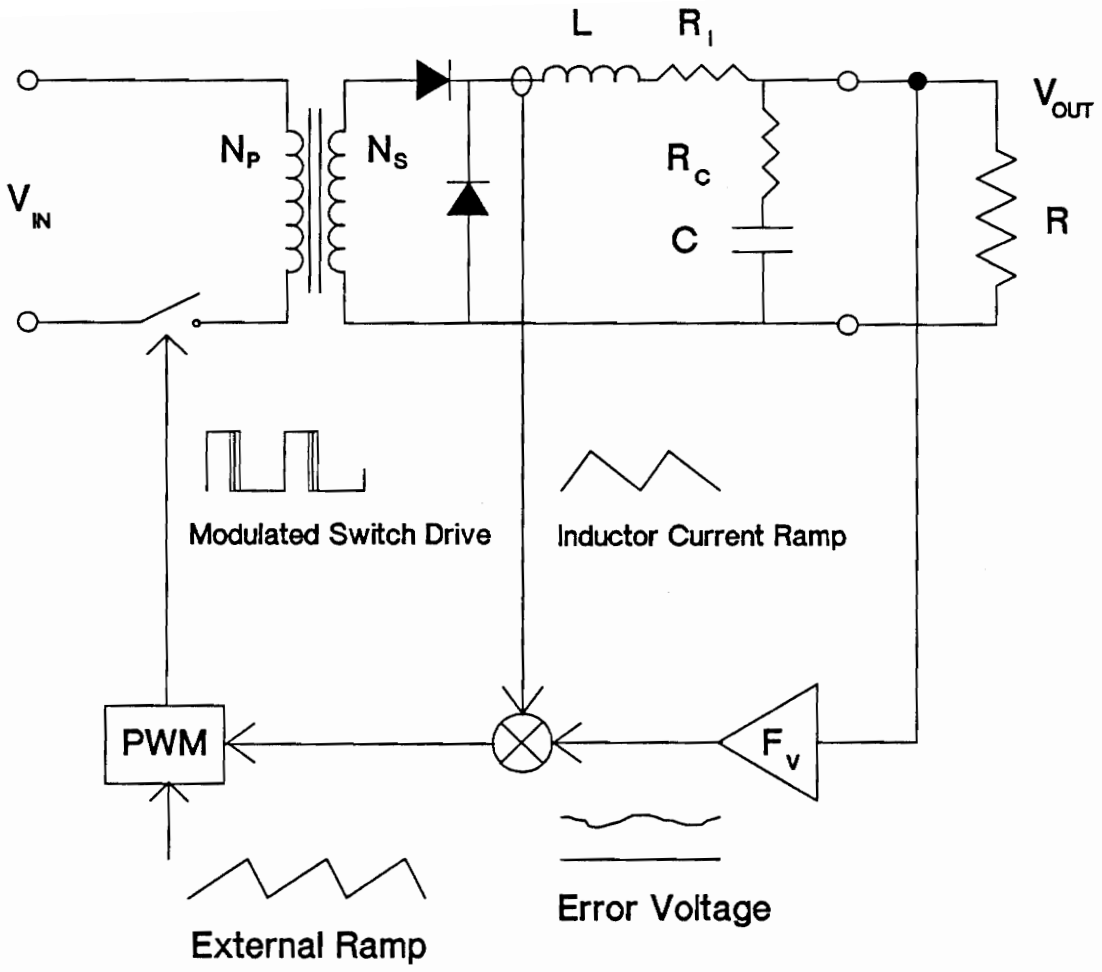


Figure 3.2. Multi-Loop Control Scheme

high level of noise immunity because its waveforms are clean and may be scaled to take full advantage of comparator limits. A set of design procedures was developed for the SCM which allows the designer to simultaneously meet specifications for audio-susceptibility, output impedance, settling time, output peaking and phase margin in a single iteration, thereby eliminating the need for trial and error design.

Another form of multi-loop control known as current-injection-control (CIC) obtains the required ramp function by sensing the switch current for comparison with the error voltage. Because the current-sense waveform for CIC contains both DC and ac information, it may be used to implement switch protection and anti-saturation circuits, and DC current sharing among parallel modules. However, it is important to note that the DC current information does not contribute to the small-signal performance of the regulator. In fact, *from the small-signal perspective, the SCM and CIC control schemes are identical.* Therefore, the design procedures developed for the SCM may be applied to CIC with only minimal change. This work was presented in reference [5], which extended the SCM procedures to CIC regulators and also introduced a combined approach which overcomes the noise problems encountered when using CIC with high-current regulators. A general discussion of the SCM procedure will be presented here. A detailed derivation and discussion of the procedures are presented in reference [6].

The small-signal block diagram of a multi-loop switching regulator is shown in Fig. 3.3. The blocks F_1 through F_4 represent power stage transfer functions obtained through the state-space averaging technique [7]. The transfer-functions for these blocks are shown below for an isolated buck converter with a resistive load. The notation corresponds to that used in Fig. 3.2.

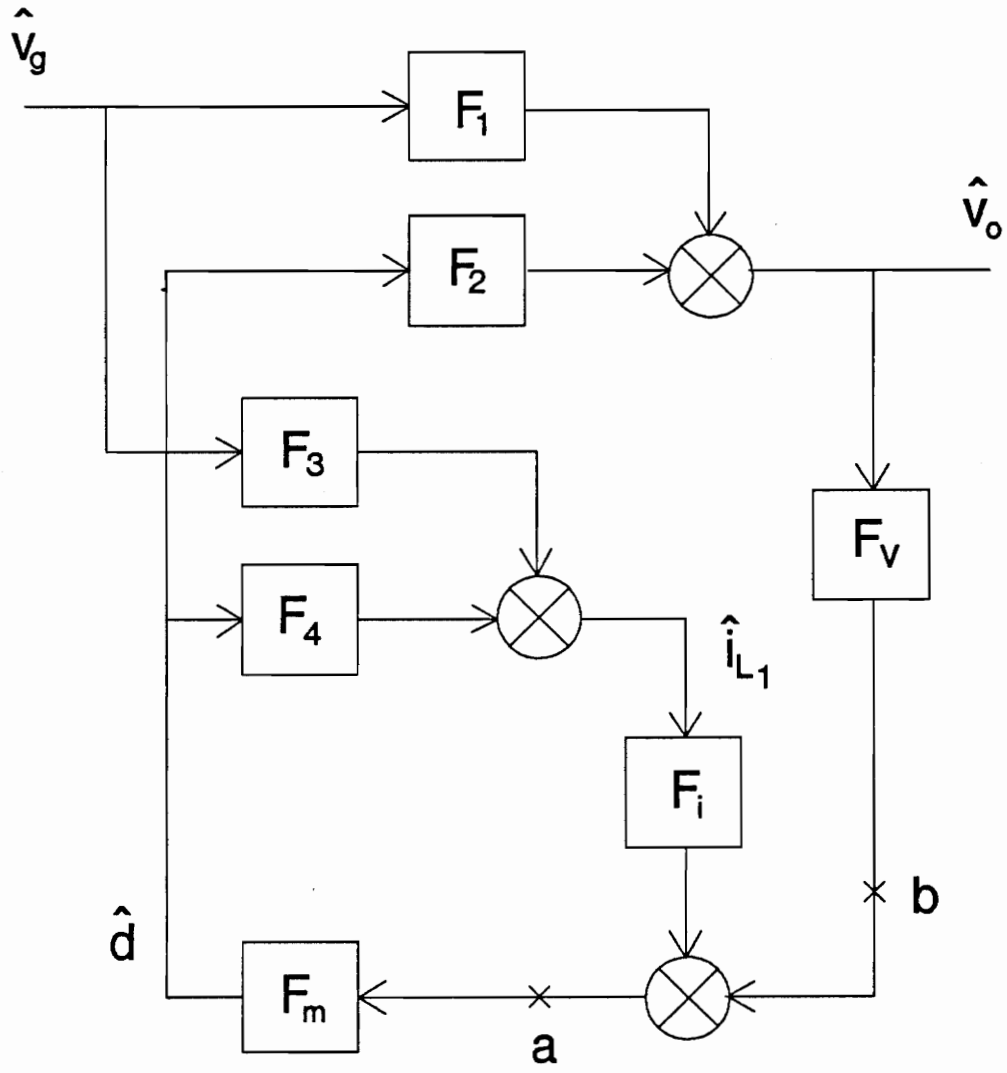


Figure 3.3. Small-Signal Block Diagram of Multi-Loop Controlled Switching Regulator

$$F_1 = \frac{\hat{v}_o}{\hat{v}_g} = \frac{\frac{N_s}{N_p} D(1 + sR_cC)}{s^2LC + s\left[(R_l + R_c)C + \frac{L}{R_L}\right] + 1}$$

$$F_2 = \frac{\hat{v}_o}{\hat{d}} = \frac{\frac{N_s}{N_p} V_g(1 + sR_cC)}{s^2LC + s\left[(R_l + R_c)C + \frac{L}{R_L}\right] + 1}$$

$$F_3 = \frac{\hat{i}_l}{\hat{v}_g} = \frac{\frac{N_s}{N_p}\frac{D}{R}(1 + sR_cC)}{s^2LC + s\left[(R_l + R_c)C + \frac{L}{R_L}\right] + 1}$$

$$F_4 = \frac{\hat{i}_l}{\hat{d}} = \frac{\frac{N_s}{N_p}\frac{V_g}{R}(1 + sR_cC)}{s^2LC + s\left[(R_l + R_c)C + \frac{L}{R_L}\right] + 1}$$

The block labeled F_M represents the small-signal gain of the PWM block. This gain was derived in reference [6] for switching regulators operating at constant frequency as

$$F_M = \frac{2}{T_S} \quad \frac{1}{S_N - S_F + 2S_e} \tag{3.1}$$

where T_S is the period of the switching cycle and S_N and S_F are the slopes of the current-sense waveform during the switch-on and -off times, respectively. S_e is the slope of the external ramp, which is required to avoid instability at duty cycles of more than 50% [6]. The blocks F_i and F_v are the sensing and compensation circuitry for the current and voltage loops, respectively. For CIC control, F_i is simply a constant gain. It was shown in reference [6] that using an integral-lead/lag compensator for F_v allows optimization of the small signal characteristics of the regulator.

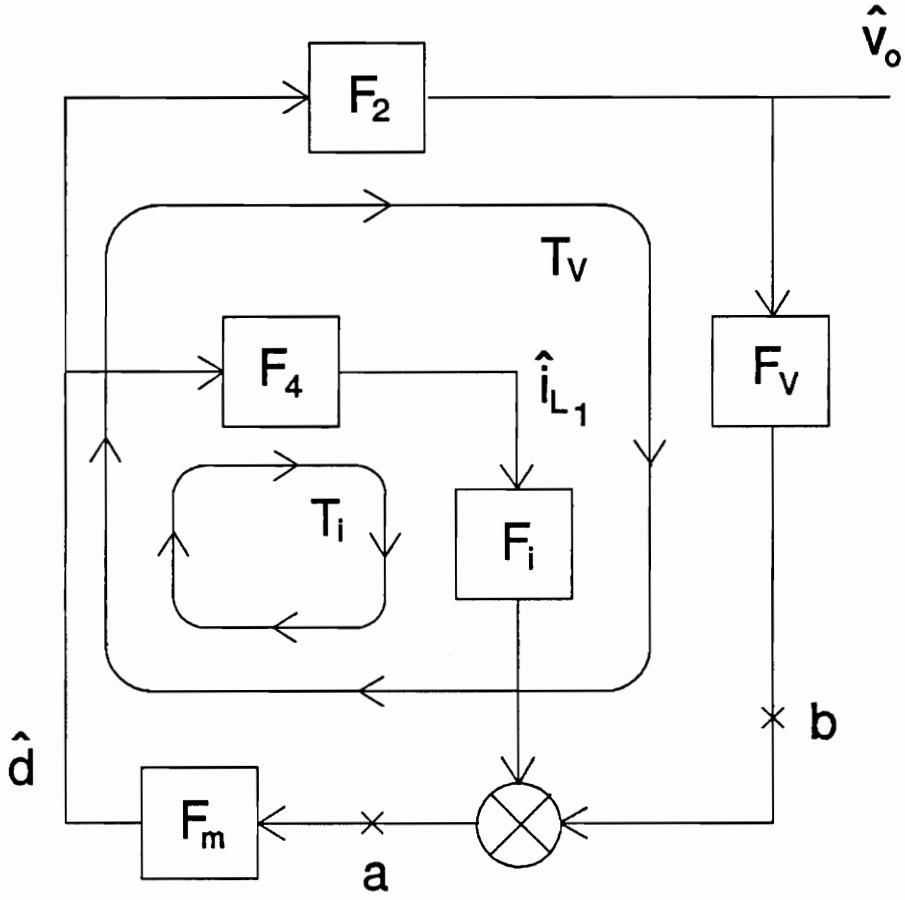


Figure 3.4. Block Diagram for Loop-Gain Analysis

Fig. 3.4 shows the small-signal block diagram for determining the loop-grains of a multi-loop-controlled switching regulator. It is obtained from Fig. 3.3 by setting $\hat{v}_g = 0$ and removing blocks F_1 and F_3. The presence of two separate loops is apparent. The inner loop, composed of blocks F_4, F_i and F_M, represents the current-loop, T_i. The outer loop, made up by blocks F_2 and F_V and F_M, represents the the voltage loop, T_V.

Two useful loop-gains may be defined for the multi-loop controlled regulator. The first, T_1, may be measured by breaking the loops at point "a" on Fig. 3.4. Since this point occurs after the summing junction and is common to both T_i and T_v , T_1 is the vector sum of the loop-gain components, and is expressed as

$$T_1 = T_i + T_v$$

In most implementations of multi-loop control, T_1 must be measured using digital modulation techniques [8]. The second useful loop-gain, T_2 , is measured by breaking the loop at point "b" in Fig. 3.4. This results in measuring the gain of the outer loop while leaving the current-loop closed. Applying basic control theory results in the expression

$$T_2 = \frac{T_v}{1 + T_i}$$

Loop gain T_2 may be measured using conventional analog techniques.

Because loop-gain T_1 is the sum of the loop-gain components T_i and T_v, it clearly displays the magnitude and phase of the larger component. This makes T_1 easy to visualize from plots of T_i and T_v. While the relationships between T_i and T_v are more complex for T_2 than for T_1, T_2 also displays useful information. If T_i is much larger than 0 dB, then

$$T_2 \cong \frac{T_v}{T_i}$$

At frequencies below the crossover of the current-loop, T_2 will show the ratio of the magnitudes of T_i and T_v. The phase of T_2 will be the phase separation between T_i and T_v. When T_i is less than 0 dB,

$$T_2 \cong T_v$$

Summary of Design Procedure

The multi-loop control design procedures presented in reference [6] are summarized below:

1. Choose the current sense gain, F_i, to provide the largest current ramp allowed by comparator limits.

2. Choose the external ramp slope, S_e, to insure that the crossover frequency of T_i is below one-half of the switching frequency at maximum duty cycle.

3. The voltage-loop compensator is

$$F_v = \frac{\omega_m}{s} \frac{(1 + \omega/\omega_z)}{(1 + s/\omega_p)}$$

   Place ω_p to cancel the capacitor ESR zero.

4. The compensator zero, ω_z, determines the settling time of the regulator's step-load response. The settling time specification will determine the minimum frequency of ω_z, which should be placed below the output filter resonance.

5. The integrator gain, ω_M, is the only design parameter remaining to be chosen. This parameter varies the gain, of the voltage loop, and provides control over the point where $T_i = T_v$ (so1 in SCM terminology). This point is the 0 dB crossover frequency of T_2, and is therefore strongly related to the closed-loop performance indices. Stability requires that this point occur well before the crossover of T_i . In addition, as shown in [5], there

is no advantage to increasing the crossover frequency of T_2 higher than the capacitor ESR zero. These two considerations provide an upper limit on the T_2 crossover. The SCM procedures allow calculation of the minimum T_2 crossover frequency required to meet all of the performance specifications. These crossover frequency limitations provide a range of acceptable values for ω_M. The final choice of ω_M is based on a trade-off between additional margins of performance or stability.

3.2 Parallel Power Modules

3.2.1 Analysis and Design of Parallel Power Modules

The use of parallel power modules is a key feature of distributed power systems. The desire to distribute regulated power supplies among the circuit boards of the load requires that each power module contain a complete converter power stage. In the preferred control scheme for distributed parallel modules, each module contains its own current feedback loop while sharing a voltage error signal with all other modules producing the same output voltage [1]. The method of paralleling switching regulators most likely to be used for distributed power systems is shown in Fig. 3.5. This differs from the method of paralleling power modules shown in Fig. 3.6, in which a module contains the power switches and filter inductor of a converter power stage, but the output-filter capacitor is a separate and fixed component. This type of arrangement is typically used for high-power applications and is discussed in detail in references [5] and [9]. While the two configurations result in systems with different small-signal characteristics, they share a similar topology. If the modules of Fig. 3.5 have identical com-

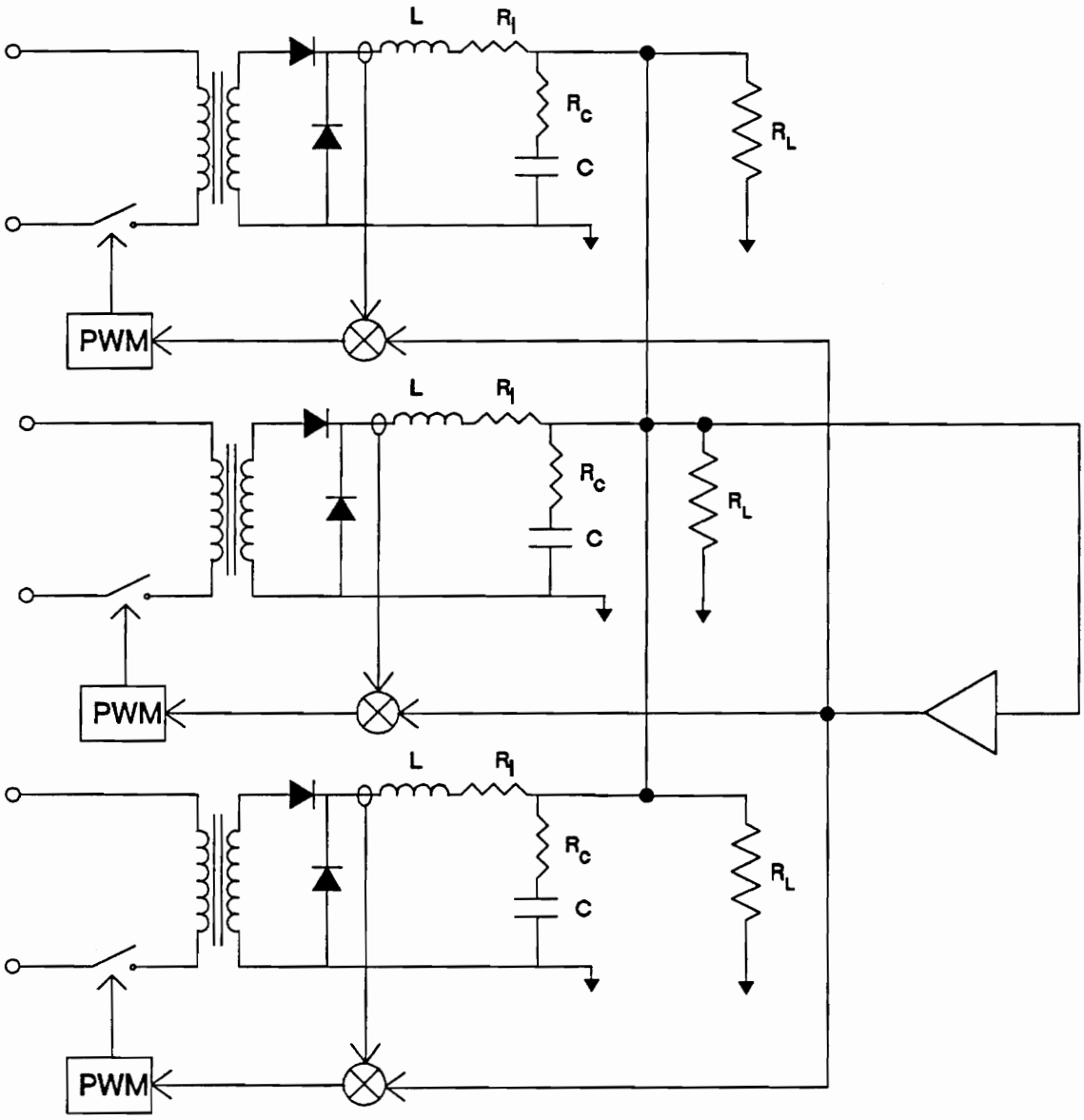


Figure 3.5. Parallel Modules for Distributed Power Systems

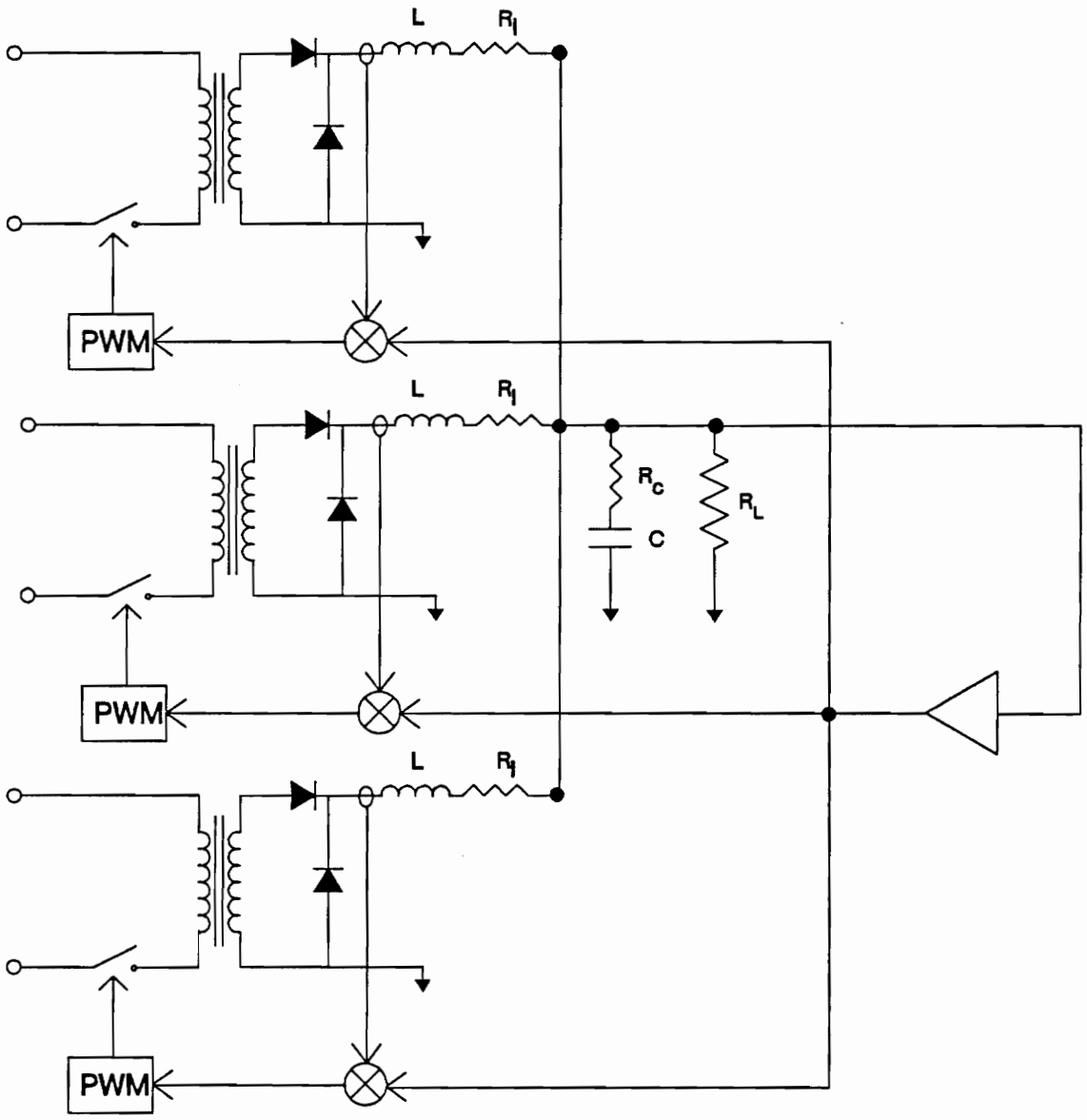


Figure 3.6. Parallel Modules for High Power Applications

ponents, then an equivalent circuit for the paralleled converter power stages is shown in Fig. 3.7, where k is the number of modules in Fig. 3.5.

Note that the circuit topology in Fig. 3.7 is identical to that in Fig. 3.6. The only difference between the circuits of 3.6 and 3.7 is that, in the latter, the values of components C, R_c and R* are dependent on the number of modules. This allows the small-signal analysis of the circuit of Fig. 3.6 developed in reference [5] to be easily extended to cover the case at hand.

Fig. 3.8 shows the small-signal block diagram for a system with k parallel buck converter modules. The blocks F_M, F_i and F_v remain unchanged from the single module case. The blocks F_1-F_6 represent the transfer-functions of the paralleled power stages. Their definitions are as follows:

$$F_1 = \text{Input-to-Output Transfer Function} = \frac{\hat{v}_o}{\hat{v}_{gi}}$$

$$F_2 = \text{Duty-Cycle-to-Output Transfer Function} = \frac{\hat{v}_o}{\hat{d}_i}$$

$$F_3 = \text{Input-to-Inductor-Current Transfer Function} = \frac{\hat{i}_{li}}{\hat{v}_i}$$

$$F_4 = \text{Duty-Cycle-to-Inductor-Current Transfer Function} = \frac{\hat{i}_{li}}{\hat{d}_i}$$

$$F_5 = \text{Duty-Cycle-to-Inductor-Current Transfer Function} = \frac{\hat{i}_{li}}{\hat{d}_j}$$

$$F_6 = \text{Input-to-Inductor-Current Transfer Function} = \frac{\hat{i}_{li}}{\hat{v}_{gj}}$$

The small-signal characteristics of the paralleled power converters of Fig. 3.6 were derived in reference [5] using state-space averaging techniques. The general case of k parallel modules was considered, which yielded a k+1 order system. Once the state equations of the system had been averaged, perturbed and linearized, n^{th} order matrix analysis techniques were utilized to obtain the transfer functions of blocks F_1-F_6. Since the parallel-module system of Fig. 3.5 is topologically equivalent to the system of Fig. 3.6, the state-equations will be identical in

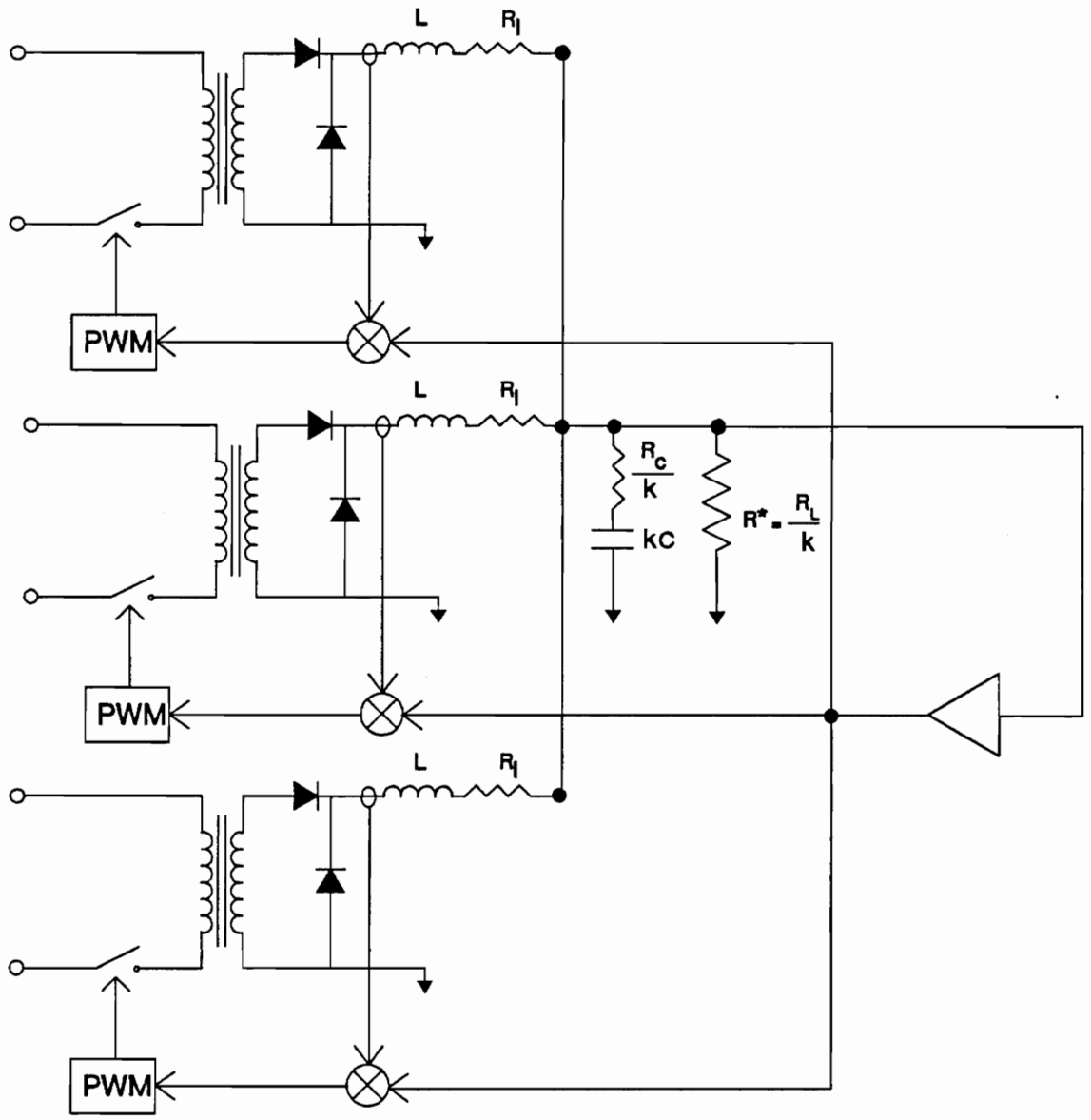


Figure 3.7. Equivalent Circuit for Fig. 3.5

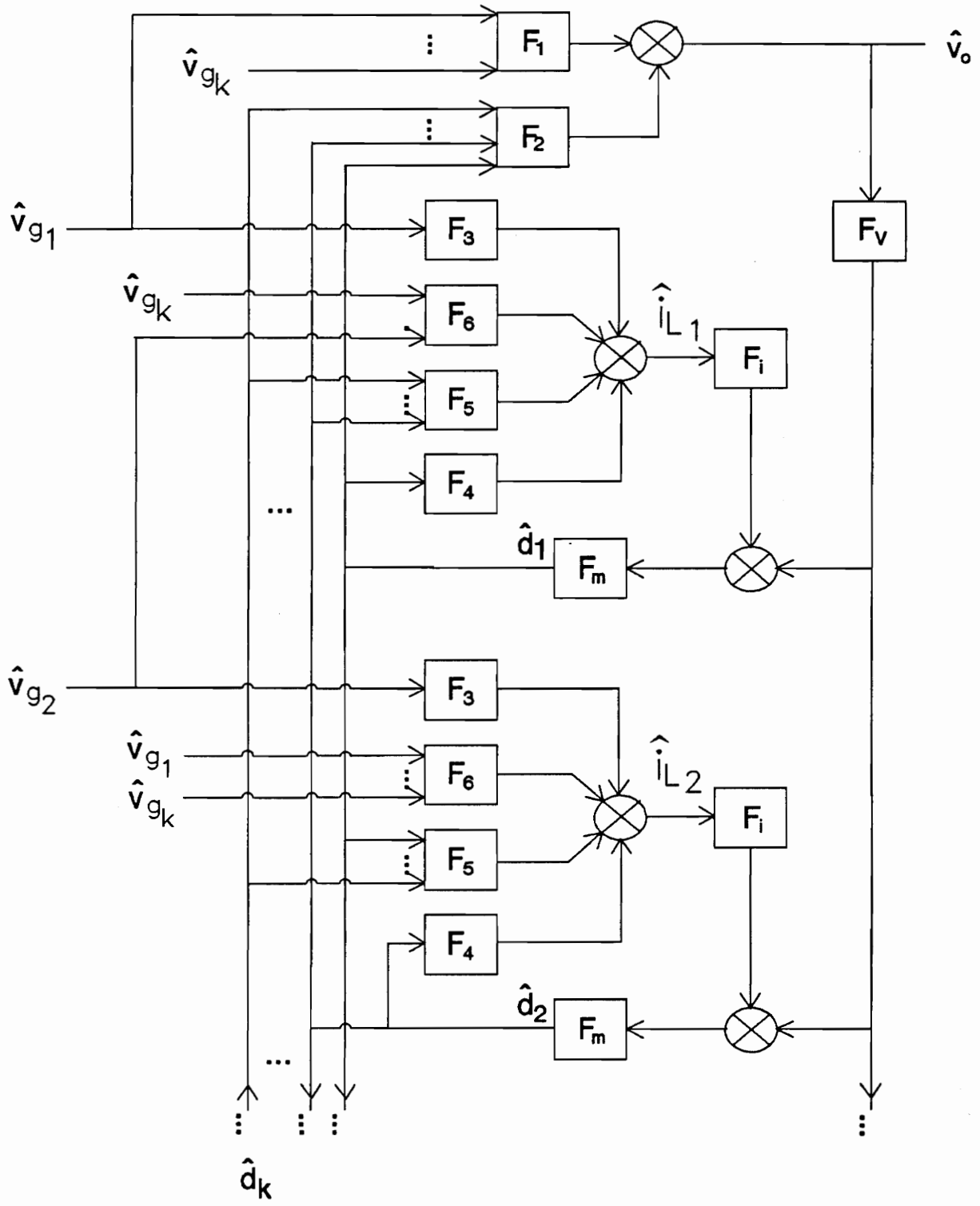


Figure 3.8. Small Signal Block Diagram for k Parallel Modules

form, and differ only by the factors of k or $\frac{1}{k}$ that appear in the circuit of Fig. 3.7. Since the analysis presented in reference [5] is lengthy it will not be replicated here. If the substitutions of C = kC, $R_C = \frac{R_C}{k}$, and $R_L = \frac{R_L}{k} = R^*$ are made into the equations of [5], the following results for F_1 through F_6 are obtained for the parallel converters of Fig. 3.5.

$$F_1 = \frac{\hat{v}_o}{\hat{v}_{gi}} = \frac{\frac{N_s}{N_p}\frac{D_i}{k}(1 + sR_cC)}{\left(s^2LC + s\left[(R_l + R_c)C + \frac{L}{kR^*}\right] + 1\right)}$$

$$F_2 = \frac{\hat{v}_o}{\hat{d}_i} = \frac{\frac{N_s}{N_p}\frac{V_{gi}}{k}(1 + sR_cC)}{\left(s^2LC + s\left[(R_l + R_c)C + \frac{L}{kR^*}\right] + 1\right)}$$

$$F_3 = \frac{\hat{i}_{li}}{\hat{v}_{gi}} = \frac{\frac{N_s}{N_p}\frac{D_i}{R_l}\left(\frac{k-1}{k}\right)\left(s^2LC\left(\frac{k}{k-1}\right) + s\left[R_e''C + \frac{L}{kR^*}\right]\left(\frac{k}{k-1}\right) + 1\right)}{\left(1 + \frac{sL}{R_l}\right)\left(s^2LC + s\left[(R_l + R_c)C + \frac{L}{kR^*}\right] + 1\right)}$$

$$F_4 = \frac{\hat{i}_{li}}{\hat{d}_i} = \frac{\frac{N_s}{N_p}\frac{V_{gi}}{R_l}\left(\frac{k-1}{k}\right)\left(s^2LC\left(\frac{k}{k-1}\right) + s\left[R_e''C + \frac{L}{kR^*}\right]\left(\frac{k}{k-1}\right) + 1\right)}{\left(1 + \frac{sL}{R_l}\right)\left(s^2LC + s\left[(R_l + R_c)C + \frac{L}{kR^*}\right] + 1\right)}$$

$$F_5 = \frac{\hat{i}_{li}}{\hat{d}_j} = \frac{\frac{-N_s}{N_p}\frac{V_{gj}}{R_l}\left(\frac{1}{k}\right)(1 + sR_cC)}{\left(1 + \frac{sL}{R_l}\right)\left(s^2LC + s\left[(R_l + R_c)C + \frac{L}{kR^*}\right] + 1\right)}$$

$$F_6 = \frac{\hat{i}_{li}}{\hat{v}_{gj}} = \frac{\frac{-N_s}{N_p}\frac{D_j}{R_l}\left(\frac{1}{k}\right)(1 + sR_cC)}{\left(1 + \frac{sL}{R_l}\right)\left(s^2LC + s\left[(R_l + R_c)C + \frac{L}{kR^*}\right] + 1\right)}$$

Where $R_e'' = R_l + \left(\frac{k-1}{k}\right)R_c$

It was shown in reference [5] that these results are independent of the large-signal switching sequence between modules.

Loop-Gains of Parallel-Module Regulators

Fig. 3.9 shows the small-signal block diagram used to determine the loop-gains of a parallel-module switching regulator system. This block diagram is obtained by setting all of the $\hat{v}_g$'s in Fig. 3.8 to zero and removing blocks F_1, F_3 and F_6. Note that for the parallel module regulator, there is no point corresponding to "a" in the single module block diagram (Fig. 3.4). This is because there is no physical point where all loops are summed together. Nor does there exist any one point that may be broken to measure the current-loop-gain of the system, since each module has its own current loop. While there are no loop-gains which physically correspond to T_1 or T_i for the parallel module system, there is a loop-gain which corresponds to T_2. This loop-gain is measured by breaking the voltage loop at point "b" and measuring the response of the system with all current loops remaining closed. This loop-gain may be expressed analytically as

$$T_2 = \frac{T_v'}{1 + F(s)}$$

where F(s) is an analytical equivalent of the current-loop gain, T_i. An expression for T_2 was derived from the block diagram in Fig. 3.9 [5]. It is:

$$T_2 = \frac{kF_M F_2 F_v}{1 + F_M F_i [F_4 + (k-1)F_5]}$$

The above expression was derived under the assumption that all modules were operating at the same DC input voltage level. This assumption was necessary to make a general analysis tractable [5]. Evaluating the expression for F(s) with the transfer functions presented above yields:

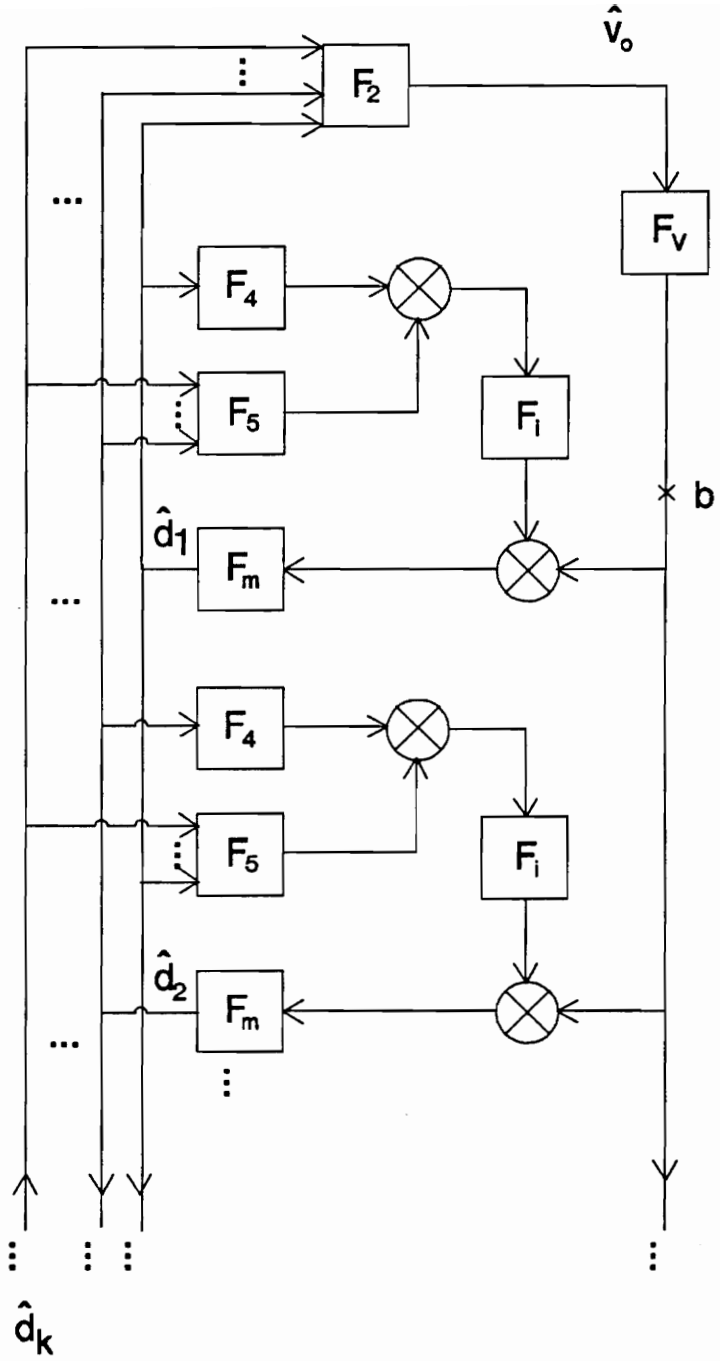


Figure 3.9. Small-Signal Block Diagram for Parallel Module Loop-Gain Analysis

$$F(s) = \frac{F_m F_i \frac{N_s}{N_p} \frac{V_g}{R_l} \left(s^2 LC + s\left(R_l C + \frac{L}{kR^*} \right) \right)}{\left(1 + \frac{sL}{R_l} \right) \left(s^2 LC + s\left[(R_l + R_c)C + \frac{L}{kR^*} + 1 \right] \right.}$$

If it is assumed that $R_l << kR^*$, then F(s) may be approximated as

$$F(s) = \frac{F_m F_i \frac{N_s}{N_p} \frac{V_g}{R_l} \left(s^2 LC + s\left(R_l C + \frac{L}{kR^*} \right) + \frac{R_l}{kR^*} \right)}{\left(1 + \frac{sL}{R_l} \right) \left(s^2 LC + s\left[(R_l + R_c)C + \frac{L}{kR^*} \right] + 1 \right)}$$

which may be factored and simplified to

$$F(s) = \frac{F_m F_i \frac{N_s}{N_p} \frac{V_g}{kR^*} (1 + skR^*C)}{\left(s^2 LC + s\left[(R_l + R_c)C + \frac{L}{kR^*} \right] + 1 \right)}$$

The resulting expression for T_2 is:

$$T_2 = \frac{\frac{F_m F_v \frac{N_s}{N_p} V_g (1 + sR_cC)}{\left(s^2 LC + s\left[(R_l + R_c)C + \frac{L}{kR^*} \right] + 1 \right)}}{1 + \left[\frac{F_m F_i \frac{N_s}{N_p} \frac{V_g}{kR^*} (1 + skR^*C)}{\left(s^2 LC + s\left[(R_l + R_c)C + \frac{L}{kR^*} \right] + 1 \right)} \right]} \qquad (3.2)$$

Substituting back in for $R^* = \frac{R_L}{k}$ gives T_2 as

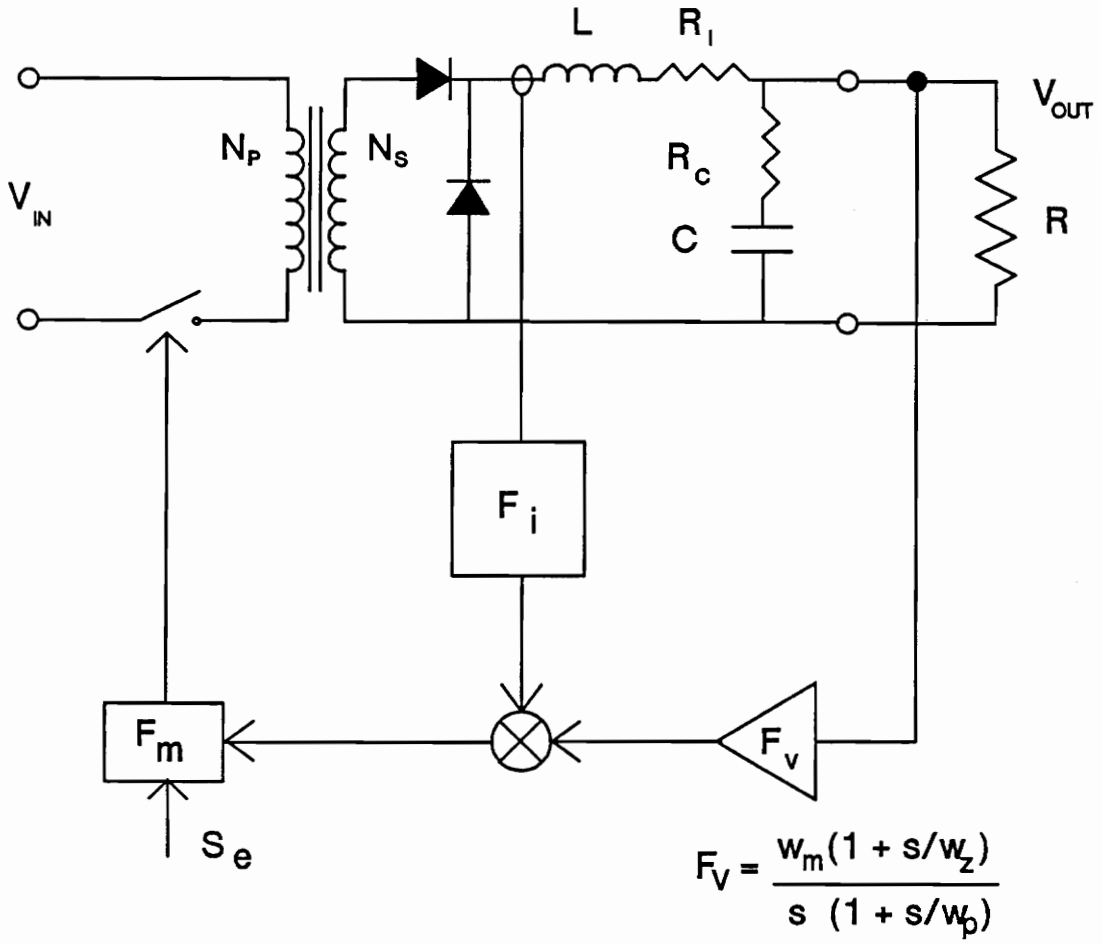
$$T_2 = \frac{\dfrac{F_m F_v \dfrac{N_s}{N_p} V_g (1 + sR_cC)}{\left(s^2LC + s\left[(R_l + R_c)C + \dfrac{L}{R_L} \right] + 1 \right)}}{1 + \left[\dfrac{F_m F_i \dfrac{N_s}{N_p} \dfrac{V_g}{R_L} (1 + R_LC)}{\left(s^2LC + s\left[(R_l + R_c)C + \dfrac{L}{R_L} \right] + 1 \right)} \right]}$$

Note that this expression is identical to T_2 for a single module. Since the loop-gain characteristics of the parallel module system are nearly identical to those of a single regulator, the control design for the parallel module system is also the same. This allows the closed-loop stability and performance of the *system* to be optimized by optimizing the control for a *single module*, and then paralleling modules as in Fig. 3.5. Since the above expression for T_2 is independent of k, there is no theoretical limit on the number of modules which may be placed in parallel. This allows systems of greatly varying power level to be configured simply by connecting the appropriate number of modules together, without modification of the control design.

Design Example

The design procedures outlined at the beginning of the chapter were used to design the control-loops for a single load converter. The load converter uses a Forward (PWM) topology to step down the 48V intermediate bus to 5V. Fig. 3.10 shows a block diagram of the load converter and its control circuitry. The parameter values for the power stage are provided in the figure as well. The following figures compare the small-signal response of three parallel load converters to the response of a single load converter.

Design Verification



V_{IN} =48V (38 - 54)	Ns/Np = 0.33
V_{OUT} = 5V	L = 1uH
P_{OUT} = 200W max	R_l = 0.01 ohm
F_S = 500kHz	C = 164uF
Inductor in CCM	R_C = 0.005 ohm

Note: Transformer Reset Circuitry Omitted For Clarity

Figure 3.10. Load Converter Power Stage/Control Loops

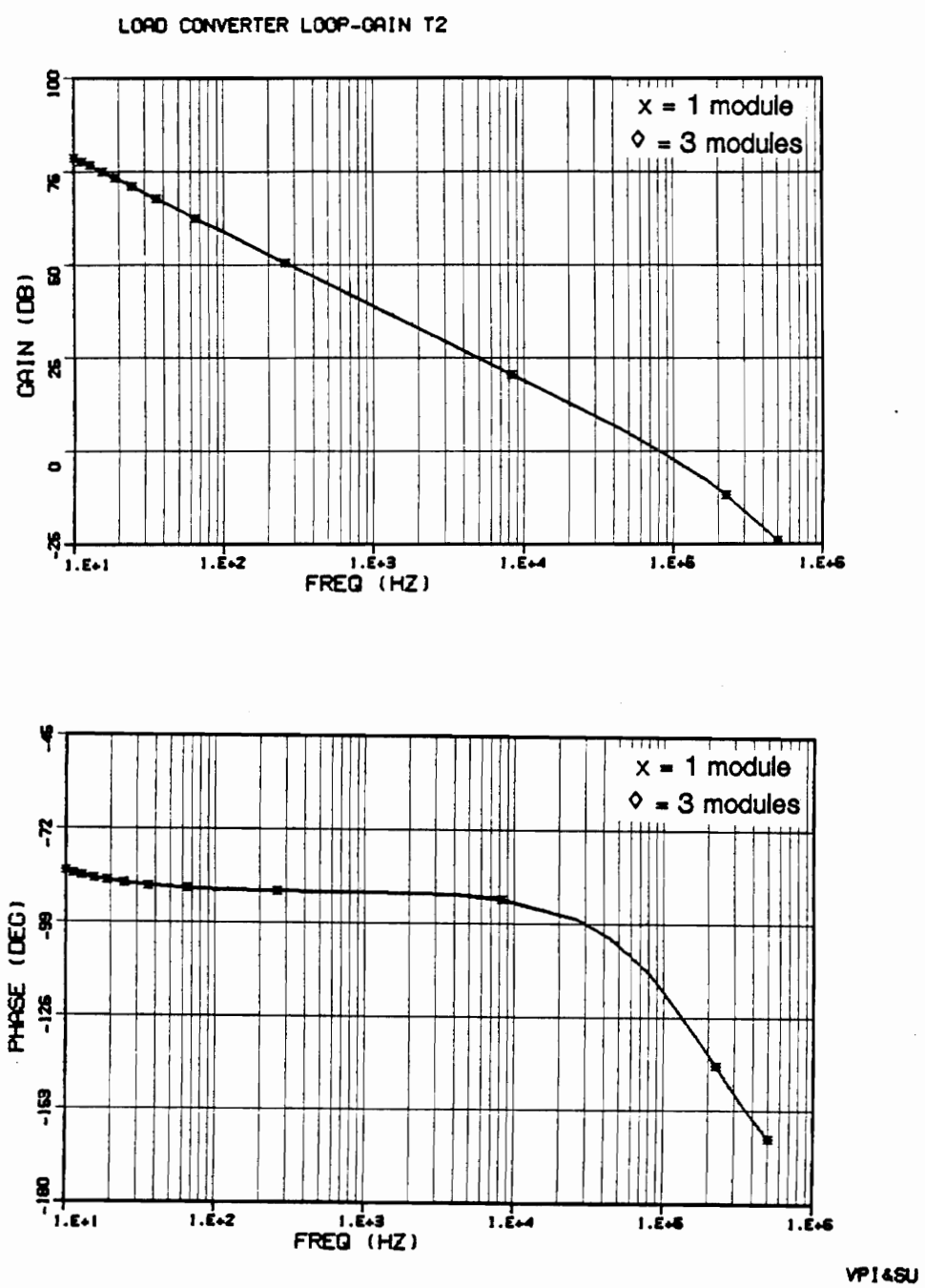


Figure 3.11. Comparison Between Single and Parallel Module Systems-Loop Gain T_2

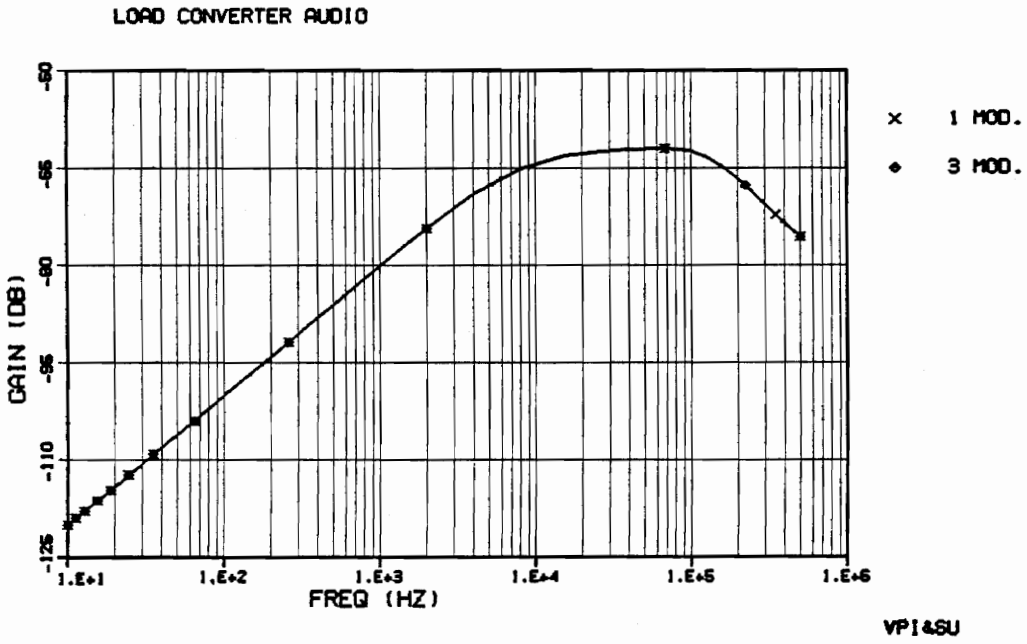
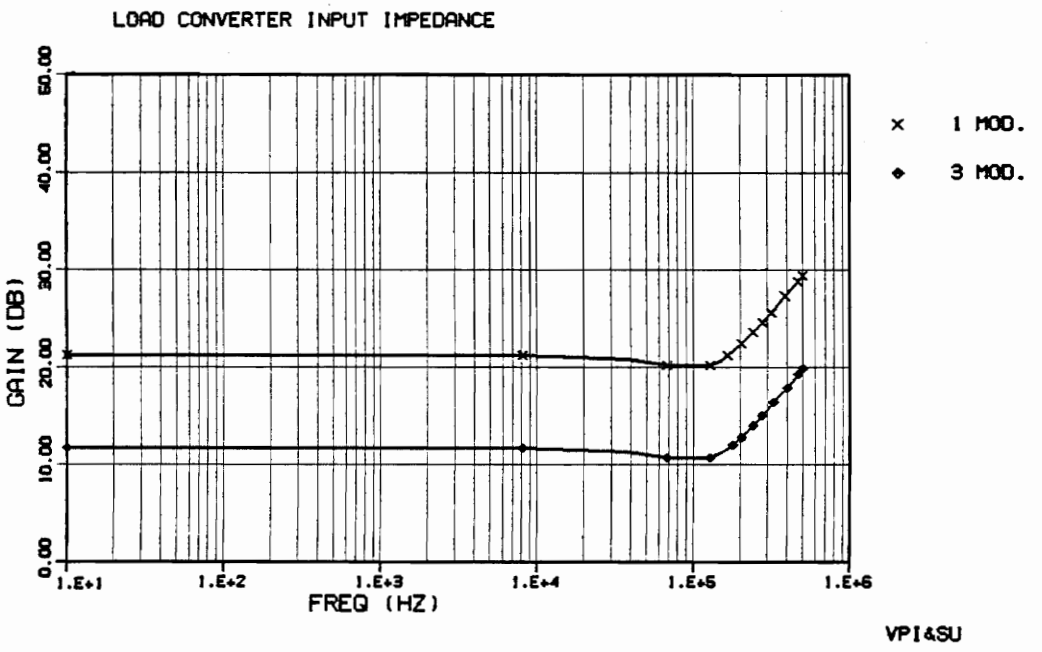


Figure 3.12. Comparison Between Single and Multi-Module Systems - Audio



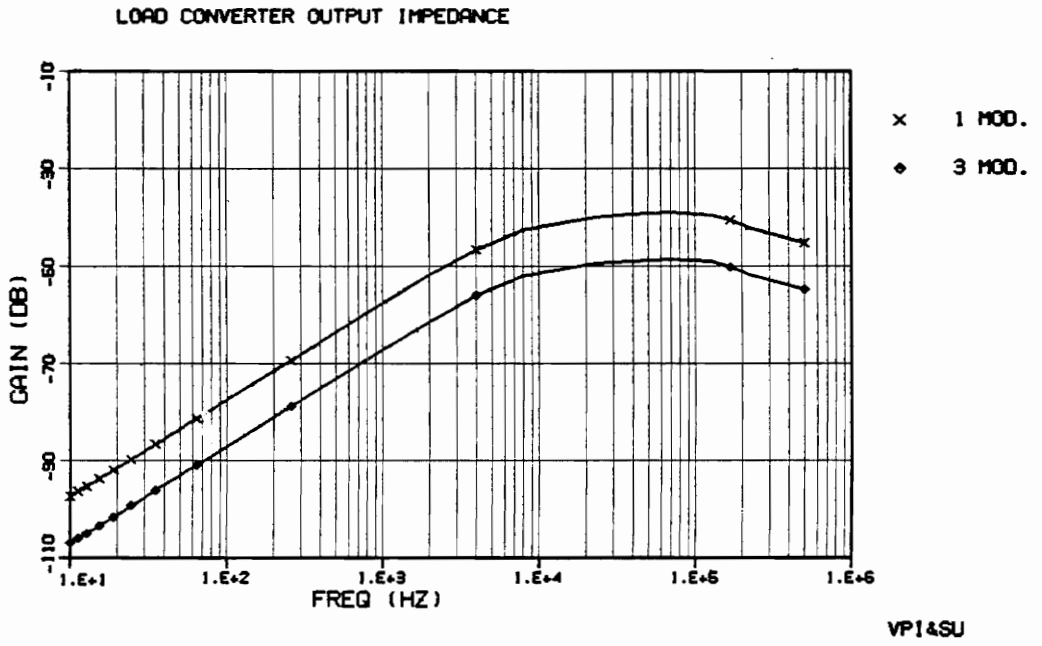


Figure 3.13. Single and Multi Module Systems - Input and Output Impedances

Fig. 3.11 shows the loop-gain T_2 for both a single module and three modules in parallel, where in both cases the system is operating at full power. Note that the loop-gain of the multi-module system is identical to that of the single module. Fig. 3.12 shows the audio for both the single and multi-module systems. Note that the two curves are identical. Fig. 3.13 shows the input and output impedance for the two systems. Note that the shape of the single-module impedance is identical to that of the multi-module impedance for both Z_i and Z_o. The 10dB separation between the curves is the expected result of placing three single-module regulators in parallel.

3.2.2 Discussion of N + 1 Redundancy

One important motivation for the use of parallel modules is that a redundant module may be added to the system, allowing continued operation even if one module fails. Although it was shown that the loop-gain characteristics are identical for the single and multi-module systems under normal conditions, the behavior of the system under failure mode conditions remains to be seen. Equation 3.2 gives the expression for loop-gain T_2 for one such situation. This expression may be used to predict the stability of the system after the failure and removal of one or more modules. Note that k, the number of modules, is always multiplied by R*, the load resistance. This allows the conclusion that the effect of the failure and removal of a redundant module is identical to an equivalent change in load. Fig. 3.14 shows loop-gain T_2 for such a situation for the three module system considered above. The upper magnitude (and lower phase) curve is T_2 for the system operating with 3 modules at 400W. The failure and removal of one module results in a two-module system operating at 400W. The effect on T_2 is to lower the low-frequency magnitude and boost the phase, an effect identical to that for an increase in load. A proportional decrease in load to 267W makes the loop gain of the two-module system identical to that of the three-module system at 400W.

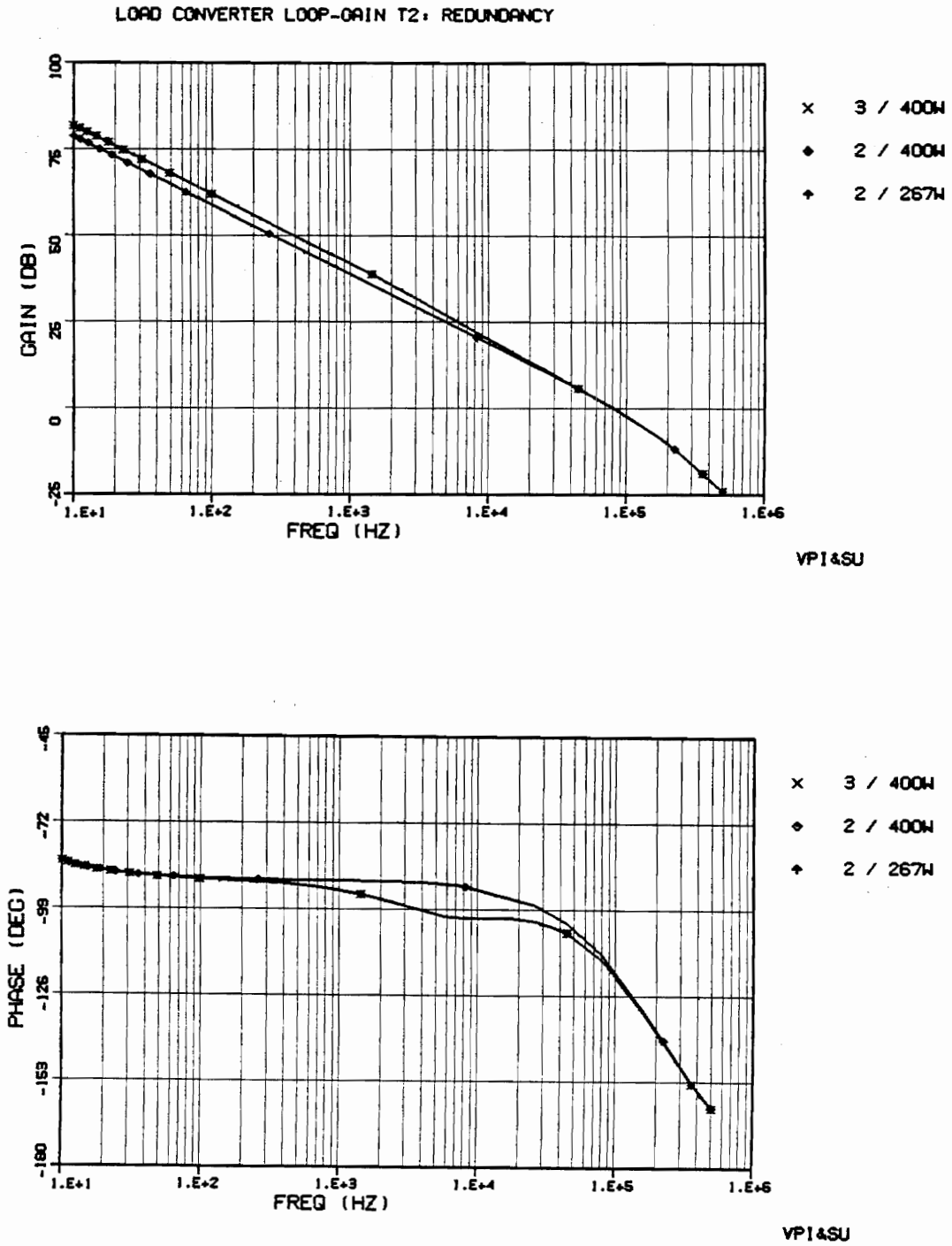


Figure 3.14. Loop-Gain T_2 for N + 1 Redundant System

Another important issue is the stability of the system with the failed module still connected to the system. One such case occurs when the power switch of one module fails in an open-circuit manner. The module's inductor current will fall to zero and the inductor will no longer have an effect on the system. However, the output filter capacitor will still be connected to the output of the parallel module system. This situation corresponds exactly to the removal of one module from the system shown in Fig. 3.6. It is shown in reference [10] that the stability of the system in Fig. 3.6 increases as the number of modules decreases, although performance indices will be degraded. Therefore this particular failure mode poses no threat to the stability of the system. A more thorough study of the DPS under failure-mode conditions is the subject of continuing research.

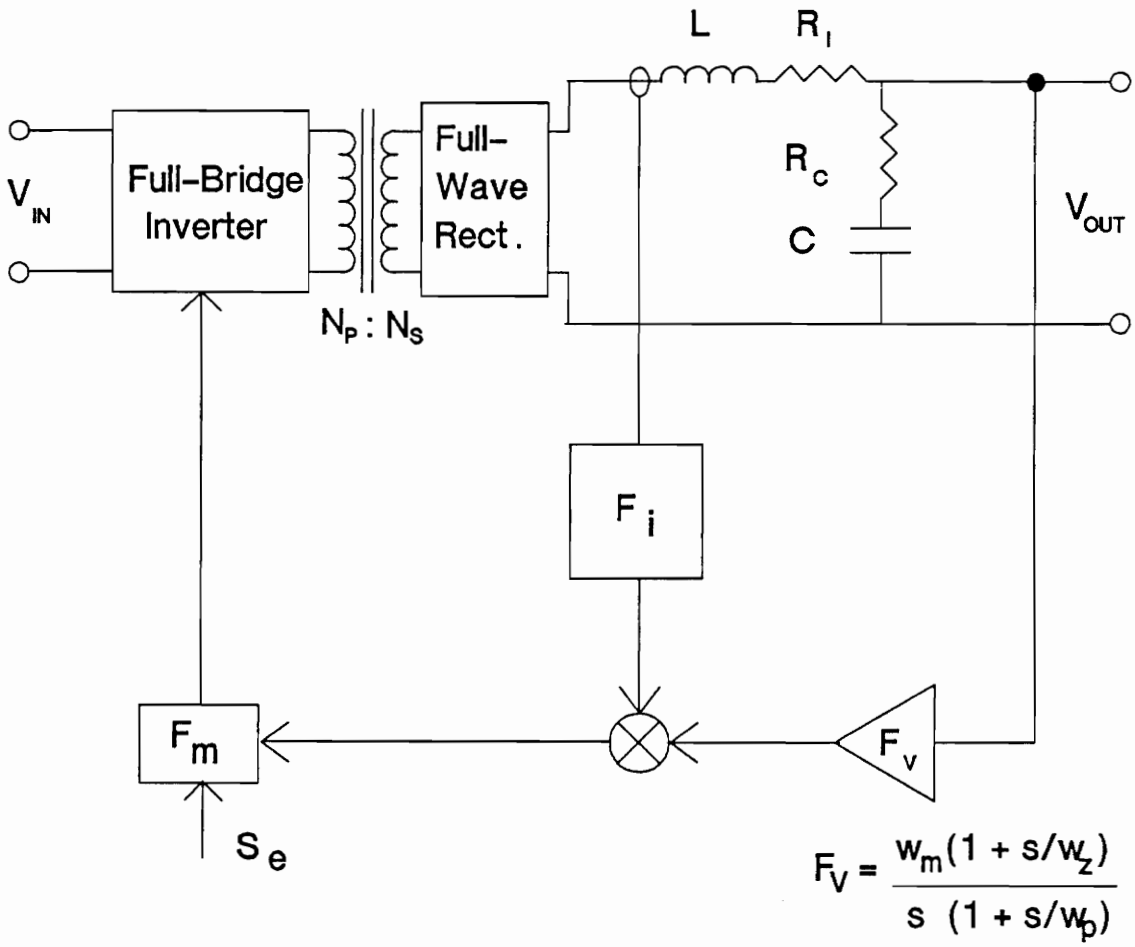
Chapter 4

ANALYSIS AND DESIGN OF CASCADED SWITCHING REGULATORS

The previous chapter discussed the control design of parallel current-mode-controlled switching regulator modules, using the load converter with a resistive load as an example. In this chapter, the effect of cascading switching regulators will be considered. When two switching regulators or groups of parallel modules are operated in cascade, undesirable interaction arises from two sources: the non-zero output impedance of the line conditioner affects the control loops of the load converters and the non-resistive nature of the load converter's input impedance affects the control loops of the line conditioner. Since the first case is very similar to the well-documented [11-13] subject of regulator / input filter interaction, it will be covered only briefly here.

The primary concern of this chapter is the effect of the second stage of switching regulators on the line conditioner. The input impedance of the load converters displays a negative dynamic resistance characteristic, which can greatly alter the characteristics of the line conditioner. An unterminated modeling approach is used to correctly account for the effects of the load converter on the line conditioner. It is found that the negative dynamic resistance of the load converter induces right-half-plane (RHP) poles in the line conditioner's loop gains. The loop-gain characteristics of the line conditioner are discussed and the stability of the line conditioner is analyzed using fundamental loop-gain analysis. Insight gained from the stability analysis is used to suggest a design approach for the control of the line conditioner.

A buck-derived full bridge converter with current injection control is used for the line conditioner. Fig. 4.1 shows a simplified circuit schematic and control block diagram as well as the parameter values for the power stage.



V_{IN} = 270V (125 - 475)
V_{OUT} = 48V
P_{OUT} = 650W max
Ripple Freq. = 250kHz
Inductor in CCM

Ns/Np = 0.533
L = 50uH
R_l = 0.01 ohm
C = 50uF
R_c = 0.15 ohm

Figure 4.1. Line Conditioner Power Stage/Control Loops

4.1 Modeling

Because the behavior of a switching regulator depends heavily upon the characteristics of its load, care must be taken when analyzing a regulator in the presence of a non-resistive load. In this section, an unterminated model is presented which forces the user to correctly account for the effects of load characteristics on the regulator. The load of a switching regulator is characterized by two quantities: the amount of DC current drawn by the load at steady-state (the DC power level) and the response of the terminal voltage of the load to a small-signal sinusoidal disturbance in the terminal current (load impedance).

In most practical situations, the load impedance becomes resistive at low frequencies and the value of this resistance is determined by the DC power drawn by the load. It is common practice to approximate the load by a resistor, making the effects of DC power level indistinguishable from the effects of load impedance. However, in a distributed power system, the load impedance seen by the line conditioner has the characteristic of a resistor with a negative value. In this case the resistive load approximation is not valid, so the DC power level and load impedance should be considered separately. Fig. 4.2 shows a small-signal linear equivalent circuit model for an unterminated isolated-buck converter (see Fig. 4.1). The model was derived using the state-space averaging technique [6] and is very similar to the canonical circuit model presented in reference [7]. One difference is that both the voltages and currents at the terminals of the regulator are treated as input variables. In order to avoid confusion with regard to source and load characteristics, the model is used for small-signal analysis only, and no attempt is made to use the model for DC analysis. Information about the DC operating point of the regulator is contained within the dependent sources of the model, and should be considered an input parameter to the model. Constructing the small-signal model in this way forces the user to recognize the distinction between DC and small-signal quantities. As discussed in Chapter 2, the unterminated model may be used to determine the effect

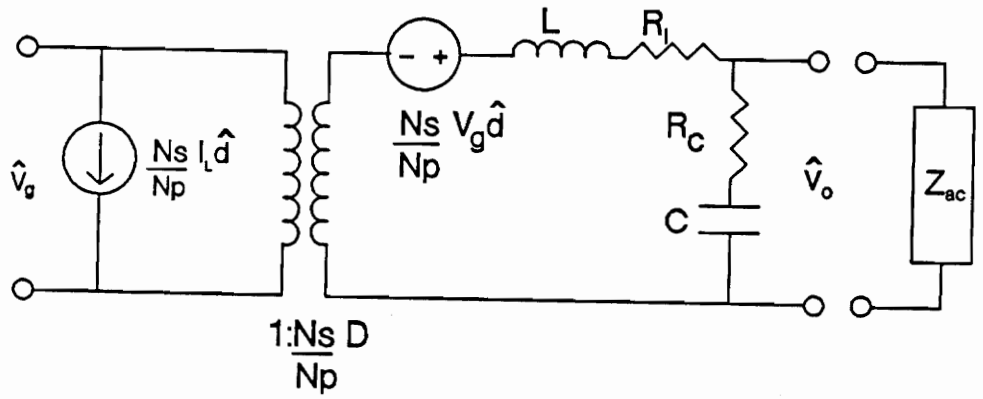


Figure 4.2. Small-Signal Equivalent Circuit of Line Conditioner

of external impedances on the converter's behavior by rewriting the circuit equations with the appropriate impedances connected to its terminals.

4.2 Analysis and Design of the Line Conditioner

4.2.1 Line Conditioner Loop-Gain Analysis

In order to gain insight into the effects of a non-resistive load on the line conditioner's behavior, a load impedance Z_{ac} is connected to the unterminated model. An ideal source impedance will be assumed. *It is very important to note that the dependent sources in the model are affected only by DC operating conditions, and are independent of load dynamics. Similarly, Z_{ac} represents the impedance of the load, and the low frequency value of Z_{ac} is not necessarily the same as the DC power drawn from the converter.* Having made this distinction, the load-terminated small-signal model may be used to derive power stage transfer functions. If the converter is operated from an ideal voltage source, the power-stage control transfer functions are:

$$\frac{\hat{i}_l}{\hat{d}} = \frac{\frac{N_s}{N_p}\frac{V_g}{Z_{ac}}(1 + sZ_{ac}C)}{s^2LC + s\left[(R_l + R_c)C + \frac{L}{Z_{ac}}\right] + 1} \tag{4.1}$$

$$\frac{\hat{v}_o}{\hat{d}} = \frac{\frac{N_s}{N_p}V_g(1 + sR_cC)}{s^2LC + s\left[(R_l + R_c)C + \frac{L}{Z_{ac}}\right] + 1}$$

The above equations reveal that when a buck derived regulator is operated from an ideal voltage source, the only external conditions that influence the regulator are the DC input voltage (V_g) and the load impedance (Z_{ac}). If current-injection-control is used, the loop-gain components T_i and T_v of the line conditioner are:

$$T_i = F_m F_i \frac{\hat{i}_l}{\hat{d}} = \frac{F_m F_i \frac{N_s}{N_p}\frac{V_g}{Z_{ac}}(1 + sZ_{ac}C)}{s^2LC + s\left[(R_l + R_c)C + \frac{L}{Z_{ac}}\right] + 1}$$

$$T_v = F_m F_v \frac{\hat{V}_o}{\hat{d}} = F_m \frac{\omega_m\left(1 + \frac{s}{\omega_z}\right)}{s\left(1 + \frac{s}{\omega_p}\right)} \frac{\frac{N_s}{N_p} V_g (1 + sR_cC)}{s^2LC + s\left[(R_l + R_c)C + \frac{L}{Z_{ac}}\right] + 1}$$

where F_i is the gain of the curent sensing circuit, F_m is the small-signal gain of the PWM block and F_v an integral / lead-lag compensator [6]. If ω_p is chosen to cancel the capacitor ESR zero, then loop-gain T_1 is given by:

$$T_1 = T_i + T_v = \frac{\frac{N_s}{N_p} V_g F_m \left(s^2 F_i C + s\left(\frac{F_i}{Z_{ac}} + \frac{\omega_m}{\omega_z}\right) + \omega_m\right)}{s\left(s^2LC + s\left[(R_l + R_c)C + \frac{L}{Z_{ac}}\right] + 1\right)}$$

The loop-gain T_2 is given by

$$T_2 = \frac{T_v}{1 + T_i} = \frac{F_m \omega_m\left(1 + \frac{s}{\omega_z}\right)\frac{N_s}{N_p} V_g}{s\left(s^2LC + s\left[\left(R_l + R_c + \frac{N_s}{N_p} V_g F_m F_i\right)C + \frac{L}{Z_{ac}}\right] + \left(1 + \frac{\frac{N_s}{N_p} V_g F_m F_i}{Z_{ac}}\right)\right)}$$

While the above equations provide intuitive insight into the effects of a given Z_{ac} on the line conditioner, detailed analysis may prove intractable if Z_{ac} is a high-order function of s.

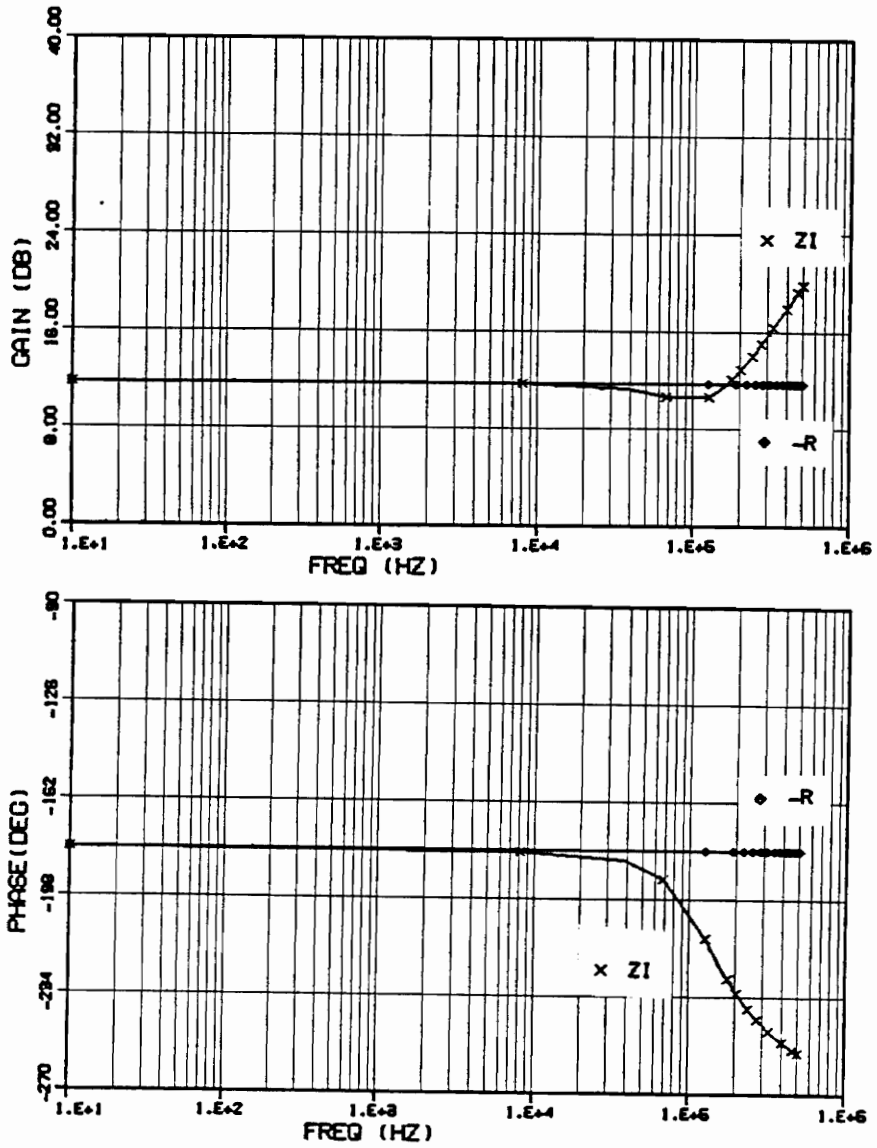


Figure 4.3. Comparison Between Load Converter Input Impedance and a Negative Resistance

If a switching regulator is assumed to be 100% efficient, then its input power must equal its output power. This causes switching regulators to draw a constant amount of power for any steady-state load condition. If the input voltage to the regulator decreases, the input current has to increase to maintain the fixed power level. This results in an input impedance with a negative dynamic resistance characteristic at low frequencies. Approximating the load converters' input impedance as a simple negative resistance makes the above equations very useful for determining the primary effects of placing regulators in cascade. Fig. 4.3 compares the magnitude and phase of the input impedance of three load converters (see Fig. 3.10) to a negative resistance with the same low frequency magnitude. The negative resistance is a very good approximation to the input impedance of the load converters below the crossover frequencies of the load converter's loop-gains. As long as the line conditioner's loop-gains cross 0 dB before those of the load converter, the approximation should be valid. While this approximation is used for analysis purposes, all frequency response simulations presented here were generated using realistic converter models.

In order to use the negative resistance approximation, $-R_{ac}$ is substituted for Z_{ac} in the previous equations. The resulting loop-gain components T_i and T_v are:

$$T_I = \frac{\frac{K_3}{-R_{ac}}(1 + s(-R_{ac})C)}{s^2LC + s\left[(R_I + R_C)C + \frac{L}{-R_{ac}}\right] + 1} \tag{4.2}$$

$$T_V = \frac{F_m \omega_m \left(1 + \frac{s}{\omega_z}\right) \frac{N_s}{N_p} V_g}{s\left(s^2LC + s\left[(R_I + R_C)C + \frac{L}{-R_{ac}}\right] + 1\right)}$$

Where $K_3 = F_M F_i \frac{N_s}{N_p} V_g$. The symbol K_3 is chosen to be consistent with the notation used in reference [6]. Note that $-R_{ac}$ appears in the damping term of the quadratic equation in the denominator of both T_i and T_v. If the magnitude of $\frac{L}{-R_{ac}}$ is large enough to make the entire first-order coefficient negative, the loop-gain components will have right-half-plane (RHP) poles. In addition, $-R_{ac}$ appears twice in the numerator of T_i, causing T_i to have a RHP zero and $-180°$ phase at low frequencies.

The loop gain

$$T_1 = T_i + T_v = \frac{\frac{N_s}{N_p} V_g F_m \left(s^2 F_i C + s\left(\frac{F_i}{-R_{ac}} + \frac{\omega_m}{\omega_z} \right) + \omega_m \right)}{s\left(s^2 LC + s\left[(R_l + R_c)C + \frac{L}{-R_{ac}} \right] + 1 \right)} \tag{4.3}$$

contains $-R_{ac}$ in the first order \oefficient of the numerator quadratic and the also has the same denominator quadratic found in the loop-gain components. As mentioned above, the denominator quadratic may cause the loop-gain to contain RHP poles. The number of RHP poles in T_1 may be determined by inspecting the bode plot of the loop-gain at frequencies near the output filter resonance. A 180° drop in phase indicates that the poles of T_1 lie in the left half-plane. A 180° increase in phase indicates the presence of two RHP poles in T_1.

The presence of RHP poles in T_1 **does not** mean that the closed-loop system is unstable. However, the presence of RHP poles in a loop-gain **does** mean that system stability cannot be determined directly from the loop-gain's Bode plot. In order to predict the stability of a system using a loop-gain with RHP poles, the Nyquist Criterion must be applied directly to the polar-plot of the loop-gain. The Nyquist Criterion can be stated as follows. Let P be the number of RHP poles present in a loop-gain T. Let N be the number of counter-clockwise encirclements of the polar plot of T about the (-1,j0) point, and let Z be the number of closed-loop system eigenvalues in the right half-plane. The Nyquist Criterion states that Z = P - N. For the system to be stable, Z must be zero, so P must equal N. If the closed-loop system is

to be stable, the polar plot of the loop-gain T must encircle the (-1,j0) point in a counter-clockwise direction once for each RHP pole present in T. Thus, before the Nyquist Criterion may be used, the number of RHP poles present in the loop-gain must be known. The Routh-Hurwitz test provides a means of determining the number of RHP roots of any polynomial equation with constant real coefficients.

The Routh-Hurwitz test is performed by generating a table from the coefficients of the polynomial and checking the first column of the table for sign changes, with the number of sign changes being equal to the number of RHP roots of the polynomial. For a second-order equation, the first column of the tabulation consists of the polynomial's coefficients, allowing the number of RHP roots of a quadratic equation to be determined by counting the number of sign changes between its coefficients. For the quadratic equation which appears in the denominator of both loop-gain components T_i and T_v and the loop-gain T_1, the second- and zeroth-order coefficients are always positive, while the first-order term will be negative for a sufficiently small magnitude of $-R_{ac}$. There will be either zero or two sign changes, depending on the sign of the first-order coefficient, and thus zero or two RHP poles in loop-gains T_i, T_v and T_1. The effect of $-R_{ac}$ on the numerator of T_1 may be neglected. This assumption is justified in Appendix A.

The loop-gain

$$T_2 = \frac{T_v}{1 + T_i} = \frac{F_m \omega_m \left(1 + \frac{s}{\omega_z}\right) \frac{N_s}{N_p} V_g}{s\left(s^2 LC + s\left[(R_l + R_c + K_3)C + \frac{L}{-R_{ac}}\right] + \left(1 + \frac{K_3}{-R_{ac}}\right)\right)} \tag{4.4}$$

contains $-R_{ac}$ in two terms of the quadratic equation in the denominator. While this makes determining the number of RHP poles more complex, it is shown in Appendix A that for practical designs the s-term coefficient should be positive. If the first two terms of the quadratic are positive, the number of RHP poles in T_2 will be determined by the zeroth-order term. Thus,

T_2 will have one RHP pole when $\frac{K_3}{-R_{ac}}$ is greater than one and no RHP poles when $\frac{K_3}{-R_{ac}}$ is less than one. Recall from Eqn 4.2 that $\frac{K_3}{-R_{ac}}$ is the low frequency asymptote of T_i, allowing the number of RHP poles in T_2 to be predicted by inspecting T_i.

Loop-Gain Characteristics vs. Load

It is apparent from the previous discussion that the loop-gain characteristics of switching regulators connected to a negative-resistance load impedance will vary as the magnitude of $-R_{ac}$ changes. Although the analysis of loop-gains with RHP poles is part of fundamental control theory, it cannot be generalized as easily as the special case where the loop-gain has no RHP poles. Since the basic criteria for stability change when the number of RHP poles in a loop-gain change, it is essential to know the number of RHP poles in the loop-gains under all conditions. This section will describe how the number of RHP poles in T_1 and T_2 changes as $-R_{ac}$ is varied. The description will utilize Equations 4.3 and 4.4 as well as the Bode Plots of the loop-gains. For this system, there are three possible cases.

The first case, called Heavy Load, occurs whenever the magnitude of $-R_{ac}$ is small enough that both T_1 and T_2 contain RHP poles. Fig 4.4 shows T_i, T_v and the loop-gain T_1 for the heavy load case. Note that the complex pole-pair of the output filter lies in the right half-plane, indicated by the increase in phase at the filter resonance. Therefore, T_1 has two RHP poles for this case.

Fig. 4.5 shows T_i, T_v and the loop-gain T_2 for the heavy load case. The above discussion of Equation 4.4 revealed that T_2 will have one RHP pole whenever the low frequency asymptote of T_i (given by $\frac{K_3}{R_{ac}}$) is above 0 dB. At heavy loads, the magnitude of $-R_{ac}$ will be small, $\frac{K_3}{-R_{ac}}$ will be large, and T_2 will have one RHP pole located at the zero of T_i. The RHP pole shifts the low-frequency phase of T_2 to $-270°$, and provides 90° of phase *boost* at higher frequencies. The compensator zero also contributes 90° of phase boost, causing the phase of T_2 to rise quickly towards $-90°$ At frequencies more than a decade above the RHP pole, the phase of T_2 will be identical to that of T_2 for the resistive load case.

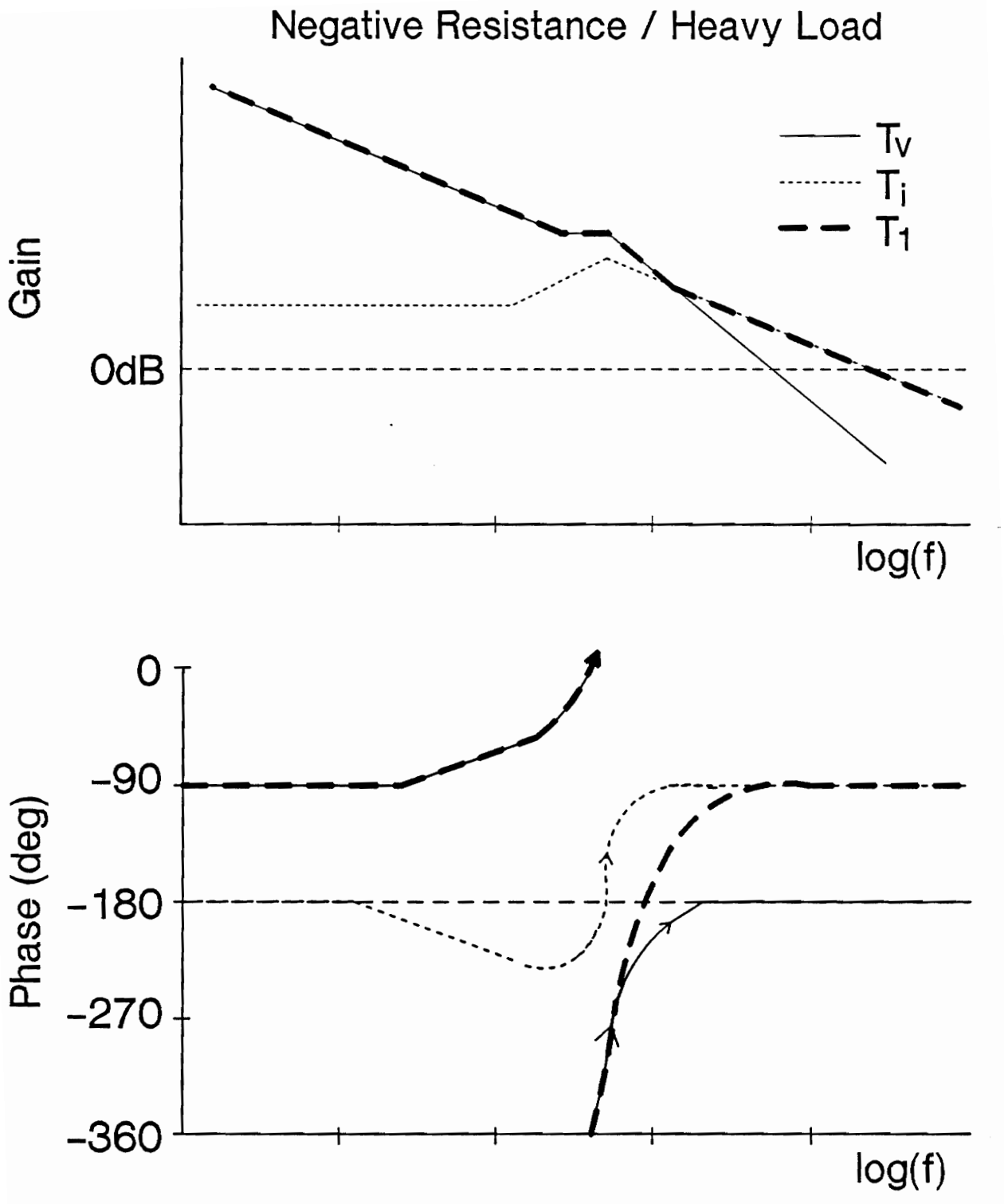


Figure 4.4. Loop Gains T_i , T_v and T_1 for Heavy Load

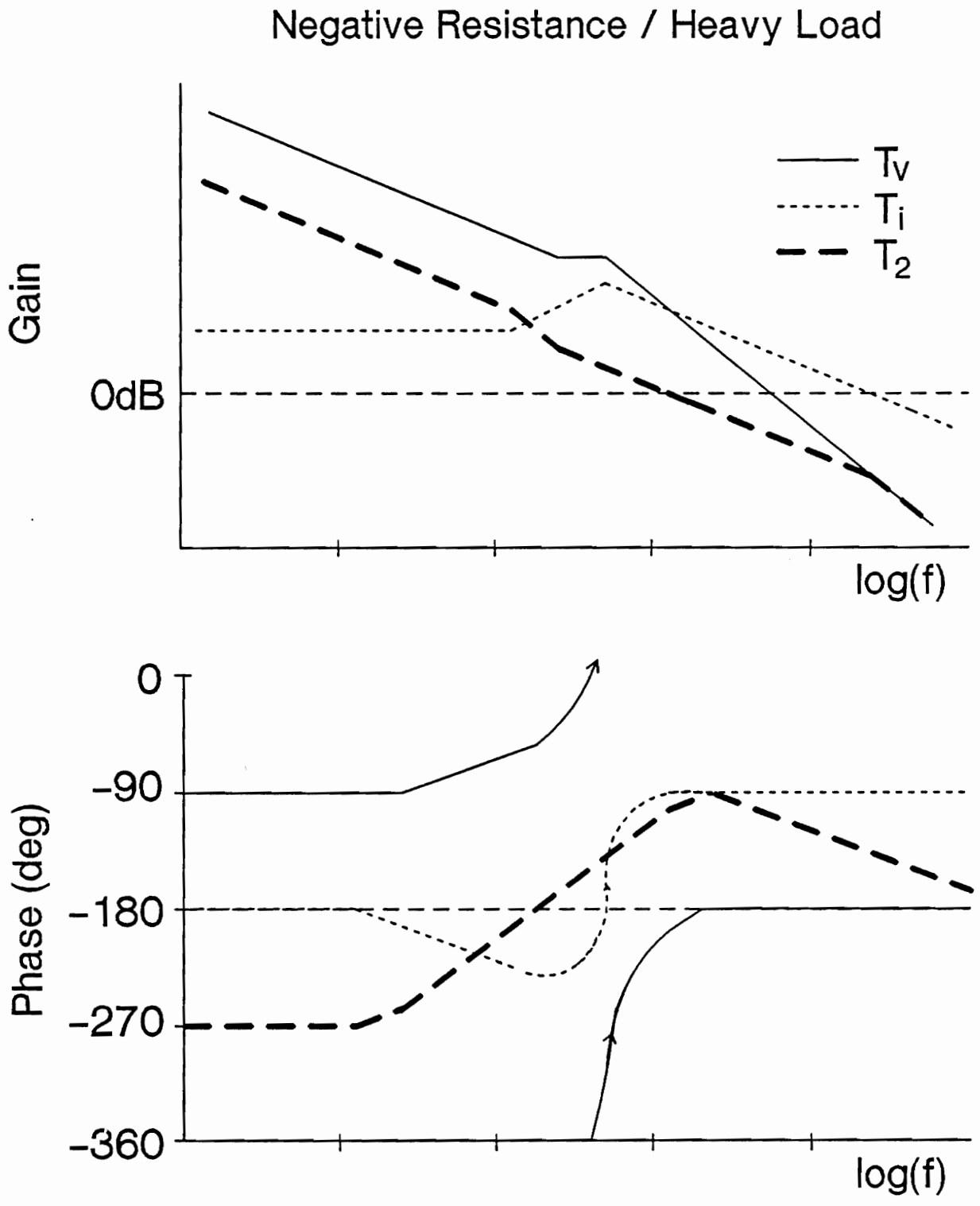


Figure 4.5. Loop Gains T_i , T_v and T_2 for Heavy Load

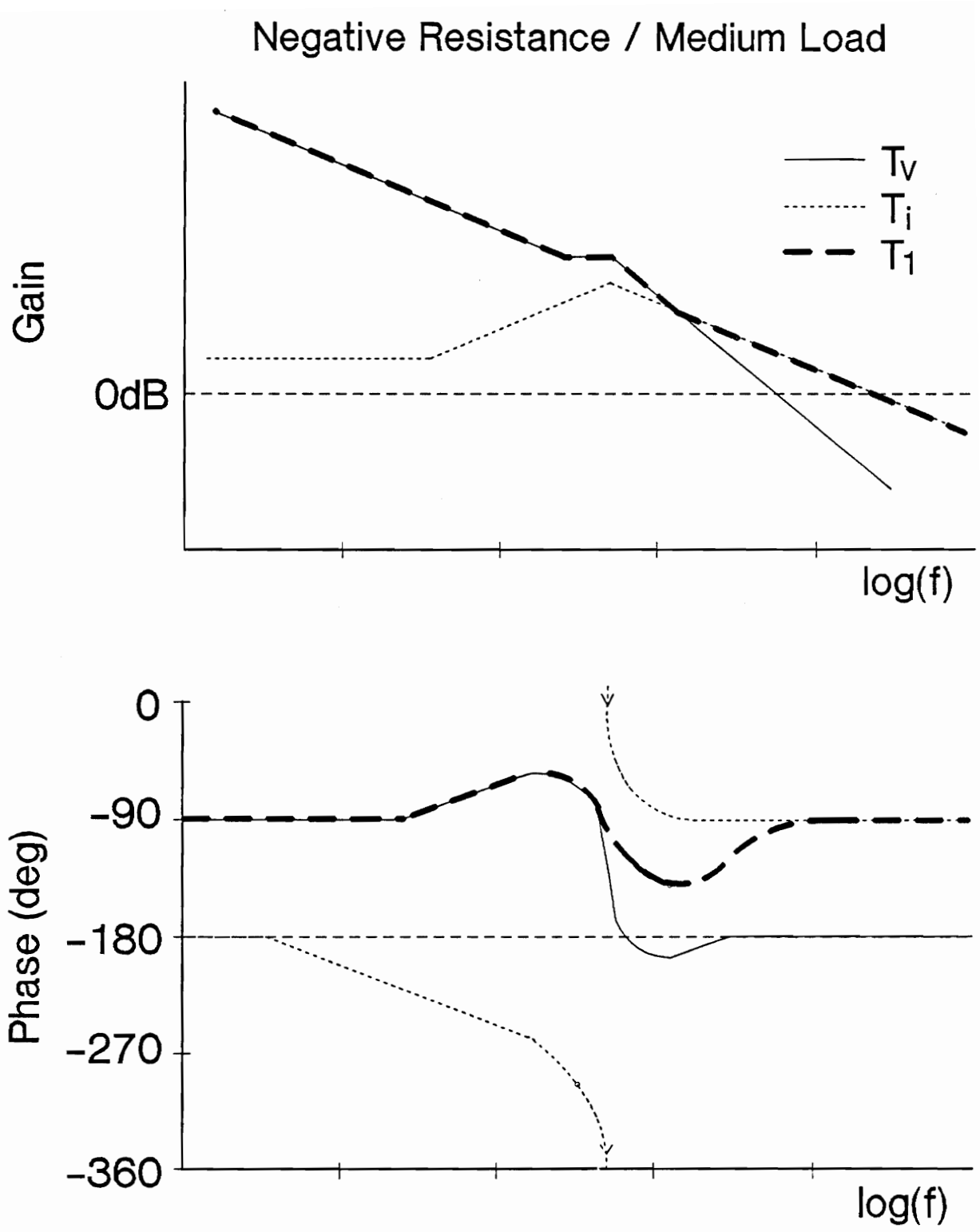


Figure 4.6. Loop Gains T_i , T_v and T_1 for Medium Load

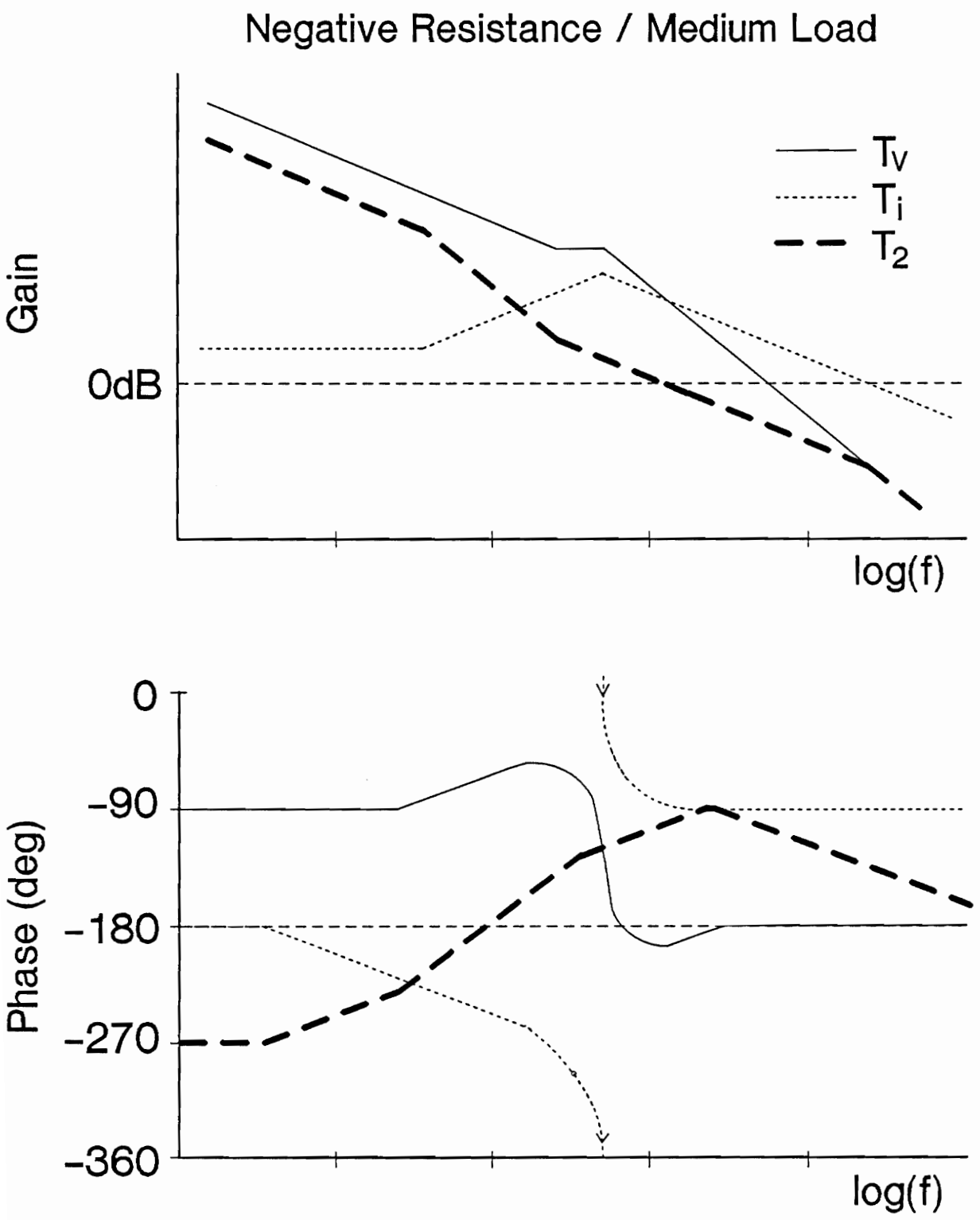


Figure 4.7. Loop Gains T_i , T_v and T_2 for Medium Load

As the system load level decreases, the magnitude of $-R_{ac}$ increases, and the negative dynamic resistance has less of an effect on the line conditioner's loop-gains (note that $-R_{ac}$ always appears as a denominator factor in the terms of Equations 4.3 and 4.4). At some critical value of $-R_{ac}$ the characteristics of one (or possibly both) loop-gain(s) will suddenly change, due to a change in the number of RHP poles in the loop-gain. For the particular system under study, it is T_1 that first displays a change in the number of RHP poles as the load level decreases. When the magnitude of $-R_{ac}$ becomes large enough to make the damping term of the denominator quadratic of Equation 4.3 positive, the complex pole-pair at the output filter resonance will move into the left half-plane. This will be indicated by a 180° *drop* in the phase of T_1 at the filter resonance, as shown in Fig. 4.6. Since $\frac{K_3}{-R_{ac}}$ is greater than unity, T_2 will continue to have one RHP pole. The range of values of $-R_{ac}$ where T_1 has zero RHP poles and T_2 has one RHP pole is referred to as Medium Load. Fig. 4.7 shows T_2 for the Medium Load case.

As the magnitude of $-R_{ac}$ increases further, $\frac{K_3}{-R_{ac}}$ will drop below unity and T_2 will change from having one RHP pole to zero RHP poles. This may be seen in Fig. 4.8, where the low frequency phase of T_2 is at −90° and drops further due to the pole at the current-loop zero. This case, where neither T_1 nor T_2 contain RHP poles, is denoted as Light Load. Fig. 4.9 shows that T_1 for Light Load conditions is identical to T_1 for Medium Load conditions. (In practice there will be a decrease in the damping of the filter for Light Load.)

In summary, this section has shown that the loop-gains' dependence on $-R_{ac}$ results in three cases for which they contain different numbers of RHP poles. For Heavy Load conditions, T_1 will contain two RHP poles while T_2 will have one RHP pole. Under Medium Load conditions, T_1 has no RHP poles and T_2 continues to have one RHP pole while for Light Load conditions, neither T_1 nor T_2 have any RHP poles. The Bode plots of both T_1 and T_2 were shown for all cases to demonstrate the loop-gain characteristics which may be encountered at different load levels. As discussed above, knowledge of the number of RHP poles in a loop-gain is prerequisite to employing the Nyquist Criterion to determine system stability. The stability analysis

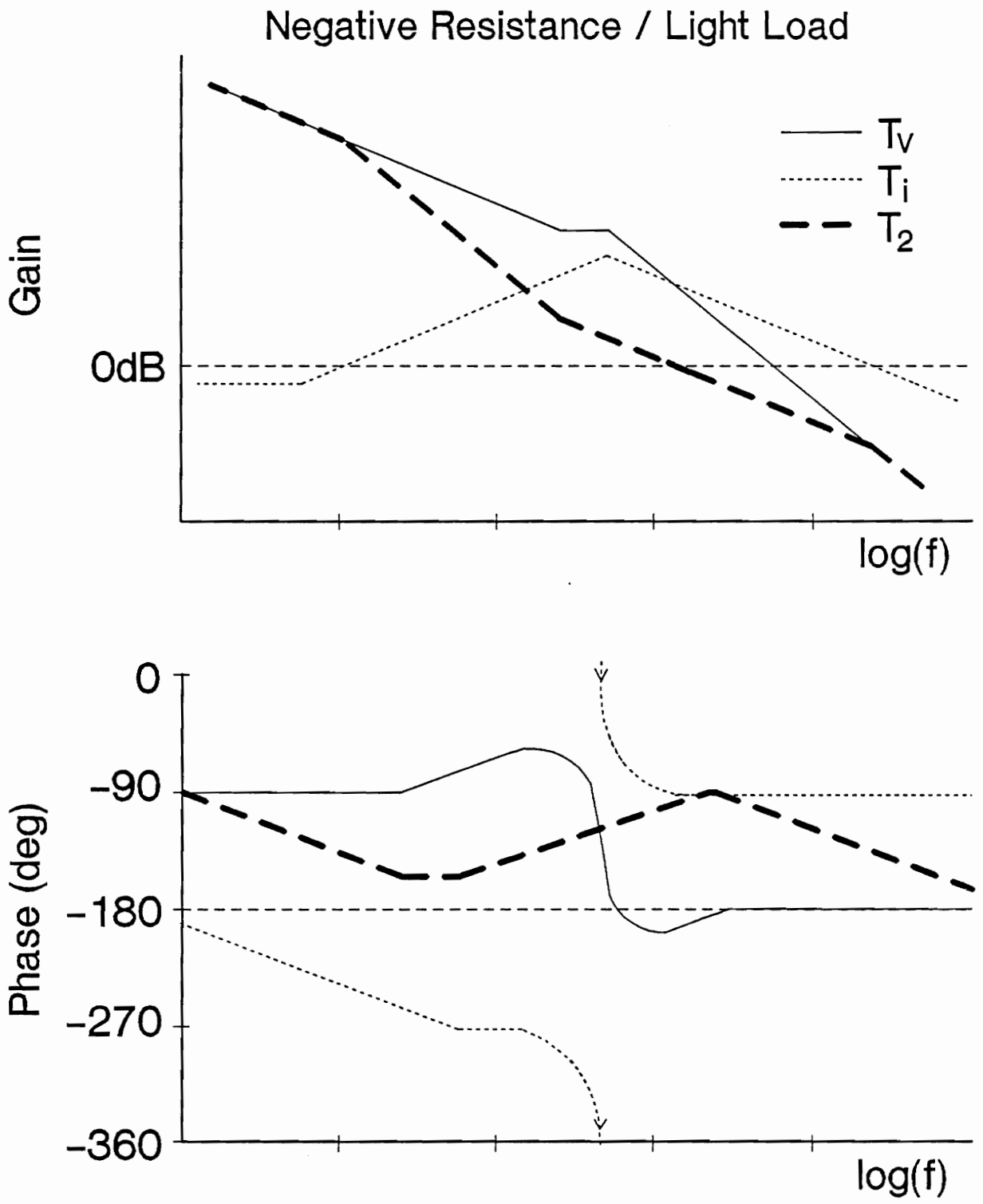


Figure 4.8. Loop Gains T_i , T_v, T_2 for Light Load

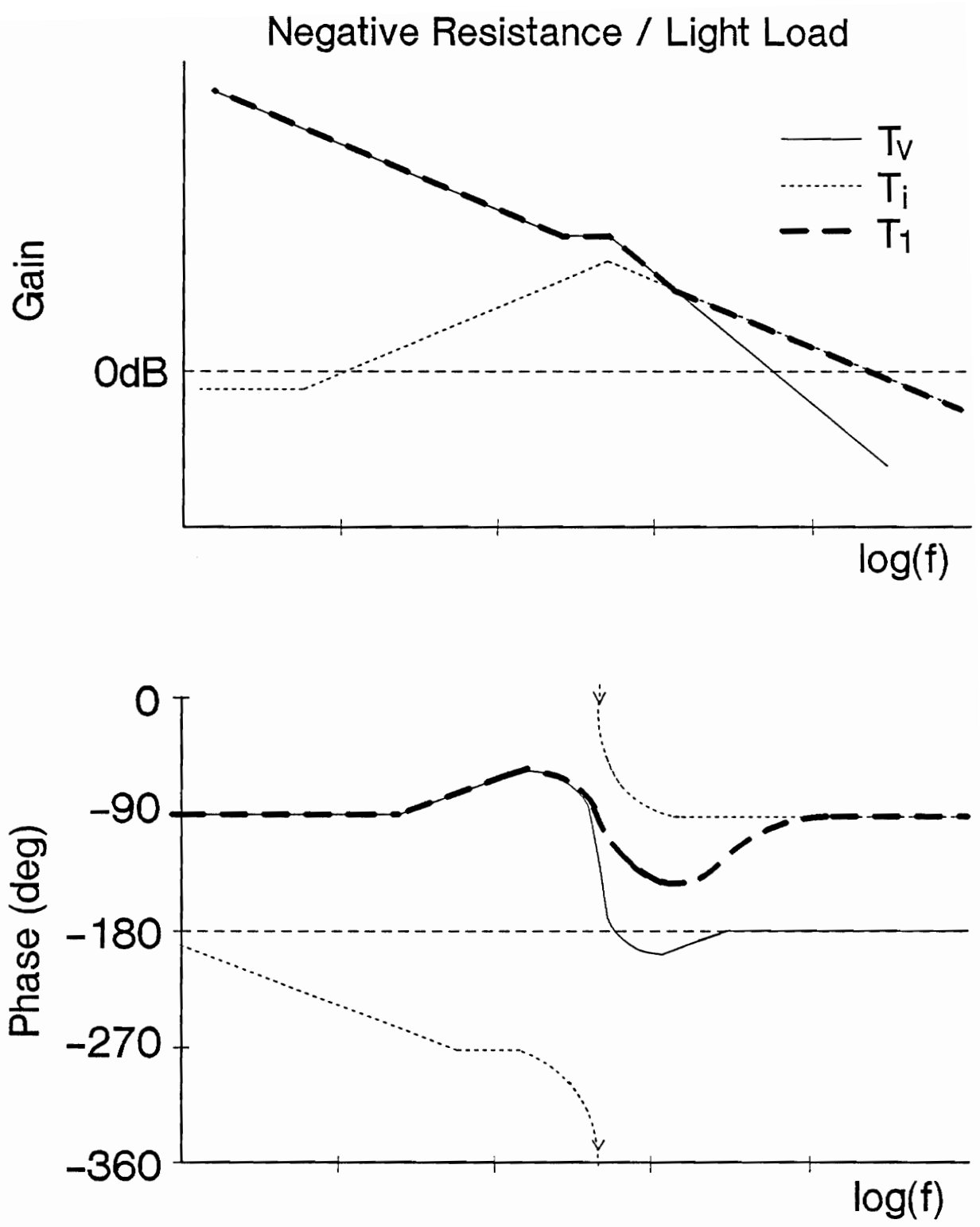


Figure 4.9. Loop Gains T_i , T_v, T_1 for Light Load

of the line conditioner with a negative dynamic resistance is considered in the following section.

4.2.2 Stability Analysis of the Line Conditioner

The stability analysis of any system should be confirmed by measurement of the loop-gain of the actual system. Most network analyzers display information in Bode plot form (i.e. gain and phase vs. frequency). Since the Bode plot contains all of the information needed to construct the polar plot of the loop-gain, the stability of the system may be predicted from the Bode plot of the loop-gain if the number of RHP poles is known. In the conventional case, where the loop-gain has no RHP poles, the Nyquist Criterion requires that the polar plot of the loop-gain must not encircle the (-1,j0) point if the system is to be stable. The equivalent "zero encirclement" condition for the Bode Plot is that the phase of the loop-gain be above $-180°$ when its magnitude drops below 0 dB. Unfortunately, many engineers are accustomed to using only the Bode Plot of the loop-gain to predict a system's stability and have forgotten that the Bode plot's interpretation depends on the number of RHP poles in the loop-gain. This interpretation must be derived by applying the Nyquist Criterion to the loop-gain's polar plot. The following example will illustrate how the Bode plot of a loop-gain can be misleading for unconventional cases.

Bode Plot Interpretation Example

Fig. 4.10 shows loop-gain T_2 for three parallel load converters. One curve is the loop-gain when the load converters are operated from an ideal voltage source, and the other is the loop-gain when the load converters are operated from a single line conditioner operating open-loop (it can be shown that this case is identical to an input filter interaction problem where the line conditioners' output filter is the load converter's input filter). While the loop-

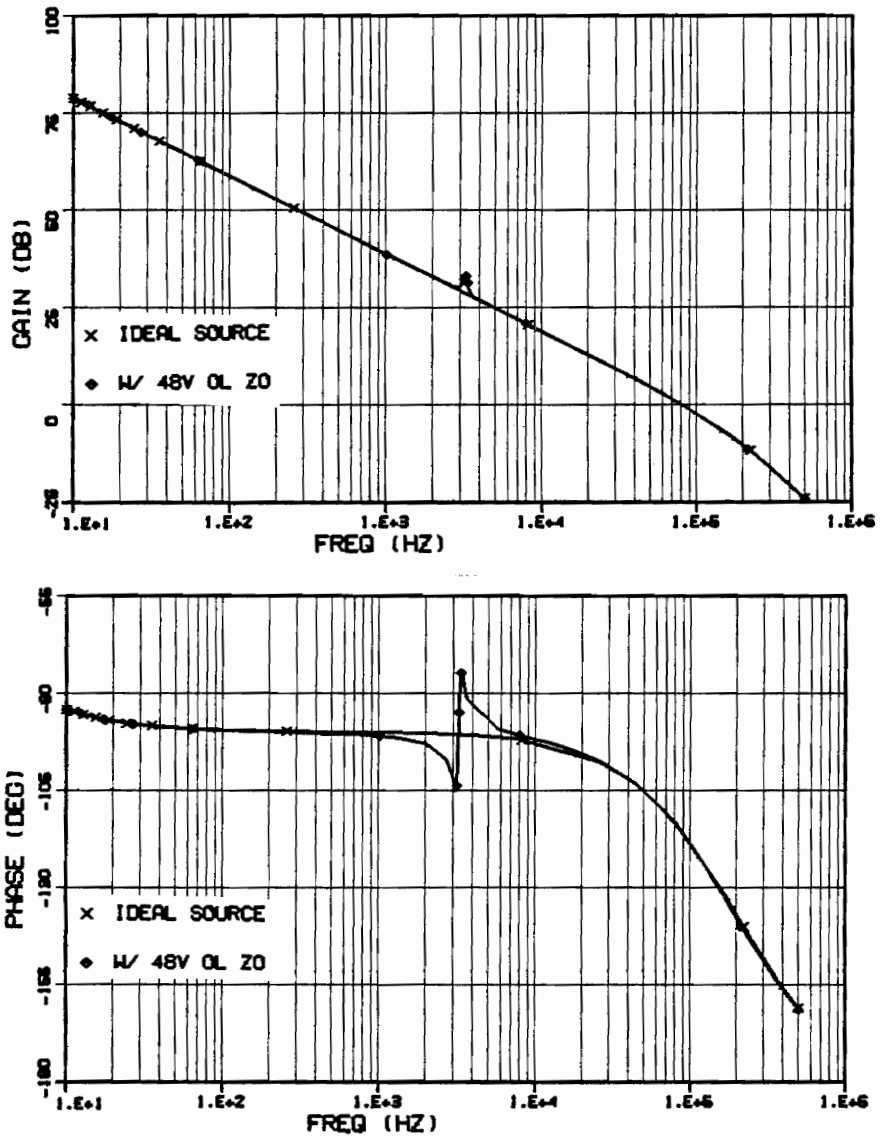


Figure 4.10. Loop Gain of Load Converter for Ideal and Non-Ideal Source.

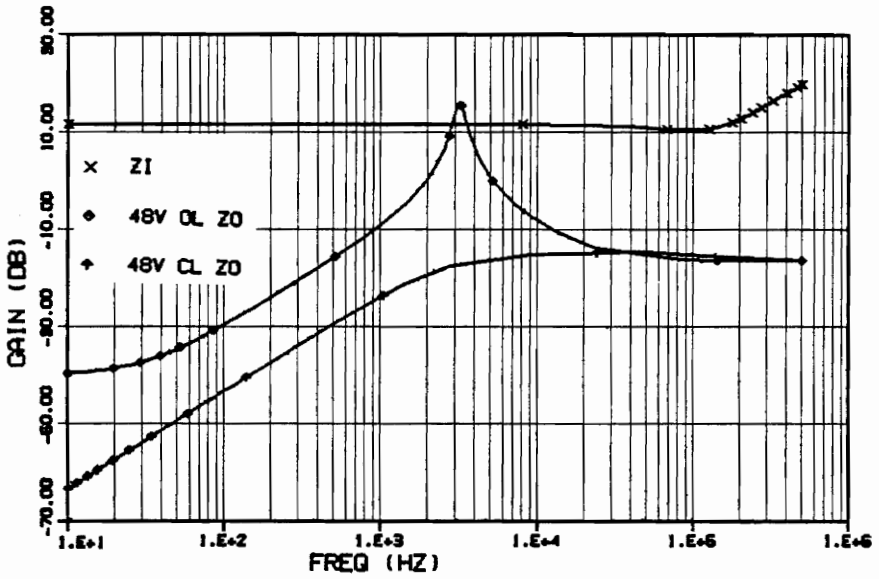


Figure 4.11. Impedance Comparison Between Load Converter and Open-Loop Line Conditioner

gain in Fig. 4.10 shows some sign of interaction between the two subsystems, the degree of interaction appears to be minor and it would seem to be quite reasonable to conclude that the interaction does not threaten the stability of the system. However, this conclusion is based on the assumption that, because the magnitude and phase of the loop-gain remain well above 0 dB and −180°, respectively, the system is stable. Fig. 4.11 shows the impedance comparison between the load converters and the open-loop line conditioner. The impedances are overlapping at the frequency where the loop-gain shows interaction, so stability problems are a concern. Fig. 4.12 shows the poles and zeros of the loop-gain with the open-loop line conditioner, and the closed-loop eigenvalues of the system (line conditioner remains open-loop). Note that the system has two RHP eigenvalues and is actually unstable. This is due to the two RHP poles which are part of T_2 due to the interaction. The correct interpretation of the Bode Plot in Fig. 4.10 is that, since the disturbance in the loop-gain is minor, the number of encirclements about (-1,j0) is still zero. However, since the number of RHP poles in the loop-gain has changed, the number of encirclements needed to satisfy the Nyquist Criterion has changed as well. Thus, use of the Bode plot of a loop-gain can be misleading if the loop-gain has RHP poles. In cases where the loop-gain is known to contain RHP poles or shows signs of interaction, the Nyquist criterion should be applied directly to the polar plot of the loop-gain, and techniques such as impedance comparison or eigenvalue calculation should be used to confirm the results.

Stability Analysis UsingT_2

Since a negative resistance load impedance can induce only one RHP pole into T_2, it is simpler to analyze, and is considered first. If the low-frequency asymptote of the current-loop gain drops below 0 dB, then T_2 will have no RHP poles and conventional analysis techniques may be used. When the low-frequency asymptote of T_i is greater than 0 dB then T_2 will have one RHP pole and the methods described above must be used to analyze the stability of the regulator. Fig. 4.13 shows a sketch of the Polar plot of loop-gain T_2 for Medium and Heavy Loads. The solid part of the plot corresponds to the Bode Plots shown in Figs. 4.4 and 4.6.

TRANSFER FUNCTION ZEROS

REAL	IMAGINARY
1049.85	+- 20327.2
-50000.0	0.000000E+00

TRANSFER FUNCTION POLES

REAL	IMAGINARY
608.264	+- 20317.9
-6.36013	0.000000E+00
-50848.2	0.000000E+00

EIGENVALUES

REAL	IMAGINARY
1048.75	+- 20310.8
-.893020	0.000000E+00
-49920.8	0.000000E+00
-150497.	0.000000E+00
-572286.	+- 547009.

Figure 4.12. Loop-Gain Poles and Zeros and System Eigenvalues

In this case P = 1, N=1 and the system is stable. In the conventional case, where the loop-gain has no RHP poles, relative stability is expressed in terms of gain and phase margins which may be read directly from the Bode plot. However, these quantities are defined using the Nyquist plot, and depend on the number of RHP poles present in the loop-gain. For the conventional case, where there are no RHP poles, N must be zero for stability, so the gain and phase margins reflect how far the loop-gain is from making an encirclement of the (-1, j0) point. For the present case, the loop-gain must make exactly one encirclement of (-1, j0) for the system to be stable.

Two gain margins and one phase margin may be defined for T_2, as shown in Fig. 4.13. The first gain margin, GM1, measures how far the loop-gain is *above* 0 dB when its polar-plot crosses the negative real axis traveling in a counter-clockwise direction. In the Bode Plots, this corresponds to the gain at the rising 180° phase crossover which occurs at low-frequency. The second gain margin, GM2, measures how far the loop-gain is *below* 0 dB when its polar plot becomes asymptotic to the negative real axis. This corresponds to the gain of the Bode plot at the point where its phase reaches −180° at high-frequency. The phase margin of T_2 measures the angle (counter-clockwise is positive) between (-1, j0) and the point where the loop-gain's magnitude decreases below unity. On the Bode plot, this corresponds to how far the phase is above −180° at the magnitude's 0 dB crossover. If any of these quantities should become less than or equal to zero, then T_2 will encircle the (-1, j0) point such that $N \neq 1$ and the system will be unstable.

To gain more insight into the meaning of the gain and phase margins, two hypothetical cases where the regulator is unstable are considered. Fig. 4.14 shows the Nyquist Plot of a case were the instability of the regulator would be indicated by negative values of both GM2 and the phase margin. GM2 is negative because the solid part of the loop-gain crosses the negative real axis for the *second* time with a magnitude *greater* than unity. The phase margin is negative because the solid part of the loop-gain drops below unity gain at an angle of −180° (the angle shown in Fig. 4.14 is less than −180° for clarity of illustration.) The loop-gain as

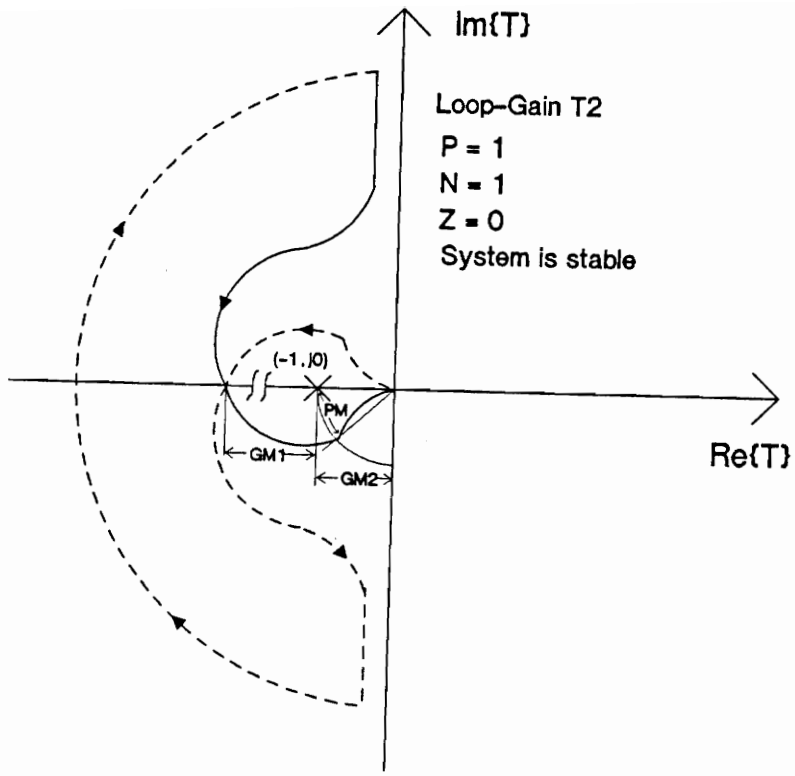


Figure 4.13. Polar Plot of Loop-Gain T_2 for Medium and Heavy Loads

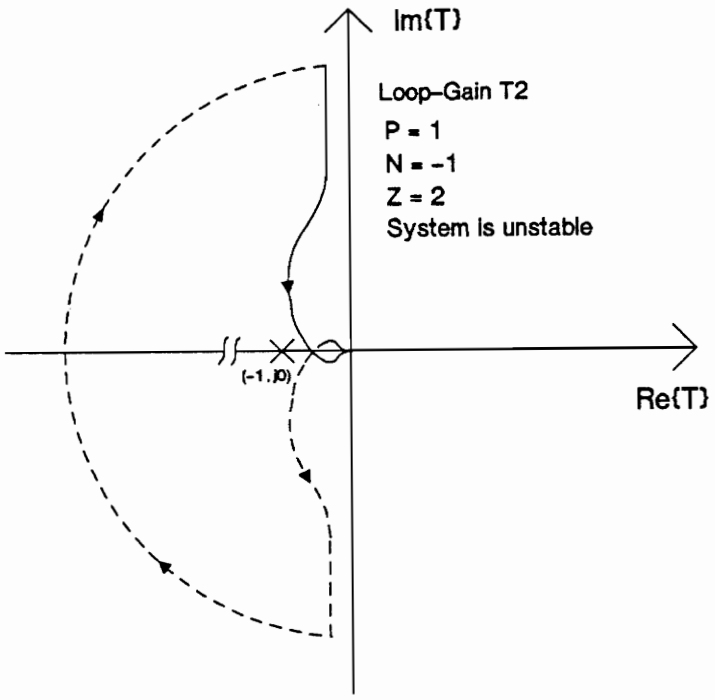


Figure 4.14. Loop-Gain T_2 for Hypothetical Unstable Case

shown in Fig. 4.14 makes one clockwise encirclement, therefore, N = -1 and the closed loop system will be unstable, with two RHP eigenvalues. Since GM2 is identical to the gain margin defined when the loop-gain has no RHP poles, it should be caused by the same physical phenomena. Thus, the instability shown in Fig. 4.14 is due to an excessive amount of gain in the voltage-loop, which is the interpretation for a negative gain margin for T_2 in the conventional case.

Fig. 4.15 shows a case where GM1 is negative. Note that the solid part of the loop-gain crosses the negative real axis for the *first* time with a gain *less* than unity. As before, the phase margin is negative because the loop-gain decreases to unity at an angle of less than $-180°$. This causes the polar plot to make one counterclockwise encirclement, resulting in two RHP poles in the closed-loop system. While GM2 is equivalent to the gain-margin used in the resistive load case, GM1 is defined only when the loop-gain has one RHP pole, so its physical cause is related to the negative resistance load impedance. Noting that the RHP pole in T_2 is caused by the RHP zero in T_i GM1 reflects the change in the stability criteria for T_2 caused by the influence of $-R_{ac}$ on T_i. The effect of the additional gain margin is to place a low-frequency boundary on the allowed crossover frequency for T_2.

The loop-gain T_1 may also be used to predict the stability of the regulator. Under Medium and Light Load conditions T_1 contains no RHP poles, allowing conventional analysis techniques to be used. Under Heavy Load conditions T_1 has two RHP poles, so the polar-plot of the loop-gain must be used. Fig. 4.16 shows the polar plot for loop-gain T_1 as shown in Fig. 4.3. Since the loop-gain has two RHP poles, the polar-plot must encircle (-1, j0) twice in a counter-clockwise (CCW) direction. Fig. 4.16 shows that T_1 does make two CCW encirclements, so the system is stable. As in the previous example, gain and phase margins must be redefined to reflect the new criteria for stability. Although the polar plot of T_1 is more complex than that of T_2 , the definition of gain and phase margins is simplified by noting that the solid portion of the curve corresponding to positive frequency accounts for one encirclement, while its mirror image (which corresponds to negative frequency) is responsible

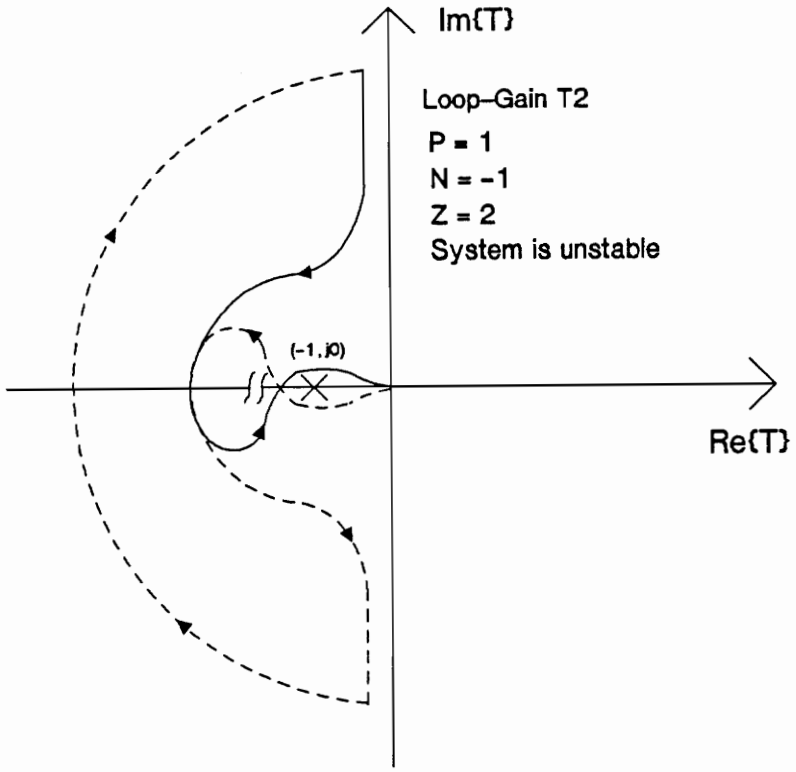


Figure 4.15. Loop-Gain T_2 for Hypothetical Unstable Case

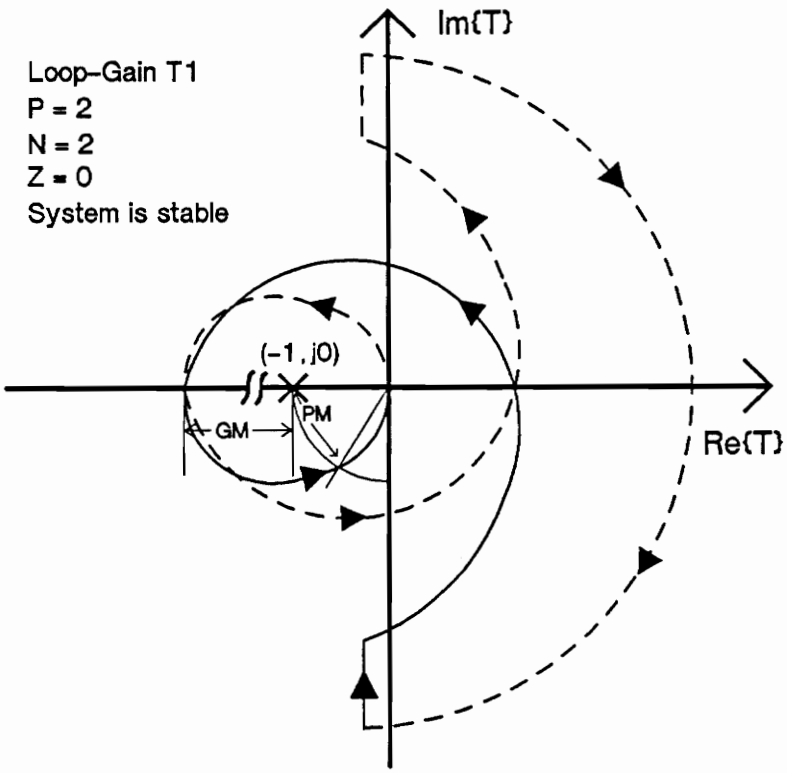


Figure 4.16. Polar Plot of Loop-Gain T_1 for Heavy Loads

for the second. This allows the stability margins to be defined in terms of the *solid portion* of the plot making *one* encirclement of (-1, j0). As with the previous case, the magnitude of the loop-gain must be above unity when the loop-gain crosses the negative real axis for the first time. This gives rise to the gain margin marked "GM" in Fig. 4.16. In order to complete the encirclement, the polar plot of the loop-gain must drop below unity gain at a point below the real axis. This is measured by the phase margin marked ΦM in Fig. 4.16. This loop-gain has only one gain margin because its phase is asymptotic to $-90°$ at high frequency.

Fig. 4.17 shows a hypothetical case where the regulator is unstable due to an excessive amount of voltage-loop gain. (Note that the phase angle as frequency goes to infinity is $-180°$, which is characteristic of T_v.) Both the gain and phase margins are negative and the polar plot does not make the required encirclements. It is interesting to note that the RHP pole-pair does *not* contribute to the instability. The RHP pole-pair contributes its 180° phase boost in a narrow frequency range at the filter resonance, where the magnitude of the loop-gain is still large. Therefore, the RHP complex pole-pair tends to be self correcting, allowing the additional constraint imposed by the new gain margin to be satisfied without special effort. Another interesting point is that, because T_1 is the vector sum of T_i and T_v, it does not display the altered phase characteristics of the current-loop at low frequencies. Thus, for a typical design where the voltage-loop dominates until well above the filter resonance, the RHP poles of the filter should cause no problems. However, for a design which is near the critical point of GM1 for the loop-gain T_2, T_1 will display a sudden drop to 0 dB because the loop-gain components are 180° apart at the point where T_i and T_v intersect. Because T_1 displays the magnitude and phase characteristics of the larger of the two loop-gain components, the above problem cannot be predicted by looking only at T_1 . Noting that the negative-resistance input impedance of the load converter affects only the phase characteristics of the line conditioner loop-gains and that loop-gain T_2 displays the phase relationships of the loop-gain components, it follows that the effects of the negative-resistance load impedance should be displayed most clearly by T_2.

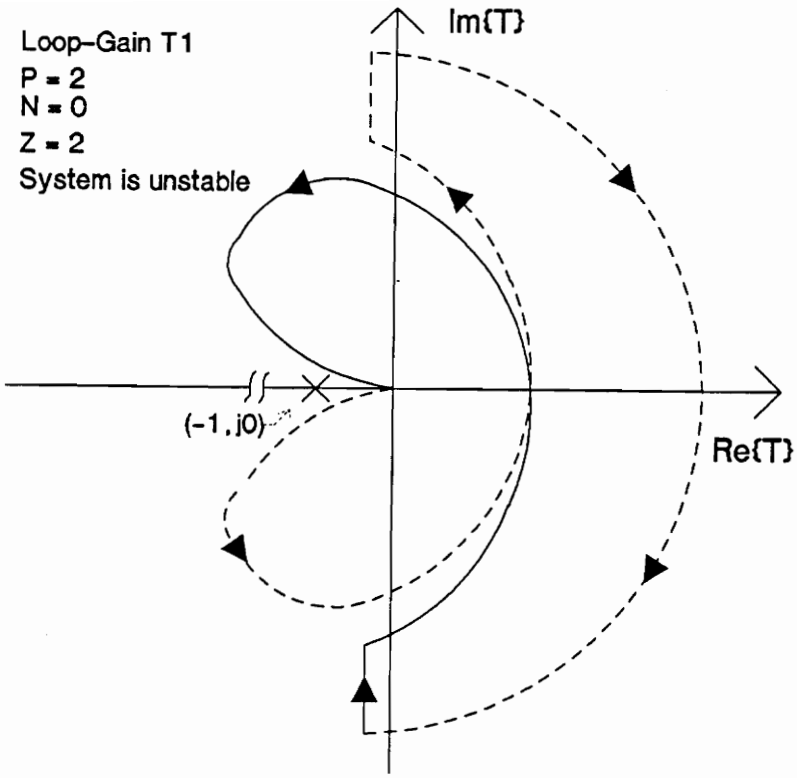


Figure 4.17. Loop-Gain T_1 for Hypothetical Unstable Case

Control Loop Design

The proceeding section demonstrated a detailed analysis of the stability of the line conditioner when its loop-gains have RHP poles. Once the number of RHP poles in a loop-gain is known, the stability of the regulator can be determined by applying the Nyquist Criterion to the loop-gain's polar plot. Gain and Phase margins are defined using the polar plot of the loop-gain, but may be translated to the Bode Plot for each particular case. Note that the stability margins change as the number of RHP poles changes. This means that the interpretation of the Bode Plot will change each time the number of RHP poles change. In addition, the analysis showed that the control design necessary to stabilize the regulator for a negative-resistance load impedance is very similar to the control for a resistive load. The negative-resistance load impedance alters the phase characteristics of the current-loop gain by shifting the numerator zero into the right half-plane. This creates a region where the loop-gain components T_i and T_v are 180° out of phase, making it undesirable to have $T_v = T_i$ in this region. As a result, a lower bound must be placed on the crossover frequency of the loop-gain T_2 to insure the stability of the regulator when operating under negative resistance conditions. Since a high crossover frequency is desired in order to achieve high performance, existing design procedures should be acceptable. In addition, the negative dynamic resistance can shift the complex poles of the output filter into the right half-plane, resulting in an additional gain margin requirement for T_1. One possible design approach is to optimize the regulator for a resistive load and then verify that the additional gain margins for T_1 and T_2 are acceptable under negative resistance conditions. The worst-case condition for GM1 will occur at full-load, since this moves the RHP pole to its highest frequency and reduces the low frequency gain of T_2.

The effect of a negative-resistance load impedance on the loop-gains and stability of the line conditioner has been accounted for. However, the relationship between the line conditioner's loop-gains and performance indices needs to be examined before proceeding with a design based on a resistive load assumption. The performance of a switching regulator is measured by its audiosusceptibility, output impedance and the ability to respond to changes in load demand. On an intuitive level, audio and output impedance are related to the *magnitudes* of the

regulator's loop-gains, which are unaffected by the -R impedance. Furthermore, both settling time and output peaking are determined by the shape of the output impedance curve, which again relates back to the magnitudes of the loop-gains. It was shown in reference [6] that the performance indices of a multi-loop controlled switching regulator are determined by the zeros of the loop-gain T_1, and are almost totally independent of the characteristics of the load for a buck converter. The effect of $-R_{ac}$ on the zeros of T_1 is shown to be negligible in Appendix A. It is concluded that design procedures based on resistive load conditions may be used for negative resistance conditions, provided that the gain margin GM1 of T_2 and the gain margin of T_1 are confirmed to be satisfactory under negative resistance conditions. A practical example follows.

Design Example

The design goal for the line conditioner control was for minimum output impedance and as large a stability margin as possible. The output capacitor ESR set the lower bound for output impedance at 0.15Ω. The control design for the line conditioner was optimized for a resistive load using the procedures discussed in Chapter 3. The resulting control parameters were: $F_i = 0.057$, $S_e = 0.044V/\mu s$, $\omega_p = 21.2kHz$, $\omega_z = 2.4kHz$, $\omega_m = 5.73krad/sec$, corresponding to an integrator crossover of 913Hz. (See Fig. 4.1 for power stage parameters). A stable, high performance design was achieved. Under resistive load conditions, the phase margin of T_1 was 81° , and the gain and phase margins of T_2 were 46 dB and 76°, respectively. The loop-gain components and loop-gains for the same regulator under worst case (full load) negative resistance conditions are shown in Figs. 4.18, 4.19 and 4.20. Note that T_1 has a phase margin of 85° and gain margin of 37 dB, while T_2 has a phase margin of 75° and gain margin GM1 = 28 dB and GM2 = 50 dB. Figs. 4.21 and 4.22 show the audio and output impedance for the regulator under both positive and negative resistance conditions. In both cases, the negative resistance curve is nearly identical to the curve for the resistive load. Figs. 4.23 and 4.24 show step load responses for the converter with a resistive load and a constant-power load, respectively. The settling times are almost identical. The simulation with the constant power

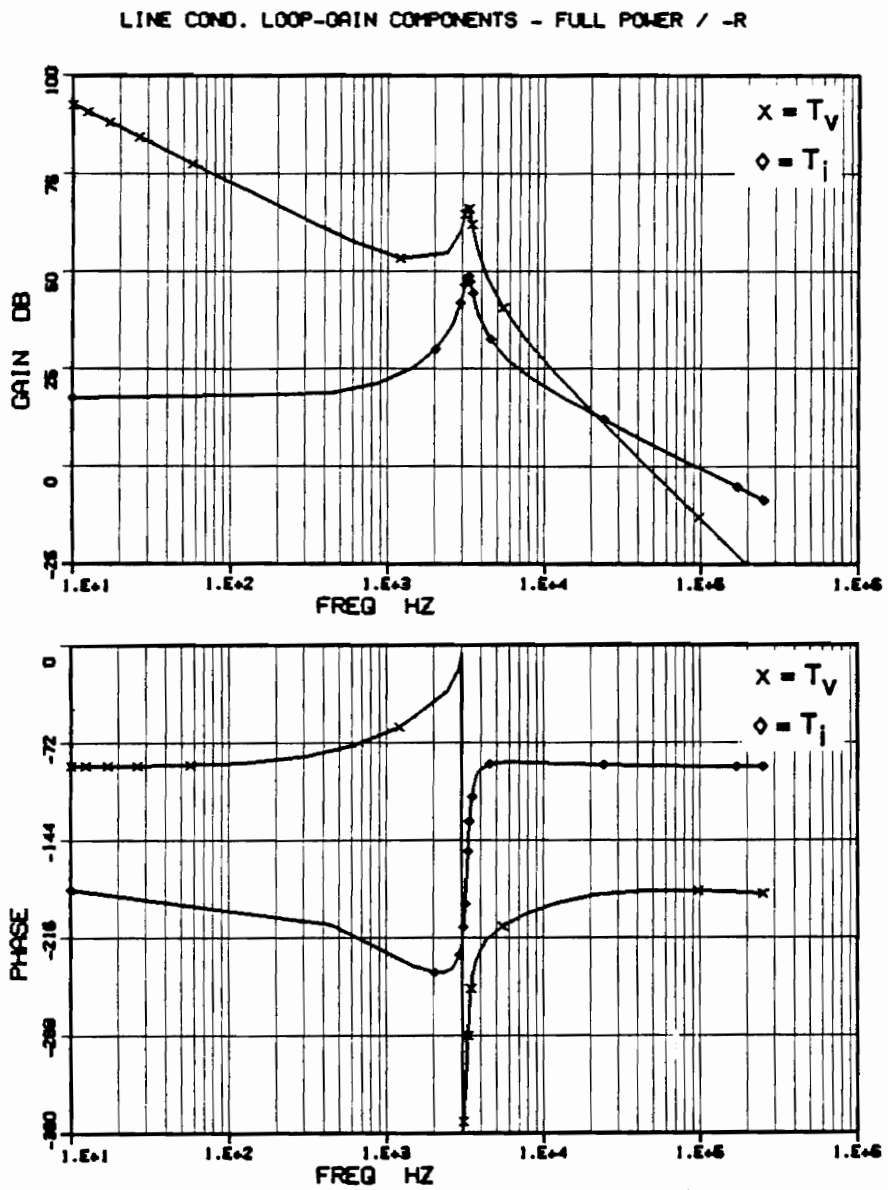


Figure 4.18. Loop-Gain Components at Heavy Load

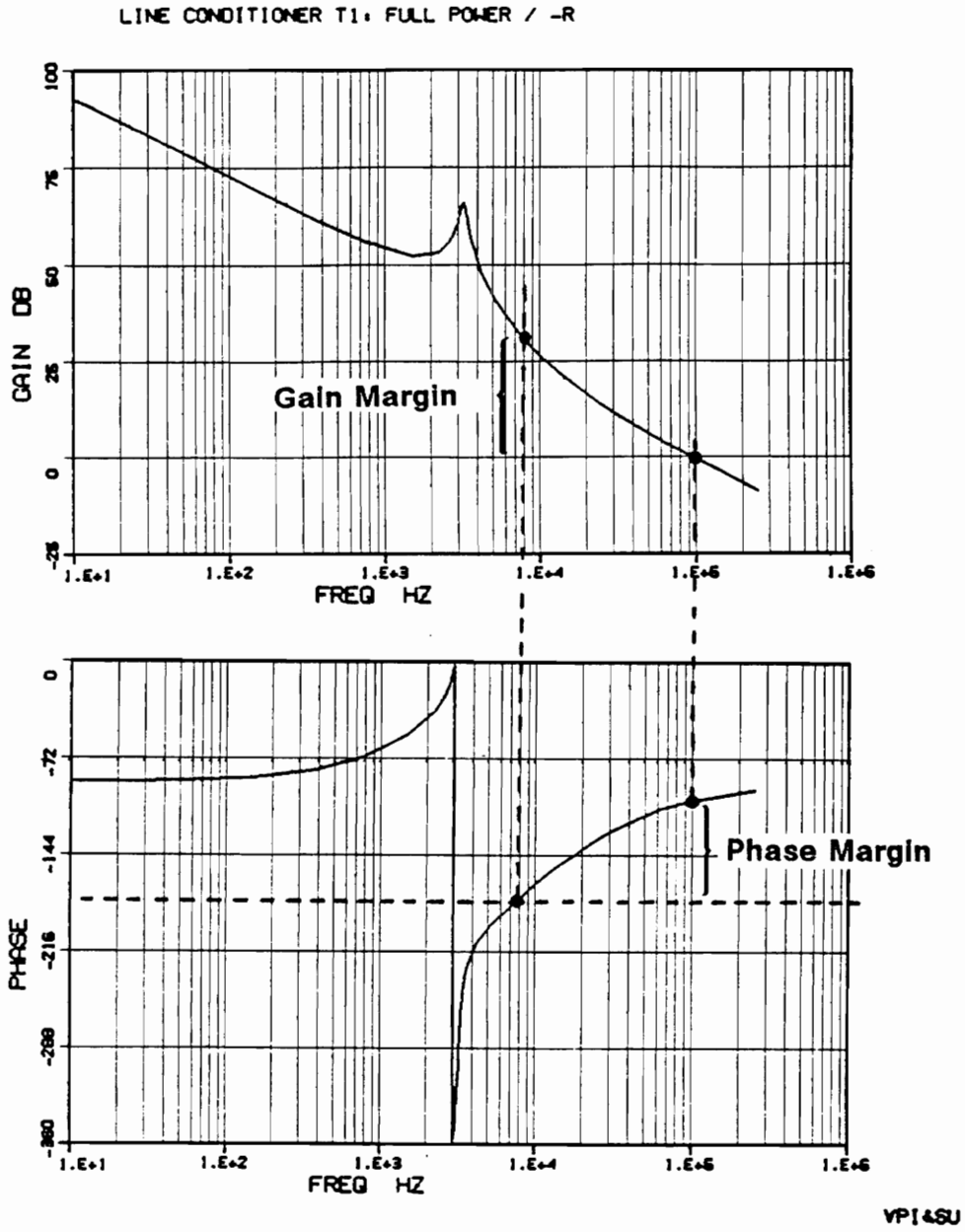


Figure 4.19. Loop-Gain T_1 for Heavy Load

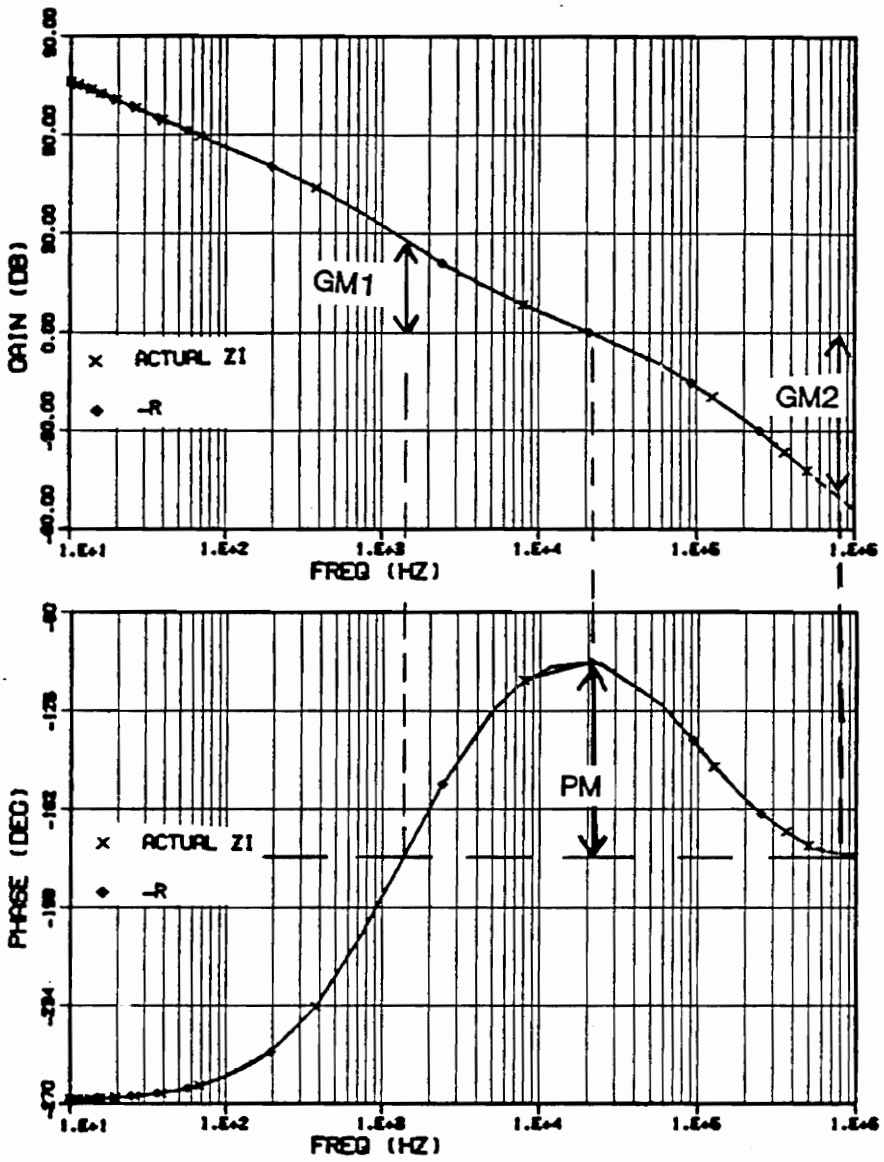


Figure 4.20. Loop-Gain T_2 for Heavy Load

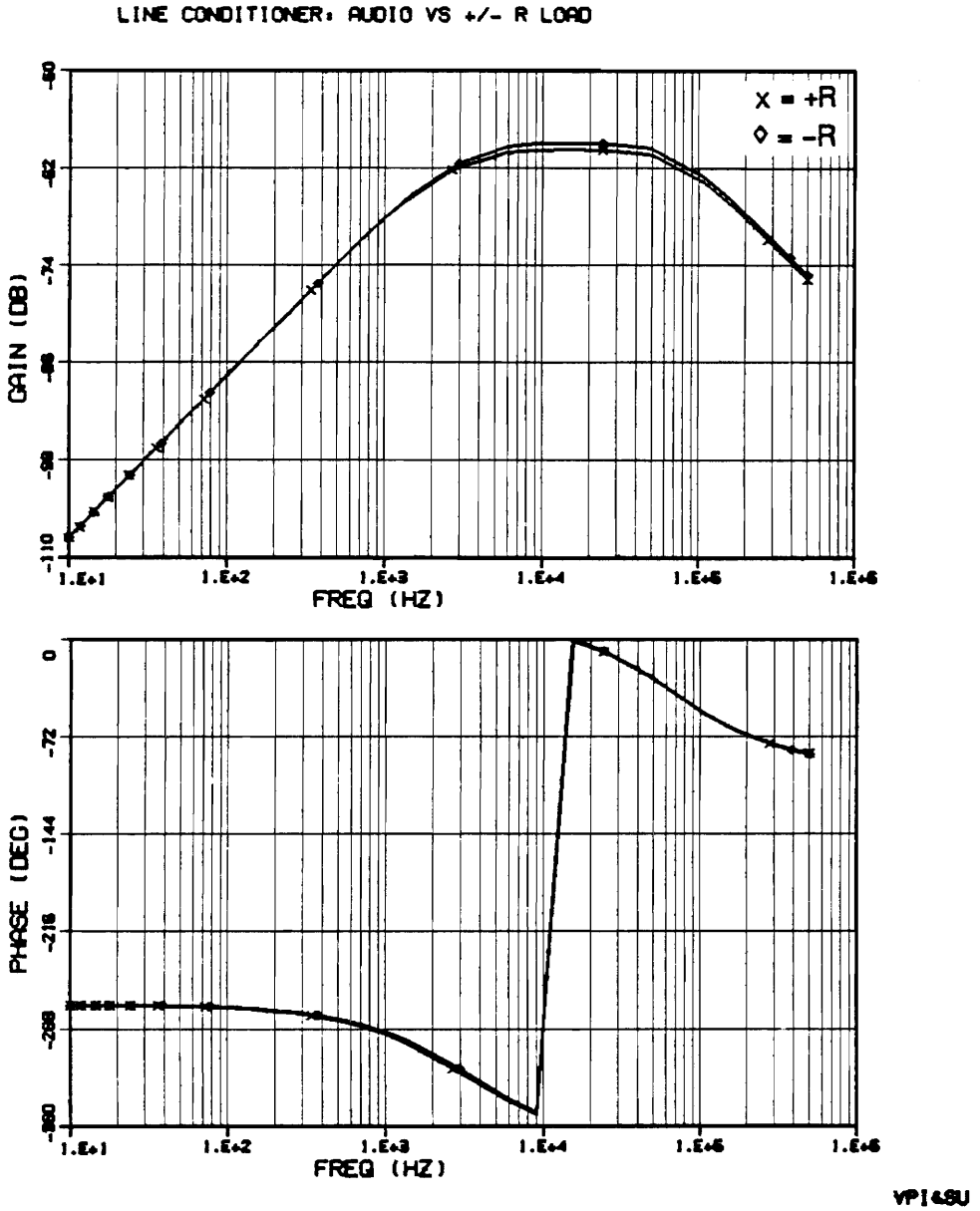


Figure 4.21. Audio for Positive and Negative Resistance Loads

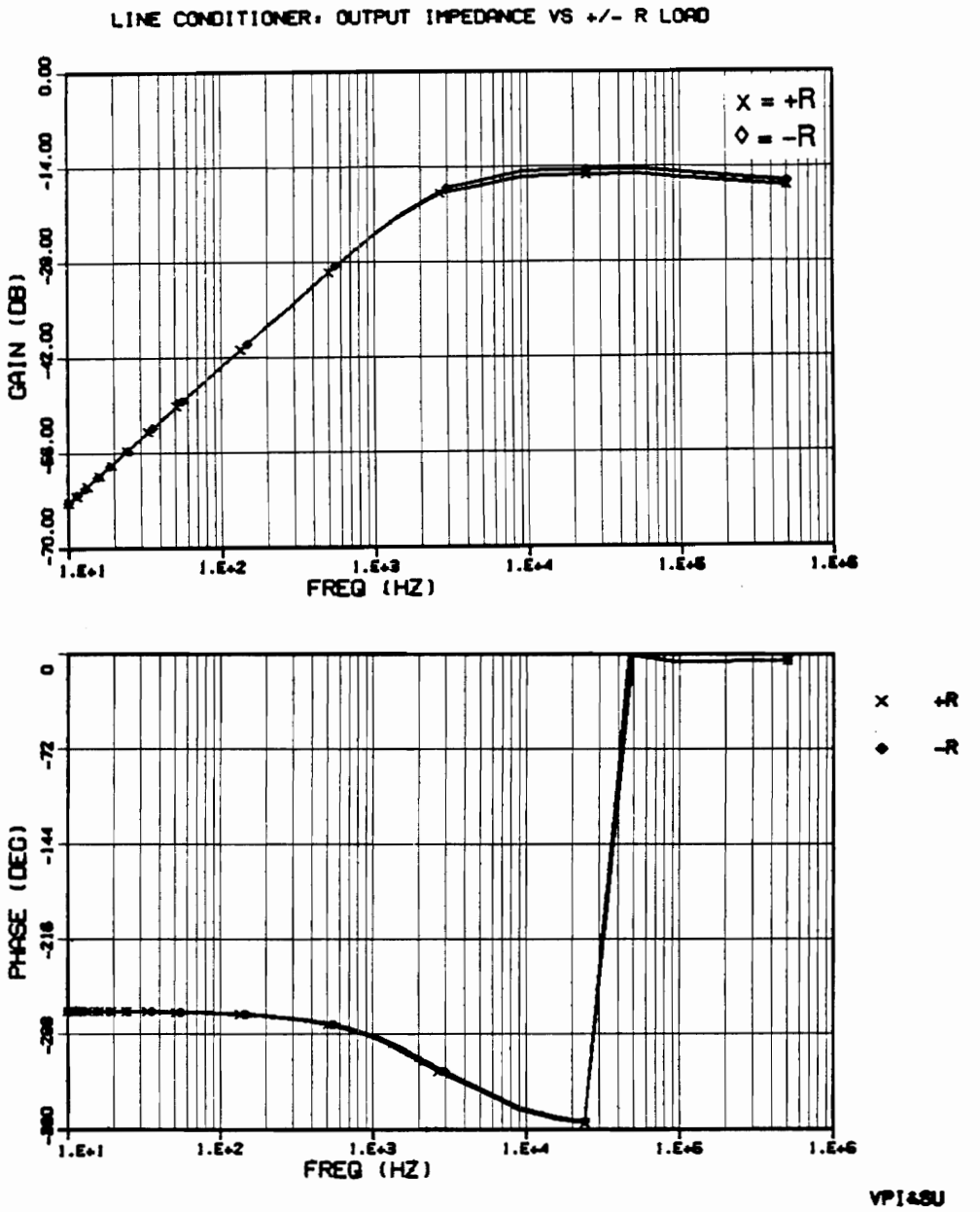


Figure 4.22. Output Impedance for Positive and Negative Resistance Loads

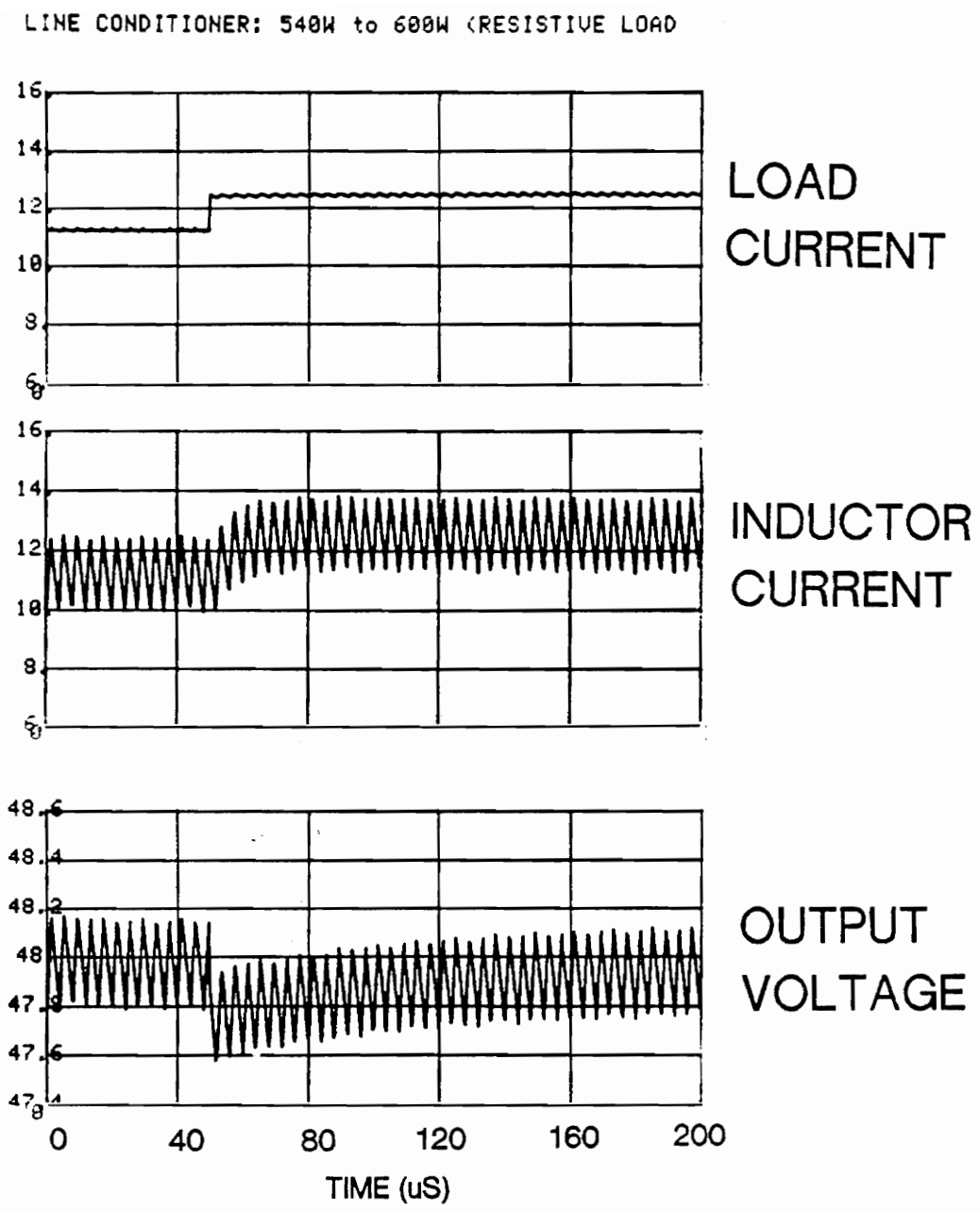


Figure 4.23. Step Load Response - Resistive Load

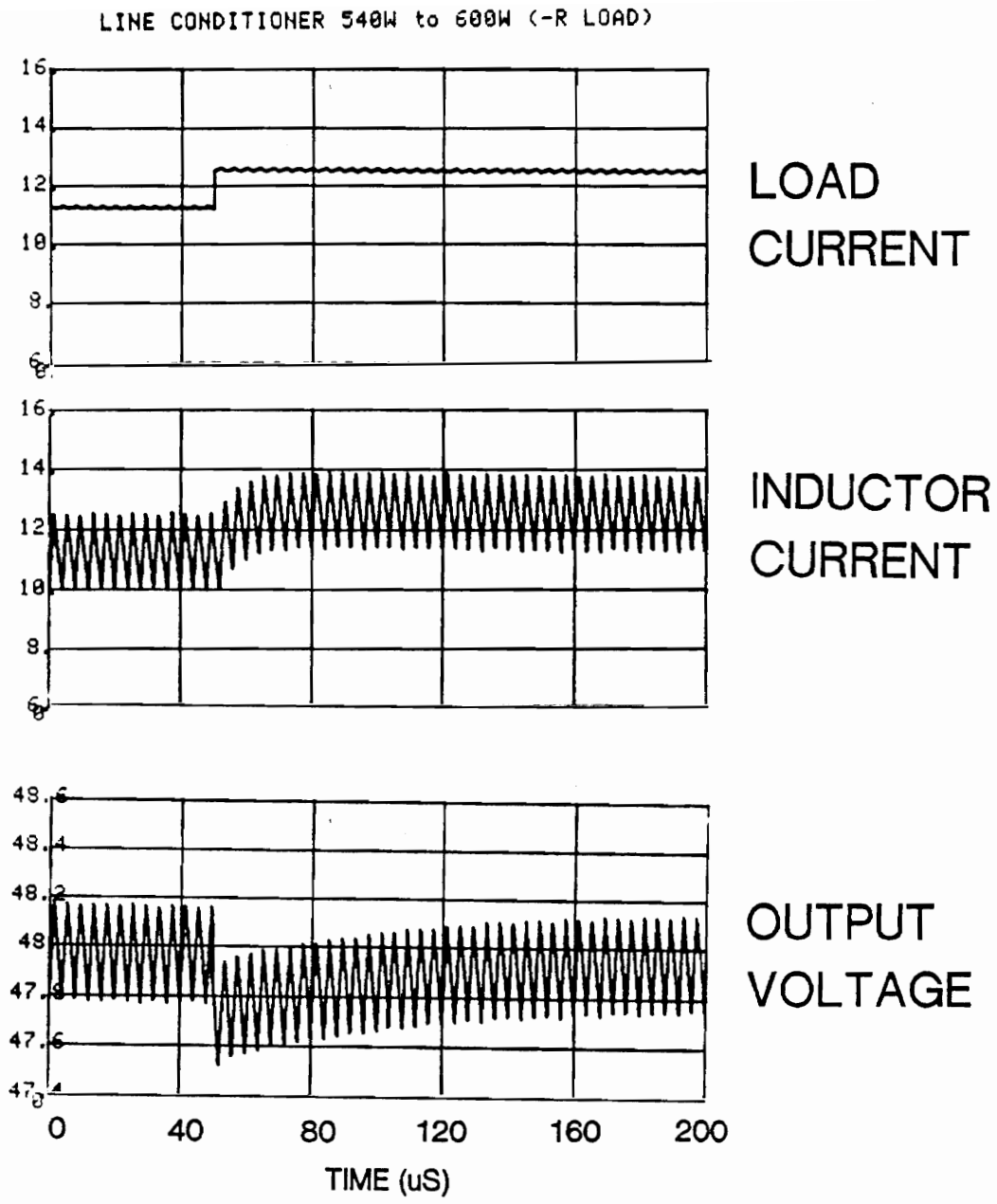


Figure 4.24. Step Load Response - Constant Power Load

load shows larger ripple and slightly worse output peaking due to effects of the negative-resistance and the output capacitor ESR. Because the line conditioner provides an intermediate bus voltage, the difference in output peaking is not important.

4.3 Effects of the Load Converter's Input Filter

The effects of a negative resistance load impedance on the line conditioner have been discussed, and methods for the analysis and design of the line conditioner with a negative resistance load have been presented. However, in an actual DPS the line conditioner will be presented with an impedance which contains frequency dependent dynamics as well as a low-frequency negative resistance characteristics. A practical two-stage DPS will have some sort of filter between the output of the line conditioner and the input of the load converters. This filter may be used for EMI suppression, avoidance of large-signal interaction caused by pulsating currents or may arise from interaction between parasitic inductance of the intermediate bus and decoupling capacitance at the input of the load converters. This section will discuss the design of filter for the intermediate bus of a DPS and the effect of the filter on the loop-gain characteristics of the line conditioner.

Although input filter design has been discussed extensively in the literature [11-13], the design of a filter for the intermediate bus of a DPS must avoid interaction with the line conditioner as well as the load converter while meeting a given attenuation requirement. As discussed in the literature [3], [11-13], a wide separation between source and load impedances at each subsystem interface is desired in order to prevent stability problems due to subsystem interaction. This leads to conflicting design goals for the intermediate bus filter. If a conventional low-pass LC filter is assumed for purpose of discussion, then the conflicting design goal be-

comes obvious if the impedances at both ends of the filter are considered. It is known from conventional filter design practice that minimizing the filter's output impedance in order to avoid interaction with the load converter generally requires keeping L small and C large. At the interface between the line conditioner and the filer/load converter, it is desirable to keep the input impedance of the filter/load converter as large as possible, which requires a large L and small C. These conflicting requirements impose a rather severe constraint on the filter design. Since the stability problems that arise when the output impedance of a filter interferes with a regulator down stream are well documented in the references above, this discussion will focus on the effects of interaction between the line conditioner and a group of load converters with input filters.

For the sake of illustration, the first example will consider a filter designed to meet the usual criteria of output impedance and attenuation. Fig. 4.25 shows a comparison between the output impedance of the line conditioner and the input impedance of the load converters without filters. The minimum spacing between the two impedances is approximately 25dB, occurring at frequencies between 3kHz and 1MHz. While this is enough separation to prevent interaction without any filters, it does not allow for the large peaks or valleys in the terminal impedances of an LC filter.

It was determined that a filter providing 35dB of attenuation at the load converter's switching frequency (500kHz) was required for EMI purposes. A single stage filter with an additional RC damping network was chosen to provide sufficient attenuation and controlled dumping. The filter was designed to meet the attenuation spec and avoid interaction with the load converter. Fig. 4.26 shows a schematic of the filter, component values and the filter's attenuation function. Fig. 4.27 shows a comparison of the input impedance of one load converter to the output impedance of the filter of Fig. 4.26. A third curve shows the output impedance of the filter when connected to the line conditioner. The absence of interaction between the filter and the load converter is verified by the loop-gain shown in Fig. 4.28.

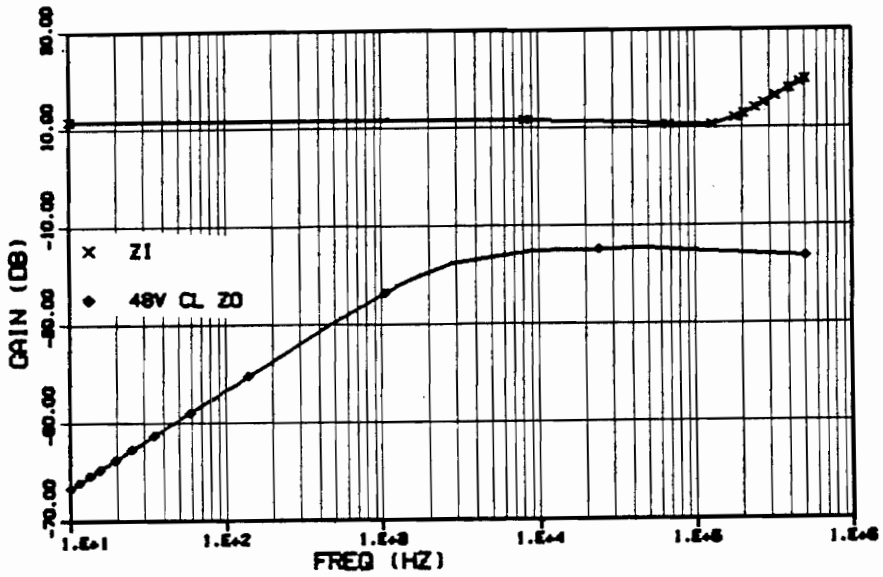
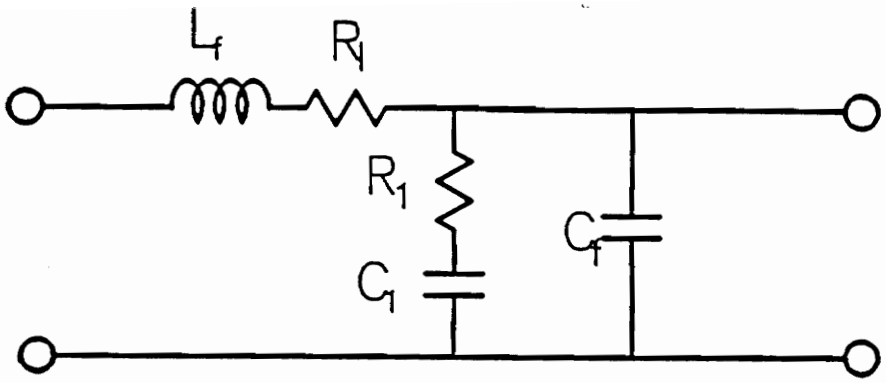


Figure 4.25. Intermediate Bus Impedance Comparison (No Filter)



Choose: $f_f = 50\text{kHz}$

$L_f = 1.0\mu\text{H}$

$C_f = 10.00\mu\text{F}$

$C_1 = 100.00\mu\text{F}$

$R_1 = 1.0\Omega$

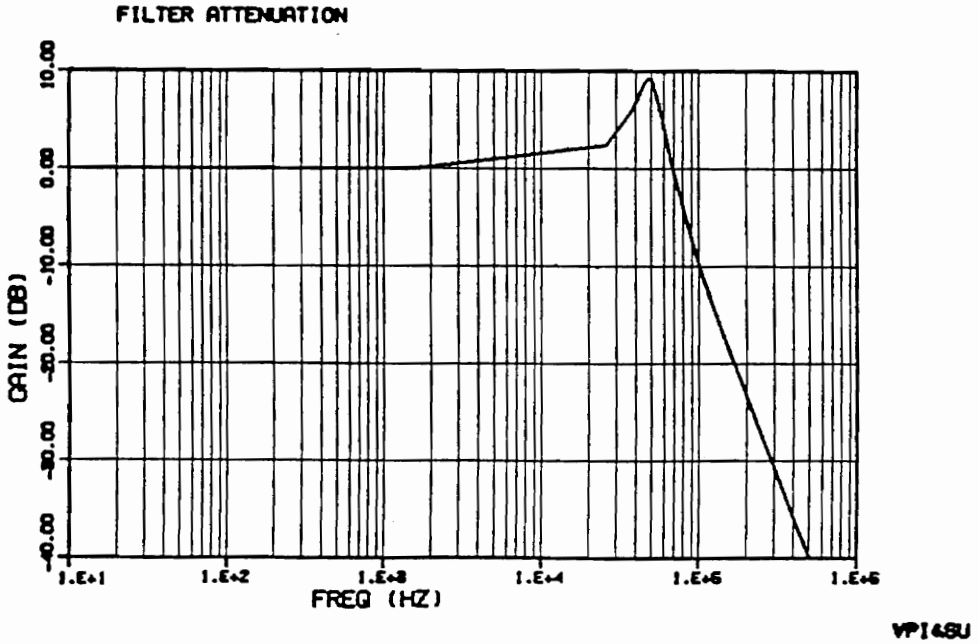


Figure 4.26. Intermediate Bus Filter

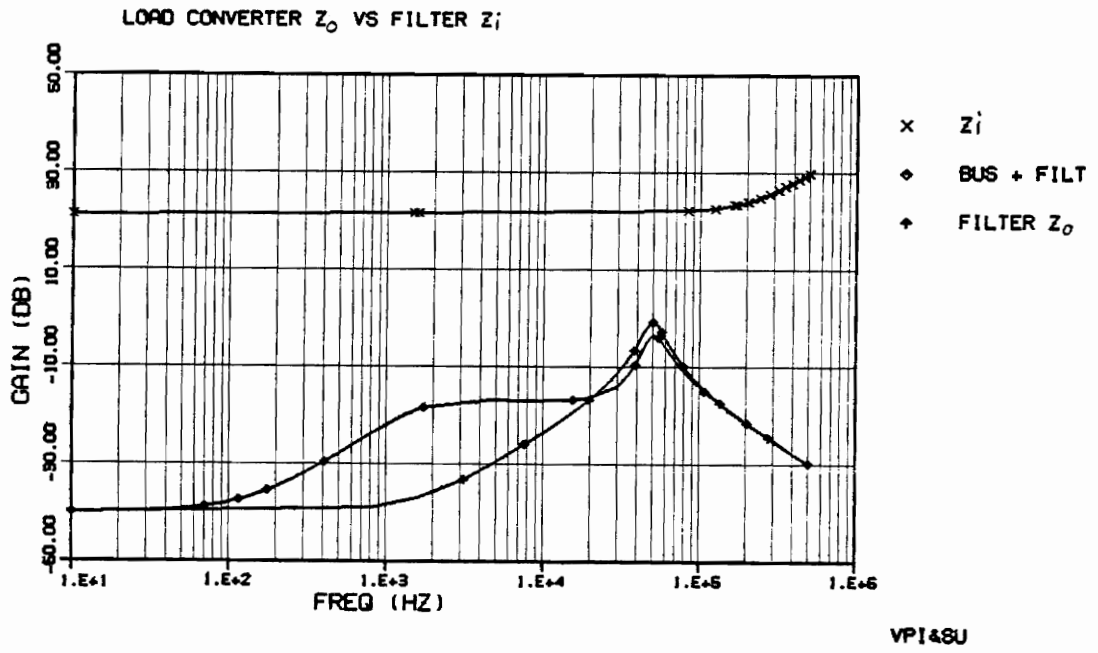


Figure 4.27. Filter/Load Converter Impedance Comparison

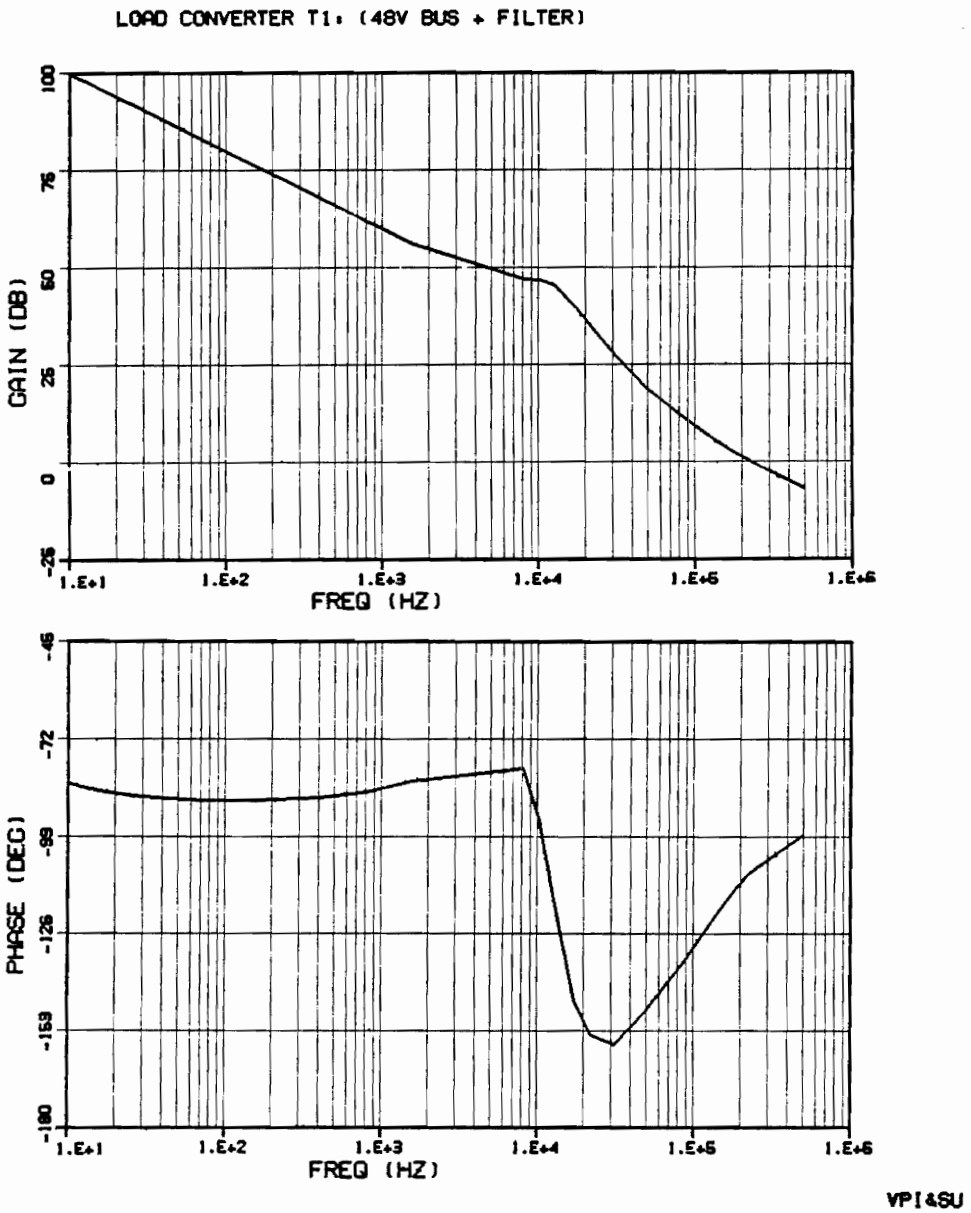


Figure 4.28. Load Converter Loop-Gain T_1 with Input Filter and Line Conditioner

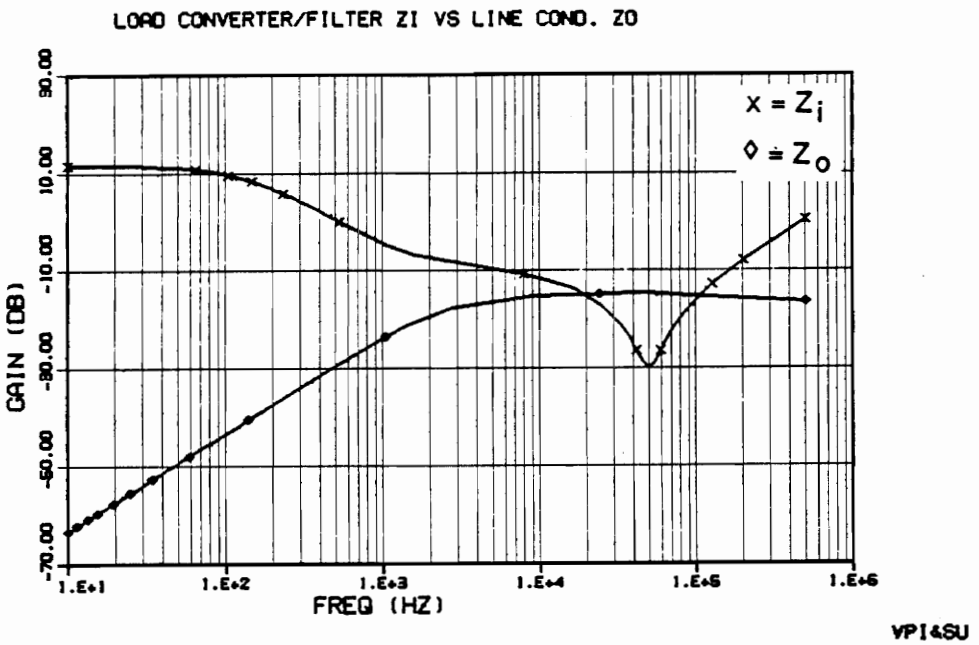


Figure 4.29. Impedance Comparison Between Line Conditioner and Load Converter/Filter Subsystem

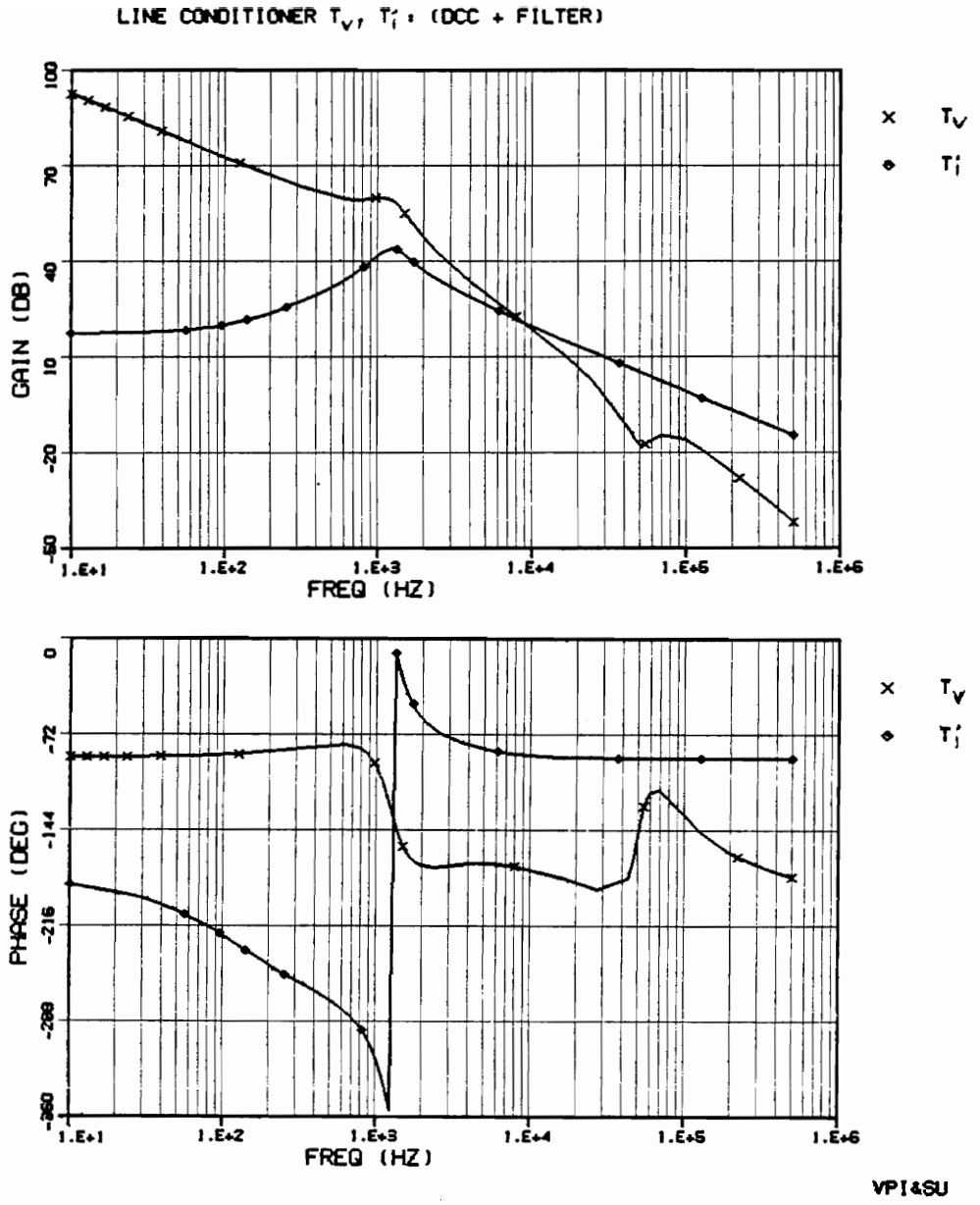


Figure 4.30. Line Conditioner Loop-Gain Components with Filter

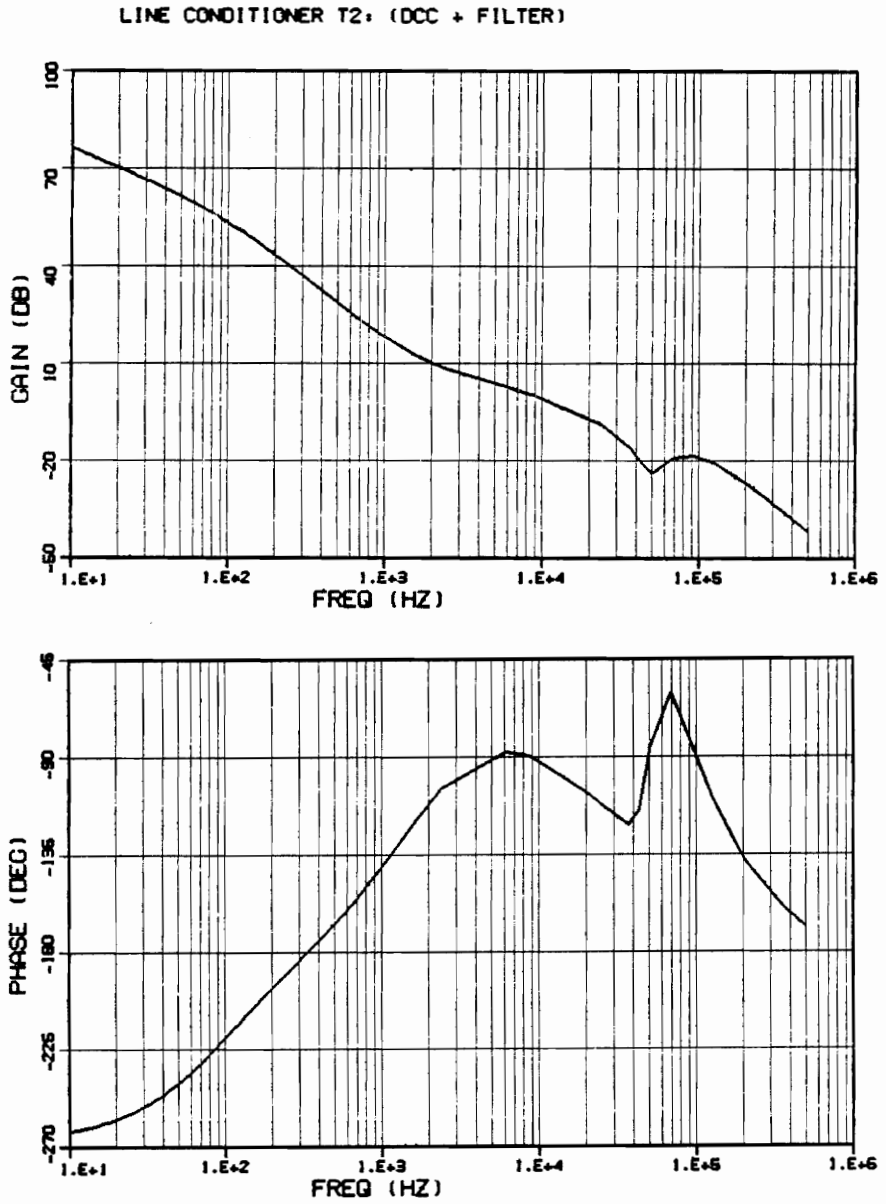


Figure 4.31. Line Conditioner Loop-Gain T_2 with Filter

Fig. 4.29 shows the output impedance of the line conditioner compared with the input impedance of three load converters with input filters. The two impedances show significant overlap in the region between 20kHz and 100kHz, so some interaction is expected. The effect of this interaction on the line conditioner is most clearly seen by looking at the loop-gain components T_i and T_v, shown in Fig. 4.30. The most obvious effect of the intermediate bus filter is the introduction of a complex pole-zero pair in T_v, near the frequencies of impedance overlap. It is important to note that since the load converter/filter subsystem was stable, the additional poles introduced in T_v by the subsystem's input impedance will lie in the left half-plane. Since these same poles are introduced into T_2, as shown in Fig. 4.31, the knowledge that they are left-half-plane poles allows the analysis procedures developed earlier in the chapter to be used with the intermediate bus filter included in the system as well.

Referring back to Fig. 4.30, it is interesting to note that the current-loop gain is unaffected in this frequency range. The reason T_i is undisturbed by the load converter/filter at these frequencies is that its shape is determined by the admittance of the effective output filter. This can be seen from the small-signal model in Fig. 4.2 by setting $\hat{v}_g$ to zero and perturbing $\hat{d}$. While T_i is sensitive to load impedance (Z_{ac}) at low frequencies, it is very insensitive to Z_{ac} at frequencies above the corner frequency of the output filter due to the low admittance of the inductor.

While T_i retains its RHP zero due to the low frequency negative characteristics of the load converter's input impedance, neither T_i nor T_v have RHP poles at the output filter's corner frequency. This is because the intermediate bus filter has interacted with the output filter of the line conditioner, shifting the open loop poles of the line conditioner's output filter back into the left half plane. This will not affect the stability analysis using T_2, since T_2 is independent of the output filter poles, but it can change the stability criteria for analysis using T_1. Fig. 4.32 shows loop-gain T_1, which now has zero RHP poles due to the damping provided by the intermediate bus filter. Comparison of Fig. 4.32 with Fig. 4.18 will show that T_1 had RHP poles for an equivalent low frequency negative resistance load.

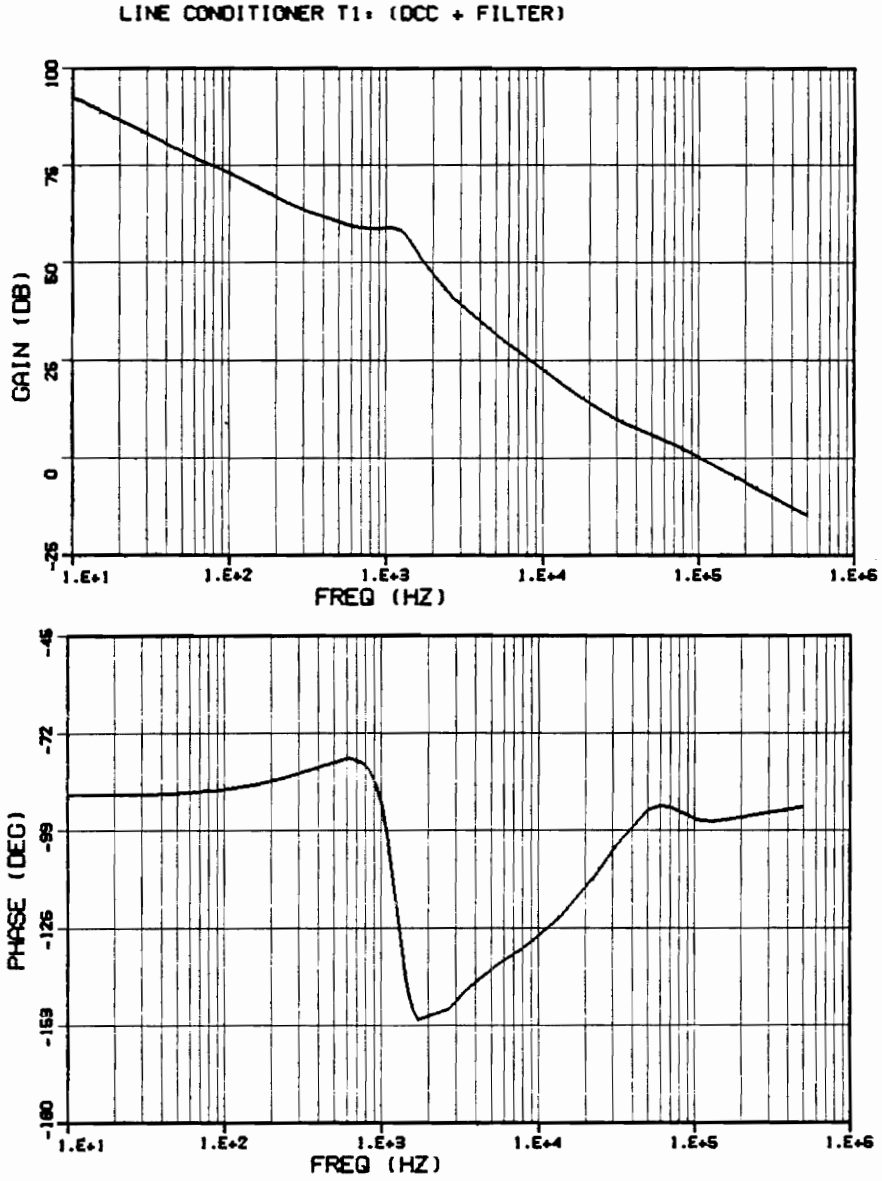


Figure 4.32. Line Conditioner Loop-Gain T_1 with Filter

Applying the stability analysis methods discussed earlier in the chapter to loop-gain T_2 in Fig. 4.31, it is observed that the system is stable, with comfortable margins for GM1, GM2 and the phase margin. Since loop-gain T_1 has no RHP poles for this case, the stability of the system may be confirmed directly from Fig. 4.32. Although the system was stable with the filter design given in Fig. 4.26, the large disturbance in the voltage-loop gain (Fig. 4.30) is undesirable since instability could occur if the voltage loop were to rise back above the current loop. An improved design method [14] was developed for the filter in Fig. 4.26, which eliminated the impedance overlap between the line conditioner and the load converter/filter subsystem. The new design improves the input impedance characteristic of the filter by allowing its output impedance to increase while still avoiding interaction with the load converter.

While the improved filter design produced a system with good characteristics, in general it may be very difficult for the designer to squeeze the impedance characteristic of the intermediate filter between the load converter's input impedance and the line conditioner's output impedance. Although the load converter's input impedance is determined by the DC load level, care should be taken when designing the line conditioner power stage. The line conditioner's output capacitor should have low ESR so as not to unduly constrain the output impedance. In some cases the use of special control techniques such as output current feedforward or input filter compensation may be required.

4.4 Summary

A modeling approach which forces the user to correctly account for the effect of load characteristics on the regulator's behavior was presented. The input impedance of the load converters was approximated by a simple negative resistance. The effect of the negative

resistance on the line conditioner was to alter the low-frequency phase characteristics of the current-loop-gain and induce RHP poles in the loop-gains. The presence of RHP poles in the loop-gains requires a return to the fundamentals of loop-gain analysis in order to determine the stability of the system. The Nyquist plot of the loop-gain can be used to define gain and phase margins, which allow the stability of the regulator to be determined from the Bode plot. However, the gain and phase margins must be redefined each time the number of RHP poles changes. The altered phase characteristics of the current-loop gain result in an additional constraint on the 0 dB crossover frequencies of both loop-gains T_1 and T_2 , which is reflected in additional gain margins. However, these constraints do not conflict with the goals of a high-performance design, allowing the use of existing design procedures. The suggested approach is to optimize the control design for a resistive load and then verify the stability of the regulator by checking that the additional constraints imposed by the new gain margins for T_1 and T_2 are satisfied.

Chapter 5

CONCLUSIONS

This thesis presents small-signal analysis methods and design guidelines for a practical distributed power system. While specific results are valid only for buck-derived switching converter topologies, the analysis methods should be similar for any DPS, regardless of converter topology. This thesis provides a small signal analysis of two key features of a two-stage DPS: the characteristics of parallel-module switching regulators and the interaction between cascaded regulators.

Chapter 2 provides a general discussion of the modeling of the system. The modeling of the system is described in detail in reference [2]. Chapter 3 presents the small-signal analysis and design of parallel module switching regulators as implemented for distributed power system applications. It is concluded that the method of paralleling modules most likely to be used in DPS applications results in a parallel module system with the same small-signal characteristics as a single module. This important result allows a system of any power level to be configured by paralleling modules which have been optimized using existing single-module procedures. Chapter 4 provides a detailed analysis of cascaded switching regulators. Loop-gain analysis is used to determine the effects of negative-resistance load impedance on the line-conditioner. It was determined that the loop-gains of the line conditioner may have right-half-plane poles, requiring a return to the fundamental application of the Nyquist Criterion to determine the stability of the regulator. It was shown that, once the number of RHP poles has been determined, gain and phase margins may be defined using the polar plot of the loop-gain. These stability margins may be translated to the Bode plot of the loop-gain, allowing the stability of the regulator to be determined directly from frequency response data. It was also determined that the negative-resistance altered the phase characteristics of the current-loop-gain, resulting in additional gain margins on both of the line conditioner's loop-gains. However, these additional constraints do not interfere with the goals of a high-performance design, allowing existing design procedures to be used. The suggested approach is to optimize the line conditioner for resistive load conditions and then verify the stability of the regulator according to the criteria in Chapter 4. Chapter 4 also discusses the effects of the load converter's input filter on the stability of the system.

Suggestions for Future Work

This thesis provides the analysis for certain key elements of a distributed power system. The analysis and simulation of the full DPS is the focus of continuing research at VPI&SU. The analysis presented here considers only buck derived switching regulator topologies. The analysis of parallel modules and cascaded regulators should be extended to boost and flyback converters and other topologies suitable for use in distributed power systems.

Appendix A

SECOND-ORDER EFFECTS OF NEGATIVE-RESISTANCE ON THE LINE CONDITIONER

In Chapter 4, two assumptions were made regarding the effects of $-R_{ac}$ on the loop-gains of the line conditioner. The first case assumed that $-R_{ac}$ has a negligible effect on the numerator of loop-gain T_1, shown in Equation 4.3. For this assumption to be true, the inequality

$$\frac{F_i}{R_{ac}} << \frac{\omega_M}{\omega_z}$$

must hold. In order to justify this assumption, first consider the compensator parameters ω_M and ω_z. It seems reasonable to assume that ω_M and ω_z will be within an order of magnitude of each other, since $\omega_M > \omega_z$ works in favor of the assumption, and $\omega_M < \omega_z$ means the compensator is attenuating the power stage control-to-output characteristic, $\frac{\hat{v}_o}{\hat{d}}$ (Eqn. 4.1), at frequencies above ω_z. Since the low-frequency gain of $\frac{\hat{v}_o}{\hat{d}}$ is determined by $\frac{N_s}{N_p} V_g$, the occurrence of $\frac{\omega_m}{\omega_z} < 1$ is most probable for off-line converters with high-voltage outputs. The assumption of $0.1 < \frac{\omega_M}{\omega_z} < 10$, therefore, seems reasonable for most designs.

The current sensing gain, F_i, represents the gain of the current-sense network from inductor current to the PWM comparator and always will be much less than unity. Finally, because the line conditioner output feeds an intermediate bus, which provides medium to high voltages and relatively low current, the magnitude of $-R_{ac}$ is expected to be fairly large. Therefore, $F_i / -R_{ac}$ is expected to be much less than 0.1, and the inequality should be satisfied. This is confirmed by the analysis in reference [6], which found that the zeros of T_1 show almost no dependence on load for a buck-derived regulator. As a numerical example, the parameter values obtained in the design example in Chapter 4 are $F_i = 0.57$, $R_{ac_{min}} = 3.54\Omega$, $\omega_M = 5.734$, and $\omega_z = 15{,}000$ This gives $\frac{F_i}{-R_{ac}} = -0.016$ and $\frac{\omega_M}{\omega_z} = 0.382$, verifying the above analysis. Although $\frac{\omega_M}{\omega_z}$ was toward the low end of the predicted range, this is expected because the line conditioner is an off-line regulator with a relatively high output voltage for a DPS line conditioner [1]. This leads to a large gain in the power stage control-to-output-voltage transfer function, and consequently the need for attenuation in the compensator.

The second assumption required that the first-order coefficient (here referred to as K*) in the denominator quadratic of T_2, as shown in Eqn. 4.4, be positive. This assumption is important for two reasons. First, K* is also a critical element in the Routh-Hurwitz tabulation of the closed-loop characteristic equation, so if it is negative, the closed-loop regulator will be unstable. Secondly, if K* is negative, it is possible for the loop-gain T_2 to have two RHP poles for the Light Load case, complicating the stability analysis of the regulator.

In order to be consistent with the notation used in previous work [6], let $K_3 = \frac{N_s}{N_p} V_g F_M F_i$. Note that $\frac{K_3}{-R_{ac}}$ is the low frequency asymptote of the magnitude of T_i. Writing T_2 in standard form using K_3 and neglecting parasitic gives

$$T_2 = \frac{F_M \omega_M \frac{N_s}{N_p} V_g}{\left(1 + \frac{K_3}{-R_{ac}}\right)s} \quad \frac{(1 + s/\omega_z)}{s^2 \frac{LC}{\left(1 + \frac{K_3}{-R_{ac}}\right)} + s \frac{\left(K_3 C + \frac{L}{-R_{ac}}\right)}{\left(1 + \frac{K_3}{-R_{ac}}\right)} + 1} \qquad (A.1)$$

As stated above,

$$K^* = \left(K_3 C + \frac{L}{-R_{ac}}\right)$$

The purpose of this discussion is to

1. Show that K* is positive for most practical designs and therefore, the stability of the regulator is not compromised by the appearance of $-R_{ac}$ in K*.

2. Show that, even if K* is negative, T_2 should still have either zero or one RHP poles, and the analysis methods and design guidelines presented in Chapter 4 remain valid.

In order to demonstrate that K* should be positive, momentarily assume that the low-frequency asymptote of the current-loop gain, $\frac{K_3}{R_{ac}}$, is much greater than 1. In this case, T_2 may be approximated by

$$T_2 = \frac{F_M \omega_M \frac{N_s}{N_p} V_g}{\left(\frac{K_3}{-R_{ac}}\right)s} \frac{(1 + s/\omega_z)}{s^2 LC\left(\frac{-R_{ac}}{K_3}\right) + s\left(-R_{ac}C + \frac{L}{K_3}\right) + 1}$$

which can be factored to give

$$T_2 = \frac{F_M \omega_M \frac{N_s}{N_p} V_g}{\left(\frac{K_3}{-R_{ac}}\right)s} \frac{(1 + s/\omega_z)}{(1 - sR_{ac}C)\left(1 + s\frac{L}{K_3}\right)}$$

It was shown in reference [6] that $K_3 = LK_1$, where $\frac{K_1}{s}$ approximates the high frequency asymptote of the current-loop and K_1 is equal to the crossover frequency of T_i. Therefore, T_2 will have poles at the current-loop zero and at $s = K_1$, the 0 dB crossover of the current-loop. Having established the approximate location of the poles of T_2, the sign of K* may be determined. If K* is negative than

$$\left(K_3 C + \frac{L}{-R_{ac}}\right) < 0$$

Multiplying both sides of the inequality by $\frac{-R_{ac}}{K_3}$ gives the equivalent inequality

$$\left(-R_{ac}C + \frac{L}{K_3}\right) > 0$$

which is true if and only if

$$R_{ac}C < \frac{L}{K_3} = \frac{1}{K_1}$$

which is equivalent to

$$\frac{1}{R_{ac}C} > K_1$$

Therefore, K* will be negative only when the zero in T_i occurs after the 0 dB crossover of T_i. Having the zero of the current-loop-gain occur above its crossover is contrary to basic assumptions made about the current loop in previous work [6], [15], and means the design is impractical since the phase of T_i would make stability nearly impossible to achieve for either resistive or negative resistance load impedances. Note that the above derivation does not depend on the previous assumption of $K_3 >> R_{ac}$. The only assumption is that $\frac{1}{R_{ac}C}$ and K_1 remain reasonable approximations to the poles of T_2.

If K* is negative it is theoretically possible for T_2 to have two RHP poles. Because the design guidelines in Chapter 3 depend on T_2 having either zero or one RHP poles, it is necessary to show that even when K* is negative, T_2 will have no more than one RHP pole for any practical design. Consider the quadratic equation in the denominator of equation A.1. If K_3 is greater in magnitude than $-R_{ac}$, the low frequency asymptote of T_i will be greater than 0 dB and the signs of the quadratic coefficient will go as (-, -K*, +). In this case, there will be one sign change between the coefficients regardless of the sign of K*, so T_2 will have one RHP pole even when K* is negative. If the magnitude of K_3 is less than that of $-R_{ac}$, so that the low-frequency asymptote of T_i is less than 0 dB, the signs of the coefficient are (+, K*, +). In this case, T_2 will have zero RHP poles if K* is positive and two RHP poles when K* is negative. It was shown above that, if K* is negative, the zero of T_i lies beyond its 0 dB crossover (and also above the filter resonance). When combined with the condition that the low-frequency asymptote of T_i be less than 0 dB, this implies that T_i is always below 0 dB, and thus has a negligible effect on the regulator. Note that as K_3 goes to zero, $T_2 \cong T_v$ over all frequencies. This is clearly an impractical implementation of current-mode-control and justifies ignoring the case where T_2 has two RHP poles. If such a case were encountered, the problem would reveal itself under resistive load conditions.

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Vita

Lucian Russell Lewis II (Rusty) was born on June 30, 1963 in Charlottesville, VA. He received the BSEE from Virginia Tech in 1986. As an undergraduate he completed a co-operation education program with General Electric in Charlottesville, VA., where he worked with programmable controllers and motor drives. Mr. Lewis entered the masters degree program at Virginia Tech in the fall of 1986 where his research interests were in power converter control and high frequency power conversion. Mr. Lewis has been employed by Inland Motor in Radford, VA. since Sept. 1986, where he works with high density power supplies.