Series DC Arc Fault Detection for a Grid-Tie Solar PV Power Generation System

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ABSTRACT

A real-time algorithm is developed for the detection of series dc arc faults in a grid-tie solar photovoltaic (PV) installation. The sensed dc bus current, which is sampled using an analog-to-digital converter with Galvanic isolation, is filtered using a wavelet-based, two-level filter bank. The filter bank, referred to as the post-processing filter, improves the robustness of the algorithm to any false tripping by rejecting power converter harmonics that are added to the dc bus current.

To determine if a fault has occurred, the algorithm calculates the variance of the filter bank output and sees if the calculated variance exceeds an upper threshold value. If the upper threshold is exceeded, and the dc bus voltage falls below a predefined lower limit for a set number of instances, the algorithm trips. The algorithm can detect a series arc fault in under two seconds and does not rely on machine learning techniques to process the sensed signal. The detection algorithm is implemented on a commercial microcontroller using C code, and the filter bank convolutions are implemented using 32-bit floating point variables.

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GENERAL AUDIENCE ABSTRACT

A device is developed for the detection of series dc arc faults in solar photovoltaic installations. Dc arc faults that result from loose connections or worn cable insulation can go unnoticed by most conventional fault detectors. Once it has ignited, the series arc can generate considerable amounts of heat and poses a significant fire risk.

By contributing to the development of a dc arc fault detection system, the intention is that dc renewable energy distribution systems, most notably solar photovoltaic installations, can gain even more widespread adoption. This would make a significant impact towards decarbonizing the energy sector and tackling the threat to society posed by climate change.

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1. Introduction

Arc-fault circuit interrupters (AFCIs) designed for ac distribution systems have been in development for quite some time [1] and numerous commercial products for ac circuits are available. To see if sustained ac arcing is present, most AFCIs look for characteristic distortion on the sensed line current [1]. While this approach is effective for most ac distribution systems, its efficacy is greatly diminished when applied to a dc distribution system [1]. Thus, new detection methods need to be developed if a robust, reliable dc AFCI is to be realized. Fig. 1 shows a system-level diagram of the solar PV power generation system considered in this paper.

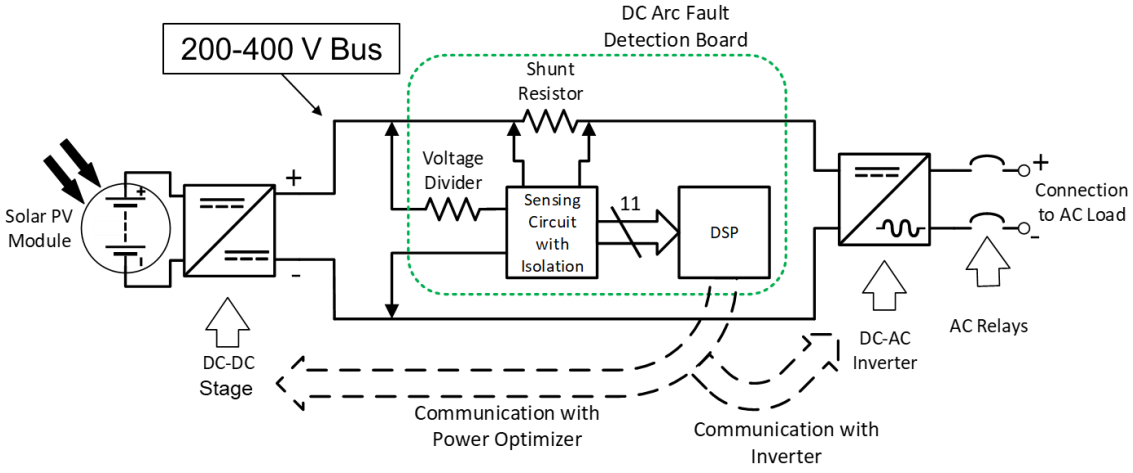

Figure 1. Diagram showing how the AFCI device senses the dc bus voltage and current and uses those signals to monitor for arc faults.

The fault detection device was designed to be placed along the dc bus connected to the input of a grid-tie voltage source inverter (VSI). It was designed to sense both current and voltage, and once a fault has been detected, notify the inverter (i.e., the VSI)

that is drawing power from the dc bus so that it can safely shut down and extinguish the arc. Unlike ac arcs, which have the potential to self-extinguish with each zero crossing, dc arcs lack the ability to self-extinguish [2]. This tends to make rapid, reliable dc arc fault detection more difficult than ac arc fault detection. Series dc arc faults, which can result from poor conductor continuity, can be difficult to detect and often require the AFCI to perform signal processing on the sensed analog signal before a determination can be made.

By communicating with the DC-DC converter, it was thought that the AFCI could enhance the robustness of the fault response by bringing the DC bus voltage to zero volts. This would extinguish any parallel arc faults along the dc bus. Any series arc faults could be extinguished by shutting down the inverter.

1.1 Scope of the Thesis

First, this paper discusses current safety and technical standards, followed by a summary of the power conversion circuits used with solar PV installations. A literature review discusses the ongoing research related to dc arc fault detection. The paper then discusses the various design elements that were considered for the AFCI device and concludes with an analysis of the testing results and a discussion of future work.

1.2 Background

The development of diagnostic algorithms is crucial for fault monitoring, and of particular importance are algorithms which look for arc faults within a dc circuit. VSIs need an input voltage of at least 180 V, along with at least 5 V to 10 V of margin, to

safely connect to a 120 V grid without becoming overmodulated. Since 2011, the National Electrical Code (NEC) has required that all solar PV circuits with dc voltages greater than 80 V be equipped with an AFCI. Standard 1699B [3] from Underwriters Laboratories (UL) details the required specifications and tests for the AFCI device. UL 1699B states that, once the arc has been initiated, the AFCI should detect or extinguish the fault within the lesser of two specified intervals, as shown in (1).

$$arg\ min\left\{2\ \text{s}, \left(\frac{750\ \text{J}}{P_{arc}}\right)\text{s}\right\} \tag{1}$$

The average arc power (P_{arc}), measured in W, is equivalent to the average voltage across the arc gap multiplied by the average current through the arc. (2) shows how P_{arc} was calculated.

$$P_{arc} = \left(\overline{v_{arc}(t)}\right)\left(\overline{\imath_{arc}(t)}\right) = (V_{arc})(I_{arc}) \tag{2}$$

Both $\overline{v_{arc}(t)}$ and $\overline{\imath_{arc}(t)}$ were averaged over two 60 Hz cycles. UL 1699B specifies values for P_{arc}, with the lowest being 300 W. The experimental results presented in [4] shows that series arcs with lower magnitudes of P_{arc} can still pose a substantial fire risk. All the series arcs generated with the detection device exhibited values of P_{arc} less than 100 W.

The specifications provided in UL 1699B detail how the arc generator apparatus should be constructed [3]. These specifications were followed during the design of the apparatus. Fig. 2 shows a diagram of the constructed apparatus. It consisted of two opposing copper rods, one of which was fixed to a block of FR4 material. A section of polycarbonate tubing was fixed to the middle FR4 block, and a second copper rod was fed through this tubing. The arcs were generated by first connecting the two copper rods,

bringing the system to the nominal power rating, and then sliding the moveable copper rod away from the fixed one.

This process, commonly referred to as the “pull-apart” method [5], was found to generate a stable dc arc and is now the recommended arc generation method in UL 1699B [5]. The ends of both rods were flat and aligned so that, when contact was made, they were completely flush with each other. Both rods had a diameter of 0.25 in. A glass rod, attached to the middle copper rod with an alligator clip, was used to slide the middle copper rod and open the arc gap. The threaded bolt was designed to catch the middle copper rod and set the maximum length of the arc gap. As an additional safety precaution, the arc generator was placed under a plastic enclosure while testing.

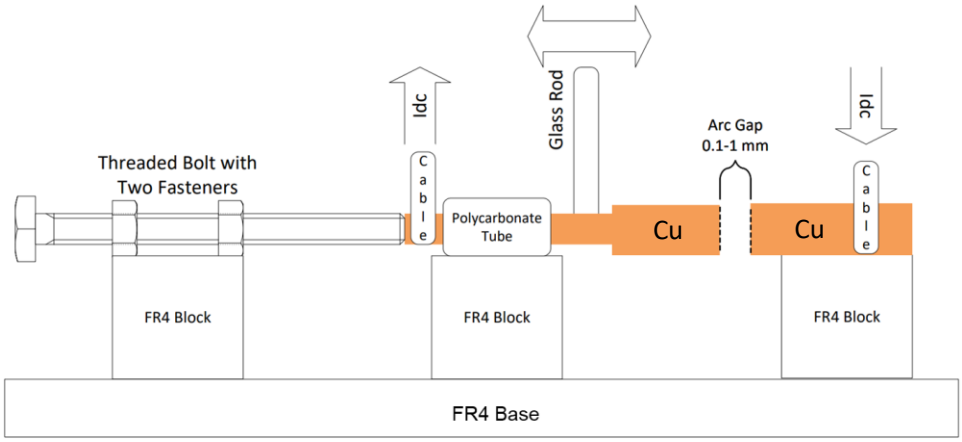

Figure 2. Diagram of the dc arc generator apparatus

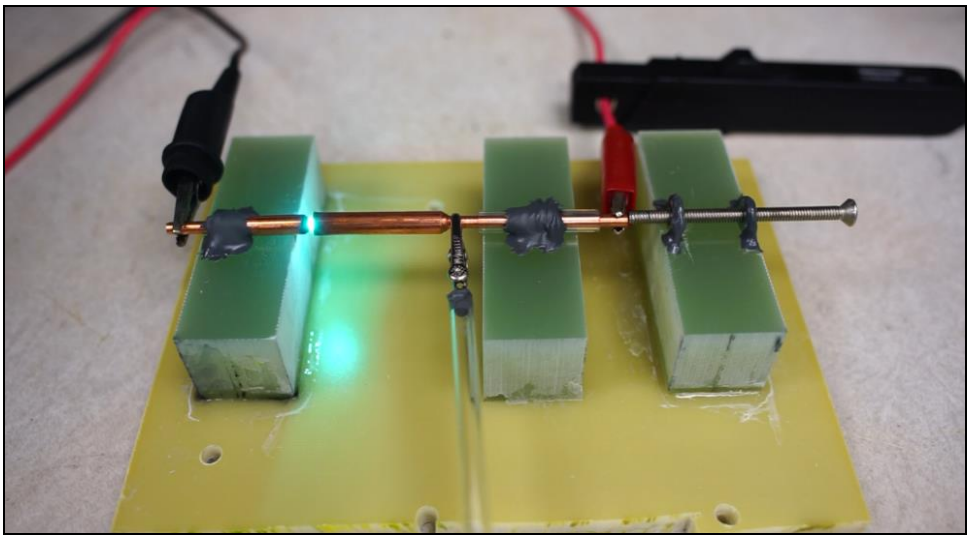

Figure 3. Picture showing an arc being generated by the apparatus.

Fig. 3 shows a picture of the apparatus generating a series arc. The arc appeared to cause the surface of the copper rods to oxidize, producing a bright green arc flash.

To efficiently convert the generated dc power to ac power, many new solar PV installations utilize either multiple microinverters or a single centralized inverter drawing dc power from multiple power optimizers [6]. Microinverters typically possess both a frontend DC-DC power optimizer stage and a DC-AC inverter stage. In both cases, the power optimizers continuously execute a maximum power point tracking (MPPT) algorithm, drawing the maximum amount of dc power from each solar PV module [7]. This distributed, “module level” approach to MPPT is an effective method for preventing a single shaded module from decreasing the power output of the entire string [6]. A downside to the distributed power optimizer approach is that the dc bus needs to be routed through cables and interconnects to the central or string inverter. With the degradation of either the electrical interconnects or cable insulation comes the possibility

of a dc arc fault [8]. Fig. 4 shows several possible locations for an arc fault for a grid-tie inverter drawing power from a string of solar PV modules.

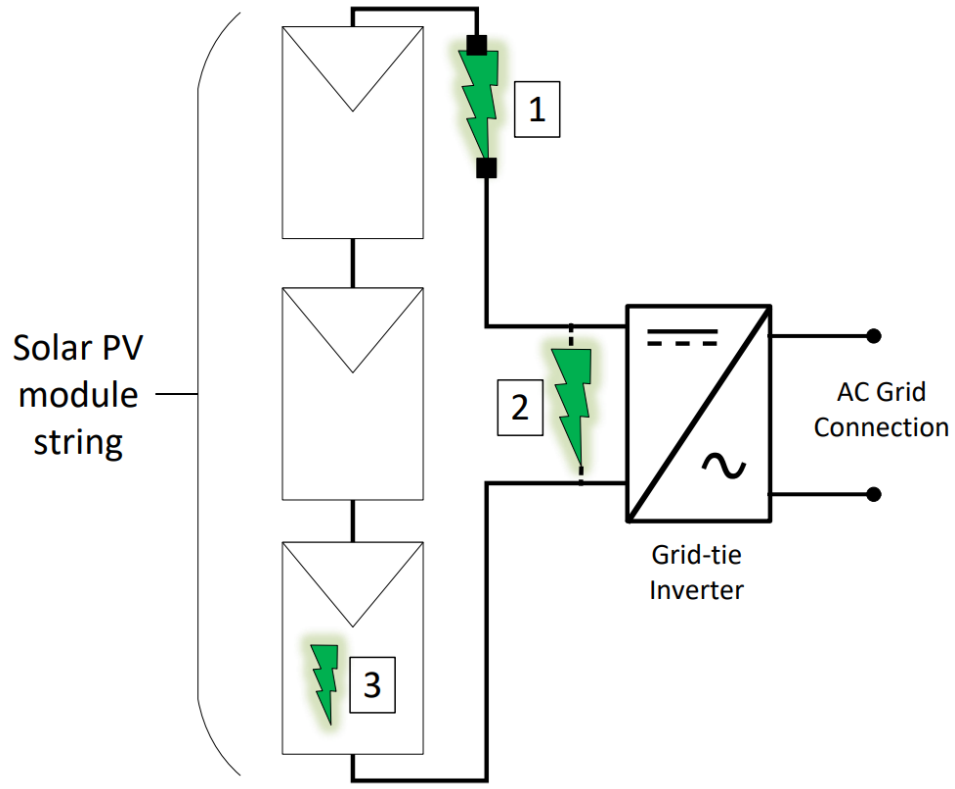

Figure 4. Possible locations for a dc arc fault in a string-based solar PV installation.

Dc arc faults are typically categorized as either series or parallel [9]. Referencing Fig. 4, location 1 shows a typical series arc fault resulting from a loose connector. Another possible cause of a series fault could involve damage to the cable insulation and underlying conductors [8]. The impedance produced by the series arc fault would induce a voltage drop and dissipate power. Location 2 shows an "intra-string" parallel arc fault [9]. This fault would cause the DC bus voltage to rapidly decrease and add a large amount of noise to the DC bus current [9]. Location 3 shows a series arc fault within a

PV module. If the system had multiple strings of modules, arcing between two strings (i.e., an “inter-string” parallel arc fault) would also be possible [5]. However, it was thought that the occurrence of an inter-string parallel arc fault would be rare. Investigating the effects of such a fault would probably be more useful for a compact dc circuit, such as the high-voltage battery bank of an electric vehicle.

The study of power system fault detection has led researchers to apply numerous signal processing techniques. Many approaches combine these signal processing techniques with machine learning to enhance the accuracy of their detection algorithms [10, 11]. These algorithms utilize the unique ability of machine learning techniques to recognize complex patterns; however, such algorithms also tend to use large amounts of power and computer memory [12]. It was concluded that, since the detection algorithm developed in this paper would be included in the same microcontroller as the control algorithms for the grid-tie inverter, a machine learning-based approach would use an excessive amount of the microcontroller’s resources. It was also thought that the machine learning approach would be best suited to large, megawatt-level PV installations. The detection algorithm presented in this paper would be most suited for kilowatt-level installations.

The windowed discrete Fourier transform (DFT) and the discrete Wavelet transform (DWT) [8] are two common signal processing transformations that have been applied to power system fault detection. The DFT converts a discrete, periodic time domain signal into a discrete, periodic frequency spectrum [13]. The DFT is implemented digitally using a Fast Fourier transform (FFT) algorithm, an algorithm which is readily available as a callable function in many popular development environments. Instead of

transforming the time domain signal into just a frequency spectrum, the DWT is an example of a combined time-frequency transform [14]. The time-frequency nature of the DWT gives it the ability to detect when specific frequency components occur in time [14]. The DWT is typically implemented digitally as a network of finite impulse response (FIR) filters, which is called a filter bank. The digital filter bank implementation of the DWT is referred to as the Fast Wavelet transform (FWT) [14]. In addition to the DWT, other digital filtering methods can be used to localize certain frequency components of the series arc fault in the time domain. A comparison of some of these other filtering methods is conducted in Chapter 2 of this paper.

Statistical methods have also been incorporated into the fault detection algorithms. They have been used on their own and have also been incorporated with the FFT to improve the detection accuracy [15]. Another statistical method that has gained recent popularity is the use of Hurst exponent analysis [16].

Many of the detection algorithms that utilize the FFT or DWT, tend to use sample rates of at least 100 kHz [8]. Megahertz-level sample rates have been used with the wavelet packet decomposition (WPD) transformation, a more computationally intensive relative of the DWT [8]. Additionally, many algorithms use Hall-effect sensors to sense the DC bus current [10, 17]. Many Hall-effect sensors tend to be either bulky or susceptible to external magnetic fields. [18] used a type of fractal antenna to monitor for a 39 MHz tone associated with an arc fault. Potential downsides to this approach are the need for a dedicated detection sensor (the antenna) and that it uses an RF signature to decide if a fault has occurred. It was thought that the presence of external RF signals could make the approach presented in [18] susceptible to false tripping. With the device

developed in this paper, a shunt resistor was used to sense the DC bus current, and the sensed signal was then band-limited using a type of moving average filter. The digitized, band-limited signal was then sent to the detection algorithm, which called a DWT function at a constant rate of 40 kHz.

By using a shunt resistor-based current sensor with a two-level DWT, the algorithm acted to be robust to detection errors induced by external noise and magnetic fields, while also being computationally straightforward by avoiding signal processing techniques that demand a high sample rate or machine learning. In past designs, the dc bus current has often been used to determine if a fault has occurred [8]. The goal of the design presented in this paper was to improve the reliability of the detection algorithm by using both the dc bus current (I_{DC}) and voltage (V_{DC}). It was thought that, if an electronic load is connected locally within the same ac distribution circuit as the inverter, the noise generated by the electronic load could be added to I_{DC} and possibly induce a false positive detection result. Thus, by incorporating V_{DC} into the detection algorithm, the goal was to reduce false detection results.

An additional goal of this research was to take the design methodologies presented in other works and show how they can be applied to a real-time detection algorithm in a microcontroller. The paper also highlights the different ways in which the fault detection can be incorporated into a two-stage solar PV power conversion system. Many other works tend to conduct a purely theoretical analysis of their proposed methods without then attempting to apply them to actual hardware. In doing so, this paper attempts to highlight the complex and varied facets inherent to the design of a dc AFCI device.

1.3 Preliminary Tests

Preliminary tests were conducted using a dc power supply, the arc generator, and a 10 Ω resistor bank. A circuit diagram of the setup is shown in Fig. 5.

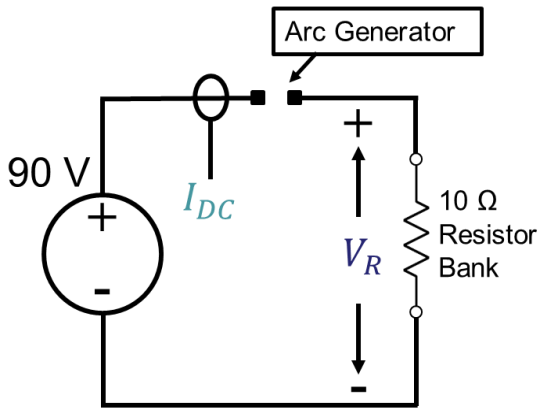

Figure 5. Circuit diagram showing the setup during preliminary testing.

The 10 Ω resistor bank acted as a current-limiting ballast resistor. Since DC arcs exhibit a negative linear V-I region [8], UL 1699B recommends using a ballast resistor in the test circuit [3]. A current clamp and differential voltage probe were used to measure the DC current: I_{DC} and the voltage across the resistor bank: V_R, respectively. The length of the arc gap was set to approximately 0.5 mm, and the arc was generated using the pull-apart method. Fig. 6 shows the current and voltage waveforms captured during the test.

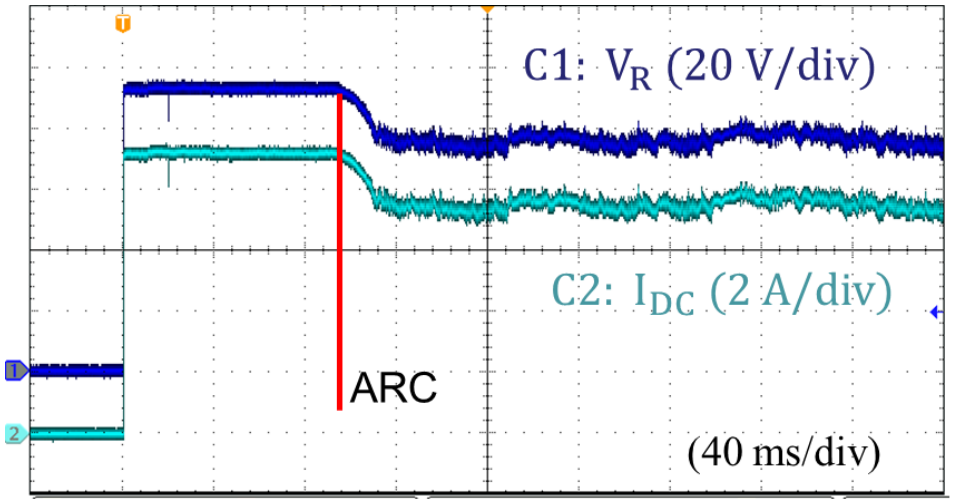

Figure 6. Waveforms captured during preliminary testing with the resistive load.

Referencing Fig. 6, after 40 ms, the contacts of the arc generator were connected. Initially some arcing appeared to be present. The evidence of this can be seen around the downward transient that appeared on both waveforms. This momentary arcing, which likely resulted from mechanical bouncing between the two contacts, appeared to resolve itself roughly 40 ms after the contacts had been closed. The red line shown in Fig. 6 marks the instance when the contacts were completely separated, and the series arc was ignited. The impedance of the series arc appeared to cause both I_{DC} and V_R to decrease in magnitude. After this, the characteristic noise and distortion were added to both waveforms.

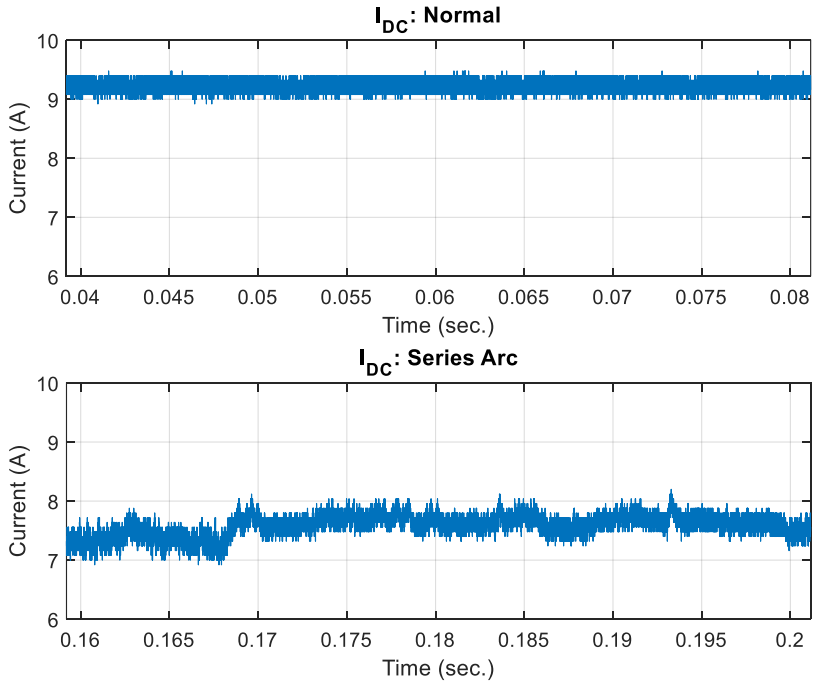

Figure 7. I_{DC} data recorded during preliminary testing with the resistive load.

Fig. 7 shows the data from Fig. 6 plotted on a smaller time scale (5 ms/div). From this, a more detailed analysis of the time domain arcing dynamics can be obtained. [5] conducts a thorough analysis of the time domain dynamics of a series arc by examining the different sub-events that take place during the arc fault. [5] identifies the "transitional arcing" state as being the primary source of noise during an arc fault. [5] shows how the arc fault tends to fluctuate between transitional and "bridged arcing" states. Bridged arcing states occur when the current magnitude increases, and the arcing noise decreases. Transitional arcing is characterized by a sharp transient decrease in current magnitude, followed by an increase in the characteristic wide-band arc noise [5]. [5] explains that the fluctuation between these two states can be attributed to changes in the resistance of the

air around the arc fault. Bridged arcing corresponds to low air resistance, while transitional arcing occurs after an increase in the air resistance.

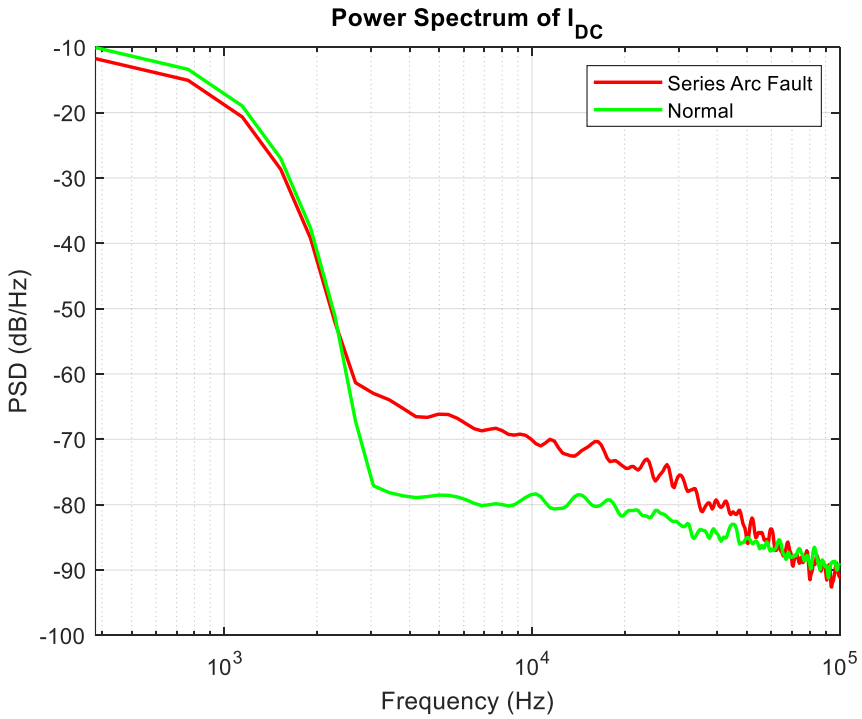

Figure 8. Power spectral density (PSD) plot of the dc current data recorded during the resistive load test.

Fig. 8 shows a power spectral density (PSD) plot of the I_{DC} waveforms shown in Fig. 7. The PSD was calculated using the Welch's power spectral density estimate (pwelch) function in MATLAB. The plot shows how the noise generated by the series arc fault produced a significant increase in the noise floor, particularly within the 3 kHz to 50 kHz frequency band. Referencing Fig. 8, the generated noise was approximately linear within the 3 kHz to 50 kHz frequency band. This implies that the series arc fault can be approximated as a source of pink ($1/f$) noise. It was determined that the detection algorithm could monitor this frequency band, and when the magnitude of this frequency

band increased above a baseline value, a series arc would be detected. It was concluded that additional testing with an inverter would need to be completed. The inverter, along with any other power converter connected to the DC bus, would add harmonics to I_{DC}. For a 60 Hz grid-tie VSI, it was thought that the most significant harmonics on I_{DC} would be the double-line frequency (120 Hz) ripple and the switching harmonics. The 120 Hz ripple results from the inverter possessing a finite amount of input capacitance [19]. In addition to maximizing the input capacitance of the inverter, control algorithms can also be used to attenuate the 120 Hz ripple [19]. Of the switching harmonics, it was thought that the fundamental harmonic would produce the most interference. Thus, by attenuating both the 120 Hz ripple and fundamental switching harmonic, the detection algorithm could observe the magnitude of the desired frequency band with minimal interference.

2. Signal Processing Considerations

The AFCI device must continuously monitor the dc bus voltage and current for any irregularities. Numerous time domain and frequency domain techniques have been applied by engineers when developing real-time algorithms that analyze the dc bus voltage and current [20]. The approach taken in this paper involved first band-limiting the sensed signal by passing it through a CIC filter. The signal was then sent to post-processing filters which acted to remove both the dc component and switching harmonics. The variance of the signal was then computed and used to determine if a fault had occurred.

A microcontroller was used to perform the digital signal processing operations that were described in the previous section. Microcontrollers developed in recent years by

companies such as Texas Instruments [21] and Infineon [22] possess numerous control and communication peripherals. Historically, two of the most critical peripherals for the closed-loop control of power converters have been the ADCs, usually a non-isolated successive approximation (SAR) architecture, and the pulse-width modulation (PWM) generator modules. With the growing popularity of isolated delta-sigma ADCs, many 32-bit microcontrollers now contain a set of cascaded integrator-comb (CIC) filters [21] as a peripheral device. Also referred to as "sinc" filters, due the shape of their magnitude responses in the frequency domain, they act to both filter and down-sample (i.e., decimate) the bitstream produced by the delta-sigma modulator [23].

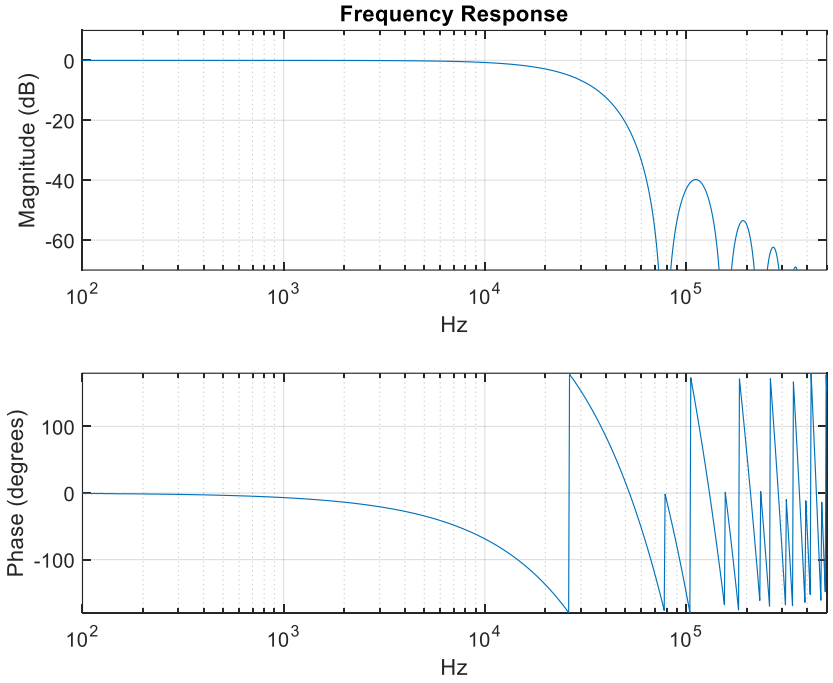

Figure 9. Bode plot showing the frequency response of a 3rd-order CIC filter. The sample rate was 20 MHz with an OSR of 256.

2.1 Analyzing the CIC Filter

Fig. 9 shows the frequency response of a 3rd-order CIC filter. With a modulator sample rate of 20 MHz and an oversampling ratio (OSR) of 256, the sample rate at the output of the CIC filter is about 79 kHz. Notice how, after the -3 dB cutoff frequency at 21 kHz, the filter provides significant attenuation along with notches at multiples of the data rate. (3) shows the transfer function for a 3rd-order CIC filter.

$$H(z) = \left(\frac{1}{(OSR)}\frac{1 - z^{-(OSR)}}{1 - z^{-1}}\right)^3 \tag{3}$$

Where: OSR was set to 256.

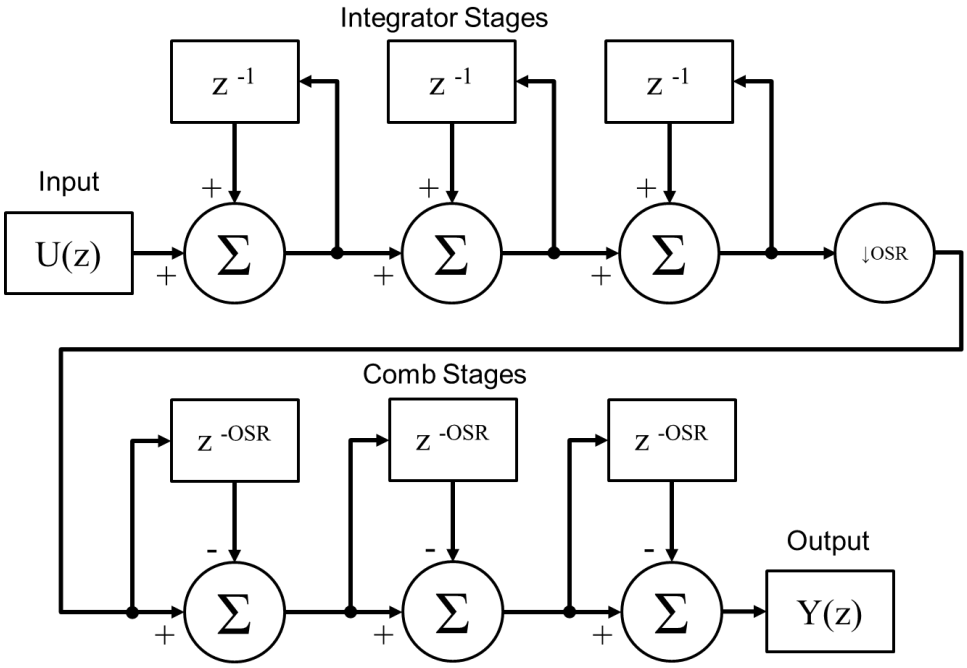

Figure 10. Block diagram of a 3rd-order decimation-type CIC filter.

Fig. 10 shows a block diagram of a 3rd-order decimating CIC filter corresponding to the transfer function shown in (3). The author of [23] discusses how a CIC filter can be

viewed as a computationally efficient moving average filter. The computational efficiency is because it solely consists of summations and delays and does not contain any multiplication operations. The integrator stages give the filter a lowpass roll off at high frequencies, and the comb stages provide attenuating notches at multiples of the data rate [23]. If a peripheral bank of CIC filters were not available in the selected microcontroller, they could still be implemented in the program code. Field-programmable gate arrays (FPGAs) have also been used to implement CIC filters [24].

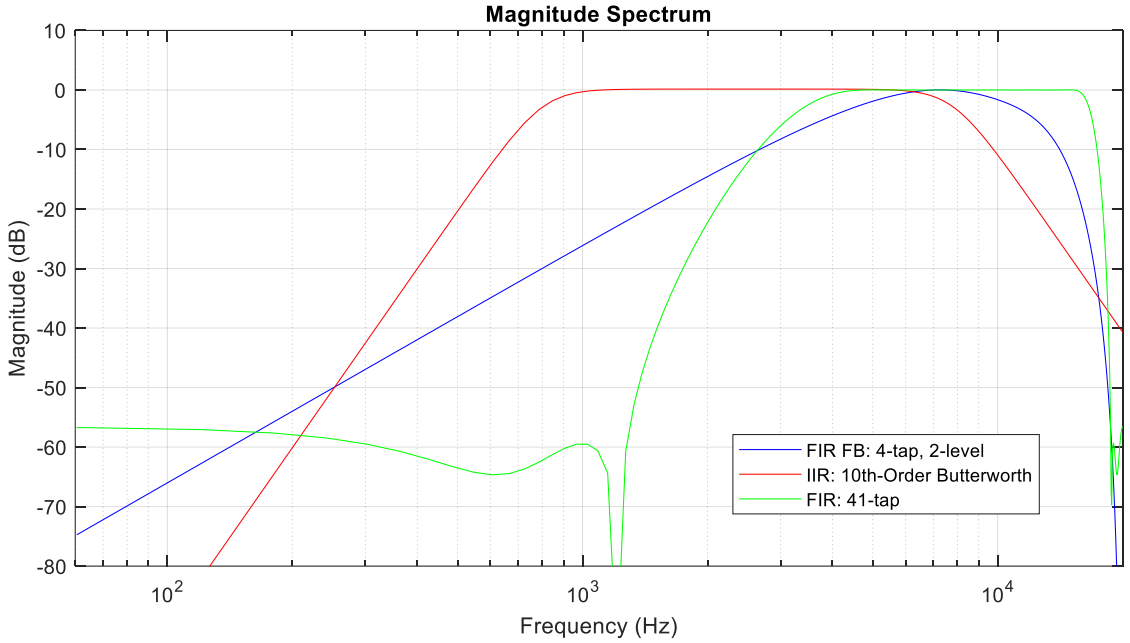

Figure 11. Magnitude responses for the three digital filters, plotted from 60 Hz to 20 kHz. A 40 kHz sample rate was used.

2.2 Selecting a Post-Processing Filter

When implementing the DWT, numerous mother wavelets can be chosen to be used with the filter bank. The Daubechies family of wavelets have been the most popular for detecting discontinuities induced by arc faults [8]. The popularity of the Daubechies

wavelets for detecting transients is due, in part, to the fact that they possess an "extremal phase" [25]. An extremal phase allows Daubechies wavelets to detect sharp discontinuities more quickly than other wavelets with equivalent impulse response lengths [25]. It was for these reasons that a Daubechies mother wavelet (db2/D4) was selected for the filter bank implemented in this paper. In addition to the DWT filter bank, two other digital filtering methods were tested. These included both infinite impulse response (IIR) and FIR filters. The IIR filter was a 10^{th}-order Butterworth bandpass, and the FIR filter was a 40^{th}-order (41-tap) bandpass filter created using the "designfilt" function in MATLAB. Fig. 11 shows the magnitude curves for all three digital filters.

When designing both the FIR filter and the IIR Butterworth filter, the primary goals were to maximize the passband size while still providing sufficient attenuation of the interfering harmonics. The 10^{th}-order IIR Butterworth filter was designed by placing five poles on both sides of the passband. The highpass poles were placed at 800 Hz, and the lowpass poles were placed 7.8 kHz. For the 41-tap FIR filter, the first cutoff frequency was placed at 3 kHz, and the second cutoff frequency was placed at 17 kHz. The order was selected such that both the 120 Hz ripple and 20 kHz switching harmonic would be attenuated by a least 50 decibels. The designfilt function used a least-squares approximation to design the FIR filter magnitude response. It was observed that, when compared to the 41-tap FIR, the Butterworth filter tended to pass lower frequency signals while simultaneously attenuating more of the 120 Hz ripple. The opposite was true for higher frequencies, where the 41-tap FIR exhibited a larger passband while still attenuating more of the 20 kHz harmonic than the Butterworth filter.

By providing adequate attenuation of both interfering harmonics and maintaining a sufficiently large passband, the magnitude response of the wavelet filter bank appeared to be a good compromise, when compared to the other two filters. Additionally, the filter bank would have a considerably lower computational complexity than the other two filters. It was thought that, due to its large number of poles, the IIR filter would be especially difficult to implement from a numerical standpoint.

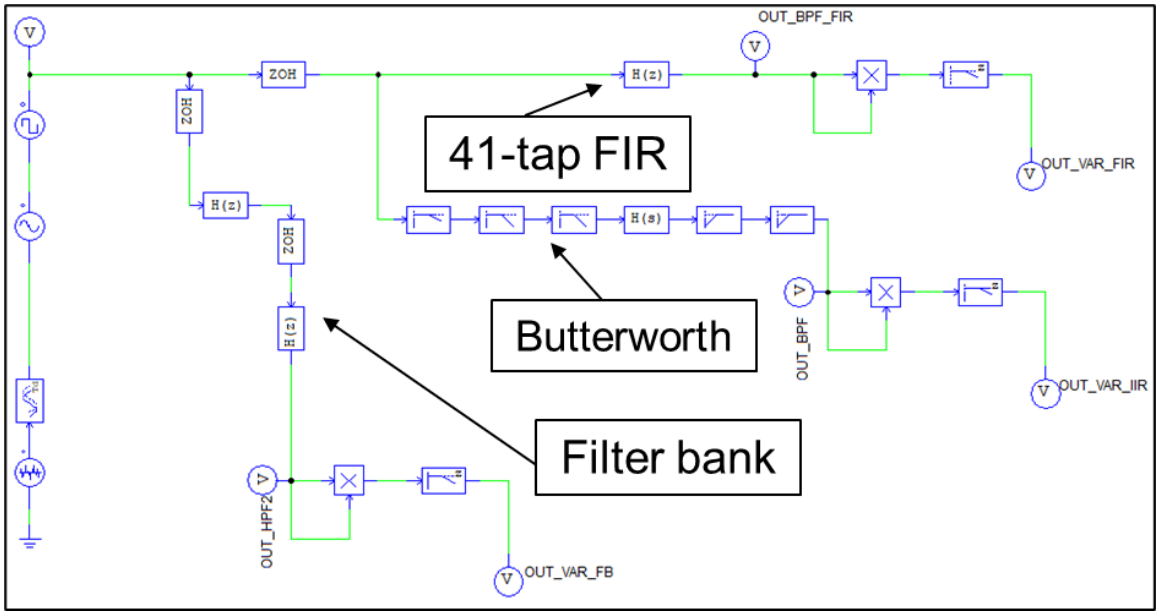

Figure 12. PSIM simulation used to test the different filtering methods.

A PSIM simulation, shown in Fig. 12, was used to compare the different filtering techniques. The simulation consisted of three parallel signal paths, all of which were connected to multiple series-connected voltage sources which acted to model the dc bus current. The output value of each signal path was then squared and passed through a lowpass filter to approximate the variance of the filtered signal.

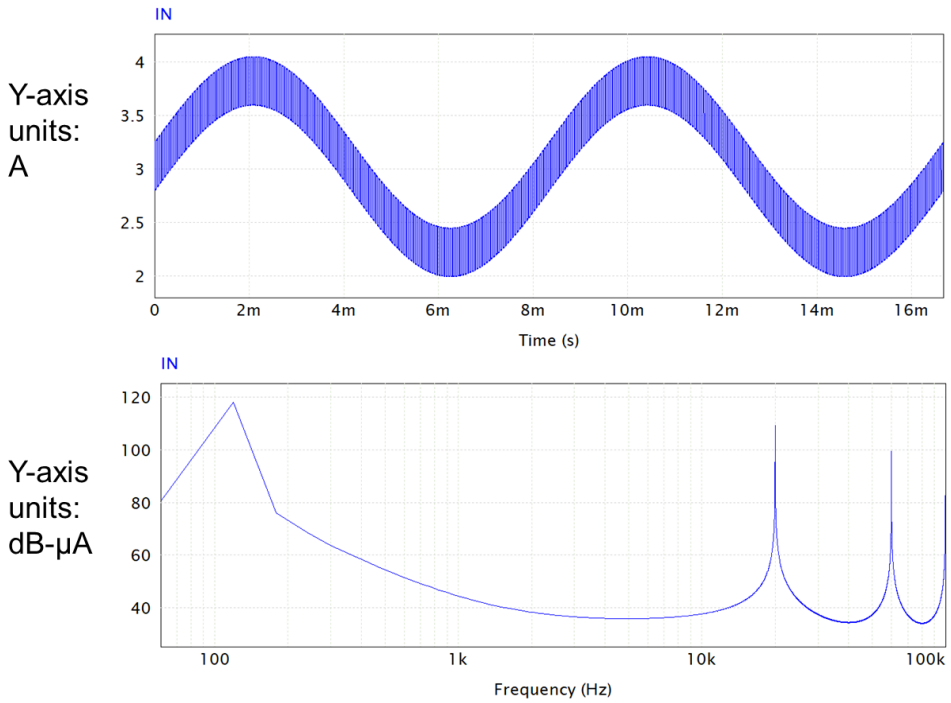

Figure 13. Simulated waveform and spectra of I_{DC} under normal operating conditions.

The top plot of Fig. 13 shows the I_{DC} waveform produced by the PSIM simulation, and the bottom plot shows the spectrum of I_{DC}. I_{DC} was modeled using a 120 Hz sinusoidal voltage source in series with a 20 kHz square wave voltage source. Both voltage sources acted to replicate the switching harmonics added to I_{DC} by the inverter. The DC offset for the sinusoidal voltage source was set to 3 V/A, and the peak-to-peak ripple was 2 V/A. The peak-to-peak value for the square wave was set to 0.45 V/A.

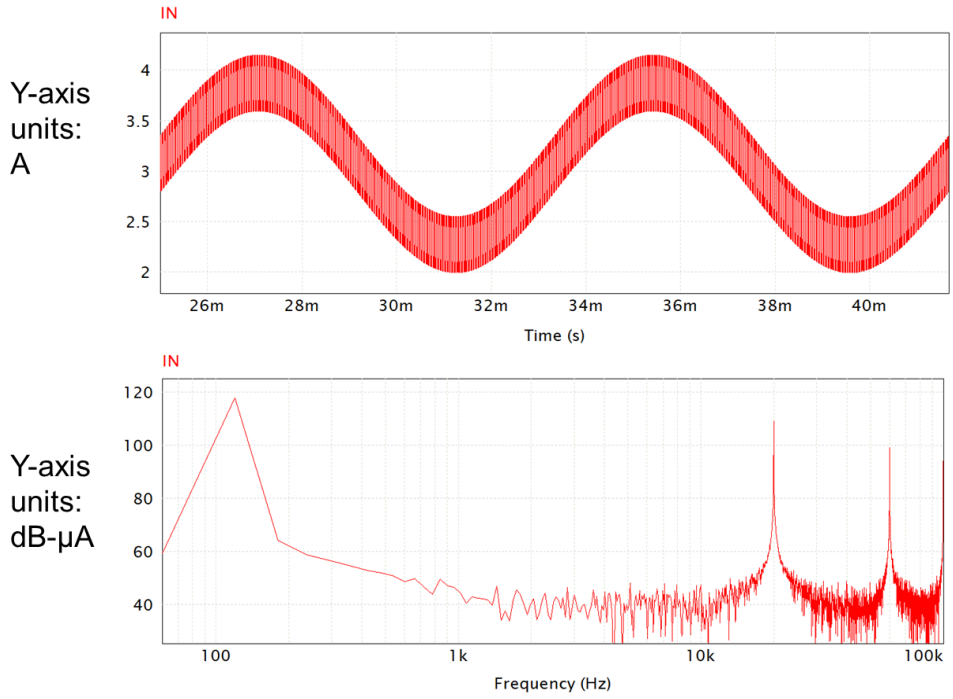

Figure 14. Simulated waveform and spectra of I_{DC} after an arc fault. A random voltage source was used to model the arc noise.

The top plot of Fig. 14 shows the arcing I_{DC} waveform produced by the PSIM simulation, and the bottom plot shows the simulated spectrum of I_{DC}, during a series arc fault. A white noise voltage source, placed in series with the DC and sinusoidal voltage sources, was used to model the series arc fault. After comparing Figures 13 and 14, it was concluded that the noise source adequately replicated the noise produced by a series arc fault within the 3 kHz to 20 kHz frequency band. The peak-to-peak amplitude of the noise source was set to 0.1 V/A. A possible drawback to the simulation was that it did not account for measurement noise. The measurement noise would cause the filters to behave worse when implemented in an actual device. It was concluded that additional averaging could be used to offset any adverse effects resulting from measurement noise.

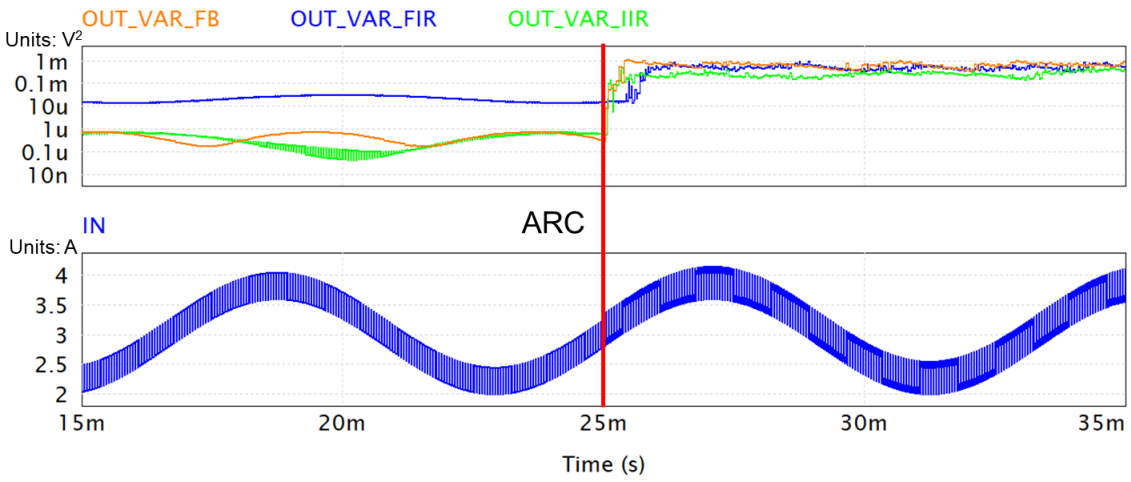

Figure 15. Waveforms produced by the PSIM simulation.

Fig. 15 shows the results from the PSIM simulation of the three different filters. Table 1 shows the average filter output variance values prior to and after the noise source had been activated. All the variance values had units of V^2.

Table 1. Average Values: Filter Output Variances

Filter	**Normal**	**Arc Noise**
D4, 2-level Filter Bank	0.564e-06	7.823e-04
41-tap FIR	2.4e-05	5.796e-04
IIR Butterworth	0.656e-06	3.05e-04

The data in Table 1 shows how the variances produced by the filter bank exhibited the largest ratio between the normal and arcing states. The IIR filter appeared to exhibit a similar time domain response as the filter bank, with a slightly smaller ratio between the normal and arcing states. The 41-tap FIR filter could not sufficiently attenuate the 120 Hz ripple and DC components, causing it to have the smallest ratio between the normal and

arcing states. In summary, the filter bank using the Daubechies 2 (db2) FIR filters seemed to achieve a good compromise between harmonic attenuation, passband size, and computational complexity and was selected as the I_{DC} post-processing filter.

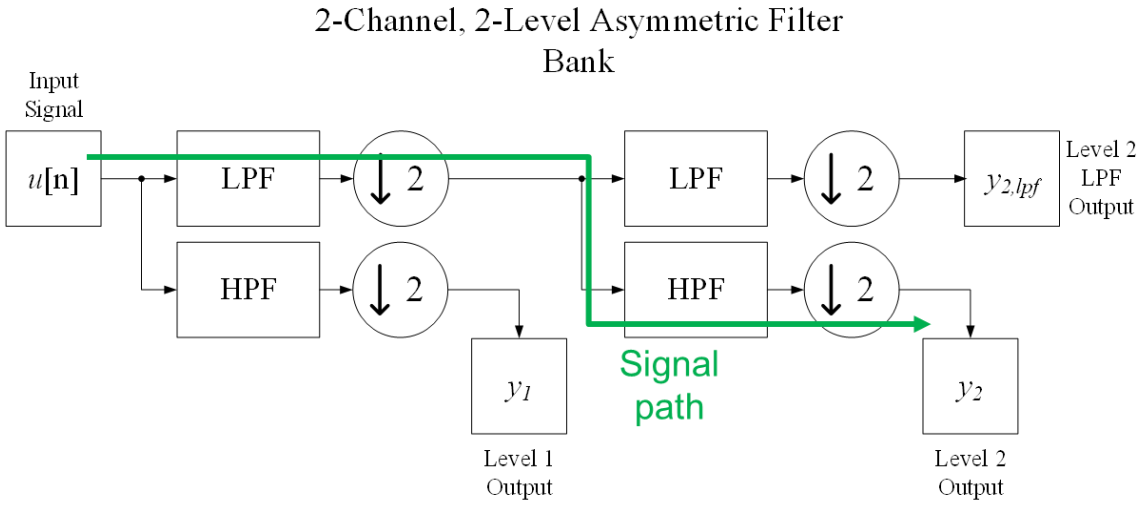

Figure 16. Block diagram showing a two-level asymmetric analysis filter bank.

Fig. 16 shows a block diagram of an asymmetric analysis filter bank; the selected signal path has been highlighted using a green arrow. Table 2 shows the coefficients for the Daubechies 2 set of filters [14].

Table 2. Daubechies 2 (db2/D4) Filter Coefficients

Index	**LPF:** h_0	**HPF:** h_1
0	-0.1294095226	-0.4829629131
1	0.2241438680	0.8365163037
2	0.8365163037	-0.2241438680
3	0.4829629131	-0.1294095226

$$y_{1,lpf}[n] = \sum_{k=0}^{N-1} (h_0[k])u[n-k] \quad (4)$$

$$y_2[n] = \sum_{k=0}^{N-1} (h_1[k])y_{1,lpf}[n-2k] \quad (5)$$

(4) and (5) show the convolutions that were used to implement the filter bank. After each sample was retrieved, the buffer was then passed as an input to the DWT function. Fig. 17 shows how the filter bank acted to isolate the arc fault wideband noise by attenuating the 120 Hz and 20 kHz harmonics produced by the inverter.

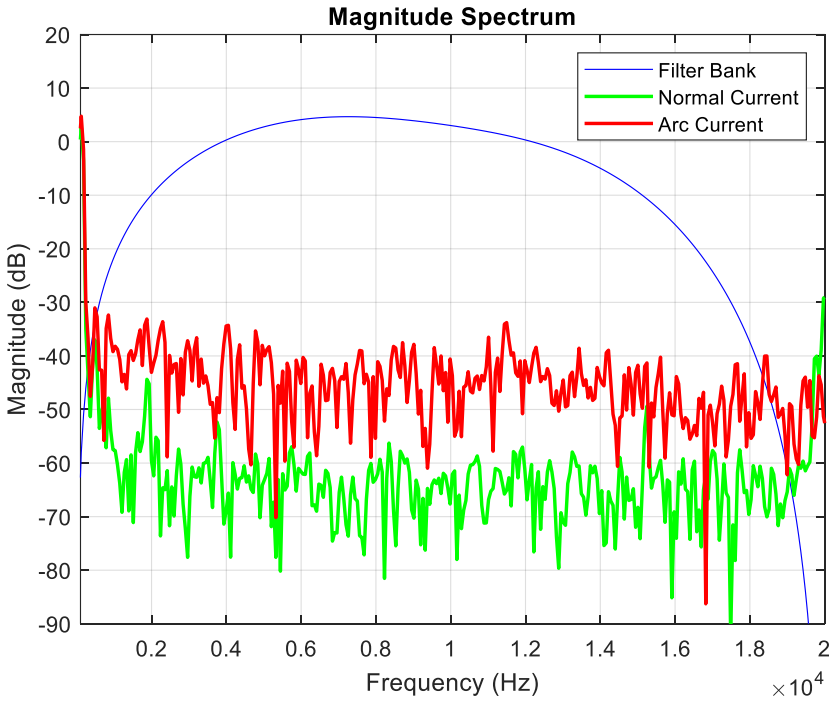

Figure 17. Magnitude spectrum of the dc bus currents with the theoretical magnitude response of the filter bank.

After eight filter bank output values ($y_2[n]$) were collected, the variance, or power, of Y_2 was approximated using (6).

$$Var(Y_2) = \frac{1}{N}\sum_{n=0}^{N-1}(y_2[n])^2 \quad (6)$$

Where: n is the sample index, and N, equal to 8, is the sample size. The variance calculation acted as an envelope detector for $y_2[n]$ and thus allowed for an upper detection threshold to be used. At system startup, both a baseline value and an upper threshold value were set.

$$\varepsilon = (threshold) + (baseline) \quad (7)$$

The values for the upper threshold and baseline were set after conducting preliminary testing. The baseline value for the variance would cease to update if the Boolean expression (8) was found to be true.

$$(Var(Y_2) > \varepsilon)\ AND\ (V_{DC} < 186\ V) \quad (8)$$

Additionally, if (8) was found to be true, an integer value, referred to as fault count, would increment. Each additional time that (8) was found to true, the fault count variable would increment. Once the fault count reached its maximum value, the detection algorithm would trip.

To use its sampled value in the detection algorithm, it was thought that the regulation of V_{DC} would need to be periodically halted. In most grid-tie PV installations, the inverter is used to regulate V_{DC} [26]. By periodically disabling the regulation of V_{DC}, the inverter could see if it deviates a certain amount beyond the set value. If this occurs, and the post-processing filter monitoring I_{DC} detects a rise in the noise floor, the inverter could determine that a series arc fault has formed somewhere along the DC bus. This was thought to be similar to the approach taken by most anti-islanding detection algorithms,

which periodically add a perturbation to the grid frequency to see if the grid is still operational. For the arc fault detector, the algorithm would disable the regulation of V_{DC} and look for a perturbation on it to determine if a fault has occurred.

3. Circuit Design Considerations

Of particular importance to delta-sigma (or sigma-delta) modulation has been its use with analog-to-digital converters (ADCs), where it can be used to produce precision ADCs with galvanic isolation between the analog and digital interfaces. A first-order delta-sigma modulator is shown in Fig. 18 and consists of a difference junction (the delta component), an integrator (the sigma component), a comparator, and a DAC. The comparator acts as a 1-bit ADC, and the DAC, per [27], "[maintains] the average output of the integrator near the comparator's reference level." The bitstream produced by the modulator possesses better noise immunity than an analog signal and can be interfaced with fiberoptic transmitters when additional isolation from high voltages is needed [28].

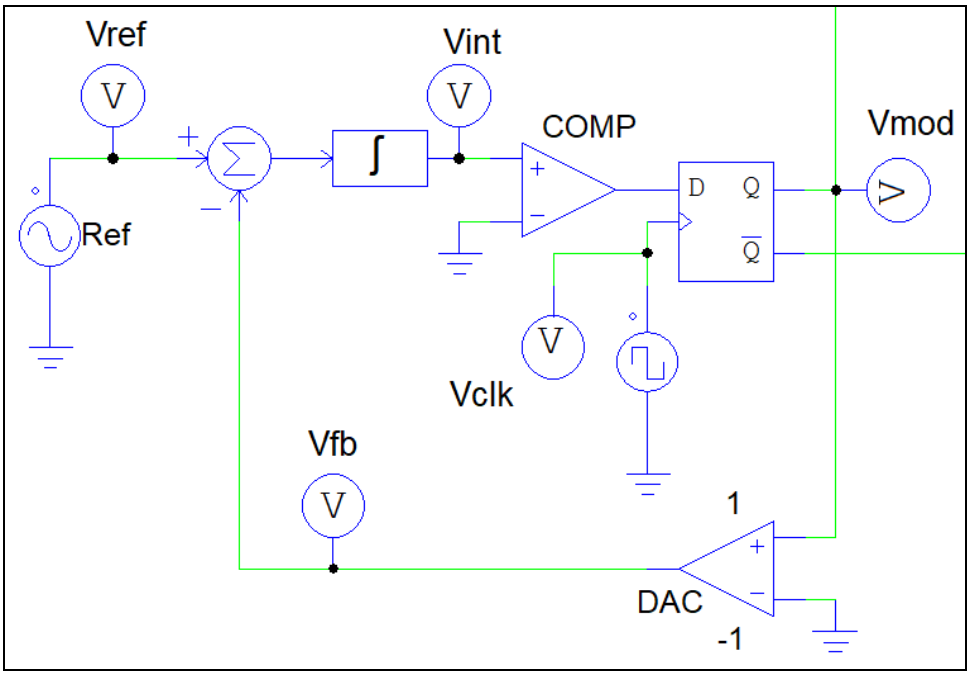

Figure 18. PSIM block diagram of a 1st-order delta-sigma modulator. The frequency of the D flip-flop clock signal (Vclk) was set to 100 kHz.

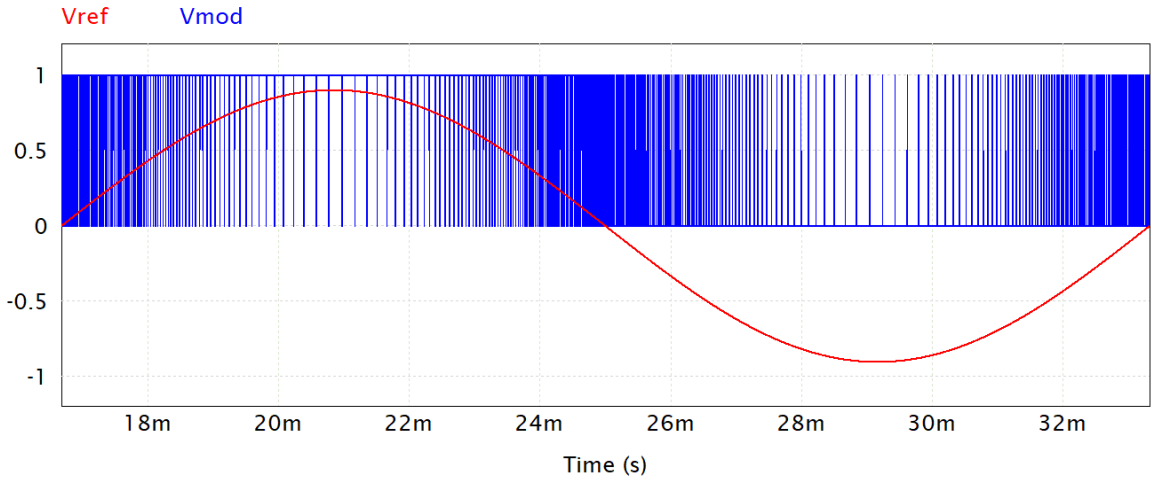

Figure 19. Waveforms produced by the delta-sigma modulator PSIM simulation.

Fig. 19 shows two waveforms from the PSIM simulation. The input voltage signal “Vref” was a pure 60 Hz sine wave with an amplitude of 0.9 V, and “Vmod” was the digital bitstream produced by the modulator. As can be seen from the plot, the density of one’s increased as the input signal approached 1 V and then decreased as the input approached -1 V.

3.1 Hardware Selection

Table 3 shows some selected dc current sensors that exhibit Galvanic isolation. The first sensor listed is a closed-loop Hall effect type sensor, and the second is an open-loop type Hall effect sensor. The third is an isolated delta-sigma modulator with a shunt resistor, and the fourth option is an isolated amplifier with a shunt resistor. Internally, the TLP7820 achieved isolation using a delta-sigma modulator and demodulator, which acted as a DAC and produced two analog outputs [29].

Table 3. Isolated DC Current Sensor Comparison

Index	Part Designation	Sensor Architecture	Current Rating (A)	3-dB BW (kHz)	Typ. Offset Error (mV)	Max. Supply Current (mA)	Unit Cost / 1,000 Units ($)	L (mm), W (mm), H (mm)
1	HX 05-P	C-L Hall Effect	±5	50	15	±15	13.62	19, 15, 20
2	ACS722LLCTR-05AB	O-L Hall Effect	±5	20, 80	20	12	1.92	5, 6, 1.6
3*	AMC1303M0520 with 15 mΩ resistor	Isolated Δ-Σ Modulator	±4	Function of OSR	0.0025	13	5.66	20, 8, 2.8
4*	TLP7820 with 75 mΩ resistor	Isolated Amplifier	±4	230	0.9	22	3.30	20, 8, 2.1

*The current rating, unit cost, and dimensions include the presence of a 2512-size SMD shunt resistor.

It was concluded that the isolated delta-sigma modulator with a current shunt would be the best option for the given application. The following factors were considered when reaching that conclusion.

- Lowest offset error voltage
- The measurement error is less susceptible to external magnetic fields than the open-loop Hall effect sensor.

- Having the ability to select the OSR and shunt resistor adds additional flexibility to the design.
- Lower maximum power dissipation than the closed-loop Hall effect sensor and isolated amplifier
- A digital CIC filter can be used to band-limit the sensed signal.
- Easily integrated with certain microcontrollers and FPGAs

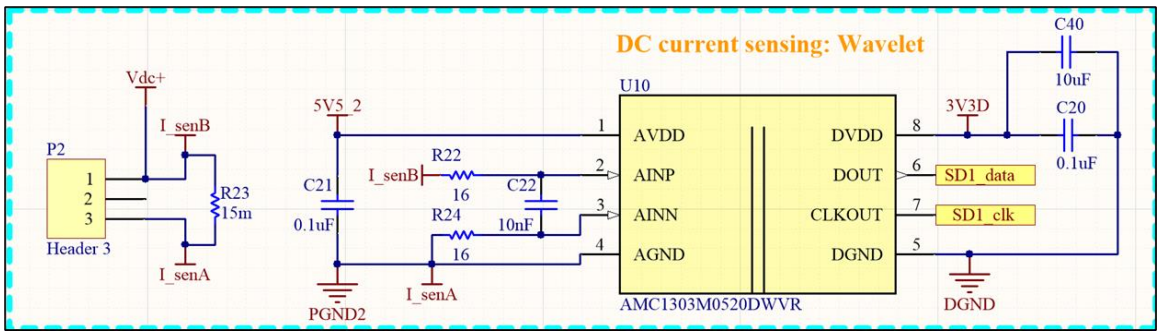

Figure 20. Schematic showing the I_{DC} sensing circuit.

3.2 PCB Design

The differential input of the modulator sensed the input current using a 15 mΩ shunt resistor and transmitted the sigma-delta bitstream to the VSI microcontroller [21].

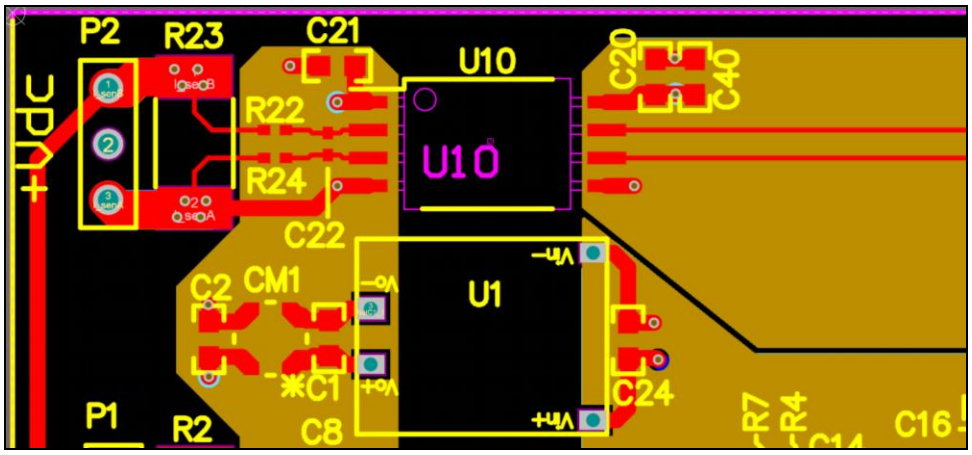

Figure 21. 4-layer PCB layout for the schematic shown in Fig. 20. The Δ-Σ modulator is labeled U10, and the isolated DC-DC converter is labeled U1.

Fig. 21 shows the PCB layout of the schematic shown in Fig. 20. To minimize any measurement biases, a four-wire connection was used to sense the voltage drop across the 15 mΩ, 2512-size shunt resistor (R23). As seen in Fig. 21, the Kelvin connection traces were routed underneath R23 and kept to approximately the same length. To maximize the current-carrying capacity of R23, all four PCB layers were connected to its pads using two sets of four vias. The differential RC filter formed by R22, R24, and C22 was used for anti-aliasing purposes. The cutoff frequency for the RC filter was at about 1 MHz. By sampling at a rate of 20 MHz, the sigma-delta ADC relaxes the anti-aliasing filter requirements and allows for a first-order filter to be used. The sigma-delta architecture shifts most of the signal path filtering from the analog domain and into the digital domain. Components C20, C21, and C40 acted as decoupling capacitors for both the analog and digital ports of the 2nd-order delta-sigma modulator (U10).

The isolated DC-DC converter (U1) supplied a floating 5 V dc to the analog side of U10. An important part of the layout involved connecting the ground of the floating 5

V supply to the negative side of R23. This connection established a reference for the current shunt voltage measurement. Without this connection, the floating 5 V ground, and the negative side of R23 would be at different potentials. This would cause the measurement to become corrupted. Both U1 and U10 were placed to maintain a consistent clearance area between the power and controller-side copper planes. The filter formed by C1, C2, and the common-mode inductor (CM1) was used to attenuate the switching ripple produced by U10.

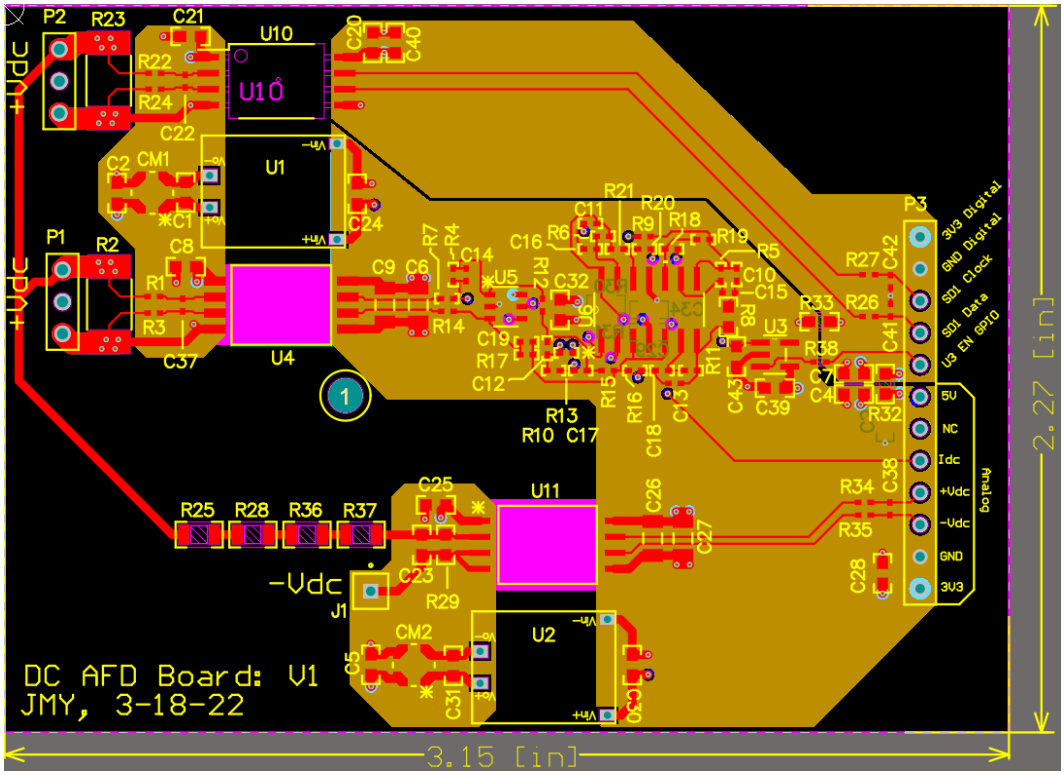

Figure 22. DC arc fault detection board layout. The layout was made using Altium.

Fig. 22 shows the entire layout for the designed arc fault detection board. Referencing the gap located below the right (digital) side of U10, the controller-side copper planes were separated into analog and digital sections. U4 was a ±250 mV-input isolated amplifier

[29] and was connected to an 8th-order analog Butterworth bandpass filter. U11 was a 2 V-input isolated amplifier [30] and was used to sense the DC bus voltage. In keeping with the analysis presented in the previous chapter, the sigma-delta modulator was found to be the best option for the given application. Thus, for the detection algorithm, only U10 and U11 were used to sense I_{DC} and V_{DC}.

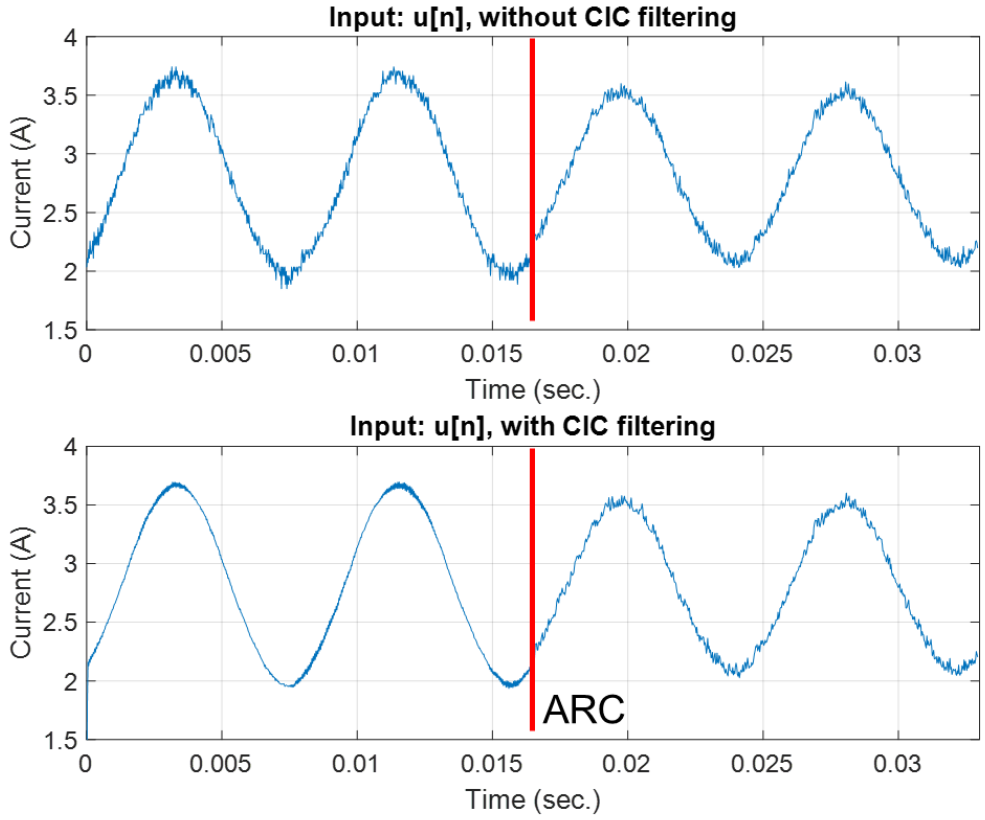

Figure 23. Dc bus current waveforms illustrating how the CIC filter band limiting improved the arc fault detection accuracy. The OSR was set to 256.

A 3rd-order CIC filter was used to filter the bitstream produced by the modulator. The CIC filtering process increases the resolution of the modulator bitstream from 1-bit up to a maximum of 26 bits and increases the effective number of bits (ENOB) for the

entire digital control loop up to 13 to 14 bits. After the cutoff frequency at 21 kHz, the three integrator sections provided significant roll off at high frequencies, and the three comb sections provided notches at multiples of the data rate (79 kHz). By decreasing the OSR, the -3 dB bandwidth of the filter increased. This caused more high-frequency noise to be sent to the DWT function filter bank and made it more difficult for the detection algorithm to distinguish between normal and fault conditions. Fig. 23 shows the effect of band-limiting the sensed signal in the time domain.

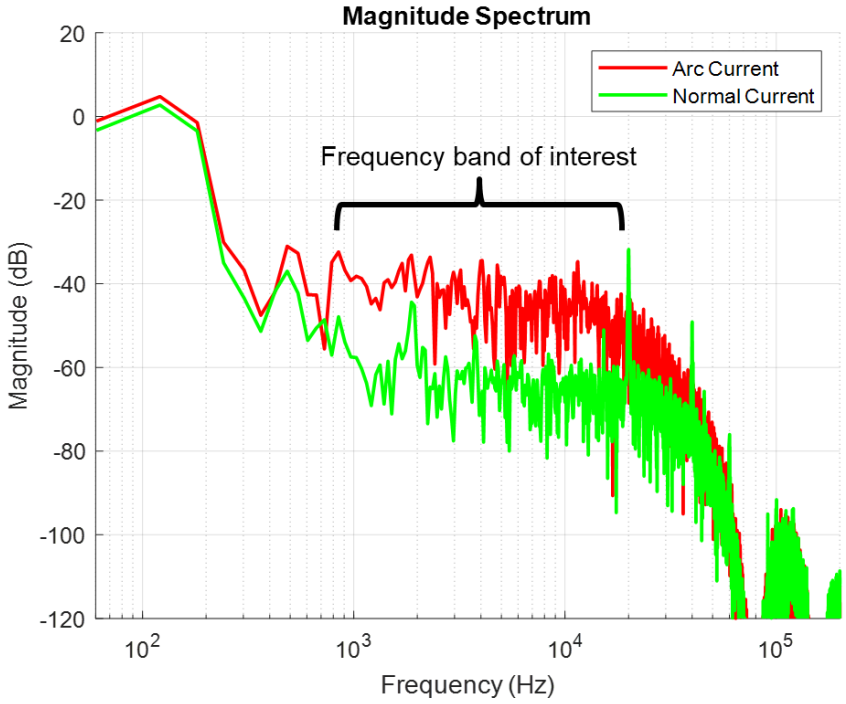

Figure 24. Magnitude spectrum of the dc bus currents after being filtered by the 3rd-order CIC filter.

Fig. 24 shows the spectrum of I_{DC} after being band-limited by the CIC filter. It was observed that band-limiting the sensed signal increased the signal-to-noise ratio (SNR) and improved the accuracy of the detection algorithm.

3.3 Preliminary Tests Using Recorded Data

Once the program for the detection algorithm had been finished, tests were conducted using a PicoScope 5444B. The waveforms recorded during previous tests were loaded onto the arbitrary function generator (AFG) of the 5444B and used to test the detection algorithm. This allowed for the detection algorithm to be tested without the need to generate an arc, and it also allowed for the amplitude of the arcing noise to be adjusted relative to the DC and 120 Hz magnitudes, similar to the testing methodology presented in [31]. Since the selected modulator had an input voltage range of ±50 mV, the magnitude of the recorded I_{DC} data had to be reduced to fall within the modulator's linear range. To maintain an adequate SNR, a voltage divider and op amp buffer were used to interface the AFG with the input of the modulator IC. Directly setting the magnitude of the AFG output to within ±50 mV dramatically reduced the SNR of the AFG output.

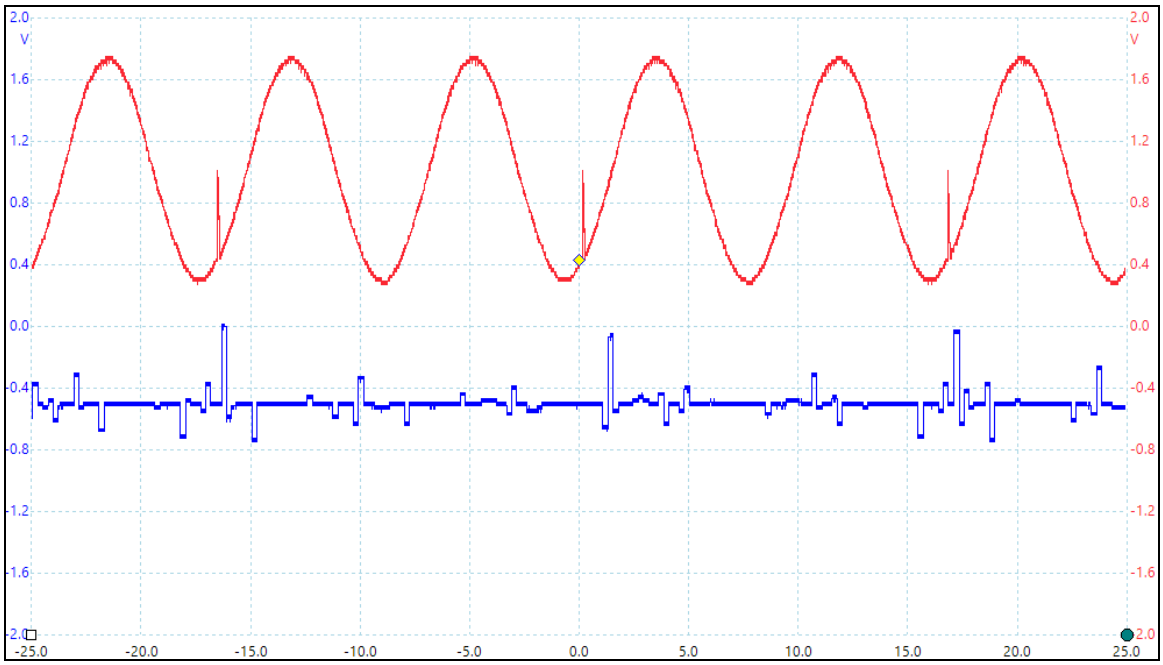

Figure 25. Boundary artifacts encountered during initial testing of the DWT function.

Initially, the arc fault detection interrupt service routine (ISR) stored 16 samples of I_{DC} in an array before passing the array to the DWT function. This "batch" processing approach is commonly used when working with FFT functions [32]; however, it does not translate well to FIR filtering. Fig. 25 shows how, when using the batch processing approach, the output from the filter bank exhibited numerous boundary artifacts. The waveforms were captured using the PicoScope, with the red curve showing the signal produced by the AFG, and the blue curve showing the filter bank output, prior to sending it to the variance function. The filter bank could detect the sharp periodic discontinuities; however, the response to the discontinuity was obscured by the numerous adjacent boundary artifacts. It was concluded that, in order to convolve the filter bank with every element of the I_{DC} array, the filter bank coefficients were being multiplied by data outside

of the I_{DC} array. It was thought that this corrupted the filter bank output and introduced the observed boundary artifacts. To correct this, a circular buffer was used.

Circular buffers, a type of data structure, are commonly used to implement FIR filters in real-time filtering algorithms [33]. The following C code shows the DWT function after implementing the circular buffer.

```
void DWT_float32 // Wavelet Transform, asymmetric filter bank
(
    float                 input,     /* Circular buffer of input values */
    uint16_t              ptr,       /* Pointer to buffer data */
    const float *restrict lp_filt,   /* Lowpass filter */
    const float *restrict hp_filt,   /* Highpass filter */
    float       *restrict output_lpf,
    float       *restrict output_hpf,
    uint16_t              buf_size,  /* Length of circ. buffer */
    uint16_t              iter,      /* Number of filter bank iterations/levels */
    uint16_t              filt_size
)
{
    static uint16_t i, j;

    // First level of the filter bank
    if (iter == 1){

        for (i = 0; i < filt_size; i++)
        {

            j = (buf_size + ptr - i) % buf_size;

            output_lpf[ptr] += lp_filt[i] * input[j];
            *output_hpf += hp_filt[i] * input[j];

        }

    }

    // If the filter bank has two levels
    else if (iter == 2){

        for (i = 0; i < filt_size; i++)
        {

            j = (buf_size + ptr - i) % buf_size;

            output_lpf[ptr] += lp_filt[i] * input[j];

        }

        for (i = 0; i < filt_size; i++)
        {

            j = (buf_size + ptr - 2*i) % buf_size;

            *output_hpf += hp_filt[i] * output_lpf[j];

        }

    }

}
```

The DWT function provided in [34] was used as a reference when producing the above code. In the detection ISR, the circular buffer was passed to the DWT function once a new I_{DC} sample had been retrieved. Fig. 26 shows a simplified flowchart of the detection routine. The flowchart shown in Fig. 26 would apply for when the fault count value equaled one. If the fault count was set to a value larger than one, the Boolean expression (8) would have to be true a fault count-number of times for the relays to open and the inverter shutdown process to initiate.

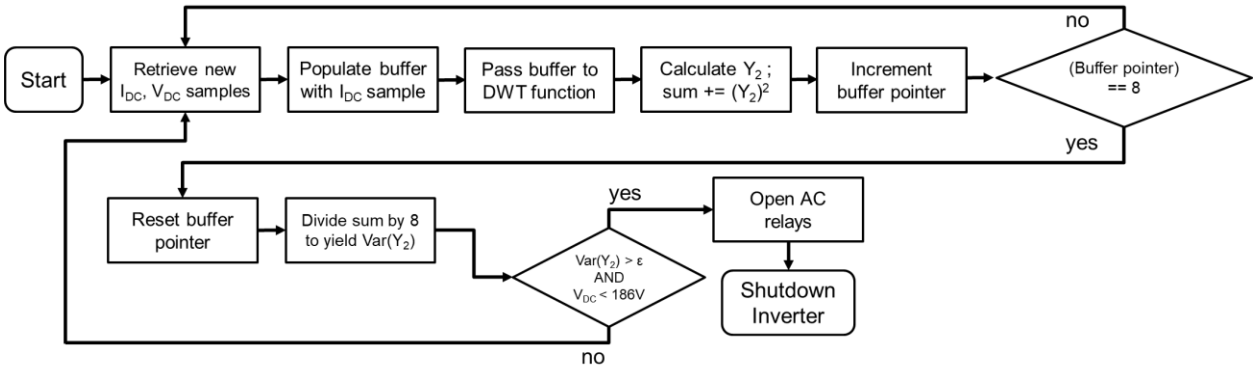

Figure 26. Simplified flowchart of the detection algorithm.

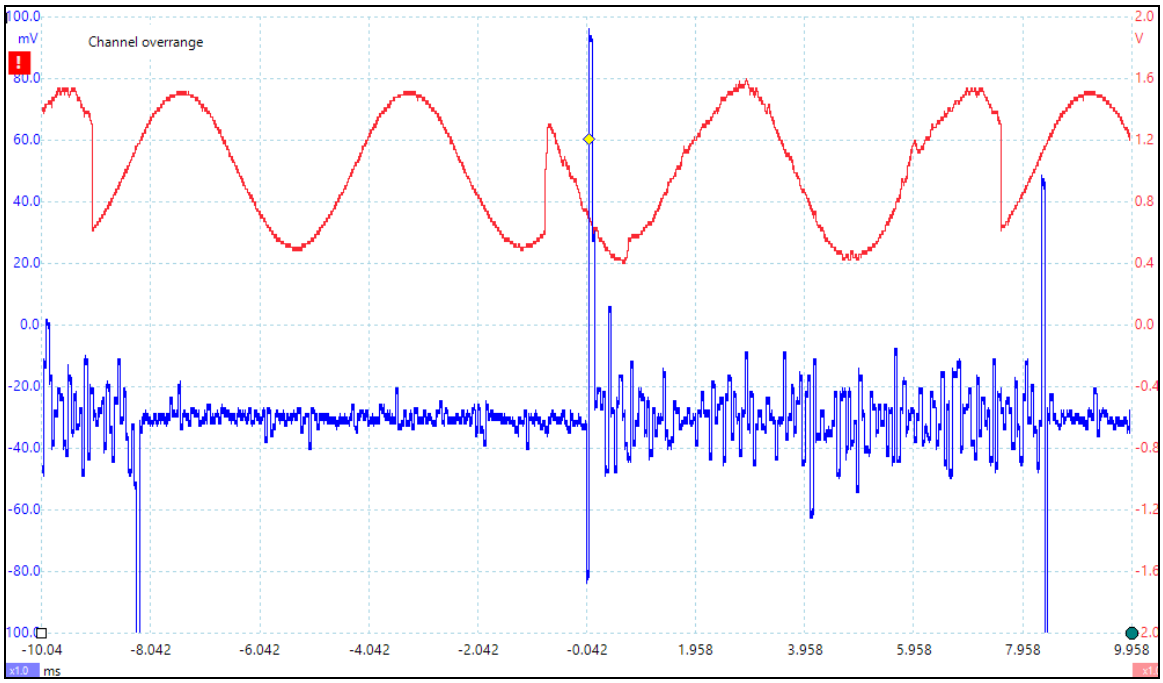

Figure 27. Waveforms captured after reducing the boundary artifacts.

Fig. 27 shows the filter bank output after updating the detection ISR and implementing the circular buffer. The waveforms were captured using the PicoScope, with the red curve showing the signal produced by the AFG, and the blue curve showing the filter bank output, prior to sending it to the variance function. The AFG signal consisted of recorded normal and fault data that was concatenated together. Observing Fig. 27, the amplitude of the filter bank output increased after both the initial transient and noise produced by the series arc fault.

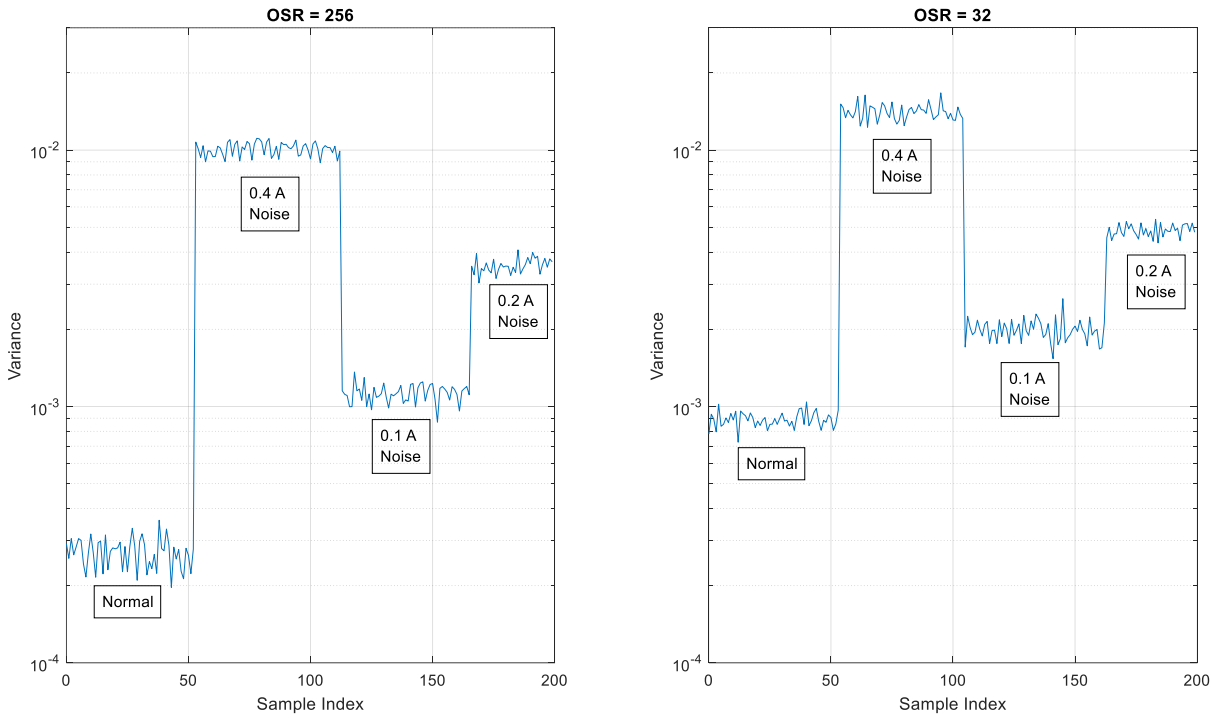

Figure 28. Calculated values for $Var(Y_1)$ using different OSR values.

The two plots shown in Fig. 28 contain data recorded while testing with the PicoScope. The plots show how, as the OSR was increased, the ratio between the arcing and non-arcing (normal) states also increased. It was concluded that, in part by selecting an adequate OSR and post-processing filter bank, the ratio between the variances produced during the arcing and non-arcing states could be maximized.

[35] presents a method for determining the optimal detection threshold by first recording a set of output values produced by the detection algorithm. [35] shows how, after recording the outputs for both the normal operation case and the arc fault case in a histogram plot, the resulting two probability density functions (PDFs) can be used to derive the optimal detection threshold. Both PDFs were approximated as log-normal distributions and were used to determine the probability of a type-1 or type-2 detection

error. (9) shows the equation for a log-normal distribution PDF of some random variable x, possessing a population mean: μ and a standard deviation: σ.

$$f(x) = \left(\frac{1}{x\sigma\sqrt{2\pi}}\right)\left(\exp\left(-\frac{(\ln(x)-\mu)^2}{2\sigma^2}\right)\right) \tag{9}$$

By using numerical integration on the derived PDF, a probability value can be calculated. Fig. 29 shows a histogram of the $Var(Y_2)$ values produced by the filter bank, along with estimated log-normal PDFs.

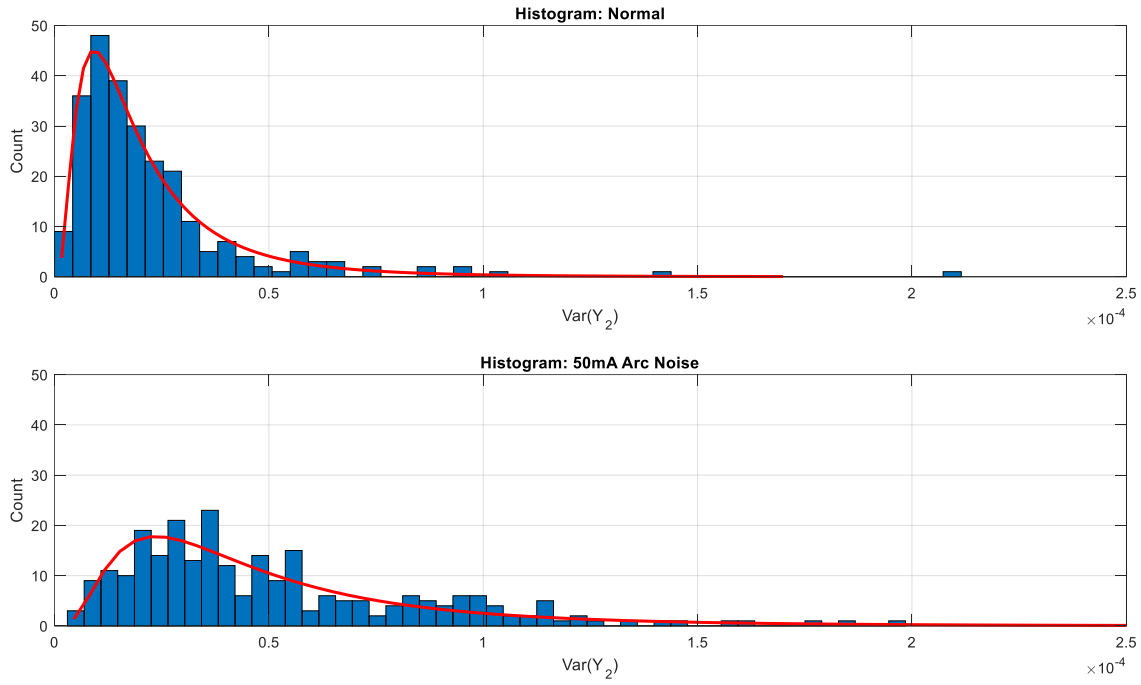

Figure 29. Histogram showing the output variances ($Var(Y_2)$) produced by the wavelet filter bank with 50 mA arc noise.

Using the AFG, 50 mA peak-to-peak arc noise was added to the recorded I_{DC} waveform and used to replicate a series arc fault. The data in Fig. 29 showed how considerable overlap existed between the PDFs for the arcing and non-arcing states. The greater the

overlap is between PDFs, the higher the probability is of receiving an incorrect detection result [35]. The PDFs shown in Fig. 30 were fitted to the data shown in Fig. 29 by using the "histfit" function in MATLAB. Table 4 shows the mean and standard deviation values of the PDFs produced by the histfit function.

Table 4. Estimated PDF Statistics: 50 mA noise

Statistic	**Normal**	**Arc Noise**
μ	-10.9975	-10.1221
σ	0.772498	0.728208

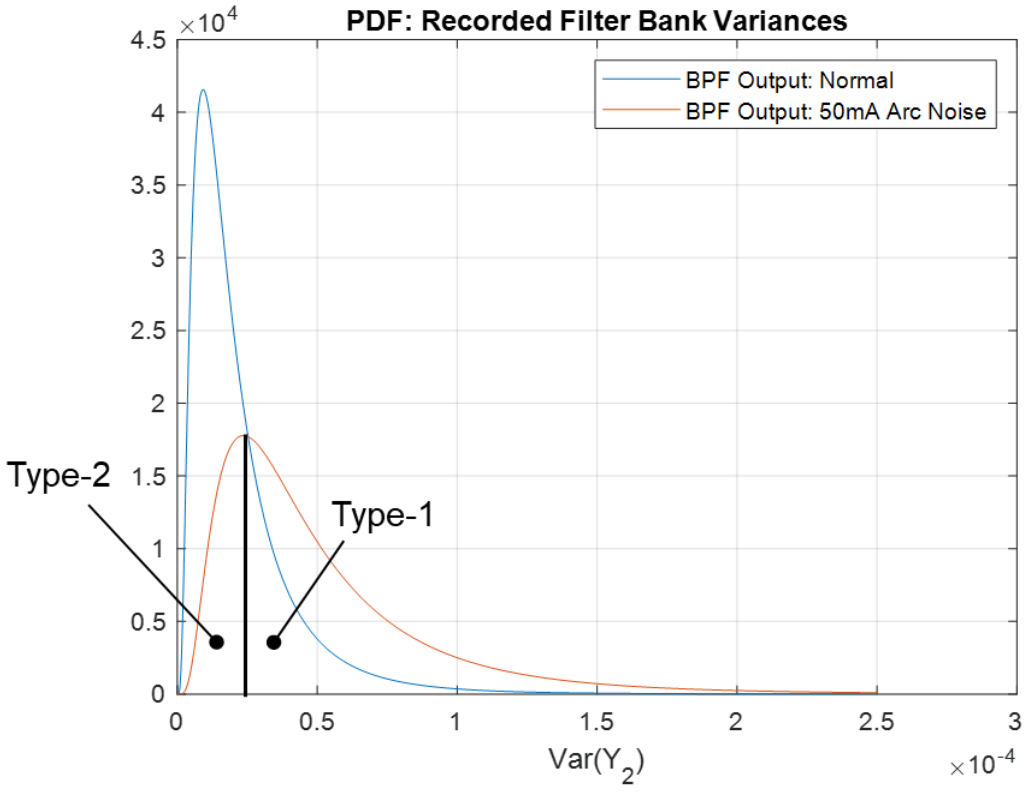

Figure 30. Estimated probability density functions (PDFs) of the recorded $Var(Y_2)$ values for the 50-mA noise case.

A type-1 detection error is a false positive, i.e., the algorithm detects an arc when no arcing is present, and a type-2 error is a false negative, i.e., an arc fault is present but is not detected. The black dividing line shown in Fig. 30 represents the optimal threshold based on the detection methodology presented in [35]. The value for the optimal detection threshold was found to be approximately 2.5e-05. Using trapezoidal integration in MATLAB, the following probabilities for type-1 and type-2 errors were calculated.

Table 5. Calculated Type-1 and Type-2 Error Probabilities: 50 mA noise

Type 1	**Type 2**
29.63%	26.26%

Fig. 31 shows a histogram of the $Var(Y_2)$ values produced by the filter bank, along with the estimated PDFs for the 0.2 A arc noise case. The top histogram is the same plot shown at the top of Fig. 29.

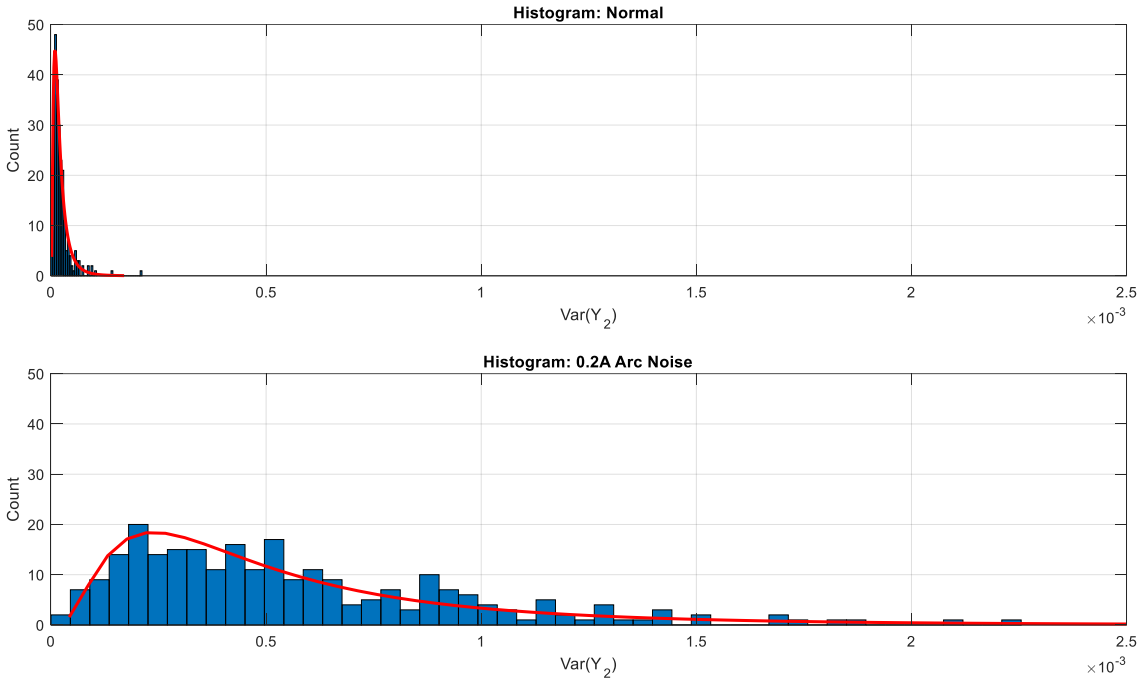

Figure 31. Histogram showing the output variances ($Var(Y_2)$) produced by the wavelet filter bank with 0.2 A arc noise.

As can be seen from Fig. 31, the filter bank output variances exhibited considerably less overlap during the 0.2 A noise case.

Table 6. Estimated PDF Statistics: 0.2 A noise

Statistic	**Normal**	**Arc Noise**
μ	-10.9975	-7.73967
σ	0.772498	0.7764

For the 0.2 A noise case, the value for the optimal detection threshold was found to be approximately 8.5e-05. The following probabilities for type-1 and type-2 errors were calculated in MATLAB.

Table 7. Calculated Type-1 and Type-2 Error Probabilities: 0.2 A noise

Type 1	Type 2
1.77%	1.77%

It was concluded that, to reduce both error probabilities, the calculated variances could be averaged. This would, in theory, reduce the standard deviation of both PDFs. By decreasing the standard deviation of both PDFs, their overlap would be reduced, thereby decreasing both error probabilities.

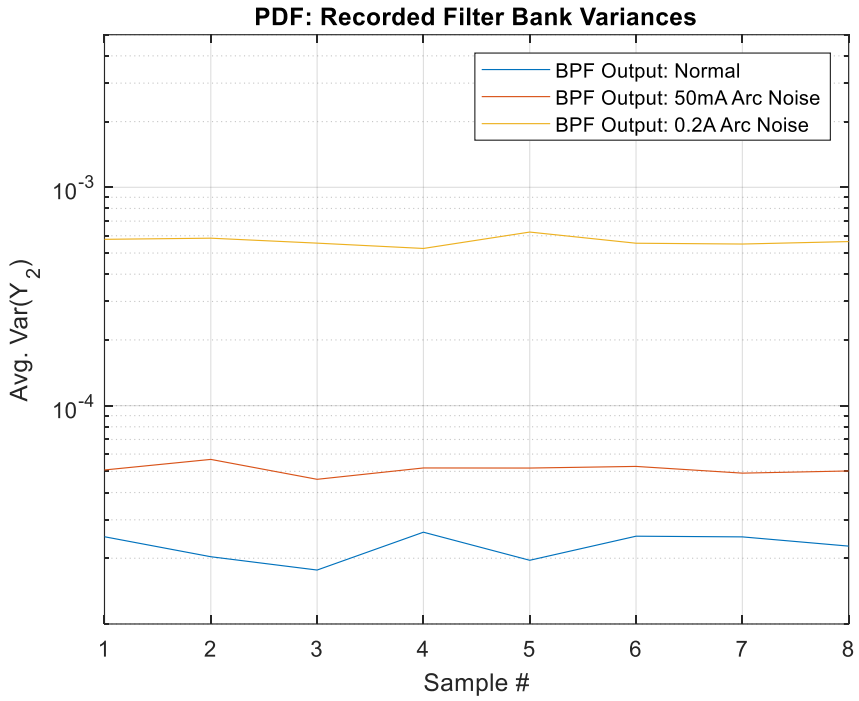

Figure 32. Calculated averages for $Var(Y_2)$ under different arc noise magnitudes.

Fig. 32 shows the calculated variances $Var(Y_2)$ after adding a 32-sample moving average calculation to the detection algorithm. By averaging the variances, the overlap between the normal and 50 mA arc noise cases was completely removed. It was thought that this

should allow the detection algorithm to better handle partial series arc faults, where the generated noise tends to be at a lower amplitude [9]. (10) shows the updated Boolean expression from the algorithm after adding the average value calculation.

$$\left(\overline{Var(Y_2)} > \varepsilon\right) AND \ (V_{DC} < 186\ V) \tag{10}$$

Additionally, the probabilities shown in Tables 5 and 7 are only valid if the variance of the filter bank output is solely used to decide if a fault has occurred. It was thought that, by also using the measured value for V_{DC} in the detection algorithm, the probability of experiencing a type-1 or type-2 error would decrease. Future work could involve quantifying the error probabilities after the V_{DC} measurement has been added to the algorithm.

4. Experimental Results and Discussion

Tests were conducted using a solar PV array simulator, a B&K Precision PVS60085. The PV simulator acted to replicate the dc bus produced by a dc source, such as a power optimizer or an array of solar PV strings. While arcing, the copper contacts were separated by about a 0.5 mm gap.

4.1 Standalone VSI Testing Results

The standalone inverter was a single-phase full-bridge circuit operating with an asymmetrical 20 kHz, 60 Hz unipolar PWM. Its control consisted of a closed current loop with a proportional-resonant (PR) controller. A 12 Ω resistor bank was placed in series with the PV simulator to act as a current limiting “ballast” resistor [3] and to increase the

output impedance of the PV simulator. During initial testing, it was observed that most of the harmonics produced by the VSI were being drawn by the low impedance of the PV simulator. The zero crossings produced by these harmonics prevented any arcs from forming. Adding the 12 Ω resistor bank increased the impedance of the PV simulator and allowed for more of the inverter harmonics to be shunted through the VSI dc bus capacitance. It was concluded that, when testing the algorithm with an actual solar PV array, the resistor bank would only be needed for current limiting purposes. Fig. 33 shows a diagram and picture of the experimental setup.

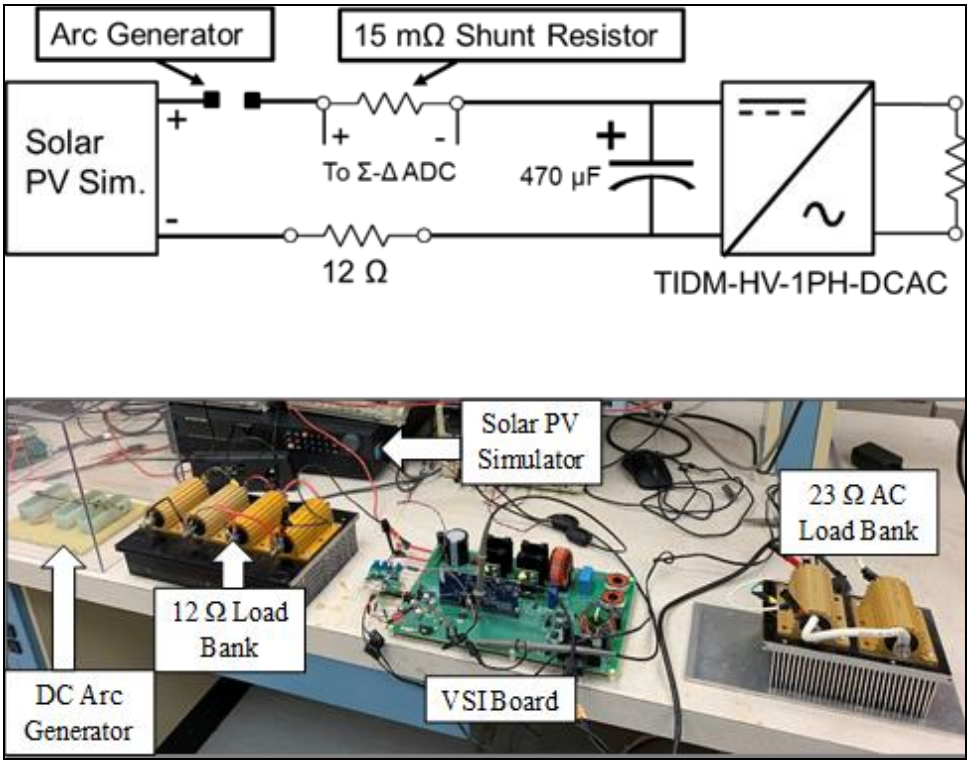

Figure 33. Schematic and picture of the experimental setup used during testing with the inverter.

The salient parameters of the experimental setup are listed in Table 8.

Table 8. Experimental Setup Parameters: Standalone Inverter

DC Power Supply	B&K PVS60085, set to 220 V
VSI Board	TIDM-HV-1PH-DCAC
VSI Nominal Power	600 W, 400 W at steady state
DC Bus Voltage	200 V
DC Bus Capacitance	470 µF
I_{DC} Shunt Resistance	15 mΩ
Ballast Resistance	12 Ω
Inverter Load Resistance	23 Ω
Microcontroller	TMS320F28379D

The nominal VSI dc bus voltage was set to 200 V, with a nominal input current of about 2.5 A to about 3 A. The minimum dc bus voltage was set to 186 V. The maximum power point (MPP) voltage of the simulator was set to 220 V to account for the voltage

drop produced by the 12 Ω resistor bank. Initial tests showed that the arc impedance produced voltage drops of about 10 V to 30 V, causing the dc bus voltage of the VSI to decrease and leading to overmodulation. The input current was found to decrease at the start of the arc fault before eventually increasing due to closed current loop controller.

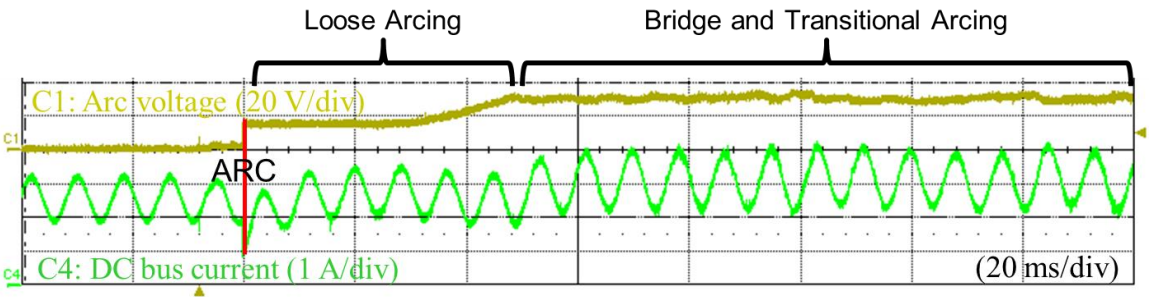

Figure 34. Waveforms captured during testing with the inverter. The different arcing states have been labeled.

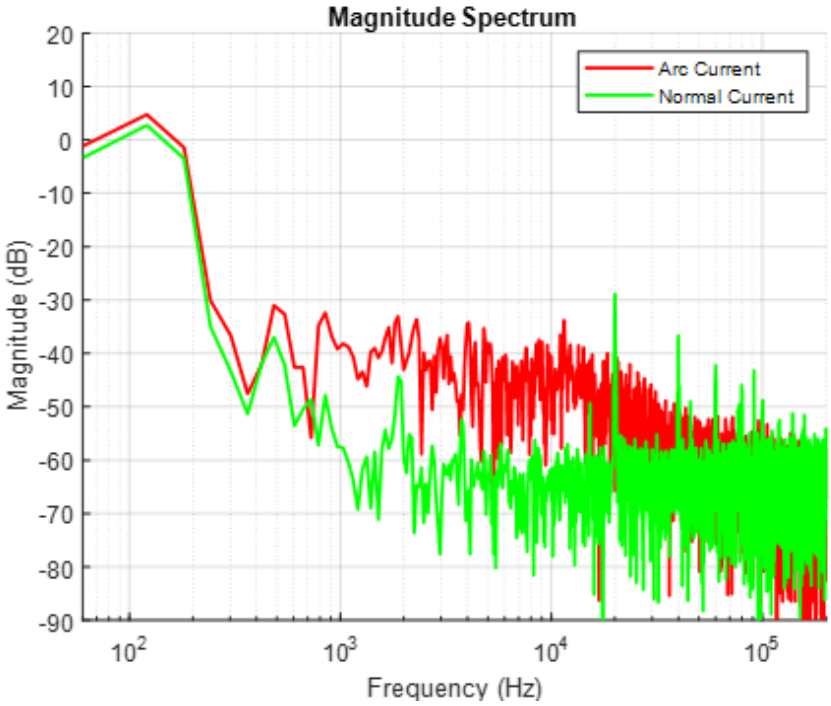

Figure 35. Magnitude spectrum of the dc bus currents prior to and after a series arc fault. The noise floor increase appeared to be consistent with the spectrum from the resistive load test.

Fig. 35 shows the spectra for I_{DC} prior to and after a series arc fault was initiated. For the normal I_{DC} spectrum, the harmonic located close to 2 kHz was thought to be the resonance produced by the LCL output filter of the inverter. This harmonic can also be seen in Fig. 40. After determining that a fault had occurred, the detection ISR was programmed to open two ac relays. Fig. 36 shows how, once both relays were opened, the inverter ceased drawing power, extinguishing the arc.

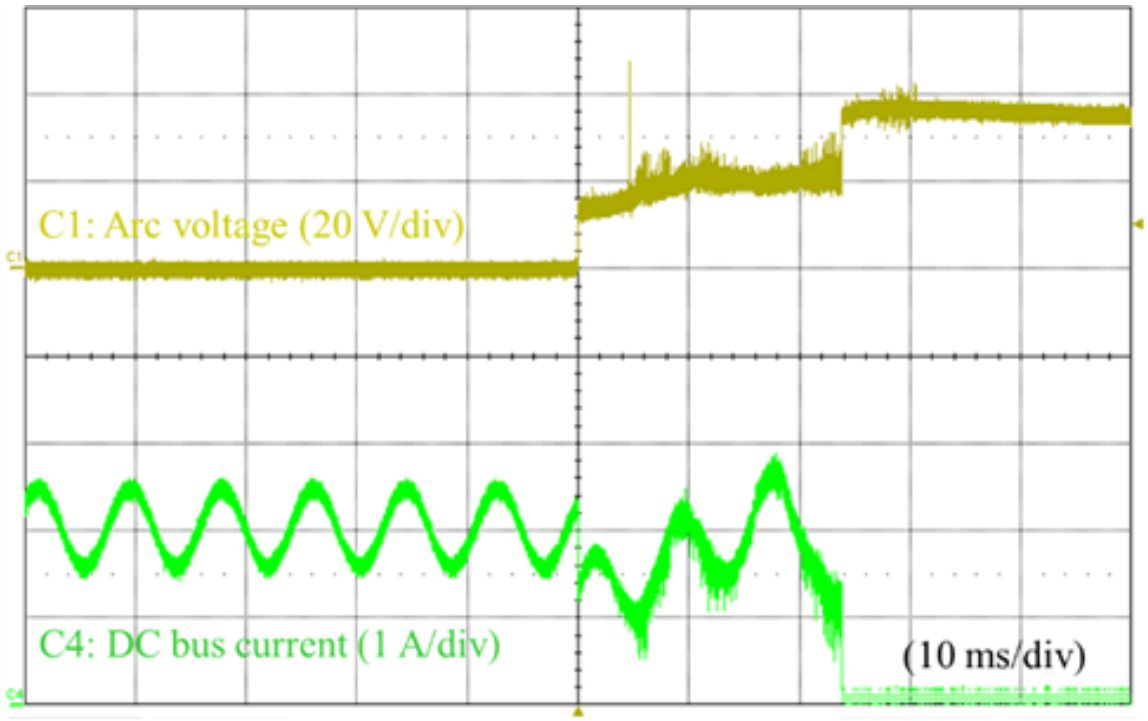

Figure 36. Captured current and voltage waveforms showing how the arc fault was successfully detected and extinguished after about 24 ms.

The arc voltage was measured using a differential probe. The 34 V seen after the arc was extinguished was calculated to be the difference between the PV simulator supply voltage (220 V) and the fault detection lower voltage limit (186 V). Fig. 36 shows the waveforms captured after using one fault count to trigger the detection algorithm.

Fig. 37 shows the waveforms captured after using ten fault counts to trigger the detection algorithm. By increasing the number of fault counts needed to trip the detection algorithm, it was thought that the sensitivity of the detection algorithm could be reduced. I was thought that this would enhance the reliability of the detection algorithm.

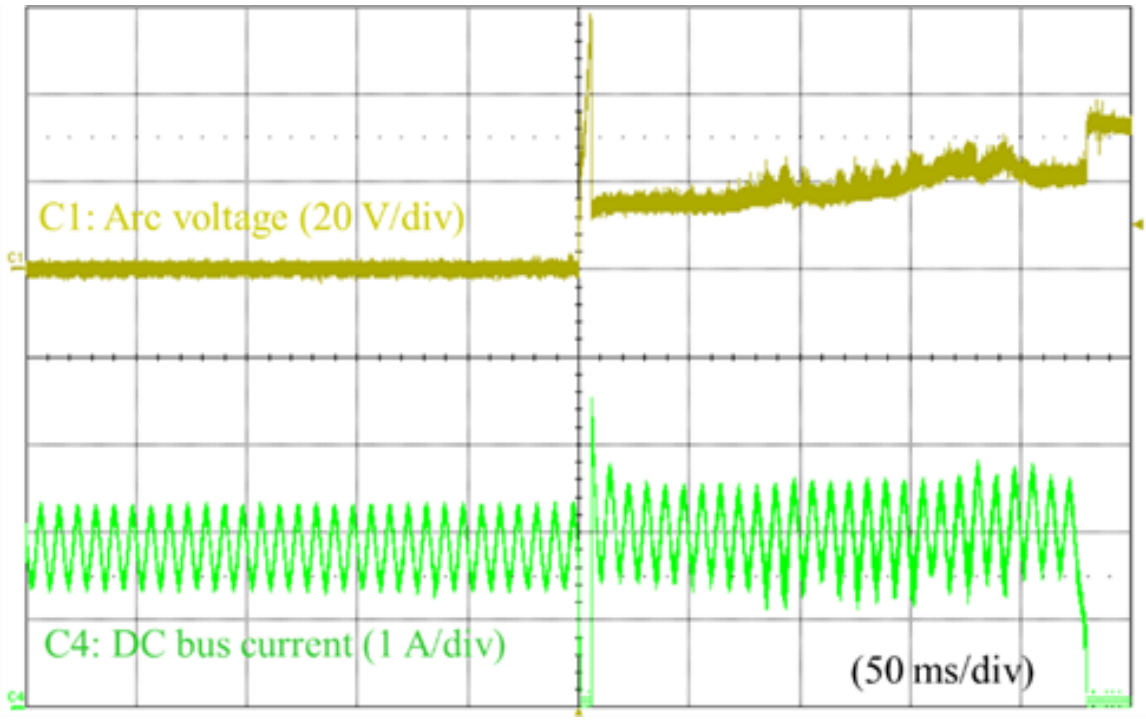

Figure 37. Captured current and voltage waveforms showing how the arc fault was successfully detected and extinguished after about 0.23 sec.

4.2 Power Optimizer-VSI Testing Results

For these tests, the nominal DC bus voltage was decreased to 150 V. The VSI was operated in open loop with the same asymmetrical 20 kHz, 60 Hz unipolar modulation scheme as before. The power optimizer also operated in open loop, with a 16% duty cycle and a 125 kHz switching frequency. Since V_{DC}, I_{DC} sensing occurred from the perspective of the power optimizer output, the detection algorithm was changed such that (10) became the following.

$$\left(\overline{Var(Y_2)} > \varepsilon\right) AND \left(V_{DC} > 164\ V\right) \tag{11}$$

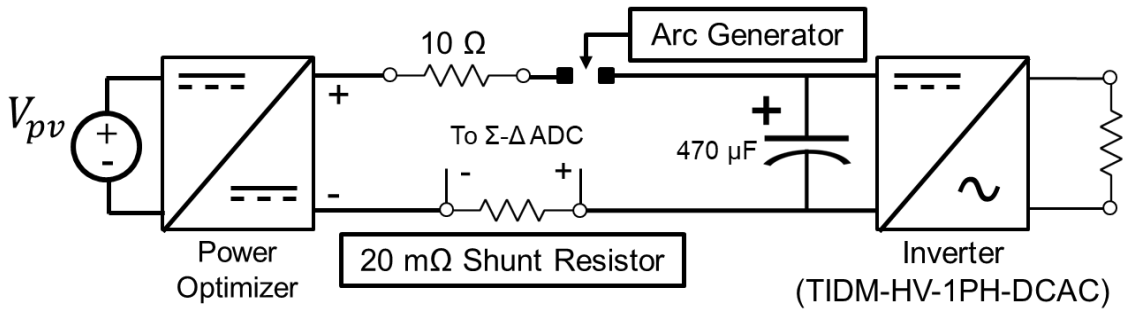

Figure 38. Schematic of the experimental setup used during testing.

Fig. 38 shows a schematic of the experiment setup, and the key parameters of the experimental setup are listed in Table 9.

Table 9. Experimental Setup Parameters: Power Optimizer and Inverter

DC Voltage Source (V_{pv})	B&K PVS60085, set to 40 V
Power Optimizer Board	FEEC Low Voltage Input
VSI Board	TIDM-HV-1PH-DCAC
Nominal Power	300 W
DC Bus Voltage	150 V
DC Bus Capacitance	470 µF
I_{DC} Shunt Resistance	20 mΩ
Ballast Resistance	10 Ω
Inverter Load Resistance	23 Ω
Microcontroller	TMS320F280049M

Five arc fault tests were conducted, and the algorithm could detect each series arc fault in less than 0.2 s.

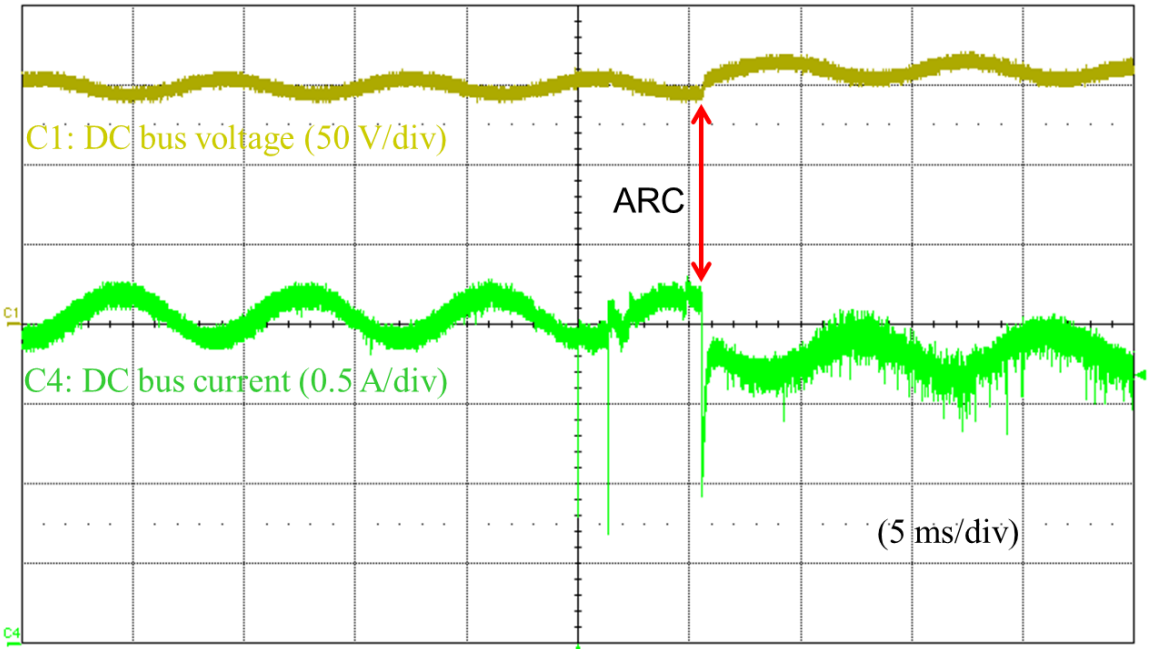

Figure 39. Waveforms captured during testing with the power optimizer and inverter.

The I_{DC}, V_{DC} waveforms shown in Fig. 39 appear to exhibit similar time domain characteristics to the waveforms shown in Figures 36 and 37. Once the arc fully ignited, a sharp transient was induced on I_{DC}. This was proceeded by the characteristic pink noise observed previously. The arc impedance voltage drop appeared to cause V_{DC} to increase in magnitude.

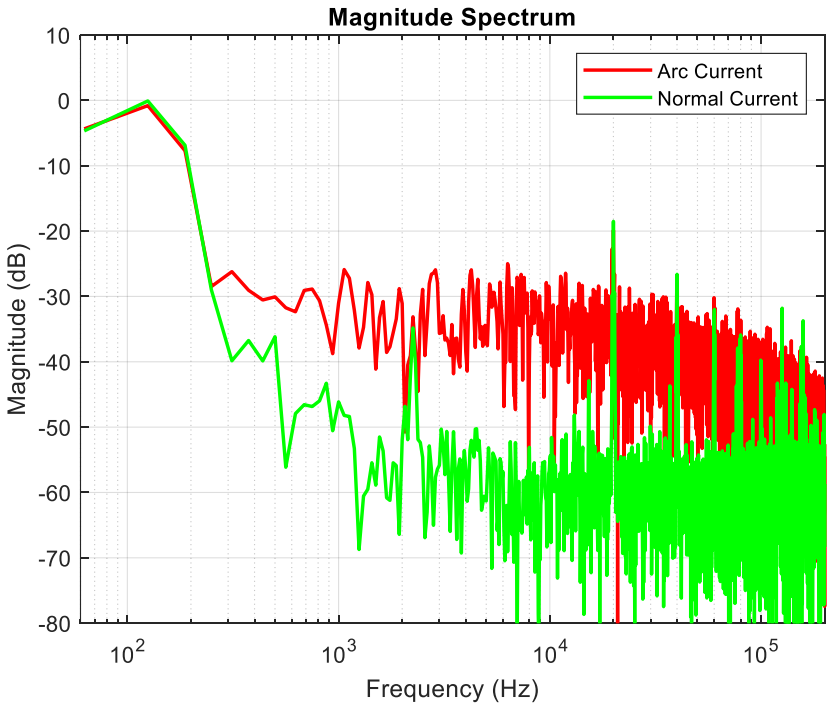

Figure 40. Power optimizer and inverter test: Magnitude spectrum of the dc bus currents prior to and after a series arc fault.

5. Conclusions and Future Work

The developed real-time algorithm could detect and extinguish a series arc fault in less than two seconds, satisfying the UL 1699B trip time requirement. The algorithm used a two-level, wavelet-based filter bank to filter the sensed dc bus current and thereby selectively monitor for the characteristic noise and distortion produced by a series arc fault. The algorithm could also detect the initial current discontinuity produced by the arc fault, in addition to the wideband noise generated during steady state arcing. A 3rd-order CIC filter was used to band-limit the sampled dc bus current and its impact on the reliability of the detection algorithm was examine. Board space was saved by not using any second-order analog filters to band-limit the sensed signal. A variance calculation

and the dc bus voltage measurements were used to enhance the reliability of the detection algorithm. The algorithm could successfully detect series arc faults when monitoring from both the inverter side and power optimizer side of a two-stage power conversion system. By shutting down all the converters that are connected to the dc bus, both series and parallel-type faults can be extinguished.

Future work could involve the following:

- Testing with a power optimizer and solar PV module
- Testing with larger values of P_{arc}, which could generate less noise [4]
- Reducing the computation time of the DWT function
    - Applying the multi-rate Noble identities [14]
    - Changing the function variables to fixed instead of floating point
- Adding automatic detection of the most significant interfering switching harmonic
    - Use an FFT function to locate the harmonic
    - The frequency could be periodically updated to account for the presence of variable switching frequency power converters.

References

[1] J. C. Kim, D. O. Neacşu, R. Ball and B. Lehman, "Clearing Series AC Arc Faults and Avoiding False Alarms Using Only Voltage Waveforms," in IEEE Transactions on Power Delivery, vol. 35, no. 2, pp. 946-956, April 2020.

[2] X. Yao, “DC Arc Fault Detection and Protection in DC Based Electrical Power Systems,” Ph. D. dissertation, The Ohio State University, 2015.

[3] Outline of Investigation for Photovoltaic (PV) dc Arc-Fault Circuit Protection, UL 1699B, 2013.

[4] J. Johnson and K. Armijo, "Parametric study of PV arc-fault generation methods and analysis of conducted DC spectrum," 2014 IEEE 40th Photovoltaic Specialist Conference (PVSC), 2014, pp. 3543-3548.

[5] J. C. Kim, B. Lehman and R. Ball, "DC Arc Fault Model Superimposing Multiple Random Arc Noise States on an Average Model," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 2019, pp. 1-8.

[6] D. Vinnikov, A. Chub, E. Liivik, R. Kosenko and O. Korkh, "Solar Optiverter—A Novel Hybrid Approach to the Photovoltaic Module Level Power Electronics," in IEEE Transactions on Industrial Electronics, vol. 66, no. 5, pp. 3869-3880, May 2019.

[7] T. Esram and P. L. Chapman, "Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques," in IEEE Transactions on Energy Conversion, vol. 22, no. 2, pp. 439-449, June 2007.

[8] S. Lu, B. T. Phung, and D. Zhang, “A comprehensive review on DC arc faults and their diagnosis methods in photovoltaic systems,” Renewable and Sustainable Energy Reviews, vol. 89, pp. 88-98, June 2018.

[9] J. Johnson et al., "Differentiating series and parallel photovoltaic arc-faults," 2012 38th IEEE Photovoltaic Specialists Conference, 2012, pp. 720-726.

[10] W. Miao, Q. Xu, K. H. Lam, P. W. T. Pong and H. V. Poor, "DC Arc-Fault Detection Based on Empirical Mode Decomposition of Arc Signatures and Support Vector Machine," in IEEE Sensors Journal, vol. 21, no. 5, pp. 7024-7033, March 1, 2021.

[11] W. Gao and R. -J. Wai, "Series Arc Fault Detection of Grid-Connected PV System via SVD Denoising and IEWT-TWSVM," in IEEE Journal of Photovoltaics, vol. 11, no. 6, pp. 1493-1510, Nov. 2021.

[12] N. Bajaj, G. T. C. Chiu and J. P. Allebach, "Reduction of memory footprint and computation time for embedded Support Vector Machine (SVM) by kernel expansion and consolidation," 2014 IEEE International Workshop on Machine Learning for Signal Processing (MLSP), 2014.

[13] S. Southward. ECE 5764. Class Lecture, Topic: “Sampled Data Systems” Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA, Feb. 11, 2021.

[14] G. Strang and T. Nguyen, Wavelets and Filter Banks. Wellesley, MA: Wellesley-Cambridge Press, 1997.

[15] H. -P. Park and S. Chae, "DC Series Arc Fault Detection Algorithm for Distributed Energy Resources Using Arc Fault Impedance Modeling," in IEEE Access, vol. 8, pp. 179039-179046, 2020.

[16] B. Shaffer, Y. Abullah, J. Wang, B. Arfaei, A. Emrani and M. Volpone, "On-Line Detection of Dc Arc Faults Using Hurst Exponents for Hybrid-Electric Vehicles," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 2020, pp. 6372-6378.

[17] Y. Abdullah et al., "Hurst-Exponent-Based Detection of High-Impedance DC Arc Events for 48-V Systems in Vehicles," in IEEE Transactions on Power Electronics, vol. 36, no. 4, pp. 3803-3813, April 2021.

[18] Q. Xiong, S. Ji, L. Zhu, L. Zhong and Y. Liu, "A Novel DC Arc Fault Detection Method Based on Electromagnetic Radiation Signal," in IEEE Transactions on Plasma Science, vol. 45, no. 3, pp. 472-478, March 2017.

[19] C. Liu and J. -S. Lai, "Low Frequency Current Ripple Reduction Technique With Active Control in a Fuel Cell Power System With Inverter Load," in IEEE Transactions on Power Electronics, vol. 22, no. 4, pp. 1429-1436, July 2007.

[20] D. S. Pillai, F. Blaabjerg and N. Rajasekar, "A Comparative Evaluation of Advanced Fault Detection Approaches for PV Systems," in IEEE Journal of Photovoltaics, vol. 9, no. 2, pp. 513-527, March 2019.

[21] Texas Instruments, “TMS320F2837xD Dual-Core Microcontrollers,” TMS320F28379D datasheet, Dec. 2013 [Revised Feb. 2021].

[22] Infineon, “XMC4400: Microcontroller Series for Industrial Applications,” XMC4400 datasheet, Sept. 2018.

[23] R. Lyons, “A Beginner's Guide To Cascaded Integrator-Comb (CIC) Filters,” dsprelated.com, Mar. 26, 2020. [Online]. Available: https://www.dsprelated.com/showarticle/1337.php. [Accessed Sept. 1, 2020].

[24] Texas Instruments, “AMC1303x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With Internal Clock,” AMC1303 datasheet, June 2017 [Revised Feb. 2020].

[25] The Mathworks Inc., “Extremal Phase,” mathworks.com, 2022. [Online]. Available:https://www.mathworks.com/help/wavelet/gs/extremal-phase-wavelet.html. [Accessed Sept. 1, 2021].

[26] Hu, Y., Du, Y., Xiao, W., Finney, S. and Cao, W. (2015), DC-link voltage control strategy for reducing capacitance and total harmonic distortion in single-phase grid-connected photovoltaic inverters. IET Power Electronics, 8: 1386-1393.

[27] Maxim Integrated, Tutorial 1870, pp. 3.

[28] J. -S. Lai et al., "A Hybrid Binary Multilevel Cascaded Inverter for Medium-Voltage Applications," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 1939-1945.

[29] Toshiba Semiconductor, “Optically Isolation Amplifiers,” TLP7820 datasheet, Sept. 2015 [Revised June 2020].

[30] Texas Instruments, “AMC1311x High-Impedance, 2-V Input, Reinforced Isolated Amplifiers,” AMC1311 datasheet, Dec. 2017 [Revised May 2020].

[31] Z. Wang, S. McConnell, R. S. Balog and J. Johnson, "Arc fault signal detection - Fourier transformation vs. wavelet decomposition techniques using synthesized data," 2014 IEEE 40th Photovoltaic Specialist Conference (PVSC), 2014, pp. 3239-3244.

[32] National Instruments, *Understanding FFTs and Windowing*, pp.8-15.

[33] Texas Instruments, Appl. Report: Circular Buffering on TMS320C6000, pp.2-9.

[34] IMGLIB: DSP Image/Video Processing Library. (2002). Texas Instruments.

[35] E. Bauer, M. Troth, J. Wang, D. Schweickart and D. Grosjean, "Optimal Threshold Selection and Efficacy Evaluation for a Generic DC Series Arc Detection Algorithm," NAECON 2018 - IEEE National Aerospace and Electronics Conference, 2018, pp. 525-528.