

MODELING AND CONTROL OF PARALLEL THREE-PHASE PWM CONVERTERS

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ABSTRACT

This dissertation studies modeling and control issues of parallel three-phase pulse-width modulated (PWM) converters. The converters include three-phase boost rectifiers, voltage source inverters, buck rectifiers and current source inverters.

The averaging of the parallel converters is performed based on a generic functional switching unit, which is called a phase leg in boost rectifiers and voltage source inverters, and a rail arm in buck rectifiers and current source inverters. Based on phase-leg and rail-arm averaging, the developed models are not only equivalent to the conventional three-phase converter models that are based on phase-to-phase averaging, but they also preserve common-mode information, which is critical in the analysis of the parallel converters. The models reveal such parallel dynamics as reactive power circulation and small-signal interaction.

A unique feature of the parallel three-phase converters is a zero-sequence circulating current. This work proposes a novel zero-sequence control concept that uses variable zero-vectors in the space-vector modulation (SVM) of the converters. The control can be implemented within an individual converter and is independent from the other control loops for the converter. Therefore, it greatly facilitates the design and expansion of a parallel system.

Proper operation of the parallel converters requires an explicit load-sharing mechanism. In order to have a modular design, a droop method is recommended. Traditionally, however, a droop method has to compromise between voltage regulation and load sharing. After parametric analysis, a novel droop method using a gain-

scheduling technique is proposed. The numeric analysis shows that the proposed droop method can achieve both good voltage regulation and good load sharing.

An interleaving technique is often used in parallel converter systems in order to reduce current ripples. Because of its symmetrical circuit structure, the parallel three-phase converter system can reduce both differential-mode and common-mode noise with a center-aligned symmetrical SVM.

Based on the concept that a symmetrical circuit can reduce common-mode dv/dt noise, a conventional three-phase, four-leg inverter is modified so that its fourth leg is symmetrical to the other three legs. The common-mode dv/dt noise can be practically eliminated with a new modulation strategy. Meanwhile, with a modified control design, the new four-leg inverter still can handle low-frequency common-mode components that occur due to unbalanced and nonlinear load.

*To my wife Fang & daughter Elva
and
my host family Elva & Herb Miller*

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"We all take different paths in life,
but no matter where we go,
we take a little of each other everywhere"

– Tim McGraw

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