

THE OPTIMIZATION OF SPICE MODELING  
PARAMETERS UTILIZING THE TAGUCHI METHODOLOGY

by

John F. Naber

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APPROVED:

Aicha Elshabini-Riad  
A.Elshabini-Riad, Chairperson

Douglas J. Nelson  
D.J.Nelson

Shin Onishi  
S.Onishi

Sedki M. Riad  
S.M.Riad

Joseph G. Tront  
J.G.Tront

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Blacksburg, Virginia

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(ABSTRACT)

A new optimization technique for SPICE modeling parameters has been developed in this dissertation to increase the accuracy of the circuit simulation. The importance of having accurate circuit simulation models is to prevent the very costly redesign of an Integrated Circuit (IC). This radically new optimization technique utilizes the Taguchi method to improve the fit between measured and simulated I-V curves for GaAs MESFETs. The Taguchi method consists of developing a Signal-to-Noise Ratio (SNR) equation that will find the optimum combination of controllable signal levels in a design or process to make it robust or as insensitive to noise as possible. In this dissertation, the control factors are considered the circuit model curve fitting parameters and the noise is considered the variation in the simulated I-V curves from the measured I-V curves. This is the first known application of the Taguchi method to the optimization of IC curve fitting model parameters. In addition, this method is not technology or device

dependent and can be applied to silicon devices as well. Improvements in the accuracy of the simulated I-V curve fit reaching 80% has been achieved between DC test extracted parameters and the Taguchi optimized parameters. Moreover, the computer CPU execution time of the optimization process is 96% less than a commercial optimizer utilizing the Levenberg-Marquardt algorithm (optimizing 31 FETs). This technique does a least square fit on the data comparing measured currents versus simulated currents for various combinations of SPICE parameters. The mean and standard deviation of this least squares fit is incorporated in determining the SNR, providing the best combination of parameters within the evaluated range. Furthermore, the optimum values of the parameters are found without additional simulation by fitting the response curves to a quadratic equation and finding the local maximum. This technique can easily be implemented with any simulator that utilizes simulation modeling parameters extracted from measured DC test data. In addition, two methods are evaluated to obtain the worst case modeling parameters. One method looks at the correlation coefficients between modeling parameters and the second looks at the actual device parameters that define the  $\pm 3\sigma$  limits of the process. Lastly, an example is given that describes the applicability of the Taguchi methodology in the design of a differential amplifier, that accounts for the effect of offset voltage.

## ACKNOWLEDGEMENTS

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I would like to thank my entire family for their enduring love and especially Mom and Dad, whose encouragement and moral support throughout my academic years will be forever appreciated. Lastly, I would like to dedicate this work to my wife Cara and newborn daughter Julia. I thank them for their unconditional love and understanding that has brought abundant joy and happiness into my life.

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## CHAPTER I

### INTRODUCTION

In the last ten years the commercial GaAs IC industry has not lived up to expectations in competition with high-speed silicon. However, recent projections for the GaAs IC industry predict up to a billion market by 1995 [1],[2]. The digital and microwave (analog circuits operating over 1 Ghz) GaAs IC markets are proliferating, but the analog or linear market is relatively non-existent. For example, no A/D converters or op-amps are commercially available. There are a multitude of reasons for the shortcomings of linear GaAs circuits, some of which are: material dependent anomalies which affect performance, direct competition with high-performance silicon processes (speed/power/cost tradeoffs), lack of experienced analog/linear designers, and lack of available models which can accurately simulate analog circuitry. The goal of this research work is to develop a generic circuit optimizer that can quickly optimize all devices on the wafer to enable a better match between measured and simulated DC I-V curves for analog as well as digital circuit design.

The impetus for this research was the poor agreement between measured and simulated circuits from the ITT Gallium

Arsenide Technology Center's (GTC) mask set GTC-305 and GTC-282. The GTC-305 design contained various analog circuits, such as sample and holds, op-amps, differential amplifiers and comparators and the GTC-282 design contained an op-amp. The data from GTC-305 and GTC-282 showed typical DC output levels that varied up to 100%. In addition, dynamic characteristics from GTC-305, such as gain and common mode rejection, had average variations of 40% between measured and simulated results. Discrepancies between measured and simulated results of this magnitude will render the simulations ineffective for small signal analog design. This in turn will prevent customers (both captive as well as commercial) from using GTC's Multi-function Self-Aligned Gate (MSAG) GaAs IC process. ITT-GTC's MSAG process is a paradigm of GaAs IC processes because of its state-of-the art results and unmatched versatility [3].

The prior approach at GTC to simulating these types of circuits involved using the program: Simulation Program for Integrated Circuit Emulation (SPICE), with a Junction Field Effect Transistor (JFET) model and no parameter optimization. Berkeley SPICE [4] is a widely used time domain simulator developed sixteen years ago and is commercially available (cost is approximately two-hundred dollars). However, SPICE has demonstrated the large aforementioned inaccuracies due primarily to poor agreement between measured and simulated DC I-V curves for the MSAG FETs. Furthermore, SPICE does not

include the capability to optimize the model parameters or model specific problems inherent to GaAs such as, backgating and frequency dispersion [5],[6]. This research work will focus on optimizing DC I-V curves and not improving frequency dependent properties of the SPICE model because much research has been done in this area [7],[8],[9]. The newest version of SPICE (version 3e.2) is written in "C" and contains silicon BJT, MOSFET and GaAs MESFET models. The principal GaAs models used in most commercial SPICE simulators are the JFET, Curtice, Statz or Raytheon, and TriQuint (TOM) models [10],[11],[12],[9]. This research will consist of using the existing physics based models and Taguchi methods [13],[14] for I-V curve optimization to improve the correlation between measured and simulated results for both digital as well as analog GaAs integrated circuits. This is the first known use of Taguchi methods to the optimization of parameters in an IC model.

This dissertation consists of eight different chapters. This chapter, Chapter I, is a general introduction. Chapter II presents a literature survey on SPICE models for GaAs and IC model parameter optimization. Chapter III consists of the methodology used to extract the IC model parameters from DC test. Chapter IV presents an evaluation of a commercial optimizer using JFET and Curtice models. Chapter V presents the results of the initial investigation into utilizing the Taguchi methodology. Chapter VI takes the results in Chapter

V and develops a practical implementation of the Taguchi method into the current manufacturing process as well as develop a method to obtain worst case model parameters. Chapter VII uses the results of the optimized model parameters from the previous chapters to design a differential amplifier using Taguchi methods. Chapter VIII presents the over all conclusions and appendices I and II lists the computer programs used in this research.

## CHAPTER II

### LITERATURE REVIEW

#### 2.1 INTRODUCTION

The literature review will consist of summarizing the SPICE models used in simulating GaAs MESFET analog and digital circuits over the last twenty years. This review is by no means inclusive of all the GaAs SPICE models developed over the years, but the purpose is to highlight the models that had the most significant impact on the industry. The review will start with the first SPICE model used to simulate GaAs circuits in the early 1970's up to the latest TOM model published in 1990. In addition, there will be a short review on model parameter optimization. The Levenberg-Marquardt algorithm was first applied to nonlinear least squares approximation in the early 1970's. However, it wasn't utilized in the optimization of IC model parameters until ten years later. IC model parameter optimization is a very limited and relatively new topic, with the initial paper on the subject published as recently as 1983.

## 2.2 REVIEW OF SPICE MODELS FOR GaAs

The Shichman and Hodges JFET model [10] is the first primarily used SPICE model to simulate GaAs MESFET devices through the first decade of GaAs IC simulation (1970-1980). The model was developed in 1968 to describe the behavior of silicon P-N junction FETs of either N-type or P-type channel. However, the model typically showed a poor fit for currents below saturation [11].

In 1980, the Curtice square law model [11] was introduced and included two significant attributes. First was the inclusion of a hyperbolic tangent term with an additional SPICE curve fitting parameter. The method was first proposed by Van Tuyl and Liechti, but not widely publicized. This eliminated two equations to model the linear and saturation regions, as well as gate voltage independence of saturation. Secondly, a variable was introduced to account for the transit time delay of the MESFET.

In 1983 and 1985, two modeling papers by Materka and Kacprzak [15],[16] were published which were the first to introduce  $I_{dss}$  or saturation current into the drain source equation. In addition, these authors were the first to incorporate threshold voltage as a function of drain to source voltage.

The Curtice cubic model was introduced in 1985 [17]. This model improves the DC curve fit of the first Curtice model [11] using a third order polynomial. Model parameter identification is more difficult with this model than the others. Furthermore, non-physical behavior can result for gate voltages below the threshold voltage [18].

The Statz or Raytheon model was reported in 1987 [12]. The three primary distinctions of this model are: 1) a polynomial expression to approximate the hyperbolic tangent, 2) uses the square law for small currents and square root law for large currents, 3) a charge conservation approach used for nodal capacitances.

A paper by Larson in 1987 reference [19] points out deficiencies in models [10] and [11]. In [10], the limitation is the square law relationship of drain current to gate voltage. In [11], the limitation is due to a poorer agreement for enhancement mode FETs than depletion mode FETs. The new model incorporates two new parameters that models a variable exponential expression between drain current and gate voltage, as well as accounting for early saturation.

The TriQuint or TOM model [9] was published in 1990 which is a modification of the Statz model [12]. The fit around the threshold voltage ( $V_t$ ) was improved by making  $V_t$  a function of the  $V_{ds}$  voltage. The non-square law term was used as reported

in [19]. Furthermore a term was added to account for a negative slope in the I-V curves at high currents and voltages.

### 2.3 REVIEW OF I-V CURVE OPTIMIZATION

The following is a brief synopsis of the optimization of SPICE model parameters to improve the accuracy of the simulation. These techniques and methods are not particular to a single model and can be used with any SPICE model. In 1972 the Levenberg-Marquardt algorithm was described for use in nonlinear least squares approximation [20]. The Levenberg-Marquardt algorithm combines two numerical techniques resulting in a synergistic algorithm for the parameter optimization. For instance, the algorithm numerically combines the Gauss-Newton method with the steepest descent method to give the largest stability in the minimization of the error away from the minimum and fast convergence near the minimum. This results in an easy to use and computationally fast algorithm that can optimize all model parameters concurrently in a single operation.

In 1982, the SUXES FET parameter extraction program for silicon devices was introduced [21]. This program became publicly available through Stanford University, but contained

no parameter optimization capability to improve the accuracy of the extracted parameters in the model.

The following year saw the Levenberg-Marquardt algorithm introduced into the SUXES program [22] to optimize the extracted model parameters and significantly improve the accuracy of the model. This program solved all model parameters simultaneously to limit interactions between the parameters and could be used for any generic SPICE model.

From 1985 through 1991, commercial software companies started to introduce optimization capability into their simulators based on the Levenberg-Marquardt algorithm. For example, Silvaco introduced Utmost in 1988, and Electrical Engineering Software introduced its optimizer in 1990. However, these optimizers are quite expensive (excess of \$ 40,000) and can be an unrealistic expense for most individuals and universities.

## **2.4 CONCLUSION**

Hence, SPICE models for GaAs have evolved from the JFET model, which was applied directly from silicon experience to the Statz and TOM models. These latter models were developed just for GaAs MESFET devices and addressed some of the particular anomalies associated with GaAs. The accuracy of these as well as any SPICE like models can be significantly

improved by optimizing the model parameters. The Levenberg-Marquardt algorithm was utilized to give a computationally fast method that can concurrently optimize all the model parameters to any SPICE like model.

The next chapter will explain the method to extract the model parameters from the actual measured devices. It will be these extracted parameters that shall undergo the optimization procedure to improve the accuracy between measured performance and simulated performance.

## CHAPTER III

### EXTRACTION OF DC TEST PARAMETERS

#### 3.1 INTRODUCTION

A description of the extraction of SPICE modeling parameters is in order prior to doing a comparison between measured and simulated I-V curves. The JFET model described in the previous chapter requires nine parameters to be used incorporated into the model ( $V_t$ ,  $R_s$ ,  $R_d$ ,  $C_{gs}$ ,  $C_{gd}$ ,  $V_{bi}$ ,  $I_{leak}$ ,  $\beta$ , and  $\lambda$ ). The threshold voltage or  $V_t$  is the value of gate voltage which causes the FET to cease conducting current.  $R_s$  and  $R_d$  are the parasitic source and drain resistances seen by the FET.  $C_{gs}$  and  $C_{gd}$  are the parasitic diode capacitances seen from gate to source and gate to drain.  $V_{bi}$  is built in schottky barrier of the FET and  $I_{leak}$  is the leakage current between the gate and the channel. These first seven parameters are actual physical quantities, whereas the last two are curve fitting parameters. All nine parameters can be extracted by methods that physically measure the FETs as shown in references [23,24]. However, only five of the nine parameters ( $V_t$ ,  $R_s$ ,  $R_d$ ,  $\beta$ ,  $\lambda$ ) have any effect on the DC I-V curves.

There is a serious problem with these extraction techniques. These extraction techniques are only exact for an

ideal set of I-V curves, which will rarely be seen in actuality. Hence, there will be a significant difference between measured I-V curves and simulated I-V curves. Furthermore, the discrepancy between extracted parameter I-V curves and simulated I-V curves are exacerbated by variations due to: different technologies, different processes, short channel effects and so on. Therefore, a feedback mechanism must exist to compare the measured and simulated I-V curves against each other and optimize the measured model parameters to give an improved fit. The I-V curve optimizer acts as this feedback mechanism. Chapter V will give further insight into extraction with respect to the over all design flow.

### **3.2 EXTRACTION PROCEDURE**

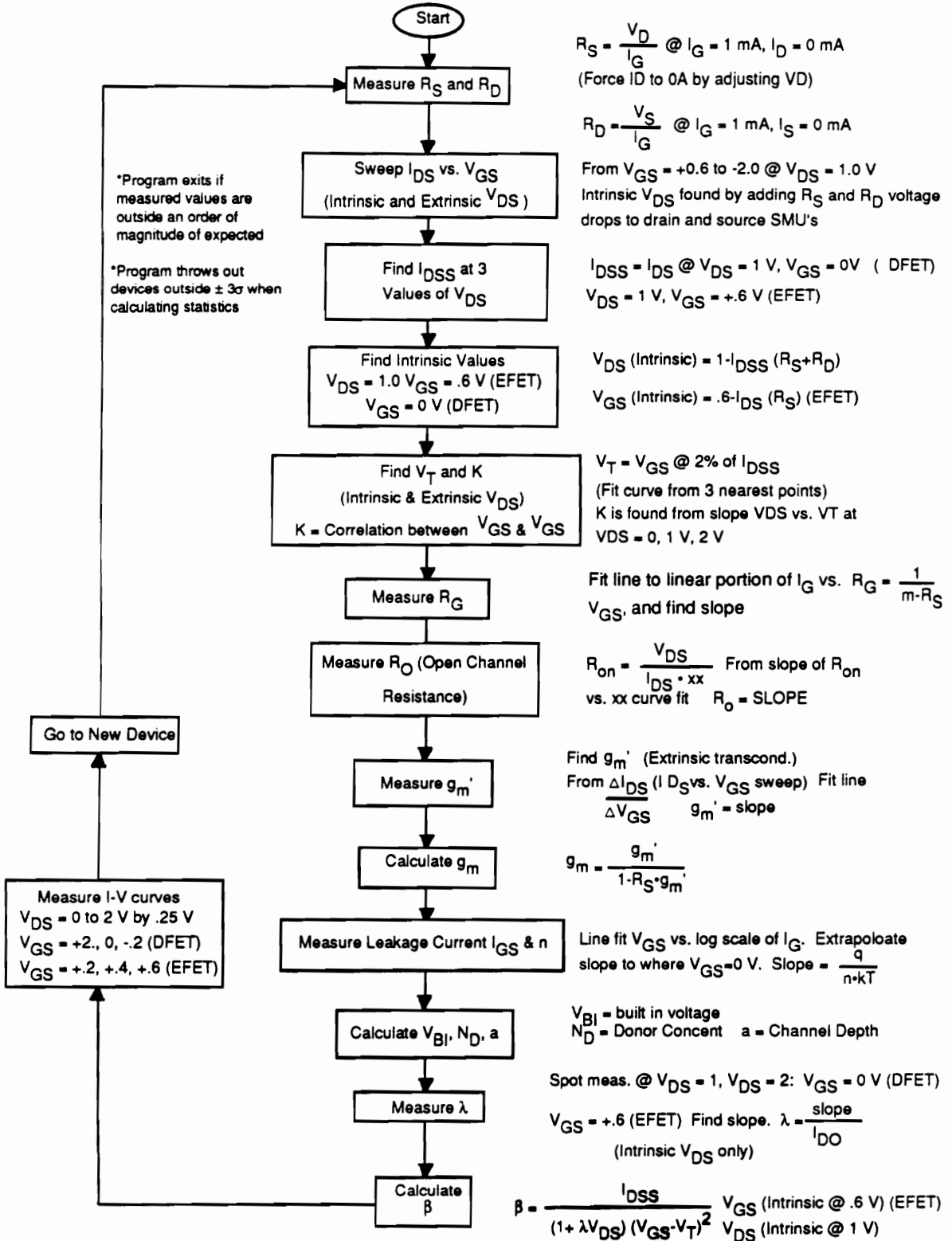
The measured DC data is attained by making on-wafer measurements of a 3-inch wafer that typically contains up to 50 Process Control Monitor (PCM) FETs. A rectangle encompassing a significant section of the 3-inch diameter wafer is chosen and all PCM FETs within this rectangle are evaluated for their measured DC parameters (threshold voltage, saturation current, transconductance, source resistance, drain resistance) and JFET SPICE parameters ( $\lambda$ ,  $\beta$ ) using techniques explained in [23],[24]. The mean and standard deviation for all SPICE modeling parameters as well as some additional parameters are determined with built-in hard limits

to eliminate bad data. The measured data was obtained using an HP-4142 parameter analyzer by sweeping the gate voltage from 0 to -1 V in 100 mV steps and the drain voltage from 0 to 2 V in 100 mV steps.

Figure (3.1) shows a flow chart of the currently used program at ITT-GTC for extracting the various FET and SPICE parameters. A modification to the aforementioned references is in the extraction of  $V_t$ . For instance,  $V_t$  is not found from the slope of the square-root of  $I_{ds}$  versus gate voltage as indicated in the references. Instead,  $V_t$  is found from the gate voltage that coincides with 2% of  $I_{dss}$ . This is the same method used by the fabrication engineers at ITT and allows direct correlation of their measurements. Finding  $V_t$  using both methods on numerous wafers showed the results to be quite close (within 20 mV). Another deviation from references [23,24] is in the calculation of beta. Instead of measuring beta from the slope of  $I_{ds}$  versus  $V_{gs}$ , beta is calculated as shown in Figure (3.1). This method guarantees very close agreement at the  $V_{ds}$  voltage  $I_{dss}$  is measured, which results in an overall improvement in the fit from the beta extraction technique in references [23,24].

The local and global variation in the threshold voltage was evaluated to determine if the FET characteristics in the PCM of a mask reticle or die could be applied to the circuit in that same reticle. However, an average wafer showed the

Figure (3.1). DC FET parameter extraction flow chart.



standard deviation of the threshold voltage ( $\sigma V_t$ ) within a 416 mm<sup>2</sup> area containing 8 FETs is 43 mV and the  $\sigma V_t$  within a 1156 mm<sup>2</sup> area containing 23 FETs is 37 mV. This result shows the intradie local parameter variation is less than 416 mm<sup>2</sup> and it is useless trying to localize the FET parameters of a particular die within the circuit of that same die. Hence, the FET data and circuit data must be averaged over the wafer for comparison purposes. The FET extraction program has the capability to filter outliers in the database to obtain a meaningful representation of the averaged FET parameters for an entire wafer without corruption from outliers. The program can eliminate data outside one, two or three standard deviations and recalculates the data set without the outliers. For example, one average wafer contained a total of 49 FETs, which were averaged together giving a  $\sigma V_t=62$  mV. All FETs outside  $\pm 3\sigma$  were thrown out (1 device) and the devices re-averaged. The new  $\sigma V_t$  became 29 mV because that one bad device was throwing the  $\sigma V_t$  off considerably. Next, all devices within  $\pm 1\sigma$  of this new average were averaged together to give an even smaller population of 36 FETs with a  $\sigma V_t=17$  mV. However, unless otherwise stated the standard outlier filter is set-up to eliminate data outside  $\pm 3\sigma$ .

The next chapter will graphically show the large discrepancy between measured and simulated I-V curves based on the extraction of DC parameters described in this chapter. Furthermore, a commercial optimizer will be evaluated using

two different IC models.

## CHAPTER IV

### PRECISE OPTIMIZER EVALUATION

#### 4.1 INTRODUCTION

This chapter will show the significant benefits and tradeoffs to modeling I-V curves with a commercial SPICE simulator and optimizer from Electrical Engineering Software. The simulator uses a modified version of Berkeley SPICE called PRECISE. The software contains various models for simulating GaAs FETs, such as the JFET, Curtice and Statz models. This work will only evaluate the JFET and Curtice models due to convergence problems found using the Statz model. The PRECISE optimizer uses the Levenberg-Marquardt algorithm as described in Chapter II to do the optimization. The goal of this chapter is to examine the many optimization routines offered to the user and determine if one is superior for the particular measured data. For instance, different parameters in the model will be optimized and an additional parameter ( $R_{ds}$ ) will be added to determine its effect on the fit. Furthermore, the extracted parameters from DC test will be done at different  $V_{ds}$  values giving a significantly different set of simulated I-V curves. The last option to be evaluated in the PRECISE optimizer will be the curve weighting capability in which the

priority to fit each curve can be varied or weighted.

#### 4.2 JFET MODEL

The Shichman and Hodges JFET model found in SPICE has been used extensively to simulate the I-V characteristics of GaAs MESFETs because of the relatively good agreement, widely available model, and simplicity of parameter extraction [25]. Now that the DC and SPICE parameters have been obtained, a plot can be generated showing a comparison between measured and simulated results. Figures (4.1) and (4.2) show plots of the measured versus the simulated I-V curves for  $V_{gs}=0.0$ ,  $-0.1$ , and  $-0.2$  V. The SPICE parameters are extracted at  $V_{ds}=1.0$  V in (4.1) and  $V_{ds}=2.0$  V in (4.2) and are listed along with the DC parameters. This is a graphical portrayal of the need for curve optimization. The large variation between measured and simulated I-V curves has been the principal reason for the poor agreement between measured and simulated analog designs. These figures show the measured and simulated curves agree quite well around the set  $V_{ds}$  voltage, but deviate significantly elsewhere. This close agreement around the set  $V_{ds}$  voltage is due to a modification in the calculation of beta from the referenced FET parameter extraction procedure. If the reference was followed verbatim (calculating beta from the slope of  $I_{ds}$  vs.  $V_{gs}$ ) the fit would be significantly worse. Furthermore, the values for the threshold voltage when plotted at other  $V_{ds}$  values as well

MEASURED VS. ACTUAL SIMULATED FOR 305-3-5

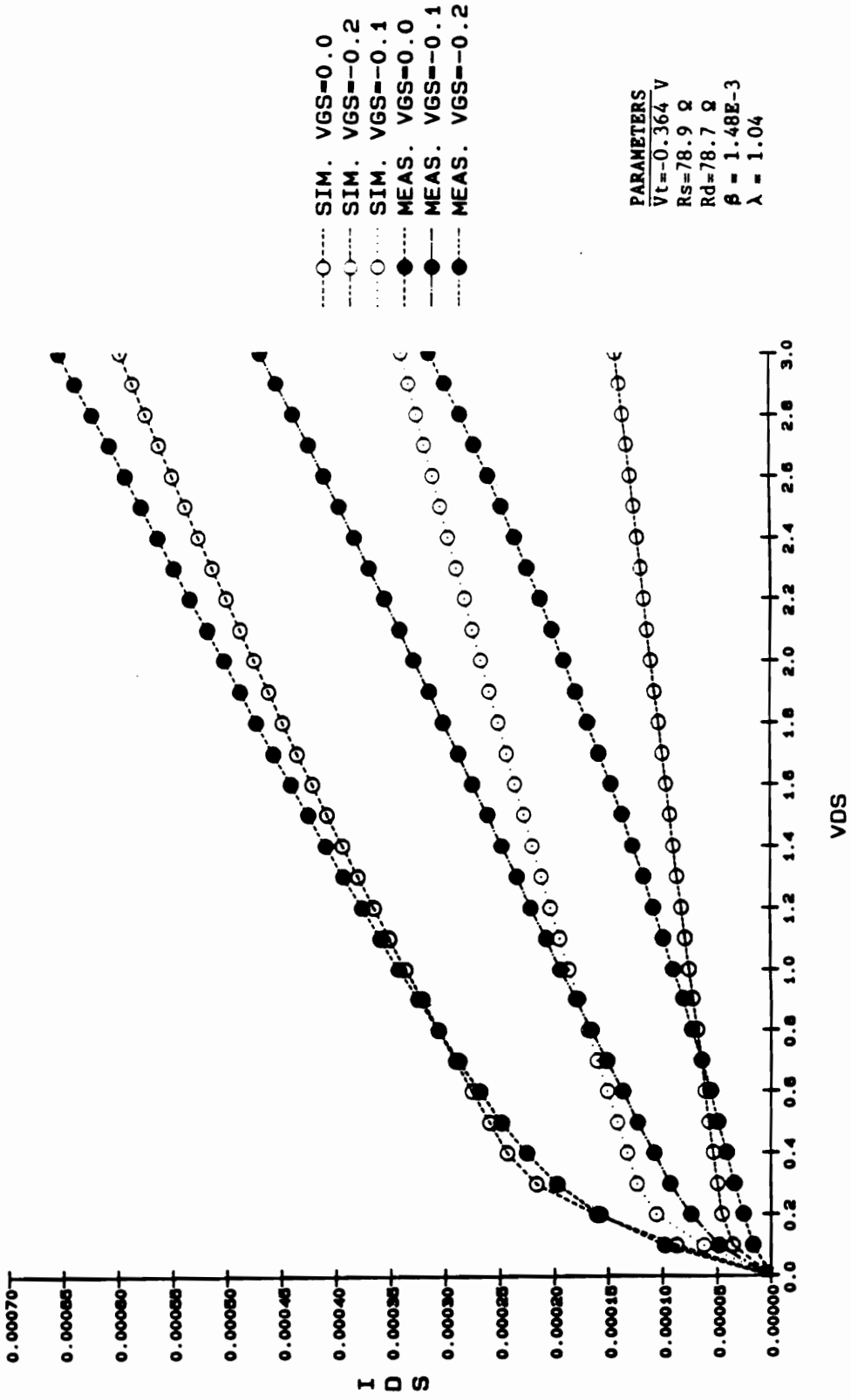


Figure (4.1). Measured versus simulated I-V curves at Vds=1.0 V.

MEASURED VS. ACTUAL SIMULATED FOR 305-3-5

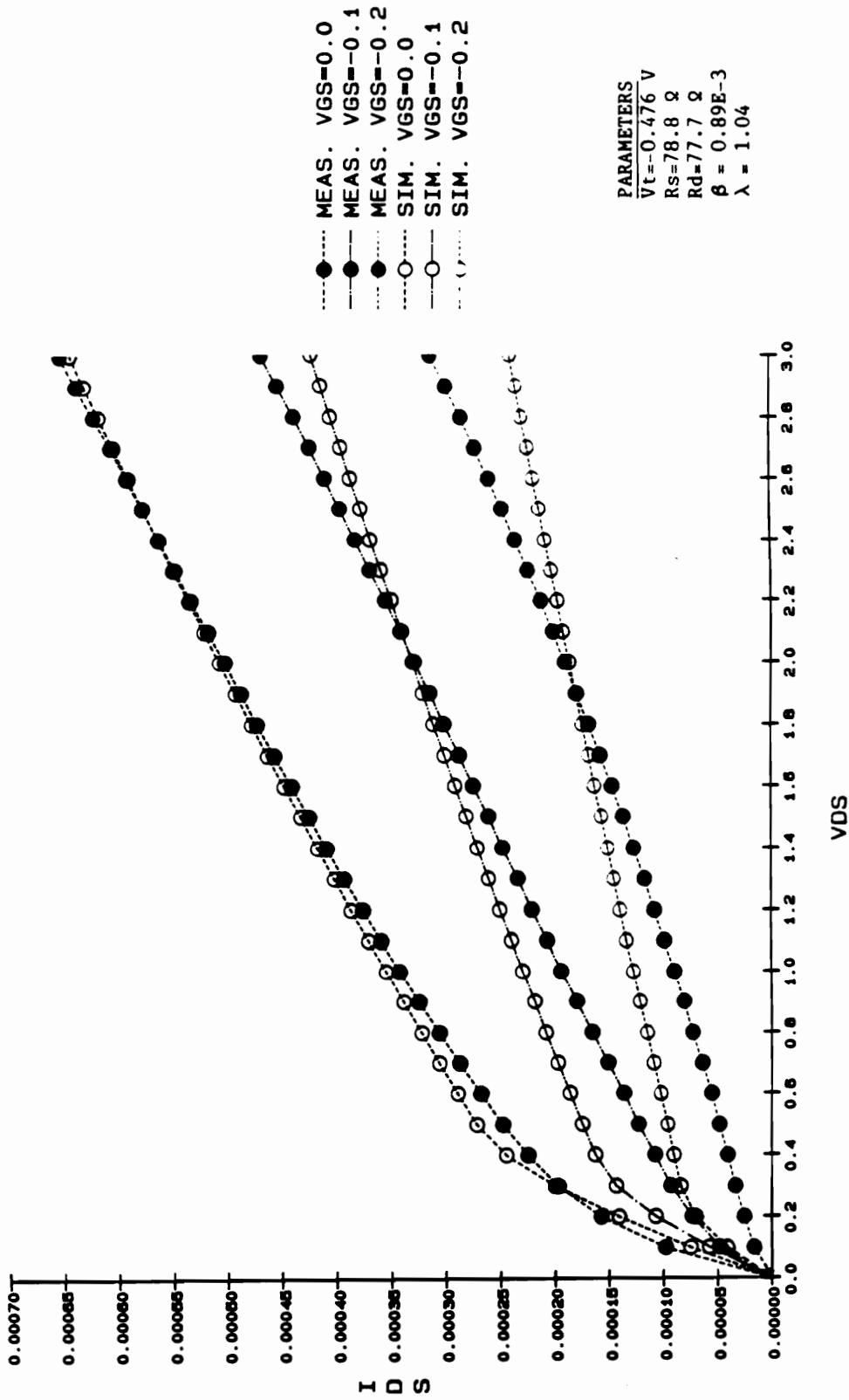


Figure (4.2). Measured versus simulated I-V curves at  $V_{ds}=2.0$  V.

show a distinct relationship as a function of  $V_{ds}$ . Reference [9] incorporates this behavior into the TOM model.

This non-ideal fit leads us to the optimization issue, which is the next step to improve the fit between measured and simulated data. Optimization is a very powerful technique that modifies the various FET parameters and compares them to a given set of curves to improve the fit between measured and simulated results [22]. Chapter V will cover optimization using the Taguchi approach. PRECISE contains optimization routines that have a wide range of capabilities. Figures (4.3) through (4.5) shows results for a progression of optimization techniques. In Figure (4.3) the SPICE parameters lambda and beta were optimized only from measured parameters at  $V_{ds}=1.0$  V and a resistor was added to the JFET model between source and drain  $R_{ds}$ . In Figure (4.4) again only lambda and beta were optimized, but a weighting function was used. The weighting function weighted the importance of each curve on a 4-2-1 ratio, which reflects the relative magnitude of current between the curves. In other words, the  $V_{gs}=0.0$  V curve carried 4 times as much significance in the optimization routine as the  $V_{gs}=-0.2$  V curve. Lastly, Figure (4.5) shows the curves being weighted and optimized with lambda, beta, and  $R_{ds}$ . Table (4.1) lists the absolute error (ABSERR) for the various techniques used to obtain the SPICE parameters and the percent improvement from directly incorporating the measured SPICE parameters into the model. The ABSERR is the RMS value

























































































































































































































































