A SiC JFET-Based Three-Phase AC PWM Buck Rectifier

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ABSTRACT

Silicon carbide (SiC) power switching devices promise to be a major breakthrough for new generation ac three-phase power converters, offering increased junction temperature, low specific on-resistance, fast switching, and low switching loss. These characteristics are desirable for increasing power density, providing faster system dynamics, and improving power quality. At present, the normally-on SiC JFET prototypes available from SiCED are the first SiC power switches close to commercialization. The objective of this work is to characterize the switching behavior of the prototype SiC JFET devices, as well as demonstrate the feasibility of achieving high switching frequency for a 2 kVA three-phase converter.

The switching characterization of the 1200 V SiC JFET prototypes is shown for a wide range of operating conditions such as switched voltage, switched current, and junction temperature. The SiC JFET is shown to be a fast-switching, low-loss device offering performance benefits compared to traditional silicon (Si) power devices of similar ratings.

Utilizing the SiC JFET, a three-phase ac buck rectifier is then demonstrated with a 150 kHz switching frequency and a rated power of 2 kVA. Additionally, improvements are made to the charge control scheme for the buck rectifier allowing power factor compensation and reduction of input current transients.

A

this work is dedicated to my kiera

to my parents

to my crazy brother

to the rest of my family

to those that have supported me

Ω

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

1.1. Motivation

Silicon carbide (SiC) power switching devices promise to be a major breakthrough for the new generation of AC three-phase power converters, offering increased junction temperature, low specific on-resistance, fast switching, and low switching loss. These characteristics are desirable for increasing power density, providing faster system dynamics, and improving power quality. In applications where high performance and high density AC converters are critical, such as electric and hybrid cars, electric ships, and more-electric aircraft, capitalizing on the advantages offered by SiC power switching devices potentially offers a major breakthrough with a significant impact on overall system performance. For example, a simultaneous reduction in weight and increase in efficiency of AC converters on board more-electric aircraft benefits the entire system, as fuel consumption decreases and economy is thus increased.

Already, SiC Schottky-barrier diodes (SBDs) are available commercially, and have demonstrated significant reduction in converter switching losses due to their practical elimination of the reverse recovery effects that dominate the silicon (Si) power diode switching behavior [1]. The benefits of using SiC SBDs are well known, and an increasing number of high-performance converters are employing the SiC SBD in combination with Si IGBTs or MOSFETs. Clearly, the next step is to replace the Si power switches with SiC devices in order to realize the full potential of elevated junction temperatures and fast switching.

The main device structures being studied for the implementation of a controlled switching device fabricated in SiC are the IGBT, MOSFET, and JFET. The SiC IGBT shows great promise for applications requiring blocking voltage in excess of several kV (3 to 5 kV and higher), leaving the FET structures as the device of choice for mid-to-lower voltage applications. Currently, the SiC MOSFET has reliability problems due to the interface of the gate oxide layer with SiC, especially at elevated temperatures. As a result, the SiC JFET was developed in order to avoid the gate oxide reliability problems, as no oxide is required to form the device gate [2].

At present, the normally-on SiC JFET prototypes available from SiCED are the first SiC power switches close to commercialization. Prototype JFET devices with a blocking voltage exceeding 1200 V and a current capability of 5 A have been obtained for the purpose of

characterizing their switching performance and demonstration in a three-phase current-type buck rectifier. The overarching motivation of this thesis is to experimentally demonstrate application of the SiC JFET in a three-phase ac converter at a 2 kW power level with 150 kHz switching frequency, which is not practically feasible with traditional Si devices. For many applications, increasing the switching frequency is desirable for reducing the size of passive components and increasing the system dynamic performance. The target switching frequency of 150 kHz has been identified as one of the optimal points for reduction of input filter size for applications in more-electric aircraft.

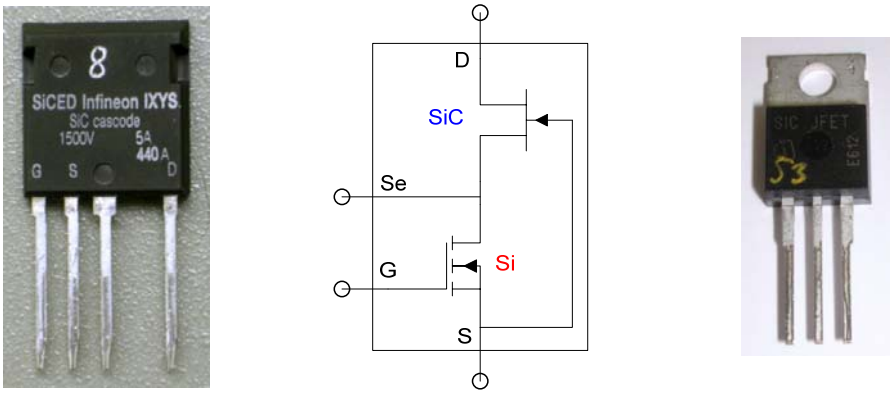
1.2. The SiC JFET

1.2.1. Prototype Device Fabricated by SiCED

The structure of the normally-on SiC JFET was discussed in detail by SiCED in [2]. There were 2 JFET structures proposed—one which offered lower on-resistance but high miller capacitance (called type A), and one which offered increased on-resistance and lower miller capacitance (called type B). Because of the increased miller capacitance, devices of type A place more current demand on the gate drive circuit, and yield lower switching speed. Type B devices, however, are capable of much faster switching, and still have on-resistance lower than comparable Si devices. Thus, type B was chosen as the preferred structure.

Prototype SiC JFET devices with a 1200 V and 5 A rating are available in limited quantities for evaluation. Initially, the SiC JFET was packaged in a cascode structure with a low-voltage SiC MOSFET in an IXYS ISOPLUS i4-Pac package (Fig. 1-1) in order to provide a normally-off 3-terminal equivalent switch. In this way, the gate of the MOSFET can be driven using a conventional MOSFET gate drive circuit. When the Si MOSFET is turned off (by applying 0 V to the gate), it begins to block voltage; this blocked voltage appears as a negative voltage from the SiC JFET gate to source. When V_{DS} of the Si MOSFET reaches the negative pinch-off voltage of the SiC JFET, the JFET is then turned off, blocking the remainder of the drain voltage. This cascode connection, however, limits overall switch performance in that maximum operating temperature is limited by the presence of the Si MOSFET, switching time and losses are increased, and total on-resistance is increased. For these reasons, it is thus desirable to use only the normally-on SiC JFET; pins G and S may be shorted together and used as the JFET gate,

while pins D and S are the JFET drain and source, respectively. This allows the SiC JFET to be operated in an effectively isolated manner, leaving only a small parasitic capacitance from gate to source of the JFET due to the presence of the Si MOSFET. Recently, the SiC JFET has been made available in a single JFET-only TO-220 package, as pictured in Fig. 1-1c.



(a) (b) (c)

Figure 1-1. The SiC JFET: (a) cascode package and (b) circuit diagram, and (c) JFET only in the TO-220 package.

1.2.2. SiC JFET Static Characteristics

The JFET on-resistance measurement is necessary for calculation of conduction losses. For the gate driver design, it was necessary to measure the pinch-off and gate breakdown characteristics. The static characteristics presented were measured using the cascode-packaged device with the SiC JFET effectively isolated as described previously.

1.2.2.1. On-Resistance

The on-resistance ($R_{DS,on}$) of the SiC JFET in the cascode package was measured and is plotted against device junction temperature in Fig. 1-2. As the device is normally-on, the on-resistance was measured with 0 V applied to the gate. Though the device may be driven with a small positive voltage (less than 2 V) in order to marginally decrease the on-state resistance, the benefit is minimal [3, 4]. This incremental performance increase is outweighed by the complexity required of the corresponding gate drive circuit implementation. For simplicity and increased reliability, we chose to use 0 V for device turn-on.

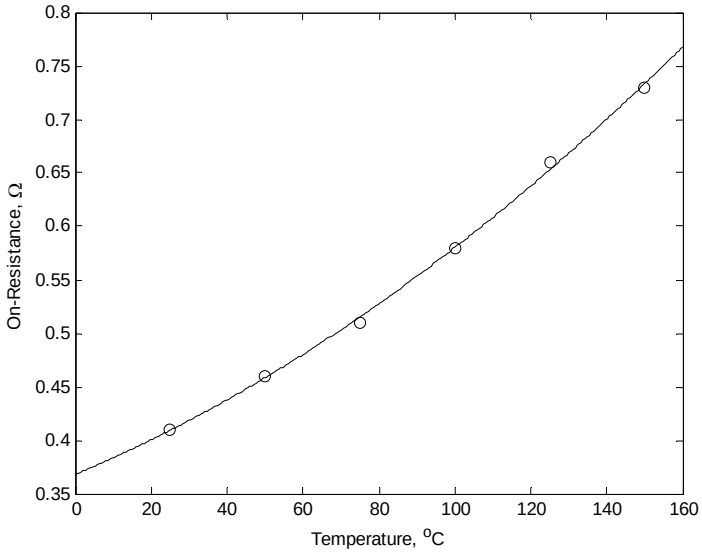


Figure 1-2. On-resistance of the SiC JFET vs. junction temperature (courtesy of Yi Wang and Dr. T. P. Chow, Rensselaer Polytechnic Institute).

1.2.2.2. Pinch-Off Voltage

The normally-on SiC JFET is a voltage-controlled device requiring a negative voltage to be applied to the gate-source junction in order to hold the device in its off-state. In Fig. 1-3, the drain current of a typical device is plotted versus its gate-source voltage for several junction temperatures. The pinch-off voltage was observed to be –17.5 V at room temperature, and became slightly more negative as temperature increases. For all of the cascode-packaged prototype devices tested, the pinch-off voltages were in the range of –17 to –18 V.

The upper magnitude limit of the negative gate voltage that can be applied is determined by the reverse avalanche breakdown voltage of the gate-source junction. Though the device maintains an off-state during gate breakdown, it draws a continuous large current from the gate drive circuit, making such operation undesirable. From Fig. 1-4, a typical plot of the gate current versus the gate-source voltage, we observed that the gate breakdown occurs at –24 V at room temperature, and approaches –23 V as temperature increases.

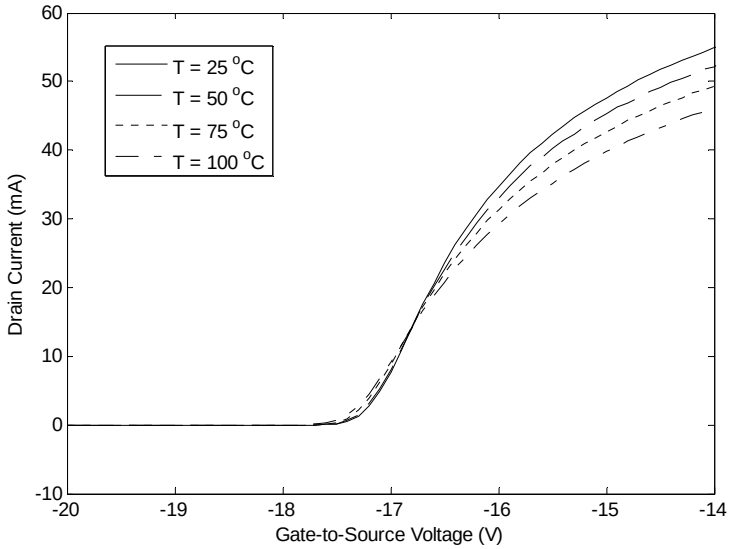


Figure 1-3. Pinch-off voltage of a typical SiC JFET in cascode package, with JFET effectively isolated from the Si MOSFET (courtesy Yi Wang and Dr. T. P. Chow, RPI).

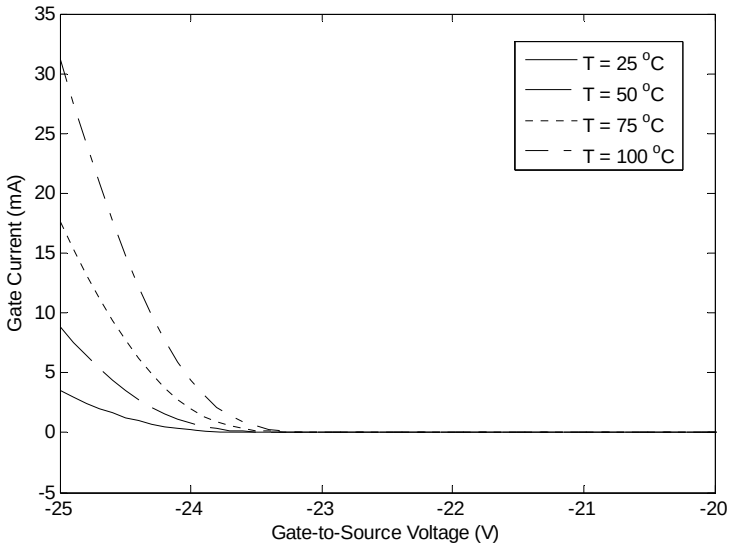


Figure 1-4. Reverse breakdown of the gate-source junction (courtesy Yi Wang and Dr. T. P. Chow, RPI). *(Note: the direction of the gate current is flowing out of the JFET gate terminal.)*

Previous reports had shown that the SiC JFET pinch-off and gate breakdown voltages varied widely between individual devices [3, 5, 6]. Pinch-off voltages were reported in the range of –22 to –35 V, and gate breakdown voltages were reported in the range of –25 to –45 V. In contrast, results from testing these particular cascode-packaged JFETs indicate more uniform characteristics.

More recently, TO-220 packaged JFETs were obtained and tested. Although the characteristics were not as uniform as the cascode devices tested, they were more uniform than previously reported [3, 5, 6]. Among the TO-220 packaged JFETs received, half of them were fabricated with a target pinch-off of –19 V and the other half were fabricated with a –22 V target. For the –19 V target devices, the lowest pinch-off voltage is –18.2 V and the highest is –20.7 V. The –22 V target devices ranged from –21.6 to –24.6 V.

1.3. Survey of Previous Works on the SiC JFET

1.3.1. Device Characterization

Characterization of the cascode-packaged SiC JFETs was presented in [7]. The turn-off times were shown to be under 300 ns for the equivalent 3-terminal switch. Though the series connection of the body diodes of both the SiC JFET and the Si MOSFET in the cascode package could serve as the anti-parallel diode, the reverse recovery behavior was very poor due to the Si MOSFET body diode that dominated the turn-off action. Short-circuit capability of the cascode package was also demonstrated, with the device sustaining 600 V and an average of 3 A for 1 ms. The short-circuit current began at 3.8 A, but reduced due to the resistance increase as the SiC JFET junction temperature increased.

Typical switching waveforms of the SiC JFET have been demonstrated in both [6] (isolated JFET in cascode package) and [3] (JFET only in TO-220 package). Though the focus of these works was on the gate drive design, switching times and energies were shown for a limited number of operating conditions. The results presented are a valuable benchmark for assessing the performance of the SiC JFET and providing a reference point for future characterization; however, the data presented was not complete enough to be used for the loss calculations required for the design of a converter.

1.3.2. Gate Drivers for the Normally-on SiC JFET

A gate drive circuit for the SiC JFET must provide sufficient charge to negatively-bias the gate-to-source junction, however, should not apply excessive gate voltage. A voltage-based gate driver has a narrow range of the gate voltage that may be applied in order to turn off the device yet prevent gate breakdown; this window is on the order of 4 to 5 V between complete pinch-off and gate breakdown. The challenge is increased by the fact that it is common for the gate

characteristics from device-to-device may vary significantly. Here, several approaches to the gate drive design are summarized.

A SiC JFET gate drive circuit requiring a dual-ended power supply was presented in [4]. The gate drive power supply voltages must be set independently for each device, as there is no protection for ensuring that gate breakdown is not reached. If the JFET device being driven is changed and the gate driver is not recalibrated, there is the likelihood that the gate driver will not drive enough gate voltage in order to completely pinch-of the device, or the gate driver will apply excessive voltage, causing gate breakdown.

To deal with the gate breakdown problem, the gate drive circuit presented in [5] utilized a transistor to switch a diode in and out of the gate drive circuit path in order to limit gate current during gate breakdown. In this way, a single gate voltage may be chosen as long as it is greater than the highest possible pinch-off voltage. As such, the devices may be driven into gate breakdown, which is non-destructive to the SiC JFET. The switched diode is used to limit the gate current, thus reducing gate drive loss should gate breakdown occur. The impedance of the gate network must be designed with consideration of the converter switching frequency.

Another gate driver capitalized on the fact that the SiC JFET can be biased with a negative gate voltage while still remaining in a conducting state [8], although the on-resistance in this case is higher than for 0 V applied to the gate. The advantage is that a conventional MOSFET driver with a relatively low voltage swing may be used. For example, a constant dc bias of -9 V was applied to the gate, and the driver provided an additional -13 V swing. In this manner, the JFET was considered to be in an on-state at -9 V, and was turned off completely when the driver swings low, for a total of -22 V applied to the gate. While this gate drive is a viable fast-switching option using conveniently available gate drive ICs, the disadvantage of this method is that the conduction losses are increased.

A gate drive capable of automatically adapting to the pinch-off and gate breakdown characteristics of the JFET being driven was presented in [6]. Refinement was shown later in [3], ultimately resulting in an elegant solution whereby a simple R-C-D network was placed in the gate drive path, as shown in Fig. 1-5. This network is capable of limiting gate current during operation in the gate breakdown region. The gate drive voltage V_S was chosen to be more negative than the lowest pinch-off voltage of any JFET that may be driven. During the turn-off transient, the gate current flows through the capacitor until it charges the capacitor to the

difference between V_S and the gate breakdown voltage, at which point the JFET is held securely off. In this manner, any gate drive power stage may be used as long as it can provide the negative voltage large enough to pinch-off the device.

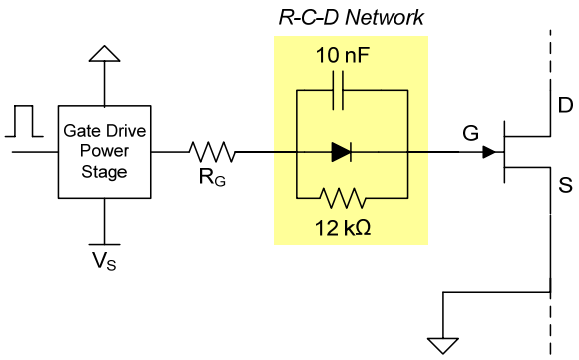


Figure 1-5. Generic gate drive based on the R-C-D network presented in [6].

The gate drive circuit presented in [9] includes short-circuit and negative voltage protection for the JFET. The JFET gate breakdown condition is not addressed, however. In the work, it was cited that a disadvantage of the proposed gate drive circuit was that the gate drive power stage contained a capacitor that must be sized according to the switching frequency of the JFET. If this capacitor was too small, it caused a transistor in the power stage to turn on at an inappropriate time, causing a low-resistance short of the gate drive power supply.

The gate drive circuit presented in [10] used a constant-current source principle to drive the SiC JFET. The main advantage cited was that despite the relatively high gate drive supply voltage, the SiC JFET gate junction was not continually operated in breakdown; this was due to driving the gate with only the necessary voltage to charge all junction capacitances and pinch off the channel. In [11], however, it was suggested that the JFET gate should be driven with a voltage driver rather than a current driver. Though driving the JFET gate with a current is possible, it cannot limit the gate voltage, thereby increasing the risk of gate breakdown. The gate drive circuit presented utilizes a small positive voltage (roughly 3 V) to turn on the JFET, and a negative voltage of –25 V to turn off the JFET. The gate drive signal is isolated using a magnetic isolation device (Iso-Loop) that is claimed to be faster than optocouplers, fiber optics, and standard pulse transformers. A commercially-available gate drive power stage is used (IXYS IXDD414). Gate breakdown is not addressed, but JFET over-voltage and short-circuit protections are included.

More recently, [12] presented a gate drive circuit that uses a transformer in the gate drive path, thus avoiding the need for isolated gate drive power supplies. This gate drive circuit may be thought of as a flyback converter that takes advantage of the JFET gate-source junction diode acting as the freewheeling diode. For the normally-on JFET, it could be disadvantageous to use this gate drive, since the time the switch may be held off is governed by the discharge of a capacitor that holds the turn-off gate voltage across the JFET gate-source. Recommended applications for this gate drive are in half- and full-bridge dc-dc topologies, or in topologies using transformer-isolated dc output.

1.3.3. Application of the SiC JFET in Three-phase Converters

A three-phase voltage-source inverter using SiC JFETs was demonstrated in [4]. The converter operated at 4 kHz switching frequency and had no additional anti-parallel diodes; instead, the body diode of the JFET was used as the anti-parallel diode. Although the body diode of the SiC JFET had relatively high conduction loss, its recovery time was very fast.

In [13], a motor drive was demonstrated using SiC MOS-enhanced JFETs and SiC SBDs fabricated, packaged, and tested at Rockwell Scientific. Even at a low switching frequency of 4 kHz, benefits were seen in reduced size and increased efficiency compared to a Si-based motor drive.

Loss calculations presented in [14] showed that a very-sparse matrix converter utilizing the SiC JFET cascode device can achieve a switching frequency greater than 7 times higher than achievable with comparable Si IGBTs in the same topology. The comparison was based on losses and device utilization. Later, a three-phase sparse matrix converter with 150 kHz switching frequency using only the SiC JFET for the power switch was proposed [6]. A gate driver for the SiC JFET was developed; however, experimental results of the proposed converter are yet to be presented.

1.4. Topology Considerations for the Normally-on SiC JFET

Perhaps the most popular three-phase ac hard-switching converter topology is the voltage-source converter (VSC) type, pictured in Fig. 1-6a. Concerns arise, however, when using a normally-on device such as the SiC JFET with the VSC topology. Under certain conditions, including converter startup and loss of gate drive power, the JFET will return to a normally-on

condition, thus allowing for shoot-through of the dc voltage link. Without the development of adequate protection schemes, there is a lack of inherent ruggedness when using the SiC JFETs in voltage-type converters.

On the contrary, it is advantageous to use the current-source converter (CSC) topology, as pictured in Fig. 1-6b, given the normally-on characteristic of the SiC JFET. The CSC naturally favors normally-on switching devices for inherent ruggedness and simplicity of implementation. Under certain faults, including the loss of gate drive control power, the SiC JFETs return to a normally-on state, reducing the topology to a three-phase diode bridge rectifier. This dc-link current will have a natural freewheeling path, thus avoiding the inductor open-circuit condition. Thus, for the purpose of demonstrating a hard-switching converter using the SiC JFETs at high switching frequency, the CSC topology is chosen.

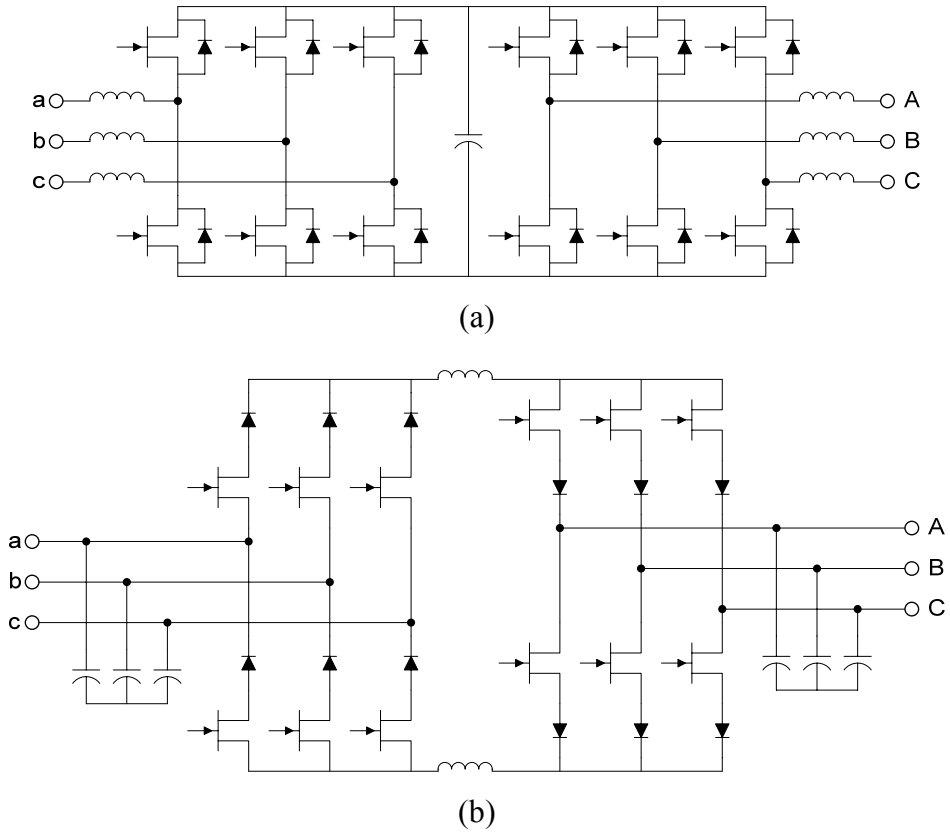


Figure 1-6. Back-to-back (a) voltage-source converter (VSC) and (b) current-source converter (CSC) topologies.

1.5. Objectives

1.5.1. Switching Characterization of the SiC JFET

As the SiC JFET is a prototype device, a datasheet providing the device characteristics vital for the design of a converter is not currently available. Thus, the requisite step before design and implementation of a converter is first the characterization of the SiC JFET device. The relevant static characteristics have been presented earlier in this introduction. The dynamic switching characterization is presented in Chapter 2 of this work. First, a gate drive circuit design based on the relevant static characteristics is presented. Then, the results of a two-pulse experiment show the turn-on and turn-off characteristics for various operating conditions, including junction temperature (T_j) up to 200 °C, switched voltage (V_{dc}) up to 600 V, switched current (I_{dc}) up to 5 A, and gate resistance (R_G) from 1 to 10 Ω. Finally, some comparisons are made to switching performance of Si IGBT and Si MOSFET devices with similar ratings.

1.5.2. Demonstration of SiC JFET in the Current-Type Buck Rectifier

As previously discussed, it is advantageous in the sense of simplicity and ruggedness to use the SiC JFET in the current-type topology. The three-phase buck rectifier pictured in Fig. 1-7 is designed, simulated, and demonstrated experimentally. The demonstration unit uses the 1200 V, 5 A SiC JFETs from SiCED packaged individually in TO-220 packages, as well as 1200 V, 15 A SiC SBDs. Nominal electrical operating conditions are summarized in Table 1-1.

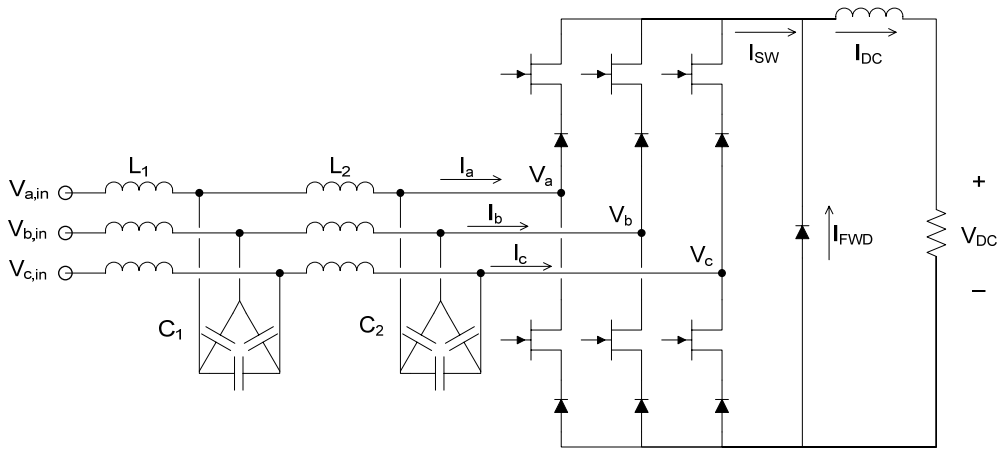


Figure 1-7. The three-phase buck rectifier topology with input filter, freewheeling diode, and resistive load.

TABLE 1-1: NOMINAL OPERATING CONDITIONS OF THE BUCK RECTIFIER

Input Voltage $V_{ac,ph}$:	230 V_{RMS}
Line Frequency:	400 to 800 Hz
Switching Frequency:	150 kHz
Load Current I_{dc}:	5 A
Rated Power:	2 kVA

Chapter 3 discusses the converter design, including semiconductor loss calculation, thermal design, and controller design. For the semiconductor loss calculations, the SiC JFET data presented in Chapter 2 is utilized. The controller design is based on the charge controller concept presented in [15] with addition of a modification allowing phase compensation of the input currents up to ±30°. The phase compensation for this charge control method is developed and presented in this work. Additionally, an improved charge control scheme resulting in dramatically reduced THD of the input currents is proposed.

The objective of Chapter 4 is to experimentally demonstrate the SiC buck rectifier with high switching frequency. The SiC JFET device switching performance in the buck rectifier is compared to the switching characterization results from the two-pulse test. For nominal operating conditions, the basic converter functionality is demonstrated. The measured converter losses are also compared to the theoretical calculations. Additionally, common-mode noise issues are briefly discussed.

Finally, Chapter 5 summarizes the work and highlights the lessons learned from both device characterization and the converter demonstration. Future work, including increasing the converter switching frequency to 300-400 kHz, the next optimum point for filter size reduction for the particular application, is also briefly discussed.

2. SWITCHING CHARACTERIZATION OF THE SIC JFET

2.1. SiC JFET Devices Used

The SiC JFET prototype cascode-packaged devices obtained from SiCED are rated for blocking voltage above 1200 V, with a current rating of 5 A. The relevant static characteristics of the device were presented in Chapter 1. In order to isolate the SiC JFET in the cascode package, the external connections shown in Fig. 2-1 were used. Pins G and S were shorted together and used as the JFET gate, while pins D and S were the JFET drain and source, respectively. This connection leaves only a small parasitic capacitance from gate to source of the JFET due to the presence of the Si MOSFET.

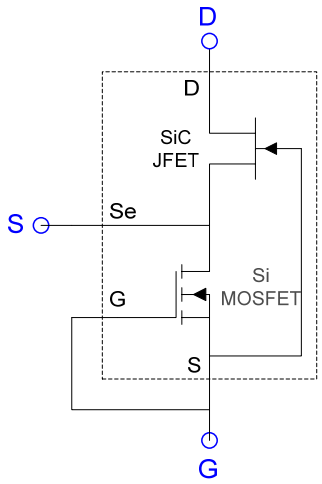


Figure 2-1. Connection of SiC JFET cascode circuit used to effectively isolate the JFET.
*(Package terminals indicated by **black font**, effective JFET terminals indicated by **blue font**.)*

2.2. Design of Gate Driver and Two-Pulse Test

2.2.1. Gate Driver Design

In previous works on the gate drive circuit for the SiC JFET, the wide variance in pinch-off and gate breakdown voltages for earlier prototype devices led to the design of a gate drive circuit capable of adapting to the characteristics of the particular device being driven, without the need to manually tune the gate drive bias voltage for each device [5, 6]. However, it was observed in

the test results of the cascode-packaged SiC JFETs presented in Chapter 1.2.2 that the device gate characteristics were more uniform in behavior. The increased uniformity of these devices led to the development of a simplified gate drive circuit. As the pinch-off voltage varied by less than 1 V among all devices tested, a self-adapting gate drive was not necessary. A circuit with fewer components, thus simpler and more reliable operation, was then developed.

Considering the narrow range of voltages that could be applied to ensure complete device turn-off yet avoid reaching gate breakdown (between –18 and –23 V), we chose to drive the device with –20 V for turn-off. As mentioned previously, 0 V was used for device turn-on. The specific gate drive circuit employed (Fig. 2-2) consisted of an optical-isolation and gate drive stage (an HCPL-3120 IC), a gate resistor, and an optional zener diode circuit. For the optical-isolation and high-current output gate drive stages, the HCPL-3120 was chosen due to its simplicity in that it integrates both functions into a single package. An optional zener diode clamp circuit may be connected from the JFET gate to source in order to prevent the JFET from being driven into the gate breakdown region by clamping any over-voltage spikes on the gate signal to –20.7 V. The clamp circuit adds a small parasitic gate capacitance whose effects are negligible compared to the presence of the parasitic Si MOSFET in the cascode package. For the device characterization results presented later, the zener diode circuit was not used. Basic operation of the gate drive circuit is demonstrated in Fig. 2-3.

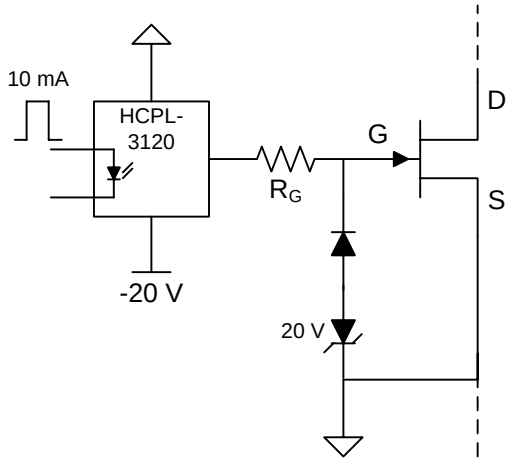


Figure 2-2. Simplified gate drive for use with SiC JFET.

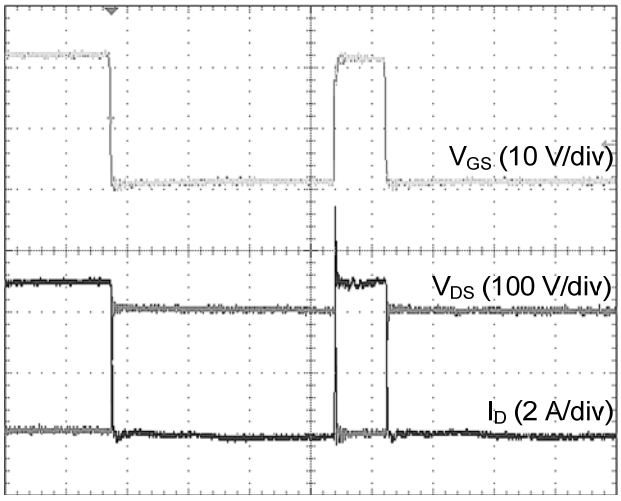
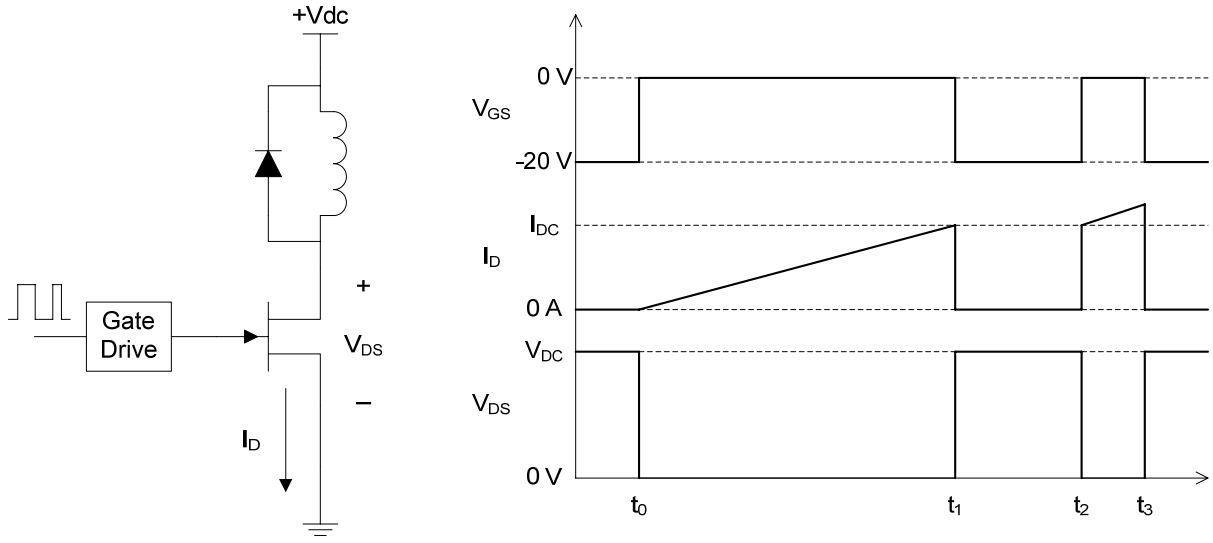


Figure 2-3. Demonstration of gate drive (Tj = 125 °C, R_G = 5 Ω, time: 1 μs/div).

2.2.2. Two-Pulse Test Concept and Test Fixture

The two-pulse inductive-load switching test is a standard method used to characterize the dynamic behavior of a power switching device. A simplified two-pulse test schematic and basic waveforms are shown in Fig. 2-4. At time t_0, the test begins by turning on the device under test (DUT); the drain current I_D is then allowed to ramp to the desired level, at which point the DUT is turned off. The turn-off transition is then observed at time t_1. The current is allowed to freewheel for a short time from t_1 until t_2, at which point the device is turned on again, thus yielding the turn-on transient at time t_2. The test ends when the DUT is finally switched off at time t_3, and the inductor is allowed to completely discharge through the freewheeling diode. The desired switched voltage level is set by directly adjusting Vdc, while the desired switched current level is set by varying the time between t_0 and t_1 such that the current builds to the desired level, as governed by the inductor charging equation. In order to avoid-self heating, this train of 2 pulses is repeated at distant intervals of 200 ms.



(a) (b)

Figure 2-4. Two-pulse test (a) simplified schematic and (b) fundamental waveforms.

To implement a good two-pulse test fixture requires minimization and cancellation of parasitic inductances in the power current path, as well as in the gate drive current path. Figure 2-5 is the electrical schematic of the actual test fixture constructed. On the dc voltage bus, decoupling capacitors were used to minimize the effects of parasitic inductance. High-frequency ceramic and polymer capacitors were placed as close as possible to the DUT, while low-frequency electrolytic caps were used closer to the dc source to effectively increase its bandwidth. Additionally, the positive dc bus was physically placed on the direct opposite side of the FR4 circuit board from the negative bus, thus allowing a cancellation of parasitic inductance on both the positive and negative rails. A similar strategy was employed with the gate drive circuit. Both high-frequency ceramic and low-frequency electrolytic capacitors were used on the gate drive power supply to ensure the quick response of the gate drive output. The gate drive current loop was also optimized such that the gate current output and return paths were physically paralleled, working to cancel stray inductance.

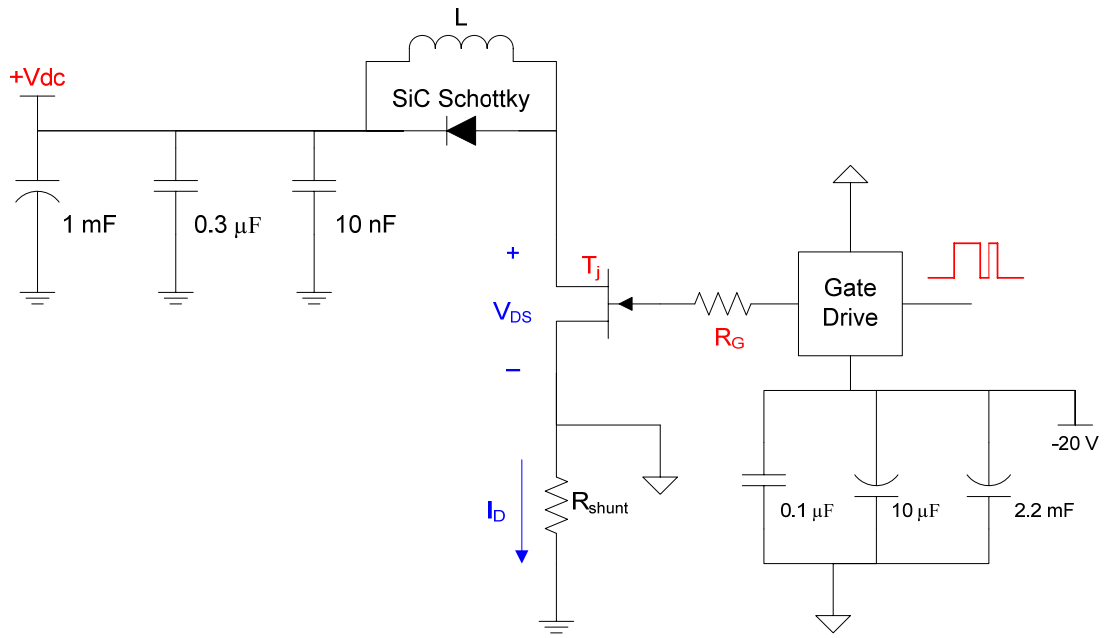


Figure 2-5. Schematic of two-pulse test fixture.

(Test variables indicated by red font; measured signals indicated by blue font.)

The test conditions were controlled by varying the dc voltage bus (V_{dc}), the gate resistance (R_G), the junction temperature (T_j), and the width of the gate command pulses. These variables are indicated in red text on the two-pulse test schematic (Fig. 2-5). The junction temperature was set by attaching the DUT to a hot plate and allowing it to soak until the entire device was at the desired temperature, as measured by thermocouples attached to either side of the device. For each combination of operating conditions, the raw data of the drain-source voltage (V_{DS}) and the drain current (I_D) waveforms was captured at both turn-on and turn-off transients (times t_2 and t_1, respectively, indicated in Fig. 2-4b). The switching energy was then calculated by numerically integrating the instantaneous power dissipation over the switching transient. The drain current was obtained by measuring the voltage across a low-inductance shunt resistor, comprised of 8 surface-mount chip resistors in parallel, each with a parasitic inductance of less than 10 nH. The two-pulse test fixture is pictured in Figs. 2-6 and 2-7; not pictured are the hot plate used to soak the SiC JFET, as well as the inductor. The freewheeling diode was a SiC Schottky barrier diode (SBD).

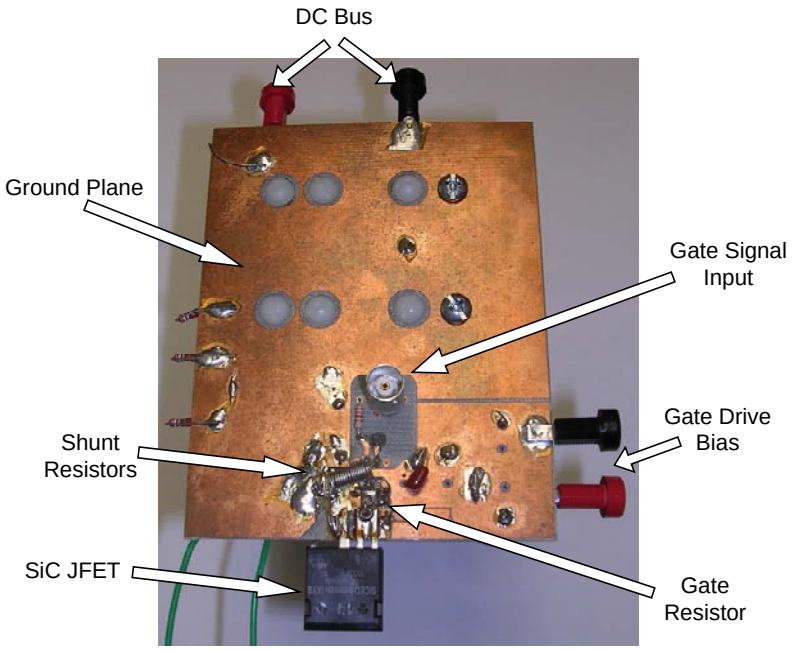


Figure 2-6. Top view of two-pulse test fixture.

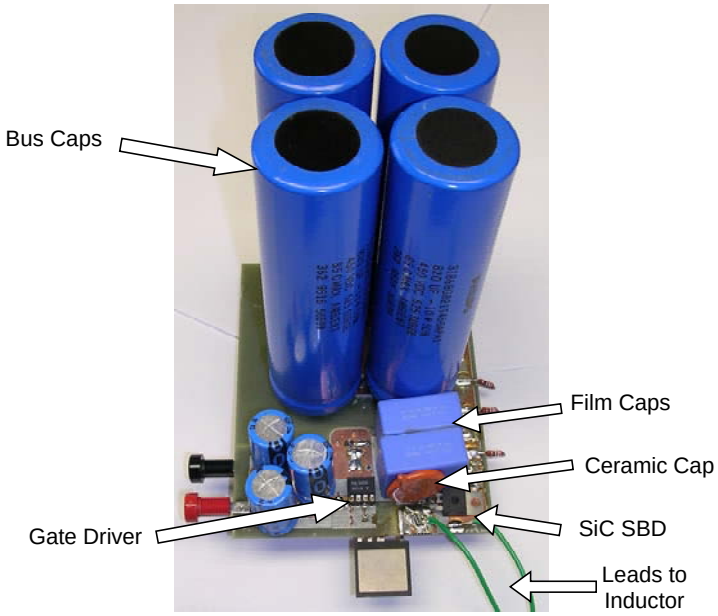


Figure 2-7. Bottom view of two-pulse test fixture.

2.3. Switching Characterization

Utilizing the test fixture described previously, the switching characteristics of the SiC JFET were measured experimentally. Table 2-1 summarizes the tested operating conditions; at each

junction temperature (T_j), all possible combinations of switched voltage (V_{dc}), switched current (I_{dc}), and gate resistance (R_G) were tested. It should be noted that although this thesis focuses on application of the SiC JFET to the dc current-type topology, the characterization results obtained from the double-pulse test are valid for dc voltage-type topologies as well. Each switching event involves the charge or discharge of the junction capacitance of a single diode, which describes commutation in both dc current-type or dc voltage-type topologies.

TABLE 2-1: SUMMARY OF TWO-PULSE TEST CONDITIONS

T_j (°C)	V_{dc} (V)	I_{dc} (A)	R_G (Ω)
25			
90	200	1	1
125	400	3	5
175	600	5	10
200			

Typical turn-on and turn-off transients are shown in Fig. 2-8 and Fig. 2-9, respectively, for a 600 Vdc bus, 5 A switched current, 5 Ω gate resistance, and operation at 125 °C junction temperature. Fig. 2-8 demonstrates the main characteristics of the SiC JFET turn-on behavior. First, the current rises very quickly, in about 10 ns here, while almost the entire dc voltage remains across the device. The voltage fall fully occurs only after the current rise. The voltage fall time is about 4 times longer than the current rise. The typical JFET turn-off behavior is shown in Fig. 2-9. Unlike for turn-on, during the turn-off transition, the voltage fall and current rise happen simultaneously. The current fall is about 1.5 times longer than the voltage rise; in this typical case, the current fall is 45 ns, while the current rise is 31 ns.

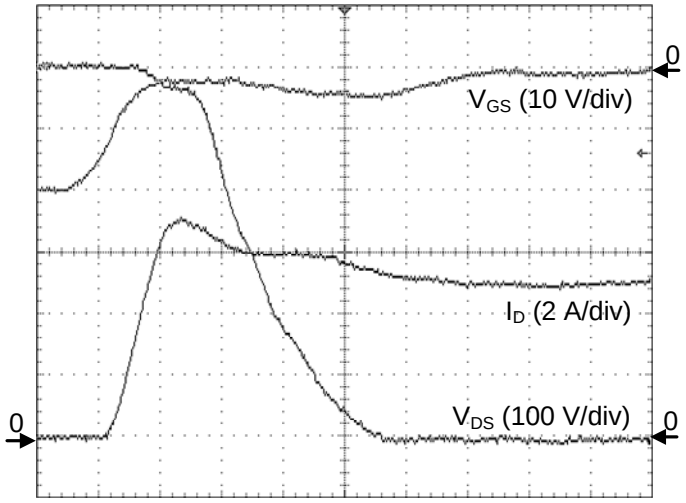


Figure 2-8. Typical turn-on waveform.
(V_{dc} = 600 V, I_{dc} = 5 A, Tj = 125 °C, R_G = 5 Ω, time: 20 ns/div)

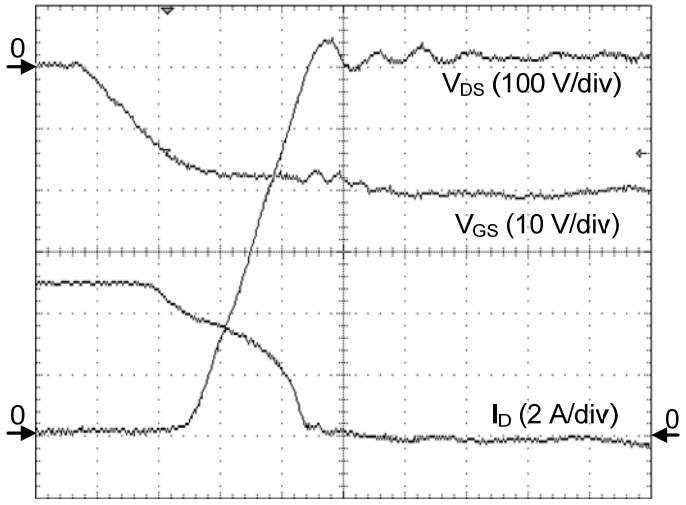
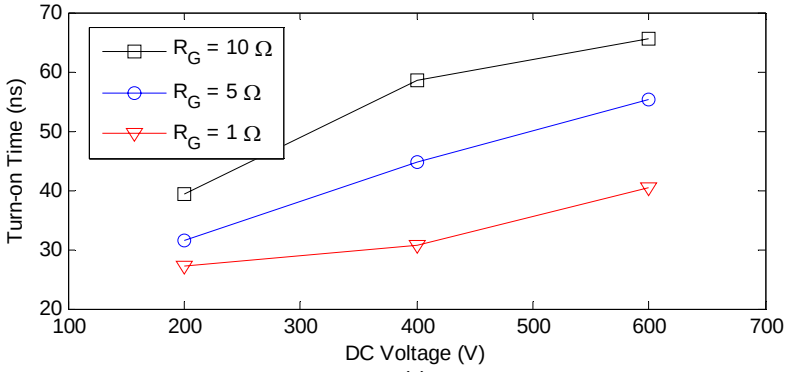


Figure 2-9. Typical turn-off waveform.
(V_{dc} = 600 V, I_{dc} = 5 A, Tj = 125 °C, R_G = 5 Ω, time: 20 ns/div)

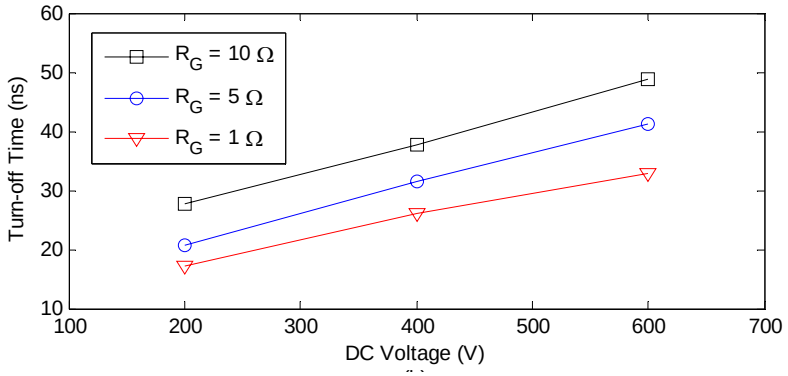
It is expected that the turn-on energy will be larger than the turn-off energy due to the overlap of peak current and voltage that occurs. Additionally, due to the sequential nature of the turn-on switching, the total turn-on time for a particular condition is longer than the corresponding turn-off time. The typical waveform also exhibits the current overshoot at turn-on due to the SiC SBD. Although the use of the SiC SBD eliminates the reverse recovery effect associated with traditional PiN diodes, the turn-on behavior is dominated by the charging of the diode junction capacitance, which causes the current overshoot.

2.3.1. Switching Speed and Current Overshoot

The SiC JFET is a fast unipolar switching device. Compared to the MOSFET, the JFET has lower junction capacitances, particularly due to the absence of a gate oxide layer, and thus a faster switching speed [5]. The small junction capacitances dominate the switching behavior; storage charge and other bipolar effects are not present [6]. Typical turn-on and turn-off times are plotted in Fig. 2-10 versus switched voltage level for 5 A switched current and varying gate resistance values. Turn-on time was defined as the time between the current rising to 5% of its dc value and the voltage falling to 5% of the dc voltage bus. Similarly, turn-off time was defined as the time from the current falling to 95% of the dc value until the voltage rises to 95% of its dc value. As expected, a direct relationship is observed between gate resistance and switching times, with the smallest gate resistance achieving the fastest switching speed.



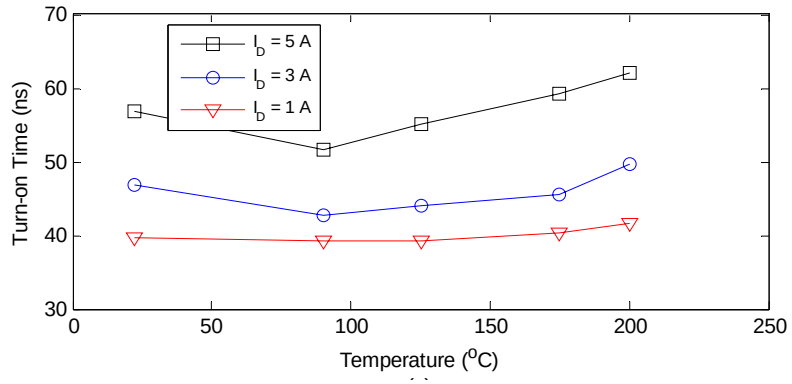
(a)



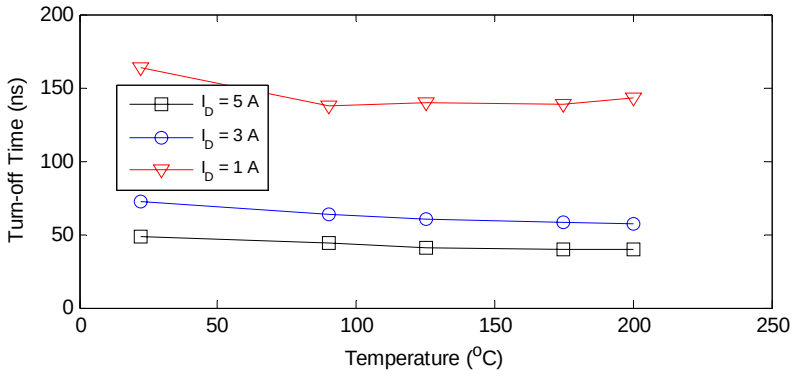
(b)

Figure 2-10. Effect of gate resistance, R_G, on (a) turn-on and (b) turn-off times as a function of dc voltage (I_D = 5 A, Tj = 125 °C).

The relationship between switching times and junction temperature is shown for different current levels in Fig. 2-11. The turn-on time is directly proportional to the switched current level—that is, a larger current requires a longer turn-on time (Fig. 2-11a). The relationship of turn-on time to junction temperature is not linear, however, as the minimum turn-on times occur just below 100 °C, and increase for both lower and higher operating temperatures. Fig. 2-11b shows that turn-off times are roughly proportional to the junction temperature, as higher temperatures produce faster turn-off times. Note, however, that the slowest turn-off times occur for a switched current of 1 A, while the fastest times are for 3 A switched current.



(a)



(b)

Figure 2-11. Effect of switched current level on (a) turn-on and (b) turn-off times as a function of junction temperature (V_{DC} = 600 V, R_G = 5 Ω).

As seen in Fig. 2-8, there is an overshoot of the drain current during the turn-on transition. This current overshoot is due to the junction capacitances of the device and the fast switching speed of the SiC JFET. Figure 2-12 plots the magnitude of the current overshoot that occurs at turn-on against the pulsed drain current value for gate resistances of 1 Ω and 10 Ω. Additionally,

the data are plotted for junction temperatures of 125 and 200 °C. From Fig. 2-12, the tradeoff between switching speed and current overshoot can be inferred. While using the 10 Ω gate resistance yields a lower current overshoot, the switching time, and hence the switching energy, will be higher than if 1 Ω gate resistance is used. Also, the current overshoot is reduced at higher junction temperature due to the increased on-resistance of the SiC at higher temperature.

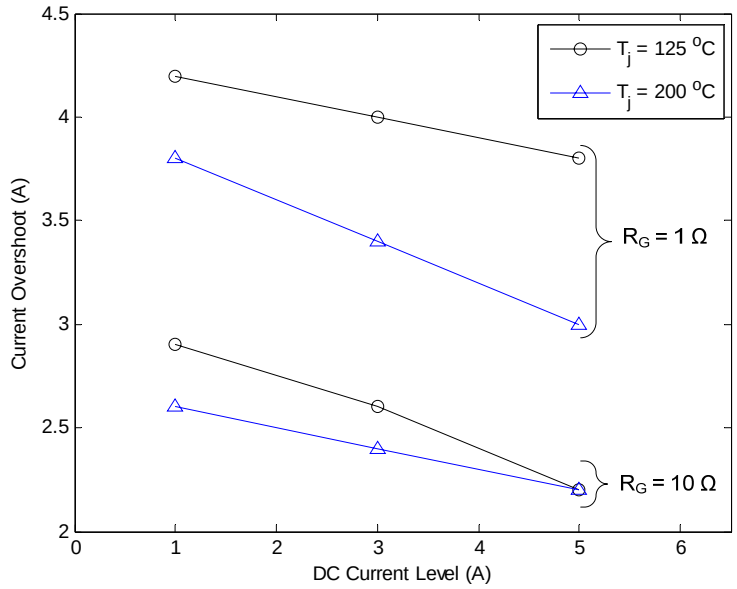


Figure 2-12. Magnitude of current overshoot at turn-on as a function of the dc current level.

2.3.2. Switching Energy

From each turn-on and turn-off waveform measured experimentally, the switching energy was calculated. The product of the voltage and current waveforms was numerically integrated through the switching transient time, resulting in the energy of the particular switching event. In Fig. 2-13, the turn-on and turn-off energies are plotted against switched voltage for various gate resistances and a fixed junction temperature of 125 °C. As expected from the switching time results of Fig. 2-10, the larger gate resistance resulted in greater switching energy due to the increased switching time. We also observe that the relationship between switching energy and switched voltage is linear, which agrees with the switching time relationship shown in Fig. 2-10. As expected due to the longer overlap of voltage and current waveforms, the turn-on energy was significantly larger than the turn-off energy for given switching condition.

The switched current level directly impacted the switching energy, as shown in Fig. 2-14. Again, this relationship appears linear with respect to both voltage and current. The turn-on

energy was affected more strongly than was the turn-off energy as switched current increases. At maximum voltage, the turn-on energy was three times larger at 5 A than at 1 A switched current, whereas the turn-off energy was only twice as large.

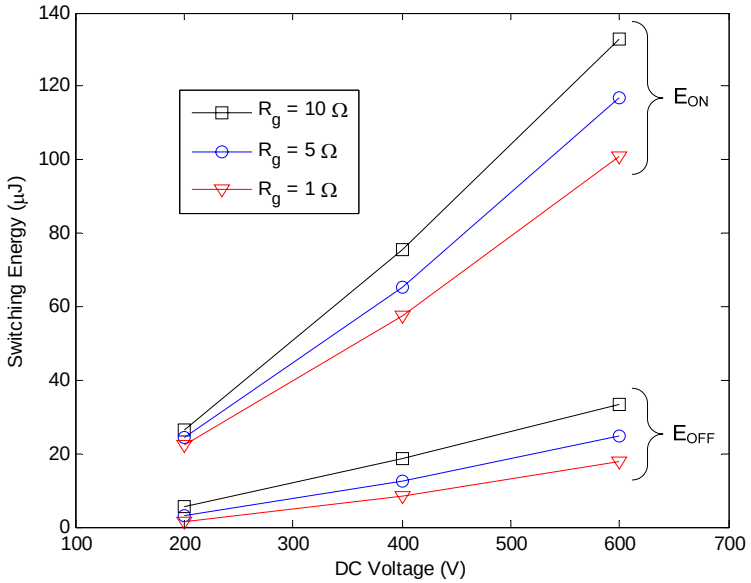


Figure 2-13. Switching energy plotted as a function of dc voltage for various gate resistance values (Tj = 125 °C, I_D = 5 A).

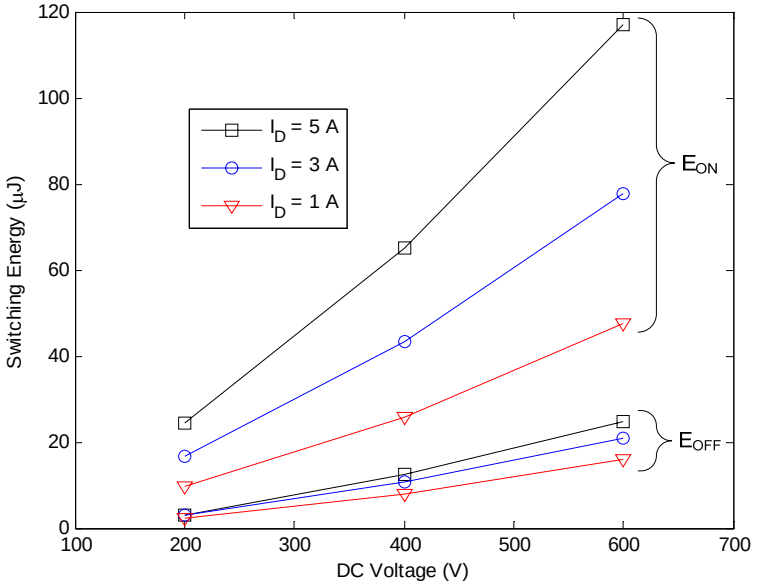


Figure 2-14. Switching energy as a function of dc voltage for varying levels of switched current (Tj = 125 °C, R_G = 5 Ω).

Fig. 2-15 shows the relationship between switching energy and temperature for different switched current levels, with a fixed voltage level of 600 V. Again, it is observed that current level had a stronger influence over turn-on energy than turn-off energy. For temperatures of 90 °C and higher, we also observe that turn-on energy dominated the total switching energy. For example, when switching 5 A, the turn-on energy was roughly 6 times greater than the turn-off energy for elevated temperatures. This is caused by two factors—namely, the current overshoot and the relatively long current-voltage overlap time at turn-on.

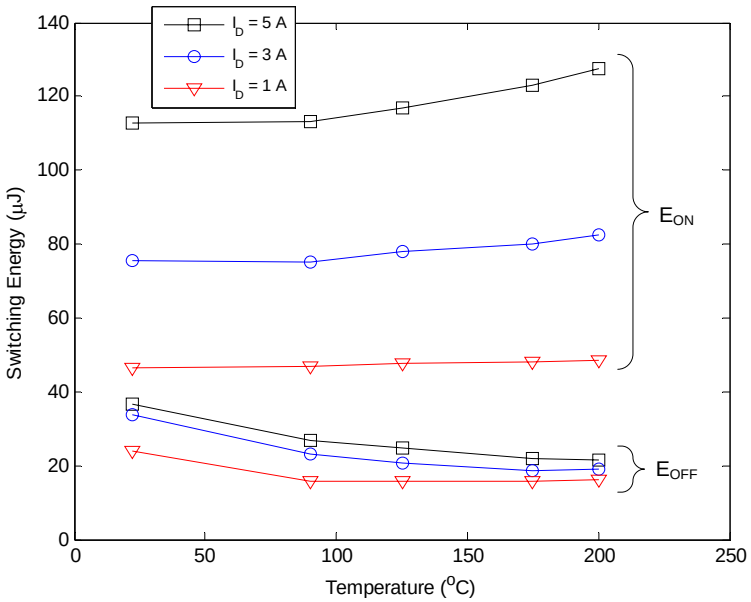


Figure 2-15. Effect of junction temperature on switching energy for varying current levels. (R_G = 5 Ω, V_{DC} = 600 V.)

2.4. Comparison to Silicon Power Switching Devices

One of the significant features of SiC devices is their capability of operating at high junction temperature without large leakage currents, especially compared to Si devices. The prototype devices tested, however, only come in standard-temperature rated packages. As such, this major advantage of SiC is not applicable unless the devices are packaged in custom high-temperature packaging. Nevertheless, the SiC JFET offers performance advantages at low temperatures compared to similarly rated Si power switching devices, as shown by Table 2-2. Both the Si IGBT and MOSFET chosen are typical examples of popular, commercially-available devices. The Si IGBT switching energies were calculated from switching energy given on the device data

sheet [16] and assuming the 1st-order approximation that switching losses are scaled linearly with voltage. Additionally, the Saber device model provided by the vendor was simulated in an ideal two-pulse test with only package parasitics and an ideal diode (results marked with an asterisk) [17]. Similarly, the switching energies of the Si MOSFET were found by simulation using the Saber device model [18]. SiC JFET switching energies were taken from the two-pulse characterization data (Appendix I).

As seen in Table 2-2, the Si MOSFET boasts switching performance comparable with the SiC JFET. The Si IGBT, however, suffers from significantly larger switching energy at both turn-on and turn-off. One of the other benefits of SiC is also apparent—low on-resistance for high blocking voltages. The SiC JFET has 5 times lower on-resistance than the Si MOSFET. Considering the forward drop of the JFET at 5 A to be 2.1 V, the JFET also has lower conduction loss than the IGBT.

TABLE 2-2: COMPARISON OF SIC JFET WITH COMMERCIALLY-AVAILABLE SI IGBT AND SI MOSFET DEVICES [16, 19]

		Si IGBT (IRG4PH20K)	**Si MOSFET (IRFPG50)**	**SiC JFET (SiCED)**
Rating		1200 V, 5 A	1000V, 6.1 A	1200 V, 5 A
Collector-Emitter Saturation Voltage (V)		3.2	–	–
On-resistance (Ω)		–	2	0.41
Switching Energy (μJ) @ 600 V, 5 A	E_{on}	234 *(153*)*	97*	113
	E_{off}	229 *(650*)*	74*	37
	E_{tot}	***463 (803*)***	***171****	***150***

***Denotes result obtained by simulated ideal two-pulse test using Saber device model provided by the device vendor.**

Note: The recommended gate resistance of 50 Ω used for Si IGBT; 5 Ω gate resistance used for Si MOSFET to simulate same gate drive circuit used for the SiC JFET.

2.5. Conclusions

While a simplified gate drive circuit was demonstrated, it was based on the fact that the SiC JFETs to be switched had a relatively uniform static gate characteristic. If the SiC JFETs being used did not have such uniformly matched characteristics, the gate voltage applied would need to be adjusted for each device. In such a case, then a gate drive circuit capable of limiting gate breakdown current regardless of the variance in device characteristics, such as the circuit presented in [20], may be more desirable.

The switching characterization results presented in this chapter showed the switching times and energies of the SiC JFET for a wide range of operating conditions, including switched voltage and current, junction temperature, and gate resistance. The operating conditions chosen cover a wide range of realistic design conditions for hard-switching converters. As such, the characterization is valuable for determining the maximum switching frequency and the switching losses of a converter design. It was shown that the SiC JFET is capable of low switching losses and fast switching speeds over a wide range of operating conditions. Although the target application is a three-phase buck rectifier in this thesis, the switching characterization is also useful for any hard-switching converter design, including three-phase voltage-type converters as well as dc-dc converters.

3. DESIGN OF THE BUCK RECTIFIER AND CHARGE CONTROLLER WITH POWER FACTOR COMPENSATION

3.1. Converter Design

3.1.1. Topology and Nominal Operating Conditions

The basic three-phase buck rectifier topology, including an additional freewheeling diode, is shown in Fig. 3-1. While the freewheeling diode is effective in reducing total conduction losses during application of the zero-state vector, it also limits the angle between input phase voltages and currents to ±30°. The freewheeling diode also serves to increase the converter's robustness, however, as it provides a path for the dc choke current regardless of commutation errors. Additionally, the converter may be disabled by simply commanding all switches to remain off instead of requiring application of zero-state for a period until the inductor can discharge; the dc current will freewheel and dissipate through the freewheeling diode.

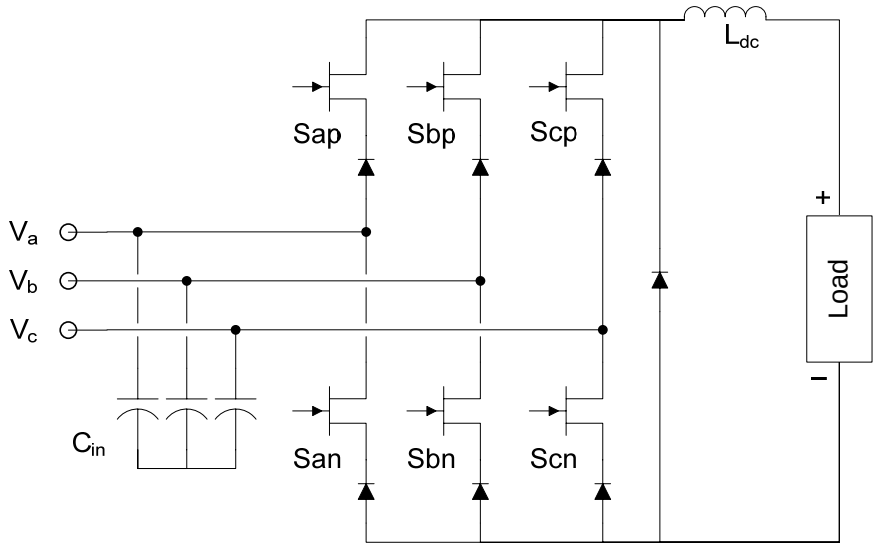


Figure 3-1. Basic three-phase buck rectifier topology.

In Table 3-1, the design specification for the SiC buck rectifier is given. Considering the SiC JFETs are known to be safely rated to 5 A, this is chosen as the dc output current rating. The load resistance is 8 Ω, providing a maximum 2 kW output power. The three-phase ac input is specified by the potential target application for the converter, which is a three-phase converter in

a more-electric aircraft. Because of the presence of the input capacitors (C_{in}), the converter has an inherently leading, low power factor. In order to meet the specification of high power factor, phase compensation of the input currents was necessary. Temperature specifications were chosen such that the devices should operate safely within the limits of the standard packaging technology used by the TO-220 packaged SiC JFETs and SBDs. As there are no limits on output ripple, the dc choke was sized to allow 20% output current ripple at nominal load; the choke inductance used was 500 µH. For improved common-mode noise performance, the dc-choke should be implemented as two 250 µH inductors, one each on the positive and negative dc rails.

TABLE 3-1: SIC BUCK RECTIFIER DESIGN SPECIFICATIONS

Rated Power	2 kVA
Ac Input (3-phase)	230 $V_{l\text{-}n,rms}$ 400 – 800 Hz
Dc Load	5 A
Input Current THD	< 5%
Input Power Factor	> 0.95 @ 400 Hz
Input Capacitance	Line-to-neutral < 2.5 µF per kVA
Ambient Temperature	25 to 70 °C
Device Junction Temperature	< 175 °C
Switching Frequency	150 kHz

The modulation index, M, of the converter is defined by (3.1), where I_m is the peak value of the fundamental of the input PWM phase current and I_{dc} is the average dc current. The voltage gain of the converter is also expressed in terms of the modulation index, as given by (3.2). Here, V_{dc} is the dc voltage, V_m is the peak line-to-line voltage, and θ is the phase angle between the input phase current and phase voltage.

$$M = \frac{I_m}{I_{dc}} \tag{3.1}$$

$$V_{dc} = \frac{\sqrt{3}}{2} \cdot M \cdot V_m \cdot \cos\theta \tag{3.2}$$

Rearranging (3.2) to solve for M as a function of dc and line voltages yields (3.3). Considering that the input capacitance causes a leading power factor, the converter should be operated with the power stage input phase currents lagging the phase voltages. The modulation index is then plotted against input current phase angle from 0 to 30° for the nominal input phase voltage and output dc voltage level, as given in Table 3-1.

$$M = \frac{2}{\sqrt{3}} \cdot \frac{V_{dc}}{V_m \cdot \cos\theta} \tag{3.3}$$

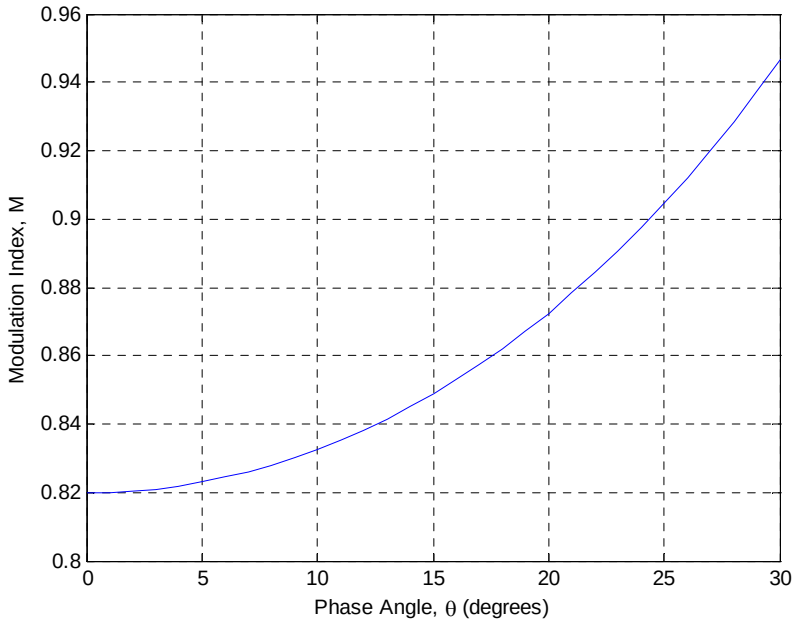


Figure 3-2. Modulation index as a function of phase angle between input voltage and current for nominal converter operating conditions.

3.1.2. Power Stage and Thermal Design

3.1.2.1. Devices

The SiC JFETs used for the converter are single JFETs packaged in a TO-220 case, which utilize the same size JFET die as those in the cascode package (2.4 mm x 2.4 mm). These JFETs were obtained after the cascode-packaged devices were characterized (Chapter 2), and are used here because the cascode device is not necessary. The TO-220 package is thus more convenient

to use and has less package parasitics. Though the cascode-packaged JFET was characterized in Chapter 2 of this thesis, the TO-220 packaged devices are expected to have similar characteristics given that the same technology was used to fabricate both device die; furthermore, the SiC JFET die are the same size for both packages. As mentioned in Chapter 1.3.2.2 of this work, the TO-220 packaged devices were fabricated with a different range of pinch-off voltages than that of the cascode packaged samples tested. Table 3-2 summarizes the static characteristics of the TO-220 packaged JFETs, including pinch-off voltage, on-resistance, and drain-source breakdown voltage. It should be noted that the prototypes received were from two fabrication lots, one with a target pinch-off voltage of -19 V and another with target pinch-off of -22 V.

TABLE 3-2: SUMMARY OF STATIC CHARACTERISTICS PROVIDED WITH TO-220 PACKAGED SIC JFET PROTOTYPES

	Min.	**Typ.**	Max.	Unit
Pinch-off	18.2	**22.3**	24.6	- V
Drain-Source Breakdown	1240	**1310**	1544	V
On-resistance	0.31	**0.35**	0.36	Ω

The diodes used were also prototype devices provided by Infineon. These SiC Schottky-barrier diodes (SBDs) are rated at 1200 V and 15 A. The forward drop of these diodes at 5 A is fairly independent of junction temperature, and is typically 1.2 V.

3.1.2.2. Gate Drive Modules

Due to the fact that the TO-220 JFETs have a wider range of pinch-off voltages than did the cascode-packaged devices, the gate drive as used for device characterization in Chapter 2 cannot be used here without modification. One option was to adjust the gate voltage individually for each JFET; the gate voltage required must be of large enough negative magnitude to pinch off the device, but not so large as to drive the gate-source junction into breakdown. This choice, however, was not a practical or robust solution. Instead, the gate driver was modified to incorporate an R-C-D network in the gate drive path [3], as shown in Fig. 3-3. Then, the gate drive supply voltage was increased to a value larger than the largest pinch-off voltage; in this design, -28 V was chosen. The R-C-D network limits the gate current such that the device cannot be driven into the gate breakdown. When the gate voltage is applied during the off-state, the

10 nF capacitor charges to the difference between the device gate breakdown voltage and the applied voltage, preventing continual operation in the gate breakdown region.

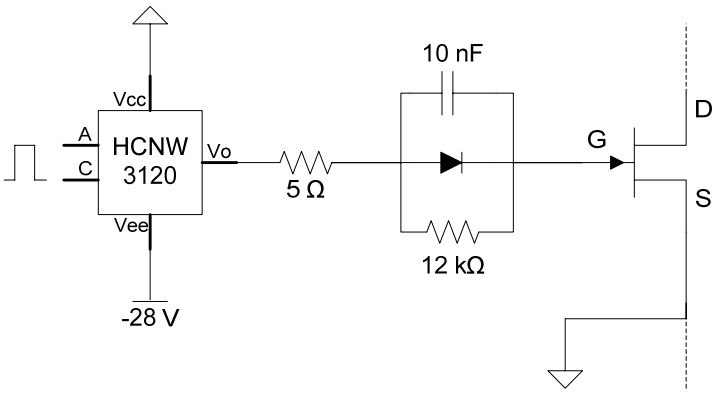


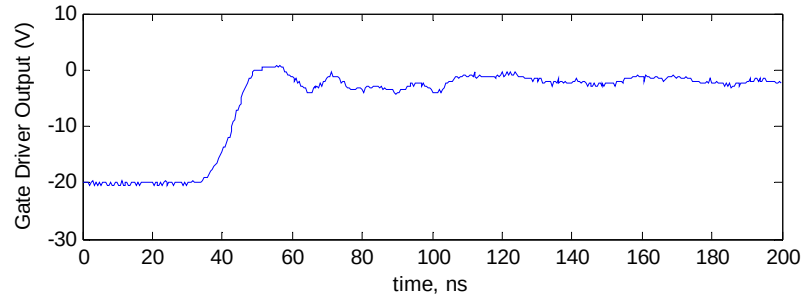
Figure 3-3. Gate drive used in SiC buck rectifier.

Each gate drive was fabricated as a modular unit facilitating easy replacement and interchangeability. In addition to the gate drive circuit, each gate drive module included an isolated dc-dc converter so that the modules may all be fed from a single supply. The required power rating for the isolated converters was determined by averaging the total gate drive energy over the switching period. Figures 3-4 and 3-5 plot the gate drive output voltage and gate current over the turn-on and turn-off transients, respectively. The gate drive energy, E_{drv}, was calculated by (3.4) for both turn-on and turn-off transients. Next, the gate drive energy was averaged over the switching period, resulting in the average power dissipation of the gate drive ($P_{drv,tot}$) as shown by (3.5) and (3.6). The isolated converter chosen was the CC1R5-2412-DF-E manufactured by TDK, which has an adjustable output voltage up to 30 V with a 1.5 W power rating.

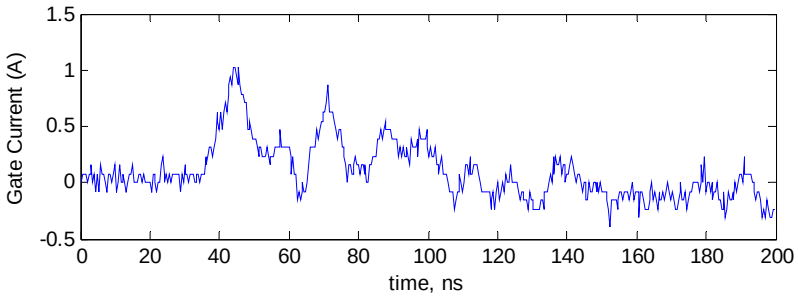
$$E_{drv} = \int (V_O \cdot I_G) dt \tag{3.4}$$

$$P_{drv,tot} = \left(E_{drv,turn-on} + E_{drv,turn-off}\right) \cdot f_s \tag{3.5}$$

$$P_{drv,tot} = (1.0\,\mu J + 0.97\,\mu J) \cdot 150\,kHz = 296\,mW \tag{3.6}$$

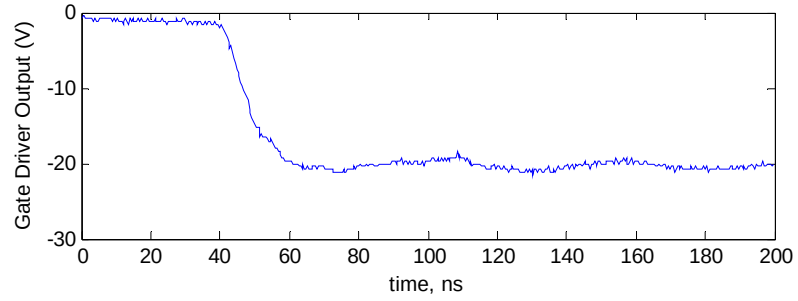


(a)

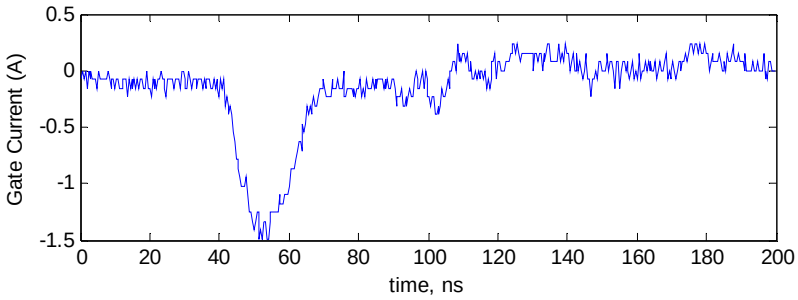


(b)

Figure 3-4 Gate drive voltage (a) and current (b) during turn-on for switching 400 V and 5 A.



(a)



(b)

Figure 3-5 Gate drive voltage (a) and current (b) during turn-off for switching 400 V and 5 A.

3.1.2.3. Semiconductor Loss Calculations

For the conduction losses of the buck rectifier, the calculation is straightforward. First the freewheeling diode was neglected in order to find the general form of the conduction losses. Then, the equations were modified to account for the freewheeling diode. The modulation rule of the buck rectifier is such that at any given time, the dc current must have a path through one of the top-rail switches and one of the bottom-rail switches. This means that at all times, 2 JFETs must be conducting and 2 series diodes must be conducting; the total conduction losses for all JFETs and diodes may be then be written as (3.8) and (3.8), respectively. Here, I_{dc} is the average dc current, $R_{DS,on}$ is the JFET on-resistance, and V_f is the diode forward voltage. Relevant values ($R_{DS,on}$, V_f) are a function of the device operating conditions (current, temperature, etc.).

$$P_{cond,JFET,tot} = 2 \cdot I_{dc}^2 \cdot R_{DS,on} \tag{3.7}$$

$$P_{cond,D,tot} = 2 \cdot I_{dc} \cdot V_f \tag{3.8}$$

Then, considering that the freewheeling diode provides a lower impedance path for the current during the application of the zero vector, the switches and diodes only conduct during application of the active vectors. The result is that the losses are scaled by a factor of the modulation index, M, as shown in (3.9) and (3.10). The freewheeling diode then conducts the full dc current during zero vector, and its loss, $P_{cond,FWD}$, may be expressed as (3.11).

$$P_{cond,JFET,tot} = 2 \cdot M \cdot I_{dc}^2 \cdot R_{DS,on} \tag{3.9}$$

$$P_{cond,D,tot} = 2 \cdot M \cdot I_{dc} \cdot V_f \tag{3.10}$$

$$P_{cond,FWD} = (1 - M) \cdot I_{dc} \cdot V_f \tag{3.11}$$

Because the conduction losses are distributed evenly among all 6 switches and main diodes, (3.9) and (3.10) were divided by 6, yielding the expressions for conduction loss of a single JFET (3.12) and diode (3.13).

$$P_{cond,JFET} = \frac{1}{3} \cdot M \cdot I_{dc}^2 \cdot R_{DS,on} \tag{3.12}$$

$$P_{cond,D} = \frac{1}{3} \cdot M \cdot I_{dc} \cdot V_f \tag{3.13}$$

It has thus been shown that the conduction losses for the buck rectifier are dependent on the modulation index M, which is dependent on the phase angle θ of the input currents. The

conduction losses for each device were then calculated for the nominal operating conditions. For the SiC SBD, the forward voltage at 5 A is 1.2 V; the JFET on-resistance is 0.74 Ω at the junction temperature of 175 °C. Conduction losses for the single JFET, single SBD, and the freewheeling diode are plotted against power stage input phase angle in Fig. 3-6.

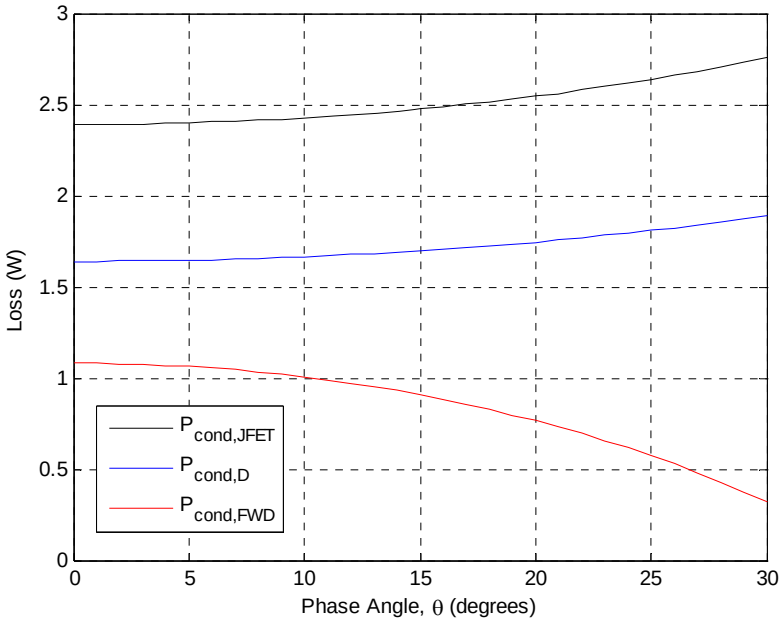


Figure 3-6. Conduction losses as a function of input current phase angle for nominal operating conditions.

The switching losses for the buck rectifier are also dependent on the modulation pattern [21]. As will be shown later, the charge control scheme results in a pattern where in a given switching period, the 2 active vectors are applied sequentially, followed by the zero vector. For this pattern, the total switching loss for the converter has been derived in [21]. The total converter switching losses are expressed as given in (3.14), where $E_{on,JFET}$ is the JFET turn-on energy, $E_{off,JFET}$ is the JFET turn-off energy, and $E_{rr,D}$ is the diode reverse recovery energy. The values used for the switching energies are for the conditions of switching current at the value I_{ref}, and switching voltage V_{ref}. Assuming the energies are linear with respect to switched voltage and current to a 1st-order approximation, they are scaled by the converters actual dc current, I_{dc}, and peak line-to-line voltage, V_m.

$$P_{SW,JFET,tot} = f_S \cdot \frac{3}{\pi} \cdot \left(E_{ON,JFET} + E_{OFF,JFET} + E_{rr,D}\right) \cdot \frac{I_{dc}}{I_{ref}} \cdot \frac{V_m}{V_{ref}} \qquad (3.14)$$

For the specific case of the SiC buck rectifier, SiC SBDs are used; as such, the reverse recovery energy is considered to be zero. Again, considering that the total switching losses are distributed evenly among all switches, the switching loss for each JFET ($P_{SW,JFET}$) is given by (3.15).

$$P_{SW,JFET} = \frac{1}{2\pi} \cdot f_S \cdot \left(E_{ON} + E_{OFF}\right) \cdot \frac{I_{dc}}{I_{ref}} \cdot \frac{V_m}{V_{ref}} \tag{3.15}$$

The switching loss is thus independent of the converter's modulation index, and may be calculated by reading the switching energy values from Fig. 2-15 for the nominal junction temperature of 175 °C. From the plot, the energies were read at V_{ref} of 600 V and I_{ref} of 5 A; the turn-on energy is 123 µJ and the turn off energy is 21.9 µJ. Given the nominal switching frequency of 150 kHz, the switching losses of a single JFET are expressed in (3.16).

$$P_{SW,JFET} = \frac{1}{2\pi} \cdot 150\,kHz \cdot \left(123\,\mu J + 21.9\,\mu J\right) \cdot \frac{5\,A}{5\,A} \cdot \frac{563.4}{600} = 3.25\,W \tag{3.16}$$

From Fig. 3-6 and using (3.16), the worst-case ($\theta = 30°$) total loss of a single JFET is 6.0 W. The series diode loss is 1.9 W for the same condition, while the freewheeling diode loss is 0.32 W. The total semiconductor losses (6 switches, 6 series diodes, 1 freewheeling diode) for the nominal switching frequency are plotted against the power stage input current phase angle in Fig. 3-7.

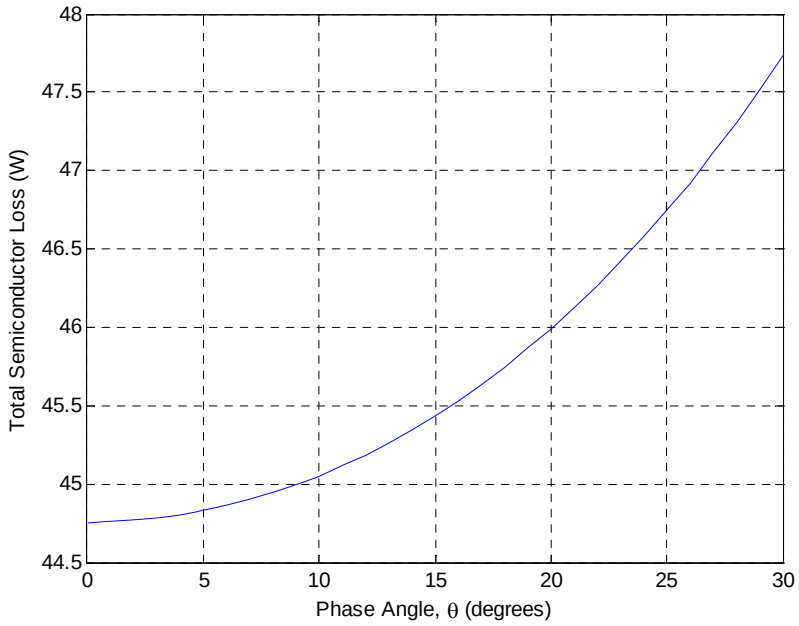
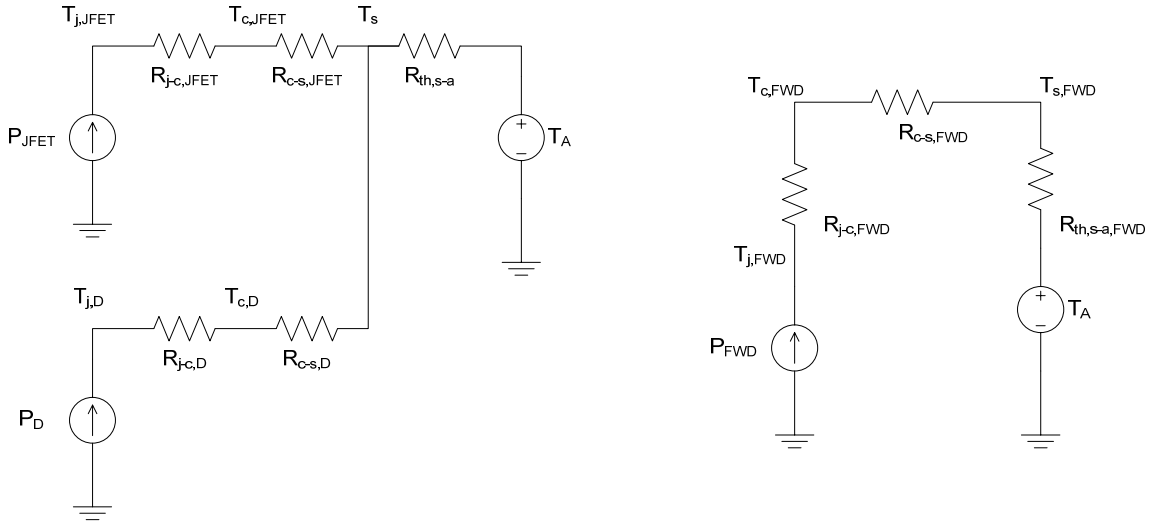


Figure 3-7. Total semiconductor loss as a function of input current phase angle.

3.1.2.4. Thermal Design

The basic rule of the thermal design was to limit the device junction temperature to the specified limit (175 °C) for the specified maximum ambient temperature (70 °C). A single heat sink was used for each SiC JFET and SBD pair, while the freewheeling diode had its own small heat sink. The steady-state equivalent thermal networks for both cases are shown in Fig. 3-8; subscript JFET indicates the SiC JFETs, D indicates the main diodes, and FWD indicates the freewheeling diode. The variable names are as follows:

P	:	Semiconductor loss for a single device
T_j	:	Junction temperature
T_c	:	Case temperature
T_s	:	Heat sink temperature
T_A	:	Ambient temperature
$R_{j\text{-}c}$	:	Junction-to-case thermal resistance
$R_{c\text{-}s}$	:	Case-to-heat sink thermal resistance
$R_{th,s\text{-}a}$	:	Heat sink-to-ambient thermal resistance



(a) (b)

Figure 3-8. Steady-state equivalent thermal network for (a) a SiC JFET and SBD pair mounted on a single heat sink and (b) the freewheeling diode.

The JFET and main diode junction temperatures are expressed as (3.17) and (3.18) by solution of the steady-state equivalent thermal network shown in Fig. 3-8(a). As the losses of the

JFET are greater than the main diode, its junction temperature will be higher; as such, the solution for the maximum thermal resistance of the heat sink ($R_{th,s\text{-}a}$) was derived from (3.17), resulting in (3.19). Given the typical JFET junction-to-case resistance of 0.24 °C/W, and assuming the case-to-heat sink resistance of 0.95 °C/W (electrical isolation and gap pad used were Bergquist 1500 material with 0.02" thickness), the limit of the heat sink thermal resistance was calculated by (3.20).

$$T_{j,JFET} = T_A + \left(P_{JFET} + P_D\right) \cdot R_{th,s-a} + P_{JFET} \cdot \left(R_{j-c,JFET} + R_{c-s,JFET}\right) \tag{3.17}$$

$$T_{j,D} = T_A + \left(P_{JFET} + P_D\right) \cdot R_{th,s-a} + P_D \cdot \left(R_{j-c,D} + R_{c-s,D}\right) \tag{3.18}$$

$$R_{th,s-a} \le \frac{T_{j,JFET} - T_A - P_{JFET} \cdot \left(R_{j-c,JFET} + R_{c-s,JFET}\right)}{P_{JFET} + P_D} \tag{3.19}$$

$$R_{th,s-a} \le \frac{175^o C - 70^o C - 6.0W \cdot \left(0.24 + 0.95\right)^o C/W}{6W + 1.9W} = 12.4\ ^o C/W \tag{3.20}$$

In a similar manner, the heat sink thermal resistance for the freewheeling diode was calculated. The thermal network of Fig. 3-8(b) was solved directly for $R_{th,s\text{-}a,FWD}$, yielding (3.21). The maximum thermal resistance was then given in (3.22).

$$R_{th,s-a,FWD} = \frac{T_{j,FWD} - T_A}{P_{FWD}} - R_{j-c,FWD} - R_{c-s,FWD} \tag{3.21}$$

$$R_{th,s-a,FWD} \le \frac{175^o C - 70^o C}{0.32\ ^o C/W} - 0.24^o C/W - 0.95^o C/W = 327\ ^o C/W \tag{3.22}$$

The heat sink chosen for SiC JFET and SBD pair is Aavid Thermalloy #531302, which has a thermal resistance of 8.0 °C/W at minimal airflow (100 ft./min.). The heat sink choice exceeds specification (3.20), thus allowing a safety margin. In the case of the freewheeling diode, the calculated heat sink thermal resistance limit in (3.22) was so large that a heat sink was not required. Nevertheless, a small TO-220 heat sink was used for the freewheeling diode to ensure that specification was met.

Using the thermal impedance of the chosen heat sink for the SiC JFET and SBD pair, the temperature rises from ambient to junction of the SiC JFET ($\Delta T_{j\text{-}a,JFET}$) and ambient to heat sink of the JFET-SBD pair ($\Delta T_{j\text{-}a}$) are plotted in Fig. 3-9 as a function of power stage input current phase angle.

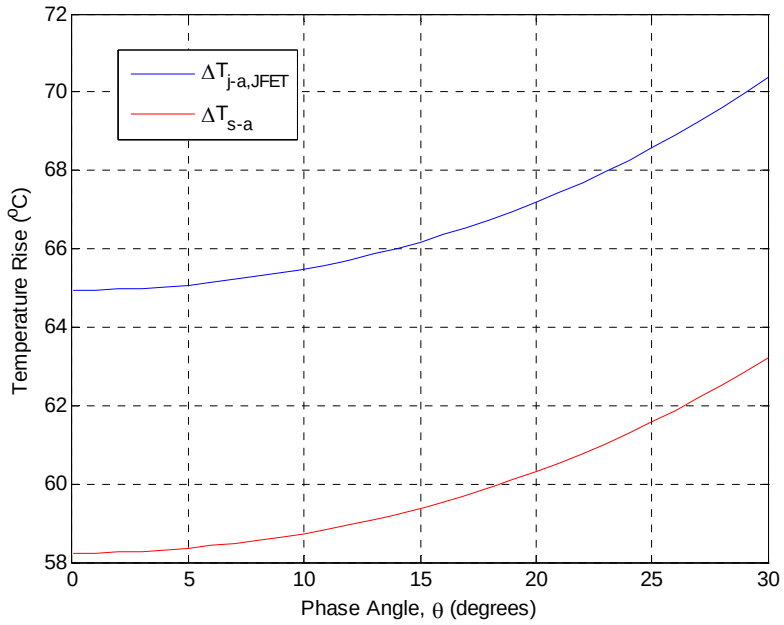


Figure 3-9. Temperature rise for minimal airflow as a function of input current phase angle.

3.1.3. Input Filter Design

The input filter is designed to meet high-frequency EMI specifications for the target application in a more-electric aircraft, as well as the maximum input capacitance specification from Table 3-1. Though the filter design was not the concern of this thesis, the general idea of the design process is shown for completeness.

In Fig. 3-10, the input phase current spectrum of the buck rectifier is shown from simulation. As can be seen, the dc-side inductor value has little effect on the input current. Because the EMI limits start at 150 kHz, the switching frequency was chosen to actually be slightly lower, such that the noise at the switching frequency does not require attenuation. As expected, the largest component of the input current is at the input line frequency, while the second largest components are around the switching frequency. The 2nd harmonic of the switching frequency requires the most attenuation in order to comply with the specification. A closer view of the region of interest is shown in Fig. 3-11; the current spectrum is shown before and after the filter is added, and compared with the narrowband EMI limit.

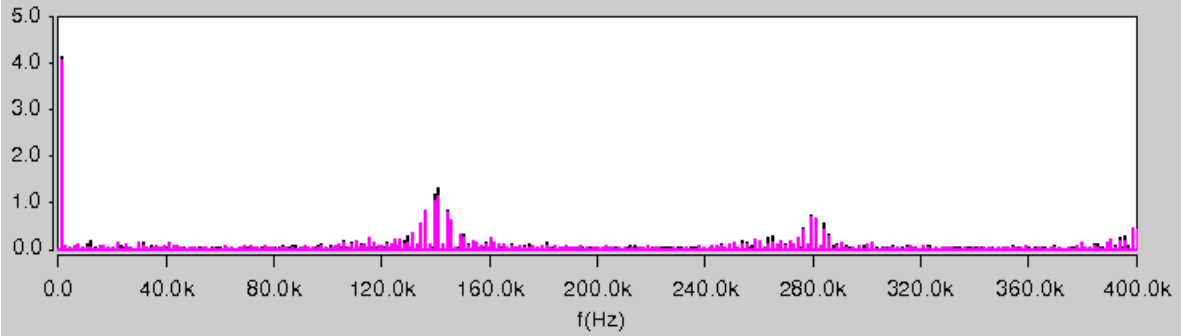


Figure 3-10. Buck rectifier input current spectrum for infinite load inductance (purple) and for 0.25 mH load inductance (black). (Y-axis is current magnitude in A; line frequency 800 Hz.)

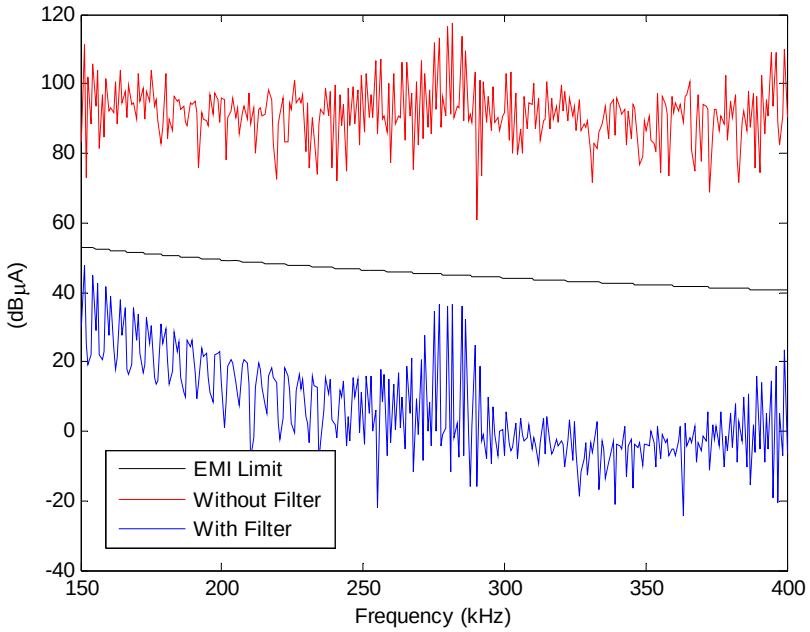


Figure 3-11. Input current spectrum in range of concern for EMI limits.

The topology for the input filter is a 4th order cascaded LC-LC filter (Fig. 3-12). In order to attenuate the 2nd harmonic of the switching frequency (greater than 75 dBμA attenuation), the corner frequency of the filter must be 34.9 kHz. This corner frequency is more than an order of magnitude higher than the maximum line frequency, so there should be no oscillation caused by the line fundamental frequency assuming there are also no small-signal impedance interactions. The inductance and capacitance were chosen such that both stages utilize the same LC values; additionally, some damping resistance is used in series with both L_1 and C_1. The final filter component choice is shown in Table 3-3.

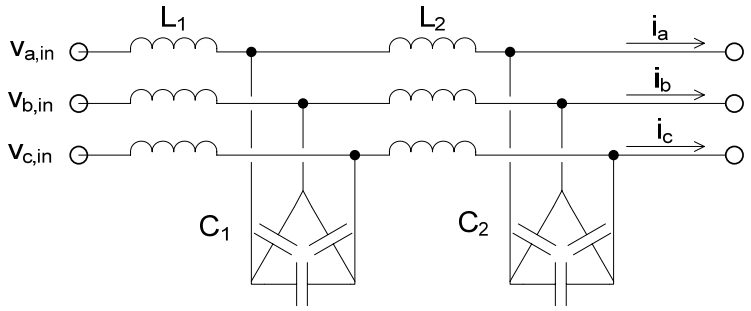


Figure 3-12. Input filter for a single phase.

TABLE 3-3: INDUCTOR AND CAPACITOR USED FOR INPUT FILTER

	Description	Value	Type
L_1, L_2	Ac filter inductors	52.1 μH	Custom FINEMET FT-3M toroid core, 6 cm ID, 5 cm OD, 0.5 cm thickness
C_1, C_2	Ac filter capacitors	0.33 μF	Cornell Dubilier 940C16P33K-F, 1600 V, poly film
R_{L1}	Damping resistance in series with first-stage inductors	1 Ω	TO-220 resistor, 35 W
R_{C1}	Damping resistance in series with first-stage capacitors	4.7 Ω	Metal film, 3 W

3.2. Implementation of Charge Control with Phase Angle Compensation

3.2.1. Overview of Charge Control Method for the Three-Phase Buck Rectifier

The controller for the SiC buck rectifier is based on the charge-control method that was first adapted to the three-phase ac buck rectifier in [15]. As initially demonstrated, the control method forces the input phase currents to be aligned with the phase voltages. First, a brief overview of the original charge control method is given. Then, the next section discusses the extension of the charge control method to allow for phase angle compensation of the input phase currents, and details the specific controller implementation realized in hardware.

The basic charge control method for the three-phase buck rectifier needs only to sense the input phase voltages (v_a, v_b, v_c) and the switch current (I_{SW}), measured at the points indicated by the power stage schematic in Fig. 3-13. In Fig. 3-14, the block diagram of the charge controller is shown. The control voltage, V_{con}, may be given directly by a reference voltage for open-loop

voltage operation, or a compensator can be added with feedback from the converter output voltage, V_{dc}, to provide closed-loop voltage control.

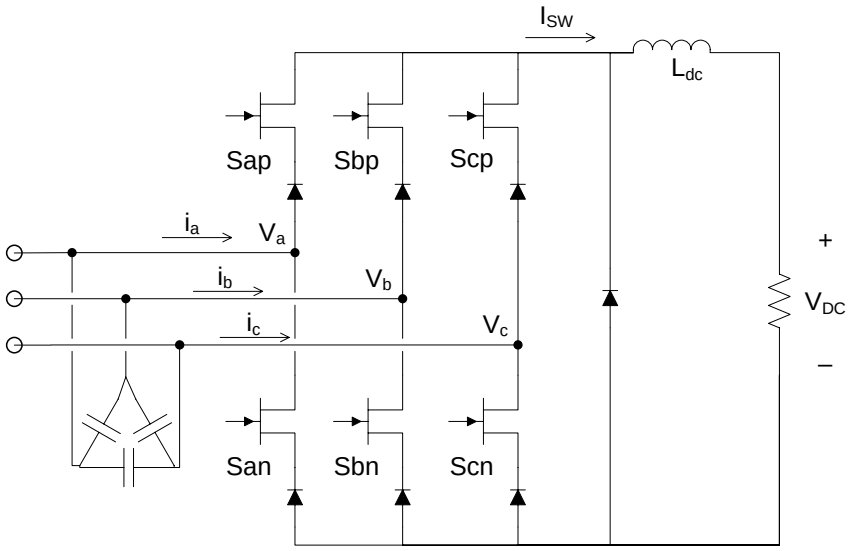


Figure 3-13. Buck rectifier power stage indicating signals relevant to the charge control method.

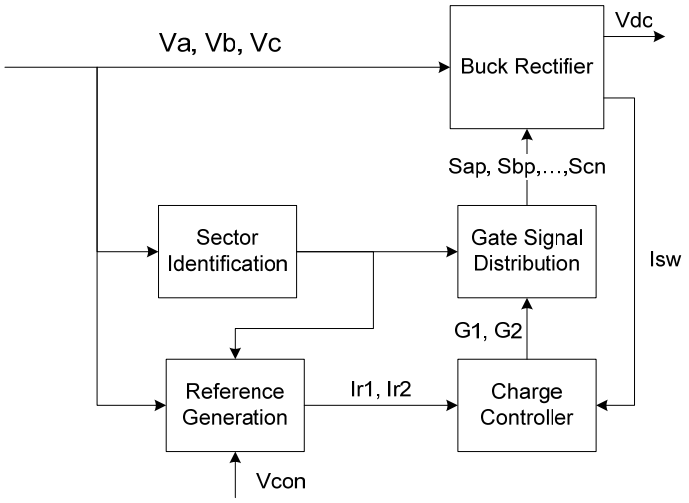


Figure 3-14. Block diagram of original charge control method.

The basic operating principle of the charge control is that the input phase currents (i_a, i_b, i_c) are shaped by a reference generated from the phase voltages. The control scheme achieves this by sensing only the switch current, which at any instant is equivalent to the phase currents of the active switches. First, the input phase voltages are sensed and passed to both the *Sector Identification* and *Reference Generation* blocks. The *Sector Identification* block not only

determines which 60° line sector that the input voltages are in, but also identifies whether the phase voltages are in the first half (0-30°) or second half (30-60°) of the active sector. The *Reference Generation* function is to generate 2 reference levels from the sensed phase voltages using the sector information; the control voltage (V_{con}) is the gain that directly scales both references. Using the generated references (I_{r1}, I_{r2}) and the sensed switch current (I_{SW}), the *Charge Controller* generates the switching pulses for the 2 active vectors and the zero vector. It does this by integrating the switch current during each switching period; the gate signal G_1 for the first active vector is applied until the integrator reaches the first reference, I_{r1}. At this point, the second vector is applied (gate signal G_2) until the integrator reaches I_{r2}. Then, the integrator is reset and the zero vector is applied for the remainder of the switching period. Finally, the *Gate Signal Distribution* block distributes the gating signals $_{G1}$, $_{G2}$, and zero vector to the appropriate switches based on the input line sector.

3.2.2. Implementation and Functional Description of the Controller

In order to compensate for the leading power factor introduced by the input capacitance, it is necessary to lag the phase currents at the power stage input with respect to the phase voltages. Because the charge control method synthesizes the input phase currents according to references generated from sensing the input phase voltage, it is thus necessary to apply a phase shift to these references. The modified charge control block diagram is shown in Fig. 3-15; a *Phase Compensation* block has been added. Furthermore, the logic of the *Charge Controller* block is changed in order to correctly apply the desired switching vectors, even when a phase shift is introduced. The controller operation and implementation are described block-by-block in the following sections. The complete circuit schematics of the controller implementation are shown in Appendix II.

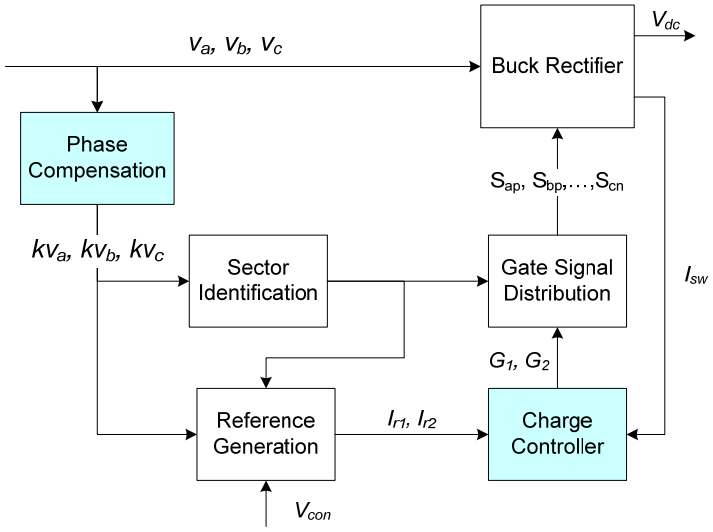


Figure 3-15. Block diagram of charge control method with phase angle compensation.

3.2.2.1. Implementation of Logic Functions

Several of the blocks of Fig. 3-15 require the implementation of logic functions. Instead of using individual logic gates in the respective blocks, all logic functions are implemented in a complex programmable logic device (CPLD). The CPLD chosen is the Xilinx XC9572XL in a socketed PC44 package. Main features of the device include 5 ns pin-to-pin logic delay, 1,600 usable logic gates in 72 macrocells, and 34 assignable I/O pins. The control scheme implemented requires 21 I/O pins, and the VHDL code (Appendix III-A) requires the use of 30% of the CPLD resources. There is a single high-speed 555 timer circuit generating the switching frequency clock. The CPLD input and output signals are shown in Fig. 3-16.

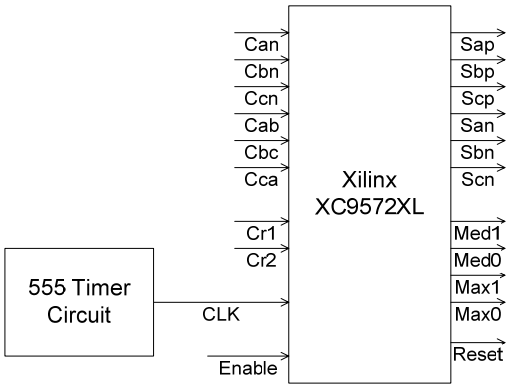


Figure 3-16. I/O signals of logic device and connection of timer circuit.

3.2.2.2. Phase Compensation

As the controller references are generated from the input phase voltages, the voltage signals must be sensed, scaled, conditioned, and phase shifted. Fig. 3-17 shows the signal diagram for a single input phase; this function is duplicated for each input phase voltage. First, the phase voltages are sensed using a LEM LV 25-P voltage sensor. Next, the voltages are scaled and filtered by a low-pass Butterworth filter to eliminate any high frequency noise. Finally, the phase shift is applied by a unity-gain phase delay circuit. The phase delay is designed to be adjustable with maximum achievable phase shift of 30° for 800 Hz line frequency. As the phase delay is fairly linear in this range, for any given setting, the phase shift of a 400 Hz signal is always half that of an 800 Hz signal.

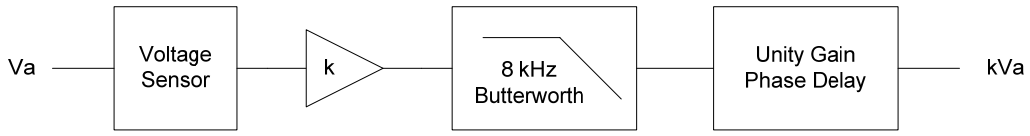


Figure 3-17. Phase compensation schematic for a single phase.

3.2.2.3. Sector Identification

In the original charge control method, the *Sector Identification* block detected the sector of the input phase voltages, to which the input currents were aligned. Now that a phase shift has been added in front of the *Sector Identification* function, the function of the *Sector Identification* block is to identify the sector of the desired input current. The 60° sectors and 30° sub-sectors of the three-phase reference signals are labeled in Fig. 3-18. The sensed, conditioned, and phase shifted voltage signals *kVa*, *kVb*, and *kVc* are fed to comparators as shown in Fig. 3-19, and the resulting signals are sent to the CPLD to implement the logic function described by Table 3-4.

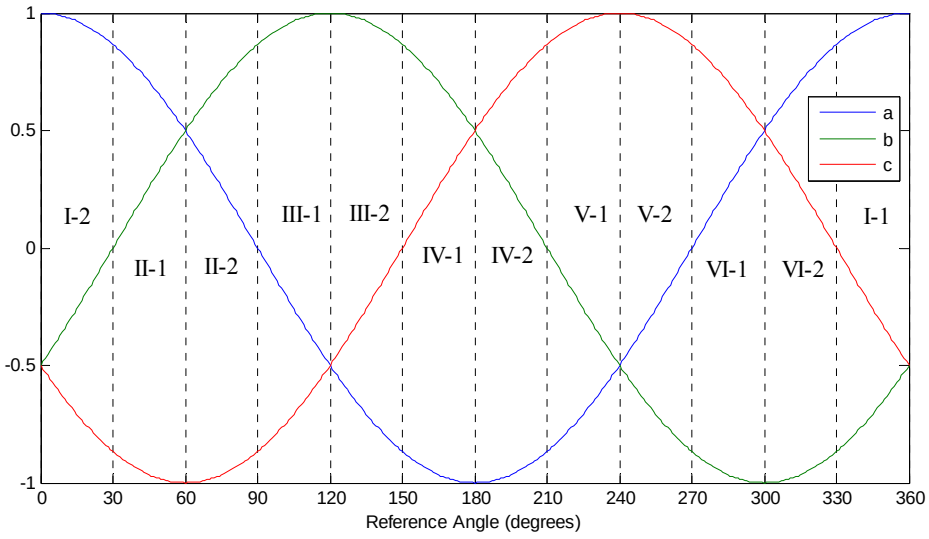


Figure 3-18. Three-phase reference sectors and sub-sectors.

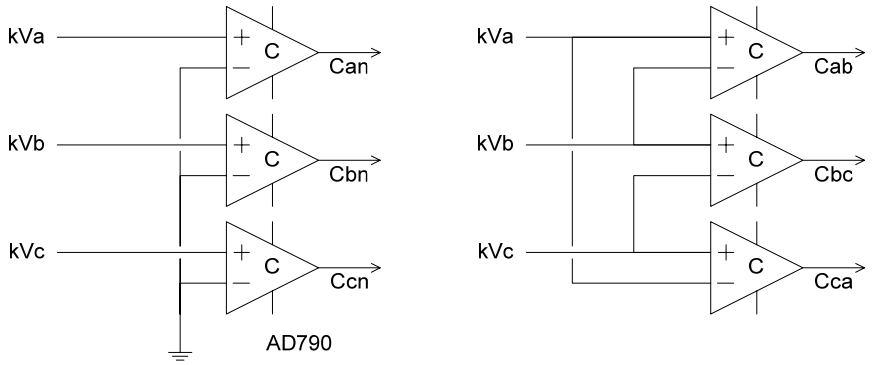


Figure 3-19. Comparator arrangement used for the sector identification function.

TABLE 3-4: SECTOR IDENTIFICATION TRUTH TABLE

Sector	Can	Cbn	Ccn	Cab	Cbc	Cca	$y_3y_2y_1y_0$
I-1	1			1			0000
I-2	1			1	1		0001
II-1	1	1		1	1		0010
II-2	1	1			1		0011
III-1		1			1		0100
III-2		1			1	1	0101
IV-1		1	1		1	1	0110
IV-2		1	1			1	0111
V-1			1			1	1000
V-2			1	1		1	1001
VI-1	1		1	1		1	1010
VI-2	1		1	1			1011

3.2.2.4. Reference Generation

The charge controller references must now be synthesized from the conditioned and phase-shifted three-phase signals *kVa*, *kVb*, and *kVc*. The first step is to take the absolute value of each signal; this is done using an analog precision absolute value circuit for each phase, as shown in Fig. 3-20. Next, the absolute values are selected to generate the charge control references *Ir1* and *Ir2*. The reference signal *Ir2* is synthesized by always selecting the maximum of signals |*kVa*|, |*kVb*|, and |*kVc*|; *Ir1* is generated by selecting the signal with the middle magnitude. The signals Med1, Med0, Max1, and Max0 are generated in the CPLD according to the truth table (Table 3-5) and select the appropriate signals to pass through the analog multiplexer. The absolute value of the three-phase reference signals and the synthesized charge controller references are shown in Fig. 3-22.

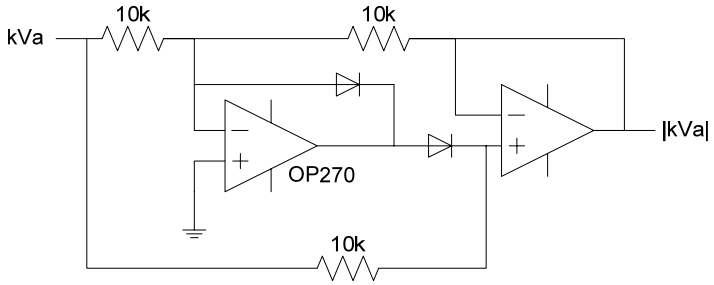


Figure 3-20. Absolute value circuit for a single phase.

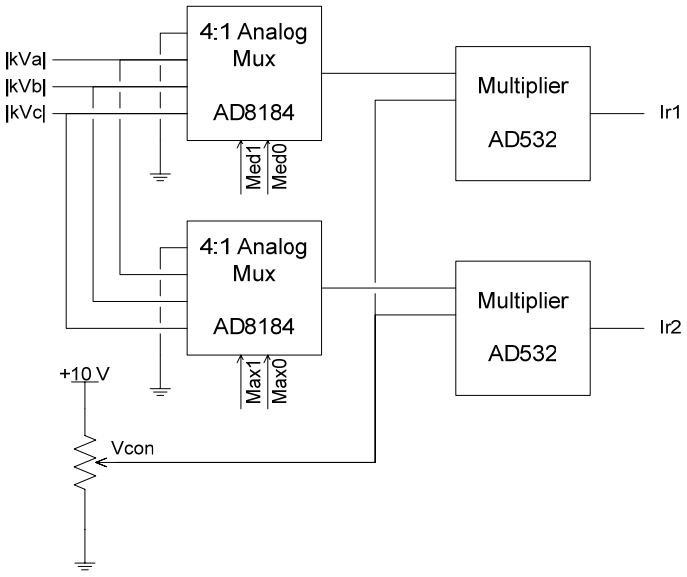


Figure 3-21. Reference generation circuit.

TABLE 3-5: REFERENCE GENERATION TRUTH TABLE

Sector	$y_3y_2y_1y_0$	Med1	Med0	Max1	Max0
I-1	0000	1			1
I-2	0001	1	1		1
II-1	0010		1	1	1
II-2	0011	1		1	1
III-1	0100	1	1	1	
III-2	0101		1	1	
IV-1	0110	1			1
IV-2	0111	1	1		1
V-1	1000		1	1	1
V-2	1001	1		1	1
VI-1	1010	1	1	1	
VI-2	1011		1	1	

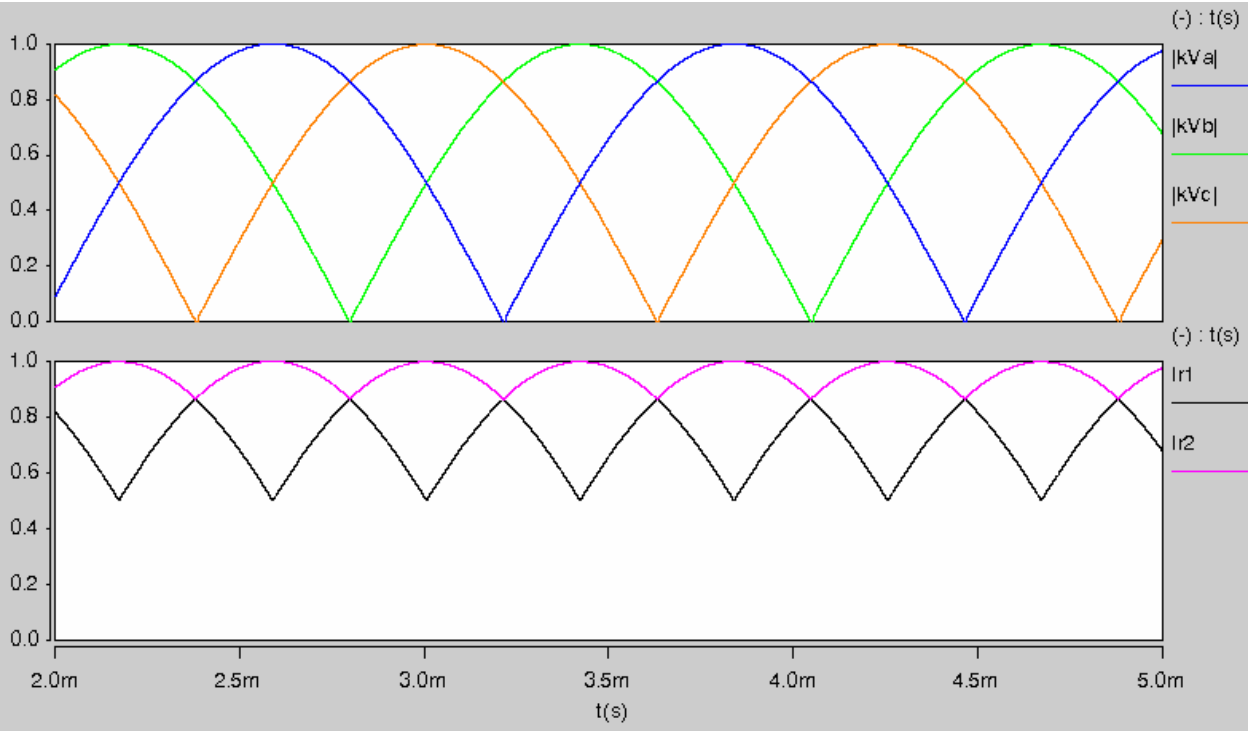


Figure 3-22. Absolute value of three-phase reference signals and synthesized charge controller references (*Ir1* and *Ir2*).

3.2.2.5. Charge Controller

The charge controller as pictured in Fig. 3-23 consists of a resettable integrator, 2 comparators, and a logic function implemented in the CPLD. For the implementation of the resettable integrator, an integrating capacitor (*Cint*) and a small MOSFET are used. The

MOSFET is turned on to allow the discharge of *Cint*, thereby resetting the integrator. The switch current (*Isw*) is sensed using a high-frequency current transformer with a 50-turn secondary side. The diode in the current sensing circuit is critical, as it allows the current transformer to reset itself when the integrator is reset.

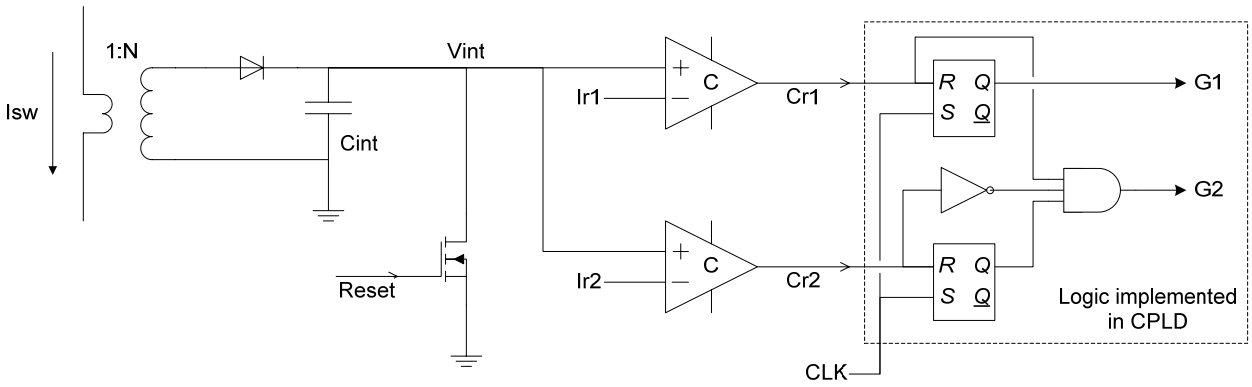


Figure 3-23. Modified charge controller circuit including logic function implemented in the CPLD.

The operation of the charge controller is shown in Fig. 3-24. At the beginning of the switching period, the gating signal *G1* for the first switching vector is applied. The switch current integrates until *Vint* reaches the level of *Ir1*, at which point *G1* is turned off and *G2* is applied. It should be noted that this differs from the original charge control concept [15]; there, both *G1* and *G2* are applied at the beginning of each switching period. The assumption is that the vector applied by *G1* is of larger magnitude; therefore, it will conduct and prevent the second vector from being applied until *G1* is turned off. This assumption is valid if there is no phase angle compensation applied. As soon as the input phase currents are not aligned with the phase voltages, this assumption will be wrong near the beginning and end of each sector. The modification is necessary in order to apply *G1* and *G2* sequentially, regardless of the magnitude of each corresponding vector. Finally, when *Vint* reaches *Ir2*, *G2* is turned off, and zero vector is applied for the remainder of the switching period.

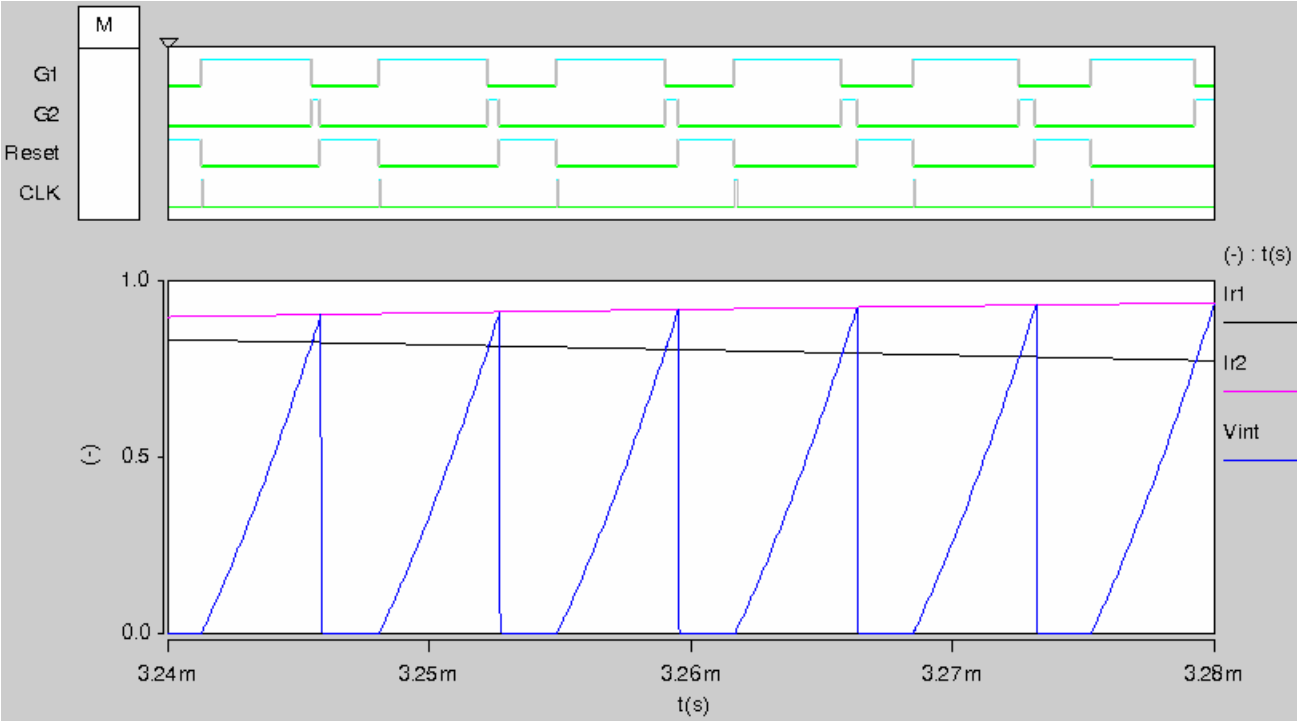


Figure 3-24. Charge controller operation and gating signals.

The integrating capacitor *Cint* is sized such that the integrator voltage is limited to a chosen maximum value within each switching period [15]. The equation for sizing the integrating capacitor is rewritten in (3.23) in terms of the notation of design variables in this work. In (3.23), P_o is the rated output power of the converter and N is the number of secondary-side turns on the current transformer. All other variables have been introduced previously.

$$C_{\text{int}} \geq \frac{2}{\sqrt{3}} \cdot \frac{P_o}{V_{\text{int}}^{\max} N f_S V_m \cos\theta} \tag{3.23}$$

The integrating capacitor is solved for at the nominal design conditions and the worst-case phase angle θ in (3.24). The integrating capacitor is realized in the actual controller circuit with a 200 nF capacitor.

$$C_{\text{int}} \geq \frac{2}{\sqrt{3}} \cdot \frac{2\,kW}{(5V)(50)(150\,kHz)(563.4V)\cos 30^o} = 126\,nF \tag{3.24}$$

3.2.2.6. Gate Signal Distribution

The modulation scheme of the buck rectifier is such that during any given switching period, one switch on either the top or bottom dc rail will be turned on for both active vectors, with the vector being selected by turning on the opposing phases on the opposite dc rail. For example, in sector III-2, switch *Sbp* will be turned on for both active vectors. Then *San* is turned on to apply the first switching vector, and *Scn* is turned on to apply the second switching vector. In Table 3-6, the switch that should be turned on is indicated (listed in the 'ON' column), as are the switches that should receive the gating commands *G1* and *G2*, depending on which sector the input phase currents are in. Again, the distribution logic is implemented in the CPLD. An example of the operation of the gate signal distribution logic is shown in Fig. 3-25.

TABLE 3-6: GATE SIGNAL DISTRIBUTION

Sector	$y_3y_2y_1y_0$	ON	G1	G2
I-1	0000	Sap	Sbn	Scn
I-2	0001	Sap	Scn	Sbn
II-1	0010	Scn	Sap	Sbp
II-2	0011	Scn	Sbp	Sap
III-1	0100	Sbp	Scn	San
III-2	0101	Sbp	San	Scn
IV-1	0110	San	Sbp	Scp
IV-2	0111	San	Scp	Sbp
V-1	1000	Scp	San	Sbn
V-2	1001	Scp	Sbn	San
VI-1	1010	Sbn	Scp	Sap
VI-2	1011	Sbn	Sap	Scp

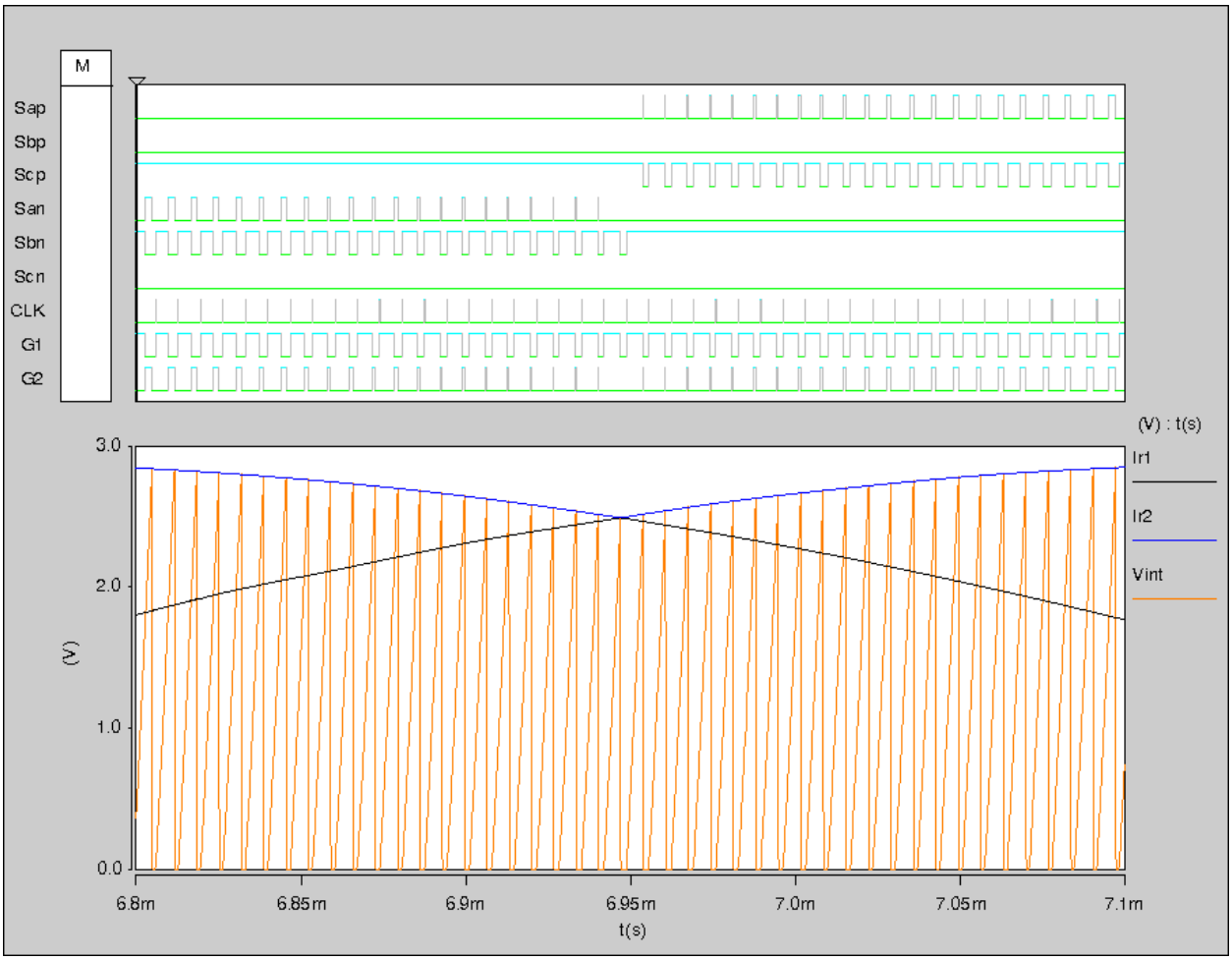


Figure 3-25. Example of gate signal distribution.

3.3. Simulation of Controller and Converter System

3.3.1. Simulated System

The entire converter and controller system was simulated using Saber. All of the analog signal conditioning circuits were implemented with op-amp networks to verify desired operation for final design. All op-amps, analog multiplexers, and multipliers were simulated with their respective bandwidth and slew rate parameters. The logic functions programmed in the CPLD were implemented using a combination of logic gates, flip-flops, and truth tables to simulate the functional operation of the CPLD.

The power stage was simulated as is shown in Fig. 3-26. Ideal switch and diode models were used in order to simulate the basic behavior of the converter. The simulated input filter also

includes the series damping resistances. The equivalent series resistance (ESR) of each passive component was also modeled. An ideal three-phase voltage source was used. During testing of the actual hardware, it became necessary to add a small output capacitance of 1 μF in order to stabilize oscillation on the output voltage V_{dc} due to parasitics of the resistive load bank used. The output capacitor was included in this simulation model.

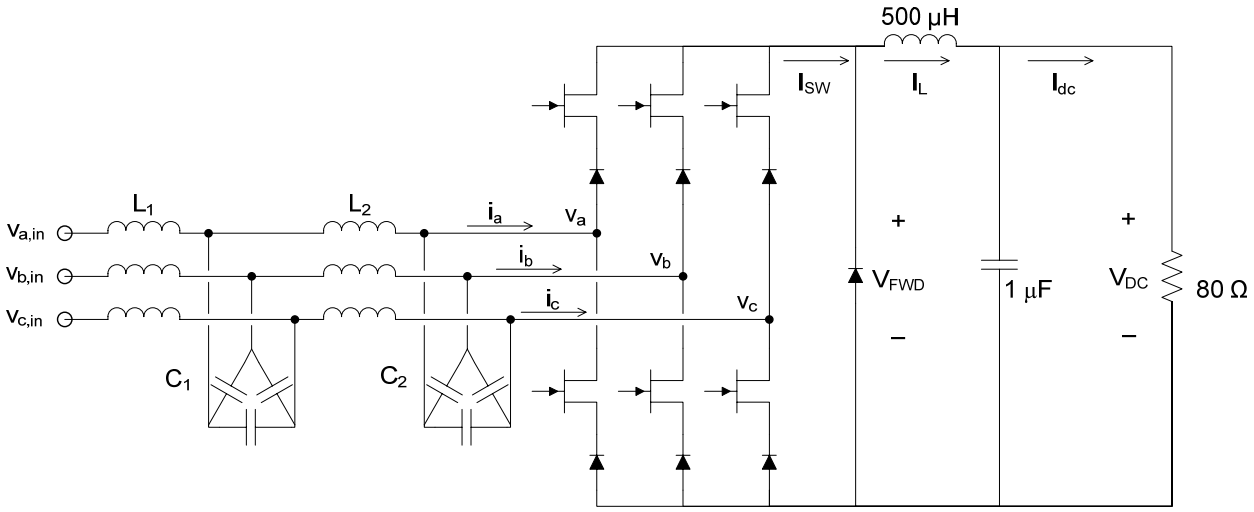


Figure 3-26. Power stage of the buck rectifier as simulated.

3.3.2. Simulation at 400 Hz Line Frequency

The gain of the converter was set by selecting the control voltage V_{con} to a constant value such that the output power is 2 kW, and the controller is tuned to provide a 10° lag of the phase currents (labeled i_a, i_b, i_c in Fig. 3-26) at the power stage terminals. The load voltage and current, Fig. 3-27, is shown to be 400 V and 5 A by simulation. The three-phase input phase (line-to-neutral) voltages and phase currents are shown in Fig. 3-28; though the input power is determined to be 2.118 kW from this simulation, the semiconductor losses (particularly switching losses) are not modeled correctly in simulation. For this reason, the only useful losses that can be determined from the simulation are the input filter losses. The total semiconductor losses for 10° phase angle are given as 45.05 W from Fig. 3-7. From simulation, the total filter losses are measured as 33.7 W. This yields a combined loss of 78.75 W for a theoretical efficiency of 96.2%.

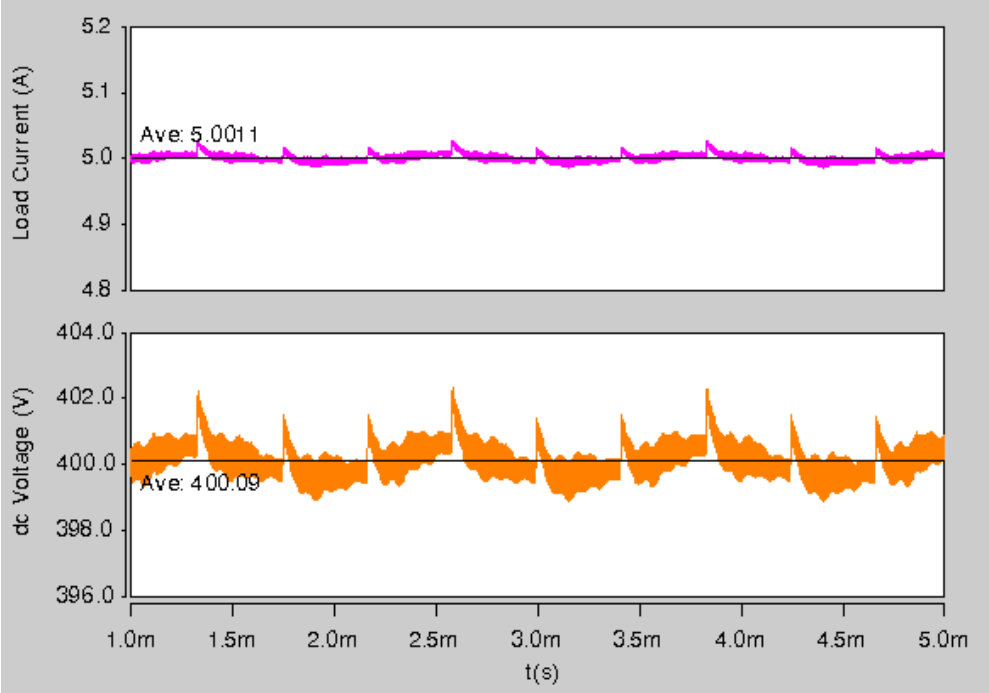


Figure 3-27. Load current and voltage for 400 Hz line frequency.

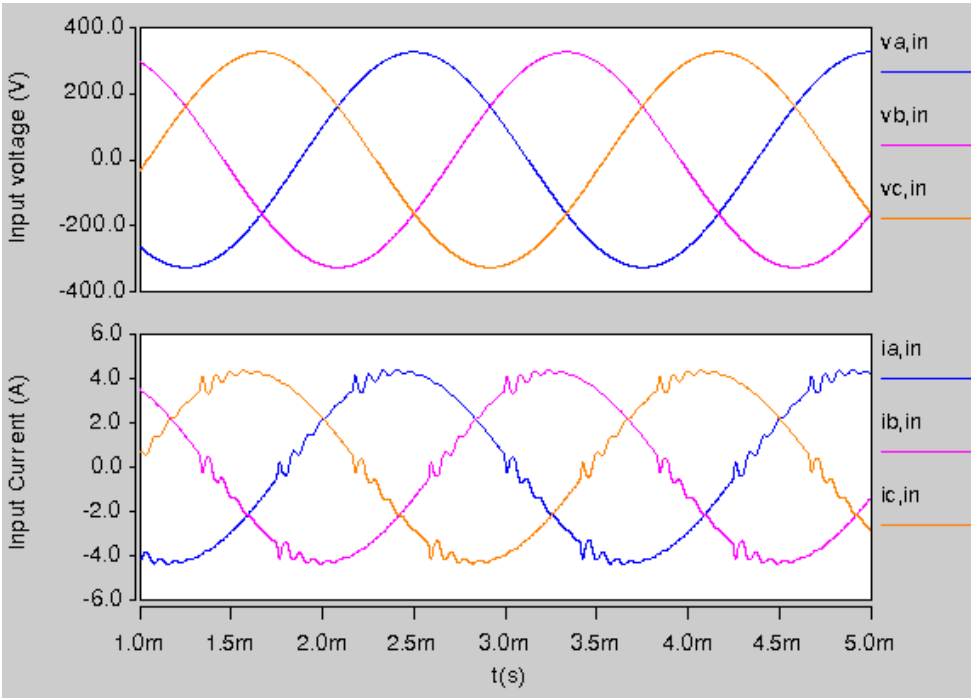


Figure 3-28. Three-phase input line-to-neutral voltages and phase currents at 400 Hz; voltage is 230 V_{rms} and current is 3.07 A_{rms}.

Ringing of the input phase currents is observed in Fig. 3-28 to occur 6 times over a single line period. The ringing is due to the way in which the charge controller generates its integrator references and distributes the gating signals; specifically, the gating pattern changes half-way through the input sector. So the ringing occurs in the middle of each sector instead of at the transition from one sector to another. In the second-stage inductor current, the ringing is less pronounced than in the input current, as can be seen in Fig. 3-29.

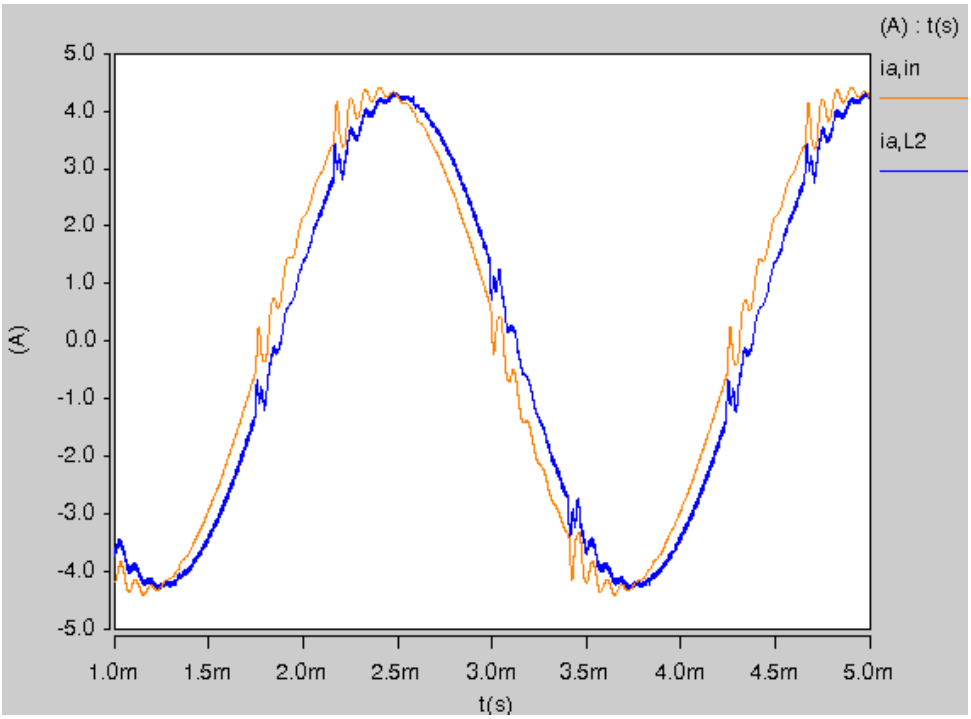


Figure 3-29. Comparison of input current ($i_{a,in}$) and second-stage inductor current ($i_{a,L2}$) for operation at 400 Hz.

The ringing is evidently due to the discontinuity of the gating pattern exciting the input filter. The simulated input current THD is 4.67%. Although the THD meets the design specification, it is not attractive given the high switching frequency of 150 kHz; such a fast switching converter is expected to achieve much lower THD. It is undesirable to reduce the THD by merely increasing the size of the input filter, as this would only mask the problem inherent with the charge control method. An improvement has been made to the charge control scheme that eliminates the transient that excites the input filter ringing. The improved charge control method is discussed in detail and demonstrated by simulation later in this chapter, section 3.4.

Figure 3-30 shows that the input phase current and voltage are nearly in phase. The current is leading the voltage by 8.77°, corresponding to a leading power factor 0.988. Including the simulated filter losses and the calculated semiconductor losses, the input apparent power is 2.02 kVA.

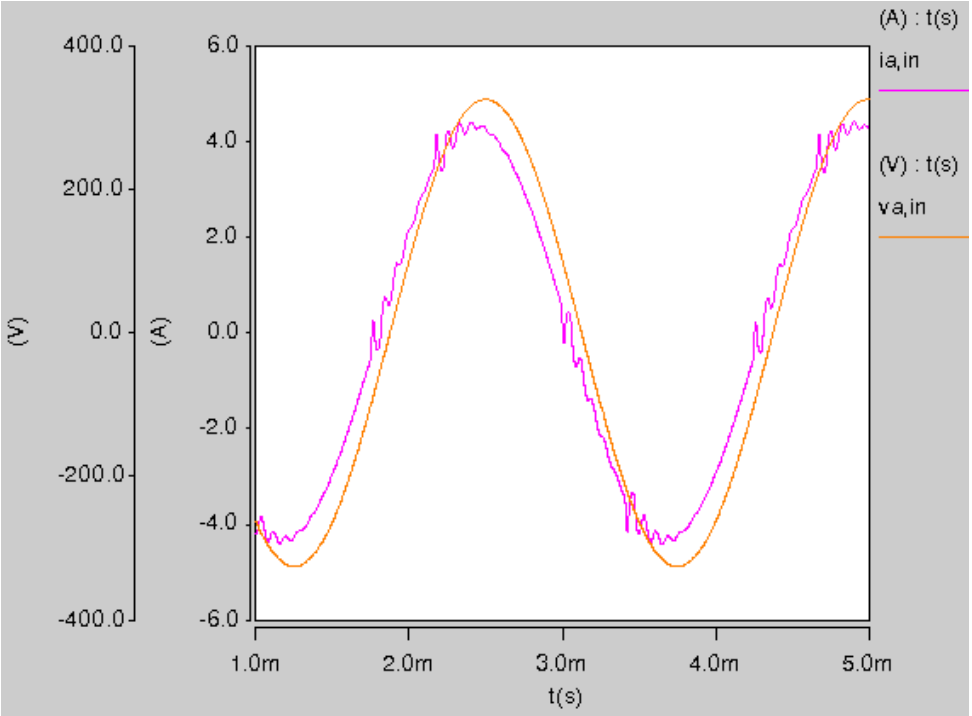


Figure 3-30. Input phase voltage and current for operation at 400 Hz line frequency.

To determine the gain M that the converter was working at, (3.1) was calculated as shown in (3.25). From (3.2), the theoretical output voltage was calculated in (3.26). The theoretical output voltage is 2.75% higher than the simulated output voltage, however, the calculation does not consider conduction losses.

$$M = \frac{I_m}{I_{dc}} = \frac{4.34\,A}{5\,A} = 0.868 \tag{3.25}$$

$$V_{dc} = \frac{\sqrt{3}}{2} \cdot M \cdot V_m \cdot \cos\theta = \frac{\sqrt{3}}{2} \cdot 0.868 \cdot 555.2 \cdot \cos 10^o = 411V \tag{3.26}$$

The dc choke current and the freewheeling diode voltages are shown in Fig. 3-31.

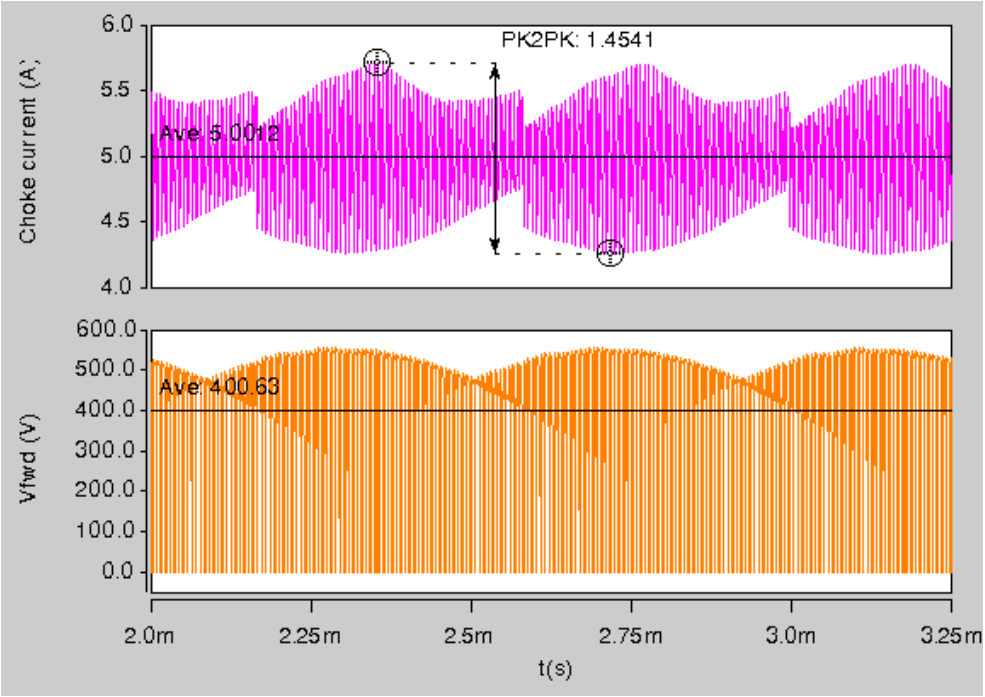


Figure 3-31. Dc-side choke current and freewheeling diode voltage for 400 Hz line frequency.

3.3.3. Simulation at 800 Hz Line Frequency

At 800 Hz line frequency, the controller lags the input phase currents by 20° with respect to the phase voltages. The output power is 1.7 kW, and the load voltage and current are shown in Fig. 3-32. In Fig. 3-33, the three phase input voltages and currents are shown. The filter losses are 35.9 W from simulation, and the semiconductor losses are read from Fig. 3-7 as 46 W. The resulting theoretical efficiency is 95.4%.

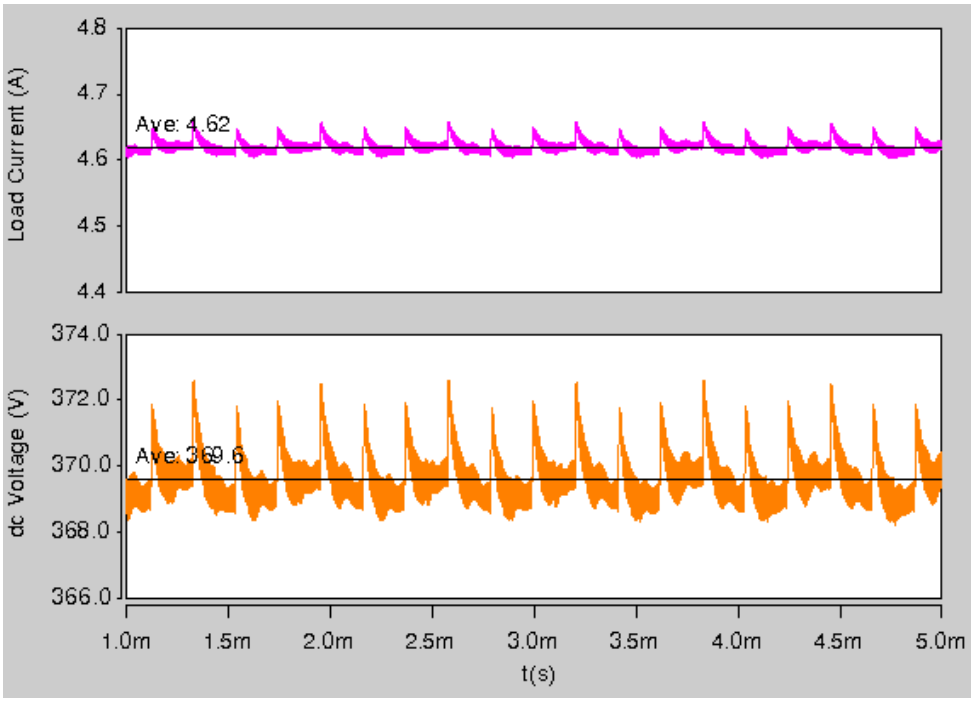


Figure 3-32. Load current and voltage for 800 Hz line frequency.

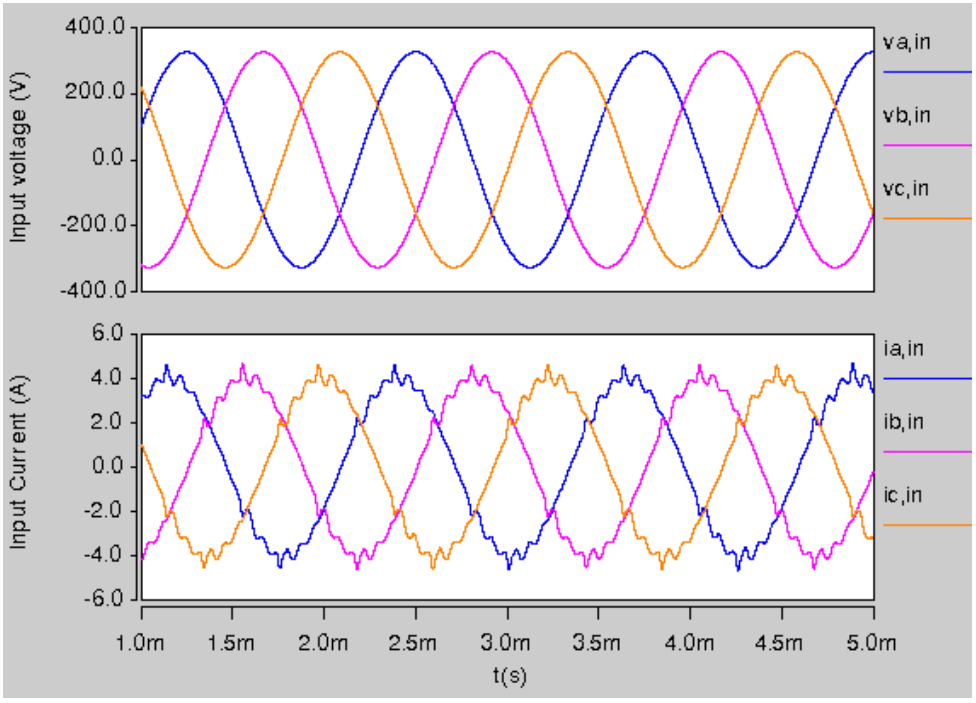


Figure 3-33. Three-phase input line-to-neutral voltages and phase currents at 800 Hz; voltage is 230 V_{rms} and current is 2.90 A_{rms}.

Again, the input current ringing due to the charge control scheme is observed in Figs. 3-33 and 3-34. The THD of the input phase currents is 5.689%. Although the THD exceeds specification, it should be solved by improving the control scheme rather than increasing the input filter size and damping, as mentioned previously.

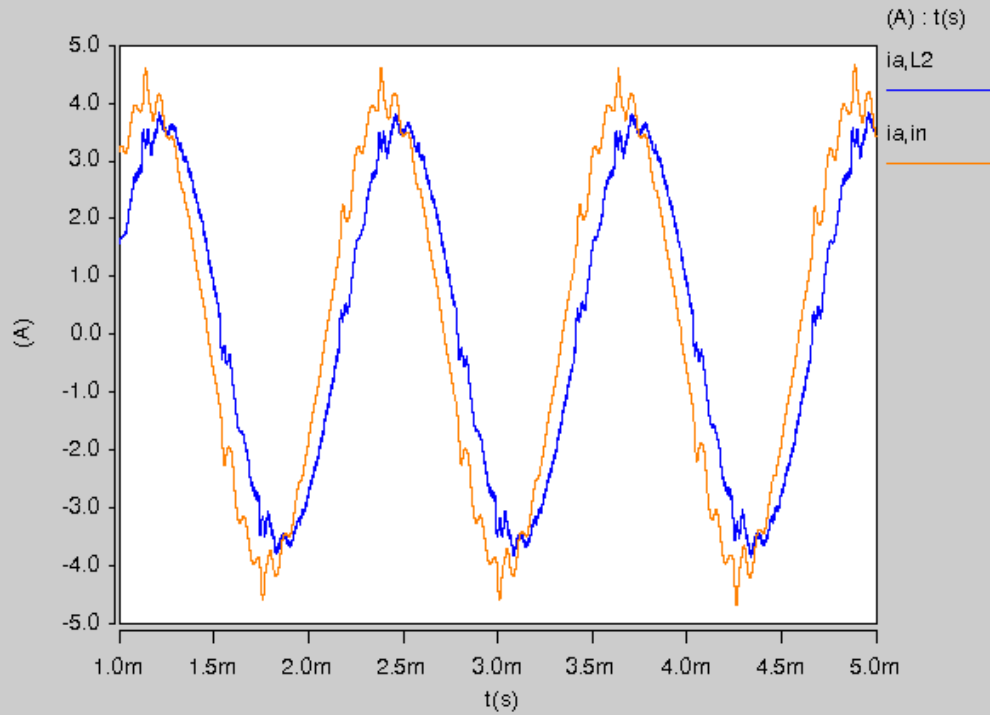


Figure 3-34. Comparison of input current ($i_{a,in}$) and second-stage inductor current ($i_{a,L2}$) for operation at 800 Hz.

For operation at 800 Hz line frequency, the power factor was lower. The input current and voltage for phase a are shown in Fig. 3-35; the phase current now leads the input voltage by 27.6°. The converter has a 0.886 leading power factor and an apparent power of 2.01 kVA at the three-phase input.

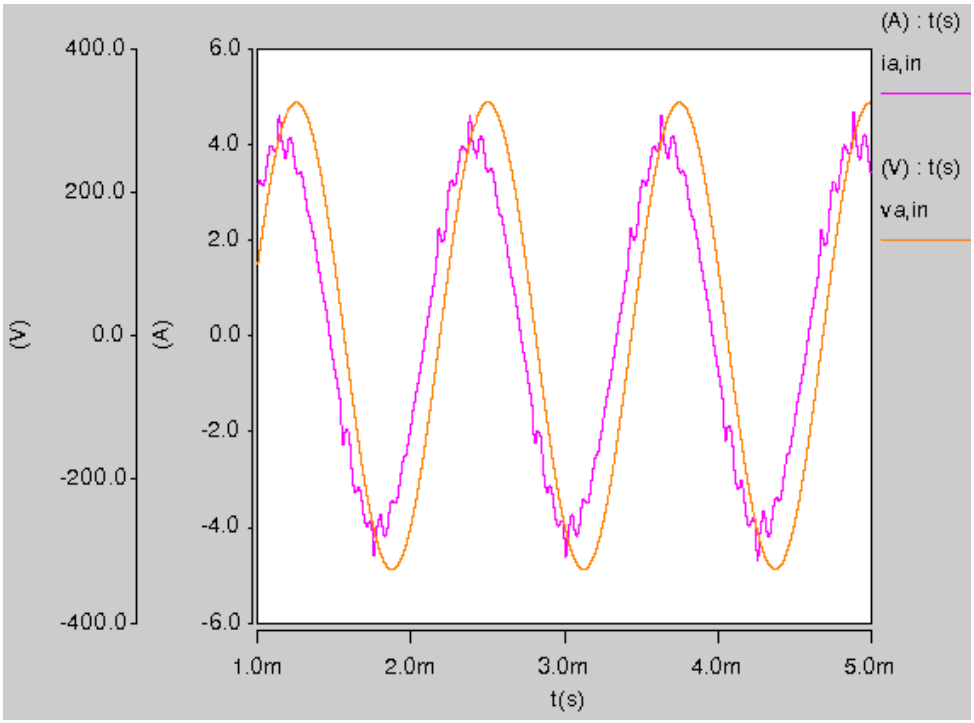


Figure 3-35. Input phase voltage and current for operation at 800 Hz line frequency.

The modulator gain M can again be calculated using (3.1). For this operating condition, the gain is calculated by (3.27), and the theoretical output voltage is then given by (3.28). The dc choke current and freewheeling diode voltage are both shown in Fig. 3-36.

$$M = \frac{I_m}{I_{dc}} = \frac{3.86\,A}{4.62\,A} = 0.835 \tag{3.27}$$

$$V_{dc} = \frac{\sqrt{3}}{2} \cdot M \cdot V_m \cdot \cos\theta = \frac{\sqrt{3}}{2} \cdot 0.835 \cdot 557.7 \cdot \cos 20^o = 379.0\,V \tag{3.28}$$

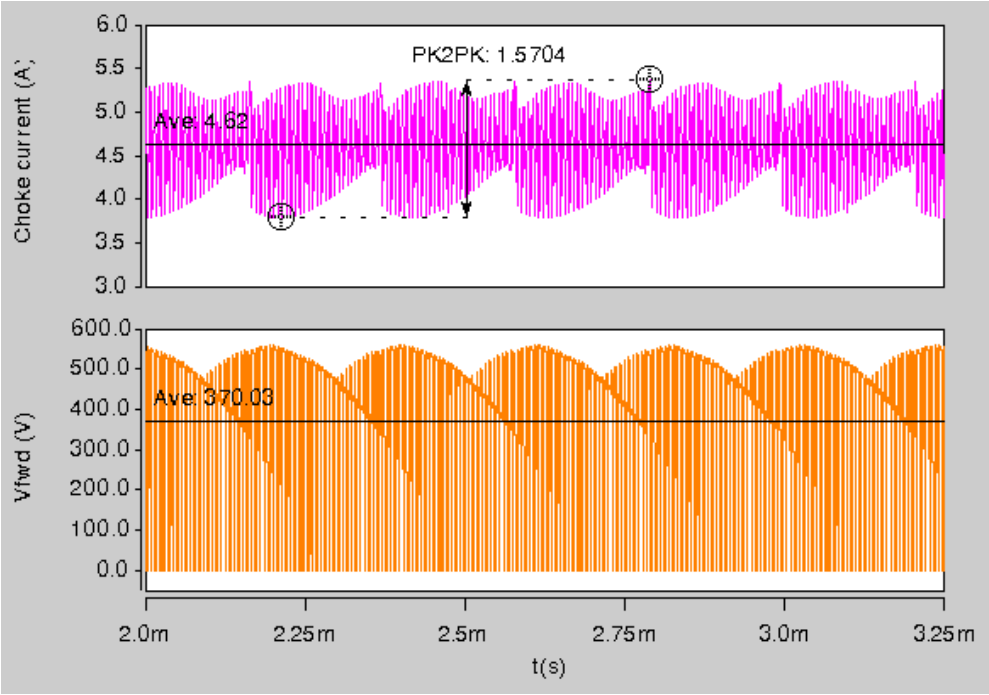


Figure 3-36. Dc-side inductor current and freewheeling diode voltage for 800 Hz line frequency.

3.4. Improved Reference Generation to Eliminate Input Current Transient

3.4.1. Cause of Transient

The transient observed in the input phase current is due to the assumption made by the *Charge Controller* block in the original control method [15], in that it presumes that the vector of largest magnitude is always applied first. Based on this presumption, it is necessary to generate the integrator references as shown in Fig. 3-37. In the figure, the sub-sector changes from *I-1* to *I-2* near time 2.57 ms. As can be observed, from the beginning of each switching period, the integrating capacitor charges (V_{int}), always crossing I_{r1} first, and then I_{r2}. From the shape of the reference waveform, it is apparent that the time it takes to integrate from zero to I_{r1} is always longer than the time to integrate from I_{r1} to I_{r2}. As such, the gate pulses *G1* and *G2* must be distributed in a different order for each sub-sector. In the example shown (Fig. 3-37), switch *Sap* is always on for both sub-sectors *I-1* and *I-2*. In sub-sector *I-1*, the longer pulse (*G1*) must be distributed to *Sbn*, while the shorter pulse (*G2*) must be sent to *Scn*. Once the sector changes to *I-2*, the order is reversed; *Scn* must receive the first pulse (*G1*) and *Sbn* must receive the second

(*G2*). This causes both a gap in the pulses sent to one switch (*Sbn* in this case) and generates 2 closely-spaced pulses in the other switch (here, *Scn*) at the moment the sub-sector changes.

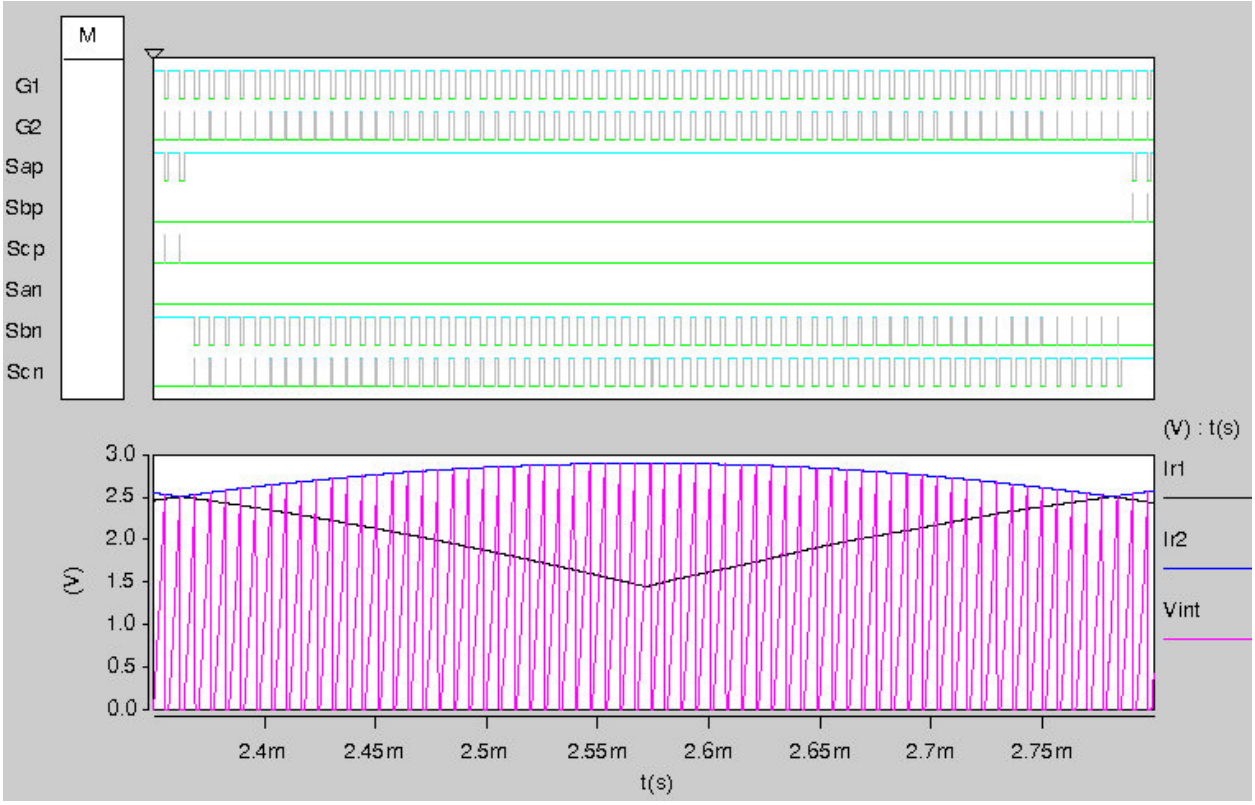


Figure 3-37. Integrator and reference waveforms and resulting gating signals for original scheme showing cause of transient at sub-sector change near 2.57 ms.

The new *Charge Controller* block described in section 3.2.2.5 was developed in order to allow phase angle compensation. The resulting *Charge Controller* (Fig. 3-23) no longer assumes that the largest magnitude vector is applied first. Now, this modification may be further exploited to allow a new shape for the integrator references, and eliminate the need to reverse the order in which the gating signals are sent in sub-sectors.

3.4.2. Improved Charge Control Scheme

The improved charge control scheme generates the integrator references and resulting gating signals as shown in Fig. 3-38. The improved scheme has eliminated the need for sub-sectors, and has changed the shape of *Ir1*. With this scheme, the generated pulse *G1* starts with a high duty cycle at the beginning of the sector, which decreases every switching period until the duty cycle

is almost zero at the end of the sector. The gating pulse *G2* does the opposite, starting with low duty cycle and ending with high duty cycle at the end of each sector. The end result is that the first switch (*Sbn* in this case, sector *I*) may receive gating pulse *G1* throughout the entire sector; similarly, *G2* is sent to the second switch (here, *Scn*) for the entire sector. The gaps and crowded pulses apparent in the original scheme no longer occur, and the resulting switching commands resemble that of standard space-vector modulation for the buck rectifier. The following sections describe the changes necessary in the controller logic in order to achieve the improved control scheme. The VHDL code listing for the improved control scheme is given in Appendix III-B.

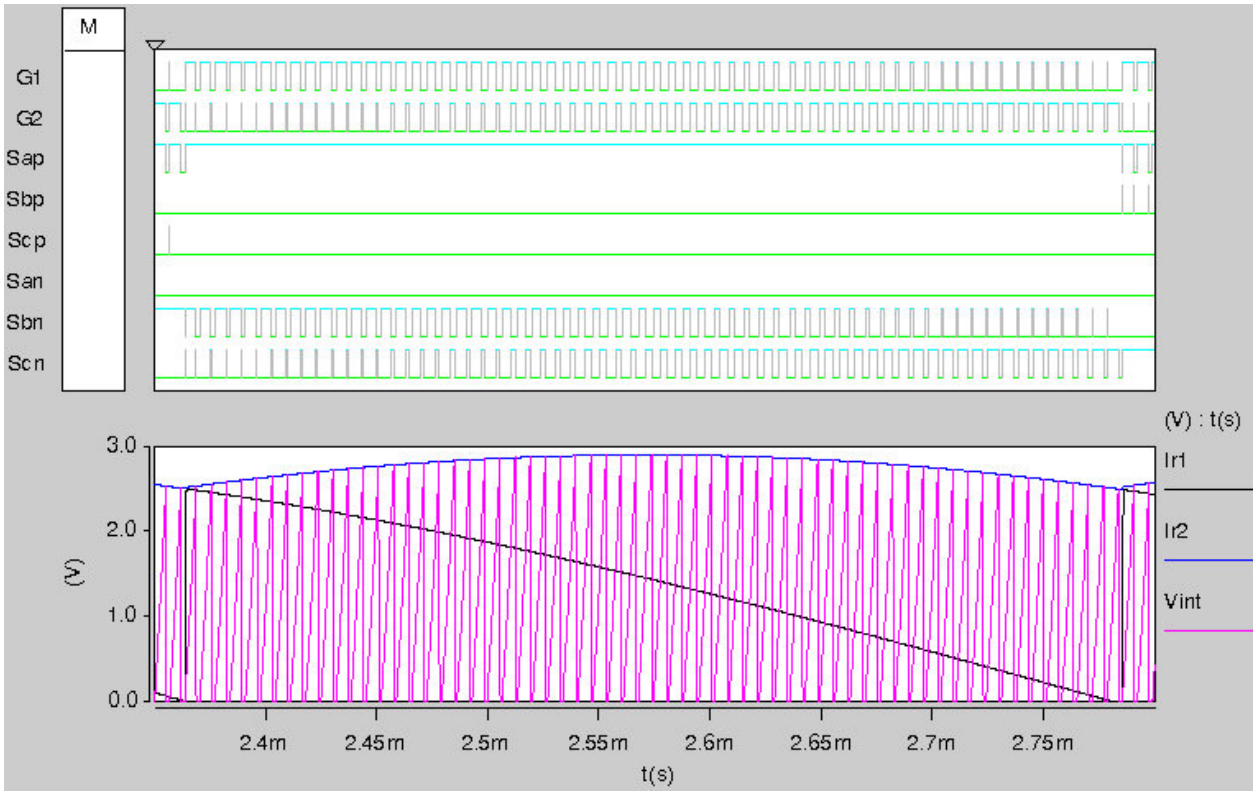


Figure 3-38. Charge control waveforms using new scheme to eliminate transients.

3.4.2.1. Simplified Sector Identification Scheme

As the sub-sectors do not need to be identified in the improved scheme, the sector detection is simplified. The six sectors that need to be detected are shown in Fig. 3-39; they are identical to the sectors used in standard space vector modulation for the buck rectifier. The improved scheme has also reduced the number of comparators needed for sector detection from 6 comparators to 3

(Fig. 3-40). In Table 3-7, the corresponding sector detection logic is shown; the sector ID bits y_3, y_2, and y_1 are the same as for the original scheme, while bit y_0 has been eliminated.

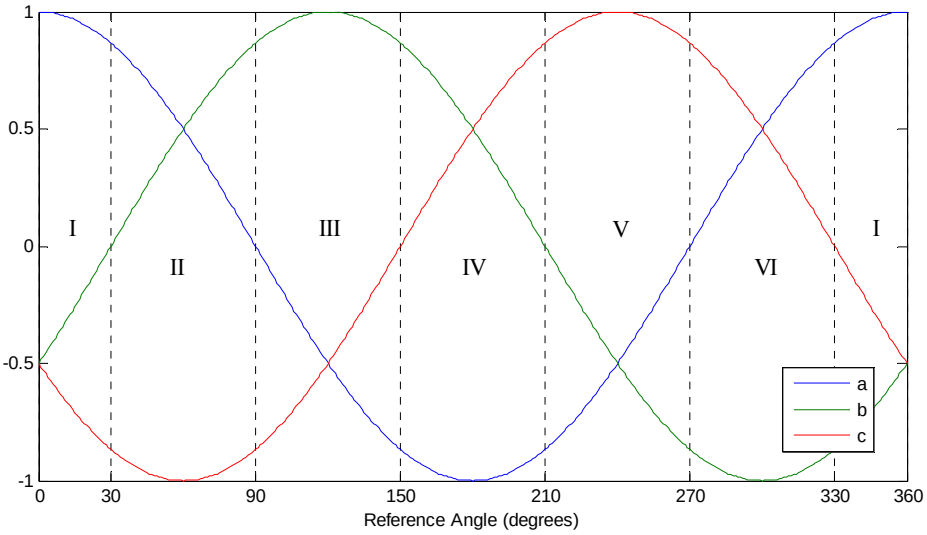


Figure 3-39. Three-phase reference sectors for improved control scheme.

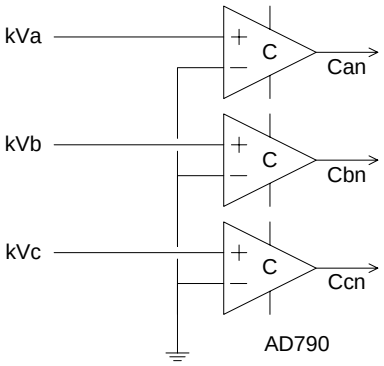


Figure 3-40. Simplified comparator circuit.

TABLE 3-7: SECTOR IDENTIFICATION TRUTH TABLE FOR IMPROVED CONTROL SCHEME

Sector	Can	Cbn	Ccn	$y_3y_2y_1$
I	1			000
II	1	1		001
III		1		010
IV		1	1	011
V			1	100
VI	1		1	101

3.4.2.2. Reference Generation

Using the same three-phase absolute value reference signals as the original scheme, the new reference *Ir1* may be generated as given by Table 3-8. The multiplexer select bits *Max1* and *Max0* still select the reference with the largest magnitude. Different than the original control scheme, bits *Med1* and *Med0* now select the reference of median magnitude only at the beginning of each switching sector, and are not reevaluated for the remainder of the sector. Previously, the median value signal was reevaluated at the sub-sector change. In Fig. 3-41, the

absolute value three-phase references are shown, along with the resulting integrator references for the improved control scheme.

TABLE 3-8: REFERENCE GENERATION TRUTH TABLEFOR IMPROVED CONTROL SCHEME

Sector	$y_3y_2y_1$	Med1	Med0	Max1	Max0
I	000	1			1
II	001		1	1	1
III	010	1	1	1	
IV	011	1			1
V	100		1	1	1
VI	101	1	1	1	

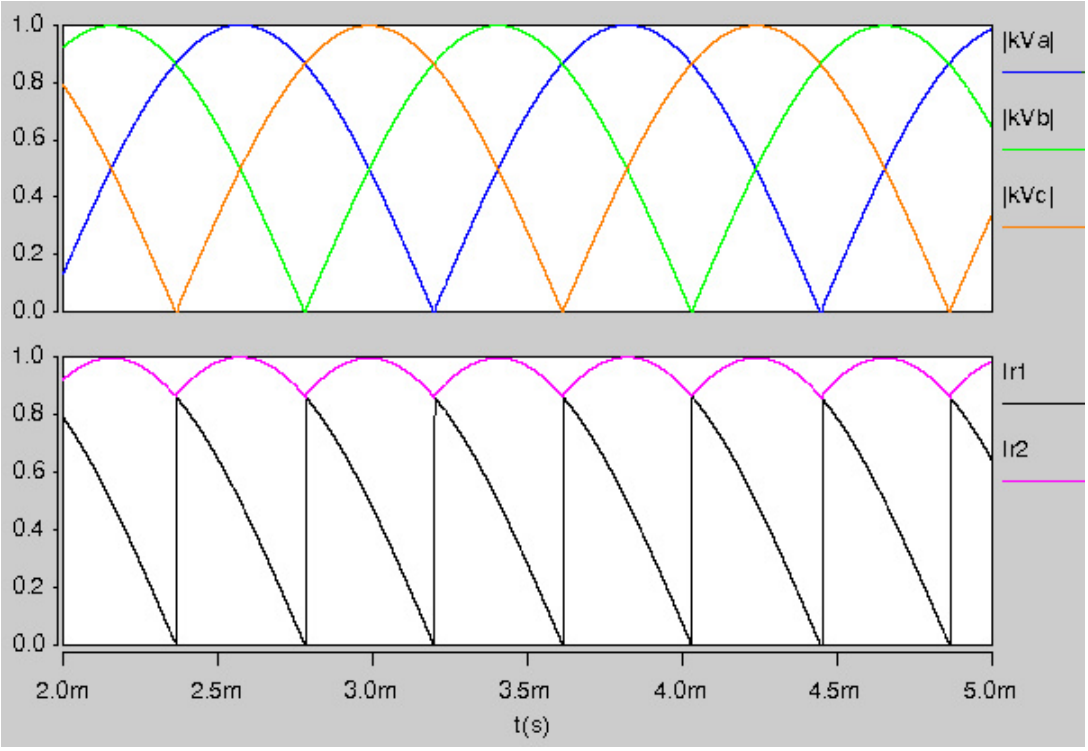


Figure 3-41. Integrator references I_r1 and I_{r2} for improved control scheme are generated using the same three-phase reference absolute value signals as the original scheme.

3.4.2.3. Gate Signal Distribution

As mentioned previously, the gating signals *G1* and *G2* are sent to the same switches throughout each sector, eliminating the swap that previously occurred at sub-sector changes. Table 3-9 indicates the gate signal distribution for the improved charge control scheme.

TABLE 3-9: GATE SIGNAL DISTRIBUTION FOR IMPROVED CONTROL SCHEME

Sector	$y_3y_2y_1$	ON	G1	G2
I	000	Sap	Sbn	Scn
II	001	Scn	Sap	Sbp
III	010	Sbp	Scn	San
IV	011	San	Sbp	Scp
V	100	Scp	San	Sbn
VI	101	Sbn	Scp	Sap

3.4.3. Simulation of Converter with Improved Charge Control Scheme

The buck rectifier is again simulated with 400 Hz input line frequency, and 2 kW output power (same conditions as section 3.3.2). As observed in Fig. 3-42, the input currents no longer exhibit the transients caused by sub-sector changes in the original control scheme. The only transients that occur are due to the lack of synchronization between the switching clock and the input sectors; that is, the controller latches the sector during each switching period, so if the input sector changes during the switching period, it is not reflected in the controller until the start of the next switching period. The switching frequency is sufficiently high enough that the effect is minimal, and the transients are not easily observable in the input phase currents. The input current THD is improved to 0.24%. As seen in Fig. 3-43, the output waveform quality is improved as well. The improved control scheme has also elminated the sharp transients previously visible in the load voltage and current (Fig. 3-27).

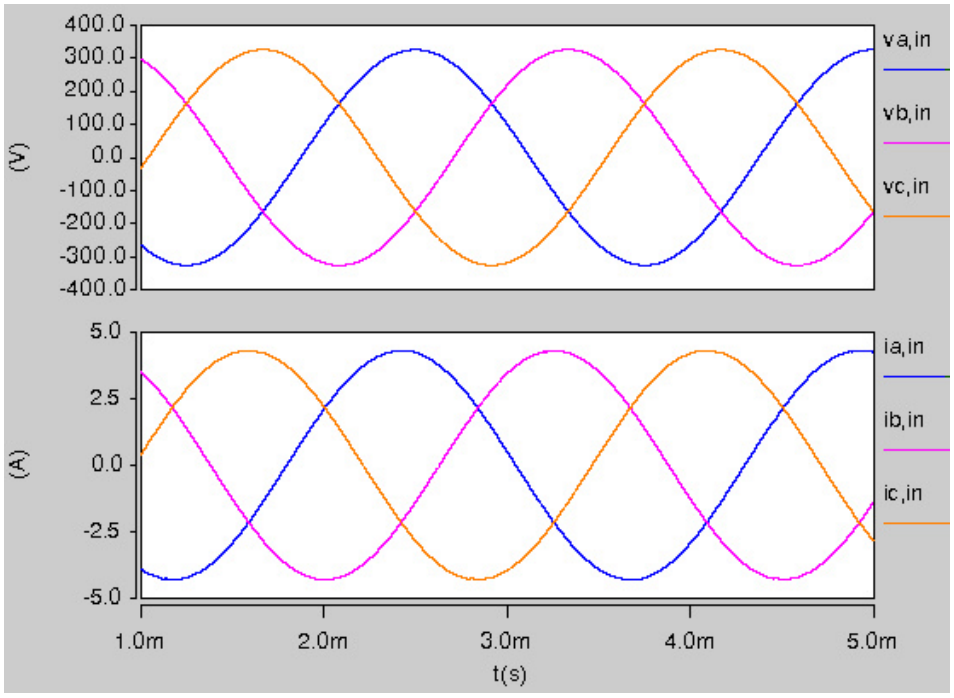


Figure 3-42. Simulated input line-to-neutral voltages and phase currents for the buck rectifier using the improved charge control scheme.

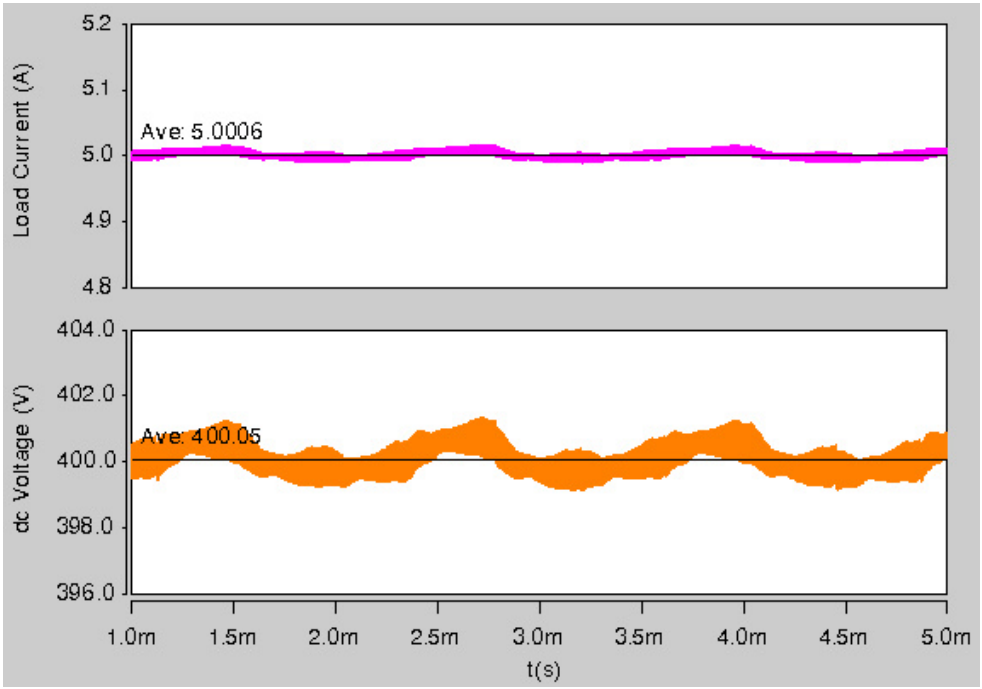


Figure 3-43. Simulated load current and voltage with new control scheme.

4. THE SIC JFET BUCK RECTIFIER

4.1. The Converter

The SiC JFET buck rectifier is constructed according to the design presented in chapter 3. Complete power stage, input filter, and controller schematics are shown in Appendix II. The controller VHDL code is listed in Appendix III. The assembled converter hardware is pictured in Fig. 4-1. The input filter, power stage, and output filter were all mounted inside the enclosure, along with fans. The voltage sensors and controller board were mounted in the enclosure above the power stage, as shown in Fig. 4-2. The 24 V dc bias supply for the controller and gate drivers was provided by a bench-top power supply. At each board, the dc supply is fed to an isolated converter, which regulates the voltage supplied to the circuits. The three-phase ac power source was an HP6834B and a resistive load bank was used as the load.

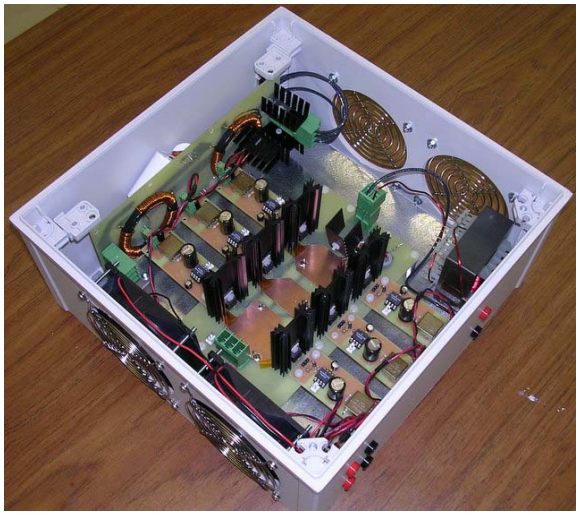


Figure 4-1. SiC buck rectifier power stage and filter hardware in enclosure.

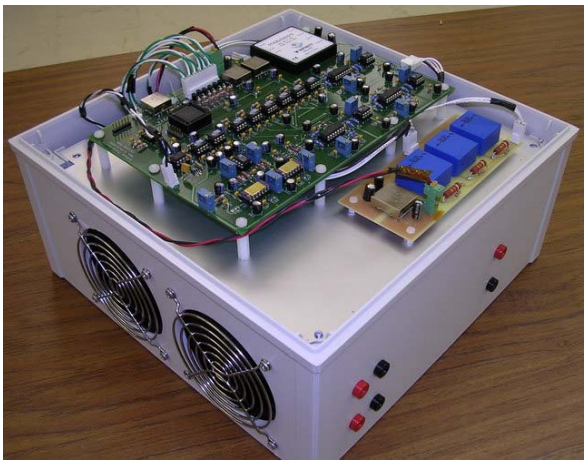


Figure 4-2. Buck rectifier enclosure with controller installed.

4.2. Experimental Demonstration and Analysis

4.2.1. Basic Operation at Rated Power

The converter is operated at the nominal apparent power rating of 2 kVA for both 400 Hz and 800 Hz input line frequency and nominal input voltage. This section shows the basic operating waveforms at the converter input and output terminals to verify operation of the buck rectifier. In Table 4-1, the operating points for both test conditions are summarized.

TABLE 4-1: SUMMARY OF OPERATION AT 400 HZ AND 800 HZ LINE FREQUENCIES

	400 Hz	**800 Hz**
Converter Gain M	0.82	0.82
Input apparent power (VA)	2,093.3	2,032.4
Power factor	0.976 (+)	0.906 (+)
Input real power, P_{in} (W)	2,043.1	1,840.4
Input phase voltage (V_{rms})	228.4	228.8
Input phase current (A_{rms})	3.056	2.961
Input phase angle (degrees)	12.65°	25.11°
Freewheeling diode average voltage, V_{fwd} (V)	390.6	367.5
Average dc load voltage, V_{dc} (V)	384.1	361.2
Average dc choke current, I_L (A)	4.859	4.688
Average dc load current, I_{dc} (A)	4.86	4.7
Output power, P_{out} (W)	1,866.7	1,697.6

For operation at the nominal conditions with 400 Hz input line frequency, Fig. 4-3 plots the input phase-to-neutral voltages and phase currents over two line periods. It is observed that the input voltage and current are nearly in phase, with the current leading the voltage by 12.65°, resulting in an input power factor of 0.976 leading (Fig. 4-4). The distortion on the input phase currents are due to the sector changes, generating a small transient 6 times per line period. Though the input filter is damped, the transients cause a slight ringing of the phase current in the input filter; the frequency of the ringing is 5.2 kHz, which is the 13^{th} harmonic of the line

frequency, as shown by the input current spectrum of Fig. 4-5. Total harmonic distortion (THD) of the input current is 4.2%.

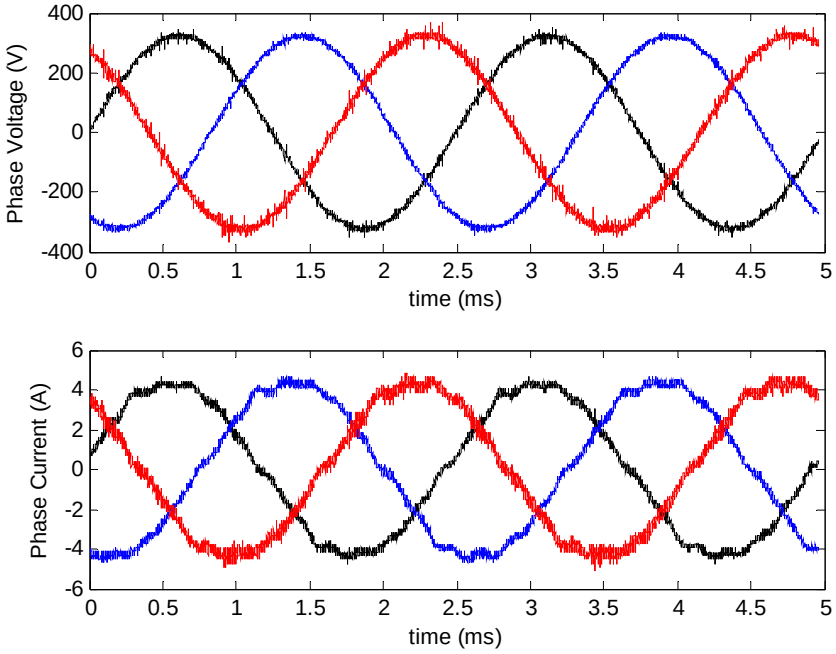


Figure 4-3. Input waveforms for 400 Hz line frequency.

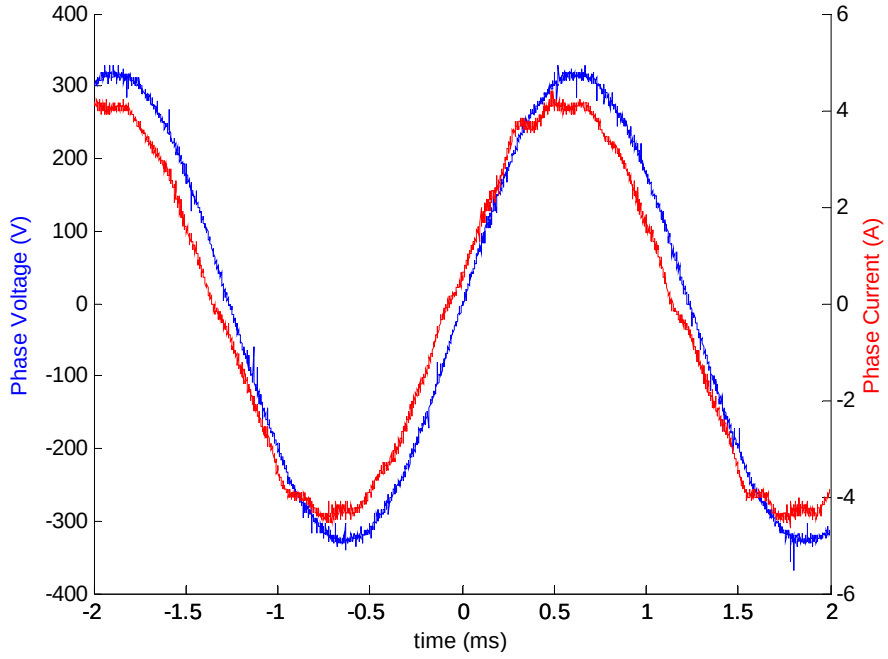


Figure 4-4. Power stage input phase (line-to-neutral) voltage and current (phase a) for 400 Hz line frequency.

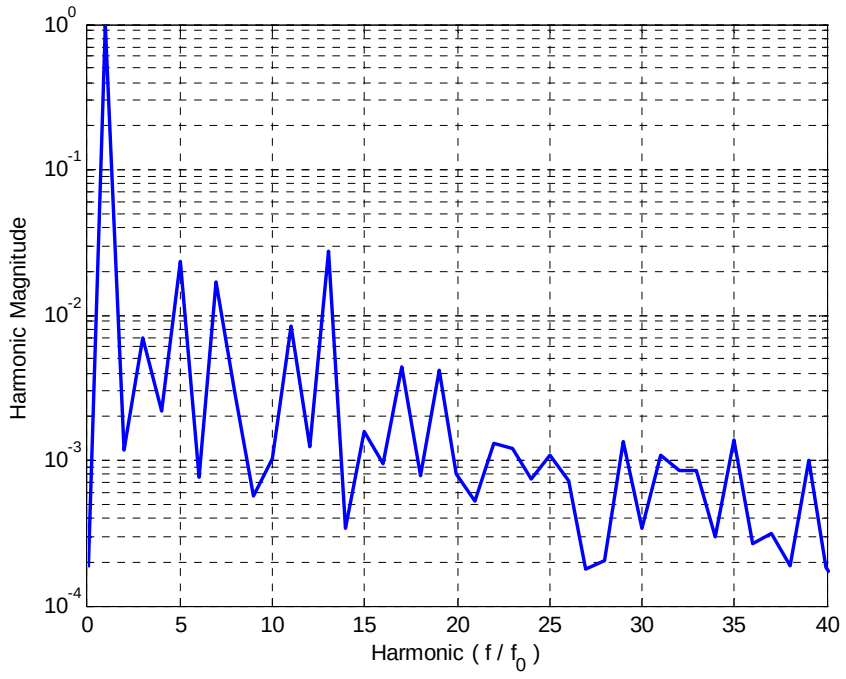


Figure 4-5. Input current harmonic magnitude as a fraction of fundamental current (400 Hz line frequency).

In Fig. 4-6, the output waveforms of the buck rectifier at nominal condition for 400 Hz input line frequency are shown. The figure shows the freewheeling diode voltage (V_{fwd}), dc load voltage (V_{dc}), the dc inductor current (I_L), and the dc load current (I_{dc}) into the 80 Ω resistive load. The ripple of the dc inductor current is 1.6 A peak-to-peak. The actual switching frequency of the converter is 147 kHz, as shown by the PWM waveform of the freewheeling diode voltage (V_{fwd}).

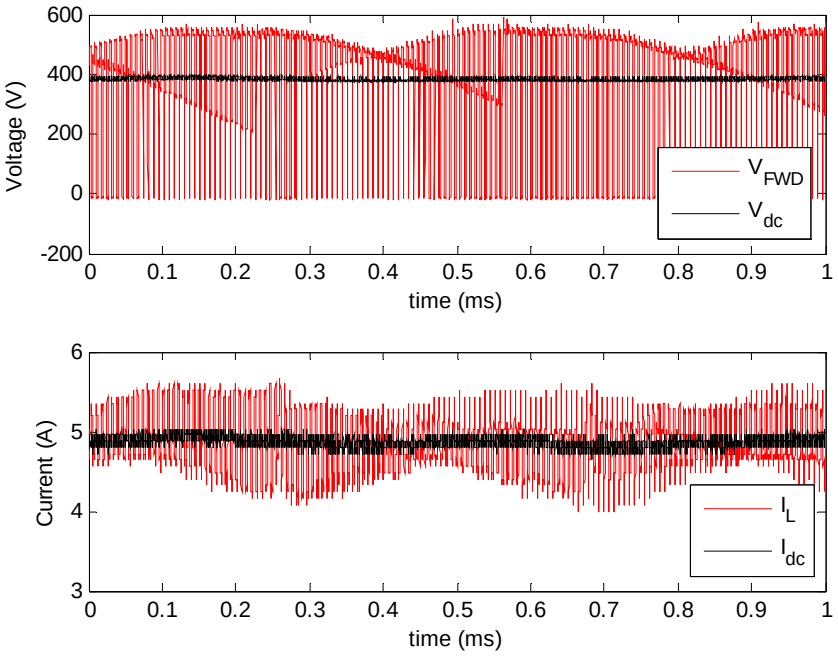


Figure 4-6. Output waveforms for 400 Hz line frequency.

The input phase voltage and current waveforms for nominal operation at 800 Hz are shown in Fig. 4-7. The angle of the input phase currents was more capacitive, as expected from the capacitive nature of the input filter. The input phase current lead the voltage by 25.11°, yielding a leading power factor of 0.906. Again, the sector change occurring at 6 times the line frequency causes ringing of the phase currents in the input filter. From the input current spectrum for 800 Hz line frequency (Fig. 4-8), it is seen that the ringing is at the 5^{th} and 7^{th} harmonics of the line frequency, corresponding to 4 kHz and 5.6 kHz, respectively. Because the ringing is at a lower harmonic than for the 400 Hz case, the distortion of the input currents becomes more noticeable; THD is 7.4%. Careful tuning of the input filter and its damping network would be needed in order for operation at 800 Hz to become tolerable with respect to input current THD. Another option could be active damping of the input currents [22, 23]. In Fig. 4-9, the freewheeling diode and load voltages are shown, as well as the dc inductor and load currents.

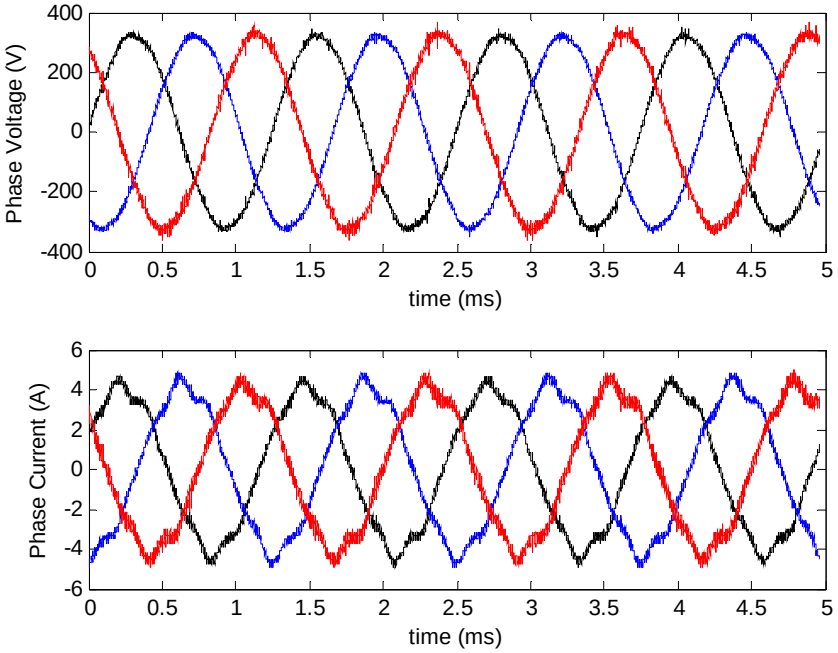


Figure 4-7. Input waveforms for 800 Hz line frequency.

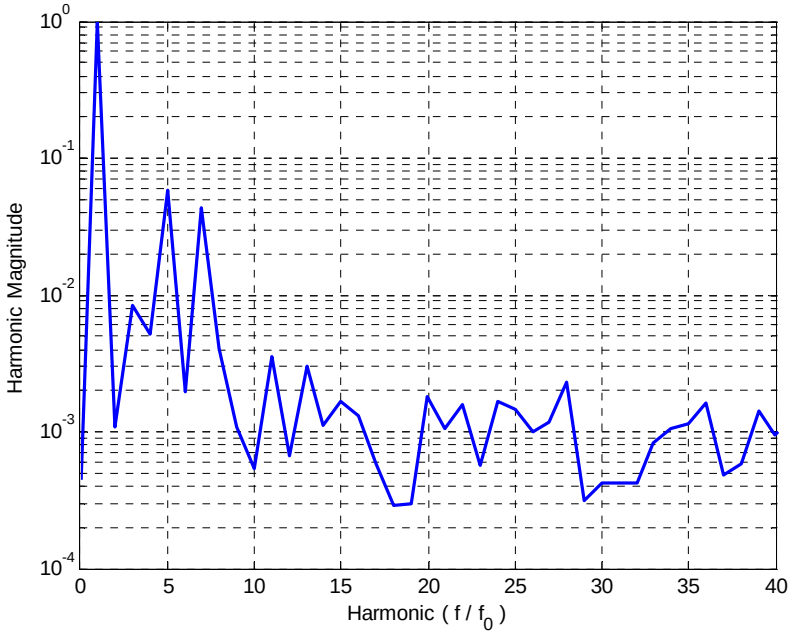


Figure 4-8. Input current harmonic magnitude as a fraction of fundamental current (800 Hz line frequency).

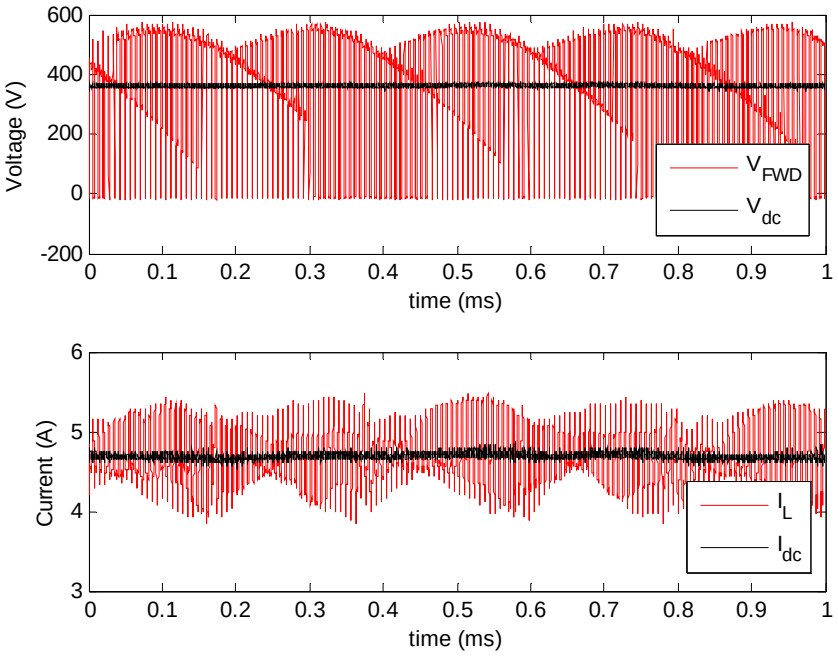
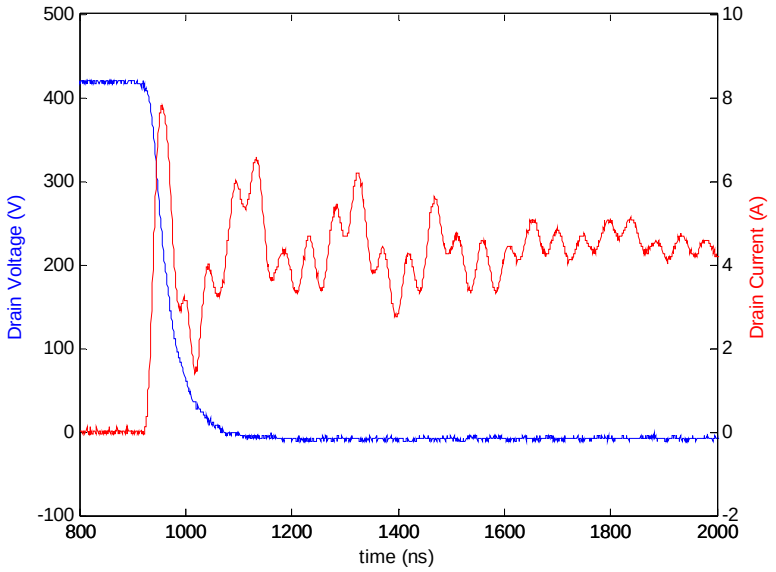


Figure 4-9. Output waveforms at 800 Hz line frequency.

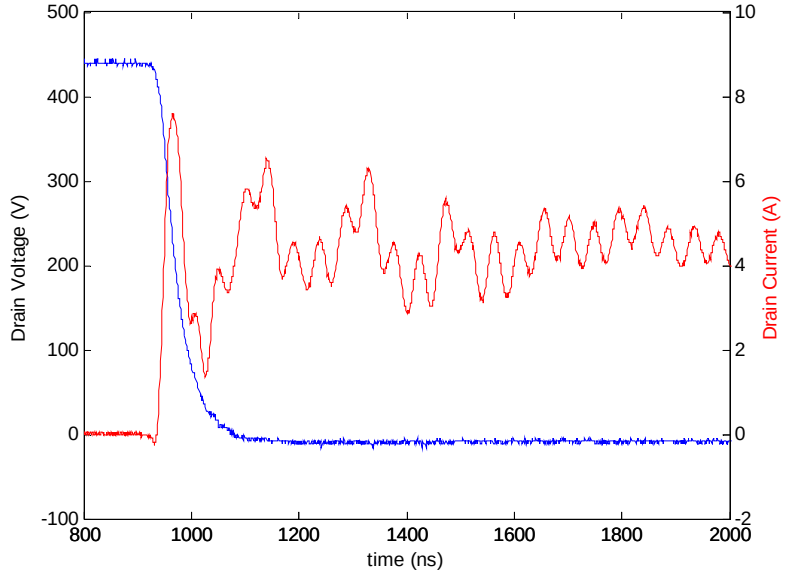
The basic operation of the SiC JFET buck rectifier has been demonstrated for the nominal 2 kVA rating, at both 400 and 800 Hz line frequencies. Though the input currents may be improved by increased damping, either passive or active, the waveforms are acceptable for analyzing the characteristics relevant to the focus of this work. The following sections analyze the switching performance of the SiC JFET in the buck rectifier, the converter losses, and common-mode noise issues of the SiC JFET buck rectifier.

4.2.2. Switching Performance of the SiC JFET in the Power Stage

In order to provide a comparison point for the validity of the switching characterization done in chapter 2, switching waveforms of the SiC JFET were observed while the converter was operating at full power (2 kW output). The surface temperature of the heat sink was measured to provide a reference point for estimation of the junction temperature. Typical JFET turn-on and turn-off waveforms are shown in Figs. 4-10 and 4-11 for two different conditions. In the first condition, the fans were turned on resulting in a heat sink temperature of 51 °C. The second condition was for the fans turned off, which caused the heat sink temperature to rise to 88 °C.



(a)



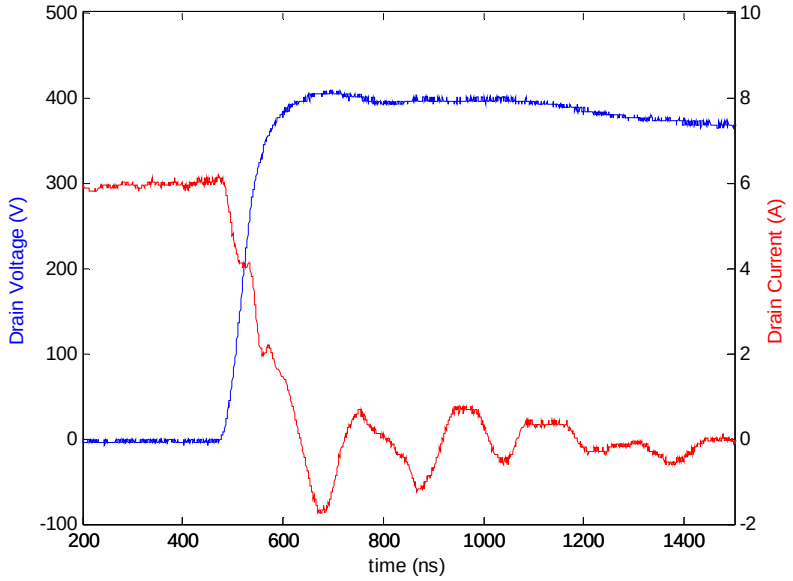
(b)

Figure 4-10. Turn on behavior of the SiC JFET during normal operation of the buck rectifier for heat sink surface temperature of (a) 51 °C and (b) 88 °C.

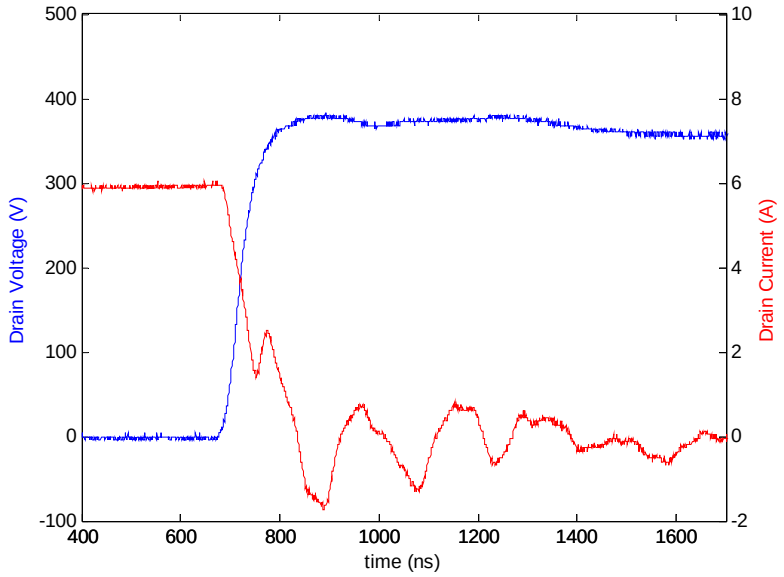
For the turn-on waveforms of Fig. 4-10, it is observed that there is a considerable ringing of the current waveform compared to the two-pulse switching results shown in Chapter 2 (Fig. 2-8).While the two-pulse test results displayed a similar current overshoot at turn-on, there was virtually no ringing following the overshoot. The ringing is due to the increased parasitics

present in the power stage in the form of additional switches, diodes, and other components. The components not only add parasitic capacitances due to their presence, but also make a compact layout more difficult, thereby increasing trace lengths on the circuit board, thus increasing parasitic inductance. Additionally, the current transformer used to sense the switch current adds a considerable length of wire between the switches and the freewheeling diode. This inductance is directly in the conduction path when a switch commutates current from the freewheeling diode.

The current rise time at turn-on is 14 ns and 12 ns for Figs. 4-10a and 4-10b, respectively, which is in agreement with the typical current rise times observed in the switching characterization. The voltage fall times, however, are 2 to 3 times longer than observed in the switching characterization, at 101 ns for both conditions shown. For the condition of 51 °C heat sink temperature, the total turn-on switching time is 107 ns; the turn-on time is 101 ns for condition of heat sink temperature of 88 °C. In general, the turn-on times are twice as long as observed in the two-pulse test. The main contributor is the increase in the time of the voltage fall. Turn-on energies are 78.4 µJ and 75.0 µJ for heat sink temperatures of 51 °C and 88 °C, respectively.



(a)



(b)

Figure 4-11. Turn off behavior of the SiC JFET during normal operation of the buck rectifier for heat sink surface temperature of (a) 51 °C and (b) 88 °C

The JFET turn-off waveforms of Fig. 4-11 also display significantly more ringing of the current waveform when compared with the two-pulse characterization. As stated previously, the ringing is due to increased parasitics in the current switching path. The current fall times are 140 ns for both conditions shown in the figure; this is a factor of 3 times longer than observed in the two-pulse tests. The voltage rise times are also 3 times longer, at 109 ns and 99 ns for Figs. 4-11a and 4-11b, respectively. Consequently, it is expected that the turn-off energies will be considerably larger than observed in the characterization. For heat sink temperature at 51 °C, turn-off energy is 87.7 µJ, while the turn-off energy for 88 °C is 78.4 µJ.

Using the switching energies and the recorded heat sink temperatures, it was estimated that the junction temperature rise of the SiC JFET is 10 °C above the heat sink temperature. To compare the switching energy of the JFET in the power stage to those obtained in the two-pulse test more directly, Table 4-2 presents the results of the power stage switching for the case where the fans are turned off and the two-pulse test result from the nearest similar conditions (Appendix I). Though the estimated junction temperature of the power stage switching case is 98 °C, it is shown from Fig. 2-15 that both the turn-on and turn-off energies remain effectively constant for junction temperatures between 90 °C and 125 °C; therefore, comparison with two-pulse test results at 90 °C is reasonable. Because the switched voltage and current levels for the

power stage measurements differ from the nearest two-pulse condition (400 V and 5 A), the approximation is made that to the first-order, the measured switching energy (E_{meas}) may be scaled linearly with respect to switched voltage (V_{sw}) and current (I_{sw}), as given by (4.1).

TABLE 4-2: SIC JFET SWITCHING ENERGY COMPARED TO TWO-PULSE CHARACTERIZATION

		T_{sink} (°C)	T_j (°C)	E (µJ)	Switch Voltage (V)	Switch Current (A)	E (scaled, µJ)
Turn-on	**Two-Pulse**	–	90	62.7	400	5	***62.7***
	Power Stage	88	98	75.0	440	4.5	***75.8***
Turn-off	**Two-Pulse**	–	90	14.1	400	5	***14.1***
	Power Stage	88	98	78.4	375	5.9	***70.9***

$$E = E_{meas} \cdot \frac{400V}{V_{sw}} \cdot \frac{5A}{I_{sw}} \tag{4.1}$$

While the switching energy at turn-on agrees well with the two-pulse test, at only 21% larger than predicted, the turn-off energy is significantly larger. Compared to the two-pulse test results, the turn-off energy for the SiC JFET in the power stage is 5 times greater. The increase in turn-off energy is attributed to the increased switching time, which in turn creates a longer overlap where the switch is starting to block voltage while still conducting a large current (see Fig. 4-11b). A reduction in parasitics could significantly decrease the turn-off energy, as the turn-off current transient is slowed by the ringing that occurs near the time of 800 ns in Fig. 4-11b. From the results, it is observed that using the two-pulse test to calculate turn-on losses is reasonable; however, when calculating turn-off losses, the turn-off energy from the two-pulse test should be scaled by a factor of 5. This analysis is for the particular hardware demonstrated in this work; other hardware using the SiC JFET may have different parasitic characteristics, making the switching behavior either more or less ideal compared to the two-pulse test. The effort for minimizing parasitics in this particular implementation was moderate, and consisted of

minimizing the length of traces and maximizing trace width, while being constrained by the physical spacing of the devices and heat sinks.

4.2.3. Converter Loss and Efficiency

This section shows calculation of the semiconductor losses based on the switching energies measured in the preceding section. The total converter efficiency is calculated, and the losses due to passive components (input and output filter) are calculated from measured current and voltage waveforms.

As the first step in analyzing the breakdown of converter losses, the semiconductor losses are estimated. Here, only the calculation values for 400 Hz line frequency are shown for example. The main diode, freewheeling diode, and JFET conduction losses are calculated by (4.2) through (4.4). The semiconductor losses are calculated by (4.5) using the switching energies measured in the previous section for converter operation with 51.4 °C heat sink temperature, scaled to the average switching voltage (563.4 V) and current (5 A) of the converter. Finally, the estimated 10 °C junction temperature rise above heat sink temperature is verified by (4.6).

$$P_{cond,D} = \frac{1}{3} \cdot M \cdot I_{dc} \cdot V_f = \frac{1}{3} \cdot 0.82 \cdot (4.974\,A) \cdot (1.2V) = 1.63W \tag{4.2}$$

$$P_{cond,FWD} = (1 - M) \cdot I_{dc} \cdot V_f = (1 - 0.82) \cdot (4.974\,A) \cdot (1.2V) = 1.07W \tag{4.3}$$

$$P_{cond,JFET} = \frac{1}{3} \cdot M \cdot I_{dc}^2 \cdot R_{DS,on} = \frac{1}{3} \cdot 0.82 \cdot (4.974\,A)^2 \cdot (0.5\Omega) = 3.38W \tag{4.4}$$

$$P_{sw,JFET} = \frac{1}{2\pi} \cdot 150\,kHz \cdot \left(78.4\,\mu J \cdot \frac{5\,A}{4.5\,A} \cdot \frac{563.4V}{420V} + 87.7\,\mu J \cdot \frac{5\,A}{6\,A} \cdot \frac{563.4V}{400} \right) = 5.25W \tag{4.5}$$

$$\begin{aligned} T_{j,JFET} - T_s &= P_{JFET} \cdot (R_{j-c,JFET} + R_{c-s,JFET}) \\ &= 8.63W \cdot (0.24 + 0.95)\,^oC/W = 10.3\,^oC \end{aligned} \tag{4.6}$$

The total switching loss calculated in (4.5) is increased by 10 W (50%) compared to that predicted from the two-pulse test characterization. Table 4-3 summarizes the switching loss comparison of both cases, where the two-pulse test results have been interpolated from data in Appendix I for 5 Ω gate resistance. As seen by the data in the table, the increase in turn-off energy (E_{off}) dominates the total increase in switching loss.

TABLE 4-3: COMPARISON OF SWITCHING LOSS PREDICTED BY TWO-PULSE TEST AND CALCULATED FROM IN-CONVERTER MEASUREMENTS

	Two-Pulse (T_j = 90 °C)	**In-Converter (T_c = 51.4 °C)**
E_{on} (563.4 V, 5 A)	108 µJ	117 µJ
E_{off} (563.4 V, 5 A)	33 µJ	103 µJ
$P_{sw,JFET}$	3.36 W	5.25 W
Total Switching Loss (6 x $P_{sw,JFET}$)	20.2 W	31.5 W

In addition to the semiconductor losses, there were losses due to the series resistances of the input filter and output filter. These losses were calculated directly from measured voltage and current waveforms, and are summarized in Table 4-4. Also shown in the table are the total measured loss (difference of input and output real power), efficiency, the breakdown of losses calculated from measured waveforms, and the difference between measured and calculated losses. For the case of 400 Hz line frequency, there are 41.6 W of unaccounted for loss, while there are 17.9 W unaccounted for at 800 Hz line frequency. These differences between measured and calculated losses are due to three reasons: (1) measurement error, (2) additional series resistances in the power stage, and (3) approximations in the switching loss calculation. The first two reasons are easily understood. However, the switching loss calculation assumed that the switching energies scale linearly with switched voltage and current, which is a simple 1st-order approximation. Hence, the switching loss is most likely greater than calculated. If the total unaccounted loss of the 800 Hz line frequency condition is attributed to additional switching losses, this is an increase of 30% in semiconductor losses compared to calculation.

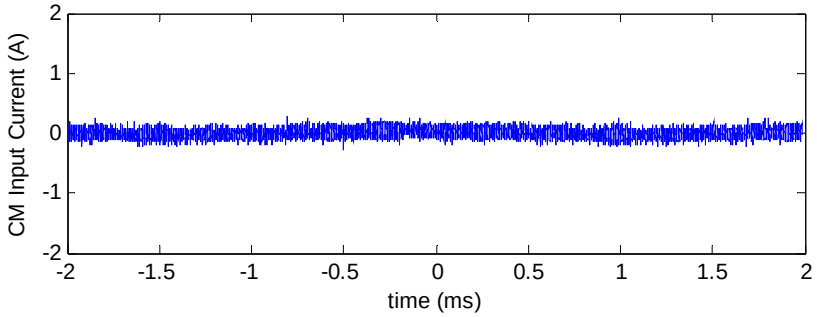
TABLE 4-4: CONVERTER LOSSES AT NOMINAL OPERATING CONDITIONS

	Loss (W) ***400 Hz***	**Loss (W)** ***800 Hz***
Total Measured Loss, P_{meas} (P_{in}-P_{out})	**176.4**	**142.7**
Efficiency (P_{out}/P_{in})	**91.4%**	**92.3%**
Total Calculated Loss, P_{calc}	**134.8**	**124.8**
Input Filter Loss	40.6	36.8
Semiconductor Loss	62.6	58.3
Output Filter Loss	31.6	29.7
Loss Unaccounted For ($P_{meas} - P_{calc}$)	**41.6**	**17.9**

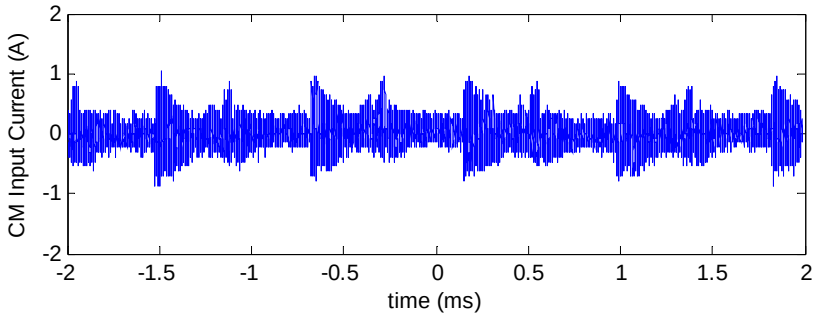
4.2.4. Common Mode Noise

The high-frequency switching action of the SiC JFET devices generated common-mode noise on the various current waveforms of the buck rectifier. The noise was distributed throughout the converter according to the impedances of the various common-mode noise paths to ground. Although there was no direct path to ground in either the converter, controller, or load, capacitive coupling to ground always exists. High-frequency common-mode chokes were placed on dc bias supplies for the gate drives and controller, as well as on the gate signals to the converter. Common-mode currents were observed at various points for the converter operating with a single dc-link choke (500 μH on the positive rail) and a split dc-link choke (250 μH on each positive and negative rail), which provides a symmetric path that should improve common-mode noise.

Figs. 4-12 and 4-13 show the common-mode current for the input phase currents and the dc load current, respectively, for both the single dc choke and the split dc choke. It was observed that the input phase current common-mode noise is reduced by using the single dc choke, while the dc load current common-mode is improved for the split dc choke.

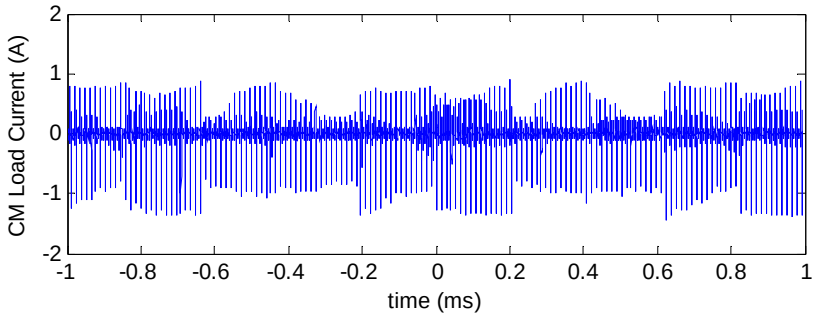


(a)

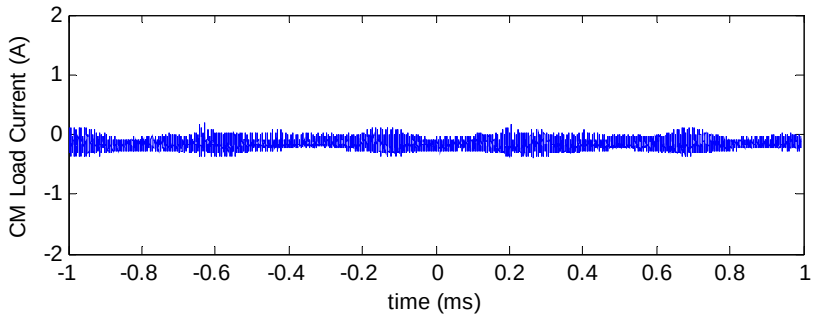


(b)

Figure 4-12. Common-mode input current for (a) single dc choke and (b) split dc choke.



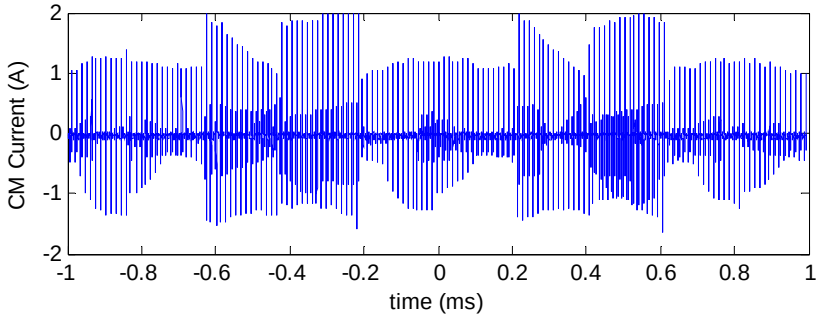
(a)



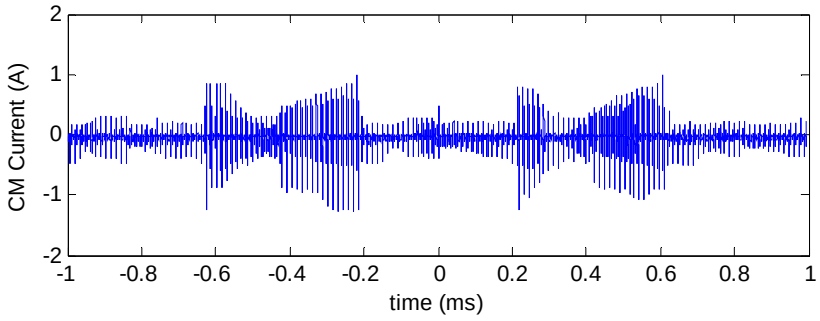
(b)

Figure 4-13. Dc load common-mode current for (a) single dc choke and (b) split dc choke.

Common-mode noise also conducts through the gate drivers as well. The relatively high capacitance between primary and secondary windings of the commercially-available isolated power supplies used provides a relatively low impedance path for the high-frequency common-mode noise. While each of the gate drivers has its own isolated input converter, the 3 positive-rail switches share a common wiring to the external dc bias, and the 3 negative-rail switches share a common wiring. In Fig. 4-14, the common-mode current is shown for the external dc bias supply to both the positive-rail and negative-rail gate drivers. The common-mode noise has the largest amplitudes for the input line sectors where the negative-rail switches are actively modulating (sectors I, III, and V), and the smallest amplitudes when the positive-rail switches are actively modulating (sectors II, IV, and VI). The common-mode current spikes are quite large for both, with maximum spikes of 2 A in amplitude. At 40% of the nominal dc output current of 5 A, this much common-mode noise would normally be unacceptable. The SiC JFET buck rectifier seems to show no ill effects in terms of converter operation due to the noise, however.



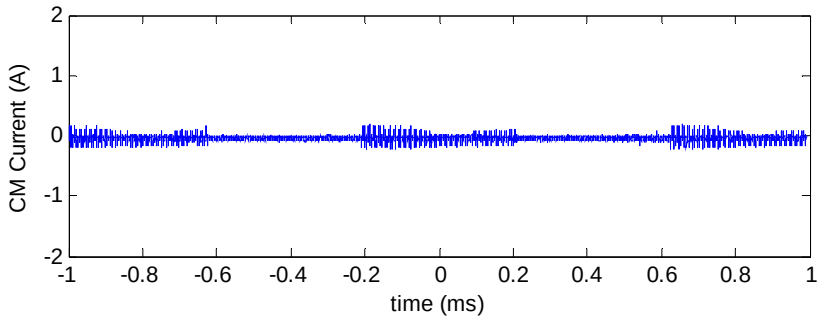
(a)



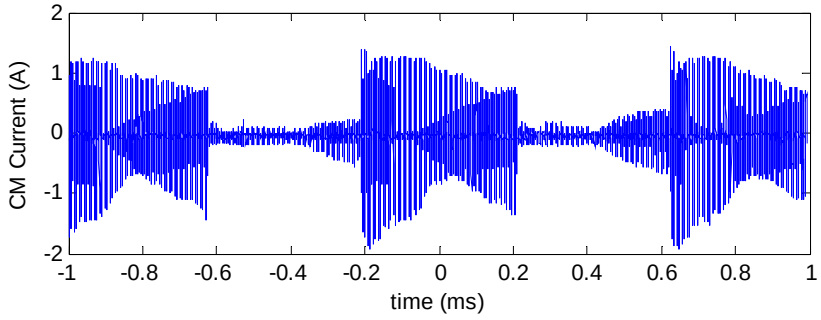
(b)

Figure 4-14. Common-mode current on the gate drive bias supply for (a) the positive-rail gate drivers and (b) the negative-rail gate drivers (with single dc choke).

For the case of the split dc choke, the gate drive bias supply common-mode noise improved greatly, as observed in Fig. 4-15. The common-mode noise on the positive-rail gate drivers was practically eliminated (Fig. 4-15a). On the other hand, the negative-rail gate driver common-mode noise was improved during sectors II, IV, and VI, but slightly increased in sectors I, III, and V, as observed in Fig. 4-15b.



(a)



(b)

Figure 4-15. Common-mode current on the gate drive bias supply for (a) the positive-rail gate drivers and (b) the negative-rail gate drivers (with split dc choke).

The fast switching behavior of the SiC JFET generates noise with high frequency content. This noise propagates through common-mode paths via parasitic capacitances to ground. When using the balanced split dc-link choke, much of this noise is contained from the load; the noise must conduct back through the input phase currents and the gate drive power supplies. The negative-rail gate drive power supplies are particularly susceptible to conducting noise. Perhaps this is due to the fact that in addition to the generated common-mode noise, the outputs of the negative-rail isolated power supplies are all at different voltage potentials, whereas the positive-rail isolated supply outputs are all tied together on the positive dc-rail. Overall, the common-mode noise is generally reduced when using the split dc-link choke.

4.3. Conclusions

The SiC JFET buck rectifier has been demonstrated with a 150 kHz switching frequency at the nominal power rating of 2 kVA. Operating waveforms have been shown for both 400 Hz and 800 Hz input line frequency conditions, and the breakdown of converter losses has been given for both conditions. Additionally, the switching behavior of the SiC JFET in the converter has been investigated. It was shown that while the turn-on energy of the SiC JFET agrees well with the two-pulse characterization, the turn-off energy is increased by about a factor of 5. The turn-off energy could be reduced in future designs by a more careful layout of the converter, minimizing parasitics in the path of switched current.

For industry application of this converter, the input filter should be redesigned such that the resonant frequency is much higher than the low-order line harmonics [24]. Additionally, alternative damping methods should be considered for the input filter [22, 23].

Further improvement of the common-mode rejection may be made by utilizing isolated power supplies with lower capacitance between primary and secondary windings. Although there is very little common-mode noise transmitted to the load, a dc choke such as that presented in [25] may be considered. The proposed choke utilizes a pair of differential mode and a pair of common-mode inductor windings on a single E-I type core in order to improve common-mode performance at the dc link.

5. CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

This work has shown the switching characterization of the SiC JFET prototypes fabricated by SiCED for a wise range of operating conditions. The results are suitable for calculating the switching losses of a hard-switching converter. Additionally, the SiC JFET was shown to have higher performance in terms of on-resistance and switching energy as compared to similarly-rated commercially-available Si IGBTs and MOSFETs.

Utilizing the SiC JFETs, a 2 kVA three-phase ac buck rectifier was designed with a switching frequency of 150 kHz. An important modification was made to the charge control method, allowing elimination of phase current transients at the sub-sector changes and simplifying the controller logic. The power stage thermal design was based on loss calculations from the device characterization. Furthermore, the switching behavior of the SiC JFET in the buck rectifier was compared to the results from the two-pulse switching test. It has been observed that the turn-on energy is estimated very closely by the two-pulse test. For the turn-off transient, however, a discrepancy was observed whereby the in-converter switching behavior exhibited 5 times the turn-off energy as compared to the two-pulse test. The increase in turn-off energy was due to the increased parasitics in the buck rectifier circuit, as well as the parasitic capacitance of the series diode used in the buck rectifier.

The SiC JFET buck rectifier has been successfully demonstrated with a rated power of 2 kVA and a switching frequency of 150 kHz. This work has shown that such a converter, though difficult to practically implement using Si power devices, is feasible with the SiC JFET. Loss analysis has been done for the converter at nominal operating conditions, and common-mode noise has been briefly observed.

Improvement can still be made in the input filter. The implemented filter has a resonant peak that is too close to the low-order line harmonics. As such, it is difficult to damp the input filter. For the target application, active damping of the input currents would need to be implemented. Additionally, the gate drive power supplies could be improved. While the commercially-available isolated converters provided a simple solution, custom-made isolated supplies with low

primary-to-secondary capacitance should be used in the future. This would help greatly in reducing common-mode noise through the gate drive bias supply.

5.2. Future Work

Areas for expanding upon this work include switching characterization of the SiC JFET and closed-loop charge control with input current damping. The switching characterization presented was done only up to the known safe current limit of the devices, and only to the highest voltage level that could be realized in the target converter design. If some SiC JFETs can be considered expendable, an investigation should be made into the actual pulsed current capability of the device. This limit may be 2 or 3 times higher than the known safe limit. Additionally, the switched voltage level could be increased to 80% of the rated blocking voltage or higher, as there are no dangerous voltage overshoots at the switching transients.

The future work to be immediately pursued is the increase of switching frequency to the order of 300 to 400 kHz. This range of switching frequency is predicted to be the next optimum point for reduction in input filter size for the target aircraft application.

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APPENDIX I: SIC JFET SWITCHING CHARACTERIZATION DATA

Eon (uJ)

T = 22 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	9.714	15.251	21.094
400	26.091	39.721	55.166
600	46.656	68.471	96.344

Rg = 5 Ω

Id / Vdc	1	3	5
200	9.442	16.064	22.493
400	25.408	41.577	61.033
600	46.267	75.636	112.972

Rg = 10 Ω

Id / Vdc	1	3	5
200	9.519	16.821	25.257
400	25.737	45.529	72.513
600	48.297	84.855	133.61

T = 90 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	9.675	15.46	21.599
400	26.342	40.329	56.524
600	47.184	71.085	99.663

Rg = 5 Ω

Id / Vdc	1	3	5
200	9.584	16.481	23.723
400	26.011	42.349	62.703
600	47.07	75.129	113.254

Rg = 10 Ω

Id / Vdc	1	3	5
200	9.778	17.398	26.403
400	25.962	45.948	72.895
600	47.516	83.953	129.557

Eon (uJ)

T = 125 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	9.745	16.027	22.388
400	26.893	41.657	57.45
600	48.195	71.55	100.889

Rg = 5 Ω

Id / Vdc	1	3	5
200	9.793	16.753	24.44
400	25.921	43.275	65.177
600	47.617	77.783	116.911

Rg = 10 Ω

Id / Vdc	1	3	5
200	9.7	17.498	26.473
400	25.95	46.909	75.476
600	48.051	85.26	133.009

T = 175 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	9.713	16.157	22.838
400	27.008	41.617	59.342
600	48.106	74.108	107.705

Rg = 5 Ω

Id / Vdc	1	3	5
200	9.713	17.023	25.346
400	25.952	44.64	66.775
600	47.918	79.903	123.214

Rg = 10 Ω

Id / Vdc	1	3	5
200	9.776	18.06	29.263
400	26.666	48.201	78.882
600	49.065	87.078	140.381

Eon (uJ)

T = 200 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	9.855	16.417	23.686
400	26.777	42.41	61.981
600	48.652	75.804	109.639

Rg = 5 Ω

Id / Vdc	1	3	5
200	9.784	17.443	26.121
400	26.835	46.027	70.536
600	48.583	82.683	127.438

Rg = 10 Ω

Id / Vdc	1	3	5
200	9.822	18.719	30.466
400	26.942	49.993	82.004
600	49.826	89.939	148.302

Eoff (uJ)

T = 22 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	3.241	3.259	1.71
400	11.12	12.791	11.288
600	21.889	26.212	24.49

Rg = 5 Ω

Id / Vdc	1	3	5
200	3.283	4.907	4.99
400	12.213	17.136	18.552
600	24.002	33.7	36.696

Rg = 10 Ω

Id / Vdc	1	3	5
200	3.91	7.436	8.919
400	14.263	24.005	28.371
600	27.429	44.944	53.189

T = 90 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	2.334	2.145	1.149
400	7.749	9.19	8.791
600	15.694	18.667	18.323

Rg = 5 Ω

Id / Vdc	1	3	5
200	2.319	3.311	3.476
400	7.785	12.025	14.061
600	15.726	23.174	26.624

Rg = 10 Ω

Id / Vdc	1	3	5
200	2.507	4.647	6.321
400	8.128	15.343	21.274
600	16.313	29.616	38.69

Eoff (uJ)

T = 125 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	2.438	2.004	1.335
400	7.933	8.582	8.255
600	15.985	17.844	17.756

Rg = 5 Ω

Id / Vdc	1	3	5
200	2.377	2.929	2.948
400	7.857	10.771	12.543
600	15.919	20.813	24.878

Rg = 10 Ω

Id / Vdc	1	3	5
200	2.492	4.062	5.419
400	8.13	13.405	18.686
600	16.051	25.224	33.558

T = 175 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	2.421	1.885	1.328
400	7.678	7.769	7.397
600	15.816	16.604	16.785

Rg = 5 Ω

Id / Vdc	1	3	5
200	2.389	2.582	2.583
400	7.765	8.965	10.357
600	15.928	18.581	21.857

Rg = 10 Ω

Id / Vdc	1	3	5
200	2.43	3.542	4.638
400	7.91	11.121	14.59
600	16.058	21.564	28.685

Eoff (uJ)

T = 200 °C

Rg = 1 Ω

Id / Vdc	1	3	5
200	2.415	1.967	1.365
400	8.243	7.954	7.36
600	16.238	16.928	16.925

Rg = 5 Ω

Id / Vdc	1	3	5
200	2.429	2.614	2.546
400	7.946	9.079	10.289
600	16.182	18.909	21.582

Rg = 10 Ω

Id / Vdc	1	3	5
200	2.48	3.467	4.286
400	8.213	11.155	14.121
600	16.275	21.668	27.893

APPENDIX II: BUCK RECTIFIER POWER STAGE AND CONTROLLER SCHEMATICS

A. Power Stage

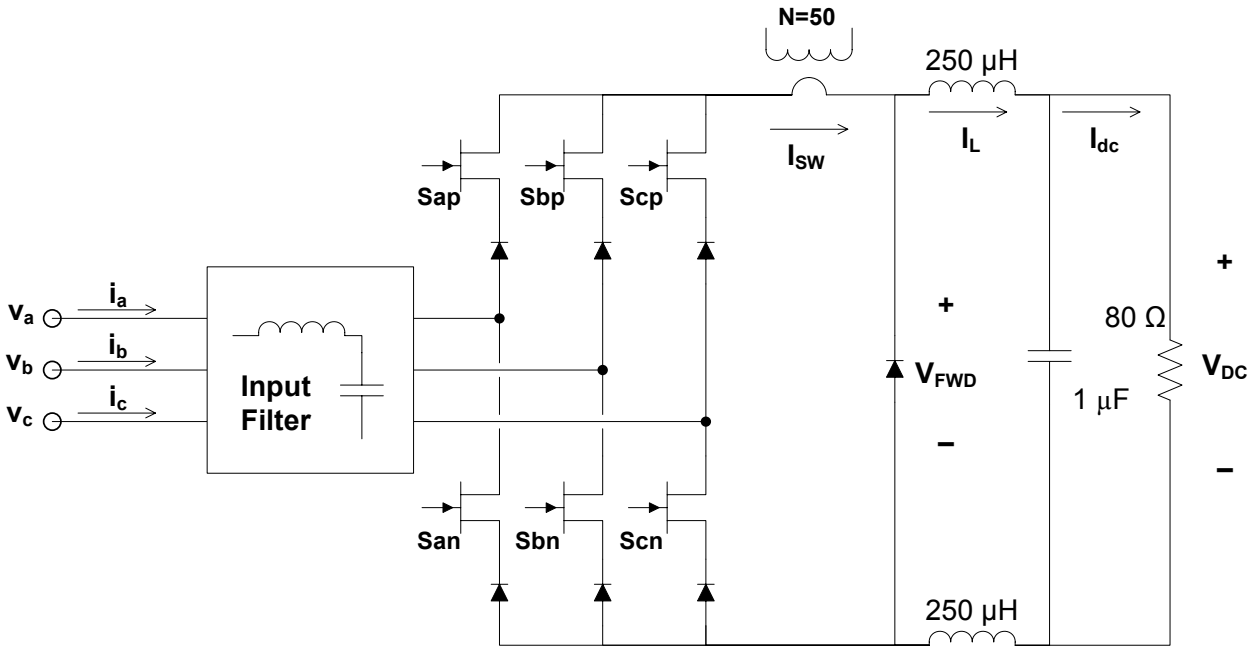

Figure A-1. Power stage schematic.

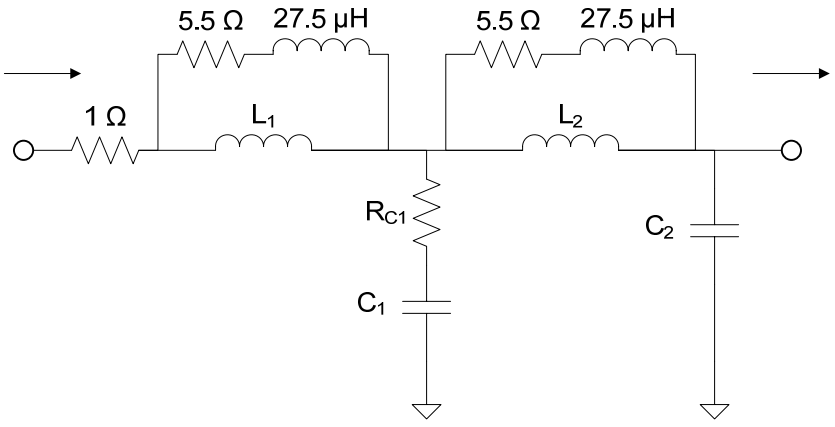

Figure A-2. Input filter for a single phase including damping networks.

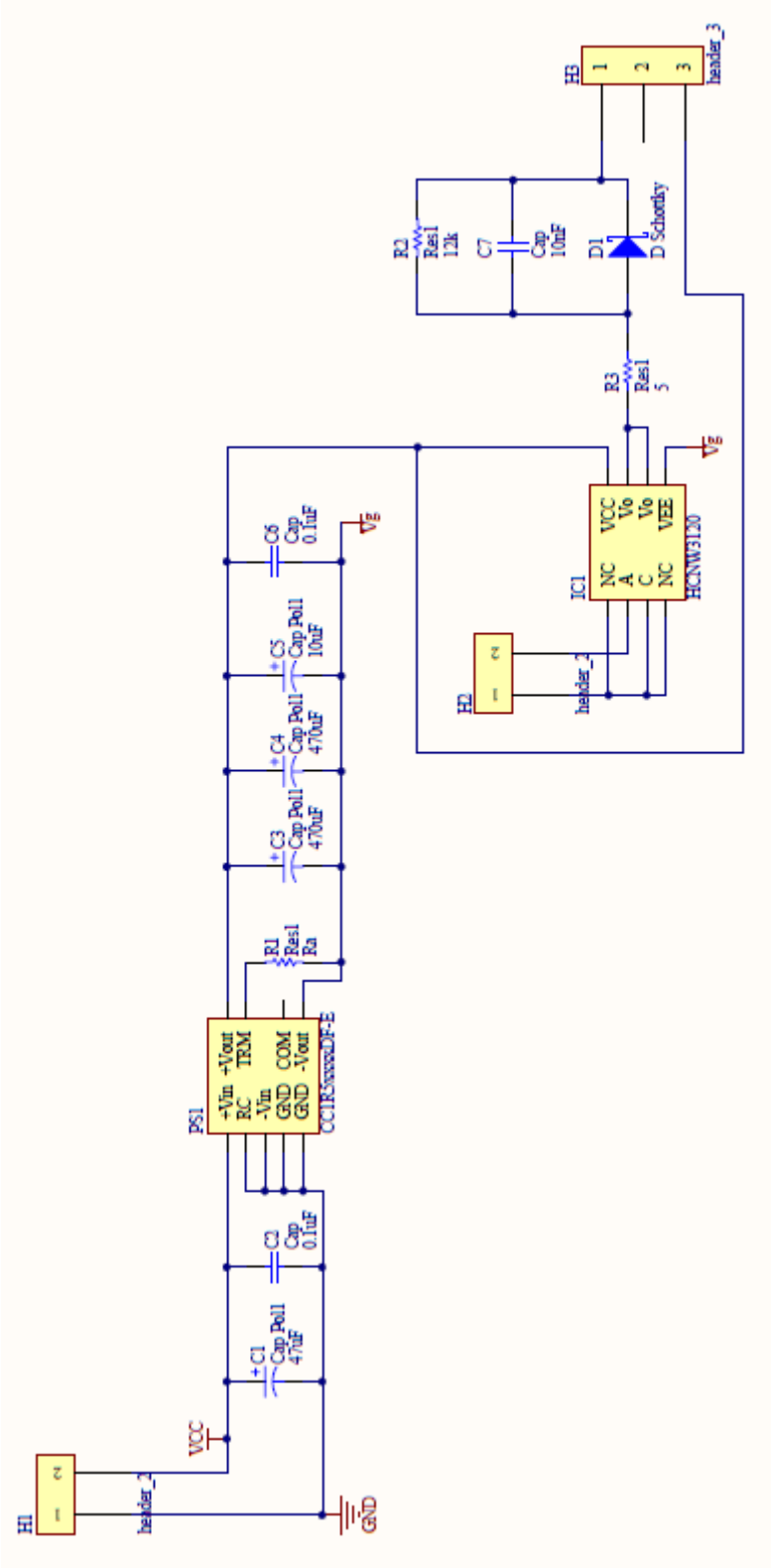

Figure A-3. Gate drive module for the SiC JFET.

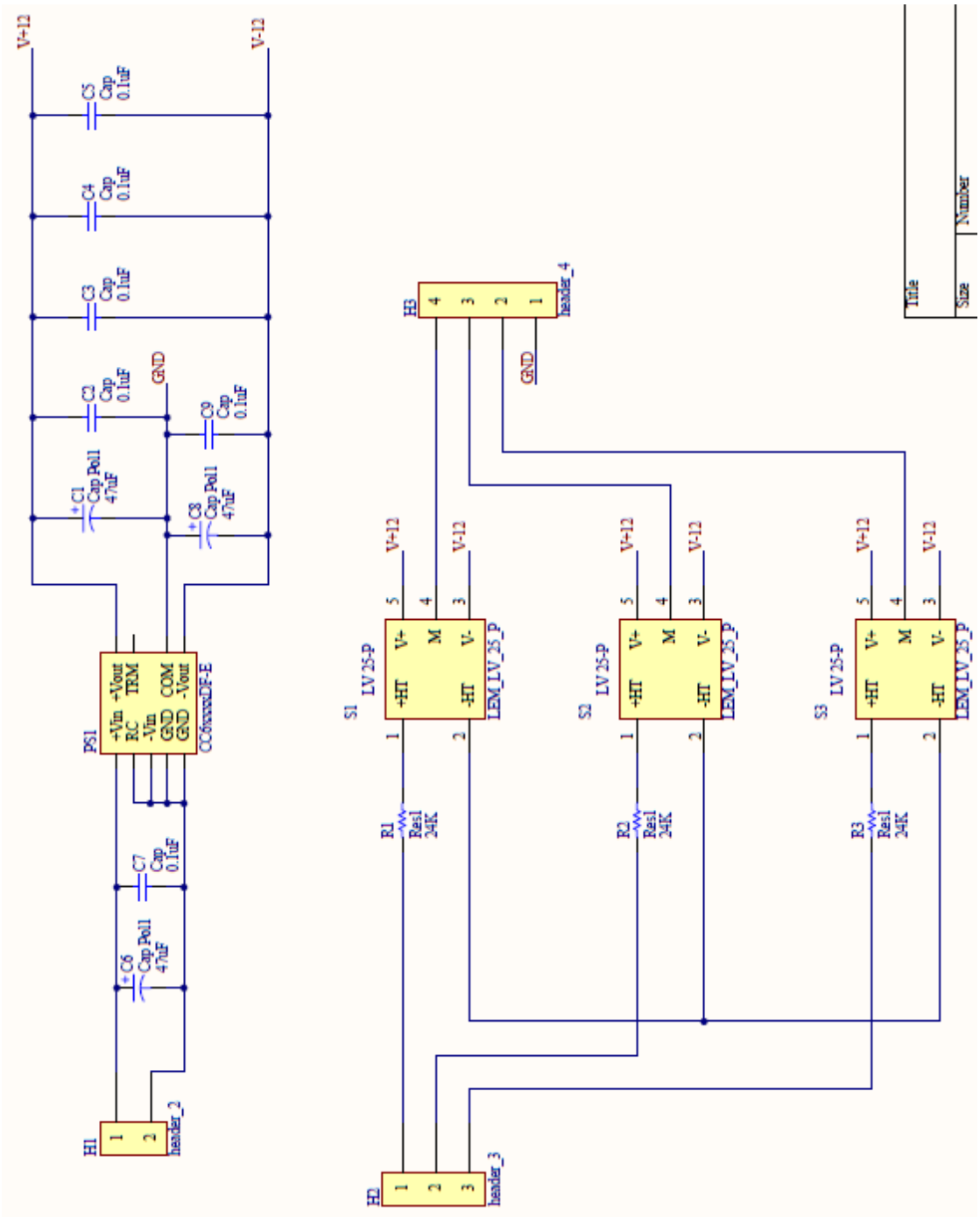

Figure A-4. Voltage sensor board for sensing phase voltages at power stage terminals.

B. Controller

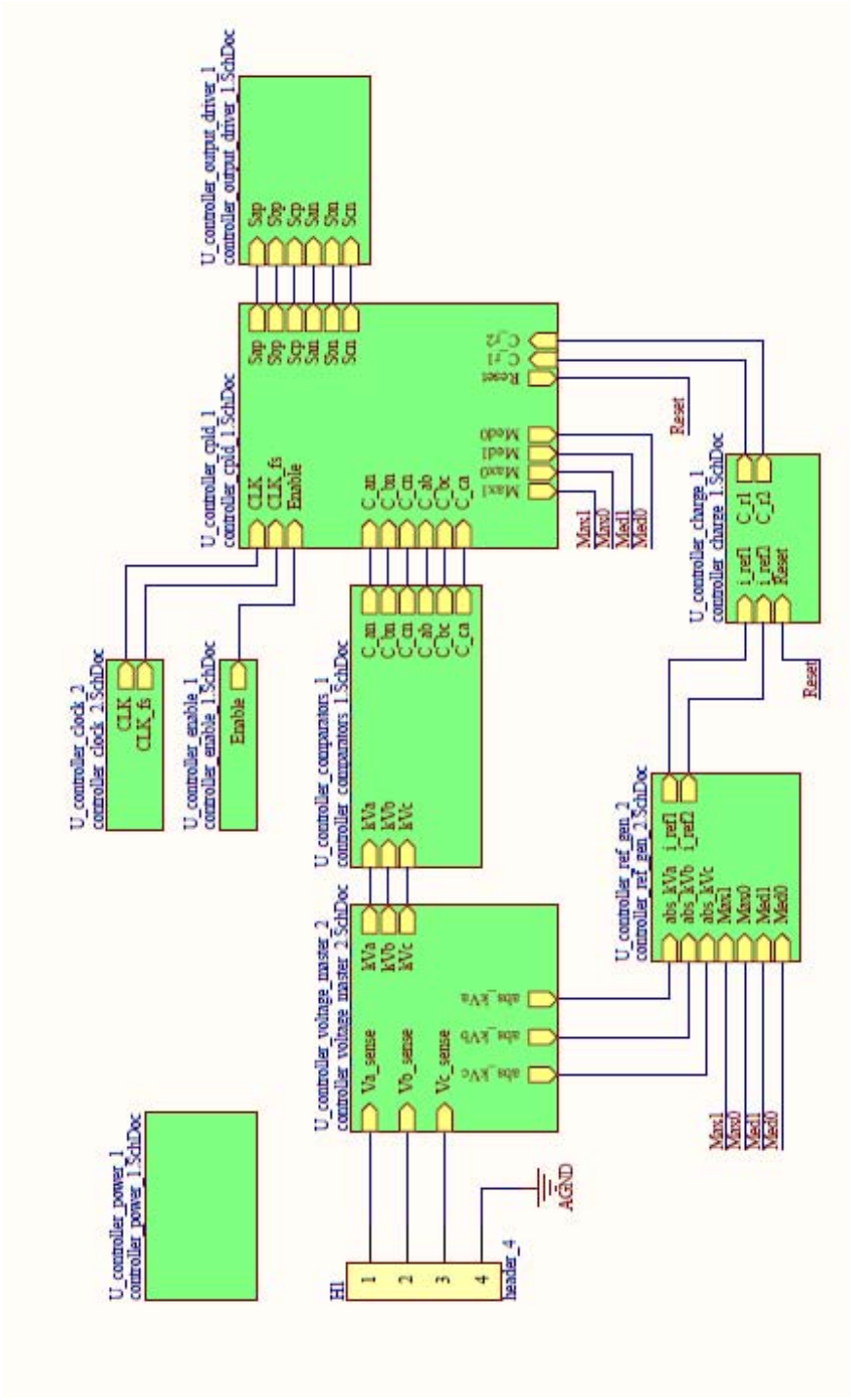

Figure A-5. Controller top-level schematic.

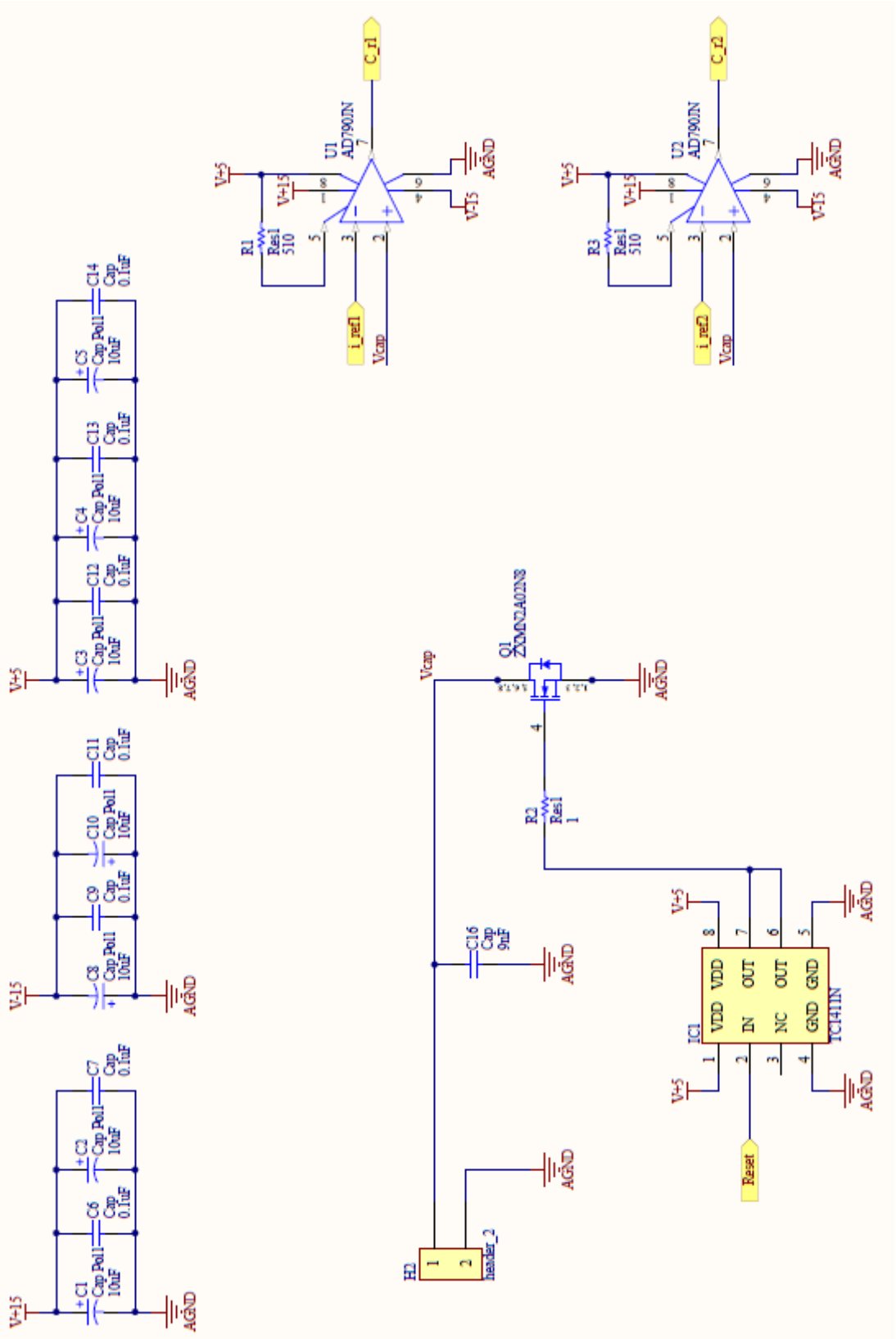

Figure A-6. Charge controller.

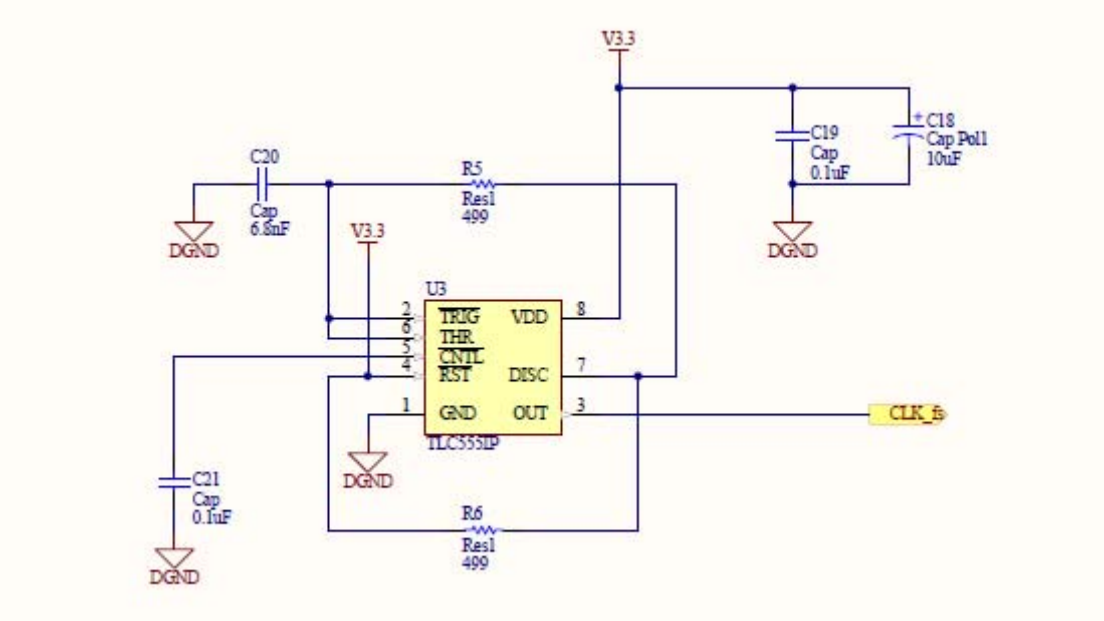

Figure A-7. Switching frequency clock generator.

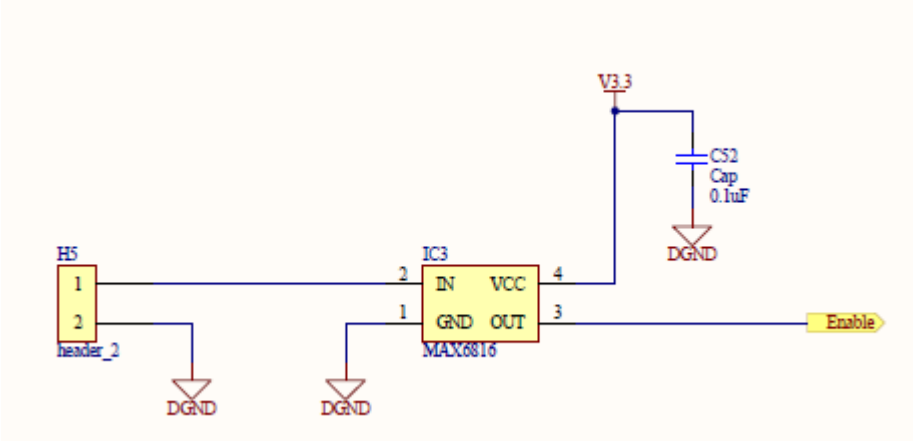

Figure A-8. Controller enable switch de-bouncer.

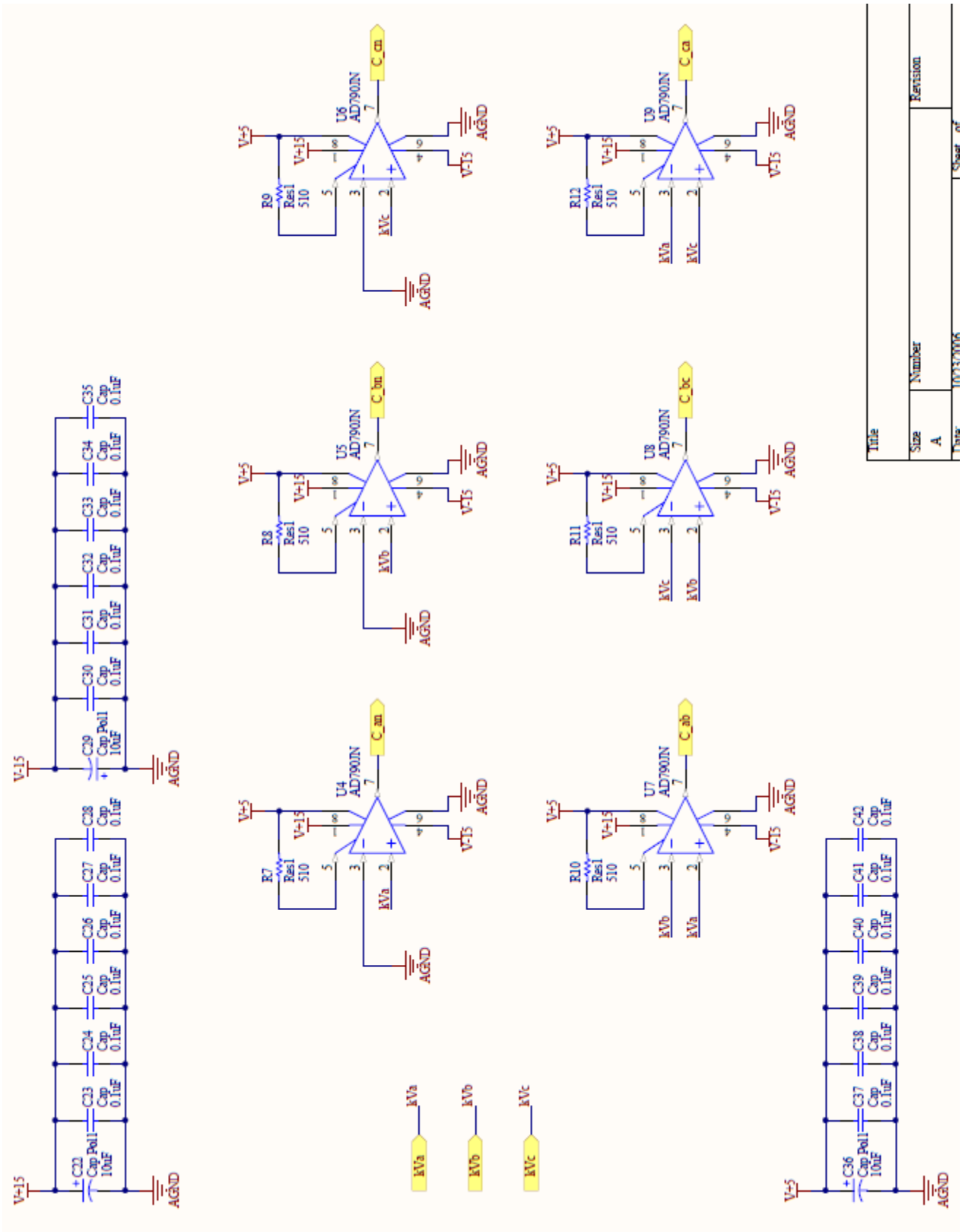

Figure A-9. Comparators for sensing input line sector.

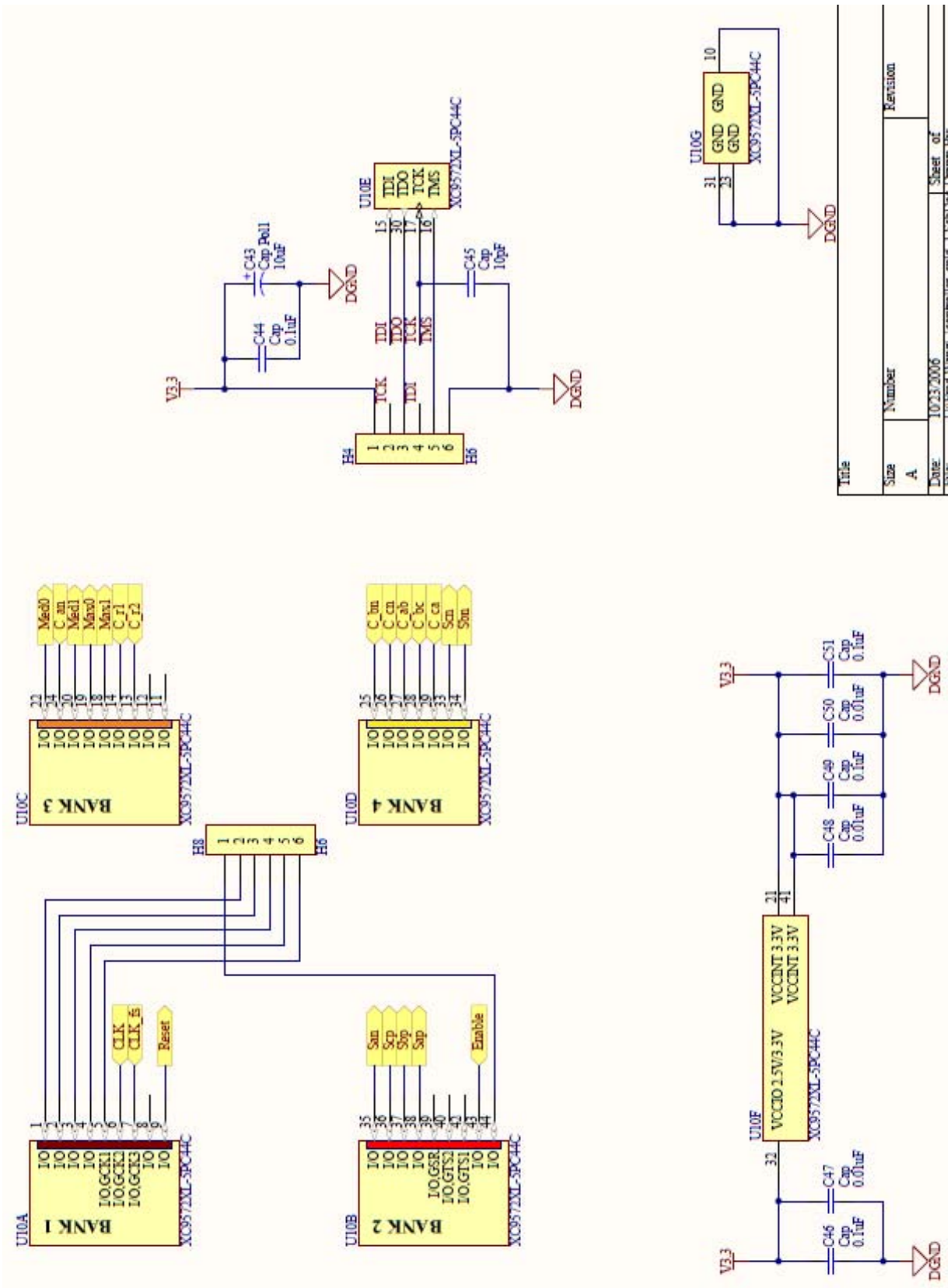

Figure A-10. Xilinx XC9572XL complex programmable logic device.

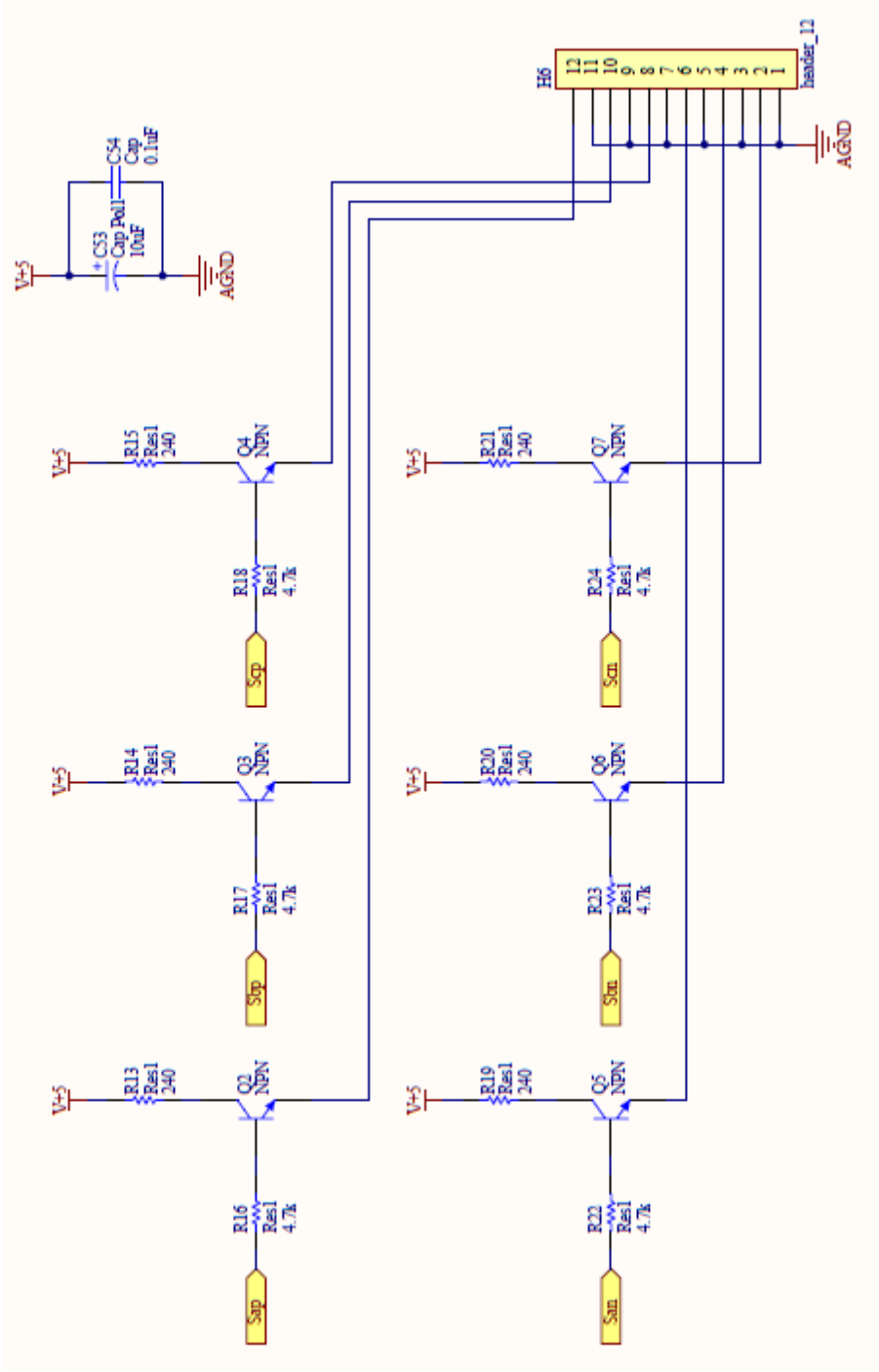

Figure A-11. Gate signal output to gate drive modules.

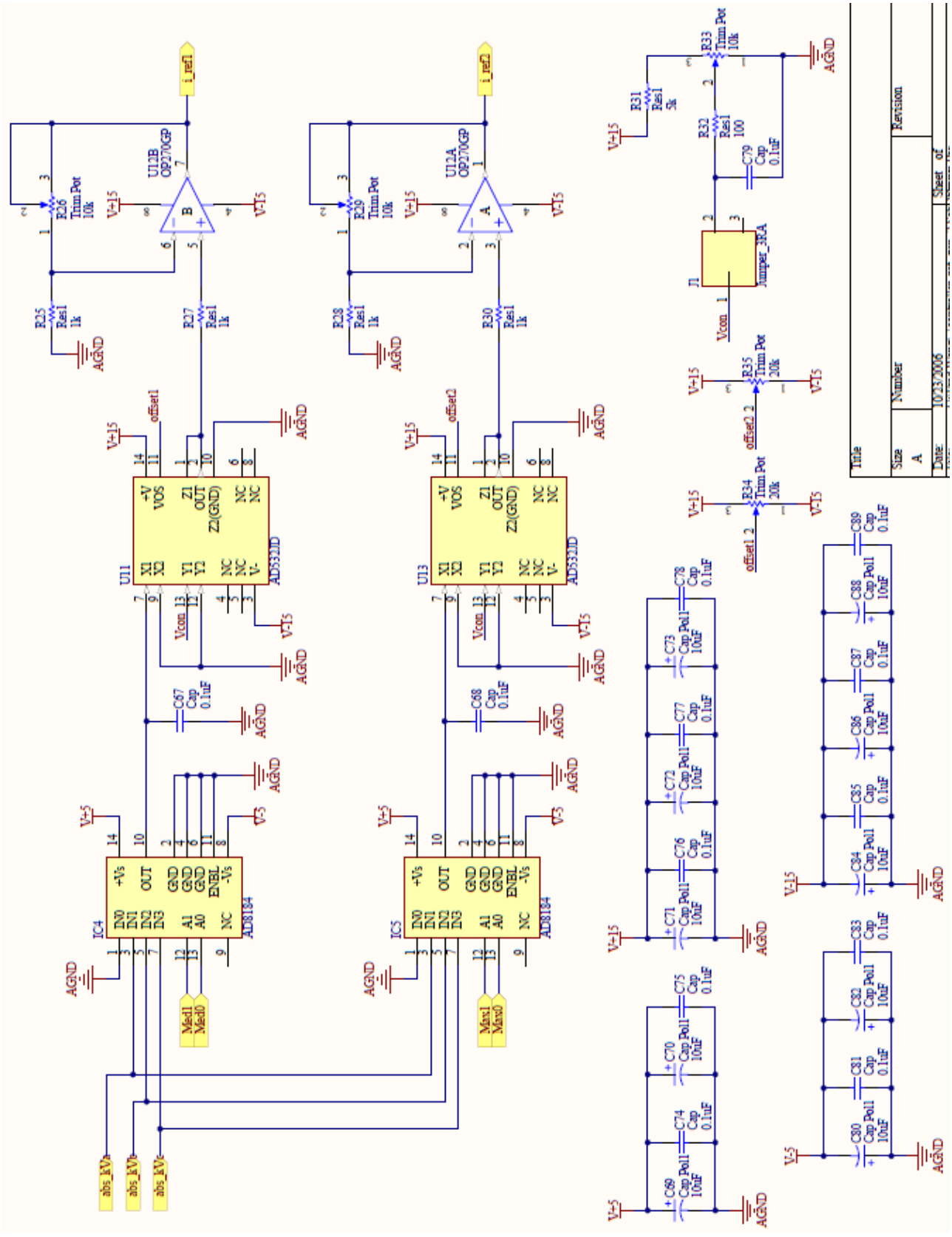

Figure A-12. Reference generation and analog multiplexer circuit.

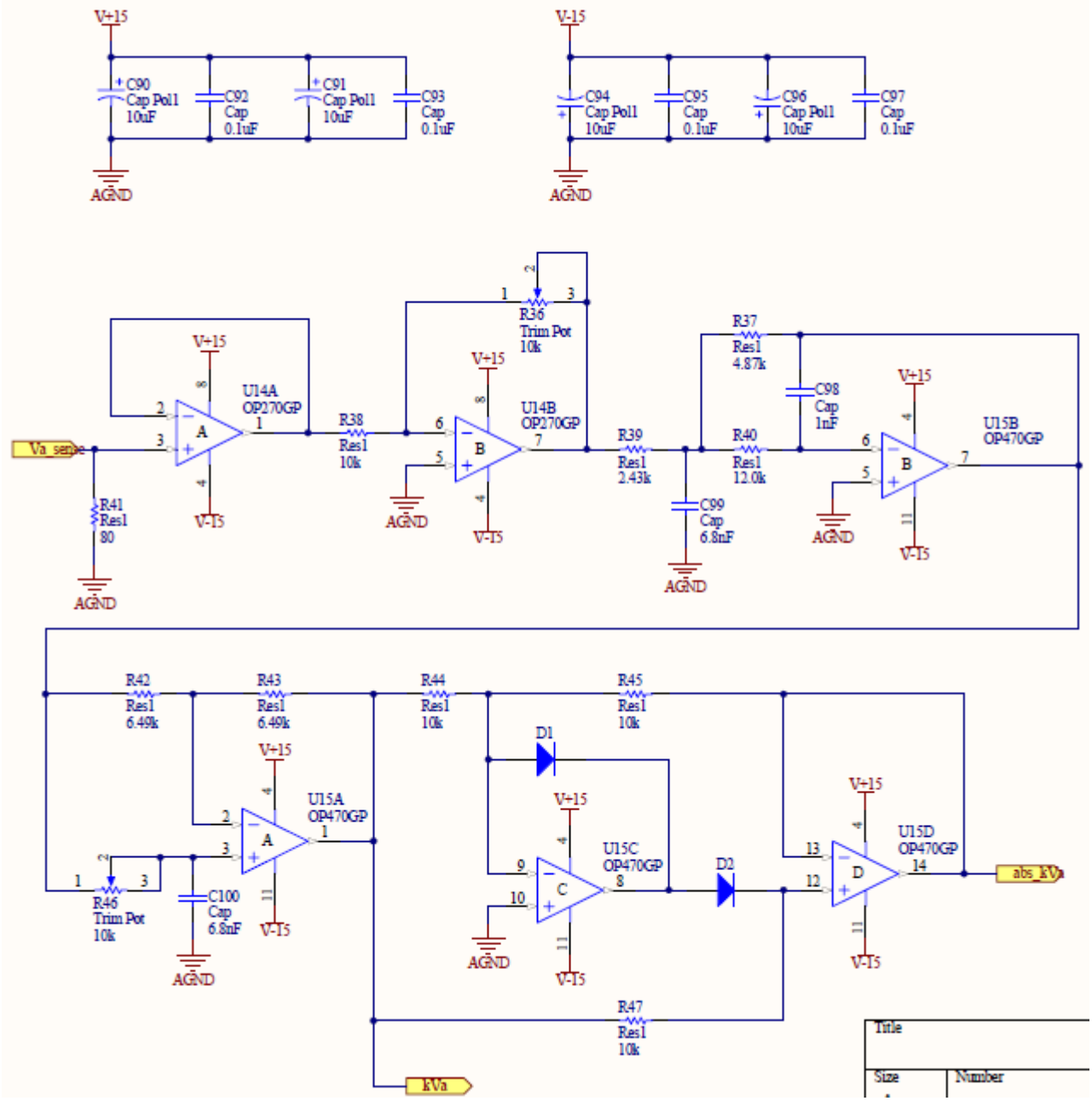

Figure A-13. Signal conditioning and absolute value for a single sensed phase voltage.

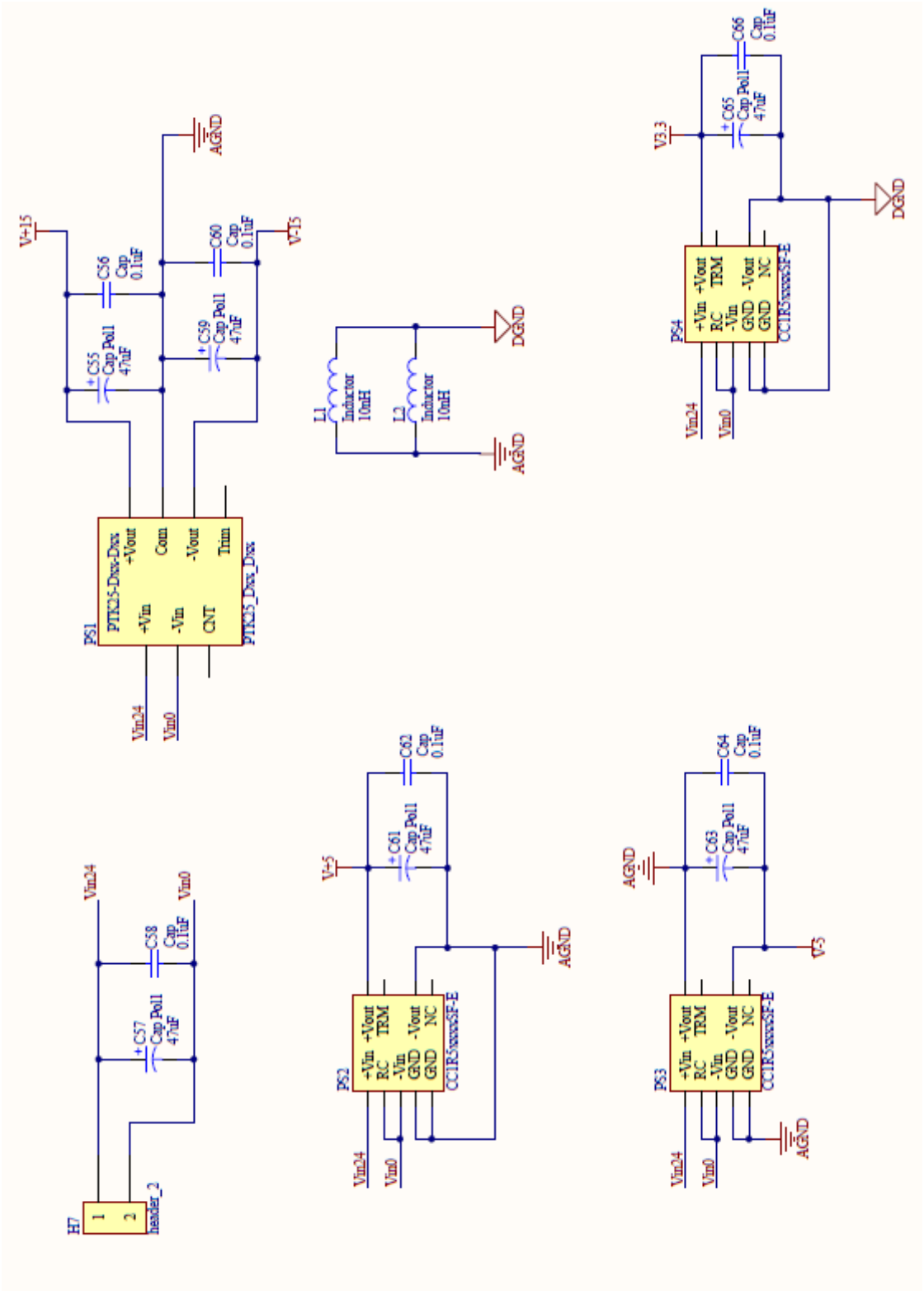

Figure A-14. Power supplies for controller board.

APPENDIX III: VHDL CODE FOR CONTROLLER

A. Original Charge Control

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    15:57:51 10/14/2006
-- Design Name:
-- Module Name:    charge_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- 11-01-2006 -- changed code such that comparator inputs are not latched, but
--               instead, the seg_id is latched.  this way each block can choose
--               to use latched seg_id or not.
--
-- 12-18-2006 -- modified to get rid of forced zero vector.
--
-- 12-22-2006 -- modified to turn ON complementary switch during zero vector.
--
-- 12-28-2006 -- modified to turn OFF all switches during zero vector.
--
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
--use IEEE.STD_LOGIC_ARITH.ALL;
--use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity charge_1 is
    Port ( Aux1 : inout  STD_LOGIC;
           Aux2 : inout  STD_LOGIC;
           Aux3 : inout  STD_LOGIC;
           Aux4 : inout  STD_LOGIC;
           Aux5 : inout  STD_LOGIC;
           Aux6 : inout  STD_LOGIC;
           C_an : in  STD_LOGIC;
           C_bn : in  STD_LOGIC;
           C_cn : in  STD_LOGIC;
           C_ab : in  STD_LOGIC;
           C_bc : in  STD_LOGIC;
           C_ca : in  STD_LOGIC;
           C_r1 : in  STD_LOGIC;
           C_r2 : in  STD_LOGIC;
           CLK : in  STD_LOGIC;
```

```
--           HSCLK : in  STD_LOGIC;
           Enable : in  STD_LOGIC;
           Max0 : out  STD_LOGIC;
           Max1 : out  STD_LOGIC;
           Med0 : out  STD_LOGIC;
           Med1 : out  STD_LOGIC;
           Reset : out  STD_LOGIC;
           Sap : out  STD_LOGIC;
           Sbp : out  STD_LOGIC;
           Scp : out  STD_LOGIC;
           San : out  STD_LOGIC;
           Sbn : out  STD_LOGIC;
           Scn : out  STD_LOGIC);
end charge_1;

architecture Behavioral of charge_1 is
    signal seg_id, seg_id_latch: STD_LOGIC_VECTOR(3 downto 0);
--  signal Ap, Bp, Cp, An, Bn, Cn: STD_LOGIC_VECTOR(3 downto 0);
    signal Ap, Bp, Cp, An, Bn, Cn: STD_LOGIC_VECTOR(2 downto 0);
    signal G1, G2, G3: STD_LOGIC;
    signal MedMax: STD_LOGIC_VECTOR(3 downto 0);
    signal A, B, C, D, E, F: STD_LOGIC;
    signal ABC: STD_LOGIC_VECTOR(11 downto 0);
    signal G2_temp: STD_LOGIC;
    signal Reset_temp: STD_LOGIC;
    signal flag, flag_temp: STD_LOGIC;
--  signal screwy: STD_LOGIC;   --using this to identify the sectors messing up
--  signal Sbn_temp, Scn_temp: STD_LOGIC;

begin

--Output signals for debugging
Aux1 <= seg_id(1);
Aux2 <= seg_id(2);
Aux3 <= seg_id(3);
Aux4 <= C_r2;
Aux5 <= flag_temp;
Aux6 <= flag;


--set "screwy" signal to high during sectors I, III, IV
--screwy <= '1' when seg_id_latch(3 downto 1) = "000" or
--                    seg_id_latch(3 downto 1) = "010" or
--                    seg_id_latch(3 downto 1) = "100"
--                    else '0';

--Keep old signals from original code (previously these were latched)
A <= C_an;
B <= C_bn;
C <= C_cn;
D <= C_ab;
E <= C_bc;
F <= C_ca;

--**Block 1: Segment Identification**--
seg_id(3) <= not B and C;
seg_id(2) <= not A and B;
seg_id(1) <= ( A and B and not C ) or
                ( A and not B and C ) or
                ( not A and B and C );
seg_id(0) <= ( A and not B and C and D and not E and not F ) or
                ( not A and not B and C and D and not E and F ) or
                ( not A and B and C and not D and not E and F ) or
```

```
                ( not A and B and not C and not D and E and F ) or
                ( A and B and not C and not D and E and not F ) or
                ( A and not B and not C and D and E and not F );

--create latched copy of seg_id
process (CLK) is
begin
    if (rising_edge(CLK)) then
        seg_id_latch(3 downto 0) <= seg_id(3 downto 0);
    end if;
end process;

--end of Block 1


--**Block 2: Multiplexer Select (Max/Med)**--
--Lookup Table
process(seg_id) is
begin
    case (seg_id) is
        when X"0" => MedMax <= "1001";
        when X"1" => MedMax <= "1101";
        when X"2" => MedMax <= "0111";
        when X"3" => MedMax <= "1011";
        when X"4" => MedMax <= "1110";
        when X"5" => MedMax <= "0110";
        when X"6" => MedMax <= "1001";
        when X"7" => MedMax <= "1101";
        when X"8" => MedMax <= "0111";
        when X"9" => MedMax <= "1011";
        when X"A" => MedMax <= "1110";
        when X"B" => MedMax <= "0110";
        when others => MedMax <= "0000";
    end case;
end process;

--Output Med and Max values
Med1 <= MedMax(3);
Med0 <= MedMax(2);
Max1 <= MedMax(1);
Max0 <= MedMax(0);

--end of Block 2


--**Block 3: Charge Controller**--

--Define signal G1
process (CLK, C_r1) is
begin
    if (C_r1 = '1') then
        G1 <= '0';
    elsif (rising_edge(CLK)) then
        G1 <= '1';
    end if;
end process;

--Define signal G2_temp
process (CLK, C_r2) is
begin
    if (C_r2 = '1') then
        G2_temp <= '0';
    elsif (rising_edge(CLK)) then
```

```
        G2_temp <= '1';
    end if;
end process;

--Define signal Reset_temp
process (CLK, C_r2) is
begin
    if (C_r2 = '1') then
        Reset_temp <= '1';
    elsif (rising_edge(CLK)) then
        Reset_temp <= '0';
    end if;
end process;

--Define signal G2
G2 <= C_r1 and not C_r2 and G2_temp;

--Define signal G3
--G3 <= Reset_temp;

--Set flag_temp at beginning of each switching period,
--but clear when Reset becomes active
process (CLK, C_r2) is
begin
    if (C_r2 = '1') then
        flag_temp <= '0';
    elsif (rising_edge(CLK)) then
        flag_temp <= not flag_temp;
    end if;
end process;

--Set flag for 1 switching period if reset_temp
--has not become active in the previous period
--flag <= '0';
process (CLK) is
begin
    if (rising_edge(CLK)) then
        flag <= flag_temp;
    end if;
end process;

--Assign Reset based on Enable
--with Enable select
--  Reset <= Reset_temp when '1',
--              '1' when others;

--Reset <= Reset_temp or flag;  --commented 12/18/2006
Reset <= Reset_temp;



--end of Block 3


--**Block 4: Gate Signal Distribution**--

--Designates switch that is always on in a switching period
--Use either latched or unlatched seg_id, depending on signal used
Ap(0) <= '1' when seg_id_latch(3 downto 1) = "000" else '0';
Bp(0) <= '1' when seg_id_latch(3 downto 1) = "010" else '0';
Cp(0) <= '1' when seg_id_latch(3 downto 1) = "100" else '0';
An(0) <= '1' when seg_id_latch(3 downto 1) = "011" else '0';
Bn(0) <= '1' when seg_id_latch(3 downto 1) = "101" else '0';
```

```
Cn(0) <= '1' when seg_id_latch(3 downto 1) = "001" else '0';

--Designates switch that turns on to apply zero vector in a given sector
--Ap(3) <= '1' when seg_id_latch(3 downto 1) = "011" else '0';
--Bp(3) <= '1' when seg_id_latch(3 downto 1) = "101" else '0';
--Cp(3) <= '1' when seg_id_latch(3 downto 1) = "001" else '0';
--An(3) <= '1' when seg_id_latch(3 downto 1) = "000" else '0';
--Bn(3) <= '1' when seg_id_latch(3 downto 1) = "010" else '0';
--Cn(3) <= '1' when seg_id_latch(3 downto 1) = "100" else '0';

--Designates switches 1 and 2 in a switching period
process(seg_id_latch) is
begin
    case (seg_id_latch) is
        when X"0" => ABC <= "000000000110";
        when X"1" => ABC <= "000000001001";
        when X"2" => ABC <= "011000000000";
        when X"3" => ABC <= "100100000000";
        when X"4" => ABC <= "000000100001";
        when X"5" => ABC <= "000000010010";
        when X"6" => ABC <= "000110000000";
        when X"7" => ABC <= "001001000000";
        when X"8" => ABC <= "000000011000";
        when X"9" => ABC <= "000000100100";
        when X"A" => ABC <= "100001000000";
        when X"B" => ABC <= "010010000000";
        when others => ABC <= "000000000000";
    end case;
end process;
--breakout vector ABC
Ap(2 downto 1) <= ABC(11 downto 10);
Bp(2 downto 1) <= ABC(9 downto 8);
Cp(2 downto 1) <= ABC(7 downto 6);
An(2 downto 1) <= ABC(5 downto 4);
Bn(2 downto 1) <= ABC(3 downto 2);
Cn(2 downto 1) <= ABC(1 downto 0);

--Output Gate Signals
--Enable will enable or disable outputs
--Sap <= ( Ap(0) or (Ap(1) and G1) or (Ap(2) and G2) or (Ap(3) and G3) ) and Enable;
--Sbp <= ( Bp(0) or (Bp(1) and G1) or (Bp(2) and G2) or (Bp(3) and G3) ) and Enable;
--Scp <= ( Cp(0) or (Cp(1) and G1) or (Cp(2) and G2) or (Cp(3) and G3) ) and Enable;
--San <= ( An(0) or (An(1) and G1) or (An(2) and G2) or (An(3) and G3) ) and Enable;
--Sbn <= ( Bn(0) or (Bn(1) and G1) or (Bn(2) and G2) or (Bn(3) and G3) ) and Enable;
--Scn <= ( Cn(0) or (Cn(1) and G1) or (Cn(2) and G2) or (Cn(3) and G3) ) and Enable;

Sap <= ( Ap(0) or (Ap(1) and G1) or (Ap(2) and G2) ) and Enable and not reset_temp;
Sbp <= ( Bp(0) or (Bp(1) and G1) or (Bp(2) and G2) ) and Enable and not reset_temp;
Scp <= ( Cp(0) or (Cp(1) and G1) or (Cp(2) and G2) ) and Enable and not reset_temp;
San <= ( An(0) or (An(1) and G1) or (An(2) and G2) ) and Enable and not reset_temp;
Sbn <= ( Bn(0) or (Bn(1) and G1) or (Bn(2) and G2) ) and Enable and not reset_temp;
Scn <= ( Cn(0) or (Cn(1) and G1) or (Cn(2) and G2) ) and Enable and not reset_temp;

--end of Block 4


end Behavioral;
```

B. Improved Charge Control to Eliminate Sub-Sector Transients

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    15:57:51 10/14/2006
-- Design Name:
-- Module Name:    charge_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- 11-01-2006 -- changed code such that comparator inputs are not latched, but
--               instead, the seg_id is latched.  this way each block can choose
--               to use latched seg_id or not.
--
-- 12-18-2006 -- modified to get rid of forced zero vector.
--
-- 12-22-2006 -- modified to turn ON complementary switch during zero vector.
--
-- 12-28-2006 -- modified to turn OFF all switches during zero vector.
--
--  01-28-2007 -- modified to change reference generation to eliminate transients
--
--  02-07-2007 -- now, CLK will be 8*fs. At sector change, comparator trips ignored
--                    for first 8*fs clock immediately following sector
--
--
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
--use IEEE.STD_LOGIC_ARITH.ALL;
--use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity charge_1 is
    Port ( Aux1 : inout  STD_LOGIC;
           Aux2 : inout  STD_LOGIC;
           Aux3 : inout  STD_LOGIC;
           Aux4 : inout  STD_LOGIC;
           Aux5 : inout  STD_LOGIC;
           Aux6 : inout  STD_LOGIC;
           C_an, C_bn, C_cn : in STD_LOGIC;
--           C_ab, C_bc, C_ca : in STD_LOGIC;
           C_r1, C_r2 : in  STD_LOGIC;
           CLK : in  STD_LOGIC;
--           HSCLK : in  STD_LOGIC;
           Enable : in  STD_LOGIC;
```

```
           Max0, Max1, Med0, Med1 : out  STD_LOGIC;
           Reset : out  STD_LOGIC;
           Sap, Sbp, Scp, San, Sbn, Scn : out  STD_LOGIC);
end charge_1;

architecture Behavioral of charge_1 is
    signal seg_id, seg_id_latch: STD_LOGIC_VECTOR(3 downto 1);
--  signal Ap, Bp, Cp, An, Bn, Cn: STD_LOGIC_VECTOR(3 downto 0);
    signal Ap, Bp, Cp, An, Bn, Cn: STD_LOGIC_VECTOR(2 downto 0);
    signal G1, G2, G3: STD_LOGIC;
    signal MedMax: STD_LOGIC_VECTOR(3 downto 0);
    signal A, B, C: STD_LOGIC;
--  signal D, E, F: STD_LOGIC;
    signal ABC: STD_LOGIC_VECTOR(11 downto 0);
    signal G1_temp, G2_temp: STD_LOGIC;
    signal sect_flag, Reset_temp: STD_LOGIC;
    signal flag, flag_temp: STD_LOGIC;
    signal CLKd2, CLKd4, CLKd8: STD_LOGIC;
    signal sect_edge: STD_LOGIC_VECTOR(1 downto 0);
    signal C_r1_temp: STD_LOGIC;
--  signal Sbn_temp, Scn_temp: STD_LOGIC;

--define state variables
--type

begin

--Output signals for debugging
Aux1 <= CLKd8;
Aux2 <= seg_id_latch(1);
Aux3 <= C_r1;
Aux4 <= G1_temp;
Aux5 <= sect_flag;
Aux6 <= G1;


--Keep old signals from original code (previously these were latched)
A <= C_an;
B <= C_bn;
C <= C_cn;
--D <= C_ab;
--E <= C_bc;
--F <= C_ca;

--**Block 1: Segment Identification**--
seg_id(3) <= not B and C;
seg_id(2) <= not A and B;
seg_id(1) <= ( A and B and not C ) or
                ( A and not B and C ) or
                ( not A and B and C );
--seg_id(0) <= '0';

--Generate CLKd2
process (CLK) is
begin
    if (rising_edge(CLK)) then
        CLKd2 <= not CLKd2;
    end if;
end process;

--Generate CLKd4
process (CLKd2) is
begin
```

```
    if (rising_edge(CLKd2)) then
        CLKd4 <= not CLKd4;
    end if;
end process;

--Generate CLKd8
process (CLKd4) is
begin
    if (rising_edge(CLKd4)) then
        CLKd8 <= not CLKd8;
    end if;
end process;

--create latched copy of seg_id
process (CLKd8) is
begin
    if (rising_edge(CLKd8)) then
        seg_id_latch(3 downto 1) <= seg_id(3 downto 1);
    end if;
end process;

--end of Block 1


--**Block 2: Multiplexer Select (Max/Med)**--
--Lookup Table
process(seg_id_latch) is
begin
    case (seg_id_latch) is
        when "000" => MedMax <= "1001";
        when "001" => MedMax <= "0111";
        when "010" => MedMax <= "1110";
        when "011" => MedMax <= "1001";
        when "100" => MedMax <= "0111";
        when "101" => MedMax <= "1110";
        when others => MedMax <= "0000";
    end case;
end process;

--Output Med and Max values
Med1 <= MedMax(3);
Med0 <= MedMax(2);
Max1 <= MedMax(1);
Max0 <= MedMax(0);

--end of Block 2


--**Block 3: Charge Controller**--

--Define signal G1
--G1 is held on for first 8*fs (CLK) after sector change
--so, sect_flag should be high for first 8*fs clock after sector change
--process(CLK) is
--begin
--  if (rising_edge(CLK)) then
--      sect_edge(0) <= seg_id_latch(1);
--  end if;
--end process;

--because CLKd8 is derived from CLK, it is slightly lagging
--so sect_edge(0) is loaded by CLK, which will be the old sector bit
--and sect_edge(1) is loaded by CLKd8, which will be the new sector bit
```

```
--process(CLKd8) is
--begin
--  if (rising_edge(CLKd8)) then
--      sect_edge(1) <= seg_id_latch(1);
--  end if;
--end process;


--new theory: load old sector with CLK, and new sector triggered by the bit itself
process(CLK) is
begin
    if (rising_edge(CLK)) then
        sect_edge(1) <= seg_id_latch(1);
    end if;
end process;

sect_edge(0) <= seg_id_latch(1);


sect_flag <= '1' when sect_edge = "01" or sect_edge = "10" else '0';

C_r1_temp <= C_r1 and not sect_flag;

process (CLKd8, C_r1_temp) is
begin
    if (C_r1_temp = '1') then
        G1 <= '0';
    elsif (rising_edge(CLKd8)) then
        G1 <= '1';
    end if;
end process;

--Define signal G2_temp
process (CLKd8, C_r2) is
begin
    if (C_r2 = '1') then
        G2_temp <= '0';
    elsif (rising_edge(CLKd8)) then
        G2_temp <= '1';
    end if;
end process;

--Define signal Reset_temp
process (CLKd8, C_r2) is
begin
    if (C_r2 = '1') then
        Reset_temp <= '1';
    elsif (rising_edge(CLKd8)) then
        Reset_temp <= '0';
    end if;
end process;

--Define signal G2
--G2 <= C_r1 and not C_r2 and G2_temp;
G2 <= NOT G1 and not C_r2 and G2_temp;

--Define signal G3
--G3 <= Reset_temp;

--Set flag_temp at beginning of each switching period,
--but clear when Reset becomes active
process (CLKd8, C_r2) is
begin
```

```
    if (C_r2 = '1') then
        flag_temp <= '0';
    elsif (rising_edge(CLKd8)) then
        flag_temp <= not flag_temp;
    end if;
end process;

--Set flag for 1 switching period if reset_temp
--has not become active in the previous period
--flag <= '0';
process (CLKd8) is
begin
    if (rising_edge(CLKd8)) then
        flag <= flag_temp;
    end if;
end process;

--Assign Reset based on Enable
--with Enable select
--  Reset <= Reset_temp when '1',
--              '1' when others;

--Reset <= Reset_temp or flag;  --commented 12/18/2006
Reset <= Reset_temp;



--end of Block 3


--**Block 4: Gate Signal Distribution**--

--Designates switch that is always on in a switching period
--Use either latched or unlatched seg_id, depending on signal used
Ap(0) <= '1' when seg_id_latch(3 downto 1) = "000" else '0';
Bp(0) <= '1' when seg_id_latch(3 downto 1) = "010" else '0';
Cp(0) <= '1' when seg_id_latch(3 downto 1) = "100" else '0';
An(0) <= '1' when seg_id_latch(3 downto 1) = "011" else '0';
Bn(0) <= '1' when seg_id_latch(3 downto 1) = "101" else '0';
Cn(0) <= '1' when seg_id_latch(3 downto 1) = "001" else '0';

--Designates switch that turns on to apply zero vector in a given sector
--Ap(3) <= '1' when seg_id_latch(3 downto 1) = "011" else '0';
--Bp(3) <= '1' when seg_id_latch(3 downto 1) = "101" else '0';
--Cp(3) <= '1' when seg_id_latch(3 downto 1) = "001" else '0';
--An(3) <= '1' when seg_id_latch(3 downto 1) = "000" else '0';
--Bn(3) <= '1' when seg_id_latch(3 downto 1) = "010" else '0';
--Cn(3) <= '1' when seg_id_latch(3 downto 1) = "100" else '0';

--Designates switches 1 and 2 in a switching period
process(seg_id_latch) is
begin
    case (seg_id_latch) is
        when "000" => ABC <= "000000000110";
        when "001" => ABC <= "011000000000";
        when "010" => ABC <= "000000100001";
        when "011" => ABC <= "000110000000";
        when "100" => ABC <= "000000011000";
        when "101" => ABC <= "100001000000";
        when others => ABC <= "000000000000";
    end case;
end process;
--breakout vector ABC
```

```
Ap(2 downto 1) <= ABC(11 downto 10);
Bp(2 downto 1) <= ABC(9 downto 8);
Cp(2 downto 1) <= ABC(7 downto 6);
An(2 downto 1) <= ABC(5 downto 4);
Bn(2 downto 1) <= ABC(3 downto 2);
Cn(2 downto 1) <= ABC(1 downto 0);

--Output Gate Signals
--Enable will enable or disable outputs
--Sap <= ( Ap(0) or (Ap(1) and G1) or (Ap(2) and G2) or (Ap(3) and G3) ) and Enable;
--Sbp <= ( Bp(0) or (Bp(1) and G1) or (Bp(2) and G2) or (Bp(3) and G3) ) and Enable;
--Scp <= ( Cp(0) or (Cp(1) and G1) or (Cp(2) and G2) or (Cp(3) and G3) ) and Enable;
--San <= ( An(0) or (An(1) and G1) or (An(2) and G2) or (An(3) and G3) ) and Enable;
--Sbn <= ( Bn(0) or (Bn(1) and G1) or (Bn(2) and G2) or (Bn(3) and G3) ) and Enable;
--Scn <= ( Cn(0) or (Cn(1) and G1) or (Cn(2) and G2) or (Cn(3) and G3) ) and Enable;

Sap <= ( Ap(0) or (Ap(1) and G1) or (Ap(2) and G2) ) and Enable and not reset_temp;
Sbp <= ( Bp(0) or (Bp(1) and G1) or (Bp(2) and G2) ) and Enable and not reset_temp;
Scp <= ( Cp(0) or (Cp(1) and G1) or (Cp(2) and G2) ) and Enable and not reset_temp;
San <= ( An(0) or (An(1) and G1) or (An(2) and G2) ) and Enable and not reset_temp;
Sbn <= ( Bn(0) or (Bn(1) and G1) or (Bn(2) and G2) ) and Enable and not reset_temp;
Scn <= ( Cn(0) or (Cn(1) and G1) or (Cn(2) and G2) ) and Enable and not reset_temp;

--end of Block 4


end Behavioral;
```