

# **Output Capacitance Loss Measurement and Validation for Low-Voltage Silicon and GaN Devices in DC-DC Converter Applications**

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Thesis submitted to the faculty of the  
Virginia Polytechnic Institute and State University  
in partial fulfillment of the requirements for the degree of

Master of Science  
In  
Electrical Engineering

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May 1, 2023  
Blacksburg, Virginia

Keywords:  $C_{oss}$  hysteresis loss, calorimetric test, non-linear resonance test,  
ZVS figure of merit

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## ABSTRACT

With the rise of soft-switched converter topologies which enable high-frequency power conversion, there has been a premise that these converter topologies can help achieve loss-less switching in a power device. However, this theory is not completely true as there even with soft-switching there is some degree of loss associated in the form of output capacitance-related hysteresis loss, channel turn-off loss, and loss during the dead-time period in these converter topologies.

The soft-switching converters utilize the existence of the device's output capacitance ( $C_{oss}$ ), which is charged and discharged consecutively at each switching cycle, and a hysteresis loss exists due to the difference in charging and discharging output capacitance. In order fully utilize the potential of these novel soft-switching topologies, we need to investigate further into the origins of these losses or loss mechanisms, methods to measure or compute these losses, and then devise ways to optimize the loss for a given application.

This work focuses on exploring methods to quantify this loss for different operating conditions like device current, switching frequency,  $dV/dT$ , etc. In this aspect, some methods have been studied and used to quantify this hysteresis loss for a variety of power devices like SI and GaN. It is reported that only channel turn-off losses exist in devices with ZVS transition, however, we found that the charging and discharging of  $C_{oss}$  is not loss-free and thus it is important that we account for this loss in the design process.

Finally, the loss data obtained from these tests are compared with each other for five different power devices to validate their applicability, and later these test results are used to get an optimized device selection criterion for the best possible efficiency and minimal losses for a ZVS application.

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## GENERAL AUDIENCE ABSTRACT

Pioneers in power conversion are pushing for higher power delivery, and smaller size which can be achieved by turning ON and OFF semiconductor switches of a power converter at a high frequency. However, due to this increased frequency the converter can exhibit significant losses.

To eliminate power losses in these converters, a soft-switching or zero-voltage switching (ZVS) was introduced which provides a soft transition of voltage and current for a semiconductor switch. These switches have a capacitor across their terminals which is labeled as output capacitance. This capacitor can incur a power loss (hysteresis loss) when a voltage is applied and removed repeatedly across it at high frequency even if we have soft switching. This loss can be a significant part of total power loss occurring in the system; thus, it is important to study it.

In this work, two different test methods are explored to measure this loss, so that we can quantify the loss for a variety of semiconductor switches which are emerging in today's technology, and based on these results a semiconductor switch selection criterion can be developed to get minimal hysteresis loss, which can also reduce overall power loss of the power converter and increase its efficiency.

In conclusion, the test results obtained for five different switches are compared for minimal hysteresis losses, and the one with smallest loss is selected for the power converter which will help reduce the hysteresis loss in the output capacitance of the switch.

## Acknowledgements

I would like to express my immense gratitude to my advisor Dr. Jih-Sheng (Jason) Lai, for his guidance and support throughout the entire duration of my master's degree. I am grateful to have gained a better understanding of power electronics and research methodology through his profound knowledge, extensive experience, and his inverter circuits and control coursework which helped me understand digital control better for power converter applications.

I would also like to acknowledge my committee members, Dr. Qiang Li, for his helpful guidance, feedback on this work, and the two of the courses I attended during my master's degree, and Dr. Christina DiMarino for her helpful guidance, feedback for this work, and support as my GTA instructor for two semesters. I thank you both for being my committee member.

I'm thankful to the FEEC staff, Ms. Fran Gailie, for her immense support during my time in the lab therein. I thank all my peers in the FEEC lab, Mr. Dong Jiao, Mr. Zhenming Hou, Mr. Brian Gutierrez, Dr. Suenghoon Baek, Mr. Joseph Yaeger, Mr. Shengcheng Kao, Dr. Hsin-Che Hsieh though I didn't get chance to work with every one of them, I the interaction was great with you all, especially our lab trips.

I would like to thank all my friends who supported me through my engineering journey in India, and without whom it was not possible to be in this position of my life, thank you, Mr. Saurav Chandel, Mr. Piyush Menghani, Mr. Sarthak Jain, Mr. Shantanu Gupta, Mr. Abhishek Kumar, Mr. Ankit Mohapatra, Mr. Mohan Sahu, Mr. Himanshu Chauhan, Mr. Himanshu Goyal, Mr. Tarun Saxena, Mr. Arnav Wadhwa, Ms. Rachna Pathak, and Ms. Surbhi Rastogi.

It is not easy to move your whole life from one continent to another, so a big thanks to all my friends here at Virginia Tech. who made me feel at home, thank you, Ms. Aishworya Roy, Ms. Aparajita Sengupta, Ms. Vaibhavi Pandit, Mr. Gitansh Kataria, Mr. Sengrurthur Karthik, Mr.

Aditya Raj, Mr. Pranav Raj Prakash, Mr. Yugal Gupta, Mr. Vivek Goyal, Mr. Dishant Shah, Mr. Prakhar Sah, Mr. Shiva Alapati, and Ms. Anoushka Vyas. Special thanks to Mr. Jeet Bhavick Panchal, for being a constant support, someone who challenges and inspires me all the time.

Where I am is ultimate because of my family, I would like to express my immense gratitude to my parents Mrs. Navinta Soni, Mr. Naresh Chander Soni, and my little sister Ms. Shefali Soni, for their incessant love and support throughout my life.

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# Chapter 1. Introduction

## 1.1 Output Capacitance Loss in a MOSFET

With the technological advancement in the realm of the semiconductor industry, the metal-oxide-semiconductor field effect transistor (MOSFET) has become an integral part of almost every technology involving electronics. With the increasing demand for MOSFETs, the industry has responded with the best technology possible in the last 50 years like Trench FET [1], Hex FET[2], and Super-Junction (SJ) Silicon [3] from manufacturers like International Rectifier (Infineon Now), ST Microelectronics, and Fairchild Semiconductor (Analog Devices Now), etc.

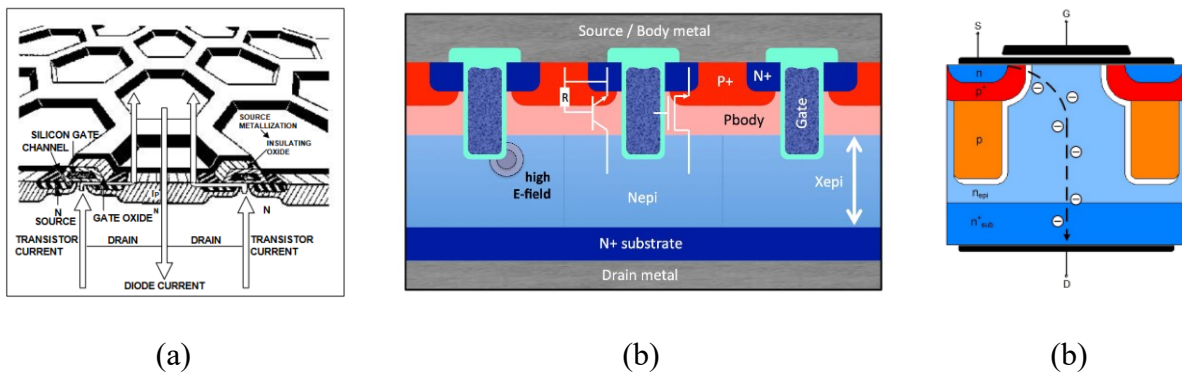


Fig. 1.1 Cross section of (a) HexFET [2], (b) Trench MOSFET [1], (c) Super-Junction Si FET [3].

With these technologies comes their unique advantages like better On-state resistance, and high-voltage blocking, within a smaller chip size, and at an affordable price. However, these devices are generally evaluated for applications like Buck [4], Boost [5], and their derived topologies [6], and are mainly aimed toward hard-switching applications. With the rise and popularity of resonance-based topologies like series resonant converter[7], parallel resonant

converter [8], *LLC* [9], *CLLC* [10], and *DAB* [11]. The wide-bandgap devices like gallium nitride [12] and silicon carbide [13] have been inducted into the power electronics application due to their ability to switch at high-frequency and attain advantages from soft-switched topologies. Structures for GaN HEMT and SiC MOSFET are shown in Fig. 1.2 and Fig. 1.3, respectively.

It has been assumed that with the incorporation of soft-switching converter topologies or zero-voltage switching (*ZVS*), the switching losses can be fully eliminated, which is untrue, as only turn-on losses can be eliminated with *ZVS*; turn-off related losses remain in the device which needs to be accounted for [14], and it also incorporates the channel related turn-off loss which has been investigated in [15].

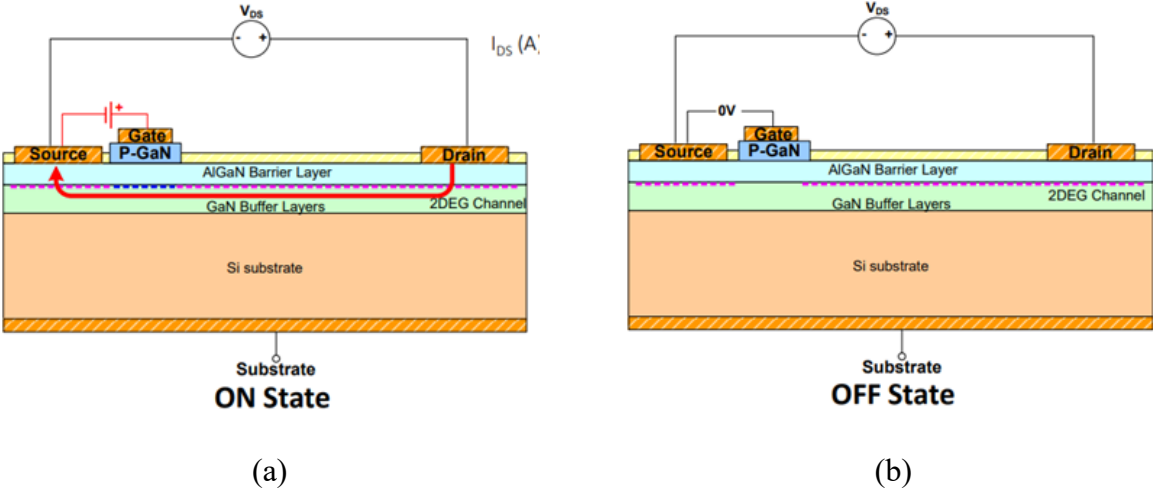


Fig. 1.2 E-Mode GaN HEMT structure from GaN Systems [12] (a) when the channel is turned-on, (b) when the channel is turned-off.

With the increasing switching frequencies for applications like wireless power transfer where the switching frequency is in several MHz, the  $C_{oss}$ -related hysteresis loss might be significant due to the charging and discharging of  $C_{oss}$  at MHz frequency range, like in [17] where the loss

characterization has been presented for applications like class-DE rectifier in which the losses related to junction capacitance of a SiC diode is characterized by using Sawyer-Tower (ST) test method, the dissipated energies are computed using the charge-voltage curves obtained through ST test, later a device selection procedure based on the loss minimization is presented. In another literature [18], a comparison is performed for the different technology of GaN devices for a class 2 amplifier application. The GaN devices are characterized for different ranges of frequencies 5-35 MHz with sine, square wave nature, using the similar ST method which is adopted in [17] as well. It is also reported that the  $C_{oss}$ -related loss data has not been reported in many literatures or GaN device manufacturers, which needs to be addressed for better designs in the future.

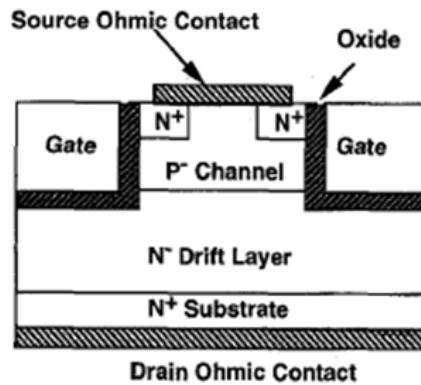


Fig. 1.3 Cross section of a SiC UMOSFET [13].

Currently, the challenge associated with the optimized design of power converters for ZVS applications is related to the measurement of  $C_{oss}$  which is usually performed using an impedance analyzer or an LCR meter, where both instruments use a small-amplitude to excite the DUT, and only measures the impedance at a bias point and chosen test frequency, thereby only computing the small-signal value of the  $C_{oss}$  which is not usable when the hysteresis is present in the device under test [19]. Manufacturer's data only includes the small-signal  $C_{oss}$  which can be misleading

while selecting the switching device for ZVS applications as the  $C_{oss}$  contributes majorly to achieving a soft-switching transition in the device.

## 1.2 Methods to measure the hysteresis loss related to the output capacitance

Several methods have been explored, which can be used to obtain the large-signal behavior of the output capacitance and the loss associated with it. Some of these methods are Sawyer-Tower (ST) circuit test [18][19], Calorimetric Test [20], Non-linear (NR) resonance test [21], and Unclamped Inductive Switching (UIS) [16].

The ST circuit has been widely adopted to measure hysteresis in the output capacitance of switching devices, it separately measures the charging and discharging behavior of this non-linear capacitor and gives a charge-voltage curve which can be used directly to get the hysteresis loss. However, the test needs a power amplifier with sufficient amplitude and frequency range and an external reference capacitor which needs to be very accurate as it can affect the Q-V hysteresis curve, and it can only be used with sinusoidal voltage waveforms. Section 2.1 presents the detailed test procedure and working mechanism for the ST circuit test.

The calorimetric test method is one popular method that overcomes the difficulty of the ST test by eliminating any need for an external reference capacitor, or power amplifier. The test charges/discharges the  $C_{oss}$  by keeping the channel turned-off and measuring thermal resistance, and temperature rise during the steady-state operation, which can be used to get dissipated energy in the  $C_{oss}$  of the device. As shown in [20] the test method achieves voltage waveforms like ones in a soft-switched converter, thus the results are quite close to the actual application. Section 2.2 presents the detailed test procedure for the calorimetric test.

NR test method has gained quite an interest to characterize the output capacitance and its related losses due to a few advantages like, it doesn't require a high voltage DC supply unlike ST

and Calorimetric methods, it can quickly perform the  $C_{OSS}$  loss characterization unlike the ST and Calorimetric test where the test must be carried out at steady-state or thermal equilibrium. The only additional parts required for this test are a gate driver to supply gate voltage to the device, and an inductor to tune the frequency of non-linear resonance. Section 2.3 broadly describes the test process of the NR test.

In a further section, we explore the reasoning for the origins of the  $C_{OSS}$ -related loss in different device technologies like Silicon, GaN, and SiC.

### 1.3 Origins of the Soft-Switching Losses in Silicon Super-Junction Devices

The root cause for the anomalous behavior of  $C_{OSS}$  losses in power devices has not been studied in the literature until recently [19]. It is evident that even at slow speeds or lower switching frequencies SI MOSFETs exhibit significant  $C_{OSS}$ -related losses, rendering them unusable at higher switching frequencies. In [22] it is reported that the loss mechanism is a result of a stranded charge between the SI pillars as the depletion layer expands during the OFF-state operation.

Further, mixed mode simulations along with the finite element analysis (FEA) of the MOSFETs channels are carried out to validate the cause of the loss, the study covers two technology for the SI-FET, one is Multi-implant multi-epitaxy (MEMI), and the other is the trench-filling epitaxial growth (TFEG), from an electrical point of view, both SI structures are equivalent, showing almost identical area-specific  $R_{ds,on}$  and the break-down voltage. However, despite this similarity, they behave differently to the resonant HB test [23], the TFEG structure shows symmetry while the MEMI structure shows asymmetry in the  $V_{DS}$  voltage waveforms shown in Fig. 1.4.

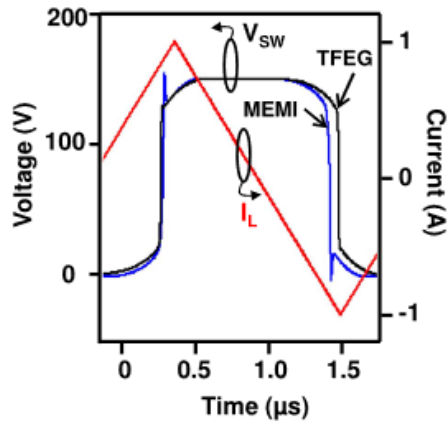


Fig. 1.4 Simulated  $V_{SW}$  and  $I_L$  versus time in one cycle for MEMI and TFEG structure ( $V_{DD} = 150V$  and  $F_{SW} = 400$  kHz) [23].

It is reported that there is an irregular depletion front in the MEMI structure where the electron and hole charges become dynamically stranded ( $Q_{STR}$ ), and this stranded charge is concentrated in undepleted islands along the n and p pillar centers. The  $Q_{STR}$  is removed through a depleted region with high lateral electric field ( $E_x$ ). In both structures, the current flows transversal to the  $E_x$  and eventually, a high-resistance path induces significant joule heat for the electrons and holes at the n and p pillars, respectively. It is reported that in MEMI structure, the large-signal  $C_{OSS}$  shows a clear hysteresis effect Fig. 1.5 (a), and in conclusion, the MEMI structures are more prone to  $C_{OSS}$ -related energy loss, whereas SI-FETs based on the TFEG structures appear to be the best choice for resonant converters.

In further discussion, enlarging the n pillar for the same given charge reduces the energy loss in the  $C_{OSS}$ , indicating that the old technologies, with a larger cell pitch, have more immunity to the  $C_{OSS}$  hysteresis. A similar type of conclusion has been mentioned in [19] where the  $C_{OSS}$  is charging, then the n and p pillars initially have mobile carriers; however, when discharging, the n

and p carriers are completely depleted of mobile carriers. During, the charging phase, some mobile carriers get islanded where the non-uniform spread of the depletion region causes pockets of undepleted regions along both n and p pillars, which lead to the charge imbalance during charging and discharging, giving rise to hysteresis effect and thus dissipation of some energy in  $C_{oss}$ .

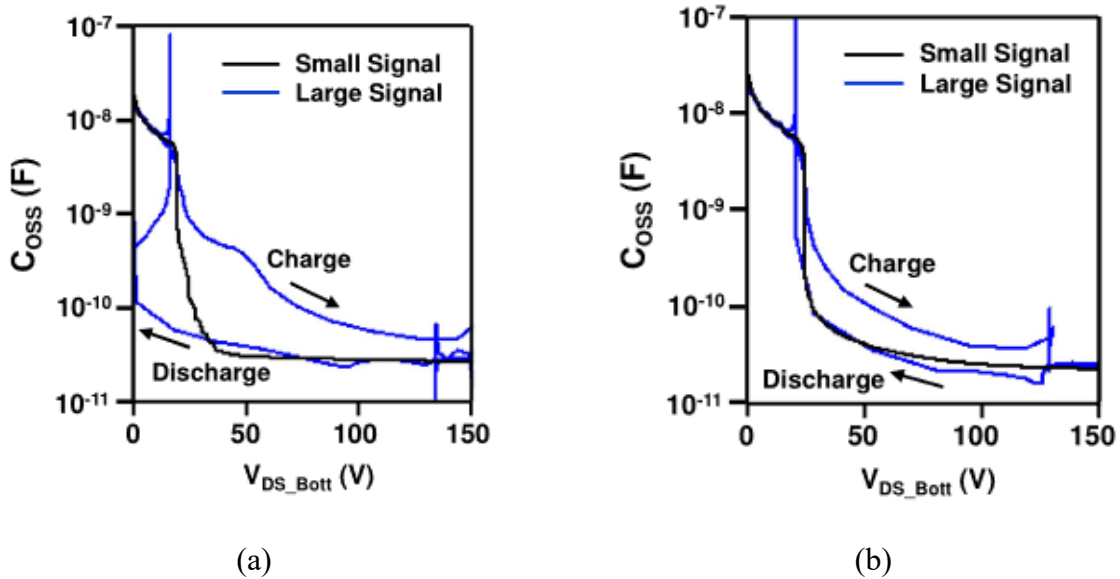


Fig. 1.5 Comparison between  $C_{oss}$  extracted by small-signal and large-signal simulation for (a) MEMI and (b) TFEG SI-FETs [23].

#### 1.4 Origin of the Soft-Switching Losses in GaN/GaN-on-Si/SiC Devices

The same mechanism of  $C_{oss}$ -related hysteresis loss can't be applied to the GaN HEMTs as they don't have SI-type pillars. Thus, there must be some other phenomenon explaining  $C_{oss}$ -related loss. TCAD simulations can be used to analyze the underlying loss mechanism for the GaN devices [24], where the simulations show the imbalance between the stored and released charges in the device, which can be further used to point in the direction of exploring the origin of these losses. Moreover, in [25] a detailed test concludes that the dielectric of the parasitic capacitance between the drain and the substrate of the device could be responsible for the observed  $C_{oss}$ -related

loss. The simulations can present the transfer of charges between the electron current and displacement current, which can be used to verify the energy transfer to the  $C_{OSS}$  and reveal the underlying loss mechanism.

For the Silicon Carbide (SiC) devices,  $C_{OSS}$ -related losses occur due to the resistive power dissipation in the termination region. The variation in the losses with changing the switching frequency,  $dV/dT$ , and device temperature arise from the incomplete ionization which causes the time-dependent charge storage in the device's  $C_{OSS}$  which is usually not reported in the manufacturer's datasheet or the SPICE models but can be explained using a 2D TCAD simulation [22]. Understanding the loss mechanism can help optimize the efficiency of a power converter that is being used for high-power, or high frequency like wireless power transfer applications [26].

Based on the above discussion, the end application product or design can be optimized, not completely though, as we still need to evaluate the  $C_{OSS}$ -related loss to have a design process or a guide. It is critical to know the underlying physics of the device being used in an application, however, the focus of this work is mainly to quantify the hysteresis loss in the  $C_{OSS}$  of the device and validate the results, which can be incorporated to develop a design criterion for the soft-switched power converter.

In conclusion of this section, the underlying mechanism for the  $C_{OSS}$ -related loss for different device physics is discussed, and it is majorly related to the stranded charge carriers in the super-junction pillars for the SI devices, for the GaN devices it is mainly due to the unbalance of the stored and released charges which cause hysteresis, but there still has some work left to get the exact cause for this loss, and for the SiC devices, the loss arises due to incomplete ionization and the resistive dissipation in the termination region.

Chapter 2 presents how we can evaluate the  $C_{OSS}$ -related loss for a variety of different devices emerging from SI and GaN technology. It is mainly divided into two three subparts which discuss the three basic methods to analyze the losses in device  $C_{OSS}$ ; namely Sawyer-Tower circuit-based method, Calorimetric test-based method, and Non-linear Resonance based method. Further, the chapter presents the fundamental test methodology of each test, the advantages, and possible disadvantages of each of the methods, and the scope of applicability for each method.

Chapter 3 presents the experimental test setup and practical considerations to implement the two different test methods to measure the  $C_{OSS}$ -related hysteresis loss. Further, it includes a detailed discussion about the hardware setup, mainly the test board-related aspects like the optimal temperature rise in DUT to get better thermal data to compute losses using the calorimetric test, PCB layout considerations for the NR test method to get the hysteresis loss in the  $C_{OSS}$ . In conclusion, the chapter presents the experimental hardware results obtained using the above-mentioned methods for  $C_{OSS}$ -related hysteresis loss.

In chapter 4, the experimental test results obtained in chapter 3 are validated on a  $\sim 270W$  DC-DC converter using 4 different devices (3 Silicon, 1 GaN), by performing a total loss breakdown procedure, and identifying the individual loss elements; out of these loss elements, the switching loss is breakdown into three main losses,  $C_{OSS}$  related hysteresis loss, channel turn-off loss, and dead-time loss in the DUTs. Other loss elements are also presented and discussed such as FET conduction loss, transformer-related core and winding losses, rectifier-related conduction loss, capacitive loss, bus capacitor-related conduction losses, input-coupled inductor-related core, and winding losses, and PCB parasitics-related miscellaneous losses. Using the insights from this

chapter, a design approach incorporating a new figure of merit (FOM) for ZVS-based converters is adopted and used for the optimized design of the power converter.

Chapter 5 presents a design example of a soft-switched LLC resonant converter to highlight the impact of  $C_{oss}$  hysteresis loss on the overall switching loss of the converter, the two main contributors to the switching loss are compared and it is found that hysteresis loss has significant contribution in the switching loss compared to the channel turn-off loss. Moreover, the chapter is concluded by selecting an optimal device which gives smallest total loss using the ZVS FOM explored in Chapter 4.

# Chapter 2. Evaluation of Output Capacitance-Related Loss

## 2.1 Sawyer-Tower Based Test Method to Measure the $C_{OSS}$ -related Switching Loss

Sawyer-Tower (ST) circuit-based tests methods have been used previously to measure the hysteresis loss in commercial fixed value capacitors (Film, Ceramic) and MOSFETs which enables the direct measurement of the charge voltage characteristics of the device under test (DUT). For the first time, the Sawyer-Tower circuit was used to characterize the saturation and hysteresis occurring in a Braun tube with the dielectric material called Rochelle Salt, ultimately to make large value capacitors [42]. This method is adopted as an alternative to the impedance analyzer or LCR meter, as these instruments can only measure the device  $C_{OSS}$  when hysteresis is not present. However, an ST circuit can be used to measure the  $C_{OSS}$  irrespective of the hysteresis in the DUT, and a typical circuit for the ST test is shown in Fig. 2.1 consisting of a function generator that provides a signal to the power amplifier (boosts the voltage level), a reference capacitor to measure the charge stored, and the device itself.

There are some advantages of using the ST method as it doesn't require any external components (inductors, active switches, gate drivers, or control circuits) other than a reference capacitor (which provides a DC bias to ensure that the body diode doesn't conduct) and the DUT itself. The test setup only measures the input voltage ( $V_{IN}$ ) and reference voltage  $V_{ref}$  from the reference capacitor, thus being very accurate even at very high frequencies (VHF) range as the current measurements often be prone to inaccuracies.

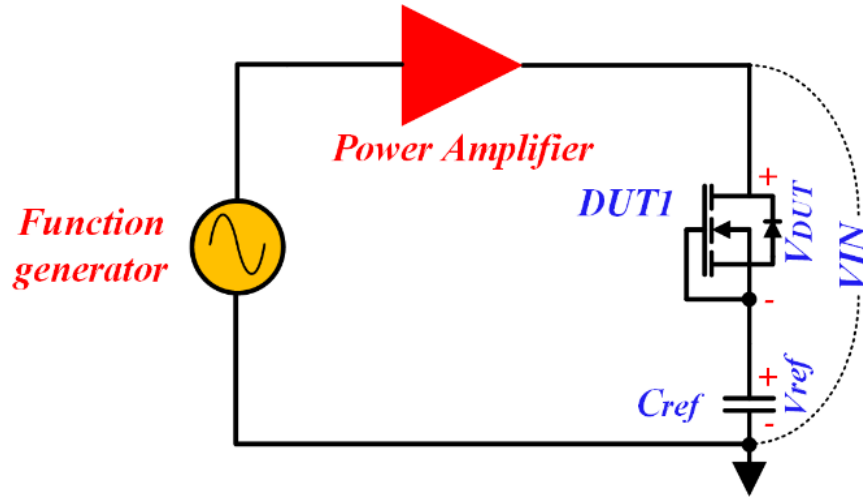


Fig. 2.1 Sawyer-Tower circuit for  $C_{OSS}$  hysteresis loss measurement.

$$Q_{OSS} = C_{ref}V_{ref} \quad (2.1)$$

$$V_{DUT} = V_{IN} - V_{ref} \quad (2.2)$$

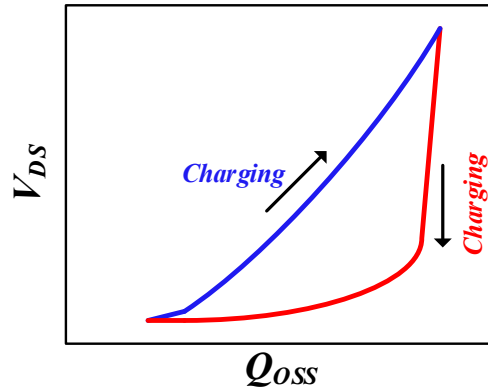


Fig. 2.2 Charge-voltage hysteresis curve.

The (2.1) presents the output charge of the FET or DUT, where  $C_{ref}$  is the high precision, low tolerance reference capacitor, and  $V_{ref}$  is the voltage measured across this reference capacitor. Further, (2.2) can be used to get the voltage across the DUT, where  $V_{IN}$  is the voltage across the DUT and  $C_{ref}$ , this can be used to get the charge-voltage hysteresis of something like in Fig. 2.2

Charge-voltage hysteresis curve Fig. 2.2 which shows the charging and discharging behavior in the  $C_{OSS}$  of DUT.

In this work, the ST method has not been accounted for to measure the large signal  $C_{OSS}$ -related hysteresis loss in the DUT for a variety of reasons. Firstly, the power amplifier is required to excite the DUT with desired voltage and frequency which might not be accessible, and if an amplifier using a Half-bridge or Full-bridge converter is designed to excite the DUT, it is imperative to match the equivalent load for the given frequency and power. The gain of the power amplifier degrades with the increase in excitation frequency  $f_e$ , and thus, the application of pulsed waveforms is highly limited by the bandwidth of voltage or power amplifier and the value of equivalent load capacitance  $C_{eq}$  [27].

Second, the reference capacitor ( $C_{REF}$ ) suffers from frequency, and voltage dependency which can impact the measured charge-voltage hysteresis and impact the overall loss measurement and it can also distort the input voltage waveform if not chosen correctly.

Third is the impact of DUT's  $C_{OSS}$  as it directly impacts the load impedance, the value of  $C_{OSS}$  regulates the current entering the DUT, and if it is too large, it can destabilize the power amplifier, and there might occur a distortion in the voltage being applied to the DUT.

Fourth, the reverse conduction of the DUT's body diode; it is assumed that the body diode is reverse biased during the test (no conduction in III quadrant), but due to the leakage current, there is an additional loss in the DUT which compromises the use of ST test. However, this adverse effect is countered by choosing an excitation frequency such that rate of charge build-up due to leakage current is at least two orders of magnitude lower than the DUT's  $Q_{OSS}$  [27]. The authors

in [27] also proposed a new Q-V curve variation which considers the finite reverse voltage of the DUT and ensures that the charge when  $V_{DS} = 0$  is equal to zero.

## 2.2 Calorimetric Test Method to Measure the $C_{OSS}$ -related Switching Loss

This section presents a thermal or calorimetric approach to evaluate the soft-switching losses of power converters. Calorimetric tests were used to obtain the core loss in the magnetic materials [29] however, the setup used here for the soft-switching loss measurement is unique from the test setup used for the core loss measurements. Usually, the electrical measurements for the  $C_{OSS}$ -related loss in a soft-switching application are prone to inaccuracies as discussed in the previous section.

In [20] a calorimetric measurement method is presented to characterize the energy loss due to hysteresis in  $C_{OSS}$ , which incorporates the thermal measurements (which are less prone to inaccuracies) to compute the thermal resistance ( $R_{th,CA}$ ) and the dissipated energy ( $P_{dissipated}$ ) in the device  $C_{OSS}$ .

The test uses a resonant half-bridge circuit to mimic the actual operation conditions of the power converter shown in Fig. 2.3 comprising of a half-bridge (HB) converter exciting the two devices (DUT1, DUT2) connected in series with each other with their gate terminal tied to their sources to keep the channel turned OFF and connected to the excitation HB circuit via an Inductor whose value is calculated as per the test requirements like the frequency of excitation, current going through the device  $C_{OSS}$ .

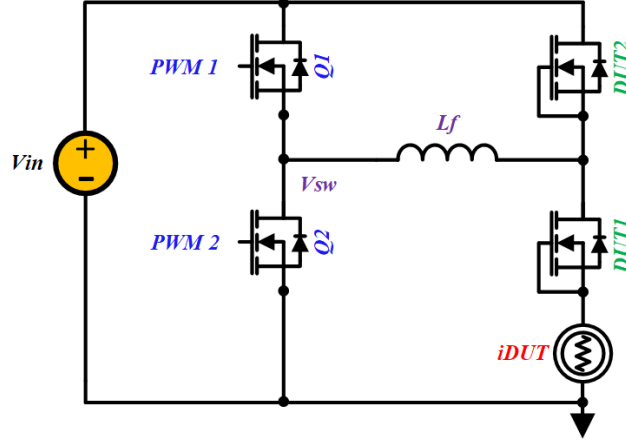


Fig. 2.3 Half-bridge (HB) resonant circuit for Calorimetric test.

In this test, the circuit is operated in steady-state conditions and the temperatures are recorded for both DUTs and the air they have been soaked in to get the ambient temperature data. The temperature difference is between the DUTs, and the ambient temperature is recorded to get the rise in temperature  $\Delta T_{CA}$  which will be later used to get the dissipated energy loss.

For the other part of this measurement, we need the case-ambient thermal resistance ( $R_{th,CA}$ ) of the DUT, which can be computed by passing a DC current through the device, using the same hardware setup with the inductor connection being removed. With this, the temperature rise in the DUT is recorded along with ambient temperature, voltage and current across the DUT.

$$R_{th,CA} = \frac{\Delta T_{CA,DC}}{|I_{DUT} V_{DUT}|} \quad (2.3)$$

$$P_{dissipated} = \frac{\Delta T_{CA,SS}}{R_{th,CA}} \quad (2.4)$$

However, there are some practical aspects required to be taken care of just like in the ST method. It is critical to keep the  $\Delta T_{CA,SS}$  larger than  $2^\circ C$  to get sufficient temperature measurement

resolution and ensure that the self-resonant frequency of the inductor is much larger than the excitation frequency from the HB circuit. Further design concerns for the calorimetric test will be discussed in the upcoming sections where we discuss the experimental setup used in this work.

In [28] the calorimetric test is used to evaluate the losses between a SI and two GaN devices under soft-switching operation at an MHz frequency range, and when compared to the predicted simulation results showed a significantly lower efficiency, which explains for the unaccounted loss data in manufacturer's datasheet and the SPICE model. Thus, it is important to perform calorimetric tests to get the real picture of the devices which can render quite helpful for optimizing the design and getting the best performance.

Based on the same principle of calorimetry, [25] made a novel measurement procedure, aiming to identify the region of transistors where the losses originated, and potentially conclude the cause behind it, and based on that they present a new GaN-on-Si device which is free from the  $C_{oss}$  related loss and the dynamic  $R_{ds,on}$  phenomenon; thereby capable of extracting the full potential of the GaN-on-Si substrate.

In this work, a similar calorimetric approach to that of [20] has been used to obtain the energy loss data for the device  $C_{oss}$  in a soft-switching application. For this purpose, the circuit of Fig. 2.3 is used to evaluate the dissipated energies in the  $C_{oss}$  of the five different devices.

### 2.3 Non-Linear Resonance (NR) Based Test Method to Measure the C<sub>oss</sub>-related Switching.

This method was used by [30] to measure the large-signal output capacitance of transistors, MOSFETs, as discussed before that the small-signal values don't depict the true picture to evaluate the C<sub>oss</sub>-related losses in the devices. This method overcomes the limitation of the ST method as, the fixed value of reference capacitor in ST method can't be suitable to measure large non-linearity, as at high temperatures the leakage current can be comparable to the displacement currents in the C<sub>oss</sub> and C<sub>ref</sub>.

Another restriction that it overcomes is the limitation of the voltage swing/frequency applied to the DUT before its thermal runaway. This method only requires a low-voltage DC source to evaluate the charge/discharge behavior of the DUT, therefore eliminating any need for the high-voltage amplifier unlike the ST method and even the Calorimetric method. Moreover, the test setup is not complicated unlike ST or even the calorimetric method.

The NR method utilizes the resonance between a pre-calibrated inductor and the C<sub>oss</sub> of the DUT, this inductance can be tuned to get the desired frequency and  $dV/dT$  in the voltage excitation applied to the DUT, all of this with just a small DC voltage source connected to the DUT via this inductor. The frequency of the excitation signal varies inversely with the value of the inductor used, for small values of inductance, the frequency of the excitation signal will be higher.

In addition, the test setup can be used to obtain the large-signal C<sub>oss</sub> and the energy loss associated with it during the charge-discharge cycle, which eliminates the self-heating of the

device and does not thermally limit the maximum voltage swing unlike in the calorimetric or ST test where the device is subjected to steady-state conditions, which can also alter the measurement due to trapping phenomenon discussed in [22].

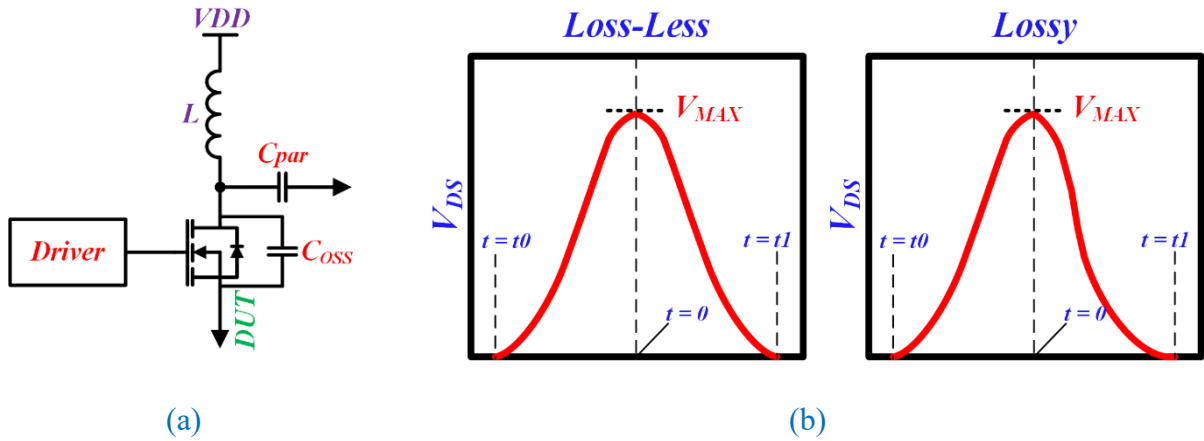


Fig. 2.4 (a) Non-linear resonance test circuit, (b)  $V_{DS}$  versus time plot to depict loss-less and lossy behavior.

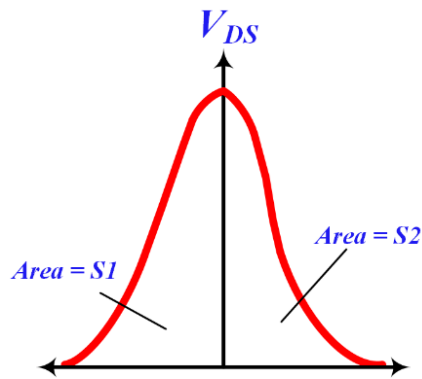


Fig. 2.5 Area under the  $V_{DS}$  vs time curve to get the energy dissipated in the  $C_{OSS}$  during a single charge-discharge cycle.

The test method uses resonance between the inductor  $L$  and the output capacitance ( $C_{OSS}$ ) as mentioned above. In this test, the gate of the DUT is actively driven using a gate driver and control

circuit; during this time the inductor is charged through the low-voltage DC source, and when the gate of the device is turned-OFF, a resonance occurs between the inductor and the  $C_{OSS}$  of the device shown in Fig. 2.3. (b)

The charging and discharging energies can be computed using (2.5), and (2.6). The difference between these two equations gives the dissipated energy (2.7) in the device's output capacitance. These equations can be computed in MATLAB to get curves like Fig. 2.6 which depicts the energy dissipated in the  $C_{OSS}$  of the device.

$$E_{OSS,chg} = \frac{1}{2L} \int_{t_0}^0 (V_{ds}(t))^2 \quad (2.5)$$

$$E_{OSS,dchg} = \frac{1}{2L} \int_0^{t_1} (V_{ds}(t))^2 \quad (2.6)$$

$$E_{DISS} = \frac{1}{2L} \int_{t_0}^0 (V_{ds}(t))^2 - \int_0^{t_1} (V_{ds}(t))^2 \quad (2.7)$$

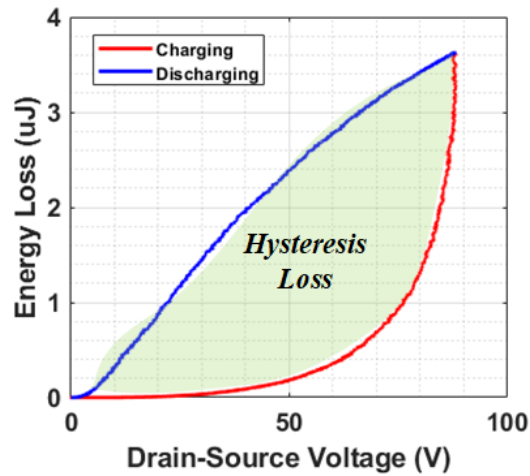


Fig. 2.6 Dissipated loss in the device's  $C_{OSS}$  obtained through of  $V_{DS}$  data.

In [30] it is mentioned that the results for the large-signal  $C_{OSS}$  were verified using Sawyer-Tower method-based measurements at  $300\text{ kHz}$ , though the measurements were taken at a maximum voltage of  $100V$ , the supply voltage  $V_{DD}$  was only  $100\text{ mV}$ , that is the device was characterized by using a small voltage input, thus it is one of the advantages of NR test method.

This method is used in a single-pulse mode, which doesn't heat up the junction or increase the leakage current in the device and has the nature of resonant power converters. The circuit minimizes the possible number of parasitics to avoid spikes on the drain terminal of the device, through resonance smooth charging, discharging curves are obtained. This method can be widely used for any kind of device like GaN, SiC, and SI with only a few components, and a similar approach is used in this work to characterize different SI, and GaN devices for  $C_{OSS}$ -related hysteresis loss measurement.

In this work, the NR test method is used extensively to evaluate FETs with different device physics like SI, and GaN, and for different frequencies and thus the  $dV/dT$ . The test circuit of [30] has been incorporated to implement this method for low-voltage SI FETs, and GaN HEMTs.

# Chapter 3. Experimental Test Setup and Results for Calorimetric and NR Methods

## 3.1 Experimental Test Setup for Small-signal $C_{OSS}$ Measurements

For the first test, we measure the  $C_{OSS}$  with the DC bias voltage applied to the device, using the test circuit of Fig. 3.1 with a blocking resistor  $R_{block}$  to limit the current drawn through the DC source, and a DC blocking capacitor  $C_{block}$  to prevent DC voltage entering the input terminals of the LCR meter to avoid any damage, and only allow small-signal AC voltage to measure the  $C_{OSS}$ . The experimental test hardware of Fig. 3.2 is used to implement this test, where the components of the test are highlighted as, the device itself,  $R_{block}$ ,  $C_{block}$ , input DC source terminal, and the measurement terminal.

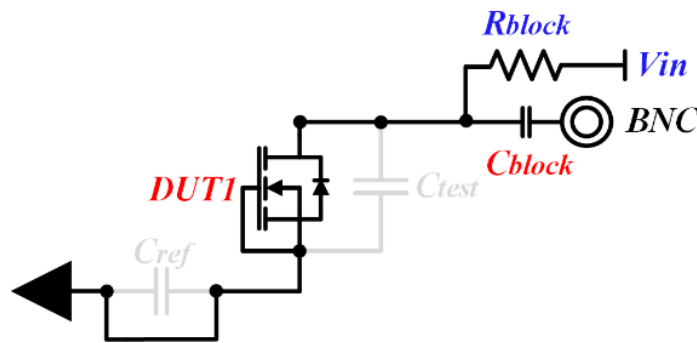
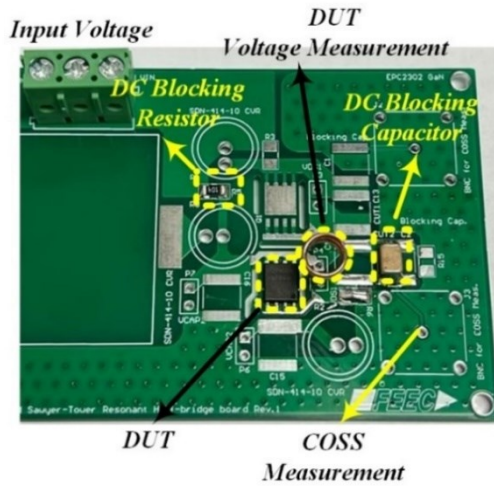


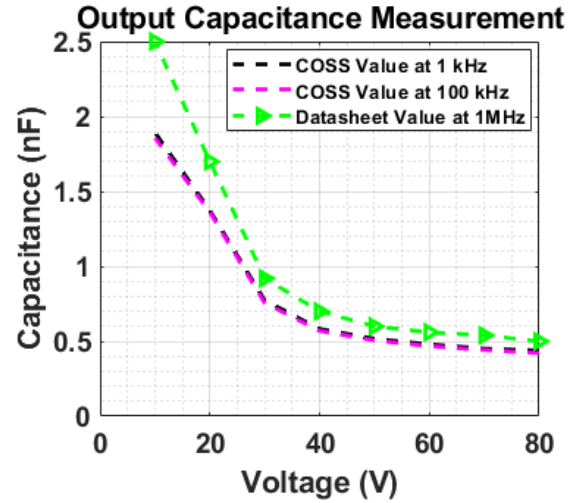
Fig. 3.1 Test circuit to measure the small-signal  $C_{OSS}$ .

We can observe the small-signal  $C_{OSS}$  data tested for two different frequencies (1 kHz, 100 kHz) with the DC bias across the device and measure it using an LCR meter. The two  $C_{OSS}$  values match well; however, the datasheet value is a bit different as it was computed with only small-signal injection at a frequency of 1 MHz.

Thus, even with this simple setup, we can observe the discrepancy between the datasheet value and the small-signal (measured with DC bias applied to the device).

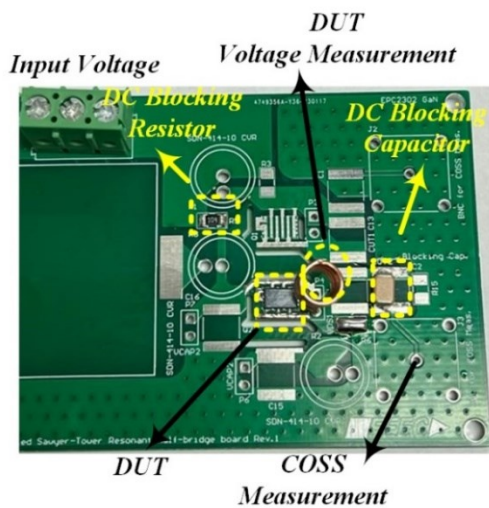


(a)

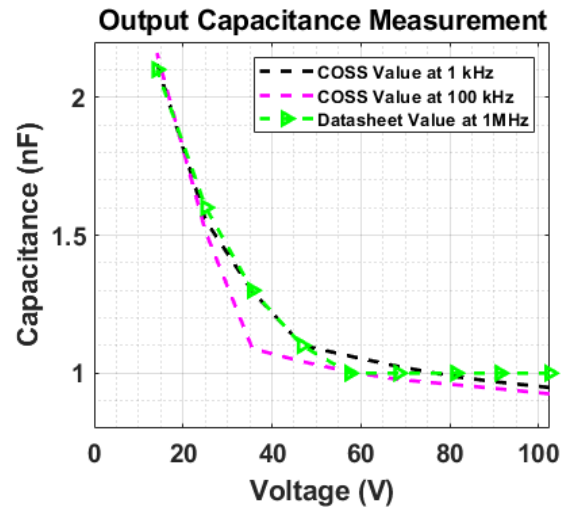


(b)

Fig. 3.2 (a) Experimental hardware for small-signal  $C_{oss}$  measurement (SI FETs), (b) Experimental small-signal output capacitance test results for SI FET (BSC037N08NS5).



(a)

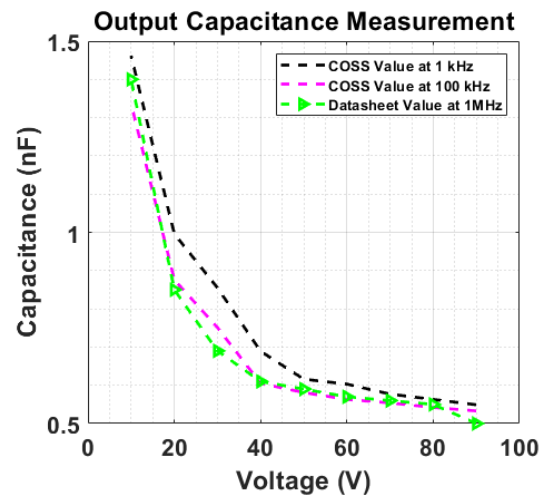
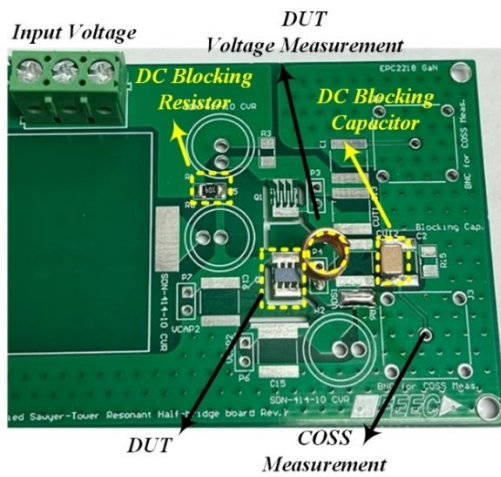


(b)

Fig. 3.3 (a) Experimental hardware for small-signal  $C_{oss}$  measurement (EPC 2302), (b) Experimental small-signal output capacitance test results for GaN FET (EPC 2302).

A similar test can be performed for the other device technology like GaN (EPC-2302, EPC-2218) shown in Fig. 3.3 where we can observe that the measured  $C_{OSS}$  is in accordance with the datasheet values but with a little deviation for the value at 100 kHz; and for EPC-2218 we can observe in Fig. 3.4 that the capacitances are deviated from the datasheet values, clearly showing the shift in  $C_{OSS}$  values when it is measured with the DC bias applied across the device.

The circuit of Fig. 3.5 is used to carry out the calorimetric test on the SI FETs which is comprised of a half-bridge evaluation module from EPC (EPC 9034) to supply excitation signals, a digital C2000 MCU from Texas Instruments to supply PWMs to the half-bridge evaluation board, SDN-414 high-precision co-axial current shunt from T&M Research, and DUTs.



(a) Experimental hardware for small-signal  $C_{OSS}$  measurement (EPC 2218), (b) Experimental small-signal output capacitance test results for GaN FET (EPC 2218).

In the calorimetric test, we capture the temperature of either of the DUT and monitor the temperature rise of the DUTs, which can be used to get the dissipated power (2.4) in the  $C_{OSS}$  if thermal resistance  $R_{th,CA}$  is known as in (2.3) which can be computed using the test mentioned in

section 2.2 where we forward bias the body diode of the devices so that the channel and  $C_{oss}$  would not conduct and a current is applied through these body diodes which generates a temperature rise in both DUTs, we can monitor and record this temperature rise to compute for the  $R_{th,CA}$  as per (2.3).

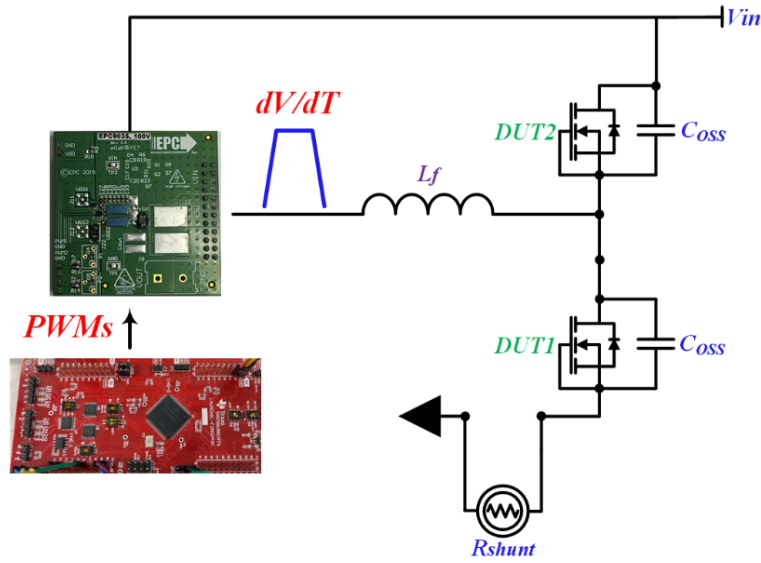


Fig. 3.5 Calorimetric test circuit to measure large-signal  $C_{oss}$  measurement and energy loss related to it.

An experimental prototype for the calorimetric test of devices is shown in Fig. 3.6 in which the half-bridge evaluation board is used to get switched voltage waveforms with desired frequencies to excite the DUTs, followed by an inductor which is used for controlling the amount of current entering the device capacitance, and the DUTs in a half-bridge configuration.

The overall test setup acts like a resonant half-bridge converter mimicking the voltage waveforms across the DUTs to that of a soft-switched resonant converter (*LLC* [9], *IBR-Z* [31]). The current and voltage waveforms for the SI FET BSC037N08NS5 [32] are shown in Fig. 3.8 and Fig. 3.9, respectively.

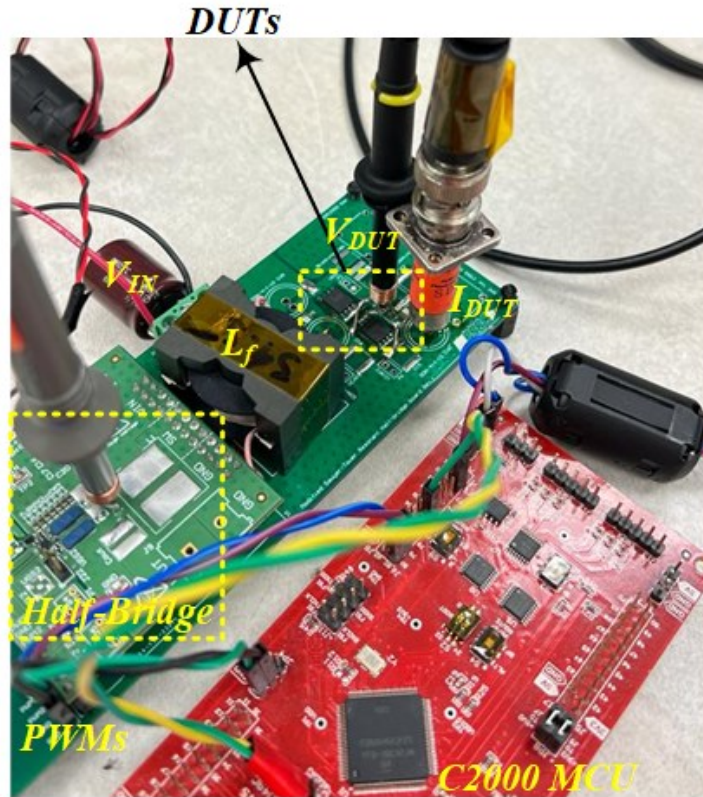


Fig. 3.6 Experimental hardware setup for thermal validation/calorimetric test

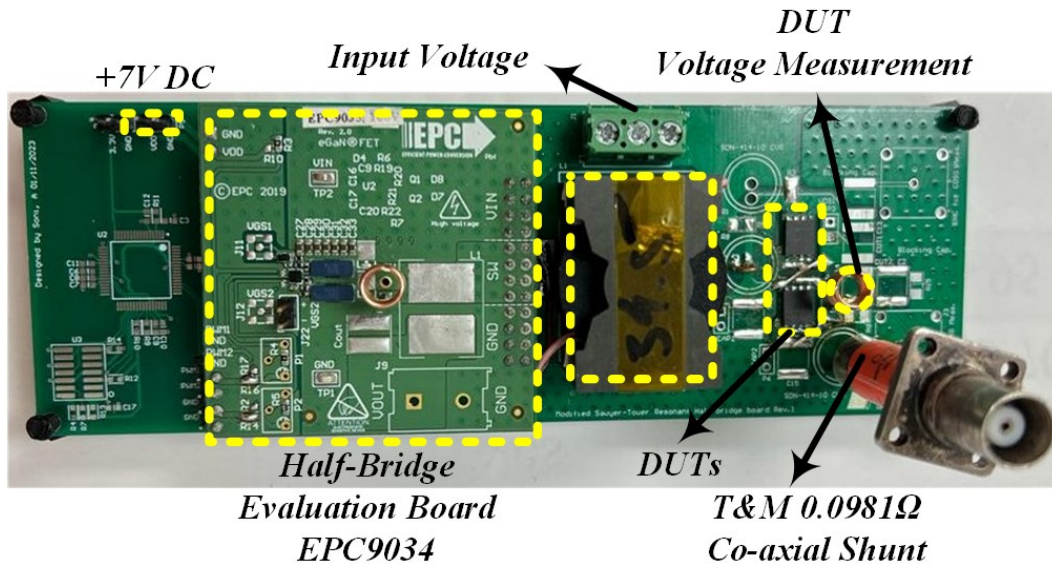


Fig. 3.7 Experimental setup for thermal validation/calorimetric test of SI FETs

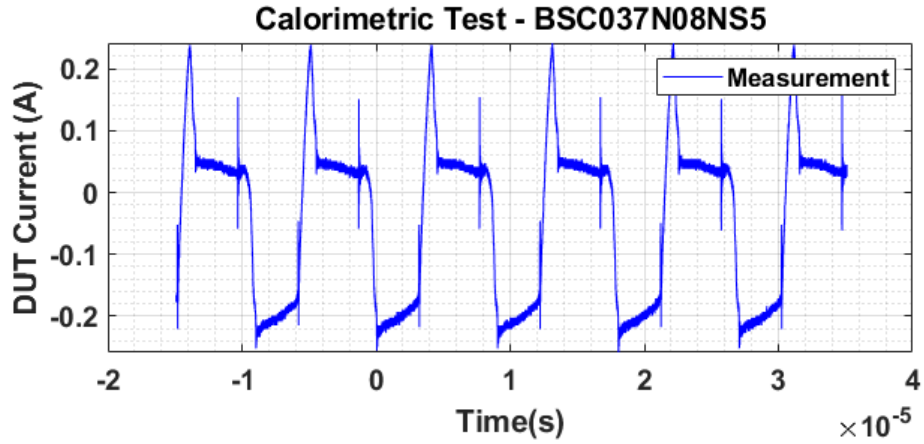


Fig. 3.8 Measured current through the device  $C_{OSS}$  for SI FET BSC037N08NS5.

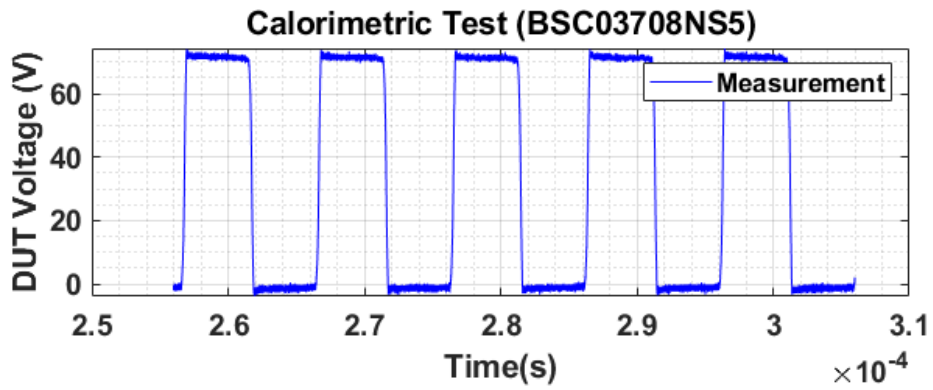


Fig. 3.9 Measured voltage across the device  $C_{OSS}$  for SI FET BSC037N08NS5.

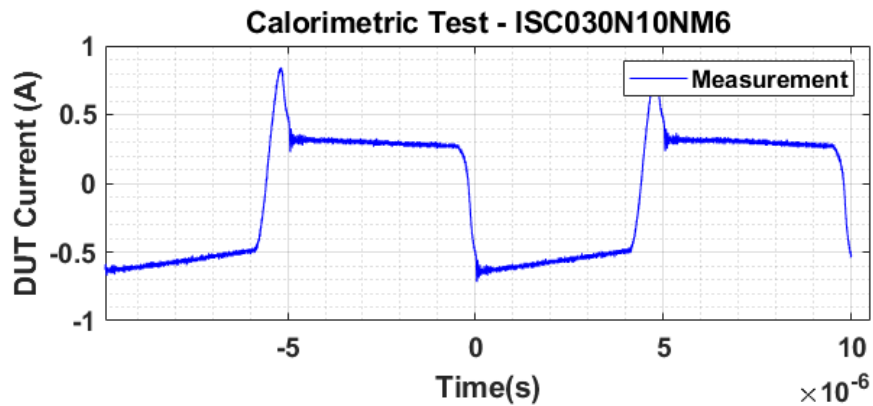


Fig. 3.10 Measured current through the device  $C_{OSS}$  for SI FET ISC030N10NM6.

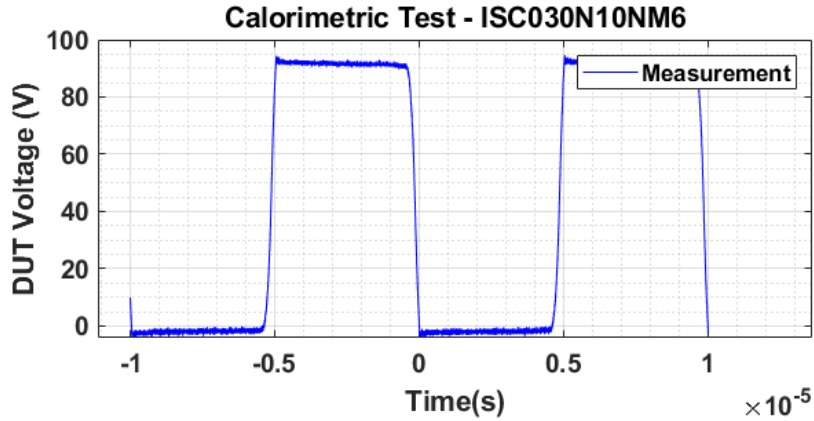


Fig. 3.11 Measured voltage across the device  $C_{OSS}$  for SI FET ISC030N10NM6.

Further, the test is carried out for different devices as well, like ISC030N10NM6 [33], and ISC060N10NM6 [34], both are generation 6 Optimos devices from Infineon Technologies, with better area-specific on-state resistance, output capacitance, and rugged body diode. Moreover, the GaN devices from EPC [35] are tested using the hardware setup of Fig. 3.12, and Fig. 3.15, the current and voltage waveforms for this device are shown in Fig. 3.13 and Fig. 3.14, respectively.

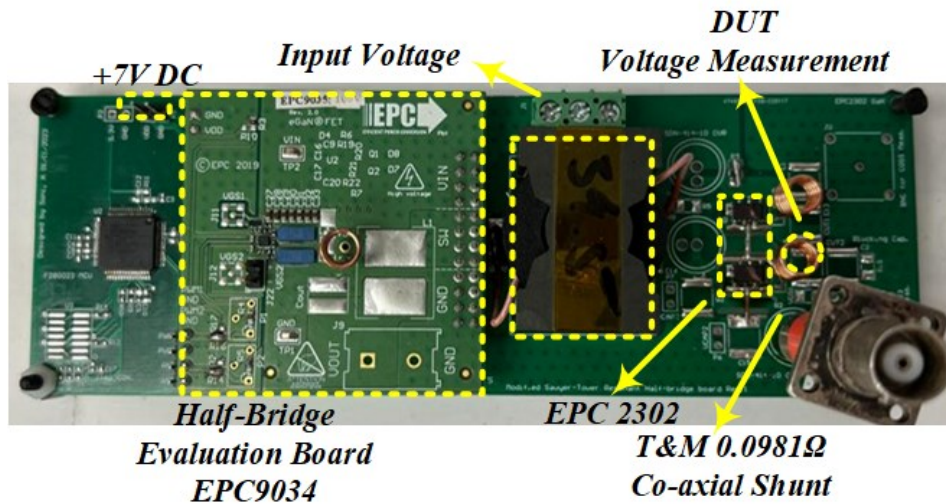


Fig. 3.12 Experimental setup for thermal validation/calorimetric test of GaN FET (EPC 2302).

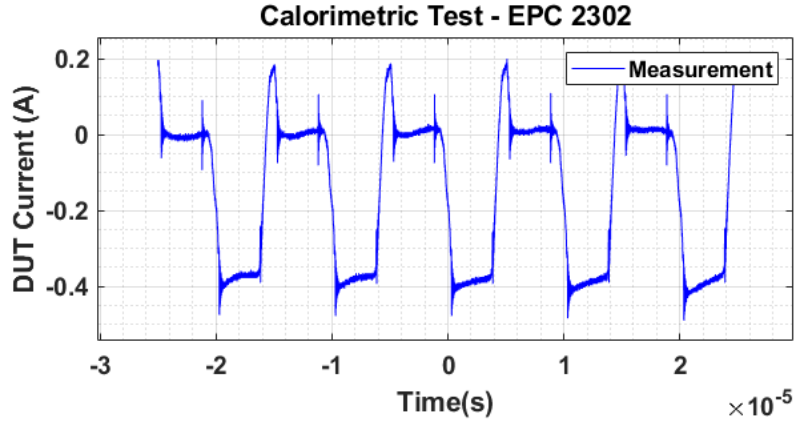


Fig. 3.13 Measured current through the device  $C_{OSS}$  for GaN FET EPC 2302.

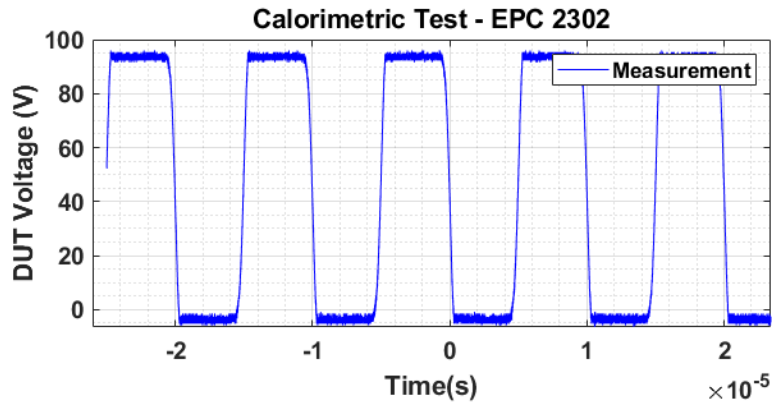


Fig. 3.14 Measured voltage across the device  $C_{OSS}$  for GaN FET EPC 2302.

The spikes in DUT current are due to the  $dV/dT$  involved with the HB circuit, this  $dV/dT$  is coupled with the parasitic capacitance of the inductor and hence induces a spike in the DUT current.

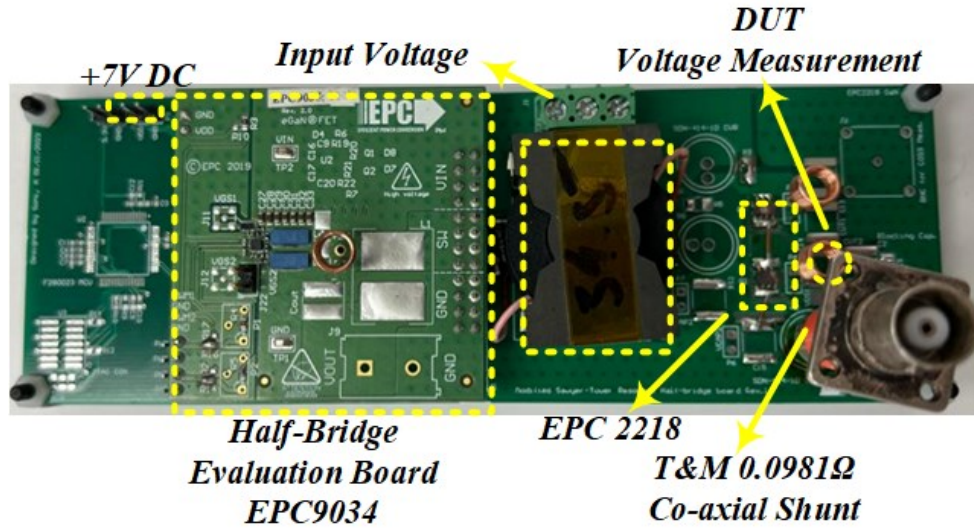


Fig. 3.15 Experimental setup for thermal validation/calorimetric test of GaN FET (EPC 2218).

Fig. 3.12 and Fig. 3.15 show the experimental hardware board for the calorimetric test of the GaN devices (EPC 2218 and EPC 2302) where all the components are the same as of the SI hardware, except the DUTs. The hardware setup can also be used to extract the large-signal  $C_{oss}$  of the devices by computing the RMS current going through the DUT when the channel is turned-OFF, the  $dV/dT$  across the DUT, and using (3.1) which shows that the large-signal  $C_{oss}$  clearly depends on the sweep direction as the  $dV/dT$  would not be identical for charge-discharge cycle, thereby having different  $C_{oss}$  at charge-discharge intervals.

Further, to compute the energy loss, we need the value of large-signal  $C_{oss}$  for each charge-discharge cycle, these are calculated from computing the electrical quantities like DUT current, and the  $dV/dT$  computed through the voltage waveforms across the DUT.

For the computed large-signal  $C_{oss}$ , we can observe that there is a difference between the datasheet values and the obtained large-signal values.

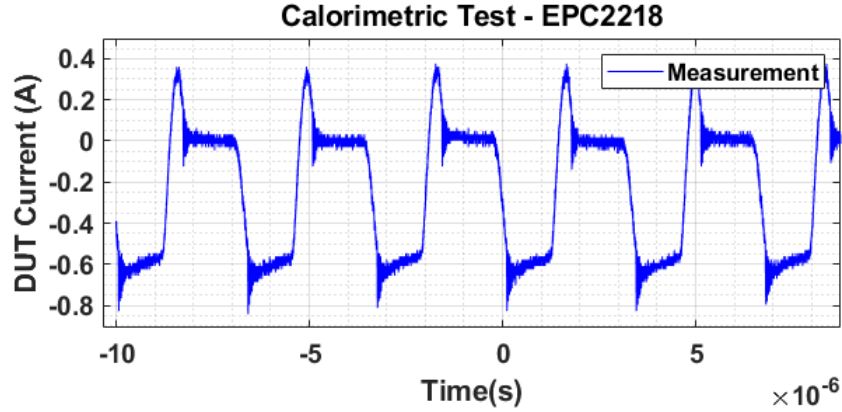


Fig. 3.16 Measured current through the device  $C_{OSS}$  for GaN FET EPC 2218.

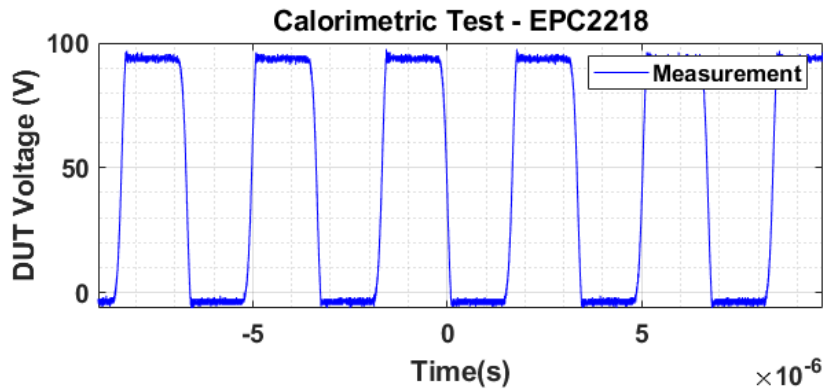


Fig. 3.17 Measured current through the device  $C_{OSS}$  for GaN FET EPC 2302.

This can adversely impact the device selection process as the  $C_{OSS}$  changes dramatically when there is a voltage across it, in words, for the ZVS applications, the design as per the datasheet values of  $C_{OSS}$  won't yield the best possible results. The large-signal  $C_{OSS}$  is computed using the test setup for calorimetric test and (3.1).

We can compute the large-signal  $C_{OSS}$  using the available current information from the coaxial shunt resistor and getting  $dV/dT$  from the voltage waveforms as in (3.1).

$$C_{OSS} = \frac{I_{DUT}}{dV_{DUT}/dT} \quad (3.1)$$

The large-signal  $C_{oss}$  values are shown in Fig. 3.18 for (a) BSC037N08NS5 which is a generation 5 Optimos, 80V SI MOSFET, the datasheet value and large-signal values have quite a difference in between. Similarly, Fig. 3.18 (b) shows the large-signal capacitance for generation 6 Optimos SI FET, ISC030N10NM6, however, the large-signal  $C_{oss}$  is even greater than the Fig. 3.18 (a), which could be due to the lower  $R_{ds,on}$  of generation 6 device.

Further, Fig. 3.19 (a) shows the large-signal  $C_{oss}$  for another generation 6 Optimos device but with lower  $C_{oss}$  compared to the above two devices which are due to the higher  $R_{ds,on}$  of this generation 6 device. The large-signal  $C_{oss}$  for two GaN devices are shown in Fig. 3.19 (b) and Fig. 3.20, where we can observe that the EPC2302 has higher large-signal capacitance than the EPC2218 which could result in more  $C_{oss}$ -related hysteresis loss in actual applications.

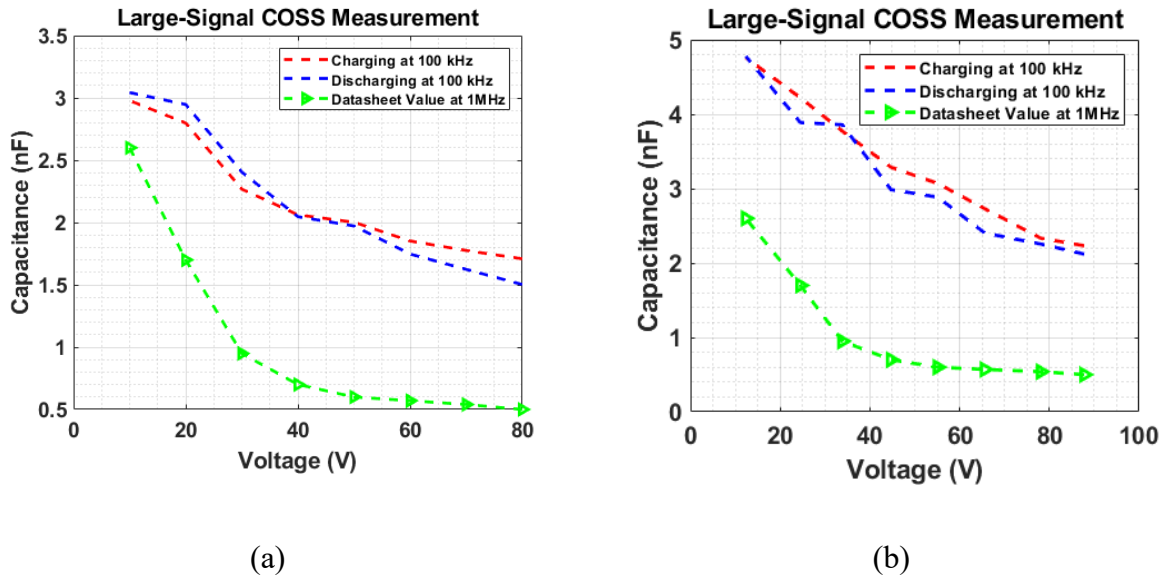


Fig. 3.18 Large-signal  $C_{oss}$  calculation for (a) SI FET (BSC037N08NS5), (b) (ISC030N10NM6), showing that there is a significant discrepancy between the datasheet value and obtained large-signal values, even with the large-signal values the  $C_{oss}$  is swept direction specific.

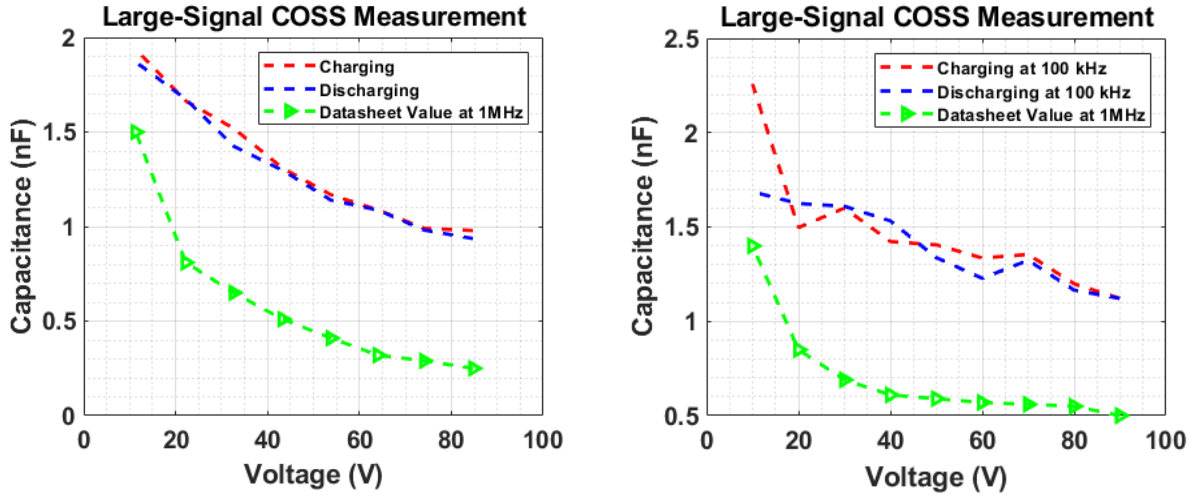


Fig. 3.19 (a) Large-signal  $C_{oss}$  calculation for SI FET (ISC060N10NM6), (b) GaN FET (EPC 2218), showing that there is a significant discrepancy between the datasheet value and obtained large-signal values, even with the large-signal values, the  $C_{oss}$  is swept direction specific.

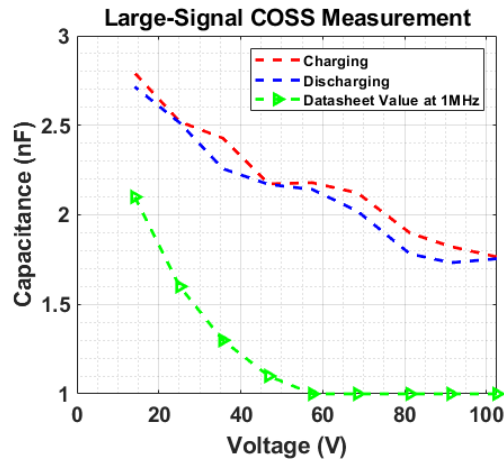


Fig. 3.20 Large-signal  $C_{oss}$  calculation for GaN FET (EPC 2302) shows that there is a significant discrepancy between the datasheet value and obtained large-signal values, even with the large-signal values, the  $C_{oss}$  is swept direction specific.

### 3.2 Design Considerations for the Calorimetric Test Hardware

As mentioned in [20] that the temperature rise should be greater than  $2^{\circ}\text{C}$  to accurately get the temperature rise in the DUTs, the PCB for this test must have either low thermal conductivity or increased thermal resistance to heat the DUT and a temperature rise can be measured with better precision. To achieve this, a few slots have been cut out in the PCB to achieve better thermal resolution, shown in Fig. 3.21.

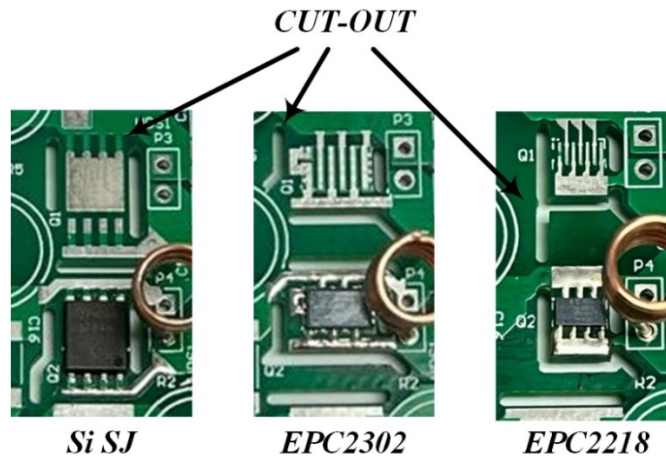


Fig. 3.21 Calorimetric test PCB with cut-outs for three different DUT.

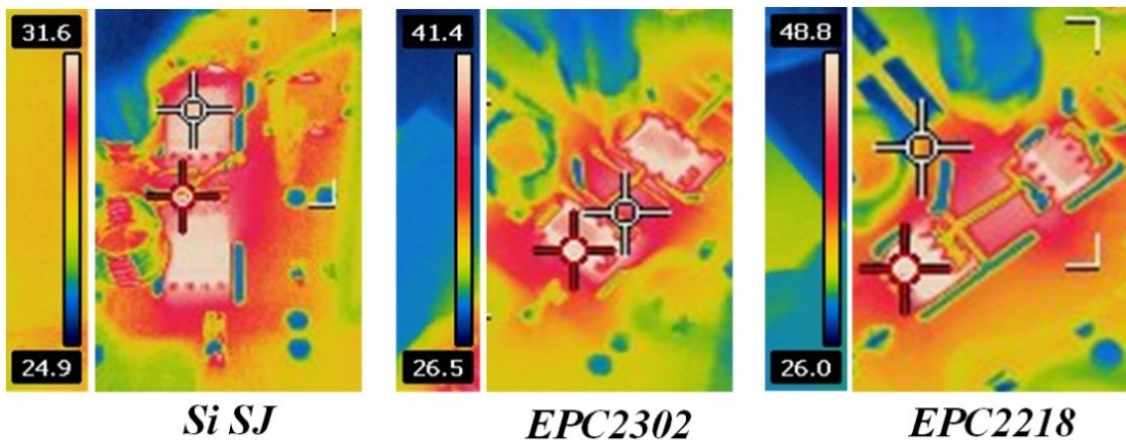
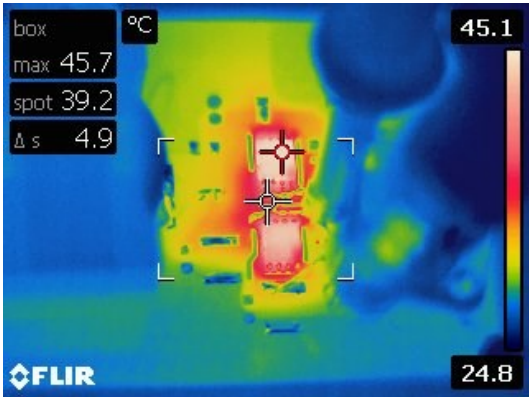


Fig. 3.22 Temperature rises in PCBs of calorimetric test for different devices.

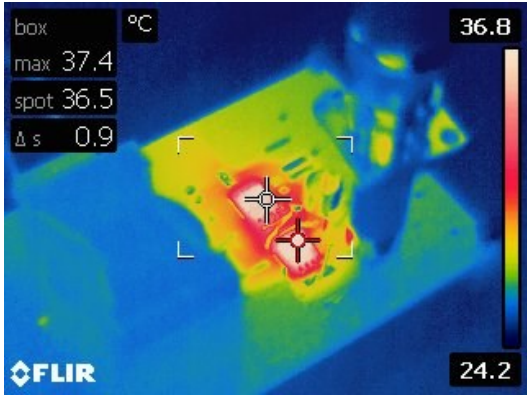
Another way to increase thermal resolution is only to have one layer of conduction, that would resist heat spreading to the other parts of the board and only the area around the DUT will get heated up. The cut-outs are connected by a 22 AWG copper wire instead of foils to minimize the area for heat conduction. It is evident in [37] where the area underneath the DUT is replaced by a wire mesh to increase thermal resolution and get better results for the temperature rise, this is verified by temperature data in Fig. 3.22 shows a good amount of temperature rise in the DUTs which can be easily read by an IR Camera [38].



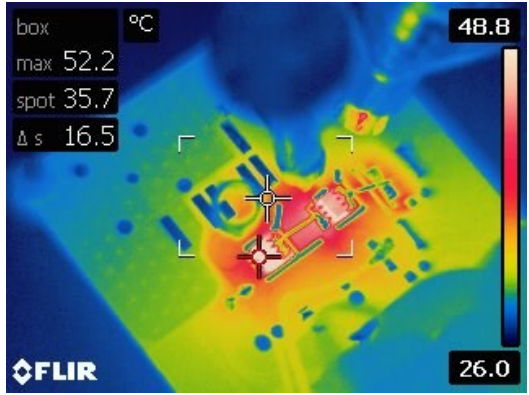
(a)



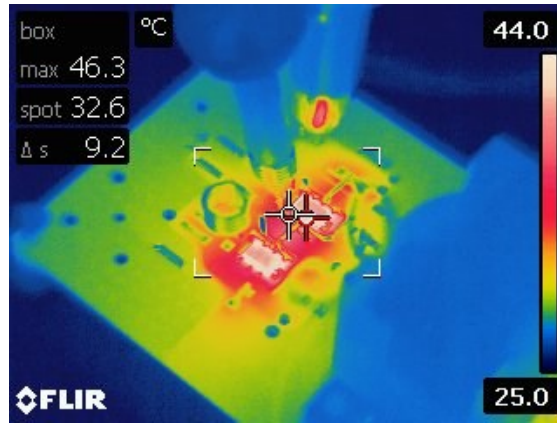
(b)



(c)



(d)



(e)

Fig. 3.23 Temperature rise during steady-state operation (calorimetric test) for 5 different devices under test; (a) BSC037N08NS5 tested at 100 kHz, (b) ISC030N10NM6 tested at 100 kHz, (c) ISC060N10NM6 tested at 100 kHz, (d) EPC 2218 tested at 100 kHz, (e) EPC 2302 tested at 100 kHz.

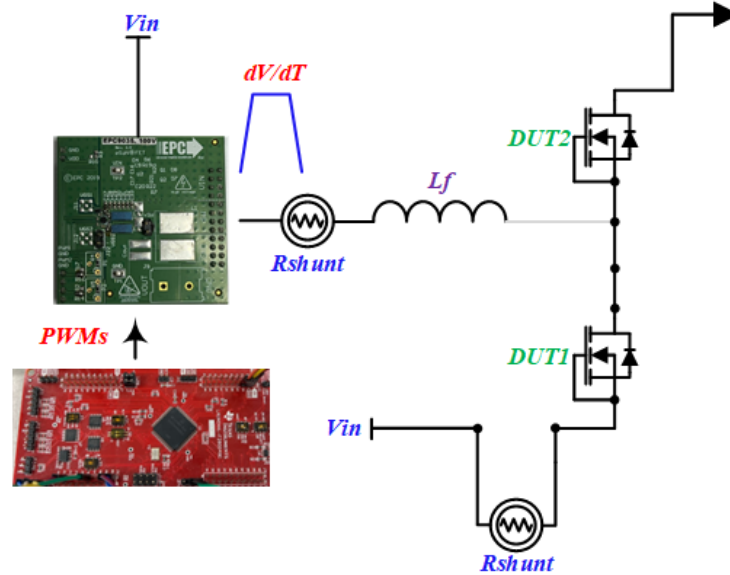


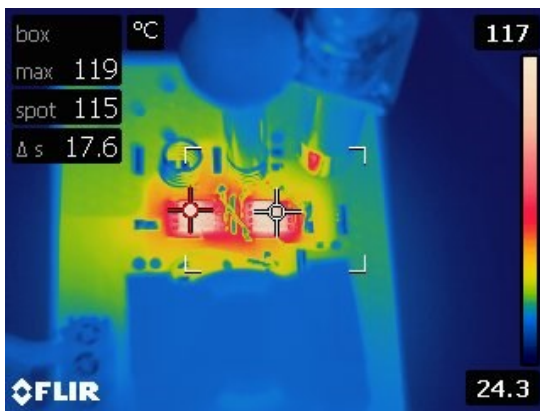
Fig. 3.24 Calorimetric test circuit to measure the  $R_{th,CA}$  of the devices by passing a DC current through the body diodes and disconnecting the inductor  $L_f$ .

The  $R_{th,CA}$  needs to be computed to get the dissipated energy in the output capacitance of the devices, for that the circuit in Fig. 3.25, Fig. 3.24 can be used to perform the thermal resistance test and get the value of  $R_{th,CA}$  which can be used in (2.3) to get the dissipated energy. The computed thermal resistances for five different devices are listed in Table 3.1.

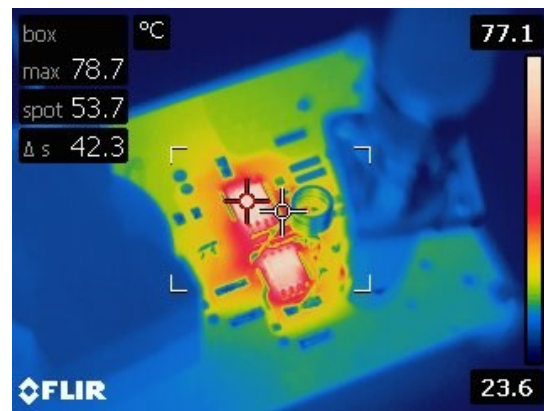
By using the data from Table 3.1, devices with higher case-ambient resistance would yield a smaller amount of dissipated energies (2.4) for a given switching frequency. This can be one of the design selection criteria, but it needs to be validated with other tests as well.

Table 3.1  $R_{th,CA}$  for five different devices

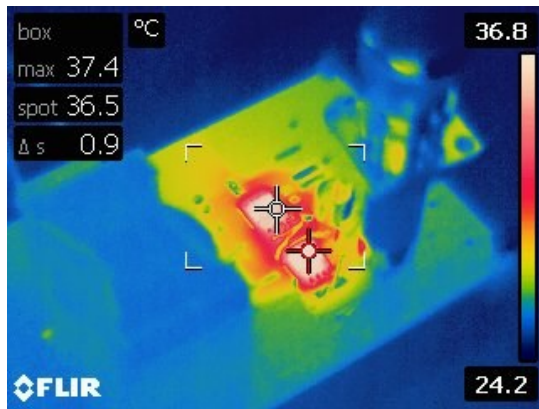
Device Under Test (DUT)	DUT Current (A)	DUT Voltage (V)	Temperature Rise (deg. C)	$R_{th,CA}$ (deg. C/W)
BSC037N08NS5	2	1.02	92.7	46.42
ISC030N10NM6	1	0.58	53.5	91.64
<b>ISC060N10NM6</b>	<b>0.2</b>	<b>0.63</b>	<b>12.6</b>	<b>97.47</b>
EPC 2218	0.6	1.42	76.6	89.40
EPC 2302	0.7	1.7	90.3	75.88



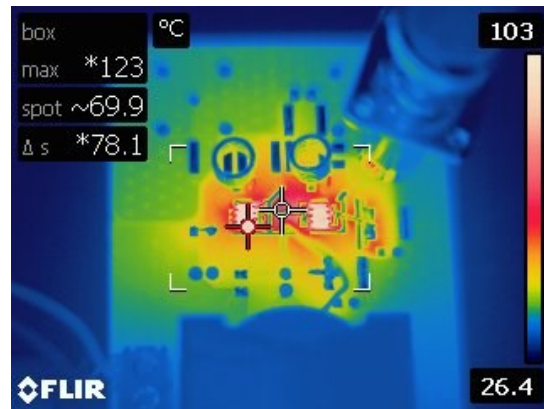
(a)



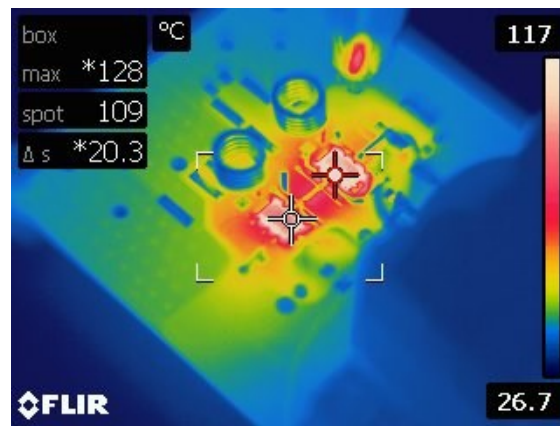
(b)



(c)



(d)



(e)

Fig. 3.25 Temperature rise, during the steady-state operation (thermal resistance test) for five different devices under test; (a) BSC037N08NS5 with  $I_{DUT} = 2A$  and  $V_{DUT} = 1.02V$ , (b) ISC030N10NM6 with  $I_{DUT} = 1A$  and  $V_{DUT} = 0.58V$ , (c) ISC060N10NM6 with  $I_{DUT} = 0.2A$  and  $V_{DUT} = 0.63V$ , (d) EPC 2218 with  $I_{DUT} = 0.6A$  and  $V_{DUT} = 1.42V$ , (e) EPC 2302 with  $I_{DUT} = 0.7A$  and  $V_{DUT} = 1.7V$ .

These thermal resistance values can be used to compute the energy loss in the output capacitance of individual devices. By using the temperature data from Fig. 3.23 Fig. 3.23 the energy loss is presented in Table 3.2 calculated in Watts but to get a better understanding of this loss, the power loss is converted to energy loss per cycle by dividing by the switching frequency.

The data in Table 3.1 coheres to the data in Table 3.2 as the device with a higher  $R_{th,CA}$  yields less dissipative loss in the  $C_{OSS}$  compared to the other devices. Further, other tests like NR, can be performed to validate the coherence observed here.

Table 3.2 Energy loss in the  $C_{OSS}$  for five different devices at 100 kHz

Device Under Test (DUT)	Temperature Difference (deg. C)	$R_{th,CA}$ (deg. C/W)	Power Loss (W)	Energy Loss ( $\mu$ J/Cycle)
BSC037N08NS5	6.7	46.42	0.144	1.44
ISC030N10NM6	20.3	91.64	0.221	2.21
<b>ISC060N10NM6</b>	<b>12.6</b>	<b>97.47</b>	<b>0.129</b>	<b>1.29</b>
EPC 2218	22.8	89.40	0.255	2.25
EPC 2302	19	75.88	0.250	2.50

This test concludes the calorimetric test method, which gives us an estimate of large-signal capacitance results for five different devices, where we observed that the large-signal capacitance differs from the datasheet value for each of the devices, this indicates that there needs to mechanism to include this large-signal  $C_{OSS}$  data into the datasheet of the devices. However, the large-signal capacitances obtained are not the correct representation as it is difficult to identify the charging and discharging points in a rectangular waveform unlike a sinusoidal waveform.

Further, the energy loss related to the  $C_{OSS}$  is also obtained and matched with a two-way process, by computing the  $R_{th,CA}$  for all devices and then computing the energy loss per switching cycle for each device, which validates the coherence between the two results.

However, to validate the results obtained in this test needs to be validated with another test method which will discuss the next method to evaluate the hysteresis loss in the device  $C_{OSS}$  using non-linear resonance.

### 3.3 Experimental Test Setup for Non-Linear Resonance Method

It is important to incorporate more than one method to measure the hysteresis loss in the output capacitance of a device as it provides a sense of reliability and two-factor authentication while evaluating these losses. Moreover, this method has the advantage of being simple and quick to implement unlike Sawyer-Tower, and Calorimetric tests, which can save the design hours, and quickly estimate the capacitive losses in a power semiconductor device.

Fig. 3.26 shows the test circuit of the NR method which can be used for all types of devices. In this test, all the same, five devices have been tested for hysteresis loss in the  $C_{oss}$  and later compared to the results achieved from the calorimetric method.

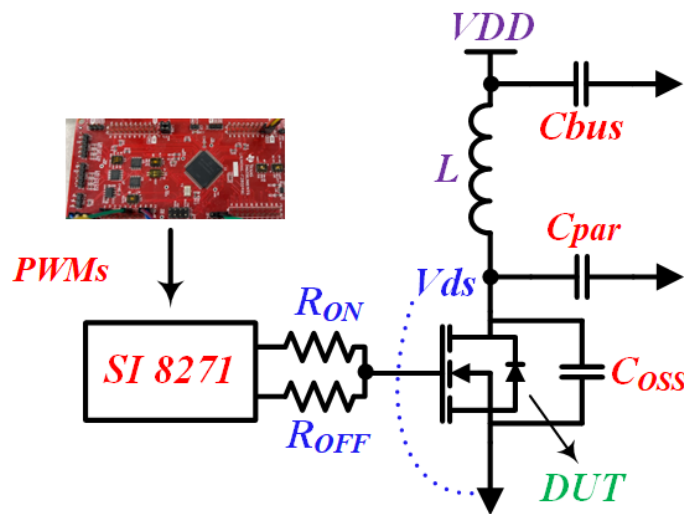


Fig. 3.26 Non-linear resonance test circuit for all DUTs

### 3.4 Design considerations for the test board used in the Non-linear Resonance method

Fig. 3.27 shows the actual experimental hardware setup to carry out the NR test, this comprises of a test PCB with DUTs (SI FET, GaN FET), isolated gate drivers (Si 8271 shown in white boxes)

with separate source/sink channels to drive the DUTs, inductors for non-linear resonance between the  $C_{OSS}$  and itself,  $V_{DD}$  is a low-voltage DC power supply.

The energy is stored in the inductor when the DUT is turned-on, and utilized for resonance when the DUT is turned-off; a digital MCU provides a pulse signal, it uses a switch that triggers an external interrupt in the MCU's Code to generate a single pulse of desired duration/frequency for the gate driver.

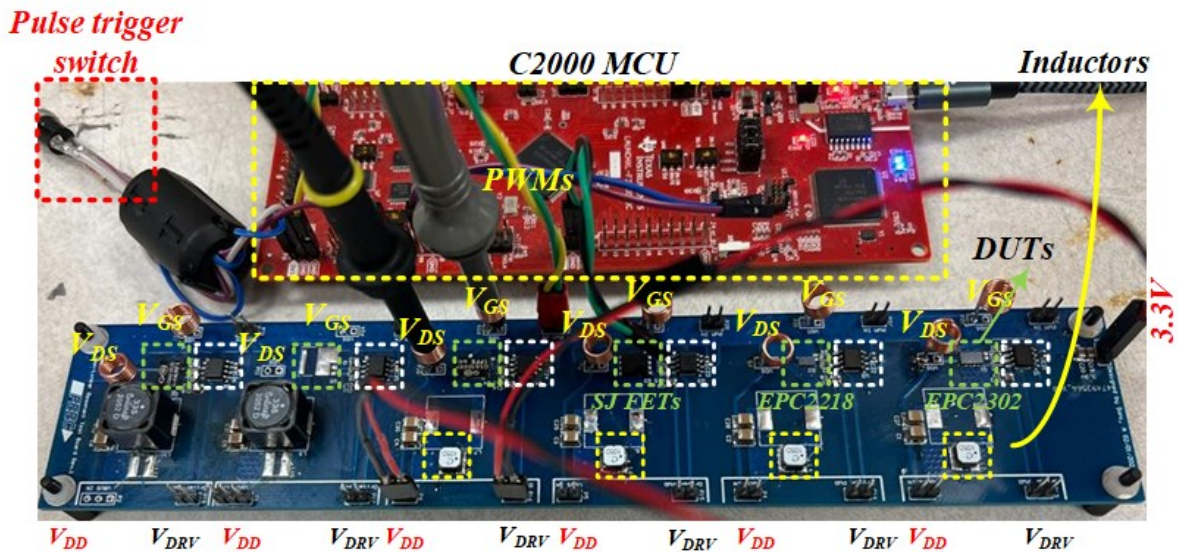


Fig. 3.27 Experimental setup for NR test incorporating all the DUTs in a single PCB.

Key aspects in the hardware design are to keep a small gate drive loop to minimize the loop inductance which if not kept small can introduce spikes in the gate signal and damage the gate of the DUT, another concern is to place the inductor as close as possible to the drain terminal of the DUT to minimize any parasitic inductance which can impact the resonance frequency and DUT's voltage adversely. Lastly, it is important to correctly measure the gate and drain voltage, thus we avoid probes with long ground returns and instead, a ground spring made of conductive copper wire is used to place a probe and measure the signals which remove any spikes related to the ground, and can be seen in Fig. 3.28 where the probes have been directly inserting into the slot

for the ground springs, it is a cost-effective method to measure the signals without any ground related noise. Another advantage of this test is that it captures only the voltage across the devices and not the current, which avoids parasitics due to current-related measurements.

This also helps save costs by eliminating any requirement for the expensive current shunts like the SDN-414 series. For the voltage probes, a 500 MHz passive probe with 10X attenuation is used to capture the drain and gate voltages, as the DUT in this test is referenced to the ground, it is possible to use a passive probe, which is quite affordable and is an advantage of using this method.

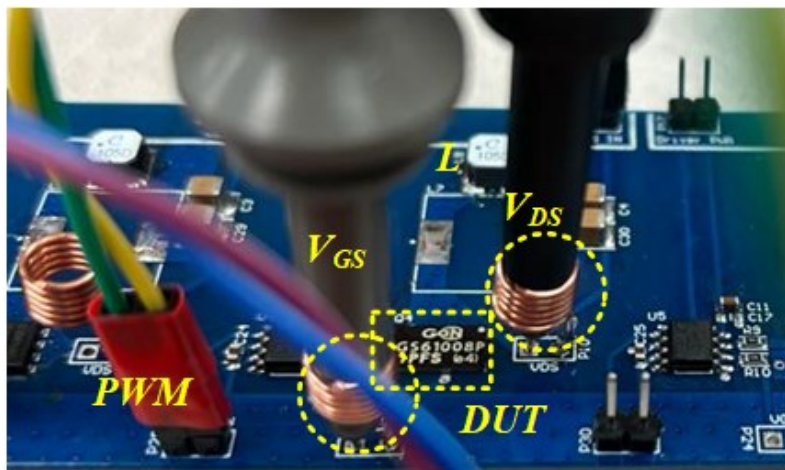


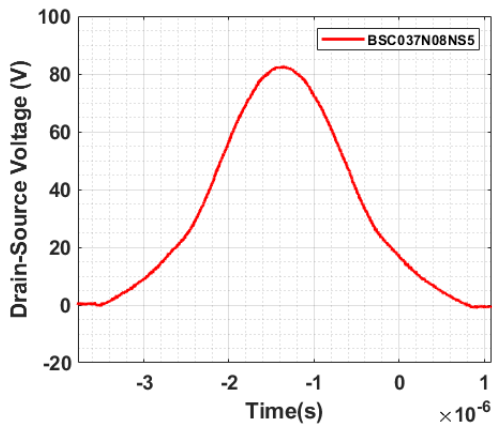
Fig. 3.28 Experimental setup for NR test incorporating all the DUTs in a single PCB.

### 3.5 Experimental test results for $C_{oss}$ -related hysteresis loss

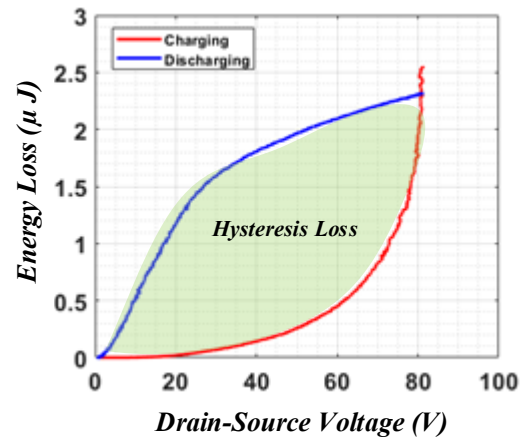
Five different devices are tested for the  $C_{oss}$ -related hysteresis loss in them, starting from three different SI FETs, and two GaN FETs. The test methodology of [20] has been adopted here to obtain the charging, discharging, and dissipated energies in the  $C_{oss}$  of the DUTs.

The DUTs are tested with the NR test setup of Fig. 3.27 to obtain the drain-source voltage waveforms, which can be used along with the inductor values to extract the energy loss information

in the  $C_{oss}$  starting from Fig. 3.29 these voltage waveforms comprise of a complete charge-discharge cycle which can be integrated over time, squared, and divided by the twice the value of inductor used, to get the energy loss as from (2.5), (2.6), and (2.7). The computations performed for this test are numerically simple and can be implemented in a python script.

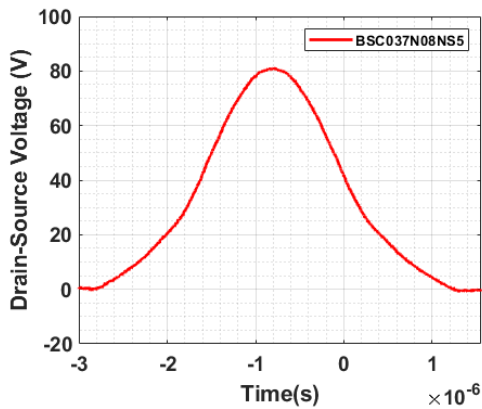


(a)

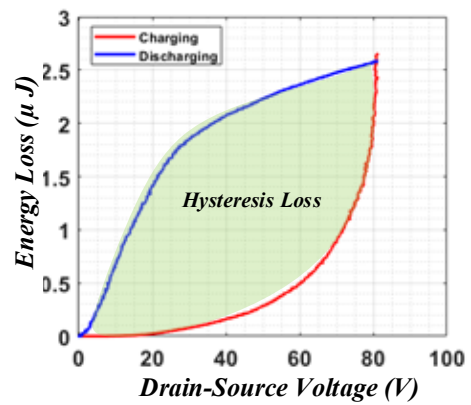


(b)

Fig. 3.29 (a) Drain-source voltage across the SI FET BSC037N08NS5 for inductor value of  $1mH$  and applied gate pulse of duration  $3\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.



(a)



(b)

Fig. 3.30 (a) Drain-source voltage across the SI FET BSC037N08NS5 for inductor value of  $1mH$  and applied gate pulse of duration  $5\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

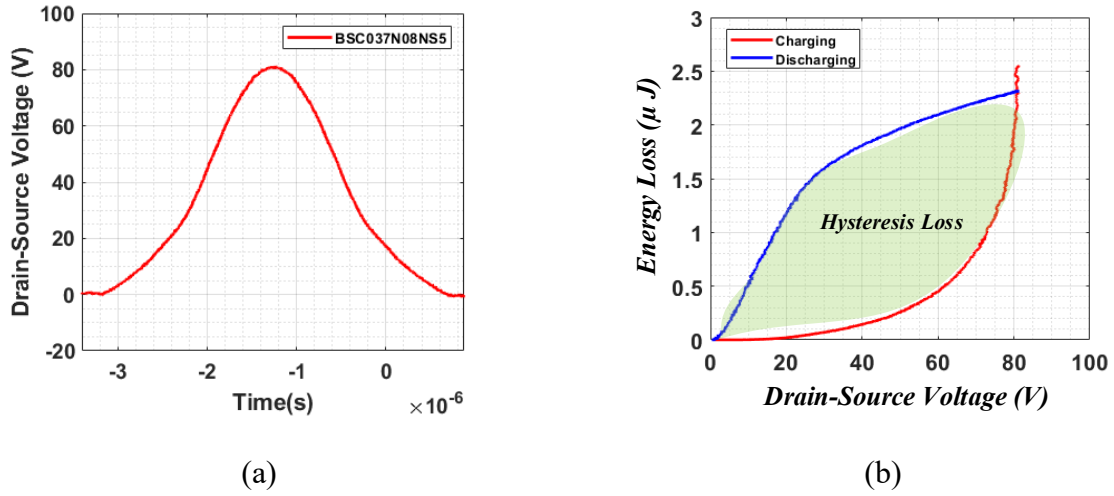


Fig. 3.31 (a) Drain-source voltage across the SI FET BSC037N08NS5 for inductor value of  $1mH$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

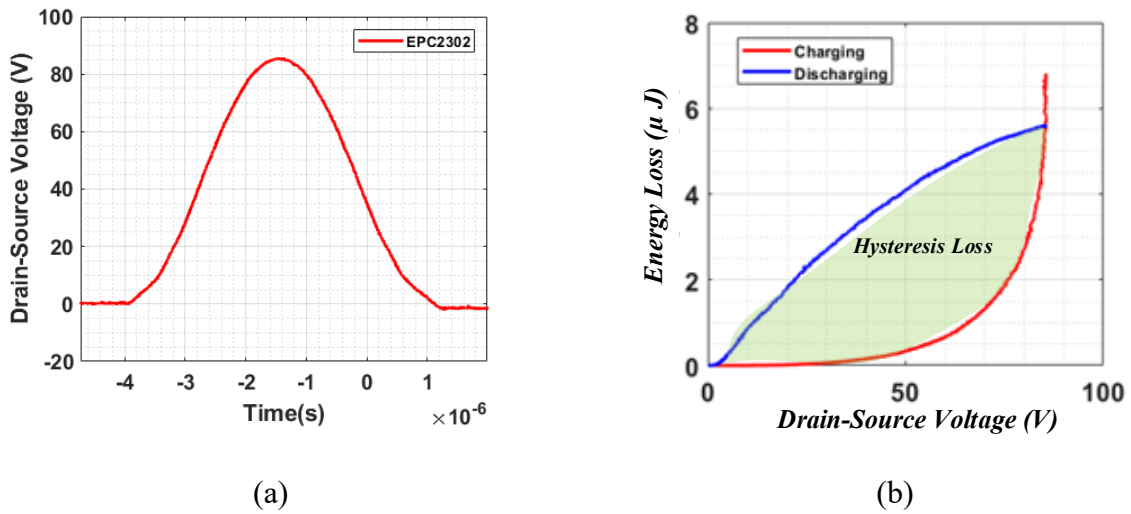


Fig. 3.32 (a) Drain-source voltage across the GaN FET EPC 2302 for inductor value of  $1mH$  and applied gate pulse of duration  $3\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

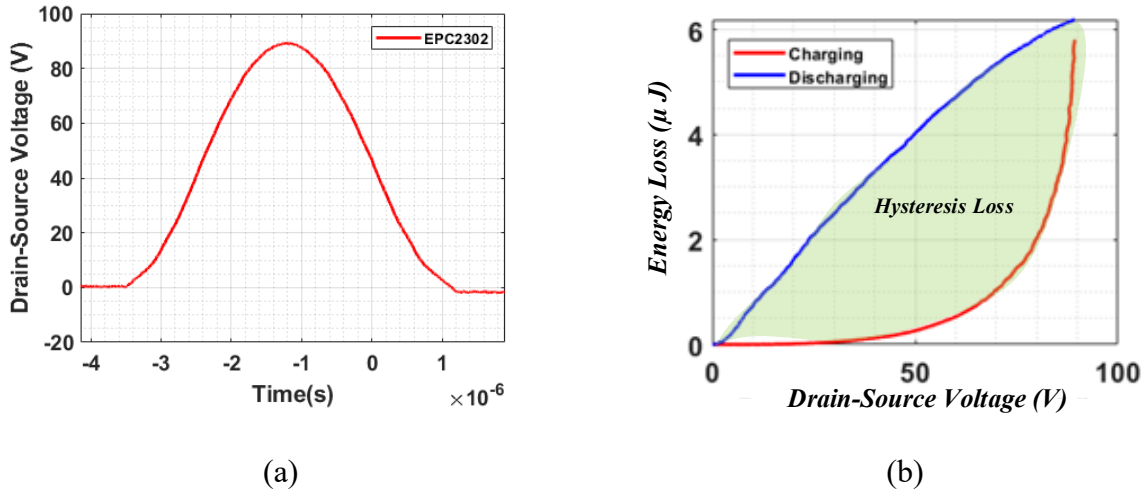


Fig. 3.33 (a) Drain-source voltage across the GaN FET EPC 2302 for inductor value of  $1mH$  and applied gate pulse of duration  $5\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

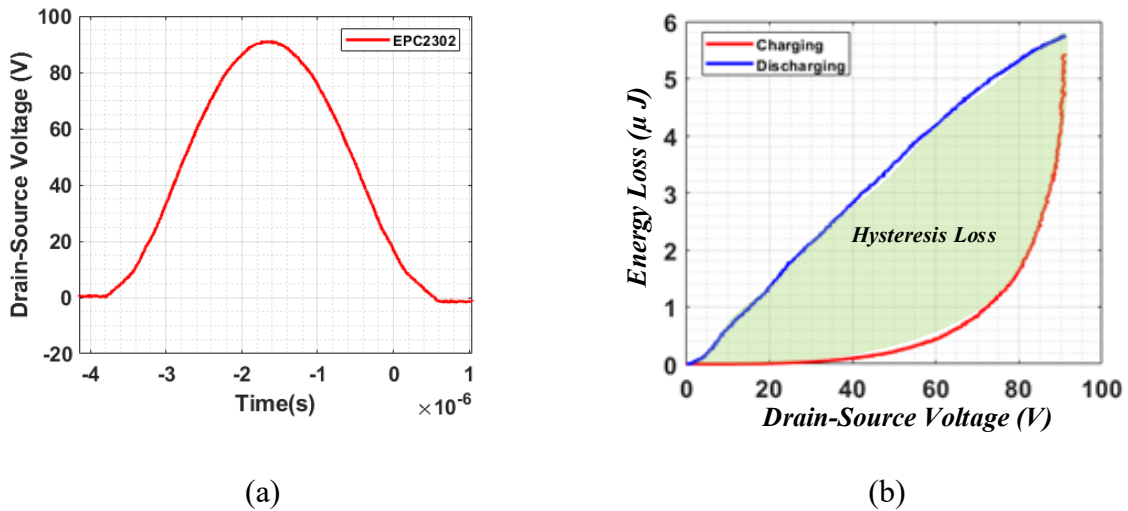


Fig. 3.34 (a) Drain-source voltage across the GaN FET EPC 2302 for inductor value of  $1mH$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

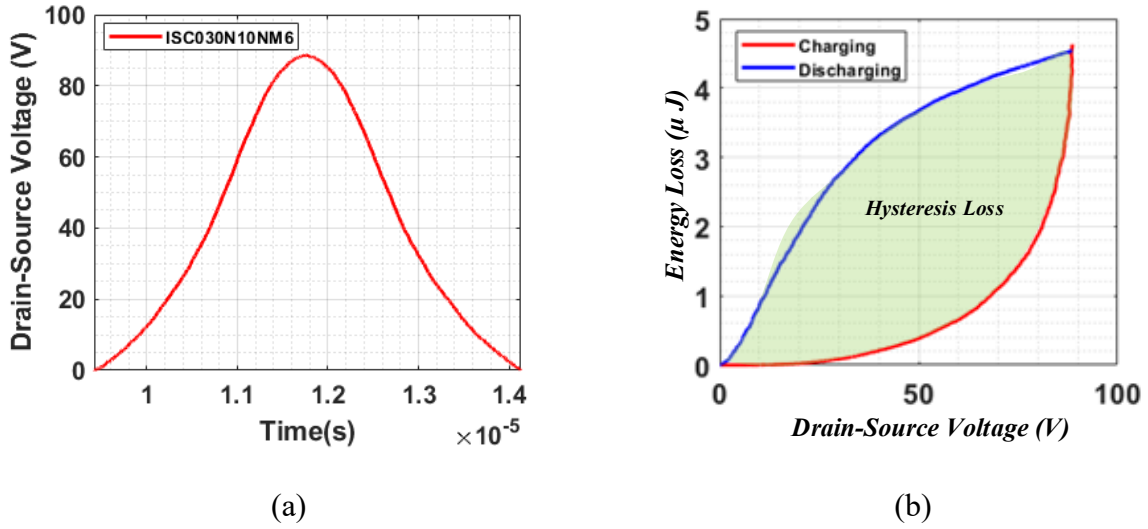


Fig. 3.35 (a) Drain-source voltage across the SI FET ISC030N10NM6 for inductor value of  $1mH$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

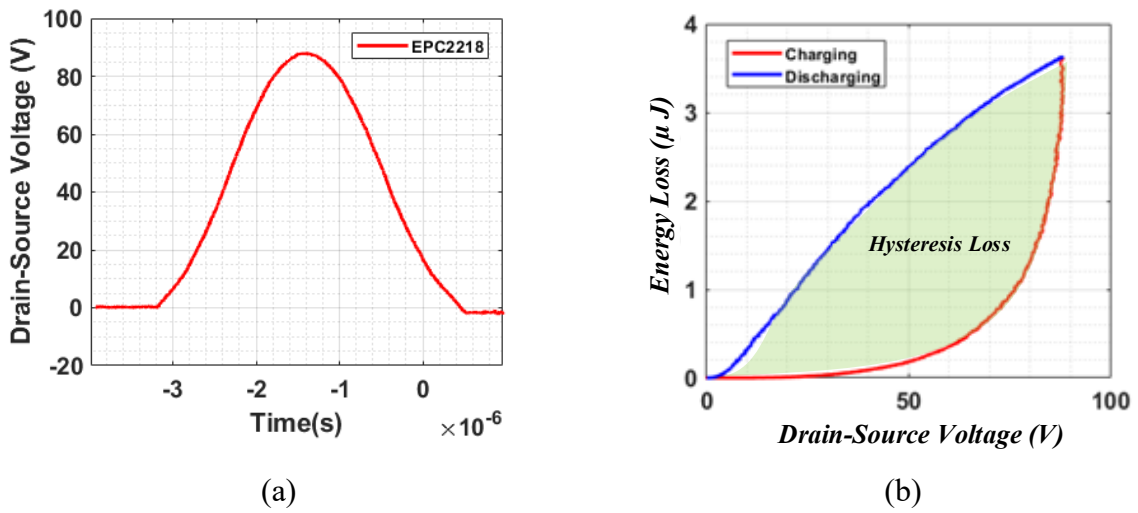


Fig. 3.36 (a) Drain-source voltage across the GaN FET EPC 2218 for inductor value of  $1mH$  and applied gate pulse of duration  $3\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

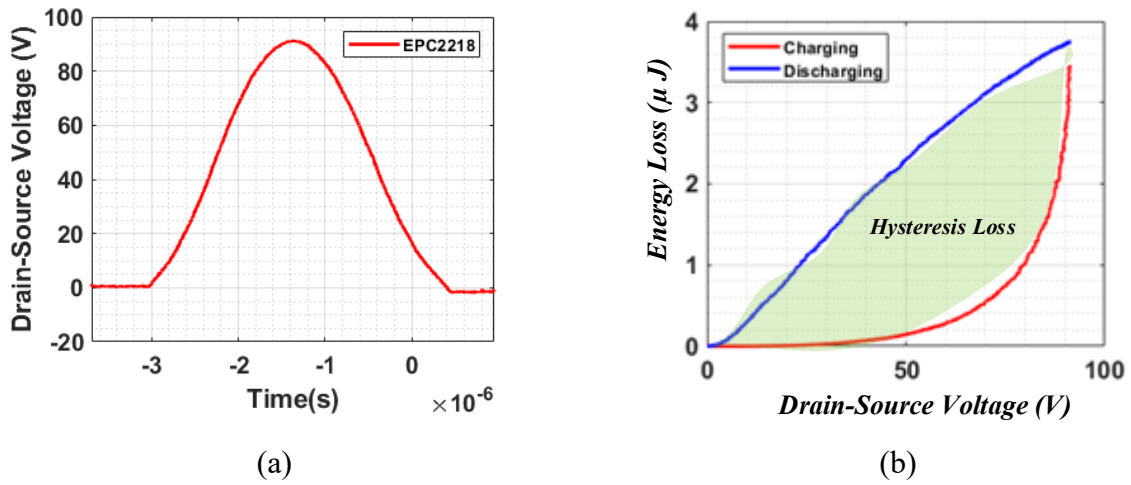


Fig. 3.37 (a) Drain-source voltage across the GaN FET EPC 2218 for inductor value of  $1mH$  and applied gate pulse of duration  $5\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

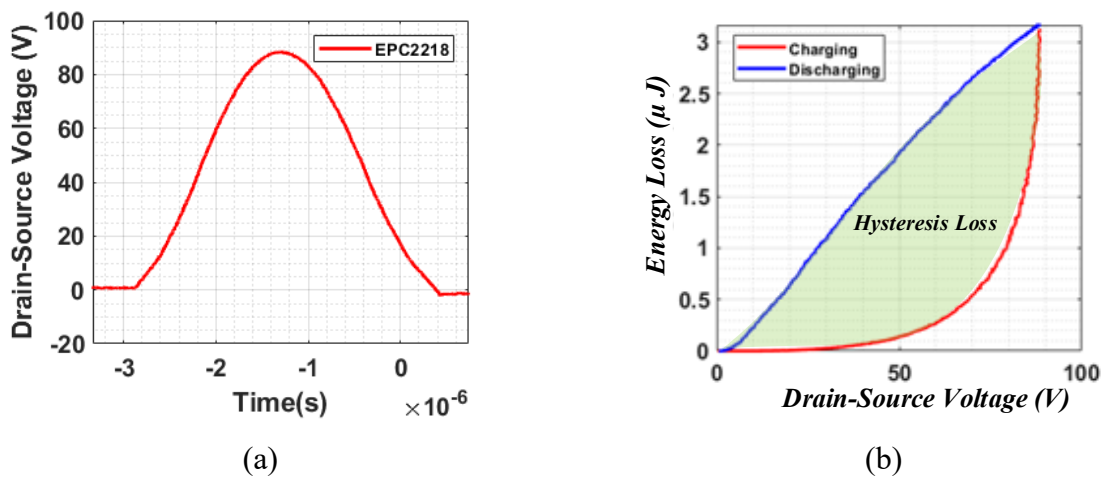


Fig. 3.38 (a) Drain-source voltage across the GaN FET EPC 2218 for inductor value of  $1mH$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

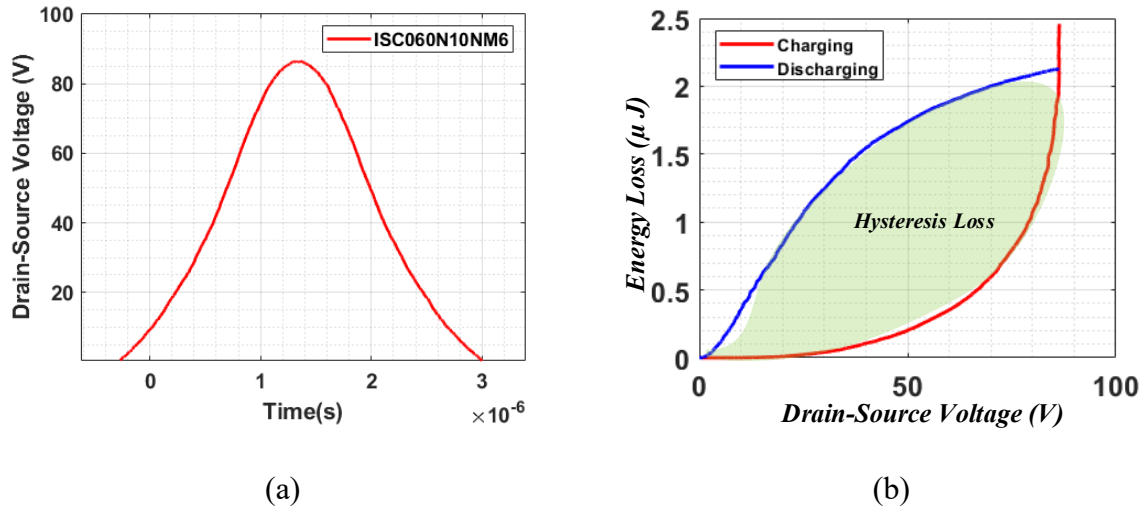


Fig. 3.39 (a) Drain-source voltage across the ISC060N10NM6 for inductor value of  $1mH$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

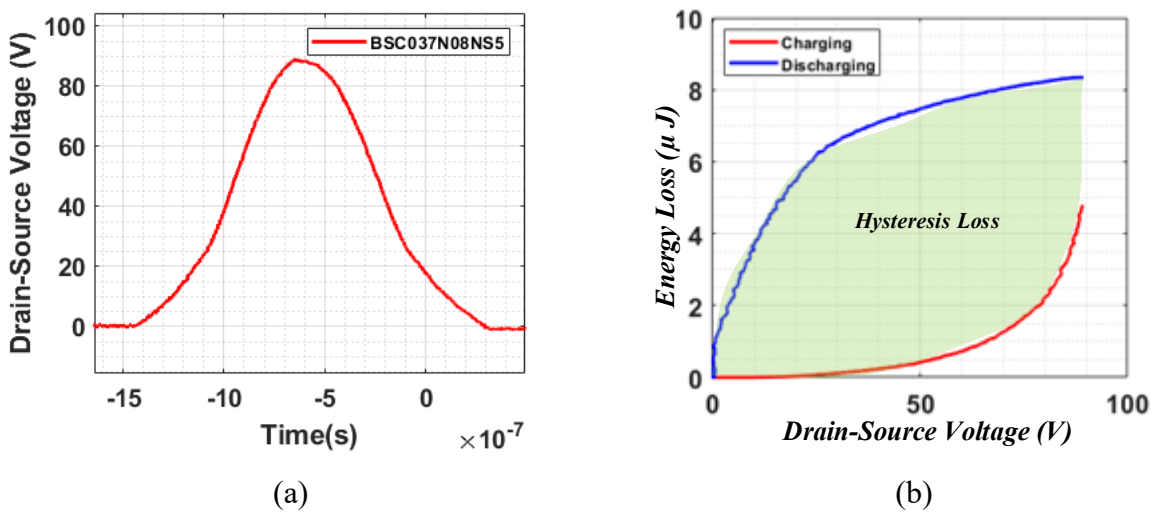


Fig. 3.40 (a) Drain-source voltage across the SI FET BSC037N08NS5 for inductor value of  $22\mu H$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

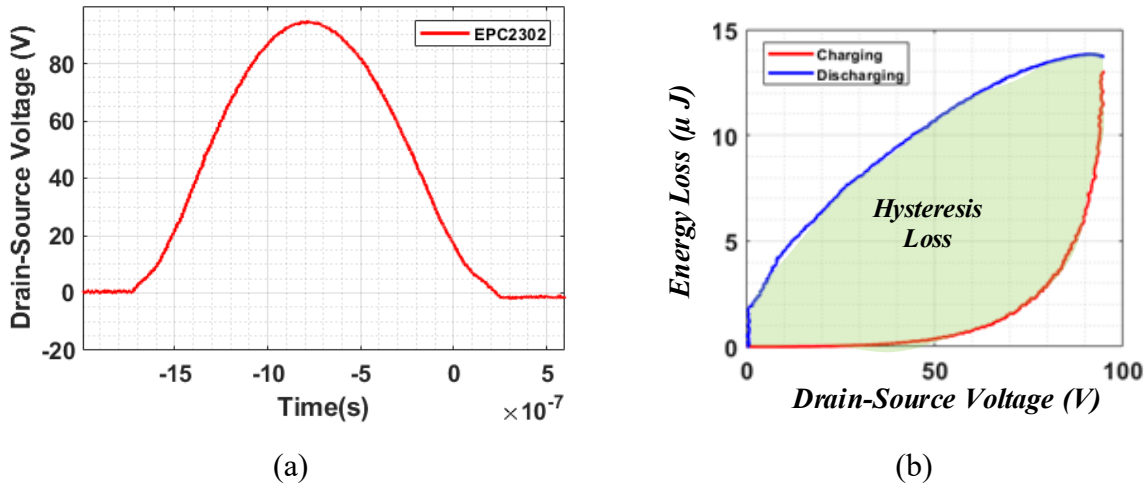


Fig. 3.41 (a) Drain-source voltage across the GaN FET EPC 2302 for inductor value of  $22\mu H$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

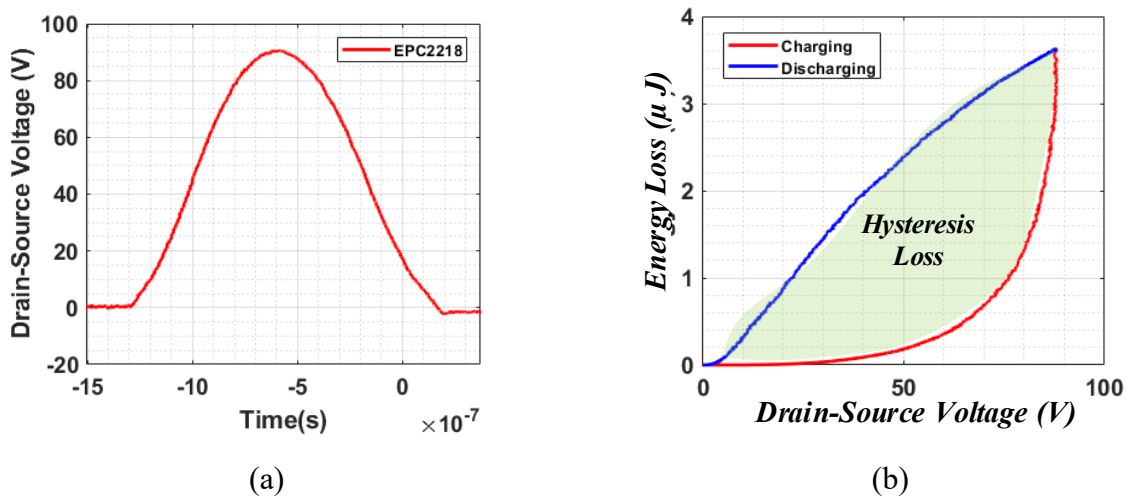
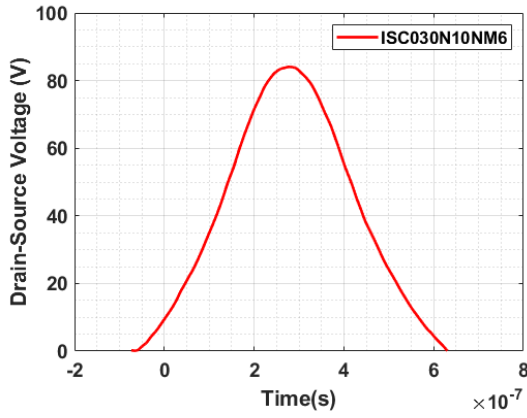
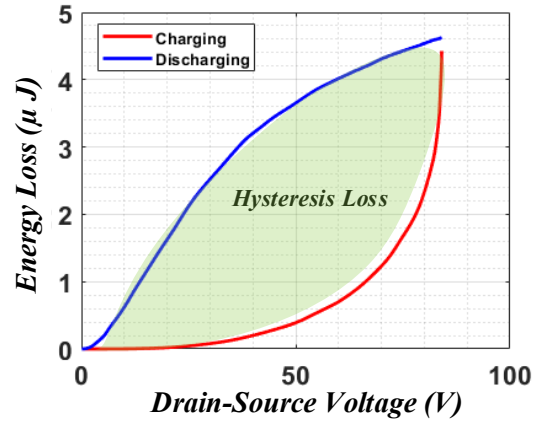


Fig. 3.42 (a) Drain-source voltage across the GaN FET EPC 2218 for inductor value of  $22\mu H$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

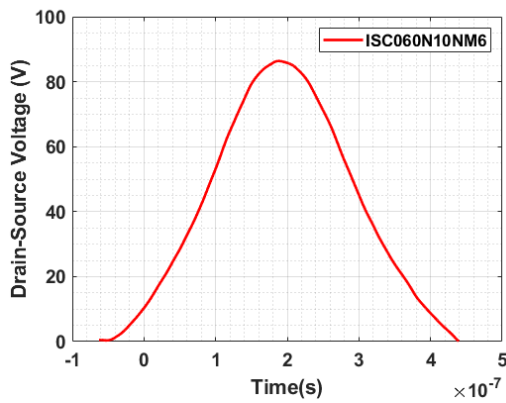


(a)

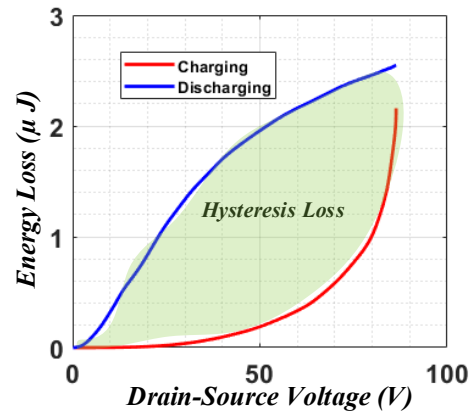


(b)

Fig. 3.43 (a) Drain-source voltage across the ISC030N10NM6 for inductor value of  $22\mu H$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.



(a)



(b)

Fig. 3.44 (a) Drain-source voltage across the ISC060N10NM6 for inductor value of  $22\mu H$  and applied gate pulse of duration  $10\mu s$ , (b) Energy loss in  $\mu J$  during charge/discharge cycle for the same FET.

NR test has been performed for five different devices (same as for calorimetric test) where we have measured the drain-source voltage for each DUT and computed the charge/discharge energies which are plotted adjacent to each  $V_{DS}$  waveform. These energies have been computed for different values of the inductor  $L$ , and the pulse duration applied to the gate of each DUT.

The results give a broad spectrum of energy loss in the  $C_{oss}$  depending upon the conditions mentioned above ( $L$ , and pulse duration). These results are tabulated and compared to the loss obtained in the calorimetric method in Table 3.3 and Table 3.4, respectively. We can conclude that the two methods are in accordance with each other as the SI device ISC060N10NM6 has minimal loss for both test methods.

Table 3.3 Energy loss comparison between Calorimetric and NR test method ( $10\mu s$  pulse, and inductor value of  $1mH$ )

Device Under Test (DUT)	Voltage (V)	Energy Loss in NR test ( $\mu J/cycle$ )	Energy Loss in Calorimetric test ( $\mu J/cycle$ )
BSC037N08NS5	80	1.2	1.44
ISC030N10NM6	100	2.3	2.21
ISC060N10NM6	100	1.3	1.29
EPC 2218	100	2.2	2.25
EPC 2302	100	3	2.50

Table 3.4 Energy loss comparison between Calorimetric and NR test method ( $10\mu s$  pulse, and inductor value of  $22\mu H$ )

Device Under Test (DUT)	Voltage (V)	Energy Loss in NR test ( $\mu J/cycle$ )	Energy Loss in Calorimetric test ( $\mu J/cycle$ )
BSC037N08NS5	80	6	1.44
ISC030N10NM6	100	10.5	2.21
ISC060N10NM6	100	3.75	1.29
EPC 2218	100	4.5	2.25
EPC 2302	100	10	2.50

# Chapter 4. Validation of Test Results on a 300W DC-DC Converter

## 4.1 Overview of a 300W DC-DC converter Test Board for SI FETs

A DC-DC converter has been developed and built to be used as a part of a PV optimizer, where an integrated boost resonant (IBR-Z)[31] topology has been adopted which provides the desired voltage gain and at the same time it provides galvanic isolation between the input and output for safety purposes.

This converter is used for the validation of the energy loss data we obtained using the two test methods (Calorimetric and NR method) for five different DUTs, out of these five, four devices are tested in this DC-DC converter for efficiency, and consequently, the losses occurring in the systems.

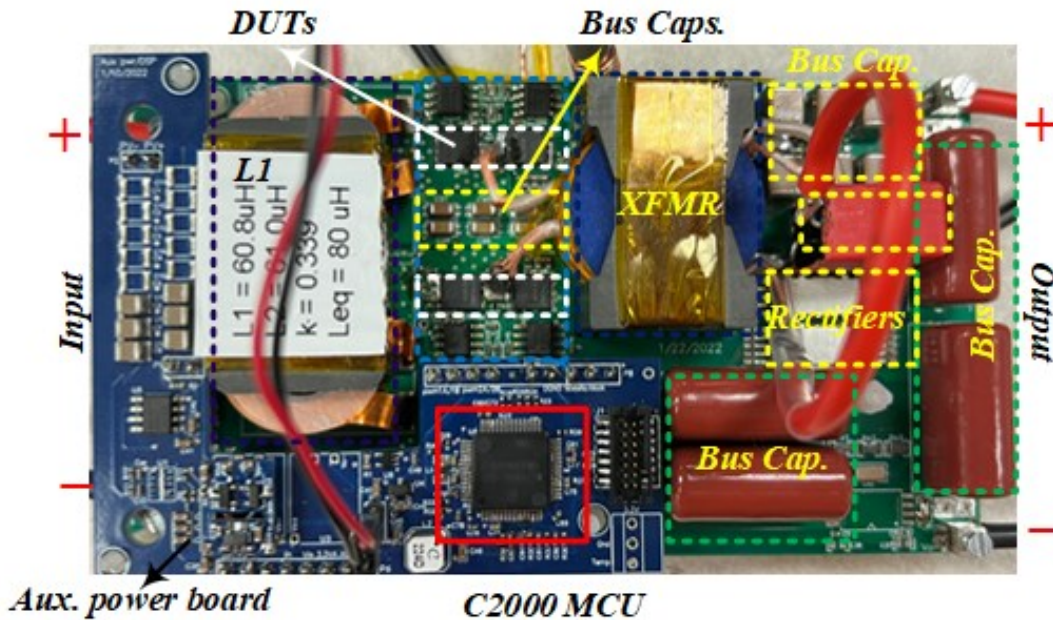


Fig. 4.1 DC-DC converter prototype for SI FET validation with its key components.

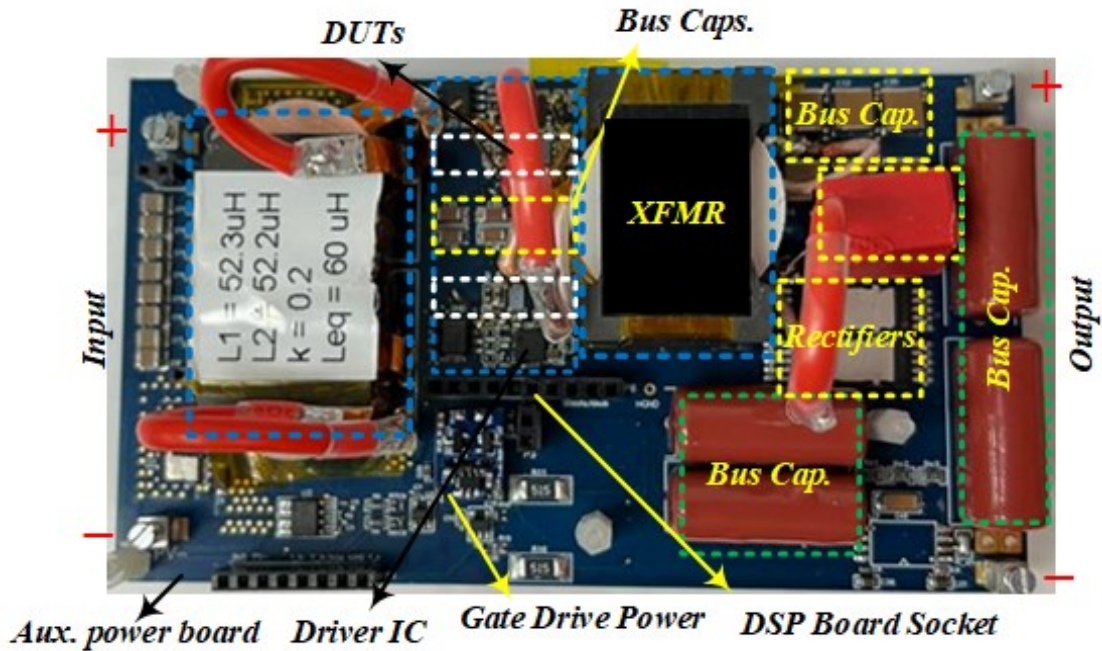


Fig. 4.2 DC-DC converter prototype for GaN FET validation with its key components.

Fig. 4.1 presents the experimental hardware prototype for the above-mentioned DC-DC converter which is used to evaluate SI FETs (BSC037N08NS5, ISC030N10NM6, ISC060N10NM6).

Fig. 4.2 presents the experimental hardware prototype for the DC-DC converter involving GaN FET, EPC 2218 (only 1 GaN FET has been evaluated for this prototype).

The main elements of the converter are highlighted in the above-cited figures, where we can observe that both have elements like input coupled inductor, gate drivers (UCC27211, LM5113), DUTs with different packages (landing patterns), transformer, silicon carbide diode rectifiers, resonant/DC blocking capacitors, DC bus capacitors.

The converter specifications are provided in Table 4.1 which are the same for the two different prototypes each for SI and GaN FET, and the component description is mentioned in Table 4.2.

Further, the values for the transformer and two coupled inductors (each for SI and GaN FET) are presented in Table 4.3, Table 4.5, and Table 4.6, respectively. These parameters are used for loss analysis for the given converter in section 4.4.

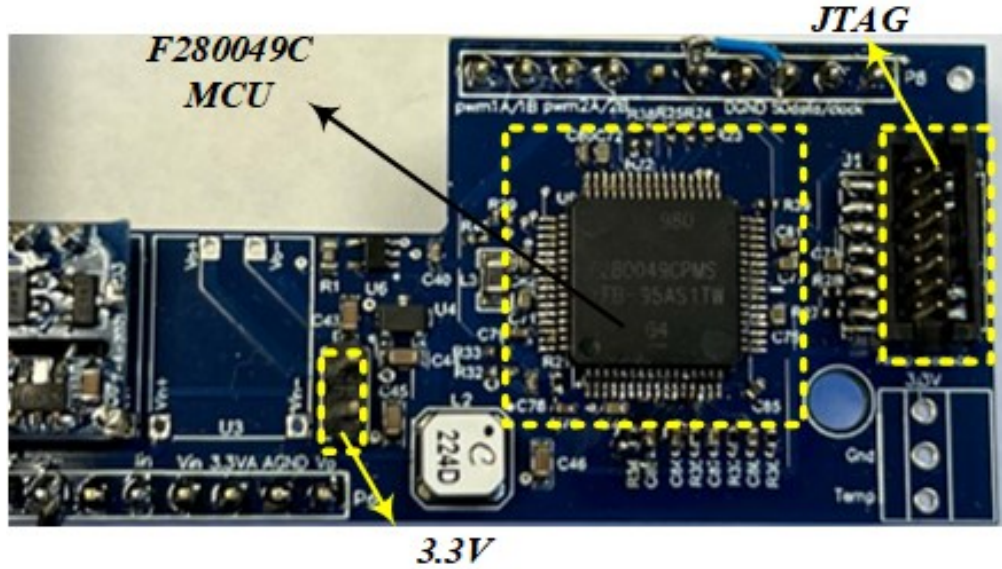


Fig. 4.3 DSP board for both DC-DC converters.

Table 4.1 Operating parameters for the DC-DC converter prototype (both SI and GaN FET).

Parameter	Value
Input Voltage	30-45V
Input Current	10A at Full Load
Output Voltage	350-380V
Output Current	0.8A at Full Load
Output Power	300W
Output capacitance	20 $\mu$ F
Switching Frequency	100 kHz
Dead-Time	50-80ns

Table 4.2 Description of key components used in both SI and GaN FET-based DC-DC converter prototype.

Components	Part Number	Manufacturer
80V DUT1	BSC037N08NS5	Infineon
100V DUT2	ISC030N10NM6	Infineon
100V DUT3	ISC060N10NM6	Infineon
100V DUT4	EPC2218	EPC
100V DUT5	EPC2302	EPC
Gate Driver 100V	LM5113	Texas Instruments
Gate Driver 100V	UCC27211	Texas Instruments
Isolators	ISO7420	Texas Instruments
SiC Rectifiers	IDH04G65C6	Infineon
MCU	TMS320F280049C	Texas Instruments

Table 4.3 Transformer parameters for DC-DC converter prototype with SI Devices

Parameter	Value
$L_{m1}$	31.2 $\mu\text{H}$
$L_{m2}$	206.1 $\mu\text{H}$
$L_{lk1}$	1.104 $\mu\text{H}$
$L_{lk2}$	7.28 $\mu\text{H}$
$DCR_{pri}$	0.03 $\Omega$
$DCR_{sec}$	0.10 $\Omega$
$ACR_{pri}$	0.046 $\Omega$
$ACR_{sec}$	0.039 $\Omega$

Table 4.4 Transformer parameters for DC-DC converter prototype with GaN Device

Parameter	Value
$L_{m1}$	28.4 $\mu\text{H}$
$L_{m2}$	192 $\mu\text{H}$
$L_{lk1}$	0.97 $\mu\text{H}$
$L_{lk2}$	6.58 $\mu\text{H}$
$DCR_{pri}$	0.03 $\Omega$
$DCR_{sec}$	0.10 $\Omega$
$ACR_{pri}$	0.051 $\Omega$
$ACR_{sec}$	0.047 $\Omega$

Table 4.5 Coupled inductor parameters for SI FET-based DC-DC converter prototype.

Parameter	Value
$L_1$	60.8 $\mu\text{H}$
$L_2$	61.0 $\mu\text{H}$
$L_{eq}$	80 $\mu\text{H}$
$DCR_{L1}$	0.03 $\Omega$
$DCR_{L2}$	0.03 $\Omega$
$ACR_{L1}$	0.585 $\Omega$
$ACR_{L2}$	0.577 $\Omega$

Table 4.6 Coupled inductor parameters for GaN FET-based DC-DC converter prototype.

Parameter	Value
$L_1$	52.3 $\mu\text{H}$
$L_2$	52.2 $\mu\text{H}$
$L_{eq}$	60 $\mu\text{H}$
$DCR_{L1}$	0.06 $\Omega$
$DCR_{L2}$	0.06 $\Omega$
$ACR_{L1}$	0.785 $\Omega$
$ACR_{L2}$	0.777 $\Omega$

## 4.2 Test Results of a 300W PV Optimizer Test Board with Different Switching Devices

The DC-DC converter prototype is tested at the power output of  $\sim 270W$  which is almost 75% of the total rated power, as the converter is expected to run mostly at this power level. The purpose of this test is to validate that there is a ZVS condition for the operation, compute the overall converter efficiency/losses ranging from light-load to full-load, perform loss breakdown, and validate it with the losses obtained through tests performed in Chapter 3 using the Calorimetric and NR method.

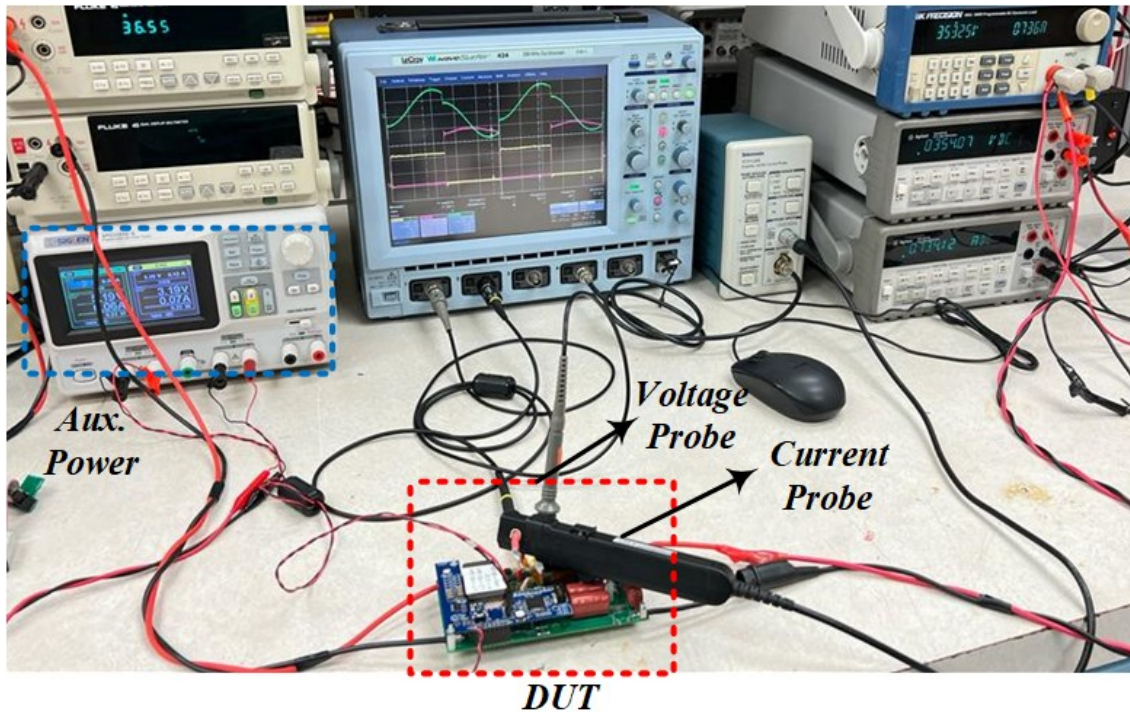
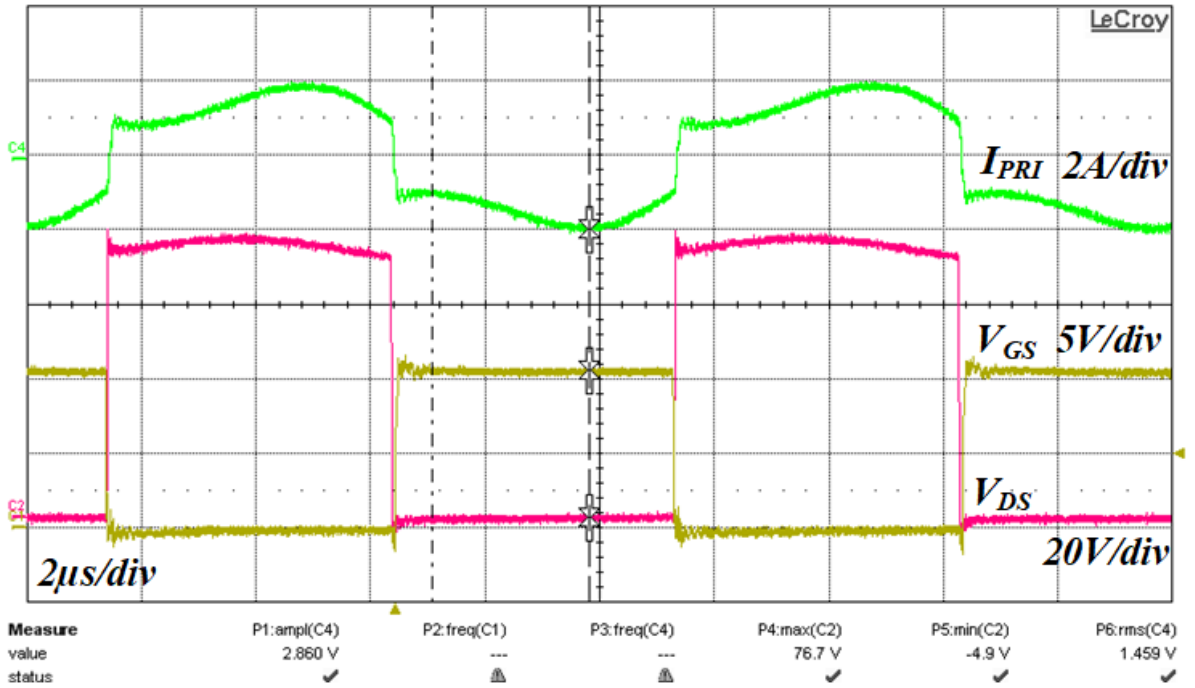
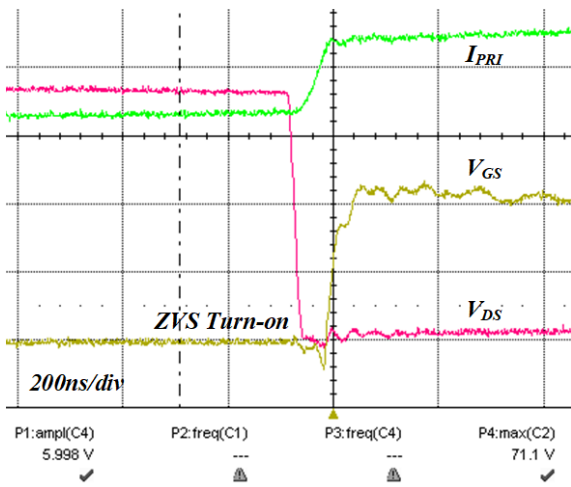


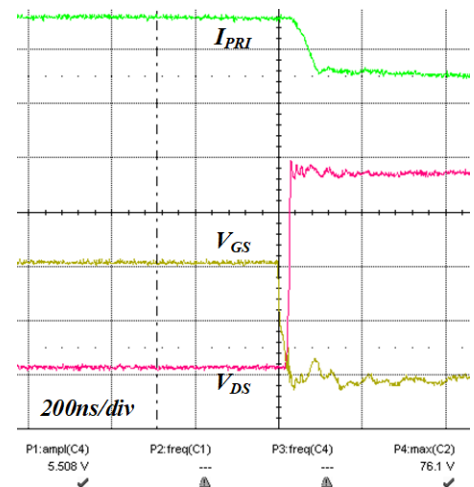
Fig. 4.4 Experimental test bench setup for the DC-DC converter to validate different DUTs.



(a)

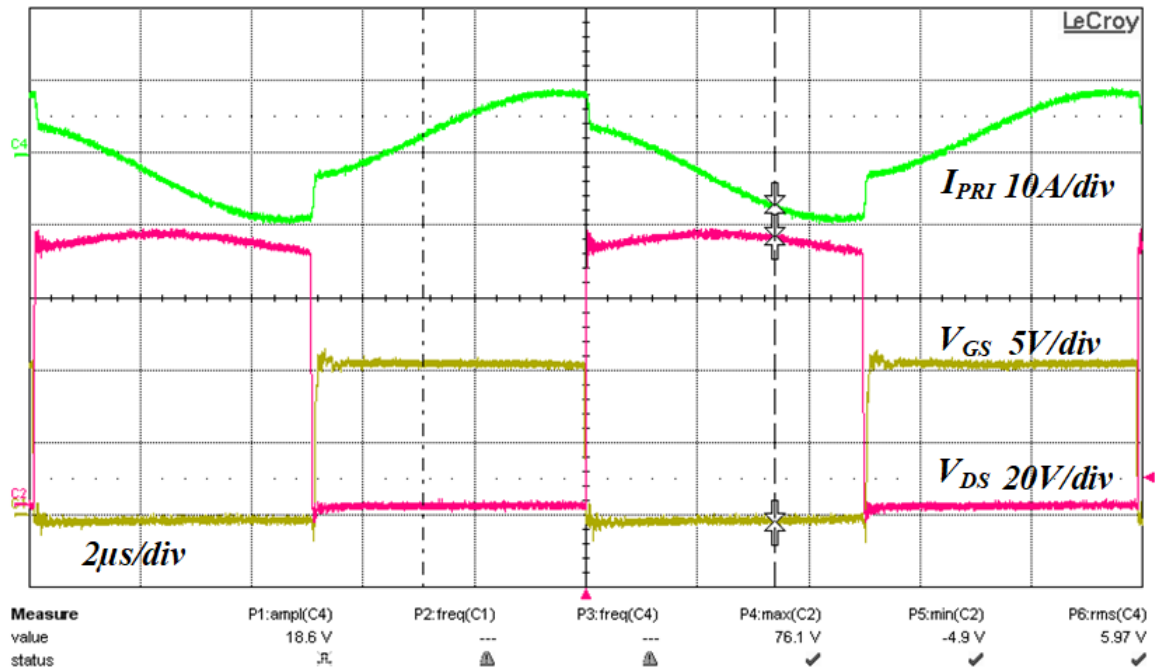


(b)

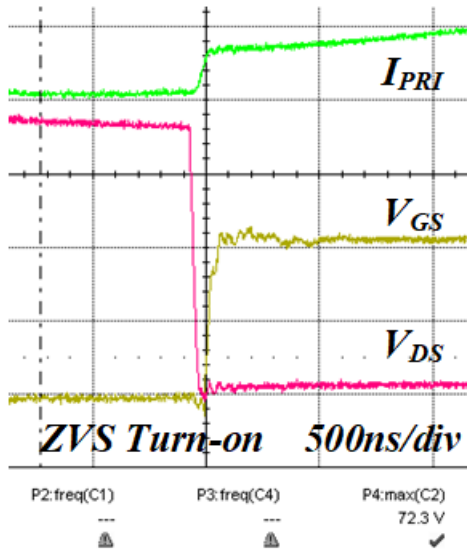


(c)

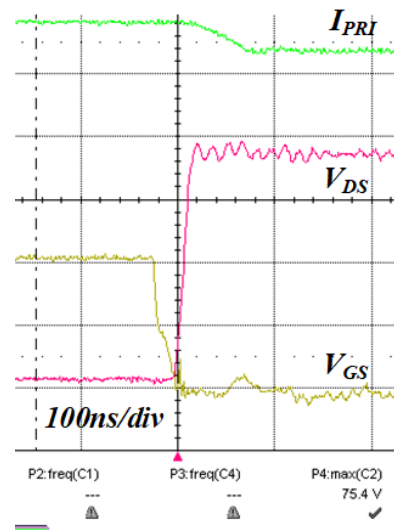
Fig. 4.5 Experimental test results for BSC037N08NS5 (a) steady-state waveforms for primary current through transformer winding, (b) ZVS turn-on shown for one low-side device (out of four), (c) hard turn-off for one low-side device (out of four).



(a)

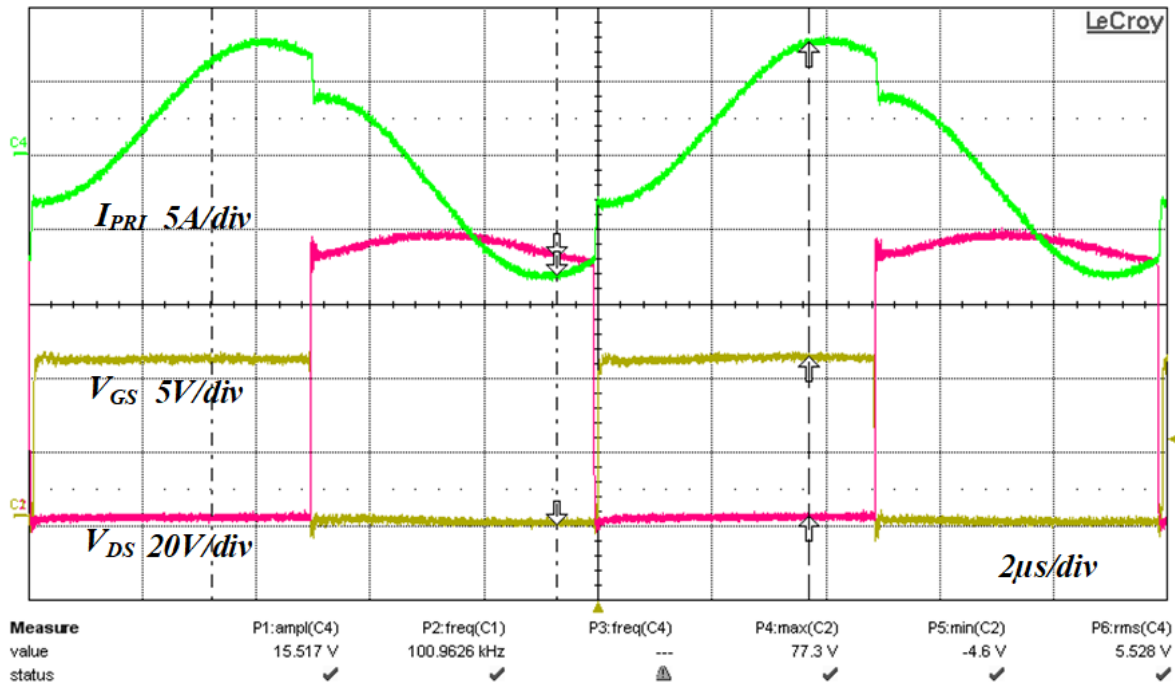


(a)

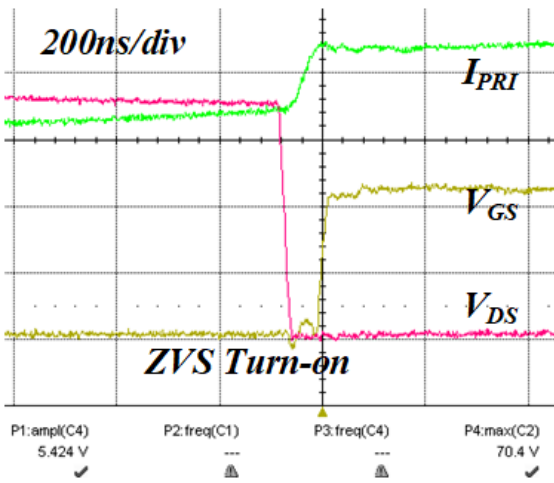


(b)

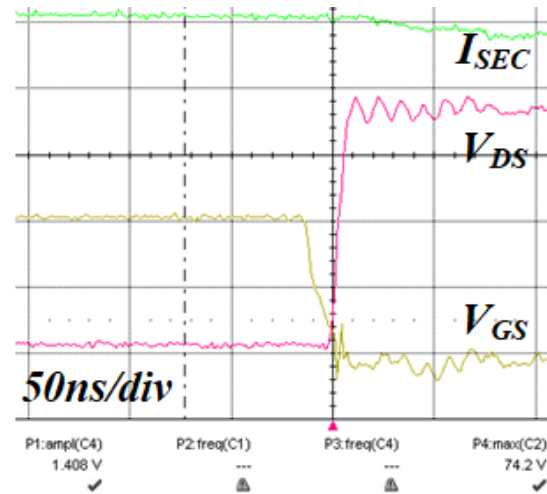
Fig. 4.6 Experimental test results for ISC030N10NM6 (a) steady-state waveforms for primary current through transformer winding, (b) ZVS turn-on shown for one low-side device (out of four), (c) hard turn-off for one low-side device (out of four).



(a)

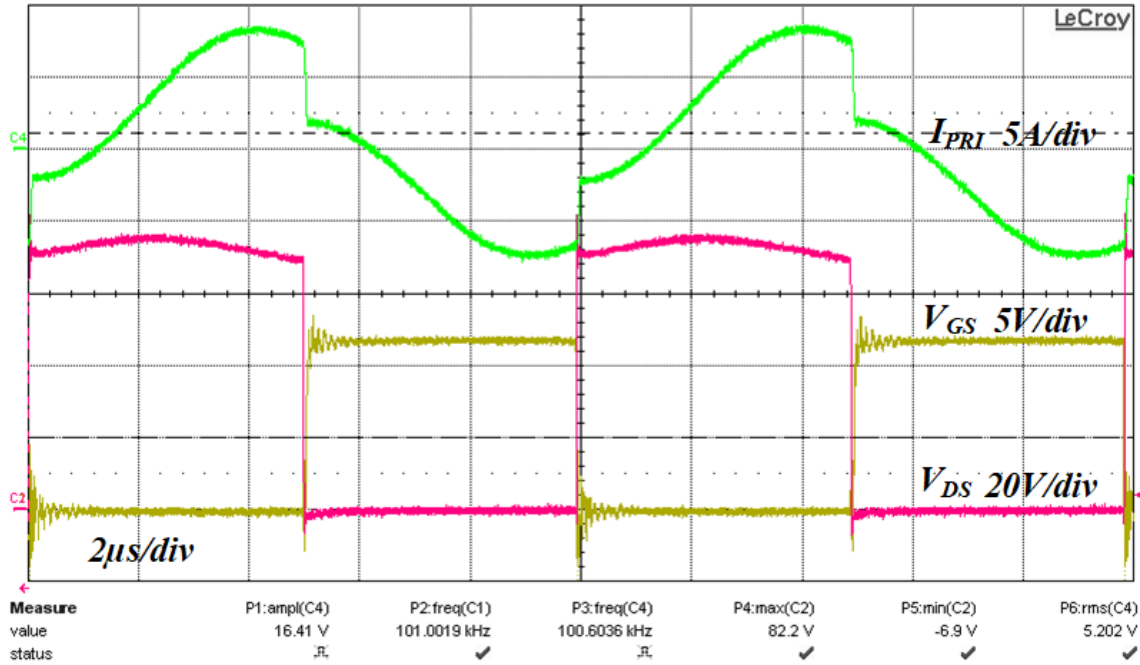


(b)

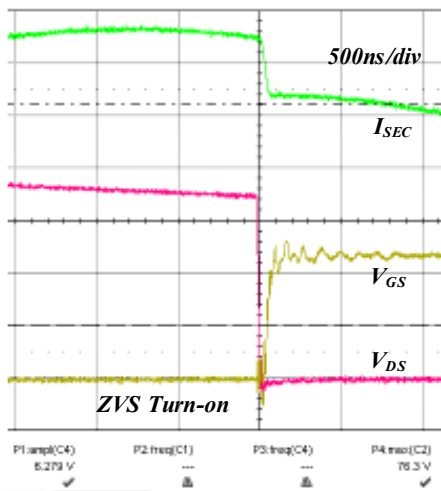


(b)

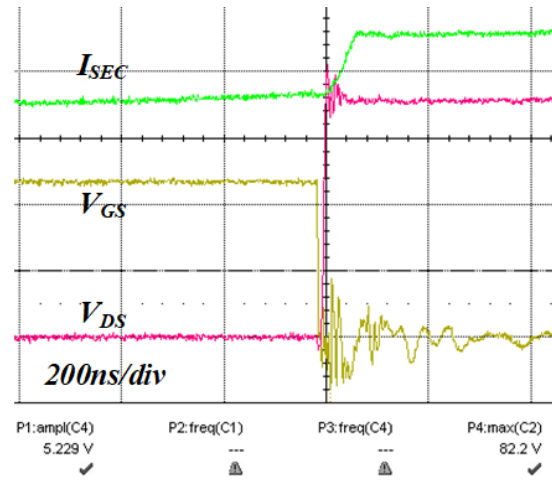
Fig. 4.7 Experimental test results for ISC060N10NM6 (a) steady-state waveforms for primary current through transformer winding, (b) ZVS turn-on shown for one low-side device (out of four), (c) hard turn-off for one low-side device (out of four).



(a)

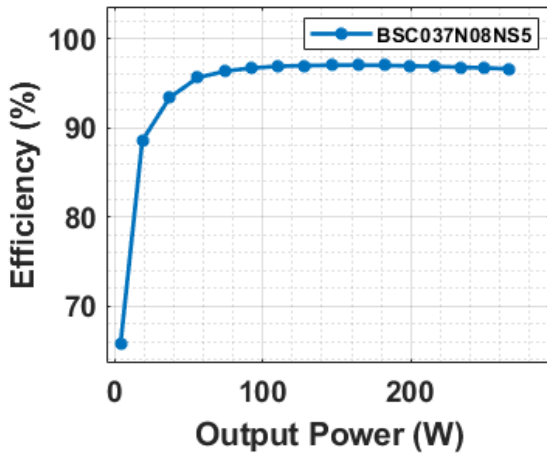


(a)

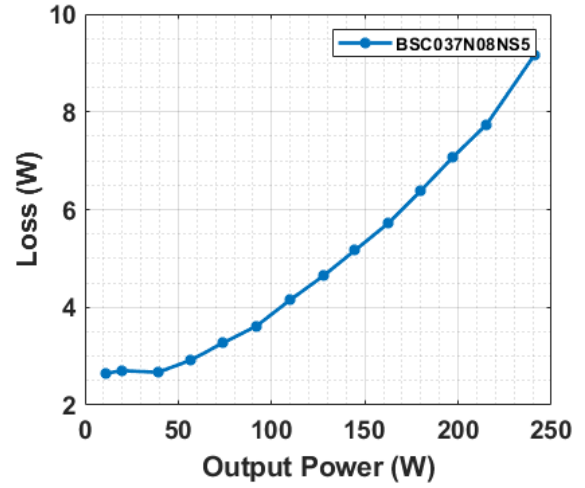


(b)

Fig. 4.8 Experimental test results for EPC2218 (a) steady-state waveforms for primary current through transformer winding, (b) ZVS turn-on shown for one low-side device (out of four), (c) hard turn-off for one low-side device (out of four).

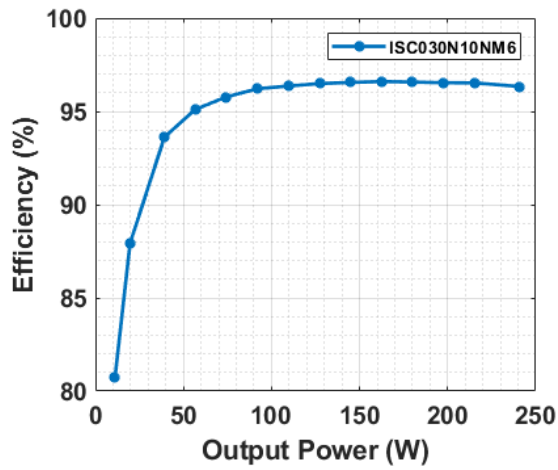


(a)

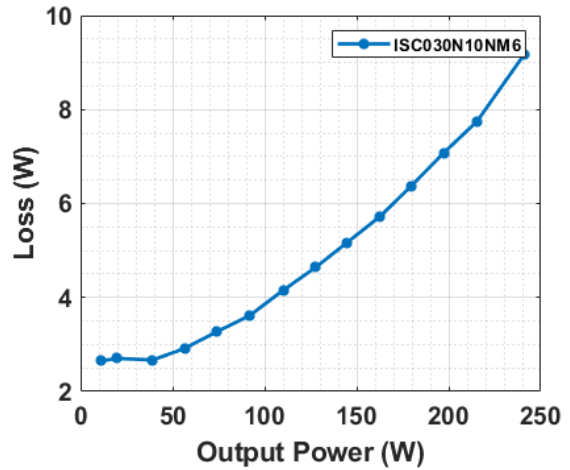


(b)

Fig. 4.9 Experimental test results for BSC037N08NS5 (a) Efficiency, (b) Loss, over a range of output power.

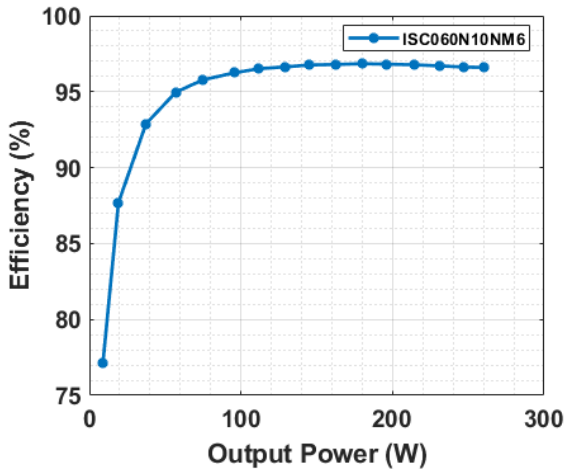


(a)

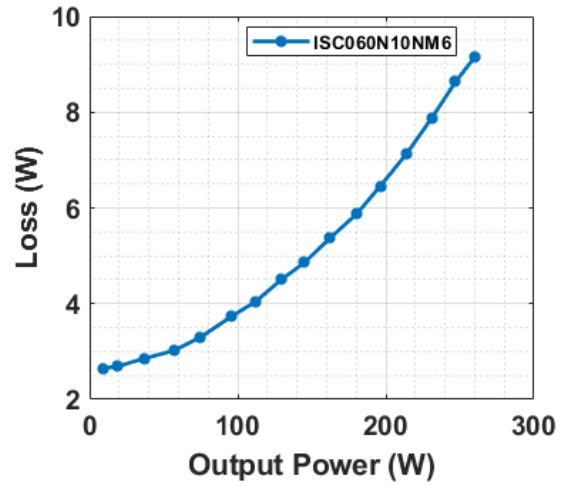


(b)

Fig. 4.10 Experimental test results for IS030N10NM6 (a) Efficiency, (b) Loss, over a range of output power.

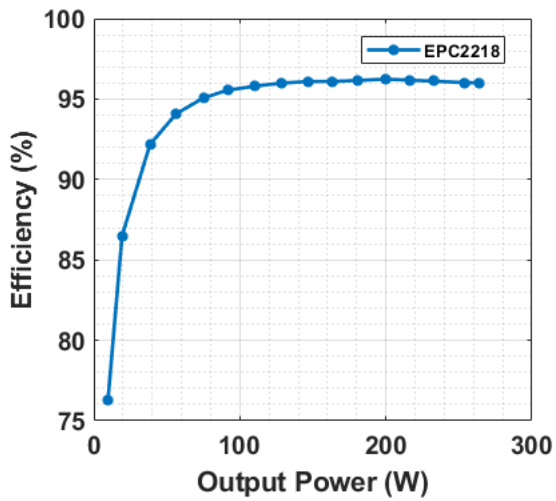


(a)

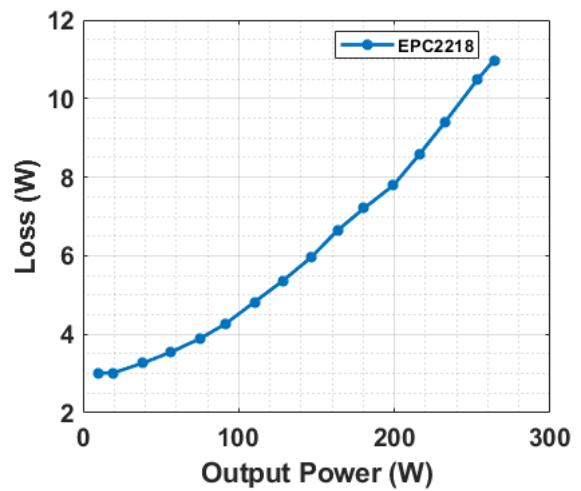


(b)

Fig. 4.11 Experimental test results for IS060N10NM6 (a) Efficiency, (b) Loss, over a range of output power.



(a)



(b)

Fig. 4.12 Experimental test results for EPC2218 (a) Efficiency, (b) Loss, over a range of output power.

### 4.3 Application and Validation of Test Results from Calorimetric and Non-Linear Resonance Test

The results obtained in Chapter 3 are used to validate and compute the switching loss breakdown (including the  $C_{OSS}$ -related hysteresis loss) for four different cases of DC-DC converter. The loss computation procedure is discussed in this section for these four different cases.

#### 4.3.1 FET-related switching losses

The switching loss in the FETs comprises three major elements, first,  $C_{OSS}$ -related hysteresis loss [20], loss during the dead time, and channel turn-off loss as for ZVS applications turn-on is loss-free but not turn-off [15].

First, we use the results obtained in Chapter 3 to get the calorimetric and NR test data for all devices being used in the DC-DC converter shown in Table 3.3 and the power loss during the  $C_{OSS}$  hysteresis can be computed as (4.1).

The dead-time power loss is shown in (4.2), where  $V_r$  is the reverse conduction voltage across the FET,  $T_d$  is dead-time duration,  $I_{inst}$  is the instantaneous current during the turn-off, there is a significant turn-off current through the channel and body diode, thus it is important to quantify this loss as it can be significant for GaN HEMTs due to non-zero source-drain  $V_{SD}$  voltage during body diode imitation mode.

$$P_{COSS,hys} = E_{COSS,hys}F_{sw} \quad (4.1)$$

$$P_{td} = V_r I_{inst} T_d \quad (4.2)$$

Finally, we can compute the channel turn-off loss (4.4) by subtracting the stored energy (from Chapter 3) in  $C_{OSS}$  from the total turn-off loss (4.3) where  $V_{off}$  is the voltage across

the FETs during turn-off process,  $I_{off}$  is the current through the FETs during turn-off, and  $E_{OSS,stored}$  is the stored energy in the device  $C_{OSS}$  during the charging process, which can be computed using (4.5) or the data from NR test.

$$E_{turn-off} = 0.5V_{off}I_{off}T_{off} \quad (4.3)$$

$$E_{ch,turn-off} = E_{turn-off} - E_{OSS,stored} \quad (4.4)$$

$$E_{OSS,stored} = \int_0^{V_{DS,max}} C_{OSS}(V_{DS})V_{DS}dV_{DS} \quad (4.5)$$

#### 4.3.2 FET related conduction losses

Conduction loss can contribute significantly towards the converter efficiency especially for low-voltage, high-current applications. The conduction loss can be computed for each the primary side device as (4.6), where  $I_{RMS,pri}$  is the primary side RMS current, and  $R_{DS,ON}$  is the on-state resistance of switching devices.

$$P_{FET,cond} = I_{RMS,pri}^2 R_{DS,ON} \quad (4.6)$$

#### 4.3.3 Transformer related losses

There are two major losses in a transformer, the first being core losses and the other being winding or conduction losses. We can divide the winding losses into two different categories, one due to the DCR of the windings and the other due to the ACR of windings, each for primary and secondary windings.

Skin effect can be eliminated by using litz wires of appropriate strands and the number of conductors [43], proximity effects can be present as interleaving has not been implemented for the design as it also impacts the leakage inductance, resulting in the reduction of available leakage without any interleaving [43].

An Mn-Zn-based ferrite core from Ferroxcube [39] is used to have high magnetic flux density in the core and reduce the core loss in the core. The air gap is introduced in the core to reduce the chances of magnetic saturation and control the magnetizing inductance well enough to achieve ZVS [40].

Core loss in the transformer can be presented by (4.7), where  $P_v$  is the core loss density for the given material at desired magnetic flux density  $B$ , switching frequency  $F_{sw}$ , and temperature  $T$ . The conduction loss can be expressed using (4.8) where  $I_{RMS,pri}$  is the RMS current through the primary windings,  $I_{RMS,sec}$  is the RMS current through the secondary windings,  $DCR_{pri}$  is the DC resistance of primary windings,  $DCR_{sec}$  is the DC resistance of secondary windings,  $ACR_{pri}$  is the AC resistance of primary windings at switching frequency  $F_{sw}$ ,  $ACR_{sec}$  is the AC resistance of secondary windings,  $V_e$  is the volume of the core, and  $P_{xfmr}$  is the total transformer related losses. Total transformer-related losses are given by (4.9).

$$P_{core\_xfmr} = P_v V_e \quad (4.7)$$

$$P_{cond} = I_{RMS,pri}^2 (DCR_{pri} + ACR_{pri}) + I_{RMS,sec}^2 (DCR_{sec} + ACR_{sec}) \quad (4.8)$$

$$P_{xfmr} = P_{core} + P_{cond} \quad (4.9)$$

#### 4.3.4 Inductor related losses

The input coupled inductor exhibited AC flux in its core thus there is a core loss associated with the core material, and there is a winding loss in the two different windings

of the inductor. A high flux density, low core loss material [41] has opted for the design of an input-coupled inductor.

The conduction loss is expressed in (4.10), where  $I_{RMS,L1}$  is the RMS current through the inductor 1 windings,  $I_{RMS,L2}$  is the RMS current through the inductor 2 windings,  $DCR_{L1}$  is the DC resistance of inductor 1 winding,  $DCR_{L2}$  is the DC resistance of inductor 2 windings,  $ACR_{L1}$  is the AC resistance of inductor 1 winding at the switching frequency  $F_{sw}$ ,  $ACR_{L2}$  is the AC resistance of inductor 2 windings, and  $P_{condL}$  is the total conduction loss in the coupled inductor.

For the core losses, the core data is used to obtain core loss density  $P_{vL}$  of the material for the given switching frequency, and flux density  $B$  shown in (4.11).

$$P_{condL} = I_{RMS,L1}^2(DCR_{L1} + ACR_{L1}) + I_{RMS,L2}^2(DCR_{L2} + ACR_{L2}) \quad (4.10)$$

$$P_{core\_L} = P_{vL}V_{eL} \quad (4.11)$$

#### 4.3.5 Rectifier related losses

Rectifiers in a converter contribute to significant conduction loss due to large forward-voltage drop  $V_f$  which is multiplied by the amount of current going through the diode to get the total conduction loss, apart from the conduction losses we also have reverse recovery losses in conventional diode rectifiers which can contribute to losses equivalent to that of conduction losses. In this design, we incorporated a SiC Schottky rectifier diode with zero reverse recovery which helps to mitigate the losses due to the reverse recovery phenomenon and improve the overall efficiency of the converter. The only loss element in the SiC Schottky rectifier diode is the capacitive loss which is not significant compared to the conduction losses.

The conduction and capacitive loss are shown in (4.12), (4.12) and (4.13) where,  $V_f$  is the forward voltage-drop of SiC Schottky diode,  $I_{sec}$  is the RMS current going through the diode,  $E_c$  is the energy stored in junction-capacitor of the diode, and  $F_{sw}$  is the switching frequency.

$$P_{Cond,rect} = V_f I_{sec} \quad (4.12)$$

$$P_{qc,rect} = E_c F_{sw} \quad (4.13)$$

#### 4.3.6 Clamping capacitor-related losses

There are two sets of capacitors that are used for clamping the input of the transformer to either input voltage or ground, depending on the operating modes of the converter [31]. These capacitors carry the half of RMS current as the primary winding of the transformer; thus, it is important to compute the loss occurring in two capacitors shown in (4.14), where  $R_{ESR1}$  and  $R_{ESR2}$  are the equivalent series resistances of these two capacitors which are almost equal, and  $I_{rms,pri}$  is the primary side RMS current.

$$P_{Cbus} = \left(\frac{I_{rms,pri}}{2}\right)^2 R_{ESR1} + \left(\frac{I_{rms,pri}}{2}\right)^2 R_{ESR2} \quad (4.14)$$

#### 4.3.7 Miscellaneous losses

These losses are negligible but still need to be accounted for. They occur mainly due to the resistance of the PCB traces, the inductance of the traces, and the capacitance in between the layers which gives rise to capacitive currents in the board. The average miscellaneous loss for the SI FET-based DC-DC converter is  $\sim 60mW$  whereas, for the

GaN FET-based converter, it is  $\sim 300mW$  due to different layouts and the parasitics involved with the board.

Using the loss elements mentioned above, a loss-breakdown has been presented for total losses, switching losses (using calorimetric and NR test data), and transformer-related losses. This loss break-down is presented in a subsequent section.

#### **4.4 Loss Breakdown for a 300W DC-DC converter**

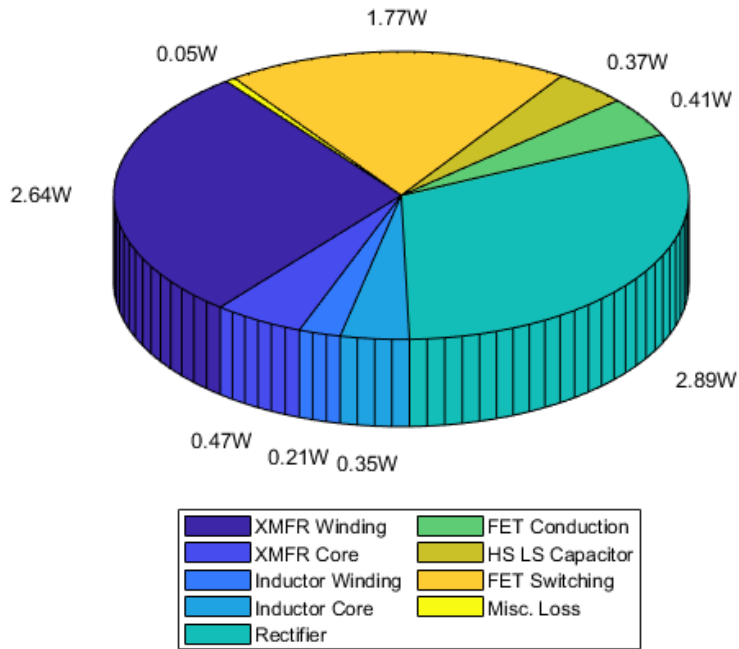
The loss elements are identified in the given DC-DC converter and are analyzed for individual contributions to the total loss in the converter. These loss elements are identified as, transformer core and winding losses, FET switching loss can be classified into three different loss elements namely,  $C_{oss}$ -related hysteresis loss, dead-time related loss, and channel conduction loss; other loss elements are inductor core and winding losses, rectifier conduction and capacitive losses, FET conduction losses, input side bus capacitor losses, and some miscellaneous losses due to PCB parasitics. These loss elements are evaluated for different DUTs, to justify the loss occurring in the converter.

Fig. 4.13 presents the loss breakdown for the DC-DC converter employing SI FET BSC037N08NS5 having a total measured loss of  $9.18W$  and calculated loss of  $9.14W$  with accuracy of 99.5% or an error rate of 0.5% which can be attributed to the miscellaneous losses due to PCB parasitics like stray inductance of the traces and capacitance between the traces.

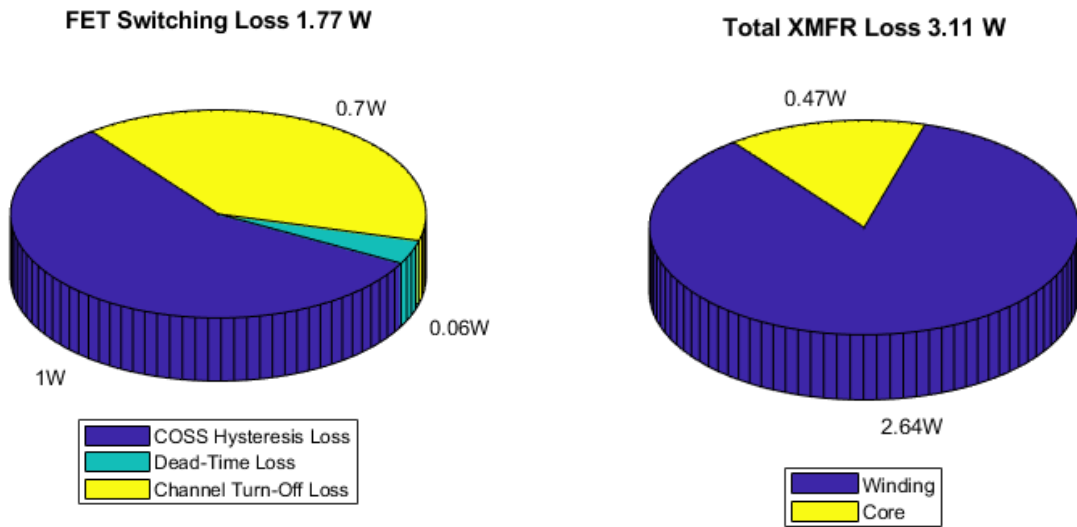
Fig. 4.14 presents the loss breakdown of the DC-DC converter employing SI FET ISC060N10NM6 having a total measured loss of  $9.15W$  and calculated loss of  $9.12W$  with accuracy of 99.5% or an error rate of 0.5% which can be attributed to miscellaneous losses due to PCB parasitics. Fig. 4.15 presents the loss breakdown of the DC-DC converter employing SI FET

ISC030N10NM6 having a total measured loss of  $9.16W$  and calculated loss of  $9.10W$  with accuracy of 99.4% or an error rate of 0.6% which can be attributed to miscellaneous losses due to PCB parasitics.

Fig. 4.16 presents the loss breakdown of the DC-DC converter employing GaN FET EPC 2218 having a total measured loss of  $10.98W$  and calculated loss of  $10.90W$  with accuracy of 99.7% or an error rate of 0.7% which can be attributed to a different PCB layout for GaN FET and miscellaneous losses due to PCB parasitics. The loss analysis principle can be used to get an estimate of losses that may occur in a hardware prototype for the FET-related switching loss, incorporating  $C_{oss}$ -related hysteresis.



(a)

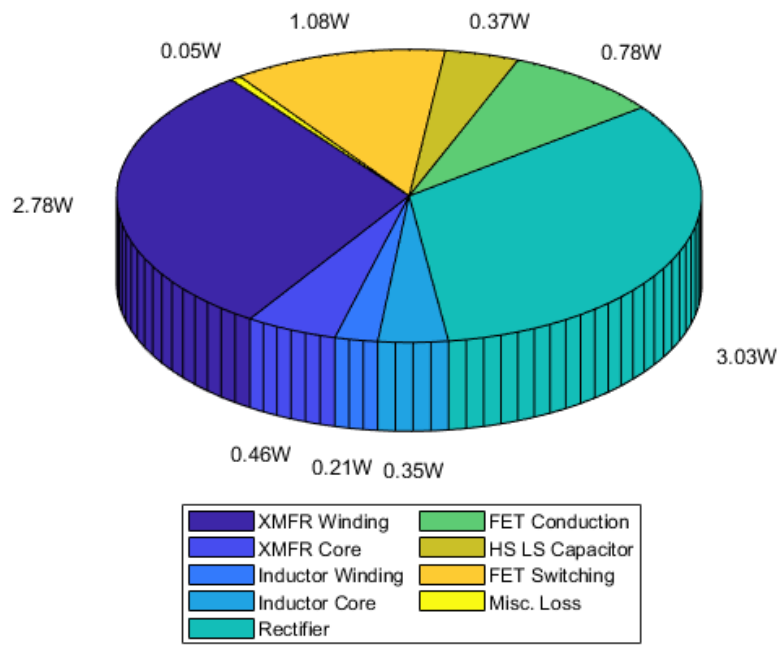


(b)

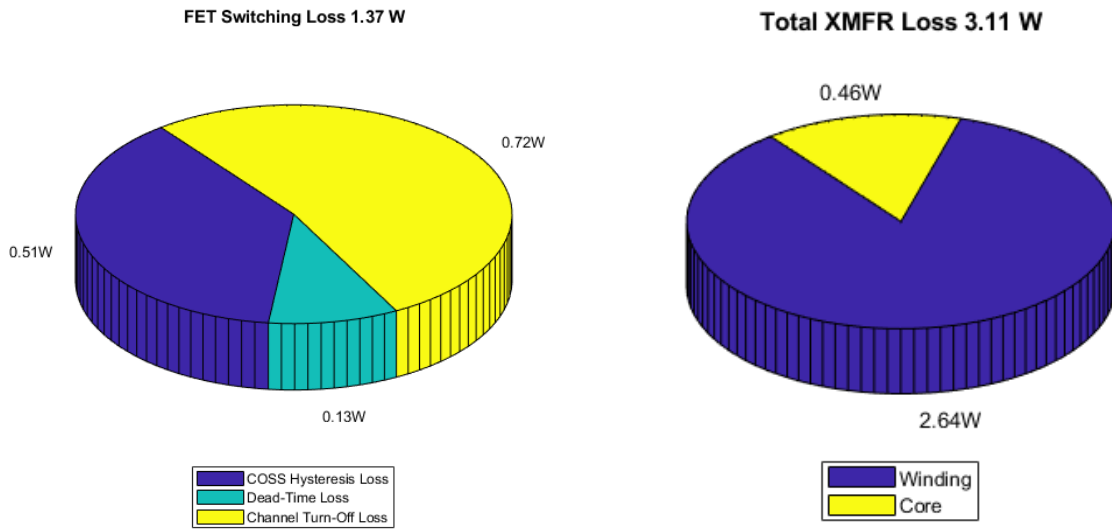
(c)

Fig. 4.13 Loss breakdown for the DC-DC converter incorporating SI FET BSC037N08NS5,

(a) Total loss 9.18W, (b) FET switching loss 1.77W, (c) Transformer loss 3.11W.



(a)

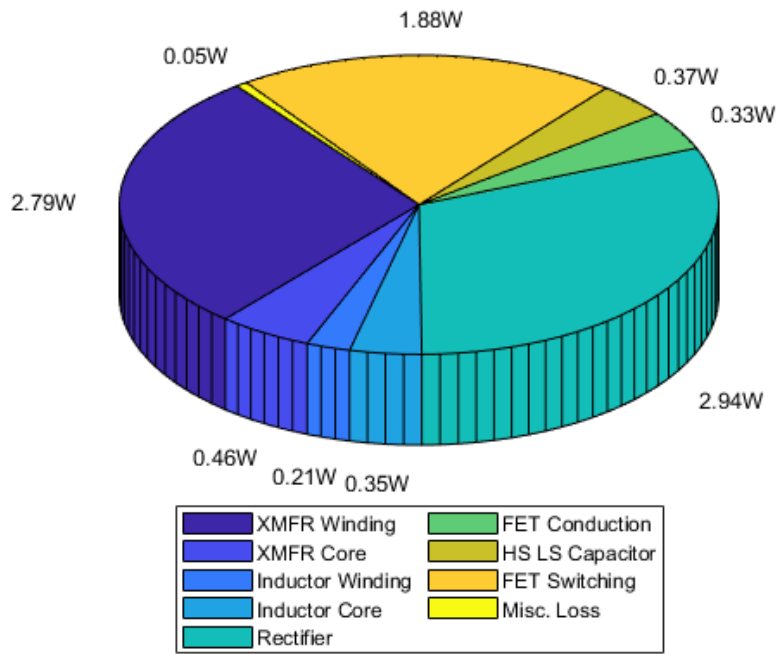


(b)

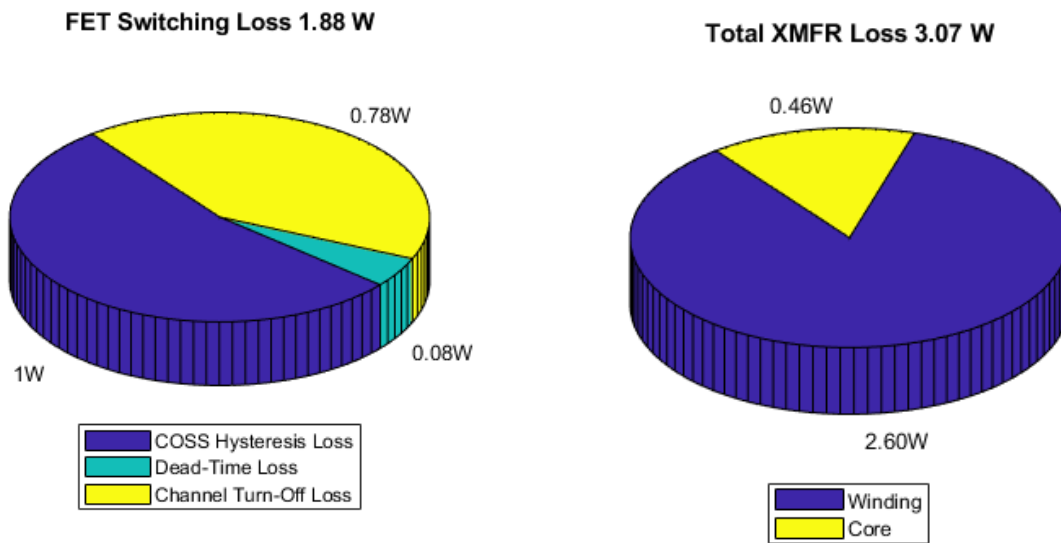
(c)

Fig. 4.14 Loss breakdown for the DC-DC converter incorporating SI FET ISC060N10NM6,

(a) Total 9.12W, (b) FET switching loss 1.37W, (c) Transformer loss 3.11W.



(a)

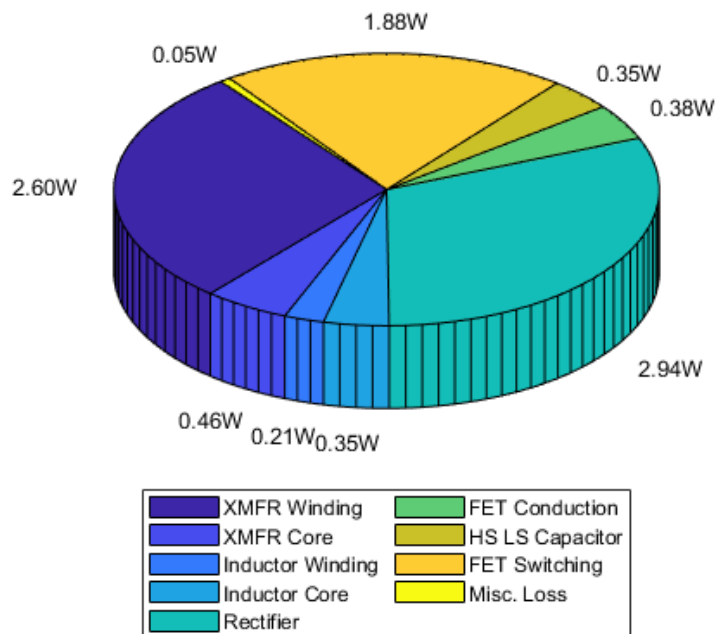


(b)

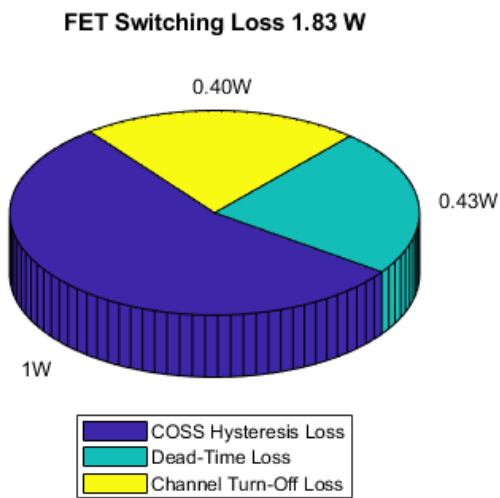
(c)

Fig. 4.15 Loss breakdown for the DC-DC converter incorporating SI FET ISC030N10NM6,

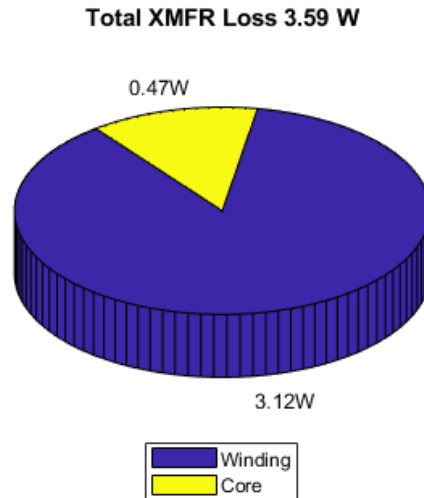
(a) Total loss 9.10W, (b) FET switching loss 1.88W, (c) Transformer loss 3.07W.



(a)

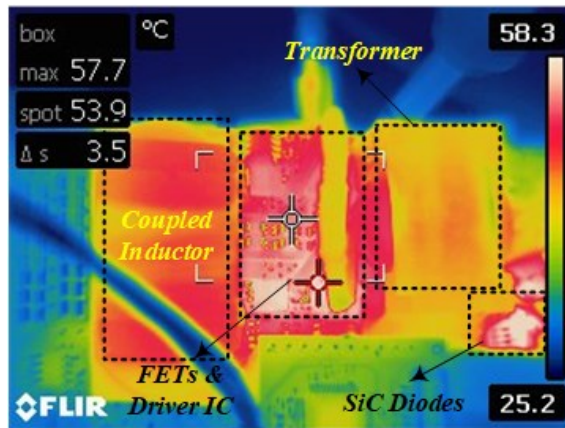


(b)

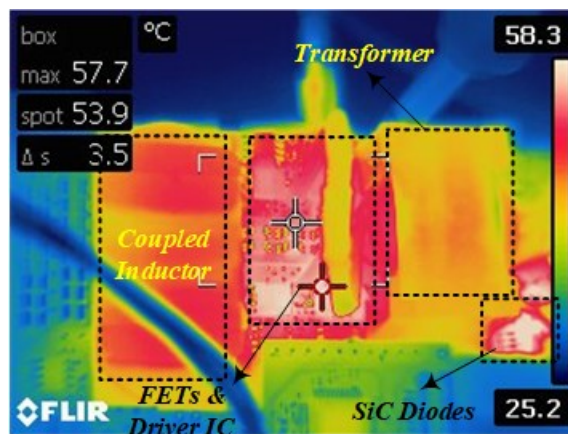


(c)

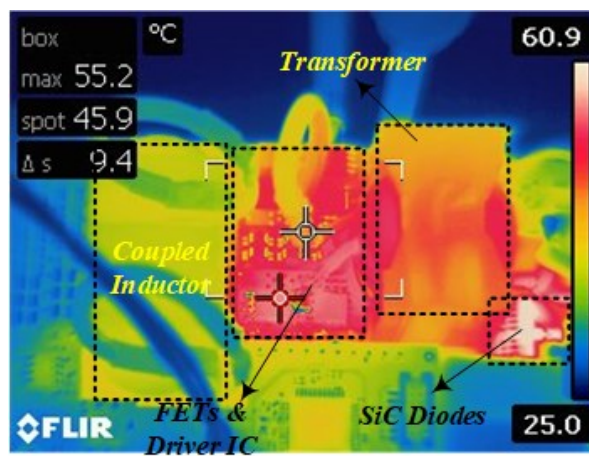
Fig. 4.16 Loss breakdown for the DC-DC converter incorporating GaN FET EPC 2218, (a) Total computed loss 10.90W, (b) FET switching loss 1.83W, (c) Transformer loss 3.59W.



(a)



(b)



(c)

Fig. 4.17 Temperature measurement for the DC-DC converter at ~270W for three silicon devices a) BSC037N08NS5 (b) ISC060N10NM6, (c) ISC030N10NM6.

Fig. 4.17 shows the temperature rise for the three different DUTs when operating at steady-state without any forced cooling, (a) is the SI FET rated for 80V and an on-state resistance of  $3.7m\Omega$ , which shows a temperature rise on the region where devices are soldered, this temperature rise is mainly due to the conduction losses occurring in the device, similarly for the (b) the device has even higher on-state resistance of  $6.1m\Omega$  which means there would be higher conduction losses but smaller losses related to the  $C_{OSS}$  of the device, for the part (c) the temperature rise for the devices is little as the on-state resistance  $3m\Omega$  is smallest of the two other devices, which will increase the  $C_{OSS}$  related loss as the output capacitance will be highest in this device.

It is important to have a design criterion that is optimized for the converters with ZVS applications, such one type of optimization is presented in the form of a new figure of merit (FOM) for converters with soft-switching or ZVS applications [20].

This work also incorporates the same type of techniques used but for low-voltage FETs, having a ZVS FOM can help to optimize the design by selecting the best possible FET among the available ones. This new ZVS FOM (4.15) uses the  $C_{OSS}$  loss data ( $E_{dissipated}$ ) obtained from either the Calorimetric or NR test, which can be used to get a new FOM that would serve our purpose of having an optimal device selection process.  $C_{ISS}$  is the input capacitance of the DUT and  $E_{CISS}$  is the energy loss per switching cycle [44] associated with the input capacitance  $C_{ISS}$ . However, the loss related to the  $C_{ISS}$  can be eliminated if a resonant gate drive is incorporated into the design [20].

$$FOM_{ZVS} = R_{DS,ON}(E_{dissipated} + E_{CISS}) \quad (4.15)$$

$$E_{CISS} = \frac{1}{2}(Q_g - Q_{gd})V_{gs} \quad (4.16)$$

We can observe that the hard-switched (HS) and ZVS FOMs are computed and listed for five different DUTs which were used in the Calorimetric and NR tests; we can observe that even though some DUTs may have lower HS FOM, but they aren't suited for ZVS applications as they have higher ZVS FOM compared to the other DUTs. It is also reported that there is no such correlation between the HS and ZVS FOM, a device having a smaller HS FOM need not necessarily perform well in ZVS applications.

Table 4.7 ZVS and non-ZVS FOM comparison for five different DUTs using data obtained from Calorimetric Test

<b>Part Number</b>	<b>R<sub>DS,ON</sub></b>	<b>C<sub>ISS</sub></b>	<b>C<sub>OSS</sub></b>	<b>Q<sub>GD</sub></b>	<b>V<sub>DS</sub></b>	<b>HS-FOM</b>	<b>ZVS-FOM</b>
BSC037N08NS5	3.2mΩ	3200pF	530pF	10nC	80V	0.010nJΩ	5.76nJΩ
ISC030N10NM6	2.6mΩ	4000pF	900pF	9.1nC	100V	0.023nJΩ	6.93nJΩ
ISC060N10NM6	5.1mΩ	1900pF	430pF	4.5nC	100V	0.022nJΩ	7.67nJΩ
EPC2218	2.4mΩ	1189pF	562pF	1.5nC	100V	0.003nJΩ	5.58nJΩ

Table 4.8 ZVS and non-ZVS FOM comparison for five different DUTs using data obtained from non-linear Resonance Tests at  $L = 22\mu H$

<b>Part Number</b>	<b>R<sub>DS,ON</sub></b>	<b>C<sub>ISS</sub></b>	<b>C<sub>OSS</sub></b>	<b>Q<sub>GD</sub></b>	<b>V<sub>DS</sub></b>	<b>HS-FOM</b>	<b>ZVS-FOM</b>
BSC037N08NS5	3.2mΩ	3200pF	530pF	10nC	80V	0.010nJΩ	20.38nJΩ
ISC030N10NM6	2.6mΩ	4000pF	900pF	9.1nC	100V	0.023nJΩ	28.49nJΩ
ISC060N10NM6	5.1mΩ	1900pF	430pF	4.5nC	100V	0.022nJΩ	20.22nJΩ
EPC2218	2.4mΩ	1189pF	562pF	1.5nC	100V	0.003nJΩ	12.10nJΩ

Table 4.9 ZVS and non-ZVS FOM comparison for five different DUTs using data obtained from converter tests

<b>Part Number</b>	<b>R<sub>DS,ON</sub></b>	<b>C<sub>ISS</sub></b>	<b>C<sub>OSS</sub></b>	<b>Q<sub>GD</sub></b>	<b>V<sub>DS</sub></b>	<b>HS-FOM</b>	<b>ZVS-FOM</b>
BSC037N08NS5	3.2mΩ	3200pF	530pF	10nC	80V	0.010nJΩ	33.15nJΩ
ISC030N10NM6	2.6mΩ	4000pF	900pF	9.1nC	100V	0.023nJΩ	27.19nJΩ
ISC060N10NM6	5.1mΩ	1900pF	430pF	4.5nC	100V	0.022nJΩ	27.10nJΩ
EPC2218	2.4mΩ	1189pF	562pF	1.5nC	100V	0.003nJΩ	24.18nJΩ

From data of Table 4.7 we observe that the new ZVS FOM is computed using the data obtained in the calorimetric test, and we can conclude that as per this data, best choice for our device would be EPC2218, which has smallest ZVS FOM.

From data of Table 4.8 we observe that the ZVS FOM is computed using the data obtained from NR test with the inductance selection of  $22\mu H$ , we can conclude that the best devices of choice would be EPC2218. From the data of Table 4.9 we observe that the ZVS FOM is computed using the data obtained from actual converter testing and yield the same device as an optimal choice as before.

However, we would like to mention that though the best device to be selected for this application is EPC2218, the device with minimal  $C_{OSS}$ -related hysteresis loss will still be ISC060N10NM6 as depicted by the calorimetric and NR test results.

The reason that the test prototype couldn't achieve best efficiency and minimal losses with the EPC2218 is that the originally converter was designed to be tested at much higher frequency ( $\sim 140 kHz$ ), and that would not have been a fair comparison with the silicon (SI) device, thus the converter was tested at  $100kHz$  with the magnetics optimized for  $\sim 140kHz$ , as a results the input RMS current increases in the test prototype and induces loss greater than expected when being operated at  $100kHz$ . Thus, we believe that operating the GaN prototype at frequency, which is optimized for the magnetics, will yield best results.

## Chapter 5. Design example of a soft-switching converter with the impact of hysteresis loss in $C_{OSS}$

To highlight the importance of capacitive hysteresis loss for converters with soft-switching, we will present a design example involving a soft-switched topology that can be impacted by the existence of  $C_{OSS}$ -related hysteresis loss.

Fig. 5.1 shows the path of the drain current during the turn-off transition where it separates into channel current and  $C_{OSS}$  current. It is shown in (5.1) that during the turn-off switching transient, the drain current divides into channel current  $I_{ch}$  and the current  $I_{C_{OSS}}$  that charges the output capacitance. The total turn-off energy in the device can be expressed as per (5.2) where  $E_{ch,off}$  is the channel turn-off energy, and  $E_{C_{OSS}}$  is the energy stored in  $C_{OSS}$  of the device during turn-off transition [15].

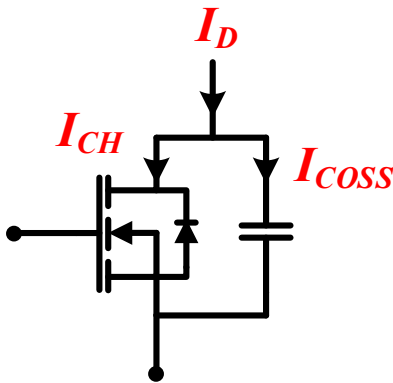


Fig. 5.1 Device current during switching transient

$$I_d = I_{ch} + I_{C_{OSS}} \quad (5.1)$$

$$E_{off} = E_{ch,off} + E_{C_{OSS}} \quad (5.2)$$

$$E_{ch,off} = E_{off} - E_{C_{OSS}} \quad (5.3)$$

In the total turn-off energy, the energy is lost only in the channel due to resistive dissipation, for ZVS applications the  $C_{OSS}$  is charged, discharged, and utilized to achieve ZVS turn-on transition [45]. Thus, the only energy loss during a turn-off transition should be channel turn-off related shown in (5.2), where  $E_{off}$  is the turn-off energy of the device which can be obtained from a double pulse test (DPT) performed in LTspice using the SPICE model of the devices, the circuit to perform DPT is shown in Fig. 5.2

However, in addition to the channel turn-off loss, it is found that the charging and discharging of output capacitances are not free of losses as they exhibit hysteresis [19][20] which needs to be accounted for when performing device selection for a ZVS application as the hysteresis loss can contribute significantly to the switching losses even in under ZVS switching.

The  $C_{OSS}$  hysteresis energy can be included with the channel turn-off energy for a device under ZVS as (5.4), and the loss can be computed by multiplying the (5.4) by switching frequency  $F_s$ . We can refer to the turn-off energy, energy stored in the  $C_{OSS}$ , and the channel turn-off energy as in Table 5.1.

$$E_{Loss} = E_{ch,off} + E_{hysteresis} \quad (5.4)$$

$$P_{sw,ZVS} = (E_{ch,off} + E_{hysteresis})F_s \quad (5.5)$$

Before we proceed to the design example, some prerequisite data has been presented to compute the channel turn-off loss (4.4) for the devices we selected in the previous chapters. These devices are also evaluated for  $C_{OSS}$ -related hysteresis loss using the two test methods (Calorimetric and Non-linear resonance) in Chapter 3. The energy loss relating to  $C_{OSS}$  hysteresis is presented in Table 5.2 which will be used for this design example.

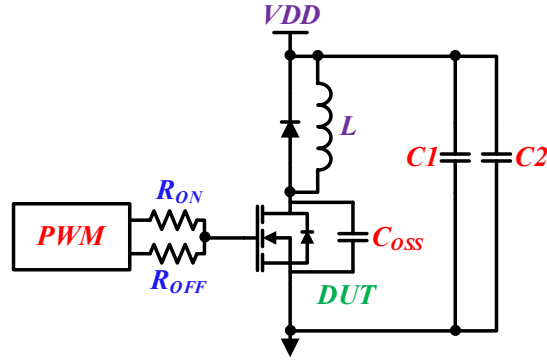


Fig. 5.2 Test circuit used to perform double pulse test in LTspice for different devices with

$$L = 47\mu H, C_1 = 220nF, C_2 = 100\mu F, R_{on} = 10\Omega, R_{off} = 1\Omega, V_{DD} = 50V$$

Table 5.1 Turn-off energy, energy stored in  $C_{oss}$ , and channel turn-off energy data obtained for each device at 50V using a double-pulse test (DPT) in LTspice using the SPICE models

Device part	$C_{oss}$ (Datasheet)	$E_{off}$	$E_{C_{oss}}$	$E_{ch,off}$
BSC037N08NS5	530pF	3.07uJ	0.66uJ	2.41uJ
ISC030N10NM6	900pF	1.94uJ	1.13uJ	0.85uJ
ISC060N10NM6	430pF	0.97uJ	0.53uJ	0.43uJ
EPC2218	562pF	1.02uJ	0.70uJ	0.31uJ
EPC2302	1000pF	1.66uJ	1.25uJ	0.41uJ

Table 5.2 Energy loss in the  $C_{oss}$ -related hysteresis using NR and Calorimetric tests

Device part	$E_{hysteresis}$ using NR	$E_{hysteresis}$ using Calorimetric
BSC037N08NS5	1.8μJ	1.44μJ
ISC030N10NM6	3.2μJ	2.21μJ
ISC060N10NM6	1.5μJ	1.29μJ
EPC2218	2.0μJ	2.55μJ
EPC2302	3.2μJ	2.50μJ

## 5.1 Design Example of an LLC (DCX mode)

It is important to characterize the hysteresis loss in the  $C_{OSS}$  of the devices as it often goes unnoticed and later accounts for unexpected losses in the converter. In this section, we will explore an LLC-DCX which works on the resonant frequency with a voltage gain of unity [46]. The operating parameters are selected in a way that the voltage and frequency range somewhat match the devices we tested for hysteresis loss in previous chapters.

The resonant tank can be designed using the process presented in [47] where we select the transformer turns ratio  $N$ , followed by optimal dead-time  $t_d$ , magnetizing inductance  $L_m$  required for minimal conduction losses, and optimal  $L_n$  to achieve the required peak gain (unity for the case of DCX). However, in this task, we focus on the impact of  $C_{OSS}$ -related hysteresis loss on overall switching losses in primary side devices.

Moreover, we can use the expressions provided in [47] for the primary (5.10) and secondary (5.11) RMS currents to obtain optimal dead-time and magnetizing inductance for each switching device.

Table 5.3 Operating parameters for LLC-DCX converter

Parameters	Values
Input Voltage	48V
Output Voltage	12V
Output Current	25A
Output Power	300W
Switching Frequency $F_s$	100kHz

$$M = 1, N = \frac{V_{in}}{2V_o}, N = 2 \quad (5.6)$$

$$T_o = \frac{1}{F_o}, F_o = F_s = 100kHz \quad (5.7)$$

$$R_L = \frac{V_o}{I_o} = \frac{12}{25} = 0.48\Omega \quad (5.8)$$

$$L_m = \frac{T_o t_d}{16C_{oss}} \quad (5.9)$$

$$I_{pri\_RMS} = \frac{1}{4\sqrt{2}} \frac{V_o}{NR_L} \sqrt{\frac{256N^4 C_{oss}^2 R_L^2}{t_d^2} + 4\pi^2 + \frac{16\pi^2(T_o t_d + t_d^2)}{T_o^2}} \quad (5.10)$$

$$I_{sec\_RMS} = \frac{\sqrt{3}}{24\pi} \frac{V_o}{R_L} \sqrt{\frac{256N^4 C_{oss}^2 R_L^2}{L_m^2 (T_o + 2t_d)} + \frac{12\pi^4 T_o}{T_o + 2t_d} + \frac{48\pi^4 (T_o t_d + t_d^2)}{T_o (T_o + 2t_d)}} \quad (5.11)$$

Equations (5.6), (5.7), (5.8), and (5.9) can be substituted into (5.10), and (5.11) which can be swept for a range of dead-time  $t_d$  to select a value which gives smallest current to minimize the conduction loss. For switches achieving ZVS turn-on, the loss is contributed by channel, and hysteresis in the  $C_{oss}$  of the devices which will be compared to the channel turn-off loss to highlight the impact and importance of evaluating the switching devices for hysteresis loss when using ZVS applications.

Table 5.4 On-state resistance of the devices at  $I_d = 25A$ ,  $Q_g$ , and  $Q_{gd}$

Device part	$C_{oss}$	$R_{ds,on}$	$Q_g$	$Q_{gd}$
BSC037N08NS5	530pF	4.4m $\Omega$	46nC	10nC
ISC030N10NM6	900pF	3.1m $\Omega$	55nC	9.1nC
ISC060N10NM6	430pF	6.2m $\Omega$	26nC	4.5nC
EPC2218	562pF	2.4m $\Omega$	10.5nC	1.5nC
EPC2302	1000pF	1.4m $\Omega$	23nC	2.3nC

We can compute the conduction loss in the primary switching devices using the expression for RMS current  $I_{pri,RMS} \sim 13.9A$  in (5.10) and using the on-state resistances for the devices from Table 5.4 and substituting the values in (5.12). The primary devices are being driven by supplying the required gate charge, this loss is labeled as driving loss and can be computed using (5.13) where  $Q_g$  is the gate charge,  $Q_{gd}$  is the miller charge, and  $V_{gs}$  is the gate-source voltage applied to the device.

The switching loss  $P_{sw}$  in the primary devices can be computed using channel turn-off energy loss and hysteresis energy loss obtained in Table 5.1, Table 5.2, and substituting it in (5.14), (5.15), and (5.16).

$$P_{cond,FETs} = I_{pri,RMS}^2 R_{ds(on)} \quad (5.12)$$

$$P_{drv,FET} = (Q_g - Q_{gd})V_{gs}F_s \quad (5.13)$$

$$P_{ch,off,FETs} = E_{ch,off}F_s \quad (5.14)$$

$$P_{hys,FETs} = E_{hysteresis}F_s \quad (5.15)$$

$$P_{sw,FETs} = P_{ch,off,FETs} + P_{hys,FETs} \quad (5.16)$$

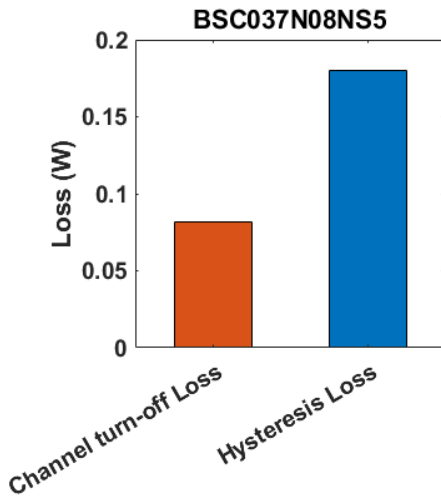
Table 5.5 On-state resistance, conduction loss, and driving loss of individual primary devices at full-load

Device part	$R_{ds,on}$	$P_{cond,FET}$	$P_{drv,FET}$
BSC037N08NS5	4.4m $\Omega$	0.85W	0.043W
ISC030N10NM6	3.1m $\Omega$	0.60W	0.055W
ISC060N10NM6	6.2m $\Omega$	1.20W	0.026W
EPC2218	2.4m $\Omega$	0.45W	0.006W
EPC2302	1.4m $\Omega$	0.27W	0.013W

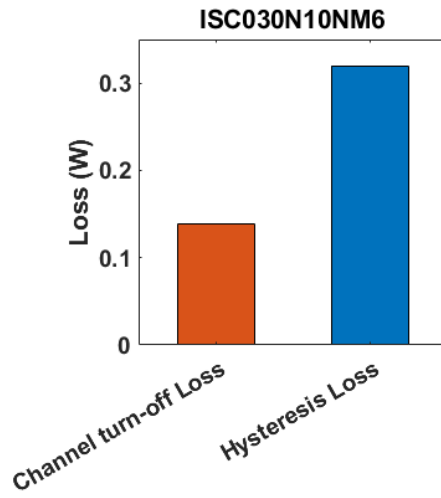
To highlight the impact of hysteresis loss on the overall switching loss of the primary side devices, the channel turn-off data and hysteresis loss data are plotted for this design example, where both losses are computed for a  $V_{DS} = 50V$  in Fig. 5.3 where we can observe that the hysteresis loss in the  $C_{OSS}$  shares a large percentage of the switching losses, thus it is important to include this loss while selecting the devices for ZVS applications.

Table 5.6  $C_{OSS}$  hysteresis loss, and channel turn-off loss of individual primary devices at full-load for  $V_{DS} = 50V$

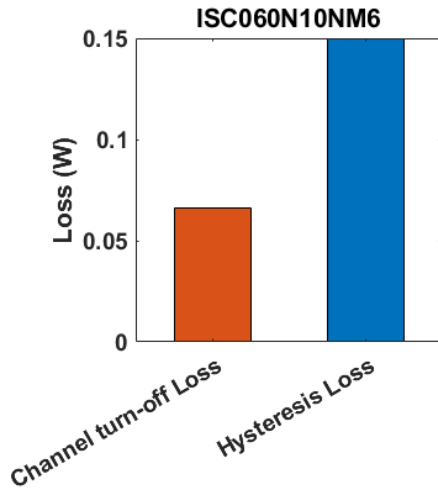
Device part	$P_{hys,FETs}$	$P_{ch,off,FETs}$
BSC037N08NS5	0.18W	0.241W
ISC030N10NM6	0.32W	0.085W
ISC060N10NM6	0.15W	0.043W
EPC2218	0.20W	0.031W
EPC2302	0.32W	0.041W



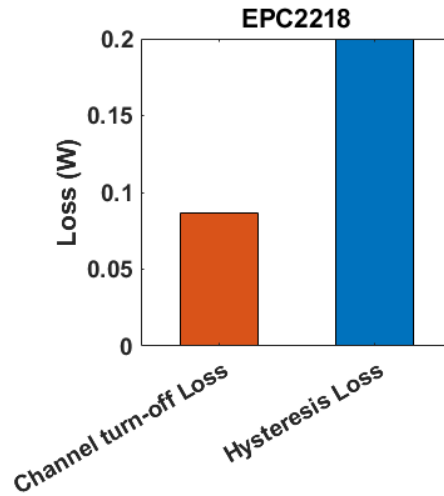
(a)



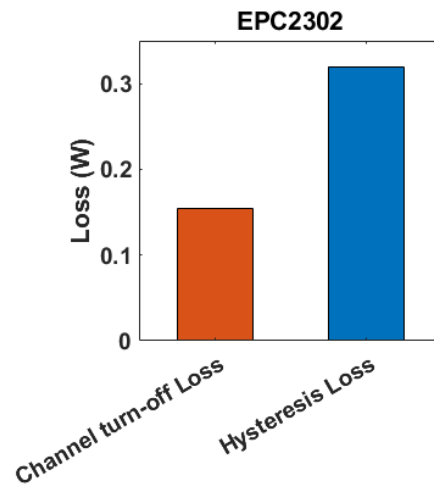
(b)



(c)



(d)



(e)

Fig. 5.3 Comparison between the channel turn-off loss and hysteresis loss in  $C_{oss}$  for a single switching device (a) BSC037N08NS5 SI FET, (b) ISC030N10NM6 SI FET, (c) ISC060N10NM6 SI FET, (d) EPC2218 GaN HEMT, (e) EPC2302 GaN HEMT.

We can recall the design paradigm to select the devices for ZVS applications using the novel ZVS FOM mentioned in Chapter 4 to compare the different devices we evaluated for hysteresis

and channel turn-off loss in this design example. For a fair design comparison, only the devices with similar voltage ratings are compared for hard-switching (HS) FOM and ZVS FOM. It can be observed in Table 5.7 that the best-performing device obtained through the HS FOM is ~7 times better than the worst-performing device, and when we adopt ZVS FOM, the best-performing device is about ~2 times better than the worst-performing device, this reduction indicates that the inclusion of energy dissipated in  $C_{oss}$  due to hysteresis can impact the device selection process significantly. It can be verified from the total loss data for the primary device in Table 5.8 that the ZVS FOM gives the best-performing device as EPC2302.

Table 5.7 Hard-switching FOM vs. ZVS soft-switching FOM comparison for devices rated for  $V_{DS} = 100V$

Device part	$V_{DS}$	HS-FOM	ZVS FOM
ISC030N10NM6	100V	0.028	11.34
ISC060N10NM6	100V	0.027	10.63
EPC2218	100V	0.0048	6.54
<b>EPC2302</b>	<b>100V</b>	<b>0.0041</b>	<b>5.94</b>

Table 5.8 Total loss in an individual primary device (w/ hysteresis loss included)

Device part	$P_{cond,FET}$	$P_{drv,FET}$	$P_{hys,FETs}$	$P_{ch,off,FETs}$	$P_{total}$
ISC030N10NM6	0.60W	0.055W	0.32W	0.085W	1.06W
ISC060N10NM6	1.20W	0.026W	0.15W	0.043W	1.41W
EPC2218	0.45W	0.006W	0.20W	0.031W	0.68W
<b>EPC2302</b>	<b>0.27W</b>	<b>0.013W</b>	<b>0.32W</b>	<b>0.041W</b>	<b>0.64W</b>

Table 5.9 Total loss in an individual primary device (w/o considering hysteresis loss)

<b>Device part</b>	$P_{cond,FET}$	$P_{drv,FET}$	$P_{ch,off,FETs}$	$P_{total}$	<b>Mismatch</b>
ISC030N10NM6	0.60W	0.055W	0.085W	0.74W	30.18%
ISC060N10NM6	1.20W	0.026W	0.043W	1.26W	10.63%
EPC2218	0.45W	0.006W	0.031W	0.48W	29.41%
EPC2302	0.27W	0.013W	0.041W	0.32W	50%

Table 5.9 shows the total loss if we don't include the impact of hysteresis, as a result, the mismatch in total loss is significant for each device. Thus, with this design example, it is shown that the hysteresis loss in  $C_{oss}$  is crucial to incorporate in a design for soft-switching applications to have an explanation of losses that may not be present if we exclude the  $C_{oss}$ -related hysteresis loss from the design process. Moreover, it drives the ZVS FOM which would give an optimal device selection, by incorporating the impacts of  $R_{ds,on}$ ,  $E_{CISS}$ , and  $E_{hys,FETs}$ .

## Chapter 6. Conclusion and Future Work

In this work, the issue of output capacitance-related hysteresis loss has been identified, and different methods are explored to observe and measure this loss in the different switching devices like SI FET, and GaN HEMT. The origins related to  $C_{OSS}$ -related hysteresis loss are discussed, and some reasonings explaining the origins of this loss are found which can be quite useful when it comes down to improving the structure of the device to avoid this hysteresis loss.

The loss in SI devices is caused by the accumulation of stranded charge at the top and bottom of n and p pillars in the depletion layer, in SiC FETs and diodes the  $C_{OSS}$  losses occur due to resistive power dissipation in the termination region, and incomplete ionization causes time-dependent charge storage in the device's  $C_{OSS}$ , which is the main cause of  $C_{OSS}$  related hysteresis loss in SiC devices. In GaN devices, the  $C_{OSS}$ -related loss is due to the imbalance of stored and released charges depicted by dynamic trapping [24].

Methods to measure the hysteresis loss in  $C_{OSS}$  are found (NR and Calorimetric test) and implemented for five different DUTs, including both SI FETs and GaN HEMTs. This work quantifies the  $C_{OSS}$ -related hysteresis loss in the form of tabulated data from the calorimetric test, and energy loss curves from the NR test which are used to explain losses in devices exhibiting ZVS transitions.

The test results obtained from the NR method and Calorimetric method are used to validate a DC-DC converter hardware prototype, explaining the switching loss breakdown for four different devices (3 SI FETs, 1 GaN HEMT), and presenting a device selection paradigm (ZVS FOM) for converters having ZVS transitions.

The only loss reported for the ZVS of the devices was channel turn-off loss and it was assumed that the energy dissipated in the output capacitance is zero [15]. However, with this work, we

found that charging and discharging of  $C_{oss}$  is not loss-free and exhibit hysteresis loss, which should be included in the design to account for unexpected losses. To shed some more light, a design example has been presented in Chapter 5 which highlights the impact of hysteresis loss on the overall switching and total loss of a device, and how it impacts the device selection process for ZVS applications.

For future work, a few more things can be incorporated into the test procedures, first, the calorimetric test procedure can be further refined by performing it on an actual converter prototype by making provisions to place low-inductive co-axial shunts for current measurements, which would enable much better evaluation of the losses in the devices and give more accurate results. Further improvements can be made to the setup by integrating high-precision temperature sensing in the converter itself and performing an online computation using a digital MCU to get run-time results for the hysteresis loss.

However, for applications with very high switching frequencies like  $\sim MHz$  the required inductance is much smaller, and only the PCB trace inductance may serve the purpose of an inductor, which can save some board area, and the test method can be implemented with the converter prototype. An online test method can be implemented for the NR test as long as the  $V_{DS}$  is sinusoidal.

Also, an automated design tool can be developed where the user needs to enter the data from the datasheet, converter parameters, and Non-Linear or Calorimetric test data, to estimate the hysteresis loss in the DUTs and return an optimized device selected which can be used in the converter prototype.

## Chapter 7. Appendix

### 7.1. LTspice simulation results for double pulse test (DPT) of devices

This section presents the test results for the turn-off loss obtained using a double pulse test in LTspice using the SPICE models of the devices. The test is conducted using the test circuit of Fig.

5.2.

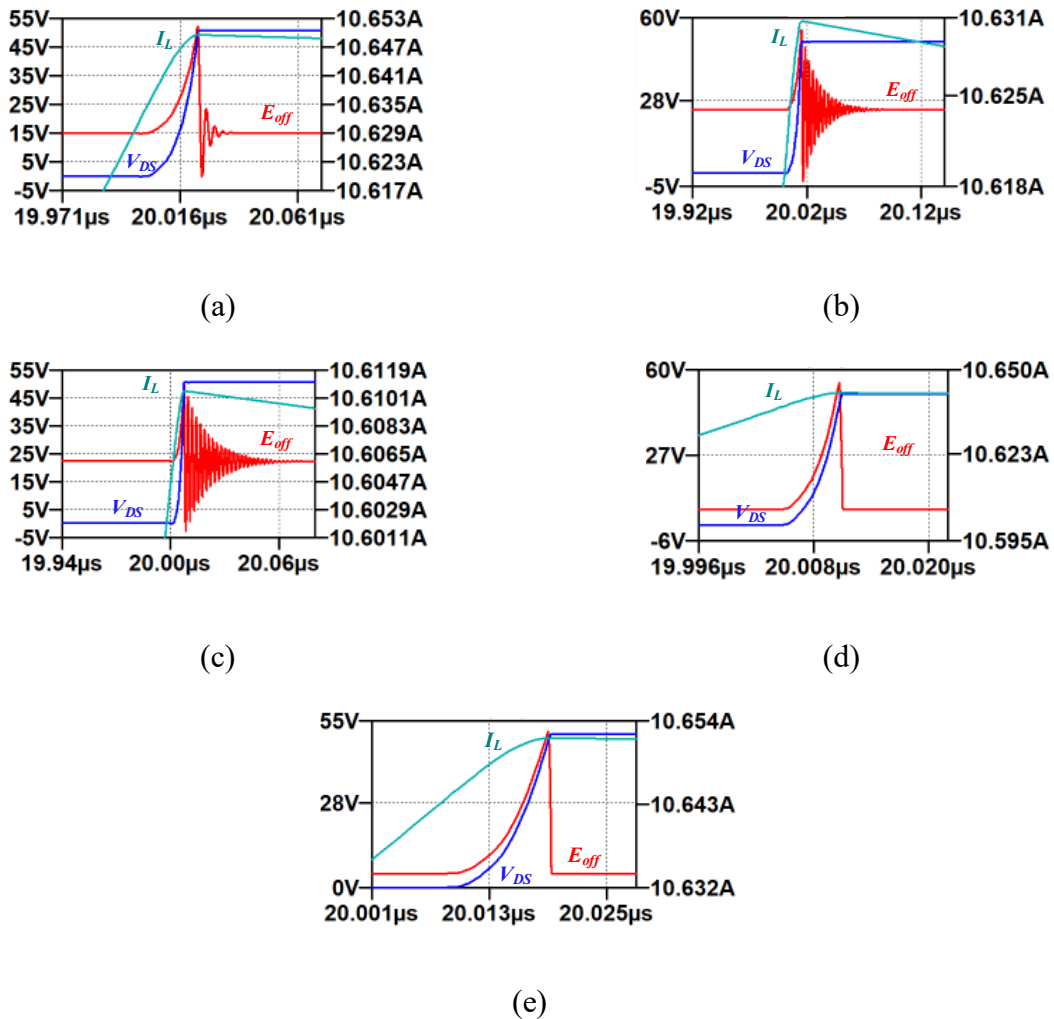


Fig. 7.1 Turn-off loss data obtained using a double pulse test circuit in LTspice for (a) BSC037N08NS5  $E_{off} = 3.07\mu J$ , (b) ISC030N10NM6  $E_{off} = 1.94\mu J$ , (c) ISC060N10NM6  $E_{off} = 0.97\mu J$ , (d) EPC22128  $E_{off} = 1.02\mu J$ , (e) EPC2302  $E_{off} = 1.66\mu J$

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