CHAPTER 4

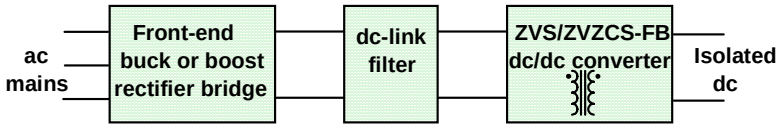
QSS ISOLATED THREE-PHASE ZVZCS BUCK RECTIFIER

4.1 Introduction

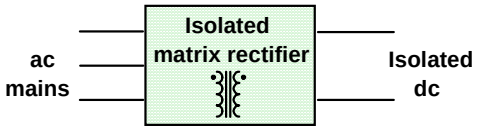
For high-power high-performance ac-dc conversion where isolation of the ground path is required, the standard two-stage approach as shown in Fig. 4.1(a) is usually adopted. The whole system is composed of a front-end three-phase rectifier followed by a high-power dc-dc converter. The front-end converter can be a high-frequency PWM rectifier of either buck, or boost type, and correspondingly the intermediate low-pass dc-link filter can be inductive for the buck rectifier case or capacitive for the boost rectifier case. The high-power dc-dc converter provides high-frequency isolation, voltage scaling, and further output regulation and is usually of full-bridge (FB) type, typically with the known phase-shift PWM control to achieve zero-voltage-switching (ZVS) [D21]-[D29], or hybrid zero-voltage, zero-current-switching (ZVZCS) as proposed more recently [D31]-[D36], [D38]-[D39].

It has been known that all the functions as realized in the two-stage scheme can also be achieved in a single-stage without performance compromise, and the circuit topology turns out to be of matrix type as shown in Fig. 1.4(a) [B1]-[B4]. Although the boost version also exists [B13]-[B14] [H6], as shown in Fig. 1.4(b), its switches suffer from high steady-state and transient voltage stress, as revealed from the discussions at the end of the previous

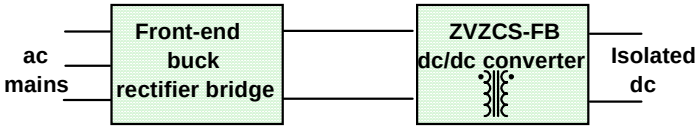
chapter, so the buck version is practically more useful. In the single-stage scheme, power needs to be processed only once, and for that reason, more efficient power conversion can be achieved.



(a) Conventional two-stage scheme.



(b) Single-stage (matrix type) scheme.



(c) Quasi-single-stage (QSS) scheme.

Fig. 4.1. High-power high-performance ac-dc conversion schemes.

ZVS for all the switches in the matrix buck rectifier can be realized in a similar way to that in a ZVS-FB dc-dc converter [B3]-[B4] [H6]. However, the PWM modulation algorithm for the ZVS matrix buck rectifier is relatively complicated, and digital signal processor (DSP)-based digital modulation is usually used to realize the required center-aligned six-step PWM [B4]. For high power applications where IGBTs are now prevalently used, high turn-off loss of the symmetrically positioned switches in the converter is still a concern although they are turned on under ZVS. Another concern is the high freewheeling loss in the primary side as associated with the ZVS-FB dc-dc converter operation.

A new quasi-single-stage isolated three-phase zero-voltage/zero-current-switched (ZVZCS) buck PWM rectifier suitable for high-power off-line applications is proposed in this chapter[B5]-[B8]. It consists of a front buck rectifier bridge and a full-bridge ZVZCS dc-dc converter in direct cascading, as abstractly shown in Fig. 4.1(c). With the absence of intermediate dc-link filtering components, all the features attributed to the single-stage matrix rectifier are retained, i.e. the power is processed only once from the input to the output. Moreover, as the analysis below will show, switching losses are further reduced because of the hybrid ZVZCS operation. As a result, it can run at high switching frequency while still maintain high efficiency.

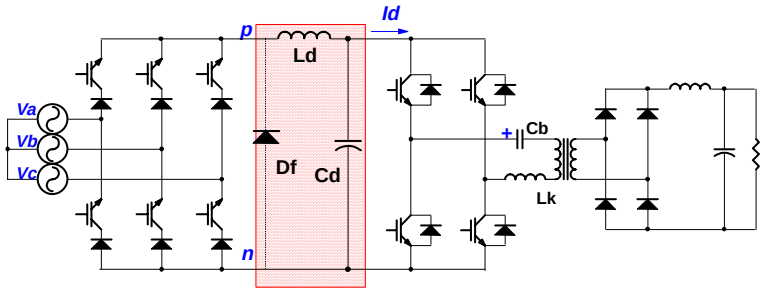
In the rest of this Chapter, the QSS isolated ZVZCS buck rectifier topology will be introduced in Section 4.2. In Section 4.3, the operation principles of the QSS isolated ZVZCS buck rectifier are presented. In Section 4.4, the conditions to achieve global ZVZCS in a line cycle is analyzed, and various power stage implementation issues are discussed. The experimental results of a 6 kW, 80 kHz prototype for typical telecommunication applications are presented in Section 4.5. A simplified circuit with alternative modulation scheme is briefly discussed in Section 4.6, and finally in Section 4.7, a family of QSS isolated ZVZCS buck rectifiers are obtained based on the generalization of the ZVZCS full-bridge converter concept.

4.2 QSS Isolated Buck ZVZCS Rectifier

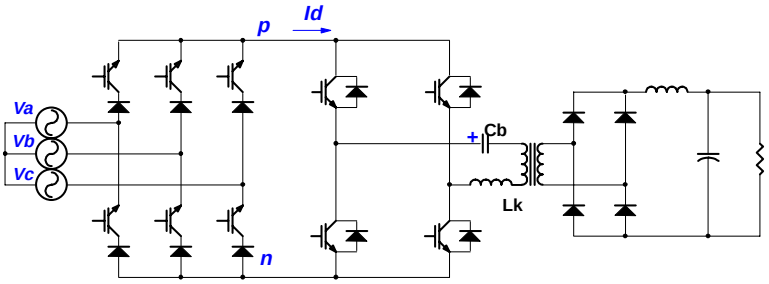
4.2.1 Topology Derivation of QSS Isolated ZVZCS Rectifier

A two-stage rectifier system is shown in Fig. 4.2(a). It consists of a front three-phase buck rectifier which shapes the three-phase input current and regulates the dc bus, and a

ZVS full-bridge dc-dc converter. Because both of the two cascading stages are of buck type, it may be possible to eliminate the intermediate LC filter to obtain a QSS isolated buck rectifier according to the concept of QSS power conversion defined in Chapter 2. The resulting topology is illustrated in Fig. 4.2(b).



(a) Two-stage ac-dc converter system with a front-end buck rectifier and a full-bridge ZVS dc-dc converter.



(b) Corresponding QSS isolated buck rectifier.

Fig. 4.2. Topology derivation of QSS isolated buck rectifier.

It is noticeable that some circuit properties are changed with the above topology simplification. In the original two-stage scheme, the input current of the dc-dc converter stage or the dc-rail current, I_d, can flow in both directions. However, in the QSS topology, the reverse path for the dc-rail current is blocked by the current-unidirectional buck rectifier bridge. Unfortunately, from the operation principles of the ZVS full-bridge dc-dc converters [D21]-[D29], it is known that at the end of each half cycle, the freewheeling leakage current on the primary side of the isolation transformer has to be fed back to the

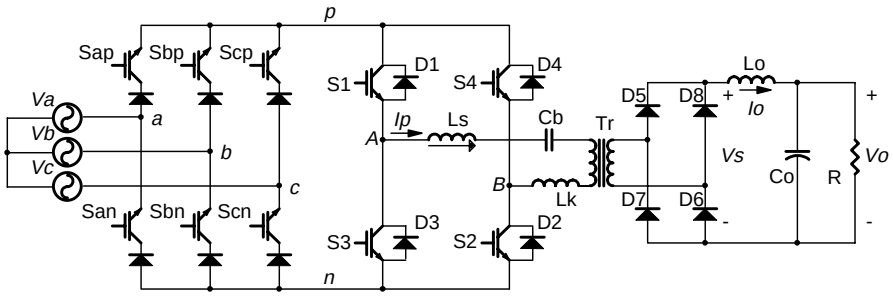
source. The blockage of this current reverse path inevitably leads to a transient voltage appearing across *p* and *n*.

Also noticed is that in the ZVZCS full-bridge converter proposed in [D31], the freewheeling primary current is reset to and kept around zero during the freewheeling or off duty cycle. As a result, there is no reverse current fed back to the source. Therefore, the blockage of the reverse current path does not present any problem if a ZVZCS full-bridge topology is used to replace the ZVS full-bridge topology shown in Fig. 4.2(b). The resulting QSS isolated ZVZCS buck rectifier is shown in Fig. 4.3(a), and its high-frequency operation waveforms is shown in Fig. 4.3(b), which correspond to the first half of sector *I* of an input line cycle as shown in Fig. 4.4.

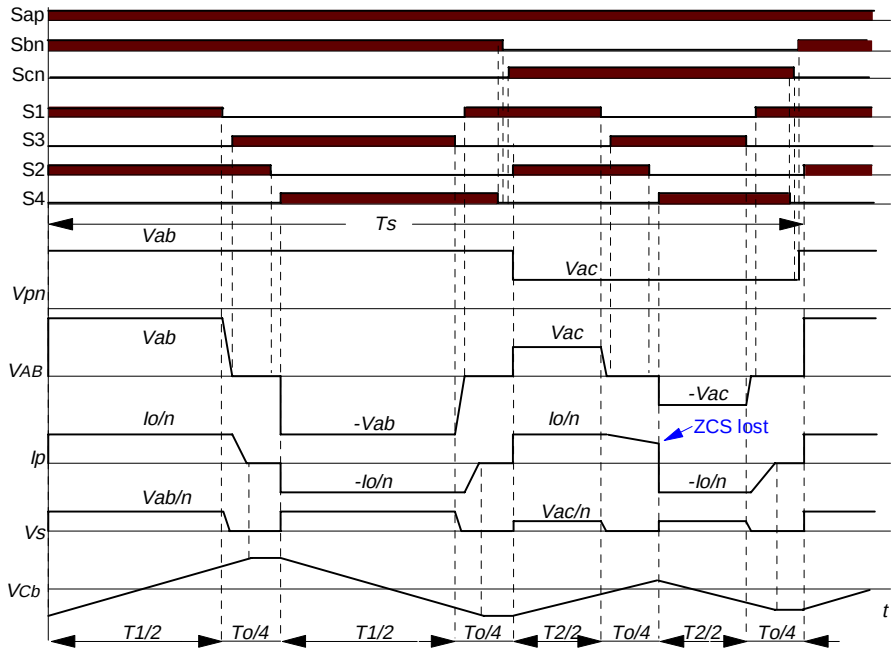
The proposed rectifier realizes, in a unified single stage, all the circuit functions as were achieved by the established two-stage power conversion, while there are no dc-link filtering components. It is also functionally equivalent to the matrix rectifiers in [B1]-[B4]. Moreover, it possesses unique features of very low switching losses, as will be explained below.

As in the cascaded buck rectifier discussed in Chapter 2, the duty-cycle control and other control functions in the QSS isolated ZVZCS rectifier can be realized by the full-bridge dc-dc converter, while the front three-phase buck bridge only needs to do lossless switching to connect the active phases to the pulsating dc link. The ZVZCS full-bridge dc-dc converter can be controlled with the well-known phase-shift PWM control [D21]-[D29]]. That is, the turn-on of the switches on the right leg composed of S_2 and S_4 (referred to as lagging leg thereafter) is delayed relative to that on the left leg (leading leg). With the ZVZCS scheme, the leakage current during off-time is reset by the voltage established on

the blocking capacitor C_b, whose value is intentionally reduced, and further kept around zero by a saturable reactor L*s*. Because of this, the lagging-leg switches can be turned off under zero-current, and slower devices such as IGBTs can be comfortably used. Detailed operation of the ZVZCS full-bridge can be found in [D31].



(a) Circuit diagram.



(b) High-frequency waveforms.

Fig. 4.3. QSS isolated three-phase ZVZCS buck PWM rectifier.

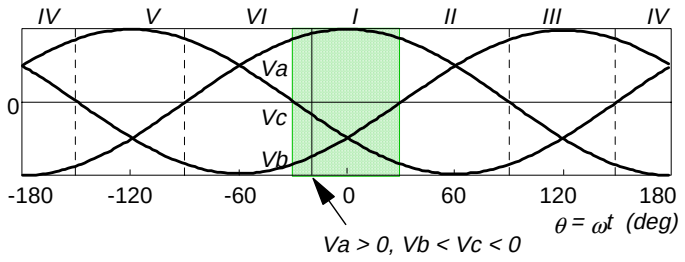


Fig. 4.4. Input phase voltages.

4.2.2 QSS Isolated ZVZCS Rectifier with Split Full-Bridges

In the basic topology shown in Fig. 4.3, ZCS for the lagging switches is difficult to achieve for some portions of a line cycle when the two consecutive duty cycles, d_1 and d_2, can be radically different in magnitude near the 60^o sector boundaries. Hence, the voltage on the small blocking capacitor, V_{Cb}, which is used to reset the primary current, contains a strong subhamonic at twice the switching frequency, or $2/T_s$, as is clearly seen in Fig. 4.3(b). As a result, the polarity and magnitude of V_{Cb} may be incorrect for the current in the leakage inductance to be reset, especially after running very small duty cycles.

The above problem can be solved by splitting the full-bridge in two, as shown in Fig. 4.5, one operating with duty cycle d_1 and the other one with d_2. The corresponding timing and key circuit waveforms are illustrated in Fig. 4.6, and will be discussed further in the next section.

It can be concluded from the analysis above that the proposed QSS isolated rectifier has very low switching losses because of ZCS operation for all but the leading-leg switches, which switch under zero voltage. Consequently, it is suited for high frequency/high power applications.

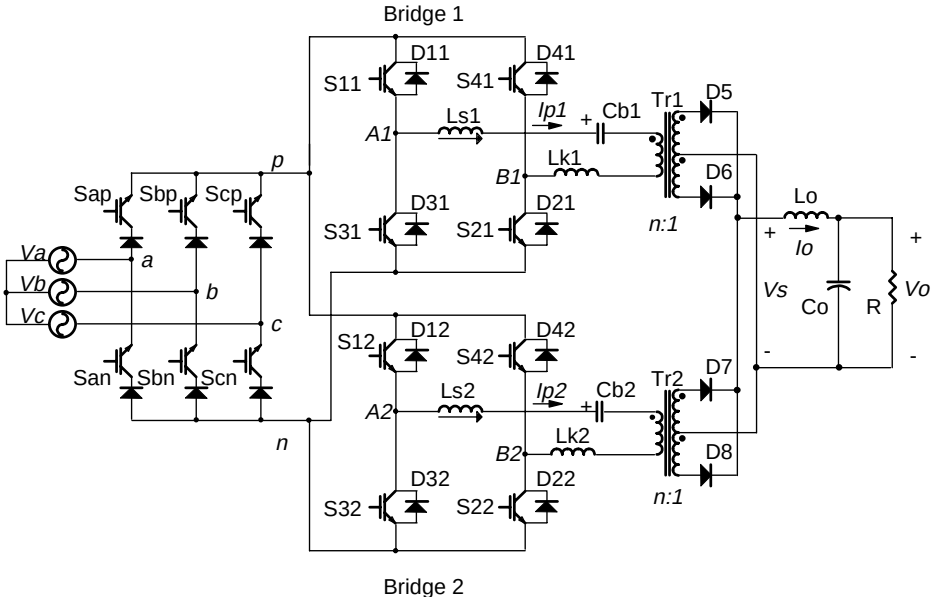


Fig. 4.5. QSS isolated buck rectifier with global ZVZCS capability.

4.2.3 Summary of Features

In addition to the advantages attributed to the matrix rectifier, i.e. no intermediate dc-link filter and one-time power processing, the QSS isolated ZVZCS buck rectifier has the following distinctive advantages:

a) Front-end buck bridge does not need to switch any current, i.e. is complete ZCS;

b) ZCS for the lagging leg switches in the FB dc-dc converter is achieved by primary freewheeling current resetting;

c) Low primary freewheeling loss for the same reason;

d) Fast turn-off switches are needed only for the leading leg switches, which works under ZVS turn-on.

For these reasons, it is promising to be used in high power ac-dc applications with isolation requirement, such as battery chargers, UPSs and telecommunication power stations.

4.3 Operation Principles

4.3.1 PWM and Timing Sequence

The PWM operation for the QSS isolated ZVZCS buck rectifier is similar to that for the non-isolated buck rectifiers. In this case, the active duty cycles, d_1 and d_2, need to be broken into two equal portions, and applied sequentially to ensure flux balance on the isolation transformer, as shown in the timing diagram in Fig. 4.3(b). Correspondingly, it is advantageous to break the freewheeling duty cycle into four equal portions, each with $d_o/4$ [B3]. This is equivalent to the PWM scheme with distributed zero duty cycle for the non-isolated buck rectifier.

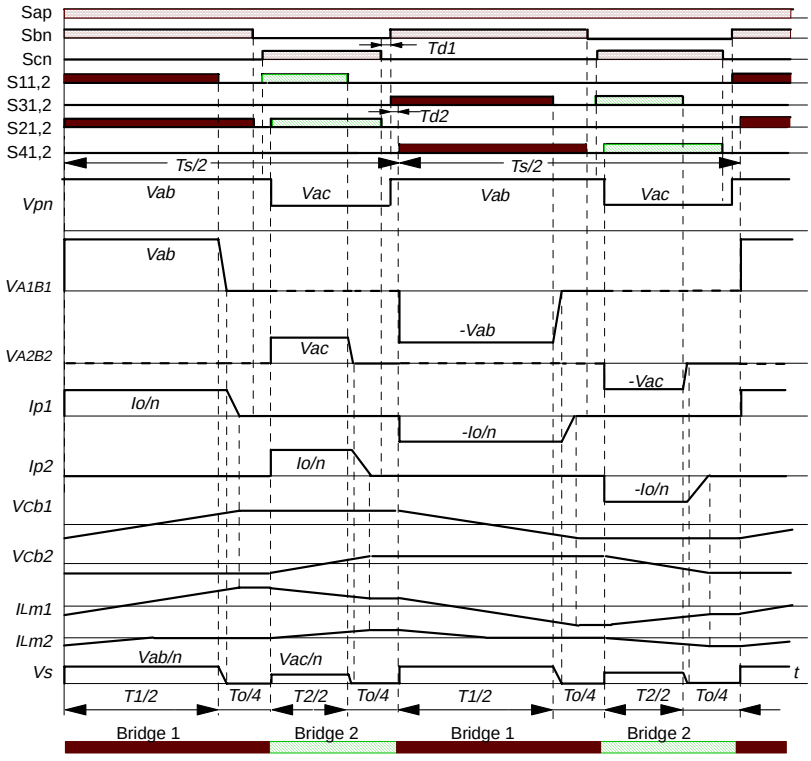


Fig. 4.6. High frequency waveforms.

With a single isolation transformer in Fig. 4.3(a), to exercise balanced flux on the transformer, half of an active duty cycle, for example $d_1/2$, has to be followed by another

half of the same duty, $d_1/2$. But with the split dual full-bridges as shown in Fig. 4.5, more freedom is created for the pairing of the active duty cycles within a PWM switching cycle and different timing sequences are feasible because the neighboring two half duty cycles can now be exerted on different bridges.

One of such possible sequences is illustrated in Fig. 4.6. With this sequence, the half active duty cycles, $d_1/2$ and $d_2/2$, are consecutively applied to the alternative bridges, and the two bridges work alternatively, or in time-division. This results in symmetrical control pulsing within half of a switching period, i.e. $T_s/2$, and facilitates digital implementation of the timing sequence generation. Also, the effective output ripple frequency and the input current pulse frequency are doubled, as is clear from the switching waveform of the rectified secondary voltage, V_s, and the primary bus voltage, V_{pn}, respectively, in Fig. 4.6. It becomes possible for the sampling frequency in the control to be doubled and for a wider control bandwidth to be achieved. This is especially important when digital control is used. In that case, the sampling delay usually dominates the obtainable maximum control bandwidth.

4.3.2 Operation within a PWM Period

To simplify the analysis, it is assumed in the following analysis that the output choke, L_o, is large, so that the output current is constant; the voltages across the blocking capacitors, C_{b1} and C_{b2}, are low compared to the rectified input voltage, V_{pn}; and the magnetizing currents of the transformers are negligible compared to the reflected output current, so the primaries see the constant reflected output current. All these assumptions are reflected in the switching waveforms in Figs. 4.3(b) and 4.6. The timing sequences shown are all corresponding to the input voltage combination within the first half of sector *I*, with $\theta = \omega t \in (-30^o, 0^o)$.

During the first $d_1T_s/2$, or $T_1/2$ in Fig. 4.6, the switches S_{ap}, S_{bn}, S_{11} and S_{21} are on, and the rectified input line voltage is applied to the primary of T_{r1}. The magnetizing current, I_{Lm1}, of T_{r1} and the blocking capacitor voltage, V_{Cb1}, across C_{b1} increase linearly from their initial negative values. During this time, all the switches in bridge 2 are off, and the voltage, V_{Cb2}, across its blocking capacitor is kept constant. Meanwhile, the negative initial magnetizing current of T_{r2}, I_{Lm2}, is reset through the antiparallel diodes, D_{12} and D_{22}. The dotted line in the waveform of V_{A2B2} shows that it may fluctuate after the magnetizing current is reset because of the parasitic oscillation between the leakage inductance, L_{k2}, in series with the saturable inductor, L_{s2}, (when it is desaturated) and the magnetizing inductance, L_{m2}, and the parasitic capacitance across nodes A_2, and B_2, mainly the parasitic capacitance of the switches. Because the blocking capacitor is large compared with the parasitic capacitance, V_{Cb2} will not be modified.

At the end of the first $T_1/2$, S_{11} is turned off, and the freewheeling period, $d_0T_s/4$, or $T_o/4$, is initiated. The voltage at node A_1 is first discharged to zero by the primary current, and the load current starts to freewheel in the secondary. At the same time, the current remaining in the primary leakage inductance, L_{k1}, is reset to zero by the voltage established on the blocking capacitor, C_{b1}, in the same way as in the ZVZCS dc-dc converter [D31]. The primary current remains around zero due to the increased inductance of the saturable inductor, L_{s1}. During this period, the magnetizing current of T_{r1}, I_{Lm1}, also freewheels through the secondary.

At the end of the $T_o/4$, S_{21} is turned off under zero current. The delay time, T_{d1}, between turn-off of S_{11} and S_{21} is $T_o/4$ minus the dead times, T_{d2} through T_{d5} shown in Fig. 4.5.

With S_{12} in bridge 2 having already been gated on slightly before the end of the last $T_s/4$, turning on S_{22} at the beginning of $d_2T_s/2$, or $T_2/2$, initiates the other active duty cycle, d_2. The events are similar to that in the first active duty cycle. However, in this case, the magnetizing current in T_{r1}, I_{Lm1}, will not be completely reset but only decreased, as shown in Fig. 4.6, because $d_2 \cdot V_{ac} < d_1 \cdot V_{ab}$. The final value depends on the relative lengths of the two active duty cycles.

The circuit operation in the second half of the switching period, i.e. after $T_s/2$, is symmetrical to the first half, with the other half of the switches in the full-bridges working.

As shown in Figs. 4.5 and 4.7, two delay times, T_{d1} and T_{d2}, need to be inserted into the ideal pulses generated by the PWM modulator. T_{d1} is needed to ensure the switching of the front buck bridge switches, while T_{d2} is used to achieve lossless turn on of the front buck bridge. These fixed delays are easy to generate and can be easily compensated by extending the trailing edges of the lagging leg switch pulses.

4.4 Implementation Issues

4.4.1 Global ZVZCS Capability

As can be seen from the analysis above, the ZVS of the leading leg switches, S_{1j} and S_{3j}, $j \in \{1, 2\}$, is similar to that in the typical phase-shift-controlled full-bridge dc-dc converter, and the ZVS can be achieved easily in the whole line cycle. It should be noted that there may be some residual voltage across the leading leg switches when they are turned on, resulting from the parasitic oscillation during the dormant period when the other bridge is working. So there is some capacitive discharge loss, but there is no turn-on loss due to reverse recovery of the antiparallel diode.

The ZCS range for the lagging leg switches, S_{2j} and S_{4j}, $j \in \{1, 2\}$, is of concern because it is a strong function of the duty cycles, which change drastically within every 30^o of a line cycle.

One convenient and illustrative way to study the ZCS range is to study the state trajectories of the resonant circuit consisting of each leakage inductance of the transformer, L_{k1} or L_{k2} in Fig. 4.5, and each blocking capacitor, C_{b1} or C_{b2}. Considering the fact that the switching frequency is much higher than the input line frequency, it is justified to assume that the state-trajectories of the resonant circuits in one switching cycle are closed curves. If the current ripple reflected from the secondary and the magnetizing currents are further assumed to be low, the trajectories of the leakage (primary) currents are straight lines in parallel with the blocking capacitor voltage (V_b) axis, as shown in Fig. 4.7. The trajectory $\{a_1$-b_1-c_1-d_1-e_1-$f_1\}$ in Fig. 4.7 corresponds to the bridge 1 in Fig. 4.5, while the trajectory $\{a_2$-b_2-c_2-d_2-e_2-$f_2\}$ corresponds to the bridge 2. The top portion ($I_{Lk} > 0$) represents the first half of the switching period in Fig. 4.6, while the negative half portion represents the second half.

Restricting our discussions to the first half cycle (due to symmetry), the trajectories {a, b, c, d} can be divided into three segments. The first segment {a, b} corresponds to the turn-on of the lower switch, S_{21} or S_{22}, in the lagging legs, when the saturable inductor saturates rapidly while V_{Cb} does not change significantly. The second segment {b, c} corresponds to the active duty cycles; while the third segment {c, d} represents the leakage current resetting stage. Once the current is reset to around zero, it just stays at d due to the effects of the saturable inductor.

From Figs. 4.6 and 4.7, the blocking capacitor voltage and the reset time of the leakage inductor current and can be easily derived. Specifically, it can be shown that

$$V_{Cbj}(c) = \frac{Io/n}{2}\left(\frac{d_j T_s}{C_{bj}} - \frac{L_{kj}}{d_j T_s}\right), \tag{4.1}$$

and $$V_{Cbj}(jd) = \frac{Io/n}{2}\left(\frac{d_j T_s}{C_{bj}} + \frac{L_{kj}}{d_j T_s}\right), \quad j \in \{1,2\}. \tag{4.2}$$

The reset time, t_{rj}, is then

$$\tau_{rj} = \sqrt{L_{kj}C_{bj}}\left[\frac{\pi}{2} - \tan^{-1}\left(\frac{\sqrt{C_{bj}/L_{kj}}}{2}\left(\frac{d_j T_s}{C_{bj}} - \frac{L_{kj}}{d_j T_s}\right)\right)\right]. \tag{4.3}$$

Suppose $L_{k1} = L_{k2}$, $C_{b1} = C_{b2}$, and $d_1 > d_2$; then it is apparent from (4.3) that $t_{ra} < t_{rb}$. That is, the leakage current in the bridge conducting smaller duty cycle is always more difficult to be reset if two bridges are designed to be symmetrical.

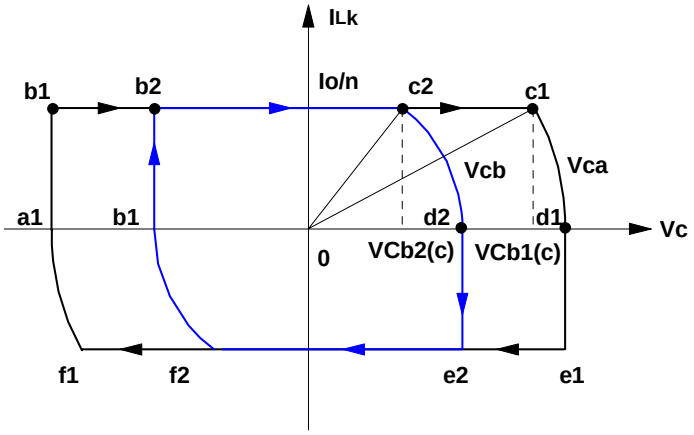


Fig. 4.7. State trajectories of blocking capacitor voltages and leakage inductor currents.

From (4.1) or Fig. 4.7, it can be seen that with very low duty cycle (of bridge 2 for this case), the voltage on the blocking capacitor, V_{Cb2}, may not reverse its polarity, i.e. point c_2 stays on the left half plane at the end of the corresponding active duty cycle d_2. From (4.1), this happens when $d_2 T_s < 1/\omega_2$, where $\omega_2 \equiv 1/\sqrt{L_{k2}C_{b2}}$. In this case, the reset time for bridge 2 becomes

$$\tau_{rb} = (1+\pi/2)/\omega_2 - d_2 T_s. \tag{4.4}$$

The worst (extreme) case occurs when d_2 approaches zero, as shown in Fig. 4.8. Point c_2 on the trajectory moves leftwards and becomes coincident with point b_2, so to reset the leakage current, the trajectory has to travel from b_2 to c' and finally to d_2. In this case, it can be shown that the worst case reset time, t_{rb}^{m} is expressed as

$$\tau_{r2}{}^{m} = (1+\pi/2)\sqrt{L_{k2}C_{b2}}. \tag{4.5}$$

So the global ZCS condition can be obtained from (4.5) as

$$\frac{d_o T_s}{4} = \frac{T_s}{4}(1-\frac{\sqrt{3}}{2}m) \geq \tau_{r2}{}^{m} + \Delta T_{ZCS}, \tag{4.6}$$

where ΔT_{ZCS} is hold-down time after the current is reset to zero. Formula (4.6) sets the limit to the leakage inductance value in a practical design for retaining global ZCS operation. It is a function of the designed maximum modulation index, blocking capacitance, the switching frequency, and the ZCS hold-down time.

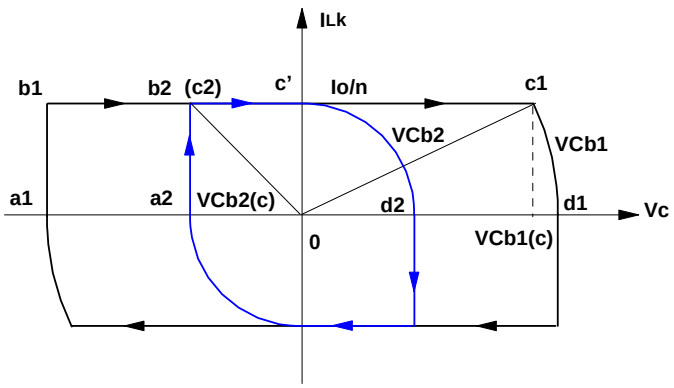


Fig. 4.8. Extreme case state trajectories, i.e. one duty cycle approaching zero.

Instead of using two identical output bridges, one could be designed to always conduct the large duty-cycle, e.g. bridge 1, and the other always to conduct the smaller duty-

cycle, as shown in Fig. 4.9. In this case, the blocking capacitor C_{b2} and the transformer T_{r2} can be designed to be smaller.

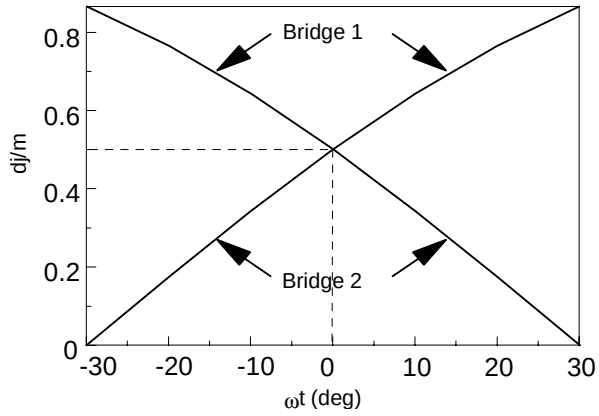


Fig. 4.9. Duty-cycle assignment.

4.4.2 Power Stage Considerations

4.4.2.1 Power Devices for QSS Isolated ZVZCS Buck Rectifier

The voltage rating of all the primary switches are the peak input line-to-line voltage, a clear advantage of buck-fed topologies. To minimize the input and output filtering component size, volume and cost, higher switching frequency is preferred. Although the switches in the front buck bridge switch at twice the PWM frequency, i.e. $2f_s$, complete ZCS operation allows slower devices such as slow IGBTs and GTO's to be used. So do the lagging-leg switches of the full-bridges, which switch at the PWM frequency f_s. The only switches which need to hard turn off the load current and so need to be fast are those in the leading legs of the full-bridges. ZVS operation of these switches favors, although not necessarily, MOSFETs to be used up to the medium power level, e.g. 5 - 10 kW. At higher power level, fast IGBT modules can be used. A small anti-parallel diode across each buck bridge IGBT is needed just to protect them from potential transient reverse voltage.

As with the dc-dc ZVZCS full-bridge converter, severe ringing can happen on the secondary rectifiers during the reverse recovery of these diodes. Minimization of the transformer leakage inductance makes this phenomenon more conspicuous. A small voltage clamp circuit across each rectifier will be effective to suppress it.

4.4.2.2 Asymmetrical Bridge Parameters

If the duty-cycle assignment as shown in Fig. 4.6 is adopted, the power handled by the two full-bridges are different. Specifically, the average current flowing through bridge 1 counts for 73.2% of the total average current processed, while that in bridge 2 is only 26.8%. As a result, the switch current rating for bridge 2 can be lower.

Besides, the blocking capacitor and the transformer parameters can also be designed to be asymmetrical, with the main aim to improve the ZCS condition of bridge 2.

4.4.2.3 Modulation Index and Isolation Transformer

The relationship between the input peak phase voltage V_m, the modulation index m, the transformer turns ratio n and the output voltage V_o under steady-state operation is given in [B3] [B5]

$$V_o = \frac{3}{2} m \cdot V_m (\cos\phi)/n, \tag{4.7}$$

where $m \in (0, 1)$, and $\cos\phi$ is the displacement factor between phase voltage and current. The maximum modulation index should be limited to about 85% to allow enough time for the primary current to reset in the worst case, that is, low input line and full load. According to (4.7), the transformer turns ratio can be decided easily.

To ease the reset of the leakage current during the free-wheeling stage, the leakage inductance of the transformers needs to be kept as low as possible. Although both

transformers in Fig. 4 need to have the same turns ratio, the average voltage-second on T_{r1} is higher than that on T_{r2} and the peak voltage second of T_{r1} is twice that of T_{r2}, so more turns should be used for T_{r1} than for T_{r2} if cores with same cross area are selected. This arrangement also helps to reduce the leakage inductance of T_{r2}, which is important practically.

4.4.2.4. Saturable Inductor and Blocking Capacitor

The criteria to size the blocking capacitor are similar to that in ZVZCS dc-dc converters. The maximum blocking capacitor voltage in each bridge is a function of load current and maximum duty-cycle. For a designed maximum modulation index, the maximum duty-cycles happen at the boundary of a 60^o sector (as defined in Figs. 4.3 and 4.6) for bridge 1 and in the middle of a sector for bridge 2. Use of a smaller blocking capacitor for bridge 2 is favorable to improve its commutation environment. However, the peak blocking capacitor voltage should be kept less than 10 - 20 % of the corresponding input voltage to limit energy circulation and secondary rectifier voltage.

The design rule for the saturable inductor in the QSS isolated ZVZCS buck rectifier is complicated by the fact that even though the voltage-second blocking capability of the saturable inductor is not enough to hold down the primary current during the freewheeling duty-cycles, the circuit still works well. This is mainly attributed to the special pulse sequence for the converter. As shown in the timing diagram in Fig. 4.5, when a bridge is in freewheeling mode, only one bridge switch is on. So even though the saturable inductor is saturated, and its inductance becomes very low, it just oscillates for a half cycle with the parasitic capacitance at the middle point of the bridge leg, while the blocking capacitor voltage will not be modified noticeably.

4.5 Design Example and Experimental Results

4.5.1 Prototype Specifications and Setup

To corroborate the operation and performance of the proposed rectifier, a 6 kW prototype intended for off-line telecommunication applications has been designed. The design is based on the following specifications:

- maximum output power: 6 kW,
- output voltage: V_o = 40 -57 V,
- input rms line voltage: 3× (305 - 457) V
- input current THD < 5%

The main designed circuit parameters and selected devices (referred to Fig. 4) are:

S_{ap}-S_{cn}, S_{2j} and S_{4j}: GT60M104 TO-264 IGBT;

D_{ap}-D_{cn}, D_{2j} and D_{4j}: DESI30-10A TO-247 diode;

S_{1j} and S_{3j}: APT8032LNR TO-264 MOSFET;

D_5/D_6, D_7/D_8: HFA140MD60C TO-244AB diode;

T_{r1}, T_{r2}: E65-3F3, 15:3:3 and 10:2:2 respectively;

L_{s1}, L_{s2}: Allied Signal MP1906× 2, 6 turns each;

L_o: EC55-3C85× 2, 16 μH;

C_{b1}: 200 V/0.47 μF× 4 polypropylene capacitor;

C_{b2}: 200 V/0.47 μF× 2 polypropylene capacitor.

The switching period T_s is selected to be 20 μs, which corresponds to a switching frequency of 50 kHz for the switches in the dual full-bridges. The front, buck bridge,

devices switch at only 33.3 kHz on the average. ZCS operation allows small package IGBTs to be used as the front bridge switches and the lagging-leg switches of the full-bridges, while ZVS operation of the leading-leg switches in the full-bridge favors MOSFETs at the targeted power level. The converter is controlled by a fast digital-signal-processor (DSP).

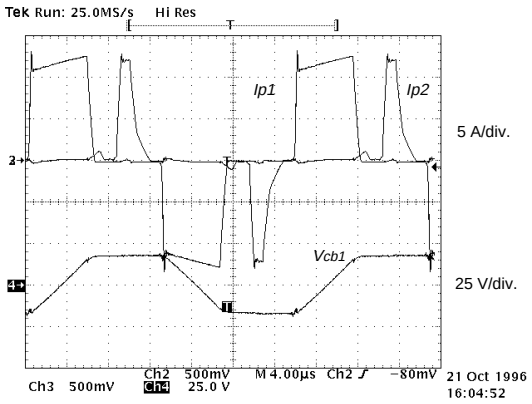
Both transformers are implemented with Philips E65-3F3 cores, but the number of turns are different. For the transformer of bridge 1, the turns ratio is 15:3:3; while the one for bridge 2 is 10:2:2, because the maximum volt-second of the latter is only half of the former. With this design, the peak flux density for the latter is about 0.11 Tesla, while that of the former is about 0.14 Tesla. With interleaving of the windings, the secondary leakage inductance is only around 100 nH for T_{r1} and 60 nH for T_{r2}.

4.5.2 Test Results with Two DC Inputs

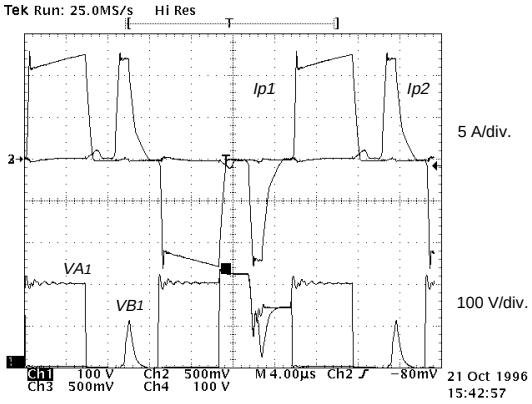
Tests of the prototype as two dc-dc ZVZCS full-bridge converters working alternatively, together with the corresponding switching of the front buck bridge switches, can be used to mimic the operation of the rectifier with ac inputs point-by-point.

Figure 4.10 shows a set of waveforms of the primary link currents and various voltages of bridge 1, which conducts the bigger duty cycle. The input dc voltages and the duty-cycles correspond to the operating condition when $wt = -20^{o}$ in Fig. 5, and modulation index $m = 0.57$.

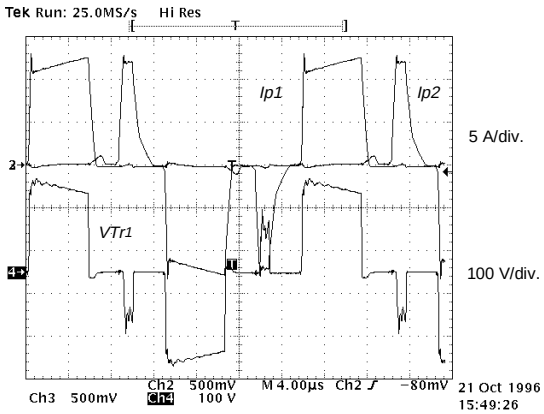
It is clear from the waveforms that both primary currents are properly reset during the freewheeling stage. The two primary currents have different on-slopes because of different acting voltages, i.e. input line to line voltages. Figure 4.10(a) shows that the voltage



(a) I_{p1}, I_{p2}, and V_{Cb1}.



(b) I_{p1}, I_{p2}, V_{A1}, and V_{B1}.



(c) I_{p1}, I_{p2}, and V_{Tr1}.

Fig. 4.10. Test results with two dc inputs corresponding to wt = -20°, m = 0.57; V_{ba} = 216 V, I_b = 5.3 A; V_{ca} = 138 V, I_c = 0.95 A; V_o = 18.3 V, I_o =60.

on the blocking capacitor holds constant when the other bridge (bridge 2 in this case) is operating. That is exactly the result of separating the two full-bridges. From the voltage waveforms at points A_1 and B_1 in Fig. 9(b), it can be seen that ZVS is achieved for the leading leg switches connected to A_1. After the freewheeling stage following the activation of the bridge, the potential of point B_1 presents an oscillatory shape. This is thought to be the resonance between the magnetizing inductance plus the saturable inductor and the parasitic capacitance of the lagging leg IGBTs. During this process, the magnetizing current is transferred to the primary side and is partially reset, as shown in the voltage waveform across the transformer, V_{Tr1}, in Fig. 4.10(c).

Figure 4.11 shows the circuit waveforms when $wt = 0^o$. In this case, the duty-cycles are the same for the two bridges. But because the value of the blocking capacitor of bridge 2 is designed to be half of that of bridge 1, its voltage is higher and the current I_{p2} is reset faster under that operating condition.

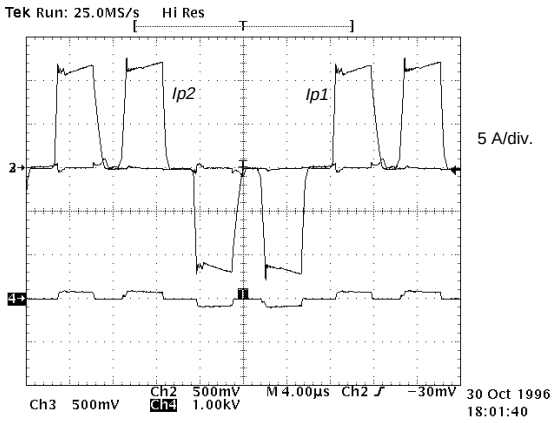


Fig. 4.11. Test results with two dc inputs corresponding to wt = 0°, m = 0.57; $V_{ba} = V_{ca} = 187$ V; V_o = 17.3 V, I_o =58 A.

Figure 4.12 shows the other extreme case, i.e. $wt = -30^o$, when the duty-cycle of bridge 2 shrinks to zero. In this case, the leading leg of bridge 2 does not receive any

switching pulse, but its lagging leg switches still receive pulses, because the duration of them is $d_0/4 + d_2/2$. As a result, with the alternative activation of the upper and lower switches, the energy stored in the output capacitance of the leading leg switches (MOSFETs) functions as an activation source, and furnishes the current which swings the potential of A_2 from one rail to the other. This current itself gets reset thereafter by the small voltage established on the blocking capacitor C_{b2}, so the resetting speed is slow. This current is a function of the input voltage and is not related to the load current. This phenomenon is particular to bridge 2 because the duty-cycle of bridge 1 never shrinks to zero.

4.5.3 Test Results with Three-Phase AC Inputs

The tests with two dc inputs ensure that the power stage can respond properly under all the input line conditions. Tests with ac inputs are undertaken with the incorporation of the input voltage sampling and digital PWM modulation to generate the duty-cycles in real time.

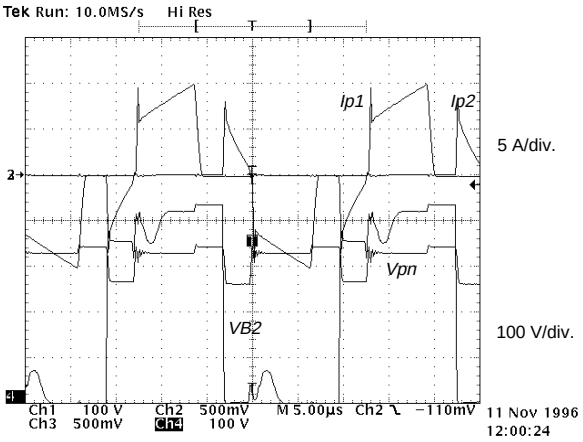
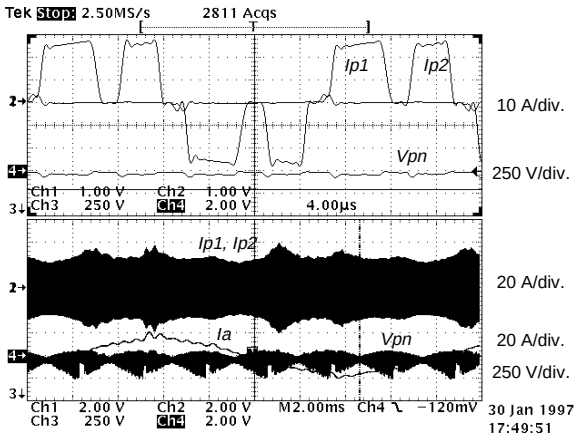
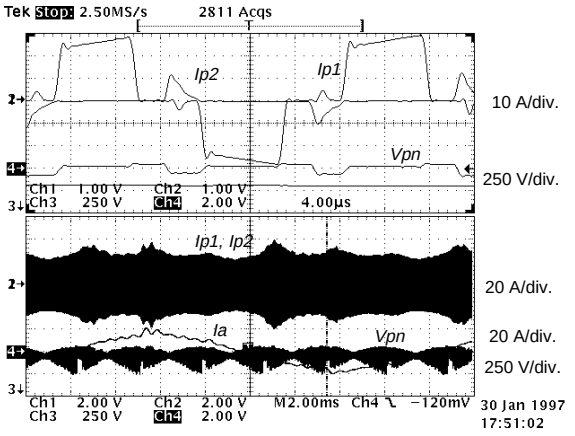


Fig. 4.12. Test results with two dc inputs corresponding to wt = -30°, m = 0.57; V_{ba} = 432 V, I_b = 4.22 A; V_{ca} = 216 V, I_c = 0 A; V_o = 41 V, I_o =50 A.

Figure 4.13 shows the measured primary waveforms, i.e. two link currents, one input phase current and the rectified primary voltage envelope V_{pn} when the power stage operates around full power under nominal input line voltage. Zoomed in Fig. 4.13(a) are the two primary currents with *wt* approaching 0^o as defined earlier. But the two duty cycles are apparently not equal. This is caused by the phase-shift introduced in the input voltage sensing path, and can be easily corrected.



(a) V_o =50.7 V, I_o = 127.7 A, P_o = 6.5 kW; zoomed part: wt approaching 0^o.



(b) V_o =50.7 V, I_o = 127.7 A, P_o = 6.5 kW; zoomed part: wt = -30^o.

Fig. 4.13. Measured waveforms at nominal input line, i.e. V_{in}=380 V.

Noticeable in Fig. 4.13(b) is an oscillatory current shape for I_{p1} when bridge 2 current is resetting, or in the second freewheeling stage after the activation of bridge 1. This is because at this instant, bridge 1 conducts the biggest duty cycle, so the voltage accumulated on its blocking capacitor is high, and this voltage exerts on the saturable inductor and makes it saturate and oscillate with the parasitic capacitance on node B_1 (the capacitance of node A_1 is much bigger than that of B_1 because MOSFETs are used for the leading leg). But as discussed above, after a half cycle of oscillation, the saturable inductor is desaturated again, so this effect is considered harmless to the circuit operation.

The measured efficiency curve at nominal input line, i.e. V_{in} = 380 V, and output voltage V_o = 50 V is shown in Fig. 4.14. The input power is measured before the input EMI filter. High efficiency is maintained for a wide load range mainly because the ZCS operation of all the IGBTs is achieved independently of load level. The peak efficiency is about 90.8%. The measured efficiency is constantly higher than the two-stage scheme with a three-phase boost rectifier with dc-side ZVT followed by a ZVZCS full-bridge dc-dc converter designed according to the same specifications [C24] [D32].

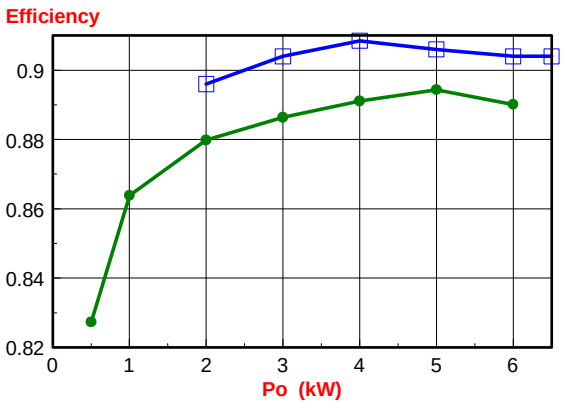


Fig. 4.14. Measured Efficiency at nominal input line V_{in}=380 V Fand output voltage V_o = 50 V.

4.6 Simplified QSS Isolated ZVZCS Buck Rectifier

The QSS isolated ZVZCS buck rectifier with split dc-dc full-bridges can realize global ZVZCS operation and achieve higher efficiency than the standard two-stage schemes because of the elimination of the switching losses in the front buck rectifier bridge. Nevertheless, the requirement for two dc-dc bridges is sometimes hindersome.

Another related issue is actually the duty-cycle loss associated with the ZVZCS operation [D33] [B8]. More specifically, when the active duty-cycles are activated, the saturable inductor needs first be driven into saturation by certain voltage-second, and theoretical analyses show that the reduction in the actually executed duty-cycle or effective duty-cycle due to this effect is a strong function of the input voltage and load current. Using two dc-dc bridges makes the situation even more complicated to compensate, and input current distortion is inevitable, as is evident from the experimental waveforms presented in the last section.

As discussed above, the reason to use split dc-dc full-bridges is the subharmonic voltage on the blocking capacitor. However, this problem is also avoided if the PWM pattern with concentrated zero duty-cycle, as shown in Fig. 2.3(a), is adopted. With this pattern, the bigger duty-cycle is also executed first and then the smaller one immediately follows. The same is true for the next half cycle with the other diagonal pair of switches in the dc-dc bridge as shown in Fig. 4.3(a) being active to keep the flux on the transformer to be balanced. As a result of this PWM pattern, the first turn-off in a PWM cycle, i.e. the switching from the bigger duty-cycle to the second (smaller) active duty-cycle, needs to happen in the front buck bridge. However, as in the non-isolated buck rectifier, the total

turn-off loss incurred on the six switches in the buck bridge is only about 21% of the total turn-off loss in the circuit. Moreover, this part of the turn-off loss is shared evenly by the six switches in the front buck bridge. The majority of the switching loss still takes place in the dc-dc bridge, and fast switches can be used to implement the leading leg switches in the dc-dc bridge.

Another advantage of this PWM pattern is that the aforementioned duty-cycle loss happens in only the first duty-cycle while the second one is left intact. This makes the compensation of the lost duty-cycle easier in some implementation, e.g. DSP-based implementation.

Figure 4.15 shows the experimental waveforms with this PWM pattern under the conditions of V_{in} = 364 V, V_o =32 V, I_o = 80 A, P_o = 2.56 kW [B8]. The duty-cycle loss is compensated through the DSP algorithm.

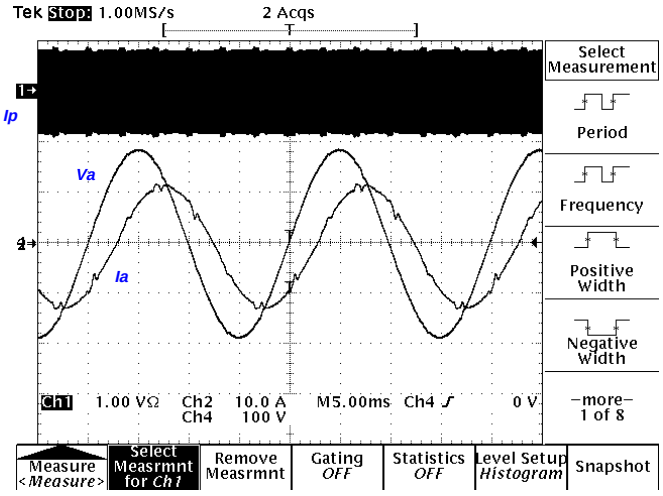


Fig. 4.15. Experimental results with PWM pattern with concentrated zero duty-cycle. V_{in} = 364 V, V_o =32 V, I_o = 80 A, P_o = 2.56 kW.

The input phase current waveform, I_a as shown, is improved compared with that with split dc-dc bridges as shown in Fig. 2.13, and the primary current which reflect the

output filter inductor current is well repeating for each 60^o sector. However, the input current distortion in the 60^o boundaries is still apparent.

4.7 Extension of QSS Isolated ZVZCS Buck Rectifiers

From the discussions above, it is known that it is the adopted ZVZCS scheme which sets some limitations on the PWM schemes. To realize certain PWM sequence, split full-bridges are necessary, which increases the circuit complexity and cost. Also, the duty-cycle loss associated with the saturation of the saturable inductor at the beginning of an active duty cycle is a strong function of several circuit operation variables, e.g. load current and input line voltages [D33]. It is usually not a concern in a ZVZCS dc-dc converter but in three-phase rectifier case, it can distort the input current, and is rather difficult to compensate.

In this section, the general topological concept of ZVZCS full-bridge dc-dc converters is first introduced, and possible implementations summarized. The concept is then extended to the case of QSS isolated three-phase buck rectifier to obtain a family of isolated ZVZCS buck rectifiers. The circuits in the family all feature a pulsating dc-link, hybrid ZVZCS operation, global soft-switching capability, and relatively simple implementation. Simulation results on selected topologies validate the principles of operation of these circuit topologies.

4.7.1 Topological Concept of ZVZCS Full-Bridge Converter

Figure 4.16 shows the circuit schematic and operation waveforms of the widely used ZVS-FB dc-dc converter with phase-shift PWM control. The shaded part corresponds to the zero duty-cycle or freewheeling stage after the leading leg switch S_1 is turned off, and the

current paths of the primary and secondary currents during that interval are also highlighted. Apparently, the freewheeling primary leakage current contributes conduction loss, extra duty-cycle loss, and energy feedback to the source. However, if the freewheeling leakage current can be reset during that interval, all the three drawbacks can be overcome or at least alleviated, moreover, the lagging leg switch, S_2 in this case, can be turned off under zero-current, and the circuit works with hybrid ZVZCS.

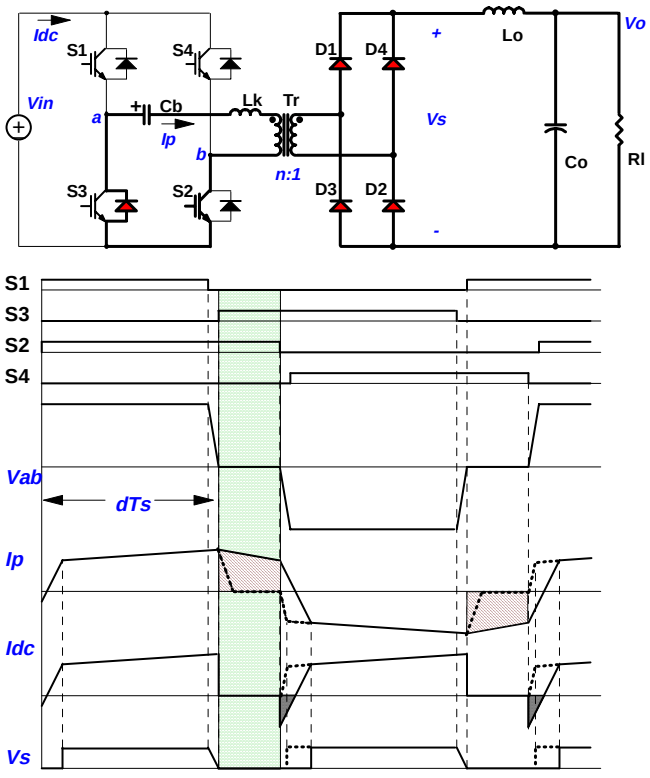


Fig. 4.16. ZVS-FB dc-dc converter and its operation waveforms.

To consider the concept to reset the primary leakage current and achieve ZVZCS, the current path in the circuit is redrawn in Fig. 4.17 with the output loading represented by a current source. Theoretically, in order to reset the primary leakage current, a voltage source with polarity opposing to the primary current direction has to be engaged in the primary current path; topologically, there can only be three such sources which can

potentially be used, as indicated with shaded circles. They are the voltage across the leading leg switch S_3, V_{s3}, the voltage on the blocking capacitor, V_{Cb}, and the voltage across the primary of the transformer, V_p.

Actually, the very first ZVZCS scheme utilizes the voltage on S_3 [D30] to achieve ZCS for the lagging leg switches. Normally V_{s3} is almost zero because of the antiparallel diode of S_3. But if the diode is removed and the switch is implemented with IGBT devices, it will reverse breakdown at about 30 -40 V, and this avalanche breakdown voltage can be used to reset the leakage current. Obviously, the leakage energy is just dissipated in the leading leg switches during the reset process, and performance improvement is very limited, if any.

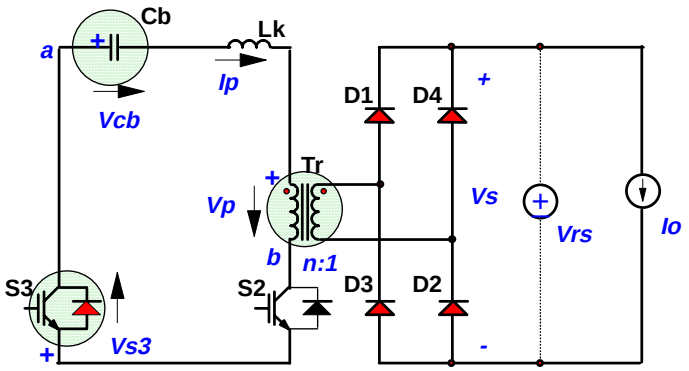


Fig. 4.17. Possible sources to reset the primary freewheeling current.

The blocking capacitor C_b is usually used in the bridge-type circuit to prevent flux unbalance, and the magnitude of the voltage across it is negligible compared to the input voltage. However, if it is intentionally shrunken, considerable voltage can be accumulated on it during the on time, and that voltage can be used to reset the primary current [D30]-[D31]. The primary current is further kept around zero by a saturable inductor during the rest of the freewheeling duty-cycle. This scheme was adopted in the QSS buck rectifier discussed earlier in this chapter [B5]-[B8].

As for as the primary voltage V_p of the transformer, normally it is zero during the freewheeling interval when both the magnetizing current of the transformer and the load current freewheels on the secondary side, and both the secondary and primary sides are shorted. Nevertheless, it is possible to temporarily engage an equivalent voltage source on the secondary side at the beginning of the freewheeling duty-cycle to hold the secondary voltage for a short interval, as shown in Fig. 4.17 with the dotted line. As long as the secondary voltage is held high, it is reflected to the primary of the transformer and the primary freewheeling current can be easily reset. Depending on the realization of that temporary voltage source V_{rs}, various different implementations have been derived recently.

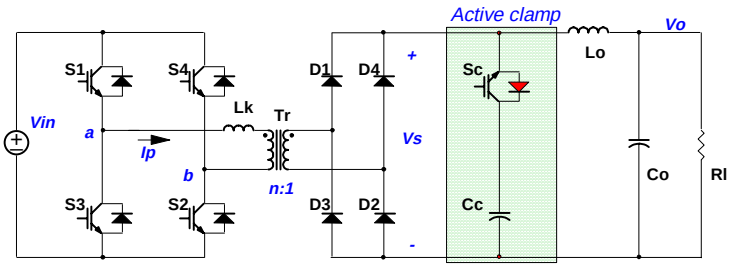
4.7.2 ZVZCS Schemes with Auxiliary Secondary Sources

The family of ZVZCS-FB dc-dc converters with auxiliary secondary sources are briefly reviewed in this subsection. All the members in the family use the temporary engagement of an auxiliary voltage source reflected to the primary of the transformer to reset the primary freewheeling current. To facilitate that, the leakage inductance of the transformers always need to be kept as low as possible. For their detailed operation principles, the original publications should be constantly referred.

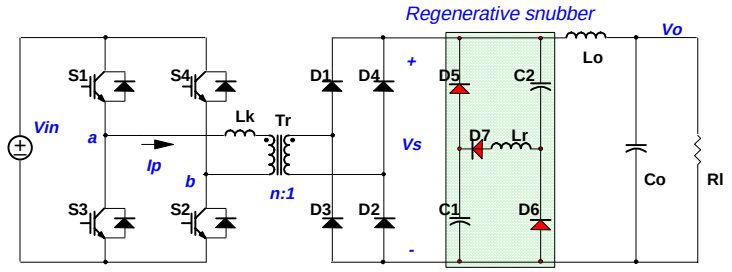
ZVZCS Scheme with a Secondary Active Clamp [D34]. As shown in Fig. 4.18(a), the circuit is the same as the ZVS-FB dc-dc converter with a secondary active clamp usually used to suppress the severe secondary ringing. However, with a slight modification to the driving timing of the clamp switch S_c, ZVZCS operation can be easily achieved. That is, with S_c turned on at the same time as or slightly later than the turn-off of the leading leg switches, the voltage on the clamp capacitor C, which is charged to the full reflected input voltage in steady-state operation, will be seen on the transformer, and the leakage current

will be reset very fast. During that time, the leakage energy is transferred to the output. The timing for S_c can be easily derived and the on-time of S_c should be just enough to reset the primary leakage current in the worst case, i.e. low-line and full load. Because of the fast resetting, ZCS can always be achieved. A side benefit of the scheme is that when the converter changes from off stage to active stage, the active clamp branch can clamp the transient voltage across the secondary rectifier, and the voltage rating of the diodes is minimized. Certainly, a fast switch is needed to implement S_c because it turns off the full load current under hard-switching at twice the switching frequency of the bridge switches.

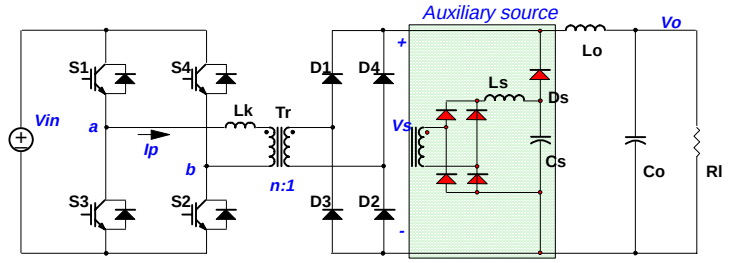
ZVZCS Scheme with a Secondary Regenerative Snubber [D38]-[D39]. As shown in Fig. 4.18(b), a regenerative or energy recovery snubber as proposed in [D37] is used on the secondary side in this scheme. Its operation principles are similar to that with an active clamp. That is, at the turn-off of the leading leg switches, the snubber capacitors C_1 and C_2 function as two temporary voltage sources in parallel to hold the otherwise fast descending secondary voltage V_s, and the primary freewheeling current is reset by this voltage. However, in this case, these temporary sources are not controllable , so that in every half period of a PWM cycle, the snubber capacitor energy is completely discharged to the output. In turn, during the transition from off stage to active stage, these sources are reestablished through a path formed by C_2, L_r, D_7 and C_1 in a resonant fashion. As a result, over-voltage on the secondary happens. Due to the relatively high impedance of the resonant tank, the snubbering or clamp effect for the secondary transient voltage is also lost, and extra voltage clamp circuit across the secondary rectifier is necessary for high power applications. The extra resonant current also flows through the bridge switches and increases their peak current rating.



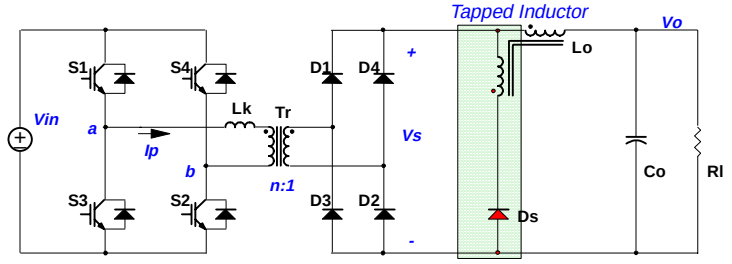
(a) With a secondary active clamp.



(b) With a secondary regenerative snubber.



(c) With an auxiliary transformer winding.



(d) With a tapping on the filter inductor.

Fig. 4.18. ZVZCS schemes with auxiliary secondary sources.

ZVZCS Scheme with an Auxiliary Transformer Winding [D35]. The auxiliary commutation source in this scheme is obtained by adding a tertiary winding on the main transformer, as shown in Fig. 4.18(c) with its number of turns less than half of the secondary winding. The primary freewheeling current is reset in exact the same way as in the regenerative snubber scheme, but by moving the snubber energy replenishing path away from the main power flow path, more freedom is created for the selection of the snuuber capacitor voltage, and for the selection of the time constants of the replenishing and discharging (current resetting) resonant tanks. The former can be achieved by varying the number of turns of the tertiary winding; the later can be achieved by adjusting the magnitude of the inductance L_s (including the leakage inductance of the tertiary winding) in the energy replenishing path, according to the active duty-cycle and freewheeling duty-cycle requirements. If the number of turns of the tertiary winding is less than half of that of the secondary winding, no over-voltage will be seen on the secondary rectifier.

ZVZCS Scheme with a Tapped Filter Inductor [D41]-[D43]. It has been known for more than twenty years that tapped inductors can be used to reduce reverse-recovery problem in basic dc-dc converters and to reset the freewheeling current in the secondary winding of the voltage-fed push-pull converter [D40] [H1]. When applied to the FB dc-dc converter, as shown in Fig. 4.18(d), it can also be used to reset the primary freewheeling current for the same reason. Several apparent drawbacks exist for this scheme. First, the ZCS capability is limited, because the available reset source on the secondary is always a fraction of the output voltage V_o, which is always lower than the reflected input voltage. Second, The output filter inductor current has jumps during switching transition stemming from the abrupt change of the magnetizing inductance of the inductor, therefore, more burden is put on the output filtering capacitor. Finally, because the secondary voltage V_s is positive during freewheeling

interval, the voltage gain of the converter is modified and is a nonlinear function of the duty-cycle. For these reasons, it is suited only for medium power applications.

4.7.3 A Family of QSS ZVZCS Buck Rectifiers

A family of QSS isolated ZVZCS buck rectifiers can be obtained by incorporating the ZVZCS-FB dc-dc converters reviewed above into the QSS scheme as shown in Fig. 4.1(c). The resulting converter topologies are shown in Fig. 4.19 in their generic form. Certainly, operation in the isolated three-phase buck rectifier setting is complicated by the fact that two different input voltages and duty-cycles will run sequentially on the same dc-dc bridge.

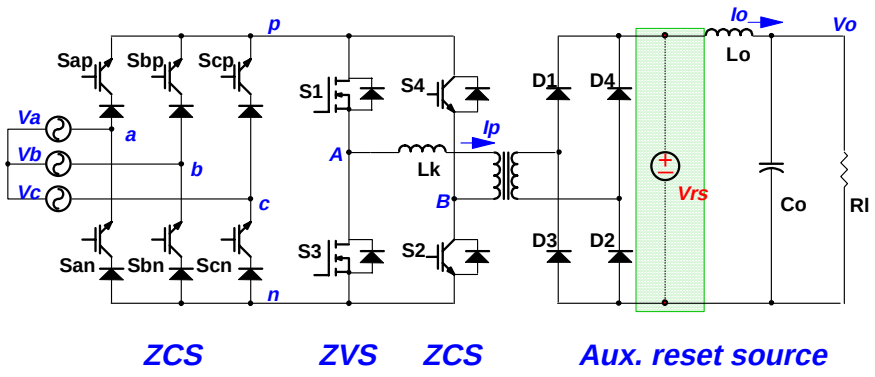


Fig. 4.19. A family of isolated ZVZCS buck rectifiers.

Because of the lack of filtering components, the dc-link voltage is a pulsating dc, with its levels always being the two rectified input line-line voltages. The leading leg switches S_1 and S_3 in the full-bridge switch under ZVS turn-on, but need to hard turn off the load current, and for that reason, faster switches such as MOSFETs or fast IGBTs are preferred. Although a full-bridge secondary rectifier is shown in Fig. 4.19, all the circuit members can work equally well with a push-pull secondary rectifier and a center-tapped transformer.

The so-called six-step PWM or space vector modulation is usually desirable to be used to control the family of ZVZCS buck rectifiers because the number of switching actions can be minimized. Different PWM patterns or sequences can be derived. Shown in Fig. 4.21 are two typical ones which correspond to the input line combination in the shaded 30^o segment within a 60^o sector of the input line cycle in Fig. 4.20.

Figure 4.21(a) shows the full-bridge output voltage V_{AB} generated by the PWM pattern with a concentrated or lumped zero (or freewheeling) duty-cycle. With this pattern, the large active duty-cycle, $T_1/2$, is always followed directly by the small duty-cycle, $T_2/2$. Actually the first and second half of the pattern is well repeating, and carrier wave with twice the complete pattern frequency can be used to achieve faster control performance. As discussed in [F11] [C6], the charge control concept for three-phase buck rectifiers can be easily extended to generate the pattern and control the family of ZVZCS buck rectifiers with very simple analog and logic circuitry.

It should be mentioned that if the pattern with concentrated zero duty-cycle is used, the turn-off after running the bigger duty-cycle has to happen in the front buck bridge switches, and the feature that the front buck bridge switches switch under complete ZCS is lost. However, because the voltage transition across the turn-off switch is only the difference between the two input line-line voltages, V_{ac} - V_{ab} for the case shown in Figs. 4.20 and 4.21(a), it can be shown that the turn-off loss transferred to the front buck bridge accounts for only about 21% of the total turn-off loss in the converter. Further, this part of the turn-off loss is evenly distributed in the six switches in the front buck bridge, thus each needs to sustain only 3.5%, and this usually does not present any problem. The majority of the turn-off loss, i.e. about 79%, still happens in the leading leg switches in the full-bridge during the transition from the second or smaller duty-cycle to the zero duty-cycle.

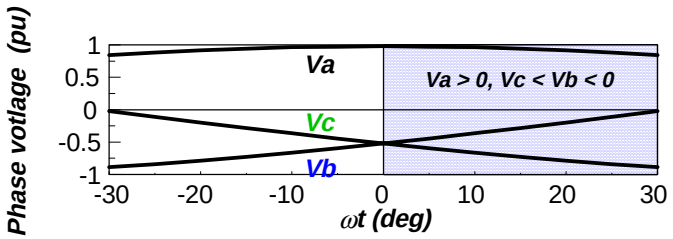
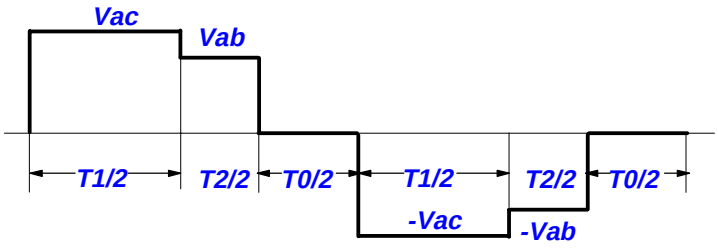
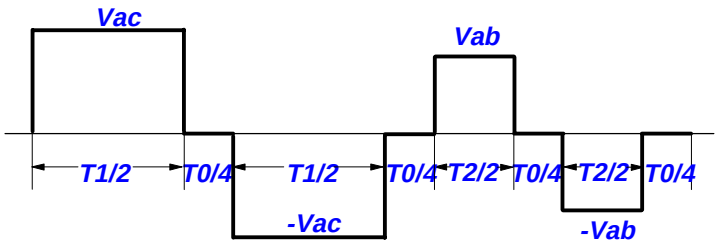


Fig. 4.20. Input phase voltages in a 60° sector.



(a) PWM with concentrated zero duty-cycle.



(b) Center-aligned PWM (with distributed zero duty-cycle).

Fig. 4.21. Six-step PWM patterns.

On the other hand, the center-aligned PWM pattern shown in Fig. 4.21(b) has evenly distributed zero duty-cycles, the bridge output voltage V_{AB} is essentially the same as that mandated in the single-stage matrix buck rectifier shown in Fig. 4.1(b). With this pattern, almost all the turn-off losses happen in the full-bridge. There is no symmetry existing within the complete pattern cycle. Therefore, it rules out the possibility to use simple analog carrier- or charge control-based realization. Digital algorithm-based modulation has to be

used. For that reason, the discussions in the rest of the paper will be concentrated on PWM with lumped zero duty-cycle.

It should be pointed out that, for most of the members in the family of QSS ZVZCS buck rectifiers, at least one of the active duty-cycles will be modified more or less by the intervention of the auxiliary commutation action if normal algorithm- or carrier-based modulations are used. One elegant solution to solve the problem is to use the charge control concept in [F11], with which the actual input phase currents are averaged respectively on a cycle-by-cycle basis, and the average input phase currents are accurately controlled, no matter what kind of waveform shapes the phase currents may take.

4.7.4 QSS ZVZCS Buck Rectifier with a Secondary Active Clamp

High-frequency PWM cycle simulations are conducted for selected members in the family to validate the operation principles of the proposed QSS ZVZCS buck rectifiers. The circuit parameters used in the simulation are listed as follows:

Input phase voltage V_ϕ = 220 V rms;

Turns ratio of the transformer n_p:n_s:n_s = 5:1:1;

Primary magnetizing inductance L_m = 1.7 mH;

Primary and secondary Leakage inductance L_{kp} = 0.5 μH and L_{ks} = 40 nH on each side, respectively;

Output voltage V_o = 48 V, and output current I_o = 125 A with constant current sink assumed;

$\omega t = 20^o$ referred to Fig. 4.20, and V_{ab} = 531 V and V_{ac} = 346 V;

Switching frequency f_s = 50 kHz with lumped zero duty-cycle in Fig. 4.21(a), and carrier frequency $f_c = 2f_s$.

Figure 4.22 shows the simulated operation waveforms for the QSS ZVZCS buck rectifier with a secondary active clamp under nominal line voltage and full load.. It can be clearly seen that the primary freewheeling current is reset very fast, and the clamp switch S_c

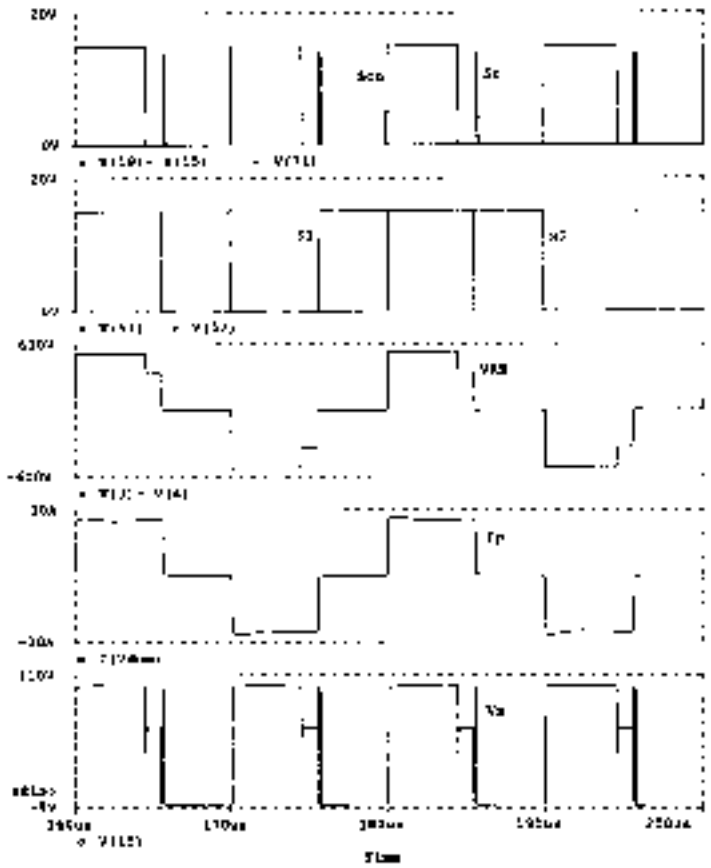


Fig. 4.22. Simulation results of QSS ZVZCS buck rectifier with an active clamp.

only needs to be on for a very short interval. The two active duty-cycles are clearly shown on the waveforms of V_{AB} and the secondary voltage V_s. The transition from the bigger duty-cycle to the smaller one happens when the front buck bridge switch, S_{cn} in this case, is turned off, while the transition from the second active duty-cycle to the freewheeling stage is activated by turning of the leading leg switches, S_1 and S_3, in the full-bridge. S_2 and S_4 switch under ZCS because the freewheeling current has already been reset at the beginning of the freewheeling stage.

As listed above, center-tapped transformer secondary windings are used. To make the secondary current freewheel smoothly after the clamp switch is suddenly turned off, an extra freewheeling diode is added to the output of the secondary rectifiers. Secondary voltage is well clamped by the active clamp branch.

The operation of the other topologies in the family are also validated by simulation. Limited by space, the results are not presented here.

4.8 Summary

A new QSS isolated three-phase ZVZCS buck PWM rectifier for high-power off-line applications is proposed in Chapter 4. It consists of a three-phase buck bridge switching under zero current and a phase-shift-controlled full-bridge with ZVZCS, while no intermediate dc-link is involved. Input power and displacement factor control, input current shaping, tight output voltage regulation, high-frequency transformer isolation, and soft-switching for all the power devices are realized in a unified single stage. Because of ZVZCS operation, it can work at high switching frequency while maintaining reliable operation and achieving higher efficiency than that with standard two-stage approaches.

The general topological concept of ZVZCS full-bridge dc-dc converters is also introduced, and possible implementations summarized. The concept is then extended to the case of QSS isolated three-phase buck PWM rectifier to obtain a family of isolated ZVZCS buck rectifiers. The circuits in the family all feature a pulsating dc-link, hybrid ZVZCS operation, global soft-switching capability, and relatively simple implementation. Simulation results validate the principles of operation of these circuit topologies.