System Design of a High-Temperature Downhole Transceiver

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ABSTRACT

The oil and gas industry, aerospace, and automotive industries are constantly pushing technology beyond their current operational boundaries, spurring the need for extreme environment electronics. The oil and gas industry, in particular, is the oldest and largest market for high-temperature electronics, where the operating environment can extend beyond to 200℃. The electronics currently employed in this field are only rated to 200℃, but with the rise of wideband gap technologies, this could be extended to 250℃ or more without the needed for active or passive cooling. This reduces the complexity, weight, and cost of the system while improving reliability. In addition, current downhole telemetry data rates are insufficient for supporting more sophisticated and higher resolution well-logging sensors. Increasing the data rates can also save the industry significant amount of time by decreasing the amount of well-logging excersions and by increasing the logging speed.

Previous work done by this research group saw the prototyping of a high bit rate transceiver operating at 230 MHz – 300 MHz and 230℃; however, at these frequencies, the system could not meet size requirements. Thus, a new high-temperature high data rate transceiver design using the 2.4 GHz – 2.5 GHz ISM band is proposed to miniaturize the design and to allow for IC implementation. The transceiver was designed to meet the minimum specifications necessary to give designers flexibility between power consumption and performance. The performance of the design was simulated using AWR design environment software, which shows the system can support a downlink data rate up to 68 Mbps and an uplink data rate up to 170 Mbps across 10 channels. The effects temperature has on the system performance is also evaluated in the simulation.

System Design of a High-Temperature Transceiver

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GENERAL AUDIENCE ABSTRACT

The oil and gas industry is currently the largest and oldest market for high-temperature electronics. One of the major applications within this industry for high-temperature electronics is known as well-logging, during which a suite of sensors and systems is lowered into a well to survey the health and geology of the well. Among these sensors and systems, the communication system is one of the most crucial components as it relays real-time data back to the surface during the well-logging operation. Current high-temperature communication systems are capable of operating up to 200 ℃, meeting the operating requirements of current wells. As these wells deplete, however, new wells must be explored, and higher operating temperatures are expected. In addition, the communication systems currently employed fail to meet increasing data rate demands due to the growing complexity of the sensors.

Recent developments in semiconductor technologies have given rise to devices, which can increase the operating temperature of electronics up to 250 ℃ while meeting demands for high data rate communication systems. Previous work has leveraged these devices to prototype such a system; however, the proof-of-concept failed to meet size and weight restrictions of practical systems. Therefore, a new system design for a high-temperature high data rate communication system is proposed. The system operates at 2.4 – 2.5 GHz to miniaturize the circuits and make chip implementation possible. The impacts of temperature on the system are investigated and the system performance is simulated within its intended operating temperature range. Developments from this research can be extended to the automotive and aerospace industries, where demand for high-temperature electronics is growing.

To my parents, grandparents, sisters, and the love of my life

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Chapter 1

Introduction

The oil and gas, aerospace, and automotive industries are constantly pushing technology past current operational boundries. This has caused a growing demand for harsh-environment electronics in high radiation, low temperature and high-temperature environments. High-temperature electronics, in particular, have seen major improvements with the advancement of wideband gap semiconductors and other technologies, including silicon-on-insulator (SOI) [1]. These technologies have been proven to operate reliably above 200℃ and extend up to 300℃ or 600℃. This significantly improves the reliability, cost and simplicity of high-temperature systems by allowing circuits to operate in a high-temperature environment without the need for bulky active or passive thermal management.

1.1 Motivation

Of the industries mentioned, the oil and gas industry is the oldest and the largest market for high-temperature electronics [2]. High-temperature electronics are deployed in this industry to monitor well health, geological features and environmental factors during well-logging operations. They also control actuators and monitor environmental and equipment status during drilling operations. Temperatures in the downhole environment typically increase at a rate of $25\ ℃/km$, reaching temperatures of 150℃ and extending beyond 260℃ [3, 4]. The size and weight restrictions of the downhole environment make the use of heat sinks or fans undesirable, therefore electronics operating downhole must do so without the need for cooling.

In addition to the need for high-temperature electronics, there exists a need for higher data rates in downhole telementry systems. Tools used in well-logging operations are becoming more sophisticated with higher resolutions and more sensors. By increasing system data rates, logging speeds can be increased or more tools can be used minimizing the amount of time or the number of trips needed for well evaluation [5].

This thesis work focuses on well-logging applications as this operation allows for wired communication channels instead of wireless systems typically employed during drilling

operations. Wired connections allow for higher bandwidths and faster data rates over longer distances.

1.2 Current Status

Technology currently employed by the oil and gas industry is only rated to operate up to 200℃ [5]. With the use of Dewar flasks, an insulating device utilizing a vacuum, downhole electronics have been able to operate in ambient temperatures up to 260℃ for a finite amount of time [3]. Current well-logging telemetry systems from Schlumberger are described as having high data rates of 2 – 4 Mbps and low errors over cables exceeding 12 km. These systems use error-correction protocols to ensure low error rates [5].

From [6], a well-logging telemetry system achieving high bitrate uplink of 2 Mbps and low BER of 10^{-6} over a 7.62 km multicore conductor is designed. The telemetry system is based on the standard ADSL operating in the low frequency spectrum (3-300 kHz) and temperatures up to 200℃. The system allocates more bandwidth to the uplink operation than the downlink to support higher data rates in the uplink direction. Additionally, the system supports multiple tools by utilizing separate conductors to transmit and receive differential signals.

Previous work done by this research group [7-15] focused on designing and prototyping a high-temperature cable modem system to increase the datarate, the number of tools and the operating temperature of well-logging telemetry systems. The system operates in the VHF band (30-300 MHz) up to 230℃ and supports up to 6 tools. The transceiver for each tool uses the superheterodyne radio architecture and supports an uplink bitrate up to 20 Mbps and a downlink bitrate of 6.7 Mbps. With the use of FDMA, the 6 tools are able to operate on dedicated channels, allowing this system to reach 120 Mbps and 36 Mbps for the uplink and downlink, respectively. Each transceiver shares a 30 m coaxial channel which interfaces with a 10 km radio over fiber (RoF) link. The use of fiber optics allows for wider bandwidths and lower losses over large distances than multicore or coaxial cables. Only the transceiver design was prototyped and tested in this works. The RoF and coaxial links were only implemented in simulation.

1.3 Major Contributions

Though the previous transceiver prototype successfully met the design goals, an integrated circuit for high-temperature high-bitrate downhole telementry has not yet been created. This work focuses on redesigning the transceiver system with that goal in mind. The first prototype of this will be a discrete design to validate the system, followed by RFIC or MMIC implementation in GaN-SiC, SiC, or SOI technologies.

Operating in the VHF band, the previous transceiver design was too large for the applications for which it was intended. At these frequencies, microstrip lines are large for discrete implementation, while passive components are too large for integrated circuits. The 2.4 – 2.5 GHz ISM band was selected for the transceiver design because of these restraints. This frequency band allows for an overall reduction in the size of microstrip lines and passive components, and it enables pratcial implementation as an RFIC or MMIC. In addition to choosing a higher frequency, the direct-conversion radio architecture was chosen for the new system design to reduce the number of filters and active blocks, which allows for easier integration as an IC and reduces the effects of temperature compared to a superheterodyne architecture.

The previous transceiver design was proven capable of significantly higher data rates of current downhole systems at temperatures up to 230℃. The overall system was able to achieve 120 Mbps uplink and 40 Mbps downlink across 6 tools. More tools and higher datarates are aquired with the use of the 2.4 – 2.5 GHz ISM band due to its larger bandwidth of 100 MHz, compared to the 62 MHz used in the previous system.

In addition, the system presented in this work is intended to operate from room temperature up to 250℃. While it is up to the circuit designers to implement system blocks that can operate up to these temperatures, the system designer must be mindful of how components in the system behave and how this affects the system performance [4]. To this effect, this work performs an analysis on how the transceiver design behaves over its intended operating temperature range based on characteristics exhibited by circuits that have been shown to operate at high temperatures. Suggestions on how to work around changes in system performance with temperature are discussed in the work, as well as comments based on behaviors not shown in the analysis that could be encountered.

Finally, while the objective of this research is to produce an IC implementation, the first iteration of the system design presented in this work will be discrete components; therefore, the

transceiver has been designed for discrete implementation. This work provides guidance and discussion on how the system should be modified for IC implementation.

1.4 Organization of this Thesis

This thesis is organized as follows: Chapter 2 explains necessary background information and concepts regarding radio system design, Chapter 3 presents the proposed system design, and Chapter 4 discusses the transceiver performance.

Chapter 2 will breifly discuss common radio architectures and modulation schemes used in communication systems, such as budget analysis, which is used to allocate system specifications, radio over fiber systems,and high temperature components useful in implementing the system design.

In Chapter 3, the proposed system design will be presented. The overall system architecture will be discussed, followed by each subsystem. The first subsystem will be the radio-over-fiber link, followed by the downhole coaxial channel. Next, the proposed RF transceiver design and frequency plan will be presented. The derivation of receiver and transmitter overall specifiations, design philosophy, and block specifications will be discussed. The chpater will conclude with comments on how the system design can be adjusted for RFIC or MMIC implementation and considerations for the surface transceiver.

Chapter 4 expands upon the transceiver design presented in the last sections of Chapter 3 by analysing the simulated performance of the design. The first section will provide a breif review of the AWR design environment from National Instruments used to simulate the transceiver. Next, the receiver performance will be analysed through its error-vector magnitude performance and its performance over a wide range of temperatures. Lastly, the same discussion will be held for the transmitter design. Chapter 5 summarizes and concludes this work.

Chapter 2

Preliminaries

This chapter will discuss necessary background and concepts for radio system design. An overview of two common radio architectures, an explanation of modulated signals, and concepts pertaining to budget analysis and radio over fiber architecture will be presented. The chapter will conclude with the identification of commercial high-temperature components for use in the system. This information gives insight into the radio system design and design procedure presented in Chapter 3.

2.1 Radio Architectures

When determining a system architecture for a design, understanding the advantages and disadvantages of radio architectures is as important as understanding the system goals and requirements. Many radio architectures can be implemented, such as superheterodyne, direct conversion, low-IF, and upconversion-downconversion [16, 17]. From these architectures, superheterodyne and direct conversion are the most relevant to this thesis work. The superheterodyne was the architecture chosen in the previous work [7-15] that serves as the basis for this thesis, and direct conversion was chosen for the system design presented in Chapter 3.

2.1.1 Superheterodyne

Of all the radio architectures, the superheterodyne – superhet for short – transceiver is one of the most common. Figure 2.1 illustrates the block diagram of a typical superheterodyne receiver. The superhet design consists of three sections: radio frequency (RF), intermediate frequency (IF) and baseband (BB). These sections were named after the frequency at which they operate. The RF section operates at the frequency band in which the desired signals' carrier frequency resides and contains the following blocks: pre-select bandpass filter, low noise amplifier (LNA), image rejection filter and the mixer. The IF section operates at a reduced frequency band from the RF section, which is determined by the difference between the RF carrier frequency and the LO frequency. This section encompasses the IF bandpass filter, IF amplifier and the quadrature mixer. The baseband section of the receiver shown uses a quadrature architecture which operates at a

frequency ranging from DC to half the signal bandwidth. Since the signal has been down-converted to be centered at 0 Hz, the baseband section is split into in-phase (I) and quadrature (Q) channels to properly demodulate signals. This section is composed of the baseband amplifiers and the lowpass filters.

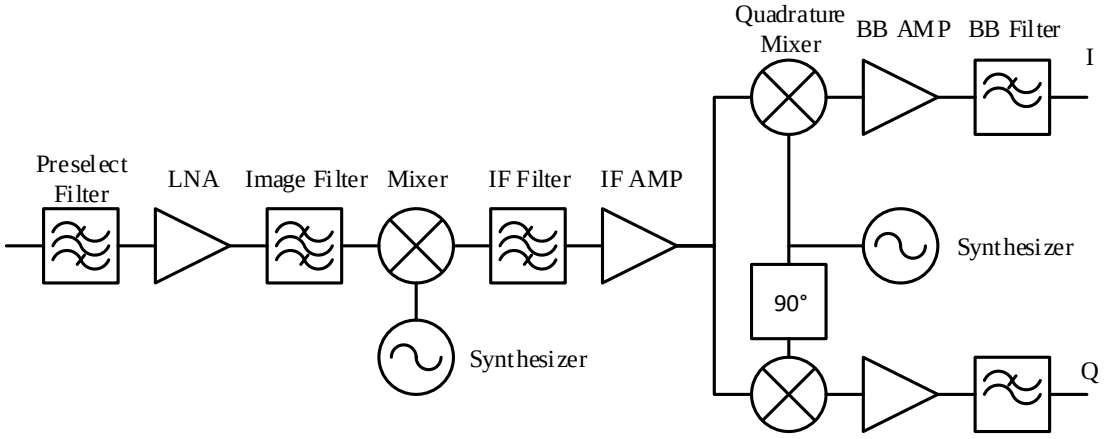

Figure 2.1: Superheterodyne Receiver Block Diagram

The RF section, IF section, and LO all operate at different frequencies, meaning IF and LO leakages can be mitigated through proper filtering to meet FCC requirements. The disadvantages to this architecture are the number of active blocks and filters required. More active blocks in this system can lead to degraded noise figure, linearity issues and design complexity. Additionally, more active blocks may lead to a larger variation in system performance over a wide temperature range. The image rejection and IF filters require the LNA and Mixer to be matched to 50 Ω and typically prevent a fully integrated design. These filters have a fundamental tradeoff between the level of image rejection that can be achieved and how well adjacent channels are rejected based on the chosen IF frequency [16, 17].

2.1.2 Direct Conversion

The direct conversion radio architecture, also referred to as homodyne or zero-IF architecture, had been a failed architecture in the era that is was invented; however, with the rise of modern integrated and wireless technology, the direct conversion architecture has become widely used within the past three decades [16, 18, 19]. The direct conversion architecture operates by converting the RF signal directly to DC, omitting the IF section entirely. An illustration of the

direct conversion receiver block diagram can be found in Figure 2.2. The RF section contains the pre-select bandpass filter, the LNA, and the quadrature mixer, while the baseband section is the same as that used in the superhet design in Figure 2.1.

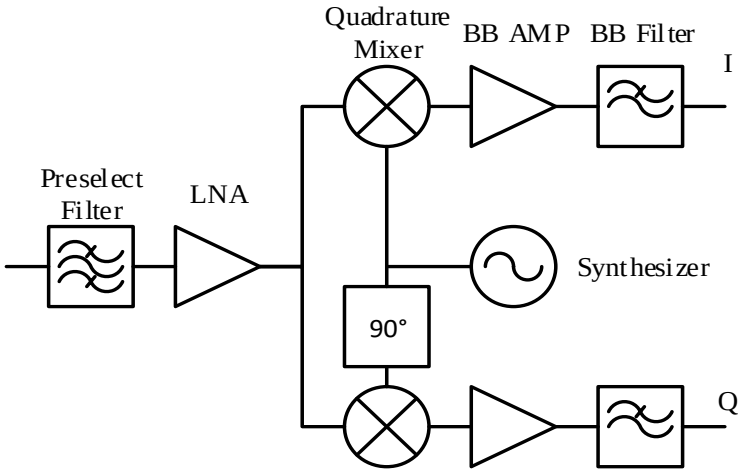

Figure 2.2: Direct Conversion Receiver Architecture

The advantages of direct conversion are as follows: the omission of the image rejection filter, the IF filter, and a down conversion stage. The omission of the filters means the LNA and mixers are no longer required to match to 50 Ω, making this architecture a candidate for a fully integrated design. The operation of the direct conversion radio makes frequency planning simple because there are no image frequencies, and the LO frequency is set equal to the desired signal's carrier frequency [16-19].

The disadvantage of direct conversion is the potential for reverse transmission and self-mixing. The removal of the IF stage requires the LO frequency to be the same as the desired signal, and LO leakage can result in reverse transmission. LO leakage can also result in self-mixing to DC in the baseband, which can saturate subsequent blocks [16-19]. This architecture also suffers from what is known as IQ mismatch which results from variations of gain and phase between the I and Q baseband channels.

2.2 Modulation

Another important aspect in radio system design is the modulation scheme the system uses to transmit and receive information. Modulation is the means by which the baseband (the data-

carrying analog signal) is used to modulate the amplitude, phase, or frequency of a sinusoidal carrier. These forms of modulation are known as amplitude shift keying (ASK), phase shift keying (PSK) and frequency shift keying (FSK), respectively [16, 17]. In addition to discussing modulation schemes most relevant to this work, the following sections will examine other concepts related to modulation scheme use in radio communications.

2.2.1 Quadrature Phase Shift Keying

Quadrature Phase Shift Keying (QPSK) is a form of PSK which contains four symbols in its constellation. All four symbols in the constellation contain the same amplitude, and each symbol is located at 45 ° in each quadrant on a real-imaginary plane. This form of modulation only transmits two bits per symbol but is relatively insensitive to noise and distortion. The four symbols of QPSK can be represented using the following equation [16]:

$$X_{QPSK}(t) = \alpha_1 A_C \cos \omega_C t + \alpha_2 A_C \sin \omega_C t \tag{2.1}$$

where $\alpha_1 \pm 1$ and $\alpha_2 = \pm 1$, A_C is the carrier amplitude and ω_c is the frequency of the carrier. The constellation for QPSK can be found in Figure 2.3. The real axis refers to the in-phase channel

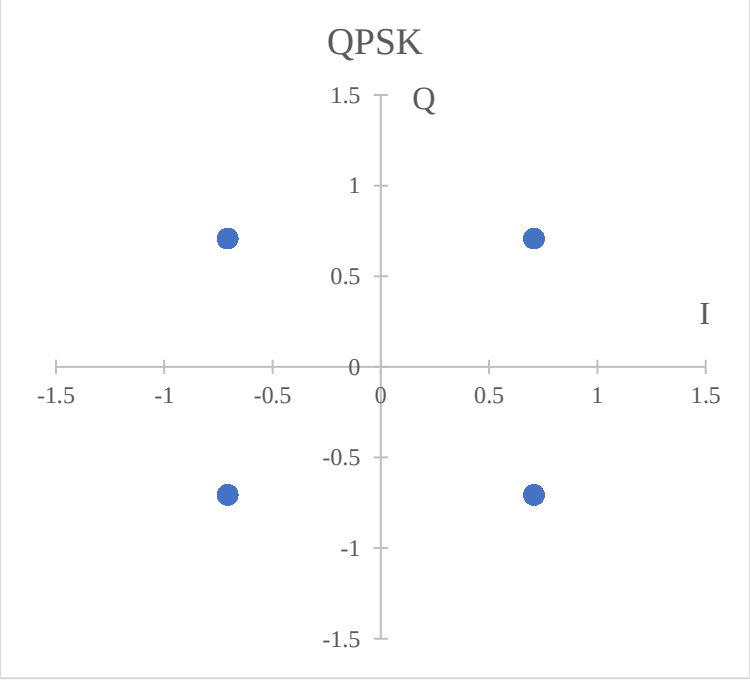

Figure 2.3: QPSK Constellation

amplitude, while the imaginary axis refers to the quadrature channel of the baseband sections of Figures 2.1 and 2.2.

2.2.2 Quadrature Amplitude Modulation

Quadrature Amplitude Modulation (QAM) is a combination of ASK and PSK modulation where both the amplitude and phase of the carrier signal is varied to achieve higher data rates than ASK and PSK can achieve alone. This scheme can have different orders denoted as M-QAM, where M refers to the number of symbols that make up its constellation and how many bits are transmitted per symbol. Common orders of QAM are 16-, 32- and 64-QAM, which transmit 4, 5 and 6 bits per symbol, respectively. Each symbol that makes up the constellations for each order of QAM can be expressed as:

$$X_{M-QAM}(t) = \alpha_1 A_C \cos \omega_C t - \alpha_2 A_C \sin \omega_C t \tag{2.2}$$

where A_C is the carrier amplitude, ω_c is the carrier frequency, and α_1 and α_2 are coefficients for each symbol [16]. As an example, the coefficients for 16-QAM are $\alpha_1 = \pm 1, \pm 2$ and $\alpha_2 = \pm 1, \pm 2$. The different combinations of coefficients result in 3 different amplitudes and 12 different phases. The power of these signal are typically defined by the average signal power and its peak-to-average power ratio. The constellations for 16-, 32- and 64-QAM are illustrated in Figure 2.4, 2.5 and 2.6.

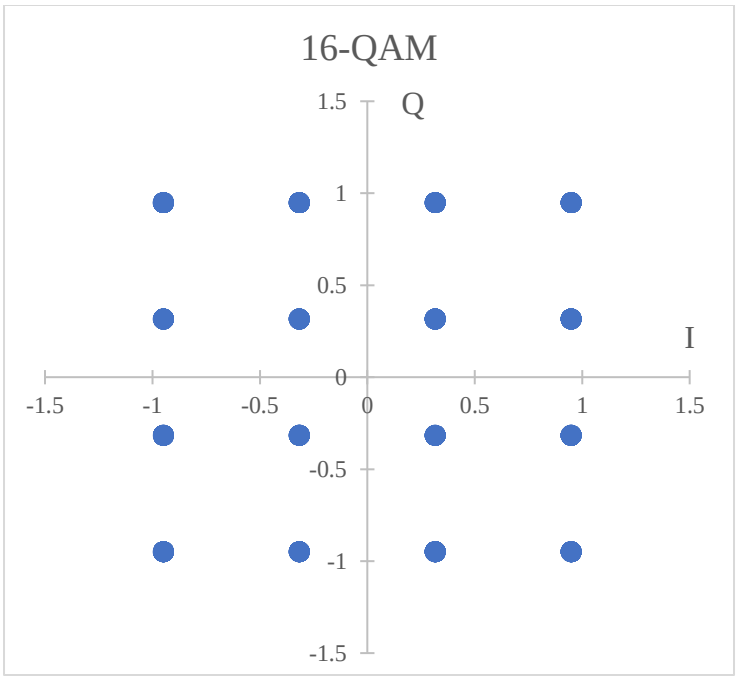

Figure 2.4: 16-QAM Constellation

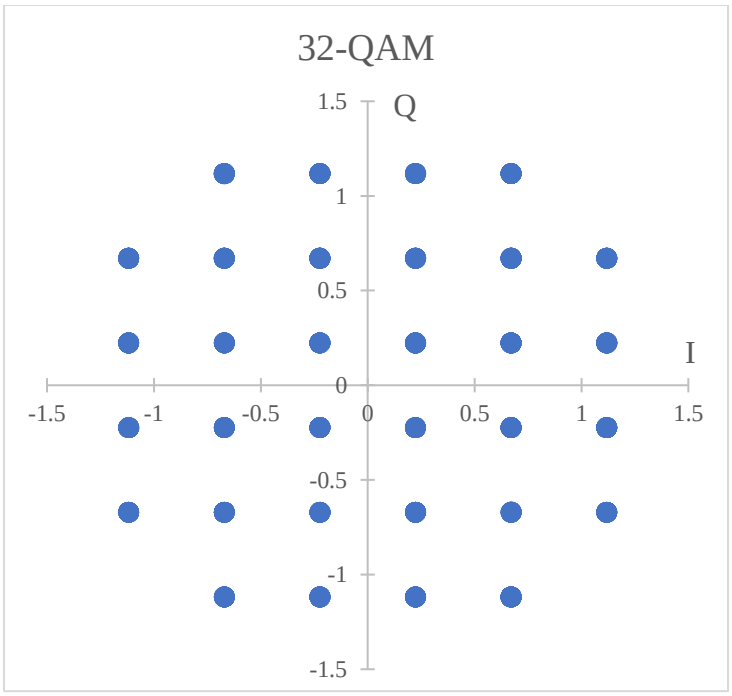

Figure 2.5: 32-QAM Constellation

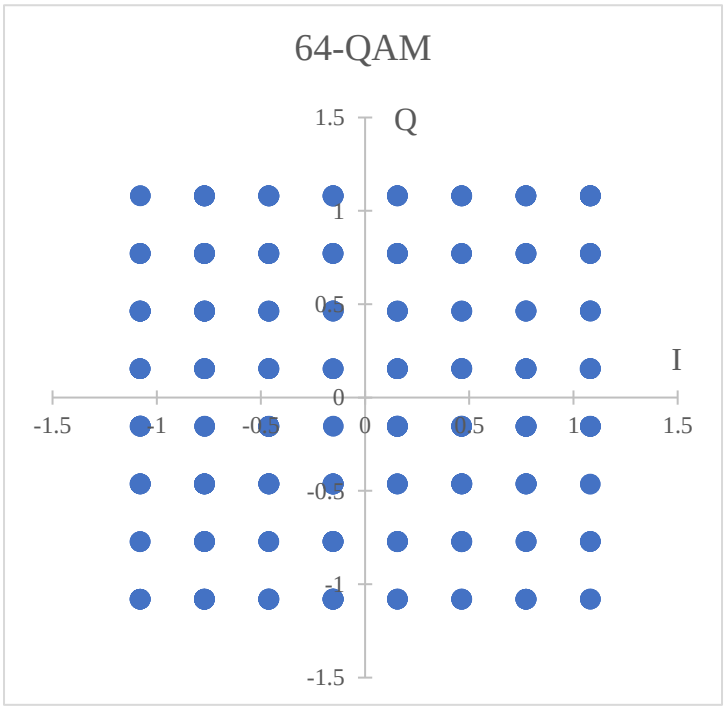

Figure 2.6: 64-QAM Constellation

2.2.3 Frequency Division Multiple Access

Frequency division multiple access (FDMA) is a technique in radio communications that allows multiple radio transceivers to operate simultaneously while achieving full-duplex communication. This designates two separate bandwidths specifically to transmitting and receiving signals. The transmit and receive bands are split further into channels that can be utilized by other transceivers. By splitting the bandwidth into a transmit band and a receive band, a diplexer, instead of duplexer, can be used at the transceiver front-end to discriminate between transmit and receive traffic. This allows a transceiver to achieve a full-duplex operation, which simultaneously transmits and receives signals without impairing either function. Splitting the bandwidth into channels allows each receiver and transmitter in the communication system to operate parallel to each other by tuning to different channels. As long as the signal is confined within the channel bandwidths, FDMA enables simultaneous parallel operation of multiple full-duplex transceivers.

2.2.4 Pulse Shaping

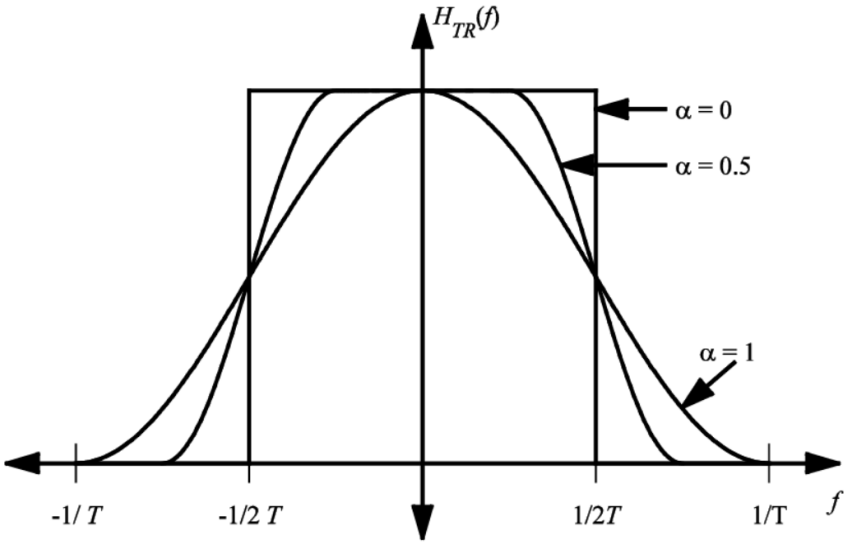

Figure 2.7: Power spectral density of raised cosine signal [17]

The purpose of pulse shaping is to choose an appropriate baseband signal shape that allows for efficient spectral efficiency while preventing intersymbol interference (ISI). This is important for implementing FDMA, because the signals must be confined within an allocated channel

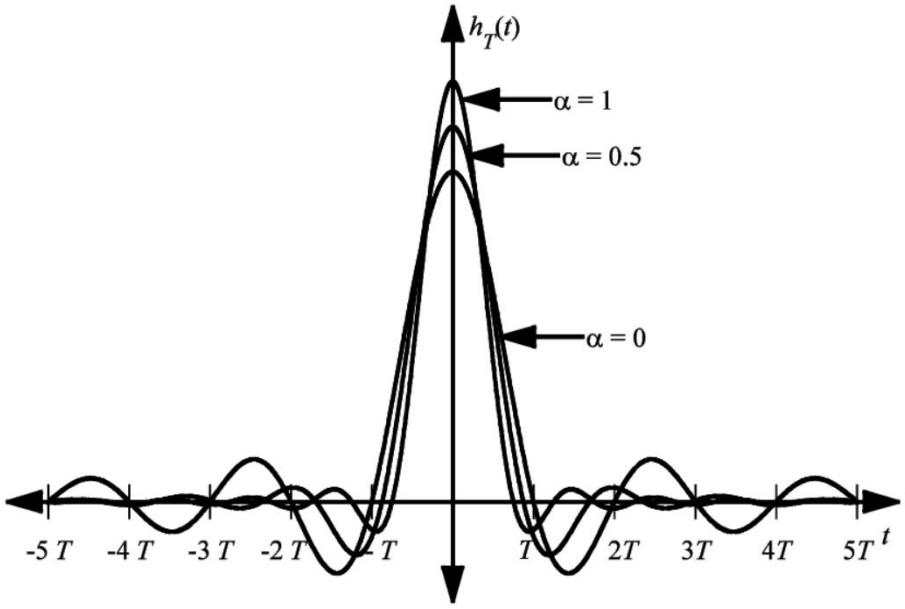

Figure 2.8: Time domain waveform of a root raised cosine signal [17]

bandwidth. Consider the basic pulse shape: the square waveform. Its spectrum – the sinc function – is infinitely wide and has significant close-in sidelobes. In FDMA, these sidelobes will land within other channel bandwidths and cause interference to those signals. When this spectrum is passed through the channel select filter of a receiver, these sidelobes are removed, resulting in an increase of error rates in the system due to time domain distortion of the square waveform causing interference with subsequent symbols. This is just one possible source of ISI, but it can also be a result of certain pulse shapes. Popular pulse shapes that prevent sidelobes and ISI are based on the raised cosine representation in the frequency domain [17]. Figures 2.7 and 2.8 illustrate the frequency respones and impulse response of the pulse shape filters. This waveform is more efficient in its use of the available channel bandwidth, allowing for higher symbol rates. The figures indicate a parameter called the roll-off factor, α, which is used to control the PSD and time-domain shapes. Larger values of α negatively affect the PAPR of the modulation and the spectral efficiency, but it also reduces the side lobes in the time-domain.

2.2.5 Signal to Noise Ratio

The signal to noise ratio (SNR) is a comparison of the signal power to the noise power and determines the detectability of the signal and the integrity of the information extracted from it. The SNR depends on factors like the modulation scheme used by the system, the bandwidth of the

receiver, the pulse shaping used, the symbol rate of the signal, and the desired bit error rate (BER) [16, 17]. These factors are combined into the following equation which calculates the required SNR for a signal [17].

$$SNR = \frac{P_S}{P_N} = \frac{E_b \log_2 M}{N_0} \frac{f_S}{W} \tag{2.3}$$

Here, P_S is the power of the signal which is given by the energy per bit (E_b) multiplied by the number of bits ($\log_2 M$) – where M is the number of symbols – and the symbol rate (f_S). P_N is the noise power which is given by the noise spectral density (N_0) multiplied by the bandwidth of the receiver (W). Most of these parameters can be determined directly from the system requirements; however, the term E_b/N_0 is extracted based on the modulation scheme being used and the desired BER. Since BER is based on statistics, it is best to obtain this parameter from a simulation or graph. Figure 2.9 graphs the simulated BER versus the E_b/N_0 of QPSK, 16-, 32- and 64-QAM signals.

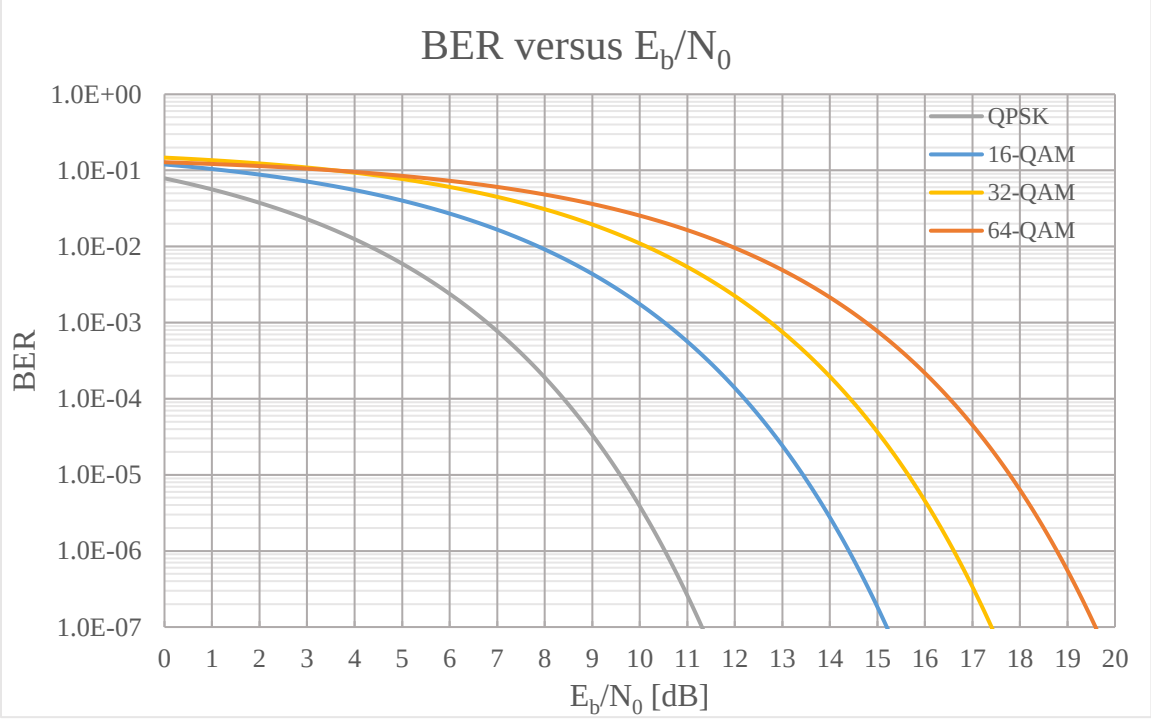

Figure 2.9: BER versus E_b/N_0 for QPSK, 16-, 32- and 64-QAM signals

2.2.6 Error Vector Magnitude

Error vector magnitude (EVM) is a measurement of the signal-to-noise and distortion ratio (SNDR) of a radio system. The measurement includes all sources of distortion in a system and provides an alternative way to measure the BER of the system. The required EVM for a system is derived by the following equation, using the SNR requirements for a given modulation and BER:

$$EVM = 10^{-SNR/20} * 100 \tag{2.4}$$

where SNR is the result from (2.3) and EVM is given in percentage [17]. Unlike BER, EVM is easier to simulate or measure because it is simply $X_{QPSK}(t) = \alpha_1 A_C \cos \omega_C t + \alpha_2 A_C \sin \omega_C t$

(2.1the average error magnitude between the received symbol and its ideal constellation point divided by the average power of the ideal constellation. EVM is illustrated by Figure 2.10 and calculated using the following equation [17]:

$$EVM = \sqrt{\frac{1}{N}\sum_{i=1}^{i=N}\left(\left|\frac{e_i}{a_i}\right|\right)^2} \tag{2.5}$$

where e_i is the error vector of between the received symbol and the ideal symbol, a_i is ideal vector of the symbol, and N is the total number of symbols in the constellation. Another advantage of EVM is that the effects of all the sources of error in a system – noise, phase noise, non-linearity

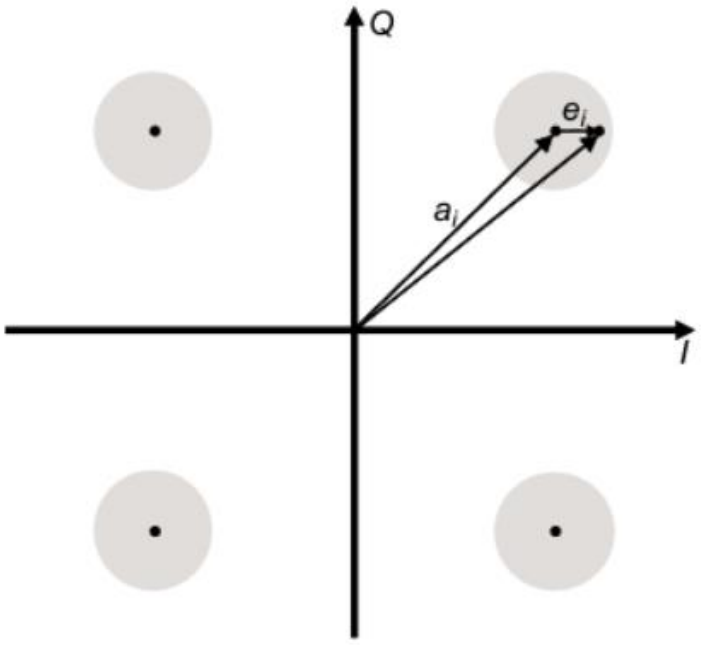

Figure 2.10: Illustration of EVM [17]

and IQ mismatch – can be quantified as is done in Chapter 5 of [17]. Each of the EVM sources in the system can be added using the equation below [17].

$$EVM_{total} = \sqrt{EVM_1^2 + EVM_2^2 + \cdots + EVM_n^2} \tag{2.6}$$

2.3 Budget Analysis

Budget analysis is the method used to break down the overall system specifications of gain, noise figure and linearity into individual block specifications. To perform this critical step in radio system design, one must understand the trade-offs between these three parameters and balance them in such a way that the system achieves the desired performance while making sure each block specification is practical. In the following sections, cascade noise figure, cascade linearity and cascade gain will be discussed.

2.3.1 Cascade Gain

The addition of the gain (in dB) for each block of the system is called cascade gain, and it is the simplest to calculate out of the three parameters mentioned. The overall gain required by a receiver can be determined by taking the difference between the signal power needed by the ADC and the expected signal power at the input of the receiver. For a transmitter, gain is determined by taking the difference between the required transmit power and the signal power supplied by the DAC. From this overall gain specification, the gain can be allocated to each individual block using the following equation:

$$G = G_1 + G_2 + G_3 + \cdots + G_m \tag{2.7}$$

G in this case is in dB, but the equation can easily be written using linear gain by changing the operation to multiplication. While the cascade gain is simple to calculate, allocating the gain may not be as easy because the cascade noise figure and cascade linearity depend on gain, which will be explained in the following sections.

2.3.2 Cascade Noise Figure

Noise figure (NF) is the measure of the degradation of SNR in a noisy circuit. Noise figure can be specified for an entire system or a single block in the system. In both cases, they measure the degradation of SNR in a noisy circuit; however, the system specification for NF is a non-linear

composition of each block NF known as cascade noise figure. The equation for determining the cascade noise figure is given in terms of the noise factor (F) – F is linear where NF is in dB – and is described by the following equation:

$$F = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_2} + \cdots + \frac{(F_m - 1)}{G_1 G_2 G_3 \ldots G_{m-1}} \tag{2.8}$$

where $F_1 - F_m$ and $G_1 - G_{m-1}$ are the individual block noise factors and linear gain, respectively [16]. The cascade noise figure is $10 \log_{10} F$. From this equation, a few conclusions regarding the cascade noise figure can be drawn. First, the cascade NF is always greater than 0 dB, meaning the input referred noise floor will be higher than the thermal noise floor. Second, the larger the gain of earlier blocks in the system, the lower of an effect the NF of later blocks have on the noise of the system. And third, the NF and gain of the first blocks of the system significantly affect the cascade NF of the system, which is why large emphasis is put on low noise amplifiers (LNA) in receiver design. The strategy is to provide low NF and large gain at the front end of the receiver to minimize the cascade NF.

2.3.3 Cascade Linearity

Unlike the cascade noise figure, the cascade linearity has major effects in both the transmitter and receiver. The cascade linearity represents the overall linearity of the system chain, and it is the limiting factor on the maximum transmit and receive signal power. The cascade linearity for the input referred 3rd intercept point (IIP3) is given by (2.7), but it can be defined for the 1 dB compression point (P1dB), the second order intercept point (IP2) or other orders of intercept points. Additionally, this can be done for input or output referred linearity as long as the parameters remain consistent [17].

$$\frac{1}{IIP3} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \cdots + \frac{G_1 G_2 G_3 \ldots G_{m-1}}{IIP3_m} \tag{2.9}$$

Again, all variables are in linear units with $IIP3_1 - IIP3_m$ and $G_1 - G_{m-1}$ representing the input referred 3rd order intercept point and gain of each block, respectively. The equation shows that the first blocks in the chain have little effect on the overall linearity of the system. Instead, the last blocks of the chain, in both receiver and transmitter, determine the linearity as these blocks experience the largest signal powers.

Large DAC outputs make the transmitter insensitive to noise, so linearity and gain are the largest concerns. The general strategy for balancing gain and linearity in the transmitter is to have little gain in the baseband and save as much gain in the budget for the later blocks. Balancing the budget in receivers is more challenging, however, because of the receiver's noise sensitivity. The receiver is required to have low noise figure and reasonably high gain in the first blocks of the system, but this could put a strain on linearity in the baseband.

2.4 Radio Over Fiber System

The idea of the radio over fiber (ROF) system is to modulate light waves using the RF analog signal transmitted by the radio system for transmission through a fiber optic channel. This type of channel is an attractive alternative to the traditional coaxial channel in downhole communications due to the distances involved. Compared to an RF signal in a coax channel, an optical signal in fiber optic experiences significantly less loss, and this reduces the transmit power requirement of the downhole transmitter and increases the allowable operating temperature of the power amplifier.

Figure 2.11 illustrates the block diagram of a ROF system. The signal chain begins with the baseband signal of the radio transmitter which is then upconverted to RF frequencies. After upconversion, the modulated RF signal is applied to an optical carrier via the radio to optical modulator, and it is transmitted over the optical link. Next, an optical to radio modulator recovers the original RF signal from the optical signal, and then, the recovered signal is processed by a radio receiver.

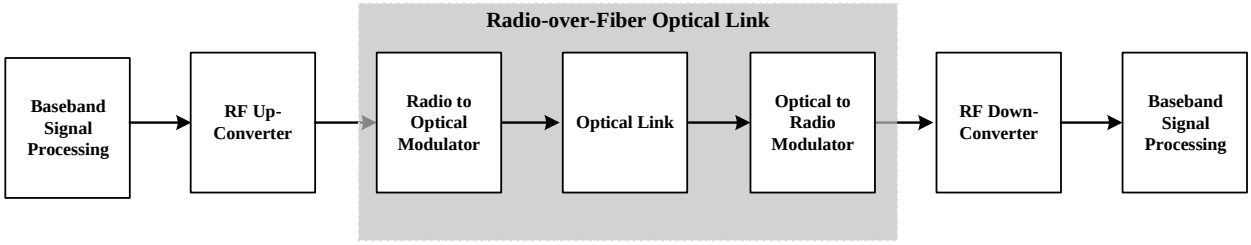

Figure 2.11: Block diagram of a typical radio over fiber system

The radio to optical modulation can be accomplished directly or externally. In a directly modulated laser link, the current of the RF signal is used to modulate the intensity of the laser source. The problem with this method is that the laser source will be in a high temperature environment, requiring the laser to operate reliably for a wide range of temperatures. An externally modulated RoF link using Mach-Zehnder modulators (MZMs) or electro-absorption modulators (EAMs) allows the optical source to remain at the surface; thus, the laser source is independent of temperature. In this type of modulation, the intensity of the light wave is varied by the RF waveform's voltage. At the receiving optical to radio modulator, a photodiode can be used to convert the intensity of the waveform to a photocurrent, which recovers the RF signal. It should be noted that, since the conversions taking place are from amplitude to power and vice versa, any loss incurred in the optical link is squared for the RF signal. For example, a 3 dB loss due to the optical fiber will cause a 6 dB RF loss [20].

2.4.1 RoF System Characterization

The RoF link can be considered as a subsystem in a larger RF system using typical system parameters such as input and output impedance, noise figure, linearity and gain parameters, as shown in Figure 2.12 [20].

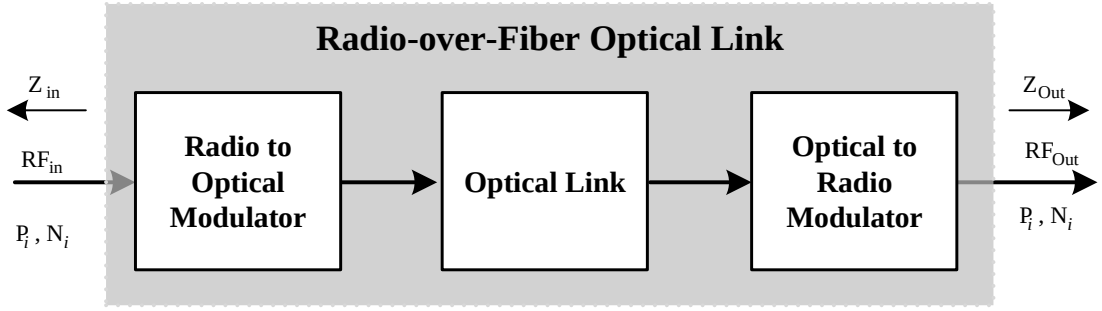

Figure 2.12: A radio over fiber link as a subsystem of a larger system [20]

The gain for an externally modulated MZM link is given by [21]:

$$G_e = \left(\frac{P_{opt}\eta_M\Re}{L_{opt}L_M}\right)^2 \frac{Z_{in}}{Z_{out}} \tag{2.10}$$

where P_{opt} is the input optical power to the modulator, L_{opt} is the loss of the optical link, η_M is the slope efficiency of the modulator at the operating point (V-1), L_M is the modulator optical insertion

loss, $\Re$ is the photodiode responsivity (A/W), and Z_{in} and Z_{out} are the input and the output impedances as shown in Figure 2.12. The slope efficiency for an MZM is given by [21]:

$$\eta_M = \frac{\pi \cos\phi}{2V_\pi} \tag{2.11}$$

where V_π is the modulator half-wave or switching voltage and ϕ represents the modulator bias point relative to the quadrature bias. Equation (2.10) shows that the link gain can be increased with higher input optical power, which will depend on the optical fiber cable characteristics and length for the downhole system since the optical source will be located remotely at the surface.

The noise figure of the RoF link can by expressed in decibels as follows [22]:

$$NF = 10\log\frac{N_o}{N_i G_e} \tag{2.12}$$

where N_o is the output noise power and N_i is the input noise power, which is typically given by $N_i = K\times T\times B$, where K is Boltzmann's constant, T is ambient temperature, and B is the noise bandwidth. G_e, in this case, is the link gain for an external modulated system, meaning the noise of the link can be reduced by increasing the optical source power. The laser relative intensity noise, thermal noise and photodiode shot noise can also have an impact in the link noise performance. Furthermore, even though the frequency of the RF signal is not explicitly shown in the above-mentioned equations does not mean the RoF link is independent of it. Laser and modulator slope efficiencies, photodiode responsivity and impedance matching all may vary over signal bandwidth. The effective fiber loss will also have some dependencies to the RF frequency due to fiber dispersion [20].

Nonlinearities in the RoF link can be expected just as in any RF system. These effects can be represented using the standard parameters used in RF budget analysis such as P1dB, IP2 and IP3 [23].

2.5 High Temperature Components

For the purpose of guiding future work, the following sections identify components and materials that may be used to implement the system design presented in this thesis work. The components listed in the following discusssion are not exhaustively inclusive.

2.5.1 Active Components

Gallium nitride (GaN), silicon carbide (SiC) and silicon-on-insulator (SOI) CMOS are well suited for high temperature applications [1, 2, 24, 25]. GaN and SiC technologies are capable of operation in excesses of 250℃ because of their wideband gap energy. SOI CMOS can perform reliably at 250℃, but standard bulk silicon CMOS cannot, because the structure of SOI CMOS eliminates the possibility of latch-up events and significatly reduces leakage [26, 27]. Additionally, deep N-well (DNW) CMOS has been shown to perform well at high temperature and out perform partially depleted SOI CMOS [28]. Both SOI and DNW CMOS are compatible with modern bulk Si CMOS processes, which makes these technologies extremely attractive for a fully integrated high temperature RFIC solution.

Commercial off-the-shelf (COTS) discrete GaN transistors are available from Qorvo and Cree [29, 30]. While these devices are tailored to high-power RF solutions, they can also be utilized for high temperature applications due to their maximum junction temperature ratings. Transistors from Qorvo, such as [31-33], can operate with junction temperatures up to 275℃. Offerings from Cree, like [34], are rated up to junction temperatures of 225℃, but have been shown to be capable of operating at temperatures up to 250℃ [35]. These capabilities make transistors from these companies well suited to implement the RF front-ends of high temperature radio systems.

The components offered by X-REL, Texas Instruments, and Analog Devices are excellent candidates to implement the baseband of high-temperature radio systems. X-REL offers a wide variety of SOI and SiC devices that operate up to 230° such as NMOS and PMOS discrete transistors, regulators, timers and oscillators [36]. Texas Instruments and Analog Devices also offer a high temperature portfolio of devices like op-amps and ADCs that can operate up to 210℃ [37, 38].

2.5.2 Passive Components

Without passive components – resistors, capacitors, inductors and transmission lines – that operate at high temperatures, the aforementioned active devices are useless for high temperature applications. Devices used for this application must be insensitive or independent of temperature, otherwise, the circuits' performances may vary widely with temperature.

Thin film and thick film resistors offer immense temperature stability and are commercially available in SMD form factors and a variety of values [2]. Vishay offers a family of automotive precision thin film resistors that operate up to 250℃ [39]. This family of resistors have a range of temperature coefficient of resistance from $\pm 25\ ppm/℃\ to\ \pm 100\ ppm/℃$. With a low variability versus temperature, these resistors can be used in the signal path for stabilization and feedback in both the RF and baseband sections of the system.

The type of dielectric material used to form capacitors is the largest factor of temperature dependence for these passive devices. Ceramic capacitors using X7R and C0G/NP0 dielectric are capable of operating at temperatures above 200℃; however, X7R capacitors suffer from approximately 50% of its capacitance at 200℃, where C0G/NP0 capacitors do not [40]. The C0G/NP0 capacitors can be used for signal processing, but X7R capacitors cannot be used for high temperature except potentially as bypass capacitors. Presidio and Murata offer a line of C0G/NP0 capacitors that operate up to 250℃ in SMD form factors in a wide variety of values [41, 42].

Inductors play critical rolls in RF circuits as chokes and as elements in filter designs. Again, like capacitors, inductors used in the signal path must be insensitive or independent of temperature such that the performance of the circuit is not negatively affected. Low temperature co-fired ceramic (LTCC) ferrites are a modern development in high temperature inductors [2], and NASCENTechnology offers a variety of LTCC inductors that operate up to 300℃ [43]. Furthermore, Coilcraft offers aircoil inductors that operate at 240℃ and a cored inductor capable of 300℃ [44, 45]. Unfortunately, the datasheets show these inductors are ill-suited to operate at 2.4 GHz, so RF chokes and filter design of the RF sections of this radio system should be implemented using transmission lines or planar inductors. As long as the PCB material properties remain relatively unchanged over the temperature range, the transmission line and planar inductor performance variation over temperature will be negligable [11].

2.5.3 RoF Components

The important components to the RoF system are the optical fiber, the optical source, the optical modulator and the photodetector. Optical fiber specifically designed for downhole applications up to 300℃ are commercially offered by Aflglobal [46]. The optical source is highly sensitive to temperature, but in an externally modulated system, the optical source can be a COTS device as it is located in a controlled environment at the surface. In terms of optical modulators, a

Mach-Zehnder reported by [47] has achieved $0.070\ nm/℃$ temperature sensitivity at 25℃ to 400℃. Photodiodes currently available for high temperature only reach temperatures of 225℃ [48]; however, there have been investigations into GaN based photodiodes, which could have the potential to reach even higher temperatures [49, 50].

2.5.4 Interface Materials

The PCB material chosen for the circuit design is important if any part of the system utilizes microstrip transmission lines or planar inductors. For either to be immune to temperature changes, the substrate should have a temperature stable dielectric constant and a low coefficient of thermal expansion so the characteristic impedence and the dimensions of the microstrip line remain unchanged and the quality of the inductor remains constant. Rogers 3003 and 4003C laminates are useable up to 250℃ offering termperature stable dielectric constants and low thermal expansion [51, 52]. Solder materials chosen for this application must ensure a metling point greater than 250℃ — there are many suitable solders commercially available as a wire or paste that would be appropriate.

2.6 Chapter Summary

This chapter discussed important concepts and background information in regards to radio system design. Advantages and disadvantages of superheterodyne and direct conversion radio architectures were presented followed by an overview of QPSK and QAM modulation schemes and other topics pertaining to modulation. Budget analysis was broken down to understand constraints on different circuit parameters used in system design and how they relate to the overall requirements. Next, the RoF system was explained in the context of this work. Finally, high temperature components that could be useful for high temperature circuit design were identified.

Chapter 3

Proposed System Design

In this chapter, the high temperature radio system design and specifications will be presented. First, the overall system architecture is explained. Next, different aspects of the overall system are highlighted such as the frequency plan, the coaxial channel and the RoF Link. Finally, the downhole RF transceiver design is proposed. The design philosophy for both receiver and transmitter will be discussed followed by the design specifications and guidance for IC implementation.

3.1 System Architecture

The proposed system architecture for high temperature downhole communications, illustrated by Figure 3.1, is composed of a surface radio system and a downhole radio system connected by a RoF link. The surface system is located above ground in a controlled environment and encompasses the surface radio transceiver to facilitate communications with the downhole system and an optical source and modulator for the RoF link. Because this system is located in a

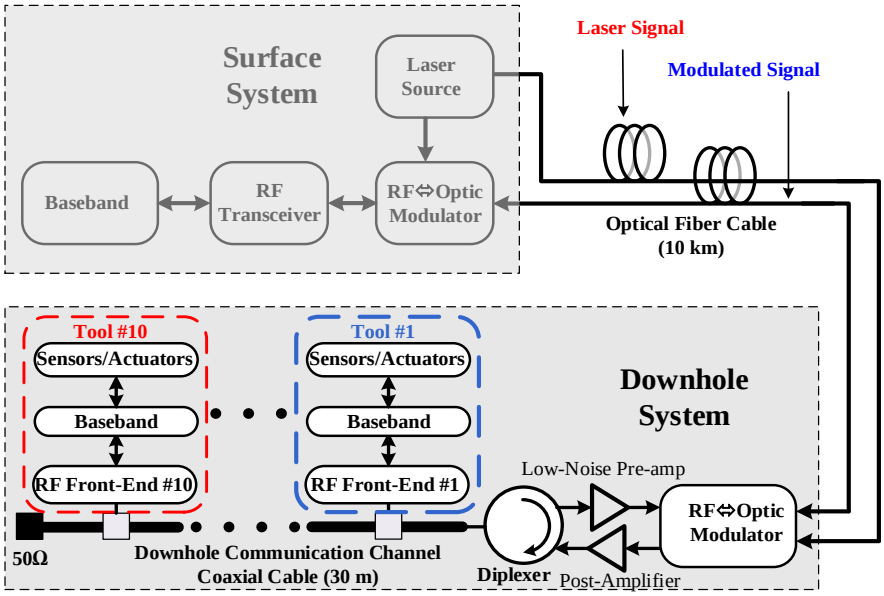

Figure 3.1: Proposed system architecture

controlled environment, it can be implemented using commercially available components. The downhole system is made up of ten tools, each interfaced with its own transceiver, operating in parallel along a single coaxial cable. This coaxial channel supports two-way communication and interfaces with the optical link through a diplexer which descriminates between downlink (surface to downhole) and uplink (downhole to surface) traffic. This system can be located anywhere from 5 km to 15 km underground. Every component of the downhole system must be designed to tolerate up to 250℃ without the use heat sinks.

3.2 RoF Link

The block diagram of the RoF link for the downhole telemetry system design is illustrated by Figure 3.2. The RoF link considered for this application is an externally modulated system to allow the laser source to reside at the surface system. The optical source feeds two optical-electrical converters (OEC) for converting electrical RF signals to an optical signal on the trasnmitting side for both uplink and downlink signals. These signals are then received at the opposite side of the optical link by a photodiode to recover the RF signal. A post-amplifier and pre-amplifier at the downhole end of the link serves to reduce the affect of the noise figure of the RoF link and the coaxial channel. The diplexer interfaces the coaxial channel to the RoF link and separates the uplink and downlink signals.

Because this work mainly focuses on the design of the downhole transceiver system, the RoF link design parameters are modeled after an example design in Chapter 5 of [20]. The design assumes a directly modulated laser link with a fiber length of 10 km. The design considers typical devices of the OEC modulated laser and photodiode. The gain of the link, which includes both OECs and the loss of the fiber optic channel, is calculated to be -34 dB with a cascade NF of 45

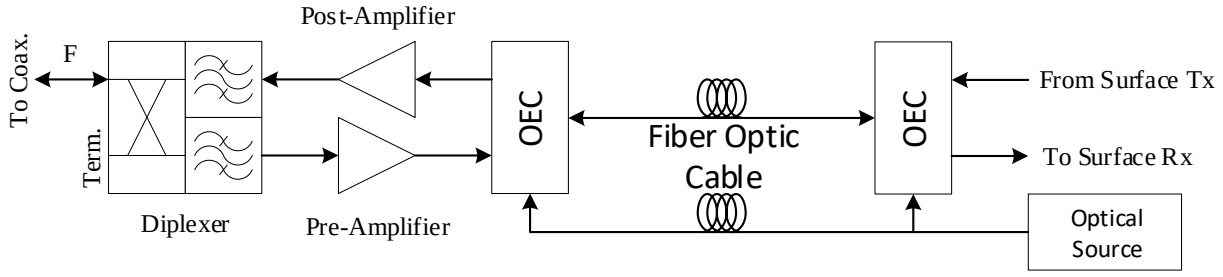

Figure 3.2: RoF Link block diagram

dB. Additionally, the IP1dB of the link is determined to be 16 dBm. These values are considered for both directions through the link. Lastly, it should be noted that the externally modulated RoF link considered for the downhole system could improve the gain of the link and support a longer cable compared to the directly modulated link.

The gain and linearity of the post- and pre-amplifiers are based on the RoF link linearity and the maximum composite signal power from the downhole transmitters. They are specified as having output linearity equal to that of the OECs so that they do not limit the linearity of the link. The diplexer will be considered to have an insertion loss of 6 dB at any port.

3.3 Downhole Coaxial Channel

The downhole coaxial communication channel interfaces each of the ten transceiver systems spaced out along the channel to the RoF link and facilitates uplink and downlink communication. The coaxial channel has a characteristic impedance of 50 Ω and has a total length of 30 m. It is broken up into 3 m segments and repeated for each transceiver. Each segment utilizes a branchline coupler to integrate the transceiver into the communication channel. A segment of the coaxial channel is illustrated in Figure 3.3. The coaxial segment is repeated each time with the next segment continuing from port two of the coupler. Port 3 of the coupler feeds to the transceiver, while port 4 is terminated into a 50 Ω. Additionally, port 2 of the final segment is terminated in a 50 Ω load. In the downlink direction, the modulated signal originates at the beginning of the

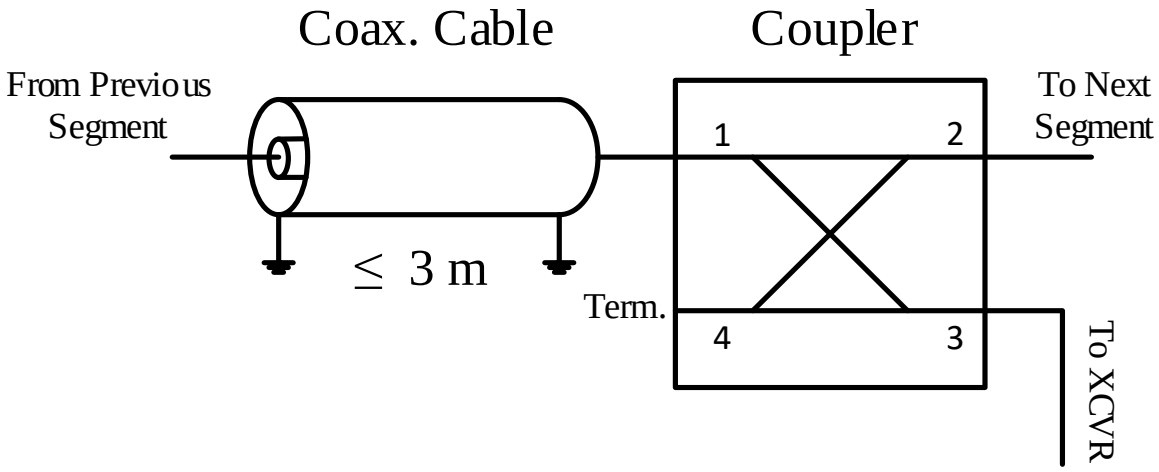

Figure 3.3: Single segment of downhole coaxial channel

coaxial cable and feeds into port 1. Due to the nature of the branchline coupler, the signal is coupled to port 3, feeding into the transceiver, and port 2, allowing the signal to continuing through the coaxial channel to the next transceiver. Port 4, on the other hand, is isolated from signals originating at port 1. For the uplink direction, the modulated signals originate from the transceiver and enter the communication channel through port 3 of the coupler. In this direction, the signal is coupled to port 1 and port 4. Port 1 allows the signal to continue up the coaxial channel, while port 4 terminates the signal. Signals continuing through the coaxial channel in the uplink direction eventualy enter a coupler through port 2, which is also coupled to ports 1 and 4.

In the design of the coaxial channel, it is important to minimize the attentuation of the channel. Since the NF of passive components is the same as their attentuation, minimizing loss in the channel improves the overall signal to noise ratio of the link. Additionally, the dynamic range requirements of the receivers – both surface and downhole – depends on channel attenuation between tool #1 and tool #10. By reducing the attentuation, dynamic range requirements are reduced. The coaxial cable modeled for this design, M17/112-RG393, has a characteristic impedance of 50 Ω, allows for operation up to 250°C and provides low attenuation at 2.4 GHz [53]. With an equal power split (-3 dB) from the coupler, the modeled coaxial channel exhibits 42.4 dB of attenuation between tool #1 and tool #10 at 2.45 GHz. While a dynamic range of 42.4 dB is acheivable, this can be further relaxed by using unequal splits in the power divider. The channel attenuation can be optimized by utilizing unique splits for each segment; however, the same coupler design is used instead to reduce design requirements. An unequal split of -1 dB from P1 to P2 and -7 dB from P1 to P3 was found to provide adequate attenuation performance between the tools while maintaining a design that is easily implemented. Figure 3.4 graphs the simulated attenuation of the coaxial channel between 2 GHz and 3 GHz. This graph shows the attenuation at the beginning of the channel to the output of the coupler for each tool. The attenuation between tool #1 and #10 is reduced to 24.3 dB at 2.45 GHz and is calculated by simply taking the difference between the attenuation shown for these tools. Note, this calculation is to determine how much more attenuation signals experience between tools #1 and #10 and is not indicative of the measured attenuation between the ports for these two tools due to the isolation provided by the couplers.

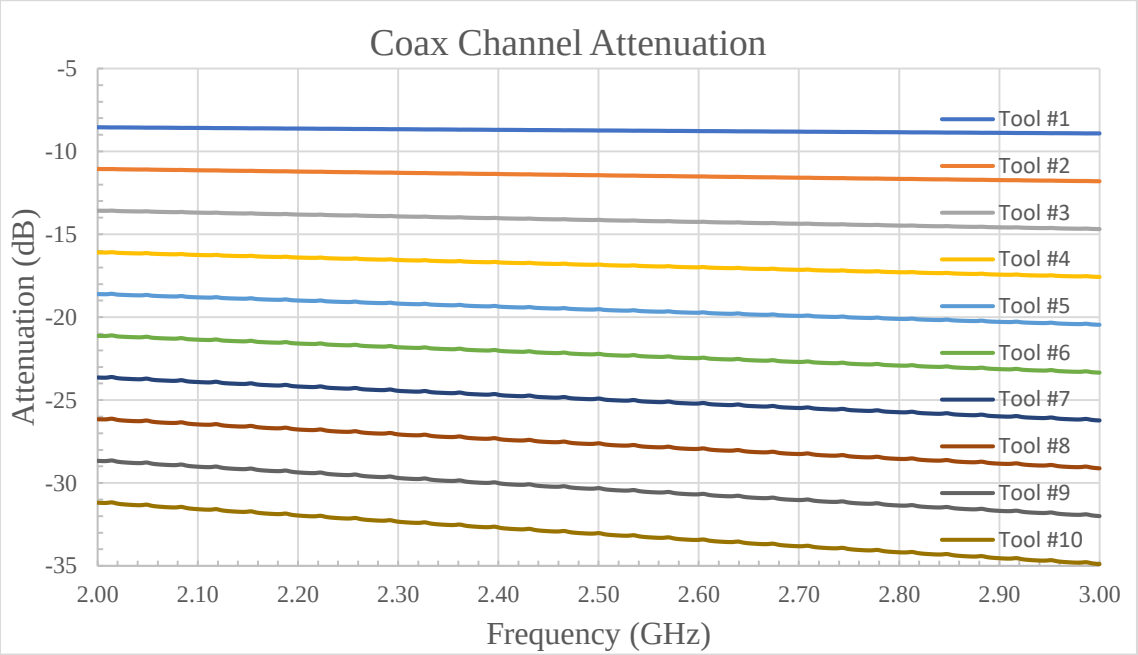

Figure 3.4: Coaxial channel attenuation

3.4 Proposed RF Transceiver

The proposed downhole RF transceiver is shown in Figure 3.5 and represents the RF front end and baseband blocks shown in the proposed system architecture diagram in Figure 3.1. The transceiver design consists of a direct conversion receiver and a direct conversion transmitter separated by a diplexer, which connects the transceiver to the coaxial channel. The diplexer directs the uplink and downlink signals to the proper destination based on the signal frequency and direction. This allows the transceiver to support FDMA. To avoid saturating the receiver, the diplexer also provides isolation between the transmit and receive paths. Both receiver and transmitter consists of a RF front end operating in the 2.4 – 2.5 GHz frequency band and a baseband section operating at DC.

The transceiver is designed to support QPSK, 16-QAM, 32-QAM, and 64-QAM modulation schemes with at most 10^{-6} BER. Table 3.1 lists the requirements that the transmitter and receiver need to meet for each modulation scheme. The values shown for E_b/N_0 are extracted from Figure 2.9 for a BER of 10^{-6}. With these values, SNR and EVM are calculated using

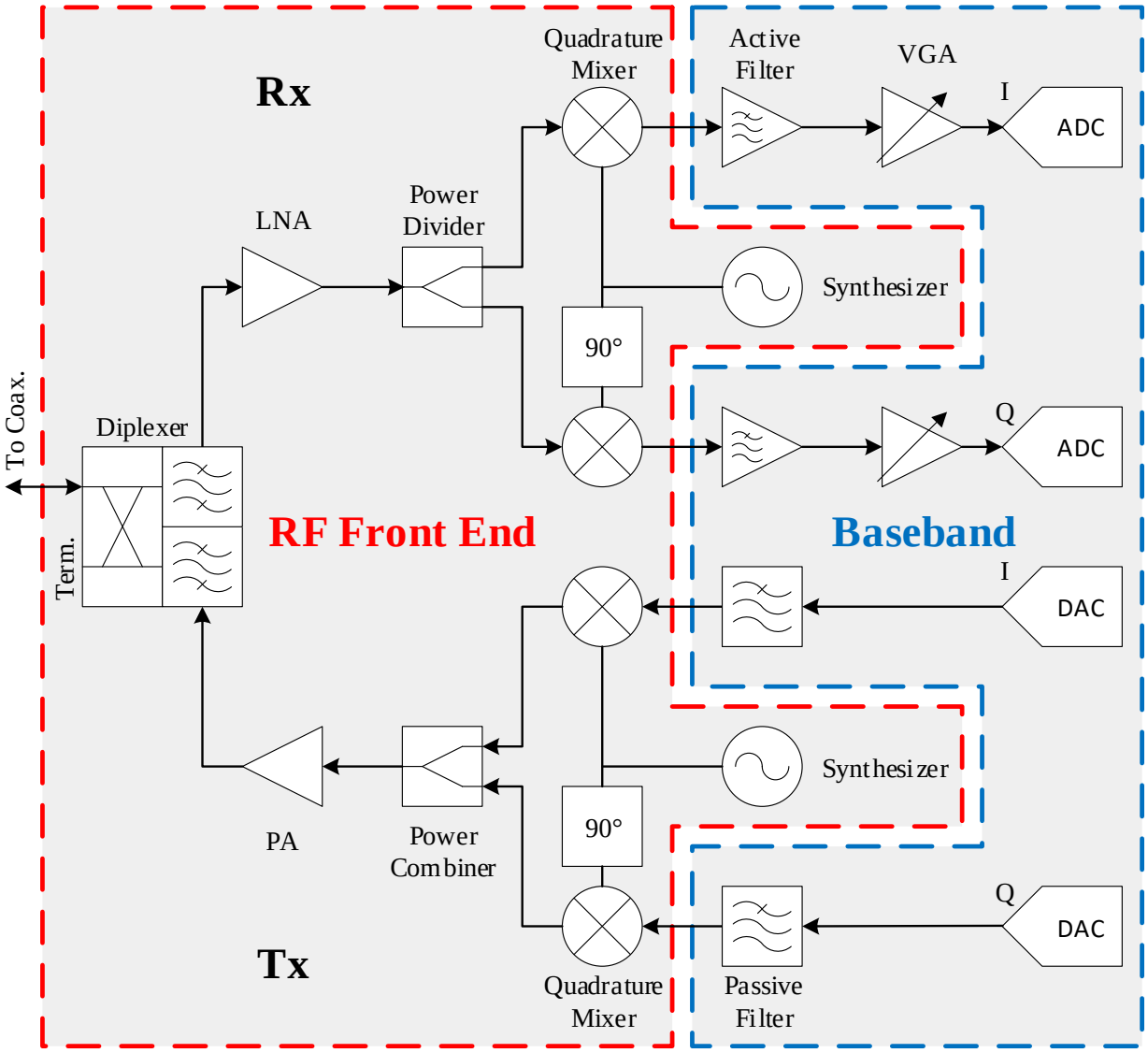

Figure 3.5: Proposed downhole transceiver design

Equations (2.3) and (2.4) assuming the signal bandwidth utilizes the entire channel bandwidth. In practice, the ratio between the signal bandwidth and the channel bandwidth will be less than one due to distortion experienced at the edges of filters, and the values for SNR and EVM will improve as the ratio is reduced. The bit rates shown in the table represent the maximum possible bit rates for each modulation in this system but will reduce as with signal bandwidth. The fact that higher orders of modulation increase the bit rates but requires better SNR performance represents the major trade off in a finite bandwidth system. Lastly, the table lists the peak-to-average power ratios (PAPR) for each modulation scheme. This parameter is important when considering linearity requirements.

Table 3.1: Modulation Requirements for 10^{-6} BER

M-QAM	Eb/N0	SNR	EVM	Bit Rate	PAPR
QPSK	$\geq$ 10.53 dB	$\geq$ 13.53 dB	$\leq$ 21.06 %	$\leq$ 7.0 Mbps	$\approx$ 4.0 dB
16	$\geq$ 14.40 dB	$\geq$ 20.42 dB	$\leq$ 9.52 %	$\leq$ 14.0 Mbps	$\approx$ 6.3 dB
32	$\geq$ 16.61 dB	$\geq$ 23.60 dB	$\leq$ 6.60 %	$\leq$ 17.5 Mbps	$\approx$ 6.0 dB
64	$\geq$ 18.78 dB	$\geq$ 26.56 dB	$\leq$ 4.69 %	$\leq$ 21 Mbps	$\approx$ 7.3 dB

The downlink for the system does not require large data rates; thus, the receiver is designed to use the QPSK modulation exclusively. This allows the receiver design to have large margins for noise and linearity and to be robust against performance changes with temperature. The uplink, on the other hand, requires much larger data rates to accommodate more sensors, higher resolutions, and quicker logging speeds. To achieve this, the transmitter is designed to utilize 16-, 32-, and 64-QAM. Despite the higher SNR requirements for these modulation schemes, the transmitter deals with much larger SNR margins due to larger signal powers and only needs to be designed against signal distortions such as IQ mismatch, LO leakage, and linearity.

The proposed transceiver design is intended to be implemented initially using discrete COTS components on PCB to validate the system design. In this implementation, the RF front end should be designed using GaN-SiC device – or SOI if suitable COTS components can be found. These technology has been proven to operate at RF frequencies and 250℃. The baseband should be designed using either SiC or SOI technologies since these technologies have also been shown to operate up to the required temperatures, but commercially available components are more suited to low frequencies. Once validated, the system design can easily be modified for an RFIC or MMIC implementation using partially depleted SOI, fully depleted SOI, or GaN-SiC processes. Suggestions for how to modify the receiver and transmitter designs are discussed in sections 3.6 and 3.7, respectively.

3.5 Frequency Planning

Frequency planning is a major aspect in radio system design. The plan must consider how to best allocate the bandwidth based on factors such as the radio architecture, the IF frequency, modulation scheme and the data rate. Since the proposed transceiver uses the direct conversion

architecture, the frequency plan in this case does not need to consider image frequencies or IF frequencies. Additionally, the LO frequencies for this architecture are selected based on the center frequency of each channel. The proposed system uses the 2.4 – 2.5 GHz ISM band based on the available bandwidth and the magnitude of the frequency. The larger bandwidth allows for more tools and higher data rates while the magnitude of the frequency enables for smaller circuits and IC implementation. The ISM band also has the added benefit that no FCC license is required to operate equipment with these frequencies. The downside to using this frequency band, however, is that component parasitics begin to have significant effects in circuit performance and higher quality and order filter designs are needed.

The proposed frequency plan is illustrated by Figures 3.6 and 3.7, which show the uplink and downlink bands, respectively. The plan supports FDMA consisting of two 44 MHz bandwidths each containing ten channels for uplink and downlink communications. Since the uplink band requires more SNR to support higher data rates, the uplink band is allocated to the lower frequencies to reduce the loss experienced through the coaxial channel. A 12 MHz guard band separates the uplink and downlink bands to allow filters to adequately select between bands. This guard band represents approximately 25% of the 44 MHz bandwidths, a typical value used to determine the bandwidth necessary for the guard bands [17]. Although the uplink band targets a higher data rate than the downlink, both bandwidths are designed to have equal widths to simplify filter design. Shrinking the downlink bandwidth to support higher data rates for the uplink would require pre-selection filter designs with a higher quality factor, making these filters more difficult to design.

Both the uplink and downlink bands are further divided into ten channels for each tool. Each channel is allocated a 3.5 MHz bandwidth separated by 0.9 MHz guard bands. Again, the guard bands represent approximately 25% of the channel bandwidths. The channels are situated in the center of the uplink/downlink bands with a 0.45 MHz buffer from the edges of the overall bandwidth. This helps to reduce signal distortion caused by the group delay experienced at the edges of filters. As seen in Figures 3.6 and 3.7, each tool is designated a specific channel based on the same reasoning that the uplink and downlink bands were allocated their frequencies. Tool #10 is located at the end of the coaxial channel, experiencing the most loss. Therefore, tool #10 is

allocated the channels with the lowest frequencies while tool #1 is allocated the channels with the highest frequencies.

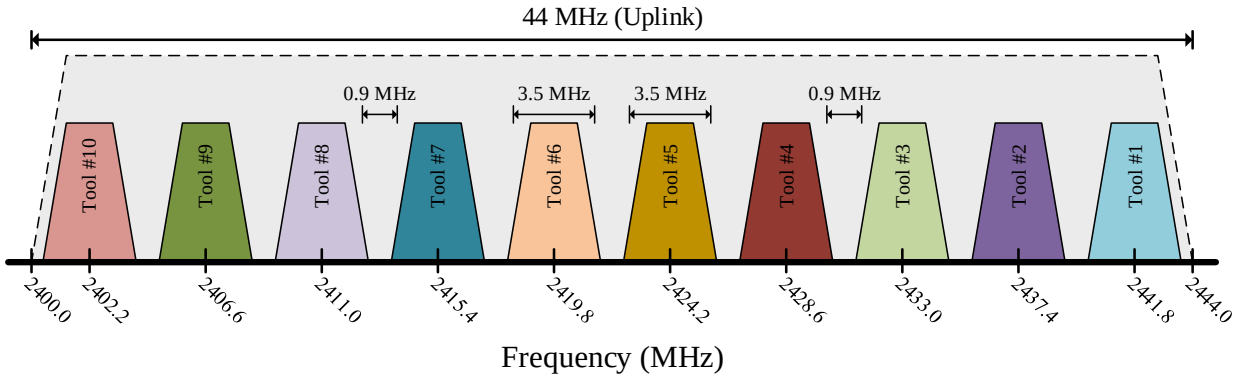

Figure 3.6: Proposed uplink frequency plan

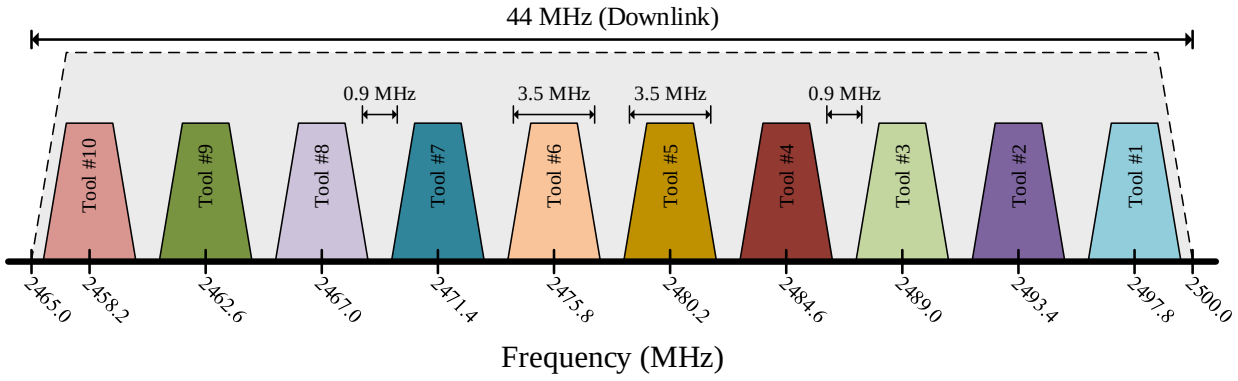

Figure 3.7: Proposed downlink frequency plan

3.6 Receiver Design

The receiver block diagram of the downhole transceiver is shown in Figures 3.8. The block diagram shown represents the direct conversion architecture used by the receiver where the quadrature mixer and baseband IQ channels are condensed into a single path. This representation is particularly useful for simulations and budget analysis as the signal conditioning and block specifications for the I & Q channels will be exactly the same. The only difference between the two paths is a phase shift of 90°.

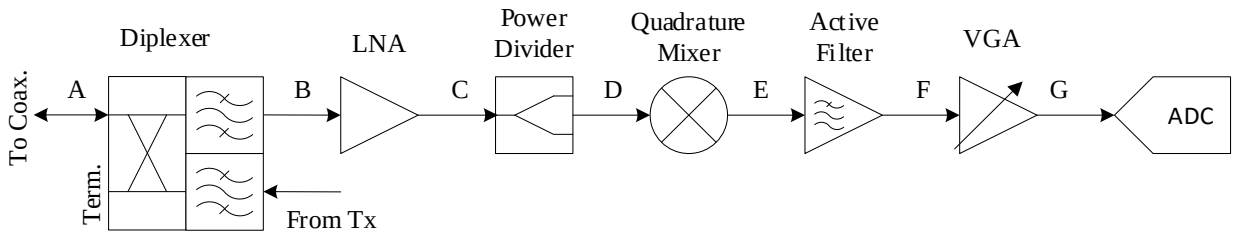

Figure 3.8: Receiver block diagram

This receiver is designed to condition and demodulate QPSK signals with a BER of 10^{-6}. The diplexer passes signals originating from the coaxial cable within a bandwidth ranging from 2456.0 – 2500.0 MHz to the LNA. The LNA amplifies the signal power with little reduction to the SNR while also reducing the impact of subsequent blocks on the receiver noise. From here, the signal power is equally split between the I & Q channels using a power divider. The power divider is necessary for discrete and MMIC designs, but can be neglected for an RFIC implementation. Next, the quadrature mixer downconverts the desired channel to baseband where the active filter provides further amplification while removing unwanted spectral content that make up the other downlink channels. Lastly, the VGA provides the final amplification so that the signal is at an appropriate level for the ADC. The VGA is also used to adjust for large IQ amplitude mismatches, while DSP is used to adjust for IQ phase mismatch and minor IQ amplitude mismatch.

3.6.1 Overall Receiver Specification

To design the receiver, the overall receiver design specifications must be determined. The design process begins with the sensitivity of the receiver and the SNR requirements of the QPSK modulation. The equation for sensitivity is given by:

$$Sensitivity = 10\log_{10}(kTB) + SNR + NF \tag{3.1}$$

where k is Boltzmann's constant (1.38×10^{-23}), T is the temperature in Kelvin, and B is the noise equivalent bandwidth given by the channel bandwidth [16]. The maximum SNR requirement for QPSK and BER of 10^{-6} can be found in Table 3.1. The NF in this equation represents the cascade NF of the receiver and will be chosen to be approximately 12 dB. For comparison, manufacturers typically target less than 10 dB cascade NF. Additionally, a safety margin of 6 dB will be added into the sensitivity calculation to provide buffer from typical design variations and the temperature variations that will be experienced in the downhole environment. Taking into

account the operating temperature of 250°C (523.15 K), the receiver sensitivity is calculated to be -74.0 dBm. This sensitivity calculation indicates the minimum signal power required at the input of the receiver for the information to be extracted with a BER of 10^{-6}.

Using a minimum signal power of -74.0 dBm, the next step is to determine the maximum signal power experienced by the receiver and the receiver dynamic range. To do this, the peak-to-average power ratio (PAPR) of the QPSK signal, the attentuation of the coaxial channel, and the relationship between all ten downlink signals' power must be considered. The PAPR of the QPSK signal, according to Table 3.1, is aproximately 4 dB. As graphed in Figures 3.4, the signals appearing at the input of the receiver diplexer will experience approximately 26 dB more attenuation from tool #1 to tool #10. This means the receiver must have a dynamic range of atleast 26 dB and the signal power at the input to tool #1 will be -44 dB including PAPR. However, this is still not the maximum power that will be experienced by the receiver. The diplexer passes the entire downlink band through to the receiver; thus, the RF front end will experience a larger composite signal power – that is the addition of all ten channel powers into a single signal – and must be designed to accommodate this power. Considering the scenario where each channel is transmitted from the surface at the same average power, the composite signal power is 10 dB greater than the average power of a single channel. Using the aditional composite signal power of 10 dB, the expected maximum signal power experienced at the input of the downhole receiver is -34 dBm.

In order to determine the receiver gain, the required output power of the receiver at node G needs to be specified to compare it with the input signal power at node A. Since the ADC is the final block of the system, it will be what determines the maximum required signal power of the receiver. According to [17], a signal power of +4 dBm (1 Vpp in a 50 Ω system) is a reasonable requirement for an ADC. After adding in in a safety margin to account for performance variations with frequency and temperature, +1 dBm will be used to specify the gain. Because this gain is for a signal which passes through the active channel select filter, the maximum and minimum single channel power at the input of the receiver (-74 dBm and -44 dBm, respectively) will be used to determine maximum and minimum gain. The gain of the receiver is determined by the difference between the required output signal power and the minimum and maximum input signal powers. This leads to a maximum gain of 75 dB and a minimum gain of 45 dB.

Finally, using the maximum signal power experienced by the receiver, the overall linearity requirements of the receiver can be determined. The linearity of a receiver is specified through the input 1 dB compression point (IP1dB), the input 3rd order intercept point (IIP3), and the input 2nd order intercept point (IIP2). There are several methods to specifying the required linearity of the receiver that take into account out-of-band blockers (i.e. large signals originating from the transmitter), in-band blockers (i.e. intermodulation products from adjacent channels), and the maximum signal power experienced by the receiver. Additionally, there will be two separate points in the receiver design at which linearity requirements will be specified. At point F in Figure 3.8, the input referred linearity requirements will specified based on the composite signal; while, at point G in the same figure, the linearity will be based on the single signal power as the other 9 channels have been filtered by the active filter. The linearity requirements due to large transmitter signals can mitigated through proper filtering and isolation from the uplink channels; thus, out-of-band blockers will not be the factor driving linearity requirements. In-band blockers, however, must be considered. The required IIP3 of the receiver at point F for in-band blockers is determined by the following equation:

$$IIP3 = P_i + \frac{1}{2}[P_1 - P_3] \tag{3.2}$$

where P_i is the input fundamental power, P_1 is the output fundamental power, and P_3 is the output power of the 3rd order intermodulation product (IM3) that interferes with the fundamental signal [17]. Furthermore, to determining the required IIP2 for the receiver, this time based on low-frequency 2nd order intermodulation products, the following equation is used:

$$IIP2 = P_i + [P_1 - P_2] \tag{3.3}$$

where P_i is the input fundamental power, P_1 is the output fundamental power, and P_2 is the output power of 2rd order intermodulation product (IM2) that falls within the baseband bandwidth of the receiver [17]. The values used for these calculations assume the worst case scenario where all ten channels contribute to the intermodulation products and experience the same gain as the fundamental signal – this is a similar scenario the receiver will face if the downlink channel powers are adjusted for the coaxial attenuation for each tool. The resulting minimum required IIP3 and IIP2 from these calculations are -47.2 dBm and -20.5 dBm, respectively. Based on these values, however, the intermodulation products for this design are not the driving factor for linearity.

Table 3.2: Summary of overall downhole receiver specifications

Specification		Comments
System Temperature	250°C	
System Impedance	50 Ω	
Noise Figure	≈ 12 dB	Manufacturers typically target 10 dB
Sensitivity	-74.0 dBm	At 250°C with 6.4 dB margin
Min individual signal power Min composite signal power	-74.0 dBm -64.0 dBm	Composite signal combines 10 channels of equal power; adds 10 dB
Dynamic Range	> 26 dB	Based on coaxial channel attenuation
Max individual signal power Max composite signal power	-44.0 dBm -34.0 dBm	Considering dynamic range and PAPR
IP1dB	> -38 dBm > -28 dBm	Specified at point G Specified at point F; max comp. signal
IIP3	> -28 dBm > -18 dBm	Specified at point G Specified at point F; max comp. signal
IIP2	> -18 dBm > -8 dBm	Specified at point G Specified at point F; max comp. signal
ADC Full-scale input	+4 dBm	1 Vpp in 50 Ω system
Max Overall Gain	75 dB	
Min Overall Gain	45 dB	

Instead, it is the maximum composite signal power that will drive linearity for this design. The minimum required IP1dB, IIP3, and IIP2 at point F and with a 6 dB margin are -28.0 dBm, -18.0 dBm, and -8.0 dBm, respectively. At point G, the P1dB, IIP3, and IIP2 are based on the maximum individual channel power with a 6 dB margin and at maximum gain. This gives a minimum P1dB of -38 dBm, IIP3 of -28 dBm, and IIP2 of -18 dBm. Table 3.2 summarizes all of the overall receiver specifications discussed in this section.

3.6.2 Block Specifications

The next step in designing the receiver is to allocate the overall receiver specifications shown in Table 3.2 into the individual block specifications for the diplexer, LNA, power divider, quadrature mixer, active filter, and VGA. The values in the table for gain, noise figure, and

linearity represent the cascade values of the receiver. Each block in the chain will be given specifications based on their role in the system and the effect the block has on the system.

Before continuing to break down the system specification, it is useful to review how gain, noise figure, and linearity effect one another in the receiver system. Recall that the cascade gain of a system is simply the cumulative of each blocks gain or loss, as given by (2.7). The cascade noise figure of the system is given by (2.8) and is heavily influenced by the noise figure of the first few blocks of the system and by the gain early in the receiver chain. Cascade linearity of the system, represented for IIP3 by (2.9), is limited by the final blocks in the receiver chain and is negatively impacted by gain early on in the system. The receiver design must find a balance the gain so that the impact of noise figure in later blocks is insignificant while maintaining the required cascade linearity. As a rule, the linearity specification of each block will be defined as atleast 6 dB greater than the maximum signal power experienced at each node in the system. For the blocks up to point F, the maximum composite signal power should be used. The maximum individual signal power can be used after point F.

To start, the diplexer will have the largest impact on the cascade noise figure of any other block in the system because it is the first block in the chain and it is a lossy network. This block consists of two elements: a coupler to provide direction and isolation between receive and transmit signals and a bandpass filter to select the downlink band. The noise figure of the diplexer will be equal to its insertion loss; thus, the insertion loss should be minimized. For this reason, the same coupler design used for the coaxial channel will be used for an insertion loss of -1 dB. The bandpass filter element will be allowed an insertion loss of -3 dB for a total diplexer insertion loss of -4 dB.

Next, the LNA should provide a low noise figure and a sizeable gain such that subsequent blocks in the receiver have insignificant impact to the cascade noise figure. Most LNA designs target a NF of 3 dB or less; however, to allow margin against temperature, this design will account for a NF of 5 dB. A gain of 15 dB is shown to adequately desensitize the cascade noise figure to the subsequent blocks and leave enough linearity headroom for to following blocks. The linearity for this LNA is specified at its output ports for OP1dB, OIP3, and OIP2 as -10 dBm, 0 dBm, and 10 dBm, respectively.

The power divider is necessary in the discrete implementation of this system due to the behavior of RF signals at this scale of design. The purpose of this block is to split the input power equally (3 dB) between the I and Q channels of the quadrature mixer and to maintain a 50 Ω impedance match at all ports. The design should be capable of operating at the center of the downlink band (2478.0 MHz) with minimal phase and amplitude mismatch between the output ports across the downlink bandwidth (2456.0 MHz – 2500.0 MHz). A Wilkinson divider is an excellent candidate to implement such a design [54]. The isolation between ports 2 and 3 is not critical to this design as the only signals entering the divider through these ports will be reflections due to any impedance mismatch.

The quadrature mixer for this receiver design is decided to be made up of two active mixers. Both mixers in this design share the same specifications, and they both share the same LO source. The only difference between the two channels is the quadrature channel receives a LO signal that is shifted 90° from that which is received by the inphase channel. The block that enacts the phase between the two channels should do so with minimal amplitude and phase error between. A 90° hybrid is sometimes used to fill this purpose, but may introduce finite errors across the downlink frequency band. As for the mixers, an active design is chosen because the signal power up to this point in the receiver is still relatively small at -30 dBm. An active design will provide some gain for the system and further reduce sensitivity to noise added by the following blocks. The mixer design should strive a gain of 7 dB with at most a noise figure of 15 dB. The IP1dB, IIP3, and IIP2 should be atleast -10 dBm, 0 dBm, and 10 dBm, respectively. Additionally, the mixer design should provide atleast 25 dB of isolation between all of its ports to minimize leakages and self-mixing.

Following the mixer is the active channel select filter. This block serves a dual purpose to provide a large amount of gain while filtering out undesired channels. The filtering characteristics should be capable of passing a single channel to relax linearity requirements of the final block in the system and to prevent aliasing from the ADC. The quality of the filter could be relaxed by over sampling at the ADC; however, this also increases the noise floor of the receiver and is not considered for the receiver design. The passband of the filter must extend from DC to 1.75 MHz; while the stop band should be atleast 13.5 dB down from the passband at 2.65 MHz. In addtion, it is advantageous for the filter to remove the DC component of the signals that arise from self-

mixing or IM2 products. To remove the DC component without significantly distorting the signal, the low corner frequency of the filter must be less than a thousandth of the signal bandwidth [19]. The DC offset could also be removed via active means if the doing so through filtering is not viable. For the active component of this block, the gain is specified to be 27 dB, providing a large portion of the overall receiver gain. Although this block filters out unwanted signals, the active component still has to deal with a composite signal power of -29 dBm at its input. Thus, the minimum IP1dB, IIP3, and IIP2 are -10 dBm, 0 dBm, and 10 dBm, respectively.

The VGA is the next block in the receiver chain. Its purpose is to provide a range of gain steps to allow amplification of the minimum signal power and maximum signal power to the required input power for the ADC and to account for some of the IQ mismatch throughout the system. Of the overall gain specification, 42 dB of gain has been accounted for in the prior blocks, leaving a maximum gain of 33 dB and a minimum gain of 3 dB for the VGA. Thus, the range of gain for the VGA will be specified as 3– 33 dB in 3 dB steps. Atleast 1 step above and below this range should be included to allow for extra gain margin. The output of the VGA must always be capable of handling the signal power supplied to the ADC. Since this was specified as a maximum of +4 dBm, the OP1dB, OIP3, and OIP2 must be atleast 10 dBm, 20 dBm, and 30 dBm, respectively, for all gain increments.

Lastly, the ADC specifications are considered for this receiver design. The ADC must have a high enough dynamic range to handle the PAPR and SNR of QPSK (13.53 dB + 4 dB) such that it does not limit the EVM performance of the transmitter. Using the following equation, the number of bits can be determined based on the required dynamic range and OSR.

$$Dynamic\ Range = 6.02 \times N + 3\log_2(OSR) + 1.76 \tag{3.4}$$

Here, N is the number of bits, and OSR is the oversampling rate [17]. As considered in the LPF specifications, the ADC will not be required to over sample; however, a sample rate slightly above nyquist will be considered. Solving for N gives a minimum number of bits of 3 for a sample rate of 4 MHz. Furthermore, the clock jitter of the ADC should be less than 12 ns based on the following equation where f_{in} is the highest input frequency component [17]:

$$SNR_{jitter} = -20\log_{20}\left(2\pi f_{in} t_{jitter}\right) \tag{3.5}$$

Table 3.3: Summary of receiver block specifications

Specification		Comments
Coupler	S_{21}=-0.97 dB; S_{31}=-6.99 dB; $S_{23}\geq$-25 dB	Coupler & BPF make up the diplexer
BPF	IL_{PASS}=3 dB; BW=2456 MHz – 2500 MHz; $IL_{STOP}\geq$ 25 dB @ 2444 MHz	Total isolation provided by diplexer should be ≥ 50 dB
LNA	G=15 dB; NF≤5 dB; OP1dB≥-10 dBm; OIP3≥0 dBm; OIP2≥10 dBm	Aim for NF≤3 dB
Power Divider	S_{21}=-3 dB; S_{31}=-3 dB	Required in discrete/MMIC designs
Active Mixer	G_{conv}=7 dB; NF≤15 dB; IP1dB≥-10 dBm; IIP3≥0dBm; IIP2≥10 dBm	> 25 dB isolation between ports
Active Filter	G=27 dB; NF≤15 dB; IP1dB≥-10 dBm; IIP3≥0 dBm; IIP2≥10 dBm	Amplifier and LPF combined for active filter
LPF	$A_{stop}\geq$13.53 dB @ 2.65 MHz; BW=1.75 MHz; f_{low_corner}<1 kHz	Prevents aliasing at the ADC
VGA	G_{min}=3 dB; G_{max}=33 dB; Step=3 dB; OP1dB≥10 dBm; OIP3≥20 dBm; OIP2≥30 dBm	Include atleast 1 step above and below G_{min} and G_{max}
ADC	DR≥17.53 dB; Bits≥ 4; $t_{jitter}\leq$8.5 ns; $f_{sample}\geq$4 MHz	Full Scale Input atleast +4 dBm

Table 3.3 summarizes all of the block design specifications discussed in this section. Each of these specifications were checked against other high temperature circuits to varify that the designs are realizable [12, 14, 15, 55]. Budget analysis on the cascade system can now be performed to verify that the cascade system meets the overall specifications from Table 3.2: Summary of overall downhole receiver specifications

Specification		Comments
System Temperature	250°C	
System Impedance	50 Ω	
Noise Figure	≈ 12 dB	Manufacturers typically target 10 dB
Sensitivity	-74.0 dBm	At 250°C with 6.4 dB margin
Min individual signal power Min composite signal power	-74.0 dBm -64.0 dBm	Composite signal combines 10 channels of equal power; adds 10 dB
Dynamic Range	> 26 dB	Based on coaxial channel attenuation
Max individual signal power Max composite signal power	-44.0 dBm -34.0 dBm	Considering dynamic range and PAPR
IP1dB	> -38 dBm > -28 dBm	Specified at point G Specified at point F; max comp. signal
IIP3	> -28 dBm > -18 dBm	Specified at point G Specified at point F; max comp. signal
IIP2	> -18 dBm > -8 dBm	Specified at point G Specified at point F; max comp. signal
ADC Full-scale input	+4 dBm	1 Vpp in 50 Ω system
Max Overall Gain	75 dB	
Min Overall Gain	45 dB	

Figure 3.8 graphs the cascade gain, noise figure, IP1dB, IIP3, and IIP2 at the minimum receiver gain, while Figure 3.9 graphs these parameters at the maximum receiver gain. These points (A-G) correspond to the nodes labeled in Figure 3.8. In the graphs, gain and noise at each node is simply the accumulation of the preceding blocks to that node. The linearity parameters on the graph, however, represent the input referred linearity metrics at the output nodes. This means these metrics are referred to the input of the receiver and the linearity at any given point takes into account the linearity performance of all blocks preceding it.

The budget analysis shows that the overall specifications for the receiver are met by this design. The maximum gain and minimum gain at point G are 73.8 dB and 49.5 dB, respectively. The noise figure at point G is 12.5 dB for both maximum and minimum gain configurations. The linearity performance at point F for both gain settings are $IP1dB = -26.6\,dBm$, $IIP3 = -16.8\,dBm$, and $IIP2 = -6.8\,dBm$. The IP1dB at this point is 7.4 dB above that of the maximum composite signal power at the input of the receiver. At point G, $IP1dB = -32.\,dBm$,

$IIP3 = -23.8\,dBm$, and $IIP2 = -13.8\,dBm$ for minimum gain and $IP1dB = -61.8\,dBm$, $IIP3 = -52.5\,dBm$, and $IIP2 = -42.8\,dBm$ for maximum gain. The IP1dB for both gain settings are atleast 8 dB above the single channel power experienced by either setting. In conclusion, the designed receiver and block specifications are able to meet and exceed the required

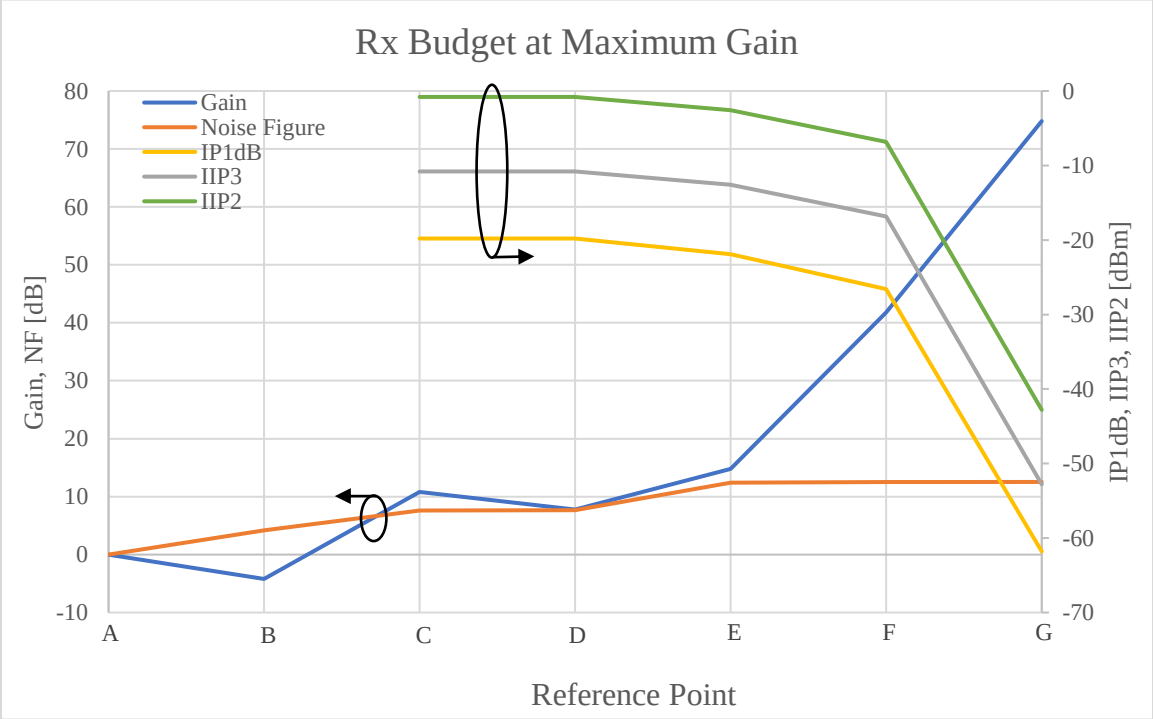

Figure 3.9: Receiver budget analysis at maximum gain

overall receiver specifications. The numbers used in the block specifications were kept as conservative as possible; thus, it is possible the system will further exceed the overall specifications.

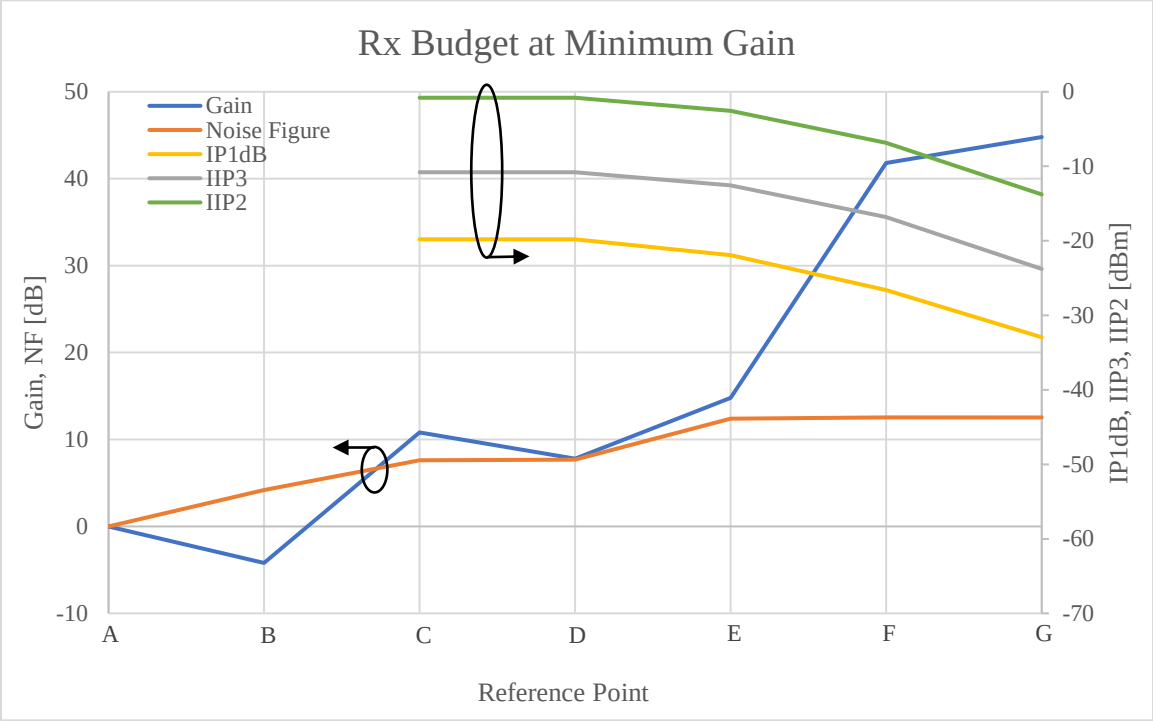

Figure 3.10: Receiver budget analysis at minimum gain

3.7 Transmitter Design

The transmitter of the downhole transceiver uses the direct conversion architecture as illustrated by its condensed block diagram in Figure 3.11. Again, this view simplifies the analysis of the transmitter system by collapsing the baseband I & Q channels into a single path. The full transmitter block diagram can be found in Figure 3.5.

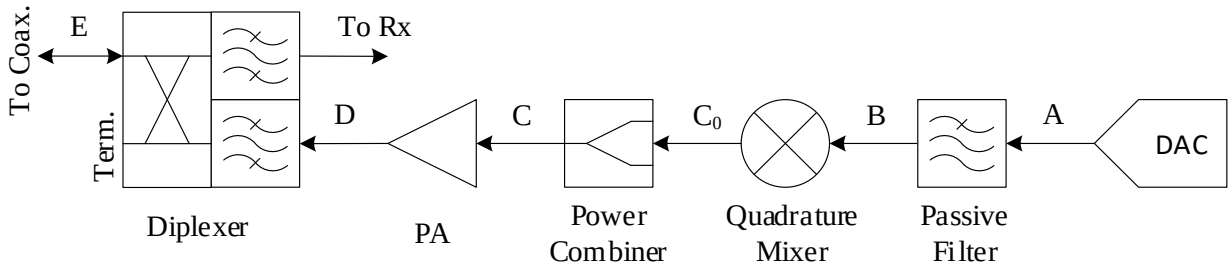

Figure 3.11: Transmitter block diagram

The transmitter is designed to support 16-, 32-, and 64-QAM signals with a BER no greater than 10^6. This allows high data rates for the uplink channel. The system will dynamically switch

between the three modulation schemes to achieve the highest data rates possible while maintaining BER. It should be noted the system is inherently capable of utilizing QPSK modulation since it has been designed for higher orders of QAM. As shown in the block diagram, the transmitter is comprised of a DAC, passive LPF, quadrature mixer, power combiner, PA, and a diplexer. The LPF filters the I & Q baseband signals to remove any harmonic content produced by the DAC. The quadrature mixer upconverts the baseband signals, applying a 90° phase difference between the two channels. The upconverted I & Q signals are then combined by the power combiner and subsequently amplified by the PA. Finally, the diplexer passes the uplink signal to the coaxial channel and provides isolation between the output of the PA and the input of the LNA on the receiver side. The PA and Mixer represent the only two blocks, not including the DAC, that are expected to show significant performance variations with temperature. The other blocks use passive RLC components or microstrip lines and are not expected to be sensitive to temperature. This minimizes the effect of temperature on the transmitter performance.

3.7.1 Overall Transmitter Specifications

The overall specifications of the transmitter will be determined by the SNR and PAPR requirements of the modulation schemes, the cascade attenuation and noise figure of the coaxial channel and RoF link, the maximum transmit power, adjacent channel power ratio, and the output power of the DAC. Each of these factors will be used to determine the required gain and linearity of the transmitter.

First, the SNR and PAPR of 16-, 32-, and 64-QAM will be considered. Table 3.1 lists the SNR for each modulation as well as its PAPR. 64-QAM has the highest requirements with an SNR of atleast 26.56 dB. It follows that the EVM performance of the transmitter be below 4.69%, preferrably with a sizeable margin. Additionally, 64-QAM has the largest PAPR at 7.3 dB. The following derivations will consider 64-QAM for the reason that it requires the best EVM and linearity performance.

Next, the link budget of the coaxial cable and the RoF link for tool #10 will be used to determine the minimum average transmitter power needed to meet the required SNR of 64-QAM. The gain and NF of the RoF link and coaxial channel, as discussed in sections 3.2 and 3.3, will be

used to determine the cascade NF of the link. The link will be performed from point D in Figure 3.11 (output of the PA) up to the surface receiver. For this analysis, the diplexer attenuation will be inferred from the receiver design as 10 dB. The diplexer for the RoF link will be assumed to have an insertion loss of 6 dB and the pre-amplifier will be assumed to have the same specifications as the LNA in the receiver design (G=15 dB, NF=5 dB). Lastly, the surface receiver is assumed to have a NF of 10 dB. Equation (2.8) is used to determine the cascade NF and the analysis is listed in Table 3.4: Budget Analysis for Uplink Channel

	Diplexer (Tx)	Coax. Channel	Diplexer	Pre-Amp	RoF Link	Surface Rx
Gain	-10.0 dB	-35.0 dB	-6.0 dB	15.0 dB	-34.0 dB	
NF	10.0 dB	35.0 dB	6.0 dB	5.0 dB	45.0 dB	10.0 dB
Cascade NF		10.0 dB	45.0 dB	56.0 dB	81.0 dB	83.4 dB

The resulting cascade noise figure is 83.4 dB which leads to the sensitiviy of the link, using (3.1), as 3.9 dBm for 64-QAM. Thus, the average transmit power at the ouput of the PA must be atleast 3.9 dBm to satisfy the SNR requirements for 64-QAM.

Table 3.4: Budget Analysis for Uplink Channel

	Diplexer (Tx)	Coax. Channel	Diplexer	Pre-Amp	RoF Link	Surface Rx
Gain	-10.0 dB	-35.0 dB	-6.0 dB	15.0 dB	-34.0 dB	
NF	10.0 dB	35.0 dB	6.0 dB	5.0 dB	45.0 dB	10.0 dB
Cascade NF		10.0 dB	45.0 dB	56.0 dB	81.0 dB	83.4 dB

With the minimum average transmit power determined, the maximum peak output power at the output of the PA must be calculated. This specification will depend solely on the linearity of the receiver and the isolation provided by the diplexer between the output of the PA and the input of the LNA. The IP1dB of the receiver's RF front end, as shown in Figure 3.10 at point F, is -26.6 dBm. Assuming the diplexer provides atleast 50 dB of isolation and including some margin, the maximum peak transmit power at the output of the PA (point D) is no more than 14 dBm. This

results in an average transmit power of 6 dBm after considering a PAPR of 8 dB for 64-QAM, which satisfies a minimum average transmit power of 3.9 dBm.

Next, the transmitter linearity requirements needed to meet adjacent channel power ratio (ACPR) is evaluated. The ACPR considers the IM3 products that land in adjacent channels generated by the transmitter OIP3. These calculations will be defined for point F, the PA output, to remain consistent with other specifications. The total power of IM3 products interfering with other channels should be low enough that the SNR requirement of the adjacent channels are still satisfied. For 64-QAM and a channel power of -74 dBm, the maximum ACPR requirement is -23.6 dBc. Using the following equation relating ACPR to OIP3, the OIP3 required to meet ACPR specifications can be determined.

$$ACPR = \frac{P_{TR}}{2} - 2OIP_3 + 10\log_{10}\left(\frac{f_2 - f_1}{BW}\right) \tag{3.6}$$

Here, P_{TR} is the average transmit power, OIP_3 is the output 3rd order intercept point, $f_2 - f_1$ is the signal bandwidth, and BW is the channel bandwidth [17]. For this calculation, P_{TR} and OIP_3 will be defined at the output of the PA, where $P_{TR} = 6\ dBm$, and the utilized bandwidth ratio will be assumed as $3/3.5$. The resulting minimum OIP_3 at the PA output is 14.7 dBm.

Another consideration for linearity is the peak transmit power determined previously. As specified previously, the maximum allowable peak transmit power should be no more than 14 dBm to prevent saturating the receiver. The minimum OP1dB with a 6 dB margin at the output of the PA is therefore 20 dBm and the minimum OIP3 is 30 dBm. Fortunately, this OIP3 is more than enough to satisfy the requirements for ACPR as well.

Lastly, the required gain of the transmitter is determined by the maximum average transmit power and the average DAC output power. A typical DAC, according to [17], is capable of achieving a full scale output power of +7 dBm; however, to prevent saturating the transmitter blocks, it will be assumed the DAC can adjust its full scale output. The average DAC output power used for the design is -10 dBm, the peak output power is -2 dBm to account for PAPR, and the full scale output is considered to be 0 dBm to adjust for IQ mismatch in the transmitter. Taking the difference between the DAC average output power and the PA average output power, a gain of 16 dB is required. Table 3.5 summarizes the overall specifications discussed in this section for the transmitter.

Table 3.5: Summary of overall downhole transmitter specifications

Specification		Comments
System Temperature	250°C	
System Impedance	50 Ω	
Modulation	16-, 32-, and 64-QAM	PAPR for 64-QAM > 7.3 dB
Max Peak Power	≤14 dBm	Based on Rx IP1dB; 60 dB isolation
ACPR	≤ -23.6 dBm	Assumes 64-QAM
OP1dB	≥ 20 dBm	Based on max peak power; 6 dB margin; Specified at PA output
OIP3	≥ 30 dBm	Specified at PA output
DAC max output PWR DAC average output PWR	-2 dBm -10 dBm	Assumes DAC full scale range is scaleable.
Gain	16 dB	Specified at PA output

3.7.2 Block Specifications

As was done for the receiver, the overall transmitter specifications from Table 3.5 will be broken down and allocated to the diplexer, PA, power combiner, passive mixer, LPF and DAC. The typical considerations for considerations for system design – gain, NF, and linearity – are given a different emphasis in transmitter design than in receiver design. The DAC typically outputs a large signal and the transmitter chain deals with much larger powers than what is handled in the receiver. For this reason, NF is not typically considered in the transmitter design, but linearity becomes a much larger issue. The signal levels at each node in the transmitter chain must be carefully considered to avoid saturating the transmitter. Saturation and the effects due to linearity can be mitigated by reserving any gain in the system for the last blocks in the transmitter (i.e. the PA). This can be accomplished since NF is no longer a constraint on where gain is required in the system.

First, the LPF and DAC performance will be considered. The only purpose the LPF serves is to remove the harmonics generated by the DAC to prevent adjacent channel interference. The quality of the LPF must be high enough to ensure the harmonics are atleast 26.56 dB down from the adjacent channel; however, too selective of a filter will cause distortions to the QAM signal. The quality of the filter can be reduced by oversampling the signal since the harmonics occur at

multiples of the sampling frequency. The nearest harmonic to the pass band of the filter will be approximately −13 dBc, as illustrated by Figure 3.12, leaving atleast 13.56 dB to be attenuated by the filter. With this in mind, the LPF is specified to have no more than 3 dB loss in the passband of 1.75 MHz and atleast 16 dB of attenuation at an oversampling rate of 2. The resulting DAC sampling frequency, in this case, is 7 MHz.

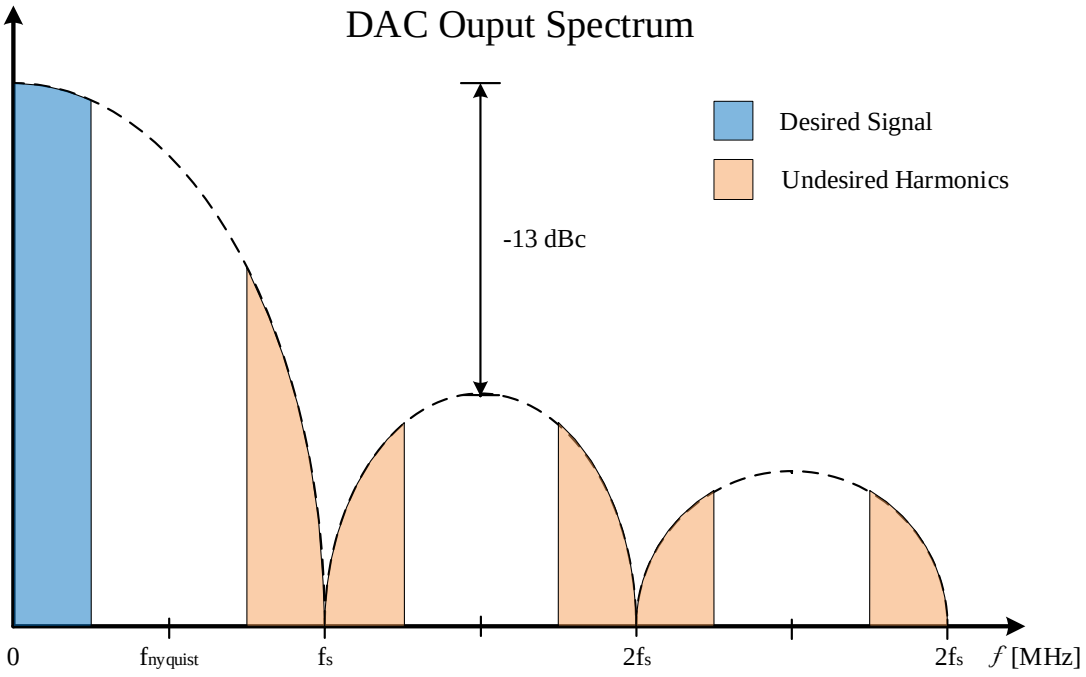

Figure 3.12: Harmonics generated by the DAC

As with the ADC in the receiver, the DAC should have a high enough dynamic range to handle the PAPR and SNR of 64-QAM (25.56 dB + 8 dB) such that it does not limit the EVM performance of the transmitter. The same equations used to evaluate the ADC performance can also be applied to the DAC. Performing the calculations using an SNR of 36.56 dB and an OSR of 2, the required number of bits is 6 with a clock jitter less than 0.68 ns.

Next, the quadrature upconversion mixer and the power combiner are considered. The mixer to perform the upconversion function utilizes a passive topology on the account of its superior linearity performance and loss compared to an active topology. Based on the peak signal power at the input to the mixer (-5 dBm), the IP1dB should be greater than 1 dBm. High temperature passive mixer designs reported by [8, 9, 56] indicate that a CL loss of 8 dB, IP1dB of 8 dBm, and IIP3 of 18 dBm is reasonable to expect. For good measure, the port isolations for

this LO is specified as 25 dB, but they do not as critical as in the receiver as long as the leakage power does not saturate the mixer or the PA and the surface receiver compensates for the DC offset resulting from LO to RF leakage.

The power combiner takes the upconverted I & Q signals at its input ports and combines at its output. The power combiner design is the same overall design as that for the receiver only shifted in frequency to accommodate uplink signals. The design must be matched to 50 Ω at all ports, operate in the uplink band (2400 – 2444 MHz), and minimize the amplitude and phase mismatch between its input ports. As with the power divider in the receiver, the Wilkinson power divider is an excellent candidate to implement a power combiner because it is a recipricol network [54]. The insertion loss of the combiner is 3 dB for an equal combination, but combining the I & Q channels results in a 6 dB increase in signal power. Thus, the power combiner has an overall gain of 3 dB.

In a typical transmitter, the PA must provide high output power and high gain with high efficiency. The PA in this design will provide nearly all of the gain required by the system, but will not be required to handle high output powers nor have high efficiency. The peak output power, as defined by Table 3.5, is no more than 14 dBm which is only 25 mW. With such a low output power, the efficiency requirement of PA is only driven by how much power dissipation the design can handle while operating at 250°C. This specification will vary based on the technology and packaging used for the design. Considering the cumulative gain up to the PA input and the average signal powers, the required gain of the PA is 24 dB. The output linearity is driven by the peak output power giving the minimum OP1dB and OIP3 as 20 dBm and 30 dBm, respectively.

Finally, the diplexer, as seen by the transmitter, is considered. The coupler design is the same as designed for the receiver, except the port connecting the transmitter to coaxial channel has an insertion loss of -6.99 dB. The BPF specifications are also the same, only shifted in frequency for the uplink band. The pass band ranges from 2400 Mhz to 2444 MHz and its insertion loss should be no more than 3 dB. The stop band insertion loss should be greater than 25 dB at 2456 MHz. Lastly, the overall isolation provided by the diplexer should be greater than 25 dB to avoid saturating the receiver. The stob band insertion loss and coupler isolation can be adjusted accordingly.

Each block specification discussed in this section is summarized in Table 3.6. The specifications discussed were compared against similar high temperature circuits, reported by [8-10, 56], to ensure no block is impractical to design. Figure 3.13 graphs the budget analysis performed for gain, OP1dB, and OIP3 of the transmitter. The reference points on the graph correspond to the point the measurement is taken in Figure 3.11. Note, C_0 is not represented in the budget analysis because the power combiner is included with the quadrature mixer in the simulation. Point D refers to the output of the PA, which is where the overall transmitter specifications are defined. The gain, OP1dB, and OIP3 are 15.0 dBm, 19.3 dBm, and 28.3 dBm, respectively. Although these values are below the design specifications, it can be shown that these values are adequate for the transmitter performance after adjusting the design for the output power.

An unaccounted for 1 dB of gain was lost from the mixer or power combiner in the budget analysis simulation, so the output power to the PA is 1 dB less as well. For a 64-QAM signal with a peak output power of 13 dBm, the desired OP1dB is 19 dBm including a 6 dB margin. It follows that the desired OIP3 must be atleast 29 dBm. These results show that the design acheives the desired specifications after adjusting for the lost gain.

Table 3.6: Summary of transmitter block specifications

Specification		Comments
DAC	DR ≥34.56 dB; Bits≥5; t_{jitter}≤1.2 ns; f_{sample}≥7 MHz	SNR value for 64-QAM with margin
LPF	IL_{PASS}=3 dB; BW=1.75 MHz; f_{low_corner}<1 kHz; IL_{STOP}≥16 dB @ 7 MHz	Tx only handles one channel; filter requirements relaxed
Passive Mixer	G_{conv}=-8 dB; NF≤7 dB; IP1dB≥5 dBm; IIP3≥15 dBm; IIP2≥25 dBm	> 25 dB isolation between ports
Power Divider	S_{21}=-3 dB; S_{31}=-3 dB	Required in discrete/MMIC designs
PA	G=24 dB; OP1dB≥20 dBm; OIP3≥30 dBm; OIP2≥40 dBm	Efficiency is not critical for this PA as P_{out_max} = 25 mW. DC power dissipation is more critical.
BPF	IL_{PASS}=3 dB; BW=2400 MHz – 2444 MHz; IL_{Stop}≥25 dB @ 2456 MHz	
Coupler	S_{21}=-0.97 dB; S_{31}=-6.99 dB; S_{23}≥-20 dB	

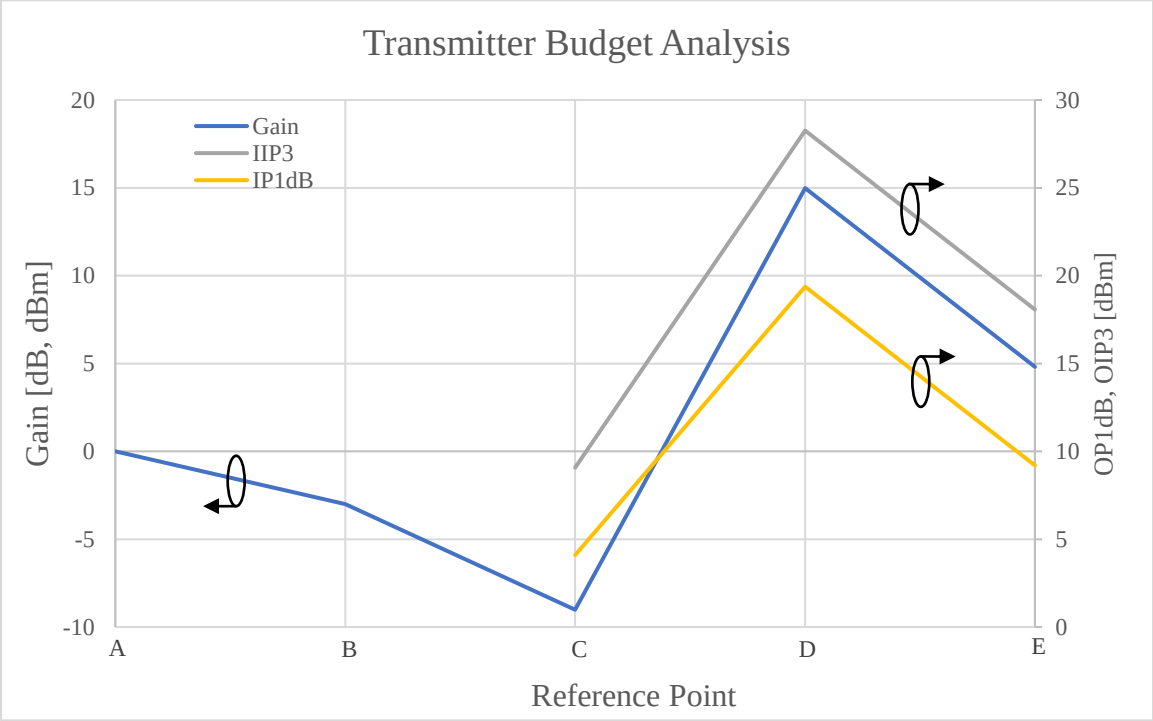

Figure 3.13: Transmitter Budget Analysis

3.8 Design and IC Considerations

When it comes to designing individual blocks and implementing the full system, whether for a discrete, RFIC, or MMIC implementation, there are some considerations that must be taken into acount. These considerations revolve around the size of the circuit, the technology used, and changes to the system for different levels of integration.

As discussed in this work, the system design is initially intended for a discrete design. Even so, there is a discussion to be had about the technology and potential modifications that could be made to the system depending of several factors. First, GaN-SiC discrete transistors are the most suitable commercially available devices to implement the RF front-end blocks of the high-temperature transceiver. These commercial devices are intended for high-power RF applications, but can be used at high-temperature RF instead. The baseband section has more flexibility to use commercial SiC or SOI devices due to its low frequency. In terms of passive devices, the RF and baseband blocks have the option to utilize commercial discrete capacitors and planar inductors or microstrip line for the design. The main consideration here is balancing performance and size of the circuit.

The system design specifications were kept as conservative as could be tolerated by the system. This was done for power consumption considerations as there typically exists a trade-off between power consumption of a design and its performance in gain, NF, and linearity. Keeping the requirements conservative allows more flexibility between performance, power dissipation, and operating temperature. As a result of this design methodology, some of the margins in the system are small. The main area of concern is the transmit power of the downhole transmitter, which was constrained by the sensitivity of the uplink channel, the linearity of downhole receiver, and the isolation between transmitter and receiver. Ideally, the transmit power of the transmitter is larger than what is specified in the system design to have a larger margin above the uplink channel sensitivity. This could be accomplished with higher linearity performance of the receiver or greater isolation provided by the diplexer. Any amount of increase of either parameter leads to the same increase for peak and average transmit power. This would require the gain and linearity of the PA to increase by the same amount. If transmit power is increased, some amount of gain controll, in the form of a variable attenuator, may be required in the baseband of the transmitter to prevent the first few transmitters along the coaxial cable from saturating the RoF link.

For a MMIC implementation of this design, the technologies available are limited. The only process currently available to implement the RF front-end is GaN-SiC; while the baseband sections are implemented off-chip in a more suitable technology. At this level of integration, microstrip lines become too large, so on-chip lumped elements must be used to acheive impedance maching and implement microwave structures, such as the power divider/combiner and the coupler. It is not anticipated that the system specifications will need to be modified for a MMIC implementation.

An RFIC implementation, on the other hand, will not require the power divider/combiner or coupler. The insertion loss of the divider/combiner in the receiver and transmitter should be accounted for by increasing the linearity requirements of subsequent blocks in the system or reducing gain of the LNA/PA. However, reducing the gain of the LNA is not recommended as this will negatively impact the NF of the receiver. An RFIC design would be best implemented using a partially-depleted (PD) or fully-depleted (FD) SOI process. FD-SOI is expected to have better high-temperature performance than PD-SOI; however, PD-SOI processes are currently more mature [57].

3.9 Surface Transceiver Considerations

Although the surface transceiver is not designed outright, the anticipated performance is considered in the design of the downhole transceiver. First, the surface receiver must be capable of supporting up to 64-QAM with a BER of 10^{-6} to match the downhole transmitter. This requires the EVM performance of the surface receiver to be better than 4.69%, as specified by Table 3.1. The expected NF of the receiver is 10 dB or better, a figure typically targeted by commercial systems. Because all ten channels are transmitted with the same average power, the dynamic range of the receiver should be atleast 26 dB with a minimum average signal power of -64 dBm. Lastly, the linearity of the receiver should be capable of handling a peak signal power of -27 dBm.

The surface transmitter is only required to support QPSK modulation with EVM performance better than 21% for a BER of 10^{-6}. The minimum average transmit power is estimated to be -26.5 dBm, while the peak transmit power is estimated to be 1 dBm. These numbers, being low for a transmitter, indicate there is overhead for a longer RoF link. Additionally, with the low transmit power, the linearity and ACPR of the surface transmitter are not a concern.

The specified performance of the surface transceiver is estimated based on the design of the downhole transceiver and are subject to change depending on how well the downhole transceiver satisfies its specifications. Even so, modern radio designs, such as software defined radios, are capable of far exceeding the performance of what is required by the surface transceiver [58, 59].

3.10 Chapter Summary

This chapter began with an overview of the proposed downhole telemetry system and proceeded to explain the design and specifications of the transceiver. First, the RoF link and coaxial channel design followed by the proposed transceiver design was presented. The frequency plan was developed to support FDMA at the 2.4 – 2.5 GHz ISM band. The overall specifications for the receiver and transmitter was extracted from the goals of the telemetry system. These overall specifications were then broken down into individual block specifications. After determining each block's specifications, the budget analysis of both the transmitter and receiver was performed showing each system met the overall specifications. Next, some design considerations were

discussed for the discrete, MMIC, and RFIC implementations. The chapter concluded with a brief consideration to the surface transceiver performance requirements.

Chapter 4

Simulation Environment & Results

This chapter begins with an explaination of the software used to simulate the receiver and transmitter performance. The simulation environment and setup will be discussed and performance targets will be reviewed. Next, the receiver performance will be presented and discussed, followed by the transmitter performance. Lastly, the effects temperature has on individual blocks will be described, and the anticipated performance of the transceiver over its intended operating temperature range will be presented.

4.1 Simulation Software

National Instruments' AWR Design Environment (AWRDE) is the software of choice to perform the transceiver system level simulation. The design environment consists of three power simulation tools, Visual System Software (VSS), Microwave Office (MWO), and Analog Office (AO), targeted at different aspects of an entire system design. VSS is targeted towards the system level simulation; MWO is geared towards microwave circuit simulation; while, AO is for analog circuits and RFIC design. Of these tools, VSS is the tool used to simulate the receiver and transmitter EVM performance, constellation, and spectrum; moreover, MWO may be used in the future to design the individual blocks of the system and add their performance into the system level simulation.

VSS is a time domain simulator which uses complex envelope representation of the signals to significantly reduce simulation time. Typical simulators for RF frequencies use the real signal representation, which is the complex envelope modulated onto a carrier signal. A comparison of the complex envelop and real signal representations can be found in Figure 4.1. The real signal representation requires the simulator to sample atleast twice the highest frequency component of the signal to satisfy Nyquist, which for this design would be > 4.8 GHz. Simulations operating at these sample rates will take a significant amount of time to run. To reduce simulation times, VSS simulates only the complex envelope used to modulate the carrier signal throughout the system simulation. The carrier signal frequency is then simply attributed to the complex envelope and

propogated throughout the entire system chain. This allows the simulator to use Nyquist's lesser known theorem which states the sampling frequency only needs to be atleast twice the signal bandwidth. In the case of this design, the simulator only needs to support a sampling frequency of > 7 MHz for a single channel or > 100 MHz for the entire uplink/downlink band. This is a significant difference compared to simulating the real signal, making VSS a much more time efficient simulation software.

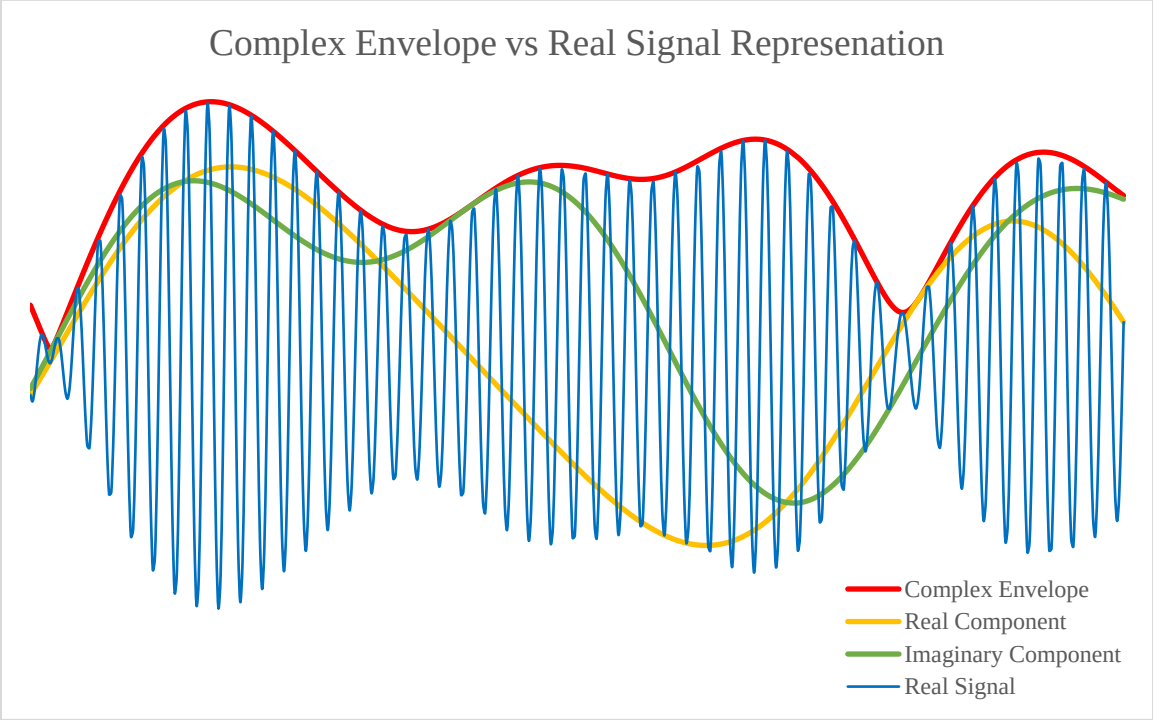

Figure 4.1: Comparison of complex envelope signals and real signals

4.2 Receiver Performance

The system level simulation for the downhole receiver is setup to simultaneously simulate four receiver systems in parallel along the coaxial channel The receivers are chosen to be equally spaced along the coaxial channel as tools #1, #4, #7, and #10. Moreover, the surface transmitter, coaxial channel, and RoF link are not modeled in the receiver system-level simulation. The performance of the coaxial channel and RoF link are compensated for by adjusting the input signal powers at the input of the receiver.

All 10 channels in the downlink band, as illustrated by Figure 3.7, are setup in the receiver testbench. The signals are generated from QPSK modulated signal sources using root-raised cosine pulse shaping with a roll-off factor of 0.35. The avg. powers of all the channels are kept equal, but they are adjusted for attenuation expected through the coaxial channel. Note, for these tests, the average signal power referrs to the power of a single channel. When all 10 channels are involved, the average composite signal power is 10 dB greater than a single channel. All 10 channels are fed to the input of each receiver, and each receiver is set to down-select to 1 channel based on which tool the receiver represents. Both the average power and symbol rate of these signals are controlled through sweeps or set as a constant, depending on the simulation.

Each block of the receiver is simulated using the minimum specifications listed in Table 3.1. The coupler and power divider are simulated using an RF attenuator set to their specified insertion losses. The VGA is set to its minimum gain for all receivers because the simulation has built in gain control. The baseband LPF and the RF front-end BPF are simulated as shown in Figure 4.2 and Figure 4.3, respectively. To achieve the necessary performance, the LPF is modeled

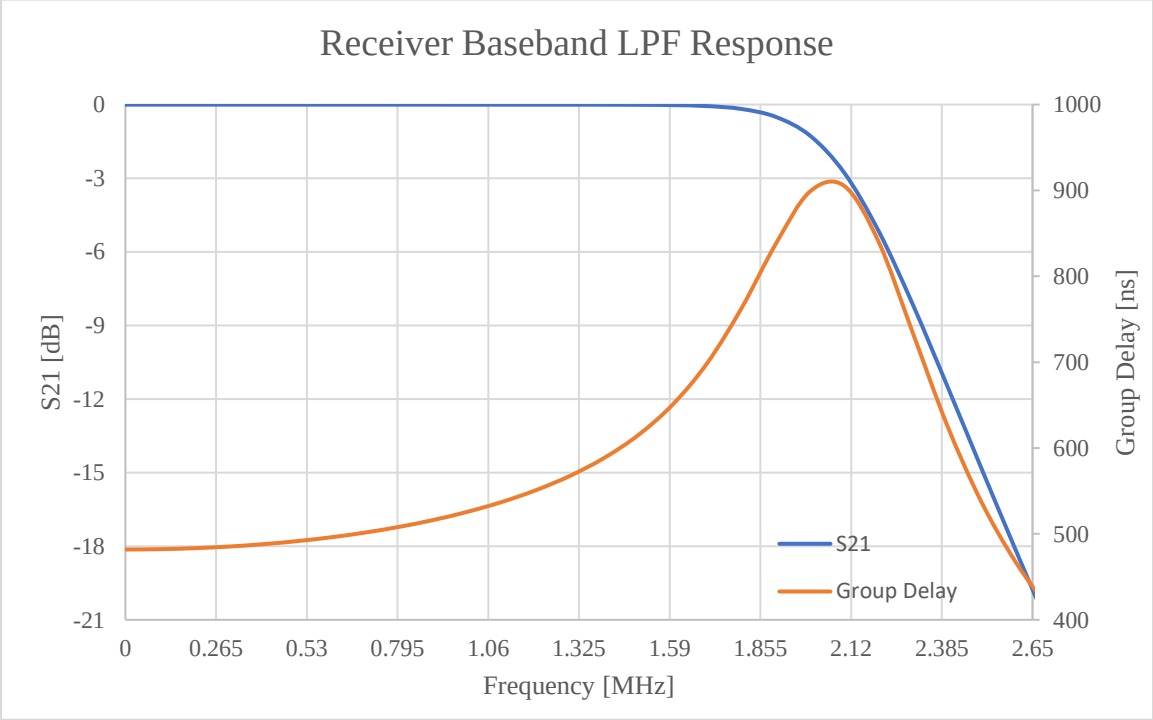

Figure 4.2: Baseband LPF response. 10th order Buttersworth filter; 0.1 dB bandwidth of 1.75 MHz.

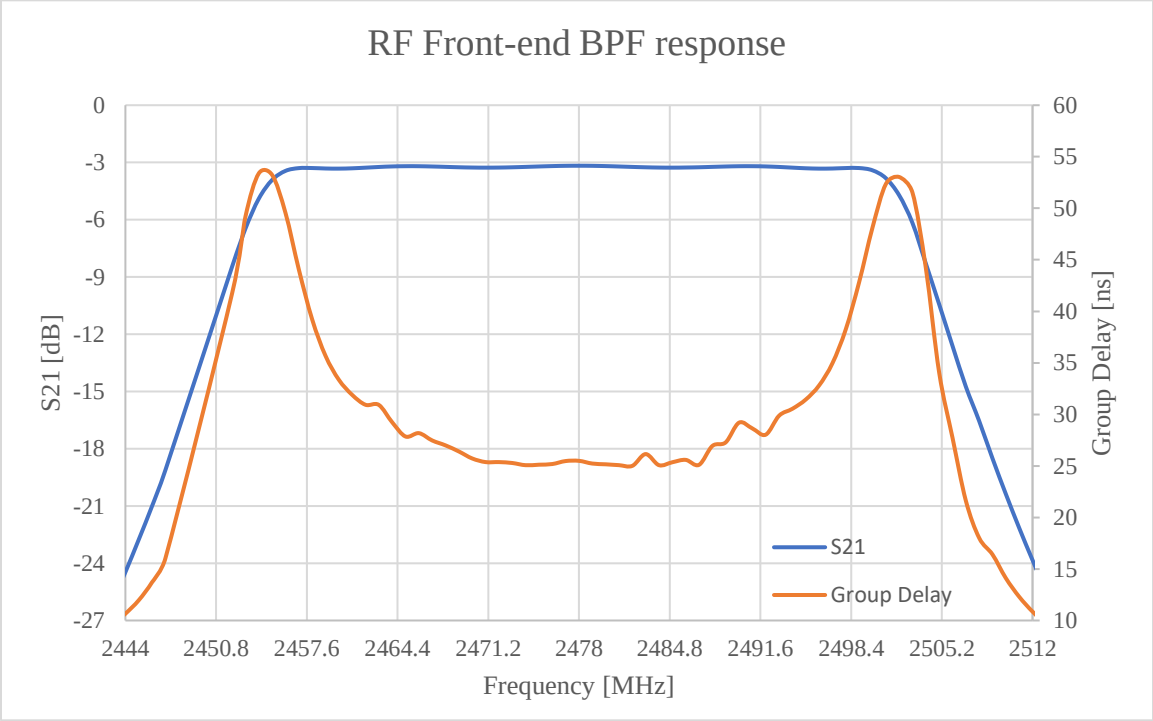

Figure 4.3: RF front-end BPF response. 5th order Chebyshev filter; 0.1 dB bandwidth of 2456 – 2500 MHz.

as a 10th order Buttersworth filter with a 0.1 dB bandwidth of 1.75 MHz. The filter acheives -20 dB of attenuation at 2.65 MHz. For the BPF filter, a 5th order Chebyshev filter with a 0.1 dB ripple is used to achieve -24.5 dB attenuation at the stop band.

The receiver test bench is designed to model all of the factors that could effect the receiver performance. The simulation considers the operating temperature of 250°C in determining the thermal noise floor of the receiver and is capable of sweeping the temperature to simulate different operating environments. The simulation includes linearity performance based on P1dB, IP3, and IP2. The phase noise mask used for the LO is -100 dBc at 100 kHz and -115 dBc at 1 MHz. This phase noise is derived from the VCO designed by a colleague specifically for this transceiver design [35]. Lastly, the IQ mismatch of the receiver is set to be 0.5 dB of amplitude mismatch and 1° of phase mismatch. These values assume the receiver will eventually be capable of calibration.

The first test conducted on the receiver design evaluates the EVM performance of all 4 simulated receivers versus the symbol rate as shown in Figure 4.4. The EVM of each receiver is

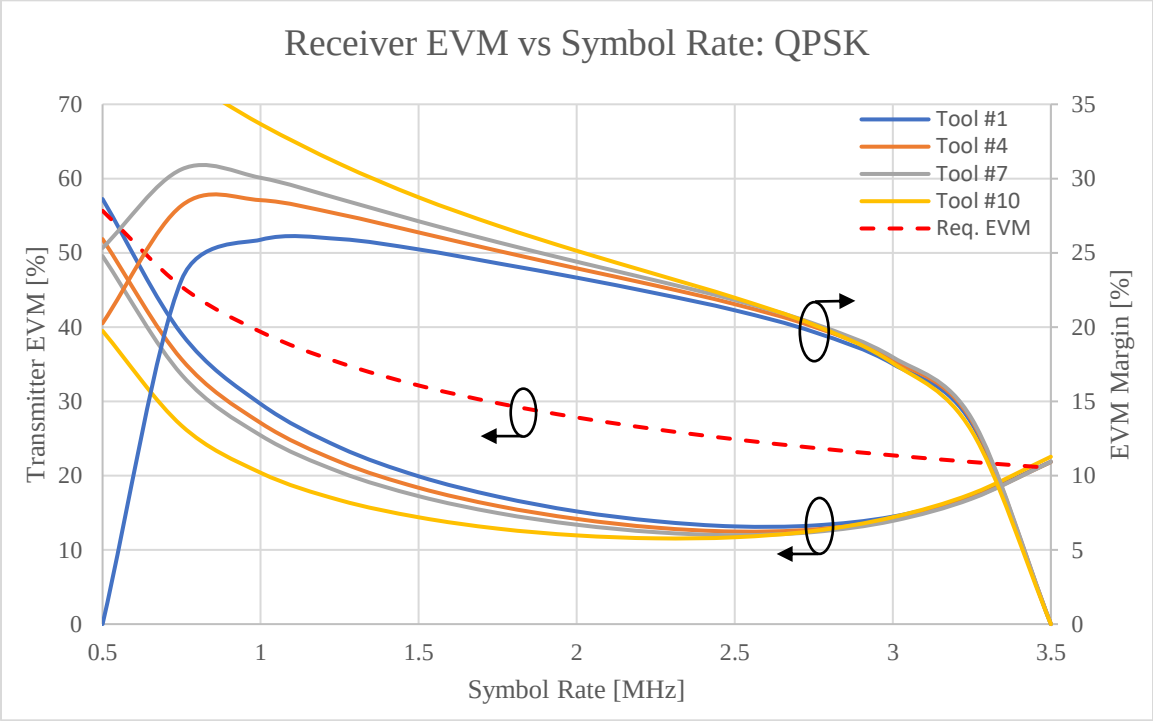

Figure 4.4: Receiver EVM performance vs symbol rate for QPSK modulation.

compared against the required EVM for QPSK modulation and BER of 10^{-6}, illustrated by the dashed line. The EVM requirement is given by (2.3) and (2.4) over the swept symbol rate (f_s). Additionally, the required EVM performance from the surface transmitter is calculated from the EVM performance of the transmitter and the QPSK EVM requirement using (2.6). An EVM margin of 4% for the surface transmitter should be easily attainable considering a controlled environment and relatively no size, weight, or power restrictions. The sweep is carried out for an average signal power of -47 dBm, -56 dBm, -65 dBm, and -74 dBm for receiver #1, #4, #7, and #10, respectively. The performance at low symbol rates is affected by the LO phase noise, while the performance at higher symbol rates is affected mostly by the group delay of the baseband filter, as shown in Figure 4.2. From the plot, it can be seen that all receivers achieve the necessary performance for symbol rates between 0.6 MHz and 3.4 MHz. This shows each receiver is capable of achieving a data rate of 6.8 Mbps per tool, which is 68 Mbps for the entire downlink band.

Next, the symbol rate is held as a constant and the average signal power is swept to determine the dynamic range achieved by the system. The average signal power across all ten channels are kept equal relative to each other. Figure 4.5 shows the results of this sweep compared

to the required EVM for QPSK at a symbol rate of 3.4 MHz. The difference between the points at which the receiver EVM cross the required EVM is regarded as the dynamic range of the receiver. It can be determined from the graph that the minimum and the maximum average signal power are -75.2 dBm and -46.8 dBm, respectively. This results in a dynamic range of 28.4 dB, exceeding the required dynamic range of 26 dB. Furthermore, the dynamic range of the receiver can be improved by several dB with only a small reduction to the symbol rate. The min and max signal powers and the dynamic range are improved to -78.7 dBm, -43.6 dBm, and 35.1 dB, respectively, by reducing the symbol rate by just 0.1 MHz to 3.3 MHz. Lastly, the lowest performing tool reaches its best EVM performance and the dynamic range increases to 52 dB ranging from -85 dBm to -34 dBm at a symbol rate of 2.5 MHz.

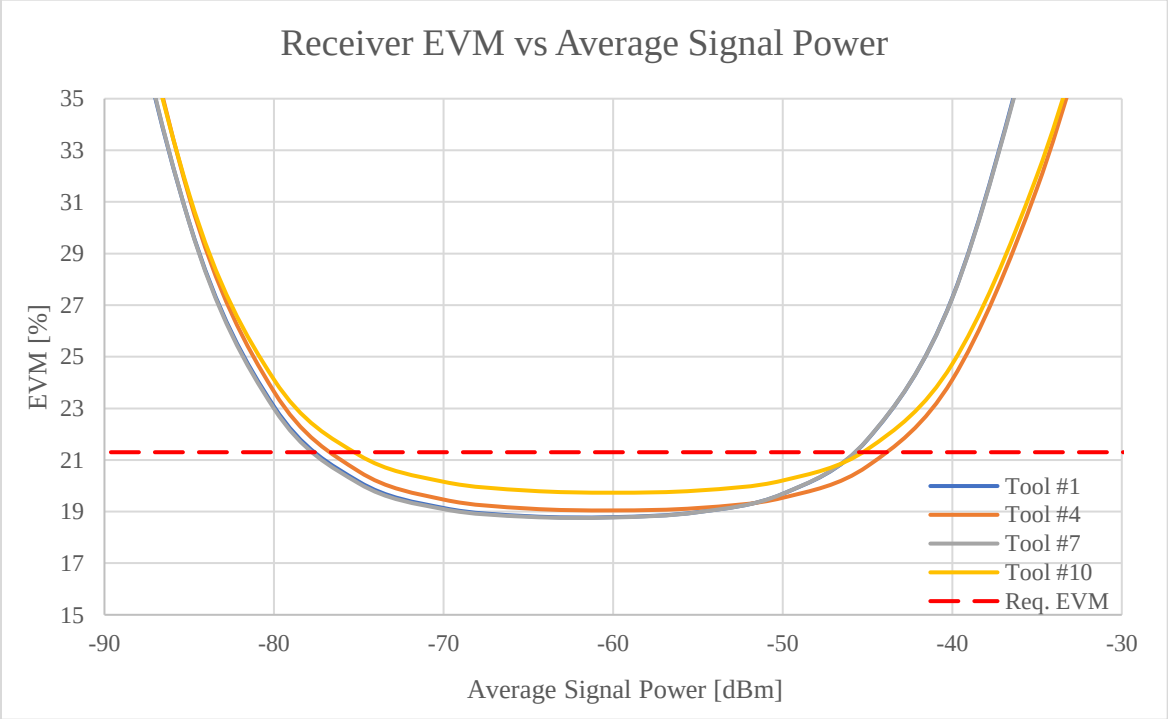

Figure 4.5: Receiver EVM performance vs avg. individual signal power for QPSK modulation. Symbol Rate = 3.4 MHz.

Lastly, setting a constant average signal power of -60 dBm and a symbol rate of 3.4 MHz, the baseband operation and received QPSK constellation are observed. Figure 4.6 illustrates the baseband signal as seen by tool #4 before and after the low-pass channel-select filter whose response is shown in Figure 4.2. This illustrates that the LPF provides adequate adjacent channel

rejection to prevent aliasing at the ADC. The signal passed on to the ADC generates an IQ constellation for QPSK, as shown in Figure 4.7. Indicative of the EVM performance, the received constellation is imperfect; however, the decision boundary between each symbol is clearly defined. The main signal distortions affecting the constellation are phase noise, filter group delay, and IQ mismatch.

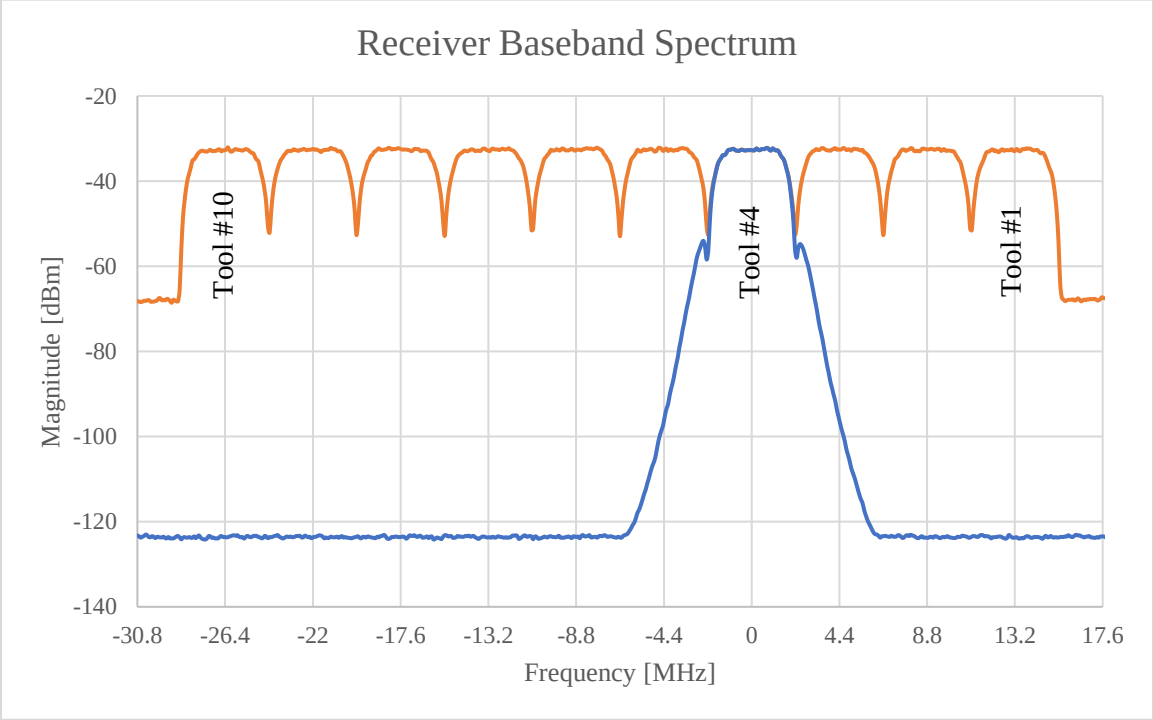

Figure 4.6: Receiver filtered and unfiltered baseband spectrum. Avg. individual signal power = −60 dBm; Symbol Rate = 3.4 MHz

In conclusion, the simulated receiver performance is able to meet and exceed design requirements. Each of the 10 receivers is capable of supporting a data rate up to 6.8 Mbps with a dynamic range of 28.4 dB given the surface transmitter EVM performance is at most 4%. Additionally, the receiver supports a minimum average signal power of -75.2 dBm and a maximum average signal power of -46.8 dBm. These correspond to a composite average signal power of -65.2 dBm and -36.8 dBm, respectively. The transmitter EVM performance requirement, dynamic range, and power handling of the receiver can be improved by lowering the symbol rate, sacrificing the data rate of the downlink channel.

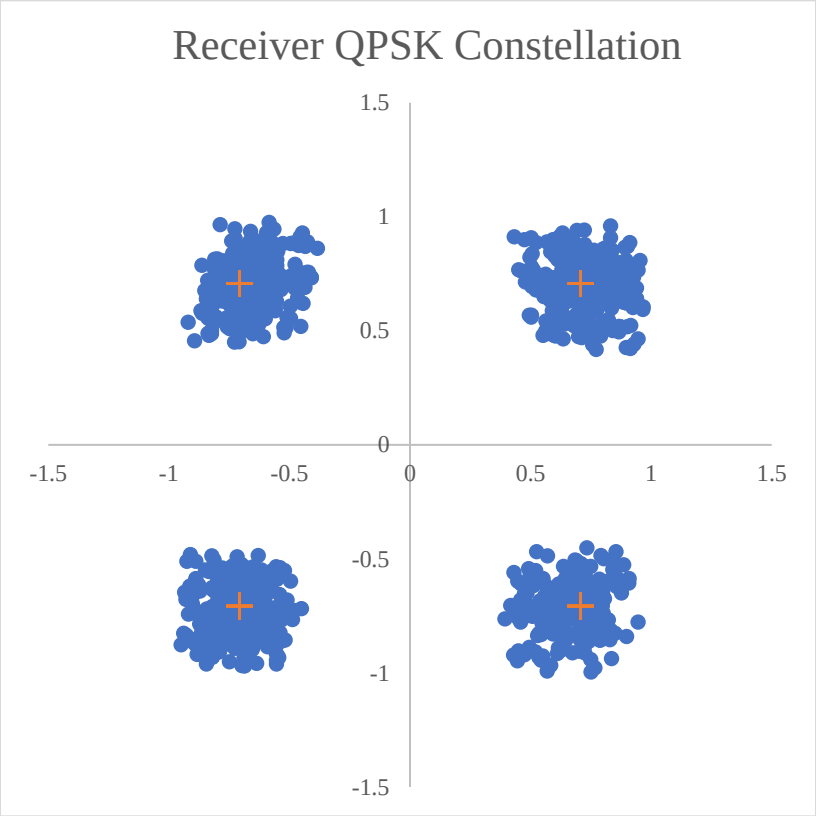

Figure 4.7: Receiver QPSK Constellation for tool #4. Avg. individual signal power = -60 dBm; Symbol Rate = 3.4 MHz.

4.3 Transmitter Performance

The transmitter system level simulation, like that of the receiver, is setup to simulate the performance of four parallel transmitters spaced out as tool #1, #4, #7, and #10 along the coaxial channel. The coaxial channel and RoF link are modeled in the test bench, but the surface receiver is not. Therefore, all simulated results are extracted from the end of the RoF link.

The signals in the test bench are generated by M-QAM sources using a root-raised cosine pulse shape filter with a roll-off factor of 0.35. These sources stand in for the DAC to generate the I & Q baseband signals for 16-, 32-, and 64-QAM. Their output frequencies are set to 0 Hz and their average output power is fixed at -10 dBm. The only parameter swept in the simulation with regards to the modulated signal source is the symbol rate. Additionally, since each transmitter only handle a single channel, only channels #1, #4, #7, and #10 are simulated in the test bench.

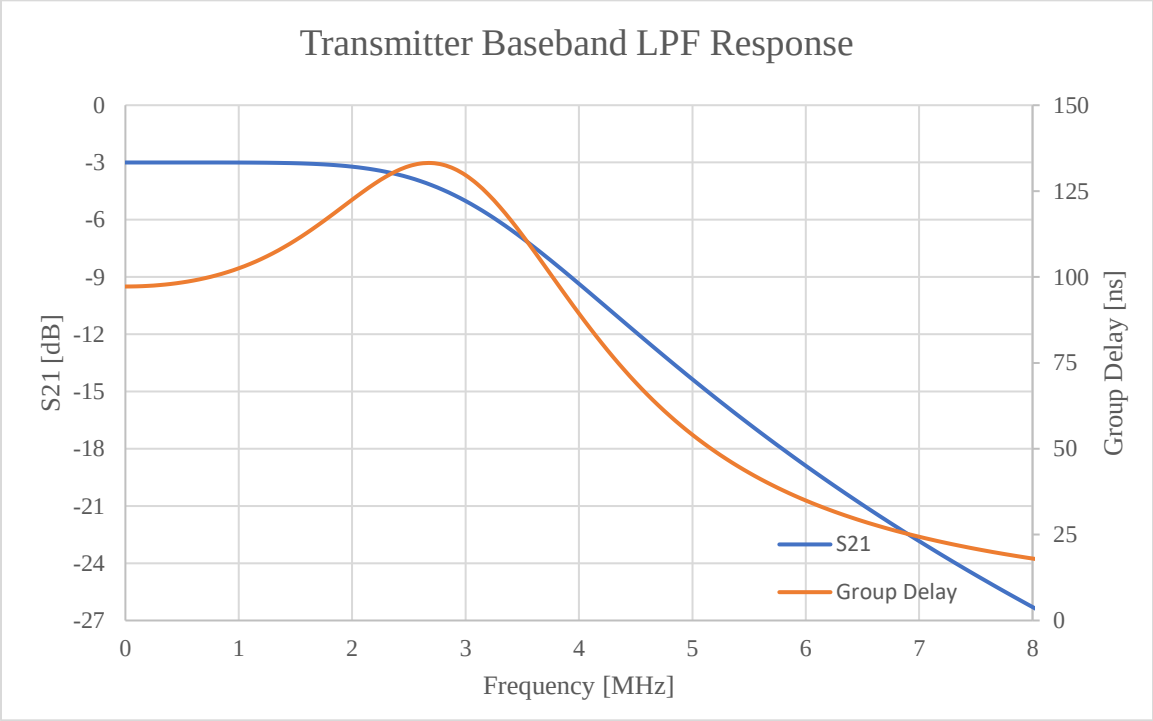

Figure 4.8: Transmitter baseband LPF response. 3rd order Buttersworth filter; 0.1 dB bandwidth of 1.75 MHz.

Table 3.6 lists all of the transmitter block specifications that are used to simulate the transmitter performance. As was done with the receiver, the insertion losses of the coupler and power combiner are simulated using an RF attenuator set to -7 dB and -3 dB, respectively. The coaxial channel is modeled using an RF attenuator as well, with attenuation set according to Figure 3.4 at 2450 MHz. The baseband LPF and the RF front-end BPF responses are dipicted by Figure 4.8 and Figure 4.9, respectively. A 3rd order Buttersworth filter with 3 dB attenuation in the pass band and a 0.1 dB bandwidth of 1.75 MHz is used to simulate the baseband LPF, while the RF front-end BPF is simulated with the same specifications used for the receiver. That is, a 5th order Chebyshev filter with a passband insertion loss of 3 dB and a 0.1 dB bandwidth from 2400 MHz to 2444 MHz. It can be determined from the figures that the baseband LPF acheives atleast -13 dBc for frequencies beyond 5.4 MHz and the RF front-end BPF acheives an insertion loss of 24.5 dB at 2456 MHz, the beginning of the downlink band.

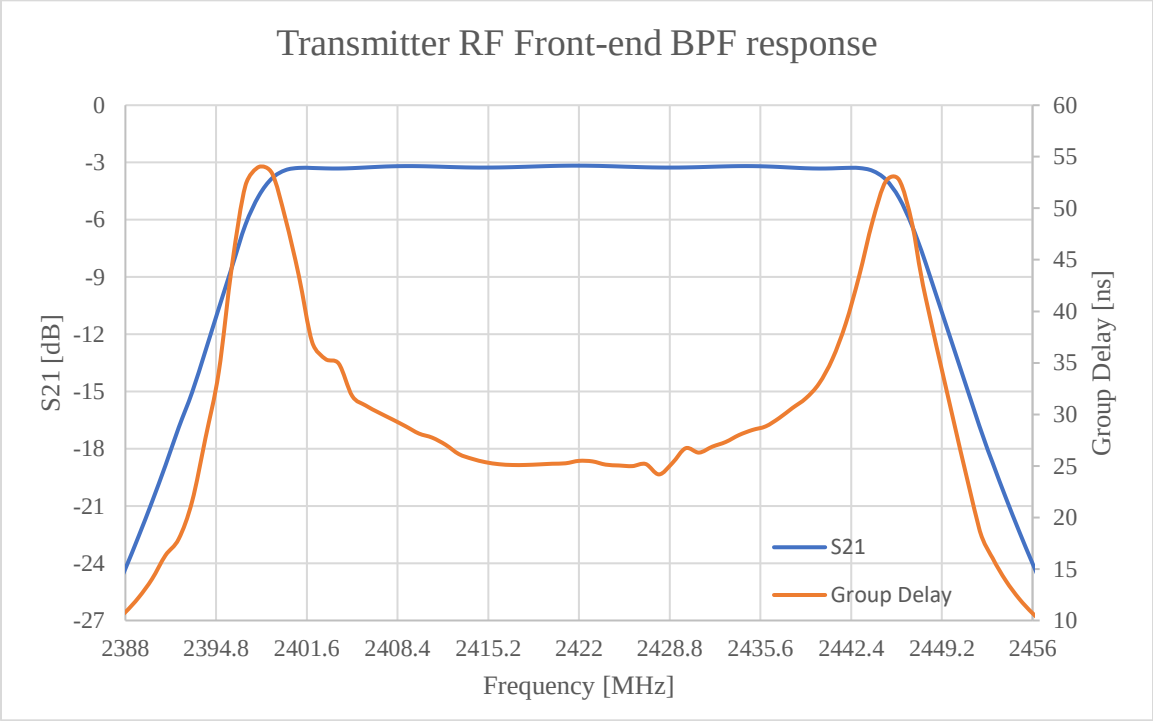

Figure 4.9: Transmitter RF front-end BPF response. 5th order Chebyshev filter; 0.1 dB bandwidth of 2400 – 2444 MHz.

The simulation test bench for the transmitter includes non-ideal factors such as the P1dB, IP3, IQ mismatch, and phase noise. IP2 is not simulated because it has little impact on the transmitter system, but impacts simulation time. The LO phase noise mask used in the transmitter simulation is -115 dBc at 100 kHz and -130 dBc at 1 MHz. Note, this phase noise mask is different from what is simulated in the receiver because higher-order QAM signals require higher performance than QPSK signals. This specification may be difficult to meet with a free-running VCO and my require a PLL or other LO designs that achieve improved phase noise performance. Finally, the IQ mismatch used is the same as in the the receiver simulation, 0.5 dB amplitude mismatch and 1° phase mismatch, likely requiring calibration of the transmitter.

As the average DAC output power is considered fixed, only the symbol rate is swept to determine the EVM performance for 16-, 32-, and 64-QAM in the transmitter. The resulting EVM performance is compared to the required EVM for each modulation calculated by Equations (2.3)

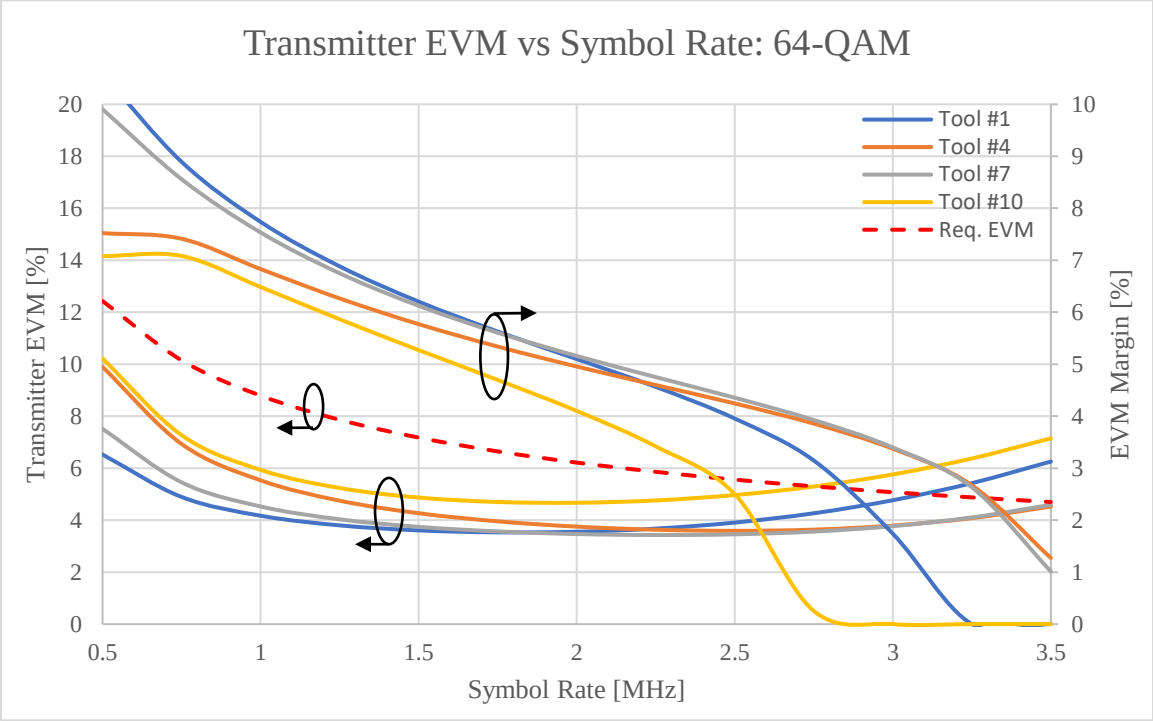

Figure 4.10: Transmitter EVM vs Symbol Rate for 64-QAM signals. DAC avg. output power = -10 dBm.

and (2.4) over the sweep range. Figure 4.10 illustrates the transmitter EVM performance for 64-QAM over the swept symbol rate. The degredation of performance at low symbol rates is caused by the phase noise generated by the LO, while the baseband filter affects the higher symbol rates. Tools #1 and #10 experience more distortion at higher symbol rates compared to the other tools due to the edges of the RF front-end BPF having large change in group delay. Tool #10 has an even high distortion relative to tool #1 due to low SNR caused by the higher attenuation of the coaxial channel. Remedies to this problem were predicted and discussed in Section 3.8. Considering an EVM of 4% or better at the surface receiver, the performance of the transmitter shows that 64-QAM symbol rates up to 12.0 MHz for tool #10, 2.7 MHz for tools #4 and #7, and 2.5 MHz for tool #1. This provides data rates of 12.0 Mbps, 16.2 Mbps, and 15.0 Mbps, respectively, and an overall uplink data rate of 151.2 Mbps, assuming that adjacent tools achieve similar performance to those shown. The 64-QAM constellation as transmitted by tool #4 at a symbol rate of 2.5 MHz is compared against the ideal constellation in Figure 4.11. The dominant impairment exhibited in the constellation is due to the phase noise, followed by the IQ mismatch and the filter group delay.

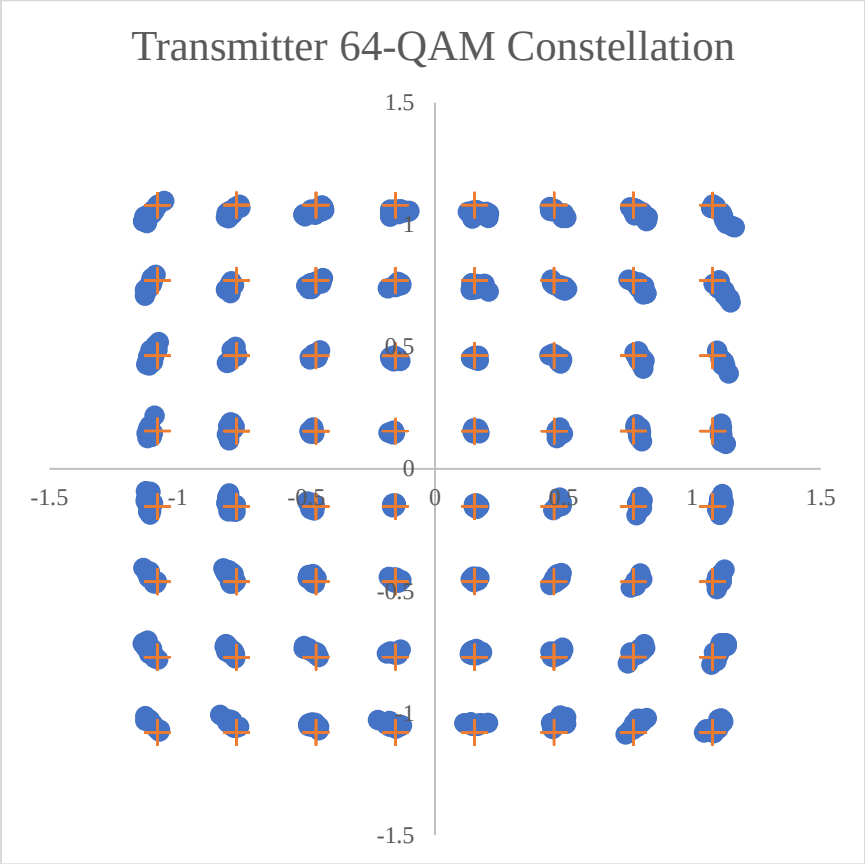

Figure 4.11: Transmitter 64-QAM Constellation. Measured for tool #4;
DAC avg. output = -10 dBm; Symbol Rate = 2.5 MHz.

The same simulation is performed for the transmitter using 32-QAM, as shown in Figure 4.12. The resulting EVM performance of the transmitter is similar to that of 64-QAM, but with the relaxed EVM requirements for 32-QAM, higher EVM margins are achieved. Again considering a 4% EVM overhead for the surface receiver, the symbol rates for tools #1, #4 and #7, and #10 are 3.3 MHz, 3.5 MHz, and 3.2 MHz, respectively. The data rates for each tool are then 16.5 Mbps, 17.5 Mbps, and 16.0 Mbps, and assuming similar performances for tools not shown, the uplink is capable of achieving an overall data rate up to 170 Mbps. This is better performance than achieved with 64-QAM; however, because tools #4 and #7 are operating at the maximum channel bandwidth, an incremental increase to the transmitter performance, or considering a better receiver performance, could allow 64-QAM to achieve higher data rates. The 32-QAM transmitter constellation for tool #4 is plotted in Figure 4.13. It is evident from the constellation that the filter

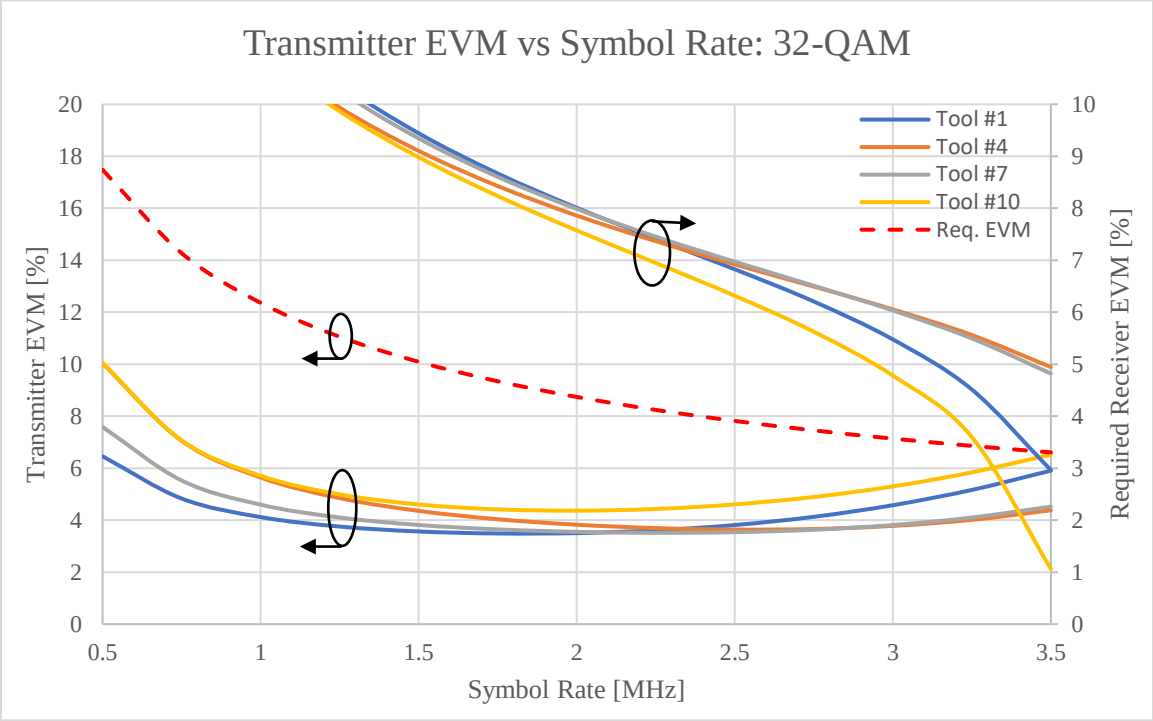

Figure 4.12: Transmitter EVM vs Symbol Rate for 32-QAM signals. DAC avg. output power = -10 dBm.

group delay has become the dominant ailment to the constellation and the phase noise is almost indisinguishable.

Continuing the analysis, the sweep is also performed for the transmitter using 16-QAM. As before, the transmitter EVM performance is similar 32- and 64-QAM, but the EVM margin has increased once again due to the relaxed requirements for 16-QAM. The results of the sweep are shown in Figure 4.15. All tools are capable of a symbol rate up to 3.5 MHz with an EVM margin greater than 6% resulting in data rates of 14 Mbps per tool and 140 Mbps for the entire uplink band. While this is lower than what is achieved with 32-QAM, the large margins for 16-QAM allow for a relatively large degredation in performance while maintaining sufficiently high data rates. The 16-QAM constellation at a symbol rate of 3.5 MHz as transmitted by tool #4 is illustrated in Figure 4.15. As with 32-QAM, the dominant distortion of the constellation is caused by the filter group delay. The IQ mismatch and phase noise have relatively little effect at this symbol rate.

A second sweep is performed for 16-QAM using the phase noise reported by [35] to investigate how much more phase noise can be tolerated by the system. The phase noise mask used

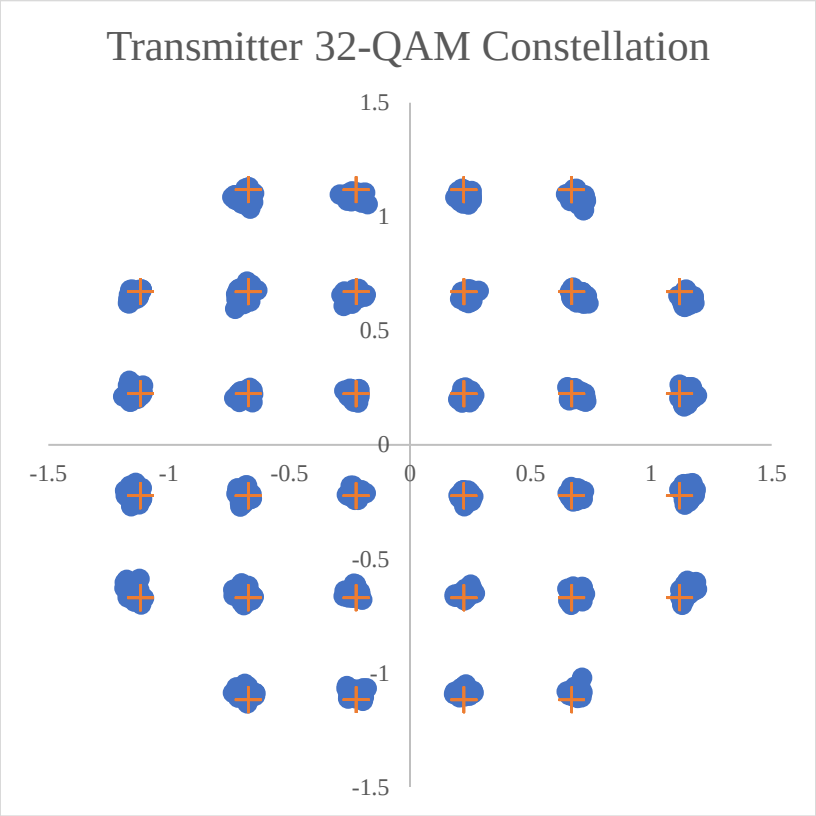

Figure 4.13: Transmitter 32-QAM Constellation. Measured for tool #4; DAC avg. output = −10 dBm; Symbol Rate = 3.5 MHz.

in the sweep is -100 dBc at 100 kHz and -115 dBc at 1 MHz, the same that was used to simulate the receiver performance in Section 4.2. The results of the sweep are graphed in Figure 4.16. From the graph, it can be seen the phase noise is too large to meet EVM requirements at low symbol rates, but the transmitters are still able to achieve a symbol rate of 3.5 MHz with approximately 5% EVM overhead for the receiver. This margin significantly improves to greater than 18% for QPSK over the entire sweep, supporting data rates up to 7 Mbps per tool. These results show the uplink channels can maintain high data rates with QPSK and 16-QAM using the current VCO design; although, to use 32- and 64-QAM an improvement in phase noise is needed. Comparing Figure 4.13 to Figure 4.11, it can be seen 32-QAM has more margin than 64-QAM for degraded phase noise from the mask used in the simulation. An improved phase noise can be accomplished by implementing a high-temperature PLL design or a fixed oscillator such as a dielectric resonator oscillator (DRO) using NP0 dielectrics.

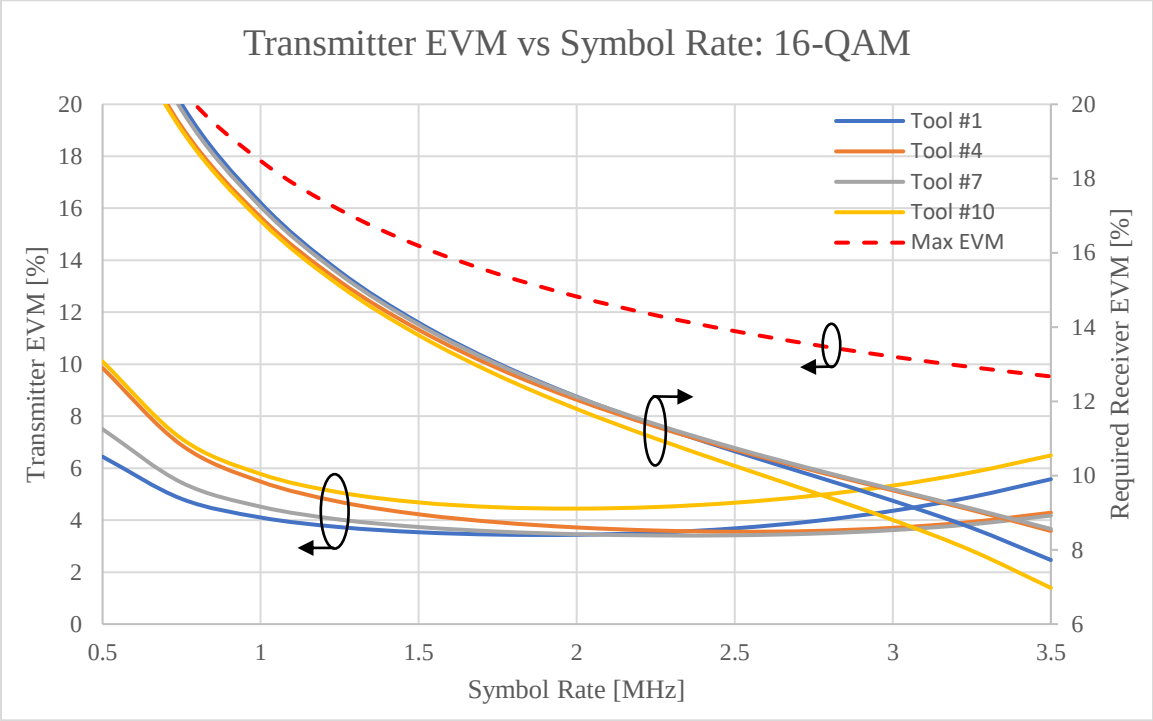

Figure 4.14: Transmitter EVM vs Symbol Rate for 16-QAM signals. DAC avg. output power = -10 dBm. Phase noise mask: -115 dBc at 100 kHz and -130 dBc at 1 MHz.

In conclusion, the transmitter system-level simulation shows the transmitter design is capable of supporting QPSK, 16-, 32-, and 64-QAM with atleast 4% EVM margin for the surface receiver perforance. As designed, the system acheives its maximum data rate of 170 Mbps with 32-QAM, but only small improvements are needed for 64-QAM to exceed the data rate provided by 32-QAM. For example, in order to make use of 64-QAM, the local oscillator must achieve low enough phase noise through the use of a PLL or dielectric oscillator. The system is also able to make use of the high-temperature VCO design intended for this system with QPSK and 16-QAM while maintaining a large enough margin for high data rates of 70 Mbps to 150 Mbps.

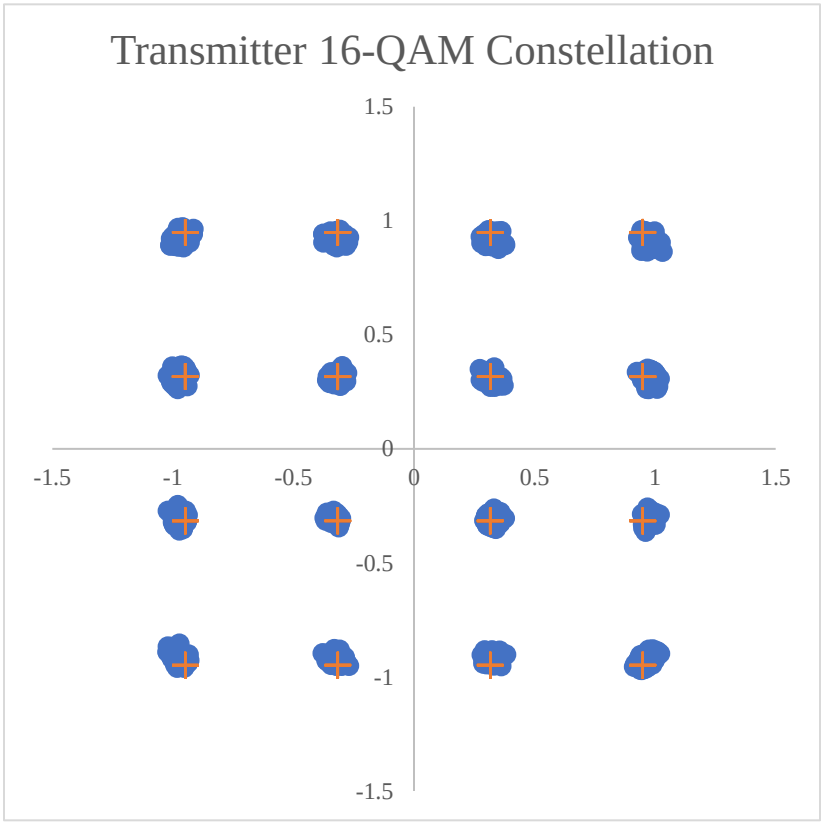

Figure 4.15: Transmitter 16-QAM Constellation. Measured for tool #4; DAC avg. output = −10 dBm; Symbol Rate = 3.5 MHz.

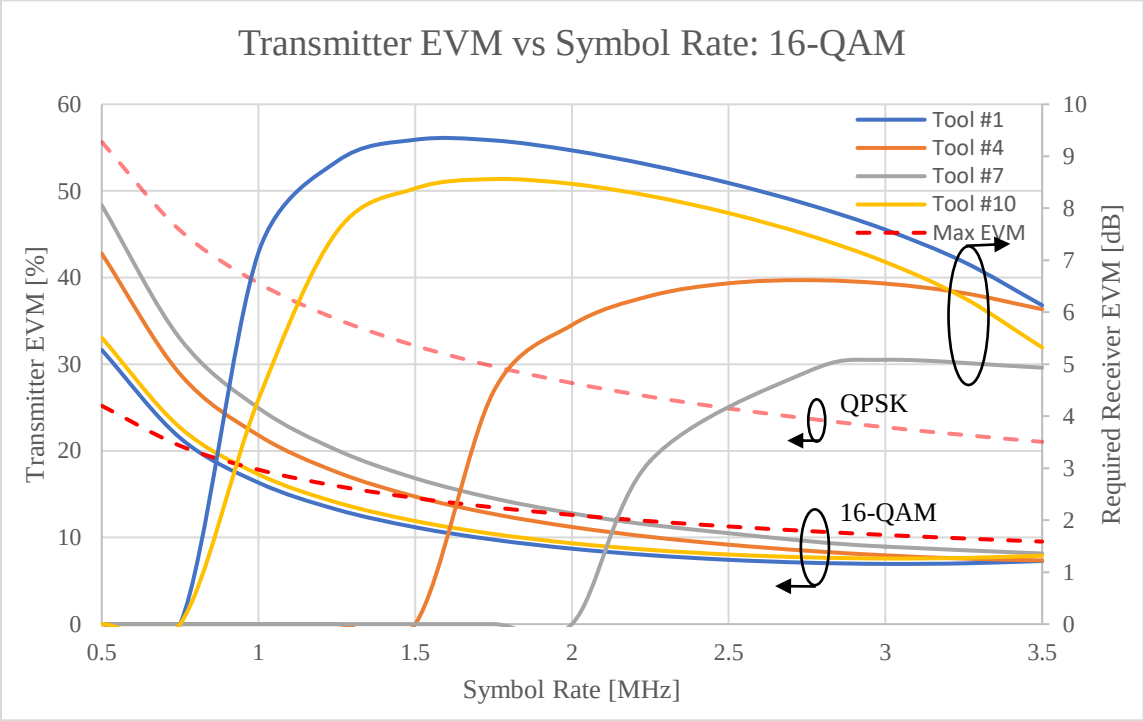

Figure 4.16: Transmitter EVM vs Symbol Rate for 16-QAM signals. DAC avg. output power = -10 dBm; Phase noise mask = -100 dBc at 100 kHz, -115 dBc at 1 MHz.

4.4 Effects of temperature

Because of the environment the transceiver design is intended, it is important to evaluate the effects temperature has on the system. The general trends of linearity, gain and noise figure are evaluated for the blocks that make up the transmitter and receiver. These trends are then input into the simulation test benches to evaluate how the performance of the system changes from 25℃ to 250℃. This analysis mainly focuses on the blocks which contain active devices since passive components that are insensitive to temperature can be designed or purchased as discussed in Section 2.5.

The temperature affect on the gain of high-temperature circuits is highly dependent on the active device, bias point selection, and impedance match. For the high-temperature technologies considered – GaN-SiC, SiC, and SOI – the transconductance, g_m, is affected over temperature by a reduction in the drain current and the threshold voltage. Plotting g_m versus the gate voltage and temperature reveals a gate voltage at which g_m is unchanging over temperature, this is referred to

as the zero temperature coefficient (ZTC) for g_m. Below this gate voltage, g_m will increase with temperature, while g_m decreases with temperature above it [14, 55]. Furthermore, the output impedance of the devices will change versus temeprature, affecting the impedance matching of the design. The matching can increase or decrease with temperature depending on the design. In the case of [15], the impedance matching was designed to initially improve with temperature and begin to decrease after a certain point causing the gain to peak at the center of the operating temperature.

The linearity of the active device is also expected to change over temperature. For this analysis, the trends for output and input P1dB points are considered and extended to the other metrics for linearity. The trend for OP1dB is to decrease with increasing temperature; however, the effect is as small as 0.5 dB/°C, as reported by [60]. It follows that the IP1dB will be affected by trends of both gain and OP1dB over temperature. The typical trend is that IP1dB will actually increase with temperature on the account that gain exhibits a larger decrease than OP1dB with increasing temperature. This is supported by [12, 14]; however, [9] shows a degredation of linearity, presumably due to a larger decrease of OP1dB compared to the increase of loss.

The trend of noise figure is highly dependent on the circuit design. It can depend on the trends of g_m, impedance match, and circuit topology, making it difficult to predict. According to [15], the general tendency is for NF is to increase with temeperature. This claim is supported by many other high-temperature circuits [12, 55].

The temperature dependence of the major blocks in the transceiver are assumed to exhibit the same general trends mentioned for gain, linearity, and NF. Because these parameters are highly dependent on the design of the block, the amount of shift with temperature for each of the parameters is assumed to be linear and is extracted from similar high-temperature circuits. The OP1dB, OIP3, OIP2 are assumed to decrease by approximately 2 dB over the temperature range. The gain of the blocks are assumed to decrease by a minimum of 2 dB for some blocks and as high as 5 dB for others. Input linearity figures are set to decrease or increase depending on the difference by which output linearity and gain change. Lastly, NF is set to increase by atleast 2-3 dB for each block.

The simulation for the receiver was set up the same as in Section 4.2 for the swept signal power. This simulation is chosen over sweeping the symbol frequency because it directly involves the changing gain, noise figure, and linearity. Figure 4.17 shows the results of the swept average

signal power for temperatures of 25℃, 125℃, and 250℃ at a symbol rate of 3.3 MHz. For reference, the traces for 250℃ are exactly the same as was simulated in Figure 4.5. As evident from the figure, the minimum EVM is not dependent over temperature. This is because the dominant distortion at this symbol rate, the group delay of the baseband filter, is assumed to be independent of temperature. The minimum detectable signal; however, increases with temperature as a result of rising thermal noise floor, increasing NF and decreasing gain all leading to decreased sensitivity at high-temperatures. As for the linearity, it can be seen the linearity of the receiver actually increases with the temperature. This is a result of a larger decrease in gain than the decrease of output linearity for the active devices. The total effect is an increase in the input linearity of the receiver. Additionally, the dynamic range – the difference between the maximum input signal power and minimum detectable signal – decompresses with temperature from 31.4 dB at 25 ℃ to 35.1 dB at 250℃. If some of the blocks were made to exhibit a peak gain at the center of the operating temperature range, as in [15], the minimum detectable signal at 125℃ would increase further while the linearity would decrease the maximum signal, compressing the dynamic range at 125℃.

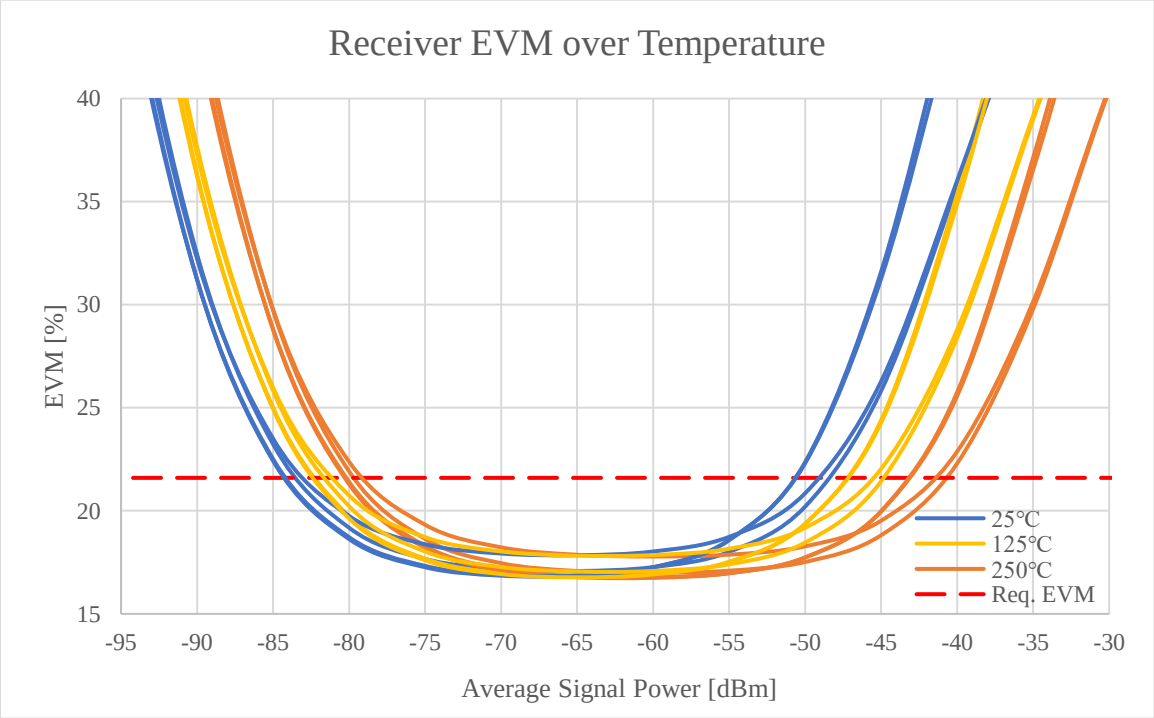

Figure 4.17: Receiver EVM performance vs avg. individual signal power and temperature for QPSK modulation. Symbol Rate = 3.3 MHz.

For simulating the temperature performance of the transmitter, the symbol rate for 64-QAM is swept. This is done because 64-QAM requires the highest performance and the sweeps for 32- and 16-QAM yielded similar EVM performance. Because the gain of the PA is set to decrease with temperature, the output power at the lower temperatures run the risk of saturating the receiver. The DAC output power is adjusted for each temperature to keep the output power a constant for this reason. In addition, [13, 35] show that the phase noise of the LO worsens over the temperature range. The results of the sweep for 25℃, 125℃, and 250℃ are illustrated by Figure 4.18, where the traces at 250℃ are the same reported by Figure 4.10. The figure shows the performance, aside from the worsening phase noise at low symbol rates, does not change much over the temperature range. This is an expected result considering the output power was compensated for the increase of gain and the filter characteristics do not change with temperature in the simulation.

The results from Figure 4.17 and Figure 4.18 illustrate how the transceiver might be expected to perform over the intended temperature range; however, because the temperature

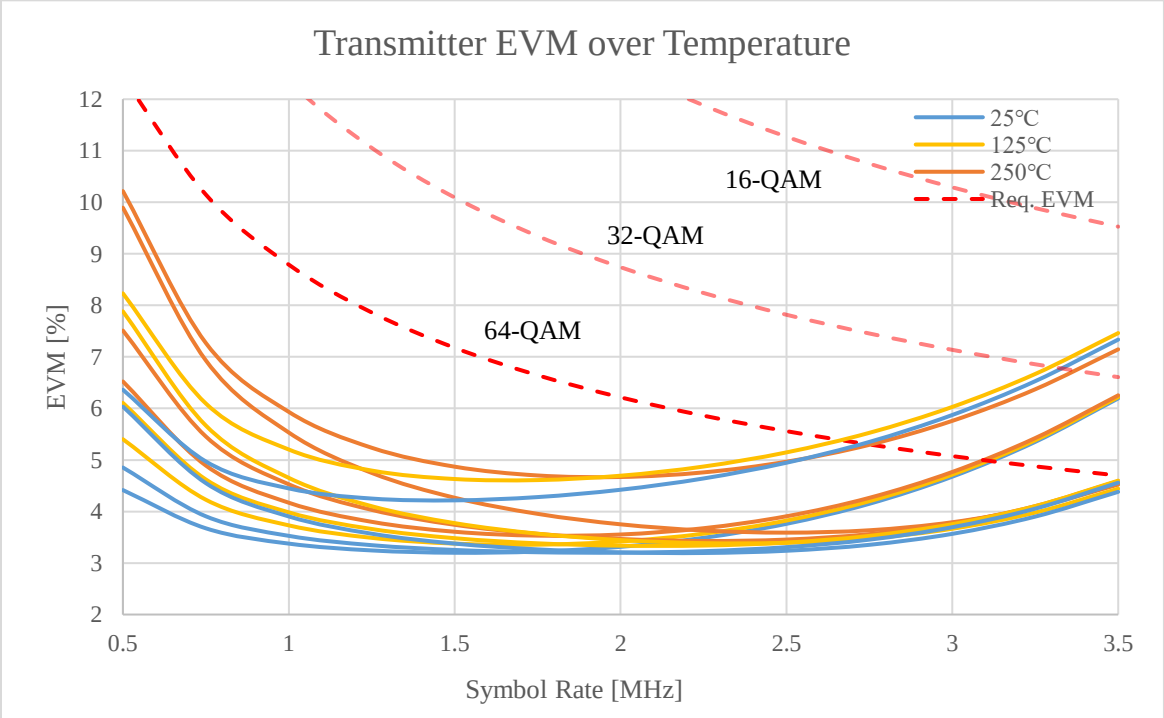

Figure 4.18: Transmitter EVM vs symbol rate and temperature. Measured for tool #4; PA output power = +6 dBm.

dependence for gain, noise figure, and linearity are deeply rooted in the design of the circuit, it is extremely difficult to predict without first choosing circuit topologies, bias points, and characterizing the chosen devices. However, some conclusions can be drawn from the simulation regarding the system design. First, the reduction in linearity of the receiver at 25℃ relative to 250℃ could become an issue due to the output power of the transmitter remaining the same, but the transmitter power cannot be reduced due to the sensitivity of the link. This indicates the isolation between the transmitter and receiver needs to be higher than specified. Second, because the sensitivity of the receiver is improved at 25℃ while linearity is degraded, the surface transmit power will have to be adjusted over the system temperature. Lastly, although it is not shown, the linearity of the transmitter is expected to decreases with increasing temperature as a result of the decreasing of output linearity of the device.

4.5 Chapter Summary

In this chapter, the AWR VSS simulator was used to simulate and analyze the transmitter and receiver performance as it was designed in Chapter 3. AWR was chosen as the simulation software for its efficiency and effectiveness at simulating radio systems. The receiver simulation environment was described and the EVM performance of the receiver was evaluated for QPSK over the symbol rate and average signal power. The results proved promising as the receiver performance exceeded the required design specifications and achieved 68 Mbps downlink data rates. Next, the transmitter simulation environment was described, this time evaluating the transmitter performance for 16-, 32-, and 64-QAM versus the symbol rate. The higher order QAM signals require high performance LO phase noise, but 16-QAM and QPSK have significant enough margin to tolerate moderate phase noise. The transmitter design acheives high uplink data rates of 170 Mbps and meets design specifications. Lastly, the effect temperature has on blocks of the system are evaluated and simulated in both the transmitter and receiver.

Chapter 5

Conclusion and Future Work

5.1 Conclusion and Summary

This work narrates the full design of a 2.4 GHz high-temperature transceiver intended for operation up to 250°C. The transceiver utilizes QPSK, 16-, 32-, and 64-QAM to support high data rates along with FDMA for simultaneous full-duplex communication. The individual blocks making up the transceiver were specified to meet the minimum specifications required to accomplish the goals of the system, providing circuit designers flexibility in the trade-off between power consumption and performance. The simulated performance achieved by the transceiver is summarized in Table 5.1. The transceiver is capable of achieving uplink data rates of 170 Mbps and downlink data rates of 68 Mbps across all 10 channels.

Chapter 3 oversaw the derivation of the overall system specifications and the subsequent allocation of the individual blocks of the system. Each consideration driving gain, noise figure, linearity and filter requirements were discussed. Additional considerations and guidance for the discrete and IC implementations, as well as the surface transceiver, were mentioned.

Table 5.1: Summary of transceiver performance

Transceiver Performance Summary			
Parameter		**Receiver**	**Transmitter**
Temperature		25°C - 250°C	
Number of Tools		10	
Frequency Range		2456.0 MHz – 2500.0 MHz	2400.0 MHz – 2444.0 MHz
Gain		45 - 75 dB	16.0 dB
NF	P_{out}	12.5 dB	14 dBm
IP1dB	OP1dB	-32 dBm	19.3 dBm
IIP3	OIP3	-23.8 dBm	28.3 dBm
IIP2	OIP2	-13.8 dBm	-
Dynamic Range		28.4 dB	-
EVM [Bit Rate per tool]		QPSK: 21% [6.8 Mbps]	16-QAM: 4.1% @ P_{out}=+6 dBm; [13.2 Mbps] 32-QAM: 4.1% @ P_{out}=+6 dBm; [17.5 Mbps] 64-QAM: 3.6% @ P_{out}=+6 dBm; [16.2 Mbps]
BER		$\leq 10^{-6}$	$\leq 10^{-6}$

Chapter 4 presented the simulation of the transceiver performance for each modulation over the symbol rate, signal power and temperature. The general trends of gain, linearity, and noise figure of the system blocks over the temperature range were evaluated and estimated. While difficult to accurately predict the actual transceiver performance over temperature, the simulation provided insight to considerations that would otherwise have gone unnoticed.

5.2 Future Work

This work serves as the foundation supporting a large quantity of future work. First, each block discussed in this work – the diplexer, band-pass filters, power divider/combiner, LNA, quadrature mixers, active and passive baseband filters, VGA, and PA – must all be designed for the discrete implementation of this system and subsequently tested. Following the design and verification of each block against the system spec, each of the block designs are to be integrated onto a single PCB. This complete system must then be validated against design specifications.

Along side the discrete design, it could prove fruitfull to investigate a high-temperature PLL or other oscillator design to improve upon the VCO phase noise. Improved phase noise for a high-temperature 2.4 GHz oscillator is required to enable use of 32- and 64-QAM in the transmitter.

Further in the future, this system design is intended to be implemented as a MMIC in GaN-SiC technology or RFIC in SOI technology. This will begin the design process back at the block level, with each block taking inspiration from lessons learned in the discrete implementation.

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