High-Frequency and High-Performance VRM Design for the Next Generations of Processors

by

Kaiwei Yao

Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

Fred C. Lee, Chairman

Dushan Boroyevich

Alex Q. Huang

Guo-Quan Lu

Yilu Liu

April 14, 2004
Blacksburg, Virginia

Keywords: power management, voltage regulator module, high frequency

High-Frequency and High-Performance VRM Design for the Next Generations of Processors

by

Kaiwei Yao

Fred C. Lee, Chairman

Electrical Engineering

(ABSTRACT)

It is perceived that Moore's Law will prevail at least for the next decade with the continuous advancement of processing technologies for integrated circuits. According to Intel's roadmap, over one billion transistors will be integrated in one processor by the year 2010; the processor's clock speed will approach 15 GHz; the core static currents will increase up to 200 A; the dynamic current slew rate will rise up to 250 A/ns; and the core voltage will decrease to 0.8 V. The rapid advancement of processor technology has posed stringent challenges to power management for both an efficient power delivery and an accurate voltage regulation.

The primary objectives of this dissertation are to understand the fundamental limitations of the state-of-the-art solution for the power management, and hence to support possible solutions for meeting the power requirement of the next generations of processors.

First, today's voltage-regulator module (VRM) design, which is based on the multiphase interleaving buck topology, is thoroughly analyzed. The analysis results of the control bandwidths versus the VRM transient voltage spikes highlight the trend of high-frequency VRM design for smaller size and faster transient response. Based on the concept of achieving constant VRM output impedance, design guidelines are proposed for different kinds of control methods. However, the high switching-related losses in the conventional multiphase buck converter limit

its further applications. This dissertation proposes a series of new topologies in order to break through the barriers by applying an inductor-coupling or autotransformer structure to reduce the switching-related losses by extending the duty cycle. Then, this dissertation pushes the topology innovation further by introducing soft-switching quasi-resonant converters for the VRM design. The combination of the quasi-resonant and active-clamped concepts derives a family of new converters, which can eliminate all the switching and body-diode losses. The experimental results at 1-2MHz switching frequencies prove that the proposed solutions for the VRM design can realize very high efficiency and high power density.

To my parents

Qingzhou Yao and Yaxian Xie

And to my wife

Rao Shen

Acknowledgments

I would like to express my sincere appreciation to my advisor, Dr. Fred C. Lee, for his guidance, encouragement and support. Dr. Lee's extensive vision and creative thinking have been the source of inspiration for me throughout this work. It was an invaluable learning experience to be one of his students. From him I have gained not only extensive knowledge, but also a careful research attitude.

I am grateful to my committee members, Dr. Dushan Boroyevich, Dr. Alex Q. Huang, Dr. Guo-Quan Lu and Dr. Yilu Liu, for their valuable suggestions and help.

It has been a great pleasure to work in the Center for Power Electronics Systems (CPES). I would like to acknowledge the CPES administrative and management staff, Ms. Ann Craig, Ms. Linda Gallagher, Ms. Teresa Shaw, Ms. Elizabeth Tranter, Ms. Trish Rose, Ms. Marianne Hawthorne, Ms. Michelle Czamanske, Mr. David Fuller, Mr. Robert Martin, Mr. Steve Z. Chen, Mr. Dan Huff, Mr. Gary Kerr and Mr. Jamie Evans, for their countless instances of help.

I would like to thank my teammates in the VRM group, Dr. Xunwei Zhou, Dr. Pitleong Wong, Dr. Peng Xu, Dr. Ming Xu, Dr. Bo Yang, Mr. Jia Wei, Mr. Mao Ye, Mr. Jinghai Zhou, Ms. Li Ma, Mr. Yuancheng Ren, Mr. Yu Meng, Mr. Yang Qiu, Mr. Kisun Li, Mr. Doug Sterk and Mr. Xing Zhang. It was a pleasure to work with such a talented, hard-working and creative group.

My heartfelt appreciation goes toward my parents, who have always encouraged me to pursue higher education. With much love, I would like to thank my wife, Rao Shen, who has always been there with her love and encouragement.

This work was supported by the VRM consortium (Intel, IBM, Delta Electronics, Texas Instruments, ST Microelectronics, National Semiconductor, Intersil, TDK, Hitachi, Hipro, Power-One, Infineon and Artesyn). Also, this work made use of ERC shared facilities supported by the National Science Foundation under Award Number EEC-9731677.

Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

1.1. Research Background

In 1965, just six years after the invention of the integrated circuit (IC), Gordon Moore predicted the annual doubling of the number of transistors on an IC [A1]. In the late 1980s, the doubling speed was adjusted to every 18 months for the expected increases in the complexity of semiconductors [A2]. Moore's Law, as it came to be known, has held sway for nearly four decades, supported by the industrial silicon engineering and manufacturing engine. The emerging nanotechnology will ensure that Moore's Law continues to prevail for at least the next decade, with continuous advancements in processing technologies for very-large-scale integration (VLSI) [A3-A6]. According to Intel's roadmap [A6], as shown in Fig. 1.1, over one billion transistors will be integrated in each processor by the year 2007, as compared to today's integration of 55 million transistors in a Pentium IV processor.

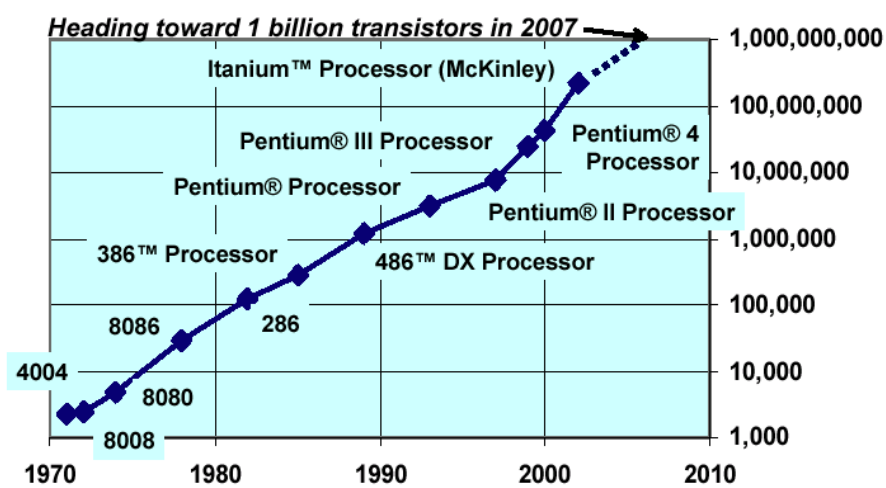


Fig. 1.1. Intel's roadmap of the number of integrated transistors in one processor.

The rising device counts, while breathtaking, are just the tip of the iceberg. Silicon's power – and its uniqueness – is that nearly all parameters of microprocessor technology improve as transistor counts climb. For example, speed and performance have ascended even more sharply than has the number of transistors. The i486 processor ran at 25 MHz. Today's Pentium IV processors run at 2.20 GHz, and this is rising. The predicted billion-transistor processor will likely run at speeds approaching 20 GHz. Fig. 1.2 clearly shows this developing trend.

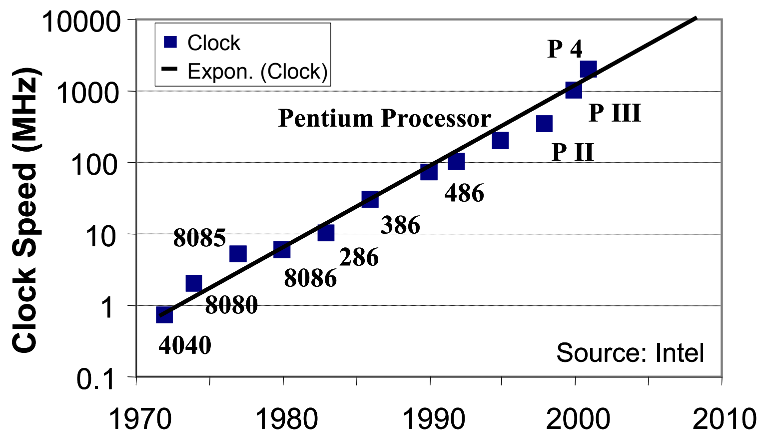


Fig. 1.2. Intel's roadmap of the processor clock speed.

However, as transistor count increases, processors consume more power and generate more heat, at an accelerating rate. Fig. 1.3 shows Intel's roadmap for the processor's required current and voltage. Although the supplied voltage is going to drop to a level of 0.7 V, the total power consumption keeps flying up because of the tremendously increased current. It was predicted that a single processor would consume over 1KW/cm^2 power in 2010 by following silicon's developing trend of the last 30 years [A7-A8]. The chip temperature would reach as high as that of a rocket nozzle. Moore's Law eventually will have to confront the laws of physics -- in this case, those of power and thermal limitations. This phenomenon is often referred to by Intel as the "power wall."

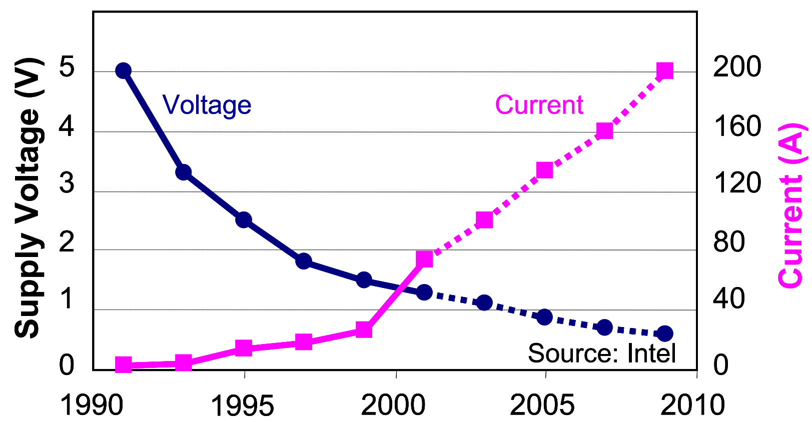


Fig. 1.3. Intel's roadmap for the processor's required voltage and current.

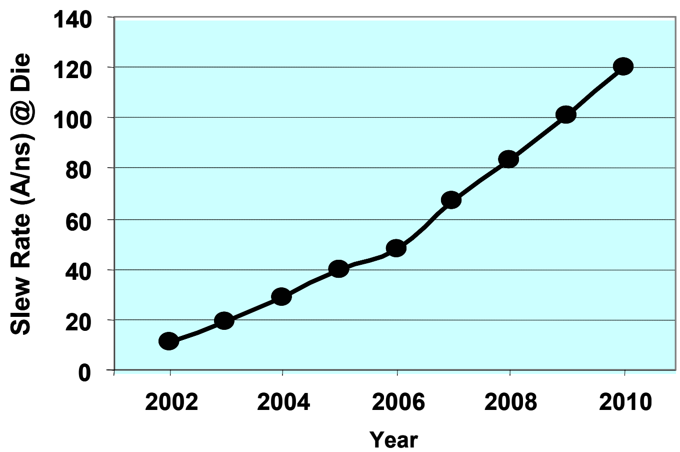


Fig. 1.4. Intel's roadmap for the processor's maximum current slew rate.

The sub-1V supplied voltage for the processor raises another serious challenge for voltage regulation. The allowed voltage regulation window becomes narrower for the effective "1" or "0" identification. Furthermore, the high clock frequency induces very fast di/dt (the current slew rate) when the microprocessor operation changes from the sleep mode to the power mode and vice versa [A9-A11]. The rate of change between these modes is no less than 1,000 times per second – much faster than your finger can move on a keyboard. Fig. 1.4 shows this developing trend. The high dynamic characteristic makes accurate voltage regulation more difficult.

Overall, power management technology is very important for breaking the "power wall," and for efficient and accurate delivery of power to the processor. If these power challenges are not resolved, the familiar trend of smaller, faster, lower-cost processors and devices could be compromised. Futuristic applications such as real-time speech and facial recognition – applications requiring far more powerful processors than today's – might never be realized. The growth of computing and communications products could slow. Successfully managing the power issue is fundamental to successfully extending Moore's Law.

1.2. State-of-the-Art Technology

For a 386 or 486 processor, a traditional centralized power supply (silver box) is sufficient to deliver all the power needed. The silver box also supports power to the memory chip, video card and other parts in the computer. When the Pentium processors emerged in the late 1990s, the centralized power systems no longer met their power requirements because of their lower operating voltages and higher clock frequencies. The physical distance from the silver box to the processor is too long, which limits the power transfer speed. Consequently, the supply voltage invariably fails to deliver the required voltage regulation. To make this matter worse, as the processor technologies have advanced, the total voltage tolerance has become much tighter -- from a tolerance of 5% for the 3.3V Pentium II to a voltage tolerance of 2% for the 1.3V Pentium IV processor. Thus, a delicate power supply, the voltage regulator module (VRM), is required. And it must be placed in close proximity to the processor in order to reduce the impedance associated with the power delivery path [A12-A13]. Fig. 1.5 shows a layout with a VRM and a processor together. The power for other parts in the computer is still supplied by the silver box.

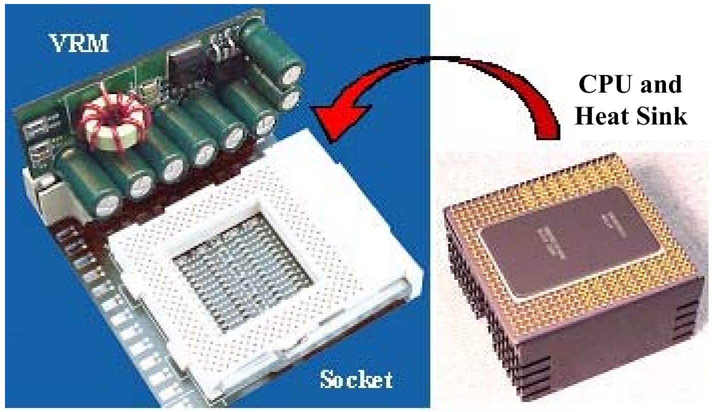


Fig. 1.5. The VRM for Pentium processors.

The original version of the VRM that accompanied the Pentium II was made up of a simple 5V-input buck converter. However, this approach was unable to meet the power requirement for the Pentium III processor, in which the operating voltage was drastically reduced from 2.8 V to 1.5 V, the current was increased from 10 A to 30 A, and the current slew rate was increased from 1 A/ns to 8 A/ns [A12]. Fig. 1.6 shows a buck converter designed for a Pentium III processor. Several devices are paralleled in order to handle the large output current. The bulk capacitor is used for energy storage, and the decoupling capacitor is nearer to the processor in order to limit the transient voltage spike. To meet the ±2% voltage regulation specification, it was deemed necessary to increase the decoupling capacitor by a factor of 23 and the VRM bulk capacitor by a factor of 3 [A14-A15]. This is not a practical solution, for two reasons. Firstly, there is simply not enough real estate in the motherboard to accommodate such a large increase in the number of capacitors. Secondly, the cost increase would also be significant.

The excessive increase in the number of output filter capacitors is mostly due to the use of a relatively large output filter inductor in the single-phase buck converter, which is required to reduce the output current ripple. During the transient period, this large inductor limits the energy transfer speed of the VRM such that the capacitor alone must discharge its stored energy to the load. The capacitance must be large enough to contain the output voltage level within the required regulation window.

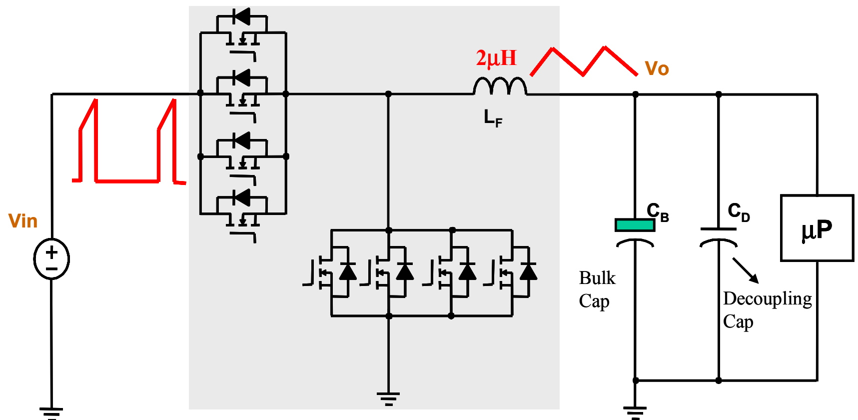


Fig. 1.6. A single-phase buck converter for a Pentium III processor.

To overcome this fundamental limitation, it was necessary to reduce the VRM output filter inductance. If the output filter inductance was reduced by one order of magnitude, that is, from 2-4 µH to 200 nH, the transient response would meet the 2% tolerance requirement without necessitating an increase in the usage of capacitors [A15]. However, there are two major disadvantages to using a smaller inductor. The first is that the small inductor results in much larger current and voltage ripples in the output, which is not acceptable. The second disadvantage is that the VRM efficiency is dramatically reduced due to the much larger current ripple.

Subsequently, in early 1997, CPES at Virginia Tech proposed a multiphase solution for the VRM. Instead of paralleling a number of transistors to improve circuit efficiency, as shown in Fig. 1.6, the team proposed the use of a number of mini-converter cells in parallel, as shown in Fig. 1.7. Each cell utilizes an inductor that is about 1/10 the size of the original. As a result, these mini-converter cells can quickly and efficiently transfer power to the microprocessor. Furthermore, these cells are controlled by phase-shifting their clock signals. The proposed interleaving approach not only results in cancellation of the current ripple generated at the output of each converter cell, but also increases its effective ripple frequency, and thus reduces by a factor of 10 the output filter capacitor requirement. In the same way, the interleaving approach can also significantly reduce the input filter capacitor requirement. In 1997, the immediate benefits of using the multiphase approach were demonstrated in the prototype hardware, which showed a sixfold improvement in power density, a threefold reduction in profile, and a fourfold improvement in its transient response [A15].

Not only can the multiphase approach improve the VRM transient response, but it can also benefit the thermal design because of its current distribution. Its power scalability characteristics make it very attractive in terms of its ability to keep step with the future microprocessor power management design. As a result, industry quickly adopted this solution. A number of companies (National Semiconductor, Semtech, Intersil, Maxim, Linear Technology, Analog Device, Fairchild Semiconductor, Texas Instruments and STMicroelectronics) have developed their IC controllers to facilitate the implementation of the proposed multiphase approach. Fig. 1.8 shows some examples.

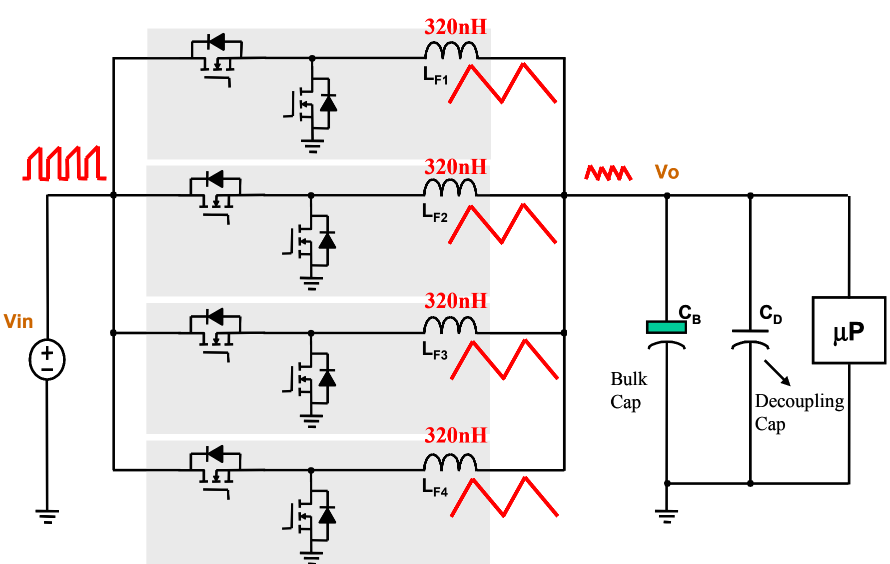


Fig. 1.7. A multiphase buck converter for a Pentium III processor.

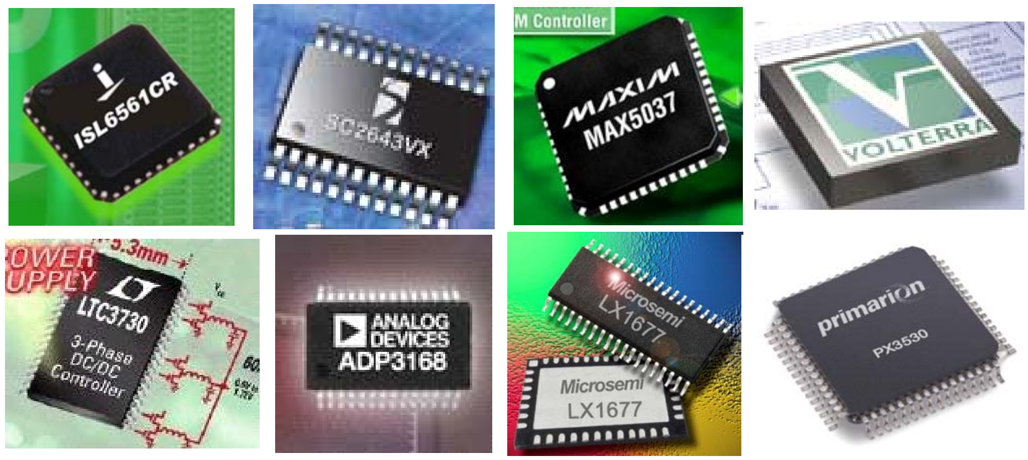


Fig. 1.8. Multiphase controllers from different companies.

The multiphase approach can be extended to power a Pentium IV processor, in which the operating voltage was reduced to 1.3 V and the current was increased to 90 A [A16-A28]. The input bus voltage was changed from 5 V to 12 V in order to reduce the bus conduction loss. Today, the multiphase VRM is adopted in every computer that uses the new-generation Pentium III and Pentium IV processors. Fig. 1.9 shows a typical structure with a plug-in version of a VRM. Fig. 1.10 shows the power delivery path with the voltage regulator on board. The following items summarize the state-of-the-art technologies for the current Intel VR 10 solution.

- Multiphase to distribute the large output current
- Interleaving to cancel current ripple and to improve transient response
- 12V-input voltage bus to reduce the input bus conduction loss
- 300KHz to 500KHz switching frequency to achieve reasonable efficiency with 30V vertical trench MOSFETs
- Analog multiphase controller with switching frequency up to 1 MHz
- Several Oscon bulk capacitors in parallel to limit the transient voltage spikes
- Powder iron inductors built with toroid core to reduce the cost

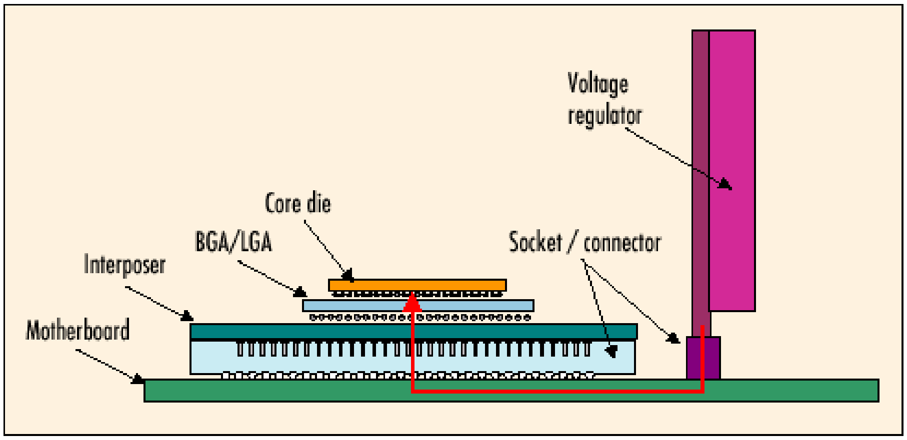


Fig. 1.9. Current system architecture for voltage regulator module and processor.

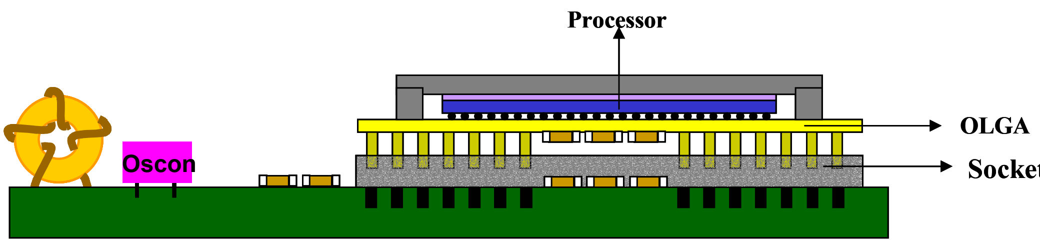


Fig. 1.10. The current power delivery structure for voltage regulator and processor.

1.3. Technology Barriers for Future Power Management

Following Intel's roadmap in Figs. 1.1, 1.2 and 1.3, in 2010 the processor will run at 20GHz clock frequency with over one billon transistors packed on a piece of silicon the size of your fingernail. It will require more than 200A current at a voltage level of around 0.7 V [A10-A11]. It is also expected that the processor die transient current will move toward 250 A/ns, which is about a tenfold increase over today's fastest processor [A29]. It is very difficult to apply today's multiphase buck topology and the power delivery structure to meet the power requirements of the next decade of processors.

The direct problem is how to keep the output voltage within the ±2% tolerance range, which is a regulation window of only about ±15 mV. Furthermore, the voltage must maintain accuracy in such a huge current transient change with very fast di/dt speed. The current VRM design will employ large numbers of output electrolytic capacitors -- approximately 168,000 μF -- which is about 2.5 times the level used today, and five times the number of decoupling capacitors (ceramic capacitors with low equivalent serious resistance [ESR]) in order to meet the processor requirement. Fig. 1.11 shows the requirements. Fig. 1.12 shows the significant cost penalty. Fig. 1.13 shows that today's VRM has already occupied about 12% of the motherboard real estate. It is impossible to put so many bulk capacitors and decoupling capacitors on the motherboard. The major reason for so many electrolytic (Oscon) capacitors is their high levels of ESR, which results in large transient voltage spikes. Although the ceramic capacitor has a smaller ESR, it has a limited capability to store energy for supplying transient power to the microprocessor. The VRM must be able to operate at significantly higher switching frequencies in order to reduce this energy storage requirement. It is predicted that when the VRM is operated at 2 MHz, only 1500μF output capacitance is required, in comparison to the 6000 μF that is required when the VRM is operated at 500 kHz [A30]. With today's high-density ceramic capacitor technology, only 15 capacitors are required, each of which has a footprint as small as 3.2mm×2.5mm. Considering the development of ceramic capacitor technology, it is very likely that the output capacitor size will be further reduced. Another significant benefit of high-frequency applications is the small size of the output filter inductors, which also occupy too much room in today's VRM design.

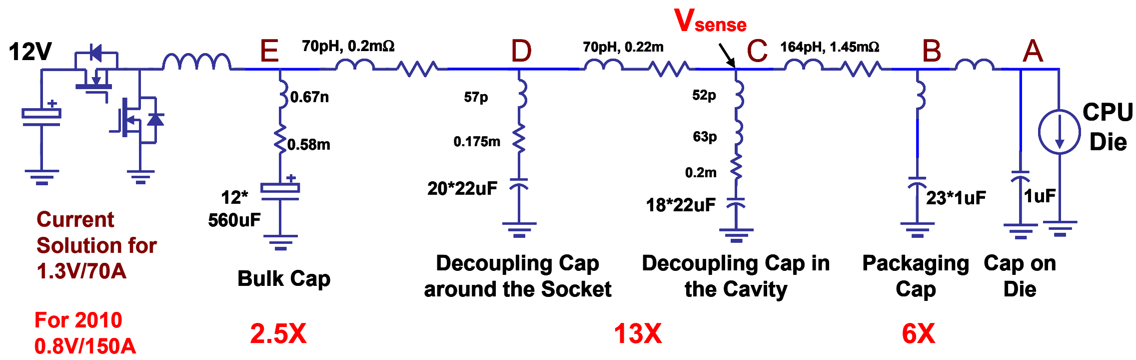


Fig. 1.11. The required output capacitors for current and the next generation microprocessors.

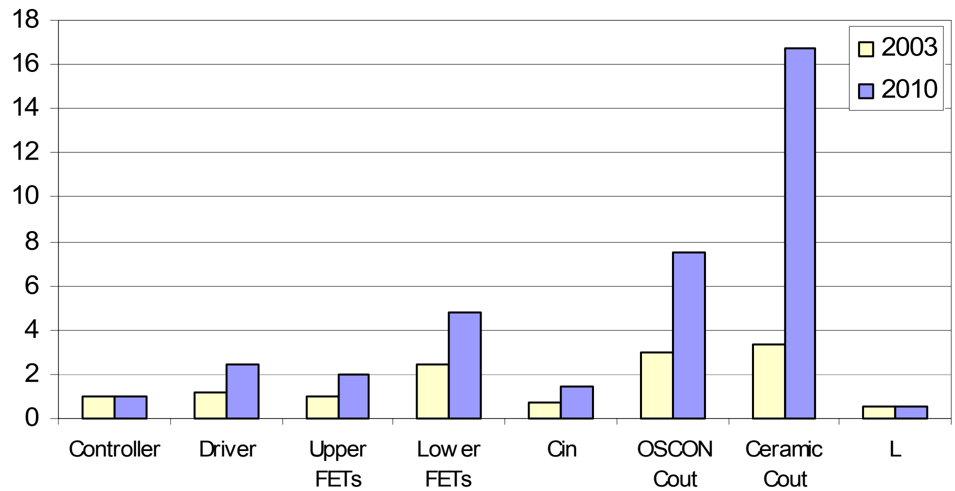


Fig. 1.12. The cost breakdown of VRM for current and the next-generation microprocessors.

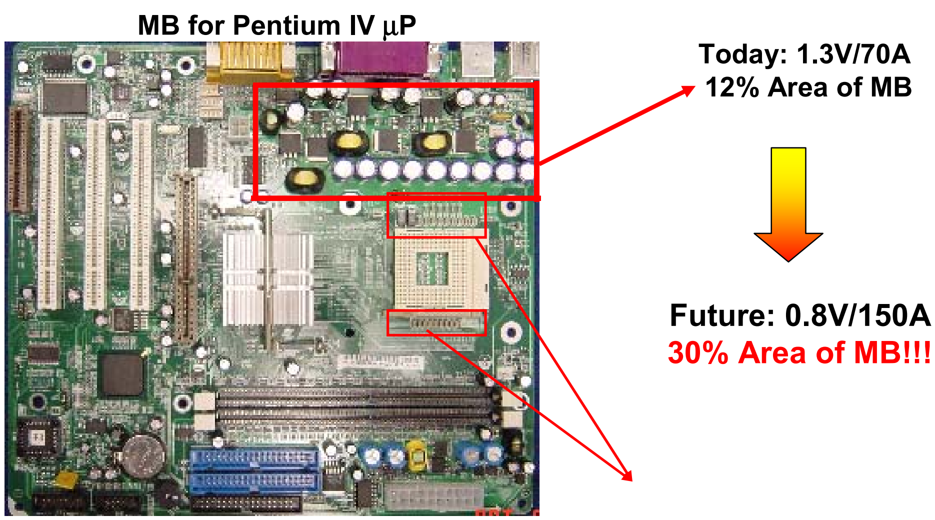


Fig. 1.13. A Pentium IV motherboard that includes a three-phase VRM.

However, high-frequency operation of the VRM raises thermal issues. Delivering the 200A current has already introduced severe conduction losses. When combined with the significant switching losses at the MHz operating frequencies, the industry's ability to economically cool the VRM would be surpassed. As a result, high-efficiency, high-power-density, fast-transient VRMs are critical for meeting the power requirements of the next generation of processors.

Another problem is related to the system's power architecture. Fig. 1.9 shows a typical structure with a plug-in version of a VRM. The power delivery path, which includes the printed circuit board (PCB) trace, central processing unit (CPU) socket, interposer layer and ball grid array (BGA) and land grid array (LGA) interconnects, accounts for about 1.1mΩ parasitic resistance and 120pH parasitic inductance [A31]. For future processors that require over 200 A and a slew rate of 250 A/ns, these interconnect parasitics alone will produce 44W power loss. The interconnect parasitics also result in a significant potential drop, such that the expected output voltage regulation window cannot be met for the next generation of processors. According to Intel's research on packaging [A32], the parasitics must be reduced by about 10 times to meet future requirements. The bottleneck is the CPU interconnect socket, which is responsible for 90% of the total parasitics. Intel has already devoted significant resources toward improving the system packaging [A32-A34].

At the same time, the improvement of the system power architecture achieved by omitting the CPU socket also calls for high-efficiency, high-power-density VRMs. The VRM must have a small size so that it is physically compatible with a processor in order for them to be packaged together in a certain way. Since the VRM is so close to the processor, its power loss will burden the processor's thermal design, the heat dissipation of which has already been problematic.

Based on these power management-related issues, it is very clear that high-efficiency, high-power-density, fast-transient VRMs are critical for meeting the power requirements of future advanced microprocessors. To achieve this target, the following technology challenges should be addressed.

1. Fundamental research on the VRM transient response must be carried out. Many papers have been published based on different models and software simulations [A35-A44]. However, many issues still need to be clarified; for example, the designs related to the control bandwidth, multiphase inductors and output capacitors. Since the processor continues to evolve, the VRM design is a moving target that calls for a design methodology.
2. Advanced power semiconductor devices also raise questions. Currently, vertical trench MOSFETs are widely used in VRM design, and industry has put a lot of effort into improving their performance. One aspect of these improvements is novel power device structure; for example, the Power JFET transistor from Lovoltech [A45-A46] and the junction barrier-controlled Schottky field effect transistor (JBSFET) from Silicon Semiconductor Corporation (SSC) [A47-A48]. The second aspect is device packaging. In order to further reduce the packaging and interconnection losses, significant efforts have been devoted to chip-scale packaging. Fairchild's bottomless and BGA packaging, Hitachi's lead-free packaging (LFPAK), International Rectifier's FlipFET and DirectFET, Siliconix's PowerPAK package, and STMicroelectronics's PowerFLAT package are a few examples of the advanced products currently available in the market. Not only can the chip-scale packaging technique reduce the conduction losses, but it can also reduce the parasitic inductance [A49-A50]. Another potential approach for improvement involves greater

device integration. Recently, IR, Philips, On-Semiconductor and Intersil have introduced the DrMOS technique, which packages together the power devices (the top and bottom switches) and the gate driver to form a surface-mounted chip [A51]. IR went a step further by packaging some high-frequency ceramic capacitors inside the chip (iP2002) to improve the performance. Volterra adopted the lateral power MOSFET process to monolithically build its DrMOS. Some simple control functions are also integrated. The DrMOS technology significantly improved performance by reducing the parasitics. CPES has pushed the integration envelope further by integrating the multiphase voltage regulator (VR) into one silicon die, based on a lateral process [A52]. There are still many areas open for research into power device improvement.

3. Advanced VRM topologies offer potential. Improving efficiency would involve the use of some other topologies, which are better than the buck converter in high-frequency applications. These topologies should feature less switching-related losses (such as turn-on and turn-off losses), lower body diode reverse-recovery loss, and reduced body diode dead-time conduction loss. Also, these topologies should maintain the benefits of simple gate drive, simple multiphase control scheme, easy magnetic component implementation, and low cost. CPES has done tremendous work to improve the efficiency at the MHz-switching-frequency range. The research runs the gamut from pulse-width modulation (PWM) hard-switching topologies to resonant soft-switching ones; from 48V-input isolated topologies to 12V-input non-isolated ones; from single-stage topologies to two-stage ones; and from externally driven topologies to self-driven ones [A54-A57].
4. An advanced gate drive scheme is also important. With multi-MHz switching frequencies, the gate drive loss will turn out to be significant, especially for high-output-current

applications in which more power MOSFETs are paralleled. This situation not only degrades efficiency, but also pushes the gate drivers to their thermal limitations. Gate drivers have already been a hot spot in the VRM design, and this will be even worse in the future. The drive voltage level complicates the issue further. A higher drive voltage level means smaller device conduction loss but more gate drive loss. The challenge is to make this trade-off yield an optimal VRM design. Also, the gate drive dead-time control is very important for avoiding shoot-through problems while minimizing body diode conduction loss in the synchronous rectifiers. As a result, some advanced gate drive schemes with less drive loss can significantly benefit the VRM design. TI proposed the predictive drive scheme to minimize the dead time so that the body diode conduction loss can be minimized [A58]. CPES proposed some preliminary research work that involves utilization of the resonant gate drive to reduce the drive loss [A59].

5. Fast transient response requires advanced control methods. A number of innovative solutions have been developed and commercialized; for example, the enhanced V^2 control from On-Semiconductor [A61], the active-droop control from Intersil [A62-A63], the charge control from Semtech [A64], the valley current-mode control from Fairchild [A65], the X-phase control from IR [A66], the multiphase hysteretic control proposed by the University of Central Florida [A67], the dynamic pulse modulator (DPM) method proposed by the University of Florida [A68], and the hybrid control proposed by Virginia Tech [A69]. The active-clamped concept has also been proposed to both improve the transient response and to limit the transient voltage spikes [A70-A71]. The digital control idea has also been introduced into the VRM application area for its benefits in terms of design flexibility, better communication, diagnostics capability, and noise immunity. The

University of Colorado at Boulder, UC-Berkley, the University of Central Florida and the University of British Columbia have done a lot of research in this area [A72-A75]. In industry, Primarion Inc. and Volterra have already developed digital control chips for the multiphase VR [A76-A79]. However, in multi-MHz VRM control, control accuracy, parameter deviation, current-sensing, current-sharing, control delay, and more-than-four-phase interleaving can all be potential problems.

6. Innovative integrated magnetics are required. The multiphase converter is the only solution for high-output-current applications. As a result, there will be more magnetic components in the VRM design. Industry has expended a lot of effort to manufacture standard surface-mounted chip inductors for the VRM application [A80]. CPES has done a lot of work related to multiphase inductor integration, based on the inductor-coupling concept [A40, A81-A82]. Magnetics designed to have low core loss, low winding loss, small size and easy manufacturability are critical for realization of high efficiency and high power density.
7. A high-density capacitor with very low parasitics is also a must. High density is directly related to the energy storage capability, which is very important for the achievement of high-power-density VRM design and for meeting the transient response requirement. Also, low parasitics such as the ESR and the equivalent series inductor (ESL) are indispensable for limiting the transient voltage spikes. Many companies, such as Sanyo, Panasonic, Cornell Dubilier Electronics, Nichicon and KEMET Electronics Corporation, are continuing to reduce the ESR of the capacitor, based on the polymer cathodes technique [A83-A84]. TDK is in the lead in improving the density of the ceramic capacitors. Currently, a 1210 package can have 100μF capacitance [A85].

8. Advanced packaging technologies can help to improve the circuit efficiency by reducing the package resistance and reducing parasitic voltage-ringing in the circuit. Packaging the gate drivers and the power devices together can improve the drive speed so that the switching loss can be reduced. Further system integration between the VRM and the processor will totally change the system power architecture by minimizing the parasitics in the power delivery path. Integration not only helps the transient voltage regulation, but also improves power density and system efficiency. However, there are many challenges involved with integrating the active and passive components together, solving all the interposer problems, and finding the best thermal design for optimal heat dissipation. Primarion proposed a wide-band power architecture [A76]. A MHz regulator delivers the average power to the microprocessor, while a GHz regulator (based on SiGe BiCMOS technology) delivers the transient power at a response speed of several ns. Bump-soldering is the way in which all the regulators and the microprocessor are connected. INCEP proposed a more detailed power architecture, called ZVRM [A86]. The VR is imbedded in the CPU heat sink, and several special connectors deliver the power to the microprocessor through the interposer layer. As a microprocessor manufacturer, Intel also has expended significant effort to improve processor packaging [A87]. The bumpless build-up layer (BBUL) technique is proposed to reduce the interconnection parasitics by imbedding the processor in a built-up layer [A88-A89].

1.4. The Work of this Dissertation

Section 1.3 lists several technology barriers challenging future power management. This dissertation focuses on the high-frequency and high-efficiency VRM design issues.

First, the VRM transient response is thoroughly analyzed. Chapter 2 investigates the relationship between the control bandwidth and the transient response in buck converters in both voltage- and current-mode controls [A90]. A critical bandwidth value is discovered, beyond which pushing the bandwidth can do very little help to reduce the output voltage spike during the transient period. The voltage spike value is dominated by the voltage drop across the ESR and ESL of the output capacitors. This critical bandwidth concept highlights the trend of high-frequency VRMs to be designed with ceramic capacitors for smaller size and faster transient response. Also, guidelines are provided for the design of the output filter inductors, the output filter capacitors, and the control bandwidth for an optimal VRM.

Based on the understanding of the VRM transient response discussed in Chapter 2, Chapter 3 introduces the concept of adaptive voltage position (AVP) used in order to further improve the VRM transient response [A91-A92]. The basic idea is to control the output voltage level so that it is slightly higher than the minimum value at full load and slightly lower than the maximum value at light load. As a result, the entire voltage tolerance window can be used for the voltage jump or drop during the transient period. Compared with the conventional constant-output voltage feedback control, AVP control can halve the number of output capacitors needed to meet the same transient requirement. In this chapter, the idea of constant output impedance design is proposed in order to achieve AVP. Feedback compensator design guidelines are provided for all existing control methods with different kinds of output capacitors.

Another technology barrier this dissertation tries to break involves advanced VRM topologies. Chapter 4 analyzes the fundamental limitations of the conventional buck converter at high switching frequencies, and introduces two novel multiphase converters to overcome the related problems [A93-A96]. The basic idea is to extend the duty cycle by introducing coupled windings into the multiphase buck converters. Also, integrated magnetics structures are discussed for these windings so that the magnetic cores used in the buck converter can be used here. These two topologies can employ the same controllers and gate drivers as are in the buck converter, so the technology evolution is simplified. Furthermore, this chapter extends the basic concept further with an autotransformer structure to derive a series of new topologies, some of which are very suitable for high-frequency VRM design.

Chapter 5 pushes the topology innovation further by introducing the soft-switching quasi-resonant converters for VRM design [A97]. The combination of the quasi-resonant and active-clamped concepts derives a family of new converters, which can realize constant switching-frequency modulation, zero-voltage switching (ZVS), small turn-off currents, small circulating currents in the active-clamped circuit, no body diode reverse-recovery loss, and no body diode dead-time conduction loss. Experimental results prove the high efficiency and high power density of the proposed topology designs.

Finally, Chapter 6 summarizes the entire dissertation and proposes some ideas for future work.

Chapter 2. The Impact of the Control Bandwidth on the VRM Transient Voltage Spikes

A lot of research has gone into VRM transient design because of its serious challenge to the VRM output dynamic voltage regulation [B1-B30]. However, no paper has discussed the relationship between control bandwidth and the transient response. It is just assumed that the higher the bandwidth, the faster the transient response. And all of the analysis for the transient voltage spike is based on an ideal control in which the bandwidth is very high and the duty cycle is saturated during the transient period.

This chapter investigates the relationship between the control bandwidth and the transient voltage spike for both the voltage- and current-mode controls. Section 2.1 studies the fundamental reason for the transient voltage spikes. With the help of small-signal models, Section 2.2 establishes the relationship between the transient voltage spike values and the control bandwidths. Section 2.3 discusses the validity of the small-signal analysis method, and the critical inductance concept is introduced. Finally, in Section 2.4, the simulation and experimental results are shown to prove all of the theoretical analysis.

2.1. The Reason for Transient Voltage Spikes

As a first step, the basic reason for the output voltage spike during the transient is analyzed. For transient analysis, a multiphase interleaved VRM can be more simply considered as a single phase [B31, B32]. Fig. 2.1 shows the structure of the current power delivery architecture and the related lump model with a single-phase buck converter. For a 12V-input VRM, since the output filter inductor current increases faster than it decreases, the transient during step-down is worse than during step-up. As a result, only the step-down transient is analyzed here. For simplicity, all the delay effects, such as gate-drive delay, signal propagation delay in the control loop, are ignored.

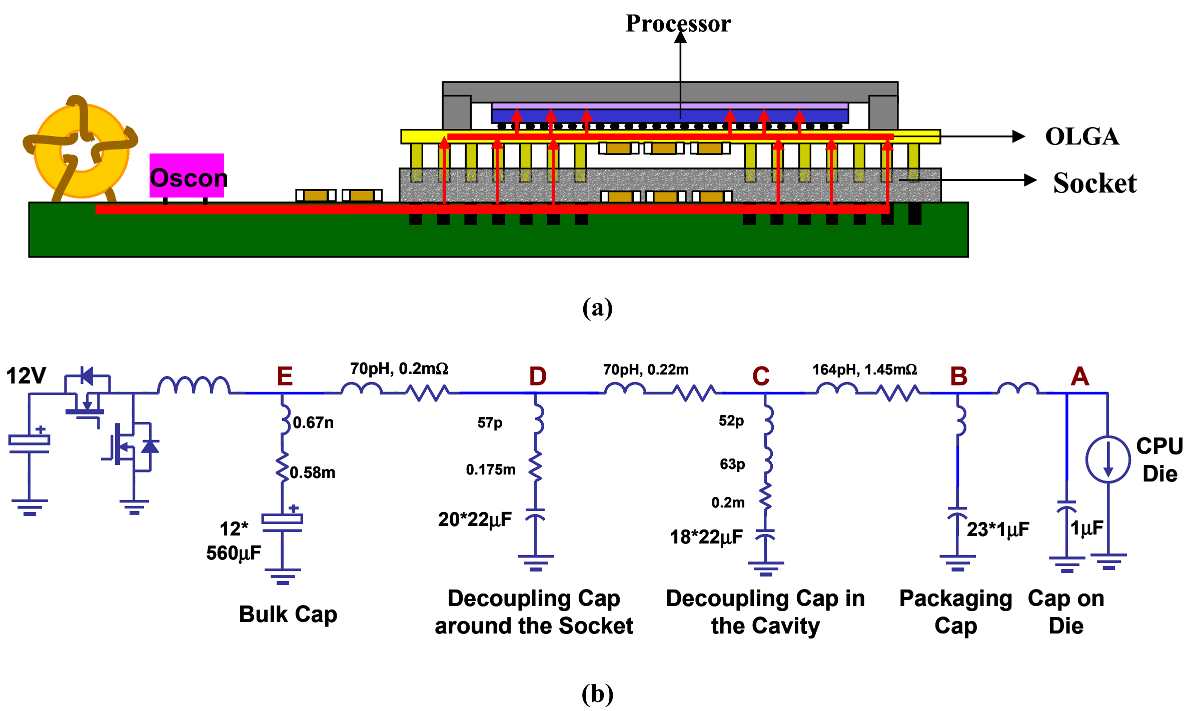


Fig. 2.1. Modeling for power delivery architecture: (a) physical structure and (b) lumped model.

Fig. 2.2(a) shows the reason for the output voltage spike during the load step-down transient. Since the output filter inductor current i_L cannot follow the fast-changing load current i_o, some extra current i_c goes through the output capacitor C, its equivalent series resistance (ESR_c) and its equivalent series inductor (ESL_c). Both the capacitor C charge and the ESR_c and ESL_c voltage drop form the output voltage spike that occurs in the transient period. The output voltage waveform during the step-down transient can be calculated as:

$$v_o(t) = i_c(t) \cdot ESR_c + ESL_c \cdot \frac{d}{dt} i_c(t) + \frac{1}{C_o} \cdot \int_0^t i_c(t) \cdot dt \,. \tag{2.1}$$

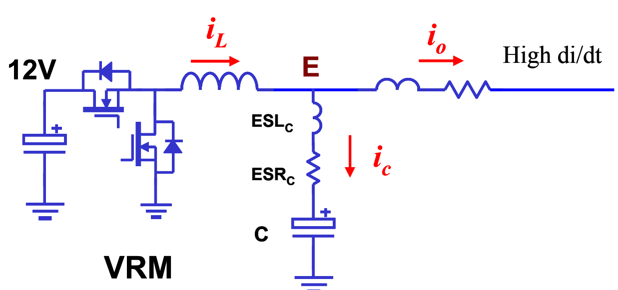
The capacitor charging current is:

$$i_c(t) = i_L(t) - i_o(t) \,. \tag{2.2}$$

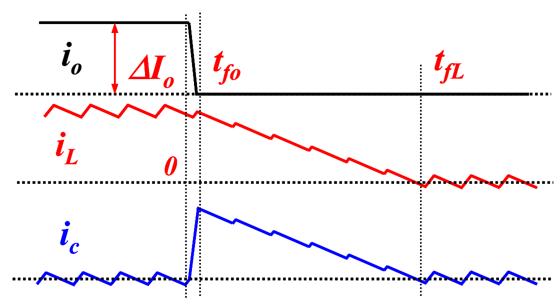
Fig. 2.2(b) shows the inductor current falling-time period t_{fL} from the full load current to the light load current. The load current falling time is t_{fo}, which is normally much smaller than t_{fL}. After t_{fL}, i_c goes to negative and the output voltage v_o continues decreasing. As a result, the voltage spike occurs only in the t_{fL} period.

$$V_{o\_peak} = Max[v_o(t)], \quad (0 \le t \le t_{fL}) \tag{2.3}$$

Equations (2.1) to (2.3) show that the inductor current information obtained during the t_{fL} period is good enough to use for calculating the transient voltage spike. Also, it is necessary to know the load current slew rate so that the output voltage spikes can be calculated. The next two sections will discuss how to derive the inductor current information (based on the small-signal analysis) and the load current slew rate (based on the network analysis).



(a)



(b)

Fig. 2.2. The reason for the voltage spikes at VRM output: (a) VRM circuit and (b) the current through the output capacitors.

2.2. The Inductor Current Slew Rate

To further simplify the analysis, the inductor current ripples can be ignored. The inductor average current information obtained during the transient period can be used to analyze the transient voltage spike according to (2.1) to (2.3). Fig. 2.3 illustrates this idea. So if the relationship can be developed between the control bandwidth and the inductor average current during the transient period, it is easy to investigate the relationship between the transient voltage spike and the control bandwidth. This section will accomplish this goal using the average small-signal model.

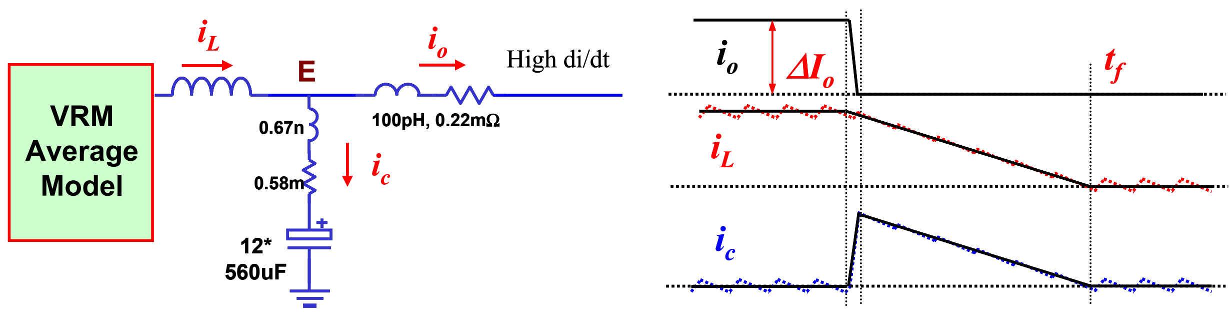
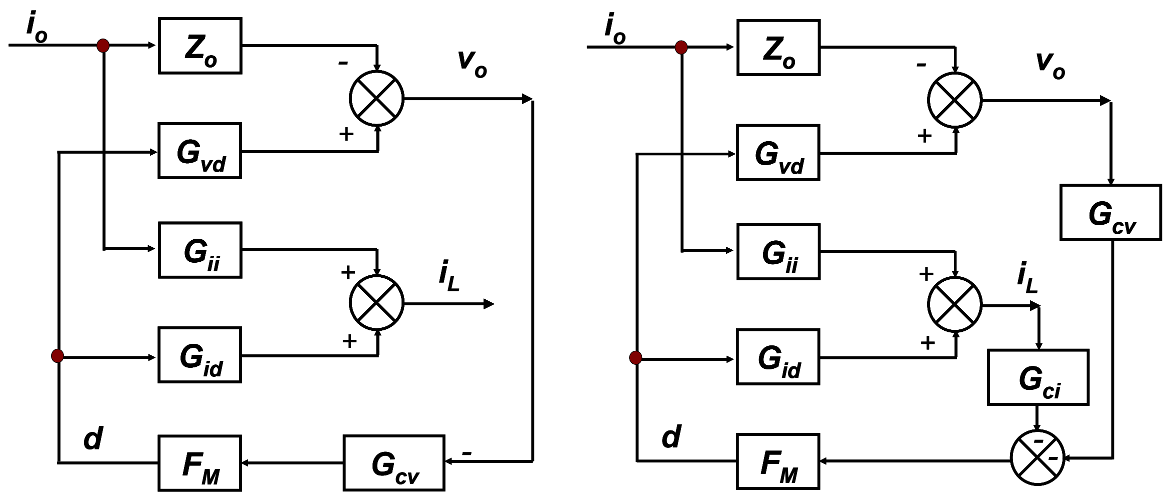


Fig. 2.3. Transient voltage spike analysis based on the average model.

2.2.1. Small-Signal Analysis

Fig. 2.4 shows the small-signal block of the buck converter with voltage- and current-mode controls that follows the feedback-control model [B34-B35]. Z_o is the power stage open-loop output impedance. G_{vd} is the transfer function of output voltage V_o to the duty cycle d. G_{ii} is the transfer function of inductor current i_L to load current i_o. G_{id} is the transfer function of inductor current to the duty cycle d. F_m represents the comparator effect. G_{ci} is the current-loop compensator transfer function, and G_{cv} is the voltage-loop compensator transfer function. The compensator designs here just follow the classic methods outlined in previous work [B34-B35].



(a) **(b)**

Fig. 2.4. Small-signal blocks: (a) voltage-mode control and (b) current-mode control.

In voltage-mode control, the control loop is defined as:

$$T_v = G_{cv} \cdot F_M \cdot G_{vd} \, . \tag{2.4}$$

In current-mode control, the voltage loop is the same as (2.4). The current loop is defined as:

$$T_i = G_{ci} \cdot F_M \cdot G_{id} \, . \tag{2.5}$$

Since current-mode control is a multi-loop control system, the system stability is finally determined by the outer loop, as follows:

$$T_2 = \frac{T_v}{1 + T_i} \, . \tag{2.6}$$

In the small-signal blocks, the current transfer function $G_{ii}(s)$ represents the relationship between the inductor current and the load current in the open-loop condition, as follows:

$$G_{ii} = \frac{1+\dfrac{s}{\omega_{ESR}}}{1+\dfrac{s}{\omega_o \cdot Q}+\dfrac{s^2}{\omega_o^{\,2}}}, \text{ and} \tag{2.7}$$

$$\omega_{ESR} = \frac{1}{ESR_c \cdot C_o},\ \omega_o = \frac{1}{\sqrt{L \cdot C_o}},\ Q = R_L \cdot \sqrt{\frac{C_o}{L}}, \tag{2.8}$$

where ω_{ESR} is the ESR zero of the output capacitor, ω_o is the power stage double pole, and Q represents the damping effect that exists in the second-order system because of the resistance R_L in the power stage. The ESR of the inductor, the trace resistance, and the turn-on resistance of the power MOSFETs all contribute to R_L [B35].

With a closed voltage loop, the current transfer function is modified to:

$$G_{ii\_cv} = G_{ii} + G_{id} \cdot G_{cv} \cdot F_M \cdot \frac{Z_o}{1+T_v}. \tag{2.9}$$

With both the current and voltage loops closed, the current transfer function is modified to:

$$G_{ii\_ci} = \frac{G_{ii} \cdot (1+T_v) + F_M \cdot G_{id} \cdot G_{cv} \cdot Z_o}{1+T_i+T_v}. \tag{2.10}$$

Further mathematic analysis can simplify (2.9) and (2.10) as follows:

$$G_{ii\_cv} = \frac{1+\dfrac{s}{\omega_c}}{1+\dfrac{s}{\omega_c \cdot Q}+\dfrac{s^2}{\omega_c^{\,2}}}, \text{ and} \tag{2.11}$$

$$G_{ii\_ci} = \frac{1}{1+\dfrac{s}{\omega_c}} \cdot \frac{1}{1+\dfrac{s}{\omega_n}+\dfrac{s^2}{\omega_n^{\,2}}}, \tag{2.12}$$

where ω_c is the crossover frequency of the control loop; i.e., it is the voltage loop in voltage-mode control, but is the outer loop in current-mode control. The ω_n is half of the switching frequency.

Now, we can see that the current transfer function $G_{ii}(s)$ is related to the control bandwidth. Consequently, the average inductor current information is a function of the control bandwidth, as follows:

$$i_L(s) = G_{ii}(s) \cdot i_o(s) = f(\omega_o, s)\,, \tag{2.13}$$

where, $i_o(s)$ is the expression of the transient load current information.

Based on all the information in the frequency domain, the average inductor current waveform in the transient period, which is in the time domain, can be easily derived using an inverse Laplace transformation. Also, the relationship between the inductor average current and the control bandwidth can be derived in this transformation. According to (2.1) and (2.2), the transient response voltage waveform can be calculated. Finally, the transient voltage spike values, which are the maximum values of the voltage waveforms, can be related to the control bandwidth.

Since the load current slew rate of the microprocessor is much higher than the output filter inductor current slew rate (for example, 450A/μs for a Pentium 4) [B33], the load current transient is simply discussed as an ideal step change in this section.

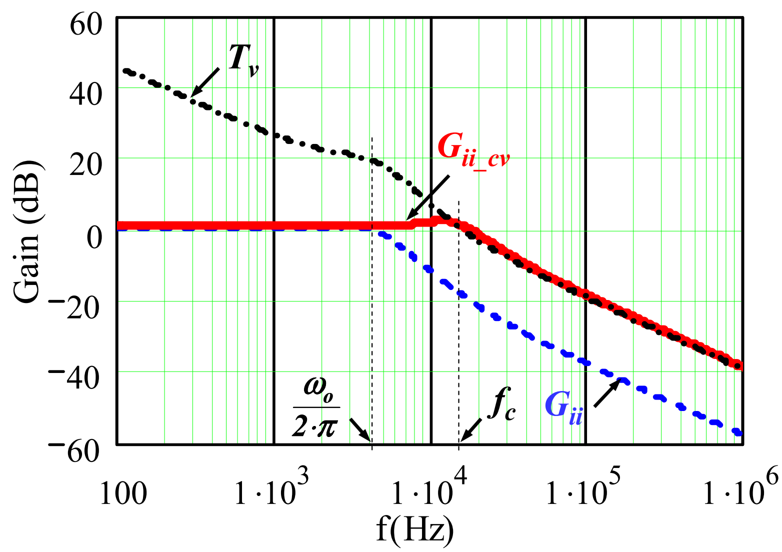
In the frequency domain, the normalized load current with step change can be expressed as:

$$i_o = 1/s\,. \tag{2.14}$$

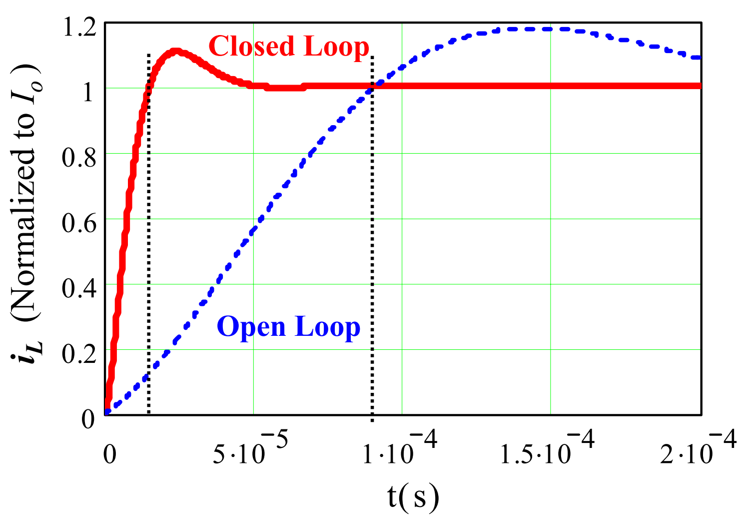
Fig. 2.5 shows the current transfer function and the step response inductor current with voltage-mode control. In the open loop, the inductor current responds to the load current step change as a second-order system, in which the oscillation frequency is the power stage double pole. With the loop closed, the oscillation frequency is modified to the level of the control bandwidth, which is much faster than the condition in the open loop. The inductor current rising time is approximately a quarter of the oscillation period. Thus, the average inductor current during the step-down transient is about:

$$i_L(t) \approx \Delta I_o \cdot (1 - 4 \cdot f_c \cdot t) \quad (t \le \frac{1}{4 \cdot f_c}). \tag{2.15}$$

where $f_c = \dfrac{\omega_c}{2 \cdot \pi}$. (2.16)



(a)

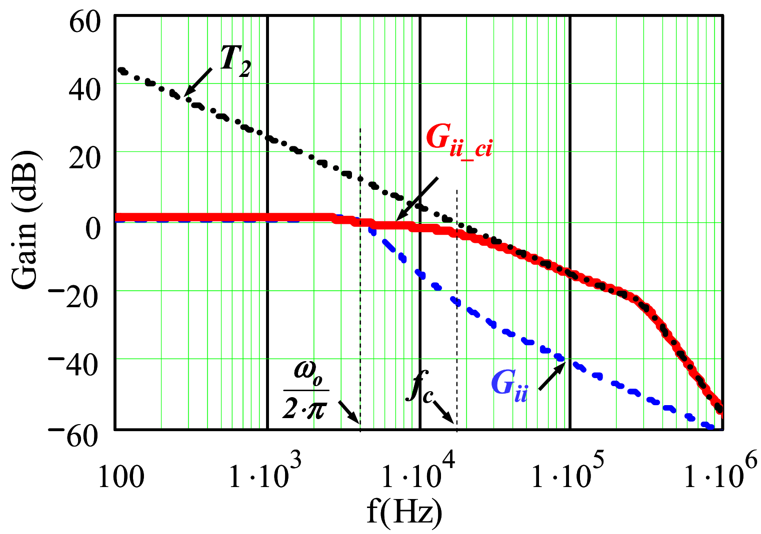


(b)

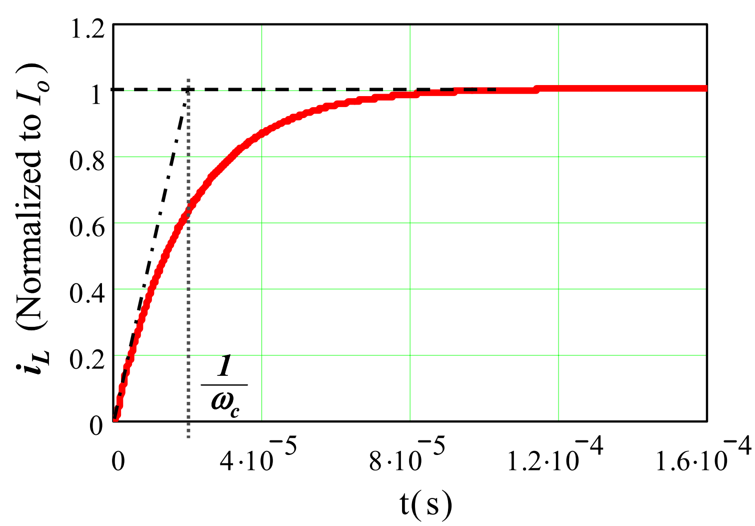
Fig. 2.5. Voltage-mode control: (a) current transfer function $G_{ii}(s)$ and (b) step response inductor current.

Fig. 2.6 shows the current transfer function and the step response inductor current with peak-current-mode control. The inductor current with closed loop responds to the load current step change as a first-order system, in which the time constant is the outer-loop control bandwidth. The average inductor current during the transient is approximately:

$$i_L(t) \approx \Delta I_o \cdot (1 - e^{-t\cdot\omega_c}) = \Delta I_o \cdot (1 - e^{-t\cdot 2\cdot\pi\cdot f_c}). \tag{2.17}$$



(a)



(b)

Fig. 2.6. Current-mode control: (a) current transfer function G_{ii}(s) and (b) step response inductor current.

2.2.2. The Critical Inductance Design

The preceding analysis is based on small-signal models. If the duty cycle is saturated, the closed-loop current transfer function can no longer be used for transient analysis. Instead, the output filter inductance determines the inductor current during the transient period. The inductor current slew rates during the step-up and step-down are:

$$\left. {di}/{dt} \right|_{up} = \frac{V_{in} - V_o}{L} \text{, and} \tag{2.18}$$

$$\left. {di}/{dt} \right|_{down} = \frac{V_o}{L} . \tag{2.19}$$

According to (2.15) and (2.17), the small-signal model analysis also determines an inductor current slew rate during the transient. For voltage-mode control,

$$ {di}/{dt} = 4 \cdot f_c \cdot \Delta I_o . \tag{2.20}$$

For current-mode control,

$$ {di}/{dt} = 2 \cdot \pi \cdot f_c \cdot \Delta I_o \cdot e^{-t \cdot 2 \cdot \pi \cdot f_c} \text{, and} \tag{2.21}$$

$$\left. {di}/{dt} \right|_{\max} = 2 \cdot \pi \cdot f_c \cdot \Delta I_o . \tag{2.22}$$

However, the maximum inductor current slew rates derived from the small-signal models in (2.20) and (2.22) cannot exceed the Faraday Law limitations given in (2.18) and (2.19). Larger values from (2.20) and (2.22) mean that the duty cycles are saturated and the small-signal model is no longer valid. The equivalent points give a critical inductance value. For voltage-mode control,

$$L_{cv} = \frac{V_{in}}{4 \cdot \Delta I_o \cdot f_c} \cdot \min(D, 1 - D) . \tag{2.23}$$

For current-mode control,

$$L_{ci} = \frac{V_{in}}{2 \cdot \pi \cdot \Delta I_o \cdot f_c} \cdot \min(D, 1-D)\,. \tag{2.24}$$

For the 12V-input VRMs, D is smaller than (1-D). As a result, Equations (2.23) and (2.24) can be further simplified as:

$$L_{cv} = \frac{V_o}{4 \cdot \Delta I_o \cdot f_c}, \text{ and} \tag{2.25}$$

$$L_{ci} = \frac{V_o}{2 \cdot \pi \cdot \Delta I_o \cdot f_c}\,. \tag{2.26}$$

The critical inductance concept reveals the point at which the duty cycle will go to saturation in a closed-loop controlled converter. The crossover frequency determines the critical inductance value. More detailed analysis is provided in other work [B36].

Also, the preceding analysis shows that both the control bandwidth and the inductance impact the inductor current transient response speed. With the inductance designed to be smaller than the critical value, the control bandwidth determines the effect. But for an inductance design that is larger than the critical value, the same control bandwidth is over-designed and the inductor itself determines its current transient response speed. For each inductance design, an effective control bandwidth can be derived from (2.25), as follows:

$$f_{ce} = \frac{V_o}{4 \cdot \Delta I_o \cdot L}\,. \tag{2.27}$$

Any bandwidth design beyond this value saturates the duty cycle but can not improve the transient response speed.

The preceding analysis shows that for the critical bandwidth design, the relative critical inductance value is a good design point in terms of both the transient response speed and the efficiency. There is no need to further reduce the inductance or to push the bandwidth. Of course, a certain design margin should be considered in real VRM applications.

2.3. The VRM Output Voltage Spike Approximate Analysis

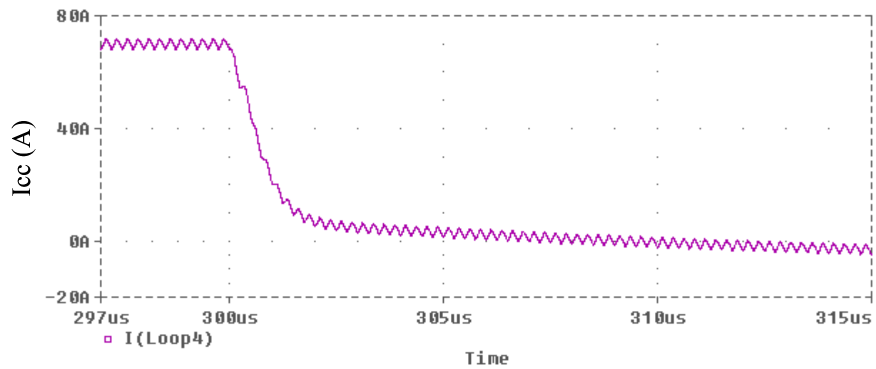
Section 2.2 derived the inductor current slew rate, which is related to the control bandwidth. The next step is to know the transient load current slew rate. According to Intel's design guidelines [B33], the worst di/dt for a VRM is about 50 A/µs. Fig. 2.7(a) shows the load current transient waveform with PSpice simulation. To simplify the analysis, the load current transient waveform in Fig. 2.7(b) is used. Here the current ripple is ignored, and the maximum di/dt is used for the load step-change analysis. The objective is to show how the control bandwidth will impact the output voltage spikes. For accurate voltage spike values, we still need to do the system simulation. Section 2.4 will show the results.

Then, we can determine the level of charging current flowing through the output capacitors. Fig. 2.8 shows the capacitor current waveform. There are two intervals for i_c. The first interval starts from t_0 and ends at t_1, and has a positive current slew rate SR_{io}-SR_{iL}. The second interval is from t_1 to t_2, and has a negative current slew rate $-SR_{iL}$.

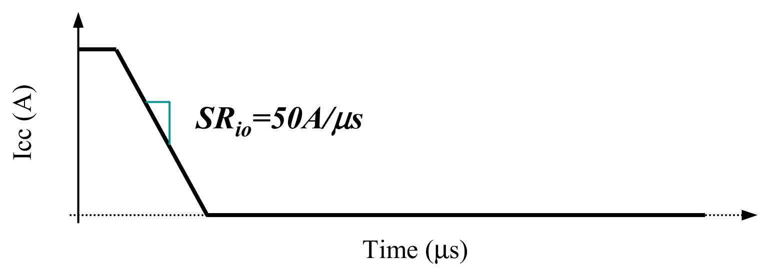
$$i_c = \begin{cases} (SR_{io} - SR_{iL}) \cdot t & t_0 \le t \le t_1 \\ -SR_{iL} \cdot t & t_1 \le t \le t_2 \\ 0 & t_2 \le t \end{cases} \tag{2.28}$$

Then it is easy to derive the output voltage transient waveform according to (2.1). Here we show the equation again, as follows:

$$v_o(t) = i_c(t) \cdot ESR_c + ESL_c \cdot \frac{d}{dt} i_c(t) + \frac{1}{C_o} \cdot \int_0^t i_c(t) \cdot dt\,. \tag{2.29}$$



(a)



(b)

Fig. 2.7. The VRM load slew rate: (a) simulation waveform supported by Intel, and (b) the simplified waveform used for analysis.

Based on the output voltage waveform, the voltage spike value can be identified. The maximum voltage spike could only appear at t_1 or later than t_1, but before t_2. Based on Fig. 2.8 and (2.29), the voltage spike at t_1 can be easily determined as the maximum value during t_0 to t_1. On the other hand, the voltage spike expression and the maximum value during t_1 to t_2 can also be derived based on Fig. 2.8 and (2.29). By letting these two maximum voltage spikes be equal, a criterion time (2.30) can be derived, which is used to judge the point at which the absolute maximum voltage spike appears in the range.

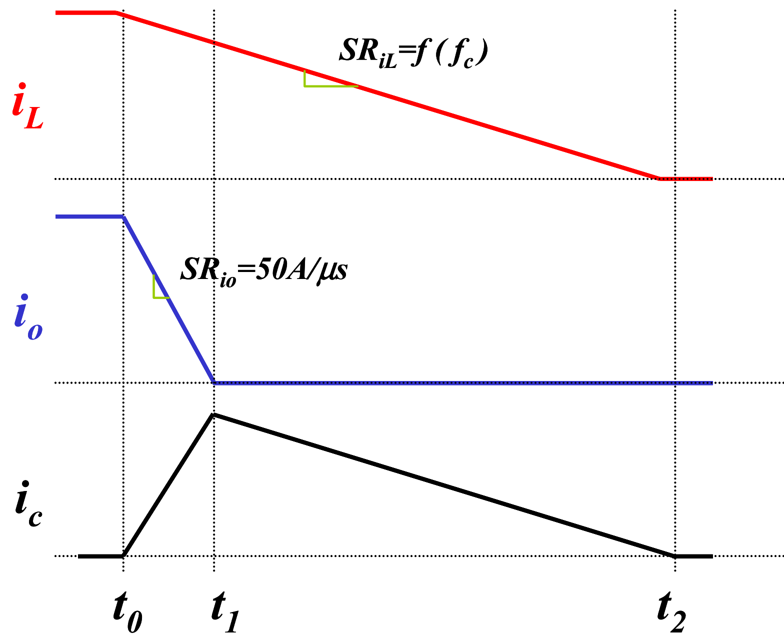


Fig. 2.8. The simplified output capacitor charging current waveform

$$t_{cr} = \frac{\Delta I_o}{SR_{io}} + ESR_c \cdot C_o + \sqrt{2 \cdot \frac{SR_{io}}{SR_{iL}} \cdot ESL_c \cdot C_o} \tag{2.30}$$

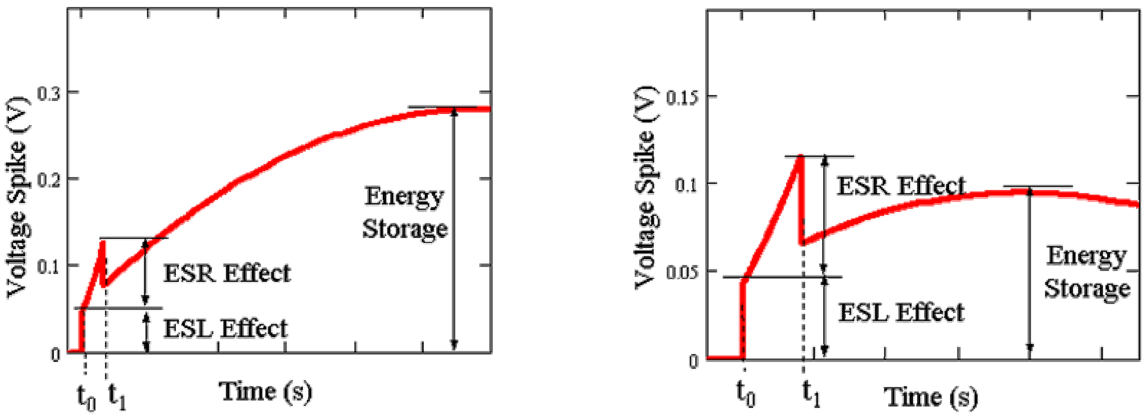
When the rise time of current i_L is less than or equal to t_{cr} the maximum voltage deviation always appears at the moment t_1 (see Fig. 2.9(a)), such that:

$$v_{o\_\max} = \frac{(SR_{io} - SR_{iL})}{2 \cdot C_o} \cdot \left(\frac{\Delta I_o}{SR_{io}}\right)^2 + (SR_{io} - SR_{iL}) \cdot \frac{\Delta I_o}{SR_{io}} \cdot ESR_c + ESL_c \cdot (SR_{io} - SR_{iL}) \,. \tag{2.31a}$$

When the rise time of current i_L is greater than t_{cr} (see Fig. 2.9(b)), the maximum voltage deviation appears at a certain moment after t_1, such that:

$$v_{o\_\max} = \frac{SR_{io}}{2 \cdot C_o} \cdot \left(\frac{\Delta I_o}{SR_{io}}\right)^2 + \frac{SR_{iL} \cdot ESR_c^{\ 2} \cdot C_o}{2} + \frac{\Delta I_o^{\ 2}}{2 \cdot C_o \cdot SR_{iL}} - \frac{\Delta I_o^{\ 2}}{C_o \cdot SR_{io}} - ESL_c \cdot SR_{iL} \,. \tag{2.31b}$$

Fig. 2.9 clearly shows that the voltage spike across the capacitor includes three parts: the voltage deviation caused by the ESR, the voltage deviation caused by the ESL, and the voltage deviation caused by the energy storage. Fig. 2.11 shows the impact of the control bandwidth on the output voltage transient response waveforms. The higher the control bandwidth, the faster the slew rate of i_L, and the smaller the voltage deviation caused by energy storage. When the control bandwidth is high enough, the ESR and ESL of the output capacitors dominate the transient voltage spikes. Fig. 2.10 shows the relationship between the control bandwidth and the transient voltage spikes.



(a) **(b)**

Fig. 2.9. The voltage waveform across the capacitor: (a) the maximum voltage deviation appears at t_1, and (b) the maximum voltage deviation appears at a certain moment after t_1.

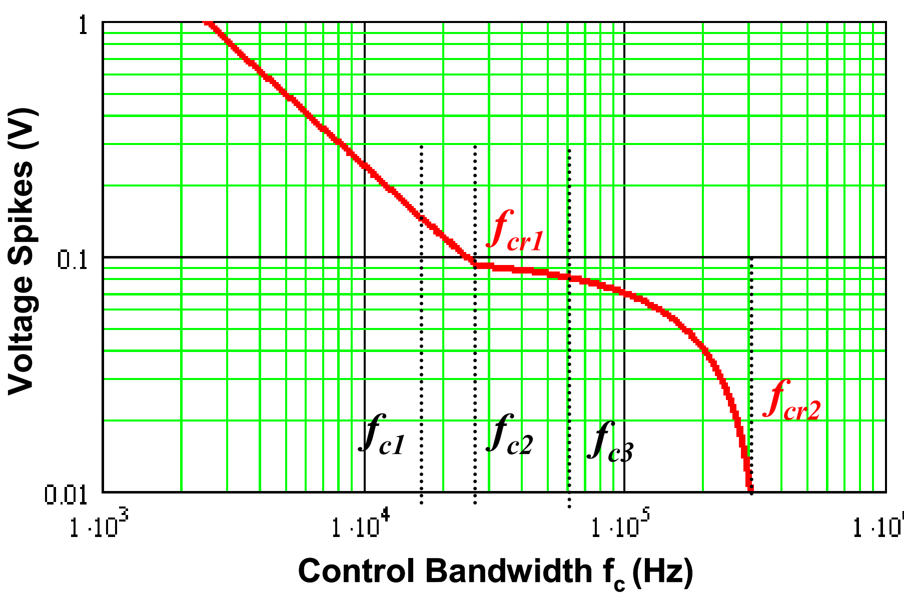


Fig. 2.10. The impact of the control bandwidth on the transient voltage spikes.

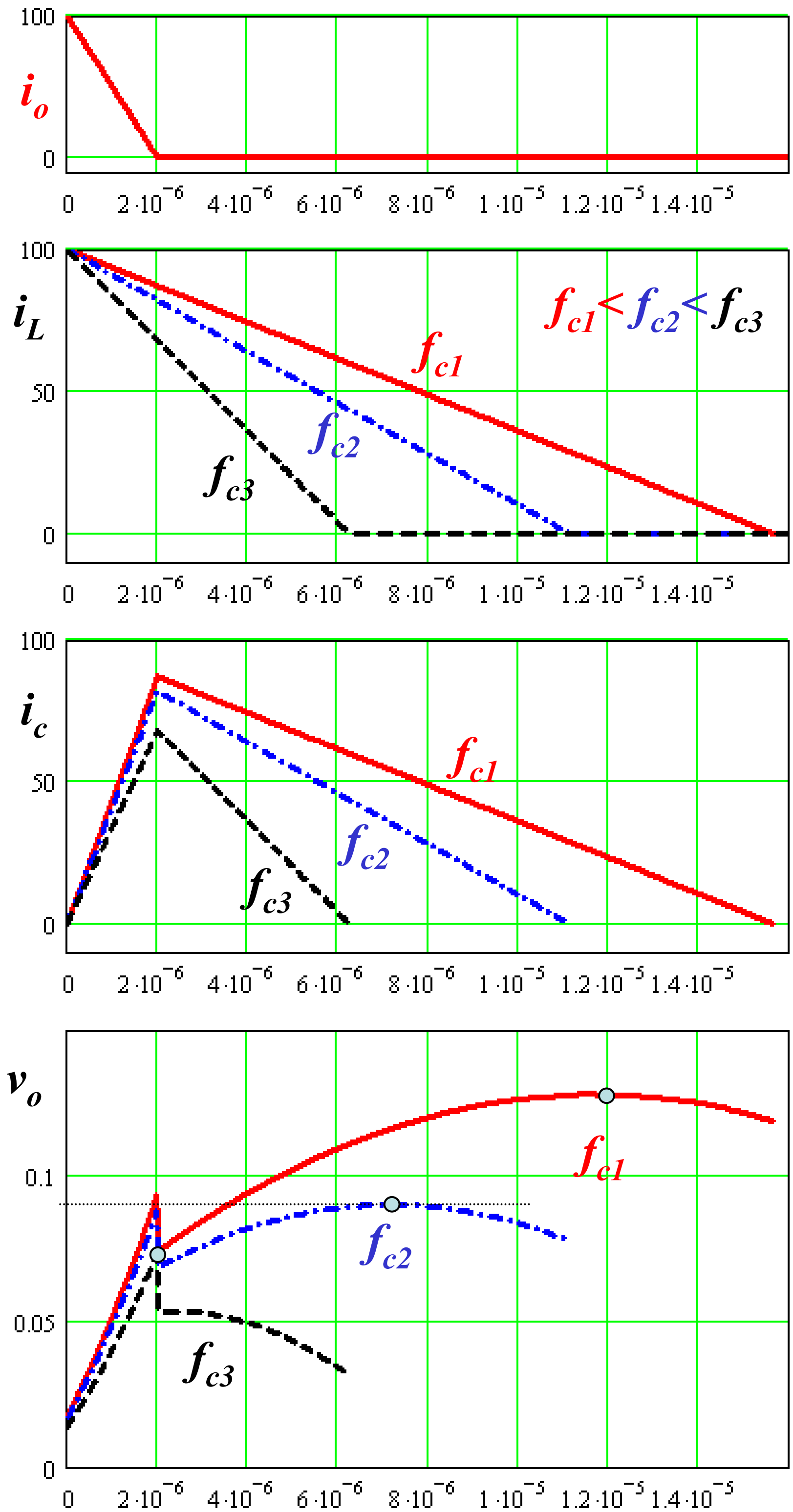


Fig. 2.11. The impact of the control bandwidth on the output voltage transient response waveforms

In Fig. 2.10, there are two critical bandwidths: f_{cr1} and f_{cr2}. When the bandwidth of the VR is smaller than f_{cr1}, the voltage spike across the capacitor is determined by the energy storage factor. This expression is shown in (2.31a). Therefore, it is necessary to parallel more capacitors in order to increase the capacitance so that the voltage specification can be satisfied. When the bandwidth of the VR is greater than f_{cr1}, the ESR and ESL effects determine the voltage spike. This expression is shown in (2.31b). The purpose of paralleling more capacitors is not to achieve a larger capacitance, but to reduce the ESR and ESL.

Based on Equations (2.30) and (2.31), a critical bandwidth of current-mode control is derived.

$$f_{cr1} = \frac{\left(ESR_c \cdot C_o + \frac{\Delta I_o}{SR_{io}} + \frac{ESL_c \cdot C_o \cdot SR_{io}}{\Delta I_o} \right)}{\pi \cdot \left(ESR_c \cdot C_o + \frac{\Delta I_o}{SR_{io}} \right)^2} - \frac{\sqrt{\left(ESR_c \cdot C_o + \frac{\Delta I_o}{SR_{io}} + \frac{ESL_c \cdot C_o \cdot SR_{io}}{\Delta I_o} \right)^2 - \left(ESR_c \cdot C_o + \frac{\Delta I_o}{SR_{io}} \right)^2}}{\pi \cdot \left(ESR_c \cdot C_o + \frac{\Delta I_o}{SR_{io}} \right)^2} \tag{2.32}$$

To get a clear picture and the fundamental results, an assumption is made that the ESL effect of the bulk capacitor is ignored because some ceramic capacitors with small levels of ESL are normally paralleled with bulk capacitors; meanwhile the slew rates of i_3 and i_L are small compared with the slew rates of the die-side and socket-sensing point. For example, the slew rate of i_3 is 50 A/us and the ESL is 200 pH; the voltage deviation due to the ESL is only 10 mV. Compared with the 150mV voltage window of today's specification, this value is negligible. Therefore, by assuming the ESL=0, the critical bandwidth can be simplified as follows:

$$f_{cr1\_ESR} = \frac{1}{\pi \cdot \left(\frac{\Delta I_o}{SR_{io}} + ESR_c \cdot C \right)}. \tag{2.33}$$

Accordingly, (2.30) and (2.31) can be simplified as:

$$t_{cr\_ESR} = \frac{\Delta I_o}{SR_{io}} + ESR_c \cdot C_o \text{, and} \tag{2.34}$$

$$v_{o\_\max} = \begin{cases} \left(SR_{io} - SR_{iL}\right) \cdot \frac{\Delta I_o}{SR_{io}} \cdot ESR_c + \frac{1}{2 \cdot C_o} \cdot \left(\frac{\Delta I_o}{SR_{io}} \right)^2 \cdot \left(SR_{io} - SR_{iL}\right) & t \geq t_{cr\_ESR} \\ \frac{1}{2 \cdot C_o} \cdot \left(\frac{\Delta I_o}{SR_{io}} \right)^2 \cdot SR_{io} + \frac{SR_{iL} \cdot ESR_c^{\ 2} \cdot C_o}{2} + \frac{\Delta I_o^{\ 2}}{2 \cdot C_o \cdot SR_{iL}} - \frac{\Delta I_o^{\ 2}}{C_o \cdot SR_{io}} & t < t_{cr\_ESR} \end{cases}. \tag{2.35}$$

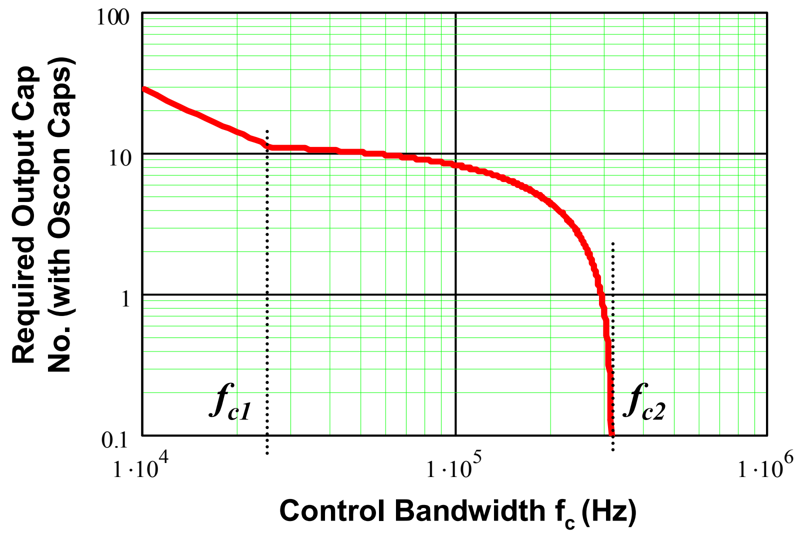
There is another critical bandwidth, to which point the output voltage spike is reduced to zero. That means the inductor current slew rate is fast enough to follow the load current slew rate. With such a bandwidth design, there is no need to use the bulk output capacitors. The decoupling capacitors play the roles of both the decoupling and the energy storage.

$$f_{cr2} = \frac{SR_o}{\pi \cdot I_o} \tag{2.41}$$

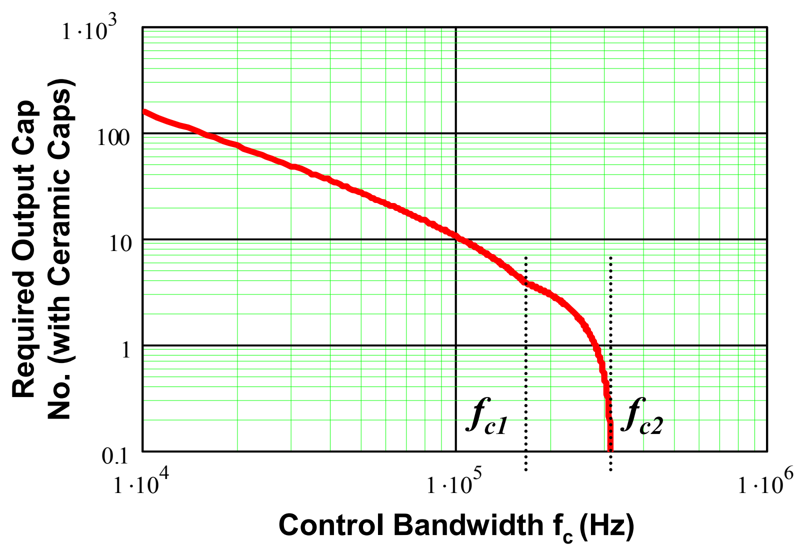
2.4. The Design Considerations for the Output Capacitors

The number of capacitors can be easily derived according to the voltage deviation specification. Please note that a change in the number of capacitors also changes the slew rate of each loop. Therefore, this calculation is iterative.

Fig. 2.12 shows the bandwidth vs. the output bulk capacitor number at the condition of I_o=100A and with today's power delivery structure. As the bandwidth increases, the capacitor number can be continually reduced. This is a big motivation for high-frequency VRs. A very interesting phenomenon can be observed: When the bandwidth is pushed to a certain value, the output bulk capacitor will be eliminated no matter whether an Oscon capacitor or a ceramic capacitor is used. Actually, a 300kHz~400kHz bandwidth is already high enough to eliminate the bulk capacitors, because the slew rate of the inductor current is already very close to that of the current demand.



(a)



(b)

Fig. 2.12. The control bandwidth vs. the bulk output capacitor number: (a) design with Oscon capacitors and (b) design with ceramic capacitors.

2.5. Simulation and Experimental Results

PSpice software is used to simulate a four-phase interleaved synchronous buck converter with voltage-mode controls. The DC-DC conversion is from 12 V to 1.3 V with 70A full load current. The switching frequency is set at 2 MHz in order to determine the effect of pushing the bandwidth to 350 KHz. Fig. 2.13 shows the PSpice simulation circuits with all the detailed information.

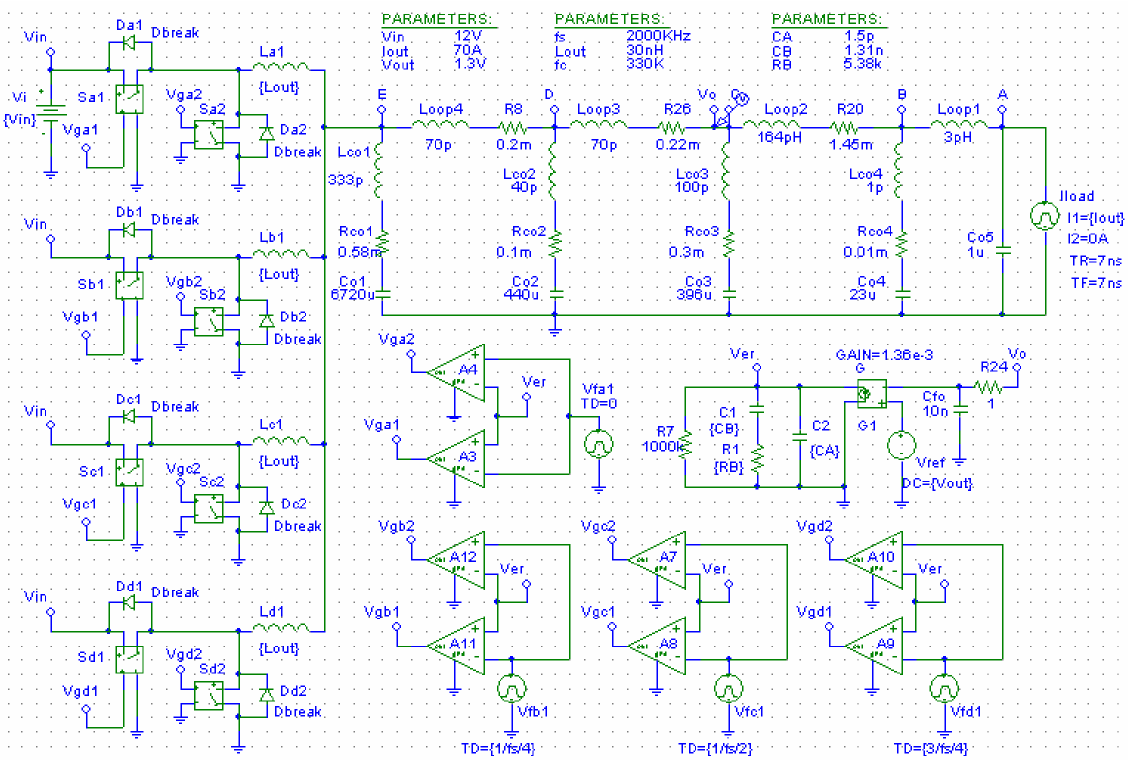


Fig. 2.13. The system simulation circuit with Oscon bulk output capacitors.

Fig. 2.14 shows the simulation results with different control bandwidths. We can see that increasing the control bandwidth can continue to increase the inductor current response speed. When f_c<25KHz, increasing f_c can significantly reduce the third voltage spike, which is determined by energy storage. But there is little impact on the second and first voltage spikes, which are determined by the ESR and ESL of the bulk and decoupling capacitors.

When f_c>40KHz, the third and second spikes merge together; increasing f_c can slowly reduce the second voltage spike, but has no impact on the first. When f_c>160KHz, the second voltage spike is smaller than the first; increasing f_c can slowly reduce the second voltage spike, but has very little impact on the first voltage spike.

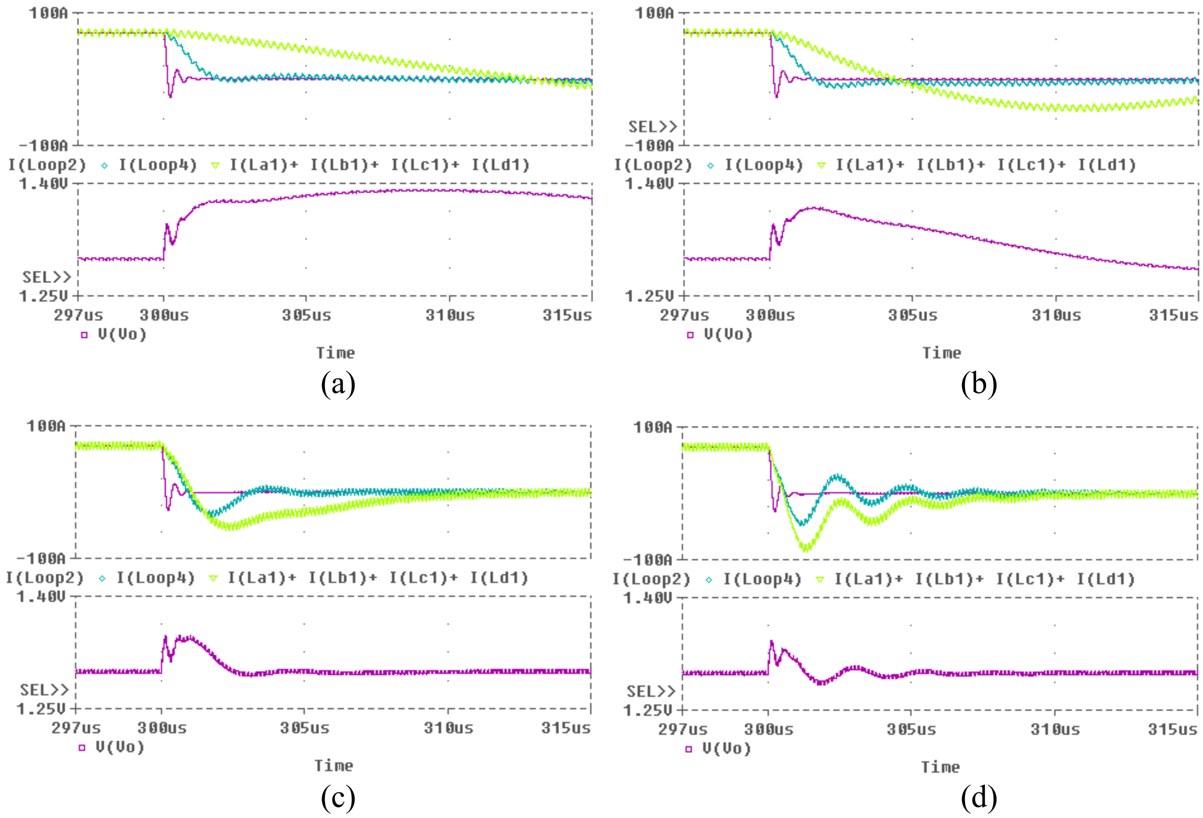


Fig. 2.14. Transient response vs. control bandwidth with Oscon capacitors: (a) f_c=16KHz, (b) (a) f_c=40KHz, (c) f_c=160KHz, and (d) f_c=330KHz.

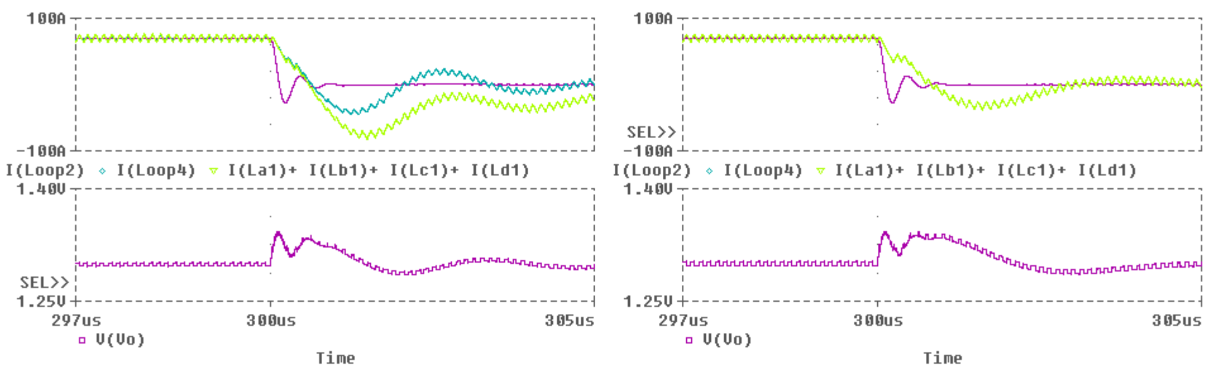


Fig. 2.15. Transient response at f_c=330KHz: (a) with Oscon bulk capacitors and (b) without Oscon bulk capacitors.

When f_c>330KHz, the Oscon bulk capacitor can be eliminated, because the VRM output inductor current can follow the load current change speed. Fig. 2.15 shows the output transient response waveforms with and without the bulk Oscon capacitors. The control bandwidths are the same at 330 KHz.

Fig. 2.16 shows the PSpice simulation circuits with ceramic capacitors as the bulk output capacitors. The switching frequency is set at 2 MHz in order to determine the effect of pushing the bandwidth to 350 KHz. Fig. 2.17 shows the simulation results with different control bandwidths. We can see that increasing the control bandwidth can continue to increase the inductor current response speed. Because of the very low ESL of the ceramic capacitors, there are only two voltage spikes in the output.

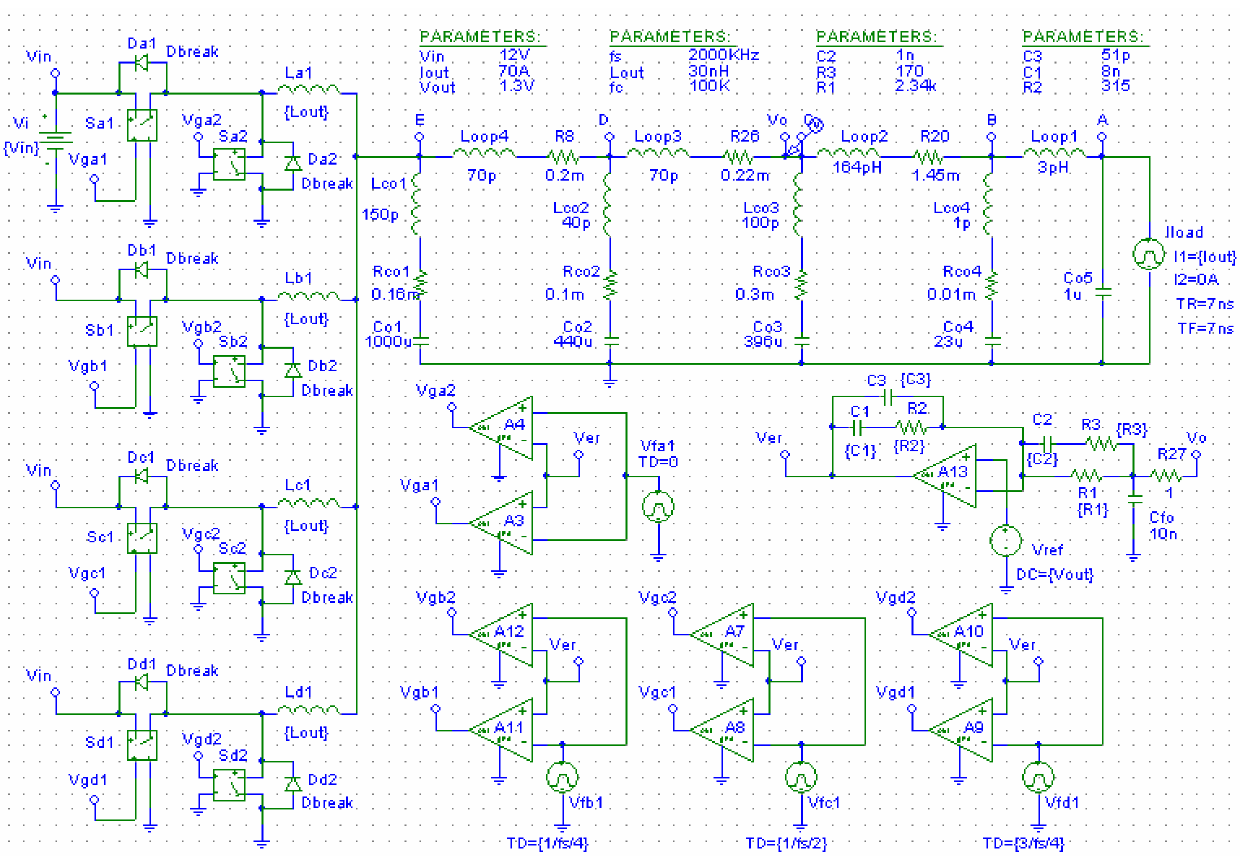
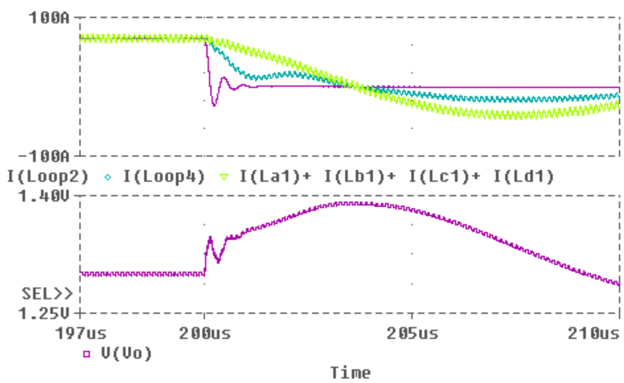


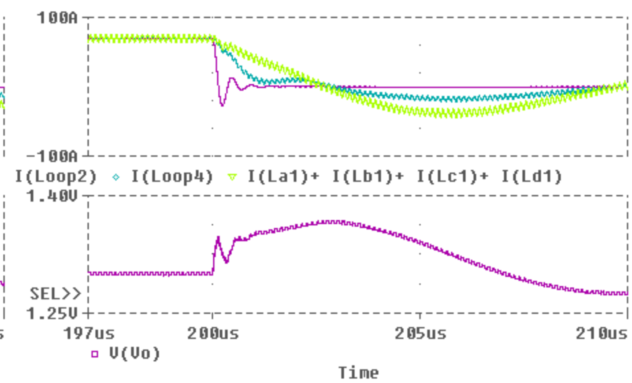
Fig. 2.16. The PSpice simulation file for the entire power delivery system with ceramic capacitors.

When f_c<200KHz, increasing f_c can significantly reduce the second voltage spike, but has no impact on the first. When f_c>200KHz, the second voltage spike is smaller than the first; increasing f_c can slowly reduce the second voltage spike, but has very little impact on the first.

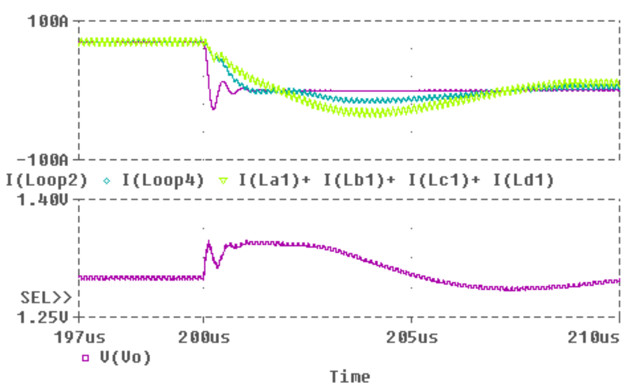
When f_c>330KHz, the ceramic bulk capacitors can also be eliminated, because the VRM output inductor current can follow the load current change speed. Fig. 2.18 shows the output transient response waveforms with and without the bulk ceramic capacitors. The control bandwidths are the same at 330 KHz.



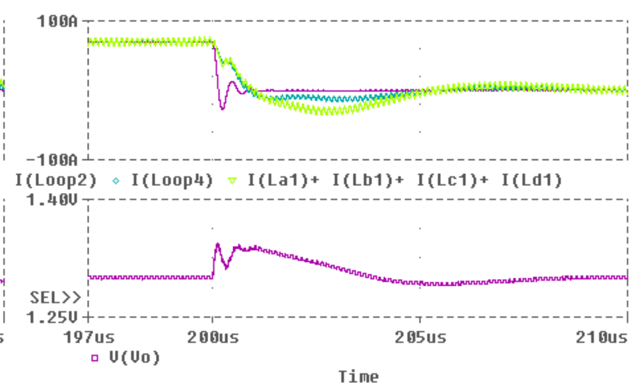
(a)



(b)



(c)



(d)

Fig. 2.17. Transient response vs. control bandwidth with ceramic capacitors: (a) f_c=100KHz, (b) (a) f_c=130KHz, (c) f_c=200KHz, and (d) f_c=330KHz.

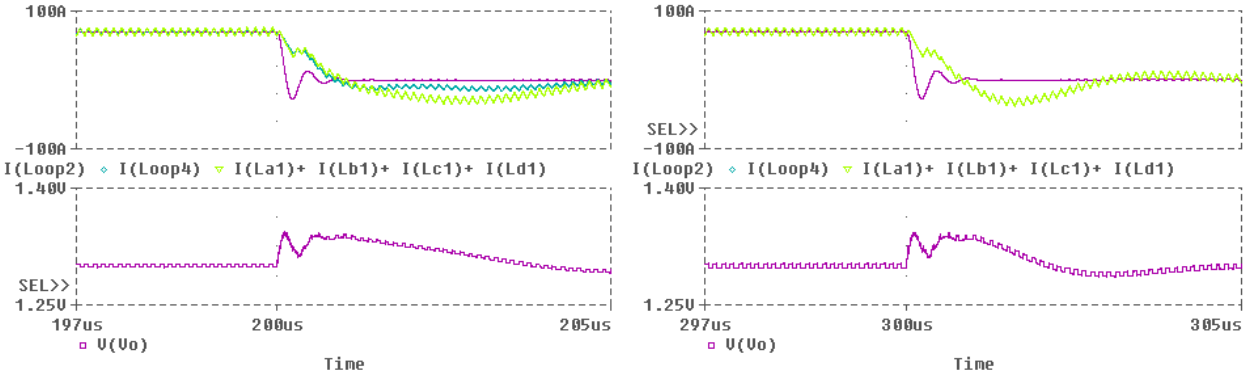


Fig. 2.18. Transient response at f_c=330KHz: (a) with bulk ceramic capacitors and (b) without ceramic bulk capacitors.

A two-phase interleaving synchronous buck converter is developed to verify the results of the theoretical analysis. The DC-DC conversion is from 12V to 1.5V with 25A full load current. The switching frequency of each phase is 300 KHz. Four Sanyo Oscon capacitors (4SP820M) are used for the output capacitor. The output filter choke in each phase is 800 nH (DELTA DPF146-0R8).

Fig. 2.19 shows the transient waveforms with voltage-mode control. The experimental results agree with the theoretical analysis. Because the output interconnection resistor is also responsible for some voltage drop that occurs in the transient period, the real voltage spike limitation is slightly larger than the theoretical result (75 mV).

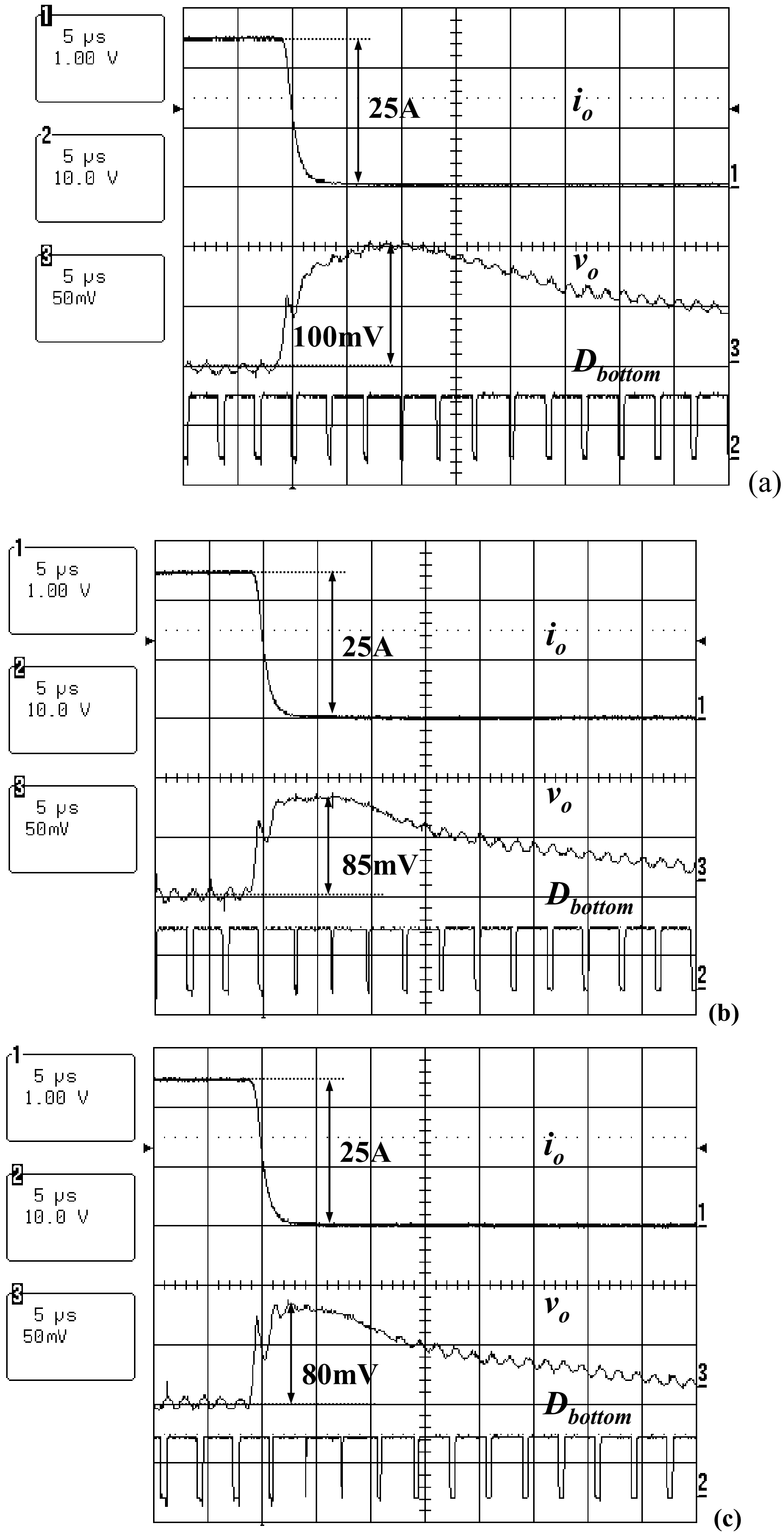
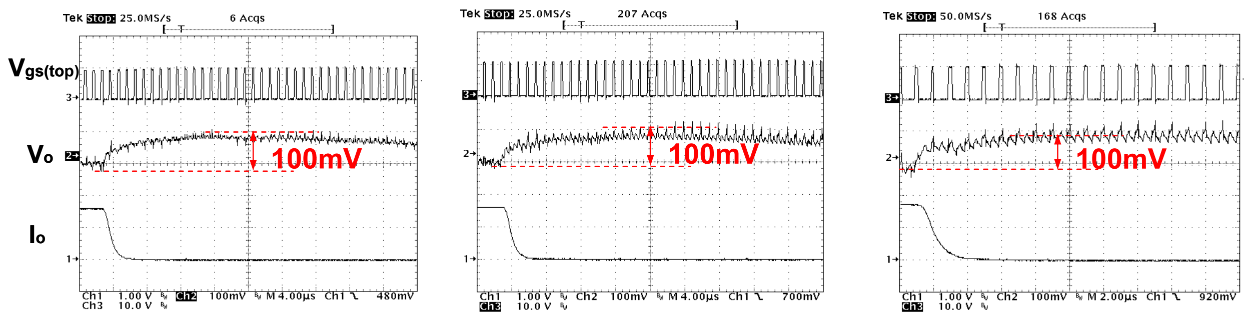


Fig. 2.19. Transient voltage spikes with voltage-mode control: (a)f_c=10KHz, (b) f_c=f_{ct_v}=25KHz, and (c) f_c=36KHz.



(a) **(b)** **(c)**

Fig. 2.20. The output capacitor reduction achieved by pushing the control bandwidth: (a) fc=140KHz, C=4*100uF, (b) fc=200KHz, C=2*100uF and (c) fc=320KHz, C=0.

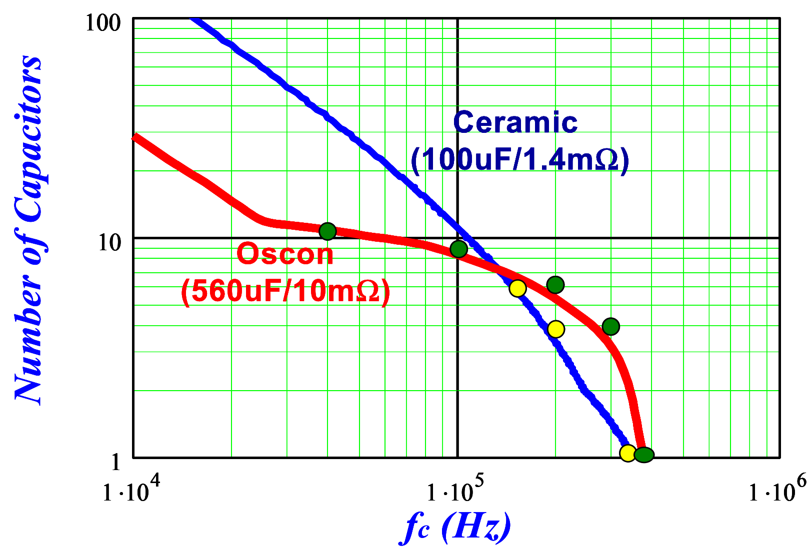


Fig. 2.21. The verification of the relationship between the bandwidth and the capacitor number.

2.6. Summary

The dynamic output voltage regulation during the fast load transient changes is a severe challenge for VRM design. This paper investigates the relationship between the control bandwidth and the output voltage spike during the load transient change. A critical bandwidth is derived to improve the VRM design. In the low-frequency range (below the critical bandwidth), the control bandwidth determines the transient voltage spike value, and increasing the control bandwidth can reduce the transient voltage spike. However, further pushing the control bandwidth higher than the critical value offers no help, because the transient voltage drop across the ESR of the output capacitors dominates the transient voltage spike. Since the critical bandwidth is related to the time constant of the output capacitors, the critical bandwidths are different for VRM designs with different kinds of output capacitors. Currently, the Oscon capacitors are widely used for VRM design, but their large ESR value determines the critical bandwidth to be around 20 to 30 KHz. Further increasing the switching frequency with a higher control bandwidth offers only a little help in further reducing the capacitor numbers. The chance and trend for high-frequency VRM design with small size depend on the use of capacitors with smaller ESR values, such as ceramic capacitors.

Chapter 3.   Adaptive Voltage Position Design for VRM

As a special power supply for the microprocessor, the VRM must maintain a low output voltage within a tight tolerance range during operation with a large current step change and high slew rate.

To meet such transient requirements, the VRM must use many output capacitors, which increase its size and cost. When the VRM first emerged, feedback control kept the output voltage at the same level for the entire load range. As a result, the output voltage spike during the transient had to be smaller than half of the voltage tolerance window. However, if the output voltage level is a little higher than the minimum value at full load and a little lower than the maximum value at light load, the whole voltage tolerance range can be used for the voltage jump or drop during the transient. This is the concept of adaptive voltage position (AVP) design [B37-B41]. Fig. 3.1 shows the transient comparison between non-AVP and AVP designs. It is very clear that the AVP design allows the use of fewer output capacitors, and hence reduces the VRM cost. Another benefit of the AVP design is that the VRM output power at full load is reduced, which greatly facilitates the thermal design. Also, the AVP design is indispensable for meeting the processor load-line specifications [B42, B43].

The AVP is related to the steady-state operation of the VRM. If the transients between the two steady-state stages have no spikes and no oscillations, as is the situation shown in Fig. 3.2 (a), the AVP design is optimal. The transient can take advantage of the entire voltage tolerance window. The comparison between the current and the related output voltage waveforms reveals that the VRM equals an ideal voltage source in series with a resistor $R_{O,}$ such that:

$$R_o = \Delta v_o / \Delta i_o \,. \tag{3.1}$$

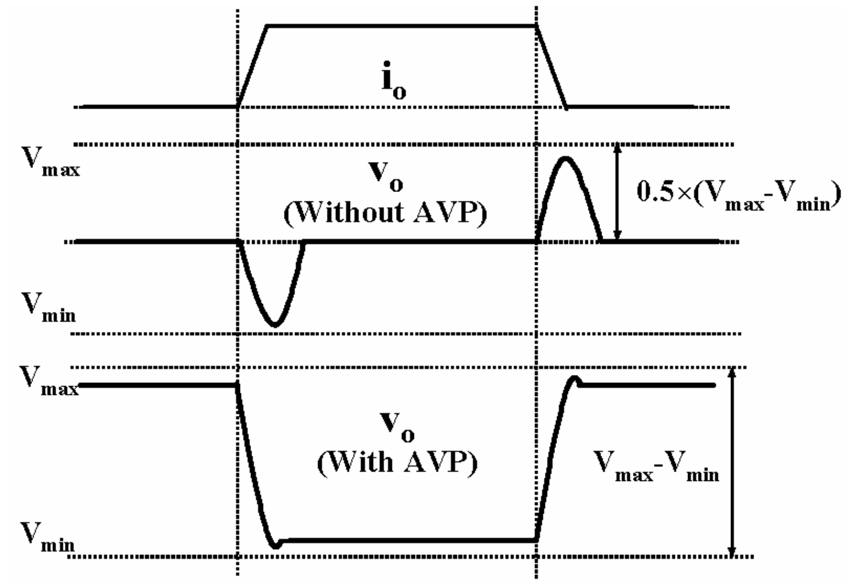


Fig. 3.1. Transient response without and with AVP designs.

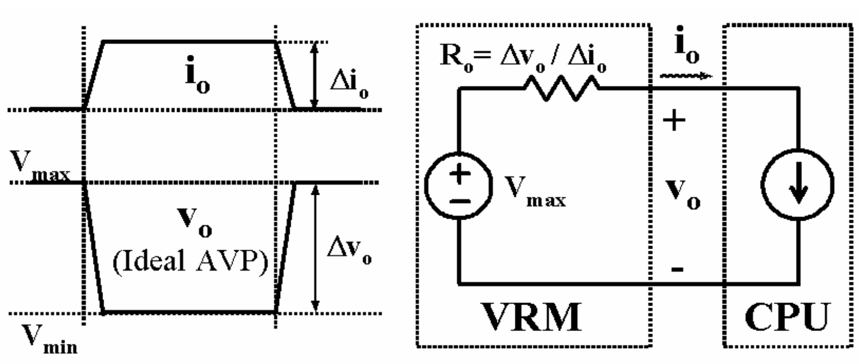


Fig. 3.2. (a) The ideal AVP design and (b) the equivalent circuit of the VRM.

Fig. 3.2 (b) shows the equivalent circuit of the VRM.

Now it is very clear that the constant resistive output impedance design for the VRM is an optimal design for the transient. Actually, improving the dynamic regulation of a converter based on the output impedance consideration is an old concept [B44-B52]. However, not every converter can achieve constant resistive output impedance. Additionally, it is not clear how to design the feedback control loop. This chapter clarifies these issues for all kinds of existing control methods. Different kinds of output capacitors are discussed for the AVP design based on the constant output impedance concept. Section 3.1 discusses the current-mode control, Section 3.2 discusses the active-drop control, and Section 3.3 extends the AVP design with ceramic output capacitors.

For the following analysis, the small-signal model uses a single-phase buck in continuous-current mode (CCM) to simplify the analysis of the multiphase VRM [B31, B32]. The ESL of the output capacitor is ignored here, since the high-frequency ceramic capacitors in parallel greatly reduce its effect. Also, the inductor design follows the critical inductance design, as discussed in Section 2.3.

3.1. Output Impedance Design Considerations with Current-Mode Control

Fig. 3.3 shows the dual-loop feedback control system in the current-mode control. Peak-current-mode control is used as an example for this analysis. Since the current-loop design is normally fixed according to the applied control chip, the major issue is how to design the voltage-loop compensator.

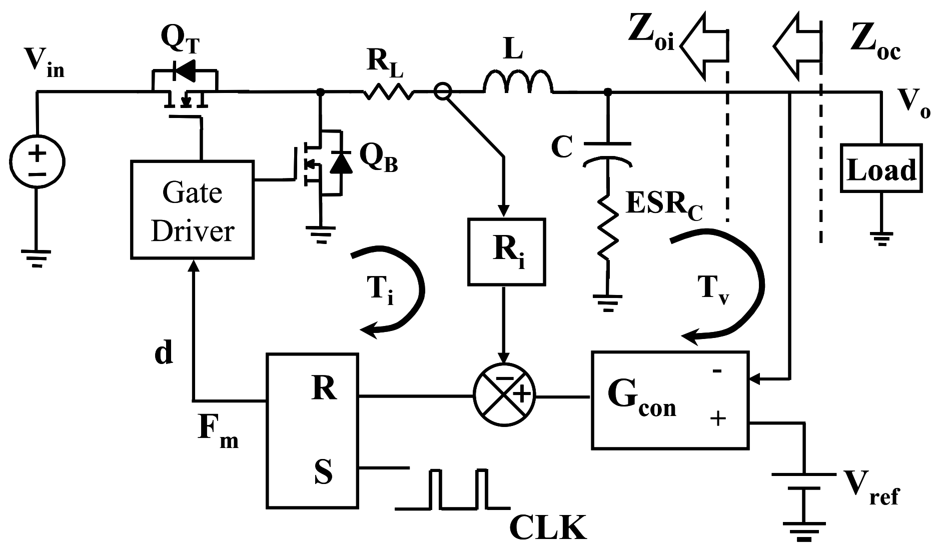


Fig. 3.3. A buck converter using current-mode control.

3.1.1. Small-Signal Model Analysis

Fig. 3.4 shows the small-signal block for the current-mode control. G_{ii} is the transfer function of inductor current i_L to load current i_o. G_{id} is the transfer function of the inductor current to the duty cycle. F_m models the inductor current ramp effect. G_i represents the current-sensing function, which normally is the current-sensing resistance R_i. G_{con} is the voltage-loop compensator transfer function.

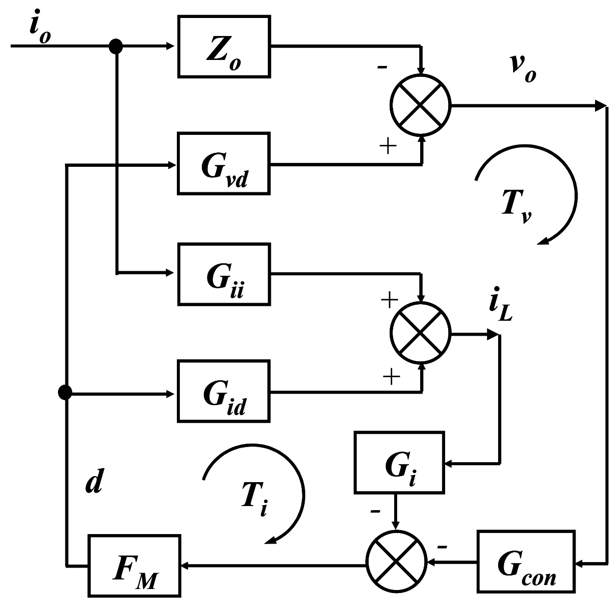


Fig. 3.4. The small-signal block for current-mode control.

$$Z_o(s) = R_L \frac{(1 + s/\omega_{ESR}) \cdot (1 + s/\omega_L)}{1 + s/(Q \cdot \omega_o) + s^2/\omega_o^{\ 2}} \tag{3.2}$$

$$G_{vd}(s) = V_{in} \frac{(1 + s/\omega_{ESR})}{1 + s/(Q \cdot \omega_o) + s^2/\omega_o^{\ 2}} \tag{3.3}$$

$$G_{ii}(s) = \frac{1 + s/\omega_{ESR}}{1 + s/(Q \cdot \omega_o) + s^2/\omega_o^{\ 2}} \tag{3.4}$$

$$G_{id}(s) = V_{in} \frac{s \cdot C}{1 + s/(Q \cdot \omega_o) + s^2/\omega_o^{\ 2}} \tag{3.5}$$

where $\omega_{ESR} = \dfrac{1}{C \cdot ESR_C}$, $\omega_L = \dfrac{L}{R_L}$, $\omega_o \approx \dfrac{1}{\sqrt{C \cdot L}}$, $Q \approx \dfrac{\sqrt{L/C}}{R_L + ESR_C}$ (3.6)

Here, R_L includes the DC resistance of the inductor L, the conduction resistance $R_{ds\text{-}on}$ of the MOSFETs Q_T and Q_B, and the parasitic resistance of the traces. The ESR_C is the ESR of the output capacitor C. The ω_o is the power stage double pole.

With the current loop closed, the output impedance with the open voltage loop is:

$$Z_{oi}(s) = Z_o(s) + \frac{T_i(s)}{1+T_i(s)} \cdot \frac{G_{vd}(s) \cdot G_{ii}(s)}{G_{id}(s)}, \tag{3.7}$$

where $T_i(s)$ is the current-loop gain:

$$T_i(s) = F_M \cdot G_{id}(s) \cdot R_i \cdot H_e(s). \tag{3.8}$$

where $H_e(s)$ models the current-sampling effect in current-mode control:

$$H_e(s) = 1 - \frac{s}{2 \cdot f_s} + \frac{s^2}{(\pi \cdot f_s)^2}. \tag{3.9}$$

The voltage-loop gain is:

$$T_v(s) = F_M \cdot G_{vd}(s) \cdot G_{con}(s). \tag{3.10}$$

3.1.2. Constant Output Impedance Design

The design for current-mode control to realize a stable system has already been discussed [B53-B55]. A high-bandwidth current-loop design can simplify the buck converter from a two-order system to a one-order system. When the current loop is closed and the voltage loop is open, the buck converter operates as an ideal current source, and its output impedance can be approximately represented as:

$$Z_{oi}(s) = \frac{1}{s \cdot C} + ESR_C = \frac{1 + s \cdot ESR_C \cdot C}{s \cdot C} = \frac{1 + s/\omega_{ESR}}{s \cdot C}. \tag{3.11}$$

Fig. 3.5 shows the simplified circuit for the current-mode control method. The power converter is changed from a second-order system to a first-order one. Fig. 3.6 shows the output impedance with current loop closed but voltage loop open. Since the controlled current source has infinite impedance, only the output capacitors contribute to the system output impedance.

When the voltage loop is closed, the closed-loop output impedance is:

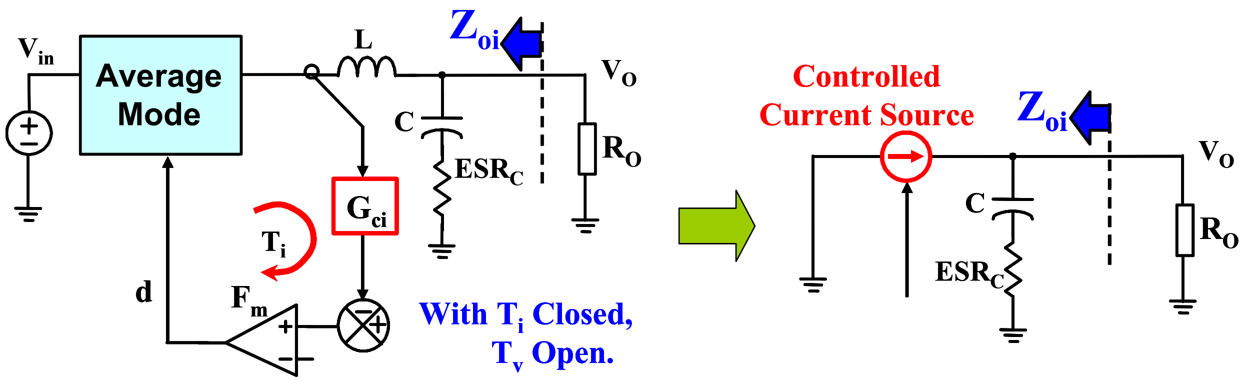


Fig. 3.5. Simplified circuit for the current-mode control.

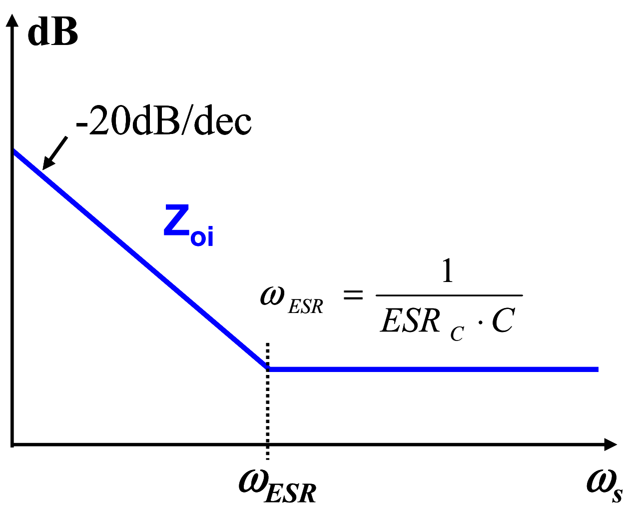


Fig. 3.6. The output impedance in the current-mode control with current-loop closed but voltage-loop open.

$$Z_{oc}(s) = \frac{Z_{oi}(s)}{1+T_2(s)} = \frac{(1+T_i(s)) \cdot Z_{oi}(s)}{1+T_i(s)+F_m \cdot G_{vd}(s) \cdot G_{con}(s)}, \tag{3.12}$$

where $T_2(s)$ is the outer-loop gain, which determines the system bandwidth and phase margin.

$$T_2(s) = \frac{T_v(s)}{1+T_i(s)} \tag{3.13}$$

With a logarithm union, the closed-loop output impedance is:

$$Z_{oc}(dB) \cong \begin{cases} Z_{oi}(dB) - T_2(dB) & (T_2 >> 1) \\ Z_{oi}(dB) & (T_2 << 1) \end{cases}. \tag{3.14}$$

For the output impedance Z_{oi}, the corner frequency is just at the capacitor ESR zero ω_{ESR}. Following the constant output impedance design concept, it is easy to derive that the system loop T_2 should be designed with a -20dB/dec slope and a bandwidth (ω_c) at ω_{ESR}. This bandwidth design is right on the critical value that is discussed in Chapter 2. Fig. 3.7 shows this clearly. Consequently, the desired system loop T_2 is:

$$T_2(s) = \frac{\omega_c}{s}. \tag{3.15}$$

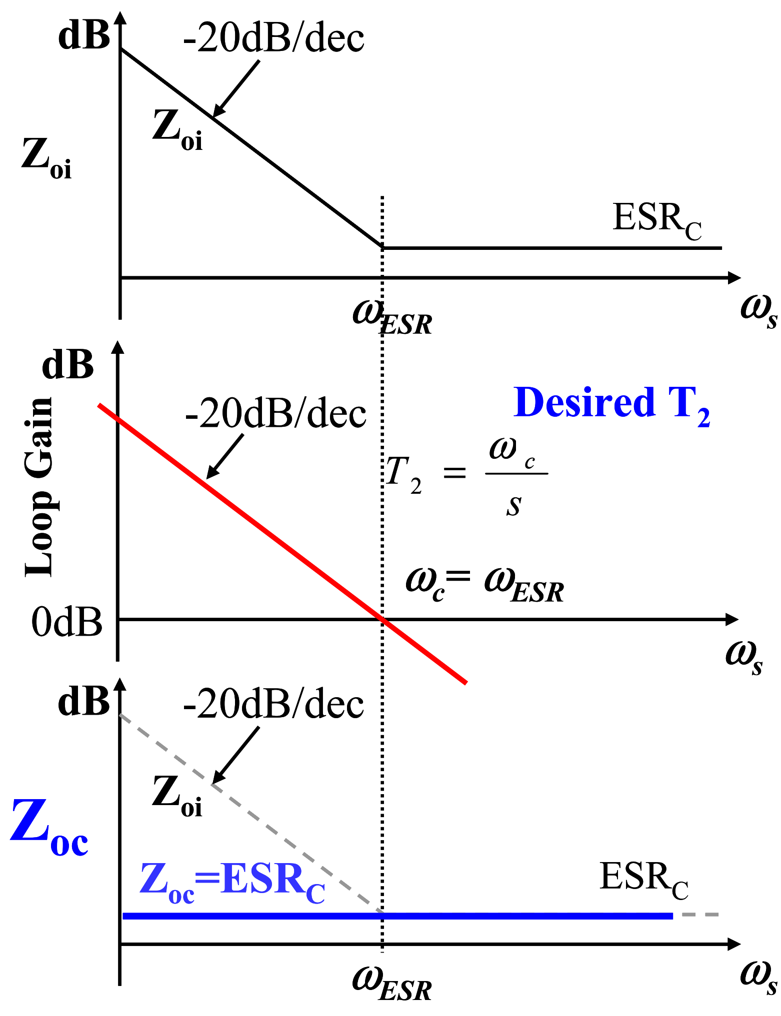


Fig. 3.7. The constant output impedance design for current-mode control.

If the current-loop bandwidth is much larger than the system bandwidth, (3.13) can be simplified as:

$$T_2(s) \approx \frac{T_v(s)}{T_i(s)} = \frac{G_{vd}(s) \cdot G_{con}(s)}{R_i \cdot G_{id}(s) \cdot H_e(s)}. \tag{3.16}$$

From (3.15) and (3.16), we can derive the desired compensator design as:

$$G_{con}(s) = \frac{R_i}{ESR_C} \cdot \frac{H_e(s)}{1 + s / \omega_{ESR}}. \tag{3.17}$$

As an approximation, we can put a zero at half of the switching frequency to simplify the compensator design. Fig. 3.8 shows a good match below half of the switching frequency.

$$G_{con}(s) \approx \frac{R_i}{ESR_C} \cdot \frac{1 + s /(\pi \cdot f_s)}{1 + s / \omega_{ESR}} \tag{3.18}$$

There is physical meaning for the compensator design. A pole compensates the output capacitor ESR zero, and a zero compensates the double right-half-plane zero introduced by the current sample and hold effect. The finite DC gain design adjusts the steady-stage output error in order to achieve AVP. Also, the current-mode control has none of the limitations that exist in voltage-mode control. The closed current loop makes the converter operate like a current source, which has very high output impedance at low frequencies. As a result, the outer loop T_2 requires a high DC gain to attenuate the output impedance at low frequencies. The high DC gain eliminates all the problems that existed in voltage-mode control.

Fig. 3.9 shows the closed-loop output impedance with this compensator design. It is almost constant.

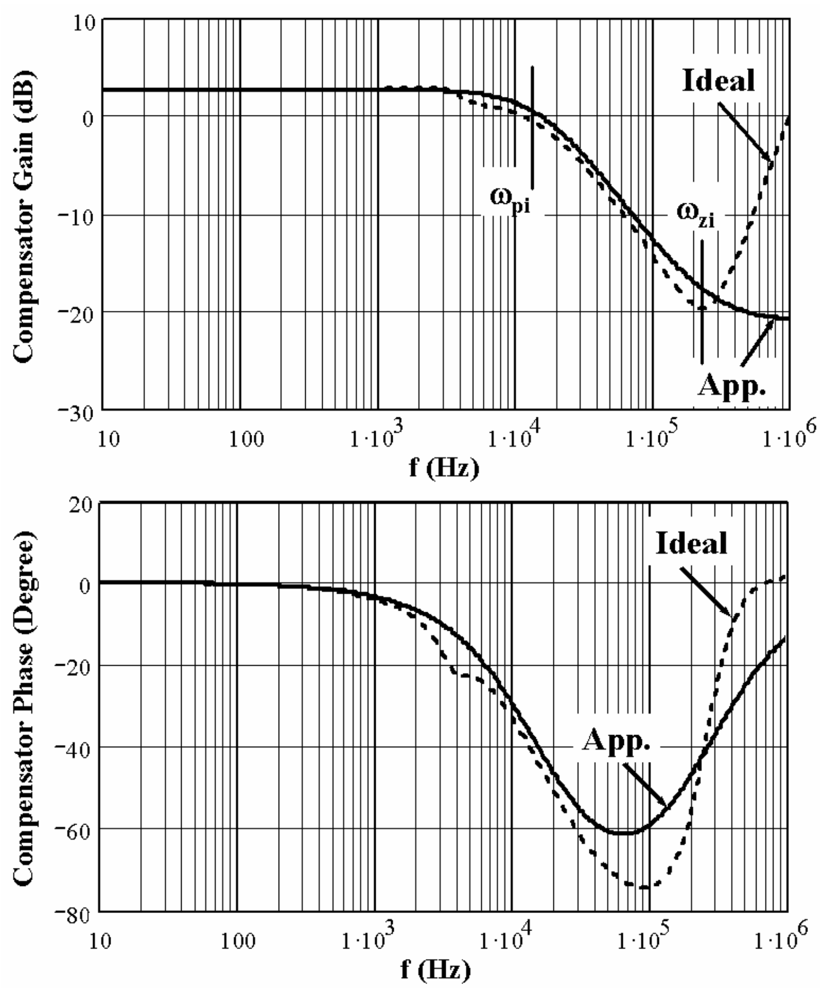


Fig. 3.8. Compensator design for current-mode control.

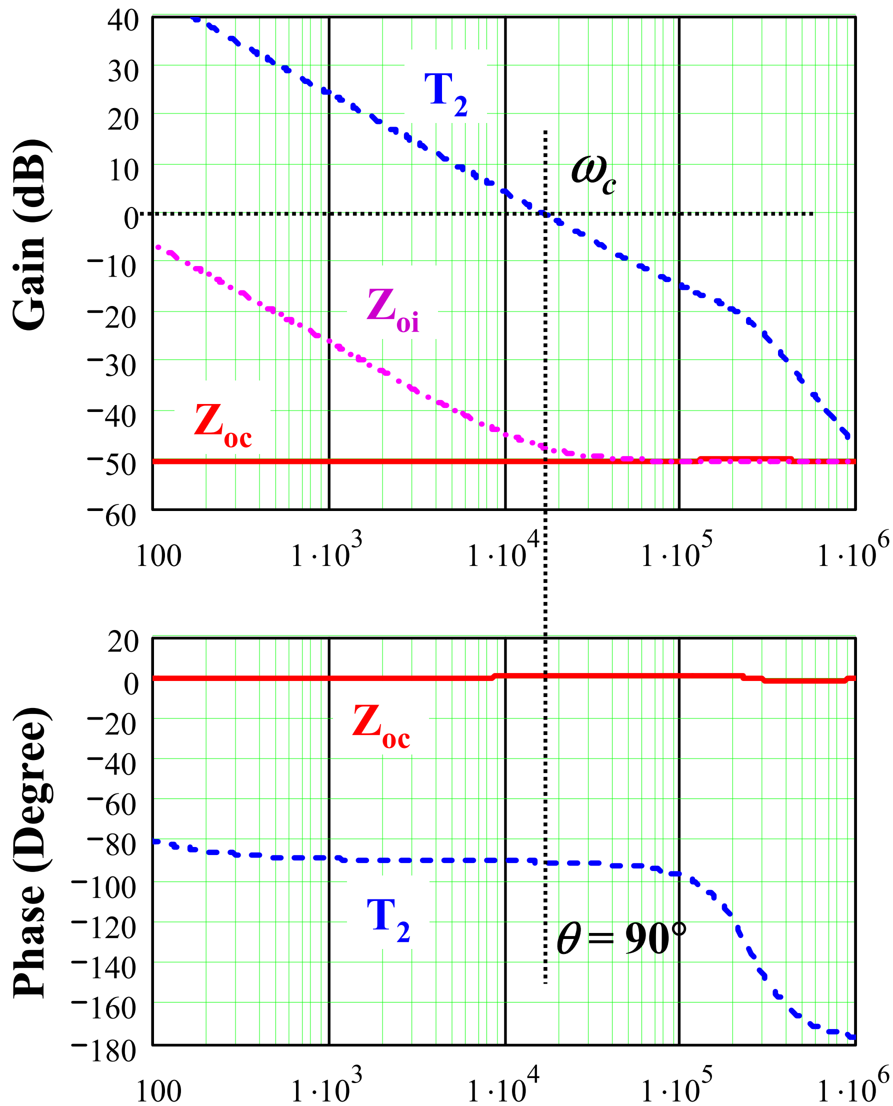


Fig. 3.9. The output impedance with the proposed compensator design in current-mode control.

3.1.3. Simulation and Experimental Results

A two-phase interleaved buck converter is designed for a 12V-to-1.5V/25A VR to verify the theoretical analysis. Fig. 3.10 shows the circuit. Four Oscon capacitors (820µF/4V) are used in parallel as the bulk output filter capacitor C_o. Each capacitor has an ESR of about 12 mΩ.

According to (3.6), the ESR zero of the output capacitor is about 16 KHz. A switching frequency of 300 KHz is good enough to achieve such a bandwidth, and at this frequency the VRM can achieve high efficiency. The output filter inductor in each phase is set at 1 μH, following the design guideline of the critical inductance discussed in Chapter 2. The ADP3160 two-phase controller from Analog Device is used. The compensator design follows the discussion in (3.18).

Fig. 3.11 shows the Simplis simulation results for the transient response. Fig. 3.12 shows the tested transient response waveform. Perfect AVP is achieved. Fig. 3.13 shows the extended transient waveforms during the step-up and step-down periods. With the critical inductance design, the duty cycle is not saturated during the transient response.

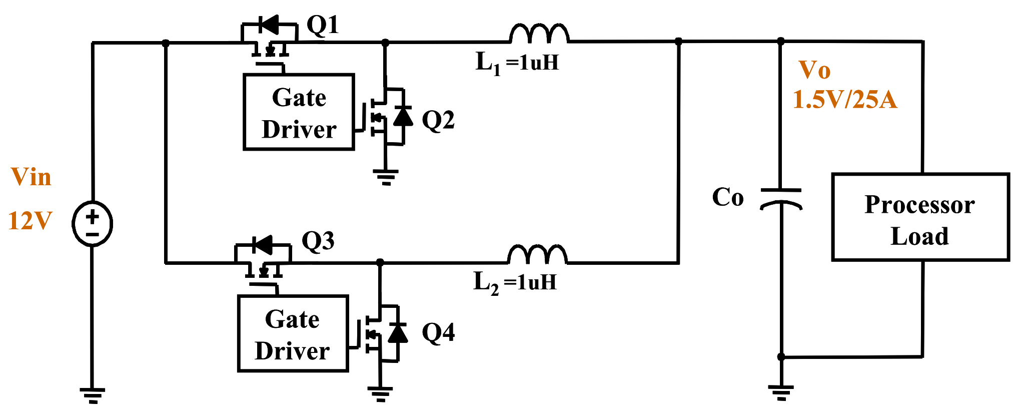


Fig. 3.10. The designed two-phase interleaved buck converter.

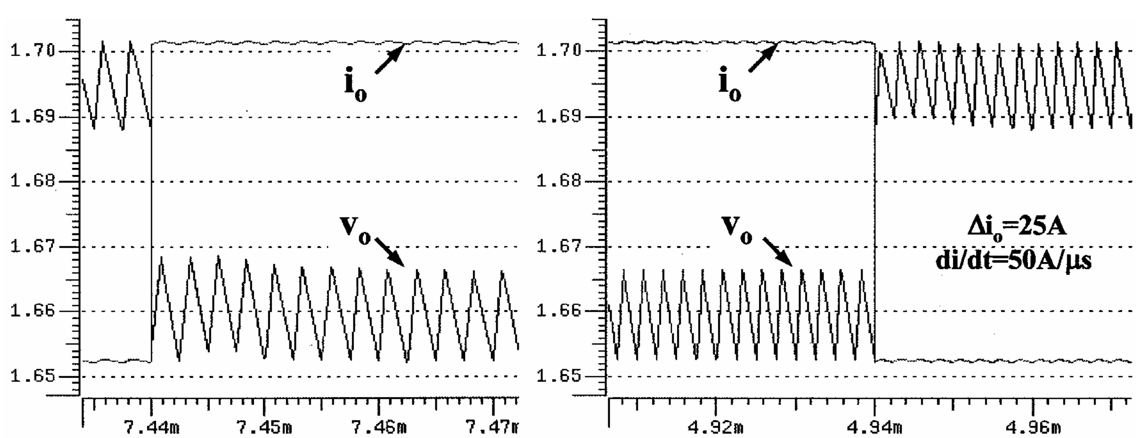


Fig. 3.11. Simulation results with current-mode control.

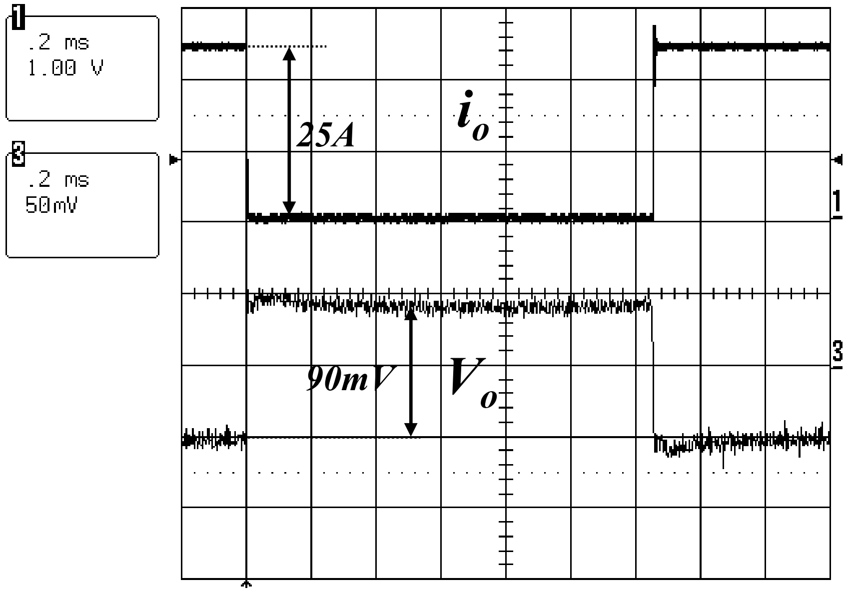


Fig. 3.12. Experimental results for the transient response in current-mode control.

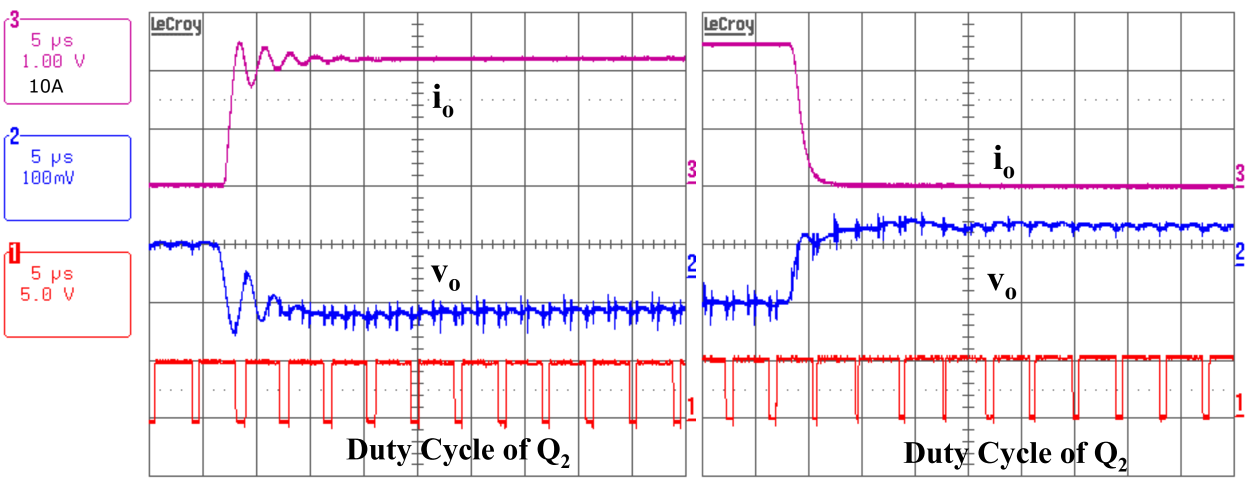


Fig. 3.13. Expanded waveforms for the transient response in current-mode control: (a) for step-up, and (b) for step-down.

The tested outer-loop bandwidth in Fig. 3.14 shows that the crossover frequency is exactly on the ESR zero of the output capacitor.

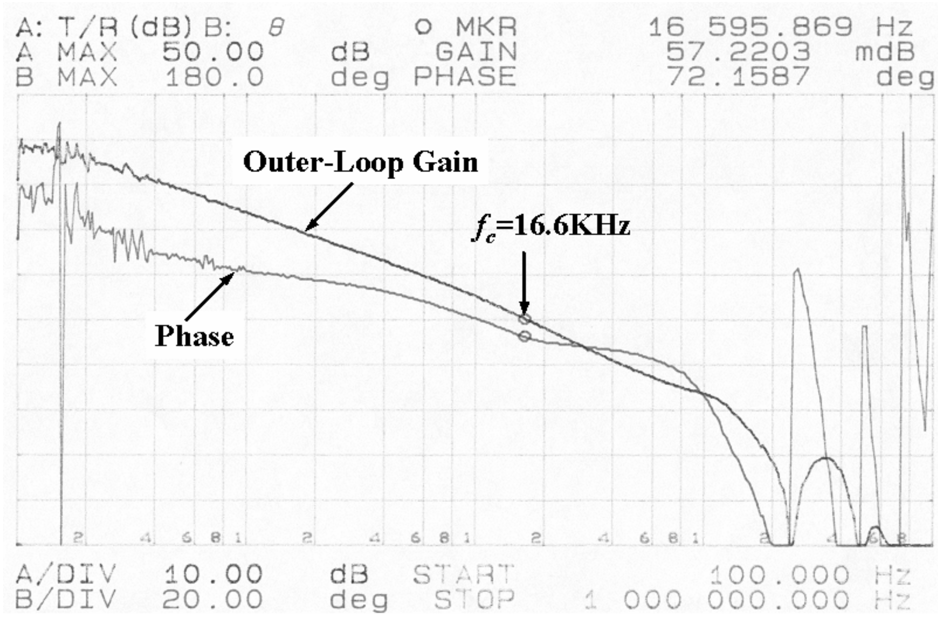


Fig. 3.14. The tested outer-loop gain and phase in current-mode control.

3.2. Output Impedance Design Considerations with Active-Droop Control

In current-mode control, the AVP design depends on the accuracy of the DC gain. A DC gain that is too small will introduce a greater output voltage error, but a DC gain that is too large cannot take advantage of the entire voltage tolerance window for the transient. Fig. 3.15 shows these limitations clearly.

As a result, the active-droop control method is proposed to solve these problems by using an infinite DC gain design for the feedback compensator [B10-11]. From the standpoint of the output characteristics of the VR, AVP control is comparable to introducing a droop function. Droop control has been widely discussed in applications involving current-sharing between multi-power supplies [B12-13]. However, there are few reports about its transient performance. Although Intersil, Fairchild and some other IC manufacturers have already developed control ICs for VRs based on the droop control idea, there is no design guideline for the feedback compensator, and good transient response cannot be achieved. This section clarifies all these issues.

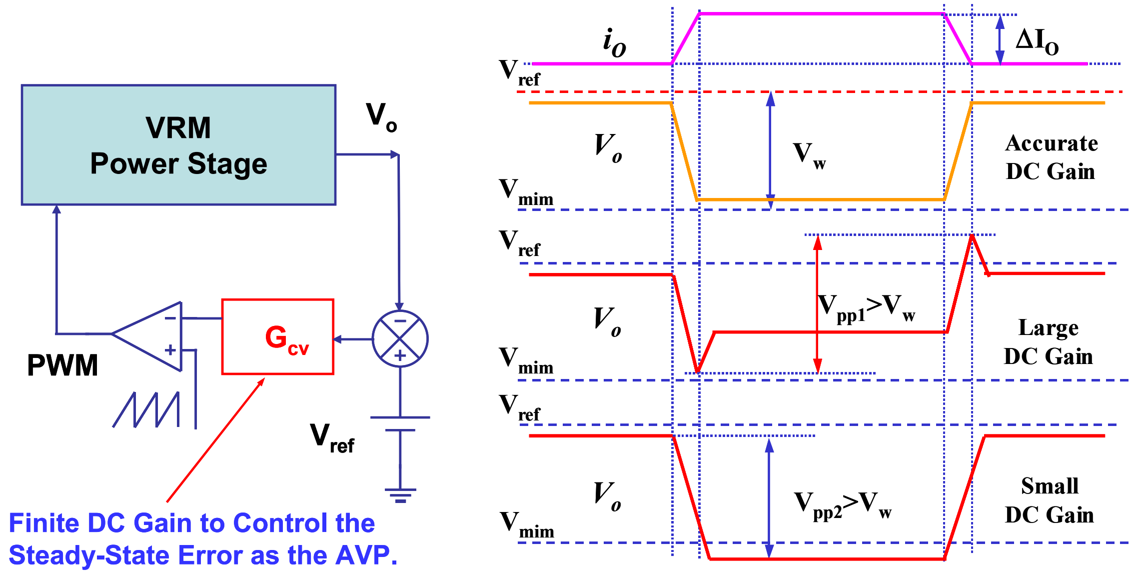


Fig. 3.15. The limitations of the finite DC gain to achieve AVP.

Fig. 3.16 shows the active-droop control concept, and Fig. 3.17 shows the circuit. The inductor current information is sensed and fed back to adjust the output voltage reference according to the droop requirement. Larger current means smaller voltage reference. (As a result, this control method is also referred to as current-injection control.) Then, the feedback control forces the output voltage to follow the voltage reference. The infinite DC gain of the feedback compensator A_v ensures that the values of the output voltage and the voltage reference are equal. Since the output voltage droop is related to the output load current, it can be controlled perfectly.

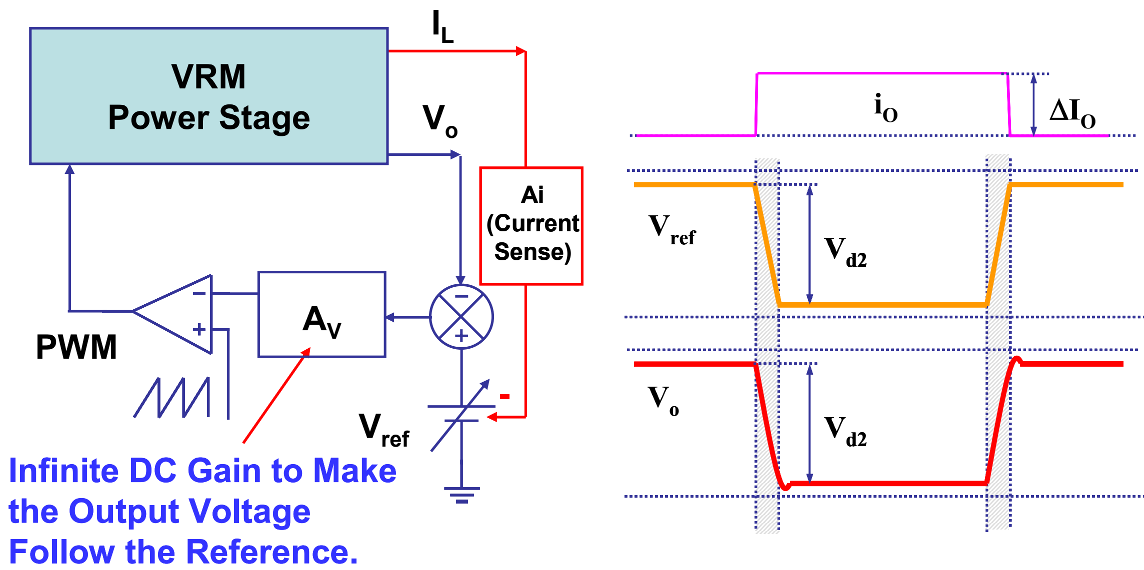


Fig. 3.16. The concept of active-droop control.

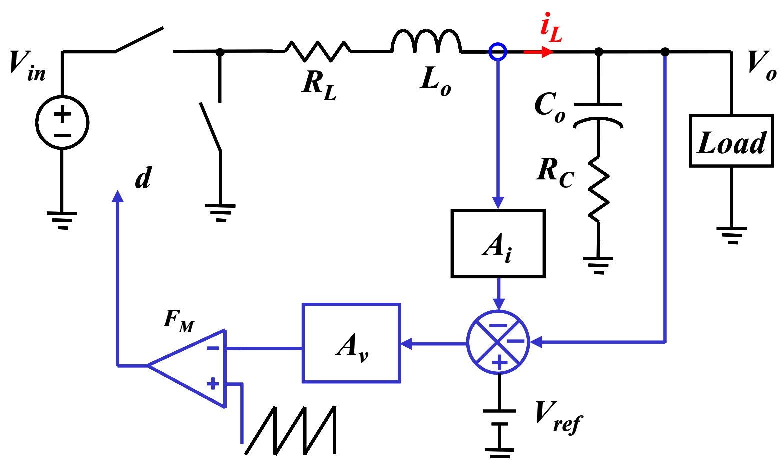


Fig. 3.17. A buck converter with active-droop control.

3.2.1. Small-Signal Model Analysis

Fig. 3.18(a) shows the small-signal block for active-droop control. A_i represents the current-sensing function, and A_v is the voltage-loop compensator transfer function. It is very clear that the active-droop control is a two-loop feedback system. The current loop T_i and voltage loop T_v are defined as:

$$T_i = A_v \cdot F_M \cdot G_{id} \cdot A_i \text{, and} \tag{3.19}$$

$$T_v = A_v \cdot F_M \cdot G_{vd} \,. \tag{3.20}$$

A comparison between Fig. 3.18 (a) and (b) shows that active-droop control is very similar to current-mode control. When G_{cv}=A_v and G_{ci}=A_i×A_v, these two small-signal blocks are equivalent. As a result, the active-droop control is a special case of current-mode control. The AVP design for the active-droop control method can simply follow the design for the current-mode control discussed in Section 3.1.

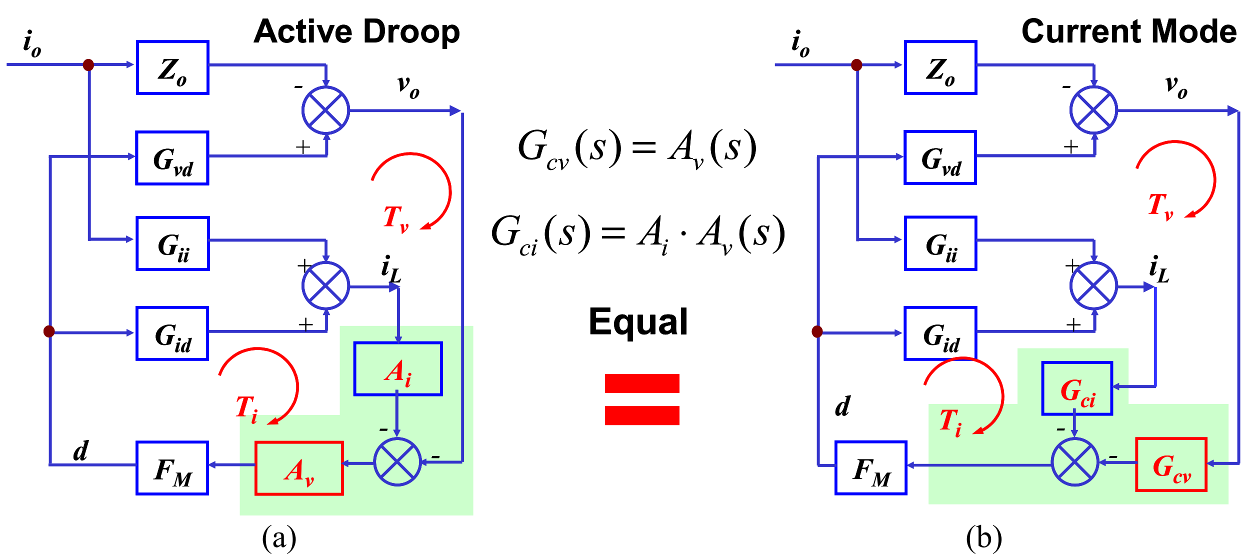


Fig. 3.18. The small-signal block comparison: (a) active-droop control, and (b) current-mode control.

However, there is a significant difference between these two control methods. In current-mode control, the current loop is inside of the voltage loop. The designs of G_{ci} and G_{cv} can be separated. But in active-droop control, the information about both current and voltage is fed back and then the two values are added together. The compensator design of A_v influences both the current and voltage loops, and requires an infinite DC gain.

3.2.2. Constant Output Impedance Design

For active-droop control, (3.13) becomes

$$T_2(s) \approx \frac{T_v(s)}{T_i(s)} \approx \frac{1+s/\omega_{ESR}}{A_i \cdot C_o \cdot s}. \tag{3.21}$$

Normally, A_i is designed with the specified R_{droop}, which is the DC output impedance. If the control bandwidth is lower than the ESR zero, (3.21) can be further simplified as:

$$T_2(s) \approx \frac{1}{R_{droop} \cdot C_o \cdot s} = \frac{\omega_c}{s}, \tag{3.22}$$

which is exactly the desired outer-loop design. And the compensator design $A_v(s)$ has no impact as long as it can meet the design assumption; i.e., the current loop must have high control bandwidths.

Then the compensator design for active-droop control is relatively simple. The current-loop design guideline in the average current-mode control can be applied here, as follows:

$$A_v = K \cdot \frac{1+s/\omega_o}{s \cdot (1+s/\omega_p)}. \tag{3.23}$$

An integrator is used to eliminate the steady-state error. A zero is used to compensate the system double pole. A pole in the high-frequency range can be used to further attenuate the switching noise, but it can be omitted to simplify the compensator design. The K is designed to achieve a high current-loop bandwidth ω_{ci}.

For $\omega_c \ll \omega_{ESR}$, the K can be expressed as:

$$K = \frac{\Delta(\omega_{ci}) \cdot \omega_c}{F_M \cdot V_{in} \cdot (1 + \omega_{ci} / \omega_o)}, \tag{3.24}$$

where $\Delta(s) = \frac{1}{1 + s/(Q \cdot \omega_o) + s^2 / \omega_o^2}$. (3.25)

Fig. 3.19 shows the outer loop T_2 with the proposed compensator design for active-droop control with Oscon output capacitors. It approximates very well to the desired design in (3.22). It is very interesting that all three loops (T_i, T_v and T_2) have almost the same control bandwidths at the capacitor ESR zero. Fig. 3.19 also shows the closed-loop output impedance with this compensator design. It is almost constant.

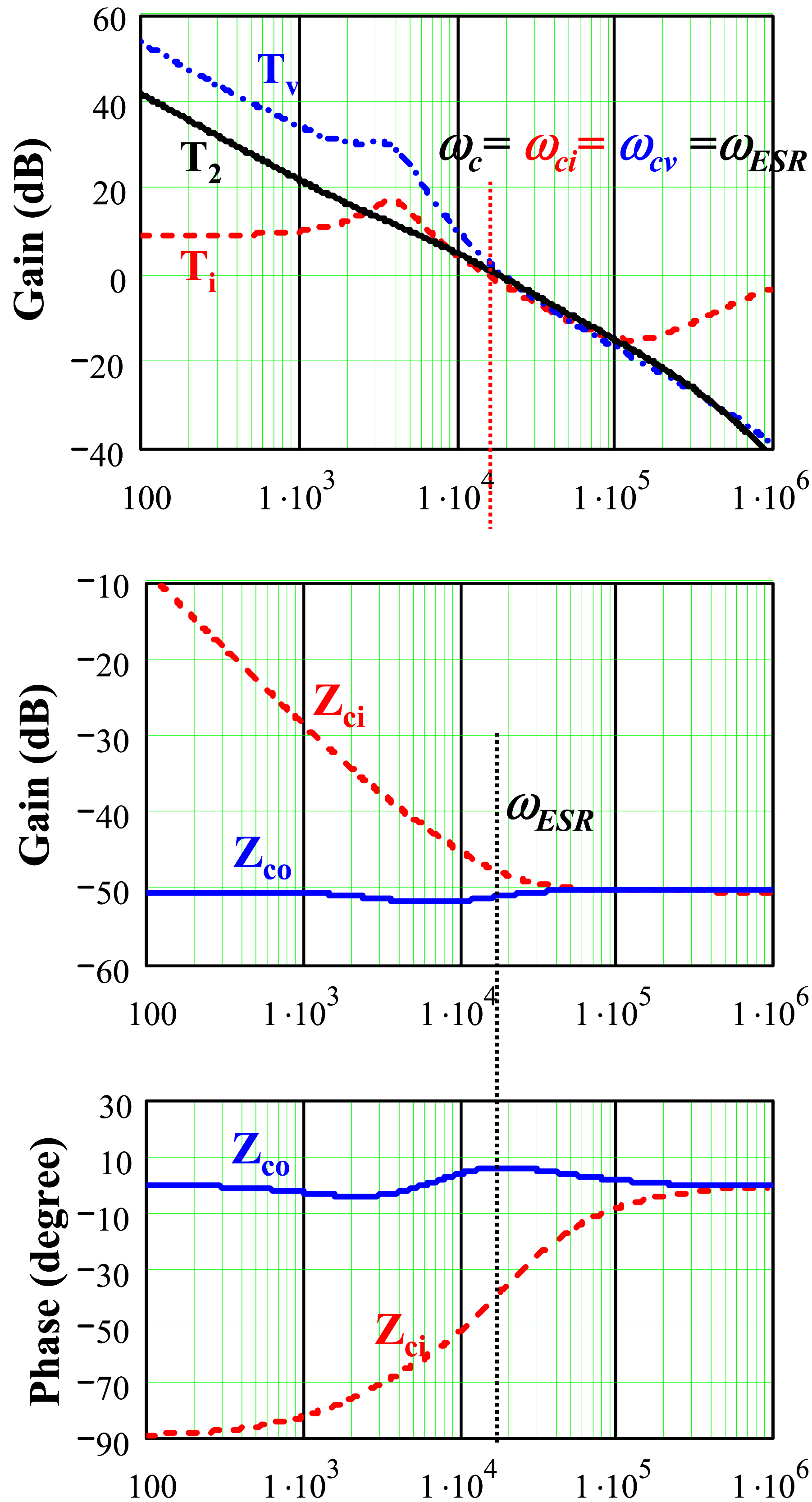


Fig. 3.19. The loop gain and output impedance for active-droop control.

3.2.3. Simulation and Experimental Results

A two-phase interleaved buck converter for a 12V-to-1.5V/25A VR is also simulated in PSpice to verify the theoretical analysis for the active-droop control method. Fig. 3.10 shows the circuit. All the parameters are the same as those of the current-mode control simulation discussed in Section 3.1.3. Fig. 3.20 shows the simulation results for the transient response. Perfect AVP is achieved.

A demonstration board (four-phase interleaved buck converter for a 12V-to-1.3V/90A VR, shown in Fig. 3.21) from Intersil is used to test the AVP design with the proposed compensator design. The controller is ISL6561. Fig. 3.22 shows the tested transient response waveform. Perfect AVP is achieved.

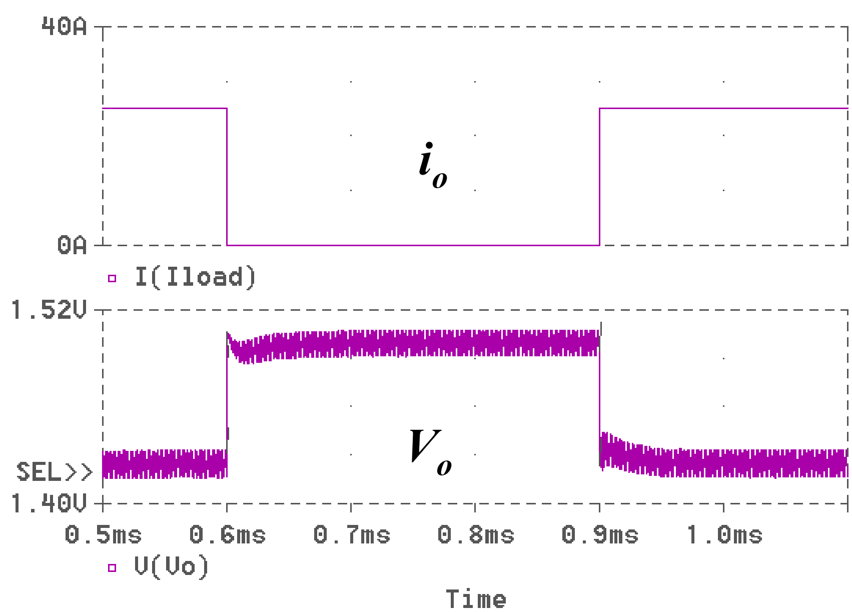


Fig. 3.20. Simulation result for the transient response with active-droop control.

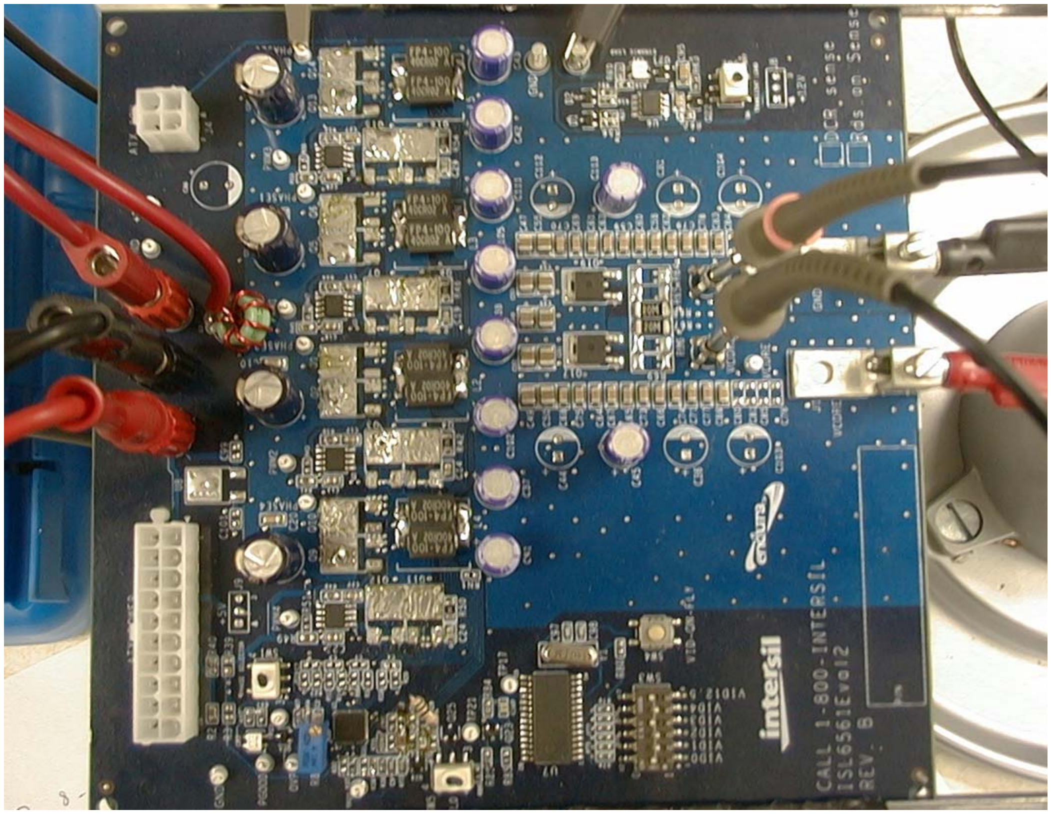


Fig. 3.21. The test hardware for the active-droop control method.

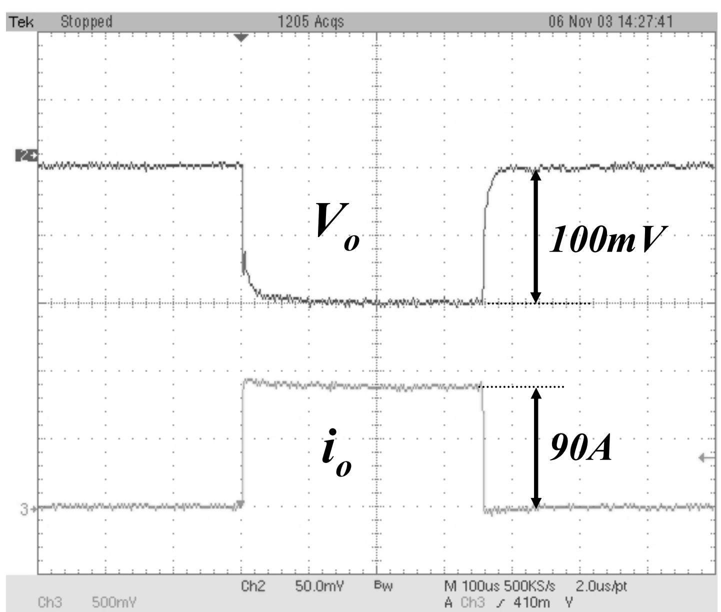


Fig. 3.22. The test transient waveforms with active-drop control method (with Oscon output capacitors).

3.3. AVP Design for Ceramic Capacitors

The preceding analysis shows that in order to achieve a constant output impedance design, the control bandwidth must be designed right on the critical bandwidth, which is the output capacitor ESR zero. However, the ESR zero for ceramic capacitors is in the MHz frequency range. For a practical design with switching frequencies of less than 2 MHz, it is impossible to realize such a high control bandwidth. Then, the question remains of how best to achieve the AVP design.

If the output impedance within the control bandwidth is still a constant resistance, then it determines the steady-state output voltage position. The output impedance beyond the control bandwidth determines how the voltage changes from one steady-state to another during the transient period. As long as the impedance value at high frequencies is smaller than that in the low frequencies, perfect AVP can still be achieved.

Fig. 3.23 shows this design situation. The desired system loop T_2 is still as determined in (3.22), but with $\omega_c < \omega_{ESR}$. The designed output impedance within the control bandwidth is:

$$R_{DC} = \frac{1}{\omega_c \cdot C}. \tag{3.26}$$

Following the method explained in Section 3.2.3, the final compensator design is as follows:

$$G_{con}(s) \approx \frac{R_i}{R_{DC}} \cdot \frac{1 + s/(\pi \cdot f_s)}{1 + s/\omega_{ESR}} = R_i \cdot C \cdot \omega_c \cdot \frac{1 + s/(\pi \cdot f_s)}{1 + s/\omega_{ESR}}. \tag{3.27}$$

The design method for pole and zero is the same as that for the Oscon capacitors. The only difference is the DC gain, which is related to the required control bandwidth and the total output capacitance value.

Fig. 3.24 shows the closed-loop output impedance with this compensator design. It is constant within the control bandwidth. Fig. 3.25 shows the simulation results for a two-phase 12V-to-1.5V/50A VRM design. Perfect AVP is achieved. The switching frequency is set at 1 MHz in order to achieve a control bandwidth at 130 KHz. The output filter uses eight ceramic capacitors (100µF/6.3V) in parallel.

Fig. 3.26 shows the experimental results by using the demonstration board shown in Fig. 3.21. The output ceramic capacitors are 10 ceramic capacitors (100µF/6.3V) in parallel. Perfect AVP is achieved. Fig. 3.27 shows the tested outer-loop bandwidth and phase.

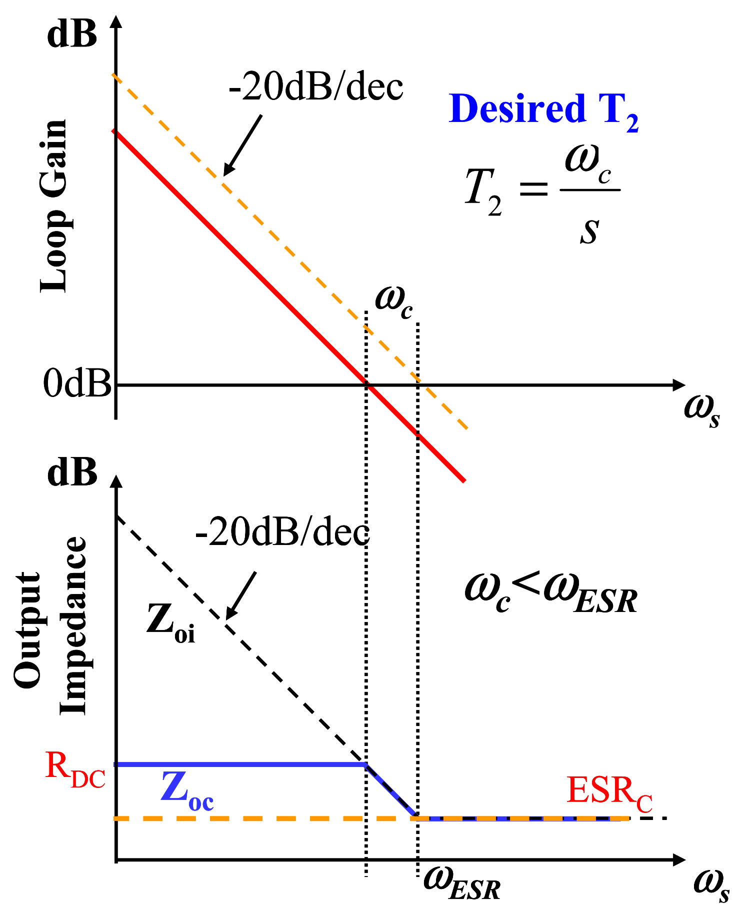


Fig. 3.23. Concept for constant output impedance design within the ceramic output capacitors.

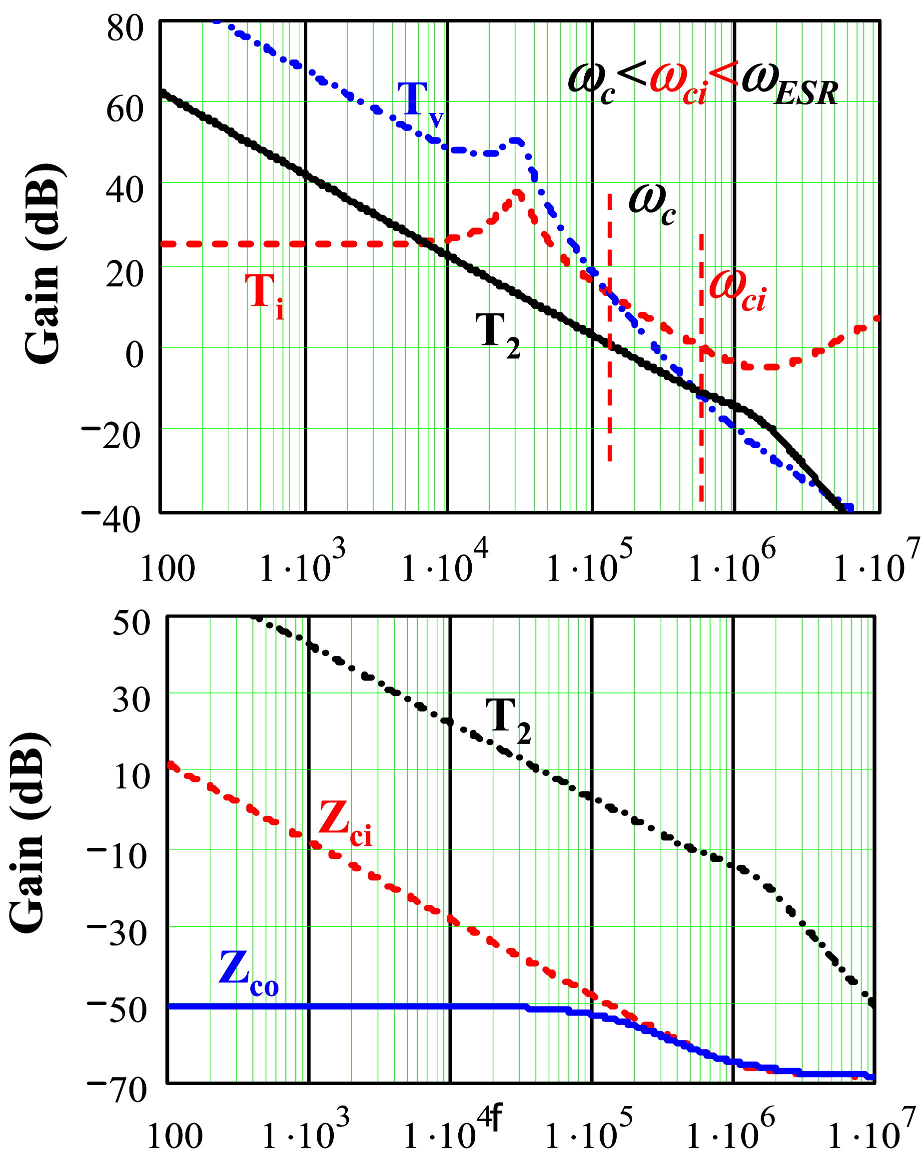


Fig. 3.24. Constant output impedance design within the control bandwidth for the ceramic output capacitors.

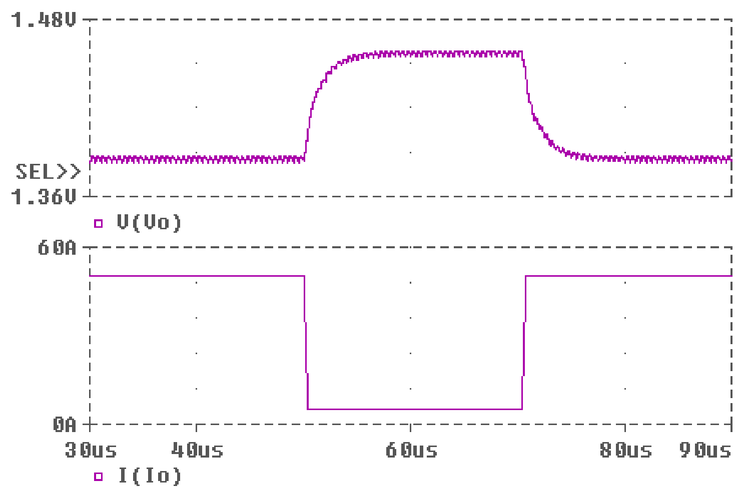


Fig. 3.25. Simulation results for the transient response with ceramic capacitor design.

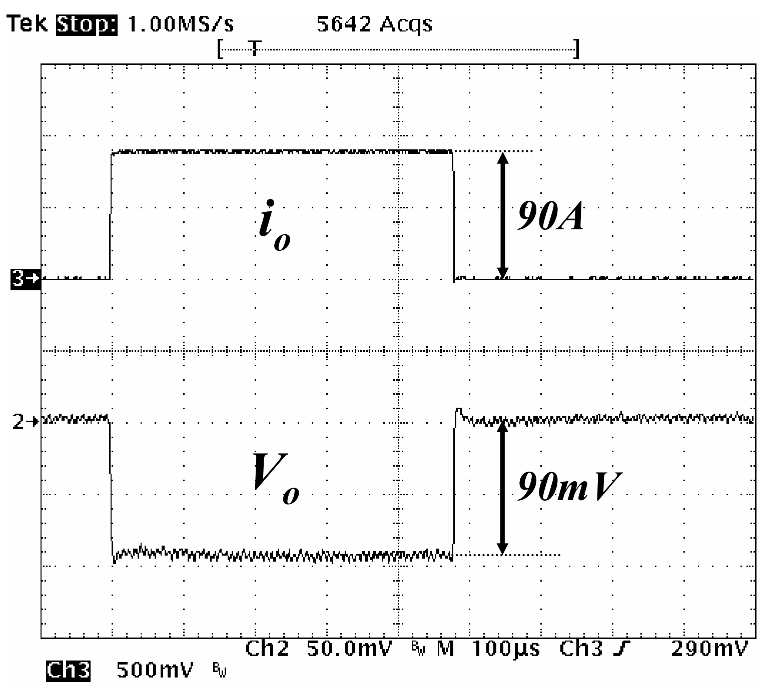


Fig. 3.26. The test transient waveforms with active-droop control method (with ceramic output capacitors).

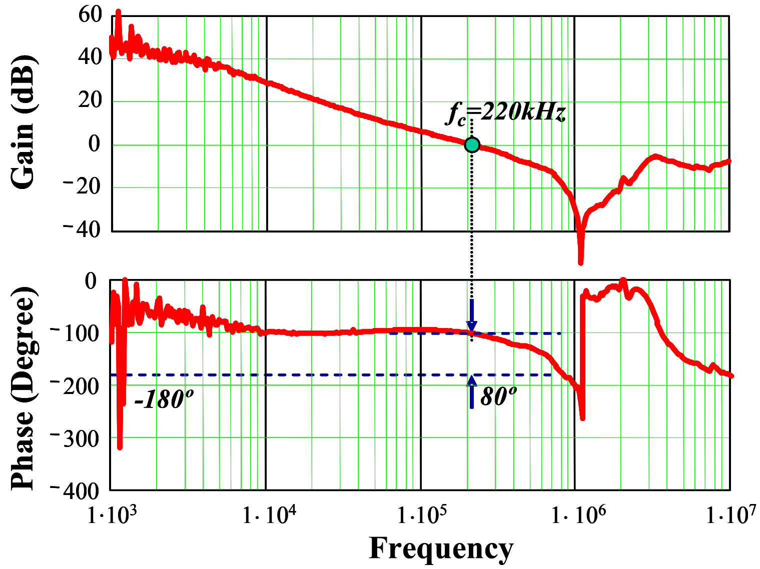


Fig. 3.27. The measured loop gain and phase with active-droop control (with ceramic capacitors).

3.4. Summary

This chapter proposes the concept of constant output impedance design for the VRM to achieve AVP. All existing control methods are covered for different kinds of output filter capacitors. Based on the small-signal model analysis, the open-loop and closed-loop output impedances are discussed. Following the proposed design guidelines, simulation and experimental results demonstrate very good VR transient response.

Chapter 4. High-Frequency Topologies Based on PWM Control

The state-of-the-art design for VRMs is based on the multiphase interleaving buck topology. The input bus voltage changes from 5 V to 12 V, since a higher bus voltage can reduce the conduction loss and cut the input filter size. However, the output voltage will go below 1 V in the near future. Such high-step-down DC-DC conversion causes a problem of very small duty cycle, which compromises the steady-state and dynamic performances. Section 4.1 analyzes the limitations in detail.

Further modification with additional coupled windings in the multiphase buck converter yields two novel topologies, which significantly improve the efficiency without compromising the transient response. The efficiency improvement is based on the duty cycle being extended by using multi-winding coupled inductors. Integrated magnetic structures are proposed for these windings so that the same magnetic cores used in the buck converter can be used here as well. Furthermore, it is easy to implement a lossless clamp circuit to limit the device voltage stress and to recover inductor leakage energy. Sections 4.2 and 4.3 explain these two novel topologies in detail.

The concept of applying winding coupling is extended in Section 4.4. With an autotransformer, a family of buck-type DC-DC converters is derived, including forward, push-pull, half-bridge, and full-bridge topologies. It is easy to understand that the autotransformer can help to extend the duty cycle. Compared with an isolated transformer, the autotransformer has a simpler winding structure, and it only needs to transfer part of the input power, which results in a smaller secondary winding current. Analysis shows that the autotransformer can also help to reduce the voltage stress and current ratings of power devices in the DC-DC converters.

4.1. The Multiphase Buck Converter

Fig. 4.1 shows a multiphase buck topology for VRM design. For the desktop application, the VRM is designed on the motherboard beside the microprocessor in order to reduce the interconnection parasitics in the power-delivery path. The VRM must have small size because of space limitations. The case is even under more stringent requirement in the laptop application, where the size and weight are more critical. The VRM deign for server applications requires a 1U profile and asks for much higher power density. However, the passive components, including the bulk output filter capacitors and inductors, are the bottleneck for further reduction of the VRM size. Increasing the switching frequency is the only way to solve this problem.

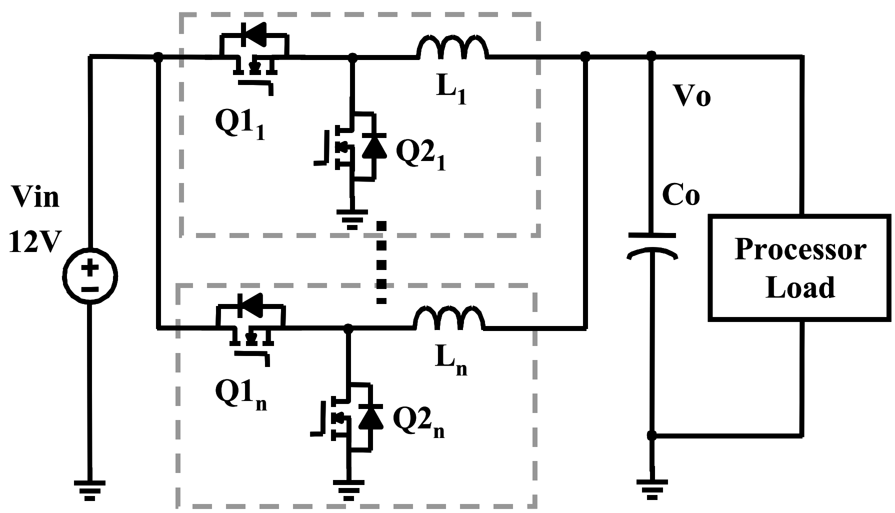


Fig. 4.1. Multiphase interleaved buck converter.

4.1.1. Limitations of the Buck Converter

As a result, the high-frequency, high-step-down DC-DC converter is required for VRM applications. But the conventional buck topology is no longer suitable. The first reason is the too-small duty cycle with 12V input:

$$D = \frac{V_o}{V_{in}} = M \ , \tag{4.1}$$

where M is the voltage gain for a DC-DC converter.

The duty cycle is completely determined by the voltage gain. For high-step-down DC-DC conversion, the duty cycle becomes very small. Consequently, the regulation period is very short, which is much worse in high-frequency applications. However, all pulse-width modulation (PWM) controllers have the limitation of a minimum controllable on-time. It is difficult to maintain the circuit control with a duty cycle of less than 10% at switching frequencies over 1 MHz. At the same time, it is problematic for the gate drive to turn the top switch off and on in such a short period. Before the switch is fully turned on, it must be turned off. The top switch will mostly work in the linear operation range, and hence causes significant loss. Also, some control methods that sense the peak current cannot be used, since there is not enough time for current-sensing. Another drawback of the small duty cycle is the poor ripple cancellation effect for both the input and output currents [C1]. More input filter capacitors are needed to filter the high-pulse input current, and more output capacitors are needed to reduce the steady-state output voltage ripple.

Fig. 4.2 shows the relationship between the output current ripple and the duty cycle and phase number. With a duty cycle of 0.25, the output current ripple can be perfectly canceled by four-phase interleaving. However, when the duty cycle is reduced to 0.1, the cancellation effect is limited. In Fig. 4.2, the output current ripple is normalized against the inductor current ripple at zero duty cycle, as follows:

$$\Delta I_{LN} = \frac{V_o}{L_{CH} \cdot f_s}, \tag{4.2}$$

where L_{CH} is the inductance value of each phase, and f_s is the switching frequency.

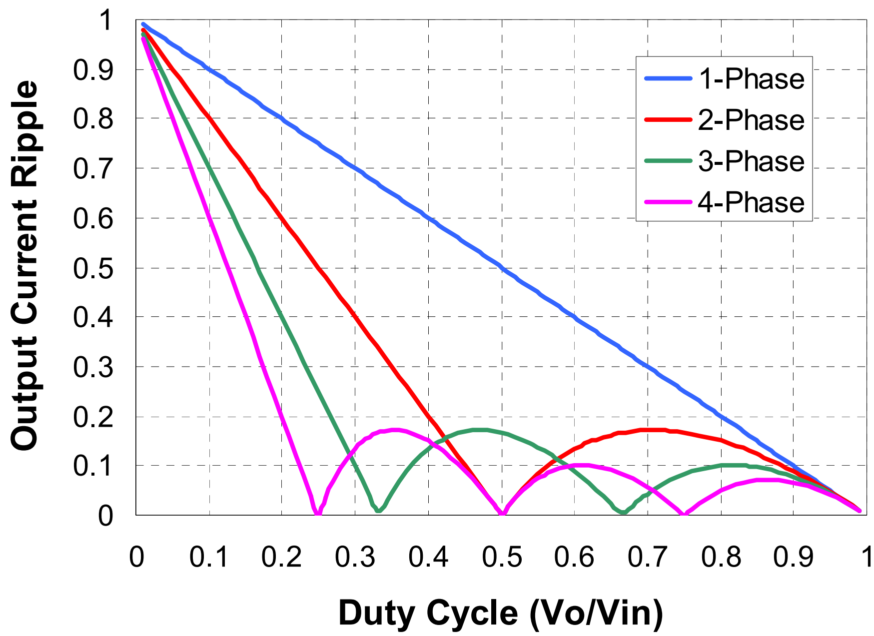


Fig. 4.2. Normalized output current ripple vs. duty cycle and phase number.

The most serious problem of the synchronous buck converter operating with very small duty cycle is its low efficiency, especially for high-frequency applications. Fig. 4.3 shows the measured efficiency comparison under input voltages V_{IN}=12 V (D=0.125) and VIN=5 V (D=0.3). The measured efficiency data include the power losses in the power stage and gate drive. At the same 500KHz switching frequency, the smaller duty cycle results in an efficiency drop of about 5% at full load. The higher switching frequency application with 1 MHz causes another 5% efficiency drop.

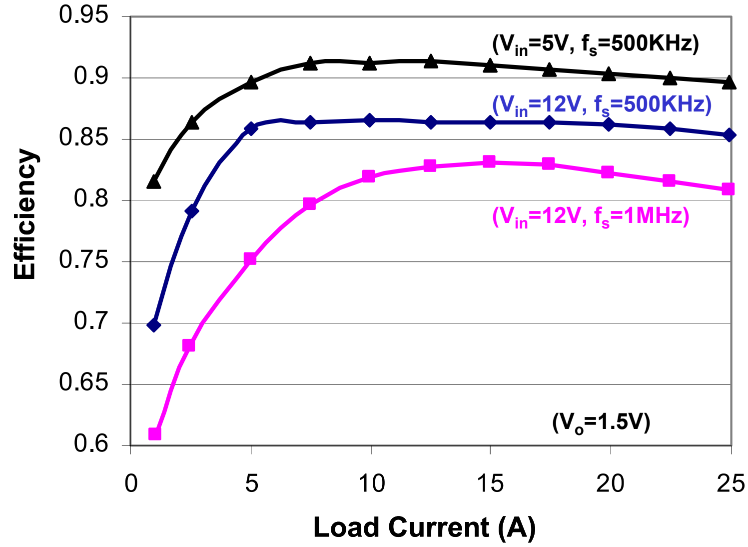


Fig. 4.3. Measured efficiency of a two-phase buck VRM under V_{IN}=5 V, 12 V and f_s=500 KHz, 1 MHz.

Fig. 4.4 shows the loss analysis results for a 12V-to-1.5V/12.5A synchronous buck converter, according to the method discussed in L. Spaziani's work [C2]. The results can be scalable to multiphase higher-output-current conditions, for example, a four-phase 50A VRM. The power devices are based on Hitachi's HAT2116H (for the top switch) and HAT2099H (for the bottom switch). To simplify the analysis, the inductor current ripples remain the same (25% of the load current) at different switching frequencies. As a result, at different switching frequencies, the conduction losses are the same. A 5V drive voltage is used in the loss analysis because of its low level of drive loss.

It is very clear that at high frequencies, the switching-related loss dominates the entire power loss and causes a significant drop in efficiency. Fig. 4.5 shows this trend. The major contribution to the switching-related loss comes from the top-switch switching loss and the bottom-switch body diode reverse-recovery loss, which are shown as follows:

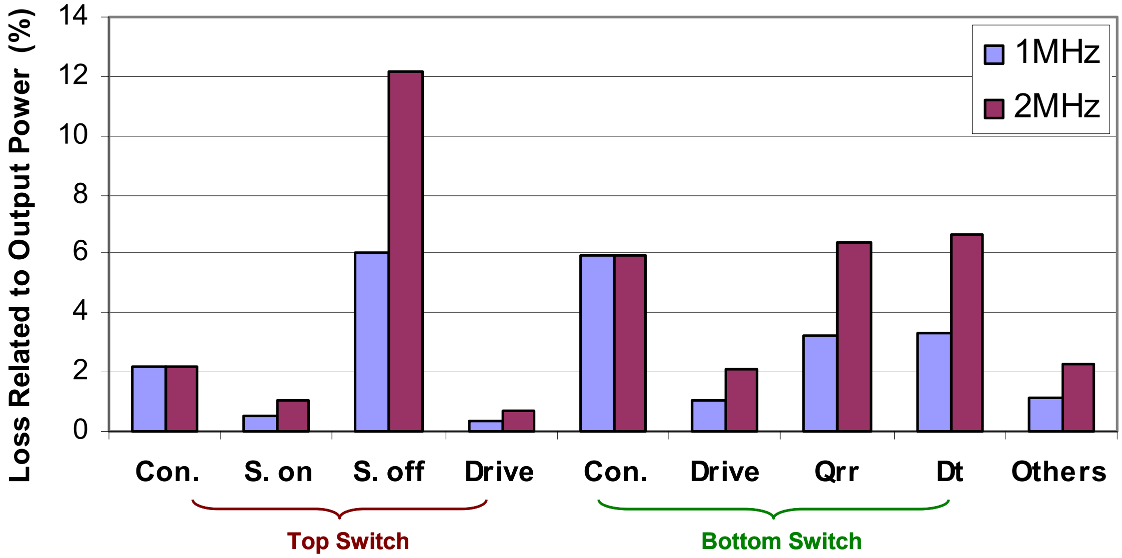


Fig. 4.4. The loss analysis for a synchronous buck converter.

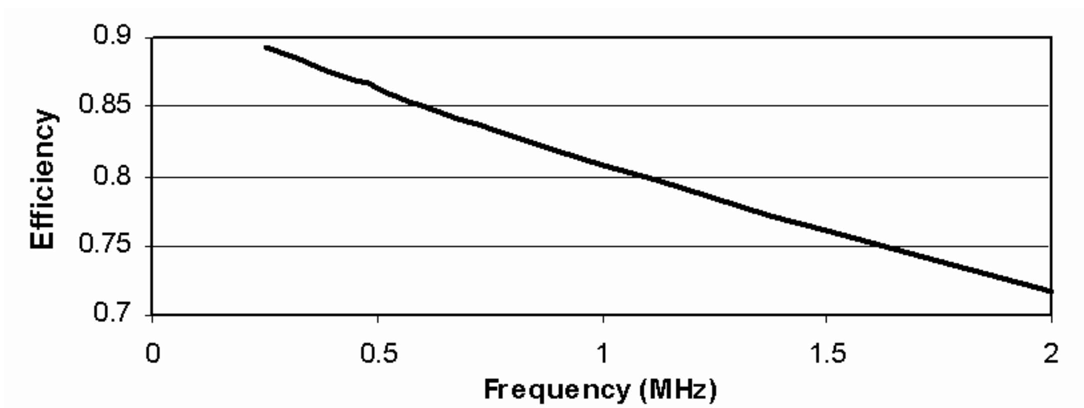


Fig. 4.5. Full-load efficiency vs. switching frequency.

$$L_{s\_top} \approx f_s \cdot V_{ds1} \cdot (i_{s\_on} \cdot t_{s\_on} + i_{s\_off} \cdot t_{s\_off}), \text{ and} \tag{4.2}$$

$$L_{s\_bottom} \approx f_s \cdot V_{ds2} \cdot Q_{rr}, \tag{4.3}$$

where f_s is the switching frequency, V_{ds1} is the top-switch voltage stress, i_{s_on} and i_{s_off} are the top-switch turn-on and turn-off currents, t_{s_on} and t_{s_off} are the relative turn-on and turn-off times, V_{ds2} is the bottom-switch voltage stress, and Q_{rr} is the diode reverse-recovery charge. For buck converters:

$$V_{ds1}=V_{ds2}=V_{in}. \tag{4.4}$$

Changing the input voltage from 5 V to 12 V, the voltage stresses of both the top and bottom switches are increased. As a result, the top-switch switching loss and the bottom-switch body diode reverse-recovery loss are significantly increased.

4.1.2. Idea to Extend the Duty Cycle

In order to avoid such an excessively small duty cycle in the high-step-down DC-DC conversion, transformers are usually incorporated into topologies. These isolated topologies include forward, half-bridge and full-bridge converters, the equivalent circuit of which is still a buck converter. The duty cycle can be adjusted to a desirable value by controlling the transformer turns ratio "n" as:

$$D = n \cdot \frac{V_o}{V_{in}} = n \cdot M \ . \tag{4.5}$$

Fig. 4.6 shows the impacts of the extended duty cycle, using the example of a doubled duty cycle. The switching current of the top switch and the voltage stress of the bottom switch are reduced by half. According to (4.3) and (4.4), the related switching loss and bodydiode reverse recovery loss can be reduced by half. Fig. 4.7 shows the expected loss reduction, which can improve the efficiency by about 4%.

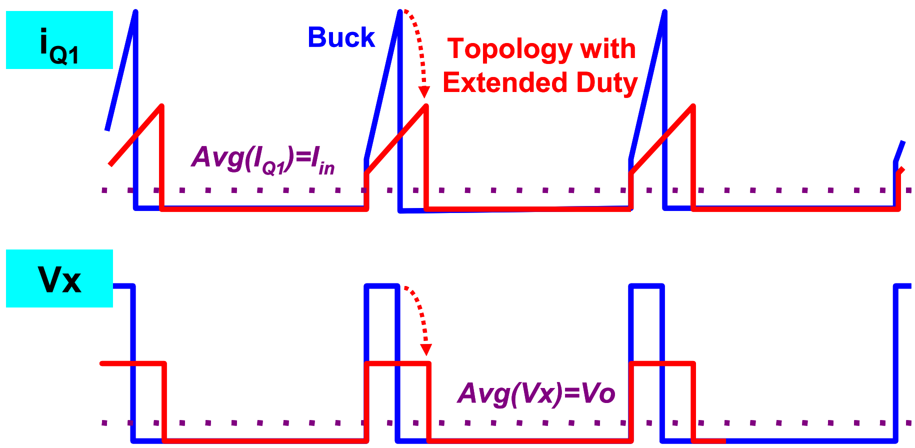


Fig. 4.6. The impacts of the extended duty cycle.

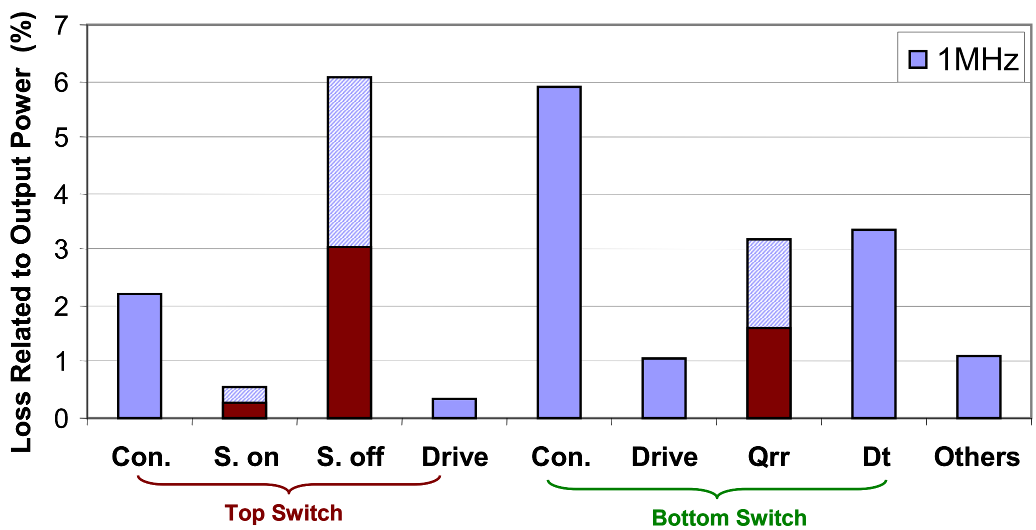


Fig. 4.7. Loss reduction expected to result from doubling the duty cycle.

However, these topologies are much more complicated than the buck converter with an additional transformer. The flyback converter is relatively simple, with its one magnetic component that functions as both the transformer and the output inductor. But the pulsating output current requires more output filter capacitors. Also, there is no simple lossless way to limit the voltage spike across the primary-side switch because of the existence of leakage inductance in the flyback transformer.

As a result, some other topologies have been proposed for high-step-down DC-DC conversion [C3-C25]. Of these, the tapped-inductor (TI) buck converter is very attractive for its simple structure. It involves only a slight modification to the buck converter. It can extend the duty cycle and maintains an output current ripple that is smaller than that of the flyback converter [C14]. However, the leakage inductance between the coupled windings causes severe voltage spikes across the MOSFETs and impairs efficiency. Section 4.2 modifies the structure of the TI buck converter and introduces a lossless clamp circuit to solve the existing problems.

4.2. The Multiphase Tapped-Inductor Buck Converter with Passive-Clamped Circuits

Fig. 4.8 shows a TI buck converter in which a tapped inductor replaces the output filter inductor of the buck converter shown in Fig. 4.1. This allows different inductances between the charging and discharging periods. The inductances of winding n_1 and n_2 are effective during the charging period, while the inductance of only winding n_1 is effective during the discharging period. In other words, the TI buck converter adds a second coupled winding n_2 to the conventional buck converter. The turns ratio is defined as:

$$n=(n_1+n_2)/n_1. \tag{4.6}$$

This modification introduces an extra degree of design freedom, in that the TI turns ratio “n” may be selected in such a way that it offers the most benefit to the DC-DC conversion.

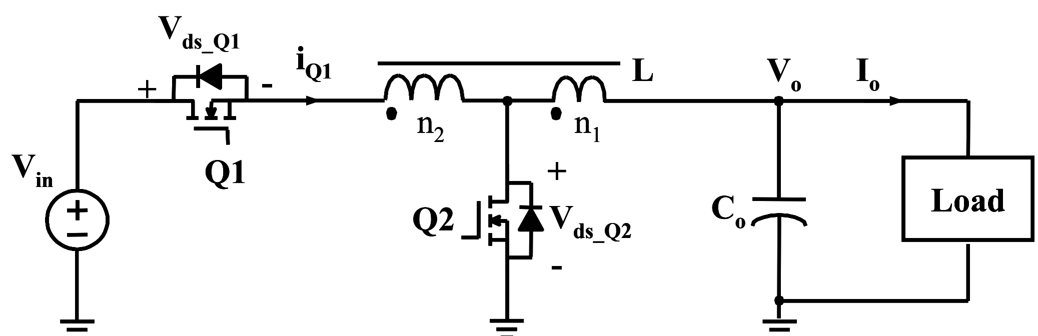


Fig. 4.8. A TI-buck converter.

4.2.1. The Advantages of the TI Buck Converter

From the voltage-second balance on the inductor, the switching duty cycle of the TI buck converter can be derived as follows:

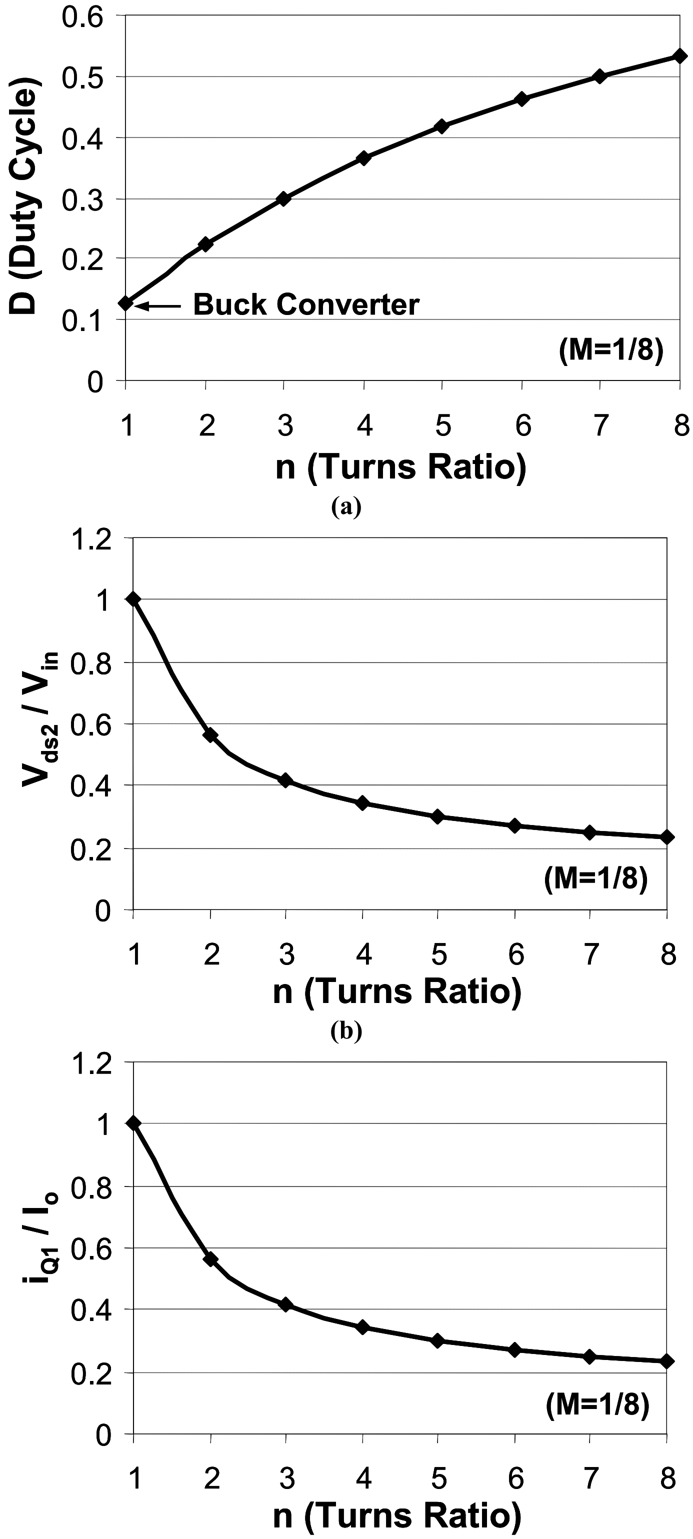
$$D = \frac{n \cdot V_o}{V_{in} + (n-1) \cdot V_o} = \frac{n \cdot M}{1 + (n-1) \cdot M} . \tag{4.7}$$

If n=1, (4.7) yields the same result as (4.4), which is the duty cycle of the conventional buck converter. When n>1, the duty cycle increases with the increase of n. Fig. 4.9 (a) shows the trend clearly with an eight-time step-down DC-DC conversion. Fig. 4.9 (b) and (c) show the reducing trends of the bottom-switch voltage stress and the top-switch switching current versus the increase in the turns ratio. The data are normalized to the input voltage or output current. Here, the current ripple is ignored in order to simplify the analysis.

$$V_{ds\_Q2} = \frac{V_{in} - V_o}{n} + V_o = \left(\frac{1-M}{n} + M \right) \cdot V_{in} \tag{4.8}$$

$$i_{Q1} = \frac{M \cdot I_o}{D} = \left(\frac{1-M}{n} + M \right) \cdot I_o \tag{4.9}$$

A smaller switching current means less switching loss in the top switch. Lower voltage stress means less body diode reverse-recovery loss in the bottom switch. Also, a low-voltage MOSFET can be used for the bottom switch to further reduce the conduction loss. It is very clear that the problem related to small duty cycle that exists for conventional buck converters is solved in the TI buck converter. High efficiency is expected.



(a)

(b)

(c)

Fig. 4.9. Improvement of the TI buck converter: (a) extended duty cycle, (b) reduced bottom-switch voltage stress, and (c) reduced top-switch switching current.

4.2.2. The Existing Problems in the TI Buck Converter

Although the TI buck converter offers many benefits, there are two problems limiting its wide applications in practice. First, there is no simple way to drive the top switch Q1, which has a floating source connection. When Q1 is off and Q2 freewheels, the source voltage of Q1 goes to negative, such that:

$$V_{s\_Q1} = -(n-1) \cdot V_o \,. \tag{4.10}$$

This is different from the case for the buck converter, in which the Q1 source is connected to the ground through Q2 when Q2 freewheels. As a result, the simple bootstrap gate driver can not be applied in the TI buck converter. A transformer-isolated or an opt-isolated gate driver is required, either of which will degrade the simplicity of the original power converter. Besides, either the parasitics in the gate drive transformer or the delay in the optocoupler limits the drive speeds, which causes more switching loss, especially in high-frequency applications.

The most serious problem for the TI buck converter is the leakage energy. It is impossible for the TI to achieve a perfect coupling effect, so leakage inductance exists in the circuit. Ideally, the voltage stress of the top switch is:

$$V_{ds\_Q1} = V_{in} + (n-1) \cdot V_o \,. \tag{4.11}$$

But in reality, when the top switch is turned off, the current in the leakage inductance of winding n_2 cannot be reflected to winding n_1, so it continuously goes through the drain-to-source capacitor of the top switch. All of the energy stored in the leakage inductance will be transferred to this small capacitance, causing a huge voltage spike across the top switch. This voltage spike can be much higher than the value in (4.11). This not only increases the switching loss, but also can destroy the top switch.

Some methods have been proposed to solve these problems, especially the leakage energy problem [C3, C12-C14]. Although all the proposed methods feature the lossless characteristic, which is better than the conventional resistor-capacitor-diode (RCD) clamp circuit, they greatly increase the circuit complexity. The active-clamped concept [C3] requires a change in the power stage, which has more coupled windings. The gate drive remains problematic. The passive-clamped circuit [C12, C13] requires a third coupled winding. The snubber circuit [C14] employs an LC resonant circuit with large circulating current; also, its voltage stress can go much higher than the value in (4.11). The next section proposes a very simple method to solve the problem.

4.2.3. The Modified TI Buck Converter with a Lossless Clamp Circuit

The gate drive problem is easy to solve by simply rearranging the connections of the tapped inductor and power devices. Fig. 4.10 shows the modified converter obtained by exchanging the positions of the winding n_2 and the top switch Q1. The TI looks more like two coupled inductors. With this change, the source of the top switch is connected with the drain of the bottom switch, which is the same structure as in the buck converter. As a result, the simple bootstrap gate driver can be used.

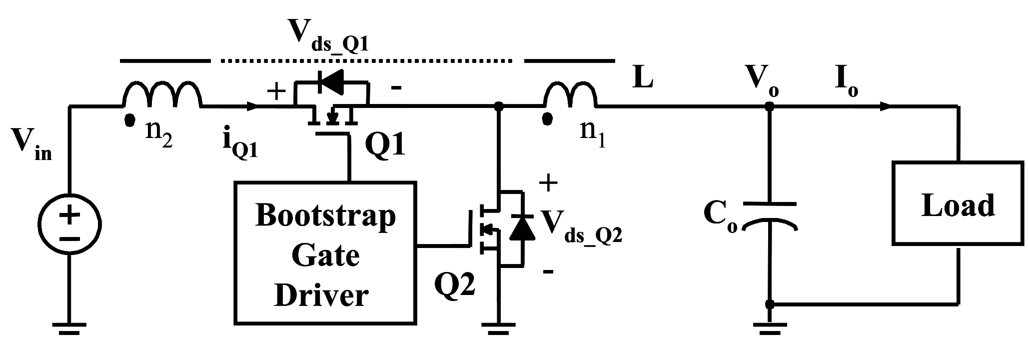


Fig. 4.10. Modified structure of the TI buck converter.

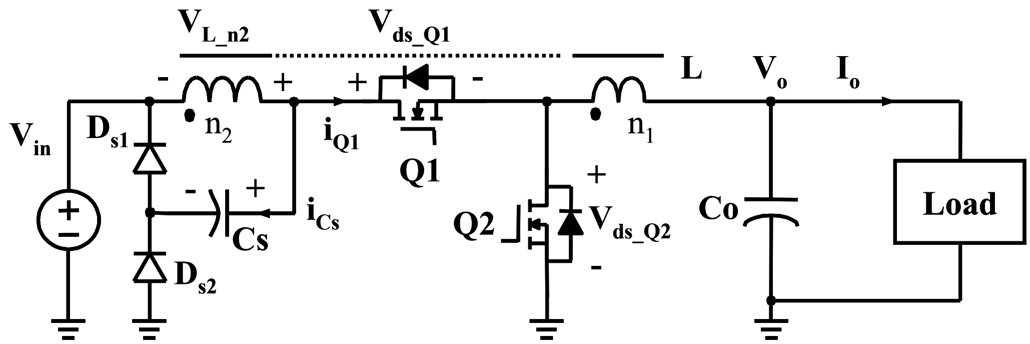


Fig. 4.11. A lossless clamp circuit for the TI buck converter.

Based on this modified circuit structure, a simple lossless clamp circuit with two diodes and a capacitor can be applied. Fig. 4.11 shows the circuit. The operation principle is as follows.

$$V_{Cs0} = \frac{V_{in} - V_o}{n} + V_o \tag{4.12}$$

During top switch Q1's turn-on period, the steady-state voltage across the clamp capacitor Cs is: $V_{Cs0}=(Vin-Vo)/n+Vo$.

Here, the diode forward voltage drop is ignored. When top switch Q1 is turned off, the current in the leakage inductance goes through Cs and D_{s1} so that the leakage inductance energy is stored in clamp capacitor Cs. If Cs is large enough, the increased voltage across Cs is relatively small, and the value is about:

$$\Delta V_{Cs} = \frac{L_{leak} \cdot i_{off}^{\ 2}}{2 \cdot Cs \cdot V_{Cs0}}. \tag{4.13}$$

As a result, the turn-off voltage stress across top switch Q1 is effectively clamped as:

$$V_{ds\_Q1\_Max} = V_{in} + V_{Cs0} + \Delta V_{Cs}. \tag{4.14}$$

When top switch Q1 is turned on, the extra energy stored in the clamp capacitor will be discharged to the output through D_{s2} and winding n_1. The voltage across Cs goes back to V_{Cs0}, which is the steady-state value. Therefore, all the leakage energy is totally recovered to the output.

Fig. 4.12 shows the key operation waveforms by simulation for a 300KHz, 12V-to-1.5V/12.5A DC-DC conversion. The tapped inductor is designed with n=2, 300 nH for each winding, and a 0.95 coupling coefficient. The currents through D_{s1} and D_{s2} are very narrow pulses. A 2μF clamp capacitor limits the ΔV_{Cs} to less than 0.2 V. The turn-off voltage of the top switch (V_{ds_Q1}) is perfectly clamped to 22 V. Compared with (4.14), there is a small error due to the diode forward conduction drop in the simulation circuit. Overall, this clamp circuit features simple structure, small size and low cost.

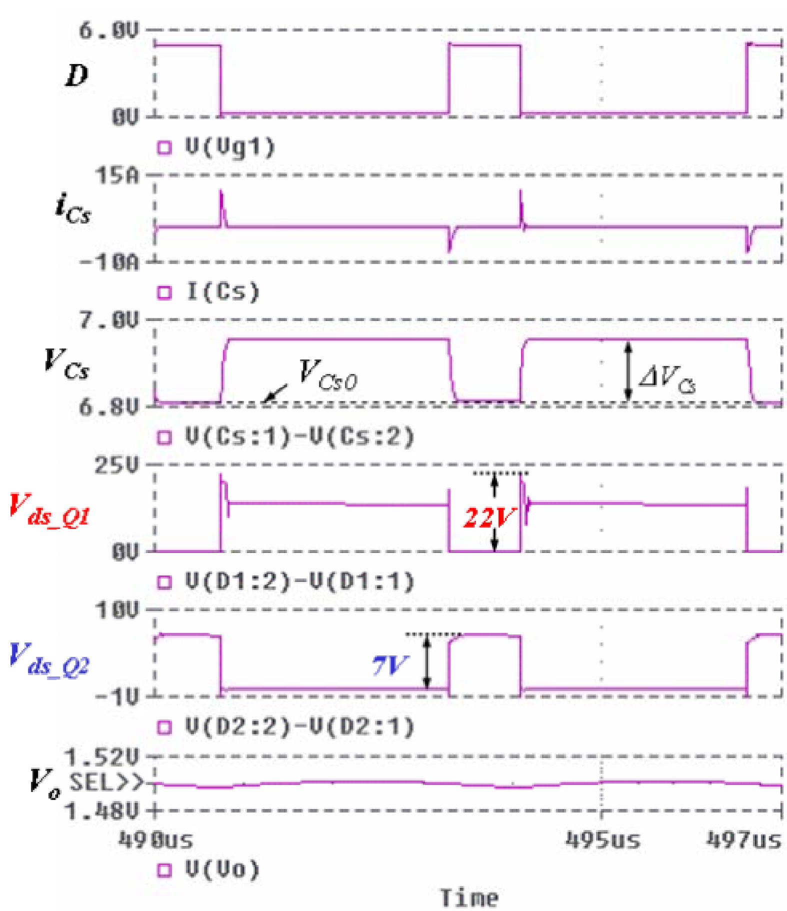
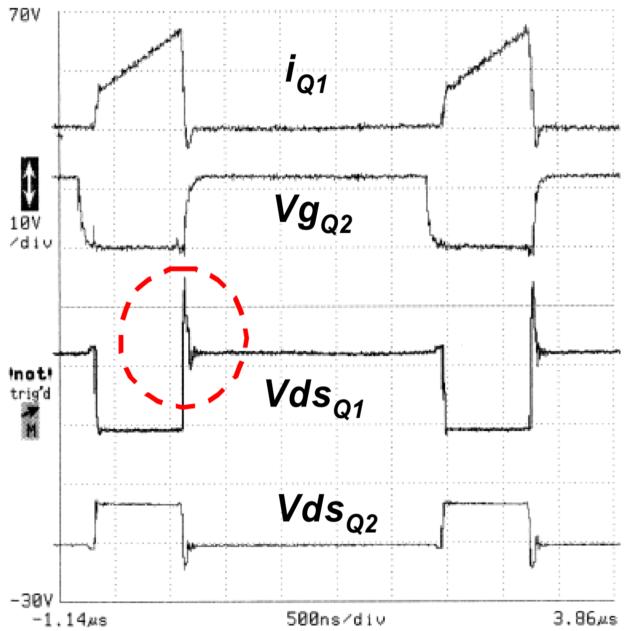
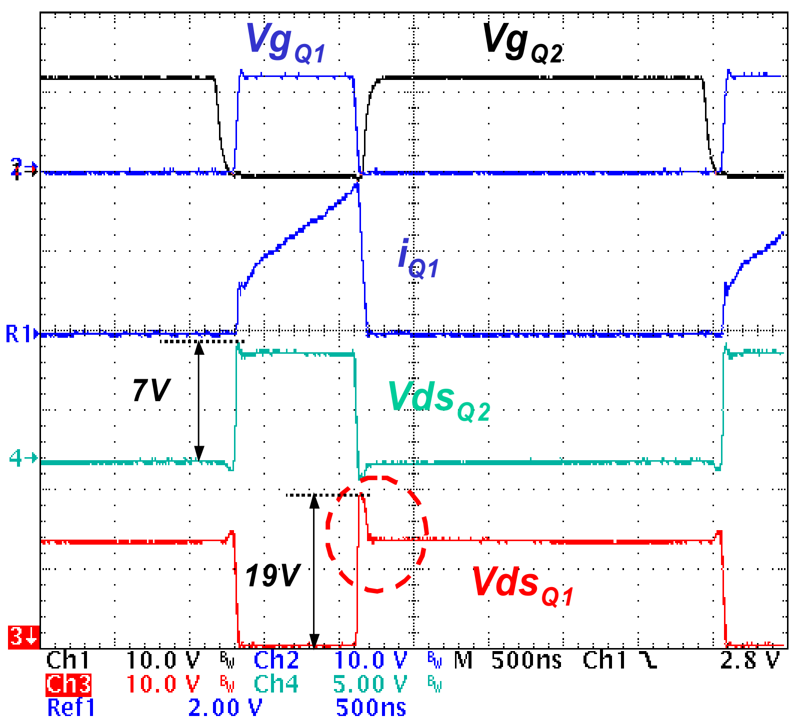


Fig. 4.12. Simulation results for the lossless clamp circuit.



(a)



(b)

Fig. 4.13. The TI buck converter for 12V-to-1.5V DC-DC conversion: (a) without the passive-clamped circuit and (b) with the passive-clamped circuit.

Fig. 4.13 shows the experimental result comparison for the TI buck converter with and without the clamp circuit. Without the clamp circuit, there is a huge voltage spike (26 V) across the top switch when it is turned off, even when the load current is 10 A. However, with the clamp circuit, the voltage stress across the top switch is perfectly clamped below 20 V at the full load current (12.5A a phase). The leakage energy can be stored in the clamp capacitor and recovered to the output.

However, there is a limitation for the simple application of this lossless clamp circuit with some turns-ratio designs. For an ideal TI buck converter without a leakage inductance or a clamp circuit, when top switch Q1 is turned off, the voltage across winding n_2 is:

$$V_{L\_n2}=(n-1)\cdot V_o. \tag{4.15}$$

To maintain correct operation, this voltage must be smaller than V_{Cs0} in (4.12). Otherwise, instead of the intended small pulse current, a large current will continue charging and discharging Cs. From (4.12) and (4.15), the limitation for this clamp circuit application is:

$$n \le \sqrt{\frac{V_{in}}{V_o}}+1=\sqrt{\frac{1}{M}}+1. \tag{4.16}$$

4.2.4. Winding Design Considerations

The most important aspect is the TI design, which is related to the efficiency, transient response and VRM size. A planar core structure is selected for its low-profile, high-power-density design. The inductor winding can be realized with the PCB copper trace in order to both simplify assembly and reduce cost. Also, the solder point resistance can be eliminated, which is very helpful for large winding currents.

Fig. 4.14 shows that the best turns ratio for the TI is about 2.5 for a symmetric transient response. Since large currents go through winding n1 during the freewheeling period, n1 should be a one-turn winding to reduce the conduction loss. As a result, one-turn or two-turn windings can be used for n2 in order to achieve an almost symmetric transient response. A one-turn design is selected for n2, because this is the simplest structure for a TI. Fig. 4.15 shows the simple implementation structure with PCB winding design.

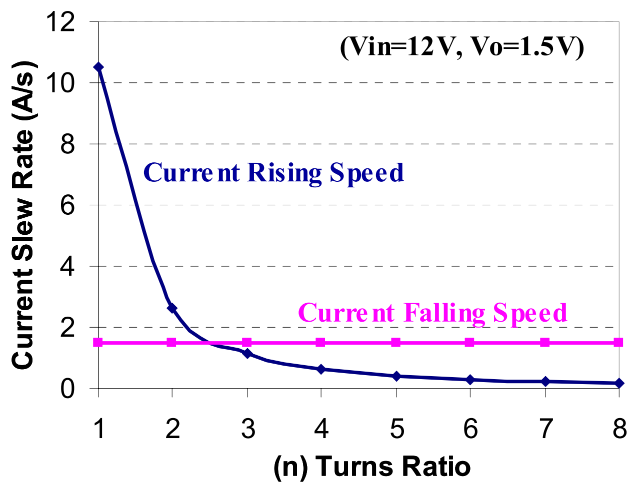


Fig. 4.14. Relationship between inductor current slew rate and turns ratio.

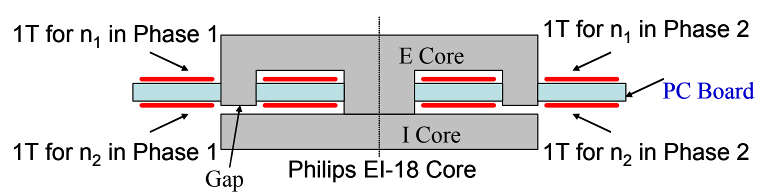


Fig. 4.15. Simple winding implementation for the tapped inductor with turns ratio of 2.

Another reason for the small turns ratio is the moving zero in the right half plane (RHP) [C5-C7]. This RHP zero reduces the system feedback loop phase margin and can impact the transient response. Fig. 4.16 shows the relationship between the RHP zero and the turns ratio at the full load condition. A large turns ratio moves the RHP zero to the low-frequency range. Also, a larger L_{w1} means a lower-frequency RHP zero. Fig. 4.17 shows the impact on the phase margin. Since a higher-frequency RHP zero has less influence on the system feedback, the turns ratio is designed to be 2. The inductance of winding w1 is designed to be 300 nH as a trade-off between the transient response and efficiency.

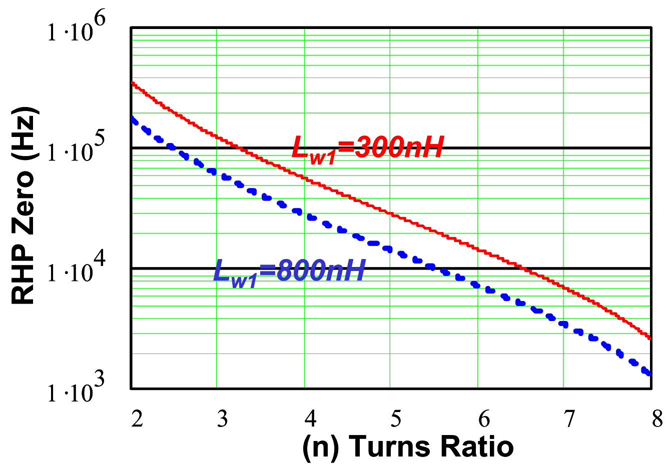


Fig. 4.16. The influence of turns ratio on RHP zero.

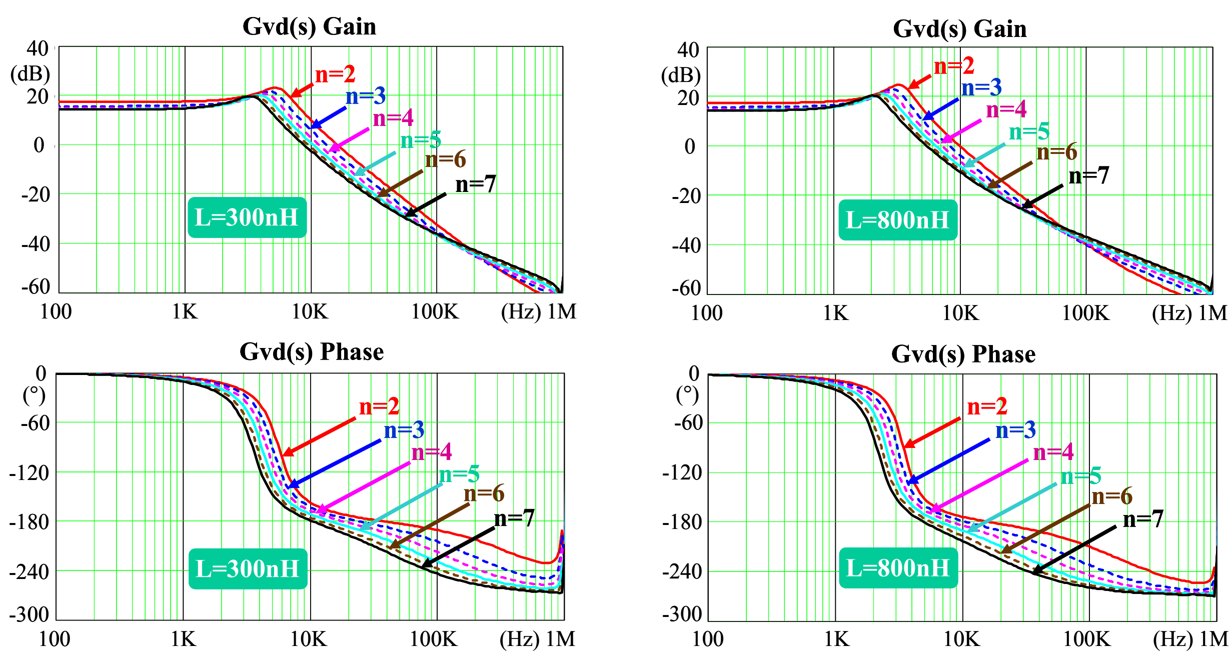


Fig. 4.17. The influence of the turns ratio and inductance on the phase margins.

4.2.5. Experimental Results of the Passive-Clamped TI Buck Converter

A 1MHz, 12V-input and 1.5V/25A-output VRM incorporating the TI buck converter is designed. A two-phase interleaving structure is used in order to distribute the large output current and to achieve current-ripple cancellation. To make a comparison, a two-phase interleaved buck converter is also developed with the same design, except that the inductors differ. Hitachi's 30V trench MOSFETs with SO-8 lead-free packaging are used for their small parasitics and excellent thermal performance. For top switch Q1, HAT2116H is used because of its fast switching speed. For bottom switch Q2, HAT2099H is used, as a trade-off between low conduction resistance R_{ds_on} and small diode reverse-recovery charge Q_{rr}. The gate driver is National Semiconductor's LM2726, which has fast driving capability and can drive both the top and bottom switches. It uses the self-adaptive control scheme to limit the dead-times to about 25 ns, so that there is no shoot-through problem and the diode conduction loss is small. Four polymer aluminum capacitors (270μF/2V) from Cornell Dubilier are used as the output bulk capacitors because of their low ESR and very small size.

The TDK EIR-18 planar cores are used for the inductors in order to achieve low profile. Nine-layer, two-ounce PCB is used for the winding design. For the conventional buck converter, all nine layers are parallel to form the single-turn inductor winding. The air gap is adjusted to achieve 200nH inductance. For the TI buck converter, six layers in parallel are used for n_1, and three layers in parallel comprise n_2. An interleaving, symmetrical winding structure is used to minimize the leakage inductance to about 5 nH. The inductance of each winding is designed to be 200 nH.

For the passive-clamped circuit, two 1A/25V Schottky diodes and one 2.2μF ceramic capacitor with 0805 packaging are used.

Fig. 4.18 shows the operation waveform comparison between the buck and TI buck converters at 1 MHz. The duty cycle of the proposed topology is almost doubled, and the voltage stress of its bottom switch is reduced by about half. The ringing voltage of V_{ds_Q2} (when Q1 is turned on) is reduced from 6 V to 2 V for the peak-to-peak value. With the clamp circuit, the top switch turn-off spike in the TI buck converter is almost the same as in the buck converter. All of these indicators predict a significant loss reduction in terms of switching and body-diode reverse recovery.

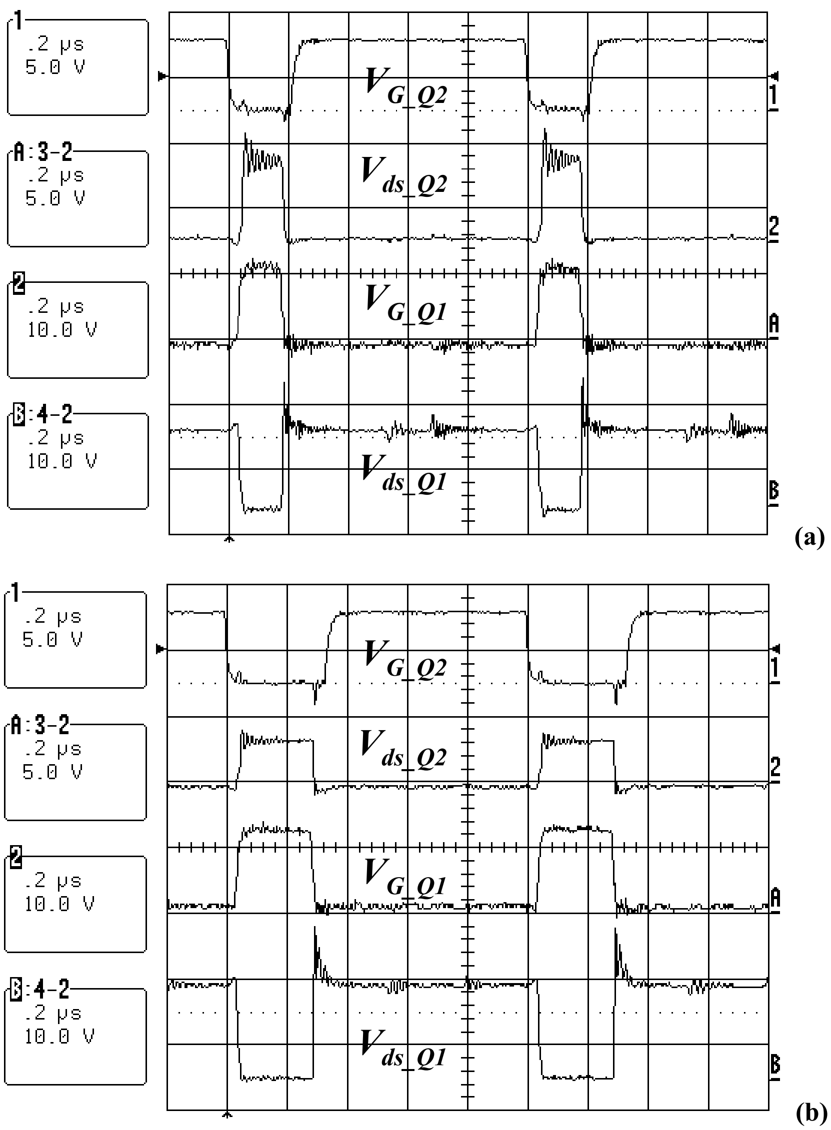


Fig. 4.18. The gate drive and voltage stress waveforms: (a) buck converter and (b) TI buck converter.

Fig. 4.19 shows the efficiency improvement and loss reduction. The TI buck converter achieves about 85% efficiency at the full load, which is a 4% improvement over the buck converter. In Fig. 4.18 (b), the voltage stress of the bottom switch is only about 7V. As a result, lower-voltage MOSFETs can be used to further reduce the R_{ds_on}. For example, by replacing the HAT2099H with a 12V trench MOSFET Si4838DY (from Siliconix), the Rds_{on} can be reduced from 5 mΩ to 3 mΩ, and the full-load efficiency will be improved by another 2%.

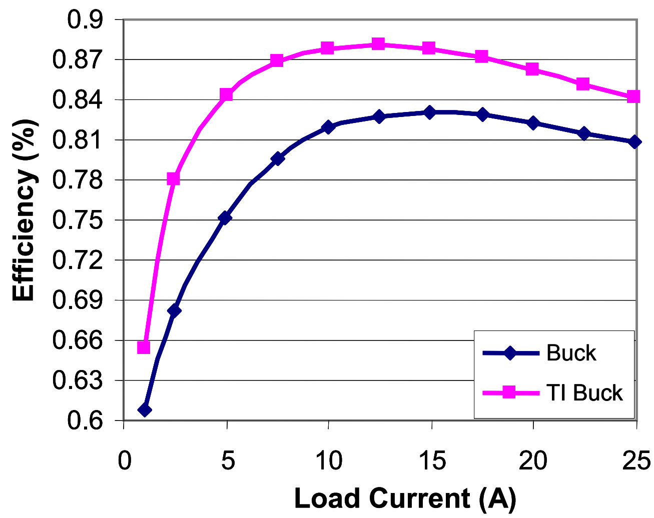


Fig. 4.19. The efficiency comparison between the buck and TI buck converter.

4.3. The Multiphase Winding-Coupled Buck Converter with Passive-Clamped Circuits

Section 4.2 shows the benefits of the passive-clamped TI buck converter. However, similar to the active-clamped buck converter discussed in other work [C17], this circuit is disadvantageous in terms of discontinuous output currents and RHP zeros in its small-signal model [C5-C7]. The current-jumping and -dropping in every switching cycle will not only increase the output voltage steady-state ripple, but will also decrease the reliability of the output capacitors. The RHP zero may negatively impact the system design as far as transient response and stability.

This section proposes another novel topology, which retains all the benefits of the previous topologies based on coupled windings but has continuous output current and no RHP zero. Its equivalent circuit is still a buck converter, but with a lower input voltage.

4.3.1. The Topology Structure and Operation Principle

Fig. 4.20 shows the proposed winding-coupled buck converter. In the right block, it is a conventional buck converter with two-phase interleaving. The two additional coupled windings for each phase are shown in the left block. The first winding is coupled to the inductor in its phase (L_{1b} vs. L_{1a} and L_{2b} vs. L_{2a}), and the second winding is coupled to the inductor in another phase (L_{1c} vs. L_{1a} and L_{2c} vs. L_{2a}). Both coupled windings have turns ratios of n. The method used for coupling is represented in Fig. 4.20 by the "*" and "^" marks. With this modification, the conventional buck converter evolves into the proposed new version.

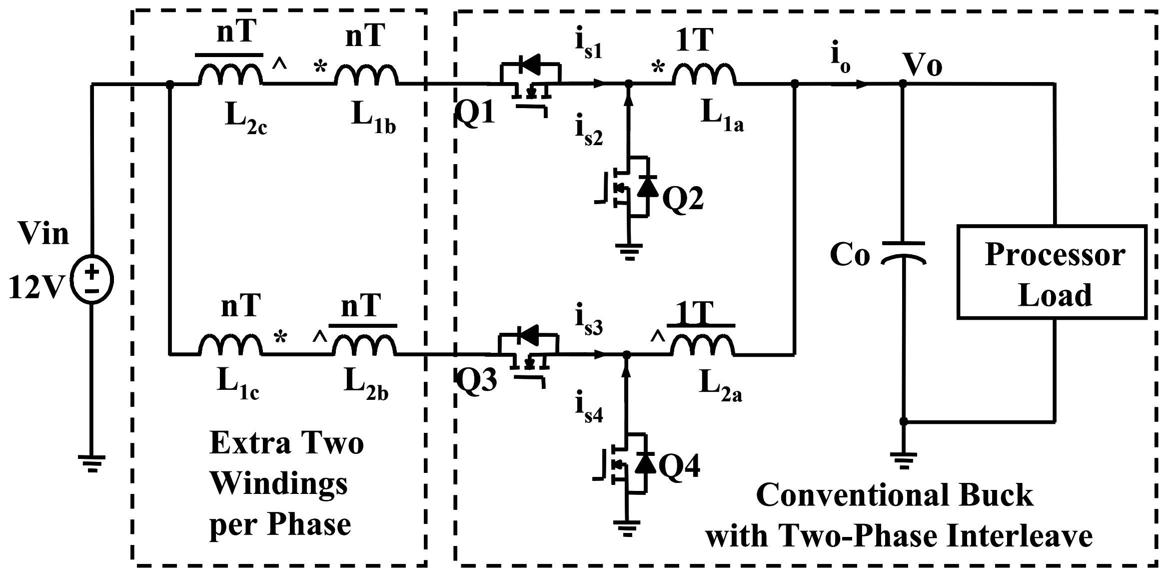


Fig. 4.20. The proposed winding-coupled buck converter.

The control principle for the proposed converter is the same as that for a two-phase interleaved buck converter. In the same phase, the top and bottom switches are controlled complementarily. As a result, the same bootstrap gate drivers used in the buck converter can continue to be used. For the different phases, they are controlled with 180-degree phase shifts. Conventional two-phase PWM controllers can be also applied for the proposed topology.

There are two major operation stages. In Stage I, one phase operates in the inductor-charging period and another phase operates in the freewheeling period. In Stage II, both phases operate in the freewheeling period. Fig. 4.21 shows the operation stages, and Fig. 4.22 shows the key operation waveforms obtained through PSpice simulation.

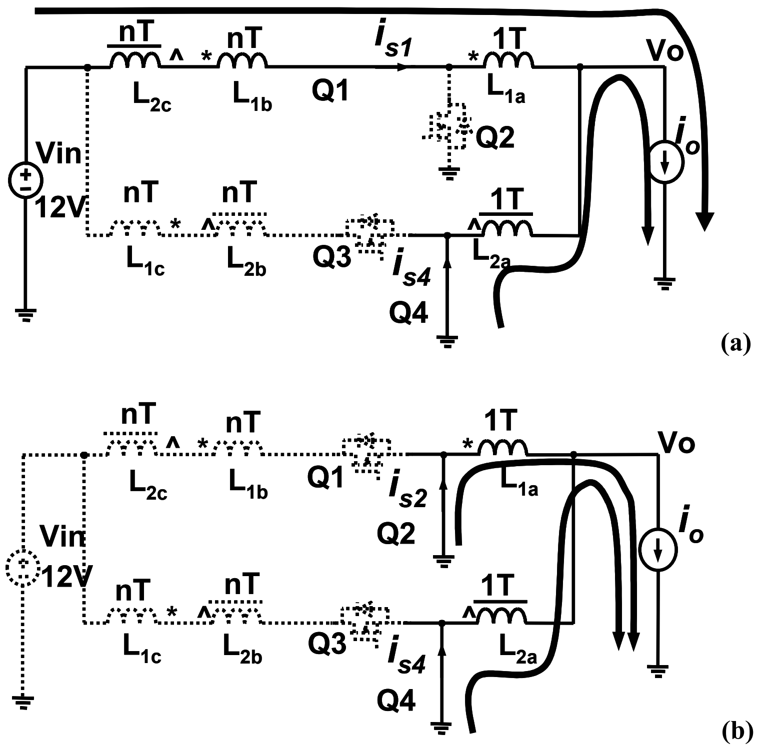


Fig. 4.21. The operation principle: (a) Stage I and (b) Stage II.

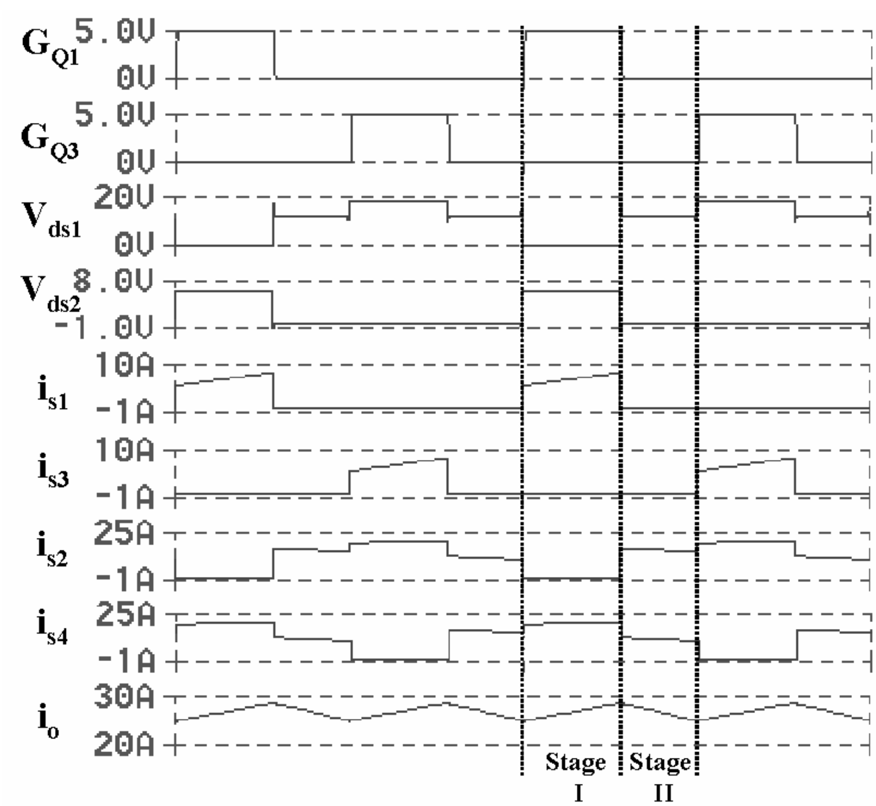


Fig. 4.22. The key operation waveforms.

In Stage I, Q1 and Q4 are on and Q2 and Q3 are off. L_2 (with coupled windings L_{2a} and L_{2c}) operates as a transformer, and L_1 (with coupled windings L_{1a} and L_{1b}) operates as an inductor. The inductor-charging current i_{s1} goes through switch Q1. Since L_2 operates as a transformer, n· i_{s1} current will be transferred to phase 2 in L_{2a}. The combination of this transferred current and the original inductor freewheeling current in phase 2 form i_{s4}. Fig. 4.22 shows these switch-current waveforms. The voltage-second across winding L_{1a} in this period is:

$$VS_1 = \left(\frac{V_{in}}{n+1} - V_o \right) \cdot \frac{D}{f_s}. \tag{4.17}$$

The voltage stress of the bottom switch Q4 is:

$$V_{ds4} = \frac{V_{in}}{n+1}, \tag{4.18}$$

which is significantly reduced. According to (4.18), the bottom-switch body diode reverse-recovery loss can be greatly reduced with the increased turns ratio. Also, the synchronous rectifiers Q3 and Q4 can use lower-voltage MOSFETs, which have less conduction loss.

The voltage stress of the top switch Q3 is:

$$V_{ds3} = V_{in} \cdot \left(2 - \frac{1}{n+1} \right), \tag{4.19}$$

which is always less than twice the level of the input voltage.

In Stage II, both L_1 (with winding L_{1a}) and L_2 (with winding L_{2a}) operate as inductors to freewheel the current to the output. The energy stored in winding L_{1b} in Stage I is reflected to winding L_{1a} as in a flyback transformer. The voltage-second across the winding L_{1a} in this period is:

$$VS_2 = V_o \cdot \frac{(1-D)}{f_s}. \tag{4.20}$$

During this period, the voltage stresses of top switches Q1 and Q3 are the same:

$$V_{ds1} = V_{ds3} = V_{in} . \tag{4.21}$$

From (4.17) and (4.20), based on the voltage-second balance, it is easy to derive that:

$$D = (n+1) \cdot \frac{V_o}{V_{in}} = (n+1) \cdot M \ . \tag{4.22}$$

Compared with (4.1), the proposed topology can extend the duty cycle by (n+1) with n turns of coupled windings.

Assume that the filter inductance value is large enough that the current ripple can be ignored. From the power balance between the input and output, it is easy to derive that the input pulse current value in each phase is:

$$i_{s1\_peak} = i_{s3\_peak} = \frac{1}{2} \cdot \frac{i_o}{n+1} . \tag{4.23}$$

Compared with the conventional buck converter, the top-switch switching current can be reduced by (1+n) times. At the same time, the relative turn-on and turn-off time can also be reduced because of the smaller switching currents [C2]. But the turns ratio has little impact on the top-switch voltage stress, which is always less than twice the level of the input voltage. The switching loss can be significantly reduced according to (4.2), (4.19) and (4.23).

The preceding analysis of the circuit operation shows that this proposed circuit operates in a manner very similar to that of a push-pull current doubler with a transformer turns ratio of n+1:1. Thus, it is easy to understand why the proposed circuit can reduce the switching loss and body diode reverse-recovery loss. Since its final equivalent circuit is still a buck converter, this topology retains all the same attributes. The output current is continuous (i_o in Fig. 4.22), and there is no RHP zero.

Although its performance is similar to that of the push-pull converter with an isolated transformer, this proposed circuit structure is much simpler. Only two magnetic cores are needed, and n-turn windings can achieve a turns ratio of n+1:1. This is a significant benefit for the 12V-input VRM application, since the additional windings can use only a single turn to double the duty cycle while halving both the switching current and the bottom-switch voltage stress. The isolated push-pull converter must have additional two-turn windings to achieve the same function. Another great benefit of the proposed circuit is its technical compatibility: All of the drivers and controllers for the conventional multiphase buck converter can be used directly.

4.3.2. The Integrated Magnetic Structure

Although the proposed topology has many advantages over the conventional buck converter, the winding structure is relatively complex. As a result, an integrated magnetic structure is proposed to simplify the implementation. The same magnetic cores as are in the conventional buck converter can be used. Fig. 4.23 shows the step-by-step integration of these three coupled windings in each core. Here, the turns ratio n=1 is selected so that single-turn windings can be used throughout and the proposed topology can still keep all the benefits.

Another consideration for the turns-ratio selection is the top-switch voltage stress. Equation (4.19) only shows the steady-state voltage stress value, which is lower than that in the real case because of the turn-off spike. As a result, n=1 is selected, and the 30V MOSFETs in the conventional buck converter can still be used.

The basic idea for the integration is that a winding goes simultaneously though the center legs of two E cores so that the two additional windings are developed concurrently, one coupled to its phase and the other coupled to another phase. In Fig. 4.23 (a), windings L_{1a} and L_{2a} go around their own E-core center leg, which is the same as the inductor structure in the conventional buck converter. But in Fig. 4.23 (b), windings L_{2b} and L_{1c} are formed simultaneously, and no solder points are needed for interconnection. Fig. 4.23 (c) shows the same process to form windings L_{1b} and L_{2c}. Interleaving structures are used for all of these coupled windings in order to reduce the leakage inductance. The two E cores can be one magnetic component, with the outer legs connected to each other. The footprint of the magnetic components is the same as that of the conventional buck converter. Although at least three layers are needed to form all of these windings, there is no cost increase if multi-layer PCB is used for the design.

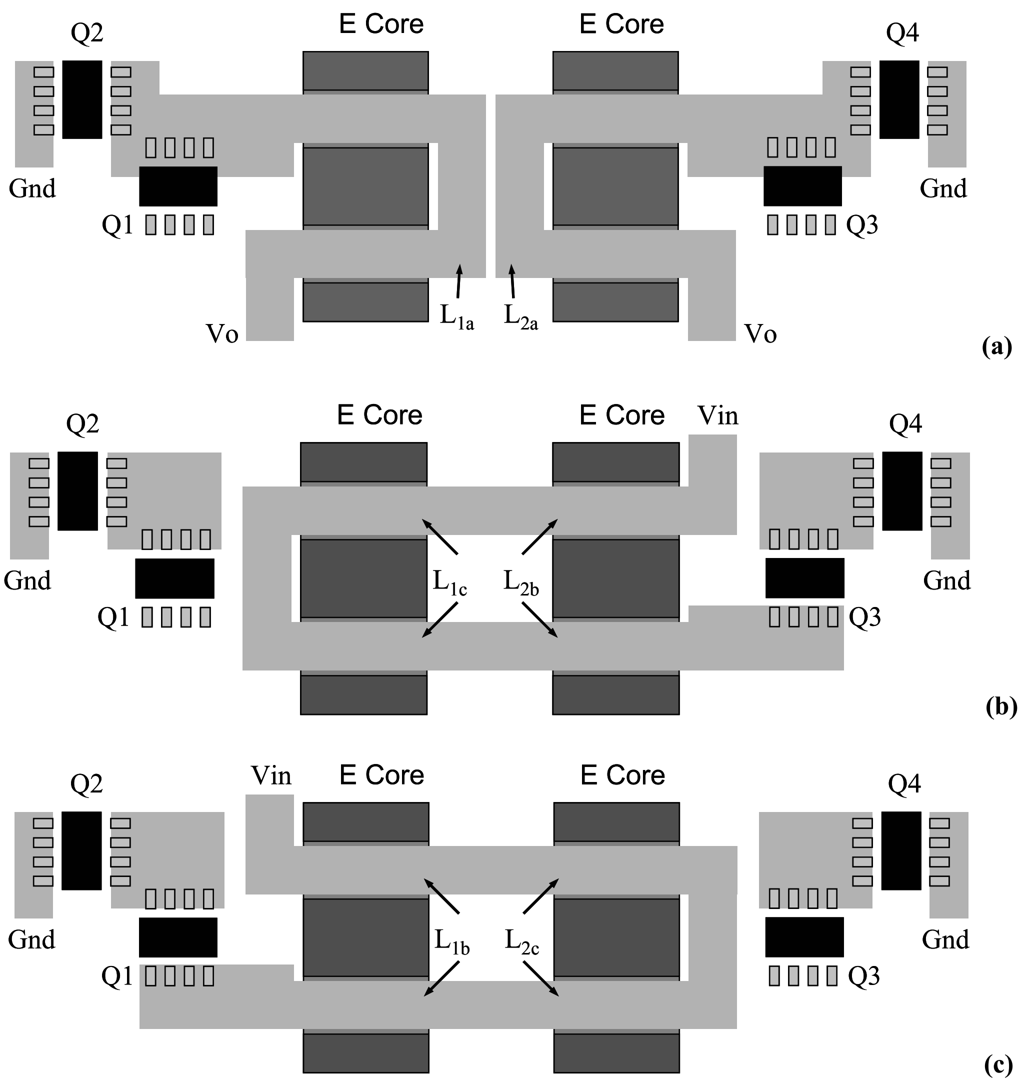


Fig. 4.23. The step-by-step integration of all the windings: (a) Step 1, (b) Step 2 and (c) Step 3.

4.3.3. The Lossless Clamp Circuit

There is one potential problem for the proposed winding-coupled buck converter. Leakage inductance always exists no matter how well the windings are coupled. When the top switch is turned off, this leakage inductance can cause a huge voltage spike across the drain source of the top MOSFET, which can destroy the device. However, with the single-turn winding design, it is easy to implement a lossless clamp circuit. Fig. 4.24 shows the clamp circuit in one phase, and Fig. 4.25 shows the operation waveforms obtained by simulation.

In Fig. 4.24, C_{s1}, D_{s1} and D_{s2} form the clamp circuit. The operation principle is very simple. When the top switch is turned off, C_{s1} clamps the voltage spike and stores the leakage energy. When the top switch is turned on, the extra stored energy is discharged to the output through D_{s2}. The discharging current will stop when the voltage of C_{s1} is lower than the clamped voltage value, such that:

$$V_{Cs1\_clamp} = \frac{1}{2} \cdot V_{in} + V_F \,, \tag{4.24}$$

where V_F is the diode forward conduction voltage drop.

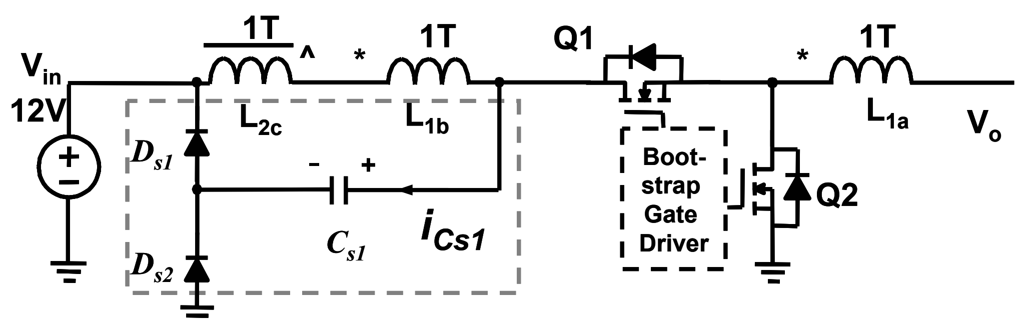


Fig. 4.24. The lossless clamp circuit for the winding-coupled buck converter.

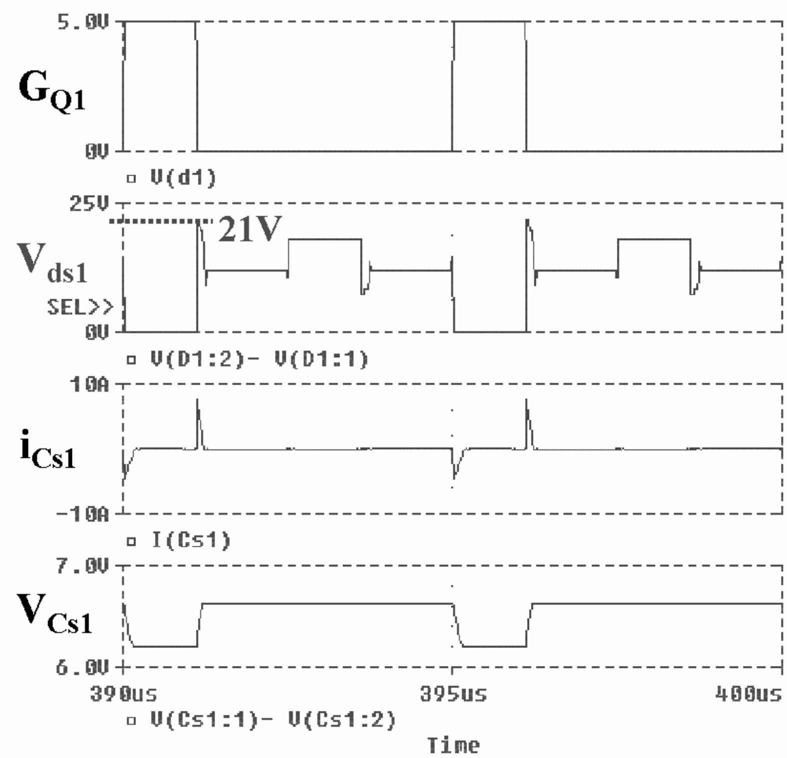


Fig. 4.25. Simulation results for the lossless clamp circuit.

As a result, narrow spike currents charge and discharge the clamp capacitor C_{s1}. The leakage inductor energy is recovered. The voltage stress of the top switch can be derived as:

$$V_{ds1\_max} \approx \frac{3}{2} \cdot V_{in} + 2 \cdot V_F + \frac{L_{leak} \cdot i_{s1}}{2 \cdot C_{s1} \cdot V_{Cs1\_clamp}}, \tag{4.25}$$

where L_{leak} is the leakage inductance and i_{s1} is the top-switch turn-off current. When the clamp capacitance is large enough, the first two items in (4.25) dominate the turn-off voltage spike. In the simulation, the coupled inductors have 500nH inductance in one turn and a coupling coefficient of 0.95. The VRM output is 1.5V/25A. A 2μF of clamping capacitance is used. Fig. 4.25 shows the perfect voltage-clamp effect for the top-switch drain-to-source voltage stress. As a result, 30V MOSFETs can still be used in the proposed winding-coupled buck converter for fast switching speed and low conduction loss.

Since the currents through D_{s1} and D_{s2} are very narrow pulses, these diodes can be small because of their low power losses. Surface-mounted multi-layer ceramic capacitors can achieve several μF and have very small footprints. As a result, this clamp circuit features simple structure, small size and low cost.

4.3.4. Experimental Results

Two 12V-input VRM prototypes are developed with the proposed topology for 1.5V/25A output at two separate switching frequencies -- 1 MHz and 2 MHz. To make a comparison, two-phase interleaved buck converters are also developed with the same design, except that the inductors are different. For the active components, Hitachi's 30V trench MOSFETs with SO-8 lead-free packaging are used for their small parasitics and excellent thermal performance. HAT2116H is used for the top switches Q1 and Q3 because of its fast switching speed. HAT2099H is used for the bottom switches Q2 and Q4 as a trade-off between low conduction resistance R_{ds_on} and small diode reverse-recovery charge Q_{rr}. The gate driver is National Semiconductor's LM2726, which has fast driving capability and can drive both the top and bottom switches. It uses the self-adaptive control scheme to limit the dead-times to about 25 ns, so that there is no shoot-through problem and the diode conduction loss is small.

For the passive components in the 1MHz VRM, four polymer aluminum capacitors (270μF/2V) from Cornell Dubilier are used because of their low ESR and very small size. TDK planar EIR-18 cores are used for a 300nH coupled-inductor design. For the 2MHz VRM, four ceramic capacitors from TDK (100μF/6.3V) and TDK planar EIR-14 cores are selected in order to further reduce the size. The inductance is 150 nH. Nine-layer, two-ounce PCB is used for the winding design. For the conventional buck converter, all nine layers are parallel to form the single-turn inductor winding. For the proposed topology, the integrated magnetic structure in

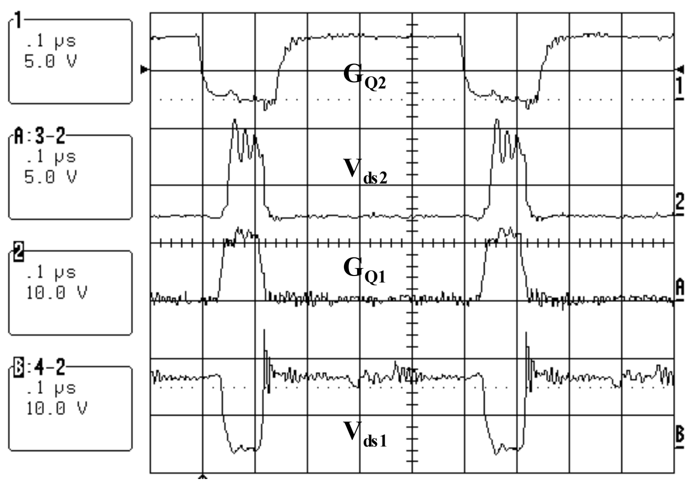
Fig. 4.23 is used. Five layers in parallel are used for L_{1a}, two layers in parallel for L_{1b}, and another two layers for L_{1c}.

For the input filter design, the proposed winding-coupled buck converter can utilize fewer input capacitors, as compared with the buck converter. The extended duty cycle significantly reduces the amplitude of the pulse input current so that smaller RMS current goes through the input capacitors. Consequently, less input capacitance is required to achieve the same filter effect. In the practical design, four ceramic capacitors from TDK (10μF/16V) are used for the 1MHz design, and four ceramic capacitors from TDK (4.7μF/16V) are used for the 2MHz design.

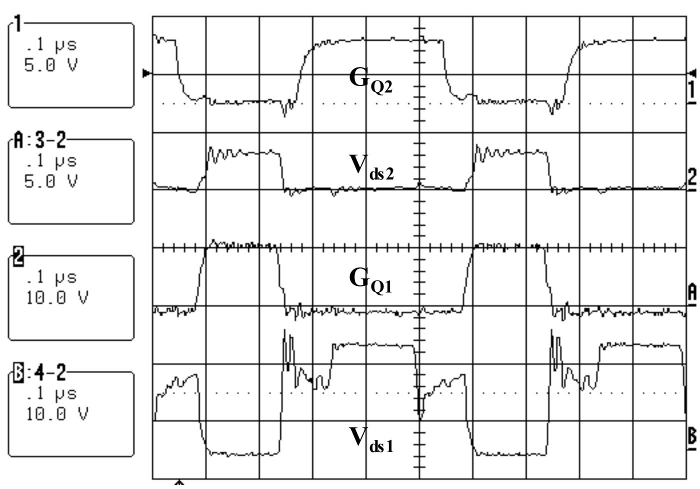
For the clamp circuit, two 1A/25V Schottky diodes and one 2.2μF ceramic capacitor with 0805 package are used. Without the clamp circuit, there is a huge voltage spike across the top switch when it is turned off. As the load current increases, the voltage spike will go even higher, which renders the 30V MOSFETs no longer safe. However, with the clamp circuit, the voltage stress across the top switch is perfectly clamped below 22 V. The leakage energy can be stored in the clamp capacitor and then recovered to the output. Furthermore, the bottom-switch voltage stress waveform V_{ds2} in Fig. 4.26 shows that the clamp circuit can also reduce the voltage-ringing when the top switch is turned on. This can help to attenuate the body diode reverse-recovery loss.

Fig. 4.26 shows the operation waveform comparison between the proposed topology and the conventional buck converter at 2 MHz. The duty cycle of the proposed topology is doubled, and the voltage stress of its bottom switch is reduced by half. The voltage-ringing of V_{ds2} is reduced from 7 V to 2 V for the peak-to-peak value. With the clamp circuit, the top-switch turn-off spike in the winding-coupled buck converter is almost the same as in the conventional buck converter. All of these indicators predict a significant loss reduction related to switching frequency.

Fig. 4.27 shows the efficiency improvement compared with the conventional buck converter. The full-load efficiency increases from 4.5% at 1 MHz to 8% at 2 MHz. More than 85% efficiency at 1 MHz and more than 80% efficiency at 2 MHz can be achieved with the discrete component design for the proposed winding-coupled buck converter.

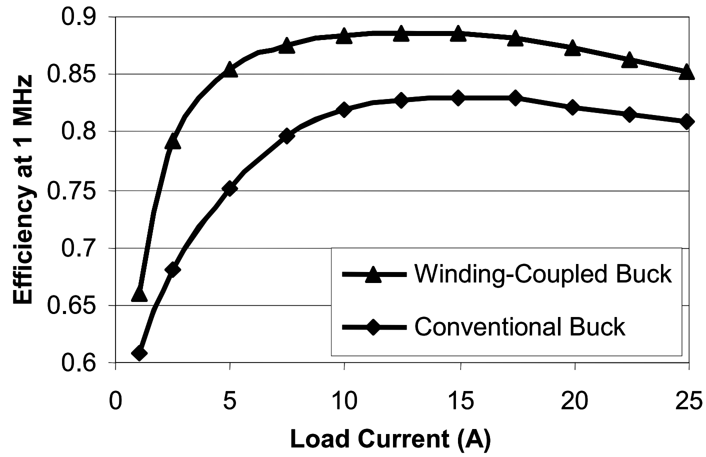


(a)

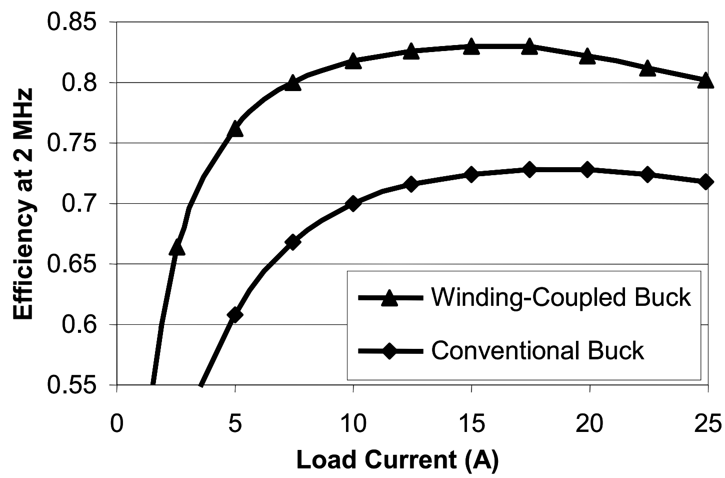


(b)

Fig. 4.26. The comparison of the operation waveforms at 2 MHz: (a) buck converter and (b) the proposed converter.



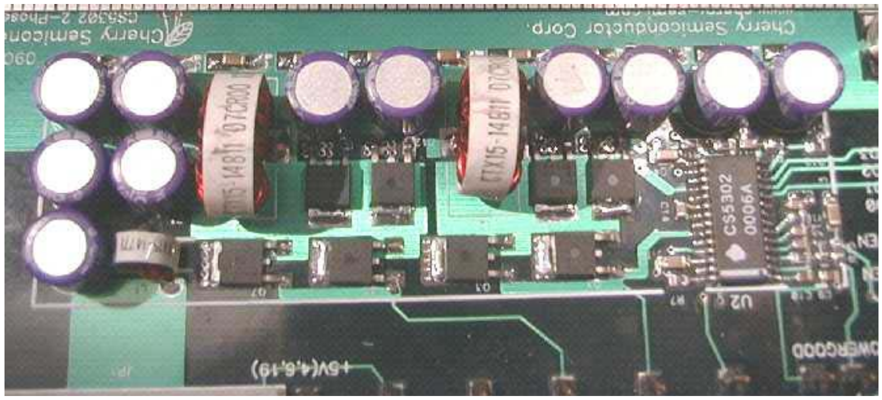
(a)



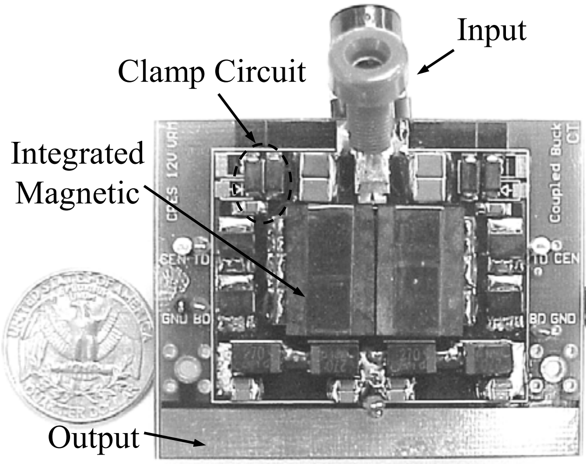
(b)

Fig. 4.27. The efficiency comparison: (a) efficiency at 1 MHz; and (b) efficiency at 2 MHz.

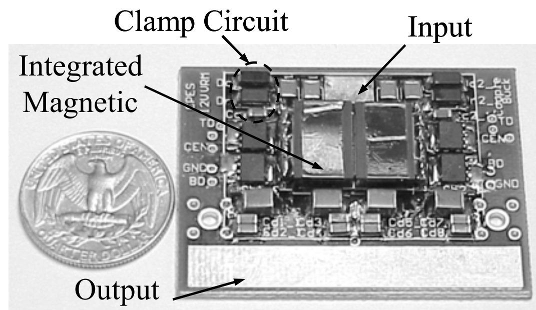
Fig. 4.28 shows the developed prototypes of the proposed winding-coupled buck converter with one-ounce, two-layer PCB. The power density is 48 w/in^3 for the 1MHz VRM and 82 w/in^3 for the 2MHz VRM. This is a significant improvement as compared with the state-of-the-art VRM design that offers about 10 w/in^3 power density.



(a)



(b)



(c)

Fig. 4.28. (a) A conventional product, and the developed prototypes: (b) 1MHz VRM and (c) 2MHZ VRM.

4.4. Concept Extension with an Autotransformer Structure

Sections 4.2 and 4.3 analyze two topologies, which are constructed with coupled inductors to extend the duty cycle. It is well known that a transformer can extend the duty cycle when the turns ratio is properly designed. Forward, push-pull, half-bridge and full-bridge converters are all isolated topologies, the equivalent circuit of which is the buck converter. More analysis shows that the coupled inductors play the same function as an autotransformer. This is clearly shown in the TI buck converter.

Fig. 4.29(b) shows the equivalent circuit with separated coupled windings. This multi-terminal inductor is exactly the transformer in the flyback converter. As a result, the TI can be looked at as a flyback autotransformer, which has simple structure and plays the same function of extending the duty cycle. Now it is natural to think that there may be other topologies, which are implemented with autotransformers and have better performance.

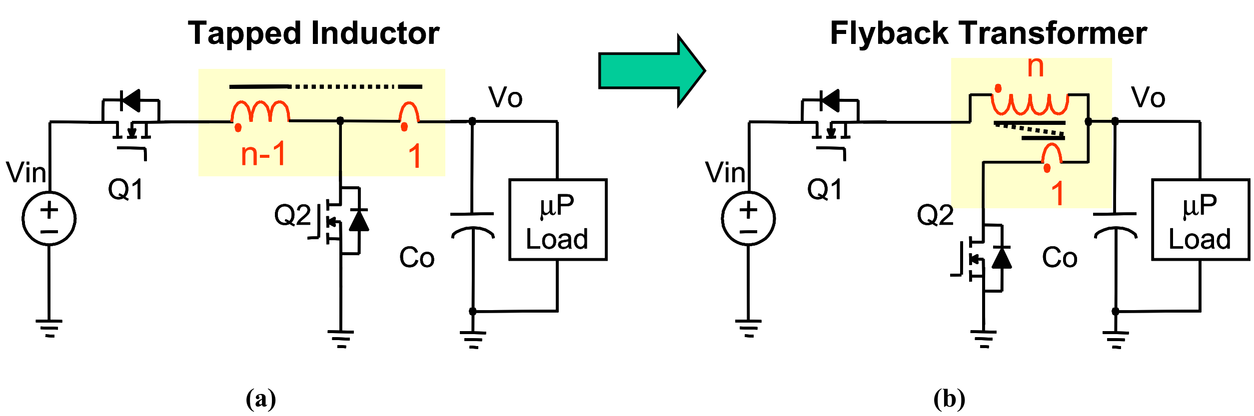


Fig. 4.29. (a) The tapped-inductor converter, and (b) the equivalent flyback transformer structure.

4.4.1. Autotransformer Structure

Autotransformers are widely used in high-power AC systems in which there is no galvanic isolation requirement [C26-C29]. Compared with an isolated transformer, which has separate primary and secondary windings, the autotransformer uses part of the primary winding as the secondary winding in a tapped version (for step-down conversion). Fig. 4.30 shows the difference between an isolated transformer and an autotransformer. The isolated transformer has a primary winding with n_p turns and a secondary winding with n_s turns. The autotransformer has only one winding with n_p turns. The tapped connection constructs the output, so that the secondary winding shares n_s turns of the total winding turns.

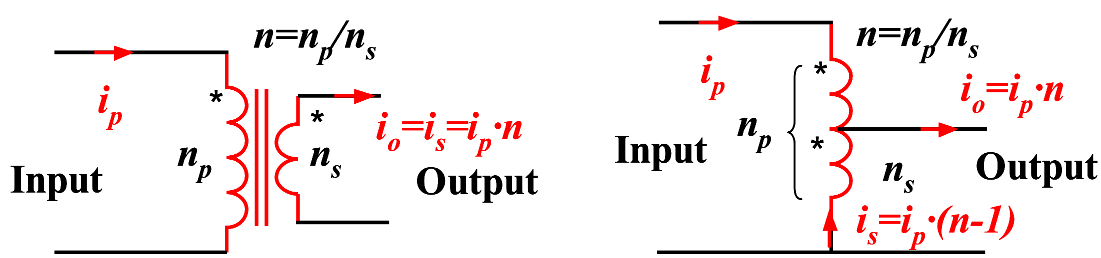


Fig. 4.30. The comparison: (a) an isolated transformer and (b) an autotransformer.

Both transformers can transfer the same power as long as their turns ratios are the same:

$$n = n_p / n_s . \tag{4.25}$$

But in the autotransformer, the input current goes directly to the output, which reduces the secondary winding current. The secondary winding current is

$$i_s = i_p \cdot n \tag{4.26}$$

in the isolated transformer, and is

$$i_s = i_p \cdot (n-1) \tag{4.27}$$

in the autotransformer. Here, i_p is the transformer primary winding current.

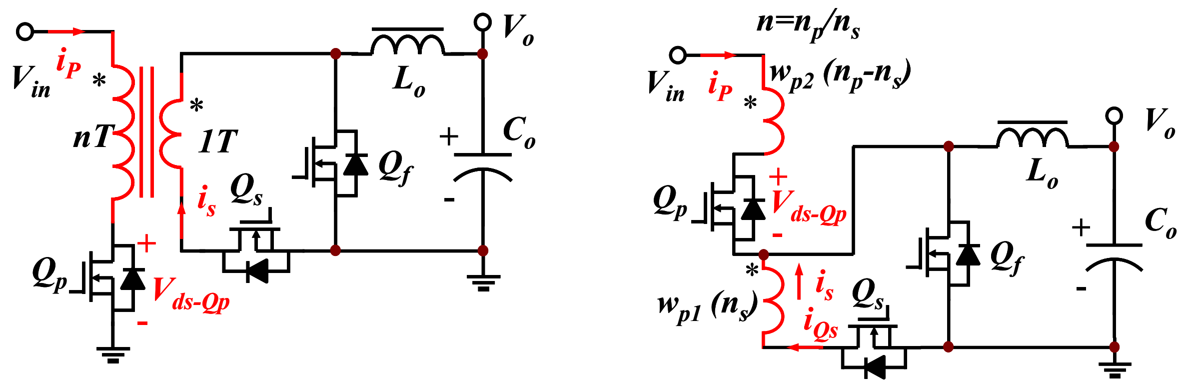
Furthermore, the primary winding current in the autotransformer goes through only *(n_p-n_s)* turns of winding, while in the isolated transformer the same current goes through n_p turns of winding. All of these factors mean that, for the same power transformation, less copper can be used with an autotransformer as compared with an isolated transformer. The savings effect is significant, especially when the transformer turns ratio is near 1 (n>1 for step-down conversion).

The autotransformer has mostly been discussed in terms of its application to the 50/60Hz high-power systems. But actually, the benefits of the autotransformer can also be extended to the high-frequency DC-DC converters controlled by PWM. The topologies discussed in Sections 4.2 and 4.3 are two examples. We can extend the concept to all isolated topologies by replacing the isolated transformer with an autotransformer.

4.4.2. A Family of Buck-Type Converters with Autotransformers

Theoretically, all topologies with isolated transformers can be implemented with autotransformers. However, the autotransformer is a three-port component while the isolated transformer has four ports. Fig. 4.30 shows the difference. Normally, an autotransformer can not simply replace an isolated transformer because of the different connection. This section derives a family of buck-type converters with autotransformers, which corresponds to forward, push-pull, half-bridge and full-bridge converters. For convenience, these topologies are referred to as non-isolated ones.

Fig. 4.31 shows the comparison between the isolated and non-isolated forward converters. For simplicity, the transformer reset winding is not drawn here. When Q_p and Q_s are on, windings w_{p1} and w_{p2} form an autotransformer to transfer the energy.



(a) (b)

Fig. 4.31. The forward converter: (a) with an isolated transformer, (b) with an autotransformer.

The preceding analysis shows that the implementation of the autotransformer is not necessarily limited in the tapped-winding connection structure, as shown in Fig. 4.30(b). Instead, it can be implemented with two coupled windings, and switches may be put between them. This kind of flexibility offers more benefits for the DC-DC converter with autotransformers.

Push-pull, half-bridge and full-bridge converters operate as two interleaved forward converters in which PWM control signals are phase-shifted by 180 degrees. There are two types of rectification circuits for this interleaving operation. One is the current-doubler rectifier with two output filter inductors. Another is the center-tapped rectifier with only one filter inductor. Both of these rectifiers can be implemented with an autotransformer.

Fig. 4.32 shows the non-isolated push-pull converters. Fig. 4.33 shows the gate-control signals. In Fig. 4.32, when Q_{p1} and Q_{f2} are on, the windings w_{p1} and w_s form an autotransformer to transfer the energy. The situation is the same when Q_{p2} and Q_{f1} are on. The only difference is that winding w_{p2} functions instead of winding w_{p1}. Because of the advantage of the autotransformer, windings w_{p1} and w_{p2} need fewer turns as compared with those in the isolated transformer. The non-isolated push-pull converters can use bootstrap gate drivers, since the primary-side and secondary-side switches are connected in a totem-pole structure (Q_{p1} and Q_{f1}, Q_{p2} and Q_{f2}).

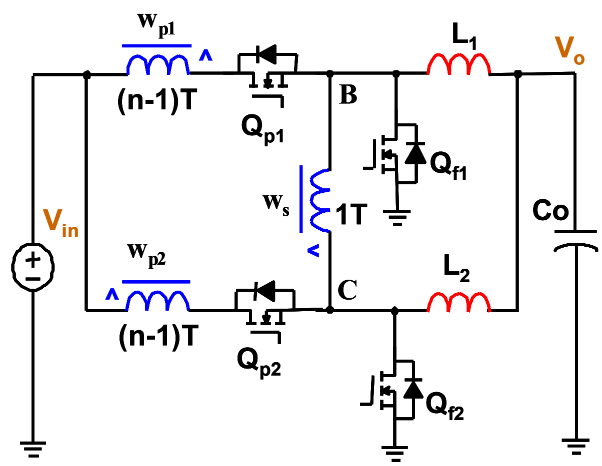


Fig. 4.32. The non-isolated push-pull converter.

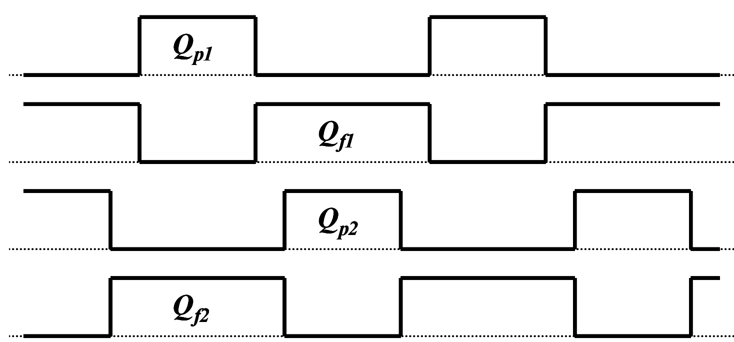


Fig. 4.33. The gate signals for the push-pull converter.

Fig. 4.34 shows the non-isolated half-bridge converters. Only one capacitor can be used, which is different from the isolated ones. This is because of the voltage-second balance for the autotransformer. For symmetrical operation of the half-bridge converters, the gate-control signals are the same as those shown in Fig. 4.33. In Fig. 4.34, when Q_{p1} and Q_{f2} or Q_{p2} and Q_{f1} are on, the windings w_p and w_s form an autotransformer to transfer the energy.

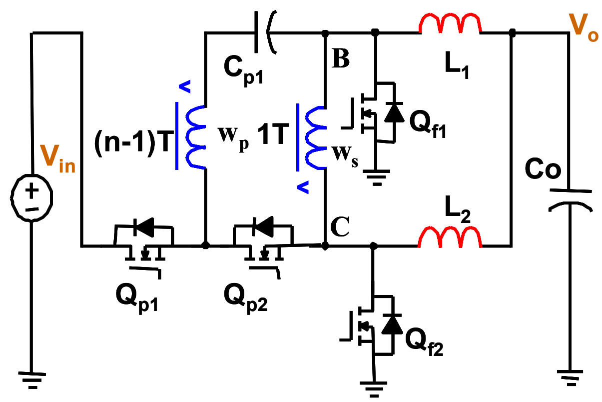


Fig. 4.34. The non-isolated half-bridge converter.

Fig. 4.35 shows the non-isolated full-bridge converters. Both phase-shifted and PWM control methods can be used. When Q_{p1}, Q_{p4} and Q_{f2} or Q_{p2}, Q_{p3} and Q_{f1} are on, the autotransformer transfers the energy. During all other periods, the currents freewheel. More detailed analysis has been done for the non-isolated full-bridge converter with a current-doubler rectifier [C24].

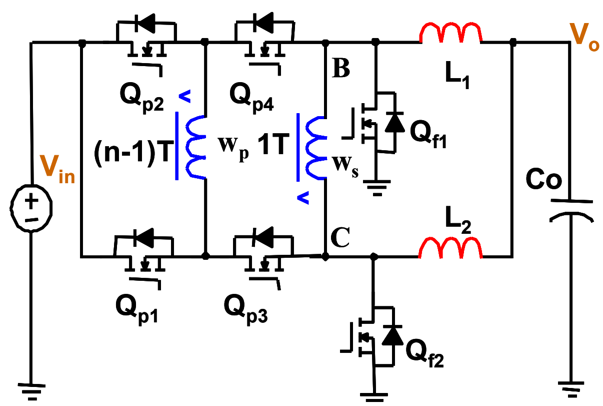


Fig. 4.35. The non-isolated full-bridge converter.

The gate drive for the non-isolated half-bridge and full-bridge converters is a little more complicated. A bootstrap gate driver can still be used to drive $Q_{p2}$and Q_{f2}. But driving $Q_{p1}$and Q_{f1} is different, since they are no longer in a totem-pole structure. For the non-isolated full-bridge converters, each of the primary switches ($Q_{p1\sim p4}$) needs a bootstrap driver.

4.4.3. Candidate Autotransformer Topologies for VRM Applications

In the following discussion, the turns number of the secondary winding is normalized to 1. The output load current is I_o. And the output filter inductance value is assumed to be large enough that the current ripple can be ignored.

All topologies discussed in Section 4.4.2 can extend the duty cycle by “n” time, which is the turns ratio. The autotransformer can also simplify the design with less winding turns and relatively low conduction loss.

Compared with the buck converter, the non-isolated forward converter is equivalent to a single-phase solution, but it requires more devices and the autotransformer. The non-isolated push-pull converter is equivalent to a two-phase solution, and there is no increase in the device numbers. However, the leakage inductance in the transformer requires extra clamp circuits to limit the device turn-off voltage spikes. The non-isolated half-bridge and full-bridge converters are also equivalent to a two-phase solution, and there is no need for a clamp circuit. When one switch is turned off, the leakage inductor current has another path to conduct, so there are no turn-off voltage spikes.

The phase-shifted buck [C24] is an isolated full-bridge converter with a current-doubler rectifier, as shown in Fig. 4.35. Two single-turn windings form an autotransformer, which doubles the duty cycle. Fig. 4.36 shows the developed prototype. With the help of ZVS soft-switching, this new approach improves the full-load efficiency by 10% for a 12V-to-1.3V/70A VRM at a switching frequency of 1 MHz. The efficiency is even higher than a buck converter operating at 500KHz frequency. Fig. 4.37 shows the efficiency comparison. The high operation frequency can help to significantly reduce the number of output capacitors, which are the highest-cost part in a VRM. Fig. 4.38 shows the 40% potential cost reduction with the proposed phase-shifted buck converter.

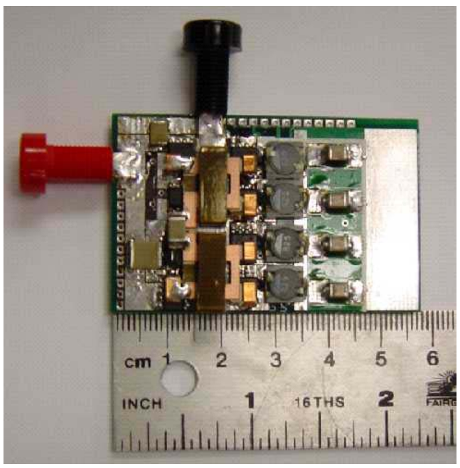


Fig. 4.36. The phase-shifted buck (non-isolated full-bridge converter with a current-doubler rectifier).

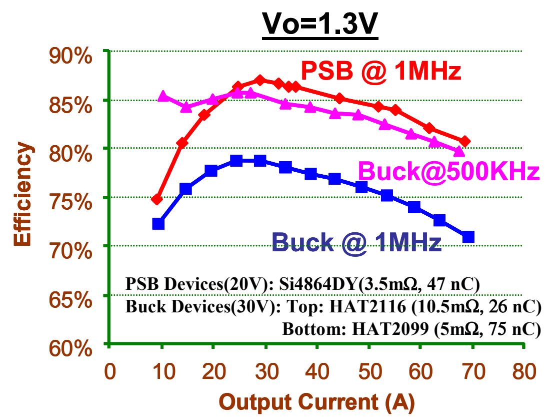
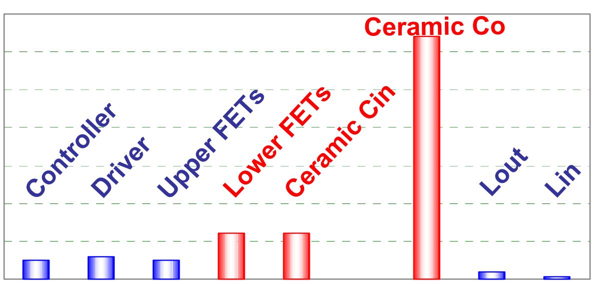
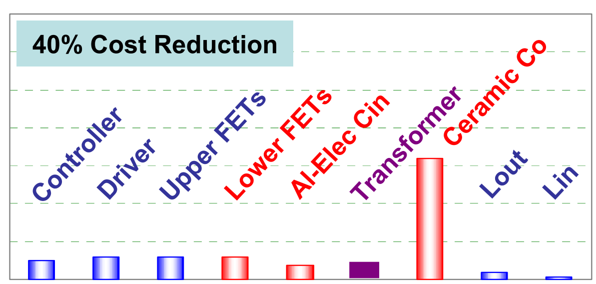


Fig. 4.37. The efficiency comparison between the phase-shifted buck and the buck converters.



(a)



(b)

Fig. 4.38. Cost analysis: (a) for a buck converter and (b) for a phase-shifted buck converter.

Fig. 4.39 shows the loss breakdown comparison between the buck and the non-isolated full-bridge converter. The switching loss is almost eliminated, and the body diode conduction loss is significantly reduced. Because of the phase-shifted operation, the bottom-switch conduction loss is slightly increased. However, since the voltage stress of the bottom switch is only about 6 V, a lower-voltage-stress MOSFET can help to reduce this part of the loss.

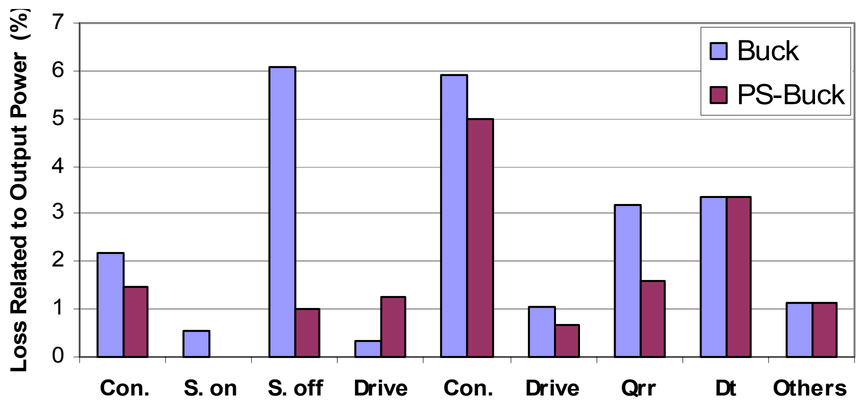


Fig. 4.39. The loss analysis for the phase-shifted buck converter.

The non-isolated half-bridge converter is very promising in extending the duty cycle. For example, in Fig. 4.40, two single-turn coupled windings can extend the duty cycle by four times compared with that in the buck converter. Consequently, the voltage stress of the synchronous rectifiers is only 3 V, which allows the use of low-voltage-stress MOSFETs to further reduce the conduction loss. Fig. 4.41 shows the simulation results.

For the non-isolated full-bridge converter, the same transformer design can only double the duty cycle.

Table 4.1 shows the comparison. In order to achieve the same duty cycle, the full-bridge converter needs one coupled winding to be three turns, which not only increases the complexity of the transformer, but also introduces more conduction loss. Also, the phase-shifted control causes more conduction loss because of the freewheeling current.

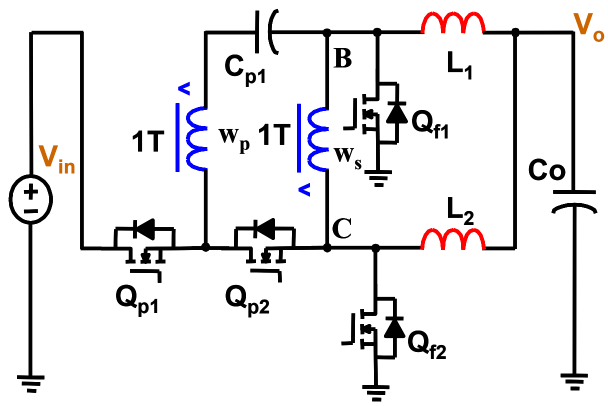


Fig. 4.40. The non-isolated half-bridge converter with single-turn autotransformer structure.

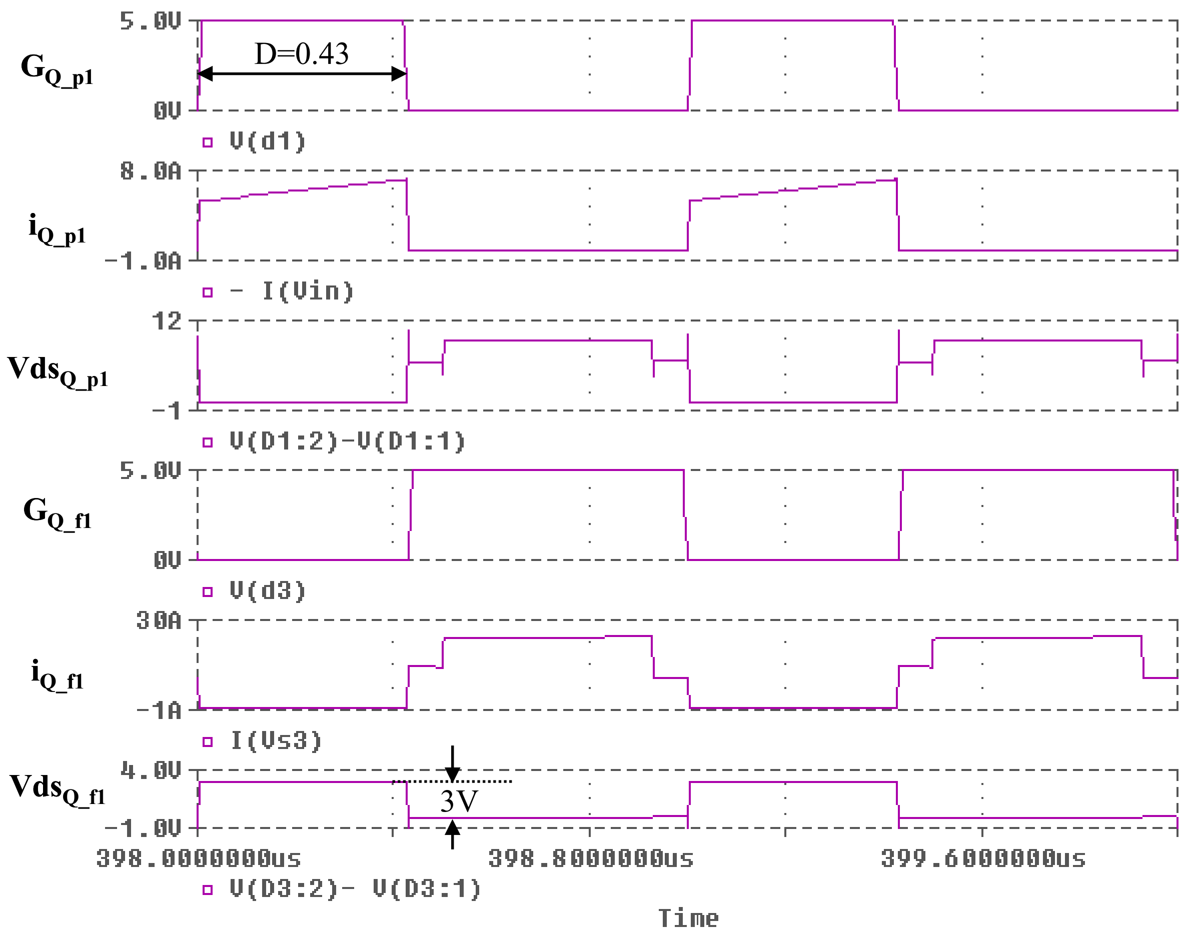


Fig. 4.41. The simulation waveforms of the non-isolated half-bridge converter.

Table 4.1. The comparison between the half-bridge and full-bridge with the same autotransformer design.

Half-Bridge vs. Full Bridge	Duty Cycle (<50%)	$Q_{p1\sim p2}$ vs. $Q_{p1\sim p4}$		Q_{f1}, Q_{f2}		Transformer Current	
		i_{Qp}	V_{ds_Qp}	i_{Qf}	V_{ds_Qf}	w_p	w_s
Half-Bridge	$\frac{2\cdot n\cdot V_o}{V_{in}}$	$\frac{I_o}{2\cdot n}$	V_{in}	$(1-\frac{1}{2\cdot n})\cdot I_o$	$\frac{V_{in}}{2\cdot n}$	$\frac{I_o}{2\cdot n}$	$(1-\frac{1}{n})\cdot\frac{I_o}{2}$
Full-Bridge	$\frac{n\cdot V_o}{V_{in}}$	$\frac{I_o}{2\cdot n}$	V_{in}	$(1-\frac{1}{2\cdot n})\cdot I_o$	$\frac{V_{in}}{n}$	$\frac{I_o}{2\cdot n}$	$(1-\frac{1}{n})\cdot\frac{I_o}{2}$

Fig. 4.42 shows the loss breakdown comparison between the non-isolated full-bridge and half-bridge converters. The half-bridge converter has less top-switch conduction loss because there is no freewheeling current. Also, the reverse-recovery loss of the synchronous rectifier body diode is smaller because of the lower voltage stress. However, the full-bridge converter has less switching loss with zero-voltage-switching (ZVS) operation. The smaller duty cycle of the full-bridge converter introduces less conduction loss on the synchronous rectifier if the same power MOSFETs are used. However, the half-bridge converter can use even lower voltage stress MOSFETs to reduce this part of the loss. Also, the circuit is relatively simpler for the half-bridge converters. Overall, both topologies are good candidates for the VRM applications. It is a design trade-off to determine which one is more suitable.

The half-bridge converters can also be controlled asymmetrically to achieve ZVS [C35].

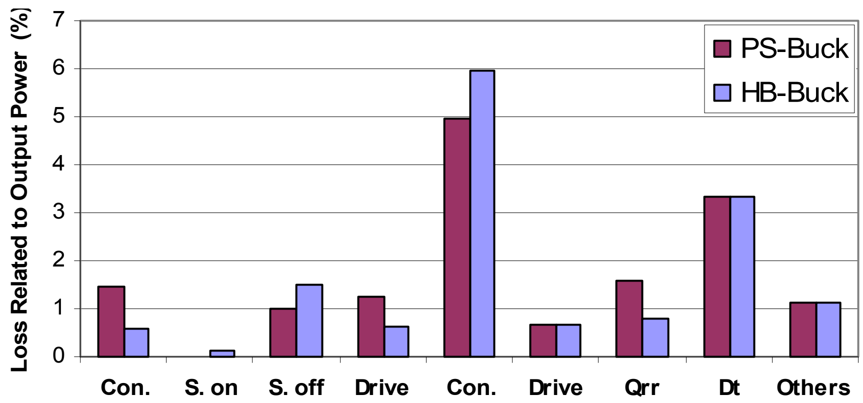


Fig. 4.42. The loss breakdown comparison between the non-isolated half-bridge and full-bridge converters.

For the 12V-input VRM applications, compared with a conventional multiphase buck converter, an autotransformer can use a simple winding structure to easily extend the duty cycle. The 30V trench MOSFETs can still be used for the control switches to achieve fast switching speed. And the lower voltage stress of the synchronous rectifiers (the switches in the secondary side) allows the use of MOSFETs with smaller R_{ds_on}. As a result, the non-isolated topologies are expected to achieve higher efficiency than the conventional multiphase synchronous buck converter, with only a slight increase of the circuit complexity.

From the loss breakdown analysis, we can see that the dead-time body diode conduction is still a potential barrier for high-frequency applications. This part of the loss is proportional to the switching frequency. The next chapter will discuss how to eliminate this loss by using a quasi-resonant topology technique.

Chapter 5. High-Frequency Topologies Based on Quasi Resonance

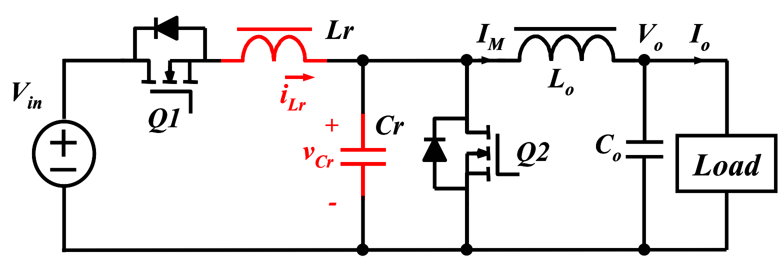
Chapter 4 introduces a series of new topologies based on PWM control in order to improve the performance of the 12V-input VRM. The basic idea is to extend the duty cycle and to reduce the switching current by using coupled inductors or autotransformers. However, most of these topologies are hard switching. Although the phase-shifted buck converter can achieve ZVS [C24], the problems related to the bottom-switch body diode remain. And its circuit structure is relatively complicated.

In order to further improve the efficiency by minimizing the switching loss and bottom-switch body diode conduction loss, this chapter introduces a novel design based on two concepts: quasi-resonant soft switching and active-clamped ZVS. Section 5.1 introduces the step-by-step circuit evolution based on a buck converter. Section 5.2 explains the operation principle based on principle operation waveforms and state-plane trajectories. Section 5.3 extends the concept to all topologies, and a circuit design for the TI buck converter is discussed in Section 5.4. Finally, experimental results in Section 5.5 show the significant efficiency improvement at 1MHz switching frequency.

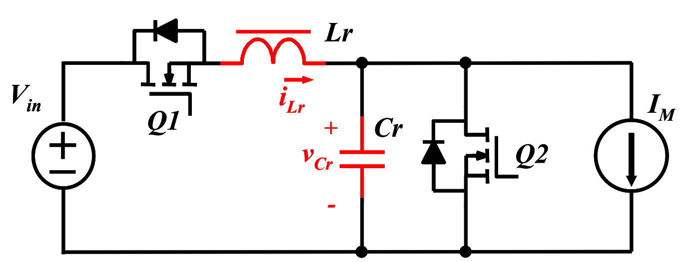
5.1. Quasi-Resonant Active-Clamped Buck Converter

5.1.1. Quasi-Resonant Buck Converter

The use of the quasi-resonant circuit to achieve zero-current switching (ZCS) is well documented [D1-D15]. Fig. 5.1(a) shows a quasi-resonant ZCS buck converter. Inductor Lr and capacitor Cr are used along with switch Q1 to form a high-frequency resonant switch, while L_o and C_o form a low-pass filter. Since the corner frequency of the low-pass filter is much lower than the operating frequency of the resonant switch, the influence of the filter dynamics on the resonant-switch behavior over several switching cycles can be ignored. Assuming that the output-filter inductance L_o is sufficiently large, the filter section can simply be replaced with a constant current source with a magnitude equal to the load current I_o. The simplified circuit is shown in Fig. 5.1(b). It is of second order, and its behavior can be conveniently described on the state plane.



(a)



(b)

Fig. 5.1. A quasi-resonant ZCS buck converter: (a) basic circuit, and (b) simplified circuit.

A synchronous rectifier Q2 is used here instead of a freewheeling diode in order to reduce the conduction loss. Another advantage of the synchronous rectifier is that the circuit can achieve constant-switching-frequency operation [D16-D23].

Fig. 5.2 shows some key operation waveforms. Controlling the time period (t_0-t_1) can adjust the initial resonant inductor current so that the output voltage can be regulated. The ZCS operation eliminates the Q1 turn-off loss. Because the resonant inductor Lr limits the di/dt of the Q1 turn-on current, there is no Q2 body diode reverse-recovery problem. Also, since there is no shoot-through problem between Q1 and Q2, dead-time control is no longer needed. Furthermore, the resonant capacitor Cr is paralleled with the synchronous rectifier Q2. Cr acts as a very large turn-off snubber for Q2. And Q2 can be turned on when V_{Cr} resonates back to zero. As a result, the body diode of Q2 never conducts currents. It is very clear that the ZCS quasi-resonant buck converter offers a very good operating condition for the synchronous rectifier Q2.

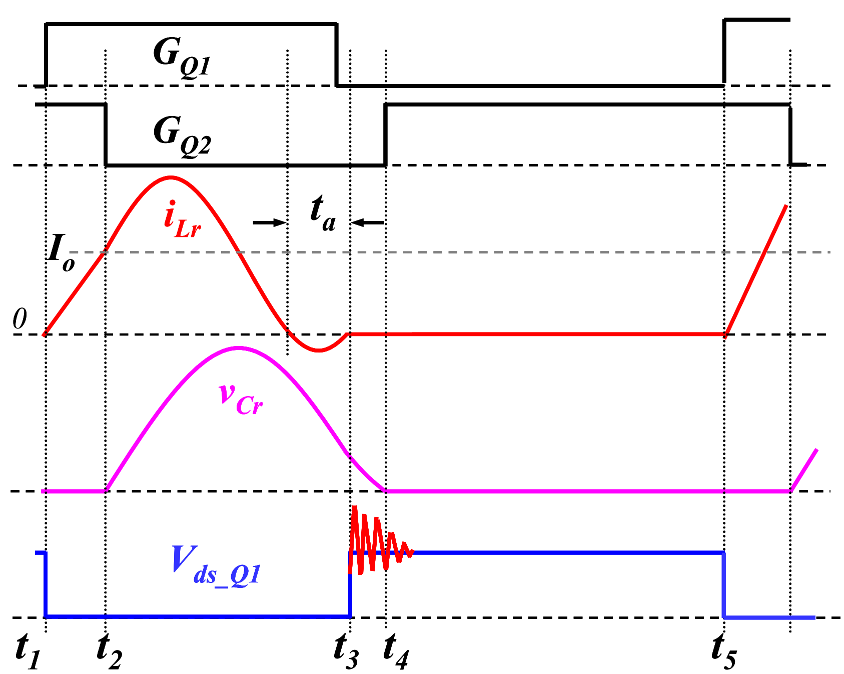


Fig. 5.2. Key operation waveforms in the quasi-resonant ZCS buck converter

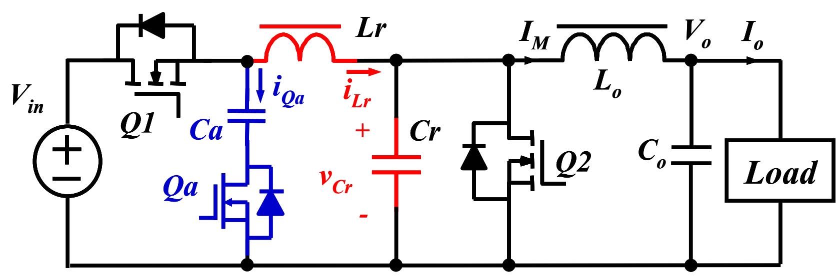
However, the operating condition for the top switch Q1 is limited by its hard turn-on and its turn-off drain-to-source voltage oscillation [D4] (as shown in Fig. 5.2). This condition not only induces switching loss, but also causes electromagnetic interference (EMI) problems. The turn-off time must be within the period t_a, which is required to sense the Q1 current. Also, the timing is not easy to control because of the short period of t_a, especially at high-frequency operations. Furthermore, the body diode of Q1 conducts current in period t_a after Q1 is turned off. The situation is even worse at light-load conditions.

The ZVS operation of Q1 can eliminate all of these problems related to Q1 [D24-D32]. However, a quasi-resonant ZVS buck converter loses all the benefits of eliminating the Q2 body diode problems. Also, the voltage stress of Q1 is too high to use 30V voltage stress MOSFETs for the 12V-input voltage. In order to maintain the benefits of Q2 and to achieve ZVS operation for Q1, the active-clamped circuit is utilized.

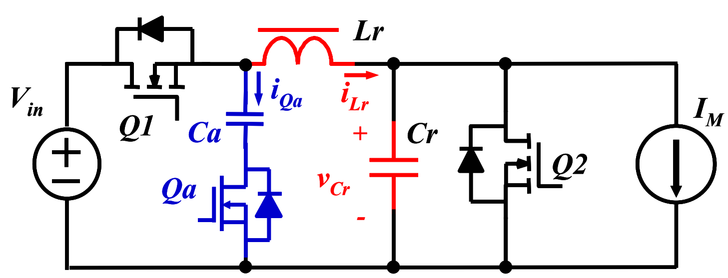
5.1.2. Idea to Use an Active-Clamped Circuit

Active-clamped methods have been explored in detail for forward and flyback converters [D33-D39]. It is well known that the active-clamped circuit provides a means of achieving ZVS. Fig. 5.3 shows the circuit, and Fig. 5.4 shows some key operation waveforms at the full-load condition. The auxiliary switch Qa and capacitor Ca form the active-clamped circuit. The gate control signal of Qa is complementary to that of Q1. The resonant tank design is modified so that the inductor current will not resonate back to negative. Instead, after three quarters of the resonant period, Q1 is controlled with a fixed duty cycle D and is turned off with a small positive current. Then, the active-clamped circuit plays its role to achieve ZVS for both Q1 and Qa. The small turn-off current not only helps to reduce the switching losses, but also limits the circulating currents in the active-clamped circuit. Furthermore, snubber capacitors can be used in parallel with Q1 and Qa to further reduce the switching loss. Meanwhile, Q2 maintains its good operating condition with no body diode reverse-recovery and no body diode current conduction because of the same L, C resonant operation.

The basic idea is very simple. For the buck converter, the quasi-resonant circuit is used to achieve ZVS for the bottom switch Q2, and the active-clamped circuit is used to achieve ZVS for the top switch Q1. As a result, the body diode and switching loss problems are solved. The combination of these two concepts can also make the circulation current in the clamp circuit very small. The next section will discuss the operation principle in detail.



(a)



(b)

Fig. 5.3. The quasi-resonant active-clamped ZVS buck converter: (a) basic circuit, and (b) simplified circuit.

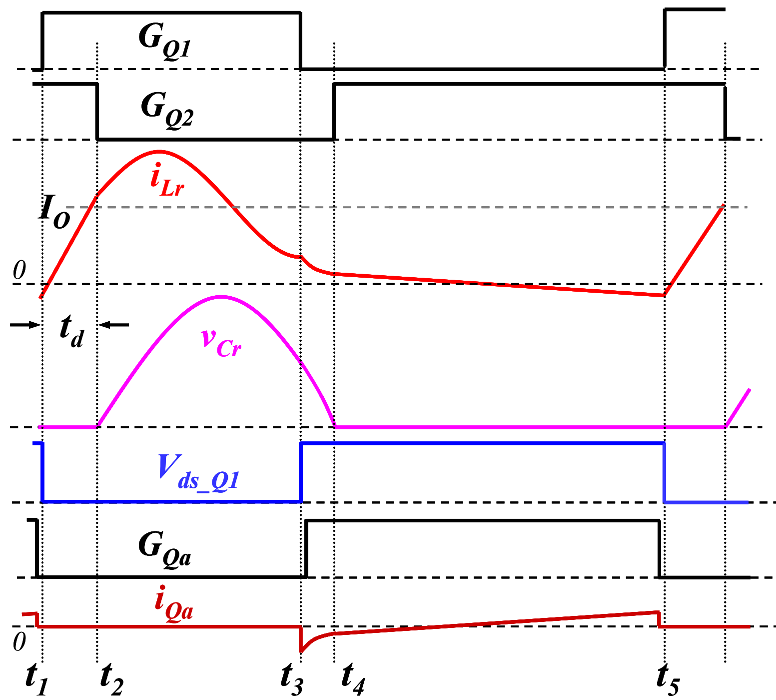


Fig. 5.4. Key operation waveforms in the quasi-resonant active-clamped ZVS buck converter at full-load condition.

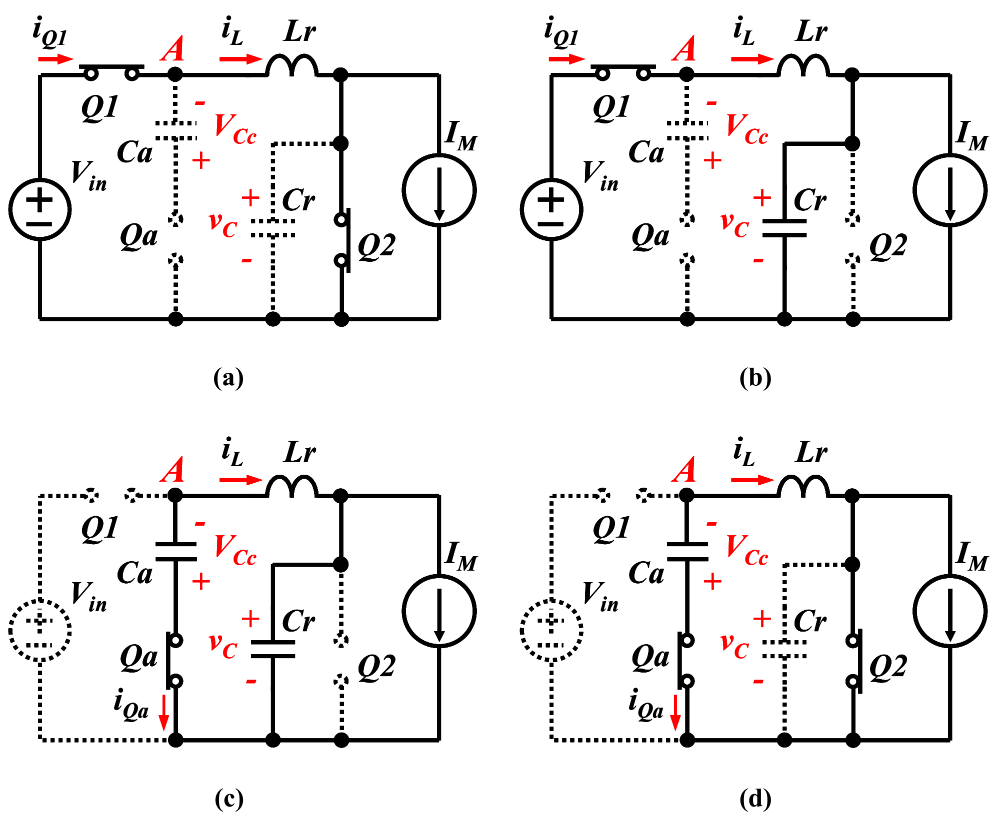
5.1.3. The Operation Principle

In Fig. 5.3, Q1 is controlled with a fixed duty ratio. A clock determines the turn-on time t_1. The fixed duty cycle makes Q1 turn off when the current resonates to the valley value at full-load condition. The gate signals of Q1 and Qa are complementary, with small dead-times to avoid shoot-through. A phase-shifted controller adjusts the delay time between the turn-on time of Q1 and the turn-off time of Q2 in order to regulate the output voltage. The active-clamped voltage is a constant, which can be derived from the voltage-second balance of the output inductor and the resonant inductor, as follows:

$$V_{Ca} = \frac{V_{in} \cdot D_{Q1} - V_o}{1 - D_{Q1}}, \tag{5.1}$$

where D_{Q1} is the fixed duty cycle of Q1.

One cycle of operation for the quasi-resonant active-clamped ZVS buck converter is described by four topological stages. The equivalent circuits for these four stages are shown in Fig. 5.5. Assuming ideal circuit components, the equations describing the circuit for each stager are given later.



(a) (b) (c) (d)

Fig. 5.5. Four major operational stages: (a) I. phase-shifted control period, (b) II. resonant period 1, (c) III. resonant period 2, and (d) IV. freewheeling period.

1) Stage I: Phase-Shifted Control Period [t_1-t_2]

In Stage I, both Q1 and Q2 are conducting. The active-clamped circuit does not work, and the resonant capacitor is shorted by Q2. The magnetizing current i_M is freewheeling through Q2 in a manner of synchronous rectification. The resonant inductor current i_L rises linearly, while capacitor voltage v_C stays at zero. This stage is described by

$$\begin{cases} i_L(t) = \dfrac{V_{S1}}{L_r} \cdot (t - t_1) \\ v_C(t) = 0 \end{cases}, \tag{5.2}$$

where $V_{S1} = V_{in}$. (5.3)

When i_L is larger than the magnetizing current I_M, which is I_o for the buck converter, Q2 will start to conduct a current in the positive direction. At t_2, Q2 is turned off, and the circuit operates into Stage II. Actually, Stage I is the phase-shifted control period. The delay time from t_1 to t_2 is controlled to generate different initial resonant currents through resonant capacitor Cr so that the output voltage can be regulated. This initial resonant current is defined as:

$$I_{C\_t2} = i_L(t_2) - i_M. \tag{5.4}$$

2) Stage II: Resonant Period 1 [t2-t3]

At t_2, Q2 is turned off with a positive current. Current $i_L(t)$-I_M is now charging capacitor Cr. The active-clamped circuit still does not work. The equations for this stage are

$$\begin{cases} i_L(t) = I_M + \dfrac{V_{S1}}{Z_n} \cdot \sin\omega_n \cdot (t - t_2) + I_{C\_t2} \cdot \cos\omega_n \cdot (t - t_2) \\ v_C(t) = V_{S1} - V_{S1} \cdot \cos\omega_n \cdot (t - t_2) + I_{C\_t2} \cdot Z_n \cdot \sin\omega_n \cdot (t - t_2) \end{cases}, \tag{5.5}$$

where $Z_n = \sqrt{Lr/Cr}$ is characteristic impedance, and $\omega_n = 1/\sqrt{Lr \cdot Cr}$ is resonant angular frequency.

By defining

$$\alpha = \tan^{-1}\left(\frac{I_{C\_t2} \cdot Z_n}{V_{S1}}\right) \text{ and} \tag{5.6}$$

$$V_{R1} = \sqrt{{V_{S1}}^2 + (I_{C\_t2} \cdot Z_n)^2}\ , \tag{5.7}$$

Equation (5.5) can be simplified as

$$\begin{cases} i_L(t) = I_M + \dfrac{V_{R1}}{Z_n} \cdot \sin[\omega_n \cdot (t - t_2) + \alpha] \\ v_C(t) = V_{S1} - V_{R1} \cdot \cos[\omega_n \cdot (t - t_2) + \alpha] \end{cases}. \tag{5.8}$$

Also, Cr plays the function of a very large turn-off snubber of Q2 so that there is almost no turn-off loss. After about three-fourths of the resonant period, when the inductor current resonates to the lowest value, Q1 is turned off at t_3 with a very low level of current. The inductor current is shifted to the active-clamped circuit branch. Qa can easily achieve ZVS. Next comes Stage III.

3) Stage III: Resonant Period 2 [t3-t4]

When Q_1 is turned off at t_3, the voltage across resonant capacitor Cr is still not zero. Also, the resonant inductor current is not zero. These form the initial condition for the next LC resonance, which is through the active-clamped circuit. For Stage III, the initial current through resonant capacitor Cr and the initial voltage across resonant inductor Lr are

$$\begin{cases} I_{C\_t3} = i_L(t_3) - I_M \\ V_{L\_t3} = V_{S2} - v_C(t_3) \end{cases}. \tag{5.9}$$

where, $V_{S2} = -V_{Ca}$. (5.10)

The equations for this stage are:

$$\begin{cases} i_L(t) = I_M + \dfrac{V_{L\_t3}}{Z_n} \cdot \sin\omega_n \cdot (t - t_3) + I_{C\_t3} \cdot \cos\omega_n \cdot (t - t_3) \\ v_C(t) = V_{S2} - V_{L\_t3} \cdot \cos\omega_n \cdot (t - t_3) + I_{C\_t3} \cdot Z_n \cdot \sin\omega_n \cdot (t - t_3) \end{cases} . \tag{5.11}$$

By defining

$$\beta = \tan^{-1}\left(\frac{I_{C\_t3} \cdot Z_n}{V_{L\_t3}} \right) \text{ and} \tag{5.12}$$

$$V_{R2} = \sqrt{{V_{L\_t3}}^2 + (I_{C\_t3} \cdot Z_n)^2} \ , \tag{5.13}$$

Equation (5.11) can be simplified as

$$\begin{cases} i_L(t) = I_M + \dfrac{V_{R2}}{Z_n} \cdot \sin[\omega_n \cdot t + \beta] \\ v_C(t) = V_{S2} - V_{R2} \cdot \cos[\omega_n \cdot t + \beta] \end{cases} . \tag{5.14}$$

4) Stage IV: Freewheeling Period [t4-t5]

At time t_4, when v_{Cr} crosses the zero, Q2 is turned on as a synchronous rectifier. The body diode of Q2 does not conduct the current. The magnetizing current i_M is freewheeling through Q2, and the resonant inductor current is charging the active-clamped capacitor Ca. This stage is described by

$$\begin{cases} i_L(t) = i_L(t_4) + \dfrac{V_{S2}}{L_r} \cdot (t - t_4) \\ v_C(t) = 0 \end{cases} . \tag{5.15}$$

Because Ca must maintain the charge balance, finally i_L will flow in the negative direction. Then at t_5, Qa is turned off with a low level of current in the positive direction, which helps Q1 to achieve ZVS. Since the Stage III is very short, from the charge balance of the clamp capacitor Ca, the inductor current at t_5 is approximately:

$$i_L(t_5) = -i_L(t_4) . \tag{5.16}$$

From (5.15) and (5.16), the turn-off current of Qa or Q1 is about

$$i_{Qa\_off} \approx i_{Q1\_off} \approx \frac{-V_{S2}}{2 \cdot L_r} \cdot \frac{1-D_{Q1}}{f_s}, \tag{5.17}$$

where f_s is the switching frequency, and D_{Q1} is the fixed duty cycle for top switch Q1. This shows that the load current has no impact on the switching current. As a result, it is easy to design a capacitor paralleling to Q_1 or Q_a as a turn-off snubber to further reduce the switching loss for the entire operating load range.

Employing (5.2), (5.8), (5.14) and (5.15), the state portrait of the converter can be easily displayed on the i_L versus v_C plane. A typical steady-state trajectory at the full-load condition is shown in Fig. 5.6, where the inductor current is represented with a factor Z_n. Fig. 5.6 shows that the state trajectory consists of four segments, corresponding to the four stages of operation.

For the phase-shifted control period, the stage trajectory lies on the $i_L \cdot Z_n$ axis, from a negative value to a positive one, which is larger than $I_M \cdot Z_n$. For the resonant period 1, the state trajectory is represented by a portion of the circle with its center located at ($I_M \cdot Z_n$, V_{S1}), and radius equal to V_{R1}. The trajectory equation for this stage is given by the circle equation

$$(i_L \cdot Z_n - I_M \cdot Z_n)^2 + (v_C - V_{S1})^2 = V_{R1}{}^2. \tag{5.18}$$

For the resonant period 2, the state trajectory is also represented by a portion of the circle. But its center is located at ($I_M \cdot Z_n$, V_{S2}), and its radius is equals to V_{R2}. The trajectory equation for this stage is given by the circle equation

$$(i_L \cdot Z_n - I_M \cdot Z_n)^2 + (v_C - V_{S2})^2 = V_{R2}{}^2. \tag{5.19}$$

For the freewheeling stage, the state trajectory lies on the $i_L \cdot Z_n$ axis, from a positive value to a negative one. The inductor current is flowing though the active-clamped capacitor Ca.

The operation at the light-load condition is a little different from that at the full-load condition. Fig. 5.7 shows some key operation waveforms, and Fig. 5.8 shows the related state-plane trajectory. First, the phase-shifted period (Stage I) is very short. The output load current is very small so that the inductor current i_L can be quickly charged up to that level. Second, at Stage II, the resonant capacitor voltage v_C resonates back to zero because of a longer resonant period so that there is no resonant operation through the clamp circuit in Stage III. Instead, if Q1 is turned off after Q2 is turned on, Stage III would be an inductor-charging period, which is similar to that in Stage I. But this period can be designed to be very narrow.

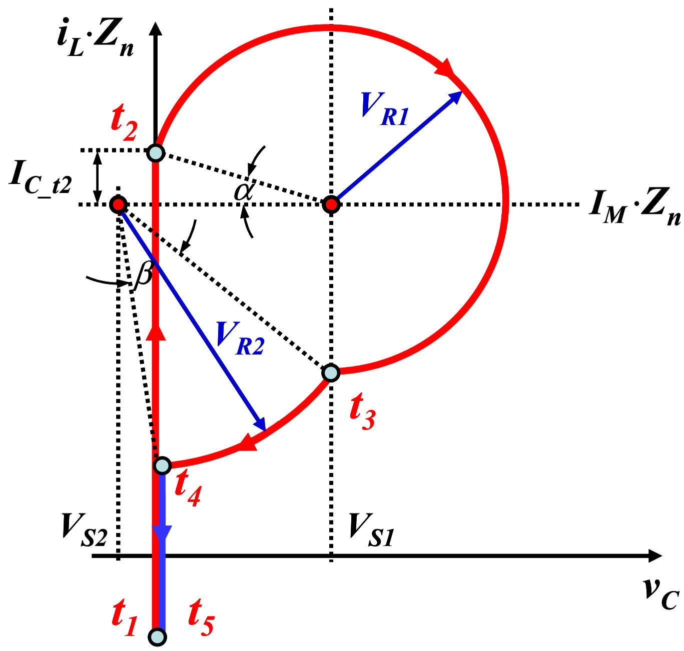


Fig. 5.6. The state-plane trajectory at full load.

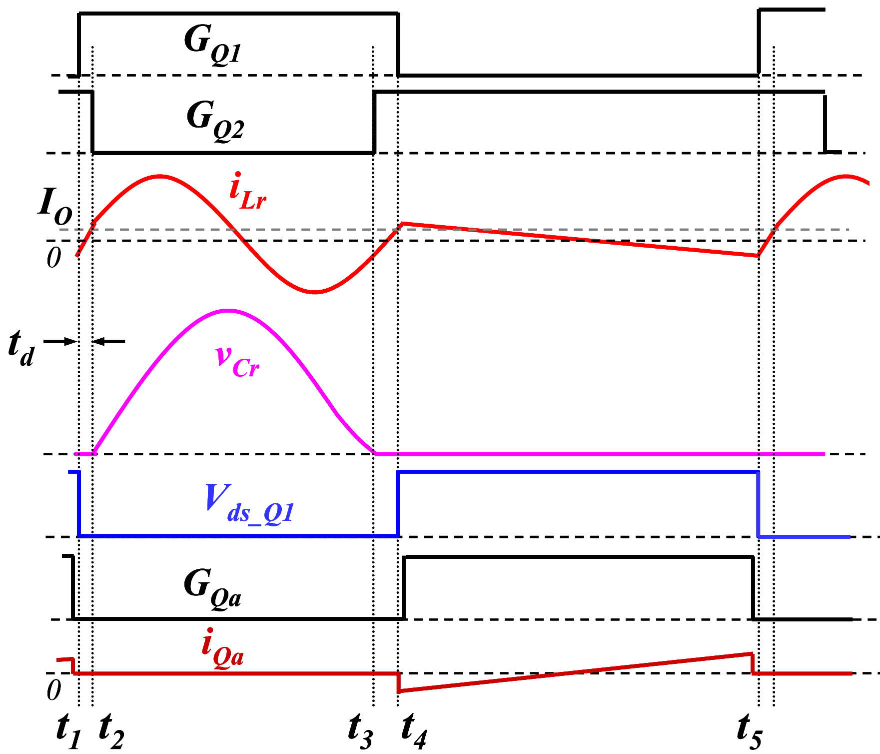


Fig. 5.7. The key operational waveforms at light load.

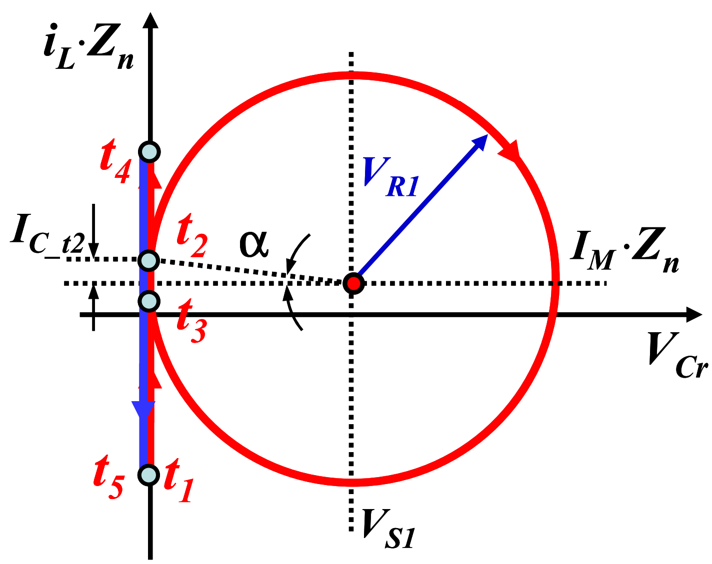


Fig. 5.8. The state-plane trajectory at light load.

5.1.4. Limitations of the Quasi-Resonant Active-Clamped Buck Converter

Section 5.1.3 analyzes the operation principle for the quasi-resonant active-clamped buck converter, which features ZVS, small switching current, small circulation current in the clamp circuit and non-body diode conduction. However, for 12V to sub-1V DC-DC conversion, the narrow duty cycle of the buck converter results in very high-pulse input current and high voltage stress for the bottom switch. The simulation results in Fig. 5.9 show that for a 11A output current, the input peak current reaches about 21 A, and the voltage stress of the bottom switch is as high as about 23 V. This causes higher conduction loss for the top switch, and there is not enough of a safety margin to use the 30V MOSFET for the bottom switch. Consequently, the bottom-switch conduction loss goes up with a higher-voltage-stress MOSFET.

Another potential problem is related to the control. The phase-shifted control period in Stage I is very short, which may cause problems in control stability.

A good way to solve all these problems is to extend the duty cycle. The next two chapters will discuss this.

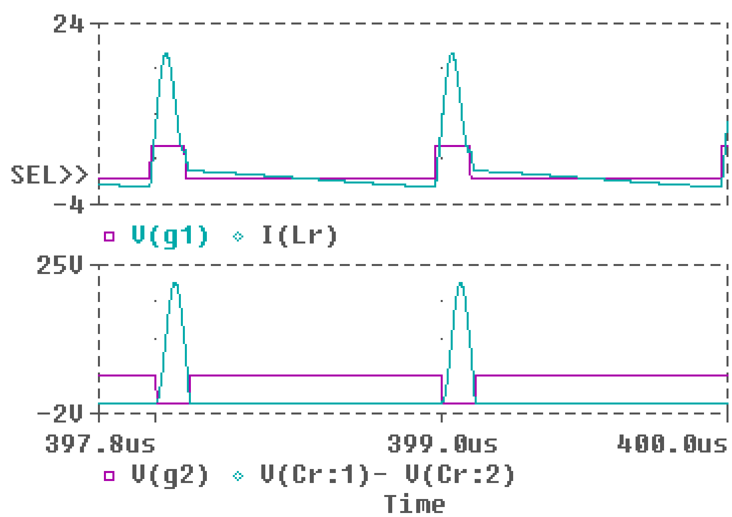


Fig. 5.9. The simulation waveforms for the quasi-resonant active-clamped buck converter.

5.2. Quasi-Resonant Active-Clamped Tapped-inductor Buck Converter

A simple way to extend the duty cycle is to use the TI buck converter. Fig. 5.10 shows a quasi-resonant active-clamped TI buck converter. Fig. 5.11 shows the equivalent circuit for this topology. It is the same circuit as shown in Fig. 5.3(b), but with different parameters. Here I_M represents the continuous magnetizing current in the TI current, which no longer equals the output load current. The following lists other parameter values that are different.

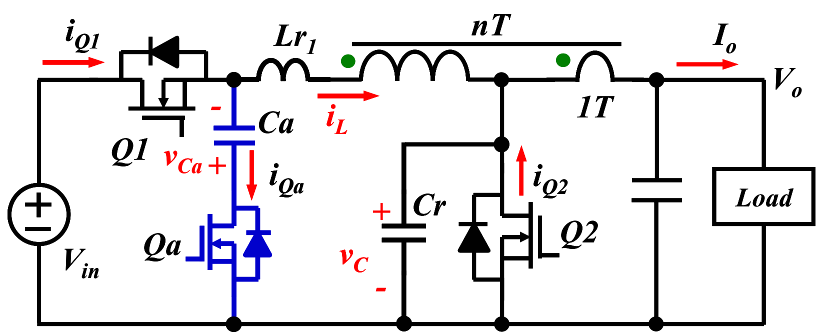


Fig. 5.10. The quasi-resonant active-clamped tapped-inductor buck converter.

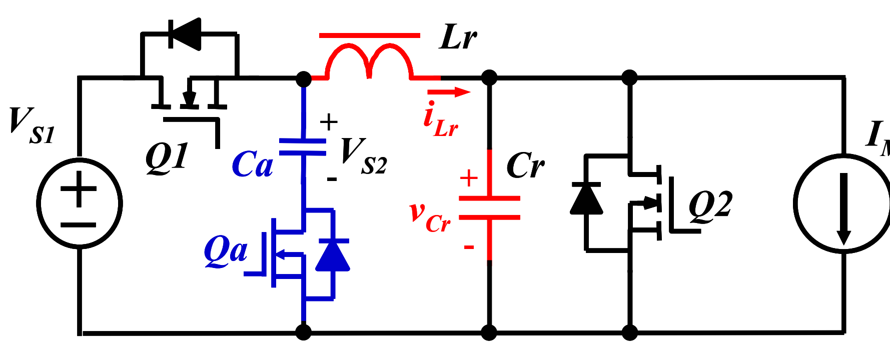


Fig. 5.11. The equivalent circuit for the quasi-resonant active-clamped tapped-inductor buck converter.

$$V_{s1} = \frac{V_{in} + (n-1) \cdot V_o}{n} \tag{5.20}$$

$$V_{s2} = \frac{-V_{Ca} + (n-1) \cdot V_o}{n} \tag{5.21}$$

$$Lr = \frac{Lr_1}{n^2} \tag{5.22}$$

5.2.1. Circuit Design Considerations

This circuit design is not easy, since it is related to the designs of the turns ratio of the TI, the fixed duty ratio of Q1, and the resonant tank. Also, we need to reduce the circulating current in the resonant tank and the switching currents of all the power devices. In this section, a simplified design process is proposed.

Fig. 5.7 and Fig. 5.8 show that Stage II can take one entire resonant period at the light-load condition. By assuming that the initial resonant current is zero, the resonant capacitor voltage can be simplified from (5.8) as follows:

$$v_c = V_{s1} \cdot [1 - \cos \omega \cdot (t - t_2)]. \tag{5.23}$$

The resonant voltage peak determines the voltage stress of device Q2, such that:

$$V_{c\_Max} = 2 \cdot V_{s1} = 2 \cdot \frac{V_{in} + (n-1) \cdot V_o}{n}. \tag{5.24}$$

The average voltage across Cr determines the output voltage. As a result, the resonant period can be derived as:

$$T_r = \frac{V_o}{V_{s1}} \cdot \frac{1}{f_s}. \tag{5.25}$$

At light load, the turn-on period of Q1 should be a little larger than the resonant period. But since Stages I and III are very short, the fixed duty cycle of Q1 can be designed according to (5.26) by adding some margin, as follows:

$$D_{Q1} = \frac{V_o}{V_{s1}} + D_M \, , \tag{5.26}$$

where D_M represents the design margin.

Equation (5.24) clearly shows that the turns ratio selection significantly impacts the device selection for Q2. Since Q2 conducts large current and switches in ZVS condition, lower voltage stress allows the use of a MOSFET with lower R_{ds_on}.

However, the turns ratio cannot be too large. The high-frequency resonant current can cause great winding AC conduction loss. Also, the turns ratio impacts the Q1 duty cycle, the clamp voltage and the voltage stress of Q1 and Qa. So, there is a trade-off for designing the turns ratio of the TI.

The resonant inductor design also requires a trade-off. Equation (5.17) shows that a large inductance value can help to reduce the switching currents of Q1 and Qa. Also, it can help to reduce the circulating current through the active-clamped circuit and Q2. However, too large an inductance limits the circuit power delivering capability. At full-load condition, in Stage I, which is about a quarter of the resonant period, the inductor current must be charged up higher than the magnetizing current. Consequently, the inductance value needs to be small. According to the maximum power delivering requirement, the inductance should be:

$$Lr_1 \le \frac{V_{in} + (n-1) \cdot V_o}{i_M + i_{s\_Qa}} \cdot n \cdot (\frac{D_{Q1}}{f_s} - \frac{3}{4} \cdot T_r) \, . \tag{5.27}$$

The turns ratio also impacts the resonant inductor design. As long as the inductance value is selected, the resonant capacitor can be designed according to (5.8), (5.25) and (5.27).

$$C_r = \frac{n^2 \cdot {T_n}^2}{Lr_1} \tag{5.28}$$

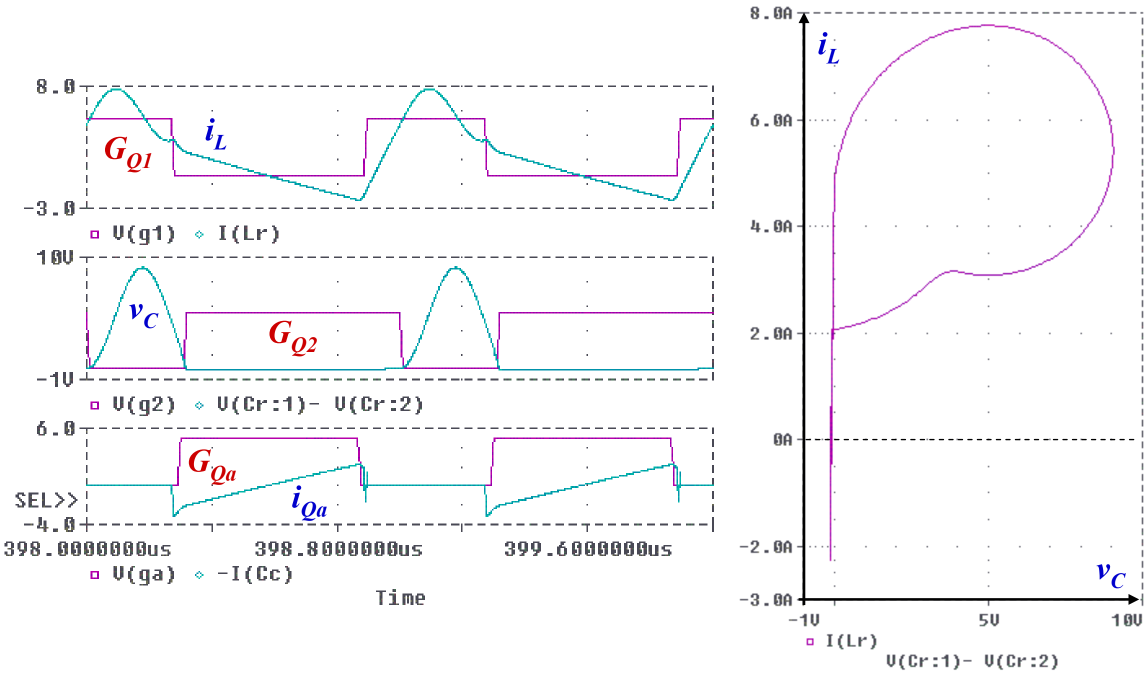
5.2.2. Simulation and Experimental Results

A 12V-input VRM prototype is developed with the quasi-resonant active-clamped TI buck converter for 1.3V/12.5A output. To make a comparison, a synchronous TI buck converter is also developed. Both circuits operate at 1MHz switching frequency. The TI is designed with a turns ratio of 3 so that high-performance 30V trench MOSFETs can be used for all the power MOSFETs. A TDK EIR-14 planar core is used to build the coupled inductor. PCB winding is used to reduce the AC winding resistance. A toroid core can also be used to reduce the cost, because this circuit is not sensitive to the leakage inductance.

Based on design considerations given in Session 5.4, the resonant tank is designed with a 260nH inductor and a 100nF capacitor. Ferrite magnetic material is used for the resonant inductor because of the high-frequency resonant current. The ceramic capacitor with NPO material is selected for the resonant capacitor for its accurate capacitance value in a wide temperature range.

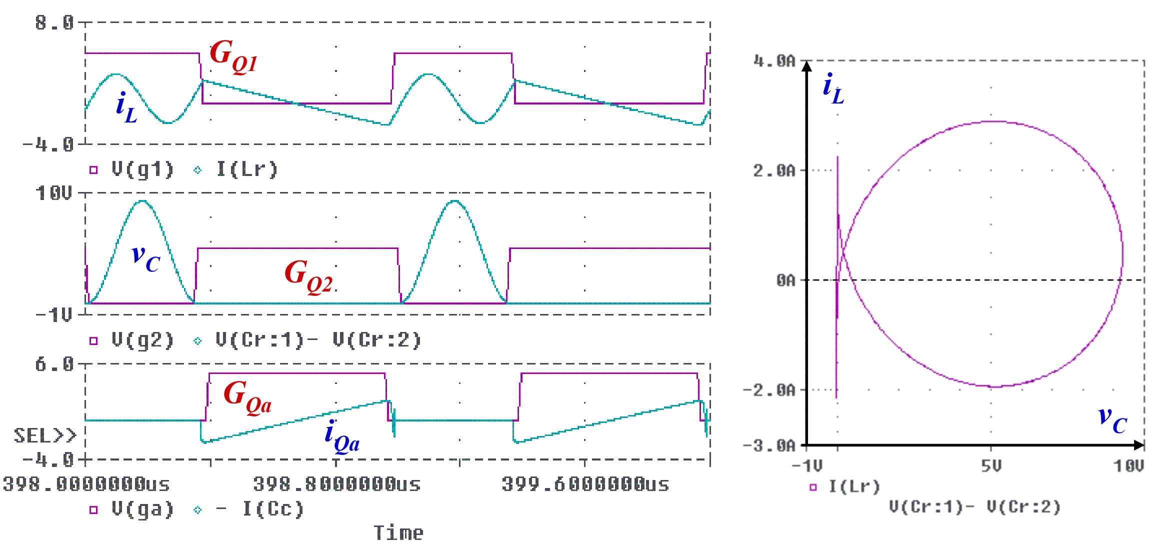
For the power stage, Hitachi's 30V trench MOSFETs with SO-8 lead-free packaging are used for their small parasitics and excellent thermal performance. HAT2096H is used for Q1 in order to reduce conduction loss without sacrificing the switching speed. HAT2099H is used for Q2 because of its very low conduction loss. HAT2116H is used for Qa because of its fast switching speed. The duty cycle of Q1 is designed to be about 0.36. A bootstrap gate driver, ADP3417, is used to drive Q1 and Qa simultaneously. A phase-shifted controller is used to control the turn-off time of Q2 in relation to the turn-on time of Q1. A comparator is used to sense the resonant capacitor voltage in order to determine the turn-on time of Q2.

Fig. 5.12 and Fig. 5.13 show the simulation waveforms and the related state-plane trajectories at full-load and light-load conditions. Fig. 5.14 shows the ZVS operation for all switches at full-load condition. The simulation results agree fairly well with the preceding theoretical analysis.



(a) **(b)**

Fig. 5.12. Simulation results at full-load condition: (a) operating waveforms and (b) state trajectory.



(a) **(b)**

Fig. 5.13. Simulation results at light-load condition: (a) operating waveforms and (b) state trajectory.

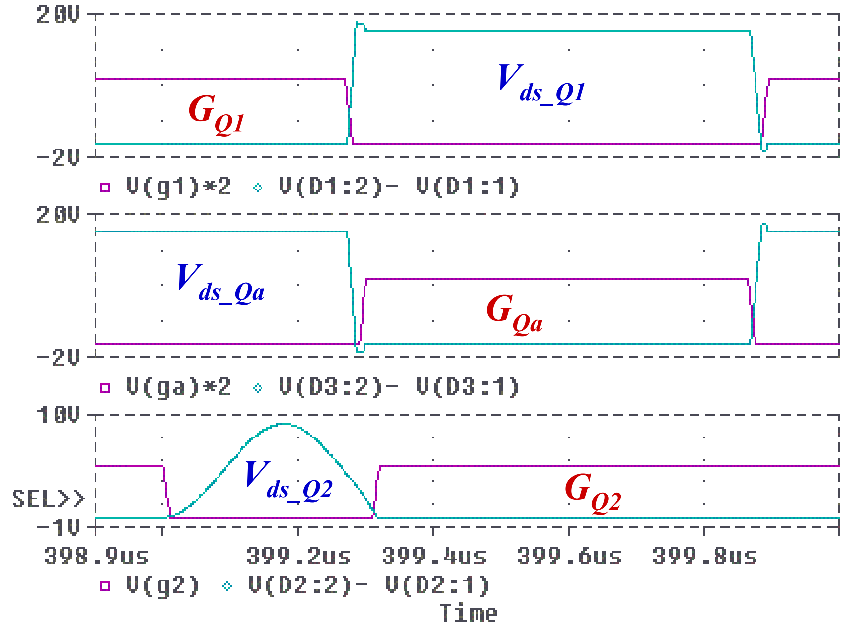
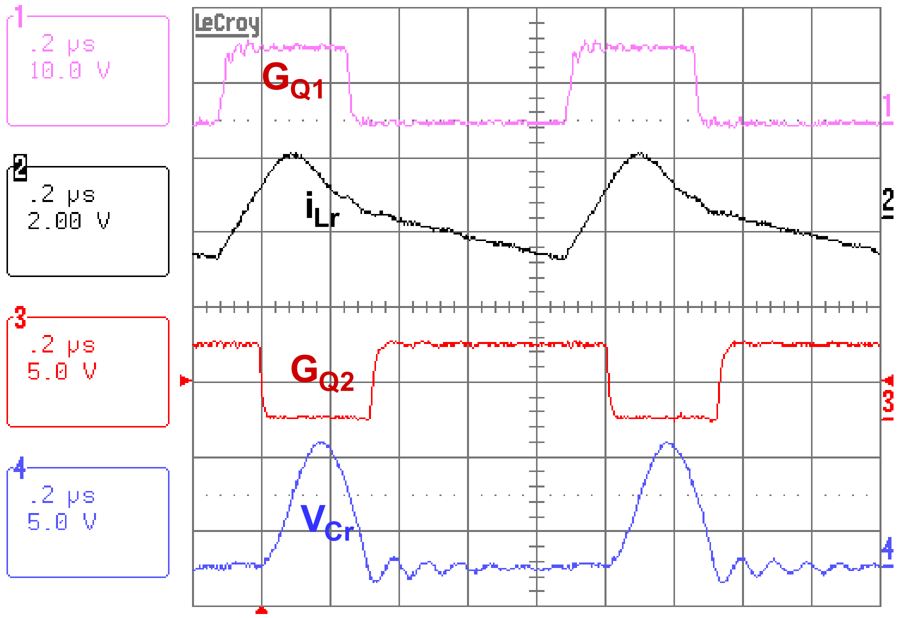
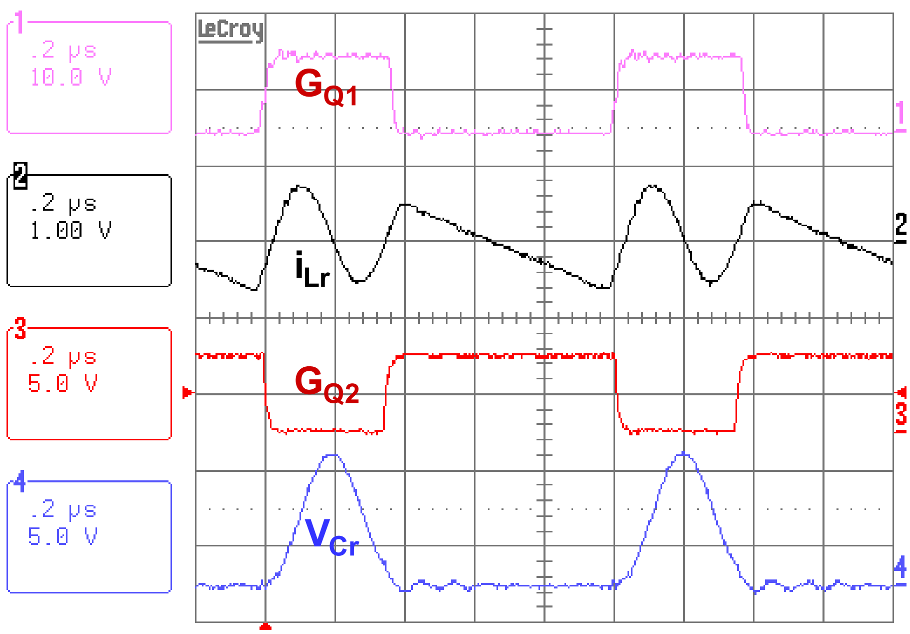


Fig. 5.14. Simulation results of ZVS operation for all switches at full-load condition.

Fig. 5.15 shows the experimental waveforms at full-load and light-load conditions. A small current transformer is used to measure the resonant inductor current. The 1V voltage level represents 3A current. Fig. 5.16 shows the measured state-plane trajectories. The circulating current through the active-clamped circuit is linearly deceased from about 1.5A to –1.5A, which causes only slightly more conduction loss. Furthermore, a 1.5nF capacitor is used to parallel with Q_1 and Q_a as a turn-off snubber. Fig. 5.17 shows that this circuit can achieve ZVS in the entire load operation range.

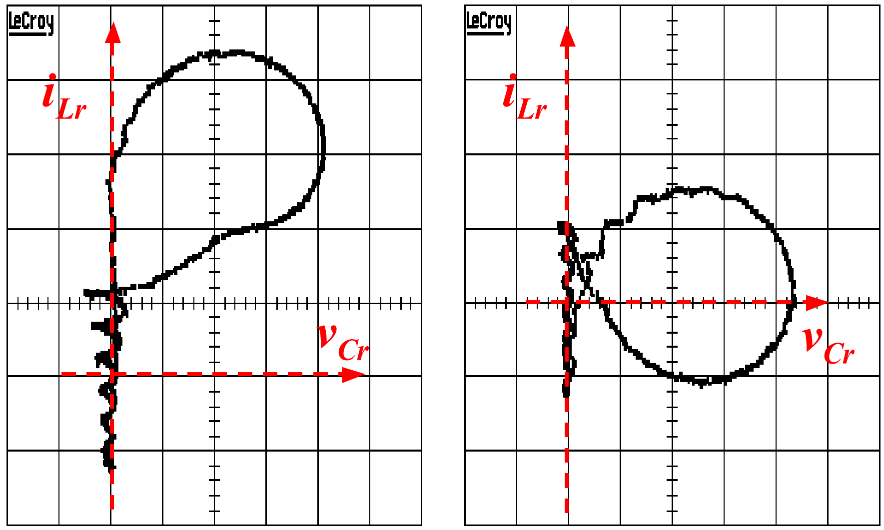


(a)



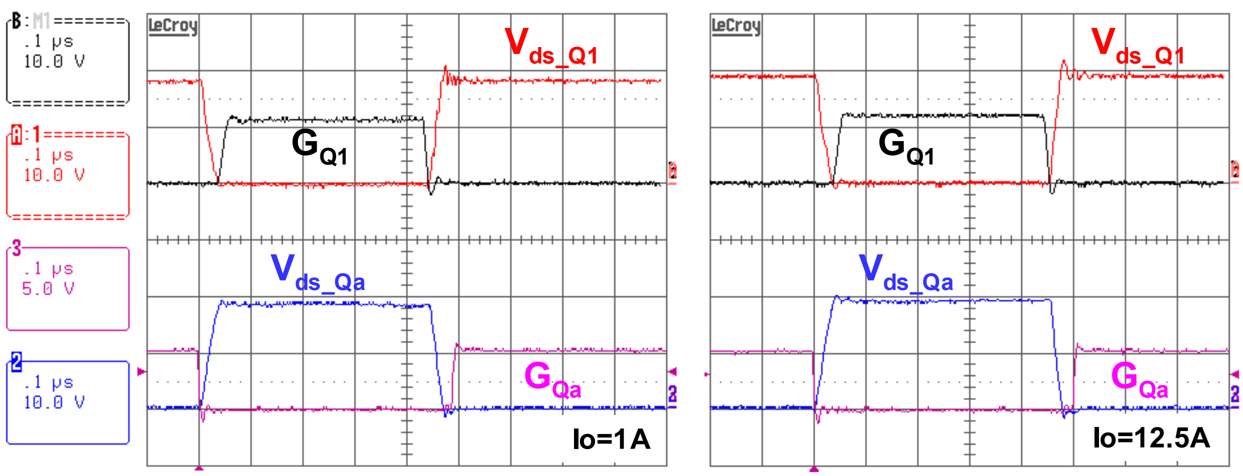
(b)

Fig. 5.15. The operation waveforms: (a) at I_o=12.5A and (b) at I_o=1A.



(a) (b)

Fig. 5.16. The state-plane trajectories: (a) at Io=12.5A and (b) at Io=1A.



(a) (b)

Fig. 5.17. The ZVS operation for Q1 and Qa: (a) at Io=12.5A and (b) at Io=1A.

Fig. 5.18 shows efficiency improvement compared with the buck and TI buck converters. At full load, the efficiency is improved by 3.8% over the TI buck converter and by 7.6% over the buck converter because of the ZVS and lack of body diode conduction loss. The relatively lower efficiency at light load is due to the resonant inductor current and the circulating current in the active-clamped circuit. But there is no thermal problem because the total loss is smaller than that in the full-load condition.

Fig. 5.19 shows the loss breakdown. It is very clear that the proposed topology almost eliminates all the switching loss and the body diode-related loss. Fig. 5.20 shows the developed prototype. The power density is about 54 W/in^3.

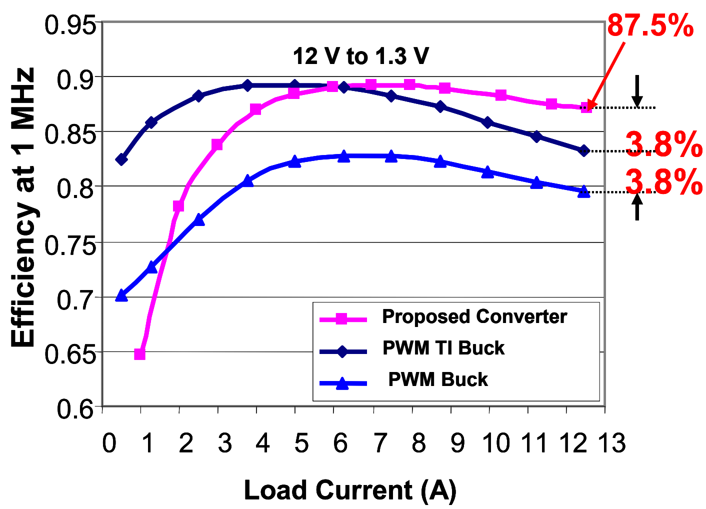


Fig. 5.18. The efficiency improvement.

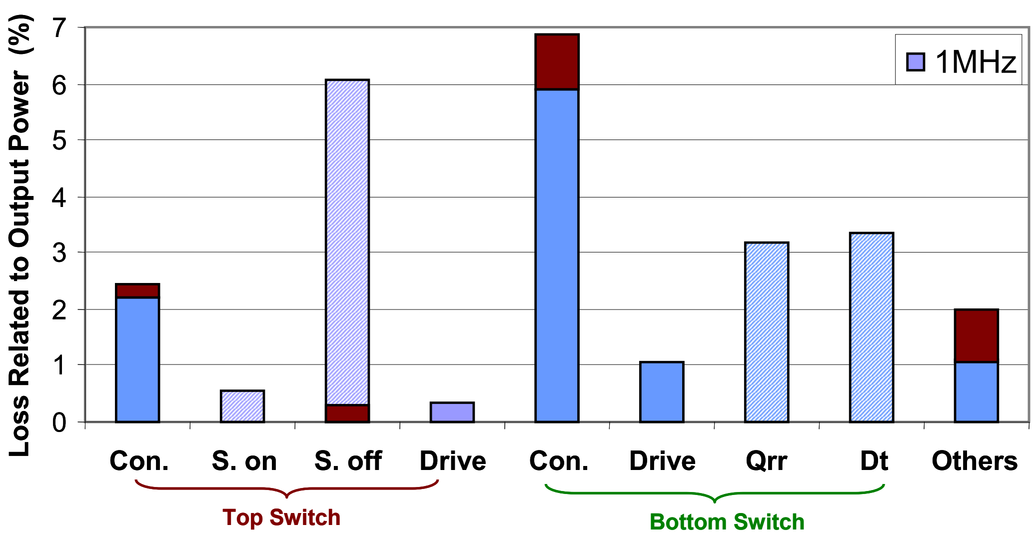


Fig. 5.19. The loss analysis of the quasi-resonant active-clamped tapped-inductor buck converter.

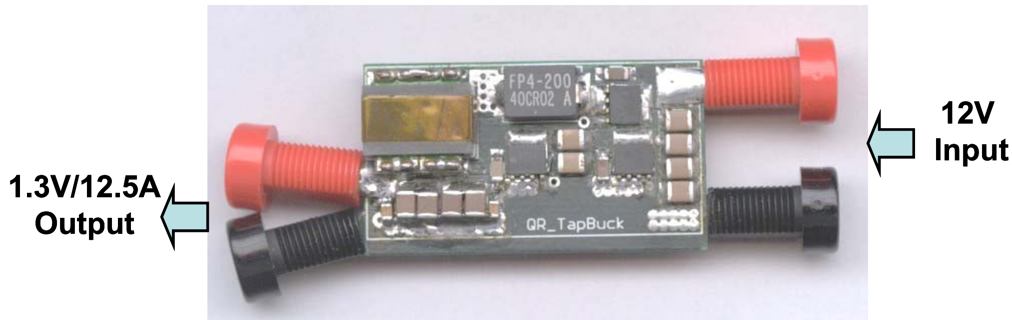


Fig. 5.20. The developed prototype with the quasi-resonant active-clamped tapped inductor buck converter.

5.3. Concept Extension

For high-frequency VRM design, which adopts the synchronous buck converter, both the top-switch switching loss and the bottom-switching body diode loss (conduction loss and reverse-recovery loss) are bottlenecks for high-efficiency and high power density design. The quasi-resonant operation can solve the problems related to the bottom switch, and an active-clamped circuit can eliminate the issues for the top switch. Furthermore, the combination of the resonant tank and the active circuit offers a possible design for reducing the switching current while reducing the freewheeling current in the clamp circuit. This idea can be extended to any quasi-resonant ZCS topology with only two modifications.

First, the LC resonant tank design is modified so that the inductor current does not resonate back to a negative value. In stead, the switch, which is in series with the resonant inductor, is turned off with a small positive current. Second, an active-clamped circuit is added to achieve ZVS operation.

Fig. 5.21 shows a family of isolated DC-DC converters achieved by applying this concept. Because of its simple structure, the quasi-resonant active-clamped flyback converter is selected to develop a 48V-to-1.2V/25A 1/16 brick DC-DC converter. At 1.8MHz operating frequency, this converter can still achieve 78% efficiency at the full load. Fig. 5.22 shows the experimental waveforms under full-load condition. Fig. 5.23 shows the measured efficiency.

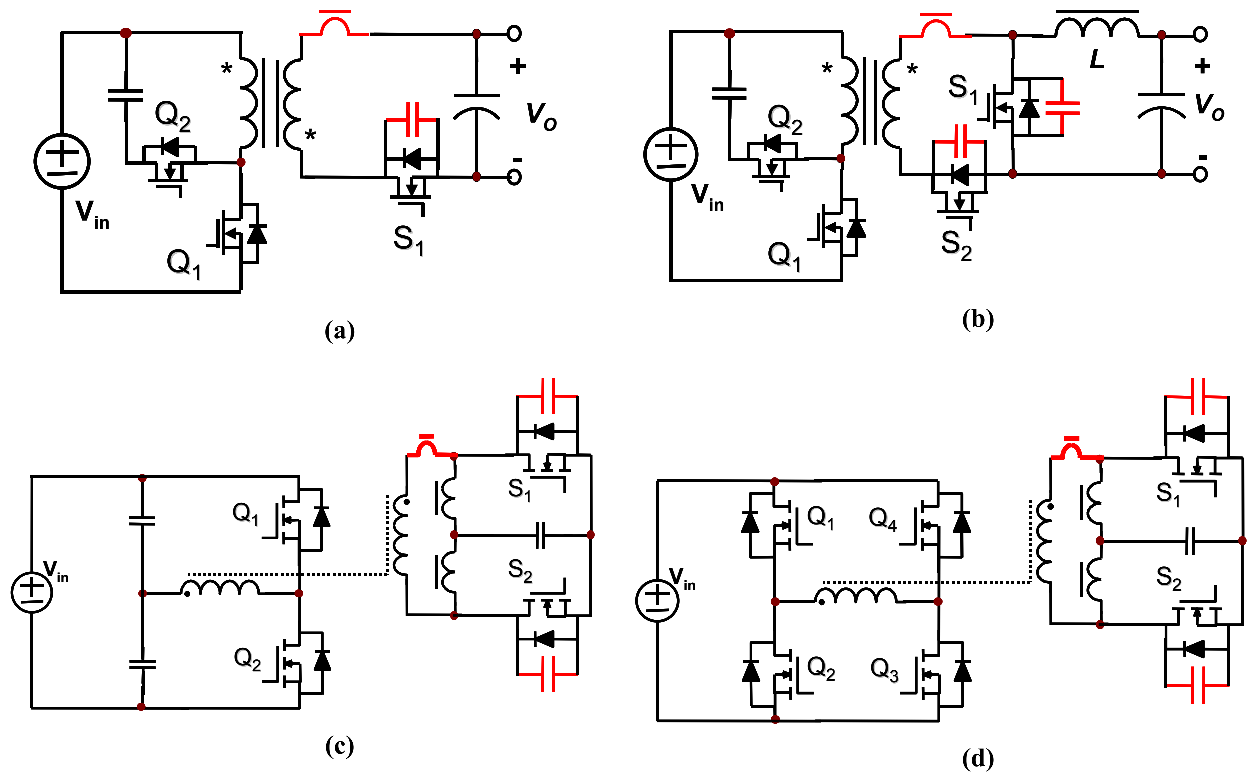


Fig. 5.21. A family of isolated quasi-resonant synchronous rectifier DC/DC converters: (a) flyback, (b) forward, (c) half-bridge, and (c) full-bridge converters.

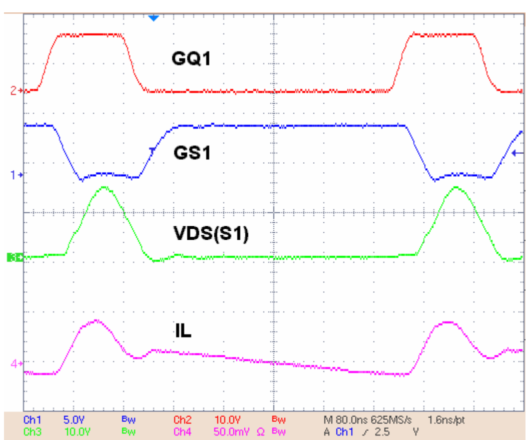


Fig. 5.22. Test waveforms of the quasi-resonant active-clamped flyback converter.

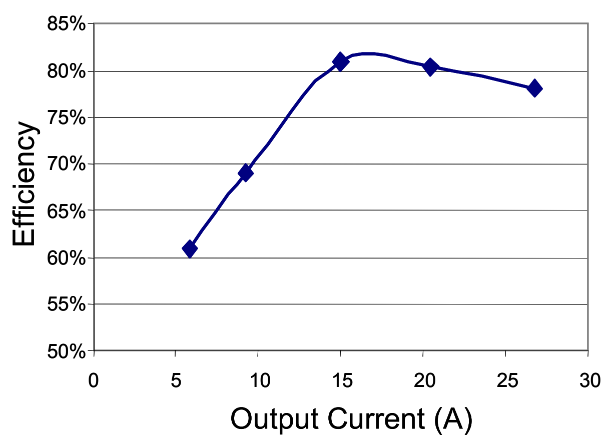


Fig. 5.23. Efficiency of the quasi-resonant active-clamped flyback converter.

Chapter 6. Summary and Future Work

It is perceived that Moore's Law will prevail at least for the next decade, with continuous advancements of processing technologies for very-large-scale integrated (VLSI) circuits. Nano technology is driving VLSI circuits in a path of greater transistor integration, faster clock frequency, and lower operation voltage. This has imposed a new challenge for delivering high-quality power to modern processors. Power management technology is critical for transferring the required high current in a highly efficient way, and to accurately regulate the sub-1V voltage in very fast dynamic transient response conditions. Furthermore, the VRM must be very small and must have the processor located right on its side in order to reduce the power delivery path.

The multiphase buck converter has become the standard industrial practice for VRM design. However, the high-frequency loss limits its further applications in power management.

It is the purpose of this work to develop high-frequency, high-efficiency, high-power-density, fast-transient VRMs to power present and future generations of processors. This dissertation has addressed the following issues.

- Fundamental understanding of the VRM transient response
- Design guidelines for the VRM transient response
- Advanced topologies for high-frequency VRM design
- Magnetic integration for certain circuit designs

6.1. Summary

6.1.1. Critical Bandwidth

For the first time, this dissertation investigates the relationship between the control bandwidth and the VRM transient voltage spike. Below the critical bandwidth, the control bandwidth determines the transient voltage spike. Beyond the critical bandwidth, the ESR of the output capacitor limits the transient voltage spike. For different kinds of capacitors, the critical bandwidths are different. Electrolytic capacitors are the major limitation of current VRM size because of their large capacitor ESR values. High frequency is the trend to improve the transient response and to reduce the VRM size by using better capacitors with smaller ESR values, such as ceramic capacitors.

The critical control bandwidth value is helpful for the design of the output filter inductor, output filter capacitor, and the control bandwidth.

6.1.2. Adaptive Voltage Position Design

This dissertation discusses the constant output impedance design method utilized to achieve perfect AVP for the VRM transient response. All the existing control methods are discussed in terms of finding the best way to design the compensator in order to achieve a constant output impedance. The limitation of voltage-mode control is discussed. Both current-mode and active-droop control methods are dual-loop feedback control systems. With a critical bandwidth design, the output capacitor ESR value turns out to be the system closed-loop output impedance. Simulation and experimental results demonstrate perfect transient response with AVP characteristics. For the capacitor, such as the ceramic capacitor, or which it is difficult to design the control bandwidth at the critical value, a constant output impedance within the control bandwidth can still be realized. The impedance beyond the control bandwidth is smaller. Simulation and experimental results show that perfect AVP can still be realized. At this time, the control bandwidth and the output capacitance determine the VRM transient response.

6.1.3. High-Frequency Topologies

Today's multiphase VRMs are almost universally based on the buck topology. This dissertation discussed its fundamental limitation for high-frequency, high-efficiency, and high-density VRM design. The multiphase buck converter suffers from a very small duty cycle for high-step-down DC-DC conversion. Loss analysis indicates that the efficiency drop is mainly caused by the switching loss of the top switches and the body diode loss of the bottom switches when the duty cycle is very small.

This dissertation introduces several new topologies to solve these problems by applying either inductor-coupling or an autotransformer structure to extend the duty cycle. Consequently, the switching loss and body diode loss are significantly reduced. The conventional TI buck converter is modified with a simple gate drive scheme. The leakage inductance problem in the coupled inductor is solved with a lossless passive-clamped circuit. By introducing two more sets of coupled windings in the two-phase interleaved TI buck converter, another new topology evolves. It offers continuous output current and maintains the benefits of simple gate drive and simple clamp circuit. The autotransformer structure extends the concept and generalizes a family of non-isolated buck-type DC-DC converters. Magnetic integration is also discussed in the new topology implementation in order to further reduce the size and to improve the performance. Simulation and experimental results for these new topologies demonstrate significant improvement in efficiency and power density for VRM design. The operating switching frequency is pushed to 2 MHz. These topologies are very good candidates for the power management of the next generation of processors.

This dissertation pushes the topology innovation further by introducing the soft-switching quasi-resonant converters for VRM design. The combination of the quasi-resonant and active-clamped concepts derives a family of new converters, which can eliminate all the switching and body diode losses. Experimental results show further efficiency improvement at a switching frequency of 1 MHz.

6.2. Future Work

This dissertation has tried to break through some technology barriers for future power management. It has explored some good ideas and solutions, but further research work is necessary.

6.2.1. Control Issues at Very High Switching Frequencies

In this dissertation, the transient analysis and AVP design are based on an ideal operating condition. It is assumed that the operation amplifier has an infinite gain and that there is no phase delay. Also, the control signal propagation delay and the gate drive delay are not considered. But in the practical design, the operation amplifier has its bandwidth limitation, and all the delays can account for tens of nanoseconds. When the system control bandwidth is far below the operation amplifier bandwidth and the delay is much smaller than a switching period, the theoretical analysis in an ideal situation is good enough to guide the practical design. However, for applications with very high switching frequencies, which is the trend of the VRM design, the entire system can no longer be simplified as an ideal one.

As a result, it is critical to accurately model the entire VRM system so that we can predict the transient performance for a VRM operating at multi-MHz switching frequencies. New issues and challenges will emerge. The design for the feedback controller may be totally different. This is a very interesting research direction.

6.2.2. Self-Driven for Advanced Non-Isolated Topologies with Autotransformers

This dissertation has generalized a family of new buck-type topologies based on the autotransformer structure. The autotransformer can not only simplify the topologies, but can also reduce the winding and synchronous rectifier conduction losses. Since it still features a transformer function, all the self-driven schemes in the isolated topologies can be transplanted. The self-driven structure can not only simplify the gate drive circuit, but also can reduce the gate drive loss. As a result, non-isolated topologies based on autotransformers can further improve the VRM performance at high frequencies. Some preliminary research in this direction has already been started at CPES [D60].

6.2.3. Dynamic Analysis for the Quasi-Resonant Active-Clamped Topologies

This dissertation has introduced the concept of combining quasi-resonant topologies and an active-clamped circuit in order to eliminate all the switching loss and body diode loss. It has demonstrated the significant efficiency improvement. However, the dynamic characteristics of these topologies remain unclear. As a result, further work should be done in modeling, small-signal analysis, transient analysis, and AVP implementation.

6.2.4. System Integration

The motivation of high-frequency, high-efficiency, and high-power-density VRM design is to meet the power requirements of future processors. The final goal is the ability to integrate the processor and its VRM together so that the parasitics in the power delivery path are minimized. This will significantly change the power delivery architecture.

To realize this vision, we must address a number of important technology fronts, including advanced power semiconductor devices, advanced circuit and control concepts, and advanced material and packaging technologies.

For the advanced power semiconductor devices, the challenges are high efficiency and packaging density. The conventional vertical trench MOSFET can not be operated at 5-10MHz switching frequencies due to its excessive switching losses. Also, it is difficult to realize the monolithic integration of power devices, driver, and controller using a vertical structure. Without integration, the parasitics associated with interconnects will seriously hamper its ability to operate at multi-MHz frequencies. Other low-voltage power devices and power IC technologies using lateral trench or lateral processes are deemed more suitable. CPES has already demonstrated the 4MHz monolithic integration of a complete buck converter based on a lateral MOSFET process [D61]. This chip includes all the control and driving functions. The submicron lateral CMOS technology offers a more than tenfold improvement in figure-of-merit as compared to the vertical devices. More than 80% conversion efficiency was demonstrated with 2A output. How to extend this approach to higher output current is a very interesting research topic.

For the advanced circuit and control concept, the power linear regulator is a possible solution for meeting the fast transient response requirement of future processors. The challenges are higher bandwidth, higher current capability, and improved thermal management. A number of important research results have been reported recently, including those from the University of Florida, UC-Berkeley and Primarion; all adopted the radio frequency (RF) linear amplifier techniques to realize high bandwidth designs for VRMs [A68, A71, A76]. Si, SiGe and GaAs have been reported as candidate RF semiconductor devices. GaAs is widely used in the RF area, but the processing power is relatively small. Also, the high processing cost limits its future application. SiGe BICMOS seems to be the obvious choice for its fast speed and relatively low cost. The lower-cost Si CMOS process is also possible for lower-cost solutions in the future.

The advanced material and packaging technologies are keys to reducing the passive component size so that system integration becomes possible. Research on a high-frequency magnetic thin-film inductor for the MHz switching frequency has been reported [D62, D63]. However, the applied current rating is still very small. CPES has demonstrated several planar integrated LC and LCT modules for 1KW converter applications [D64-D66]. But the applied frequency is limited to less than 1 MHz. For 5 to 10 multi-MHz frequency operation, an effective means of integrating passive components, such as inductors, capacitors and transformers, could be an interesting research area.

The ultimate challenge is the system-level integration, in which the integration of electrical properties must be accompanied by thermal management and integration of a mechanical structure for system integrity. Also, it must be compatible with the packaging practice of the future processors.

References: Part A

[1] G. Moore, “Cramming more components onto integrated circuits,” in Electronics, Volume 38, Number 8, April 19, 1965.

[2] P.P. Gelsinger, P. Gargini, G. Parker and A. Yu, “Microprocessor circa 2000,” in IEEE Spectrum, Oct. 1989, pp. 43-47.

[3] J. A. Maiz, “From micro to nanotechnology: A perspective from the semiconductor world,” presentation to CMIC, June 14, 2002. Available at http://www.intel.com/research/silicon/CMIC_2002_Jose_Maiz.pdf.

[4] G. Moore, “No exponential is forever … but we can delay ‘Forever,’” Presentation at International Solid State Circuits Conference (ISSCC), Feb. 10, 2003. Available at ftp://download.intel.com/research/silicon/Gordon_Moore_ISSCC_021003.pdf.

[5] “Extending and expanding Moore’s Law,” in Intel Developer Updated Magazine, April 2002, pp. 1-4. Also available at http://www.intel.com/update/departments/special/ss04021.pdf.

[6] G. Marcyk, “Breaking barriers to Moore’s Law,” Presentation at Intel Developer Forum, Spring 2002. Available at ftp://download.intel.com/research/silicon/MarcykIDF022802.pdf.

[7] A. Grove, “Changing vectors of Moore’s Law,” presentation on International Electron Devices Meeting. Available at ftp://download.intel.com/research/silicon/Grove_IEDM_1202.pdf.

[8] P.P. Gelsinger, “Microprocessors for the new millennium: Challenges, opportunities, and new frontiers,” in Proc. IEEE ISSCC, 2001, pp. 22-25.

[9] “Designing for power: Increasing performance while reducing power consumption,” Research & Development at Intel. Available at ftp://download.intel.com/labs/power/download/design4power1.pdf.

[10] Ed Stanford, “Power technology roadmap for microprocessor voltage regulators,” Presentation at PSMA, Feb. 2003.

[11] “2001 technology roadmap for semiconductors,” http://www.intel.com/research/silicon/AlanAllanIEEEComputer0102.pdf.

[12] Ed Stanford, “Intel technology VR road map,” Intel Power Supply Technology Symposium, Sept. 2001.

[13] M. Zhang, M. Jovanovic and F. C. Lee, “Design considerations for low-voltage on-board DC/DC modules for next generations of data processing circuits,” in IEEE Trans. Power Electron., Vol. 11, March 1996, pp. 328-337.

[14] P. Wong, F.C Lee, X. Zhou and J. Chen, “Voltage regulator module (VRM) transient modeling and analysis,” in Proc. IEEE IAS, 1999, pp. 1669-1676.

[15] X. Zhou, X. Zhang, J. Liu, P. Wong, J. Chen, H. Wu, L. Amoroso, F. C. Lee and D. Y. Chen, "Investigation of candidate VRM topology for future microprocessors," in Proc. IEEE APEC, 1998, pp. 145-150.

[16] Intel document, “VRM 9.0 DC-DC converter design guidelines,” Order number: 249205-004, April 2002. Available at http://www.intel.com/design/pentium4/guides/24920504.pdf.

[17] Intel document, “Intel Pentium 4 Processor VR-Down design guidelines,” Order number: 249891-002, Jan. 2002.

[18] Intel document, “Intel Pentium 4 processor /Intel 850 chipset platform design guide,” Order number: 248245-003, Aug. 2001.

[19] G. Prophet, “Multiphase DC/DC designs handle 200A,” EDN, Nov. 11, 1999.

[20] A. Gentchev, "Designing high-current, VRM-compliant CPU power supplies," EDN, Oct. 26, 2000, pp. 155-158.

[21] A. Bindra, “Power-supply ICs go multiphase to take on 100-A loads,” in Electronic Design, March 4, 2002, pp. 42-46. Also available at http://www.elecdesign.com/2002/mar0402/030402coverstory.pdf.

[22] "Multiphase controller meets Pentium's power demands," EDN, Aug. 3, 1998, p. 28.

[23] P. Xu, X. Zhou, P. L. Wong, K. Yao and F. C. Lee, "Design and performance evaluation of multi-channel interleaved quasi-square-wave buck voltage regulator module," in Proc. HFPC, 2000, pp. 82-88.

[24] G. Schuellein, “Multiphase buck converter design responds well to transients,” Planet Analog, Sept. 13, 2000. Available at http://www.planetanalog.com/story/OEG20000913S0006.

[25] G. Capponi, L. Minneci, F. Librizzi and P. Scalia, “Multiphase voltage regulator module with transient step changing phases,” in Proc. IEEE PowerCon, 2000, pp. 463-467.

[26] P. Xu, X. Zhou, P. Wong, K. Yao and F. C. Lee, "Interleaved VRM cuts ripple, improves transient response," PCIM Power Electronic Systems, Feb. 1, 2001, pp. 70-78.

[27] V. Biancomano, “ICs, modules keep pace with VRMs,” EE times, Sept. 21, 2001. Available at http://www.planetanalog.com/story/OEG20010921S0032.

[28] Vincent Biancomano, “DC/DCs find power in multichip modules,” EE Times, Jan. 30, 2001. Available at http://www.eetimes.com/story/OEG20010130S0046.

[29] B. Pohlman, “Overcoming the Barriers to 10GHz Processors,” Presentation at Microprocessor Forum Keynote, Oct. 16, 2001.

[30] K. Yao, Y. Meng and F.C. Lee, “Control bandwidth and transient response of buck converters,” in Proc. IEEE PESC, 2002, pp. 137-142.

[31] Intel Document, “Intel® Pentium® 4 Processor / Intel® 850 Chipset Platform Design Guide,” Order Number: 298245 -003.

[32] R. Mahajan, R. Nair, V. Wakharkar, J. Swan, J. Tang and G. Vandentop, “Emerging directions for packaging technologies,” in Intel Technology Journal, Vol. 6, Issue 2, May 16, 2002, pp. 62-74.

[33] S.N. Towle, H. Braunisch, C. Hu, R.D. Emery and G.J. Vandentop, “Bumpless build-up layer packaging,” in Proc. ASME Int. Mech. Eng. Congress and Exposition (IMECE), 2001. Also available at ftp://download.intel.com/research/silicon/BBULASME1101paper.pdf.

[34] H. Braunisch, S.N. Towle, R.D. Emery, C. Hu and G.J.Vandentop, “Electrical performance of bumpless build-up layer packaging,” in Proc. IEEE Electronic Components and Technology Conference, 2002, pp. 353-358. Also available at ftp://download.intel.com/research/silicon/ECTC2002Braunischpaper.pdf.

[35] M. Zhang, M. Jovanovic and F. C. Lee, “Design considerations for low-voltage on-board DC/DC modules for next generations of data processing circuits,” IEEE Trans. on Power Electronics, Vol. 11, No. 2, March 1996, pp. 328-337.

[36] J. Xu, X. Cao and Q. Luo, “The effects of control techniques on the transient response of switching DC-DC converters,” in Proc. IEEE PEDS, 1999, pp. 794-796.

[37] P. Wong, F.C. Lee, X. Zhou and J. Chen, “VRM transient study and output filter design for future processors,” in Proc. IEEE IECON, 1998, pp. 410-415.

[38] P. Wong, F.C. Lee, X. Zhou and J. Chen, “Voltage regulator module (VRM) transient modeling and analysis,” in Proc. IEEE IAS, 1999, pp. 1669-1676.

[39] P. Wong, F.C. Lee, P. Xu and K. Yao, “Critical inductance in voltage regulator modules,” in Proc. IEEE APEC, 2002, pp. 203-209. Also in IEEE Trans. Power Electron., Vol. 17, July 2002, pp. 485-492.

[40] P. Wong, “Performance improvements of multi-channel interleaving voltage regulator modules with integrated coupling inductors,” dissertation of Virginia Polytechnic Institute and State University, March 2001.

[41] C.J. Mehas, K.D. Coonley and C.R. Sullivan, "Converter and inductor design for fast-response microprocessor power delivery," in Proc. IEEE PESC, 2000, pp. 1621-1626.

[42] R. Miftakhutdinov, “Optimal design of interleaved synchronous buck converter at high slew-rate load current transients,” in Proc. IEEE PESC, 2001, pp. 1714-1718.

[43] A. Barrado, R. Vazquez, A. Lazaro, J. Pleite and E. Olias, “Fast transient response DC/DC converter for low output voltage,” in Electronics Letters, Vol. 38, Sept. 2002, pp. 1127-1128.

[44] S.A. Chickamenahalli, S. Mahadevan, E. Stanford and K. Merley, “Effect of target impedance and control loop design on VRM stability,” in Proc. IEEE APEC, 2002, pp. 196-202.

[45] H. Yu, “JFET structure and manufacture method for low on-resistance and low voltage application,” US Patent #6251716, June 26, 2001.

[46] H. Yu, “Complementary junction field effect transistors,” US Patent #6307223, Oct. 23, 2001.

[47] B. J. Baliga, “Methods of forming power semiconductor devices having tapered trench-based insulating regions therein,” US Patent #6365462, April 2, 2002.

[48] “30V JBSFETTM N-channel power MOSFET with integral Schottky diode,” Data sheet from Silicon Semiconductor Corporation, http://silicon-wireless.com/Level2/power_mosfet.html.

[49] V. Biancomano, “Road maps on course for power MOSFETs as packaging moves to fore,” EE Times, Dec. 22, 2000. Available at http://www.eetimes.com/story/OEG20001222S0023.

[50] V. Biancomano, “ON Semiconductor, Vishay raise the bar on leadless chip packaging,” EE Times, July 30, 2001. Available at http://www.eetimes.com/story/OEG20010730S0012.

[51] V. Biancomano, “Chip-scale powers MOSFET packages,” in EE Times, Oct. 18, 2001. Available at http://www.eetimes.com/story/OEG20011018S0039.

[52] D. Morrison, “Smart power blocks build new approach to DC-DC conversion,” in PlanetEE, Feb. 19, 2001. Available at http://www.planetee.com/index.htm?14396.

[53] X. Zhang, A.Q. Huang, N.X. Sun and F.C. Lee, “Microprocessor power management integration by VRB-CPU approach,” in Proc. CPES Power Electronics Seminar, 2003, pp. 9-14.

[54] P. Xu, J. Wei, K. Yao, Y. Meng and F.C. Lee, “Investigation of candidate topologies for 12V VRM,” in Proc. IEEE APEC, 2002, pp. 686-692.

[55] M. Ye, P, Xu, B, Yang and F.C. Lee, “Investigation of topology candidates for 48V VRM,” In Proc. IEEE APEC, 2002, pp. 699-705.

[56] Y. Ren, M. Xu, K. Yao and F.C. Lee, “Two-stage 48V power pod exploration for 64-bit microprocessor,” in Proc. IEEE APEC, 2003, pp. 426-431.

[57] Y. Ren, M. Xu, D. Sterk and F. C. Lee, “1MHz self-driven ZVS full bridge converter for 48V power pods,” in Proc. CPES Power Electronics Seminar, 2003, pp. 215-221.

[58] P. Mappus, “Predictive gate drive boosts synchronous DC/DC power converter efficiency,” TI Application Report, SLUA281 - April 2003. Available at http://focus.ti.com/lit/an/slua281/slua281.pdf.

[59] Yuhui Chen, “Resonant gate drive techniques for power MOSFETs,” thesis of Virginia Polytechnic Institute and State University, May 2000.

[60] W. Huang and J. Clarkin, "Analysis and design of multi-phase synchronous buck converter with enchanted V^2 control," in Proc. HFPC, 2000, pp. 74-81.

[61] W. Huang, “A new control for multi-phase buck converter with fast transient response,” in Proc. IEEE APEC, 2001, pp. 273-279.

[62] M.M. Walters, C.E. Hawkes, R.H. Isham, “Multi-phase converter with balanced currents,” US Patent #6278263, Aug. 21, 2001.

[63] C.E. Hawkes, M.M. Walters and R.H. Isham, “Current mode DC/DC converter with controlled output impedance,” US Patent #6181120, Jan. 30, 2001.

[64] P.R. Lethellier, “Method and apparatus for accurately sensing output current in a DC-to-DC voltage converter,” US Patent #6424129, July 23, 2002.

[65] N. Rossetti, “Valley design techniques outperform peak current-mode approach for CPU supplies,” in PCIM, July 2001.

[66] W. Huang, G. Schuellein and D.Clavette, “A scalable multiphase buck converter with average current share bus,” in Proc. IEEE APEC, 2003, pp. 438-443.

[67] J. Abu-Qahouq, L. Jia and I. Batarseh, “Voltage regulator module with interleaved synchronous buck converters and novel voltage-mode hysteretic control,” in IEEE Proc. MWSCAS, 2001, pp. 972-975.

[68] K.D.T. Ngo, S. Kirachaiwanich and M. Walters, “Buck modulator with improved large-power bandwidth,” in IEEE Trans. Aerosp. Electron. Syst., Vol.38, Oct. 2002, pp. 1335-1343.

[69] K. Lee, K. Yao, X. Zhang, Y. Qiu and F.C. Lee, “A novel control method for multiphase voltage regulators,” in Proc. IEEE APEC, 2003, pp. 738-743.

[70] L. Amoroso, M. Donati, X. Zhou and F.C. Lee, “Single shot transient suppressor (SSTS) for high current high slew rate microprocessor,” in Proc. IEEE APEC, 1999, pp. 284-288.

[71] A.M. Wu and S.R. Sanders. "An active clamp circuit for voltage regulation module (VRM) applications,” IEEE Trans. Power Electron., Vol. 16, Sept. 2001, pp. 623-634.

[72] A. Prodic, D. Maksimovic and R.W. Erickson, “Design and implementation of a digital PWM controller for a high-frequency switching DC-DC power converter,” in Proc. IEEE IECON, 2001, pp. 893-898.

[73] A.V. Peterchev, J. Xiao and S.R. Sanders, “Architecture and IC implementation of a digital VRM controller,” in IEEE Trans. Power Electronics, Vol. 18, Issue 1, Jan. 2003, pp. 356-364.

[74] J.A. Abu-Qahouq, N. Pongratananukul, I. Batarseh and T. Kasparis, “Multiphase voltage-mode hysteretic controlled VRM with DSP control and novel current sharing,” in Proc. IEEE APEC, 2002, pp. 663-669.

[75] S. Bibian and H. Jin, “High performance predictive dead-beat digital controller for DC power supplies,” in IEEE Trans. Power Electronics, Vol. 17, Issue 3, May 2002, pp. 420-427.

[76] B. Pohlman and M. Eisele, “An apparatus for providing regulated power to an integrated circuit,” US Patent #6429630, Aug. 6, 2002.

[77] P. Chesley, “Voltage regulation for deep sub-micro processors goes digital,” in ECN, April 2003, pp. 41-42.

[78] A.J. Burstein, D.B. Lidsky, A. Stratakos, C. Sullivan and W. Clark, “Digital voltage regulator using current control,” US Patent #6590369, July 8, 2003.

[79] A.J. Burstein and A. Schultz, “Method and apparatus for digital voltage regulation,” US Patent #6351108, Feb. 26, 2002.

[80] C. Segura, “High current inductors for multiphased / interleaved power supply topologies,” in ECN, Dec. 2002, p. 47.

[81] P. Wong, P. Xu, B. Yang and F. C. Lee, “Performance improvements of interleaving VRMs with coupling inductors,” in IEEE Trans. Power Electron., Vol. 16, July 2001, pp. 499-507.

[82] P. Wong, F. C. Lee, X. Jia and D. van Wyk, “A novel modeling concept for multi-coupling core structures,” in Proc. IEEE APEC, 2001, pp. 102-108.

[83] J.D. Prymak, “Improvements with polymer cathodes in aluminum and tantalum capacitors,” in Proc. IEEE APEC, 2001, pp. 1210-1218.

[84] J. Wright, “An introduction to low ESR capacitors,” ECN (Electronic Component News), Feb. 2002. Available at http://www.ecnmag.com/ecnmag/issues/2002/02012002/ec22ss2.asp.

[85] C.T. Burket, “Optimization of ESR/ESL in ceramic capacitors for high transient applications,” Presentation at Intel Technology Symposium, 2002.

[86] F.C. Lee, J. D. Van Wyk, D. Boroyevich and P. Barbosa, “An integrated approach to power electronics systems,” in Proc. Power Conversion Conference, 2002, pp. 7-12.

[87] “INCEP ZVRM™ architecture: Enabling the power of silicon,” available at http://www.incep.com/solutions.htm.

[88] R. Mahajan, R. Nair, V. Wakharkar, J. Swan, J. Tang and G. Vandentop, “Emerging directions for packaging technologies,” in Intel Technology Journal, Vol. 6, Issue 2, May 16, 2002, pp. 62-74.

[89] H. Braunisch, S.N. Towle, R.D. Emery, C. Hu and G.J. Vandentop, “Electrical performance of bumpless build-up layer packaging,” in Proc. IEEE Electronic Components and Technology Conference, 2002, pp. 353-358. Also available at ftp://download.intel.com/research/silicon/ECTC2002Braunischpaper.pdf.

[90] K. Yao, Y. Meng and F.C. Lee, “Control bandwidth and transient response of buck converters,” in Proc. IEEE PESC, 2002, pp. 137-142.

[91] K. Yao, Y. Meng P. Xu and F.C. Lee, “Design considerations for VRM transient response based on the output impedance,” in Proc. IEEE APEC, 2002, pp. 14-20.

[92] K. Yao, K. Lee, M. Xu and F.C. Lee, “Optimal design of the active droop control method for the transient response,” in Proc. IEEE APEC, 2003, pp. 718-723.

[93] K. Yao, P.L. Wong and F.C. Lee, "The inductor design for the multi-channel voltage regulator module," in Proc. HFPC, 2000, Vol. 15, pp. 231-238.

[94] K. Yao, F.C. Lee, Y. Meng and J. Wei, “Tapped-inductor buck converter with a lossless clamp circuit,” in Proc. IEEE APEC, 2002, pp. 693-698.

[95] K. Yao, Y. Meng and F.C. Lee, “A novel winding coupled buck converter for high step-down DC/DC conversion,” in Proc. IEEE PESC, 2002, pp. 651-656.

[96] K. Yao, Y. Ren, J. Wei, M. Xu and F.C. Lee, “A family of buck-type DC-DC converters with autotransformers,” in Proc. IEEE APEC, 2003, pp. 114-120.

[97] K. Yao, M. Xu and F.C. Lee, “Quasi-resonant, active-clamp, tapped-buck converter for high frequency voltage regulator,” in Proc. CPES Power Electronics Seminar, 2003, pp. 249-254.

[98] K. Yao and F.C. Lee, “A novel resonant gate driver for high frequency synchronous buck converters,” in IEEE Trans. Power Electron., Vol. 17, March 2002, pp. 180-186.

References: Part B

[1] K. Harada and T. Nabeshima, “Large-signal transient response of a switching regulator,” in Proc. IEEE PESC, 1981, pp. 388-394.

[2] T. Nabeshima and K. Harada, “Large-signal transient response of a switching regulator,” in IEEE Trans. Aerosp. Electron. Syst., Vol. 18, Sept. 1982, pp. 545-551.

[3] S.B. Yaakov and D. Adar, “Average models as tools for studying the dynamics of switch mode DC-DC converters,” in Proc. IEEE PESC, 1994, pp. 1369-1376.

[4] B. Choi, “Step load response of a current-mode-controlled DC-to-DC Converter,” in IEEE Trans. Aerosp. Electron. Syst., Vol. 33, Oct. 1997, pp. 1115-1121.

[5] C. Sun, B. Lehman and R. Ciprian, “Dynamic modeling and control in average current mode controlled PWM DC/DC converters,” in Proc. IEEE PESC, 1999, pp. 1152-1157.

[6] G. Nirgude, R. Tirumala and N. Mohan, “A new, large-signal average model for single-switch DC-DC converters operating in both CCM and DCM,” in Proc. IEEE PESC, 2001, pp. 1736-1741.

[7] K.D.T. Ngo, S. Kirachaiwanich and M. Walters, “Buck modulator with improved large-power bandwidth,” in IEEE Trans. Aerosp. Electron. Syst., Vol. 38, Oct. 2002, pp. 1335-1343.

[8] D. Tran and D. Bennett, "Output filter design for high frequency switching mode power supplies," in Proc. HFPC, 1986, pp. 100-108.

[9] H. Tsafrin and S. B. Yaakov, “The dynamic response of PWM DC-DC converters with input filters,” in Proc. IEEE APEC, 1992, pp. 764-771.

[10] A.F. Rozman and K.J. Fellhoelter, “Circuit considerations for fast sensitive, low-voltage loads in a distributed power system,” in Proc. IEEE APEC, 1995, pp. 34-42.

[11] J.A. O’Connor, “Converter optimization for power low voltage, high performance microprocessors,” in Proc IEEE APEC, 1996, pp. 984-989.

[12] D. Goder and W. R. Pelletier, “V^2 architecture provides ultra-fast transient response in switch mode power supplies,” in Proc. HFPC, 1996, pp. 16-23.

[13] M. Zhang, M. Jovanovic and F. C. Lee, “Design considerations for low-voltage on-board DC/DC modules for next generations of data processing circuits,” in IEEE Trans. on Power Electronics, Vol. 11, No. 2, March 1996, pp. 328-337.

[14] J. Xu, X. Cao and Q. Luo, “The effects of control techniques on the transient response of switching DC-DC converters,” in Proc. IEEE PEDS, 1999, pp. 794-796.

[15] P. Wong, F.C. Lee, X. Zhou and J. Chen, “VRM transient study and output filter design for future processors,” in Proc. IEEE IECON, 1998, pp. 410-415.

[16] P. Wong, F.C Lee, X. Zhou and J. Chen, “Voltage regulator module (VRM) transient modeling and analysis,” in Proc. IEEE IAS, 1999, pp. 1669-1676.

[17] D. Briggs, R. Martinez, R. Miftakhutdinov and D. Skelton, "A fast, efficient synchronous-buck controller for microprocessor power supplies," in Proc. HFPC, 1998, pp. 170-176.

[18] B. Arbetter and D. Maksimovic, “DC-DC converter with fast transient response and high efficiency for low-voltage microprocessor loads,” in Proc. IEEE APEC, 1998, pp. 156-162.

[19] R. Miftakhutdinov, "Analysis of synchronous buck converter with hysteretic controller at high slew-rate load current transients," in Proc. HPFC, 1999, pp. 55-69.

[20] R. Miftakhutdinov, "Analysis and optimization of synchronous buck converter at high slew-rate load current transients," in Proc. IEEE PESC, 2000, pp. 714-720.

[21] L.D. Smith, R.E. Anderson, D.W. Forehand, T.J. Pelc and T. Roy, “Power distribution system design methodology and capacitor selection for modern CMOS technology,” in IEEE Trans. Advanced Packaging, Vol. 22, Issue 3, Aug. 1999, pp. 284-291.

[22] C.J. Mehas, K.D. Coonley and C.R. Sullivan, "Converter and inductor design for fast-response microprocessor power delivery," in Proc. IEEE PESC, 2000, pp. 1621-1626.

[23] A. Barrado, R. Vazquez, A. Lazaro, J. Pleite and E. Olias, “Fast transient response DC/DC converter for low output voltage,” in Electronics Letters, Vol. 38, Sept. 2002, pp. 1127-1128.

[24] L. Amoroso, M. Donati, X. Zhou and F.C. Lee, “Single shot transient suppressor (SSTS) for high current high slew rate microprocessor,” in Proc. IEEE APEC, 1999, pp. 284-288.

[25] F.N.K. Poon, C.K. Tse and J.C.P. Liu, “Very fast transient voltage regulators based on load correction,” in Proc. IEEE PESC, 1999, pp. 66-71.

[26] F. Zhang, J.M. Zhang, D.M. Xu and Z. Qian, "A novel high performance voltage regulator module," in Proc. IEEE APEC, 2001, pp. 258-261.

[27] N.K. Poon, C.P. Li and M.H. Pong, “A low cost DC-DC stepping inductance voltage regulator with fast transient loading response,” in Proc. IEEE APEC, 2001, pp. 268-272.

[28] A. Consoli, A. Testa, G. Giannetto and F. Gennaro, "A new VRM topology for next generation microprocessors," in Proc. IEEE PESC, 2001, pp. 339-344.

[29] A.M. Wu and S.R. Sanders. "An active clamp circuit for voltage regulation module (VRM) applications", in IEEE Trans. Power Electron., Vol. 16, Sept. 2001, pp. 623-634.

[30] Y.Y. Law, J.H. Kong, J.C.P. Liu, N.K. Poon and M.H. Pong, “Comparison of three topologies for VRM fast transient application,” in Proc. IEEE APEC, 2002, pp. 210-215.

[31] P.L. Wong, “Performance improvements of multi-channel interleaving voltage regulator modules with integrated coupling inductors,” dissertation of Virginia Polytechnic Institute and State University, March 2001.

[32] R. Miftakhutdinov, “Optimal design of interleaved synchronous buck converter at high slew-rate load current transients,” in Proc. IEEE PESC, 2001, pp. 1714-1718.

[33] “VRM 9.1 DC-DC converter design guidelines,” Intel document, Order number: 298646-001, Jan. 2002.

[34] R.B. Ridley, B.H. Cho and F.C. Lee, “Analysis and interpretation of loop gains of multiloop-controlled switching regulators,” in IEEE Trans. Power Electron., Vol. 3, Issue 4, Oct. 1988, pp. 489-498.

[35] R. Tymerski, V. Vorperian, F.C. Lee and W.T. Baumann, “Nonlinear modeling of the PWM switch,” in IEEE Trans. Power Electron., Vol. 4, Issue 2, April 1989, pp. 225-233.

[36] P.L. Wong, F.C. Lee, P. Xu and K. Yao, “Critical inductance in voltage regulator modules,” in IEEE Trans. Power Electron., Vol. 17, Issue 4, July 2002, pp. 485-492.

[37] A. Waizman and C.Y. Chong, “Extended adaptive voltage positioning,” Intel Technology Symposium, 2000.

[38] A.Waizman and C.Y. Chung, "Resonant free power network design using extended adaptive voltage positioning (EAVP) methodology," IEEE Trans. Advanced Packaging, Vol. 24, Aug. 2001, pp. 236-244.

[39] M. Zhang, “Powering Intel Pentium 4 processors,” Intel Technology Symposium, 2000.

[40] R. Lenk, “Understanding droop and programmable active droop,” Fairchild application bulletin AB-24. Available at http://www.fairchildsemi.com/an/AB/AB-24.pdf.

[41] “FAN5093: two slice interleaved synchronous buck converter,” Fairchild data sheet.

[42] Intel document, “VRM 9.1 DC-DC converter design guidelines,” Order number: 298646-001, Jan. 2002.

[43] Intel document, “Intel Pentium 4 Processor VR-Down design guidelines,” Order number: 249891-002, Jan. 2002.

[44] C.E. Hawkes, M.M. Walters and R.H. Isham, “Current mode DC/DC converter with controlled output impedance,” US Patent #6181120, Jan. 30, 2001.

[45] R. Redl and N.O. Sokal, “Optimizing dynamic behavior with input and output feed-forward and current-mode control,” in Proc. Powercon7, 1980, H1, pp. 1-16.

[46] R. Redl and N.O. Sokal, “Near-optimum dynamic regulation of DC-DC converters using feed-forward of output current and input voltage with current-mode control,” IEEE Trans. Power Electron., Vol. 1, July 1986, pp. 181-192.

[47] G.K. Schoneman and D.M. Mitchell, “Output impedance considerations for switching regulators with current-injected control,” in Proc. IEEE PESC, 1987, pp. 324-335.

[48] L.D. Varga and N.A. Losic, “Synthesis of zero-impedance converter,” IEEE Trans. Power Electron., Vol. 7, Jan. 1992, pp. 152-170.

[49] R. Redl, B.P. Erisman and Z. Zansky, “Optimizing the load transient response of the buck converter,” in Proc. IEEE APEC, 1998, pp. 170-176.

[50] R. Redl and B.P. Erisman, “Designing Minimum cost VRM8.2/8.3 compliant converters,” in Proc. HFPC, 1998, pp. 172-181.

[51] N.A. Losic, L.D. Varga and Z.D. Popovic, “Generalized synthesis and applications of zero-impedance converter and its dual,” IEEE Trans. Circuits Syst. I, Vol. 46, Nov. 1999, pp. 1349-1359.

[52] S.A. Chickamenahalli, S. Mahadevan, E. Stanford and K. Merley, “Effect of target impedance and control loop design on VRM stability,” in Proc. IEEE APEC, 2002, pp. 196-202.

[53] R.B. Ridley, "A new continuous-time model for current-mode control," IEEE Trans. Power Electron., Vol. 6, April 1991, pp. 271-280.

[54] R.W. Erickson and D. Maksimovic, "Fundamentals of power electronics," 2nd ed., Kluwer Academic Publishers, 2000, ISBN 0792372700.

[55] J. Sun and R.M. Bass, "Modeling and practical design issues for average current control," in Proc. IEEE APEC, 1999, pp. 980-986.

[56] B.M. Duduman, "Three-phase buck switching converter for Pentium 4 processors," Intersil application note AN9906. Available at http://www.intersil.com/data/AN/AN9/AN9906/AN9906.pdf.

[57] R. Lenk, "Understanding droop and programmable active droop," Fairchild application bulletin AB-24. Available at http://www.fairchildsemi.com/an/AB/AB-24.pdf.

[58] J.W. Kim, H.S. Choi and B.H. Cho, "A novel droop method for the converter parallel operation," in Proc. IEEE APEC, 2001, pp. 959-964.

[59] B.T. Irving and M.M. Jovanovic, "Analysis, design, and performance evaluation of droop current-sharing method," in Proc. IEEE APEC, 2000, pp. 235-241.

[60] Z. ye, D. Boroyevich, K. Xing and F.C. Lee, "Design of parallel sources in DC distributed power systems by using gain-scheduling technique," in Proc. IEEE PESC, 1999, pp. 161-165.

[61] R.W. Ashton J.G., Ciezki and M.G. Badorf, "The synthesis and hardware validation of DC-to-DC converter feedback controls," in Proc. IEEE PESC, 1998, pp. 65-71.

References: Part C

[1] P. Xu, "Multiphase voltage regulator modules with magnetic integration to power microprocessors," dissertation of Virginia Polytechnic Institute and State University, Jan. 2002.

[2] L. Spaziani, "A study of MOSFET performance in processor targeted buck and synchronous rectifier buck converters," in Proc. HFPC, 1996, pp. 123-137.

[3] P. Xu, J. Wei and F.C. Lee, "The active-clamp couple-buck converter-a novel high efficiency voltage regulator module," in Proc. IEEE APEC, 2001, pp. 252-257.

[4] J. Lange, "Tapped inductor improves efficiency for switching regulator," in Electronic Design, Vol. 27, No. 16, 2 Aug. 1979, pp. 114-116.

[5] A. Pietkiewicz and D. Tollik, "Small-signal analysis of a coupled-inductor step-down switching DC-DC converter," in Proc. IEEE INTELEC, 1986, pp. 241-246.

[6] M. Rico, J. Uceda, J. Sebastian and F. Aldana, "Static and dynamics modeling of tapped-inductor DC-to-DC converters," in Proc. IEEE PESC, 1987, pp. 281-288.

[7] D. Edry, M. Hadar, O. Mor and S. Ben-Yaakov "A SPICE compatible model of tapped-inductor PWM converters," in Proc. IEEE APEC, 1994, pp. 1021-1027.

[8] P.H. Wurm and F.A. Himmelstoss, "Application of EXCEL for analyzing DC/DC converters," in 6th Workshop on Computers in Power Electronics, 1998, pp. 113-118.

[9] J. Li, C.R. Sullivan and A. Schultz, "Coupled-inductor design optimization for fast-response low-voltage DC-DC converters," in Proc. IEEE APEC, 2002, pp. 817-823.

[10] R. Lenk, "Introduction to the tapped buck converter," in Proc. HFPC, 2000, pp.155-166.

[11] D.A. Grant and Y. Darroman, "Extending the tapped-inductor DC-to-DC converter family," in Electronics Letters, Vol. 37, Feb. 2001, pp. 145-146.

[12] "A non-isolated high input voltage VRM topology — Improved center tapped inductor technology," VRM Quarterly Review Report, Section 2, July 1998, VPEC, Virginia Tech, pp. 29-35.

[13] R.P. Lethellier, "Buck converter with inductive turn ratio optimization," US Patent #6094038, July 25, 2000.

[14] J. Kingston, R. Morrison, M.G. Egan and G. Hallissey, “Application of a passive lossless snubber to a tapped inductor buck DC/DC converter,” in Proc. IEEE Power Electronics, Machines and Drives, 2002, pp. 445-450.

[15] J. Park and B.H. Cho, “The zero voltage switching (ZVS) critical conduction mode (CCM) buck converter with tapped-inductor,” in Proc. IEEE APEC, 2003, pp. 1077-1081.

[16] J. Wei, P. Xu, H. Wu, F.C. Lee, K. Yao and M. Ye, “Comparison of three topology candidates for 12V VRM,” in Proc. IEEE APEC, 2001, pp. 245-251.

[17] J. Wei, P. Xu, F.C. Lee, K. Yao and M. Ye, "Static and dynamic modeling of the active clamp coupled-buck converter," in Proc. IEEE PESC, 2001, pp. 260-265.

[18] P. Xu, J. Wei and F.C. Lee, “The active-clamp couple-buck converter-a novel high efficiency voltage regulator module,” in Proc. IEEE APEC, 2001, pp. 252-257.

[19] Y. Meng, K. Yao, J. Wei, P. Xu and F.C. Lee,” An investigation about five candidates for 12V VRM topology,” in Proc. CPES Seminar, 2002, pp. 178-184.

[20] P. Xu, J. Wei, K. Yao, Y. Meng and F.C. Lee, “Investigation of candidate topologies for 12V VRM,” in Proc. IEEE APEC, 2002, pp. 686-692.

[21] J. Wei, P. Xu and F.C. Lee, “A high efficiency topology for 12 V VRM-push-pull buck and its integrated magnetics implementations,” in Proc. IEEE APEC, 2002, pp. 679-685.

[22] P. Xu, J. Wei and F.C. Lee, “Multiphase coupled-buck converter-a novel high efficient 12 V voltage regulator module,” in IEEE Trans. Power Electron., Vol. 18 Issue 1, Jan. 2003, pp. 74-82.

[23] J. Wei and F.C. Lee, “A soft-switched high efficiency fast transient response 12V VRM — phase-shift buck,” in Proc. CPES Seminar, 2002, pp. 158-164.

[24] J. Wei and F.C. Lee, “A novel soft-switched, high-frequency, high-efficiency, high-current 12v voltage regulator - the phase-shift buck converter,” in Proc. IEEE APEC, 2003, pp. 724-730.

[25] J. Wei, K. Yao, M. Xu and F.C. Lee, “Applying transformer concept to non-isolated voltage regulators significantly improves the efficiency and transient response,” in Proc. IEEE PESC, 2003, pp. 1599-1604.

[26] W. Kellerman, H.M. El-Din, C.E. Graham and G.A. Maria, “Optimization of fixed tap transformer setting in bulk electric systems,” in IEEE Trans. Power Systems, Vol. 6, Aug. 1991, pp. 1126-1132.

[27] J.P.G. Abreu, C.A.M. Guimaraes and G. Paulillo, “A proposal for a power converter autotransformer,” in Proc. IEEE Electric Machines and Drives, 1997, pp. TC3/6.1-TC3/6.4.

[28] M. Kang, B.O. Woo, P.N. Enjeti and I.J. Pitel, “Auto-connected electronic transformer (ACET) based multi-pulse rectifiers for utility interface of power electronic systems,” in Proc. IEEE IAS, 1998, pp. 1554-1561.

[29] R.G. Andrei, M.E. Rahman, C. Koeppel and J.P. Arthaud, “A novel autotransformer design improving power system operation,” in IEEE Trans. Power Delivery, Vol. 17, April 2002, pp. 523-527.

[30] P. Wong, P. Xu, B. Yang and F.C. Lee, “Performance improvements of interleaving VRMs with coupling inductors,” in IEEE Trans. Power Electro., Vol. 16, July 2001, pp. 499-507.

[31] T. Ninomiya, N. Matsumoto, M. Nakahara and K. Harada, “Static and dynamic analysis of zero-voltage-switched half-bridge converter with PWM control,” In Proc. IEEE PESC, 1991, pp. 230-237.

References: Part D

[1] K. Liu, R. Oruganti and F.C. Lee, "Quasi-resonant converters – Topologies and characteristics," in IEEE Trans. Power Electronics, Vol. 2, Jan. 1987, pp. 62-71.

[2] M.M. Jovanovic, K. Liu, R. Oruganti and F.C. Lee, "State-plane analysis of quasi-resonant converters," in IEEE Trans. Power Electronics, Vol. 2, Jan. 1987, pp. 36-44.

[3] F.C. Lee, "High-frequency quasi-resonant converter technologies," in IEEE Proceedings, Vol. 76, April 1988, pp. 377-390.

[4] M.M. Jovanovic, D.C. Hopkins and F.C. Lee, "Evaluation and design of megahertz-frequency off-line zero-current-switched quasi-resonant converters," in IEEE Trans. Power Electronics, Vol. 4, Jan. 1989, pp. 136-146.

[5] M.M. Jovanovic and F.C. Lee, "DC characteristics and stability of push-pull and bridge-type zero-current-switched quasi-resonant converter," in IEEE Trans. Power Electronics, Vol. 4, July 1989, pp. 339-347.

[6] M.M. Jovanovic, F.C. Lee and D.Y. Chen, "A zero-current-switched off-line quasi-resonant converter with reduced frequency range: analysis, design, and experimental results," in IEEE Trans. Power Electronics, Vol. 4, April 1989, pp. 215-224.

[7] D.C. Hopkins, M.M. Jovanovic, F.C. Lee and F.W. Stephenson, "Hybridized off-line 2-MHz zero-current-switched quasi-resonant converter," in IEEE Trans. Power Electronics, Vol. 4, Jan. 1989, pp. 147-154.

[8] A. de Hoz and E. de la Cruz, "Analysis and design of a zero current switched quasi-resonant converter with synchronous rectification for low output voltage applications," in Proc. IEEE PESC, 1992, pp. 221-228.

[9] P. Croll and G. Grellet, "Multiple output DC/DC zero-current switch quasi-resonant converter," in Proc. IEEE INTELEC, 1993, pp. 215-220.

[10] A. Dmowski, R. Bugyi and P. Szewczyk, "Design of a buck converter with zero-current turn-off MCT," in Proc. IEEE IAS, 1994, pp. 1025-1030.

[11] A. Brambilla, E. Dallago, P. Nora and G. Sassone, "Study and implementation of a low conduction loss zero-current resonant switch," in IEEE Trans. IE, Vol. 41, Issue 2, April 1994, pp. 241-250.

[12] D. Beatty and I. Batarseh, “Topical overview of soft-switching PWM high frequency converters,” in Proc. IEEE Southcon, 1995, pp. 47-52.

[13] J. Mueko and E. Greczko, “Quasi-resonant buck converter-possible topologies, similarities and differences,” in Proc. IEEE International Symposium on Industrial Electronics (ISIE), 1996, pp. 719-723.

[14] H.S.H. Chung, S.Y.R. Hui, K.M. Chan and C.T. Chung, “A ZCS bi-directional flyback DC/DC converter using the leakage inductance of the coupled inductor,” in Proc. IEEE APEC, 2000, pp. 979-985.

[15] A. Kato, A. Ueda and A. Torii, “Characteristics of full resonant ZCS converter using a synchronous rectifier,” in Proc. IEEE Power Conversion Conference (PCC), 2002, pp. 615-620

[16] I. Barbi, J.C.O. Bolacell, D.C. Martins and F.B. Libano, “Buck quasi-resonant converter operating at constant frequency: analysis, design, and experimentation,” in IEEE Trans. Power Electronics, Vol. 5, July 1990, pp. 276-283.

[17] D. Maksimovic and S. Cuk, “Constant-frequency control of quasi-resonant converters,” in IEEE Trans. Power Electronics, Vol. 6, Oct. 1991, pp. 141-150.

[18] L. Yang, Y. Zhang and C.Q. Lee, “A family of constant-switching-frequency quasi-square-wave converters,” in Canadian Conference on Electrical and Computer Engineering, 1993, pp. 309-312.

[19] B. Ray, “Bidirectional DC/DC power conversion using constant-frequency quasi-resonant topology,” in Proc. IEEE ISCAS, 1993, pp. 2347 -2350.

[20] L. Yang, D. Long and C.Q. Lee, “From variable to constant switching frequency topologies: A general approach,” in Proc. IEEE PESC, 1993, pp. 517-523.

[21] P. Jain, H. Soin and M. Cardella, “Constant frequency resonant DC/DC converters with zero switching losses,” in IEEE Trans. Aero. & Electro. Sys., Vol. 30, April 1994, pp. 534-544.

[22] P. Dananjayan and C. Chellamuthu, “A new constant frequency zero voltage switching buck quasi-resonant converter,” in Proc. International Conference on Power Electronics, Drives and Energy Systems for Industrial Growth, 1996, pp. 176-182.

[23] R. Petkov, “Analysis and design of a quasi-resonant buck converter operating in a constant frequency, constant output power mode,” in Proc. IEEE INTELEC, 1998, pp. 123-128.

[24] L.F. Casey and M.F. Schlecht, "A high-frequency, low volume, point-of-load power supply for distributed power systems," in IEEE Trans. Power Electronics, Vol. 3, Jan. 1988, pp. 72-82.

[25] W.C. Bowman, F.T. Balicki, F.T. Dickens, R.M. Honeycutt, W.A. Nitz, W. Strauss, W.B. Suiter and N.G. Ziesse, "A resonant DC-to-DC converter operating at 22 megahertz," in Proc. IEEE APEC, 1988, pp. 3-11.

[26] W.A. Tabisz, P.M. Gradzki and F.C. Lee, "Zero-voltage-switched quasi-resonant buck and flyback converters -- Experimental results at 10 MHz," in IEEE Trans. Power Electronics, Vol. 4, April 1989, pp. 194-204.

[27] K. Yoshida, T. Ishii and N. Nagagata, "Zero voltage switching approach for flyback converter," in Proc. IEEE INTELEC, 1992, pp. 324-329.

[28] W.A. Tabisz and F.C. Lee, "Zero-voltage-switching multi-resonant technique-a novel approach to improve performance of high-frequency quasi-resonant converters," in IEEE Trans. Power Electronics, Vol. 4, Oct. 1989, pp. 450-458.

[29] M.J. Ryan, W.E. Brumsickle, D.M. Divan and R.D. Lorenz, "New ZVS LCL-resonant push-pull DC-DC converter topology," in Proc. IEEE IAS, 1997, pp. 1673-1680.

[30] A. Consoli, F. Gennaro, C. Cavallaro and A. Testa, "A comparative study of different buck topologies for high efficiency low voltage applications," in Proc. IEEE PESC, 1999, pp. 60-65.

[31] H. Tanaka, T.Ninomiya, Y. Okabe and T. Zaitsu, "Efficiency improvement of synchronous rectifier in a ZVS-PWM controlled series-resonant converter with active clamp," in Proc. IEEE APEC, 2000, pp. 679-682.

[32] Y. Zhang, P.C. Sen and Y. Liu "A novel zero voltage switched (ZVS) buck converter using coupled inductor," in Proc. Electrical and Computer Engineering in Canadian, 2001, pp. 357-362.

[33] B. Carsten, "Design techniques for transformer active reset circuits at high frequency and power levels," in Proc. HFPC, 1990, pp. 235-245.

[34] K. Yoshida, T. Ishii and N. Nagagata, "Zero voltage switching approach for flyback converter, " in Proc. IEEE INTELEC, 1992, pp. 324-329.

[35] N. Frohleke, J. Richter, P. Wallmeier and H. Grotstollen, "Soft switching forward-flyback converter with one magnetic component and current doubler rectification circuit," in Proc. IEEE IAS, 1996, pp. 1161-1168.

[36] R. Watson, F.C. Lee and G.C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," IEEE Trans. Power Electron. , Vol. 11, Jan. 1996, pp. 162-169.

[37] D.H. Park, H.J. Kim and Y.S. Sun, "A development of the off-line active clamp ZVS forward converter for telecommunication applications," in Proc. IEEE INTELEC, 1997, pp. 271-276.

[38] A. Acik and I. Cadirci, "Active clamped ZVS forward converter with soft-switched synchronous rectifier for maximum efficiency operation," in Proc. IEEE PESC, 1998, pp. 1237-1242.

[39] F.J. Nome and I. Barbi, "A ZVS clamping mode-current-fed push-pull DC-DC converter," in Symposium IEEE ISIE, 1998, pp. 617-621.

[40] R.L. Steigerwald, "High efficiency gate driver circuit for a high frequency converter," US Patent #4967109, 1990.

[41] R.L. Steigerwald, "Lossless gate driver circuit for a high frequency converter," US Patent #5010261, 1991.

[42] D. Maksimovic, "A MOS gate drive with resonant transitions," in Proc. IEEE PESC, 1991, pp. 527-532.

[43] H.L.N. Wiegman, "A resonant pulse gate drive for high frequency applications," in Proc. IEEE APEC, 1992, pp. 738-743.

[44] S.H. Weinberg, "A novel lossless resonant MOSFET driver," in Proc. IEEE PESC, 1992, pp. 1003-1010.

[45] E.T. Perusse, "High efficiency FET driver with energy recovery," US Patent #5134320, 1992.

[46] B.S. Jacobson, "High frequency resonant gate driver with partial energy recovery," in Proc. HFPC, 1993, pp. 133-141.

[47] B.S. Jacobson, "High frequency resonant gate drive for a power MOSFET," U.S. Patent #5264736, Nov. 1993.

[48] J. Diaz, M.A. Perez, F.J. Linera and F. Nuno, "New family of loss-less power MOSFET drivers," in Proc. CIEP, 1994, pp. 43-48.

[49] D.W. Cripe, "High efficiency quasi-square wave drive circuit for switching power amplifiers," US Patent #5276357, 1994.

[50] J. Diaz, M.A. Perez, F.M. Linera and F. Aldana, "A new lossless power MOSFET driver based on simple DC/DC converters," in Proc. IEEE PESC, 1995, pp. 37-43.

[51] S.H. Weinberg and T.A.A.A. Canon, "Low-loss resonant circuit for capacitance driver," US Patent #5537021, 1996.

[52] B. Arntzen and D. Maksimovic, "Switched-capacitor DC/DC converters with resonant gate drive," IEEE Trans. Power Electro., Vol. 13, Sept. 1998, pp.892-902.

[53] R.L. Kollman and J.G. Sills, "Resonant bilateral charging and discharging circuit," US Patent #5804943, 1998.

[54] Y. Panov and M.M. Jovanovic, "Design considerations for 12V/1.5V, 50A voltage regulator modules," in Proc. IEEE APEC, 2000, pp. 39-46.

[55] Y. Chen, F.C. Lee, L. Amoroso and H. Wu, "A resonant MOSFET gate driver with complete energy recovery," in Proc. IEEE PIEMC, 2000, pp. 402-406.

[56] Yuhui Chen, "Resonant gate drive techniques for power MOSFETs," thesis of Virginia Polytechnic Institute and State University, May 2000.

[57] I.D. de Vries, "A resonant power MOSFET/IGBT gate driver," in Proc. IEEE APEC, 2002, pp. 179-185.

[58] K. Shenai, "Accurate characterization of gate resistance and high-frequency switching efficiency of a power MOSFET," in Proc. IEEE PESC, 1990, pp. 107-112.

[59] T. Ohguro, H. Naruse, H. Sugaya, S. Nakamura, E. Morifuji and H. Kimijima et al. "High performance RF characteristics of raised gate/source/drain CMOS with Co salicide," in Symposium on VLSI Technology, 1998, Digest of Technical Papers, pp. 136-137.

[60] J. Zhou, M. Xu and F.C. Lee, "12V-input self-driven VRM," Invention Disclosure, VTIP 03.015.

[61] N.X. Sun, X. Duan, X. Zhang, A. Huang and F.C. Lee, "Design of a 4 MHz, 5V to 1V monolithic voltage regulator chip," in Proc. IEEE ISPSD, 2002, pp. 217-220.

[62] Y. Katayama, S. Sugahara, H. Nakazawa and M. Edo, "High-power-density MHz-switching monolithic DC-DC converter with thin-film inductor," in Proc. IEEE PESC, 2000, pp. 1485-1490.

[63] T. Sato, H. Tomita, A. Sawabe and T.Inoue, "A magnetic thin film inductor and its application to a MHz switching DC-DC converter," in IEEE Trans. Magnetics, Vol. 30, Issue 2, Aug 1993, pp. 217-223.

[64] Z. Liang, J.D. van Wyk, F.C. Lee, D. Boroyevich, E.P. Scott, J. Chen and Y. Pang, "Integrated packaging of a 1kW switching module using a novel planar integration technology," to be published in IEEE Tran. Power Electronics.

[65] J.D. van Wyk, S. Wen, Z. Liang, J.T. Strydom, S-Y. Lee, H. Odendaal and D.A. Huff, "The development of planar high density hybrid integration technologies for power electronics," in Proc. EPE-PEMC, 2002, Cavtat, Paper SSJAF-01, 14.

[66] R. Chen, J.T. Strydom and J.D. van Wyk, "Design of planar integrated passive module for zero voltage switched asymmetrical half bridge PWM converter," in Proc. IEEE IAS, 2001, pp. 2232-2238.

Vita

The author, Kaiwei Yao, was born in Yueyang, Hunan, P. R. China in 1970. He received the B.S. degree from Xi'an Jiaotong University, China in 1992 and the M.S. degree from Zhejiang University, China in 1995, both in electrical engineering. Since 1998 he has been working toward the Ph.D. degree in power electronics at Virginia Polytechnic Institute and State University, Blacksburg.

From 1995 to 1998, he was employed as an engineer for uninterrupted power supply (UPS) design at Hwadar Electronics, Shenzhen, China. From March 2003, he worked as Technical Coordinator at the Center for Power Electronics Systems (CPES). His research interests include power management, high-frequency high-density power supplies, modeling and control for converters, design for distribute-power systems, and power-factor-correction techniques.

The author is a member of the IEEE Power Electronics Society. He also served as vice-president of IEEE Power Electronics Society Student Branch at Virginia Tech, and as a Student Council member of CPES.