

A Wide Range and Precise Active and Reactive Power Flow Controller for Fuel Cell Power Conditioning Systems

Sung Yeul Park

Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

Jih-Sheng Lai, Chairman
Douglas J. Nelson
Fred Wang
Virgilio Centeno
William T. Baumann

July 27, 2009
Blacksburg, Virginia

Keywords: Active Power, Reactive Power, Power Conditioning System, Grid-Tie Inverter,
Proportional-Resonant Control, Admittance Compensator

Copyright 2009, Sung Yeul Park

A Wide Range and Precise Active and Reactive Power Flow Controller for Fuel Cell Power Conditioning Systems

Sung Yeul Park

(Abstract)

This dissertation aims to present a detailed analysis of the grid voltage disturbance in frequency domain for the current control design in the grid-tie inverter applications and to propose current control techniques in order to minimize its impact and maximize feasibility of the power conditioning system in distributed generations. Because the grid voltage is constantly changing, the inverter must be able to respond to it. If the inverter is unable to respond properly, then the grid voltage power comes back to the system and damages the fuel cell power conditioning systems.

A closed-loop dynamic model for the current control loop of the grid-tie inverter has been developed. The model explains the structure of the inverter admittance terms. The disturbance of the grid voltages has been analyzed in frequency domain. The admittance compensator has been proposed to prevent the grid voltage effect. The proposed lead-lag current control with admittance compensator transfers current properly without system failure. In order to get rid of the steady-state error of the feedback current, a proportional-resonant controller (PR) has been adopted. A PR control with admittance compensation provides great performance from zero power to full power operation. In addition, active and reactive power flow controller has been proposed based on the PR controller with admittance compensation. The proposed active and reactive power flow control scheme shows a wide range power flow control from pure leading power to pure lagging power. Finally, the proposed controller scheme has been verified its feasibility in three phase grid-tie inverter applications. First of all, a half-bridge grid-tie inverter has been designed with PR controller and admittance compensation. Then three individual grid-tie inverters has been combined and produced three phase current to the three phase grid in either balanced condition or unbalanced condition.

The proposed control scheme can be applied not only single phase grid-tie inverter application, but also three phase grid-tie inverter application. This research can be applicable to the photovoltaic PCS as well. This technology makes renewable energy source more plausible for distributed generations.

Acknowledgements

First of all, I would like to give gratitude and praise to my heavenly Father, God, my Savior, Jesus Christ, and my comforter, Holy Spirit for the grace and the love throughout my life. Without God's grace, I could not have come this far. My Lord is the source of my life!

I would also like to thank my advisor, Prof. Jason Lai, for being my advisor and presenting me an opportunity to study and do research in the Future Energy Electronics Center at Virginia Tech. Prof. Jason Lai and Mrs Lai have been provided me and my family countless advice and comments whenever I need to decide important things of my academic life.

I would also like to thank Prof. Fred Wang, Prof. William T. Baumann, Prof. Virgilio Centeno, and Prof. Douglas J. Nelson for serving as members of my Ph.D advisory committee, for making valuable comments that helped me make this work better.

My appreciation goes to Mr. Gary Kerr for providing not only mechanical parts support but also sharing his vision in faith, Mr. Hide Miwa for coming along with me with encouragement and correcting my writing, and Mr. Jian-Liang Chen for co-operating all work without complaining.

I would also like to extend my thanks to my colleagues in the Future Energy Electronics Center. Mr. Rae-Young Kim, Dr. Wensong Yu, Mr. Neil Savio D'Souza, Mr. Hao Qian, Mr. Pengwei Sun, Mr. Christopher Hutchens, Mr. Benjamin York, Mr. Bret Whitaker, Mr. Zidong Liu, Mr. Daniel Martin, and Mr. Ahmed Koran all assisted me greatly.

In addition, I would like to extend my gratitude to visiting scholars, Mr. Kenichiro Sano, Dr. Woo-Young Choi, Dr. Woo-Chul Lee, Dr. Yubin Wang, Dr. Yuang-Shung Lee, and Dr. Soon-Kurl Kwon, Dr. In-Dong Kim, Dr. Tae-Won Chun, Dr. Ju-Won Baek, and Dr. Jung-Yeul Ahn.

I would also like to extend my thanks to my colleagues in the Future Energy Electronics Center alumni: Mr. Seung-Ryul Moon, Dr. Junhong Zhang, Dr. Konstantin Louganski, Dr. Changrong, Dr. Xudong, Mr. Gregory Malone, Mr. Brennen Ball, Mr. Brad Tomlinson. Mr. Alexander Miller, Mr. Wei-Han Lai, Mr. William Gatune.

I would like to give my special thanks to my pastor, Hyun David Chung, and his family for their prayer and fellowship in God. Thank my sincere brothers and their families of Korean Baptist Church of Blacksburg (KBCB).

I can't imagine I can be here without my parents' and parents-in-law support. I really thank them for their love, care, pray and sacrifices for my family. Their endless and unconditional love have been my biggest support throughout my life.

I am deeply grateful to my wife, Song-Suk Cho, who God allowed me to marry. Without her love, pray, patience, and support, I would not have been able to finish my Ph.D. works. Finally, my special thanks go to my four children, Youngjin, Sungjin, Soojin, and Taejin for giving me such a joy during the tough times as a Ph.D. student.

Table of Contents

Chapter 1 Introduction	1
1.1 Research Background.....	1
1.2 Renewable Energy Power Conditioning System (PCS)	2
1.2.1 Front-End Converter – DC-DC Converter	2
1.2.2 Back-End Converter – Utility Grid-Tie DC-AC Inverter	3
1.2.3 Current Controller Design Issues for the Grid-Tie Inverter Applications	3
1.3 State-of-the-art Current Control Technologies	4
1.4 Research Motivation	7
1.5 Dissertation Outline and Major Results	7
Chapter 2 Current loop control with admittance compensation for a single-phase grid-tie fuel cell power conditioning system	10
2.1 Introduction	10
2.2 Grid-Tie Inverter Control System Modeling.....	12
2.3 Elimination of the Lagging Phase Admittance Effect.....	16
2.4 Current Loop Controller Design and Simulation	18
2.5 Experimental Verification.....	22
2.6 Conclusion	26
Chapter 3 Admittance compensation in current loop control for the grid-tie LCL Fuel Cell inverter	27
3.1 Introduction	27
3.2 Grid-Tie Inverter Control System Modeling.....	29
3.3 Elimination of the Undesirable Admittance Effect.....	33
3.4 LCL Filter for the Grid-Tie Inverter	35
3.5 Current Loop Controller Design and Simulation.....	38

3.6 Experimental Verification	44
3.7 Conclusion	50
Chapter 4 A wide range precise active and reactive power flow controller for a solid oxide fuel cell power conditioning system.....	52
4.1 Introduction.....	52
4.2 Control System Modeling for the LCL Filter Based Grid-Tie Inverter.....	54
4.3 Compensator Design	57
4.3.1 Admittance Compensator for the Enhance Stability.....	57
4.3.2 Proportional and Resonant Compensator.....	58
4.3.3 Control for the Active and Reactive Power Flow	59
4.3.4 DC Bus Voltage Requirement Analysis Using Phasor Diagrams.....	61
4.4 Simulation and Experimental Verification.....	64
4.4.1 DC Bus Voltage Requirement Verification	64
4.4.2 Wide Range Power Flow Control Verification.....	68
4.5 Conclusion	72
Chapter 5 Versatile Utilization of three half-bridge single phase grid tie inverters four wires configuration for the renewable energy distributed generation	74
5.1 Introduction	74
5.2 Modeling and Control of the Half-Bridge Single Phase Grid-Tie Inverter	76
5.2.1 Admittance Compensator for the Enhance Stability.....	78
5.2.2 Proportional and Resonant Compensator.....	79
5.2.3 Two Current Command Modes.....	79
5.2.4 Proposed Three Half-Bridge Single Phase Grid-Tie Inverter	80
5.3 Simulation and Experimental Verification	83

5.4 Conclusion	89
Chapter 6 Summary, Contributions, and Future Work	90
6.1 Summary	90
6.2 Contributions.....	92
6.2.1 Itemized Contributions.....	92
6.2.2 Scholarly Contributions	93
6.3 Future work	94
References	95

List of Figures

Fig. 1.1 Three major renewable energy sources and utilization	1
Fig. 1.2 Fuel cell power conditioning system for the utility grid distributed generation.....	2
Fig. 2.1 Inverter control system of a fuel cell PCS	13
Fig. 2.2 Inverter control diagram using transfer functions.....	13
Fig. 2.3 Admittance Y plot in frequency domain with uncompensated term(Y_1) and lagging phase term(Y_2)	15
Fig. 2.4 Current reference correction method	16
Fig. 2.5 Lagging phase admittance cancellation method	17
Fig. 2.6 Bode plot of the current loop gain	19
Fig. 2.7 Time-domain simulation results at $P_{ref}=1.5$ kW without $G_c(s)$ compensation	20
Fig. 2.8 Time-domain simulation results at $P_{ref}=1.5$ kW with $G_c(s)$ compensation	20
Fig. 2.9 Time-domain simulation results at $P_{ref}=4$ kW without $G_c(s)$ compensation	21
Fig. 2.10 Time-domain simulation results at $P_{ref}=4$ kW with $G_c(s)$ compensation	21
Fig. 2.11 PCS prototype test setup.....	22
Fig. 2.12 Block diagram of the software phase locked loop structure.....	23
Fig. 2.13 Synchronization waveform of v_{ac} and v_{synch}	24
Fig. 2.14 Steady-state inverter operations at 1.5 kW condition.....	25
Fig. 2.15 Steady-state inverter operations at 4 kW condition.....	25
Fig. 3.1 Control system block diagram of an LCL-filter based fuel cell PCS inverter.....	30
Fig. 3.2 Simplified inverter power circuit from LCL-filter to L-filter.....	31
Fig. 3.3 L-filter inverter control diagram using transfer functions	32
Fig. 3.4 Current reference correction method	34
Fig. 3.5 Admittance compensation method.....	34

Fig. 3.6 Admittance terms block diagram	34
Fig. 3.7 Universal inverter for standalone mode.....	36
Fig. 3.8 Universal inverter for utility grid-tie mode.....	36
Fig. 3.9 Block diagram of the complete admittance compensated LCL-filter based grid-tie inverter	37
Fig. 3.10 Bode plot with different ω_c and k_r values	39
Fig. 3.11 Frequency response measurements with designed controller.....	40
Fig. 3.12 Bode plot of the current loop gain with and without compensator.....	40
Fig. 3.13 Simulation results at zero power command start-up with admittance compensation.....	42
Fig. 3.14 Simulation results at zero power command start-up without admittance compensation.....	42
Fig. 3.15 Simulation results at peak current command $I_{ref, pk} = 20A$ with designed current controller and $G_c(s)$ compensation	43
Fig. 3.16 Solid oxide fuel cell simulator V-I Curve.....	44
Fig. 3.17 Input and output waveforms of standalone mode operation under 3kW condition.....	45
Fig. 3.18 Experimental results at zero power command start-up without compensation	46
Fig. 3.19 Experimental results at zero power command start-up with compensation	46
Fig. 3.20 Experimental results at peak current command $I_{ref, pk} = 20A$ with designed controller and $G_c(s)$ compensation	47
Fig. 3.21 Dynamic response of the power ramping up from 2.5 kW to 4 kW.....	48
Fig. 3.22 Dynamic response of the power ramping down from 4 kW to 3 kW.....	48
Fig. 3.23 PCS efficiency profiles under SOFC simulator test	49
Fig. 4.1 Proposed inverter control system of a fuel cell PCS	54
Fig. 4.2 Proposed inverter control diagram using transfer functions.....	55
Fig. 4.3 Block diagram of the adding admittance compensator after the current loop controller	58
Fig. 4.4 Block diagram of the software phase locked loop.....	60

Fig. 4.5 Block diagram of the current reference computation	61
Fig. 4.6 Simplified grid-tie inverter circuit	62
Fig. 4.7 Phasor diagram with active power only.....	63
Fig. 4.8 Phasor diagram with leading reactive power only.....	63
Fig. 4.9 Phasor diagram with lagging reactive power only.....	63
Fig. 4. 10 Simulation results of the active and reactive power with insufficient V_{dc}	65
Fig. 4. 11 Simulation results of the active and reactive power with sufficient V_{dc}	65
Fig. 4. 12 Voltage requirements with respect to the power factor angle at 5-kVA condition	66
Fig. 4. 13 Experimental results with $V_{dc} = 395$ V for the mixed 2.5 kW active and 2.5 kVAr lagging reactive power command	67
Fig. 4. 14 Experimental results with $V_{dc} = 416$ V for the mixed 2.5 kW active and 2.5 kVAr lagging reactive power command	67
Fig. 4. 15 Experimental results for the zero power command	68
Fig. 4. 16 Experimental results of the 1kVAr leading reactive power command, 1kW active power command, and 1kVAr lagging reactive power command.....	69
Fig. 4. 17 Experimental results for the 5kVAr leading reactive power command, 5kW active power command, and 5kVAr lagging reactive power command.....	70
Fig. 4. 18 Experimental results for the 5kVA apparent power with 3.5kW active power command and 3.5kVAr leading reactive power command, and the 5kVA apparent power with 3.5kW active power command and 3.5kVAr lagging reactive power command	71
Fig. 5.1 Proposed half-bridge single phase grid-tie inverter configuration	77
Fig. 5.2 Proposed inverter control diagram using transfer function	77
Fig. 5.3 Proposed three half-bridge single phase grid-tie inverters configuration.....	81
Fig. 5.4 Simulation waveform of the balance three phase grid voltage and constnat current command condition.....	84
Fig. 5.5 Simulation waveform of the unbalance three phase grid voltage and constnat power	

command condition.....	84
Fig. 5.6 Three half-bridge single phase grid-tie.....	85
Fig. 5.7 Experimental results of the three gate signals at zero crossing point.....	86
Fig. 5.8 Experimental waveform of the balanced three phase grid voltage.....	87
Fig. 5.9 Experimental waveform of the balanced three phase grid current.....	87
Fig. 5.10 Experimental waveform of the unbalanced three phase grid voltages.....	88
Fig. 5.11 Experimental waveform of the unbalanced three phase grid current for the same amount of three phase power.....	88

List of Tables

Table. 1.1 Distortion limits of the individual harmonics in IEEE 1547	4
Table. 5.1 Comparison of the computation time for the three control schemes	82

Chapter 1 Introduction

1.1 Research Background

There are three major renewable energy sources: wind power, solar photovoltaic, and fuel cell. Fig. 1.1 shows overall renewable energy sources and utilizing electricity [1]. Wind power usually comes from the wind turbine as an ac voltage; photovoltaic and fuel cell are dc voltages [2-4]. The main function of the power conditioning system is to match different voltage levels to an appropriate level, which the end user can use.

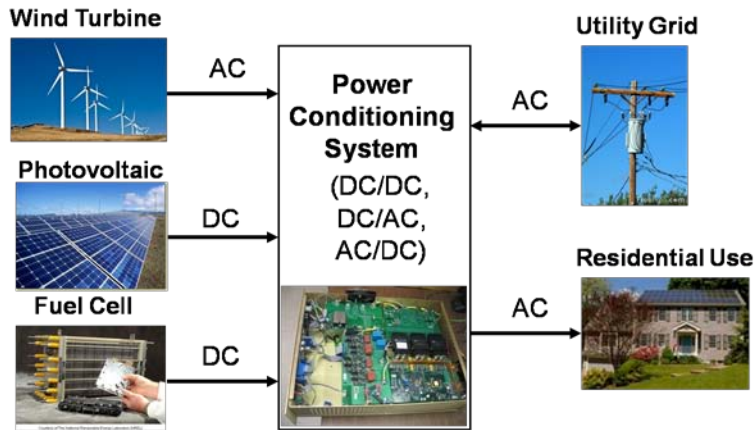


Fig. 1.1 Three major renewable energy sources and utilization

There are five major types of fuel cell systems which differ by their electrolyte: polymer electrolyte membrane fuel cell, alkaline fuel cell, solid-oxide fuel cell, phosphoric acid fuel cell, and molten carbonate fuel cell. Solid-oxide fuel cells are operated at high temperature, typically around 1000 °C. Because of this high temperature operation, not only can the cell supply heating for co-generation operation, but it can also use natural gas and coal gas for the fuel so that Co and H₂ can be reformed [5-6].

In the fuel cell power conditioning systems (PCS), the end-goal is to transfer power from the fuel cell renewable energy source to the utility. In order to accomplish this, the inverter must precisely control the output current while monitoring grid voltage. Because the grid voltage is constantly changing, the inverter must be able to respond to it. If the inverter is unable to respond properly, then energy from the grid may come back into the system and damage the fuel cell PCS. The most crucial parts of the PCS in renewable energy applications for distributed generation are to interface efficiently, reliably, and safely [4], [7-8].

1.2 Renewable Energy Power Conditioning System (PCS)

Fig. 1.2 shows the overall configuration of the fuel cell power conditioning system configuration. There are two converters. One is a front-end converter and the other is a back-end inverter.

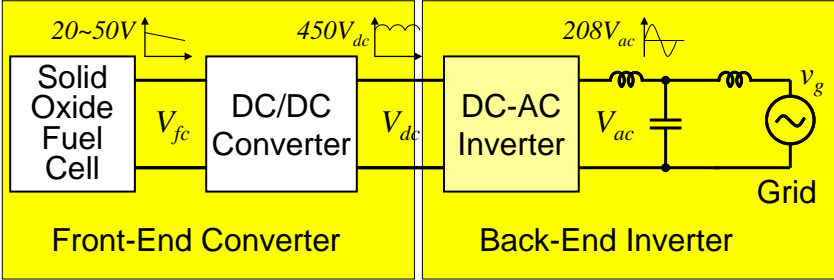


Fig. 1.2 Fuel cell power conditioning system for the utility grid distributed generation

1.2.1 Front-End Converter – DC-DC Converter

A dc-dc converter’s function is to convert the fuel cell’s low output voltage to high voltage in order for the inverter to produce either single-phase 120 V / 240 V for the residential use or

three-phase 208V for commercial use. For a 5kW power rating, the fuel cell output current can easily flow at 250A and can cause significant conduction loss. Soft-switching technology using a 3-phase, 6-leg converter has been proposed to achieve high efficiency [9]. Three-phase interleaving reduces the high frequency current ripple. The full-bridge, phase-shift modulation scheme achieves soft-switching. The closed-loop controller of the dc-dc converter regulates the dc link voltage [10].

1.2.2 Back-End Converter – Utility Grid-Tie DC-AC Inverter

While a standalone inverter controls the inverter output voltage, a utility grid-tie inverter controls the inverter output current with respect to the grid voltage. The requirements of the utility grid inverter are quite different from those of standalone operation inverters. A controller of the grid-tie inverter should control the current with respect to the grid voltage in order to transfer power to the utility grid at unity power factor. The control algorithm can be varied depending on a sensing point of either the inductor-current and the grid-current or the filter-capacitor-voltage and the grid-voltage.

1.2.3 Current Controller Design Issues for the Grid-Tie Inverter Applications

Back-end inverters or grid-tie inverters usually connect to the utility grid with filters in order to limit the switching frequency harmonics. Inductor, capacitor, and inductor configuration, or an LCL-filter, is often used for the utility grid-inverters. However, an LCL third-order-filter requires more complex current-control strategies to maintain system stability.

One of the control issues is the robustness of the controller against the grid disturbance. Another critical issue is the fast tracking capability, because it affects the grid current harmonics. IEEE standard 1547 limits the current THD to 5% with individual limits of 4% for each odd harmonic. Table. 1.1 shows the distortion limitation of the individual harmonics in IEEE 1547 [11].

Table. 1.1 Distortion limits of the individual harmonics in IEEE 1547

Individual Harmonics Order h	Distortion Limit
$h < 11$	< 4.0%
$11 \leq h < 17$	< 2.0%
$17 \leq h < 23$	< 1.5%
$23 \leq h < 35$	< 0.6%
$35 \leq h$	< 0.3%

1.3 State-of-the-art Current Control Technologies

Early research on grid-tie or grid-connected inverters dates back to the mid 1980s [12-13]. Current control technologies can be broadly classified into two groups. One is a linear control, such as proportional-integral current control, proportional-resonant current control, dq transformation current control, and predictive or deadbeat current control. The other is a non-linear control, such as hysteresis current control and sliding mode current control. A brief review of these control schemes follows below:

Proportional-integrator current control is most widely used method since the mid 1980s [13]. [14-15] proposed an output voltage feed-forward term for fast response and utility power

factor. [16] proposed a combination of deadbeat and PI control. Even though the PI control with a feed-forward term can provide faster dynamics than that of a conventional PI controller, it still has the steady-state error issue due to the sinusoidal current references.

Proportional-resonant current control has extremely high gains at the desired frequencies to reduce the amount of steady-state error. It has shown superior performance to that of a PI controller. [17] suggested a PR control, which can eliminate the steady-state error, for the voltage source inverter PWM rectifier application. [18] compared a resonant regulator and a synchronous frame PI regulator. [19] derived a theoretical equation to connect PR controller and a synchronous frame PI regulator. [20] pointed out the drawbacks to a PI and proposed a PR control with a harmonic compensator, which can improve odd-order harmonic distortions. [21] compared a PI control and a PR control. [22] implemented a PR control with a delta operator to compensate computational error. [23] introduced a quasi-PR controller for better implementation. [24] applied a PR control to a split filter capacitor configuration. [25] designed a PR connected in series with a tracking regulator for PV inverter. [26] showed a PR control with two-loop control strategy. [27] implemented a PR control with a FPGA with 100 kHz switching frequency. [28] utilized the weighted average value of two inductor currents. Due to several controller implementations, the computation delay should be considered. A key factor for operation is to align the fundamental and odd harmonic frequencies properly.

D-Q transformation control can handle the error signal as regulated dc quantity. Classical PI controller can be applied to the current controller to achieve infinite gains. After that, through re-transformation of the control value, the duty cycle can be determined. [29] suggested a DQ control, which can produce active power and reactive power, for a single-phase inverter

application. [30-31] adopted an all-pass-filter for the dq control, and [32] proposed a dq control for avoiding transformer core saturation. This control scheme can provide infinite gain at the fundamental frequency; however, it also demands more computation time and it can be a burden to the controller design and implementation.

Predictive current control or dead-beat control has a very fast dynamic response capability, so it can be utilized in the active power filter and the high performance adjustable speed drives. [33] provided a fuzzy logic predicted current control in order to provide energy with low harmonics and high power factor. [34] presented an improved predictive current controller to minimize the current error and give fast response for over-current protection by using a dual-timer and software PLL. [35] implemented a deadbeat control with a FPGA. [36] showed a robust predictive current control strategy. [37] proposed a multirate estimator for predictive control to compensate time delay. [38] suggested a model predictive control scheme based on an improved model. However, it requires the measurement of the load voltage, V_{ac} . Therefore, the noise sensitivity of the predictive controller is higher than the PI controller.

Hysteresis control provides extremely fast response and runs at variable switching frequency. [39] proposed a dead-beat adaptive hysteresis current control for simple implementation and less circuit components. A hysteresis controller was designed with MPPT neural networks at PV application [40]. [41-42] implemented a single-band hysteresis current control for robust current regulation. [43] suggested a constant frequency hysteresis current control with modified hysteresis band by prediction. Due to the variable switching frequency, proper filtering of the high-frequency components of voltage and current is an issue. Due to the non-linear control approach, the conventional feedback analysis method can not be applied.

Sliding mode control has been proposed in a power conditioning system based on variable structure control [44]. Sliding mode control can be applied to a buck-based sinusoidal generator [45]. [46] suggested a fixed-frequency quasi-sliding control algorithm. [47-48] used a sliding mode control for the grid-tie inverter applications. [49] designed an adaptive total sliding mode control for avoiding uncertainties during reaching phase. As a non-linear control approach, it has good dynamic response and robustness. However, it requires modern control theory knowledge and is difficult to show numerical data of the stability by applying conventional feedback method.

1.4 Research Motivation

The preceding section review makes clear that current control of the grid-tie inverter requires high performance capability in order to track a sinusoidal ac current reference and robust enough to prevent the disturbance of the grid voltage. So far, it has been proposed to combine either proportionl controller or a feedforward term with new controllers. PCS requires a seamless utility grid connection, with minor steady-state error and precise power control. However, there has not been much analysis done in the frequency domain for the grid voltage. The ability to control active and reactive power will be helpful in smart grid applications.

1.5 Dissertation Outline and Major Results

The dissertation includes the four relative research topics based on the proposed modeling approach, dynamic analysis, and improvement of the control structure of the single-phase utility-grid tie inverter controller design.

In chapter 2, a current loop control with admittance compensation for a single-phase grid-tie fuel cell power conditioning system will be proposed. The admittance compensator eliminates the effects of the grid voltage on either the inverter system or the controller design. Transfer functions of a single-phase grid-tie inverter are derived and fully analyzed. This method allows for current control design without considering the disturbance of the grid voltage. With this method, even in the light load condition, the grid-tie inverter can provide power to the utility grid.

In chapter 3, admittance compensation in a current loop control for a grid-tie LCL fuel cell inverter will be proposed. To improve steady-state operation, the quasi-proportional-resonant controller (QPR) was adopted with an admittance compensator. Thru zero power command can be achieved with the proposed control method. To maximize usability, LCL-filter based single-phase inverter was designed, the transfer functions of the controller were derived, and the QPR controller was explained in the frequency domain. From zero power to full power, the proposed system properly provides active power.

In chapter 4, a wide range and precise active and reactive power flow controller for the solid oxide fuel cell power conditioning system will be proposed. Active power flow control and reactive power flow control can be obtained with three controller combinations: the admittance compensator, the quasi-proportional resonant controller, and the scalar controller.

In chapter 5, versatile utilization of three half-bridge single-phase grid-tie inverters will be proposed. The proposed control scheme can provide power from renewable energy sources both balanced grid voltage source condition and unbalance grid voltage source condition. Modeling and control for the half-bridge single-phase grid-tie inverter will be derived and explained.

Chapter 6 will give a summary and contributions of this dissertation and suggest future works, which can be expanded to the other applications for renewable energy power conditioning systems.

Chapter 2 Current loop control with admittance compensation for a single-phase grid-tie fuel cell power conditioning system

2.1 Introduction

Fuel cell outputs tend to have slow time constant due to its balance of plant (BOP) controller, and thus it is more suitable for a grid-tie system where the load dynamic can be managed with slow current ramps. The fuel cell power conditioning output, however, suffers from steady-state error as seen in most single-phase inverters. Major cause of the inverter output steady-state error has long been identified as insufficient controller loop gain at the fundamental frequency such as 50 Hz or 60 Hz. Additionally, the grid-tie inverter output presents noticeable harmonic contents that have also been identified as insufficiency controller loop gains at the harmonic frequencies.

Past work [17], [19-21], [53] suggested that using proportional resonant (PR) controllers at the fundamental or selected harmonic frequencies can solve the steady-state error and eliminate the major harmonic contents. It is also possible to solve the steady-state error with dq-transformation that allows the real power and reactive power components to have an infinite controller loop gain [29-30], and thus eliminating the steady-state error. The major cause of the inverter output steady state error has been further explored in this paper. The complete circuit model analysis indicates that it comes not only from the controller loop gain, but also from an admittance path, which induces an undesirable current by the grid voltage. The desired inverter output current should be controlled by the duty cycle of the pulse width modulation (PWM), not by the external sources. The fact that the admittance path allows the grid voltage to induce an

undesirable current will eventually cause a severe impact to the waveform quality and steady-state error. In a power factor correction (PFC) boost converter, the admittance path was found to have major impact on the waveform distortion due to its leading phase with respect to the line current [55-56]. For the grid-tie inverter case, the situation is similar, except that the leading phase becomes lagging phase or out of phase with respect to the compensator design, because the admittance induced current is against the PWM output current. The impact of such a lagging phase current or an out of phase current is a severe steady-state error.

It is suggested in [55-56] that the leading phase current distortion can be compensated with a feed-forward controller which cancels the admittance induced current. The same feed-forward admittance path compensation concept is employed in this paper for the grid-tie inverter current loop compensation. Dynamic model of the current loop controller for a fuel cell based power conditioning system is derived with the complete inverter control system represented by two admittance paths. The desirable path is duty cycle to the output current, and the undesirable path is grid voltage to the output current. Two compensation methods are suggested in this paper for the undesirable admittance cancellation. The complete inverter with and without compensation is then simulated to show the effectiveness of the suggested compensation methods. With successful demonstration of the simulation result, a DSP-based controller is then implemented for a 5 kW solid oxide fuel cell power conditioning system. Both simulation and experimental results indicate that even without the PR controller or dq-transformation approach, the steady-state error can be largely reduced with the proposed admittance compensation method.

2.2 Grid-Tie Inverter Control System Modeling

The fuel cell power conditioning system (PCS) requires that the inverter output be controlled by the fuel cell BOP controller. Fig. 2.1 shows the control system of the inverter part of the entire fuel cell PCS. A dotted line indicates the link between the fuel cell and the inverter power command input, P_{ref} , which is then translated into the current command input, i_{ref} , by multiplying scaling factor, k_x and synchronization signal, $\cos(\omega t)$ produced by the digital phase lock loop (PLL). The current loop controller $G_i(s)$ is designed to compensate the error between i_{ref} and the feedback sensed current, i_{sense} . The output of the current loop controller is the duty cycle control signal, v_d , which is typically a sinusoidal signal. By feeding $v_d(t)$ signal to the PWM block, the output is gating signal, d . The inverter power circuit output needs a filter inductor, L_f to smooth the current and a solid state relay (SSR) to make grid interconnection. The utility source voltage v_g contains a source inductance L_g , thus the actual grid-tie voltage seen by the inverter is the voltage between L_f and L_g , or v_{ac} . Both output current i_{ac} and interconnect voltage v_{ac} are fed back to DSP through conditioning circuit and scaling. The v_{ac} waveform contains a large switching ripple with magnitude proportional to the ratio of L_g and L_f . Larger L_f allows smaller voltage ripple, which, however, can be filtered easily without significant delay. The filtered and sensed voltage, v_{sense} , is to produce the synchronization signal $\cos(\omega t)$ through PLL and look-up table.

Fig. 2.2 represents the inverter control diagram using transfer function blocks: G_{iv} and G_{id} — power stage transfer functions, G_i — current loop compensator, F_m — PWM gain, $H_i(s)$ — current sensor gain, $k_x P_{ref}$ — current reference gain.

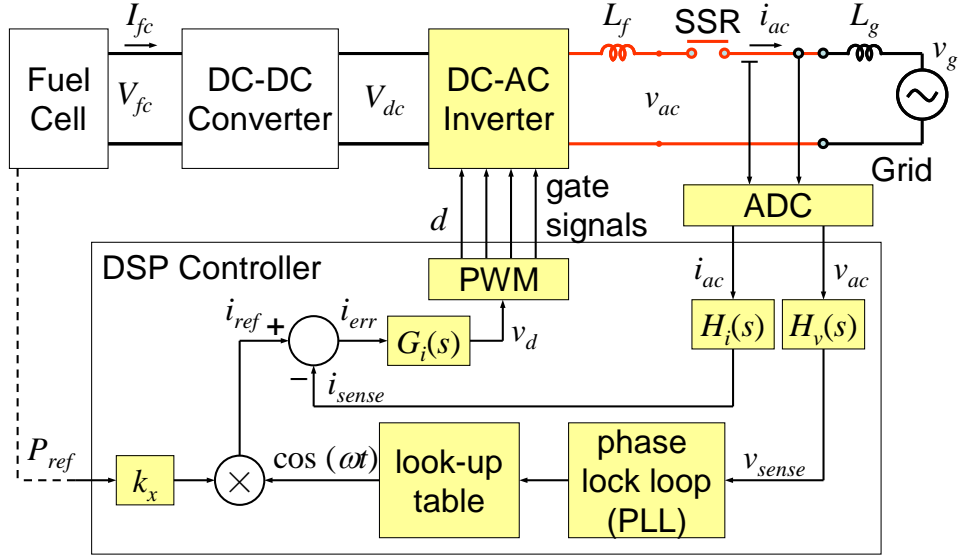


Fig. 2.1 Inverter control system of a fuel cell PCS

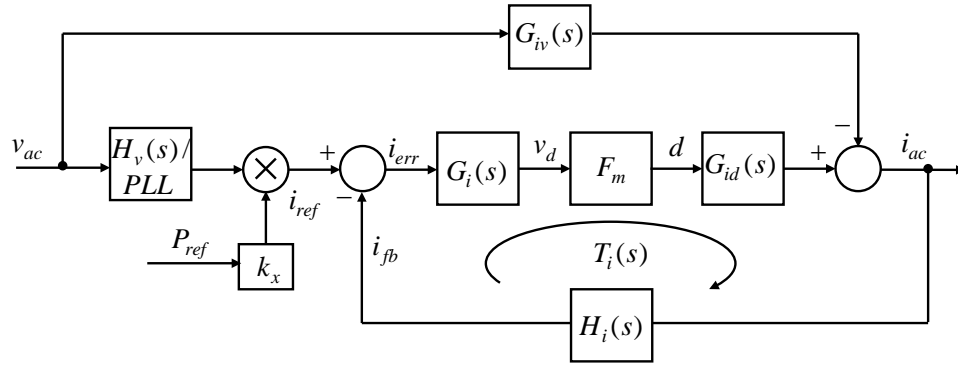


Fig. 2.2 Inverter control diagram using transfer functions

Using the average inverter output voltage dV_{dc} , the transfer function blocks can be derived in (2-1).

$$i_{ac} = G_{id}(s)d - G_{iv}(s)v_{ac} \quad (2-1)$$

where $G_{id}(s) = \frac{V_{dc}}{r + sL_f}$ and $G_{iv}(s) = \frac{1}{r + sL_f}$.

The overall equivalent admittance can be represented in (2-2), or in (2-3)

$$Y(s) = \frac{i_{ac}(s)}{v_{ac}(s)} = \frac{G_{id}(s)F_m H_i G_i(s)}{1+T_i} k_x P_{ref} H_v - \frac{G_{iv}(s)}{1+T_i(s)} \quad (2-2)$$

$$Y(s) = T_{icl} \cdot k_x P_{ref} H_v - G_{ivcl} \quad (2-3)$$

where $T_i = G_{id}F_m H_i G_i$, and $T_{icl} = G_{id}F_m G_i / (1+T_i)$. Defining $Y(s) = Y_1(s) + Y_2(s)$ yields $Y_1(s) = T_{icl} k_x P_{ref} H_v$, and $Y_2(s) = -G_{ivcl}$. The first admittance term Y_1 is the closed-loop current reference-to-current transfer function (current reference term), which provides desired input admittance magnitude with zero phase below crossover frequency of the loop gain T_i . The second admittance term Y_2 is the closed-loop voltage-to-current transfer function (voltage term).

If $G_i(s)$ is traditional PI compensator in (2-4), then $Y_1(s)$ and $Y_2(s)$ can be derived in (2-5) and (2-6), respectively. Y_2 becomes a 90° lagging phase below the crossover frequency.

$$G_i(s) = \frac{\omega_i(1 + \frac{s}{\omega_z})}{s(1 + \frac{s}{\omega_p})} \quad (2-4)$$

$$Y_1(s) = P_{ref} k_x H_v \quad (2-5)$$

$$Y_2(s) = -\frac{G_{iv}(s)}{1+T_i(s)} = \frac{-s}{H_i F_m V_{dc} \omega_i (1 + \frac{s}{\omega_z})} \quad (2-6)$$

The admittance plot at 10% power command with PI compensator for $G_i(s)$ in frequency domain can be shown in Fig. 2.3. At 60 Hz, Y_1 is in phase with v_{ac} , and Y_2 has a 90° phase lag. Note that the current induced in the Y_2 path needs to be multiplied with V_{dc} , and thus the resulting current will exceed 0 dB, which is noticeable even at the maximum power command condition. At low power command, the current induced in Y_2 will eventually exceed that in Y_1 , and thus the impact is very significant. Because Y_2 path current reduces the desired current, the resulting

steady-state output will be less than the command input, and the situation gets worse at lighter load conditions.

If $G_i(s)$ is a double-pole-double-zero lead-lag compensator shown in (2-7), then $Y_1(s)$ and $Y_2(s)$ can be derived in (2-8) and (2-9), respectively. Y_2 becomes a 180° out of phase below the crossover frequency in (2-9).

$$G_i(s) = \frac{\omega_i \left(1 + \frac{s}{\omega_z}\right)^2}{\left(1 + \frac{s}{\omega_p}\right)^2} \quad (2-7)$$

$$Y_1(s) = P_{ref} k_x H_v \quad (2-8)$$

$$Y_2(s) = -\frac{G_{iv}(s)}{1 + T_i(s)} = -\frac{1}{H_i F_m V_{dc} \omega_i \left(1 + \frac{s}{\omega_z}\right)^2} \quad (2-9)$$

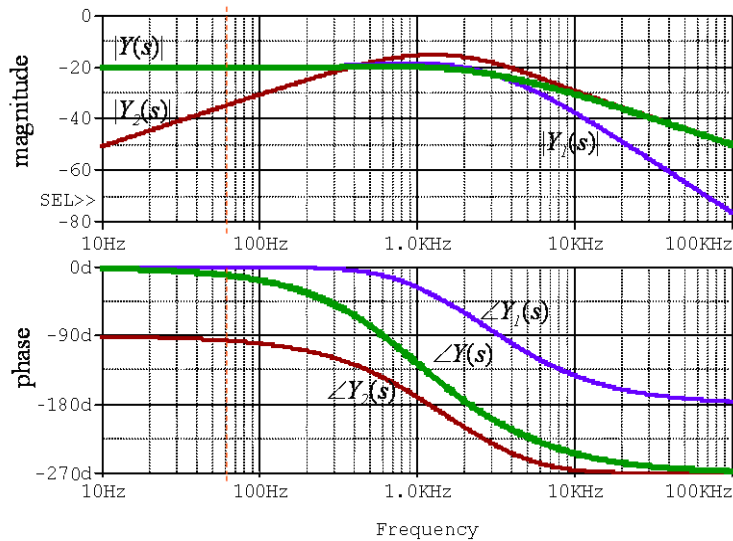


Fig. 2.3 Admittance Y plot in frequency domain with uncompensated term(Y_1) and lagging phase term(Y_2)

2.3 Elimination of the Lagging Phase Admittance Effect

The separation of two components of the admittance suggests natural ways of eliminating unwanted terms in $Y(s)$. Fig. 2.4 and Fig. 2.5 show two possibilities of adding admittance compensator. In Fig. 2.4, the admittance compensator is added at the summing junction before the current loop compensator, which can be implemented with either analog or digital controller. The compensator transfer function can be derived as shown in (2-10).

$$G_c(s) = -Y_2(s) = \frac{1}{H_v(s)V_{dc}F_m G_i(s)} \quad (2-10)$$

In Fig. 2.5, the admittance compensator is added after the current loop compensator, which can be easily implemented with digital controller, but not with conventional analog PWM chip. The compensator transfer function can be further simplified to (2-11) in this case.

$$G_c(s) = -Y_2(s) = \frac{1}{H_v(s)V_{dc}F_m} \quad (2-11)$$

Here the derivation assumes the overall loop gain has sufficiently high enough gain at low frequencies such as 50 or 60 Hz, which is by default required to lower the steady-state error.

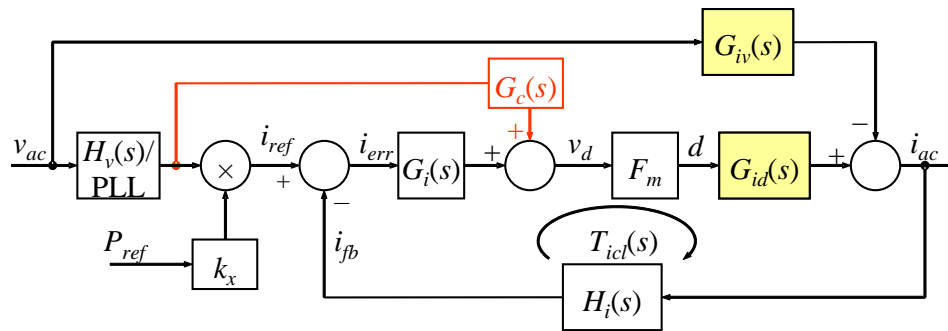


Fig. 2.4 Current reference correction method

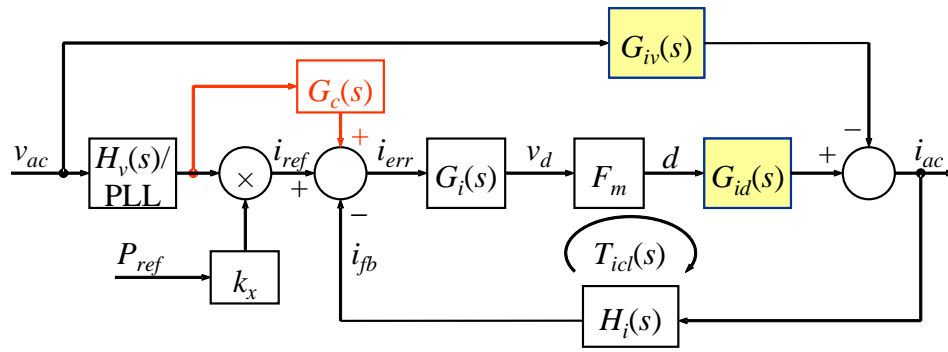


Fig. 2.5 Lagging phase admittance cancellation method

2.4 Current Loop Controller Design and Simulation

Since the duty cycle to output current transfer function contains a pole at zero frequency, adding an integrator will move the phase angle of the complete loop gain down to -180° . Thus the traditional PI or PID controller will have a great deal of difficulty to satisfy stability requirement unless a high-order zero is added. The PR control is a good approach to avoid the use of integrator while providing high gain at the fundamental frequency or harmonic frequencies. However, if the fundamental frequency is not matched with what the controller expecting value, then it can generate errors. In additions, to implement PR control algorithm with the fixed point digital signal processor takes long computation time. With the introduction of the admittance compensation, it is also possible to design the controller with lead-lag compensation simply just to provide high enough gains at low frequencies.

For the example system, the grid source inductance of the tested system was measured to be $L_g = 0.8$ mH. To avoid much noise on the sensing signal and to reduce the output current ripple as low as possible, the inverter filter inductance was selected to be $L_f = 4$ mH, which has an equivalent series resistance of 0.15Ω . The low-frequency pole is about 6 Hz, or one decade below 60 Hz. The current loop sensor has a gain of $H_i = 0.025$, a filter pole of 2 kHz in hardware, and a filter pole of 7.5 kHz in software. The voltage loop sensor has a gain of $H_v = 0.0025$ and a digital filter pole of 7.5 kHz in software. The PWM voltage gain can be determined from internal DSP timer computation as $F_m = 0.73$. By selecting the crossover frequency at 400 Hz and phase margin of 93° , a double-pole-double-zero lead-lag compensator shown in Fig. 2.6, can be designed controller with the result shown in (2-12).

$$G_i(s) = \frac{\omega_i \left(1 + \frac{s}{2\pi f_z}\right)^2}{\left(1 + \frac{s}{2\pi f_p}\right)^2} = \frac{1.37 \left(1 + \frac{s}{2\pi \cdot 1.95k}\right)^2}{\left(1 + \frac{s}{2\pi \cdot 7.8k}\right)^2} \quad (2-12)$$

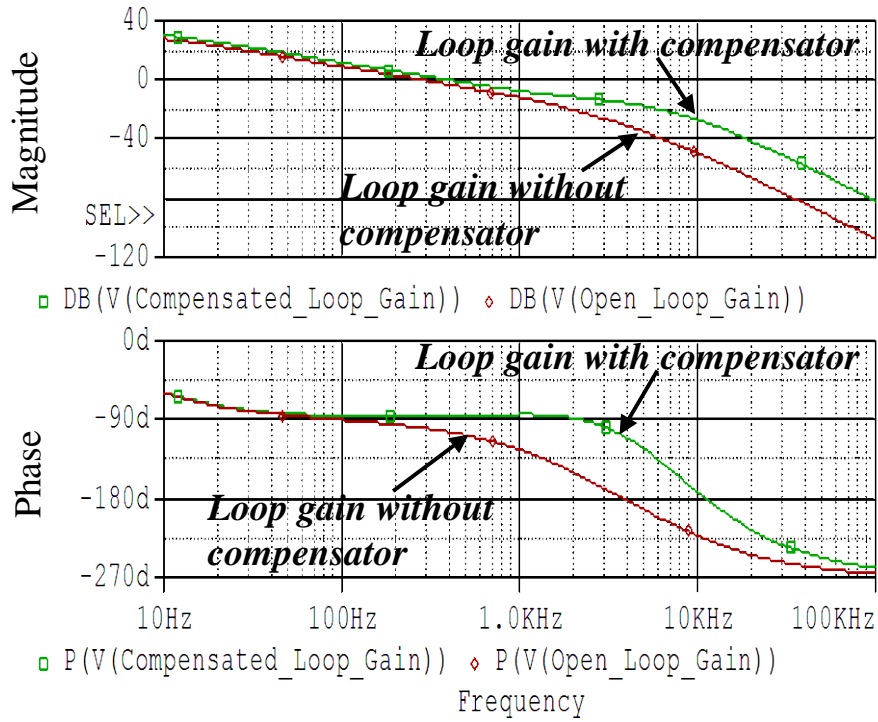


Fig. 2.6 Bode plot of the current loop gain

Base on the given parameters, the plant transfer functions can be expressed in (2-13) and (2-14), respectively.

$$G_{id}(s) = \frac{V_{dc}}{r + sL_f} = \frac{400}{0.15 + 4 \times 10^{-8} s} \quad (2-13)$$

$$G_{iv}(s) = \frac{1}{r + sL_f} = \frac{1}{0.15 + 4 \times 10^{-8} s} \quad (2-14)$$

Fig. 2.7~Fig. 2.10 compares time-domain simulation results with and without admittance compensation at two different load settings. Fig. 2.7 and Fig. 2.8 compare the power setting at 1.5 kW. Without admittance path compensation, the power actually flows back to the inverter, which will charge up the dc bus capacitor and result in catastrophe failure. Fig. 2.9 and Fig. 2.10 compare the power setting at 4 kW. Without admittance path compensation, the power sending to the inverter is 50 W.

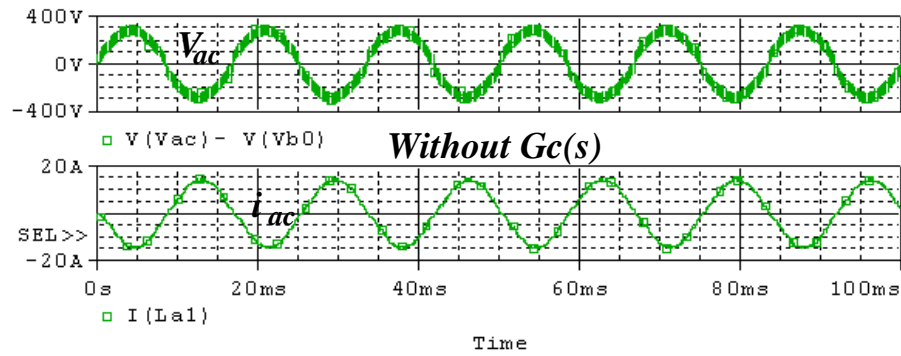


Fig. 2.7 Time-domain simulation results at $P_{ref}=1.5$ kW without $G_c(s)$ compensation

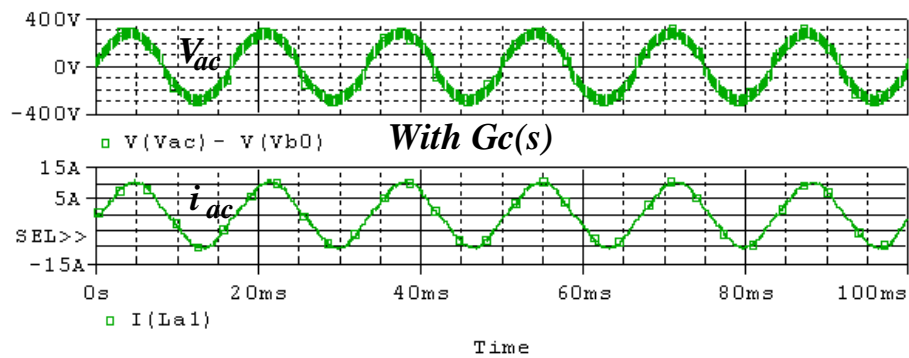


Fig. 2.8 Time-domain simulation results at $P_{ref}=1.5$ kW with $G_c(s)$ compensation

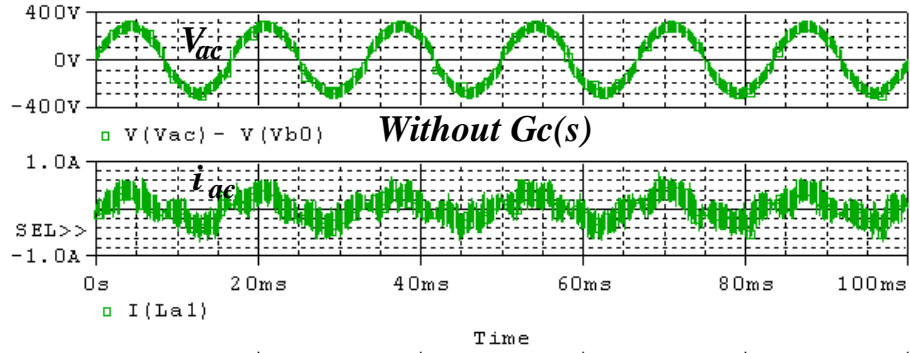


Fig. 2.9 Time-domain simulation results at $P_{ref}=4$ kW without $G_c(s)$ compensation

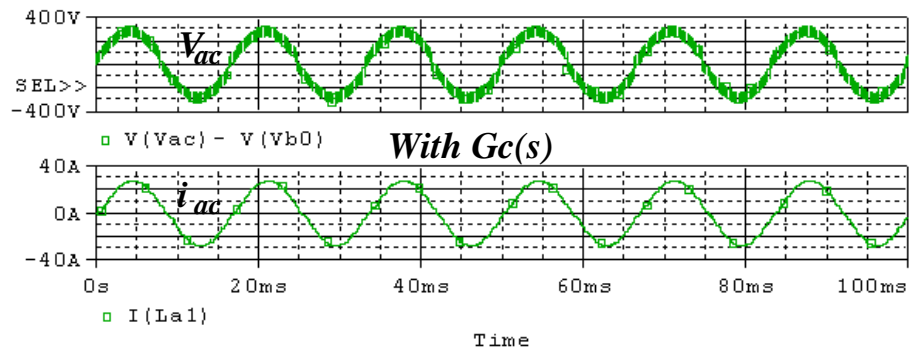


Fig. 2.10 Time-domain simulation results at $P_{ref}=4$ kW with $G_c(s)$ compensation

2.5 Experimental Verification

A PCS prototype that contains a dc-dc converter to boost the fuel cell voltage from 25 V to 400 V and a dc-ac inverter that produces 208 Vrms ac output for the grid connection is tested with a solid oxide fuel cell (SOFC) simulator which mimics an actual low-voltage SOFC that has a stack of 36 cells operating at 1000 °C. Fig. 2.11 shows test setup with the PCS prototype and associated instrumentation. A precision current shunt is used to calibrate the current measurement. The front panel of the case is open to show the DSP board.

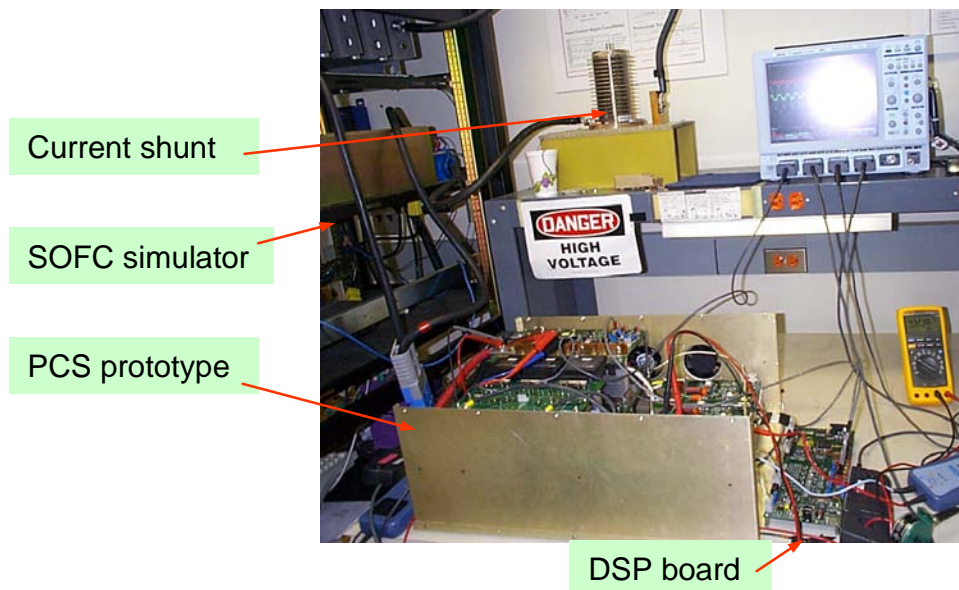


Fig. 2.11 PCS prototype test setup

If the grid tie inverter is designed in universal purpose, then it can be implemented in 208 Vrms or 110 Vrms. In conventional PLL design, the PI gain should be changed with respect to the peak voltage of utility grid. However, if the reference of the PLL is a unity magnitude, then PI gain is always constants. To synchronize the inverter current to the grid voltage, the software

phase-locked loop (SPLL) is used. Fig. 2.12 shows the block diagram of the SPLL. The orthogonal signal, $V_m \sin \theta$, can be generated from the v_{ac} or $V_m \cos \theta$, through passing the all pass filter [30].

The reference signal of the SPLL becomes $\cos \theta$ with a unity magnitude by dividing the sensed voltage signal with the peak magnitude of the grid voltage.

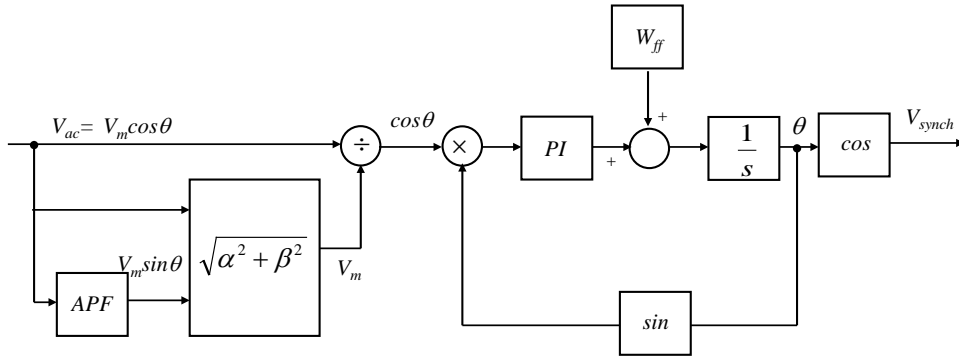


Fig. 2.12 Block diagram of the software phase locked loop structure

Fig. 2.13 shows v_{ac} and v_{synch} , which is the internal synchronizing signal. Here v_{synch} is obtained through the external digital to analog converter (DAC) circuit, which adds an extra time delay in addition to the DSP sampling time. Nevertheless, the output of SPLL does not show any appreciable delay and provides a pure sinusoidal signal to the controller that well synchronizes the grid voltage v_{ac} . The startup locking takes just a little over one fundamental cycle.

The main difference between photovoltaic (PV) power system and fuel cell power system is where the power command source comes from. The power command of PV system can be determined by the maximum power tracking algorithm.

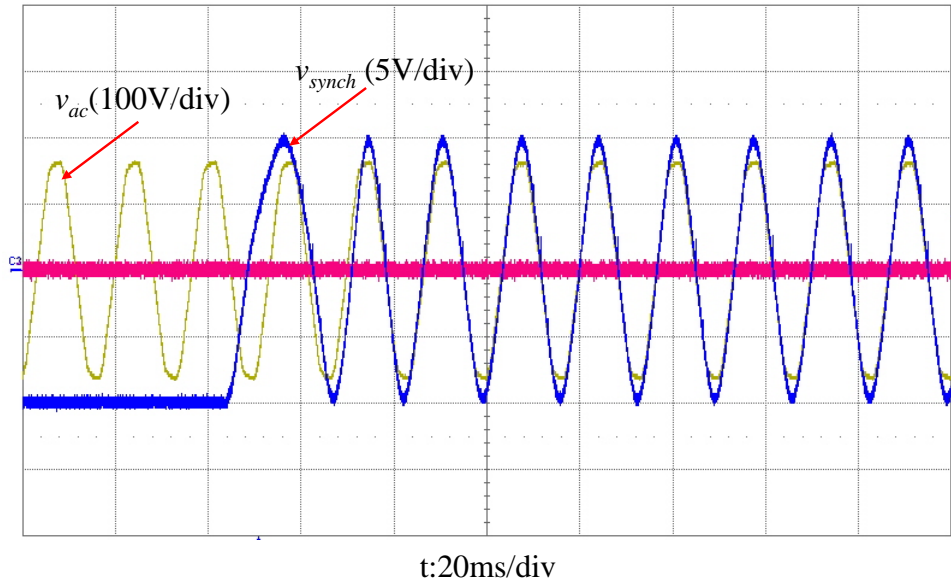


Fig. 2.13 Synchronization waveform of v_{ac} and v_{synch}

In fuel cell system, the power command can be determined by the fuel cell plant. The power command is provided by SOFC simulator from 0 to 10 V representing from 0 to 5 kW. Fig. 2.14 shows experimental results at 1.5-kW steady-state condition. Waveforms indicated that the fuel cell voltage $V_{fc} = 28$ V, fuel cell current $I_{fc} = 65$ A, output voltage $v_{ac} = 300$ Vpeak or 212 Vrms, and output current $i_{ac} = 10$ A peak or 7 Arms.

Fig. 2.15 shows experimental results at 4 kW steady-state condition. Waveforms indicated that the fuel cell voltage $V_{fc} = 25$ V, fuel cell current $I_{fc} = 167$ A, output voltage $v_{ac} = 300$ V peak or 212 V rms, and output current $i_{ac} = 26$ A peak.

Notice that the sensed voltage is highly corrupted by the noise, which contains electromagnetic interference (EMI) noise produced by the SOFC simulator and the inverter switching noise. However, the ac output current is fairly clean due to sufficiently large inductor in between.

It should also be noticed that without the proposed admittance compensation, the output

power would never reach 4 kW for the maximum setting of 5 kW.

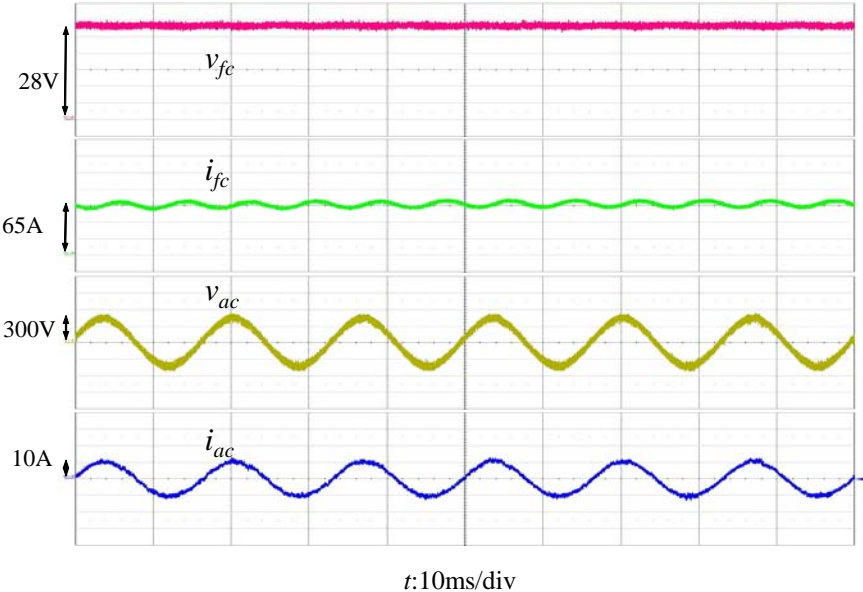


Fig. 2.14 Steady-state inverter operations at 1.5 kW condition

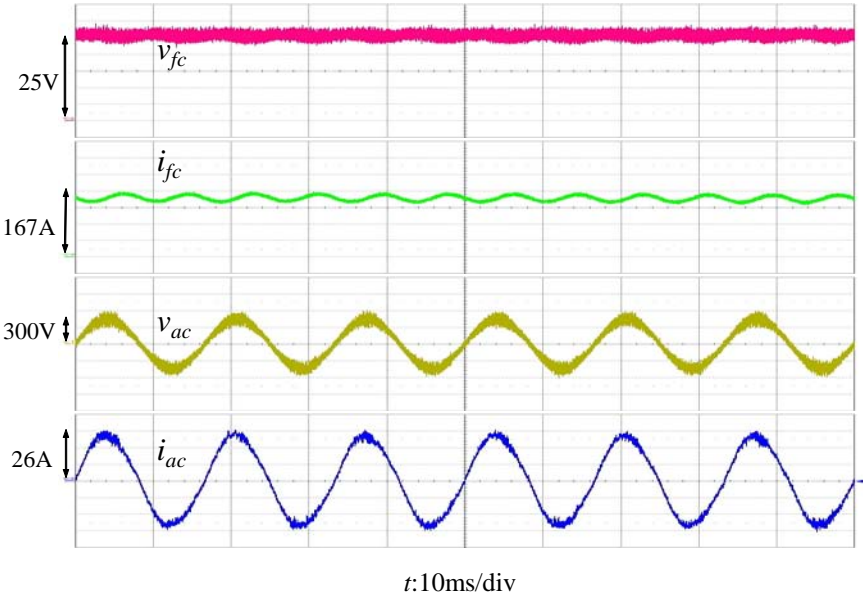


Fig. 2.15 Steady-state inverter operations at 4 kW condition

The proposed admittance compensation along with the lead-lag current loop controller can give a nearly matched power setting with the PCS efficiency of 94 %.

2.6 Conclusion

The admittance compensation method has been proposed and developed for a grid-tie single-phase fuel cell PCS. The current loop transfer function has been systematically derived with representations of conventional transfer function format and admittance terms for the sake of controller design and feed-forward compensation. A 5-kW grid-tie PCS example was given to show current loop controller design and admittance compensation. A second order lead-lag compensator is proposed to avoid low stability margin while maintaining sufficient gain at the fundamental frequency. The control loop gain deliberately sets a steady-state error that is closely related to the PCS loss so that the commanded power from fuel cell matches with the PCS input power, not the actual power sent to utility grid.

The proposed current loop controller and admittance compensation have been simulated, and the same parameters have been used for a DSP based PCS inverter controller. Simulation results indicate that without the admittance path compensation, the current loop controller output duty cycle is largely offset by the admittance path. At light load settings, the power flow may be erratically fed back to the inverter that can cause catastrophe failure. With admittance path compensation, the output power shows a steady-state offset that matches the design value. Experimental results well matched the mathematical design and simulation results. The dynamic power ramp-up and -down were also tested to show stable and consistent operation with the proposed controller design approach.

Chapter 3 Admittance compensation in current loop control for the grid-tie LCL Fuel Cell inverter

3.1 Introduction

A fuel cell system is known to have slow response with respect to load changes, especially high temperature fuel cells such as solid oxide fuel cell (SOFC) and molten carbonate fuel cell (MCFC). Thus the fuel cell inverter is more suitable for grid-tie connection applications in which the dynamic requirement can be demanded by a slow current ramp and controlled by the fuel cell balance of plant (BOP). The fuel cell power conditioning output, however, may see a current transient during start-up and a finite current flow even at the zero power command, which are undesirable conditions for the slow fuel cell systems. As identified in past papers [19-22], [29-30], [53], [57-62], the major reason of this finite-current-flow problem, or steady-state-error problem, is the lack of control loop gain at the fundamental frequency and harmonic frequencies.

The conventional proportional-integrator (PI) controller along with a feed-forward compensator has been proposed in grid-tie inverter application in [57-60], [63]. Feed-forward controller was designed to reduce the effect of the grid voltage [57], [59], [63] and to increase dynamic response [60]. A proportional resonant (PR) controller [19-22], [53], [62] having extremely high gain at the desired frequencies to reduce the amount of steady-state error is proposed. It has shown superior performance to that of PI controller [20], [22], [53]. This PR controller, however, has hardware implementation concerns including the limitation on finite gain at the desired frequencies and being prone to numerical errors, which may cause a negative power flow at start-up. Another way to solve this steady-state error problem is to use the single-

phase d-q frame transformation method [29-30], [57], [61-62], [64]. With d-q transformation, the error signal is regulated in dc quantity by an integrator to achieve infinite gain. This infinite dc gain can then be transformed back to fundamental frequency to eliminate steady-state error. However, all the frame transformations in feedback and control signals must be done within every sampling cycle which needs intensive computational effort.

By analyzing the transfer function of the complete inverter system, the main cause of the steady-state current error was found to be an unwanted current introduced by grid voltage through an undesired admittance path. The main purpose of grid-tie inverter is to send power to the grid, and the desired current should accurately reflect the command and be in phase with the output voltage. The undesired admittance path contributes a large current that is 180 degree phase shifted from the desired current flow. In a power factor correction (PFC) boost converter, the admittance path was found to have major impact on the waveform distortion due to its leading phase with respect to the line current [55], [64]. For the grid-tie inverter case, the situation is similar [64-65], except that the leading phase becomes lagging phase.

In [55], [64-66], it was found that the current leading phase current distortion can be compensated with a properly designed admittance compensator, which cancels the undesired admittance loop induced current. The same admittance path compensation concept is employed in this paper for the grid-tie inverter current loop compensation.

In this paper, the admittance compensator along with a quasi-resonant-proportional controller is adopted. The combination allows smooth start-up operation as well as elimination of the steady-state error over the entire load range. The design considerations of LCL filter such as component selections and feedback positions will be also described in this paper. The studied inverter system has been simulated with and without the admittance compensation during start-

up and steady-state operating conditions to verify of the proposed compensation method. A 5-kW solid oxide fuel cell power conditioning system (PCS) with digital signal processor (DSP)-based controller has been implemented to further confirm the effectiveness of the designed controller. Both simulation and experimental results suggest that the transient undershoot start-up problem can be avoided, and the zero-current command can be well controlled with the proposed admittance compensation method.

3.2 Grid-Tie Inverter Control System Modeling

Fig. 3.1 shows the control system of an LCL-based-filter fuel-cell power conditioning system. Fuel cell is to provide the power with low voltage and high current to the dc-dc converter. The dc-dc converter is to boost low voltage to proper dc link voltage, V_{dc} .

In this paper, grid-tie inverter is the main focus and is modeled with consideration that V_{dc} is constant because the dc-dc converter is controlled to keep V_{dc} constant [9-10]. The inverter output power command, P_{ref} , comes from fuel cell BOP and can be translated into a current command, i_{ref} , given the known grid voltage, v_g .

Unlike other state-of-the-art approaches that utilize the equivalent circuit of the LCL circuit and feed back either v_g-i_g , v_g-i_{ac} , or $v_{ac}-i_g$ pair for the control loop design, the proposed control design is to use the inverter side current i_{ac} and capacitor voltage v_{ac} as the feedback signals.

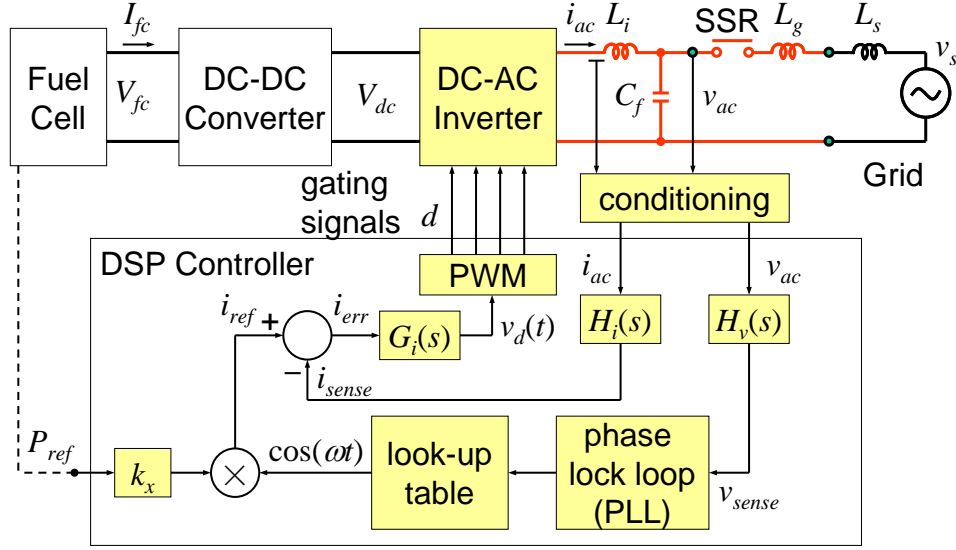


Fig. 3.1 Control system block diagram of an LCL-filter based fuel cell PCS inverter

Using the average inverter output voltage v_i which equals dV_{dc} , the current-loop transfer function can be derived in (3-1).

$$i_{ac} = G_{id}(s)d - G_{iv}(s)v_{ac} \quad (3-1)$$

where

$$G_{id}(s) = \frac{i_{ac}(s)}{d(s)} = \frac{V_{dc}}{sL_i} \quad (3-2)$$

and

$$G_{iv}(s) = \frac{i_{ac}(s)}{v_{ac}(s)} = \frac{1}{sL_i} \quad (3-3)$$

Notice the resistive components are neglected because they do not impact the controller design. Physically G_{id} represents the duty cycle to current transfer function, and G_{iv} represents

filter capacitor voltage to current transfer function. If the grid voltage v_g serves as the feedback, the above transfer functions will become

$$G_{id}(s) = \frac{i_{ac}(s)}{d(s)} = \frac{V_{dc}(1 + s^2 L_g C_f)}{s(L_i + L_g)(1 + s^2 (L_i // L_g) C_f)} \quad (3-4)$$

and

$$G_{iv}(s) = \frac{i_{ac}(s)}{v_g(s)} = \frac{1}{s(L_i + L_g)(1 + s^2 (L_i // L_g) C_f)} \quad (3-5)$$

If L_g and C_f are small enough to be negligible or if we use i_{ac} and v_{ac} as sensing and feedback signals, then (3-4) and (3-5) can be simplified to (3-2) and (3-3), respectively. Nevertheless, by using (3-2) and (3), the entire LCL current-loop transfer function can be designed using a simplified L-filter inverter, as shown in Fig. 3.2.

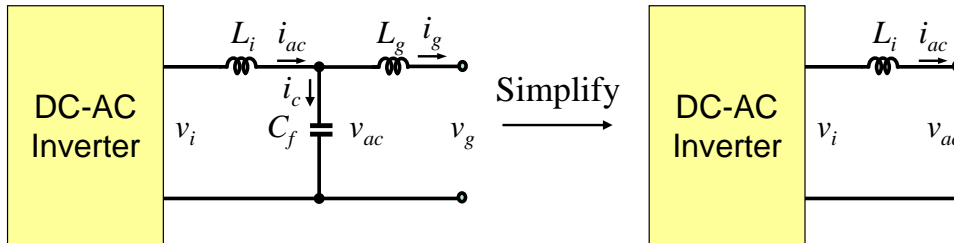


Fig. 3.2 Simplified inverter power circuit from LCL-filter to L-filter

Fig. 3.3 represents the inverter control diagram using transfer function blocks: G_{iv} – line-to-output transfer function, G_{id} – control-to-output transfer function, G_i – current loop compensator, F_m – PWM gain, $H_i(s)$ – current sensor gain, and k_x – current reference gain.

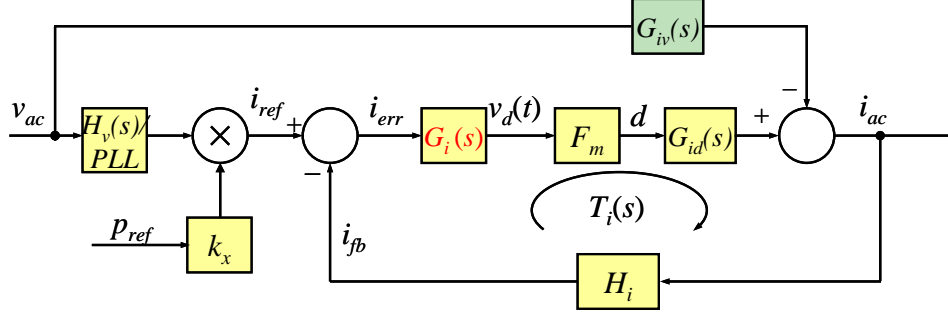


Fig. 3.3 L-filter inverter control diagram using transfer functions

The overall equivalent admittance can be represented in (3-6),

$$Y(s) = \frac{i_{ac}(s)}{v_{ac}(s)} = \frac{G_{id}(s)F_m G_i(s)}{1+T_i(s)} k_x P_{ref} H_v - \frac{G_{iv}(s)}{1+T_i(s)} \quad \text{or } Y(s) = T_{icl} \cdot k_x P_{ref} H_v - G_{ivcl} \quad (3-6)$$

where $T_i = G_{id}F_m H_i G_i$, and $T_{icl} = G_{id}F_m G_i / (1+T_i)$.

Defining $Y(s) = Y_1(s) + Y_2(s)$ yields $Y_1(s) = T_{icl} k_x P_{ref} H_v$, and $Y_2(s) = -G_{ivcl}$. The first admittance term, Y_1 , is the power command P_{ref} generated term, which provides desired output generated by the inverter. The second admittance term, Y_2 , is the closed-loop transfer function from v_{ac} to i_{ac} , calculated by assuming that the inverter output voltage v_i equals zero and the solid-state relay (SSR) is connected. Note that the current induced in the Y_2 path needs to be multiplied with v_{ac} , thus the resulting current will be rather large, which is noticeable even at the maximum power command condition. At low power command, the current induced in Y_2 will eventually exceed that in Y_1 , which the current in Y_2 path reduces the desired current, and the resulting steady state output will be less than the command input. The situation worsens at lighter load conditions [65].

3.3 Elimination of the Undesirable Admittance Effect

By observing the expression of $Y(s)$, the undesired admittance effect can be eliminated by adding one component, which is totally opposed to the second term in (3-4). As shown in Fig. 3.4 and Fig. 3.5, two possibilities to cancel the undesired admittance term can be observed. In Fig. 3.4, the admittance compensator is added at the summing junction before the current loop compensator. The compensator transfer function can be derived in (3-7).

$$G_c(s) = -Y_2(s) = \frac{1}{H_v(s)V_{dc}F_m G_i(s)} \quad (3-7)$$

The above derivation assumes the overall loop gain has sufficient gain at low frequencies (50 or 60 Hz), which is needed to lower the steady-state error. In Fig. 3.5, the admittance compensator is added after the current loop compensator, which can be expressed in (3-8).

$$G_c(s) = -Y_2(s) = \frac{1}{H_v(s)V_{dc}F_m} \quad (3-8)$$

Fig. 3.6 shows the block diagram of the admittance terms to explain the role of the admittance compensator. Differently with the conventional feed-forward control in [57-59], the admittance compensation is well defined and derived in order to reject the admittance disturbance induced from grid voltage, v_g . Equation (3-6) indicates that G_c can be implemented as a single value in DSP.

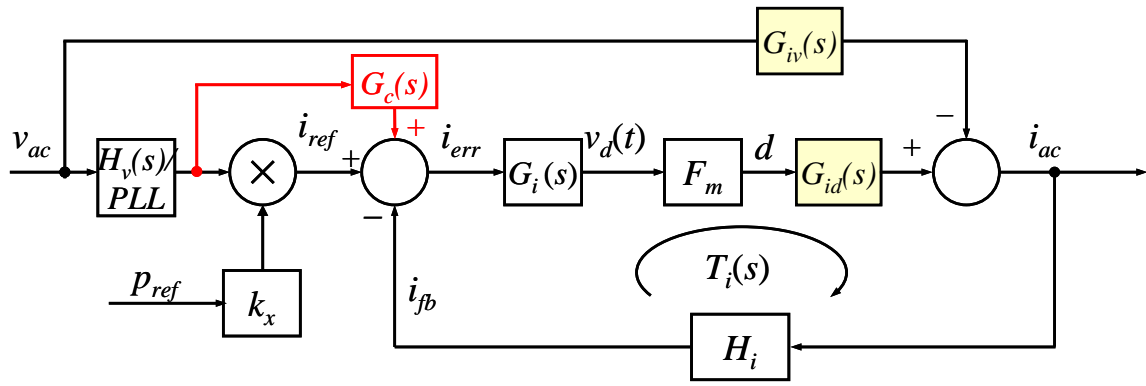


Fig. 3.4 Current reference correction method

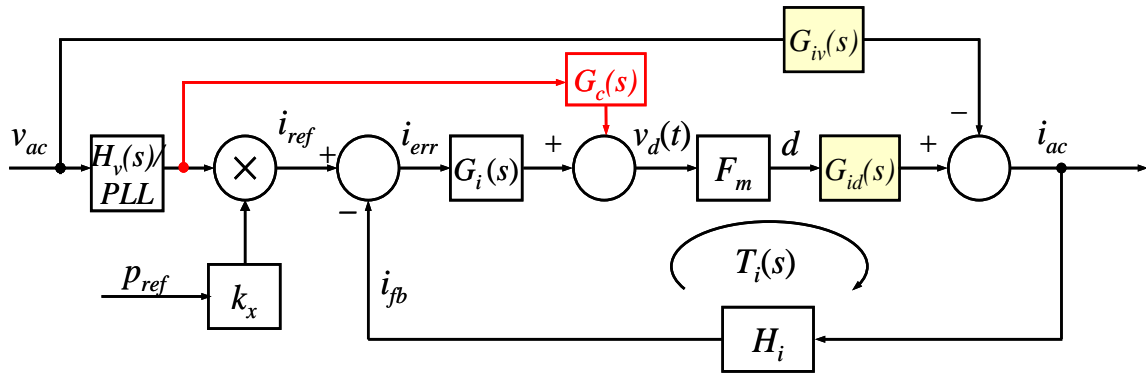


Fig. 3.5 Admittance compensation method

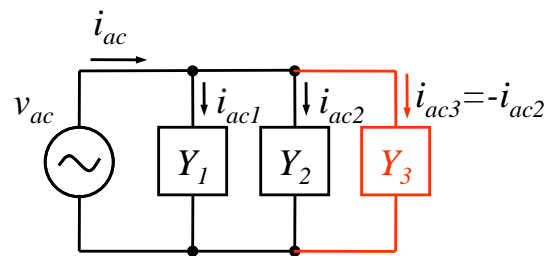


Fig. 3.6 Admittance terms block diagram

3.4 LCL Filter for the Grid-Tie Inverter

Generally, grid-tie applications require the designed inverter to meet the current THD within some ranges [18-19], [34]. Higher output current quality can be obtained if the output filter is configured as LCL type. The LCL filter configuration also allows the inverter to operate as a universal inverter. With configuration shown in Fig. 3.7, the inverter output is a standalone load. With configuration shown in Fig. 3.8, the output can be sent to the utility grid by engaging SSR, which is to provide switch turn on at zero crossing point to minimize voltage spike. Compared to the L-filter-based inverter, the LCL filter configuration allows more flexible inverter usage and also provides more attenuation of switching ripple for the grid side current. Some design considerations need to be taken into account when the LCL filter is utilized in the inverter system.

The first design consideration is the selection of components which can be determined by setting criteria on ripple current and filtering criteria. First of all, the inverter-side inductor L_i can be selected by the ripple current on the inductor. A larger inductance value allows a smaller inductor switching ripple; however, a large inductance value will increase the cost, volume and weight of the inductor. Thus, the choice of the inductor value is a trade-off between ripple current specification and cost. Second, the filter capacitor C_f is calculated by the cut-off frequency of the L_i - C_f second-order filter for the output voltage v_{ac} under standalone mode. The cut-off frequency of the L_i - C_f filter is suggested to be between 5 times less than switching frequency and 5 times higher than the fundamental frequency. Next, the grid side inductance L_g is selected by the cut-off frequency of the C_f - L_i second-order filter for the output current i_g of grid-tie connection.

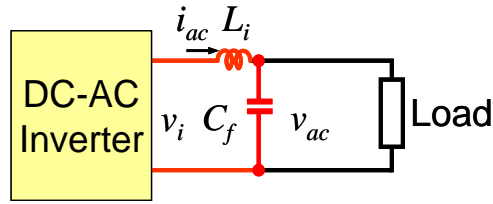


Fig. 3.7 Universal inverter for standalone mode

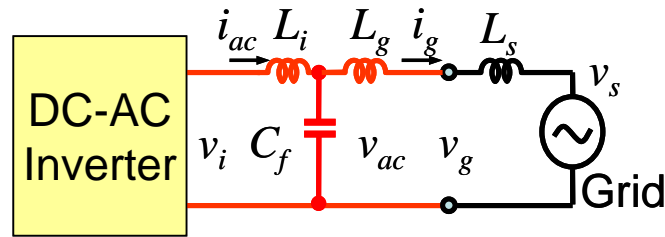


Fig. 3.8 Universal inverter for utility grid-tie mode

The second design consideration to implement the LCL filter for the inverter system is the position of feedback signals. For the simple L-filter based circuit, the control system employs the voltage right after inverter-side inductor L_i , v_{ac} as feedback voltage and the current through L_i , i_{ac} as feedback current. For the LCL filter case, four possible sensing signals i_{ac} , i_g , v_{ac} , and v_g and be used for feedback control. The proposed sensing combination is to use the voltage across filter capacitor C_f , v_{ac} and the current through L_i , i_{ac} as feedback signals. In this case, the L-filter-based admittance compensated current controller can be easily adapted. The current loop transfer function remains a first-order equation. More detailed analysis about LCL filter design and issues can be referred to [28], [62-63], [67-69].

Fig. 3.9 shows the block diagram of the complete LCL-filter based inverter control system. In a typical power circuit design, capacitor C_f is in the order of μF range, and the added 60-Hz current is in mA range. Thus, a small added leading phase current of this capacitor loop is

negligible and will not affect the first-order control system.

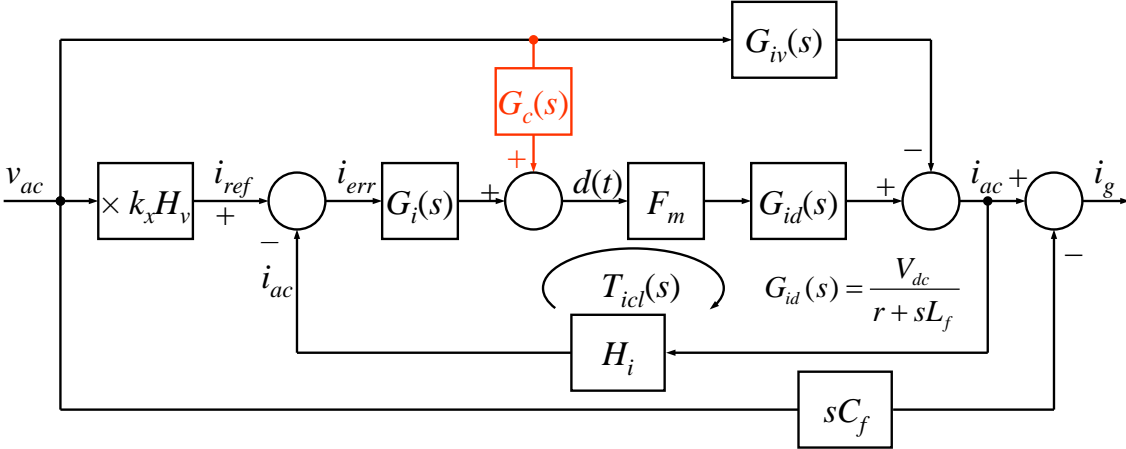


Fig. 3.9 Block diagram of the complete admittance compensated LCL-filter based grid-tie inverter

3.5 Current Loop Controller Design and Simulation

For the tested system, the grid source inductance was measured to be $L_s = 0.8$ mH. To avoid much noise effect on the sensing signal and to reduce the output current ripple as low as possible, the inverter-side inductance was selected to be $L_i = 3.6$ mH. The low-frequency pole of the inverter-side inductor, L_i is about 6.6 Hz, or about one decade below 60 Hz. The filter capacitance was chosen with $C_f = 2$ μ F, which in combination with L_i will result in a second-order voltage filter that has a 1.88 kHz cut-off frequency for standalone mode. The grid-side inductance was selected to be $L_g = 0.5$ mH, which has an equivalent series resistance of 0.01 Ω . The combination of C_f and L_g will constitute a second-order current filter at 5.03 kHz for grid-tie connection. The current loop sensor has a gain of $H_i = 0.01667$ and a double pole of 3 kHz from hardware low-pass filter. The voltage loop sensor has a gain of $H_v = 0.0025$ and a double pole of 2 kHz from hardware low-pass filter.

Because the duty-cycle-to-output current transfer function G_{id} shown in equation (3-1) contains a near-zero-frequency pole, the addition of a traditional I or PI controller to increase the loop gain will make the system unstable for lack of phase margin. The PR control is an alternative to avoid the use of an integrator while providing high gain at the fundamental frequency or harmonic frequencies. In order to reduce steady-state error at the fundamental frequency, a quasi-proportional-resonant controller [19] is selected below:

$$G_i(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad (9)$$

Here k_p is proportional gain, k_r is the resonant gain, and ω_c is equivalent bandwidth of the resonant controller. By choosing $k_p = 2.512$ with variations of ω_c and k_r values, the Bode diagram

of the current controller can be plotted on Fig. 3.10. In principle, the bandwidth ω_c needs to be as small as possible, but for digital implementation, it is quite difficult to realize a small ω_c . A large ω_c , however, will introduce a phase lag toward the crossover frequency and decrease the phase margin. As shown in the Fig. 3.10, with $\omega_c = 50$ and crossover frequency of 758 Hz, the phase margin is reduced by 18.5° . Equation (3-9) indicates that the controller gain at fundamental frequency can be increased by increasing either k_p or k_r values. However, the k_p gain can not be too high because it boosts the gain at all frequencies and will drop the system gain margin. As shown in the Fig. 3.10, the k_r gain also cannot be too high because it will reduce the phase margin at the desired cross-over frequency.

The PR controller implemented with TMS320F2808 DSP has been measured with a frequency response analyzer. Fig. 3.11 shows the frequency response measurement results with $k_p = 2.512$, $\omega_c = 10$, $k_r = 50$ under 20-kHz sampling frequency. The measured gain and phase results well match the simulated frequency response below the crossover frequency.

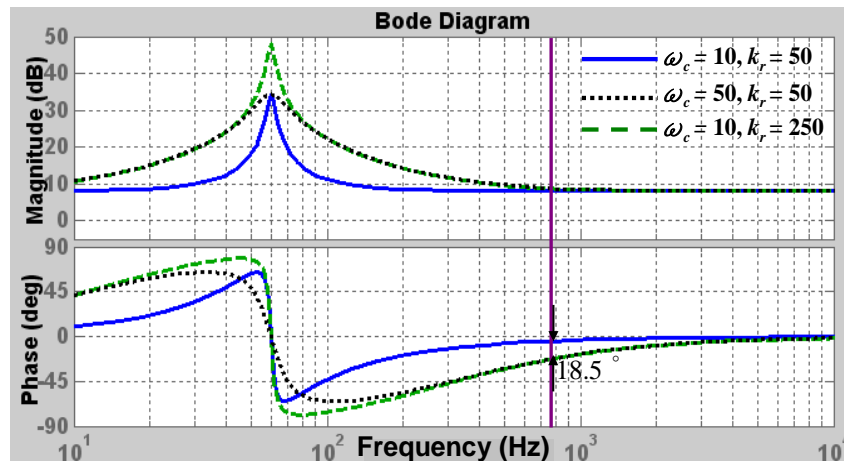


Fig. 3.10 Bode plot of PR controller with different ω_c and k_r values

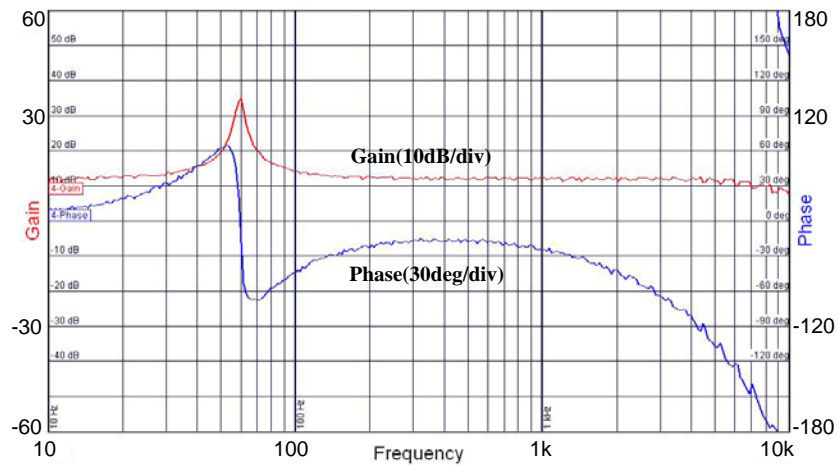


Fig. 3.11 Frequency response measurements with designed PR controller

Using the above current loop controller and system parameters, the open-loop gain $L(s)$ and compensated loop gain $T_i(s)$ are plotted in Fig. 3.12. The open-loop gain can be represented as $L(s) = F_m H_i G_{id}$ while the compensated loop gain is defined as $T_i(s) = G_i F_m H_i G_{id}$. As shown in the Bode plot, the designed controller boosts the loop gain to 50dB at the fundamental frequency. The crossover frequency and phase margin are 758 Hz and 48.3° , respectively.

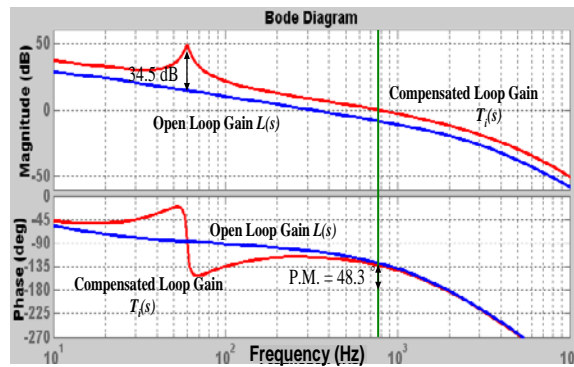


Fig. 3.12 Bode plot of the current loop gain with and without compensator

Fig. 3.13 and Fig. 3.14 show the comparison of the simulation results with and without admittance compensation at zero power command start-up in time domain. Without the admittance path compensation, power flows back to the inverter during first simulation cycle, which will cause the dc bus capacitor to be charged and may result in catastrophe failure. Furthermore, fuel cell does not want to draw any current at zero power command due to its slow response. The simulation result shows that the addition of the admittance compensation avoids current transient during system start-up and also draws near zero current at zero power command. Fig. 3.15 shows the simulation result with designed current controller and $G_c(s)$ compensation at peak current command $I_{ref, pk} = 20A$. With $G_c(s)$ compensation, the negative current, or disturbance term, caused by the plant can be totally compensated. Therefore, the grid-tie connection can be controlled like a simple feedback control without any disturbance term involved. The steady-state error can be estimated directly by the compensated loop gain. The simulation result shows that the current almost follows the 20A command with a negligible error, which is consistent with the Bode plot shown in Fig. 3.12, where the gain at 60Hz is near 50dB.

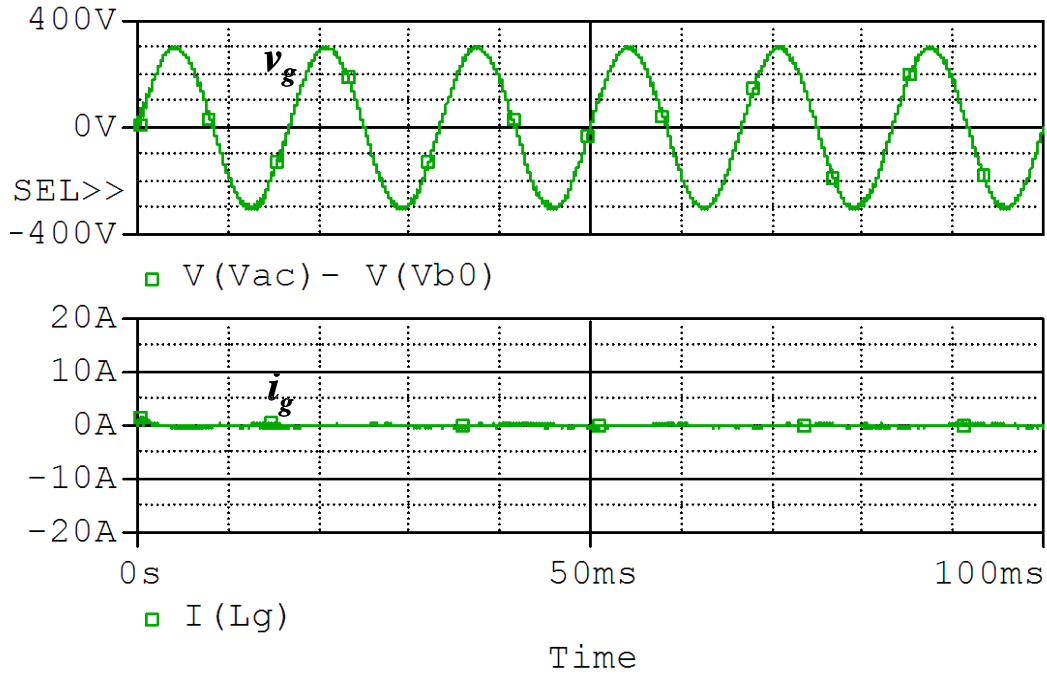


Fig. 3.13 Simulation results at zero power command start-up with admittance compensation

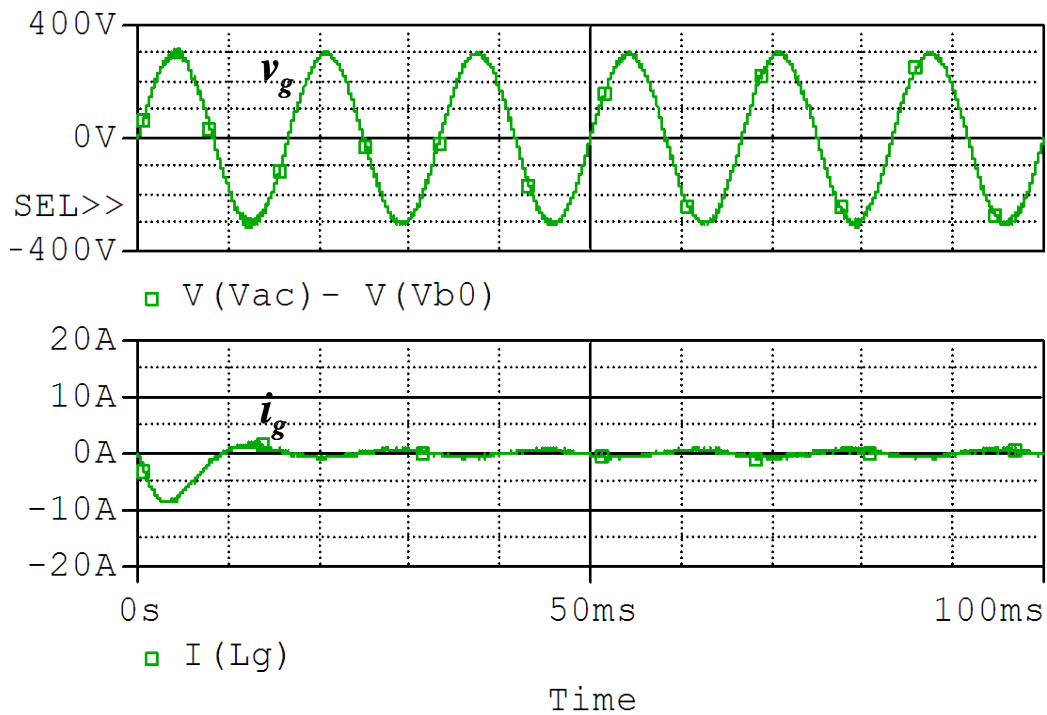


Fig. 3.14 Simulation results at zero power command start-up without admittance compensation

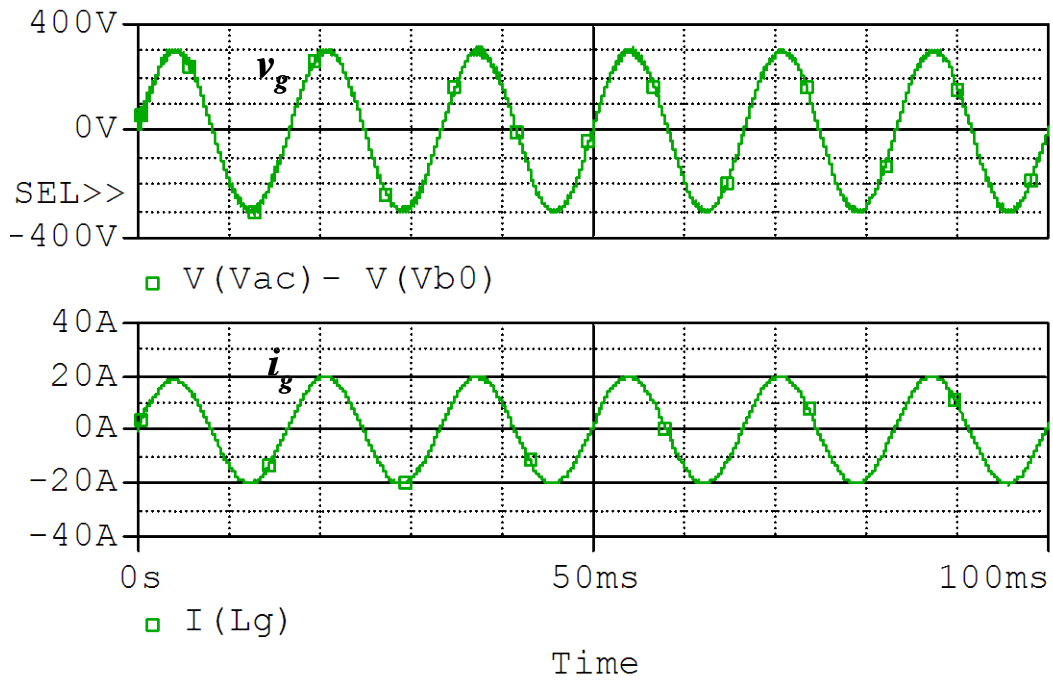


Fig. 3.15 Simulation results at peak current command $I_{ref, pk} = 20A$ with designed current controller and $G_c(s)$ compensation

3.6 Experimental Verification

A PCS prototype that contains a dc-dc converter to boost the fuel cell voltage to 400V and a dc-ac inverter that produces 208V ac output for the grid connection is tested with a solid oxide fuel cell (SOFC) simulator, which mimics an actual low-voltage SOFC that has a stack of 41 cells operating at 1000°C. Fig. 3.16 shows the polarization curve derived from an SOFC simulator [3]. The fuel cell voltage and current are represented with V_{fc} and I_{fc} , respectively. The studied system has a nominal 5-kW output and V_{fc} and I_{fc} in the neighborhood of 26V and 200A.

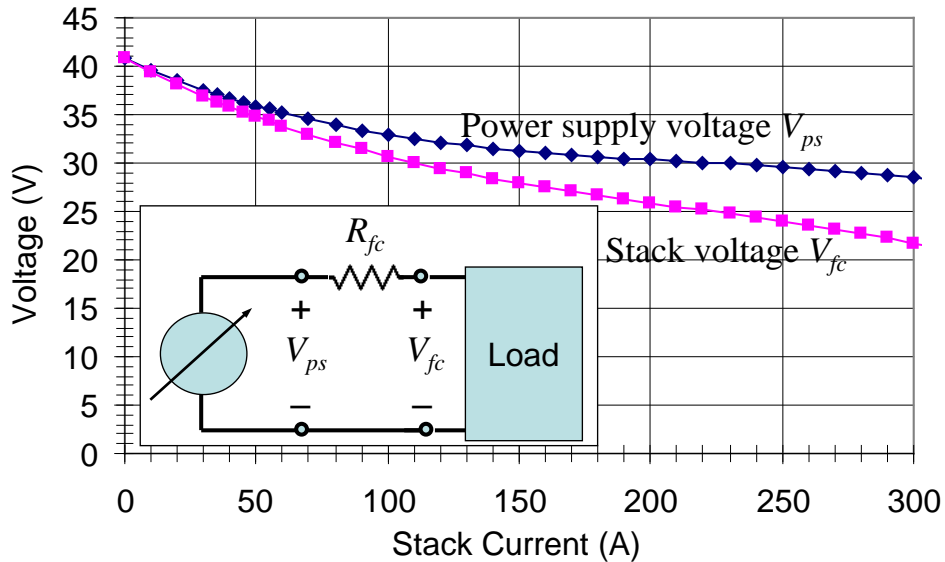


Fig. 3.16 V-I curve of the solid oxide fuel cell simulator

Fig. 3.17 shows the experimental results under the 3-kW standalone-mode condition. The test condition also includes a 500-Ω resistor at the dc-link to discharge the capacitor after experiment. The results indicate that the inverter voltage control loop works well in the standalone mode, where the output voltage and current are fairly clean. A small zero-crossing

distortion is observed due to dead time requirement and finite gains at the harmonic frequencies. The well-known 120-Hz ripple is also observed at the fuel cell current.

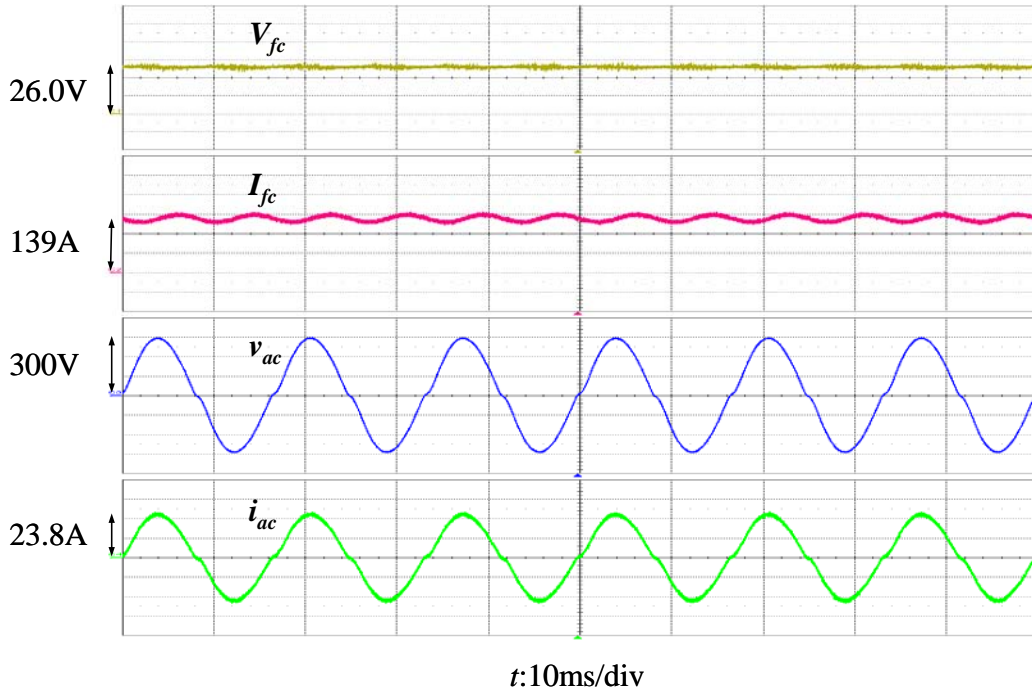


Fig. 3.17 Input and output waveforms of standalone mode operation under 3kW condition

Fig. 3.18 and Fig. 3.19 compare the experimental results without and with admittance compensation at zero power command start up. Without admittance compensation, shown in Fig. 3.18, the PR controller experiences a negative startup transient current and 100-W output power P_o . With admittance compensation, as shown in Fig. 3.19, the startup transient is eliminated, and zero power output is controlled as demanded. Although a 4-W output is observed, it can be considered as measurement error and will not cause any impact to fuel cell operation.

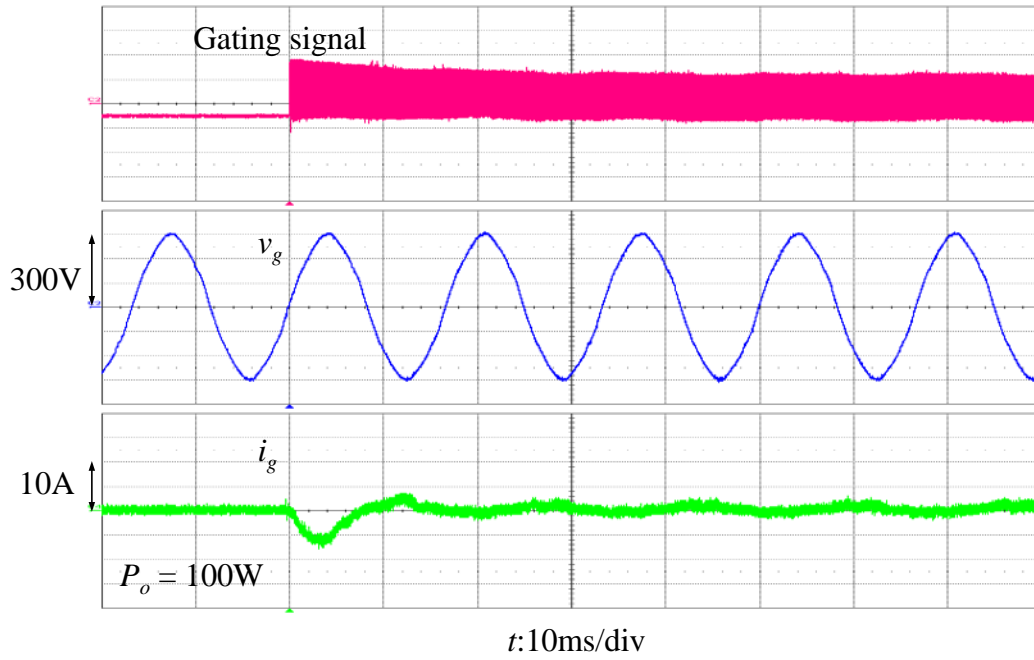


Fig. 3.18 Experimental results at zero power command start-up without compensation

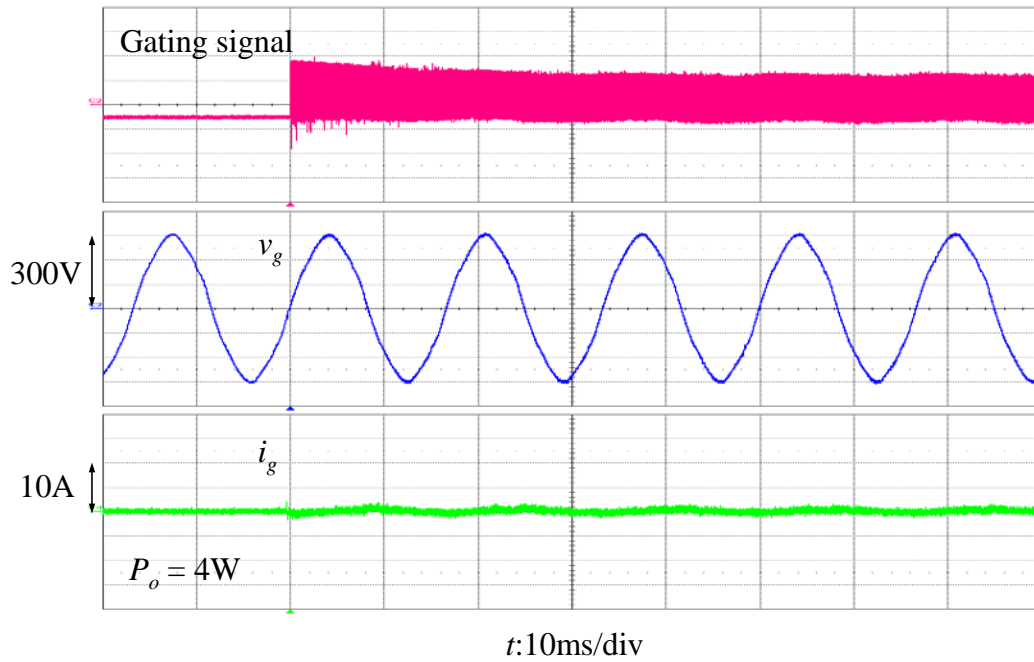


Fig. 3.19 Experimental results at zero power command start-up with compensation

Fig. 3.20 shows the experimental results under 20A peak current command grid-tie condition. Waveforms indicate that the output voltage and current are in phase. A small zero crossing distortion is observed again due to finite gain at harmonic frequencies and dead time effect. Nevertheless, the output current follows the command very well, which suggests the proposed admittance compensation along with QPR controller allows precise power control from zero to high power.

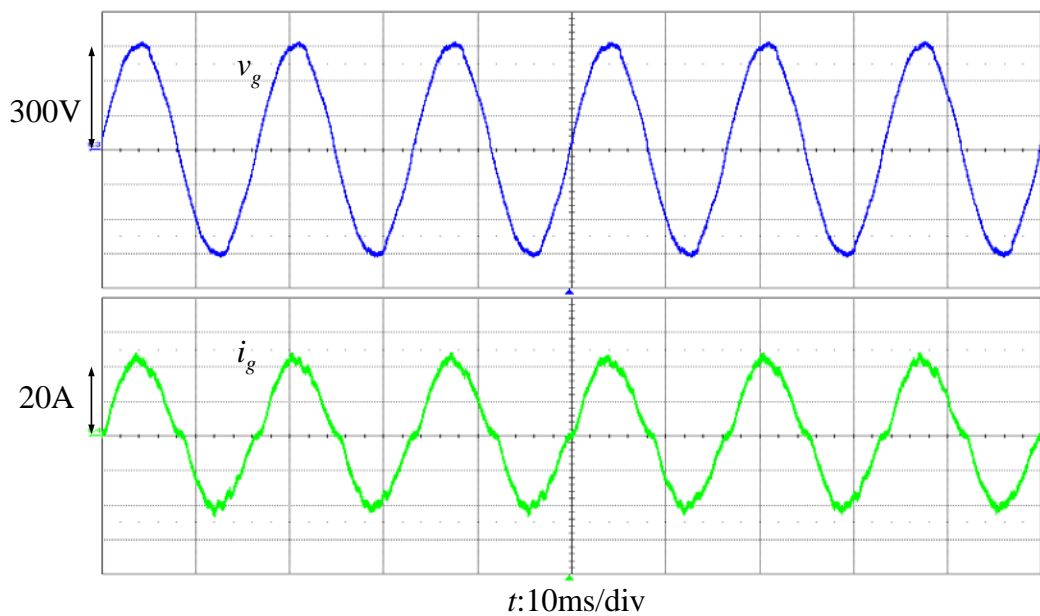


Fig. 3.20 Experimental results at peak current command $I_{ref, pk} = 20A$ with designed controller and $G_c(s)$ compensation

Fig. 3.21 and Fig. 3.22 show the experimental results under dynamic power ramping up from 2.5 kW to 4 kW and ramping down from 4kW to 3kW to show stable and consistent operation.

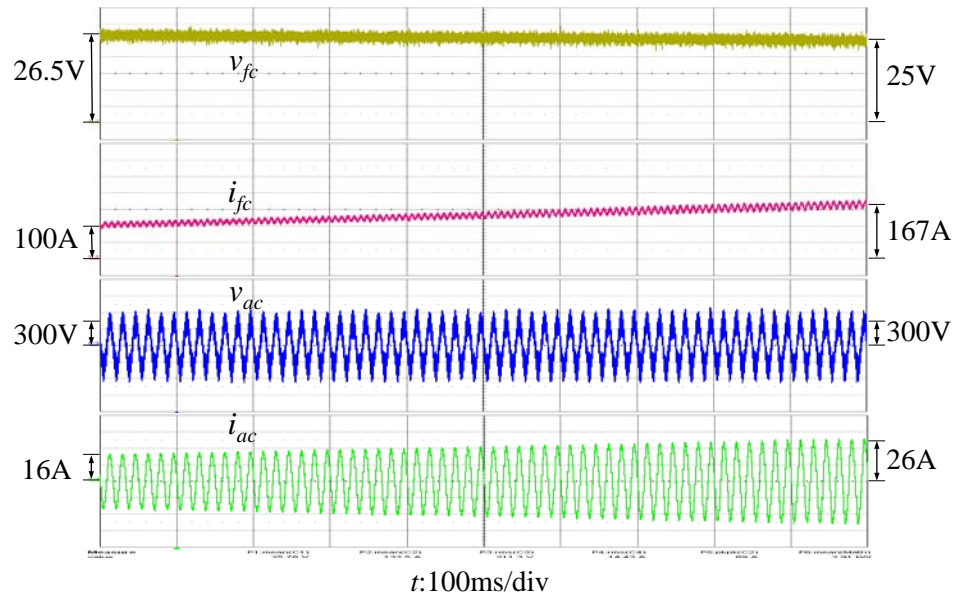


Fig. 3.21 Dynamic response of the power ramping up from 2.5 kW to 4 kW

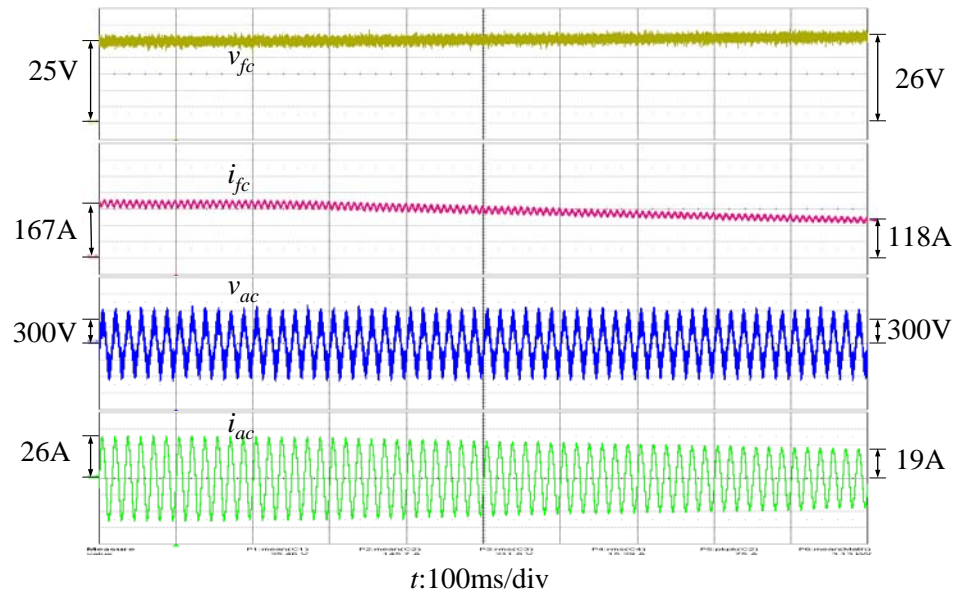


Fig. 3.22 Dynamic response of the power ramping down from 4 kW to 3 kW

Although the proposed controller design does not impact the inverter efficiency, the tested PCS efficiency profile with SOFC simulator test is reported here, as shown in Fig. 3.23, for reference. The dc-ac inverter efficiency η_{DC-AC} including output filter stage peaks at 98% at near full-load condition. This implies that without the output stage LC filter, the power stage dc-ac inverter efficiency approaches 99%. The dc-dc converter efficiency η_{DC-DC} peaks at 96.4% at about half load. The overall system efficiency η_{System} peaks at 94% in the load range from 70% to 90%. The test has been extended to 6kW, or 20% overload condition. The system efficiency maintains above 92% from 2kW to 6kW range.

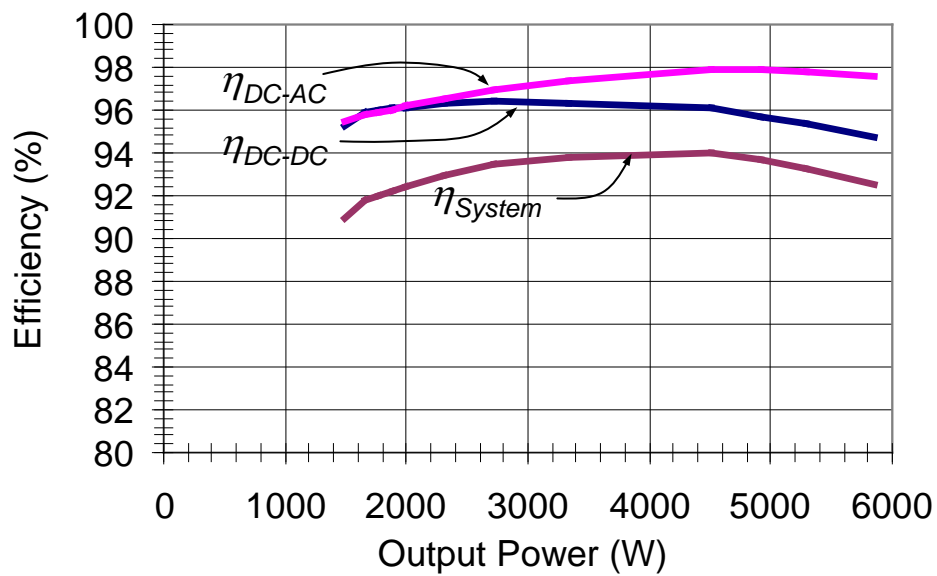


Fig. 3.23 PCS efficiency profiles under SOFC simulator test

3.7 Conclusion

The steady-state error problem in a fuel-cell power conditioning system has been studied through transfer function derivation. The current loop transfer function for an LCL grid-tie inverter has been derived with representation of admittance paths. The LCL filter circuit allows inverter operating in both standalone and grid-tie modes. By selecting proper sensor positions, the LCL-filter system can easily adopt the similar control diagram that is used in the L-based controller. This selection of sensor positions also allows first-order system transfer function to be used to simplify the controller design. Along with the admittance compensation, a quasi-proportional-resonant current controller has been designed to significantly increase the loop gain at the fundamental frequency, while maintaining enough phase margins to ensure closed-loop stability.

The proposed controller has been simulated and implemented in a DSP-based 5-kW PCS. Without admittance compensation, both simulation and experiment results show a significant startup transient and non-zero output at zero power command. The power flow in the first cycle is reversed, and the energy is erratically fed back to the inverter, which may cause over voltage in the dc link and result in catastrophic failure. With admittance compensation, a smooth startup was observed in both simulation and experiment results. The zero current command can be precisely achieved.

There are other benefits of applying the proposed admittance compensation technique. For example, in the control loop design, the disturbance term is totally cancelled, and the controller can be designed with the conventional feedback theory to ensure the stability margin. The added QPR controller further reduces the steady state error at the fundamental frequency. In the end,

the time-domain steady-state behavior can be precisely predicted by the frequency domain design.

Chapter 4 A wide range precise active and reactive power flow controller for a solid oxide fuel cell power conditioning system

4.1 Introduction

A grid-tie fuel cell power conditioning system (PCS) can be designed to have active and reactive power flow capability [70-72]. For solid oxide fuel cell (SOFC), such a power flow controller needs to be precise because SOFC has a slow time constant, and a mismatch of power flow may cause stability problem of its balance of plant (BOP) [73].

Past work [17], [19-20], [23], [53] suggested that using the proportional resonant (PR) controller can achieve precise active power flow control. It is also possible to use dq-transformation, PQ theory, or Hilbert transform to reduce the steady-state error by controlling the rotational frame active and reactive power components [30], [74-75].

In an active front end boost converter, the admittance path was found to be the major cause of the waveform distortion due to its leading phase with respect to the line current [55], [64]. By introducing feed-forward compensation, it is possible to cancel the admittance path induced current and therefore eliminate the waveform distortion. Such an admittance compensation technique also helps the precision control for the reactive power compensation in the active front end converter [64]. In [65-66], the admittance compensation technique was successfully applied to active power control in a grid-tie inverter. As indicated in [66], by combining the admittance compensation and quasi proportional resonant (QPR) controller, the active power flow can be precisely controlled from zero to full power.

The proposed power flow control approach has been analyzed with mathematical modeling. The current loop controller is then designed using frequency domain compensation technique and implemented with bilinear transformation for program coding. The entire controller is implemented with TMS320F2808 digital signal processor (DSP). A 5-kW SOFC PCS is used as the power stage platform, which includes a 5-kW dc-dc converter that converts 27 V to isolated 420 V and a 5-kW dc-ac inverter for the grid-tie power flow control. An SOFC simulator is used to emulate the fuel cell source. The entire PCS hardware prototype has been built and tested to show power flow operation from -5kVAr to $+5\text{kVAr}$ and to verify the simulation results.

4.2 Control System Modeling for the LCL Filter Based Grid-Tie Inverter

Fig. 4.1 shows the active and reactive power control system of the LCL-filter based grid-tie inverter as a part of the entire fuel cell PCS.

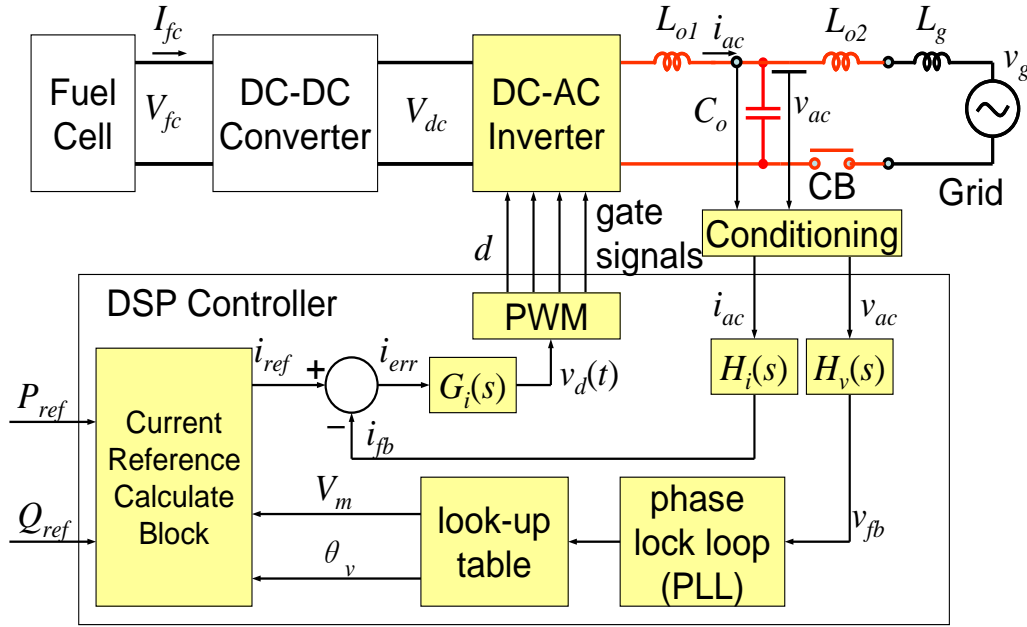


Fig. 4.1 Proposed inverter control system of a fuel cell PCS

The active power command, P_{ref} , which is commanded by the fuel cell BOP, and the reactive power command, Q_{ref} , which can be provided by the distributed generation (DG) control site, can be translated into the current command input, i_{ref} , by dividing the power command with the inverter output peak voltage, V_m , and subtracting the output voltage phase information, θ_v , produced by the digital PLL. The admittance compensator $G_c(s)$ is designed to reject a disturbance, which is due to the inverter output voltage, v_{ac} , acting on the power plant transfer function, $G_{iv}(s)$. The current loop controller $G_i(s)$ is designed to compensate the error between i_{ref} and the feedback sensed current, i_{fb} . The output of the current loop

controller is the duty cycle control signal, $v_d(t)$, which is typically a sinusoidal signal. By feeding $v_d(t)$ signal to the PWM block, the output is gating signal, d . The inverter power circuit output needs an LCL filter, $L_{o1}-C_o-L_{o2}$, to smooth the current and a circuit breaker (CB) to make grid interconnection. The utility source voltage, v_g , contains a source inductance L_g , thus the actual grid-tie voltage seen by the inverter is the voltage between L_{o2} and L_g , or v_{ac} . Both output current i_{ac} and interconnect voltage v_{ac} are fed back to DSP through conditioning circuit and scaling.

Fig. 4.2 represents the inverter control diagram using transfer function blocks: G_{iv} and G_{id} — power stage transfer functions, G_i – current loop compensator, F_m – PWM gain, $H_i(s)$ – current sensor gain.

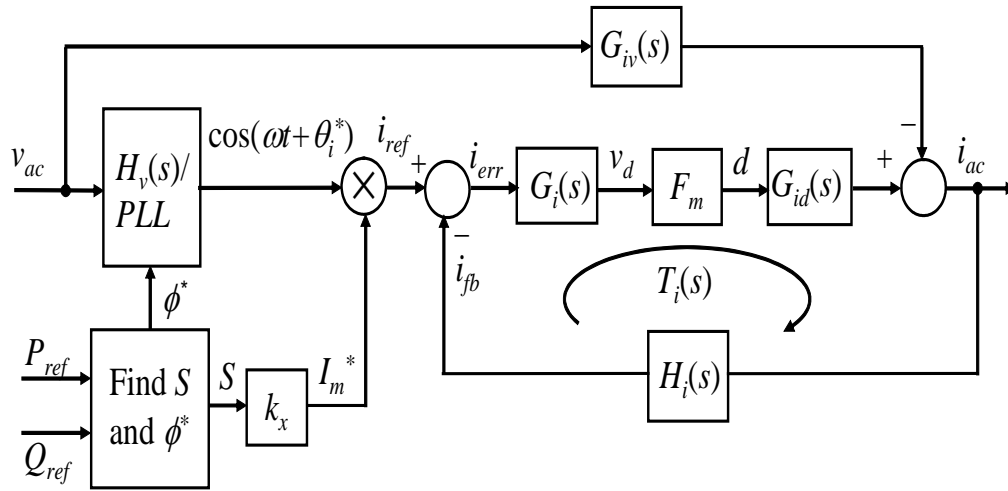


Fig. 4.2 Proposed inverter control diagram using transfer functions

The output current i_{ac} can be derived in (4-1) from Fig. 4.2

$$i_{ac}(s) = G_{id}(s)d(s) - G_{iv}(s)v_{ac}(s) \quad (4-1)$$

where $d(s)$ is the duty cycle, $G_{id}(s)$ is the duty cycle to output current transfer function, and, $G_{iv}(s)$ is the capacitor voltage to output current transfer function. These two transfer functions can be derived as follows.

$$G_{id}(s) = \frac{i_{ac}(s)}{d(s)} = \frac{V_{dc}}{r + sL_{01}} \quad (4-2)$$

$$G_{iv}(s) = \frac{i_{ac}(s)}{v_{ac}(s)} = \frac{1}{r + sL_{01}} \quad (4-3)$$

The overall equivalent admittance can be represented in (4-4),

$$i_{ac}(s) = v_{ac}(s)Y(s) = v_{ac}(s)Y_1(s) + v_{ac}(s)Y_2(s) \quad (4-4)$$

Here $Y_1(s)$ and $Y_2(s)$ represent two admittance terms and can be obtained as follows.

$$Y_1(s) = \frac{G_{id}(s)F_m H_i G_i(s)}{1 + T_i(s)} \cdot k_x S \cos(\omega t + \theta_i^*) \quad (4-5)$$

$$Y_2(s) = -\frac{G_{iv}(s)}{1 + T_i(s)} \quad (4-6)$$

where T_i is the current loop gain, or $T_i = G_{id}F_m H_i G_i$.

The reference active and reactive power can be used to calculate the apparent power reference S^* and power factor angle reference ϕ^* , as shown in (4-7) and (4-8).

$$S^* = \sqrt{P_{ref}^2 + Q_{ref}^2} \quad (4-7)$$

$$\phi^* = \angle \tan^{-1}(Q_{ref}/P_{ref}) \quad (4-8)$$

4.3 Compensator Design

The first admittance term Y_1 in (4-5) is related to the closed-loop current reference-to-current transfer function (current reference term), which provides desired input admittance magnitude with proper phase below the crossover frequency of the loop gain T_i . The second admittance term Y_2 is related to the closed-loop voltage-to-current transfer function (voltage term, or lagging phase admittance term), which has a 90° lagging phase below the crossover frequency. At low power command, the current induced in Y_2 will eventually exceed that in Y_1 , and thus the impact is very significant. Because Y_2 path current reduces the desired current, the resulting steady-state output will be less than the command input, and the situation gets worse at lighter load conditions.

4.3.1 Admittance Compensator for the Enhance Stability

The separation of two admittance terms suggests natural ways of eliminating unwanted terms in $Y(s)$. There are two possibilities of adding an admittance compensator $G_c(s)$: one is to add to the current reference summing junction, and the other is to add to the output of the current loop controller $G_i(s)$. Fig. 4.3 shows the block diagram of the compensated system that adds $G_c(s)$ after $G_i(s)$. This arrangement allows the design of $G_c(s)$ to be independent from $G_i(s)$, which can be seen from the following derivation result.

$$G_c(s) = -Y_2(s) = \frac{1}{H_v(s)V_{dc}F_m} \quad (4-9)$$

Eq. (4-9) indicates that the admittance compensator is proportional to the inverse of the dc bus voltage V_{dc} , voltage sensor gain, and the PWM gain.

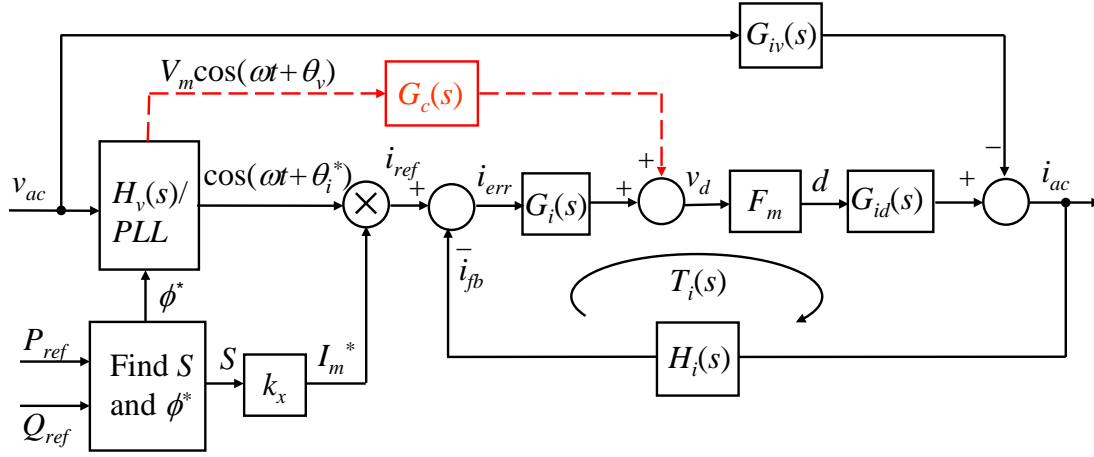


Fig. 4.3 Block diagram of the adding admittance compensator after the current loop controller

4.3.2 Proportional and Resonant Compensator

In order to reduce the steady-state error at the fundamental frequency or to provide a high gain at 50 or 60Hz, the quasi-proportional-resonant (QPR) controller, as shown in (4-10), is adopted for the current loop controller, which can provide a high gain at the fundamental frequency without phase offset.

$$G_i(s) = k_p + \frac{2k_r \omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad (4-10)$$

Here, k_p is a proportional gain, k_r is a resonant gain, and ω_c is an equivalent bandwidth of the resonant controller. With circuit parameters $L_{o1} = 3.6$ mH, $L_{o2} = 0.5$ mH, $L_g = 0.8$ mH, and $C_o = 2$ μ F, the QPR controller was designed to have the following parameters: $k_p = 2.512$, $k_r = 50$, $\omega_c =$

10 rad/sec, and $\omega_o = 2\pi \cdot 60$ rad/sec, and the resulting loop gain is 50dB at the fundamental frequency, or 60 Hz in this case. The crossover frequency and phase margin are 758 Hz and 48.3° , respectively.

4.3.3 Control for the Active and Reactive Power Flow

With the help of the admittance compensator for disturbance rejection and the QPR controller for providing the high gain at the fundamental frequency, a scalar current control approach is proposed to provide the active and reactive power control. The main role of the controller is to generate a current reference signal with respect to the P_{ref} , Q_{ref} , and V_{ac} . To synchronize I_{ac} with V_{ac} , a simple software phase-locked loop (SPLL) is adopted [21]. Fig. 4.4 shows the block diagram of the SPLL structure. Here the grid-voltage signal, V_{ac} , is divided by its peak voltage, V_m , to obtain the PLL input voltage with unity magnitude, or $V_i = \cos\theta_v$. By multiplying V_{in} and the feedback voltage, V_f , the phase error can be detected by its offset voltage. A low pass filter (LPF) filters the high-frequency portion and converts the phase error to a voltage signal. The voltage controlled oscillator (VCO), which consists of a feed-forward angular frequency, ω_{ff} , and an integrator, provides phase out, θ_v .

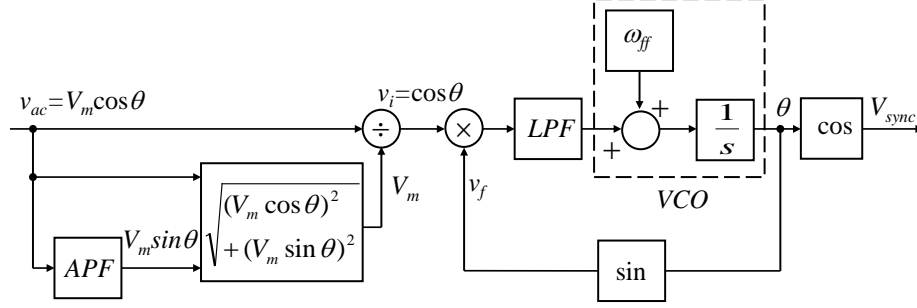


Fig. 4.4 Block diagram of the software phase locked loop

To avoid trigonometric computation in DSP, the orthogonal signal, $V_m \sin \theta_v$, can be generated from the sensed v_{ac} , or $V_m \cos \theta_v$, through an all pass filter (APF), which provides the same magnitude but 90° phase delay signal [30]. The square math block produces the peak voltage of V_{ac} through the following computation.

$$V_m = \sqrt{V_m^2 \cos^2 \theta_v + V_m^2 \sin^2 \theta_v} \quad (4-11)$$

Fig. 4.5 shows the block diagram of the current reference computation, which is to provide the current reference peak and phase information with respect to P_{ref} , Q_{ref} , and V_{ac} . Based on P_{ref} and Q_{ref} , the phase reference, or ϕ^* , can be obtained in (4-12):

$$\phi^* = \tan^{-1} \left(\frac{Q_{ref}}{P_{ref}} \right) = \theta_i^* - \theta_v \quad (4-12)$$

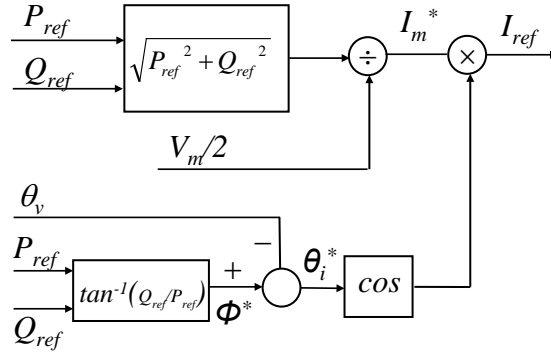


Fig. 4.5 Block diagram of the current reference computation

The current phase reference can be obtained by subtracting the voltage phase, as shown in (4-13):

$$\theta_i^* = \phi^* - \theta_v \quad (4-13)$$

The current reference peak or I_m^* , can be obtained from the magnitude of the apparent power divided by the voltage magnitude, as shown in (4-14):

$$I_m^* = \frac{2}{V_m} \sqrt{P_{ref}^2 + Q_{ref}^2} \quad (4-14)$$

4.3.4 DC Bus Voltage Requirement Analysis Using Phasor Diagrams

Fig. 4.6 shows a grid-tie LCL inverter circuit on the right side and its equivalent circuit on the left side. It can be simplified, because i_{ac} and v_{ac} are used as the feedback current and voltage signals for the current loop control.

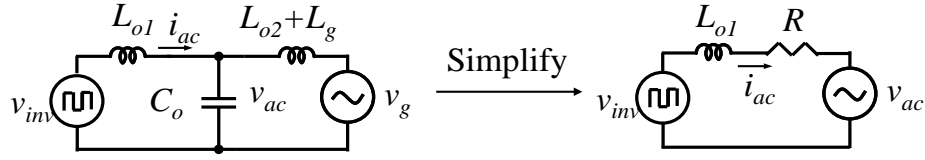


Fig. 4.6 Simplified grid-tie inverter circuit

Usually, the dc bus voltage can be determined to provide enough voltage in real power condition as shown in Fig. 4.7. Here the inverter terminal voltage v_{inv} needs to be higher than the output voltage measured at the capacitor filter, v_{ac} , with a voltage difference of $I_{ac}R + jI_{ac}X$. Here $X = \omega L_{o1}$. When the phase current is 90° leading, or capacitive type reactive power compensation, as shown in Fig. 4.8, the required V_{inv} is much reduced because $jI_{ac}X$ is 180° output of phase from V_{ac} . However, when the phase current is 90° lagging or under pure inductive type the reactive power condition, as shown in Fig. 4.9, the required V_{inv} is largest because jIX is in phase with V_{ac} . Since V_{inv} is directly proportional to the dc bus voltage minus two device voltage drops, V_{ce} , and the duty cycle, d , i.e., $V_{inv} = d \cdot (V_{dc} - 2V_{ce})$, insufficient dc bus voltage V_{dc} can easily saturate the duty cycle under lagging power flow condition. Therefore, to achieve wide range reactive power compensations, it is necessary to have sufficiently high enough V_{dc} to avoid duty cycle saturation, which will subsequently cause the waveform distortion.

If a grid-tie inverter is designed for the active power flow only, then V_{inv} can be obtained in (4-15), as referring to Fig. 4.7.

$$V_{inv} = \sqrt{(V_{ac} + I_{ac} \cdot R)^2 + (I_{ac} \cdot X)^2} . \quad (4-15)$$

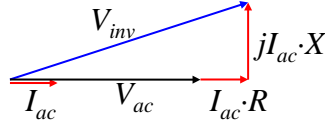


Fig. 4.7 Phasor diagram with active power only

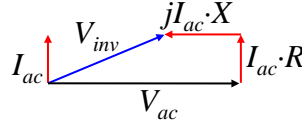


Fig. 4.8 Phasor diagram with leading reactive power only

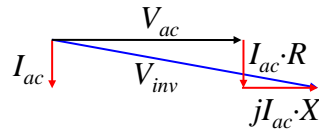


Fig. 4.9 Phasor diagram with lagging reactive power only

If a grid-tie inverter is designed for the lagging reactive power flow only, then V_{inv} can be obtained by referring to Fig. 4.9.

$$V_{inv} = \sqrt{(V_{ac} + I_{ac} \cdot X)^2 + (I_{ac} \cdot R)^2} \quad (4-16)$$

With considering of the device voltage drop, the dc link voltage, V_{dc} , can be calculated in (4-17).

$$V_{dc} = \frac{V_{inv}}{d} + 2V_{ce} \quad (4-17)$$

The inverter duty cycle can be expressed as a function of modulation index, M , or $d = M \cdot \cos(\omega t)$.

4.4 Simulation and Experimental Verificaiton

4.4.1 DC Bus Voltage Requirement Verification

Fig. 4.10 and Fig. 4.11 show simulation results for the mix of active and lagging reactive power control condition. Fig. 4.10 shows distorted i_{ac} due to insufficient V_{dc} , which was set at 400 V. Fig. 4.11 shows a clean sinusoidal i_{ac} when V_{dc} is sufficient. In this mixed active and reactive power flow case, the dc bus voltage was increased to 410 V.

The above simulation case clearly indicates the need for a higher dc bus voltage under reactive power flow condition. For an example 208-V rms, 5-kVA SOFC PCS, the circuit parameters and test condition are: $R = 0.15 \Omega$, $L = 3.5 \text{ mH}$, $V_{ac} = 208 \text{ V}$ or 220 V rms , and $\omega = 2\pi \cdot 60 \text{ rad/sec}$. Fig. 4.12 shows the voltage requirement for the entire power factor angle range under 5-kVA condition. The power factor angle is defined as the phase angle of the current with respect to the phase angle of the voltage. Here V_{inv} was calculated using (4-16), and V_{dc} was calculated using (4-17). The results clearly indicate dc bus voltage needs to be higher under lagging power factor angle than under leading power factor angle condition. The modulation index was limited to 0.85 to avoid short-pulse effect on the voltage magnitude, and the device voltage drop V_{ce} was assumed to be 2 V in the calculation.

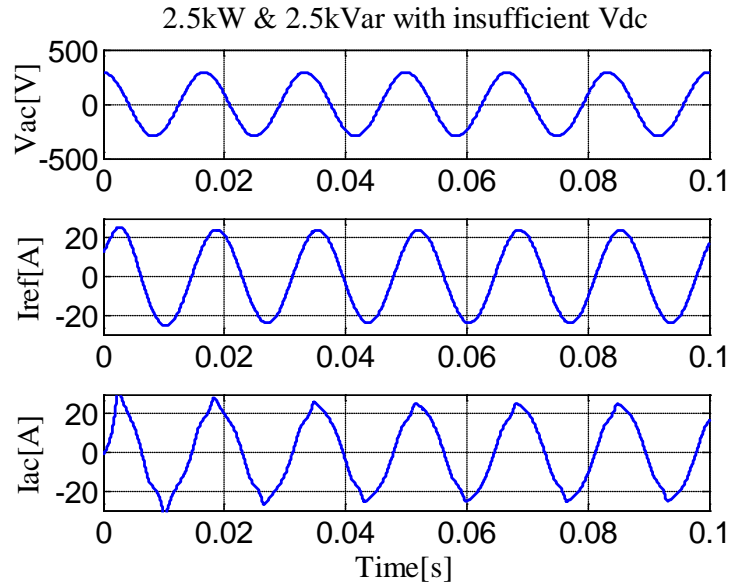


Fig. 4. 10 Simulation results of the active and reactive power with insufficient V_{dc}

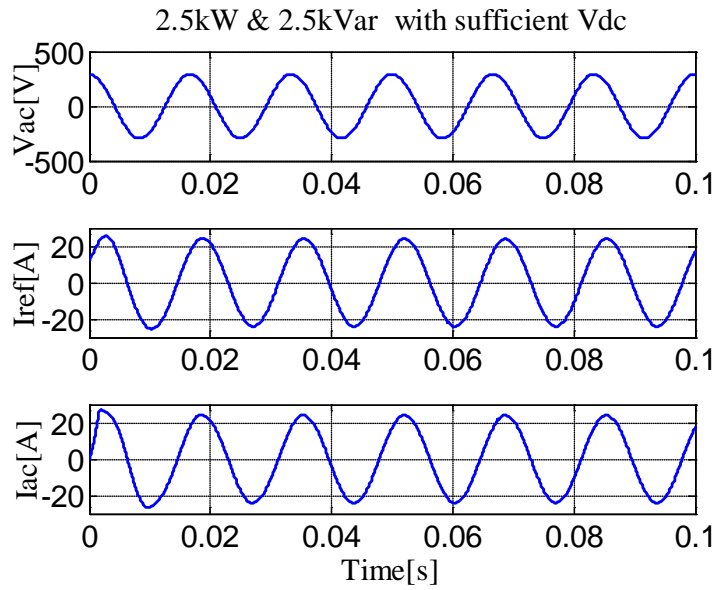


Fig. 4. 11 Simulation results of the active and reactive power with sufficient V_{dc}

Fig. 4.12 indicates the dc bus voltage needs to be at least 404 V at the 208 V-rms line and 420 V at the 220 V-rms line for 5-kVA condition.

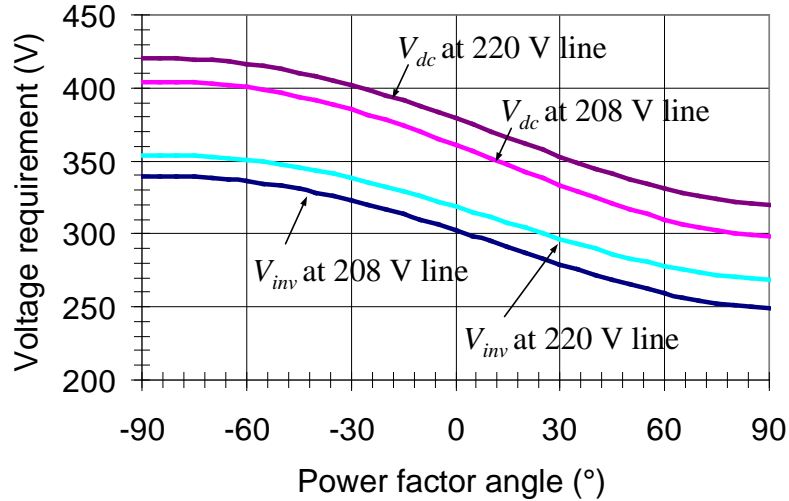


Fig. 4. 12 Voltage requirements with respect to the power factor angle at 5-kVA condition

For lower power, the voltage requirement can be scaled down. For example, at 45° lagging reactive power 3.5 kVA condition, the calculated V_{dc} should be 399 V for 220 Vrms line. Fig. 9(a) shows experimental results with $V_{dc} = 395$ V. Under such insufficient dc bus voltage level, the grid current i_g is distorted. Note that v_d is the duty cycle control voltage, which has a flat top in Fig. 4.13 and is apparently saturated.

Fig. 4.14 shows the experimental results under the same power condition, but with dc bus voltage increased to 416 V. In this case the duty cycle control voltage v_d does not saturate, and the waveform distortion completely disappears.

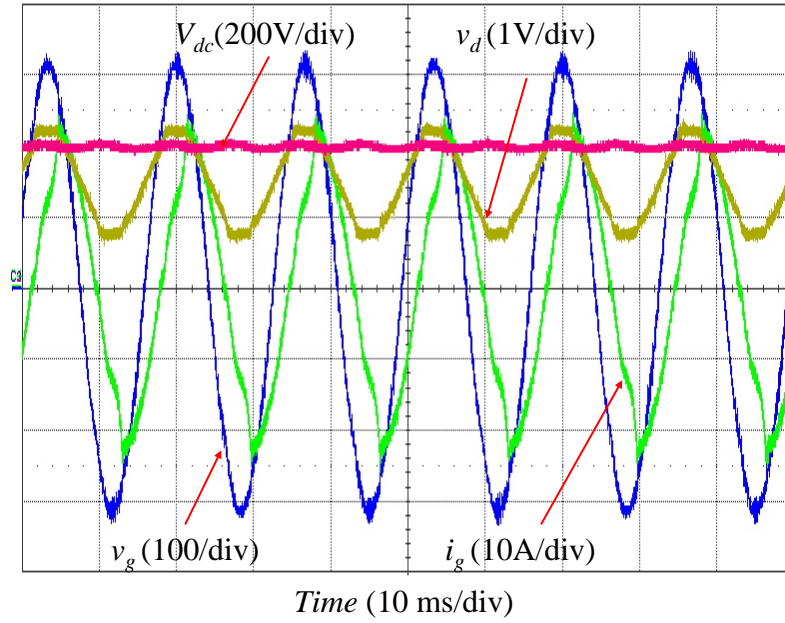


Fig. 4. 13 Experimental results with $V_{dc} = 395$ V for the mixed 2.5 kW active and 2.5 kVAr lagging reactive power command

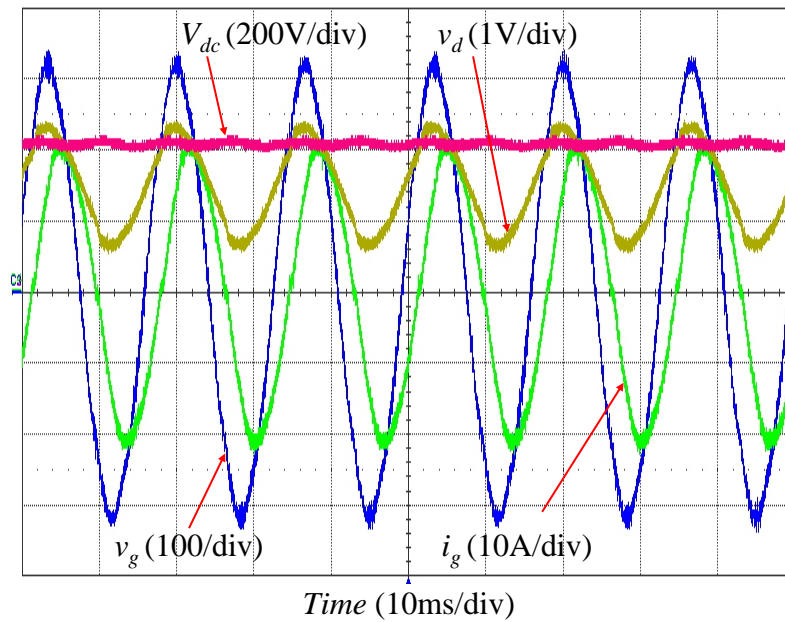


Fig. 4. 14 Experimental results with $V_{dc} = 416$ V for the mixed 2.5 kW active and 2.5 kVAr lagging reactive power command

4.4.2 Wide Range Power Flow Control Verification

With the proposed admittance compensation, the output power can be effectively controlled from zero command to full power command. Fig. 4.15 shows experimental dc bus voltage V_{dc} , ac grid voltage v_g , and output current i_g under zero power command condition. The output power is 5-W in this case. Although the proposed system using admittance compensation and PR controller can precisely control the active and reactive power flow, it cannot fully eliminate the steady-state error due to finite PR gain and limitation of actual hardware and software implementation. However, an error of 0.1% is acceptable for most applications.

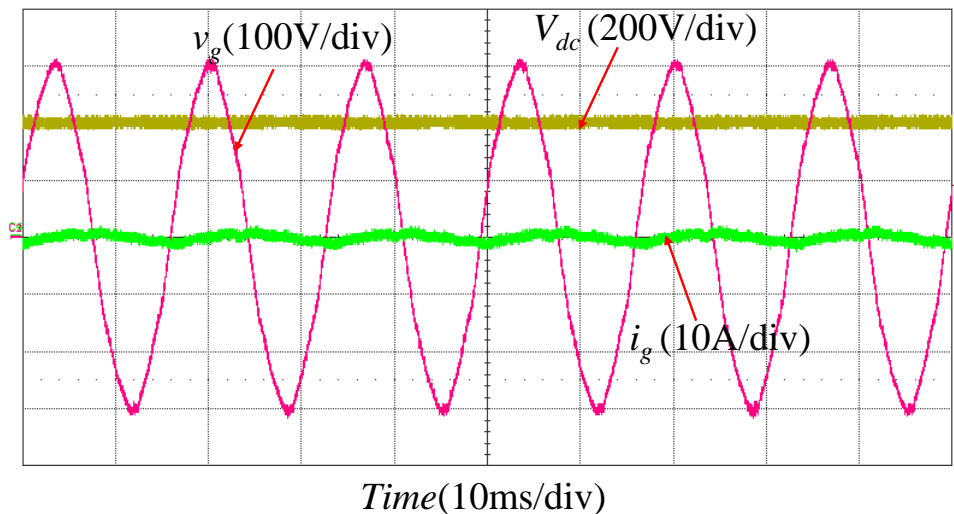


Fig. 4. 15 Experimental results for the zero power command

In Fig. 4.16, the upper window indicates pure 1-kVAr leading reactive power condition, the middle window indicates pure 1-kW pure active power condition, and the lower window indicates pure 1-kVAr lagging reactive power condition. Similar experimental results can be seen in Fig. 4.17 at a higher power level. In Fig. 4.17, the upper window indicates pure 5-kVAr leading reactive power condition, the middle window indicates pure 5-kW pure active power

condition, and the lower window indicates pure 5-kVAr lagging reactive power condition. With the change of power command from leading to lagging, the phase of i_g shifts from 90° to -90° .

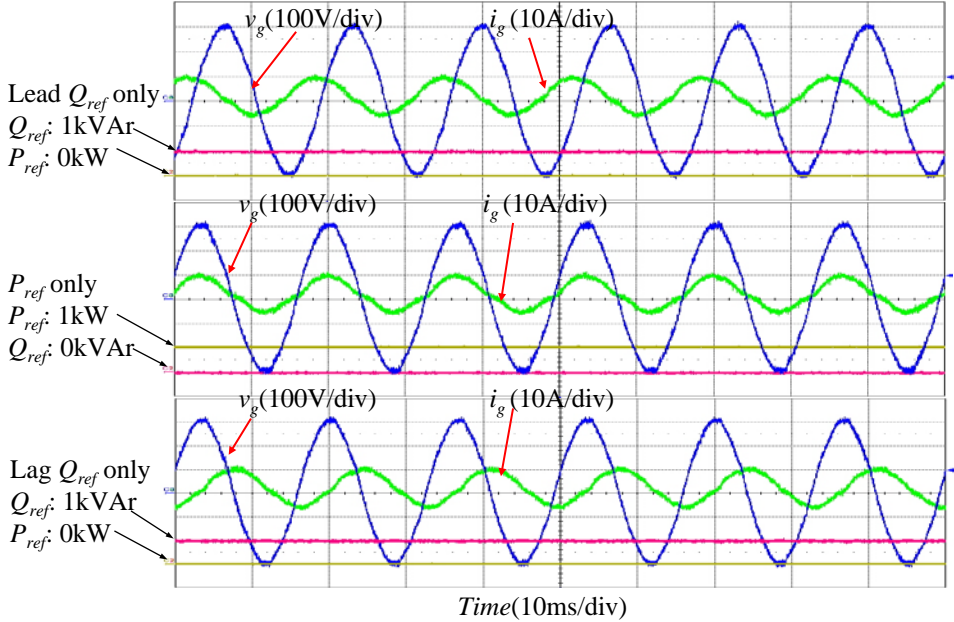


Fig. 4. 16 Experimental results of the 1kVAr leading reactive power command, 1kW active power command, and 1kVAr lagging reactive power command

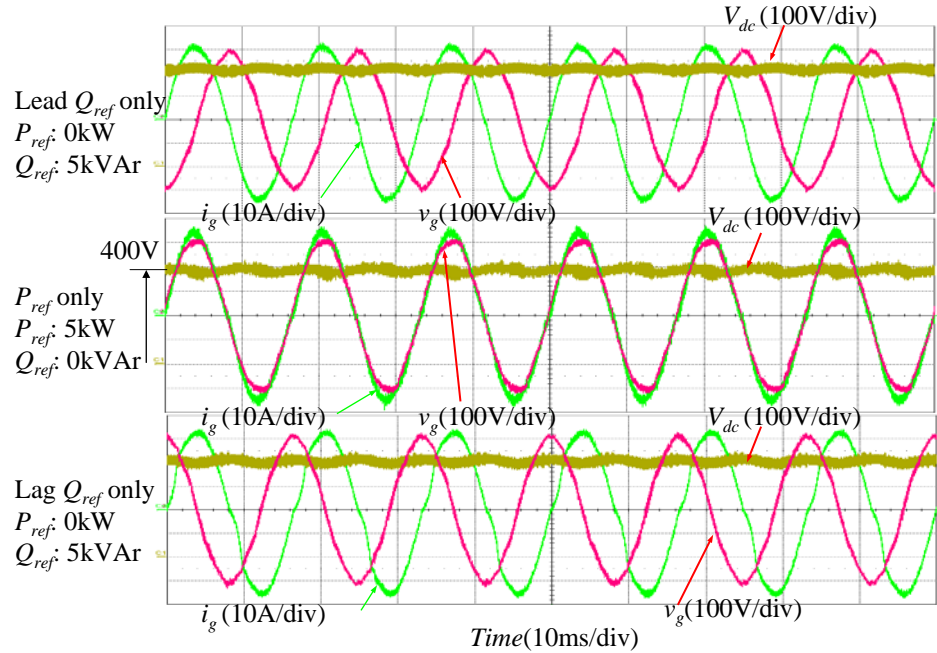


Fig. 4. 17 Experimental results for the 5kVAr leading reactive power command, 5kW active power command, and 5kVAr lagging reactive power command

Fig. 4.18 shows experimental results for the mixed active power and reactive power flow condition. The upper window shows voltage and current waveforms under 3.5-kW active power and 3.5-kVAr leading reactive power commands. The grid current i_g clearly shows 45° lead over the grid voltage v_g . The lower window shows the voltage and current waveforms under 3.5-kW active power and 3.5-kVAr lagging reactive power commands. In this case, the grid current i_g clearly shows 45° lag behind the grid voltage v_g . With the change of the power command from leading to lagging, the phase of i_g shifts from 45° to -45° . From both Fig. 4.13 and Fig. 4.18, it can be concluded that the proposed technique can effectively control a wide range active and reactive power flow.

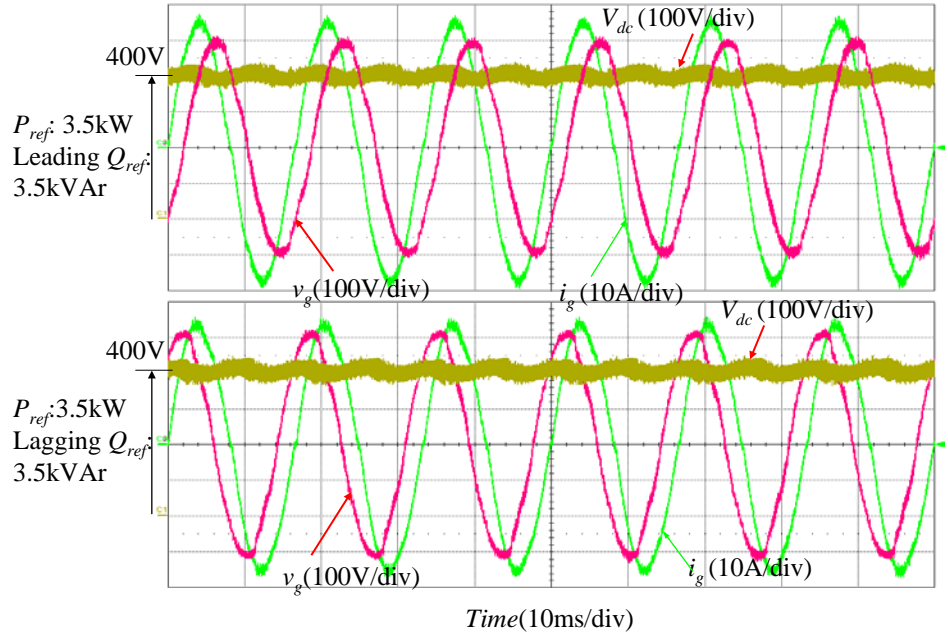


Fig. 4. 18 Experimental results for the 5kVA apparent power with 3.5kW active power command and 3.5kVAr leading reactive power command, and the 5kVA apparent power with 3.5kW active power command and 3.5kVAr lagging reactive power command

4.5 Conclusion

A wide range active and reactive power flow control has been proposed for grid-tie solid-oxide fuel cell power conditioning systems. The key to achieving smooth lagging reactive power control is the dc bus voltage. The key to achieving precision power flow control is to incorporate the QPR controller in the current loop to ensure high loop gain at the fundamental frequency and the admittance compensator to ensure cancellation of the grid voltage induced negative power flow.

It was found that under lagging reactive power flow control, the dc bus voltage needed to be higher than what was originally designed for the active power flow control. Without increasing the dc bus voltage, the output current waveform tends to be distorted because of duty cycle saturation, which agrees with the phasor analysis results. By increasing the dc bus voltage setting from 400 to 420 V, the waveform distortion disappeared, and entire range of rated active and reactive power flow control was achieved.

The current loop transfer function has been systematically derived with representations of conventional transfer function format. A 5-kVA LCL-based grid-tie inverter for the fuel cell PCS was used as the platform to show current loop controller design and admittance compensation. The QPR controller was adopted to obtain a sufficient gain at the fundamental frequency while maintaining a sufficient stability margin. Adding an admittance compensator helps cancel the negative power flow induced by the grid voltage, thus allowing precision power flow control at low power level.

The proposed active and reactive power flow control approach has been simulated, and the same parameters have been used for a DSP based PCS inverter controller. Both simulation and experimental results indicate that the grid-tie inverter can provide from zero power command to full range active and reactive power. Overall analysis and simulation have been well verified with the hardware experiments. Due to finite QPR gain and hardware and software precision limitation, the output power error was found to be 0.1%, which should be acceptable to solid oxide fuel cell and most other energy flow control applications. The design with the use of sufficient dc bus voltage level, the QPR current loop controller, and the admittance path compensation has been proven effective for a wide range active and reactive power flow control.

Chapter 5 Versatile Utilization of three half-bridge single phase grid tie inverters four wires configuration for the renewable energy distributed generation

5.1 Introduction

One of the main issues of power system engineering is how to realize smart grid technologies; which is the power system that is capable of handling distribution resources, providing more economical service to end-users, and maintaining its conditions [76]. Renewable energy sources are getting more attention as distributed generations in a smart grid [77], [78]. A power conditioning system (PCS) is a bridge to connect renewable energy sources to the utility grid [1].

Due to uneven or non-linear loads, grid voltage can be unbalanced inducing severe adverse effects such as reduced efficiency and decreased life of the system [79]. Active filters can be designed to correct unbalance voltage conditions [80], [86]. PCSs are not only capable of transferring energy from renewable energy sources, but also supporting utility grid conditions using either reactive power flow control [87] or negative sequence current control [88].

For the three phase current control scheme, proportional and integral control with synchronous frame reference current control [18] or proportional and resonant (PR) control with stationary frame reference current control [62] are proposed in order to provide high gain at the fundamental frequency range. Based on synchronous reference frame current control, space vector pulse width modulation inverter with feed-forward controller provides good dynamic

performance [81]. In addition to, direct power control with hysteresis band control [82], predictive current control [83], and pole placement current control [84] are proposed. All proposed control schemes are useful for balanced symmetrical system only.

For the unbalance grid voltage condition, three phase four wire configuration is required. [86] derived a current-regulated control method for a PWM voltage converter with four wires. Three PR control with synchronous frame reference was proposed to interface renewable energy to grid and provide unbalanced voltage correction by adding modular manner [87].

For single phase grid-tie inverter applications, PR current control can be a useful control scheme [20]. Admittance compensation was proposed based on frequency domain analysis in order to eliminate the disturbance of grid voltage [65-66]. An active and reactive power flow controller can be designed with PR control and admittance compensation [88].

In this paper, three half-bridge single phase grid-tie inverters based on the half-bridge single phase grid-tie inverter current control design is proposed for the versatile utilization of three grid-tie inverters as a renewable energy PCS. A half-bridge single phase grid-tie inverter is derived with transfer function blocks. Its controller is designed with PR controller and admittance compensation. For three phase operation, there are two current reference modes. One is constant current mode and the other is constant power mode. Constant power can be active power command only, reactive power command only, or combining active power and reactive power command in order to help utility grid unbalance condition. The entire controller is implemented with TMS320F2808 digital signal processor (DSP). A 3-kW PCS hardware is used as the power stage platform. A hardware prototype has been built and tested to show operation of power and to verify the simulation results.

5.2 Modeling and Control of the Half-Bridge Single Phase Grid-Tie Inverter

Fig. 5.1 shows the proposed a half-bridge single phase grid-tie inverter configuration. Two renewable energy voltage sources, $1/2V_{dc}$, provide power and the middle point of two dc link capacitors, C_{dc} , is connected to the neutral point of the grid phase voltage source. Two IGBT devices produce pulse width modulation (PWM) signals and inverter output filter inductor, L_f , and output filter capacitor, C_f , make the square signals into smooth sinusoidal signals. Single phase grid voltage, V_g , can be supplied through the grid line inductance, L_g and the capacitor voltage, v_{ac} is the voltage of the grid connection point. For the simple derivation, equivalent series resistances for inductor models are ignored. Filter inductor current, i_{ac} , and v_{ac} are sensed by sensor condition circuit such as current scaling and filtering block, $H_i(s)$ and voltages scaling and filtering block, $H_v(s)$. Current reference, i_{ref} , can be obtained by translating power command, P_{ref} , to current command and multiplying grid voltage angle. To track ac reference, a PR controller was adopted to provide high gains at fundamental frequency. In addition, an admittance compensator, $G_{AC}(s)$, was added to minimize the grid voltage disturbance. Duty cycle, d , is determined by multiplying the modulation gain, F_m , and compensation output.

Fig. 5.2 shows detailed control diagram with transfer function blocks: $G_{iv}(s)$ and $G_{id}(s)$ -power stage transfer functions, $G_{PR}(s)$ -current loop compensator, F_m -PWM gain, $G_{AC}(s)$ -admittance compensator, $H_i(s)$ -current sensor gain, $H_v(s)$ -voltage sensor gain [65-66].

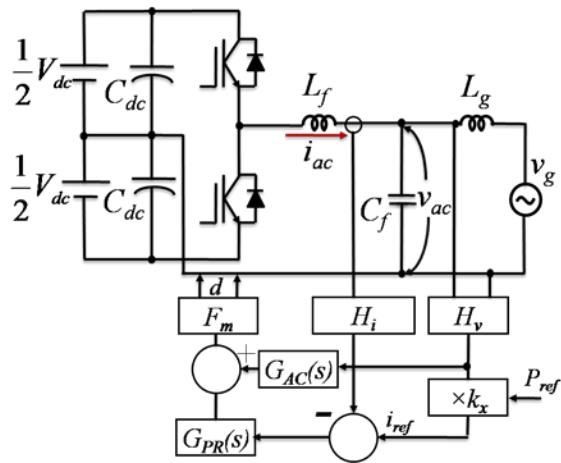


Fig. 5.1 Proposed half-bridge single phase grid-tie inverter configuration

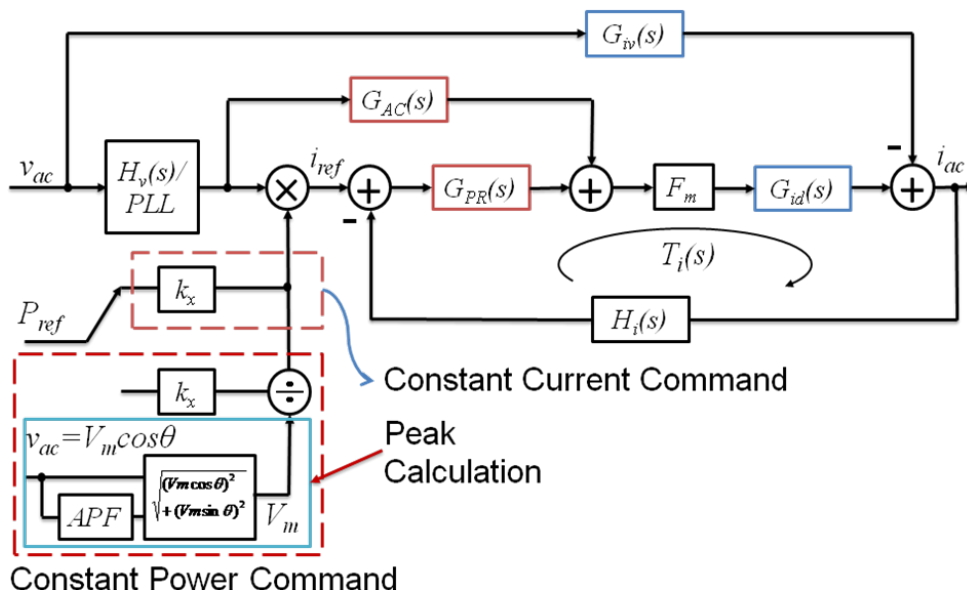


Fig. 5.2 Proposed inverter control diagram using transfer function

Since the impedance of C_f is relatively large compare to the impedance of the L_f and L_g , the current through C_f can be ignored. Using the average inverter output voltage $d \times V_{dc}/2$, i_{ac} can be derived with two plant transfer functions in (5-1).

$$i_{ac} = \frac{V_{dc}/2}{sL_f} \cdot d - \frac{1}{sL_f} \cdot v_{ac} = G_{id}(s) \cdot d - G_{iv}(s) \cdot v_{ac} \quad (5-1)$$

where, $d(s)$ is the duty cycle, $G_{id}(s)$ is the duty cycle to output current transfer function, and $G_{iv}(s)$ is the capacitor voltage to output current transfer function. The closed loop admittance can be represented in (5-2) and (5-3).

$$Y(s) = \frac{i_{ac}(s)}{v_{ac}(s)} = \frac{G_{id}(s) \cdot G_{PR}(s) \cdot F_m \cdot H_i(s)}{1 + T_i(s)} k_x \cdot P_{ref} \cdot H_v(s) - \frac{G_{id}(s)}{1 + T_i(s)} \quad (5-2)$$

where, $T_i(s) = G_{id}(s) \cdot G_{PR}(s) \cdot F_m \cdot H_i(s)$

$$Y(s) = Y_1(s) + Y_2(s) = G_{idcl}(s) - G_{ivcl}(s) \quad (5-3)$$

where, $G_{idcl}(s) = \frac{G_{id}(s) \cdot G_{PR}(s) \cdot F_m \cdot H_i(s)}{1 + T_i(s)} k_x \cdot P_{ref} \cdot H_v(s)$ and $G_{ivcl}(s) = -\frac{G_{id}(s)}{1 + T_i(s)}$

5.2.1 Admittance Compensator for the Enhance Stability

The admittance compensator, $G_{AC}(s)$ (5-4) in [34] is added after the current loop compensator in order to eliminate the disturbance from the grid voltage.

$$G_{AC}(s) = \frac{1}{H_v(s) \cdot V_{dc}/2 \cdot F_m} \quad (5-4)$$

5.2.2 Proportional and Resonant Compensator

In order to reduce steady-state error at the fundamental frequency or provide high gain at 50 or 60Hz, a PR controller is selected in (5-5), because it can provide a high gain at fundamental frequency without phase offset and sufficient loop gain.

$$G_{PR}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \quad (5-5)$$

where, k_p is a proportional gain, k_r is a resonant gain, and ω_c is an equivalent bandwidth of the resonant controller. A PR controller was designed to have the following parameters: $k_p = 1.2$, $k_r = 150$, $\omega_c = 10$ rad/sec, and $\omega_o = 2\pi \cdot 60$ rad/sec, and the resulting loop gain is 50dB at the fundamental frequency, or 60 Hz in this case. The crossover frequency and phase margin are 1 kHz and 68° , respectively [66].

5.2.3 Two Current Command Modes

There are two current command modes. One is constant current mode, and the other is constant power mode. When the constant current mode is selected, the current reference can be obtained by translating power command as current command with phase angle of grid voltage. If the constant power command mode is selected, the current reference considers the grid voltage condition and based on grid voltage level, the current reference is obtained with regards the amount of power level. (5-6) and (5-7) show the current command with respect to constant current command mode and constant power command mode, respectively.

$$i_{ref} = P_{ref} \cdot k_x \cdot \cos(\omega t + \theta_v) \quad (5-6)$$

$$i_{ref} = \frac{2 \cdot P_{ref} \cdot k_x}{V_m} \cdot \cos(\omega t + \theta_v) \quad (5-7)$$

where V_m is the peak value of the filter capacitor voltage.

5.2.4 Proposed Three Half-Bridge Single Phase Grid-Tie Inverter

Fig. 5.3 shows the proposed three half-bridge single phase grid-tie inverters with four wire configuration. Based on independent half-bridge single phase grid-tie inverter, three inverters are combined together in order to provide a renewable energy PCS capable of handling with either balanced three phase grid voltage condition or unbalanced three phase grid voltage condition.

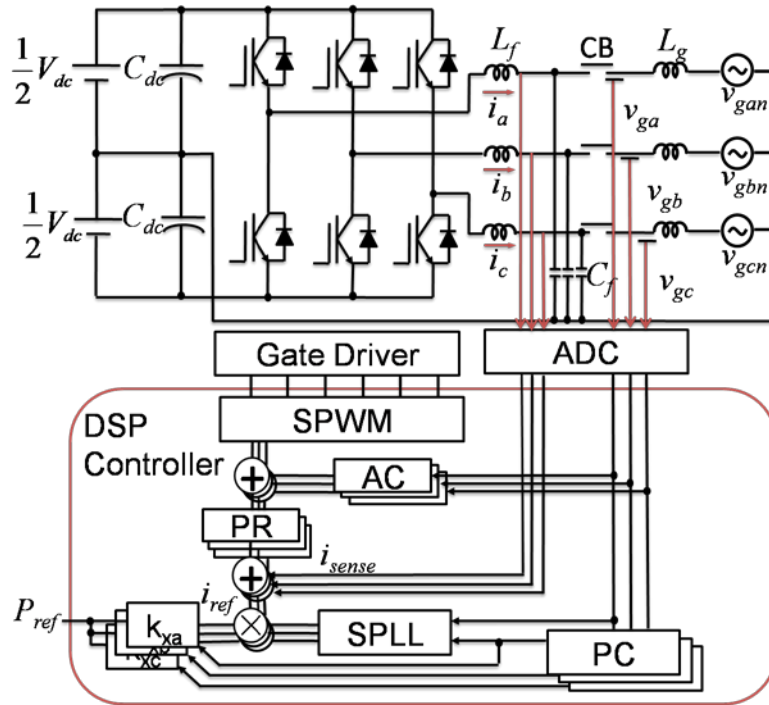


Fig. 5.3 Proposed three half-bridge single phase grid-tie inverters configuration

When the three phase grid voltage sources are balanced, either the constant current mode or constant power command mode can send the same amount of three phase currents. However, if the three phase grid voltage sources are unbalanced, then the constant power command mode can send more current to lower voltage phase than the other phases. It means that the heavily loaded phase current can be supplied more current from the renewable energy PCS.

One of the three phase grid voltages is used to provide phase angle information through software phase locked loop algorithm. Then, other two phase angles can be obtained by 120° apart from the phase angle output of the software phase locked loop. For the constant power command mode, the peak magnitude of the phase grid voltage is calculated by peak calculation routine (PC).

Instead of using the conventional three phase transformation frame, the proposed method provides a simple way of compensation design. In addition, the proposed method can be utilized, not only to transfer power, but also to help unevenly loaded phase conditions.

Based on computation time in [89], the stationary frame reference current control and the synchronous frame reference current control require 163 computation cycles, but the proposed scheme need 102 computation cycles shown in Table. 5. 1.

Table. 5.1 Comparison of the computation time for the three control schemes

Control Module	CPU Cycle	# of required module for SRFC dq	# of required module for STRF $\alpha\beta$	# of required module for Proposed Control
Park Transformation	9	2	1	X
Clarke Transformation	9	1	1	X
Inverse Clarke	9	X	1	X
Regular PI	34	4	2	X
Regular PR	>34	X	2	3
Total Cycles		163	163	102

5.3 Simulation and Experimental Verficiation

A 3-kW PCS prototype dc-ac inverter was tested as an example system. The source inductance, L_g , of the tested grid system was considered to be 0.5mH. For the inverter output filter, L_f was selected as 2.1mH, which has an equivalent series resistance of 0.1 Ω . For the inverter output filter capacitor, C_f is equal to 2 μ F. For the main power stage, a 7 IGBT module, 7MB100U2B060, with 600V and 100A power rating, was selected. To emulate unbalance three phase grid voltage condition, an auto-transformer, GE 240V, 50 /60 Hz three phase variable transformers has been used. The dc link capacitor was selected as 3.6mF in order to supply enough energy to the inverter. The switching frequency and the sampling frequency are 16 kHz. To verify the proposed current controller scheme, PSIM simulation tool was used and the results are shown in Fig. 5.4 and 5.5. Fig. 5.4 shows the simulation waveform of the balance three phase voltage condition with constant current command mode. v_{ga} , v_{gb} , and v_{gc} are 100V rms. The three phase grid currents are 6A rms.

Fig. 5.5 shows the simulation waveform at constant power command mode under unbalance three phase grid voltage conditions. v_{gan} is set at 88V rms while v_{gbn} and v_{gcn} are set at 100V rms for simulation. v_{ga} is 93V rms, v_{gb} and v_{gc} are 104V rms. i_{ga} is 7.7A rms and i_{gb} and i_{gc} are 6.7A rms and 6.8A rms, respectively. The average power of the phase A is 717W. The average power of the phase B is 703W. The average power of the phase C is 713W.

The simulation results show that the proposed control scheme is able to provide the same amount of current and power to the either balanced or unbalanced grid voltage.

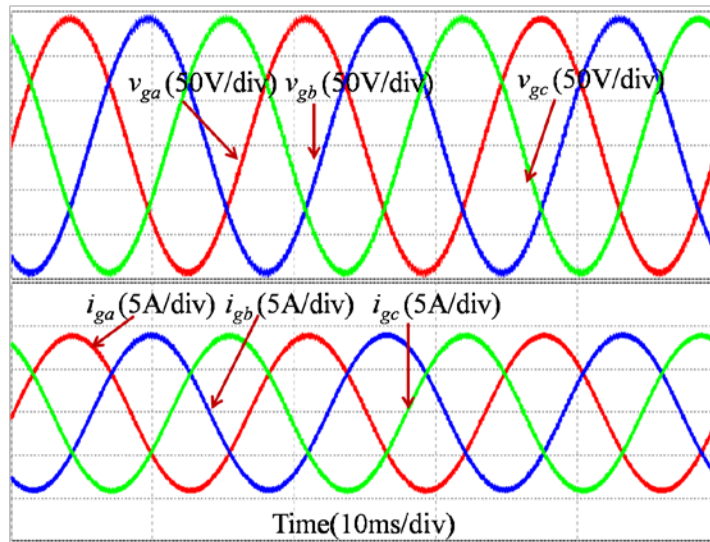


Fig. 5.4 Simulation waveform of the balance three phase grid voltage and constnat current command condition

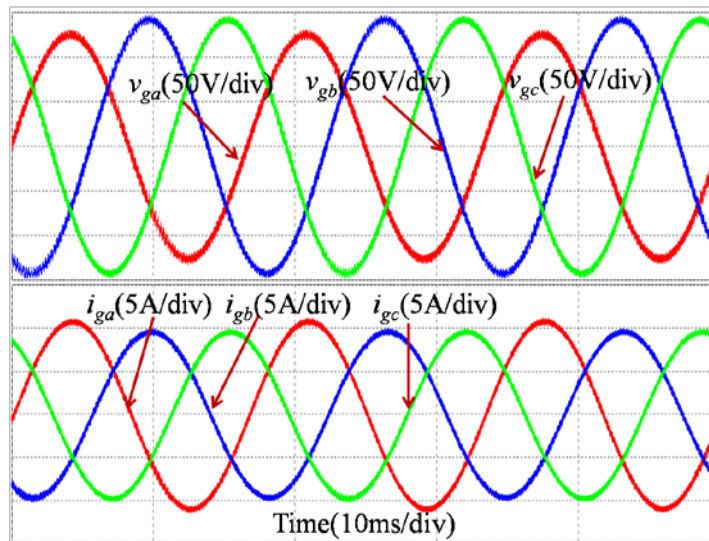


Fig. 5.5 Simulation waveform of the unbalance three phase grid voltage and constnat power command condition

Fig. 5.6 shows the three phase test setup, which includes a three phase auto-transformer on the left side lower corner and DSP controller board, grid interconnection board, filter board, IGBT power stage board, and DC link capacitors.

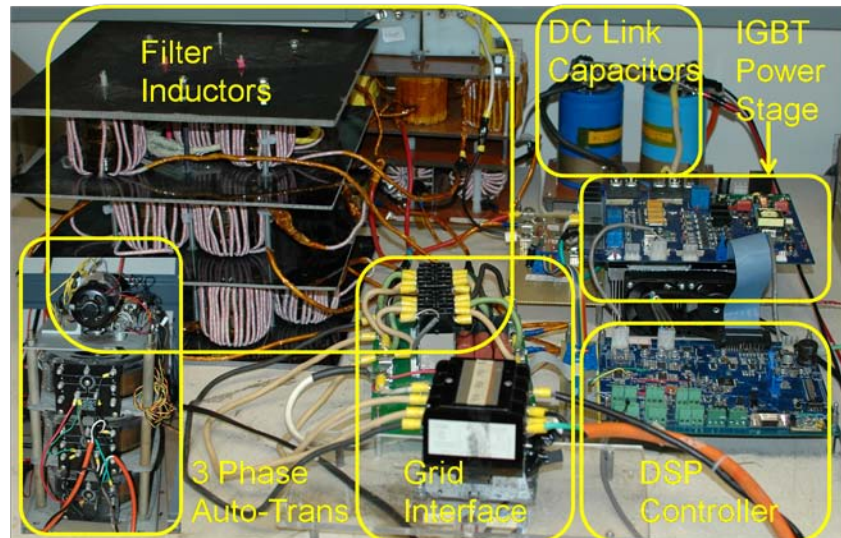


Fig. 5.6 Three half-bridge single phase grid-tie

Three half-bridge single phase grid-tie inverters operate independently with 4 wire configuration. Therefore, the gate signals can be turned on separately for each phase at zero crossing point. Fig. 5.7 shows the gate signals test results with respect to each phase grid voltage zero crossing point. The gate signal of phase B is turned on at the zero crossing point of grid voltage after 5.55ms from the gate signal of phase A is turned on.

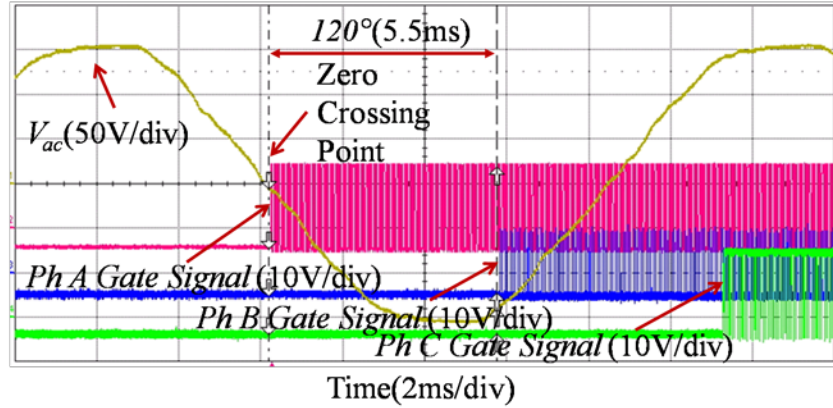


Fig. 5.7 Experimental results of the three gate signals at zero crossing point

Fig. 5.8 and Fig. 5.9 show balance three phase grid voltage sources and three phase grid currents, respectively in constant current command mode. v_{ga} , v_{gb} , and v_{gc} are 100V rms. $i_{ga}=6.14\text{A}$ rms, $i_{gb}=6.23\text{A}$ rms, and $i_{gc}=6.51\text{A}$ rms. due to slightly different filter inductance and equipment measurement error involved. Fig. 5.9 and Fig. 5.10 show the unbalanced three phase grid voltage sources and the unbalanced three phase grid currents for the same amount of phase power. v_{ga} is 88.4Vrms. v_{gb} and v_{gc} are 100Vrms. To emulate the unbalanced three phase grid voltage source condition, a three phase auto-transformer was used. With respect to the single phase input voltage of the primary side connection, the secondary side several taps provides different magnitude of output voltage for instance if the input voltage is 120V rms, then there are several taps to produce 112V rms, 107V rms, 100V rms, 88V rms, 71V rms, and 57V rms. In this paper, all three phases are connected 120V rms three phase 4 wire connection. 100V rms output and 88V rms output were selected to emulate balanced and unbalanced grid voltage conditions. Fig. 5.10 shows the different current magnitude required in order to transfer the same three phase power to each phase. i_{ga} is 7.52A rms, i_{gb} is 6.71A rms, and i_{gc} is 7A rms. Measurement error can

affect the current reference at constant power command mode. However, the overall power for the grid-tie inverter is 2kW and each phase produces about 670W.

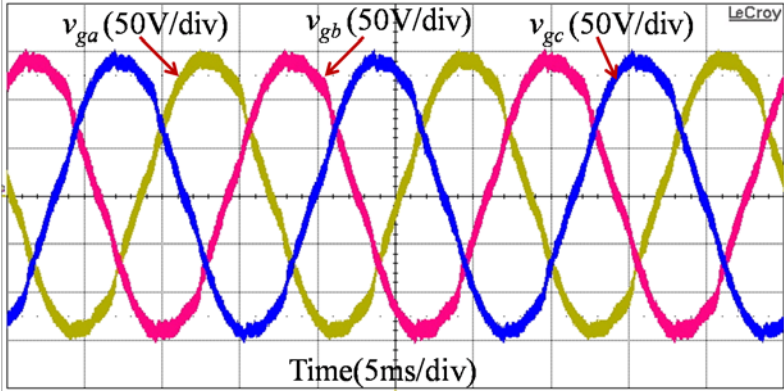


Fig. 5.8 Experimental waveform of the balanced three phase grid voltage

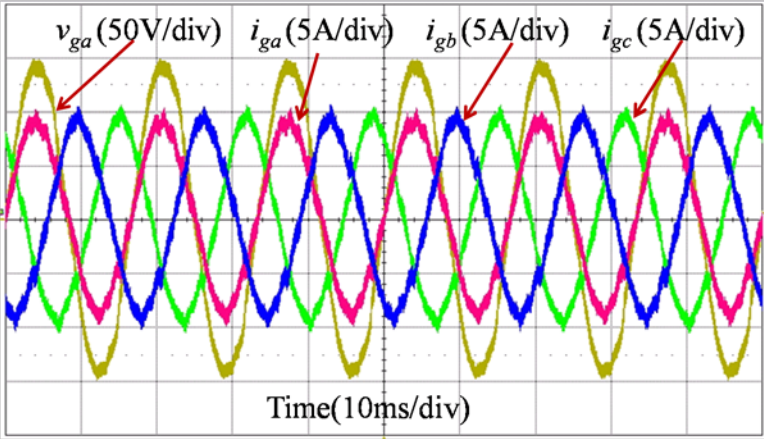


Fig. 5.9 Experimental waveform of the balanced three phase grid current

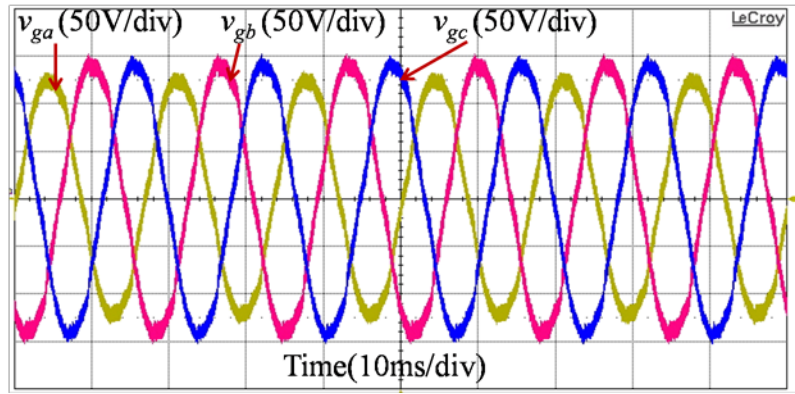


Fig. 5.10 Experimental waveform of the unbalanced three phase grid voltages

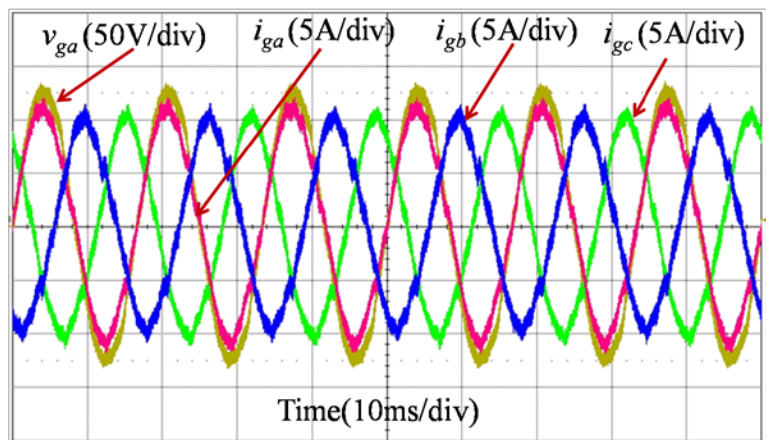


Fig. 5.11 Experimental waveform of the unbalanced three phase grid current for the same amount of three phase power

5.4 Conclusion

A system with three half-bridge single-phase grid-tie inverters with 4 wire configuration has been proposed and developed for renewable energy PCS. The half-bridge single-phase grid-tie inverter has been systematically derived with representations of conventional transfer functions. For the current control scheme, a PR controller and an admittance compensator are adopted in order to track current reference properly without grid voltage disturbance. A 3-kW prototype was built to verify the simulation results and experimental results.

The proposed method has been simulated, and the same parameters have been used for DSP based PCS inverter controller. Simulation results indicate that proposed three half-bridge single phase grid-tie inverters are capable of producing either the same amount of current to each phase or the same amount of power to each phase. Experimental results confirmed the mathematical design and simulation results.

Chapter 6 Summary, Contributions, and Future Work

6.1 Summary

A current loop transfer function of a single-phase grid-tie inverter has been systematically derived with representations of conventional transfer function format and admittance terms for the sake of controller design and feed-forward compensation. A second order lead-lag compensator is proposed to avoid low stability margin while maintaining sufficient gain at the fundamental frequency. The proposed current loop controller and admittance compensator have been simulated and the same parameters have been used for a DSP based PCS inverter controller. Simulation results indicate that without the admittance path compensation the current loop controller output duty cycle is largely offset by the admittance path. At light load settings, the power flow may be erratically fed back to the inverter which can cause catastrophe failure. With admittance path compensation, the output power shows a steady-state offset that matches the design value.

The power circuit adopts the LCL type filter to maintain a universal output that can be operated in both standalone and grid-tie modes. The proposed admittance compensation along with a quasi-proportional-resonant controller is designed to achieve high gain at the fundamental frequency while maintaining an adequate stability margin. Without the admittance path compensator, simulation results indicate that the system cannot start up smoothly and the zero current command cannot be tracked very well. At the first simulation cycle, the power flow is erratically fed back to the inverter which may cause catastrophic failure. With admittance path

compensation, the steady-state current error can be easily reduced with the loop gain design in frequency-domain.

A wide-range active and reactive power flow controller is designed to operate the inverter in pure leading, pure lagging, and the mix with active and reactive power command. The key to achieving lagging power flow control is to ensure sufficiently high dc bus voltage to avoid duty cycle saturation. The key to achieving precision power flow control for a wide-range of power levels is to adopt a QPR controller for the current loop and an admittance compensator to cancel the disturbance of the grid voltage. Phasor analysis was adopted to explain the need of the dc bus voltage requirement. A 5-kVA grid-tie fuel cell inverter was used as the platform to show current loop controller design and admittance compensation.

Three half-bridge single-phase grid-tie inverters with a 4 wire configuration have been proposed and developed for renewable energy PCS. The half-bridge single-phase grid-tie inverter has been systematically derived. For the current control scheme, a PR controller and an admittance compensator are adopted in order to track current reference properly without grid voltage disturbance. Three independent half-bridge single-phase grid-tie inverters can be combined for a three phase grid-tie inverter. A 3-kW prototype was built to verify the simulation results and experimental results.

The proposed method has been simulated and the same parameters have been used for a DSP based PCS inverter controller. Simulation results indicate that the proposed three half-bridge single phase grid-tie inverters produce either the same amount of current to each phase or the same amount of power to each phase based on the operating mode. Experimental results matched the mathematical design and simulation results well.

6.2 Contributions

6.2.1 Itemized Contributions

- A closed-loop dynamic model for the current control loop of the single phase utility grid-tie inverter with admittance compensator has been developed. The model explains the structure of the inverter with admittance terms, the current phase lagging phenomenon, and lays the groundwork for development of an admittance compensator.
- The admittance compensator principle has been proposed to completely eliminate the effect of the grid voltage to the inverter and to prevent negative power flow.
- The admittance compensator principle can be adapted not only for an L-filtered single phase grid tie inverter but also an LCL-filtered single phase grid-tie inverter effectively.
- The admittance compensator and the quasi-proportional-resonant compensator have been designed for precise active power flow control.
- In addition, to control active and reactive power flow, the scalar compensator has been proposed along with the admittance compensator and the quasi-proportional resonant compensator.
- Based on the half-bridge single phase grid-tie inverter design, three phase grid-tie inverter control scheme has been proposed.

6.2.2 Scholarly Contributions

- **US Patent Application No: 12/036,087**, Jih-Sheng Lai, **Sung Yeul Park**, Chien-Liang Chen
“Control System and Method for a Universal Power Conditioning System.”
- **S. -Y. Park**, C. -L. Chen, J. -S. Lai, “A Wide-range active and reactive power flow controller for a solid oxide fuel cell power conditioning system,” *IEEE Trans. on Power Electronics*, vol.23, pp.2703-2709, Nov 2008
- **S. -Y. Park**, C. -L. Chen, J. -S. Lai, S. -R. Moon, “Admittance Compensation in Current Loop Control for a Grid-Tie LCL Fuel Cell Inverter,” *IEEE Trans. on Power Electronics*, vol. 23, pp. 1716-1723, Jul 2008.
- C. -L. Chen, J. -S. Lai, Y. -B. Wang, **S. -Y. Park**, H. Miwa, “Design and Control for LCL-Based Inverters with Both Grid-Tie and Standalone Parallel Operations,” *Conf. Rec. of IEEE Industry Applications Annual Meeting*, 5-9 Oct. 2008, Edmonton, Alberta, Canada
- **S. -Y. Park**, C. -L. Chen, J. -S. Lai, “Wide range active and reactive power flow controller for a solid oxide fuel cell power conditioning system,” *Proc. of IEEE Applied Power Electronics Conference*, 24-29 Feb. 2008, Austin, TX, pp.952-958.
- C. -L. Chen, **S. -Y. Park**, J. -S. Lai, S.R. Moon, “Admittance Compensation in Current Loop Control for a Grid-Tie LCL Fuel Cell Inverter,” *Proc. of IEEE Power Electronics Specialists Conference* 17-21 June. 2007, Orlando, FL, pp 520-526.
- J. -S. Lai, **S. -Y. Park**, S. -R. Moon, C. -L. Chen, “A High-Efficiency 5-kW Soft-Switched Power Conditioning System for Low-Voltage Solid Oxide Fuel Cells,” *Proc. Of IEEE Power Conversion Conference*, 2-5 Apr. 2007, Nagoya, Japan, pp 463-470. **Best Paper Award**

- **S. -Y. Park, J. -S. Lai, C. -L. Chen, S. -R. Moon, T. -W. Chun;** “Current Loop Control with Admittance Compensation for a Single-Phase Grid-Tie Fuel Cell Power Conditioning System,” *Proc. of IEEE Applied Power Electronics Conference* 25 Feb. – 1 Mar. 2007, Anaheim, CA, pp 654-660.

6.3 Future work

Based on the frequency domain analysis of the grid voltage disturbance, this dissertation presents a comprehensive study of a single phase grid-tie inverter control mechanism with conventional linear feedback control method. In the future, the disturbance of the grid voltage can be analyzed and its compensator can be designed with non-linear control approach.

Current control for the grid-tie inverter can be applied to various applications such as a parallel grid-tie inverter, an active filter, a distributed generation, and micrgrid inverter applications.

It is possible to use active and reactive power flow control for three-phase unity power factor correction with measured local load currents.

The proposed compensator can be utilized not only for fuel cell systems but also for photovoltaic systems with modifying power command configuration.

References

- [1] J. J. Brey, et. al., "Integration of of renewable energy sources as an optimised solution for distributed generation," in *Proc. of IEEE Industrial Electronics Society Annual Conference*, Nov. 2002, Sevilla, Spain, pp. 3355-3359.
- [2] N. W. Miller, et. al., "Dynamic modeling of GE 1.5 and 3.6 MW wind turbine-generators for stability simulations," in *Proc. of IEEE Power Engineering Society General Meeting*, July. 2003, Toronto, Canada, pp. 1977-1983.
- [3] Fuel Cell Technologies, *Technical specification operators manual for the 5kW SOFC Simulator*, U.S.DOE Report #149-R-00-001-R1, April 2005.
- [4] K. Y. Lee, "The effect of DG using fuel cell under deregulated electricity energy markets," in *Proc. of IEEE Power Engineering Society General Meeting*, June 2006, Montreal, Canada.
- [5] R. O'Hayre, et. al., "Fuel cell fundamental," John Wiley & Sons, Inc., 2006, Chapter 1.
- [6] K. W. E. Cheng, et. al., "Exploring the power conditioning system for fuel cell," in *Proc. of IEEE Power Electronics Specialists Conference*, June. 2001, Vancouver, Canada, pp. 2197-2202.
- [7] J. -S. Lai, "Power conditioning systems for renewable energies," in *Proc. of IEEE Electrical Machines and Systems*, Oct. 2007, Seoul, Korea, pp. 209-218.
- [8] F. Blaabjerg, Z. Chen, S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. on Power Electronics*, vol. 19, pp. 1184-1194, Sept. 2004.
- [9] C. Liu, A. Johnson, and J.-S. Lai, "A novel three-phase high-power soft-switched DC/DC converter for low-voltage fuel cell applications," *IEEE Trans. on Industry Applications*, vol. 4, pp. 1691-1697, Nov. 2005.

- [10] C. Liu, A. Johnson, J. –S. Lai, “Modeling and control of a novel six-leg three-phase high-power converter for low voltage fuel cell applications,” in *Proc. of IEEE Power Electronics Specialists Conference*, June, 2004, Aachen, Germany, pp. 4715 – 4721.
- [11] J. M. Carrasco, et. al., “Power-electronic systems for the grid integration of renewable energy source: a survey,” *IEEE Trans. on Industrial Electronics*, vol. 53, pp. 1002-1016, June 2006.
- [12] D. M. Brod and D. W. Novotny, “Current control of VSI-PWM Inverers,” *IEEE Trans. on Industry Applications*, vol. IA-21, pp. 562-570, May 1985.
- [13] U. Boegli and R. Ulmi, “Realization of a new inverter circuit for direct photovoltaic energy feedback into the public grid,” *IEEE Trans. on Industry Applications*, vol. IA-22, pp. 255-258, March 1986.
- [14] S. –C. Zheng, P. –Z. Wang, and L. –S. Ge, “Study on PWM control strategy of photovoltaic grid-connected generation system,” in *Proc. of IEEE Power Electronics and Motion Control Conference*, 2006.
- [15] S. Jung, Y. Bae, S. Choi, H. Kim, “A low cost utility interactive inverter for residential fuel cell generation,” *IEEE Trans. on Power Electronics*, vol 22, pp. 2293-2298, Nov. 2007.
- [16] A. Papavasiliou, et. al., “Current control of a voltage source inverter connected to the grid vai LCL filter,” in *Proc. of IEEE Power Electronics Specialist Conference*, 2007. Pp. 2379-2384.
- [17] Y. Sato, et. al., “A new control strategy for voltage-type PWM rectifiers to realize zero steady-state control error in input current A new control strategy for voltage-type PWM rectifiers to realize zero steady-state control error in input current,” *IEEE Trans. on Industry Applications*, vol 34, pp.480-486, May/June 1998.

- [18] D. N. Zmood, D. G. Holmes, and G. Bode, "Frequency domain analysis of three phase linear current regulators," in *Rec. of IEEE Industry Applications Conference*, Oct. 1999, Phoenix AZ, pp. 818-825.
- [19] D.N. Zmood and D.G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady state error," *IEEE Trans. on Power Electronics*, vol. 2, pp. 1185-1190, May 2003.
- [20] R. Teodorescu, F.Blaabjerg, U. Borup, M. Liserre, "A new control structure for grid-connected LCL PV inverters with zero steady-state error and selective harmonic compensation," in *Proc. of IEEE Applied Power Electronics Conference*, March 2004, Anaheim CA, pp. 580-586.
- [21] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Control of single-stage single-phase PV inverter," in *Proc. of Power Electronics and Application European Conference*, Dresden, 2005.
- [22] D. Sera, et. al., "Low-cost digital implementation of proportional-resonant current controllers for PV inverter applications using delta operator," in *Proc. of IEEE Industrial Electronics Society Conference*, Nov. 2005, Raleigh, NC, pp. 2517 – 2522.
- [23] G. Xiaoqiang, Z. Qinglin, and W. Weiyang, "A single-phase grid-connected inverter system with zero steady-state error," in *Proc. of IEEE Power Electronics and Motion Control Conference*, Aug 2006, Shanghai, China, pp 1-5.
- [24] G. Shen, et. al., "An improved control strategy for grid-connected voltage source inverters with a LCL filter," *IEEE Trans. on Power Electronics*, vol. 23, pp. 1899-1906, July 2008.

- [25] M. Castilla, et. al., "Linear current control scheme with series resonant harmonic compensator for single-phase grid-connected photovoltaic inverters," *IEEE Trans. on Industrial Electronics*, vol. 55, pp. 2724-2733, July 2008.
- [26] F. Liu, et. al., "Design and research on two-loop control strategy of PV grid-connected inverter with LCL filter," in *Proc. of Electrical Machines and System Conference*, 2008.
- [27] E. Jung and S. -K. Sul, "Implementation of grid-connected single-phase inverter based on FPGA," in *Proc. of IEEE Applied Power Electronics Conference*, Washington. DC, Feb 2009, pp. 889-893.
- [28] G. Shen, et. al., "A new current feedback PR control strategy for grid-connected VSI with an LCL filter," in *Proc. of IEEE Applied Power Electronics Conference*, Feb. 2009, Washington, DC, pp. 1564-1569.
- [29] R. Zhang, et. al., "A grid simulator with control of single-phase power converters in D-Q rotating frame," in *Proc. of IEEE Power Electronics Specialists Conference*, Cairns, Australia, June 2002, pp. 1431 -1436.
- [30] R-Y Kim; S-Y Choi; I-Y Suh; "Instantaneous control of average power for grid tie inverter using single phase D-Q rotating frame with all pass filter," in *Proc. of IEEE Industrial Electronics Society Conference*, Busan, Korea, Nov. 2004, pp. 274 - 279.
- [31] H. Cha and S. Lee, "Design and implementation of photovoltaic power conditioning system using a current based maximum power point tracking," in *Rec. of IEEE Industry Application Society Conference*, Oct. 2008, Edmonton Alta, pp. 1-5.
- [32] G. Franceschini, et. al., "Synchronous reference frame grid current control for single-phase photovoltaic converters," in *Rec. of IEEE Industry Application Society Conference*, Oct. 2008, Edmonton Alta, pp. 1-7.

- [33] N. Patcharaprakiti and S. Premrudeepreechacharn, "Maximum power point tracking using adaptive fuzzy logic control for grid-connected photovoltaic system," in *Proc. of IEEE Power Engineering Society Winter Meeting*, Jan. 2002, pp. 372-377.
- [34] B. Yu and L. Chang, "Improved predictive current controlled PWM for single-phase grid-connected voltage source inverters," in *Proc. of IEEE Power Electronics Specialists Conference*, June 2005, Recife, pp. 231-236.
- [35] E. Shimada and T. Yokoyama, "Current control method using voltage deadbeat control with multi sampling pulse compensation for single phase utility interactive inverter with FPGA based hardware controller," in *Proc. of International Telecommunications Conference*, Sept. 2005, Berlin, Germany, pp. 369-374.
- [36] H. M. Kojabadi, et. al., "A novel DSP-based current-controlled PWM strategy for single phase grid connected inverters," *IEEE Trans. on Power Electronics*, vol. 21, pp 985-993, July 2006.
- [37] I. J. Gabe and H. Pinheiro, "Multirate State Estimator Applied to the Current Control of PWM-VSI Connected to the Grid," in *Proc. of IEEE Industrial Electronics Society Conference*, Nov. 2008, Orlando, FL, pp. 2189-2194.
- [38] S. Mariethoz, A. G. Beccut, and M. Morari, "Analysis and optimal current control of a voltage source inverter connected to the grid through an LCL filter," in *Proc. of IEEE Power Electronics Specialists Conference*, June. 2008, Rhodes, Greece, pp. 2132-2138.
- [39] S. Buso, et. al., "A dead-beat adaptive hysteresis current control," *IEEE Trans. on Industry Applicatinos*, vol. 36, pp. 1174-1180, July 2000.

- [40] K. Samangkool and S. Premrudeepreechacharn, "Maximum power point tracking using neural networks for grid-connected photovoltaic system," in *Proc. on Future Power Systems*, Nov. 2005, Amsterdam.
- [41] Krismadinata, N. A. Rahim, and J. Selvaraj, "Implementation of hysteresis current control for single-phase grid connected inverter," in *Proc. of Power Electronics and Drive Systems*, Nov. 2007, Bangkok, pp. 1097-1101.
- [42] N. A. Rahim, J. Selvaraj, and Krismadinata, "Hysteresis current control and sensorless MPPT for grid-connected photovoltaic systems," in *Proc. on International Symposium on Industrial Electronics*, June. 2007, Vigo, pp. 572-577.
- [43] G. Wang, et. al., "The design of constant frequency hysteresis current controller with voltage space vector in PV grid-connected inverter," in *Proc. of automation congress*, Sept. 2008, Hawaii, HI, pp. 1-5.
- [44] M. Carpita and M. Marchesoni, "Experimental study of a power conditioning system using sliding mode control," *IEEE Trans. on Power Electronics*, vol. 11, pp. 731-742, September 1996.
- [45] D. Biel, E. Fossas, and F. Guinjoan, "Application of sliding mode control to the design of a buck-based sinusoidal generator," in *Proc. on International Symposium Industrial Electronics*, July. 1999, Bled, pp. 358-361.
- [46] R. R. Ramos, D. Biel, and E. Fossas, "A fixed-frequency quasi-sliding control algorithm: application to power inverters design by means of FPGA implementation," *IEEE Trans. on Power Electronics*, vol. 18, pp. 344-355, January 2003.
- [47] M. Dai, et. al., "Power flow control of a single distributed generation unit with nonlinear local load," in *Proc. of Power Systems Conference*, Oct. 2004, pp. 398-403.

- [48] J. J. Megroni, et. al., "Control of a buck inverter for grid-connected PV systems: a digital and sliding mode control approach," in *Proc. on International Symposium Industrial Electronics*, June. 2005, pp. 739-744.
- [49] R. -J. Wai, W. -H. Wang, "Grid-connected photovoltaic generation system," *IEEE Trans. On circuits and systems*, vol. 55, pp. 953-954, April 2008.
- [50] N. Abdel-Rahim, J. E. Quaicoe, "Indirect current control scheme for a single-phase voltage-source utility interface inverter," in *Proc. of IEEE Electrical and Computer Engineering Canadian Conference*, Sept. 1993, Vancouver, Canada, pp. 305-308.
- [51] N. Uemura, T. Yokoyama, "Current control method using voltage deadbeat control for single phase utility interactive inverter," in *Proc. of IEEE International Telecommunications Energy Conference*, Oct. 2003, Yokohama, Japan, pp. 40-45.
- [52] K. Toyama, et. al., "Repetitive control of current for residential photovoltaic generation system," in *Proc of IEEE Industrial Electronics Society Conference*, Oct. 2000, Nagoya, Japan, pp. 741-745.
- [53] P. C. Loh and D. G. Holmes, "Analysis of multi loop control strategies for LC/CL/LCL-filtered voltage-source and current-source Inverters," in *Rec. of IEEE Industry Applications Conference*, Oct. 2003, pp. 1778-1785.
- [54] M. Ciobotaru, R. Teodorescu, F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *Proc. of IEEE Power Electronics Specialists Conference*, Jeju Korea, June 2006, pp. 1511-1516.
- [55] K. P. Louganski and J.-S. Lai, "Current phase lead compensation in single-phase PFC boost converters with a reduced switching frequency to line frequency ratio," in *Proc. of IEEE Applied Power Electronics Conference*, March 2006, Dallas, TX, pp. 261 -267.

- [56] L. N. Arruda, S. M. Silva, and B. J. C. Filho, "PLL Structures for Utility Connected Systems," in *Rec. of IEEE Industry Application Society Conference*, Oct. 2001, Chicago, IL, pp. 2655- 2660.
- [57] Q. Zeng, L. Chang, "Improved current controller based on SVPWM for three-phase grid-connected voltage source inverters," in *Proc. of IEEE Power Electronics Specialists Conference*, Jun. 2005, Recife, Brasil, pp. 2912-2917.
- [58] Y. Lang, et. al., "Nonlinear feedforward control of three-phase voltage source converter," in *Proc. of International Symposium on Industrial Electronics*, July. 2006, Quebec, Canada, pp. 1134-1137.
- [59] J. M. Chang, W. N. Chang, S. J. Chung, "Single-phase grid-connected PV system using three-arm rectifier-inverter," *IEEE Trans. on Aerospace and Electronic Systems*, vol. 42, pp. 211-219, Jan. 2006.
- [60] Q. Zhang, et. al., "Study on grid connected inverter used in high power wind generation system," *Rec. of IEEE Industry Applications Conference*, Oct. 2006, Tampa, FL, pp. 1053-1058.
- [61] M. Prodanovic, T. C. Green, "Control of power quality in inverter-based distributed generation," in *Proc. of IEEE Industrial Electronics Society Conference*, Nov. 2002, Sevilla, Spain, pp. 1185-1189.
- [62] T. Erika, D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. on Power Electronics*, vol. 18, pp. 888-895, May. 2003.

- [63] T. Abeyasekera, et. al., "Suppression of line voltage related distortion in current controlled grid connected inverters," *IEEE Trans. on Power Electronics*, vol. 20, pp. 1393-1401, Nov. 2005.
- [64] K. P. Louganski and J.-S. Lai, "A 20-kW, 10-kHz, single-phase multilevel active-front-end converter with reactive power control," in *Rec. of IEEE Industry Application*, Oct. 2006, Tampa, FL, pp. 576-582.
- [65] S. -Y. Park, et. al., "Current loop control with admittance compensation for a single-phase grid-tie fuel cell power conditioning system," in *Proc. of IEEE Applied Power Electronics Conference*, Feb. 2007, Anaheim, CA, pp. 654-660.
- [66] S. -Y. Park, et. al., "Admittance Compensation in Current Loop Control for a Grid-Tie LCL Fuel Cell Inverter," *IEEE Trans. on Power Electronics*, vol.23, pp.1716-1723, July. 2008.
- [67] M. Liserre, A. Dell'Aquila, F. Blaabjerg, "Genetic algorithm-based design of the active damping for an LCL-filter three-phase active rectifier," *IEEE Trans. Power Electronics*, vol. 19, pp. 76-86, Jan. 2004.
- [68] B. Bolsens, et. al., "Model-based generation of low distortion currents in grid-coupled PWM-inverters using an LCL output filter," *IEEE Trans. on Power Electronics*, vol. 21, pp. 1032-1040, Jul. 2006.
- [69] M. Liserre, R. Teodorescu, F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Trans. on Power Electronics*, vol. 21, pp. 263-272, Jan. 2006.
- [70] M. L. Doumbia, K. Agbossou, M. Dostie, "Power transfer analysis in a utility-interconnected fuel cell distributed generator," in *Proc. of IEEE Industrial Electronics Conference*, Nov. 2006, Paris, France, pp. 4331-4336.

- [71] R.J. Wai, R.-Y. Duan, "High-efficiency power conversion for low power fuel cell generation system," *IEEE Trans. on Power Electronics*, vol.20, pp. 847-856, July. 2005.
- [72] Z.B. Shen, E.F. El-Saadany, "Novel Interfacing for Fuel Cell Based Distributed Generation," in *Proc. of IEEE Power Engineering Society General Meeting*, June. 2007, Tampa, FL, pp.1-5.
- [73] S. K. Mazumder, et. al., "Solid-oxide-fuel-cell performance and durability: resolution of the effects of power-conditioning systems and application loads," *IEEE Trans. on Power Electronics*, vol.19, pp.1263-1278, Sept. 2004.
- [74] M. Saitou, and T. Shimizu, "Generalized Theory of Instantaneous Active and Reactive Powers in Single-Phase Circuits based on Hilbert Transformer," in *Proc. of IEEE Power Electronics Specialists Conference*, June 2002, Cairns, Australia, pp. 1419-1424.
- [75] B. Dobrucky, et. al., "Single-phase power active filter and compensator using instantaneous reactive power method," in *Proc. of IEEE Power Conversion Conference*, April 2002, Osaka Japan, pp. 167-171.
- [76] J. A. Momoh, "Smart grid design for efficient and flexible power networks operation and control," in *Proc Power Systems Conference*, March 2009, Seattle, WA, pp. 1-8.
- [77] J. Fan and S. Borlase, "The Evolution of Distribution," *IEEE Power and Energy Magazine*, vol. 7, pp. 63-68, March/April 2009.
- [78] C. W. Potter, A. Archambault, and K. Westrick, "Building a smarter smart grid through better renewable energy information," in *Proc. Power Systems Conference*, March 2009, Seattle, WA, pp. 1-5.
- [79] A. V. Jouanne and B. Banerjee, "Assessment of Voltage Unbalance," *IEEE Trans. Power Delivery*, vol. 16, pp. 782-790, Oct. 2001.

- [80] V. B. Bhavaraju and P. N. Enjeti, "An Active Line Conditioner to Balance Voltage in a Three-Phase System," *IEEE Trans.on Industry Applications*, vol. 32, pp. 287-293, March/April. 1996.
- [81] Q. Zeng, L. Chang, P. Song, "SVPWM-based current controller with grid harmonic compensation for three-phase grid-connected VSI," in *Proc. of IEEE Power Electronics Specialists Conference*, Jun 2004, Aachen, Germany, pp. 2494-2500.
- [82] L. A. Serpa, et al., "A Modified Direct Power Control Strategy Allowing the Connection of Three-Phase Inverters to the Grid Through LCL Filters," *IEEE Trans. on Industry Applications*, vol. 43, pp. 1388-1400, Sep/Oct. 2007
- [83] Z. Wang and L. Chang, "A Novel Vdc Voltage Monitoring and Control Method for Three-Phase Grid-Connected Inverter," in *Proc. IEEE Power Electronics Specialists Conference*, June. 2007, Orlando, FL, pp. 1221-1226.
- [84] H. S. Bae, et al., "Current Control Design for a Grid Connected Photovoltaic/Fuel Cell DC-AC Inverter," in *Proc. IEEE Applied Power Electronics Conference*, Feb. 2009, Washington, DC, pp. 1945-1950.
- [85] F. Wang, et al., "Sequence-Decoupled Resonant Controller for Three-Phase Grid-Connected Inverters," in *Proc. IEEE Applied Power Electronics Conference*, Feb. 2009, Washington, DC, pp. 1306-1312.
- [86] P. Verdelho and G. D. Marques, "Four-wire current-regulated PWM voltage converter," *IEEE Trans. on Industrial Electronics*, vol. 45, pp. 761-770, Oct. 1998
- [87] F. Wang, J. L. Duarte, and M. Hendrix, "Control of grid-interfacing inverters with integrated voltage unbalance correction," in *Proc. IEEE Power Electronics Specialists Conference*, June 2008, Rhodes, Greece, pp. 310-316.

- [88] S. -Y. Park, C. -L, Chen, and J. -S. Lai, "A Wide-Range Active and Reactive Power Flow Controller for a Solid Oxide Fuel Cell Power Conditioning System," *IEEE Trans. on Power Electronics*, vol. 23, pp. 2703-2709, Nov. 2008.
- [89] A. Lorduy, et. al., "Novel Simplified Controller for Three Phase Grid Connected Inverter Based on Instantaneous Complex Power," in *Proc. IEEE Applied Power Electronics Conference*, Feb. 2009, Washington, DC, pp. 1306-1312.