Optimization of Power MOSFET for High-Frequency Synchronous Buck Converter

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Abstract

Evolutions in microprocessor technology require the use of a high-frequency synchronous buck converter (SBC) in order to achieve low cost, low profile, fast transient response and high power density. However, high frequency also causes more power loss on MOSFETs. Optimization of the MOSFETs plays an important role in the system performance.

Circuit and device modeling is important in understanding the relationship between the device parameters and the power loss. The gate-to-drain charge (Q_{gd}) is studied by a novel nonlinear model and compared with the simulation results. A new switching model is developed, which takes into account the effect of parasitic inductance on the switching process. Another model for dv/dt-induced false triggering-on relates the false-trigger-on voltage with the parasitic elements of the device and the circuits.

Some techniques are proposed to reduce the simulation time of FEA in the circuit simulation. Based on this approach, extensive simulations are performed to study the switching performance of the MOSFET with the effect of the parasitic elements. Directed by the analytical models and the experience acquired in the circuit simulation, the MOSFET optimization is realized using FEA. Different optimization algorithms are compared. The experimental results show that the optimized MOSFETs surpass the mainstream commercialized products in both cost and performance.

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To my parents and wife

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Chapter 1 Introduction

1.1 Background

The most important factors in achieving higher speed and greater complexity for the microprocessor are the reduction of the minimum device feature size and the increase of the components per chip [E1]. Such advanced processors require lower supply voltages and produce large, fast changes in the current they draw, which in turn demands special power supplies to provide lower voltages with higher current capabilities [D1]-[D5]. There are several topology candidates for such power supply [D6]-[D9]. The most widely used in the industry is the multi-phase Synchronous Buck Converter (SBC), because it is simpler and more cost effective.

The large dynamic loads with high current slew rates, which occur when the system switches from the active mode to the sleep mode and vice versa, make the parasitic impedance of the power supply connection to the load have a dramatic effect on the power supply voltage. In order to minimize the effects of the interconnection parasitics, today’s power supply must be a point-of-load on-board power supply, which is powered up from the existing voltages available in the system and is required to have high power densities because the space of the power supply on the motherboard is very limited [D10]-[D11].

The high operating frequency of the power supply can achieve high power density and fast transient response [D12]-[D16]. However, the power loss on the semiconductor device also increases with the frequency. Such loss is converted into heat thereby causing the temperature to rise, which reduces the system reliability and can even kill the device if the temperature is too high [E2]. Indeed, it is the performance of the semiconductor device that determines the upper limit of the operating frequency of the power supply. Because it is impractical to adequately cool the converter elements on the motherboard, the key solution for reducing the loss on the semiconductor device relies on the device technology itself.

From the device standpoint, both the power bipolar transistor and the metal-oxide-semiconductor field-effect-transistor (MOSFET) can be used in the power supply. However, studies show that the MOSFET is a better choice than the bipolar transistor for such applications. First of all, the power MOSFET is a voltage-controlled device. The high input impedance of the MOSFET makes its gate drive circuitry much simpler than that of bipolar transistor. For a short duration, power MOSFETs can withstand the simultaneous application of high voltage and current without undergoing fatal failure for a short duration. Further, the MOSFETs can be easily paralleled because their on-resistance increases with increasing temperature.

Another power device candidate for VRM application is the junction field-effect transistor (JFET). In order to achieve low on-resistance, the JFET is a device that is normally on or operating in depletion mode, which means that a positive voltage must be applied on the gate terminal to turn the device off. This is the main drawback of the JFET, because it requires a more complex drive circuit, which is not compatible with the prevailing system.

1.2 Dissertation Outline

This dissertation is devoted to the optimization of the power MOSFET for use in the high-frequency DC-DC converter. Because there are many device parameters related to the optimization, a good qualitative insight into the device performance in the circuit is indispensable in understanding and simplifying the optimization process. Therefore, several analytical models are developed and presented before the introduction of the Finite Element Analysis FEA method. The dissertation is arranged as follows.

There are seven chapters including an introduction. Chapter 2 describes the background information about the power MOSFET and DC-DC buck converter.

Chapter 3 presents three analytical models regarding the switching performance of the trench MOSFET.

Chapter 4 investigates the performance of the MOSFET in the buck converter using FEA. An approach for extracting a detailed loss breakdown of the MOSFET is proposed. Analysis of the effect of the parasitic components on the loss is performed.

Chapter 5 proposes an economical Integrated Circuit (IC) process for the monolithic integration of the buck converter. In addition, a monolithic design is presented.

Chapter 6 discusses the automated optimization procedures. Experimental results are presented to verify the optimization concept.

Finally, conclusions of this work and suggestions for future work are outlined in Chapter 7.

1.3 Simulation Tools

In this dissertation, the FEA models of the device are constructed and calculated by commercial software. Because a lot of results presented in this dissertation are based on simulations, it is necessary to provide a brief description of the Technology Computer Aided-Design (TCAD) tools from Avant! Corporation. The TCAD has three main functions: device simulation, process simulation and visualization.

1) The program medici™ [E3] simulates the electrical behavior of semiconductor devices by solving the following basic Equations.

Poisson's Equation:

$$\nabla\vec{D} = \rho(x,y,z)\,, \tag{1.1}$$

where $\vec{D}$ is the displacement vector and $\rho(x,y,z)$ is the total electric charge density.

Continuity Equations:

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\cdot\nabla\vec{J}_n\,, \tag{1.2}$$

and

$$\frac{\partial p}{\partial t} = G_p - U_p + \frac{1}{q}\cdot\nabla\vec{J}_p\,, \tag{1.3}$$

where n is the electron density, p is the hole density, $\vec{J}_n$ is the electron current density, $\vec{J}_p$ is the hole current density, and G_n (U_n) and G_p (U_p) are the electron and hole generation (recombination) rates respectively.

Current-Density Equations:

$$\vec{J}_n = q\mu_n n\vec{E} + qD_n\nabla n\,, \tag{1.4}$$

and

$$\vec{J}_p = q\mu_p p\vec{E} - qD_p\nabla p\,, \tag{1.5}$$

where μ_n is the electron mobility, μ_p is the hole mobility, and D_n and D_p are diffusion constants of the electron and the hole respectively.

2) The program tsuprem4™ [E4] is a very powerful two-dimensional simulator for simulating the process steps employed in the fabrication of silicon devices. The major process steps include epitaxial growth, diffusion, oxidation, ion implantation, deposition, metallization and etching. The output information generated by the simulator includes boundaries of various materials in the structure and the impurity distributions of each material. Such information can be fed into the device simulator medici™ to evaluate the electrical performance of the device.

3) The program tv2d™ is the visualization tool for simulations. It can plot the cross-section of the device structure, showing the doping profile, electron and hole densities, electric field, current flowline, etc., as required. Moreover, tv2d™ can display either the current and voltage waveforms generated by the device or a mixed-mode circuit simulation performed using medici™.

Chapter 2 Fundamentals of the Power MOSFET and Buck Converter

2.1 Introduction to the Power MOSFET

2.1.1 Fundamentals of the Basic MOS Device

The basic structure of an n-type MOSFET [E5] [E6] is shown in Fig. 2.1, where n^+ represents heavily doped (low resistivity) n-type silicon. The difference between the source and drain is that the source n^+ is shorted to the P-substrate by the source metal. This is important for fixing the potential of the P-substrate for normal device operation. For power applications, the MOSFET is required to be off when the voltage on the gate is 0. The turn-on of the MOSFET relies on the formation of a conductive layer on the surface of the semiconductor, when a positive (negative) voltage is applied on the gate of the n (p) type MOSFET. For the n-type MOSFET, as V_g increases, electrons flow to the interface between the oxide and silicon, and a charge layer is formed to provide a "channel" for the current. When this phenomenon occurs, the value of V_g is called the threshold voltage (V_{th}). In semiconductor physics, the threshold voltage is defined as the applied gate voltage required to make the surface of the silicon as much n-type as the substrate is p-type. The threshold voltage can be written as

$$V_{th} = 2\phi_{fp} + \frac{Q_{dep} - Q_{ss}}{C_{ox}} + \phi_{ms}\,, \tag{2.1}$$

where

$$\phi_{fp} = \frac{kT}{q}\ln\frac{N_a}{n_i}\,, \tag{2.2}$$

$$Q_{dep} = \sqrt{4q\varepsilon_{si}\phi_{fp}N_a}\,, \tag{2.3}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}\,. \tag{2.4}$$

The definitions of the other symbols are:

1) k is the Boltzmann's constant: $k=1.38\times10^{-23}$ J/K,

2) T is the absolute temperature,

3) q is the electronic charge: $q=1.60\times10^{-19}$ C,

4) N_a is the acceptor doping concentration of the substrate,

5) N_i is the intrinsic carrier concentration of the silicon,

6) ε_{si} is the dielectric constant of silicon: $\varepsilon_{si}=1.03\times10^{-12}$ F/cm,

7) Q_{ss} is the fixed charge located in the oxide close to the oxide-silicon interface,

8) ε_{ox} is the dielectric constant of oxide: $\varepsilon_{ox}=3.45\times10^{-12}$ F/cm, and

9) T_{ox} is the thickness of the gate oxide.

The resistance from drain to source of the MOSFET is determined by the property of the charge layer in the channel, and can be expressed as

$$R_{ch} = \frac{L_g T_{ox}}{W_g \mu_{nch} \varepsilon_{ox} (V_{gs} - V_{th})}, \tag{2.5}$$

where μ_{nch} is the mobility of the electron in the channel. The definition of L_g (channel length) and W_g (channel width) are shown in Fig. 2.1.

2.1.2 Structures of the Power MOSFET

The basic structure shown in Fig. 2.1 is not suitable for high-voltage applications, because in order to achieve low resistance expressed in Equation (2.5), shorted channel length (L_g) and thinner gate oxide (T_{ox}) are required. However, both L_g and T_{ox} are related to the breakdown voltage of the MOSFET. If L_g is too small, the junction breakdown or punch-through of N^+PN^+ will occur; if T_{ox} is too thin, the oxide directly adjacent to the drain can be destroyed by the electric field. To alleviate the effect of the electrical filed on the gate oxide for high-voltage applications, the following structures have been developed [E7].

1) Lateral Diffusion MOSFET (LDMOS)

Compared to the structure of the basic MOSFET, LDMOS [A16]-[A18](Fig. 2.2) has an additional lightly doped (n^-) region between the oxide and the drain. Because most of the voltage applied on the drain is supported by the n^- drift region, the LDMOS can withstand high voltage with thinner gate oxide and shorter channel length. However, like the basic MOSFET, the current of the LDMOS still flows on the surface of the silicon, the utility of the silicon is low, and the specific resistance (resistance per area) is relatively high. In vertical power MOSFETs, the n^- drift region is located inside the silicon. Therefore, a cross-section of the current path is enlarged without sacrificing the silicon area.

2) Power VMOSFET (Fig. 2.3)

The name VMOSFET is derived from the V-shaped groove along which current flows. Although the VMOSFET was the first commercialized structure of the power MOSFET, it was replaced by the Double-diffusion MOSFET (DMOSFET) because of the high electrical1 field at the tip of the V-groove.

3) Power DMOSFET (Fig. 2.4)

When V_g is higher than the threshold voltage and V_{ds} is positive, the electron current of the MOSFET travels horizontally through the channel and then vertically to the drain. A more direct, shorter current path can be achieved if the channel is orientated vertically instead of along the silicon surface. This idea is realized by the structure of the UMOSFET.

4) Power UMOSFET (Fig. 2.5)

Like the VMOSFET, the name UMOSFET is also derived from the U-shaped groove formed in the gate region. Compared to the DMOSFET, the UMOSFET [A1]-[A5] has no JFET region and has higher channel density to significantly reduce the on-resistance of the device. Moreover, the UMOSFET has no sharp oxide tip (as exists in the VMOSFET), because the corners of the gate oxide located in the n-drift region can be rounded by isotropic etching. In order to prevent the catastrophic destruction of the gate oxide due to the electrical crowding at the corner of the trench, the P-body is usually designed to be deep enough and the doping concentration at the bottom of the P-body is high enough to ensure that the voltage breakdown occurs first at the junction of the P-body and in the N^- drift region. Therefore, the voltage can be clamped to save the gate oxide. In the rest of this dissertation, the discussion will focus on the UMOSFET. The important electrical performances of the UMOSFET [C1]-[C4] are reviewed in the next two sections.

2.1.3 Forward Blocking of the UMOSFET

Before the discussion of the forward blocking of the UMOSFET, the basic theory of diode breakdown must be reviewed to provide some background information.

For an ideal parallel-plane diode, the dominant breakdown mechanism is the impact ionization effect. Because the ionization coefficients strongly depend on the electric field, the diode breakdown occurs when a high electric field exists inside the structure. The maximum electric field is usually called the critical electric field and is given by

$$E_c = 4010 N^{1/8}, \tag{2.6}$$

where N is the doping concentration of the lightly doped silicon.

Ignoring the build-in potential for abrupt junction, the maximum electric field can be related to the applied voltage by

$$E_m = \sqrt{\frac{2qNV}{\varepsilon_{si}}}. \tag{2.7}$$

By substituting the critical electric field Equation (2.6) into Equation (2.7), the breakdown voltage is found to be

$$BV = 5.34 \times 10^{13} N^{-3/4}. \tag{2.8}$$

Then, the maximum depletion length at the point of breakdown is

$$L_{\max} = 2.67 \times 10^{10} N^{-7/8}. \tag{2.9}$$

If the total length of the drift region is less than L_{max}, the punch-through will occur as shown in Fig. 2.6, and the breakdown voltage is given by

$$BV = E_c L_n - \frac{qNL_n^2}{2\varepsilon_{si}}. \tag{2.10}$$

For a given breakdown voltage, Equation (2.10) shows that there are many combinations of the depletion length L_n and the doping concentration N. The root of L_n in Equation (2.10) is

$$L_n = \frac{\varepsilon_{si} E_c - \sqrt{\varepsilon_{si}^2 E_c^2 - 2\varepsilon_{si} qN \cdot BV}}{qN}. \tag{2.11}$$

Considering E_c as a function of N (2.6), (2.11) can be rewritten as

$$L_n = \frac{4010\varepsilon_{si} N^{1/8} - \sqrt{1.6\times10^7 \varepsilon_{si}^2 N^{1/4} - 2\varepsilon_{si} qN \cdot BV}}{qN}. \tag{2.12}$$

In principle, the UMOSFET can be designed as a punch-through-type device as long as the doping concentration of the drift region is less than

$$N_{\max} = \left(\frac{BV}{5.34\times10^{13}}\right)^{-4/3}, \tag{2.13}$$

which is derived from Equation (2.8).

As mentioned in section 2.1.1, because the bottom of the P-body is heavily doped, the breakdown voltage of the UMOSFET is determined by the abrupt junction of the P-body and the N^- drift region. When a positive voltage is applied to the drain of the UMOSFET, the voltage is mainly supported by the depletion layer of the drift region.

2.1.4 Specific On-resistance of the UMOSFET

The specific on-resistance of the UMOSFET is the resistance per unit area between the drain and source terminal in the on state. The simulated current flow of the UMOSFET is shown in Fig. 2.7. The main resistance components of the UMOSFET are the channel, the drift region and the substrate.

2.1.4.1 Specific Channel resistance

The definition of the UMOSFET's channel resistance is the same as that of the basic MOSFET. Therefore, the specific channel resistance can be derived from Equation (2.5), as follows:

$$R_{spch} = \frac{(W_m + W_t)L_g \varepsilon_{ox}}{2\mu_{nch} T_{ox}(V_{gs} - V_{th})}, \tag{2.14}$$

where W_m and W_t are the width of mesa and trench, respectively (Fig. 2.6).

2.1.4.2 Specific resistance of drift region

As shown in Fig. 2.6, because the current spreads from the channel into the drift region, the drift region resistance is not directly proportional to L_n or $1/W_m$. If we assume that the current-spreading angle is 45 degree, a reasonably accurate model can be expressed as

$$R_{dft} = \frac{1}{qN\mu_n}[\frac{W_m + W_t}{2}\ln\frac{W_m + W_t}{W_t} + (L_n - \frac{W_m}{2})], \tag{2.15}$$

where $q = 1.6 \times 10^{-19} C$ is the electronic charge, μ_n is the electron mobility of silicon in the N^- drift region (the typical value of μ_n is 1350 $cm^2/V.s$), and N is the doping concentration in the N^- drift region.

There are two sections in Equation (2.15). The first is contributed by the current spreading at a 45-degree angle; the second is associated with the drift region, the cross-section of which is equal to the pitch. As discussed in section 2.1.2, the length of the drift region L_n is a function of the breakdown voltage BV and the doping concentration N, as shown in Equation (2.12). Substitution of (2.12) into (2.15) yields

$$R_{dft} = \frac{1}{qN\mu_n}[\frac{W_m + W_t}{2}\ln\frac{W_m + W_t}{W_t} + \frac{4010\varepsilon_{si}N^{1/8} - \sqrt{1.6\times 10^7 \varepsilon_{si}^2 N^{1/4} - 2\varepsilon_{si} qN \cdot BV}}{qN} - \frac{W_m}{2}]. \tag{2.16}$$

The relationship between the doping concentration and the specific resistance of the drift region is illustrated in Fig. 2.8. The calculation shows that the punch-through type of power UMOSFET has a higher resistance than that of the non-punch-through power MOSFET.

2.1.4.3 Specific substrate resistance

The contribution to the specific resistance arising from the current through the heavily doped substrate is simply equal to

$$R_{spsb} = \rho_{sb} L_{sb} , \tag{2.17}$$

where ρ_{sb} is the resistivity of the substrate. The typical values of ρ_{sb} and L_{sb} are 2 mΩ.cm and 200 μm. For a low voltage, high-density UMOSFET, substrate resistance can be more than 20% of the total resistance.

In reality, the package resistance [C22]-[C27] is another important component. The typical value of a state-of-the-art package like LFPAK is about 0.8 mΩ. Currently, the synchronous MOSFET (low-side MOSFET) in the synchronous buck converter is lower than 4 mΩ [A8]-[A15]. This means that the package resistance is not negligible in terms of on-resistance or power loss.

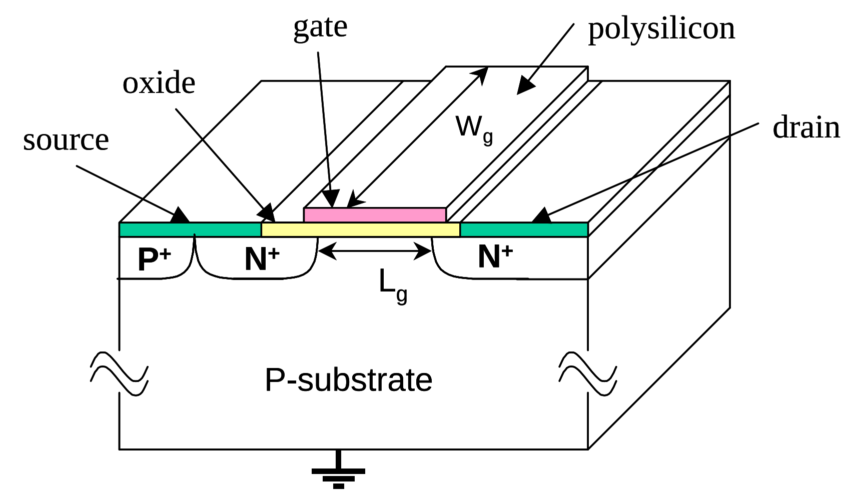


Fig. 2.1 Basic structure of an n-type MOSFET.

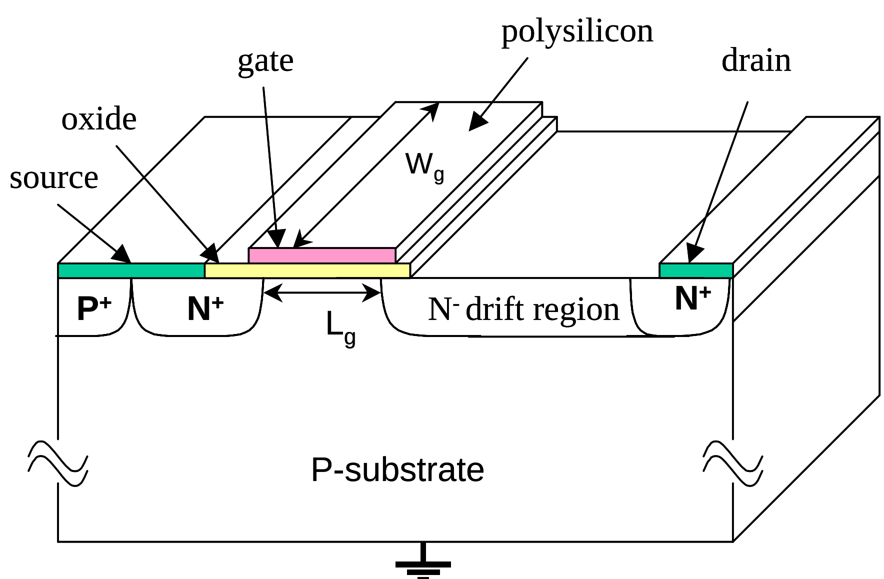


Fig. 2.2 Basic structure of LDMOS.

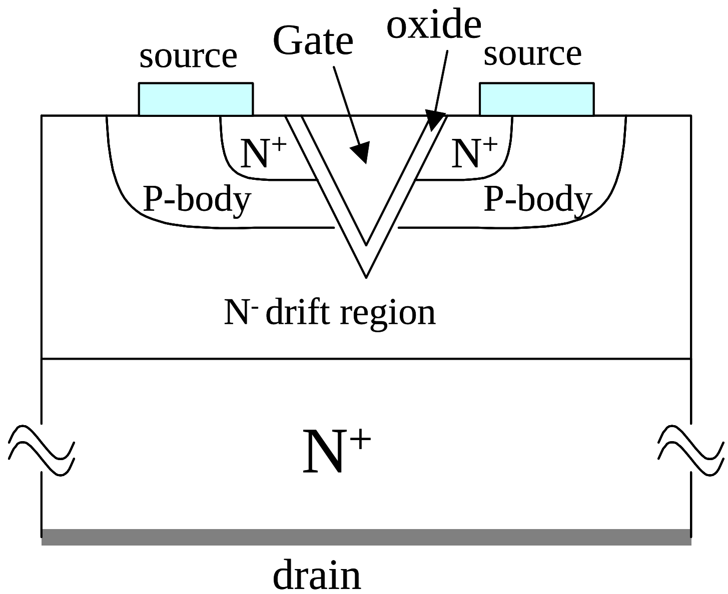


Fig. 2.3 Structure of VMOSFET.

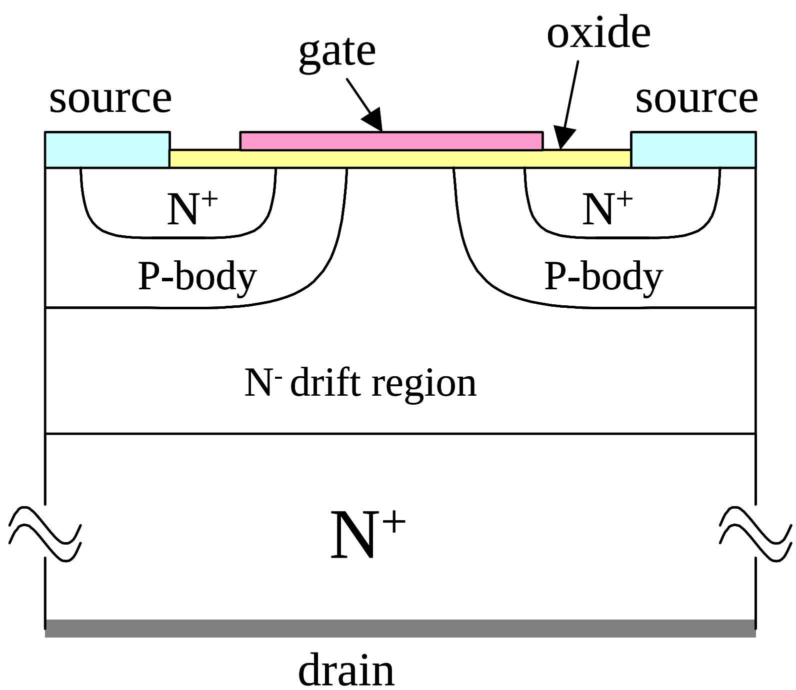


Fig. 2.4 Structure of DMOSFET.

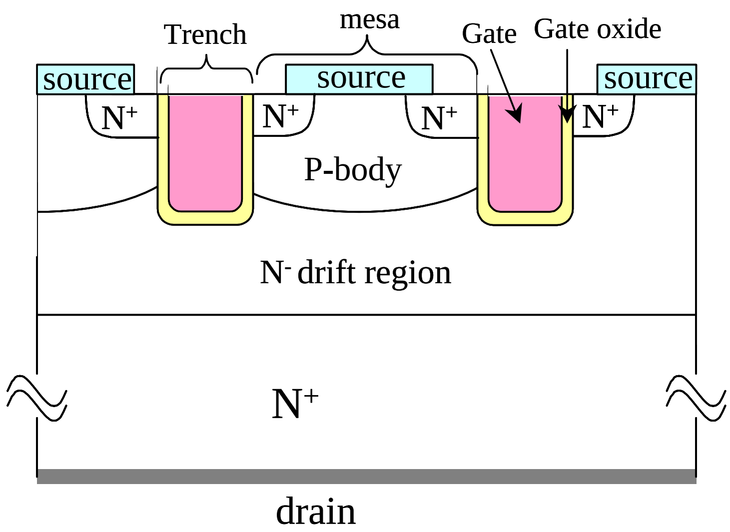


Fig. 2.5 Structure of UMOSFET.

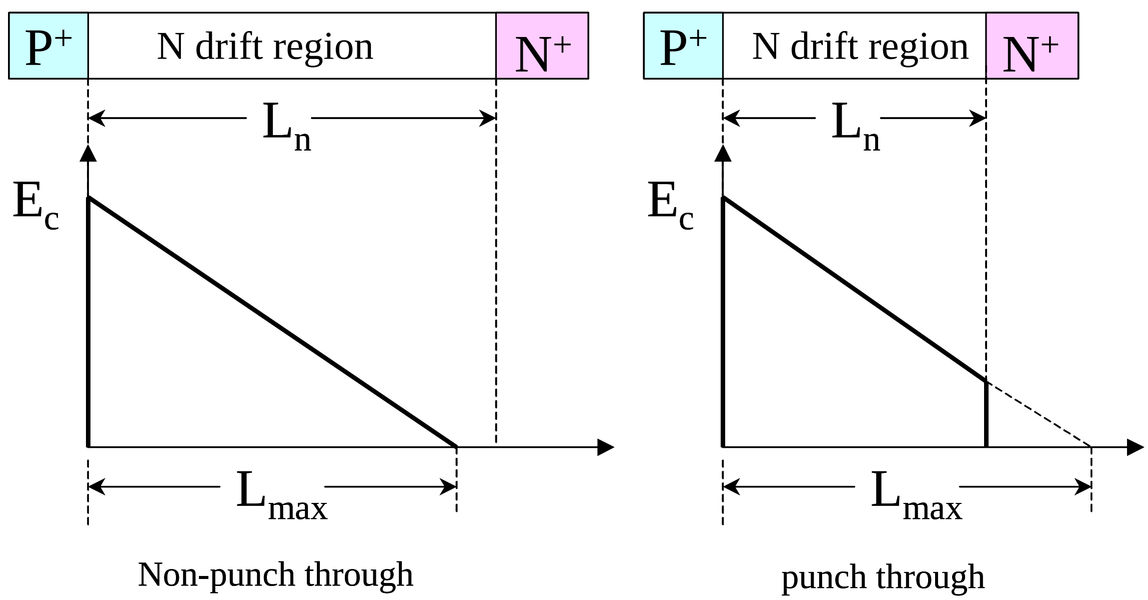


Fig. 2.6 Distribution of the electric field in the abrupt diode under different breakdown conditions.

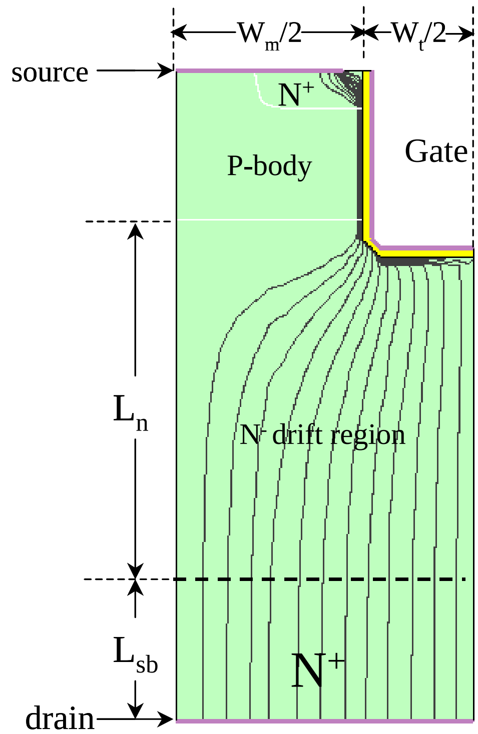


Fig. 2.7 Current flowline in UMOSFET.

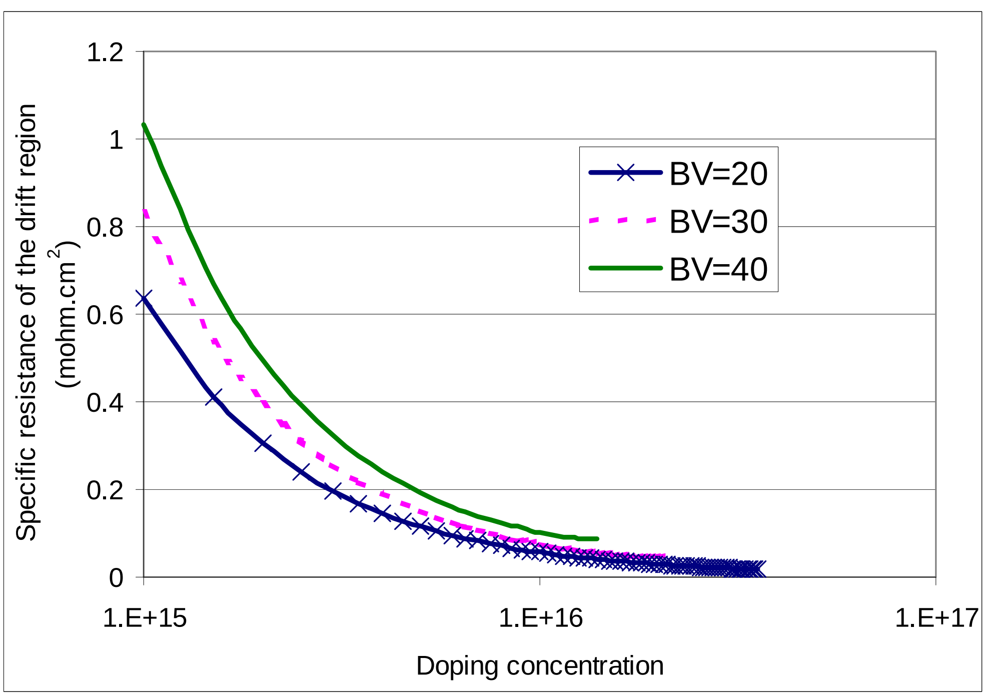


Fig. 2.8 Specific resistance of the drift region.

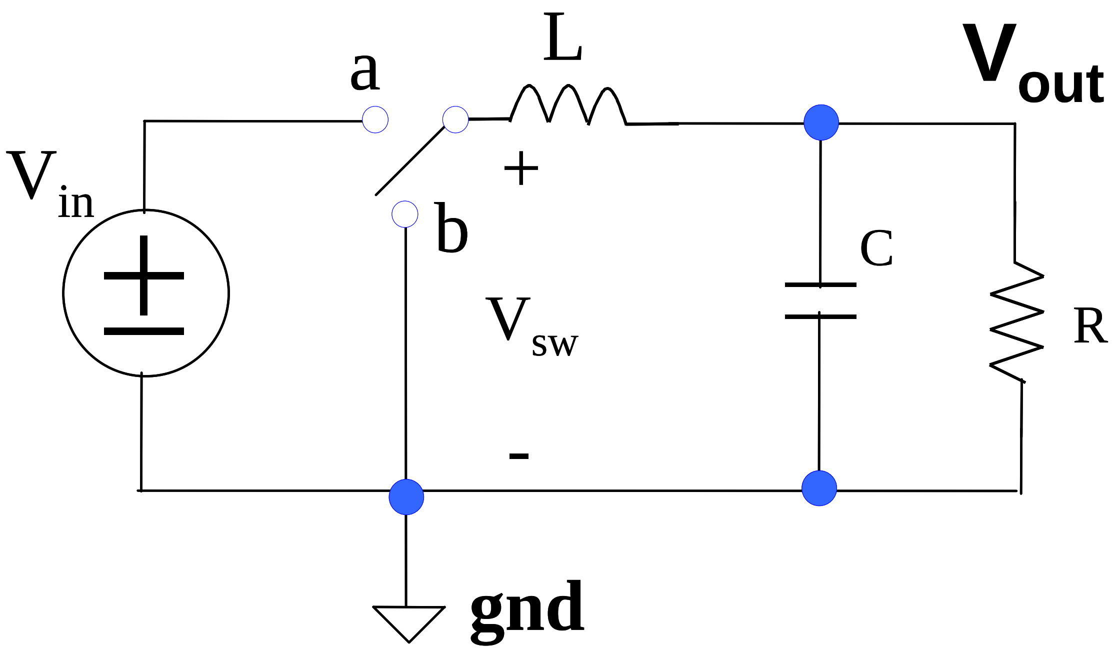


Fig. 2.9 Basic topology of the buck converter.

2.2 Introduction to the Buck Converter

2.2.1 Application Background in Personal Computers

The basic function of the DC-DC converter is to change the DC input voltage to another DC output voltage. Depending on the application, the input voltage can be lower (buck converter) or higher (boost converter) than the input voltage. In personal computers (PCs), the value of the output voltage is determined by the supply voltage needed by the microprocessor. Currently, the prevailing voltage is about 1.3 V. The input voltage of the converter is determined by the supply voltages that already exist in the system and which are used for powering other parts of the system. Today's PC employs a hybrid power system. Because the 5V output of the silver box must supply power to the memory chips and other peripherals, it cannot provide sufficient power for the high-power microprocessor. In the desktop, the DC-DC converter is powered up from a 12V voltage source, which is also shared by the disk drives. In the notebook, the DC-DC converter is powered up by the batteries or the output of the AC-DC adaptor. Because the voltage of the batteries varies with the utility time, the output of the batteries ranges from 9 V to 12 V. The output of the AC-DC adaptor is 20 V. Such high voltage levels are required to charge the battery.

In both desktops and notebooks, the input voltage of the DC-DC converter is higher than the output voltage. Therefore, the buck converter is widely used in the PC. The basic properties of the buck converter are reviewed in the next section.

2.2.2 Principle of the Buck Converter

Fig. 2.9 illustrates the topology of the buck converter. It consists of an input voltage source, a single-pole double-throw switch, a low-path LC filter and a load represented by a resistor R.

When the switch is in position a, the switch output voltage V_s is equal to the converter input voltage V_{in}; when the switch is in position b, V_s is equal to zero. The switch position is varied periodically, as illustrated in Fig. 2.10; therefore V_s is a rectangular waveform having frequency F_s and period $T_s=1/F_s$. The duty cycle D is defined as the fraction of time in which the switch occupies position a.

Because the DC component of a periodic waveform is equal to its average value, the DC component of V_s is

$$\overline{V_s} = D \times V_{in} . \tag{2.18}$$

In addition to the DC component, the voltage waveform of the switch output also contains harmonics of the switching frequency. In the applications for the DC-DC converter, these harmonics must be removed, such that the output voltage is essentially equal to the DC component. A low-pass LC filter can be employed for this purpose. The average voltage of V_{out} is equal to the average voltage of V_s. Otherwise, the current through inductor L will be infinite. This is called the principle of inductor volt-second balance: in steady state, the net volt-seconds applied on an inductor must be zero.

In practice, the switch is realized using a MOSFET and diodes, which are controlled by IC drivers, as shown in Fig. 2.11 and Fig. 2.12. Usually, the output stage of the driver is a CMOS buffer, which has two states (low and high). When the output of the buffer is low, the output is connected to the ground by an NMOSFET, which is fully on. Therefore, the output voltage level is zero, and the power MOSFETs driven by the buffer are off, because the threshold voltage of the power MOSFET is typically between 1 V and 3 V. When the output of the buffer is high, the output is connected to the supply of the IC driver by a PMOSFET, which is fully on. Hence, the output voltage level is equal to the supply voltage, the typical value of which is 5V in a notebook or 12V in a desktop, and the power MOSFETs driven by the buffer are on, because both 5 V and 12 V are higher than the threshold voltage of the power MOSFETs.

Although the circuit of the conventional buck converter is simpler than that of the synchronous one, the former is not used for the PC application. The reason is that the operation current at full load is about 10 A. Assuming the voltage drop on the low-side diode is 0.7 V, then the power loss on the diode will be 7 W. Such high temperature cannot be alleviated without an expensive cooling system.

In reality, in order to handle larger levels of output current, a multi-channel setup is usually employed, and each channel contains more than one device in parallel in order to share the current and the power loss in discrete applications.

As shown in Fig. 2.13 and Fig. 2.14, the steady state operation of the synchronous buck converter consists of the following stages.

1) From t_0 to t_1, the output of the low-side driver is high and the output of the high side driver is low. There is no current flowing through either the high-side MOSFET or the voltage source V_{in}, because the high-side MOSFET is off. Assuming the filter capacitor is large enough that the variation of the output voltage V_{out} can be ignored, then the output current of the buck converter, i.e. the current through the resistor R is

$$I_{out} = \frac{V_{out}}{R}. \tag{2.19}$$

With the assumption that output voltage V_{out} is much larger than the absolute voltage at node sw (V_{sw}), the voltage on inductor L can be considered to be equal to V_{out}. Therefore, the current variation with the time of the inductor L is

$$K_1 = \frac{di_L}{dt} = \frac{V_{out}}{L}. \tag{2.20}$$

Considering that the DC current through the capacitor C must be zero, the output current should be equal to the DC current of inductor L. So, the total current through the inductor L is a function of time t, such that

$$i_{L01}(t) = I_{out} + \frac{T_{01} - 2(t - t_0)}{2T_{01}} \Delta I_{01}, \tag{2.21}$$

where T_{01} is the during of this duration

$$T_{01} = T_1 - T_0, \tag{2.22}$$

and ΔI_{01} is the current ripple of inductor L during T_{01}, as follows:

$$\Delta I_{01} = K_1 T_{01} = \frac{V_{out}}{L} T_{01}. \tag{2.23}$$

Based on Equation (2.21), we know that the current through the inductor at the beginning ($t=t_0$) and the end ($t=t_1$) of this operating period are

$$i_{L01}(t_0) = I_{out} + \frac{\Delta I_{01}}{2}, \tag{2.24}$$

and

$$i_{L01}(t_1) = I_{out} - \frac{\Delta I_{01}}{2}, \tag{2.25}$$

respectively.

Since the high-side MOSFET is off, the current through the inductor is equal to the current though the low-side MOSFET. The current direction of the low-side MOSFET is from the source to the drain, and the voltage at node sw is

$$V_{sw}(t) = -i_L(t) \times R_{dslo}, \tag{2.26}$$

where R_{dslo} is the on-resistance of the low-side MOSFET.

In order to get some idea of the practical values of the variables addressed above, it is helpful do some simple calculations based on commercial MOSFETs and inductors. For an example using an operation frequency (F_s) of 500 KHz, an input voltage (V_{in}) of 12 V and an output voltage (V_{out}) of 1.3 V, using Equation (2.18), we know the duration of this period is about

$$T_{01} = (1-D)T_s = (1-\frac{V_{out}}{V_{in}})\frac{1}{F_s} = 1.78\mu s\,. \tag{2.27}$$

Assuming the value of the inductor is 0.8 μH, the current ripple can be found by Equation (2.23), such that

$$\Delta I_{01} = \frac{1.3}{0.8\times10^{-6}}\times1.78\times10^{-6} = 2.9A\,. \tag{2.28}$$

Using Equation (2.21), for I_{out}=10 A, the peak current through the low-side MOSFET occurs at $t=t_0$, and

$$I_{\max} = 10 + 2.9 = 12.9A\,. \tag{2.29}$$

The maximum voltage drop on the low-side MOSFET is

$$\left|V_{dslo\max}\right| = I_{\max}\times R_{dslo} = 0.0645V\,, \tag{2.30}$$

if R_{dslo}=5mΩ. This result verifies the assumption that the output voltage is much larger than the absolute voltage on the node sw.

Ignoring the voltage drop of the low-side MOSFET, the voltage stress of the high-side MOSFET is

$$V_{dshi12} = V_{in}\,. \tag{2.31}$$

After the first period, the output of the low-side driver becomes low, and the circuit comes into the second period.

2) From t_1 to t_2, the output of both the low-side and the high-side drivers are low. This duration is called the deadtime period, because the gate voltages of both MOSFETs are below the threshold voltage. The deadtime serves as a transition between the low-side MOSFET being on and the high-side MOSFET being on. Since it is dangerous to turn on

both MOSFETs, this period is indispensable as a timing margin. The typical value of this period is about 40 ns.

Since the output of the high-side driver is low, there is no current flowing through the high-side MOSFET. However, the current still can flow from the source to the drain through the body diode of the low-side MOSFET, which is formed between the P-body and the N drift region, as shown in Fig. 2.6. The di/dt of the current through the inductor in this period is larger than that of the first period, because there is more voltage drop on the inductor, so

$$K_2 = \frac{di}{dt} = \frac{V_{out} + V_{df}}{L}. \tag{2.32}$$

Assuming the forward voltage drop of the body diode is 0.8 V, for 1.3 V output voltage, the total current voltage variation is

$$\Delta I_{12} = \frac{1.3 + 0.7}{0.8 \times 10^{-6}} \times 40 \times 10^{-9} = 0.1A, \tag{2.33}$$

where the duration of this period

$$T_{12} = t_2 - t_1 \tag{2.34}$$

is assumed to be 40ns. Although K_2 is larger than K_1, the current variation during T_{12} is much smaller than that in the first period, because T_{12} is much shorter than T_{01}.

Considering the voltage drop of the body diode of the low-side MOSFET, the voltage stress of the high-side MOSFET is

$$V_{dshi12} = V_{in} + V_{df}. \tag{2.35}$$

In the next period, the high-side MOSFET is turned on.

3) From t_2 to t_3, the output of the low-side driver is low, and the output of the high-side driver is high. Ignoring the voltage drop across the drain and source of the high-side MOSFET, the voltage at node sw is equal to input voltage V_{in}. Therefore, the current through the inductor starts to rise with the following di/dt:

$$K_3 = \frac{V_{in} - V_{out}}{L}. \tag{2.36}$$

And the current can be expressed as

$$i_{L23}(t) = I_{out} + \frac{2(t-t_2)-T_{23}}{2T_{23}} \Delta I_{23}, \tag{2.37}$$

where ΔI_{23} is the total current variation

$$\Delta I_{23} = K_3 \times (t_3 - t_2) = \frac{V_{in}-V_{out}}{L}\frac{V_{out}}{V_{in}} \times T_s = \frac{V_{out}}{L} T_{01}. \tag{2.38}$$

The voltage across the drain and source of the low-side MOSFET is close to the level of voltage V_{in}.

4) From t_3 to t_4, similar to the second stage, the outputs of both low-side and high-side drivers are low, and the MOSFETs are in the off-state. This is another deadtime, and the inductor current variation is also small due to the short duration. Because both deadtimes are short, the current ripples in the first and third stage are equal, so as to maintain continuous current.

The main difference between stage two and stage four is that the current level of the low-side MOSFET is higher in stage four. If we ignore the current variation in these two stages, the current in the first deadtime (T_{12}) is equal to the minimum current through the inductor, and the current in the second deadtime (T_{34}) is equal to the maximum current through the inductor.

2.2.3 Power Loss of the Buck Converter

First, consider the power loss of the MOSFETs associated with the four steady states (Fig. 2.15) described in section 2.2.2.

1) From t_0 to t_1, the high-side MOSFET is off, and the low-side MOSFET is on. Because there is no current flowing through the high-side MOSFET, the power loss of the high-side MOSFET is zero. The power loss on the low-side MOSFET occurs due to the on-resistance R_{dslo}. Therefore, we have

$$W_{01} = \int_{t0}^{t1} I_{L01}^2(t) R_{dslo} dt \, . \tag{2.39}$$

Therefore,

$$P_{01} = (I_{out}^2 + \frac{\Delta I_{01}^2}{12}) R_{dslo} (1 - D) \, . \tag{2.40}$$

Using the numbers obtained in section 2.2.2, I_{out}=10A, ΔI_{01}=2.9A, R_{dslo}=5mΩ, and T_{01}=1.78μs, the total power loss is about 0.45 W and the contribution of the current ripple to the total power loss is less than 1%. However, at light load, for example, when I_{out} is half of the ripple current, the contribution can increase to 33%.

2) From t_1 to t_2, there is still no current through the high-side MOSFET. However, the current though the body diode of the low-side MOSFET can cause significant power loss. Assuming the forward voltage drop of the body diode is V_{df}=0.7V and T_{12}=40ns, the power loss will be

$$P_{12} = (I_{out} - \frac{\Delta I_{01}}{2}) V_{df} \frac{T_{12}}{T_s} = 0.12W \, . \tag{2.41}$$

3) From t_2 to t_3, there is no current flowing through the low-side MOSFET. The power loss on the high-side MOSFET occurs due to the on-resistance R_{dshi}. Hence, we have

$$W_{23} = \int_{t2}^{t3} I_{L23}^2(t) R_{dshi} dt \, . \tag{2.42}$$

Therefore,

$$P_{23} = (I_{out}^2 + \frac{\Delta I_{01}^2}{12}) R_{dshi} D \, . \tag{2.43}$$

Using the typical value of R_{dshi} as 10 mΩ, the conduction loss of the high-side MOSFET is 0.11 W.

4) From t_3 to t_4, the power loss occurs in the body diode of the low-side MOSFET. If T_{34}=T_{12}, the power loss in this deadtime is larger than that of the previous deadtime, because the current in this stage is larger. Still using the previous number, we have

$$P_{34} = (I_{out} + \frac{\Delta I_{01}}{2})V_{df} \frac{T_{34}}{T_s} = 0.16W \ . \tag{2.44}$$

Comparing the power loss in the four stages, the dominant one is the low-side conduction loss in the first stage. Although the duration of the two deadtimes are short, the power loss is not negligible. All the power loss of the P_{01}, P_{12} and P_{34} converts into heat in the low-side MOSFET. Only P_{23} is the power loss on the high-side MOSFET. However P_{23} is only a small part of the total loss of the high-side MOSFET, because there is other loss related to the switching of the high-side MOSFET, which includes the turn-on and turn-off losses.

When the high-side MOSFET is turning on, it takes time for the voltage to drop and current to rise. The general definition of power loss is

$$P = \int ivdt \ . \tag{2.45}$$

However, it is not practical to use Equation (2.45) to determine the power loss, because it is very difficult to monitor the instant current. Instead, the power loss is measured based on the average current and voltage.

Fig. 2.16 shows the circuit used in the efficiency test of the buck converter. M_{v1}, M_{v2}, M_{v3} and M_{v4} are high-precision voltage meters. R_1 and R_2 are high-precision resistors. The power consumed by the IC driver (usually, the driver and controller are monolithicly integrated in one package) is given by

$$P_{ic} = V_{inic} \times I_M \ , \tag{2.46}$$

where I_M is the reading of the current meter M_I. The average input current of the buck converter is given by

$$I_{in} = \frac{V_1}{R_1} \ . \tag{2.47}$$

Therefore, the input power from the voltage source V_{in} is

$$P_{in} = \frac{V_1 \times V_2}{R_1} \ . \tag{2.48}$$

The output current is

$$I_{out} = \frac{V_3}{R_2}. \tag{2.49}$$

Thus the output power is

$$P_{out} = \frac{V_3 \times V_4}{R_2}. \tag{2.50}$$

Then, the total power loss of the buck converter is

$$P_{ttloss} = P_{in} - P_{out} + P_{ic}. \tag{2.51}$$

Although the efficiency of the buck converter can be found by

$$\eta = \frac{P_{out}}{P_{in} + P_{ic}} \tag{2.52}$$

or

$$\eta = \frac{P_{out}}{P_{in}}, \tag{2.53}$$

if we ignore the power loss of the driver, the components of the power loss are still not known.

The major contributors of power loss in the buck converter are the inductor and MOSFETs. The inductor loss includes the magnetic loss and resistive loss due to the winding resistance. The MOSFETs' loss includes the gate loss and the conduction and switching losses. None of these loss components can be determined precisely by the experiment. This is another reason why an accurate model of the buck converter is needed.

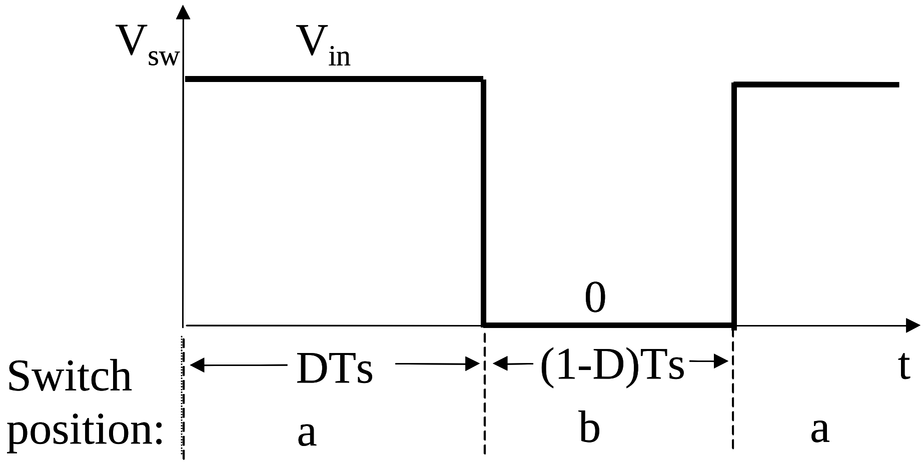


Fig. 2.10 Waveform of the output voltage (V_{sw}).

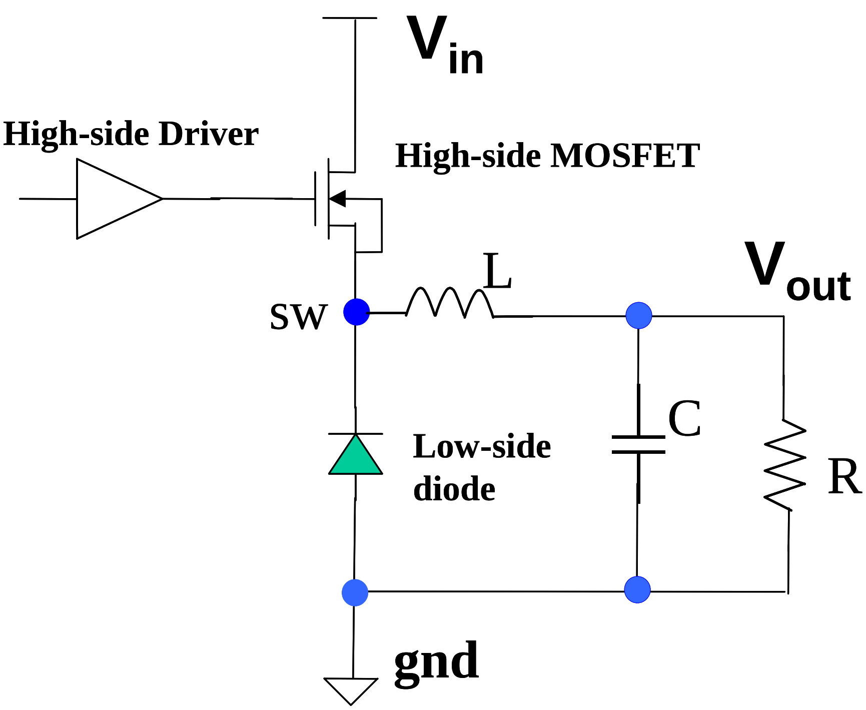


Fig. 2.11 Equivalent circuit of the conventional buck converter.

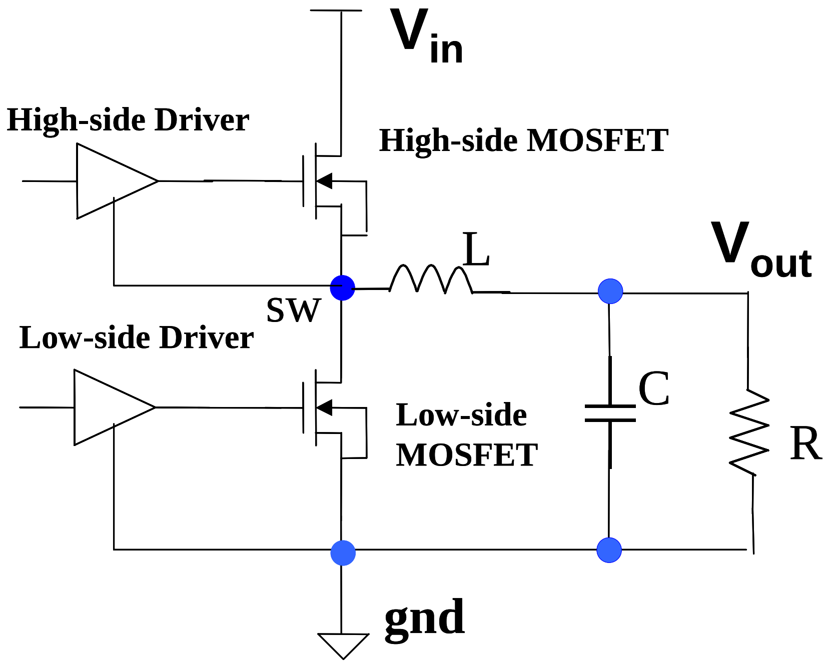


Fig. 2.12 Equivalent circuit of the synchronous buck converter.

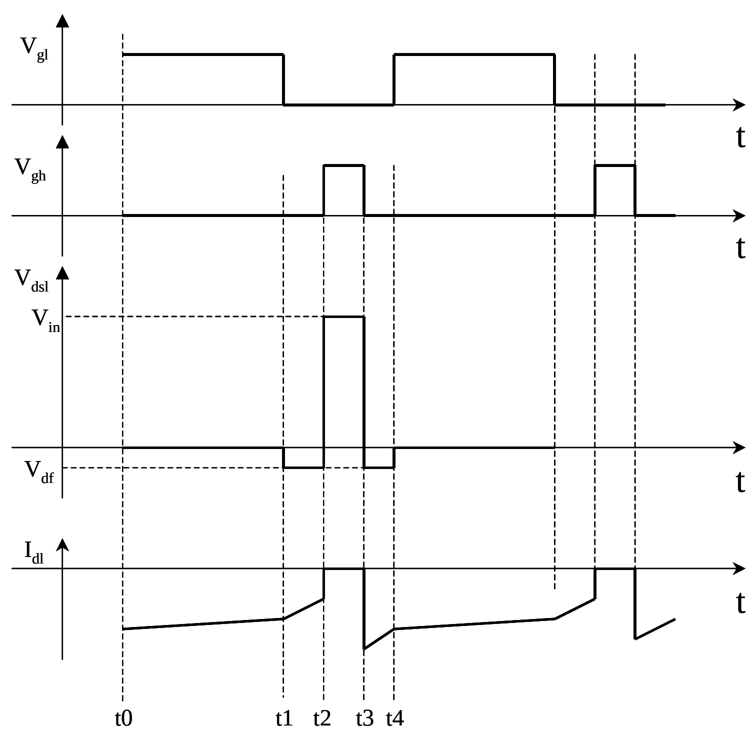


Fig. 2.13 Operating sequence of the synchronous buck converter (Part I).

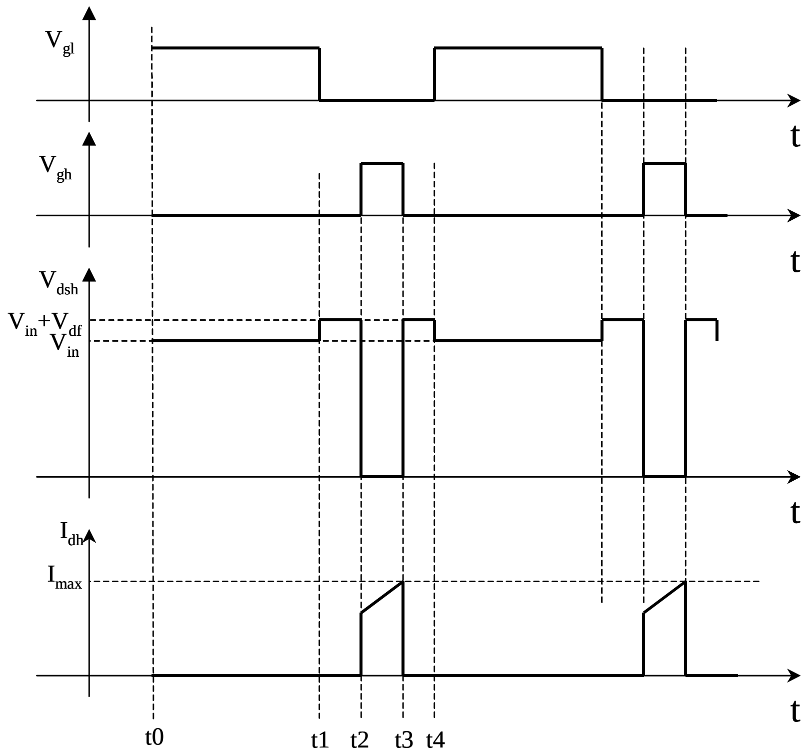


Fig. 2.14 Operating sequence of the synchronous buck converter (Part II).

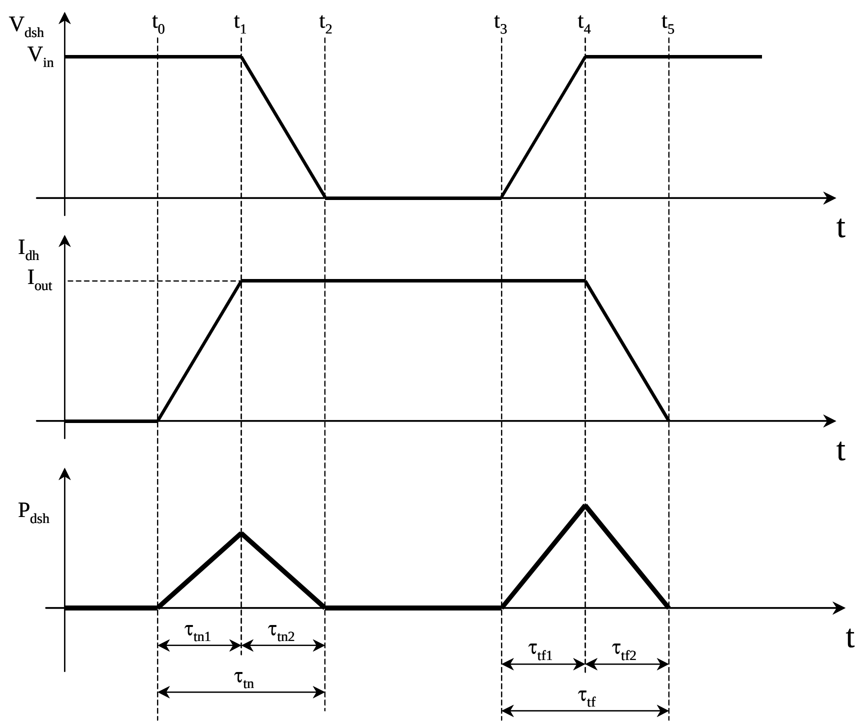


Fig. 2.15 Simplified switching waveforms of the high-side MOSFET.

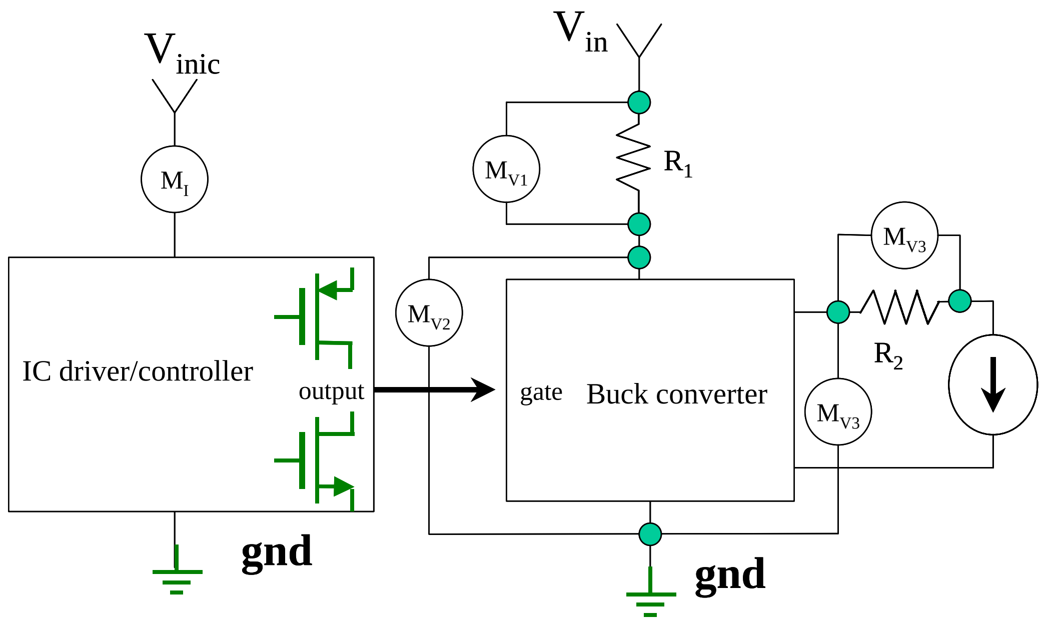


Fig. 2.16 Circuit used in the efficiency measurement.

Chapter 3 Analytical Modeling of the Buck Converter

Although the FEA-based mixed-mode simulation [B17] can provide more accurate results than an analytical model [B11]-[B16], the latter is still indispensable, because the FEA model looks like a black box, which contains many parameters. Without good understanding of the effects of these parameters, the user may get lost in the simulation. In order to efficiently use the FEA models, in this chapter, three analytical models related to the loss of the buck converter are presented after the introduction of the basic model of the power MOSFET. The first model links the switching loss of the high-side MOSFET to the design parameters of the power MOSFET. The second is a novel circuit model used to calculate the turn-on and turn-off loss of the high-side MOSFET of the buck converter with parasitic inductance. The last models the dv/dt-induced spurious turn-on of the low-side MOSFET.

3.1 Modeling of the Power MOSFET in the Steady State

Modeling the power MOSFET [B1]-[B4] is not a trivial task. However, as a switch, the power MOSFET has two states: off and on. When the gate-to-source voltage (V_{gs}) is less than the threshold voltage (V_{th}), the current cannot flow from the drain to the source. However, the current can travel from the source to the drain through the inherent body diode of the MOSFET. Therefore, when the power MOSFET is off, it should be modeled as a diode. The anode of the diode is the source of the MOSFET, and the cathode of the diode is the drain of the MOSFET. There are two operation modes when the power MOSFET is on.

1) When $V_{gs} > V_t$ and $V_{ds} < V_{gs}-V_t$, the MOSFET operates in the linear region. It can be modeled as a voltage controlled resistor, the value of which is

$$R_{ds} = \frac{L_g T_{ox}}{W_g \mu_{nch} \varepsilon_{ox} (V_{gs} - V_{th})} + \frac{R_{dft}}{A} + \frac{R_{sub}}{A} + R_{pk} , \qquad (3.1)$$

where

- $\frac{L_g T_{ox}}{W_g \mu_{nch} \varepsilon_{ox} (V_{gs} - V_{th})}$ is the channel resistance as expressed by Equation (2.5).
- R_{dft} is due to the current spreading from the channel into the drift region as expressed by the Equation (2.16).
- A is the device area.
- R_{sub} is the contribution of the substrate.
- R_{pk} is the package resistance, which is usually below 1 mΩ for the stat-of-the-art package.
-

2) When $V_{gs} > V_t$ and $V_{ds} > V_{gs} - V_t$, the MOSFET operates in the saturation region. It behaves like a voltage-controlled current source, the value of which is

$$I_d = \frac{1}{2} \mu_{nch} C_{ox} \frac{W_g}{L_g} (V_{gs} - V_{th})^2 . \qquad (3.2)$$

Due to the oxide gate and the depletion region of the silicon, the power MOSFET has capacitances associated with the terminal. Usually, they are defined as follows.

- C_{gs} is the capacitance between the gate and the source.
- C_{gd} is the capacitance between the gate and the drain. C_{gd} is also expressed as C_{rss}.
- C_{ds} is the capacitance between the drain and the source.
- $C_{iss} = C_{gs} + C_{gd}$ is called input capacitance.
- $C_{oss} = C_{ds} + C_{gd}$ is called output capacitance.

Fig. 3.1 shows the equivalent circuit of a power MOSFET, where the following definitions apply,

- L_g, L_d and L_s are the parasitic inductance associated with the package [C17]-[C21].
- R_g includes the resistance of the gate bus inside the MOSFET and the package resistance. The typical value of the gate bus is about 1 Ω, which is much larger than the package resistance.
- R_d is the sum of R_{spd}, R_{sub} and R_{pk}.

3.2 Basic Switching Model of the High-side MOSFET in the Buck Converter

The switching loss of the high-side MOSFET in the buck converter is a major part of the total loss. In this section, the effect of the device characteristics on the switching performance of the high-side MOSFET is addressed, based on the switching circuit with a clamped inductive load.

3.2.1 Equivalent Circuit of the High-side MOSFET in the Buck Converter

The equivalent switching circuit of the high-side MOSFET in the buck converter is basically a MOSFET with a clamped inductive load. However, this is not a straightforward conclusion, and many people have requested further explanation of this point. Therefore, it is worthwhile to dedicate several pages to explaining the derivation of the MOSFET with a clamped inductive load from the buck converter.

The turn-on and turn-off of the high-side MOSFET occur when the low-side MOSFET is off. Therefore, the low-side MOSFET can be simplified as a diode during the switching of the high-side MOSFET. The driver of the high-side MOSFET is basically a CMOS buffer. If we assume the following: that the NMOS and PMOS of the last stage of the buffer have the same on resistance (R_{dr}); that the voltage source of the CMOS buffer is V_{dr}; and that the switching time of the CMOS buffer is much shorter than that of the high-side MOSFET, then the driver of the high-side MOSFET can be represented by resistor (R_{dr}) in series with a pulse voltage source, the amplitude of which is V_{dr}. Therefore, the buck circuit shown in Fig. 2.12 can be reduced to the circuit shown in Fig. 3.2, where the current ripple through the inductor L is ignored, and the LCR network is simplified as a constant current source (I_o). Since the selection of the ground is arbitrary in the electrical circuit, we can define the switching node (sw) as the ground as shown in Fig. 3.3. After swapping the positions of the input voltage (V_{in}) and the parallels of the current source (I_o) and diode, the switching circuit is rearranged as shown in Fig. 3.4. If we use the power MOSFET model presented in section 3.1 to substitute for the MOSFET symbol given in Fig. 3.4, we obtain a more complex circuit, as shown in Fig. 3.5, where R_{drtt} is the sum of R_{dr} and $R_{g,}$ and L_g, C_{ds}, R_d and R_s are ignored.

Therefore, the equivalent circuit of the high-side MOSFET is essentially a MOSFET with a clamped inductive load, which is represented by a constant current, as shown in Fig. 3.5.

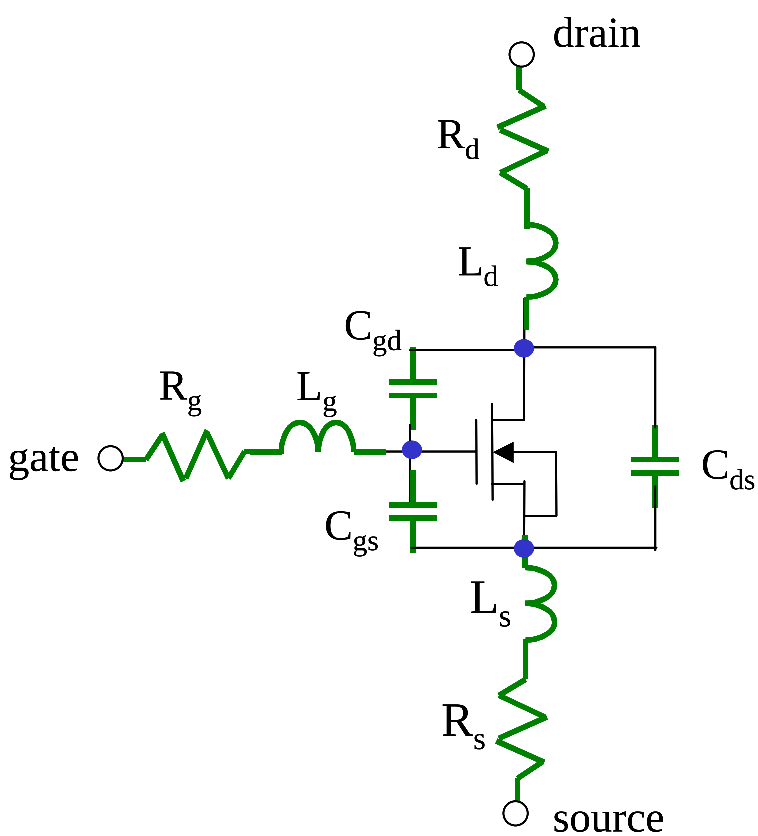
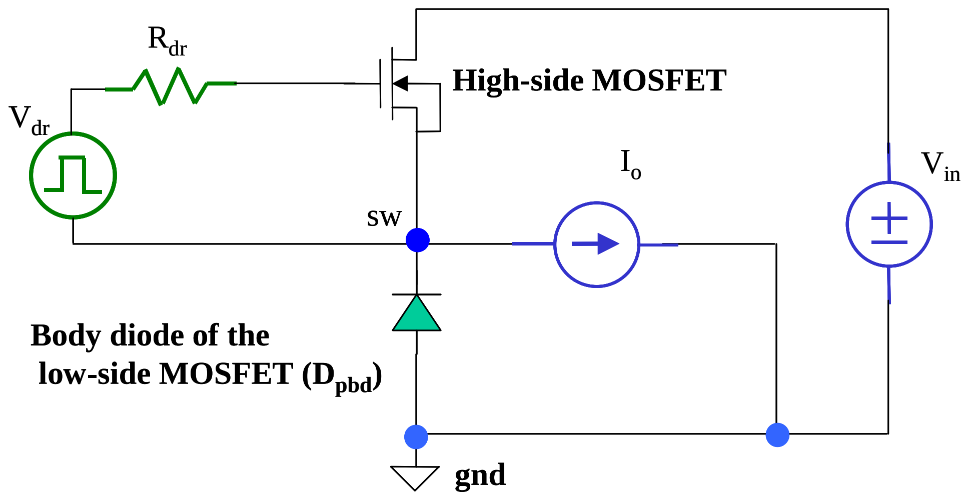
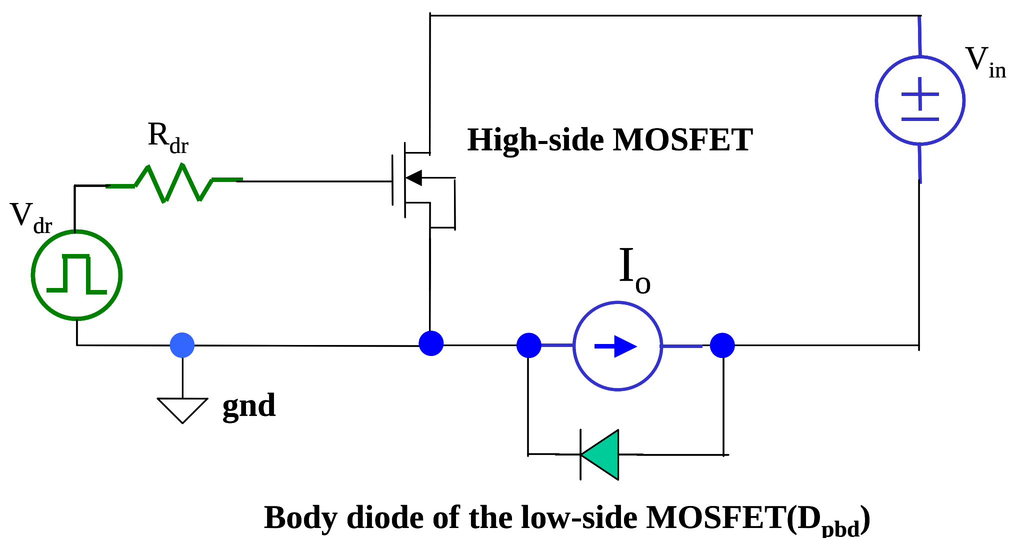


Fig. 3.1 The equivalent circuit of the power MOSFET.



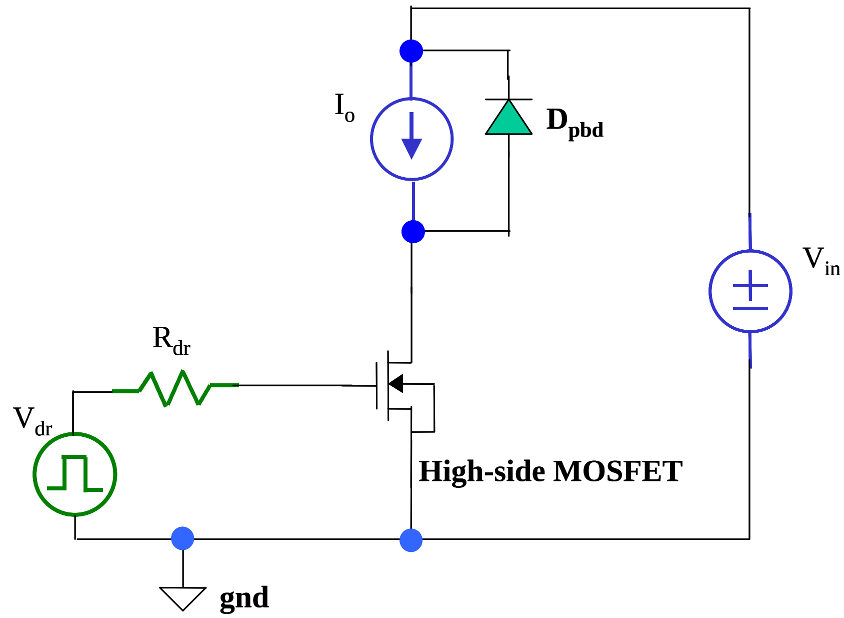
(Low side MOSFET is simplified as a diode.)

Fig. 3.2 Equivalent circuit of the high-side MOSFET.



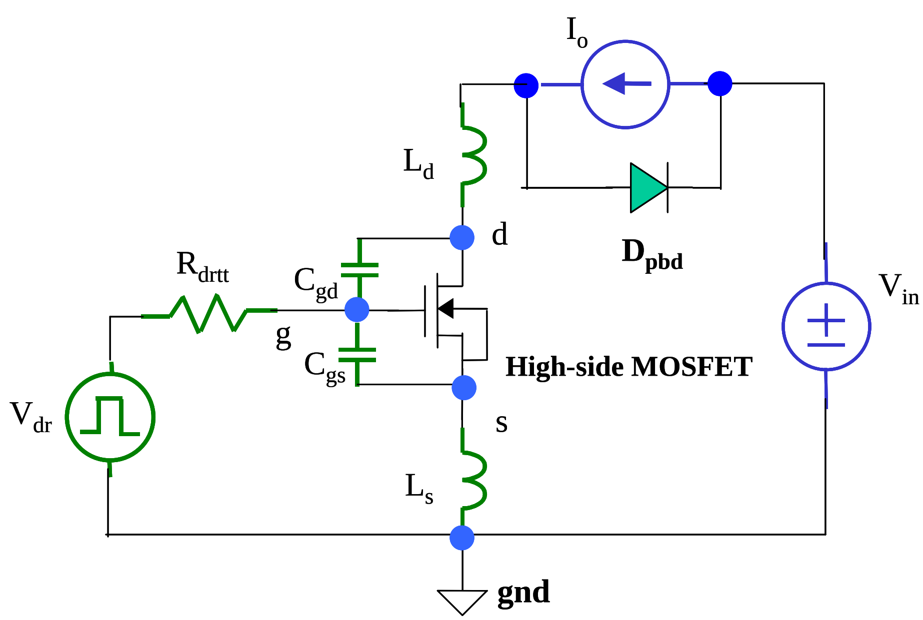
(The ground is moved from the anode of the diode to the cathode of the diode.)

Fig. 3.3 Equivalent circuit of the high-side MOSFET.



(The position of the input voltage V_{in} is swamped with the load I_o.)

Fig. 3.4 Equivalent circuit of the high-side MOSFET.



(Major parasitic elements are included in the circuit.)

Fig. 3.5 Equivalent circuit of the high-side MOSFET.

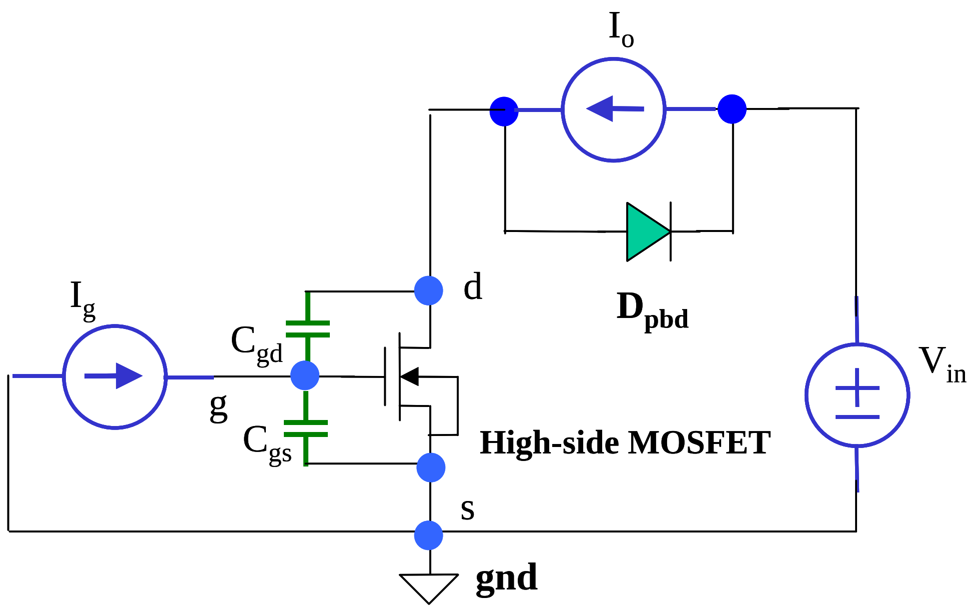


Fig. 3.6 Equivalent circuit of the high-side MOSFET with constant current source as gate driver.

3.2.2 Switching Process of MOSFET with Inductive Load

Although the equivalent circuit of the high-side MOSFET is much simpler to understand than that of the original buck converter, it is still a high-order, nonlinear system. It is unlikely that an analytical solution of the circuit illustrated in Fig. 3.5 can be found without any assumptions or simplifications. In this section, the simplest analysis is presented in order to achieve a basic concept of the switching process. More complex models are developed in section 3.3 and section 3.4.

Fig. 3.6 ignores the parasitic inductance, and uses a current source as the gate driver to further simplify the circuit. Three assumptions are made for the following discussion.

- The forward voltage drop of the freewheeling diode (D_{pbd}) is zero
- C_{gd} and C_{gs} are constant
- The gate current (I_g) is much smaller than the load current (I_o)

3.2.2.1 Turn-on process

Fig. 3.7, Fig. 3.8 and Fig. 3.9 show the waveforms associated with the turn-on process.

1) Turn-on delay. From T_0 to T_1, the MOSFET is off. Load current I_o flows through the diode (D_{pbd}), and the drain voltage of the MOSFET equals the level of V_{in}. Since a constant current is applied on the gate, the gate-to-source voltage rises linearly as

$$V_{gs} = \frac{I_g}{C_{iss}} t \,. \tag{3.3}$$

The total gate charge in this stage is

$$Q_{gs1} = V_{th} \times C_{iss} \,. \tag{3.4}$$

After V_{gs} reaches the threshold voltage (V_{th}), MOSFET starts to conduct, and the turn-on process enters the second stage.

2) Current rising. In this period, the drain current starts to increase and finally reaches the level of the total load current (I_o). Since the free-wheeling diode (D_{pbd}) is still on, the drain voltage of the MOSFET is clamped at V_{in}, and the MOSFET operates in the saturation state. Referring to Equation (3.2), its drain current can be expressed as

$$I_d = \frac{1}{2} \mu_{nch} C_{ox} \frac{W_g}{L_g} \frac{I_g^2}{C_{iss}{}^2} t^2 \,. \tag{3.5}$$

This period comes to the end when I_d is equal to load current (I_o). The gate-to-source voltage V_{gs} is determined by

$$V_{gson} = V_{th} + V_{eff} \,, \tag{3.6}$$

where the effective gate voltage V_{eff} is defined as

$$V_{eff} = \sqrt{\frac{2 I_o L_g}{\mu_{nch} C_{ox} W_g}} \,. \tag{3.7}$$

The power loss on the MOSFET in this period is

$$E_2 = \int_{t1}^{t2} I_d V_d \cdot dt = \frac{V_{in} I_o I_g^2}{V_{eff}^2 C_{iss}^2} \int_{t1}^{t2} t^2 dt = \frac{1}{3} \frac{V_{in} I_o Q_{gs2}}{I_g} \,, \tag{3.8}$$

where

$$Q_{gs2} = V_{eff} C_{iss} \tag{3.9}$$

is the variation of the gate charge in this period.

After the MOSFET takes over all of the load current, the drain voltage starts to drop, and the circuit enters the third stage.

3) Voltage falling. In this period, the drain current is equal to the load current (I_o), and the gate-to-source voltage remains at V_{gson}, as expressed in Equation (3.6), since the MOSFET still operates in the saturation region. Because V_{gs} is fixed at V_{gson}, the gate current only flows through the gate-to-drain capacitance (C_{gd}), and the voltage variation on C_{gd} is

$$\Delta V_{gd} = \frac{I_g}{C_{gd}} t \,. \tag{3.10}$$

Therefore, the drain voltage is

$$V_d = V_{in} - \Delta V_{gd} = V_{in} - \frac{I_g}{C_{gd}} t \,. \tag{3.11}$$

Assuming that V_{eff} is very small, the MOSFET remains in the saturation state until V_d reaches zero. Then, the duration of this period is

$$\Delta t_{23} = t_3 - t_2 = \frac{Q_{gd0}}{I_g} \,, \tag{3.12}$$

where
$$Q_{gd0} = V_{in} \times C_{gd} \tag{3.13}$$

is the variation of the gate charge in this stage. Therefore, the power loss in this period is

$$E_3 = \int_{t2}^{t3} V_d I_d \, dt = \int_{t2}^{t3} I_o (V_{in} - \frac{I_g}{C_{gd}} t) dt = \frac{I_o V_{in} Q_{gd0}}{2 I_g} \,. \tag{3.14}$$

The MOSFET enters the linear region when V_{ds} is less than V_{eff} and the MOSFET is in the on state.

3.2.2.2 Turn-off process

The turn-off process starts when I_g flows from the gate to the ground and the MOSFET enters the saturation region. The turn-off process is basically the reverse order of the turn-on process. Fig. 3.10, Fig. 3.11 and Fig. 3.12 show the waveforms associated with the turn-off process.

(4) Voltage rising. This period is the reverse process of the third stage.

(5) Current dropping. This period is the reverse process of the second stage.

Two Equations, (3.8) and (3.14), describe the power loss in the switching process. E_2 divided by E_3 yields the ratio of the power loss in the second and the third stage, so

$$K_{23} = \frac{E_2}{E_3} = \frac{2}{3}\frac{Q_{eff}}{Q_{gd}0}. \qquad (3.15)$$

Because usually $Q_{eff} << Q_{gd0}$, we have $E_2 << E_3$. Therefore, Q_{gd0} plays a very important role in the total switching loss. In the next section, the origin of C_{gd} and Q_{gd0} is related to the design parameters of the UMOSFET.

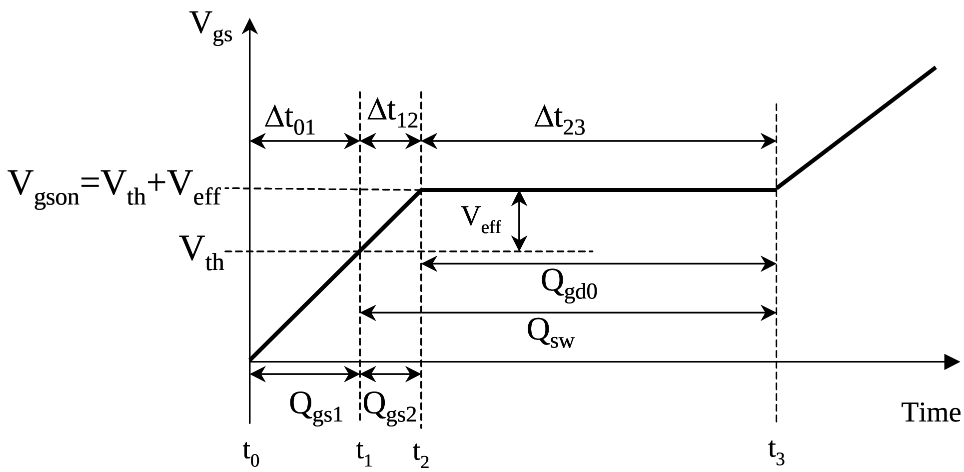


Fig. 3.7 Waveform of V_{gs} in the turn-on process of the MOSFET.

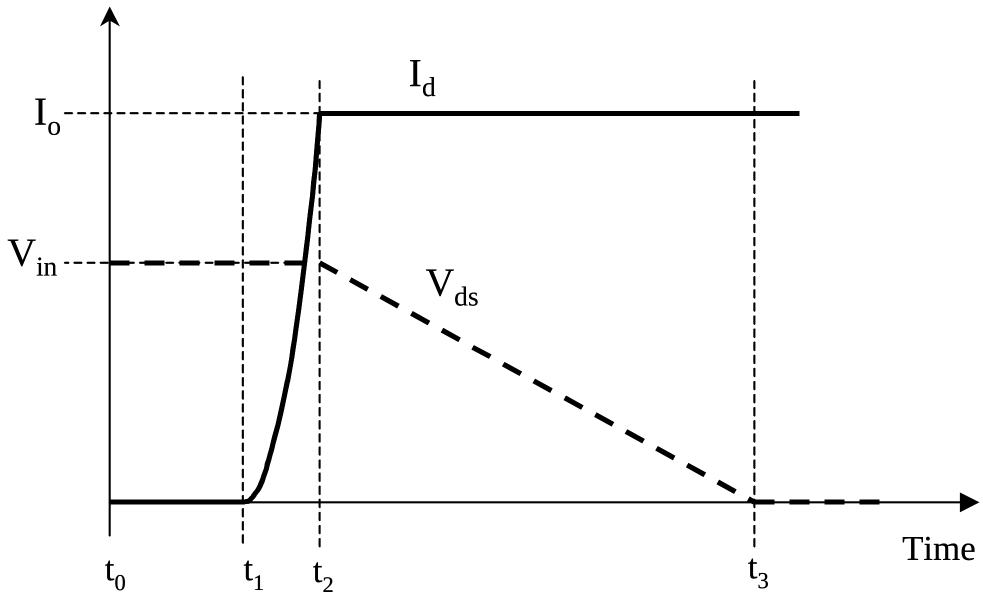


Fig. 3.8 Waveform of I_d and V_{ds} in the turn-on process of the MOSFET.

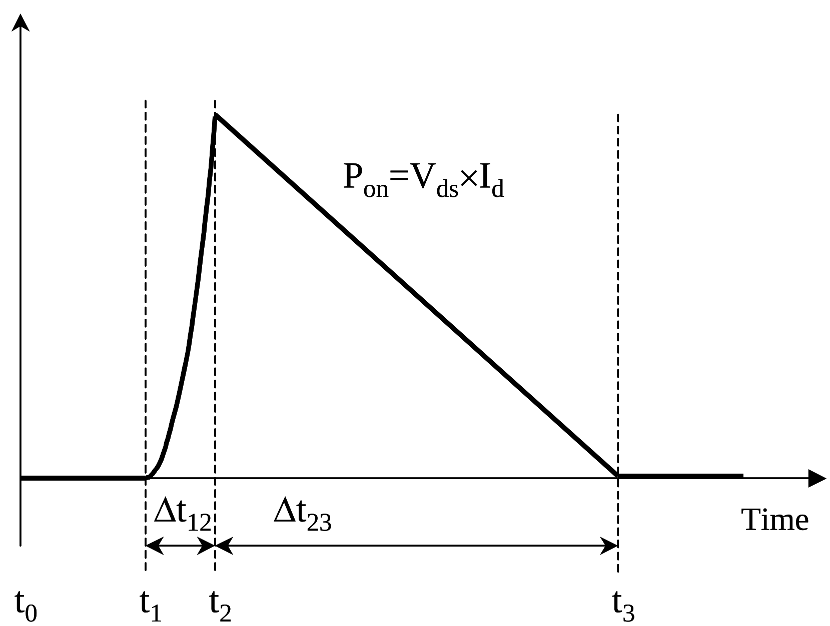


Fig. 3.9 Waveform of the power loss in the turn-on process of the MOSFET.

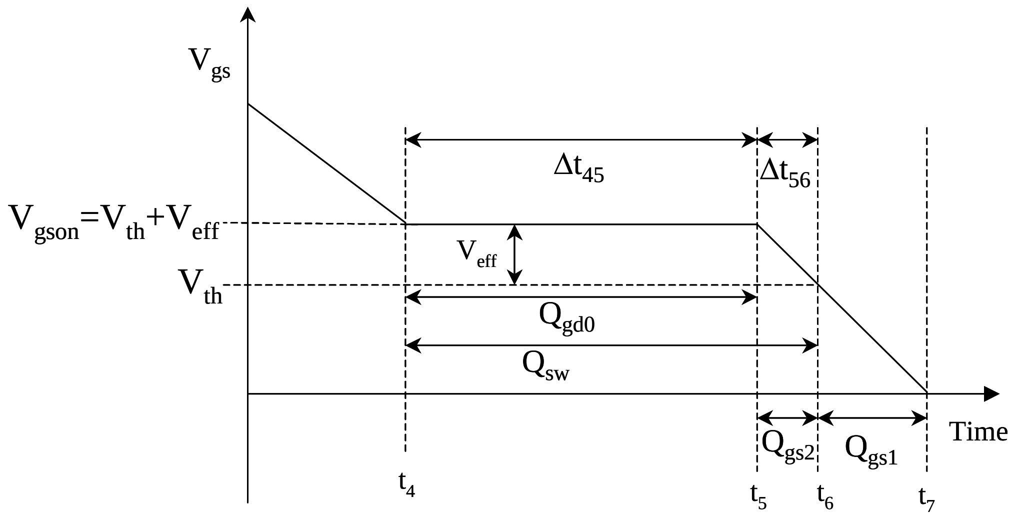


Fig. 3.10 Waveform of V_{gs} in the turn-off process of the MOSFET

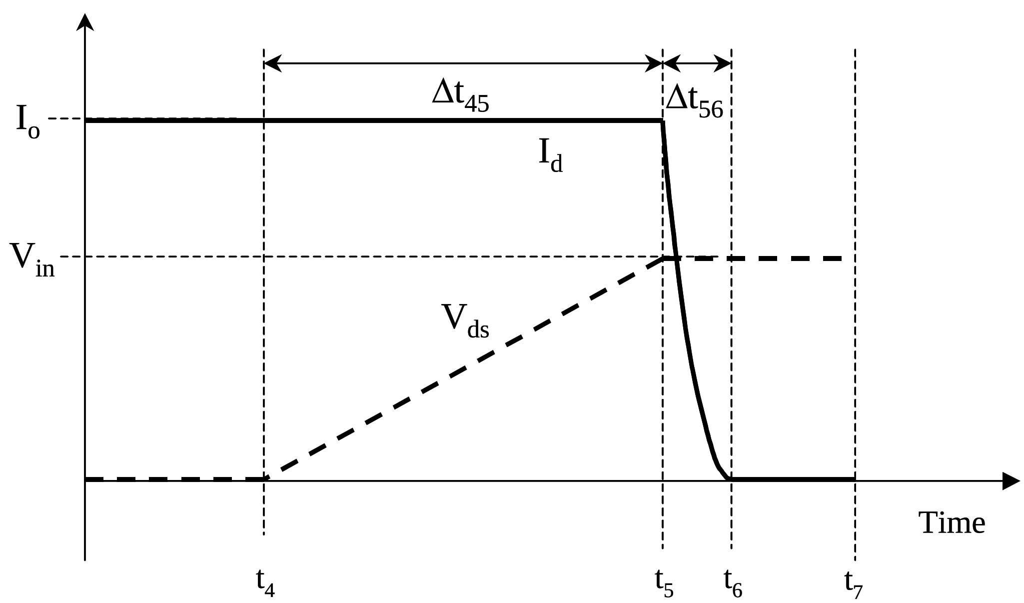


Fig. 3.11 Waveform of I_d and V_{ds} in the turn-off process of the MOSFET.

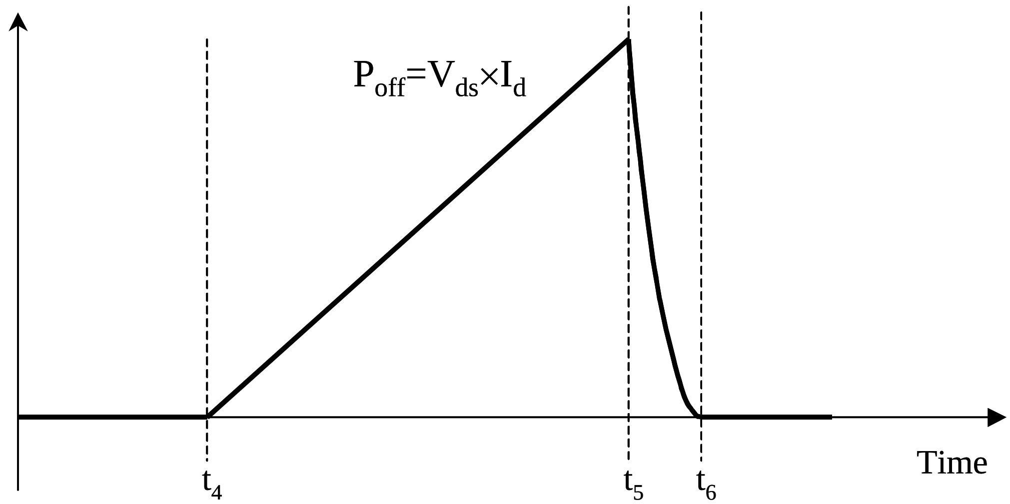


Fig. 3.12 Waveform of the power loss in the turn-off process of the MOSFET.

3.3 Modeling Gate-to-Drain Capacitance (C_{gd}) and Charge (Q_{gd})

As addressed in the preceding sections, for the high-side MOSFET, most of the switching loss of the high-side MOSFET occurs during the charging and discharging of the gate-to-drain capacitance C_{gd}. Therefore, C_{gd} plays an important role in the loss of the MOSFETs in the buck converter, and it is important to understand the characteristics of C_{gd} in the power MOSFET.

The geometry of the gate to drain capacitance in the trench MOSFET is shown in Fig. 3.13, where C_{gd} arises from the bottom of the trench and the part of the side wall of the trench, that is not covered by the P-body area.

Because the minimum trench width W_{ch} is limited by silicon technology, W_{ch} is usually much longer than Ovp, and the contribution of the side wall of the trench to the C_{gd} is less than that of the bottom of the trench. If we ignore Ovp and consider only the drain part directly opposite to the bottom of the drain, C_{gd} can be simplified as a one-dimensional capacitor.

When the drain voltage is less than the gate voltage, $V_{dg} < 0$, an accumulation layer is formed under the oxide. Because the accumulation layer is very thin and highly conductive, C_{gd} equals to the oxide capacitance C_{gdox}, so

$$C_{gd} = C_{gdox} = \frac{\varepsilon_{ox}}{T_{ox}}. \tag{3.16}$$

In switching stage 3 and 4 as addressed in the preceding section, the gate voltage is V_{gson}; when the drain voltage is less than V_{gson}, C_{gd} can be treated as a constant value. However, when the drain voltage is higher than the gate voltage, the depletion layer forms under the gate oxide, which shares part of V_{dg}. There are two cases for consideration.

- When the width of the depletion region is no more than the length of the drift region, the electric field does not reach the highly doping substrate. It is called a non-punch-through type of depletion.
- When the width of the depletion region is more than the length of the drift region, the electric field reaches the highly doping substrate. It is called a punch-through type of depletion.

Although, as demonstrated in the Appendix A, for both cases, the capacitance of the depletion region is

$$C_{dpl} = \frac{\varepsilon_{si}}{W_{dep}}, \tag{3.17}$$

the expressions of W_{dep} are different. Therefore, the derivations of C_{gd} and Q_{gs} for non-punch-through and punch-through types of depletion regions are discussed separately, as follows.

3.3.1 C_{gd} and Q_{gd} for the Non-Punch-Through Type of Depletion Region

The distributions of the electric field in the oxide and the non-punch-through type of depletion region are shown in Fig. 3.14. The electric field in the oxide is a constant (E_{ox}). So, voltage on the gate oxide is

$$V_{ox} = E_{ox} T_{ox}. \tag{3.18}$$

In the depletion region, the electric field drops linearly to zero, and its slope is

$$\beta = \frac{qN}{\varepsilon_{si}}, \tag{3.19}$$

where N is the doping concentration of the drift region. Then, the voltage on the depletion region is

$$V_{si} = \frac{E_{si}^2}{2\beta}. \tag{3.20}$$

According to Gauss's law, the ratio between the electric field on the oxide and the silicon boundary is

$$\alpha = \frac{E_{ox}}{E_{si}} = \frac{\varepsilon_{si}}{\varepsilon_{ox}}. \tag{3.21}$$

Therefore, the drain-to-gate voltage can be written as

$$V_{dg} = V_{ox} + V_{si} = \alpha E_{si} T_{ox} + \frac{E_{si}^2}{2\beta}. \tag{3.22}$$

The root of E_{si} in the above Equation is

$$E_{si} = \sqrt{\alpha^2 \beta^2 T_{ox}^2 + 2\beta V_{dg}} - \alpha\beta T_{ox}. \tag{3.23}$$

Again, using Gauss's law yields

$$Q_{gd0} = \varepsilon_{si} E_{si} = \varepsilon_{si} (\sqrt{\alpha^2 \beta^2 T_{ox}^2 + 2\beta V_{dg}} - \alpha\beta T_{ox}). \tag{3.24}$$

Then, the width of the depletion region is

$$W_{dpl} = \frac{Q_{gd}}{qN} = \frac{\varepsilon_{si} (\sqrt{\alpha^2 \beta^2 T_{ox}^2 + 2\beta V_{dg}} - \alpha\beta T_{ox})}{qN}. \tag{3.25}$$

Finally, for the non-punch-through type depletion region, the gate to drain capacitance can be expressed as

$$C_{gd} = \frac{\alpha \varepsilon_{ox}}{W_{dpl} + \alpha T_{ox}}. \tag{3.26}$$

3.3.2 C_{gd} and Q_{gd} for the Punch-Through Type of Depletion Region

The distribution of the electric field in the oxide and the non-punch-through type of depletion region is shown in Fig. 3.15. The voltage on the gate oxide still can be expressed by Equation (3.18). In the depletion region, the electric field still varies linearly, but it does not drop to zero as is the case for the non-punch-through type. The voltage on the depletion region is

$$V_{si} = E_{si} L_n - \frac{\beta L_n^2}{2}, \qquad (3.27)$$

where L_n is the length of the depletion region. Then, the drain-to-gate voltage can be written as

$$V_{dg} = V_{ox} + V_{si} = \alpha E_{si} T_{ox} + E_{si} L_n - \frac{\beta L_n^2}{2}. \qquad (3.28)$$

The solution of E_{si} in the above Equation is

$$E_{si} = \frac{V_{dg} + 0.5\beta L_n^2}{L_n + \alpha T_{ox}}. \qquad (3.29)$$

Again, using Gauss's law yields

$$Q_{gd0} = \varepsilon_{si} E_{si} = \varepsilon_{si} \frac{V_{dg} + 0.5\beta L_n^2}{L_n + \alpha T_{ox}}. \qquad (3.30)$$

As demonstrated in Appendix A, the capacitance of the punch-through type of depletion region is constant. Therefore, the total gate-to-drain capacitance is

$$C_{gd} = \frac{\alpha \varepsilon_{ox}}{L_n + \alpha T_{ox}}. \qquad (3.31)$$

Because when punch-through occurs, the width of the depletion region (W_{dpl}) is equal to the length of the drift region (L_n), Equation (3.26) is a unified expression for both punch-through and non-punch-through types of the depletion region.

An interesting result is that, although for the punch-through type of depletion region C_{gd} is constant,

$$Q_{gd} \neq V_{dg} C_{gd}. \qquad (3.32)$$

This is because the C_{gd} is defined as

$$C_{gd} = \frac{dQ_{gd}}{dV_{dg}} \qquad (3.33)$$

instead of

$$C_{gd} = \frac{Q_{gd}}{V_{dg}}. \tag{3.34}$$

If the C_{gd} is defined by Equation (3.34), for the punch-through type of depletion region, C_{gd} depends on V_{dg}. We can find the expression using Equation (3.30), such that

$$C_{gd} = \frac{Q_{gd}}{V_{dg}} = \frac{\varepsilon_{si}}{V_{dg}} \frac{V_{dg} + 0.5\beta L_n^2}{L_n + \alpha T_{ox}}. \tag{3.35}$$

In this dissertation, the capacitance is always defined by (3.34).

The one-dimensional modeling and the two-dimensional simulation results of C_{gd} are compared in Fig. 3.16. When V_{dg} is high, the simulation result is larger than that of the calculation. This is due to the two-dimensional fringing effect. However, there is not much overall difference between the calculation and simulation .

Fig. 3.17 shows the effects of the doping concentration (N) and the drift region length (L_n) on C_{gd}. When L_n is long, C_{gd} is independent of L_n, because, for the non-punch-through type of depletion region, the depletion width is determined by voltage (V_{dg}) and the doping concentration of the depletion region. Since the width of the depletion region increases as the doping concentration decreases (Equation 3.25), the lightly doped drift region has less C_{gd}. When L_n is short, the width of the depletion region is L_n. Therefore, shorter L_n leads to more C_{gd}, and the doping concentration has no effect on C_{gd}.

As shown in Fig. 3.18, L_n and N have similar effects on Q_{gd0}. Two important conclusions are that the punch-through type of the drift region is not good in terms of C_{gd} and Q_{gd0}, and the lightly doped drift region leads to less C_{gd} and Q_{gd0}.

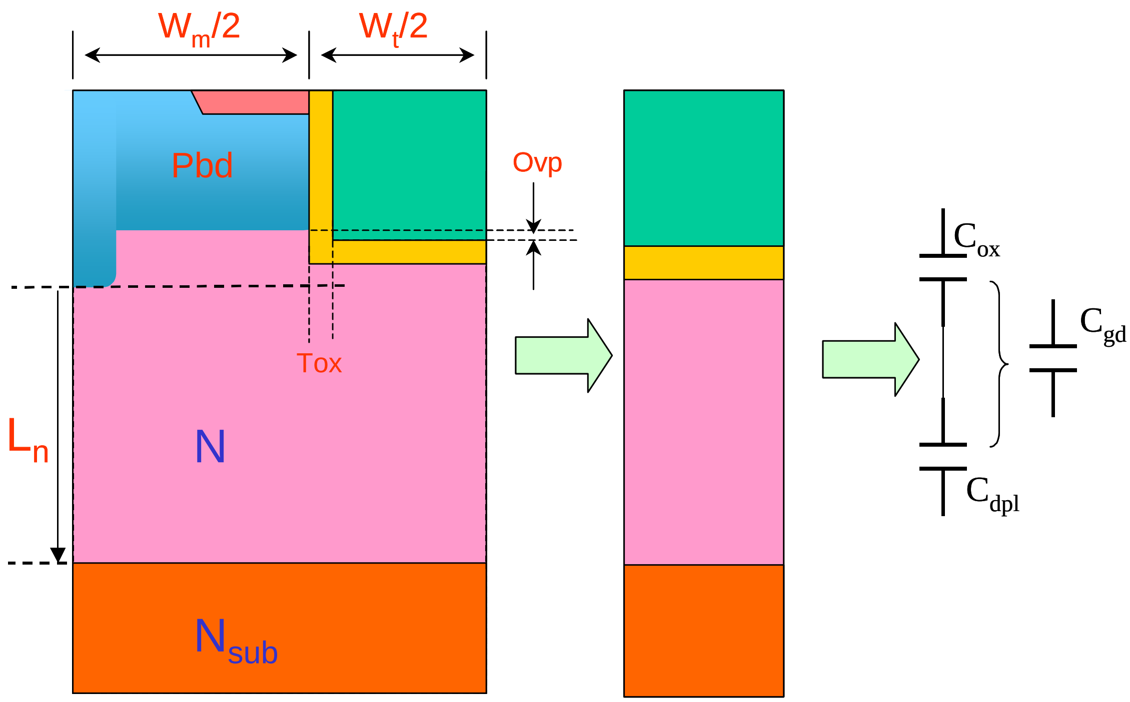


Fig. 3.13 One dimensional model of C_{gd} in the UMOSFET.

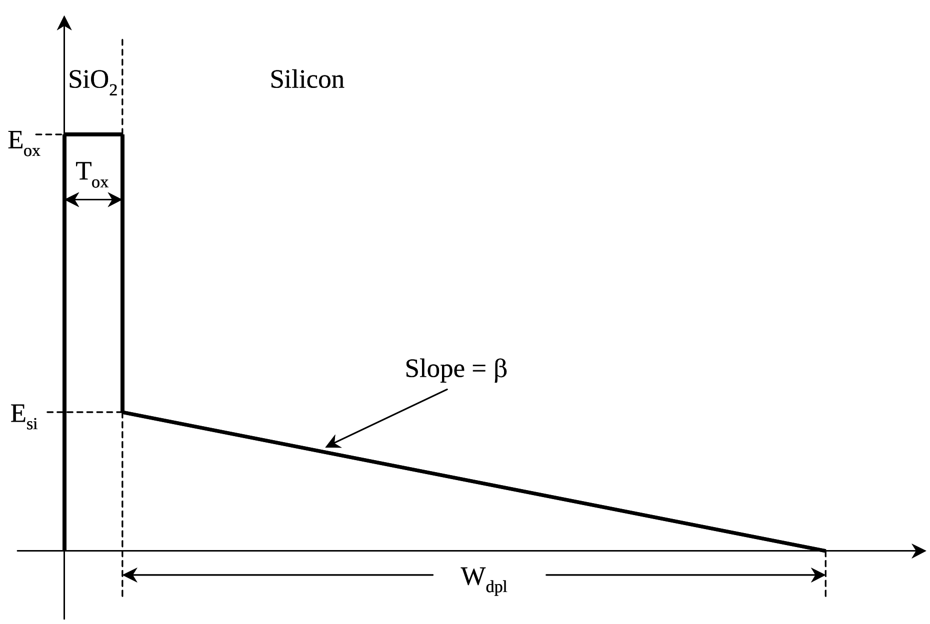


Fig. 3.14 Distribution of the electric field in the non-punch-through type of depletion region.

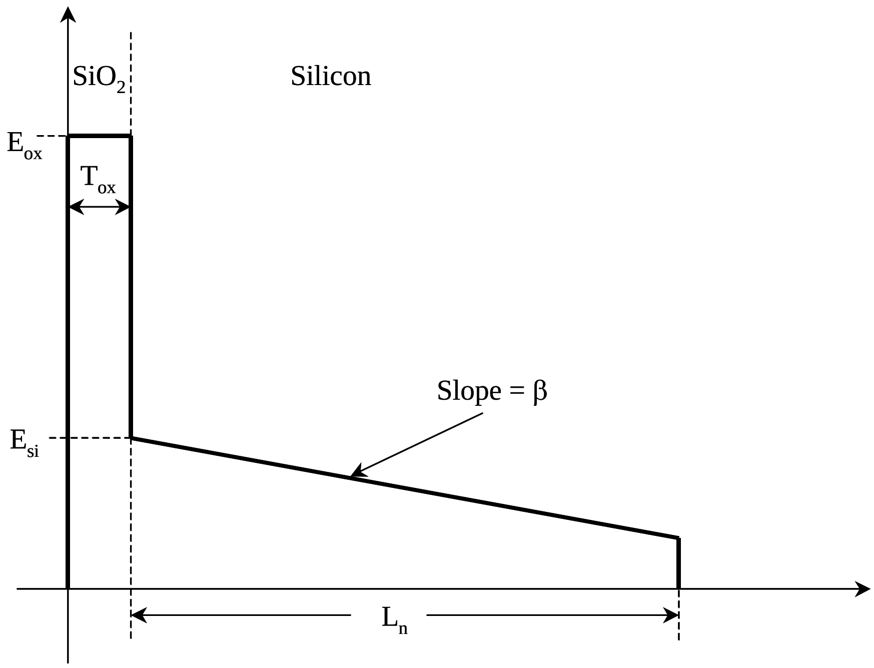


Fig. 3.15 Distribution of the electric field in the punch-through type of depletion region.

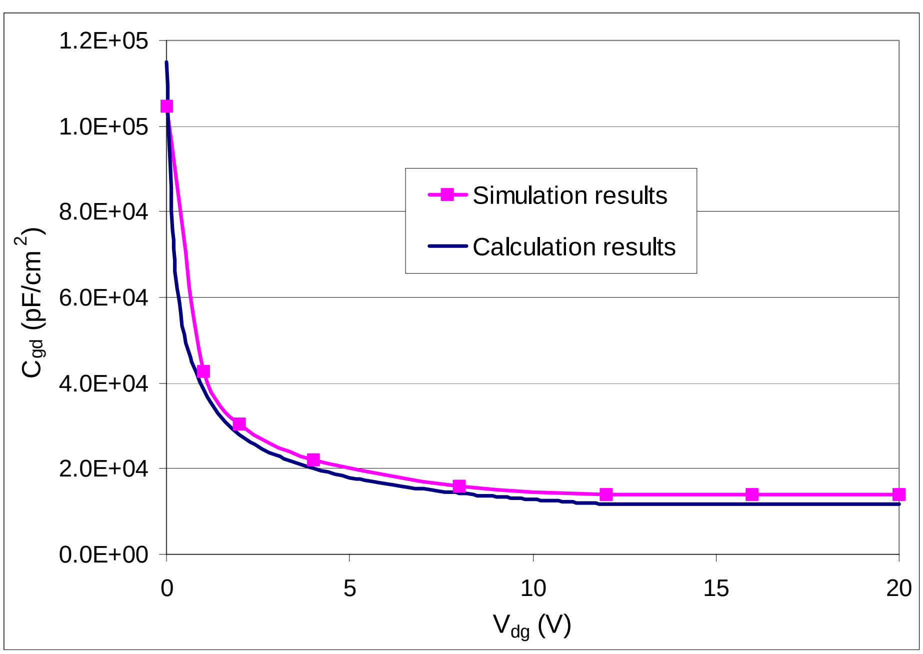


Fig. 3.16 Comparison of calculated and simulated C_{gd}.

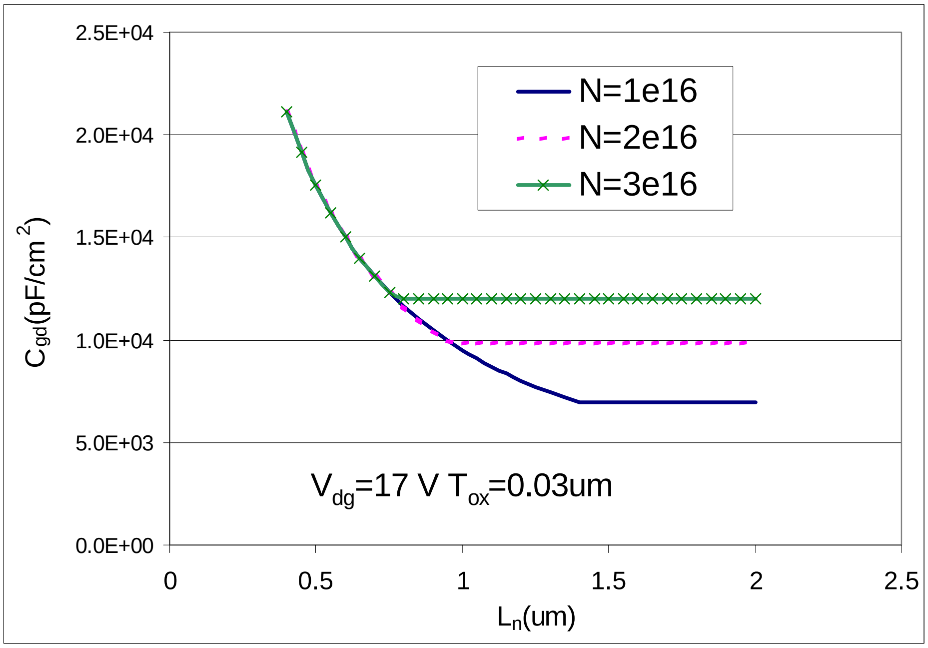


Fig. 3.17 One-dimensional modeling of C_{gd}.

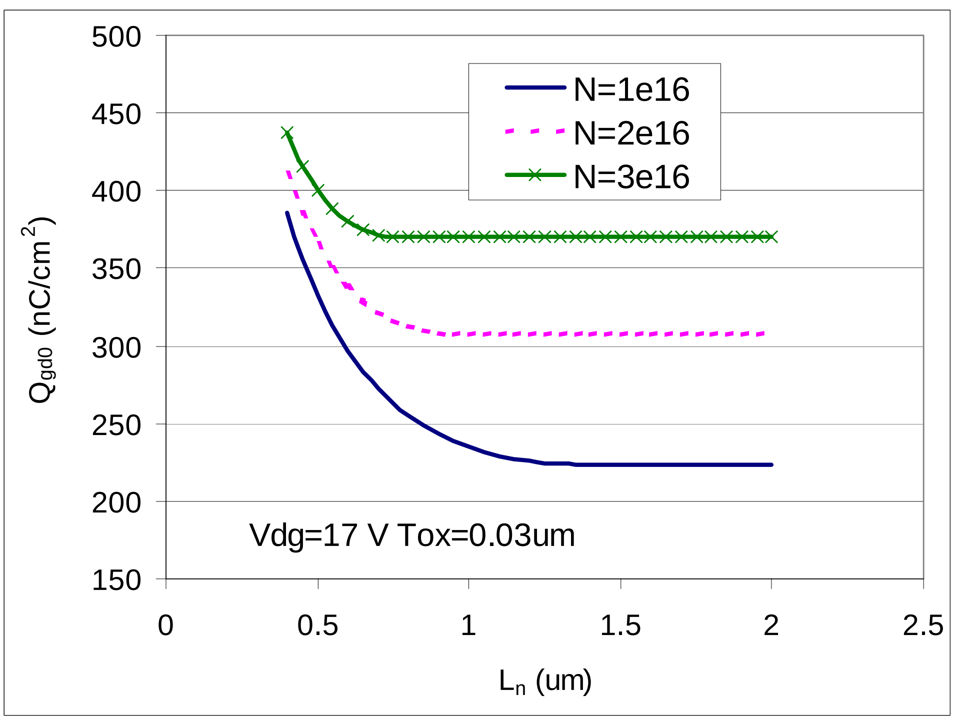


Fig. 3.18 One-dimensional modeling of Q_{gd0}.

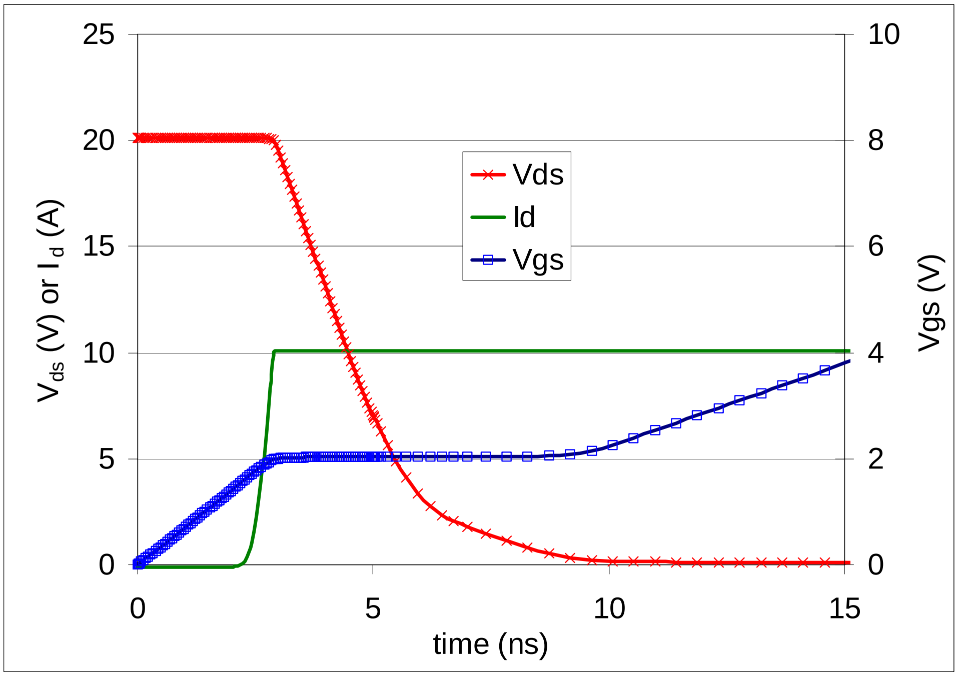


Fig. 3.19 Simulated turn-on waveforms.

3.3.3 Analysis of the Switching Process With Non-Constant C_{gd}

The switching process of the MOSFET under the inductive load is described in section 3.2.2 with the assumption that the gate-to-drain capacitance (C_{gd}) is constant. In this section, the switching process is revised based on the C_{gd} and Q_{gd} models developed in the preceding section. Because the turn-off process is a reverse order of the turn-on process, only the turn-on process is addressed in this section. The conclusions of the turn-on process are applicable for the turn-off process.

Fig. 3.19 shows the general turn-on waveforms generated by Medici simulation. The main difference between Fig. 3.19 and Fig. 3.8 is that in Fig. 3.8 the drain voltage drops linearly, while in Fig. 3.19 the drain voltage drops quickly at the beginning, then has a slow linear drop. This phenomenon is explained and described as follows.

1) Turn-on delay. From T_0 to T_1, the MOSFET is off. Load current I_o flows through the diode (D_{pbd}), and the drain voltage of the MOSFET equals the level of V_{in}. When I_g is applied on the gate, the gate voltage will rise and the V_{dg} will decrease. Fig. 3.16 shows that when V_{dg} is high, the variation of C_{gd} is not much. Therefore, the gate-to-source voltage rises linearly as

$$V_{gs} = \frac{I_g}{C_{iss}} t \approx \frac{I_g}{C_{gs} + C_{gd}} t \,, \tag{3.36}$$

where C_{gd} is expressed by Equation (3.26). The total gate charge in this stage is

$$Q_{gs1} = V_{th} \times (C_{gs} + C_{gd}) \,. \tag{3.37}$$

It takes

$$t_{01} = \frac{Q_{gs1}}{I_g} \tag{3.38}$$

for V_{gs} to reach the threshold voltage (V_{th}). Then, the MOSFET starts to conduct, and the turn-on process enters the second stage.

2) Current rising. In this period, since the drain voltage of the MOSFET is clamped at V_{in}, C_{gd} can still be approximated by Equation (3.26). For the non-punch-through type of depletion region, we can use $V_{dg} = V_{in} - V_{th}$ to find the depletion width (W_{dpl}); for the punch-through type of depletion region, the depletion width equals the length of the drift region (L_n).

Since C_{gd} is assumed to be constant, the derivation in the section (3.2.2) is still valid. The power loss on the MOSFET in this period is

$$E_{gs2} = \frac{1}{3} \frac{V_{in} I_o V_{eff} C_{iss}}{I_g} \,. \tag{3.39}$$

It takes

$$t_{gs2} = \frac{V_{eff} C_{gs}}{I_g} \tag{3.40}$$

for V_{gs} to reach

$$V_{gson} = V_{th} + V_{eff} \,. \tag{3.41}$$

Then, the drain voltage starts to drop and the circuit enters the third stage.

3) Voltage falling. At the beginning of this period, the drain-to-gate voltage is

$$V_{dg0} = V_{in} - V_{gson} . \tag{3.42}$$

The expression of the initial gate-to-drain charge Q_{gd0} depends on whether the depletion region is the punch-through type. If the depletion region is punched through, Equation (3.30) should be used to determine Q_{gd0}; otherwise Equation (3.24) should be used. Since a constant current is applied on the gate, the variation of the gate-to-drain charge Q_{gd} is

$$Q_{gd} = Q_{gd0} - I_g t . \tag{3.43}$$

For the punch-through type of depletion region, the drain voltage can be derived using Equation (3.30), such that

$$V_d = \frac{Q_{gd0} - I_g t}{\varepsilon_{si}}(L_n + \alpha T_{ox}) - \frac{\beta L_n^2}{2} + (V_{th} + V_{eff}) . \tag{3.44}$$

As Q_{gd} continues to decrease, the depletion region will change into the non-punch-through type, so

$$Q_{gd} = \frac{\beta L_n \varepsilon_{si}}{2} . \tag{3.45}$$

Canceling Q_{gd} from Equation (3.43) and (3.45) yields

$$t_{pt} = \frac{Q_{gd0} - 0.5\beta L_n \varepsilon_{si}}{I_g} . \tag{3.46}$$

This is the time period needed for the punch-through type of depletion region to change into the non-punch-through type. In Equation (3.46), $(Q_{gd0} - 0.5\beta L_n \varepsilon_{si}) < 0$ (or $t_{pt} < 0$) means the initial depletion region is the non-punch-through type. Then, t_{pt} should be zero instead of negative, so the following Equation expresses t_{pt} correctly

$$t_{pt} = \frac{(Q_{gd0} - 0.5\beta L_n \varepsilon_{si}) + \left| Q_{gd0} - 0.5\beta L_n \varepsilon_{si} \right|}{2I_g} . \tag{3.47}$$

Therefore, the power loss in this stage is

$$E_{pt} = \int_0^{t_{pt}} I_o V_d \, dt = (Q_{gd0} t_{pt} - 0.5 I_g t_{pt}^2) \frac{L_n + \alpha T_{ox}}{\varepsilon_{si}} - (0.5\beta L_n^2 - V_{th} - V_{eff}) t_{pt} . \tag{3.48}$$

After the punch-through type of depletion region changes into the non-punch-through type, Equation (3.24) can be used to find that the drain voltage varies as

$$V_d = \frac{(Q_{gd0} - I_g t)^2}{2\beta \varepsilon_{si}^2} + \frac{(Q_{gd0} - I_g t) T_{ox}}{\varepsilon_{ox}} + (V_{th} + V_{eff}) \tag{3.49}$$

It takes

$$t_{npt} = \frac{Q_{gd0}}{I_g} - t_{pt} \tag{3.50}$$

for the drain voltage to drop to the level of the gate voltage ($V_{th} + V_{eff}$). The power loss in this period is

$$E_{npt} = \int_{t_{pt}}^{t_{pt}+t_{npt}} I_o V_d \, dt = \frac{\frac{I_g^2}{3}(t_{dpl}^3 - t_{pd}^3) - I_g Q_{gd0}(t_{dpl}^2 - t_{pd}^2) + Q_{gd0}^2 (t_{dpl} - t_{pd})}{2\beta\varepsilon_{si}^2} \tag{3.51}$$
$$+ \frac{T_{ox}}{\varepsilon_{OX}}[Q_{gd0}(t_{dpl} - t_{pd}) - 0.5 I_g (t_{dpl}^2 - t_{pd}^2)] + (V_{th} + V_{eff})(t_{dpl} - t_{pd}),$$

where

$$t_{dpl} = t_{pt} + t_{npt} \tag{3.52}$$

is the total time needed to extract the charge of the drift region. Therefore, the total loss during the depletion region discharge is

$$E_{dpl} = E_{pt} + E_{npt} \tag{3.53}$$

After t_{dpl}, the depletion region disappears, and the drain voltage continues dropping, as

$$V_d = (V_{th} + V_{eff}) - \frac{I_g t}{C_{gdox}}, \tag{3.54}$$

where C_{gdox} is defined in Equation (3.16). Therefore, it takes

$$t_{ox} = \frac{V_{th} C_{gdox}}{I_g} \tag{3.55}$$

before the MOSFET enters the linear region. The power loss during t_{ox} is

$$E_{ox} = \int_0^{t_{ox}} I_o V_d \, dt = \frac{I_o (V_{th} + 2V_{eff}) V_{th} C_{gdox}}{2 I_g}, \tag{3.56}$$

and the total power loss in this stage is

$$E_{qgd} = E_{dpl} + E_{ox}. \tag{3.57}$$

4) After the third stage, the MOSFET is on, and the gate voltage continue to rise as

$$V_{gs} = V_{th} + V_{eff} + \frac{I_g}{C_{gs} + C_{gdox}} t. \tag{3.58}$$

Since the MOSFET operates in the linear region, the drain voltage is

$$V_d = \frac{V_{eff}^2}{V_{gs} - V_{th}} . \qquad (3.59)$$

In the four stages of the turn-on process, the power loss occurs only during the second and third stages. Therefore, the total turn-on time is

$$t_{tn} = t_{gs2} + t_{dpl} + t_{ox} , \qquad (3.60)$$

and the total turn-on loss is

$$E_{tn} = E_{gs2} + E_{dpl} + E_{ox} . \qquad (3.61)$$

3.3.4 Worked Examples of the Switching Process with Non-Constant C_{gd} and Q_{gd}

In order to illustrate the different waveforms expressed by the analytical expressions that have been derived, it is worthwhile to work through some numerical examples. Initially, a set of typical MOSFET and application parameters are used. Then, the effects of the doping condition and gate oxide on the power loss are examined. The chosen parameters are based on the mainstream commercial high-side MOSFET, as follows.

- Input voltage V_{in} = 20 V
- Output current I_o = 10 A
- Current of the gate driver I_g = 1 A
- Total area of the gate to drain capacitance AA = 1.04 mm^2
- Threshold voltage of the MOSFET V_{th} = 1.58 V
- The effective gate voltage V_{eff} = 0.46 V
- Gate to source capacitance C_{gs} = 1280 pF
- Thickness the gate oxide T_{ox} = 300 Å
- Doping concentration of the drift layer N = 2×10^{16} cm^{-3}
- Width of the drift region L_n = 0.8 μm

In order to show the accuracy of the analytical modeling, both the calculation and simulation results are listed in table (3.1).

Table 3.1 Calculation and simulation results of the example.

Variable name	Simulation results	Calculation result	Related Equation
Delay time: t_{01}	2.23 ns	2.22 ns	(3.39)
Current rising time: t_{gs2}	0.65 ns	0.65 ns	(3.41)
Power loss during current rise: E_{gs2}	46.5 nJ	43.2 Nj	(3.40)
Depletion time: t_{dpl}	4.13 ns	3.56 ns	(3.53)
Depletion loss: E_{dpl}	361 nJ	309 nJ	(3.54)
Discharging time of C_{ox}: t_{ox}	2.17 ns	2.00 ns	(3.56)
Discharging loss of C_{ox}: E_{ox}	21.8 nJ	24.8 nJ	(3.57)
Total turn-on time: t_{tn}	6.95 ns	6.51 ns	(3.61)
Total turn-on loss: E_{tn}	430 nJ	378 nJ	(3.62)

The calculated waveform of power loss is compared with the simulation result in Fig. 3.20. Due to the fringing effect of C_{gd}, the simulated loss is more than that of the calculation. However, the analytical model properly describes the key steps of the turn-on process. Based on the analytical model, some design issues of the MOSFET are discussed as follows.

(1) Punch-through design or non-punch-through design of the drift region

At the end of section 3.3.2, we conclude that the punch-through type of drift region has more Q_{gd0} than that of the non-punch-through type of design. Since Q_{gd0} plays a very important role in the turn-on loss, the effect of the punch-through on the turn-on loss should be addressed. Fig. 3.21 shows that the punch-through results in more turn-on loss; Fig. 3.22 illustrates the waveforms of power loss for three different designs. From the calculation, we can conclude that the punch-through results in more turn-on loss than the non-punch-through design.

(2) Effect of the doping concentration of the drift region.

For the non-punch-through design, Fig. 3.18 shows that the lightly doped drift region has less charge. Therefore, we can expect the turn-on power loss to decrease as the doping concentration of the drift region decreases, as shown in Fig. 3.23 and Fig. 3.24.

(3) Effect of the thickness of the gate oxide.

Although thicker gate oxide leads to less Q_{gd0}, its effect on the turn-on loss is not as great as the doping concentration of the drift region. As shown in Fig. 3.25 and Fig. 3.26, the turn-on loss only drops significantly at the end of the turn-on process. This is because at the beginning of the turn-on process, the width of the depletion region is longer than T_{ox}, and T_{ox} does not have much effect on C_{gd} or the power loss.

From the switching loss standpoint, it is better to use the non-punch-through design, a lightly doped drift region and thicker gate oxide. However, the latter two design trends negatively impact the conduction loss of the MOSFET. The discussion of the design optimization will be presented in Chapter 4, in which the FEA model is employed to more accurately calculate the power loss.

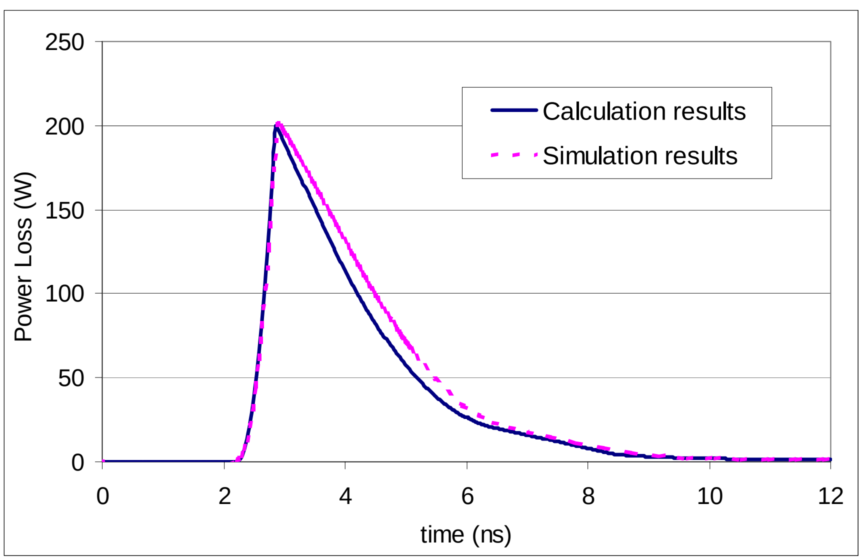


Fig. 3.20 Comparison of the simulation and calculation results.

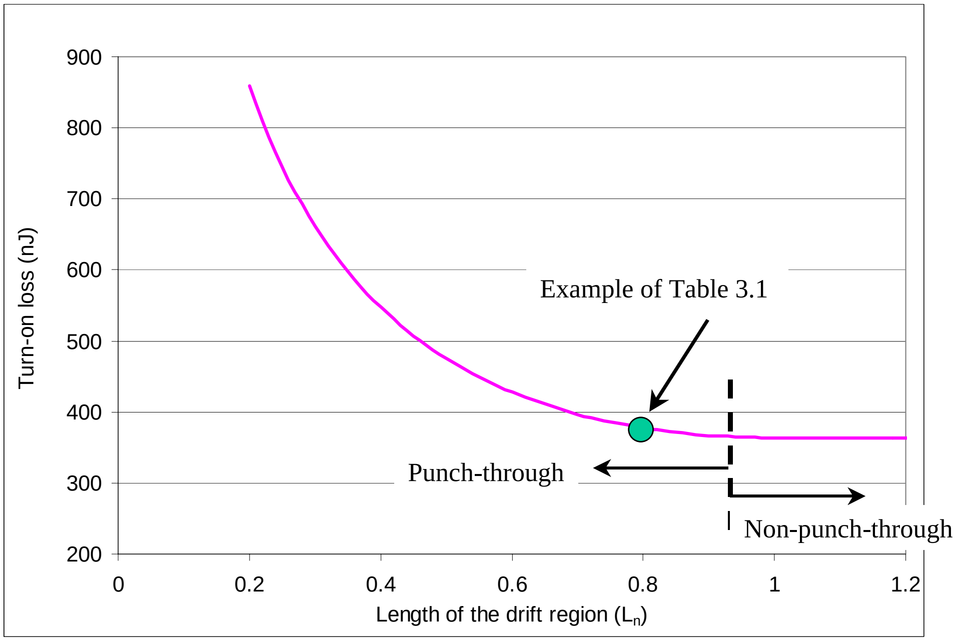


Fig. 3.21 Effect of the punch-through on the turn-on loss.

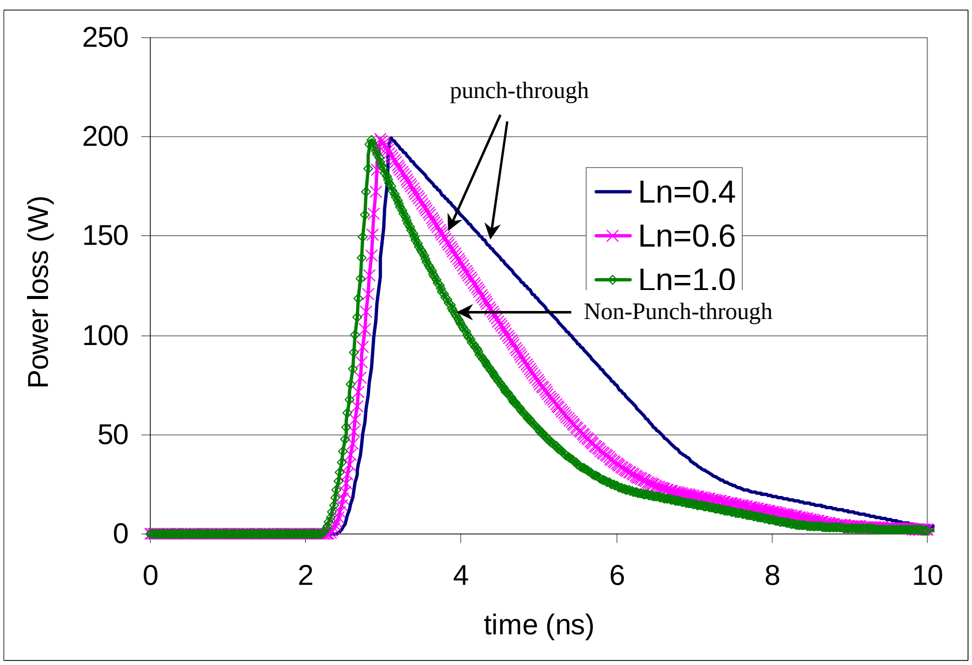


Fig. 3.22 Effect of the punch-through on the turn-on loss.

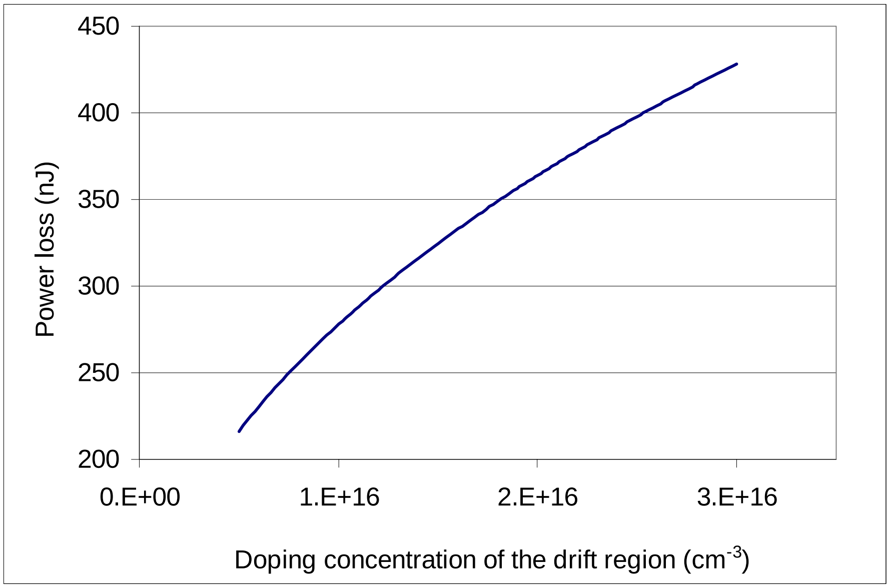


Fig. 3.23 Effect of the doping concentration on the turn-on loss.

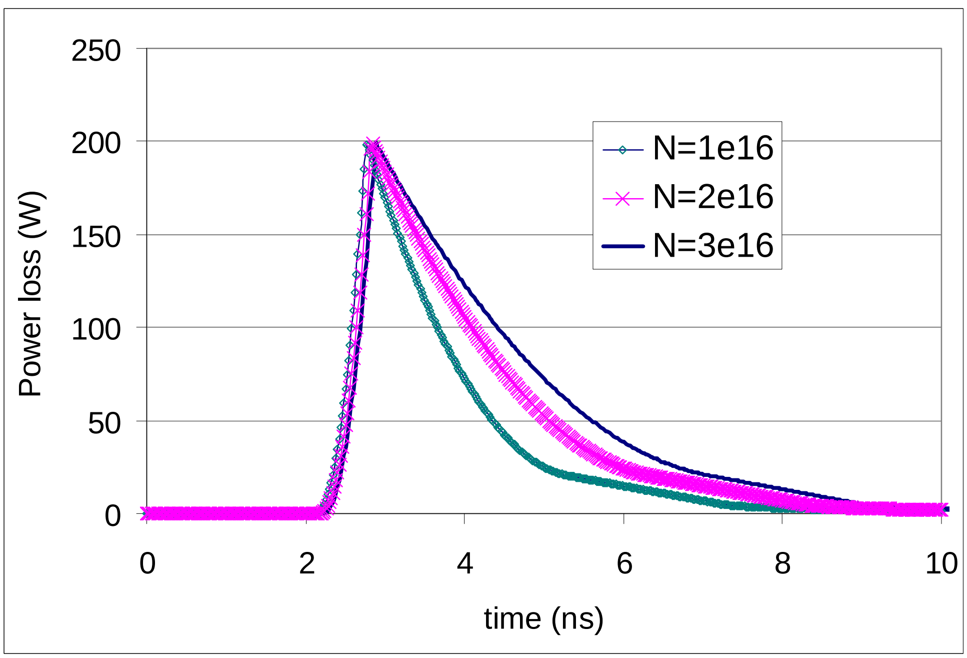


Fig. 3.24 Effect of the Doping concentration on the turn-on loss.

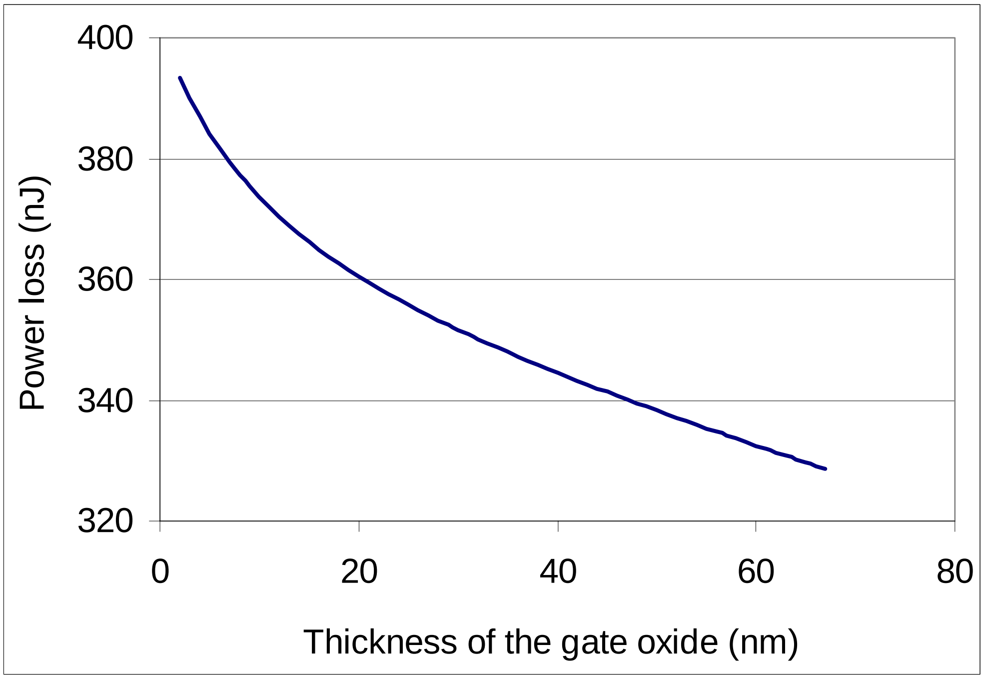


Fig. 3.25 Effect of the thickness of the gate oxide on the turn-on loss.

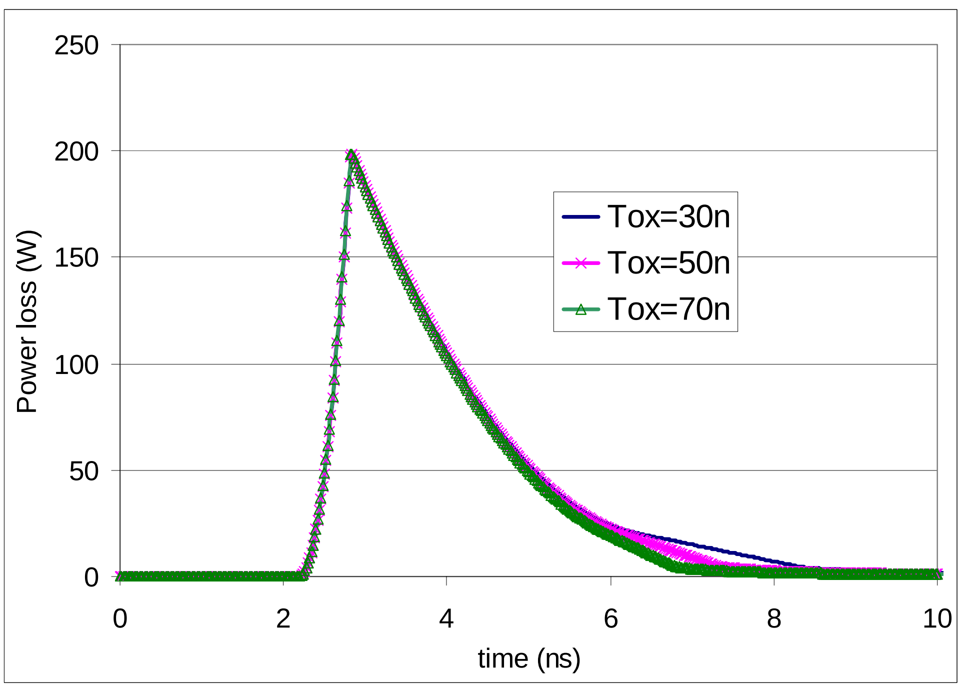


Fig. 3.26 Effect of the thickness of the gate oxide on the turn-on loss.

3.4 A Novel Model for MOSFET Switching Loss Calculation

In this section, a novel model for MOSFET switching loss calculation is presented, which takes into account the major parasitic elements ignored in Equations (3.2) and (3.3), providing more insight into the MOSFET switching process.

There are several papers dealing with the switching process of the MOSFET [B16], [B18]-[20]. However, no paper calculates the effect of L_s directly. The conclusion of the influence of L_s is that the L_s introduces an additional resistance into the gate circuit. Fig. 3.27 shows the general turn-on waveforms of I_d, V_{ds} and V_{gs}. As described before, the shape of V_{ds} is far from a straight line. The platform of V_{ds} leads to more power loss. In this section, a new method is provided to calculate the switching loss. Two assumptions are made in the following analysis: the capacitance value of C_{gd} and C_{gs} have fixed values; and The forward voltage drop of diode D_{pbd} is V_{fd}.

3.4.1 Analysis of the Turn-on Process

Based on the waveforms shown in Fig. 3.27, the turn-on process can be divided into the following four stages.

(1) Turn-on delay. In this period, the MOSFET is off. The current flows through the diode (D_{pbd}), the voltage drop on the inductor L_d is zero, and the voltage on the MOSFET drain is

$$V_{d1} = V_{in} + V_{fd} \,. \tag{3.62}$$

Ignoring the small gate current through the inductor L_s, the circuit can be reduced to the one shown in Fig. 3.28. Because when V_{ds} is high, C_{gs}>>C_{gd}, C_{gd} can be ignored. It takes time T_d for the gate voltage V_{gs} to ramp up to the level of V_t, such that

$$T_d = \tau_g \ln\left(\frac{V_{dr}}{V_{dr} - V_t}\right), \tag{3.63}$$

where

$$\tau_g = R_{drtt} C_{gs} \,. \tag{3.64}$$

Since there is no current through the MOSFET, the loss is zero in this period.

(2) I_d rises from 0 to I_o. At the beginning of this period, V_{ds} drops sharply and then stays at a rather constant value (V_{ds0}). In order to find out the value of V_{ds0}, the equivalent circuit depicted in Fig. 3.29 is employed, where C_{gd} is removed because $C_{gd} << C_{gs}$, and the Miller effect is insignificant when V_{ds} does not change much. In addition, the MOSFET is replaced with a voltage-controlled current source. Since the MOSFET works in the saturation region, the drain current can be expressed as

$$I_d = K(V_{gs} - V_t)^2 . \tag{3.65}$$

Because the current still goes through diode D_{pbd}, the voltage on the node d′ is clamped to

$$V_{clp} = V_{in} + V_{fd} . \tag{3.66}$$

Therefore, a voltage source V_{clp} is connected to the node d' directly, and both the current source Io and the diode D_{pbd} are removed from the equivalent circuit.

On the other hand, when the MOSFET operates in the saturation region, the small-signal model of the MOSFET is

$$I_{ds} = g_m V_{eff} , \tag{3.67}$$

where the transconductance g_m is

$$g_m = 2KV_{eff} . \tag{3.68}$$

In this case, it is easy to show that the input impedance has the following form in the S domain [E8]:

$$Z_{in} = R_{drtt} + g_m \frac{L_s}{C_{gs}} + sL_s + \frac{1}{sC_{gs}} . \tag{3.69}$$

At time zero, assume that a step change (V_{dr}) occurs at the gate supply voltage. Since g_m is very small when V_{gs} is small, at the beginning the term $g_m L_s/C_{gs}$ can be ignored. For the state-of-the-art 30V MOSFET, the typical value of R_{drtt} is from 2 to 4 Ω; Ls is from 1 to 2 nH; C_{gs} is from 1n to 4nF. For simplicity, we ignore the effect of L_s on Z_{in}, so the effective gate voltage ($V_{eff} = V_{gs} - V_t$) and the voltage on R_{drtt} take the form

$$V_{eff} = V_{dr}(1 - e^{-t/\tau g}) , \tag{3.70}$$

and $$V_{drtt} = V_{dr} e^{-t/\tau g} - V_t \,, \tag{3.71}$$

respectively, where the time constant τ_g is defined in Equation (3.64).

In order to determine the voltage V_{ds0}, we need to know when V_{ds} comes to a relatively stable value. Fortunately, the accuracy of the time (T_0) is not critical, because V_{ds} does not vary much in the vicinity of T_0. Assuming V_{ds} becomes stable when $V_{eff} = V_{rg}$, substituting (3.72) into (3.71) yields

$$T_0 \approx R_{drtt} C_{gs} \ln\left(\frac{2V_{dr}}{V_{dr} + V_t}\right). \tag{3.72}$$

However, from time 0 to time T_0, g_m rises rapidly. Since the time constant τ_g is not actually a constant, referring to Equation (3.69), a more precise expression for the time constant can be written as

$$\tau = \left(R_g + g_m \frac{L_s}{C_{gs}}\right) C_{gs} \,. \tag{3.73}$$

Ignoring R_g and substituting Equation (3.68) into (3.73) yields

$$\tau = 2KV_{eff} L_s \,. \tag{3.74}$$

A much more important approximation can be made, by reducing Equation (3.70) to the first order and then using Equation (3.74) to replace τ_g. This leads to

$$V_{gs} = \sqrt{\frac{V_{dr} t}{2KL_s}} + V_t \,. \tag{3.75}$$

Then, at time T_0, V_{gs} is

$$V_{gs0} = \sqrt{\frac{V_{dr} T_0}{2KL_s}} + V_t \,. \tag{3.76}$$

Because $V_{eff} = V_{rg}$ is assumed, at time T_0, the voltage drop on R_g is

$$V_{drtt0} = \sqrt{\frac{V_{dr} T_0}{2KL_s}} \,, \tag{3.77}$$

and the voltage on the source inductance L_s is

$$V_{ls0} = V_{dr} - V_{gs0} - V_{drtt00} = V_{dr} - 2\sqrt{\frac{V_{dr} T_0}{2KL_s}} - V_t \,. \tag{3.78}$$

Next, we know that the di/dt of L_s is

$$\alpha = \frac{V_{lso}}{L_s}. \tag{3.79}$$

Ignoring the gate current, L_d has the same di/dt as L_s, and the voltage on L_d is

$$V_{ld0} = V_{ls0}\frac{L_d}{L_s}. \tag{3.80}$$

Finally, we find the voltage V_{ds0},

$$V_{ds0} = V_{clp} - V_{ls0}(1 + \frac{L_d}{L_s}). \tag{3.81}$$

Equation (3.81) is valid when $V_{ds0} > V_{eff}$. Because the maximum value of V_{ls0} is V_{dr}, and $L_d < L_s$, $V_{ds0} > V_{eff}$ means that $V_{in} > 2V_{dr}$, which is true for the high-step-down DC-DC buck converter. The time needed for the current rising to I_o is

$$T_2 = \frac{I_o}{\alpha} = \frac{I_o L_s}{V_{ls0}}. \tag{3.82}$$

Then, the power loss in the second stage is

$$E_2 = 0.5 T_2 I_o V_{ds0} = 0.5\frac{I_o^2 L_s V_{ds0}}{V_{ls0}}. \tag{3.83}$$

(3) After I_d reaches I_o, the turn-on process enters into the third stage. The MOSFET is still in the saturation state. if we ignore the gate current, its drain current is equal to the level of I_o. Because I_d is rather stable in this period, L_s and L_d can be removed. The C_{gs} also can be ignored because voltage V_{gs} is almost unchanged, and is determined by

$$V_{gs3} = \sqrt{\frac{I_o}{K}} + V_t. \tag{3.84}$$

The equivalent circuit for this period is shown in Fig. 3.30. The current through C_{gd} is equal to the current through R_{drtt}, so

$$I_{cgd} = I_{drtt} = \frac{V_{dr} - V_{gs3}}{R_{drtt}}. \tag{3.85}$$

The voltage on the drain of the MOSFET is

$$V_{d3} = V_{ds0} - V_{cgd} = V_{ds0} - \frac{I_{cgd}}{C_{gd}}t. \tag{3.86}$$

where V_{ds0} is the initial voltage expressed by Equation (3.82). The time interval (T_3) for the drain voltage to drop from V_{ds0} to 0 V is

$$T_3 = \frac{V_{ds0} C_{gd}}{I_{cgd}} = \frac{V_{ds0}}{V_{dr} - V_{gs3}} \tau_{gd} \,, \tag{3.87}$$

where

$$\tau_{gd} = R_g C_{gd} \,. \tag{3.88}$$

The power loss for this period is

$$E_3 = 0.5 T_3 I_o V_{ds0} \,. \tag{3.89}$$

(4) After V_{ds} drops below V_{eff}, the MOSFET enters the linear region. V_{gs} continues rising to the level of V_{dr}, so

$$V_{gs} = V_{gs1} + (V_{dr} - V_{gs3})(1 - e^{-t/\tau iss}) \approx V_{gs3} + (V_{dr} - V_{gs3}) \frac{t}{\tau_{iss}} \,, \tag{3.90}$$

where the time constant τ_{iss} is

$$\tau_{iss} = R_g C_{iss} \,. \tag{3.91}$$

Based on the first-order approximation made in Equation (3.90), it takes time interval $T_4 = \tau_{iss}$ to finish the fourth stage. Because the MOSFET works in the linear region, it can be modeled as a voltage-controlled resistor, as shown in Fig. 3.31:

$$R_{ds} = \frac{1}{2K(V_{gs} - V_t)} \,. \tag{3.92}$$

Because the current through the MOSFET is I_o, V_{ds} is given by

$$V_{ds} = \frac{I_o}{2K(V_{gs} - V_t)} \,. \tag{3.93}$$

Then, the power loss in this phase is

$$E_4 = I_o \int_0^{\tau iss} V_{ds} dt = \frac{\tau_{iss} I_o^2}{2K(V_{dr} - V_{gs3})} \ln \frac{V_{dr} - V_t}{V_{gs3} - V_t} \,. \tag{3.94}$$

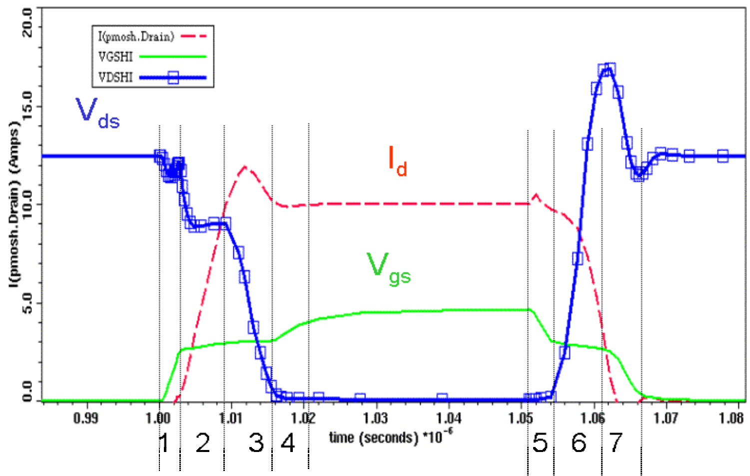


Fig. 3.27 General switching waveforms.

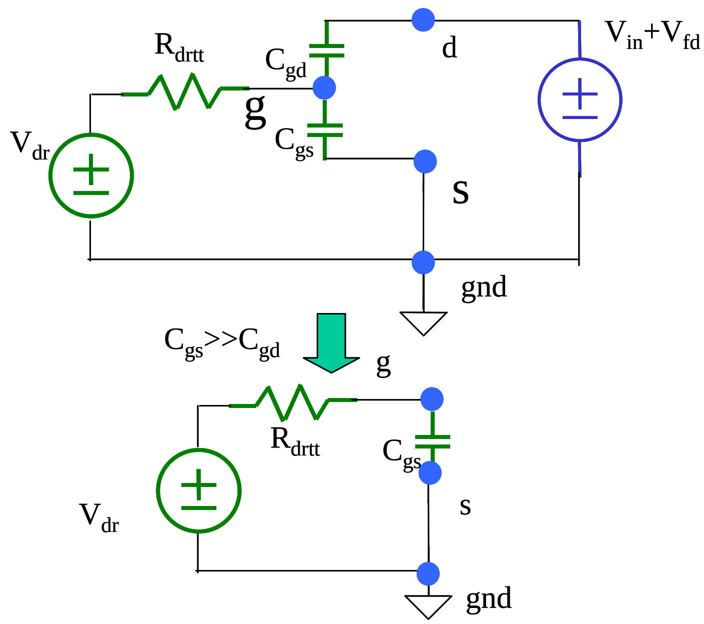


Fig. 3.28 Equivalent circuit of turn-on process.

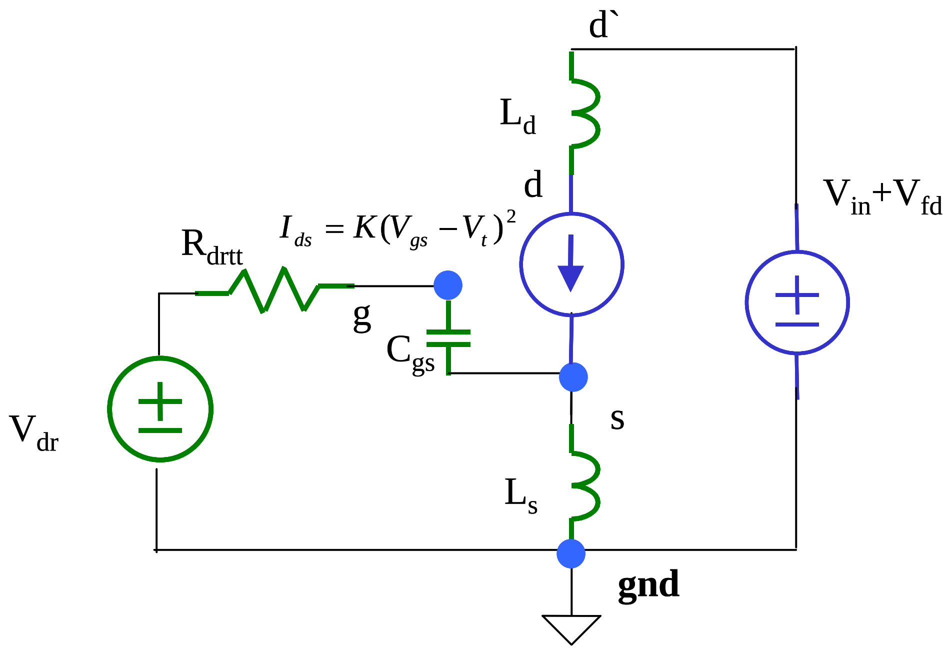


Fig. 3.29 Equivalent circuit of turn-on process.

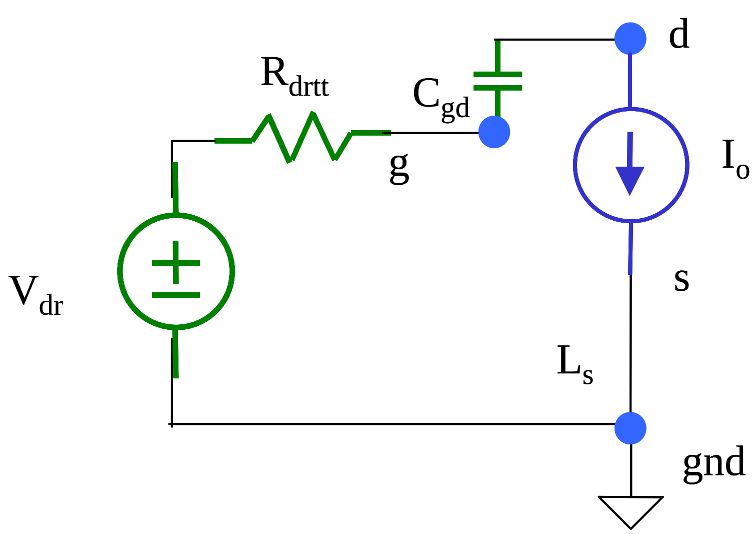


Fig. 3.30 Equivalent circuit of turn-on process.

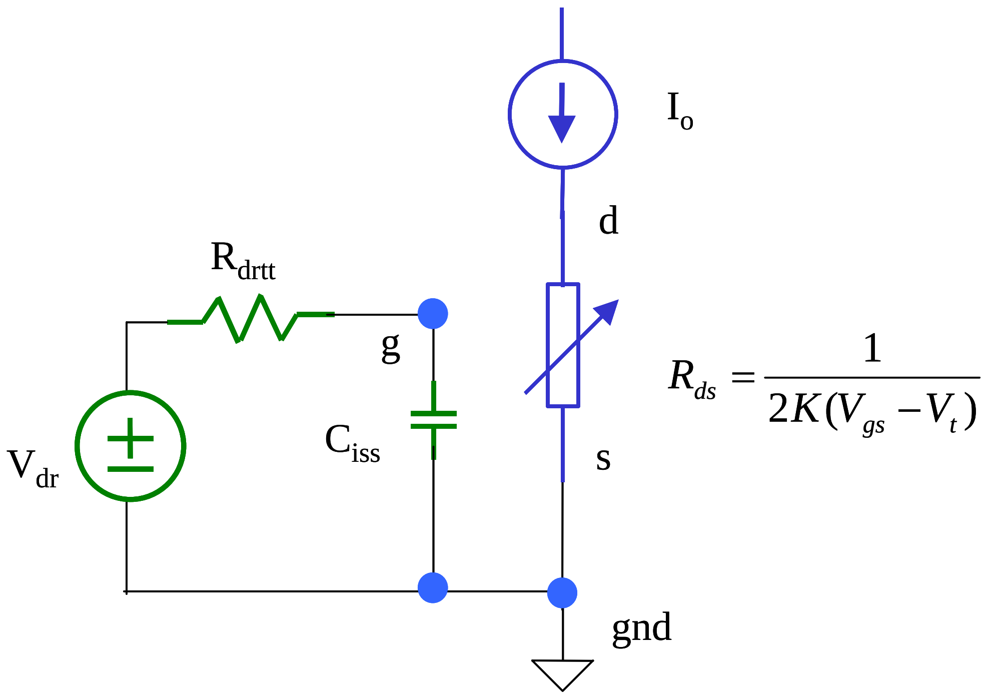


Fig. 3.31 Equivalent circuit of turn-on process.

3.4.2 Analysis of the Turn-off Process

Although the turn-off process is a reverse order of the turn-on process, its gate driving condition is not the same as that of the turn-on process. In the turn-on process, the gate current is driven by the voltage of V_{dr}, while in the turn-off process, the gate is shorted to the ground.

(5) At the beginning of the turn-off process, as shown in Fig. 3.32, I_d remains at I_o, and there is little variation in the level of V_{ds} is not much. The V_{gs} drops exponentially, as

$$V_{gs} = V_{dr} e^{-t/\tau iss} . \tag{3.95}$$

Since the MOSFET is in the linear region, V_{ds} is determined by Equation (3.93). As a first-order approximation, we can use Equation (3.95) to determine the time needed for the MOSFET to leave the linear region, so

$$T_5 = (1 - \frac{V_{gs3}}{V_{dr}})\tau_{iss} . \tag{3.96}$$

Then, the power loss in this period is

$$E_5 = \int_0^{T5} I_o V_{ds} dt = \frac{I_o^2 \tau_{iss}}{2KV_{dr}} \ln \frac{V_{dr} - V_t}{V_{gs3} - V_t} . \qquad (3.97)$$

(6) When the MOSFET enters the saturation region, the equivalent circuit depicted in Fig. 3.33 applies. It is rather like the second stage of the turn-on process. The difference is that the current through R_{drtt} (or the current through C_{gd}) is

$$I_{cgd} = I_{drtt} = \frac{V_{gs3}}{R_{drtt}} . \qquad (3.98)$$

The voltage on the drain of the MOSFET can be expressed as

$$V_{ds} = V_{gs3}(1 + \frac{t}{R_g C_{gd}}) . \qquad (3.99)$$

This stage comes to an end when V_{ds} reaches V_{in}+V_{fd}; therefore the time interval for this phase is

$$T_6 = \frac{V_{in} + V_{fb} - V_{gs3}}{V_{gs3}} \tau_{gd} . \qquad (3.100)$$

Then, the power loss in this period is

$$E_6 = 0.5(V_{gs3} + V_{in} + V_{fb}) I_o T_6 . \qquad (3.101)$$

(7) After V_{ds} reaches V_{in} + V_{fd}, the current starts to drop. Because in this phase the V_{ds} is rather stable, the effect of C_{gd} can be ignored, and the equivalent circuit shown in Fig. 3.34 applies. After ignoring the inductive part sL_s, V_{gs} takes the following form:

$$V_{gs} = V_{gs3} e^{-\frac{t}{\tau}} , \qquad (3.102)$$

where the time constant τ is

$$\tau = R_g C_{gs} + g_m L_s = R_g C_{gs} + 2KV_{gs} L_s . \qquad (3.103)$$

Actually, τ is not a constant, and the minimum value of τ is

$$\tau_g = R_g C_{gs} . \qquad (3.104)$$

If we expand Equation (3.102) to the first order and use τ_g to replace the variable τ, we obtain

$$V_{gs} = V_{gs3}(1 - \frac{t}{\tau_g}) . \qquad (3.105)$$

Since the MOSFET is in the saturation region, the current through the MOSFET can be expressed as

$$I_d = K\left[V_{gs3}(1-\frac{t}{\tau_g})-V_t\right]^2 = I_o(1-\beta\cdot t)^2\,, \tag{3.106}$$

where
$$\beta = \frac{V_{gs3}}{(V_{gs3}-V_t)\tau_g}\,. \tag{3.107}$$

Respectively, the voltages on L_s and L_d are

$$V_{ls} = L_s\frac{dI_d}{dt} = \frac{2KL_sV_{gs3}}{\tau_g}\left[(V_{gs3}-V_t)-\frac{V_{gs3}}{\tau_g}t\right], \tag{3.108}$$

and
$$V_{ld} = L_d\frac{dI_d}{dt} = \frac{2KL_dV_{gs3}}{\tau_g}\left[(V_{gs3}-V_t)-\frac{V_{gs3}}{\tau_g}t\right]. \tag{3.109}$$

Then, we can find the expression of V_{ds}, such that

$$V_{ds} = V_{in}+V_{fd}+V_{ls}+V_{ld} = V_{\max}-\gamma\cdot t\,, \tag{3.110}$$

where
$$V_{\max} = V_{in}+V_{fd}+\frac{2K(L_s+L_d)V_{gs3}}{\tau_g}(V_{gs3}-V_t)\,, \tag{3.111}$$

and
$$\gamma = \frac{2K(L_s+L_d)V_{gs3}^2}{\tau_g^2}\,. \tag{3.112}$$

This period comes to the end when V_{gs} drops to V_t. Therefore, we can find the duration from Equation (3.105), as follows

$$T_7 = (1-\frac{V_t}{V_{gs3}})\tau_g\,. \tag{3.113}$$

The power loss in this period is

$$E_7 = \int_0^{T_7}V_{ds}I_d dt = I_o\left[\frac{-\beta^2\gamma\cdot T_7^4}{4}+\frac{(2\beta\gamma+V_{\max}\beta^2)T_7^3}{3}-\frac{(\gamma+2V_{\max}\beta)T_7^2}{2}+V_{\max}T_7\right]. \tag{3.114}$$

(8) When V_{gs} drops below V_t, the MOSFET turns off. Since V_{ds} is high, C_{ds} can be ignored, and the input capacitor C_{gs} continues to discharge through the resistor R_{drtt} (Fig. 3.35) until V_{gs} reaches zero. Because

$$V_{gs} = V_t e^{-t/\tau_g}\,, \tag{3.115}$$

it takes

$$T_8 = 2.3\tau_g \tag{3.116}$$

for V_{gs} to reach 10% of the level of V_t.

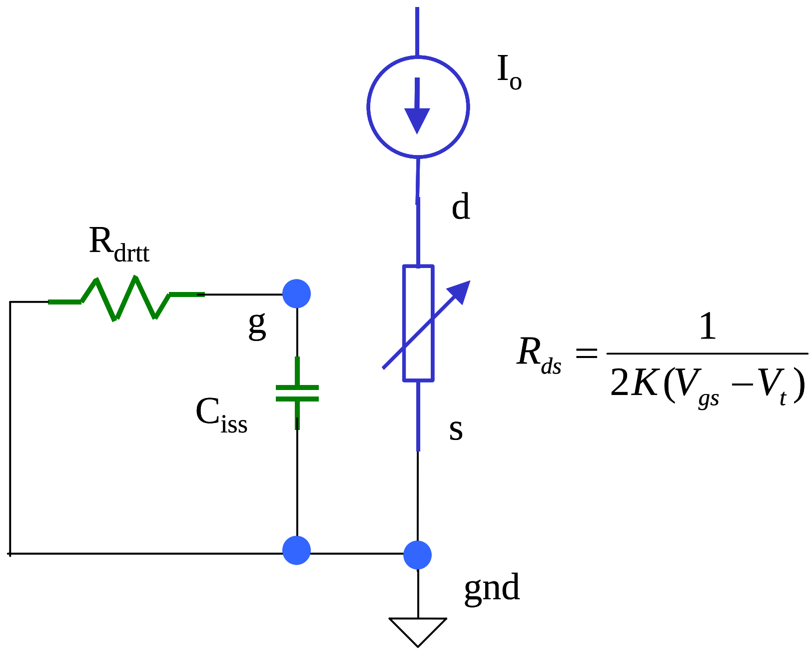


Fig. 3.32 Equivalent circuit of turn-off process.

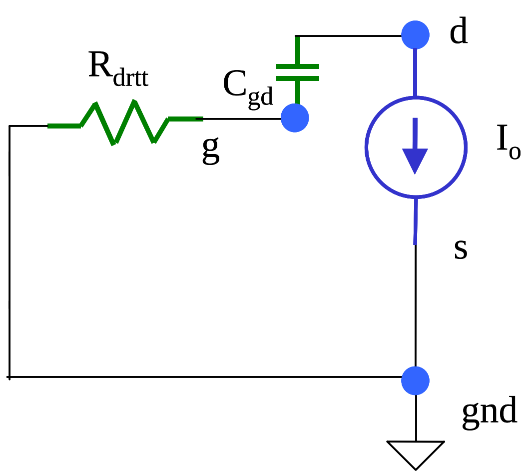


Fig. 3.33 Equivalent circuit of turn-off process.

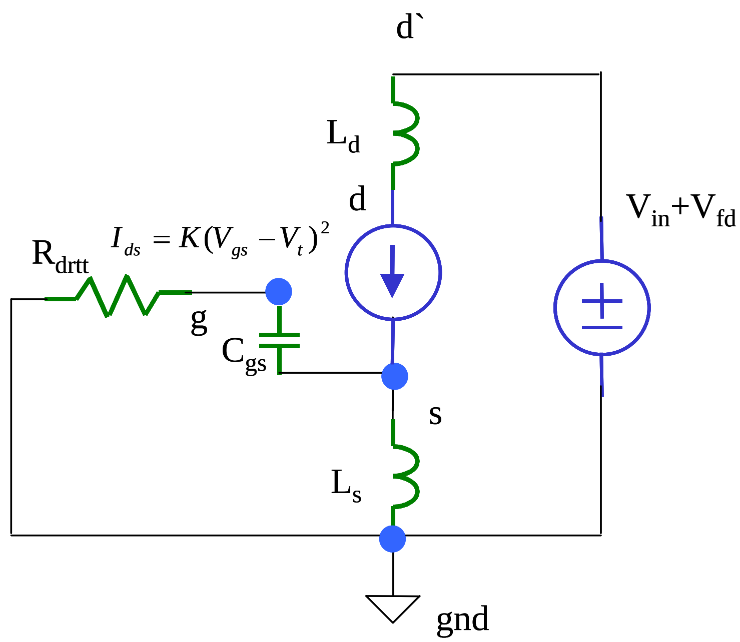


Fig. 3.34 Equivalent circuit of turn-off process.

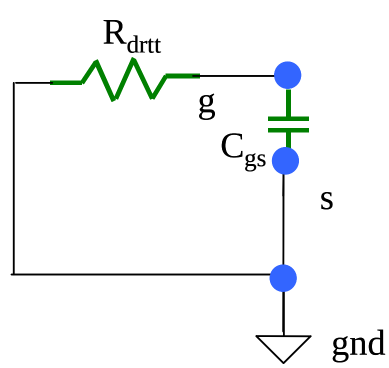


Fig. 3.35 Equivalent circuit of turn-off process.

3.4.3 Worked Example of the Switching Process

In this section, the effects of the parasitic inductance on the switching loss are examined. The chosen parameters are as follows.

- Input voltage V_{in} = 20 V
- Clamping voltage V_{clp} = 2.2 V

- Output current $I_o = 10$ A
- Gate drive current $I_g = 1$ A
- Gate drive voltage $V_{dr} = 5$ V
- Threshold voltage $V_t = 1.73$ V
- Gate-to-source capacitance $C_{gs} = 0.72$ nF
- Gate-to-drain capacitance $C_{gd} = 28.6$ pF
- $K = 3.3$ A/V^2

The effects of L_s and L_d on the switching loss are shown in Fig. 3.36 and Fig. 3.37, respectively. Larger L_s results in more turn-on and turn-off losses, but the switching loss is not sensitive to L_d. However, L_d leads to more voltage stress in the turn-on process, as expressed in Equation (3.111). Therefore, both L_s and L_d should be minimized in the package and circuit design.

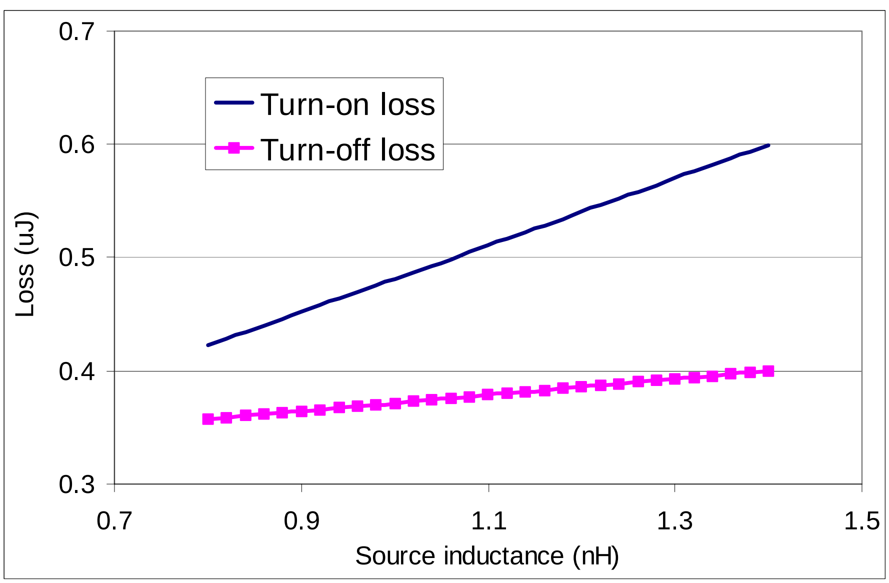


Fig. 3.36 Effect of L_s on the switching loss ($L_d = 0.8$ nH).

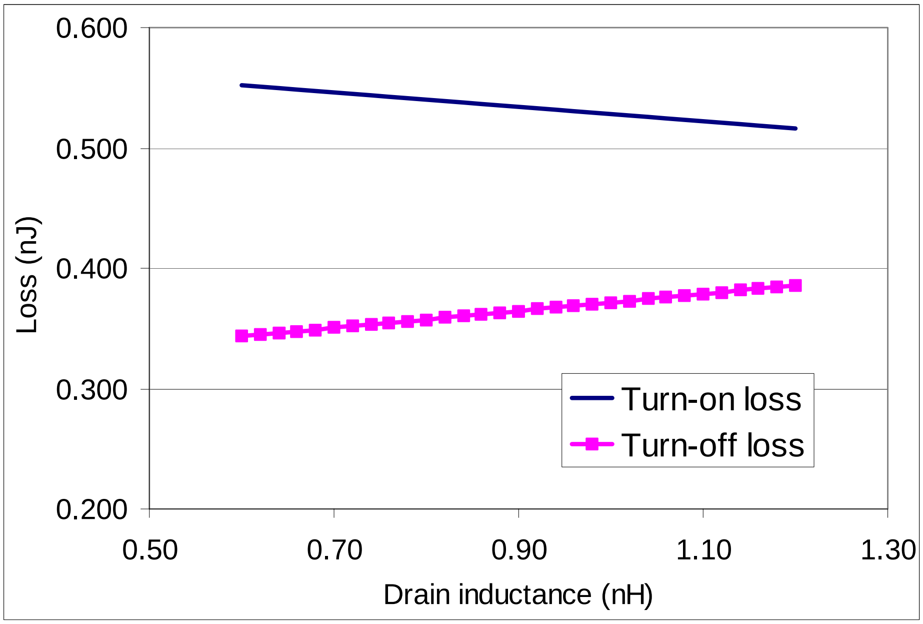


Fig. 3.37 Effect of L_d on the switching loss (L_s = 1.2 nH).

3.5 Analysis of dv/dt-Induced Spurious Turn-on of the MOSFET

In the preceding sections, the switching loss of the high-side MOSFET is analyzed. It seems that the loss of the high-side MOSFET is more difficult to model than that of the low-side MOSFET, since the dominant loss of the low-side MOSFET is the conduction loss. However, the low-side MOSFET suffers another dv/dt-induced loss [B21]-[B23], which is even more complex than the switching process of the high-side MOSFET.

When the high-side MOSFET is turning on, the drain voltage of the low-side MOSFET rises rapidly. This means the drain of the low-side MOSFET has a high-dv/dt condition, which will lead to an increase in the voltage of the gate of the low-side MOSFET. If the dv/dt is large enough, the low-side MOSFET will be turned on again even though its gate is tied to the ground by the driver. Because this is a high-order nonlinear problem, it is very difficult to determine the loss related to this type of dv/dt-induced turn-on. In this section, an analytical model is presented to calculate the spurious turn-on voltage. The analysis of the spurious turn-on loss is performed in Chapter 4 by FEA.

The equivalent circuit of the MOSFET in this case is shown in Fig. 3.38, where R_{gs} includes both the gate resistance of the power MOSFET and the pull-down resistance of the driver. Since the MOSFET is off before the spurious turn-on occurs, the MOSFET can be removed from the circuit (Fig. 3.39). Because the general solution of the problem leads to fourth order differential Equations, we have to simplify the problem by ignoring the less important parasitic components and consider their effects later. The estimation of parasitic components is based on the 20V to 30V state-of-the-art MOSFET, for which $L_g >> L_s$ and L_d, and $C_{gs}>>C_{gd}$ and C_{ds}. Because the impedance from node G to the ground is much larger than that from node S to the ground and $C_{gs}>>C_{gd}$, Fig. 3.39 can be reduced to the circuit illustrated in Fig. 3.40 and Fig. 3.41. In Fig. 3.41, the total impedance from node D to the ground is

$$Z_D = \frac{s^2 L_{ds} C + 1}{sC}, \tag{3.117}$$

where
$$C = \frac{C_{gs} \cdot C_{gd}}{C_{gs} + C_{gd}} + C_{ds} \approx C_{gd} + C_{ds} = C_{oss}, \tag{3.118}$$

and
$$L_{ds} = L_d + L_s. \tag{3.119}$$

Assuming a linearly rising voltage is applied to the drain, such that

$$V_{in} = Kt, \tag{3.120}$$

then the total current in the s domain can be expressed as

$$I_t = \frac{V_{in}}{Z_D} = \frac{K}{s} \frac{C_{oss}}{s^2 L_{ds} C_{oss} + 1} = KC_{oss}\left(\frac{1}{s} - \frac{s}{s^2 + \omega_0^2}\right), \tag{3.121}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_{ds} C_{oss}}}. \tag{3.122}$$

Next, the current through the capacitor C_{gd} can be found by:

$$I_{gd} = \frac{I_t C_{gd}}{C_{oss}} = KC_{gd}\left(\frac{1}{s} - \frac{s}{s^2 + \omega_0^2}\right), \tag{3.123}$$

and the voltage on node S is

$$V_s = I_t s L_s = \frac{K L_s C_{oss}}{s^2 L_{ds} C_{oss} + 1}. \tag{3.124}$$

Both current I_{gd} and voltage Vs contribute to the gate-to-source voltage V_{gs}. We first calculate the V_{gs} generated by the current I_{gd} based on the circuit depicted in Fig. 3.42, where the node S is connected directly to the ground. The influence of voltage V_s on voltage V_{gs} will be taken into account later. In order to simplify the calculation, the current I_{gd} is split into two parts, as follows

$$I_{gd} = I_{cgddc} + I_{cgdac}, \tag{3.125}$$

where I_{gddc} represents the constant DC current

$$I_{gddc} = K C_{gd} \frac{1}{s}, \tag{3.126}$$

and I_{gdac} represents the AC current

$$I_{gdac} = -K C_{gd} \frac{s}{s^2 + \omega_0^2}. \tag{3.127}$$

The impedance from G to the ground is

$$Z_g = \frac{R_{gs} + s L_g}{s^2 L_g C_{gs} + s R_{gs} C_{gs} + 1}. \tag{3.128}$$

Therefore, V_{gs}, excited by the DC component of I_{gd}, is

$$V_{gsdc} = I_{cgddc} \cdot Z_g = K C_{gd} \frac{R_{gs} + s L_g}{s(s^2 L_g C_{gs} + s R_{gs} C_{gs} + 1)}. \tag{3.129}$$

The V_{gsdc} in the time domain is

$$V_{gsdc} = K \cdot C_{gd} \left[R_{gs}(1 - e^{-t/\tau} \cos \omega t) + \frac{2L_g - R_{gs}^2 C_{gs}}{2\omega L_g C_{gs}} e^{-t/\tau} \sin \omega t \right], \tag{3.130}$$

where

$$\tau = \frac{2L_g}{R_{gs}}, \tag{3.131}$$

and

$$\omega = \sqrt{\frac{1}{L_g C_{gs}} - \frac{R_{gs}^2}{4L_g^2}}. \tag{3.132}$$

The V_{gs}, excited by the AC component of I_{gd}, is

$$V_{gsac} = I_{cgdac} \cdot Z_g = -K \cdot C_{gd} \cdot \frac{s}{s^2 + \omega_0^2} \cdot \frac{R_{gs} + sL_g}{s^2 L_g C_{gs} + sR_{gs} C_{gs} + 1}. \qquad (3.133)$$

In order to simplify the solution, we assume that $L_g >> R_{gs}^2 C_{gs}$, so the expression of V_{gsac} in the time domain is

$$V_{gsac} = -\frac{KC_{gd}\omega_g^2}{\omega_0}\left[\frac{R_{gs}}{\omega_0}(\cos\omega_g t - \cos\omega_0 t) + L_g \sin\omega_0 t\right], \qquad (3.134)$$

where

$$\omega_g = \sqrt{\frac{1}{L_g C_{gs}}}. \qquad (3.135)$$

Since Rgs/ω0<<Lg, Vgsac can be reduced to

$$V_{gsac} = -\frac{KL_g C_{gd}\omega_g^2}{\omega_0}\sin\omega_0 t. \qquad (3.136)$$

The sinusoidal voltage at node S, expressed by Equation (3.124), also gives rise to the voltage V_{gs}. From nodes S to G, C_{gs} provides a path with the least impedance. Therefore, we can use the simplified circuit (Fig. 3.43) to find the voltage V_{gs} generated by V_s, which in the s domain is given by

$$V_{gss} = -K\omega_0^2 L_s C_{oss}\frac{1}{s^2 + \omega_0^2}\frac{1}{s^2 L_g C_{gs} + sR_{gs} C_{gs} + 1}. \qquad (3.137)$$

With the assumption that $L_g >> R_{gs}^2 C_{gs}$, the solution of V_{gss} in the time domain can be approximated as

$$V_{gss} = -\frac{KL_s C_{oss}}{L_g C_{gs}}\left[\frac{1}{\omega_g}\sin\omega_g t - \frac{e^{-t/\tau}}{\omega_0}\sin\omega_0 t\right]. \qquad (3.138)$$

The total V_{gs} is the sum of V_{gsdc}, V_{gsac} and V_{gss}, so

$$V_{gs} = V_{gsdc} + V_{gsac} + V_{gss}. \qquad (3.139)$$

The typical waveform of V_{gs} and its three components are shown in Fig. 3.44. The peak value of Vgs can be approximated as

$$V_{\max} = KC_{gd}R_{gs} + KC_{gd}\left(\frac{1}{C_{gs}} - \frac{R_{gs}^2}{4L_g}\right)\sqrt{(L_d + L_s)(C_{gd} + C_{ds})}\ . \qquad (3.140)$$

In Equation (3.140), the first term $KC_{gd}R_{gs}$ represents the results ignoring the parasitic inductance, and the second part shows the effect of these parasitics. The inductors L_d, L_s and L_g and the capacitor C_{ds} lead to more V_{gs}. However, the capacitor C_{gs} reduces V_{gs}. Fig. 3.45 compares the V_{max} with and without the second part. Because the effect of C_{gs} is contrast to the others, the difference of the two curves in Fig. 3.45 is not significant.

Some assumptions are made in the derivation of the analytical expression of V_{gs}. The accurate solution of V_{gs} can be found by Pspice simulation. Fig. 3.46 compares the analytical and simulation results. The error of V_{max} is rather small.

Equation (3.133) shows that the most effective way to reduce the spurious turn-on voltage is to decrease the gate-to-drain capacitance. This means, for the same MOSFET structure, the larger active area has more spurious turn-on voltage as shown in Fig. 3.47.

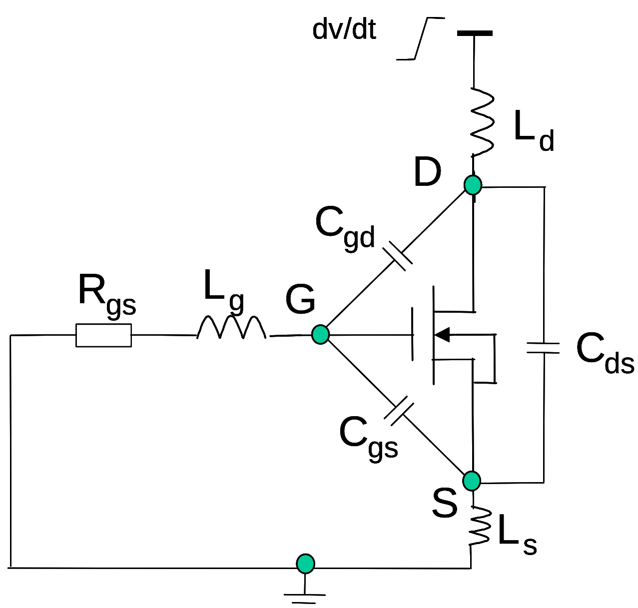


Fig. 3.38 Equivalent circuit of power MOSFET for dv/dt-induced spurious turn-on analysis.

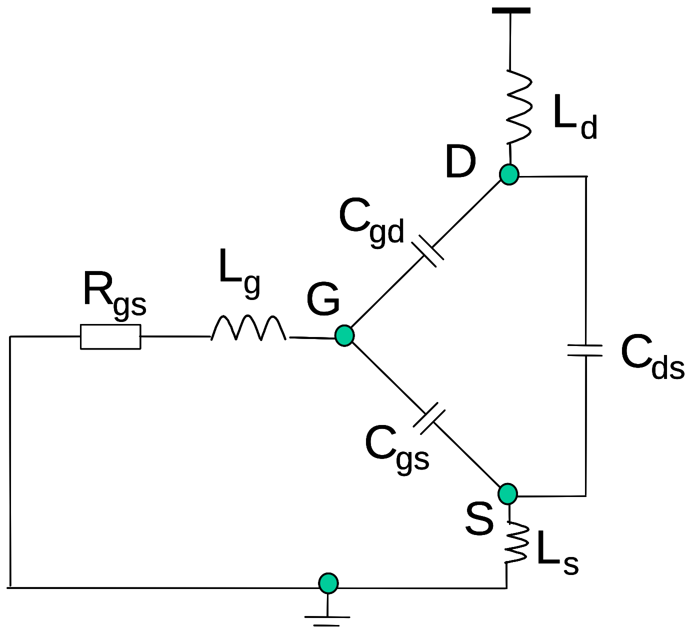


Fig. 3.39 Equivalent circuit of power MOSFET for dv/dt induced spurious urn-on analysis. MOSFET is removed from Fig. 3.38

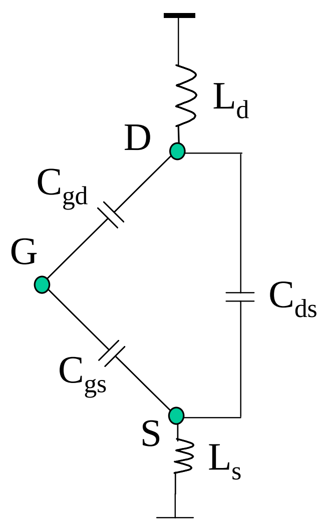


Fig. 3.40 Equivalent circuit of power MOSFET for dv/dt induced spurious urn-on analysis.

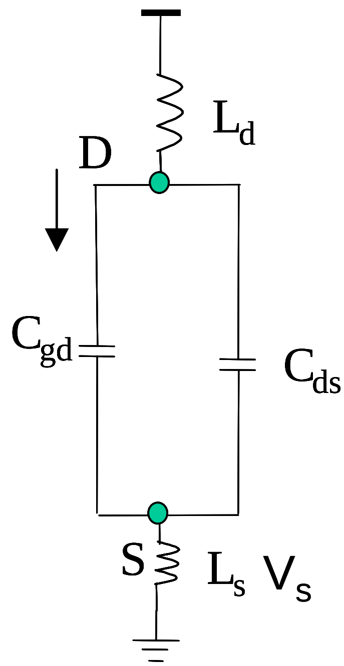


Fig. 3.41 Equivalent Circuit of Power MOSFET for dv/dt induced spurious urn-on Analysis.

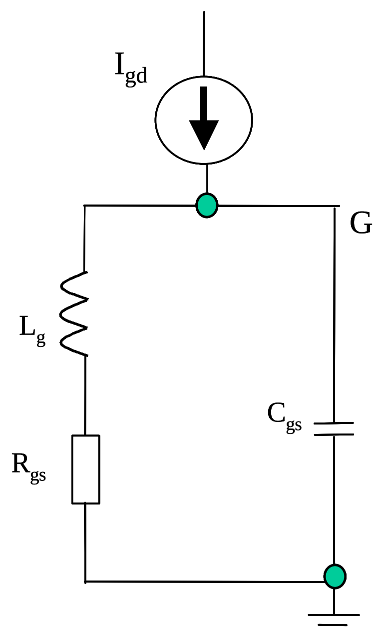


Fig. 3.42 Circuit considering the I_{gd} effect.

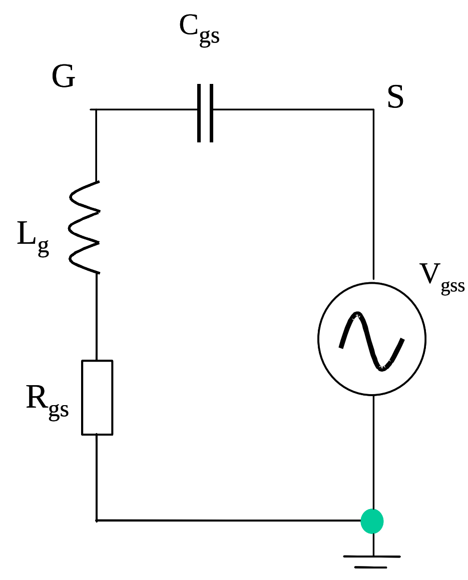


Fig. 3.43 Circuit considering the V_{gss} effect.

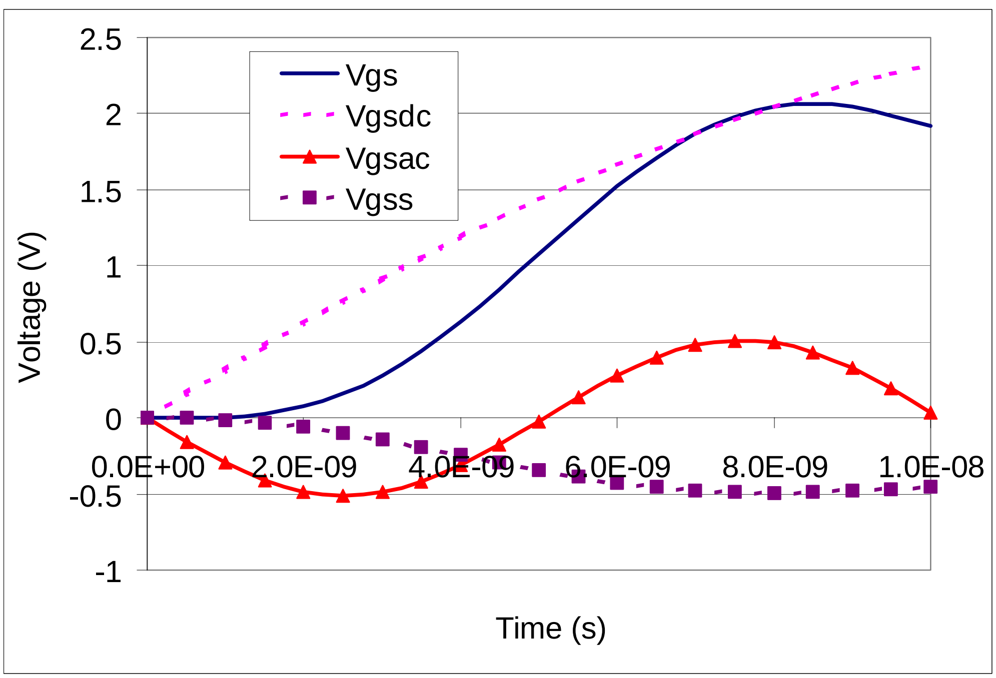


Fig. 3.44 An example of the analytical results.

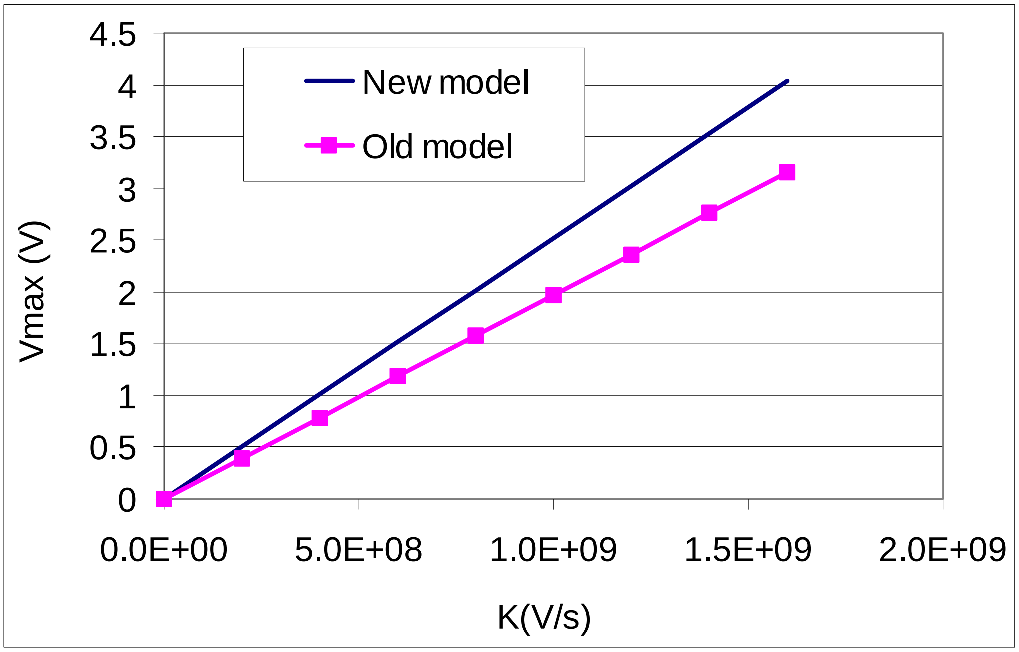


Fig. 3.45 Comparison of V_{max} between the new and old models.

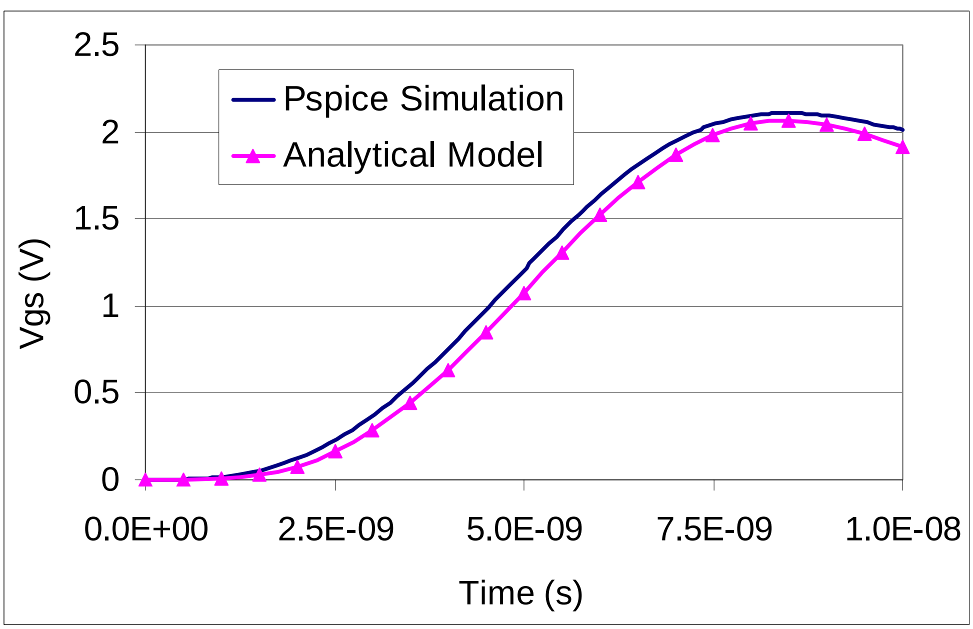


Fig. 3.46 Comparison between analytical and simulation results.

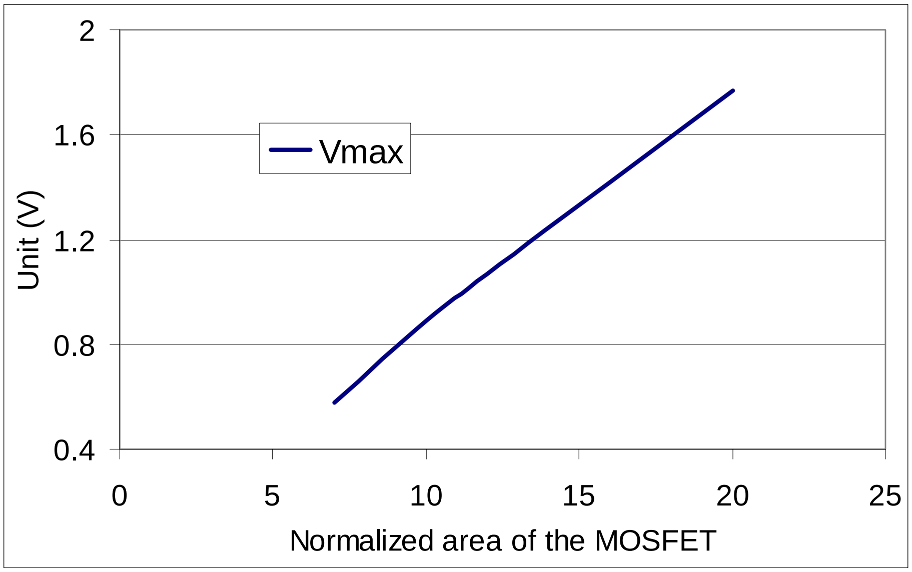


Fig. 3.47 Effect of the active area on the spurious turn-on voltage.

Chapter 4 FEA Analysis of the Power Loss of the Buck Converter

As addressed in the preceding chapter, the switching process of the buck converter is inherently a nonlinear and high-order problem. In order to allow closed-form calculations, we have to make several assumptions, which may lead to the considerable factors being ignored. Actually, besides the switching loss of the high-side MOSFET, the spurious turn-on and the body diode losses [B5]-[B10] are also very difficult to calculate using the traditional approach. Although the circuit simulation can include all the parasitic, but the accuracy is still limited by the analytical models [B27]-[B30].

FEA is a method of subdividing the problem into finite (smaller) elements. Using these elements, the complex partial differential Equations that describe the behavior of a physical structure can be reduced to a set of linear Equations that can easily be solved by the standard techniques of matrix algebra.

The FEA is not a new method. In the late 1940s, the aerospace engineers began using FEA as a structural analysis technique in aerospace design. From that time, thanks to the dramatic increases in computer speed, the method has continually developed into a very sophisticated generic tool, and is used in virtually every engineering discipline.

Although FEA has been widely used in the simulation of semiconductor devices, its application in the DC/DC converter has not been explored due to the long simulation time and the convergence problem. In this chapter, some approaches are proposed to reduce the simulation time and overcome the non-convergence. Then, based on the FEA simulation results, a detailed loss breakdown is performed. For the first time, the false-trigger-on loss is extracted quantitatively. At the end of this chapter, the effects of both the device performance and the parasitic elements on the power loss is studied extensively.

4.1 Construction of the Buck Converter Using FEA

This section addresses the following issues.

- how to build a buck converter using the FEA model
- how to reduce the simulation time
- how to make the simulation converge.

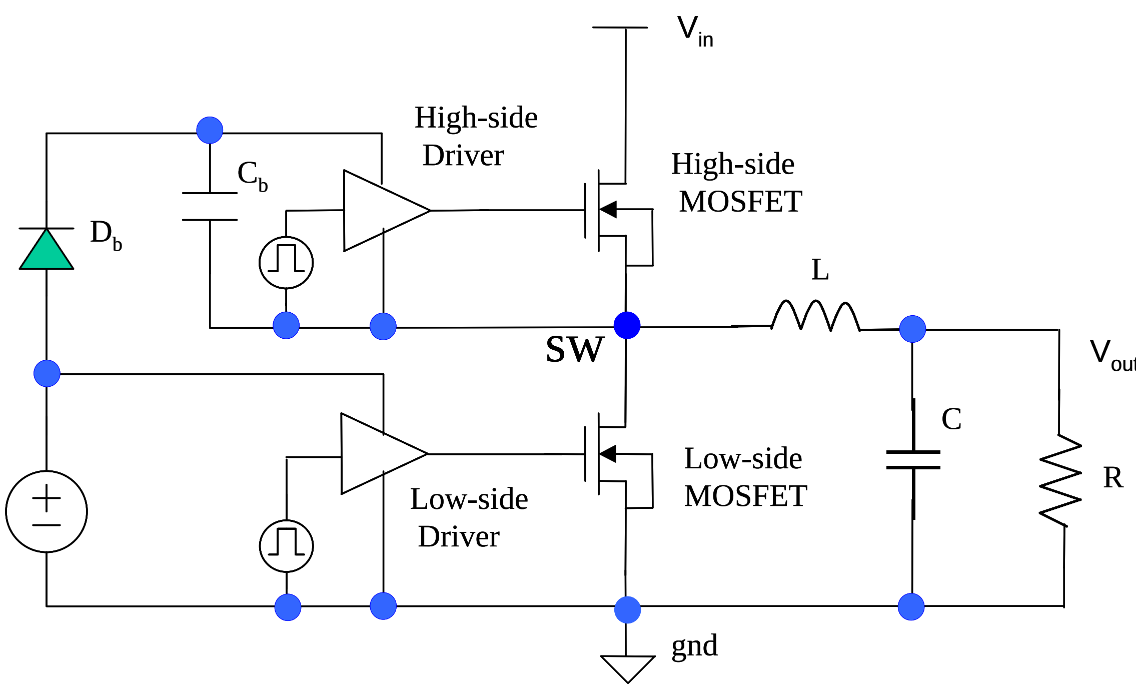


Fig. 4.1 General circuit of the buck converter.

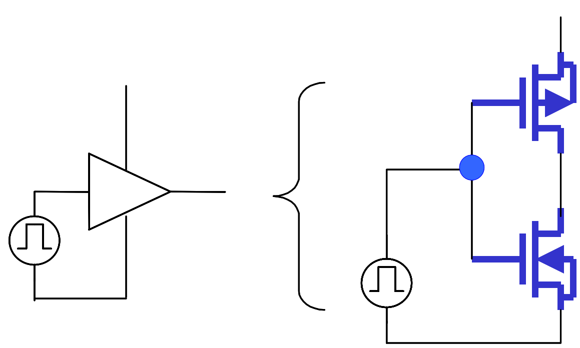


Fig. 4.2 Equivalent circuit of the driver in the buck converter.

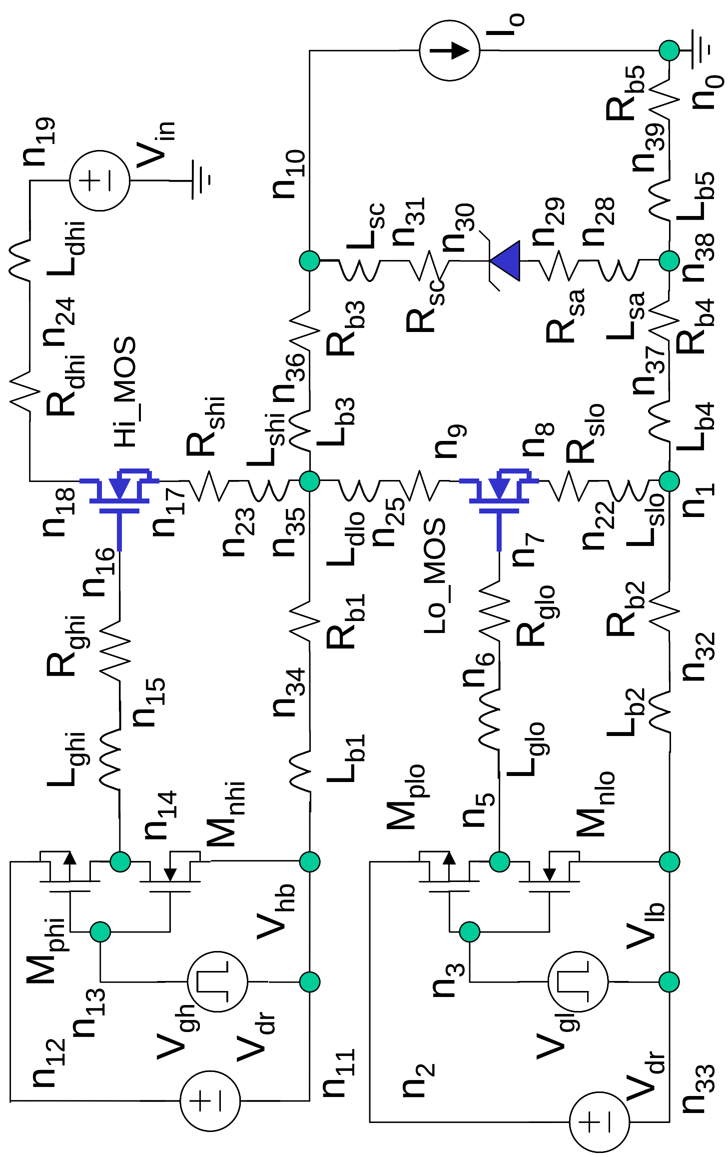


Fig. 4.3 Circuit used in the mixed-mode simulation.

4.1.1 Equivalent Circuit Used in the Simulation

The general circuit of the buck converter is shown in Fig. 4.1. In order to share the same voltage source for the gate driver, C_b and D_b comprise an auxiliary boot-strap circuit to power the high-side driver.

The main components of the buck converter include the power MOSFET, the driver of the power MOSFETs and the low-pass LC filter. Both the driver and the power MOSFETs are semiconductor devices. However, we are going to use the Pspice instead of the FEA model to describe the driver because of the following reasons.

- The switching speed of the CMOS driver is much faster than that of the power MOSFET, and the effect of the driver's switching process on the switching loss of the power MOSFET is insignificant.
- Using the Pspice model can reduce the simulation time, since it is much simpler than FEA.

Because the driver capability is determined by the last stage of the CMOS buffer, the driver can be simplified as a CMOS inverter controlled by a pulse voltage source, as shown in Fig. 4.2. The datasheet of the driver says that the output resistance of the NMOS and PMOS of the inverter has a typical value of from 1 to 2 Ω.

There are two ways to build the FEA model for the power MOSFET, as follows.

- Using the process simulator (Tsuprem4): This method starts from a highly doped silicon substrate, then an epitaxy of the drift layer is formed, and trench etching, gate oxidation, implantation, diffusion and metallization follow to generate a power MOSFET.
- Using the device simulator (Medici): This method directly defines the region of the silicon, oxide and electrode as well as the doping profile of the P-body and the source.

For a general study of the power MOSFET's switching, the second method is preferred, because the process simulation is time consuming. However, for a specific design of the MOSFET, the first method is necessary to determine the process parameters.

In principle, the simulation can be performed with mixed modeling, i.e., Pspice models are used for the driver, and FEA models are used for the power MOSFET. Similar to the process used for Pspice simulation, it is necessary to initialize both the voltage of each node and the current of each circuit branch. However, when the FEA models connect with a non-zero current inductor, the circuit usually does not converge at the beginning of the simulation. If the current set through the inductor is zero, then it takes a lot of switching cycles for the circuit to reach the steady state and the simulation time is too long. In order to eliminate the transient process and guarantee that the simulation is convergent, the inductor must be replaced by a current source. At the beginning of the simulation, both the voltage at any node and the current through the current source are zero. Then, the voltages of the voltage source and the current through the current source ramp up to the desired values in a short time (2 ns). For example, the input voltage ramps up to 20 V, the driver voltage ramps up to 5 V, and the current ramps up to 18 A. After this transient process, it is necessary to wait through another period (1 μs) for the circuit to reach the steady state. After the circuit settles down, both the high-side and low-side MOSFETs are off, and the current flows through the body diode of the low-side MOSFET. If a Schottky diode is paralleled with the low-side MOSFET, most of the current will go through the Schottky diode. Fig. 4.3 shows the equivalent circuit of the buck converter used in the mixed-mode simulation. There are two points that should be noted, as follows.

- The two parts of the boot-strap circuit (C_b and D_b) are replaced by a constant voltage source (V_{hi}) and a pulse voltage source (V_{dhi}).
- The output capacitor is removed. Since a current source is used, the output capacitor plays no role in the circuit. The output voltage of the buck converter is determined using the principle of inductor volt-second balance, such that

$$V_o = \int_0^T V_{10} dt \tag{4.1}$$

where V_{10} is the voltage of the node 10. The typical simulated waveforms of V_{dslo} (V_{ds} of the low-side MOSFET) and V_{gslo} (V_{gs} of the low-side MOSFET) are shown in Fig. 4.4.

4.1.2 Estimation of the Parasitic Inductance

In this section, the values of the parasitic inductance are estimated, based on the calculation and simulation. There two kinds of parasitic inductance to be considered in the simulation, as follows.

- The inductance of a single wire. This exists due to the bonding wired used in the package.
- The inductance of a rectangular metal. This exits due to the metal trace of the PCB.

The self inductance of a single wire can be calculated using

$$L_{wr} = \frac{\mu_0 l}{2\pi}[\ln(\frac{4l}{d}) - 1], \tag{4.2}$$

where $\mu_0 = 4\pi\times10^{-9}$ H/cm is the permeability of the free space, l is the length of the wire, and d is the diameter of the wire. As shown in Fig. 4.5, the self inductance of a single wire for the SO8 package is between approximately 0.2 nH and 2.5 nH, depending on the length and radius of the wire.

For the inductance of a rectangular metal, when the length (l) and width (w) are much larger than the thickness (t), the self inductance is

$$L_{rct} = \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{w}) + \frac{1}{2}]. \tag{4.3}$$

Depending on the length and width of the rectangle, the typical value of the inductance is between approximately 0.3 nH and 10 nH as shown in Fig. 4.6.

The assumption of Equation (4.3) is that the thickness of the rectangular metal is much less than its length and width. This is true for the case of the PCB, because the typical thickness of the PCB is between 33 μm and 132 μm.

Since the separations of the parasitic inductors are usually rather wide, the mutual inductances between the inductors are ignored in the simulation of the buck converter.

The parasitic inductance can also be determined using commercial software such as Maxwell. Fig. 4.7 shows the simulated inductance of the metal strip. Fig. 4.6 and Fig. 4.7 show sufficient agreement.

4.2 Using FEA to Extract Spurious Turn-on Loss

As discussed in Chapter 3, when the high-side MOSFET is turning on, the drain of the low-side MOSFET experiences high dv/dt, which may trigger the low-side MOSFET to turn on, thus causing more power loss. In this section, the process for extracting the spurious turn-on loss is proposed, based on the mixed-mode simulation.

When the drain voltage of the low-side MOSFET is rising, besides the possible spurious turn-on current, there are two other currents flowing the low-side MOSFET, as follows.

- The reverse-recovery current of the body diode,
- The displacement current that exists due to the charging of the output capacitance (C_{oss}).

During the increase in drain voltage of the low-side MOSFET, the loss on the low-side MOSFET can be expressed as

$$E_{vr} = \int P_{vr}\,dt = \int I_{dlo} \times V_{dslo}\,dt = \int (I_{sponlo} + I_c + I_{qrr})V_{dslo}\,dt\ , \qquad (4.4)$$

where I_{sponlo}, I_c and I_{qrr} represent the current caused by spurious turn-on, C_{oss} and the reverse recovery of the body diode, respectively. The three components are separated in three steps, as follows.

(1) When spurious turn-on occurs, there will be electron current (I_{eslo}) flowing through the channel and out of the source of the MOSFET. Fig. 4.8 and Fig. 4.9 compare the total current and the electron current of the source with and without spurious turn-on, respectively. In Fig. 4.8, the electron current is only a small part of the total source current after the low-side MOSFET recovers from reverse conduction. However, in Fig. 4.9, the electron current is a dominant factor. Therefore, the power loss that occurs in the low-side MOSFET due to spurious turn-on is

$$E_{sponlo} = \int I_{sponlo} V_{dslo}\,dt = \int I_{eslo} V_{dslo}\,dt\ . \qquad (4.5)$$

Actually, I_{sponlo} also leads to more loss on the high-side MOSFET. This type of loss (E_{sponhi}) is a part of the turn-on loss of the high-side MOSFET, such that

$$E_{sponhi} = \int I_{sponlo} V_{dshi}\, dt = \int I_{eslo} V_{dshi}\, dt\ , \qquad (4.6)$$

where V_{dshi} is the voltage between the drain and the source of the Hi-MOSFET.

(2) Because the energy stored in a capacitor depends on the voltage and is unrelated to the charging process, the loss caused by C_{oss} (E_{coss}) can be found in another simulation by slowly charging C_{oss} to avoid spurious turn-on and reverse recovery, until the drain voltage reaches V_{in}. I_{coss} also results in more loss in E_{ton}. This part of the loss can be expressed as

$$E_{\cos shi} = Q_{oss} \times V_{in} - E_{\cos s}\ , \qquad (4.7)$$

where Q_{oss} is the charge of C_{oss} at the voltage of V_{in}.

(3) Finally, the loss due to the reverse recovery can be determined by

$$E_{qrr} = \int I_{qrr} V_{dslo}\, dt = E_{vr} - E_{sponlo} - E_{\cos s}\ . \qquad (4.8)$$

The total reverse-recovery charge is

$$Q_{rr} = \int (I_{dlo} - I_{eslo})\, dt - Q_{oss}\ , \qquad (4.9)$$

and the loss on the high-side MOSFET due to Q_{rr} is

$$E_{Qrrhi} = Q_{rr} \times V_{in} - E_{qrr}\ .$$

(4.10)

Usually, when finding the Q_{rr} in actual measurements, no distinction is made between Q_{rr} and Q_{oss}. This will lead to significant error of Q_{rr} when it is much smaller than Q_{oss}.

The key step in the separation of the three kinds of loss is that FEA can monitor the electron current through the source. This is an important feature of the modeling.

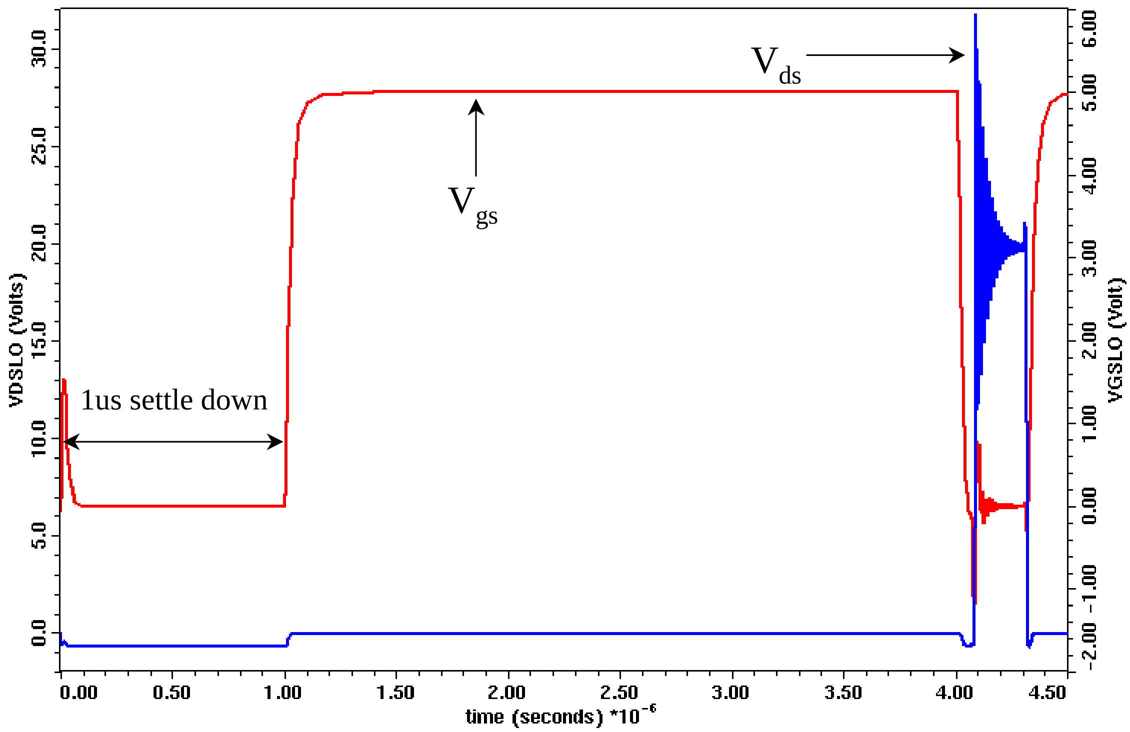


Fig. 4.4 Simulated V_{ds} and V_{gs} of the low-side MOSFET.

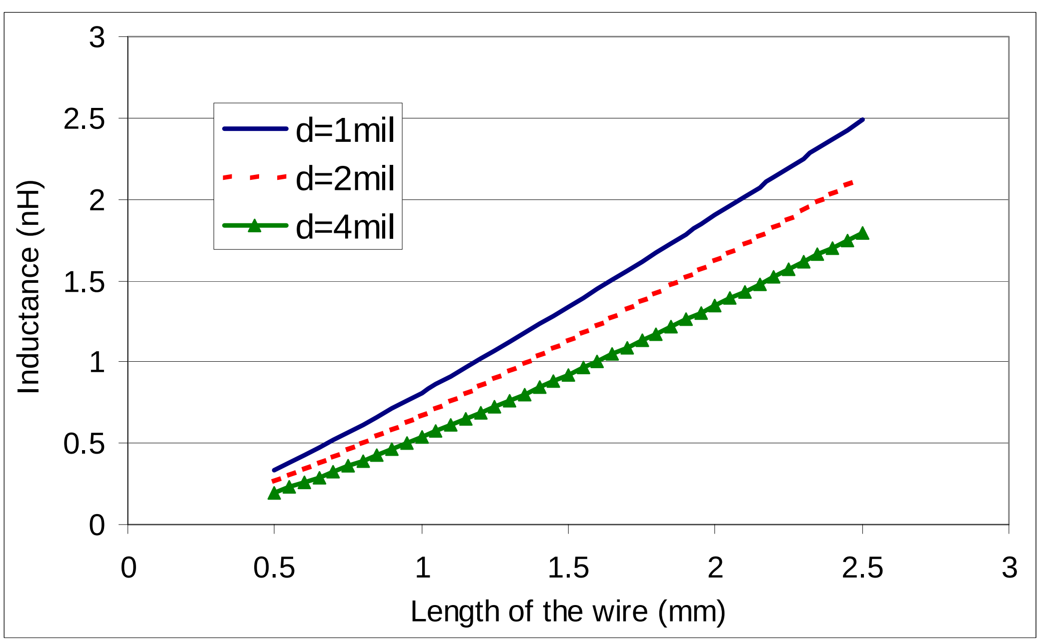


Fig. 4.5 Calculated inductance of a single wire.

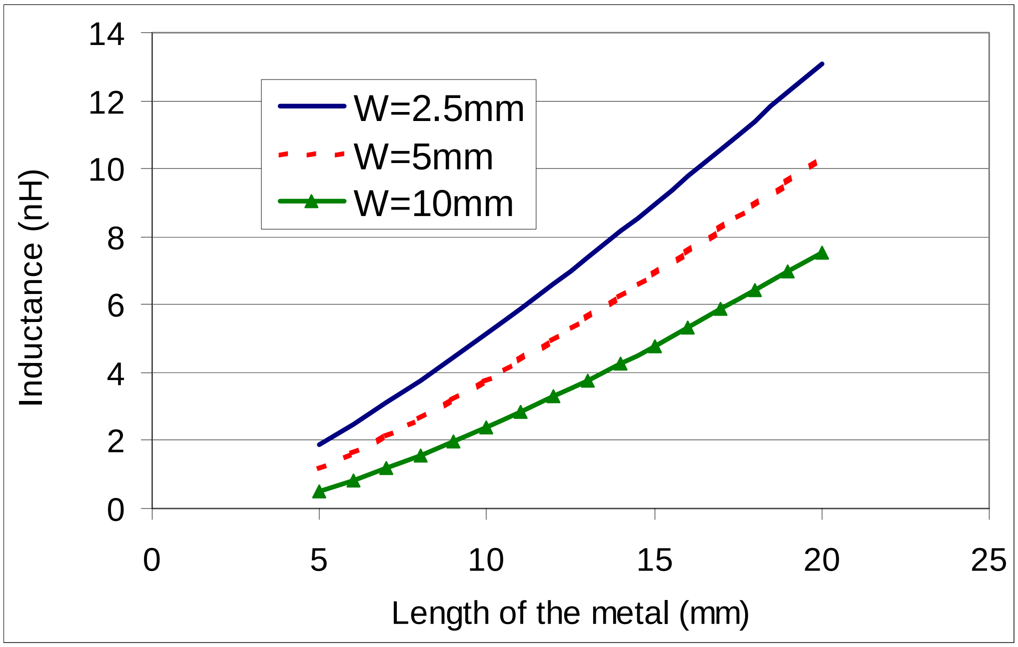


Fig. 4.6 Calculated inductance of the metal strip.

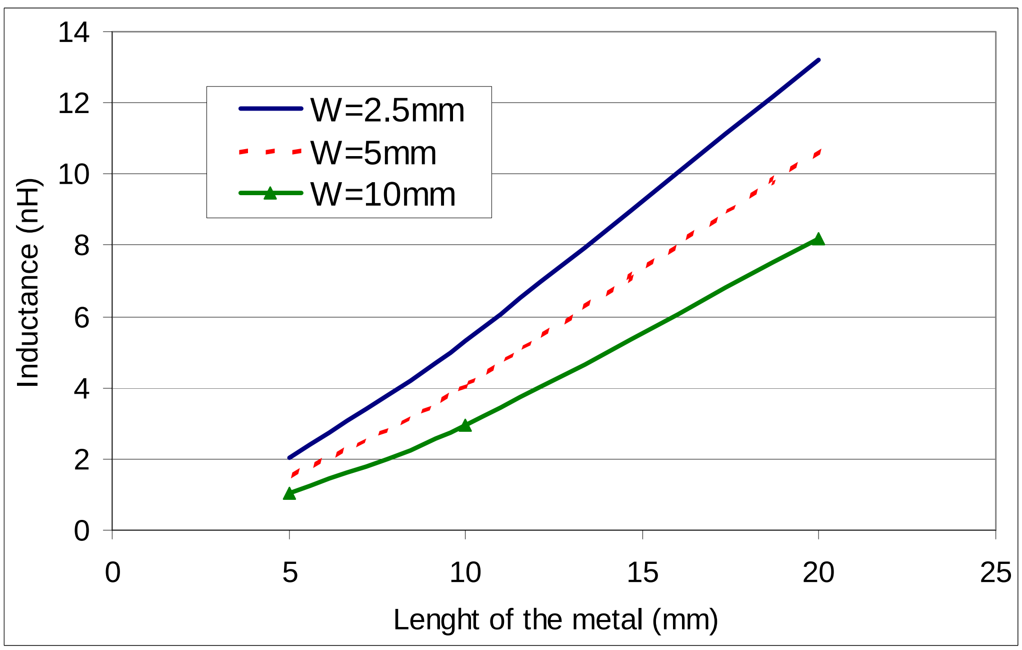


Fig. 4.7 Simulated inductance of the metal strip.

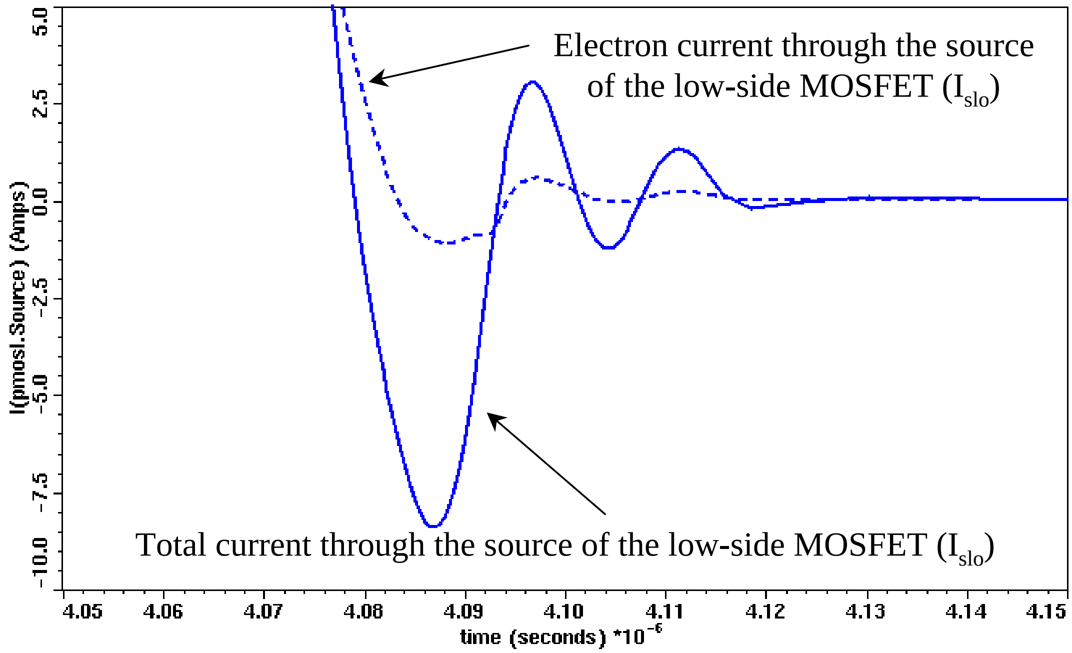


Fig. 4.8 Current through the source of the low-side MOSFET without spurious turn-on.

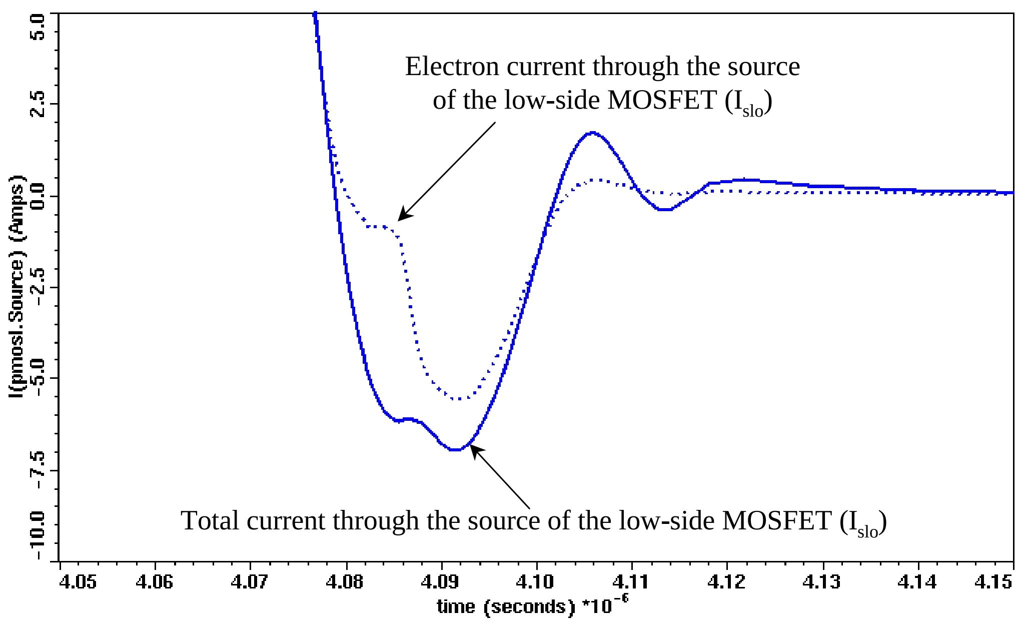


Fig. 4.9 Current through the source of the low-side MOSFET with spurious turn-on.

4.3 Automated Analysis of Power Loss

So far, the power losses in the buck converter can be divided into four parts.

- The loss on the high-side MOSFET includes: turn-on loss, conduction loss, turn-off loss, gate loss and package loss.
- The loss on the low-side MOSFET includes: conduction loss, deadtime loss, spurious turn-on loss, Q_{rr} loss Q_{oss} loss, gate loss and package loss.
- The loss on the Schottky diode includes: conduction loss and package loss.
- The equivalent series resistance (ESR) loss of the inductor and the capacitor.

Although the mixed-mode simulation can be finished in less than half an hour, the calculation of all these losses is not a trivial job. Therefore, a C program is built to automatically perform the loss breakdown. This section defines of each kinds of loss and describes how to use this program.

4.3.1 Critical Timings in the Simulation

In the automated power loss extraction program, the time boundary of conduction loss, switching loss, deadtime loss etc. have to be defined mathematically, because, for example, there is no abrupt switch between the turn-on loss and conduction loss of the high-side MOSFET.

Before the simulation, the user must set some time parameters in the input simulation file of Medici. The definitions of these time parameters are as follows.

- Period: The switching period of the buck converter.
- Ldelay: At Ldelay, the voltage source V_{gl} starts to drop and the low-side MOSFET starts to turn on gradually. As explained in section 4.1.1, Ldelay is needed to settle down the circuit. In the simulation file, T_{glben} is usually selected as 1 μs.
- Hon: During Hon, the pulse voltage V_{hb} keeps the voltage level at zero.

- Deadtime1 and Deadtime2. There are two deadtimes in one switching cycle. In this dissertation, deadtime1 (the first deadtime) represents the deadtime after the low-side MOSFET turns off and before the high-side MOSFET turn-on; deadtime2 (the second deadtime) represents the deadtime after the high-side MOSFET turn-off and before the low-side MOSFET turn-on.

Besides these basic timing parameters, the power loss extraction program uses the simulation results to determine other timing variables. The definitions of these timing variables are listed as follows.

- L_{on}: The time period when the pulse voltage source V_{gl} keeps the voltage level low.

$$Lon = Period - Deadtime1 - Deadtime2 - Hon \tag{4.11}$$

- T_{bgn}: At T_{bgn}, V_{gslo} (V_{gs} of the low-side MOSFET) rises up to 98% of V_{dr}. T_{bgn} is defined as the beginning of the conduction of the low-side MOSFET.
- T_{glend}: At T_{glend}, the voltage source V_{gl} starts to drop, and the low-side MOSFET starts to turn off gradually, such that

$$T_{glend} = Ldelay + Lon \tag{4.12}$$

- $T_{cndlend}$: At $T_{cndlend}$, V_{gslo} drops below 98% of V_{dr}. $T_{cndlend}$ is defined as the end of the conduction of the low-side MOSFET.
- T_{dd1end}: At T_{dd1end}, I_{dl} (drain current of the low-side MOSFET) changes from negative to positive. T_{dd1end} is defined as the end of the first deadtime. The beginning of the first deadtime is the end of the conduction of the low-side MOSFET ($T_{cndlend}$).
- T_{ghbgn}: At T_{ghbgn}, the voltage source V_{gh} starts to drop, and the high-side MOSFET starts to turn on gradually.
- $T_{sponbgn}$: At $T_{sponbgn}$, the electron current through the source of the low-side MOSFET changes from positive to negative. $T_{sponbgn}$ is used to determine the possible spurious turn-on loss.
- $T_{cndhbgn}$: At $T_{cndhbgn}$, the instantaneous drain-to-source power loss of the high-side MOSFET

$$P_{dshi} = V_{dshi} \times I_{dhi} \tag{4.13}$$

drops from the peak to the first valley. Tcndhbgn is defined as the end of the turn-on period and the beginning of the conduction period of the high-side MOSFET.

- T_{ghend}: At T_{ghend}, the voltage source V_{gh} starts to rise, and the high-side MOSFET starts to turn off gradually, such that

$$T_{ghend} = V_{ghbgn} + Hon \tag{4.14}$$

- $T_{cndhend}$: At $T_{cndhend}$, V_{gshi} (V_{gs} of the high-side MOSFET) drops below 98% of V_{dr}.. $T_{cndhend}$ is defined as the end of the conduction period and the beginning of the turn-off period of the high-side MOSFET.
- T_{dd2bgn}: At T_{dd2bgn}, the instantaneous drain-to-source power loss of the low-side MOSFET

$$P_{dslo} = V_{dslo} \times I_{dlo} \tag{4.15}$$

reaches the minimum value. T_{dd2bgn} is defined as the beginning of the second deadtime.

- T_{end}: T_{end} is defined as

$$T_{end} = T_{bgn} + Period \tag{4.16}$$

T_{end} is the end of both deadtime2 and the power loss calculation.

4.3.2 Expressions of the Power loss

This section presents the strict definitions of various power losses in the buck converter based on the timings described in the preceding section.

1) Power loss of the low-side MOSFET

- Conduction loss of the low-side MOSFET

$$P_{cndlo} = \frac{1}{Period} \int_{Tbgn}^{Tcndlend} V_{dslo} \times I_{dlo} dt \tag{4.17}$$

- The first deadtime loss of the low-side MOSFET

$$P_{dd1} = \frac{1}{Period} \int_{Tcndlend}^{Tdd1end} V_{dslo} \times I_{dlo} dt \tag{4.18}$$

- Power loss associated with the turn-on of the high-side MOSFET

$$P_{vr} = \frac{1}{Period} \int_{Tdd1end}^{Tghend} V_{dslo} \times I_{dlo} dt \tag{4.19}$$

- Spurious turn-on loss

$$P_{sponl} = \frac{1}{Period} \int_{Tsponbgn}^{Ttghend} V_{eslo} \times I_{dlo} dt \tag{4.20}$$

- Power loss associated with the turn-off of the high-side MOSFET

$$P_{vf} = \frac{1}{Period} \int_{Tghend}^{Tdd2bgn} V_{dslo} \times I_{dlo} dt \tag{4.21}$$

- The second deadtime loss of the low-side MOSFET

$$P_{dd2} = \frac{1}{Period} \int_{T_{dd2bgn}}^{Tdd2end} V_{dslo} \times I_{dlo} dt \tag{4.22}$$

- Gate loss of the low-side MOSFET

$$P_{glo} = \frac{V_{dr}}{Period} \int_{Ldelay}^{Tglend} I_{glo} dt\ , \tag{4.23}$$

  where I_{glo} is the gate current of the low-side MOSFET.

Package loss of the low-side MOSFET

$$P_{pklo} = \frac{1}{Period} \int_{Tbgn}^{Tend} (I_{dl}^2 \times R_{dlo} + I_{sl}^2 \times R_{slo}) dt \tag{4.24}$$

2) Power loss of the high-side MOSFET

- Turn-on loss of the high-side MOSFET

$$P_{tonhi} = \frac{1}{Period} \int_{Tglend}^{Tcndhbgn} V_{dshi} \times I_{dhi} dt \tag{4.25}$$

- Conduction loss of the high-side MOSFET

$$P_{cndhi} = \frac{1}{Period} \int_{Tcndhbgn}^{Tcndhend} V_{dshi} \times I_{dhi} dt \tag{4.26}$$

- Turn-off loss of the high-side MOSFET

$$P_{tofhi} = \frac{1}{Period} \int_{Tcndhend}^{Tend} V_{dshi} \times I_{dhi} dt \tag{4.27}$$

- Gate loss of the high-side MOSFET

$$P_{ghi} = \frac{V_{dr}}{Period} \int_{Ldelay}^{Tglend} I_{ghi} dt \tag{4.28}$$

- Package loss of the high-side MOSFET

$$P_{pkhi} = \frac{1}{Period} \int_{Tbgn}^{Tend} (I_{dhi}^2 \times R_{dhi} + I_{shi}^2 \times R_{shi}) dt \tag{4.29}$$

3) Power loss on the Schottky diode

The Schottky diode is an optional device in the buck converter. The power loss extraction program can determine whether or not the Schottky diode is used in the simulation, and can automatically calculate the power loss associated with the Schottky diode.

- The first deadtime loss of the Schottky diode

$$P_{stkydd1} = \int_{Tbgn}^{Tghend} I_A \times V_{AK} dt \;, \tag{4.30}$$

  where I_A is the anode current of the Schottky diode and V_{AK} is the voltage between the anode and the cathode of the Schottky diode.

- The second deadtime loss of the Schottky diode

$$P_{stkydd2} = \int_{Tghend}^{Tend} I_A \times V_{AK} dt \tag{4.31}$$

- Package loss of the Schottky diode

$$P_{pkstky} = \frac{1}{Period} \int_{Tbgn}^{Tend} I_A^2 \times (R_{sa} + R_{sc}) dt \tag{4.32}$$

4) ESR loss of the inductor

Although in the simulation, the inductor is replaced by a current source, the ESR loss of the inductor still can be determined by

$$P_{esrl} = \frac{1}{Period} \int_{Tbgn}^{Tend} (I_o^2 \times ESRL) dt\ , \tag{4.33}$$

where Io is the output current and ESRL is the ESR of the inductor.

5) ESR loss of the capacitor

Calculation of the ESR loss of the capacitor is based on the current ripple of the current source, which can be approximated as

$$\Delta I = \frac{V_{in} - V_{out}}{2L} \cdot Hon\ , \tag{4.34}$$

where L is the value of the inductor and Hon is defined in section 4.3.1. Therefore, the power loss on the ESR of the capacitor is

$$P_{esrc} = \frac{1}{Hon} \int_{0}^{Hon} [(\frac{\Delta I}{Hon} t)^2 ESRC] dt = \frac{\Delta I^2 R}{3}\ , \tag{4.35}$$

where ESRC is the ESR of the capacitor.

5) Other resistive losses

The power loss of other parasitic resistors in Fig. 4.3 is determined by

$$P_{res} = \frac{1}{Period} \int_{Tbgn}^{Tend} (I_{res}^2 \times R) dt\ . \tag{4.36}$$

4.3.3 Worked Example of the Program

The application of the power loss extraction program is rather simple. After the circuit simulation, run the program in the same directory, for example

>sbc filename

where sbc is the name of the power loss extraction program and the filename is the input file name for the circuit simulation. The analysis results will be displayed on the screen and also be saved in the file named filename.rst under the current directory.

An example of the analysis result is shown in Fig. 4.10. There are eight sections in the result. The first part shows the input voltage, output current and the output voltage of the buck converter. The second part includes the voltage and current stress on the power MOSFETs. The definitions of some symbols are given as follows

- V_{spon}: the maximum spurious turn-on voltage across the gate and the source of the low-side MOSFET.
- $V_{dsmaxhi}$: the maximum voltage across the drain and the source of the high-side MOSFET.
- $V_{dsmaxlo}$: the maximum voltage across the drain and the source of the low-side MOSFET.
- $V_{gsmaxhi}$: the maximum voltage across the gate and the source of the high-side MOSFET.
- $V_{gsminhi}$: the minimum voltage across the gate and the source of the high-side MOSFET.
- $V_{gsmaxlo}$: the maximum voltage across the gate and the source of the low-side MOSFET.
- $V_{gsminlo}$: the minimum voltage across the gate and the source of the low-side MOSFET.
- I_{dmaxhi}: the maximum current through the drain of the high-side MOSFET.
- I_{dmaxlo}: the maximum current through the drain of the low-side MOSFET.
- I_{dminlo}: the minimum current through the drain of the low-side MOSFET.
- I_{gmaxhi}: the maximum current through the gate of the high-side MOSFET.

- I_{gminhi}: the minimum current through the gate of the high-side MOSFET.
- I_{gmaxlo}: the maximum current through the gate of the low-side MOSFET.
- I_{gminlo}: the minimum current through the gate of the low-side MOSFET.

The third part describes the power loss on the high-side MOSFET. The definitions of the symbols are as follows.

- P_{hi}: total power loss related to the high-side MOSFET.

$$P_{hi} = P_{sihi} + P_{pkhi} \tag{4.37}$$

- P_{sihi}: the sum of the switching loss and conduction loss of the high-side MOSFET

$$P_{sihi} = P_{tonhi} + P_{cndhi} + P_{tofhi} + P_{ghi} \tag{4.38}$$

- P_{swdshi}: the sum of the turn-on and the turn-off loss of the high-side MOSFET

$$P_{swdshi} = P_{tonhi} + P_{tofhi} \tag{4.39}$$

- P_{swhi}: the total switching loss of the high-side MOSFET

$$P_{swhi} = P_{swdshi} + P_{ghi} \tag{4.40}$$

- Q_{ghi}: the total gate charge of the high-side MOSFET during the switching.

$$Q_{ghi} = \int_{Ldelay}^{Tglend} I_{ghi} dt \tag{4.41}$$

The fourth part describes the power loss on the low-side MOSFET. The definitions of some symbols are as follows

- P_{lo}: total power loss related to the low-side MOSFET.

$$P_{lo} = P_{silo} + P_{pklo} \tag{4.42}$$

- P_{silo}: the sum of the switching loss and conduction loss of the low-side MOSFET

$$P_{silo} = P_{swlo} + P_{cndlo} \tag{4.43}$$

- P_{swdslo}: the sum of P_{vr}, P_{dd1}, P_{dd2} and P_{vf}.

$$P_{swdslo} = P_{vri} + P_{dd1} + P_{dd2} + P_{vf} \tag{4.44}$$

- P_{swlo}: the total switching loss of the low-side MOSFET

$$P_{swlo} = P_{swdslo} + P_{glo} \tag{4.45}$$

- Q_{glo}: the total gate charge of the low-side MOSFET during the switching.

$$P_{glo} = \int_{Ldelay}^{Tglend} I_{glo} dt \tag{4.46}$$

The fifth part describes the power loss on the low-side MOSFET. The definitions of some symbols are as follows.

- P_{stkytt}: total power loss related to the Schottky diode.

$$P_{stkytt} = P_{sistky} + P_{pkstky} \tag{4.47}$$

- P_{sistky}: the sum of Pstkydd1 and Pstkydd2.

$$P_{sistky} = P_{stkydd1} + P_{stkydd2} \tag{4.48}$$

The sixth part describes miscellaneous losses of the buck converter. The definitions of some symbols are as follows.

- P_{pcb}: the total loss associated with the parasitic resistance on the PCB.

$$P_{pcb} = \frac{1}{Period}\left[\int_{Tbgn}^{Tend} (I_{b3}^2 \times R_{bs} + I_{b4}^2 \times R_{b4} + I_{b5}^2 \times R_{b5}) dt\right] \tag{4.49}$$

- P_{sitt}: is the sum of Psihi, Psilo and Psistky.
- P_{other}: is the power loss that cannot be determined by the circuit simulation, for example, the magnetic loss of the inductor. The value of Pother is set in the input file. The power loss extraction program reads Pother and uses it in the efficiency calculation.
- P_{tt}: is the total power loss.

$$P_{tt} = P_{hi} + P_{lo} + P_{stkytt} + P_{esrl} + P_{esrc} + P_{pcb} + P_{other} \tag{4.50}$$

The seventh part describes the power loss associated with the spurious turn-on, C_{oss} and Q_{rr}, as addressed in section 4.2.

The eighth part shows the efficiency. The efficiency without gate loss is defined as

$$\eta_{ng} = \frac{I_{out} \cdot V_{out}}{I_{out} \cdot V_{out} + (P_{tt} - P_{ghi} - P_{glo})} . \tag{4.51}$$

The efficiency with the gate loss is defined as

$$\eta_{g} = \frac{I_{out} \cdot V_{out}}{I_{out} \cdot V_{out} + P_{tt}} . \tag{4.52}$$

```
Text Editor - std_dt0.01_stk.rst
File  Edit  Format  Options                                    Help
***********************Begin of output*******************************************
Vin = 20.00 (V)      Iout = 20.00 (A)      Vout = 1.3  (V)
***********************Voltage and current stress*****************************
The Vspon = 2.31   V (Vg=1.39  V,Vs=-0.92  V) at time=4.063039e-06
Vdsmaxhi = 26.29 V (Vd=21.87 V, Vs=-4.42  V) at time=4.305600e-06
Vdsmaxlo = 23.63 V (Vd=21.98 V, Vs=-1.64  V) at time=4.068330e-06
Vgsmaxhi = 6.00  V (Vg=25.78 V, Vs=19.79  V) at time=4.076490e-06
Vgsminhi = -0.40 V (Vg=-0.91 V, Vs=-0.52  V) at time=4.321361e-06
Vgsmaxlo = 5.00  V (Vg=4.99  V, Vs=-0.01  V) at time=2.175116e-06
Vgsminlo = -1.09 V (Vg=-1.47 V, Vs=-4.08  V) at time=4.307600e-06
Idmaxhi = 24.85   at time=4.059100e-06
Idmaxlo = 7.72    at time=4.059100e-06
Idminlo = -23.50  at time=4.511687e-06
Igmaxhi = 1.36    at time=4.066290e-06
Igminhi = -2.11   at time=4.301600e-06
Igmaxlo =  1.39    at time=4.306200e-06
Igminlo = -1.26   at time=3.970897e-06
************** Loss on the high side MOSFET ************************************
Phi = 2.049  (W) Psihi = 2.036  (W)  Ppkhi = 0.013  (W)
Ptonhi =1.132 (W)  Pcndhi =0.325 (W)  Ptofhi =0.551 (W)  Pghi = 0.028  (W)
Pswdshi =1.682 (W)  Pswhi =1.710 (W)  Qghi =18.607(nC)
**************** Loss on the low side MOSFET **********************************
Plo = 1.629 (W) Psilo = 1.477  (W)  Ppklo = 0.151  (W)
Pcndlo = 0.684 (W)  Pdd1 = 0.090 (W) Pvr = 0.346 (W)
Pvf = -0.092(W) Pdd2 = 0.316 (W)  Pglo = 0.134  (W)
Pswdslo =0.660 (W)  Pswlo =0.794 (W)  Qglo =89.361(nC)
**************** Loss on the  Schottky diode **********************************
Pstkytt = 0.122 (W) Psistky = 0.121  (W)  Ppkstky = 0.001  (W)
Pstkydd1 = 0.021 (W)  Pstkydd2 = 0.099 (W)
************************** Other losses ****************************************
Pesrl = 1.021  (W)  Pesrc = 0.064  (W) Ppcb = 0.236  (W)
Psitt = 3.634  (W)  Ptt = 5.621  (W)  Pother = 0.500  (W)
************************** Shoot-through analysis ****************************
Pvr = 0.346  (W)  Psponl = 0.161  (W)  Posslo = 0.104  (W)  Pqrrlo = 0.081  (W)
Psponhi = 0.022  (W)  Posshi = 0.170  (W)  Pqrrhi = 0.053  (W)
Pflsontt = 0.022  (W)  Posstt = 0.274  (W)  Pqrrtt = 0.134  (W)
Qtotal = 9.553e-08 Qoss = 4.570e-08  Qflson = 2.743e-08 Qrr = 2.239e-08
**********************Efficiency@Vout = 1.3  V*****************************
Efficiency without gate loss = 82.646%
Efficiency with gate loss = 82.223%
**********************End of analysis****************************
```

Fig. 4.10 An example of the power analysis result.

4.4 Application of the FEA Simulator

In this section, the FEA simulator is used to study the effects of the power MOSFET design parameters and the parasitic inductance. The conclusions are compared with the analytical models presented in Chapter 3.

4.4.1 Effect of the Design Parameters of the High-side MOSFET on Efficiency

The major losses of the high-side MOSFET are those related to switching and conduction. As addressed in Chapter 3, the switching loss is mainly determined by Q_{gd}, and the conduction loss by R_{ds}. The effect of numerous design parameters on Q_{gd}, R_{ds} and the efficiency are studied. In addition, the Figure of Merit (FOM = $Q_{sw} \times R_{ds}$) [B25] is also investigated for each case in order to determine whether less FOM always results in higher efficiency. In the following discussion, the operation condition of the buck converter is V_{in} = 20V, I_{out} = 20A, and V_{ou}t = 1.3V. 300KHz switching frequencies is used in the simulation.

(1) Trench width (W_t)

The effects of W_t on Q_{sw}, R_{ds} and the FOM are shown in Fig. 4.11. Because W_t introduces C_{gd}, larger W_t results in more Q_{sw}. On the other hand, wider W_t reduces the R_{ds} by enhancing the spread of current under the trench. However, the FOM increases with W_t. Fig. 4.12 shows the simulated efficiency.

Conclusion 4.1: Less W_t leads to higher efficiency, if the device area is chosen properly.

Obviously, the device area plays a very important role in efficiency. If the device area is too small, the conduction loss will be very high; if the device area is too large, the switching loss will be dominant. An optimized value for the area depends on the relative values of the conduction and switching losses. For example, at a higher frequency (1 MHz), the optimized area is less than at a low frequency (300 KHz). The reason is that the switching loss is proportional to the switching frequency; the higher the frequency, the smaller the area needed to reduce the switching loss. The optimized area also decreases with larger W_t. This is also because larger W_t leads to more switching loss.

(2) Mesa width (W_m)

The effects of W_m on Q_{sw}, R_{ds} and the FOM are shown in Fig. 4.13. Interestingly, the FOM decreases with the increase of W_m. The reason is that, for the fixed channel width (W_g in Equation (2.5)), the wider W_m reduces the spreading resistance in the mesa region without introducing much Q_{gd}. In Fig. 4.13, the R_{ds} increases with W_m because of the specific R_{ds} is used in the plot. Fig. 4.14 shows the simulated efficiency for different mesa widths.

Conclusion 4.2: Wider Wm leads to higher efficiency, if the device area is chosen properly.

Although wider W_m results in higher efficiency, it negatively impacts the device area. For example, at 300 KHz, the optimized area is about 10 mm^2 for W_m = 2.5 um, while the optimized area is about 4 mm^2 for W_m = 1.0 um. The efficiency difference is less than 0.5%. Therefore, the selection of W_m is a tradeoff between the cost and the performance.

(3) Thickness of the gate oxide (T_{ox})

The effects of T_{ox} on Q_{sw}, R_{ds} and the FOM are shown in Fig. 4.15. As expected, thicker T_{ox} leads to higher R_{ds} and lower Q_{sw}. The overall effect is that the FOM decreases with the increase of T_{ox}. However, for T_{ox} > 50 nm, the reduction of FOM is trivial. Fig. 4.16 shows the effect of T_{ox} on efficiency.

Conclusion 4.3: Thinner gate oxide leads to higher efficiency.

However, the gate oxide can be too thin, because it needs to support the gate-to-source voltage. Typically, the minimum thickness of the gate oxide for such applications is about 30nm.

(4) The separation between the bottom of the trench and the bottom of the P-body (Ovp).

This parameter determines the C_{gd} of the trench sidewall. Less Ovp means less C_{gd}. However, if Ovp is very small, the current spreading in the mesa region could be weakened dramatically, which would results in huge R_{ds}. Therefore, there is an optimized Ovp in terms of FOM, as shown in Fig. 4.17. The negative Ovp in Fig. 4.17 means that the bottom of the P-body is below the bottom of the gate trench. The effect of Ovp on the efficiency is shown in Fig. 4.18. The optimized value of Ovp is zero. Therefore, we have the next conclusion:

Conclusion 4.4: the optimum design of the p-body depth is as close as possible to the trench depth.

(5) The doping concentration of the drift region (N).

For a given breakdown voltage, the selection of doping concentration of the drift region can span a wide range. As addressed in Chapter 3, the lightly doped N could lead to less Q_{gd}. Fig. 4.19 shows the effects of N on Q_{sw}, R_{ds} and the FOM for BV = 30 V. The lightly doped drift region has less Q_{gd}, however, the increase of R_{ds} is more significant. Therefore, the non-punch-through is a better design in terms of FOM. Fig. 4.20 shows that the non-punch-through design not only has slightly higher efficiency, but also has less device area at the optimized point.

Conclusion 4.5: Non-punch-through design is preferred for the optimized design.

(6) Effect of the breakdown voltage on efficiency.

Currently, most commercial MOSFETs for the application of the 20V input buck converter have a breakdown voltage (BV) of 30V. Fig. 4.21 shows the effect of the BV on efficiency. Actually, the performance of the low-breakdown (BV<30V) MOSFET is not as good as the MOSFET with higher BV. This is because when the high-side MOSFET is turning off, the parasitic inductances (L_{dhi} and L_{shi}) induce a voltage spike, which leads to extra loss on the high-side MOSFET. Fig. 4.22 compares the turn-off losses of high-side MOSFETs with different BV ratings. Apparently, the voltage spike is related to both the value of the parasitic inductance (L_{dhi} and L_{shi}) and the turn-off speed of the high-side MOSFET. However, from 30 V to 35 V, the efficiency difference is less than 0.05%. Therefore, we have the following conclusion.

Conclusion 4.6: For the high-side MOSFET, 30V voltage rating is a good choice for 20V input buck converter.

(7) Effect of the threshold voltage the efficiency.

In the preceding simulations, all the threshold voltages of the high-side MOSFETs are fixed at 1.7 V. However, the V_t influences the power loss in three ways, as follows,

- Lower V_t decreases the turn-on loss by introducing higher effective $V_{gs} = V_{dr} - V_t$, if the associated spurious turn-on loss is trivial.
- But lower V_t also increases the turn-off loss by reducing the effective $V_{gs} = V_t$.
- Lower V_t leads to less on-resistance of the MOSFET.

Actually, there must be an optimum V_t for the high-side MSFET in terms of the power loss, because of these facts.

- if Vt is close to 0, the MOSFET is very difficult to turn off. As a result, the turn-off loss will be very large.
- if V_t is close to V_{dr}, the MOSFET is very difficult to turn on . Consequently, both the turn-on and conduction losses will be very large.

Indeed, the optimum value of V_t can be found by FEA simulation. As shown in Fig. 4.23, the optimum V_t is about 1 V. It should be noted that the optimum value of V_t depends on many conditions, for example, the switching frequency, the input and output voltage, etc.

Conclusion 4.7: There is an optimum V_t of the hgih-side MOSFET

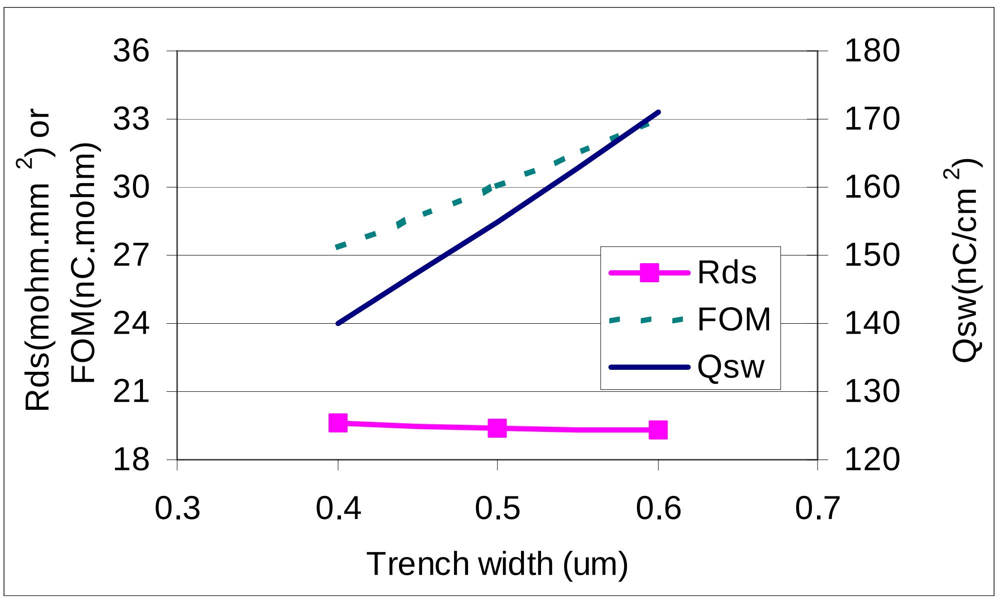


Fig. 4.11 Effects of trench width on the Q_{sw}, R_{ds} and FOM.

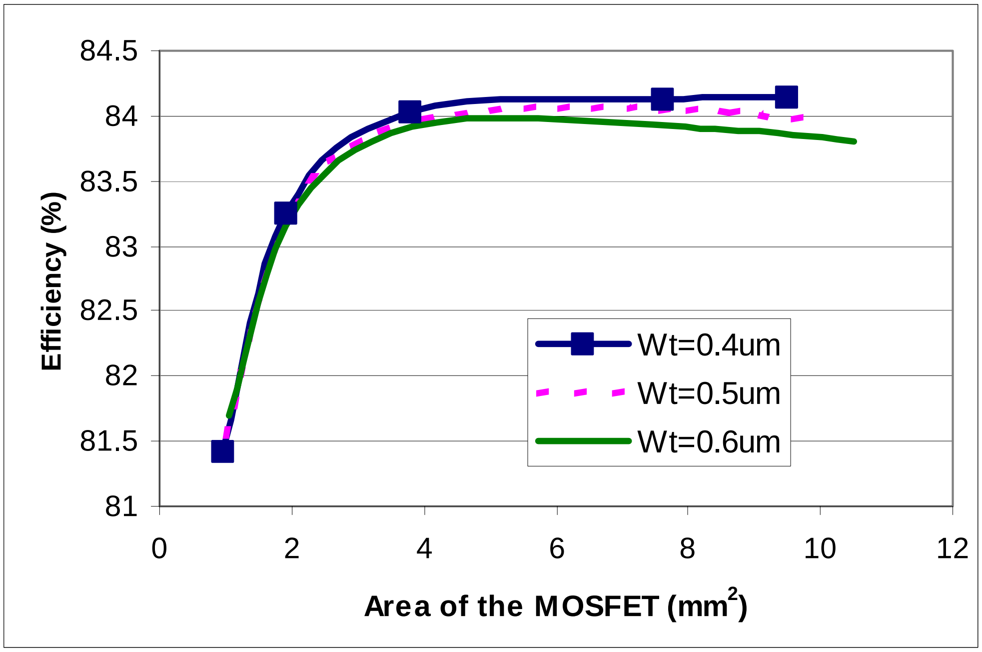


Fig. 4.12 Effect of trench width on efficiency.

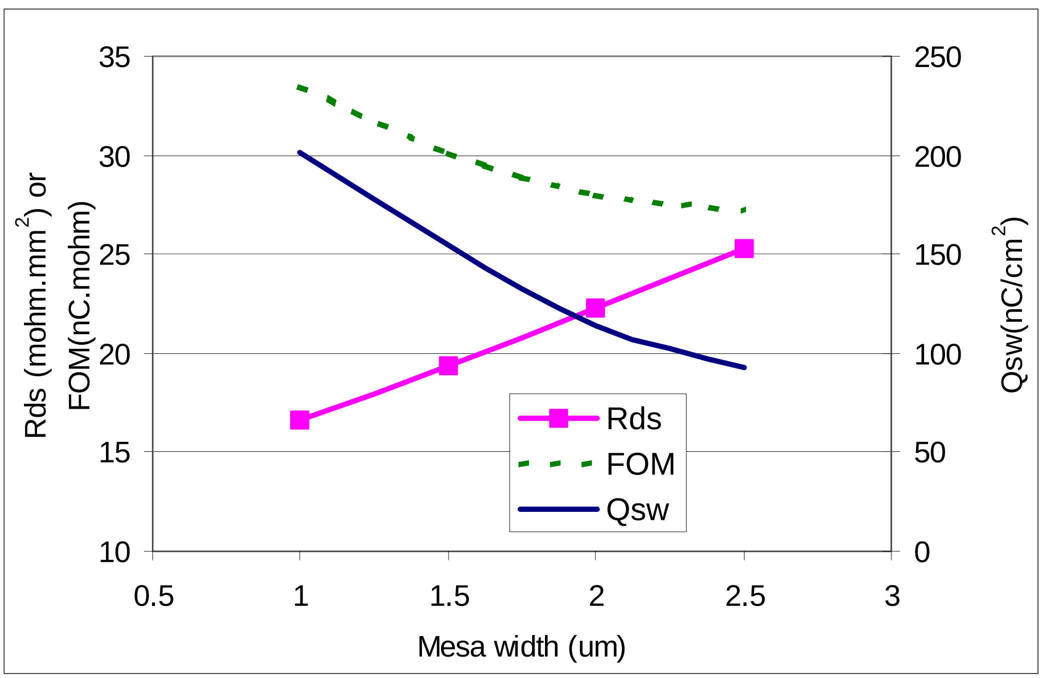


Fig. 4.13 Effects of mesa width on Q_{sw}, R_{ds} and FOM.

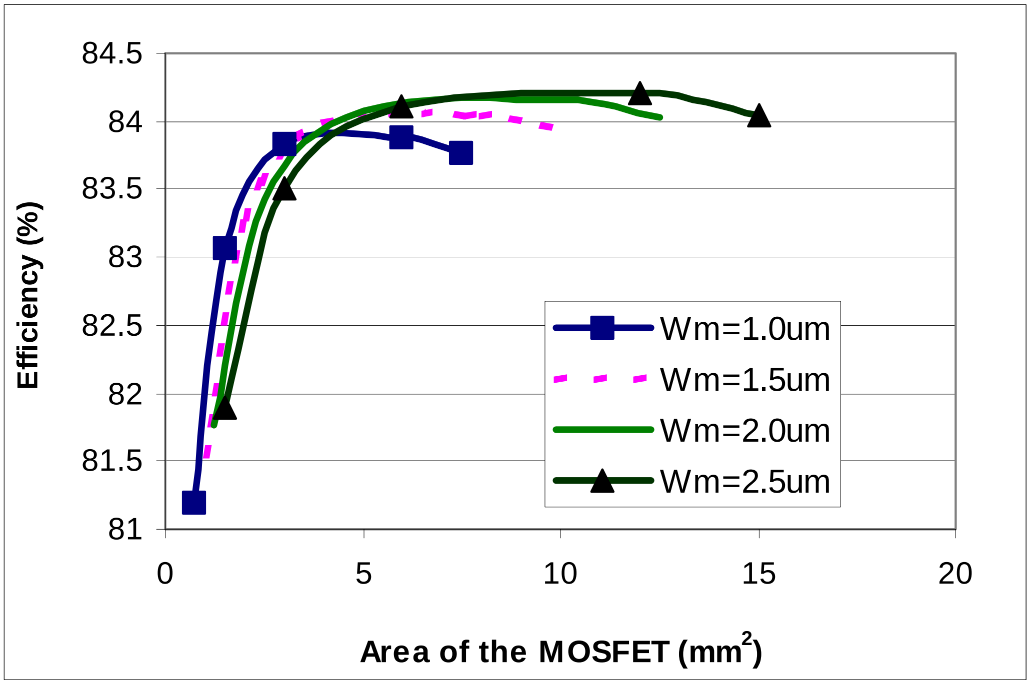


Fig. 4.14 Effect of mesa width on efficiency.

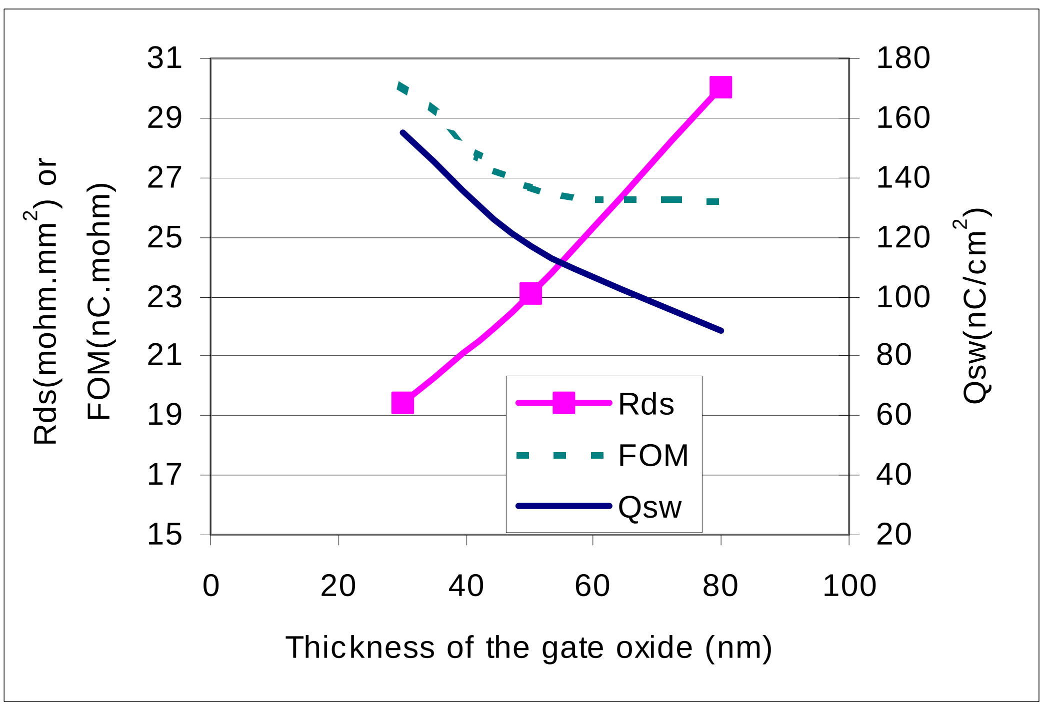


Fig. 4.15 Effects of the gate oxide thickness on Q_{gd}, R_{ds} and FOM.

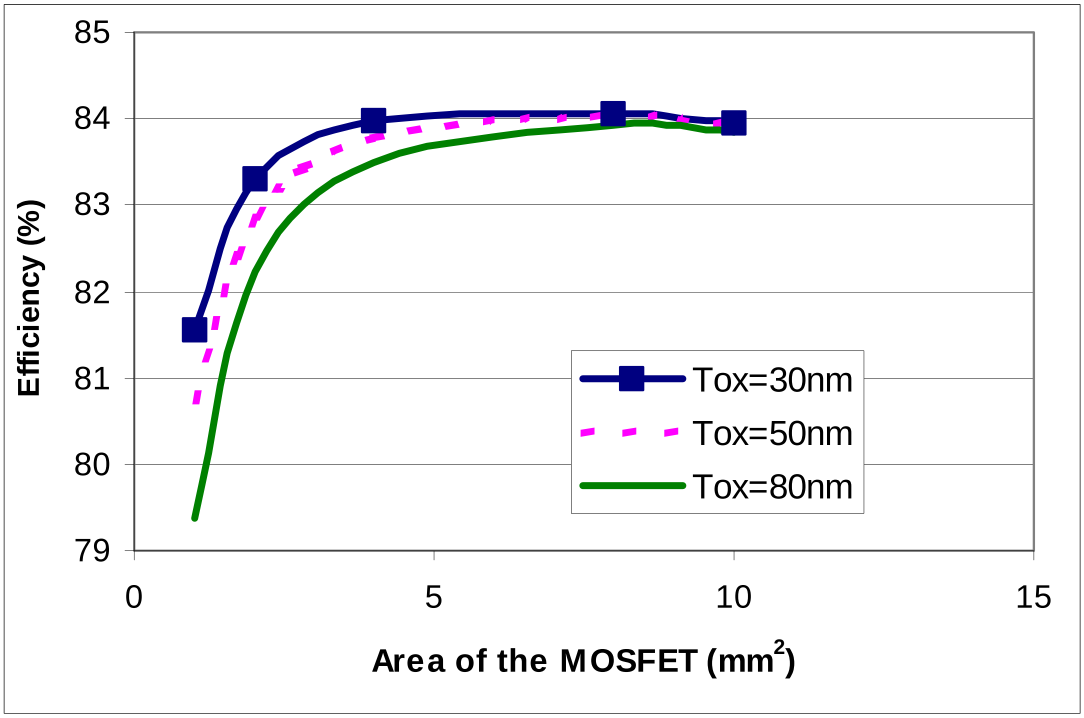


Fig. 4.16 Effect of the gate oxide thickness on efficiency.

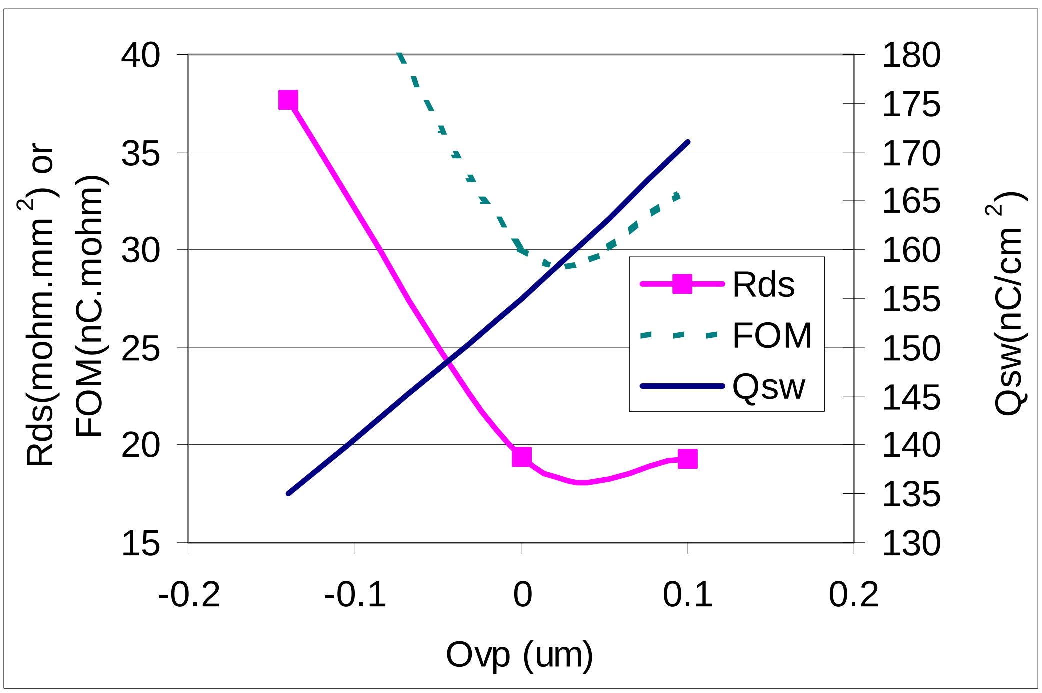


Fig. 4.17 Effects of Ovp on Q_{gd}, R_{ds} and FOM.

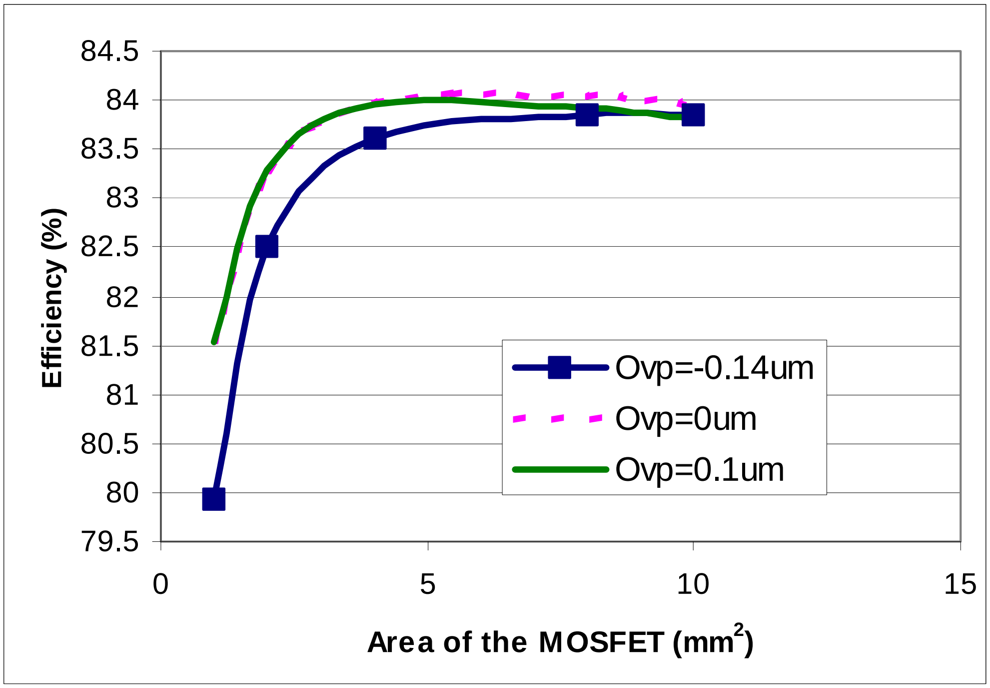


Fig. 4.18 Effect of Ovp on efficiency.

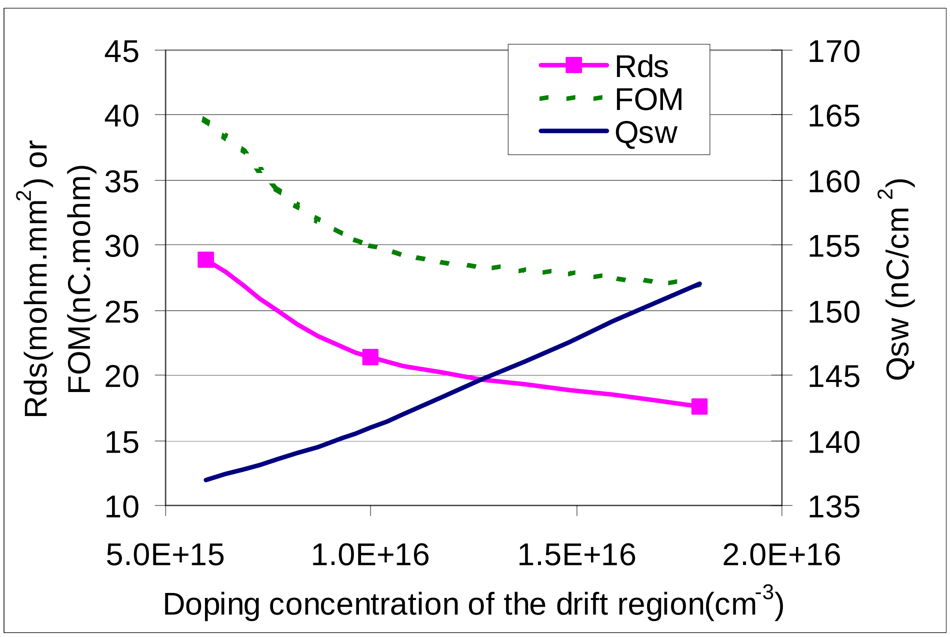


Fig. 4.19 Effects of the doping concentration of the drift region on Q_{gd}, R_{ds} and FOM.

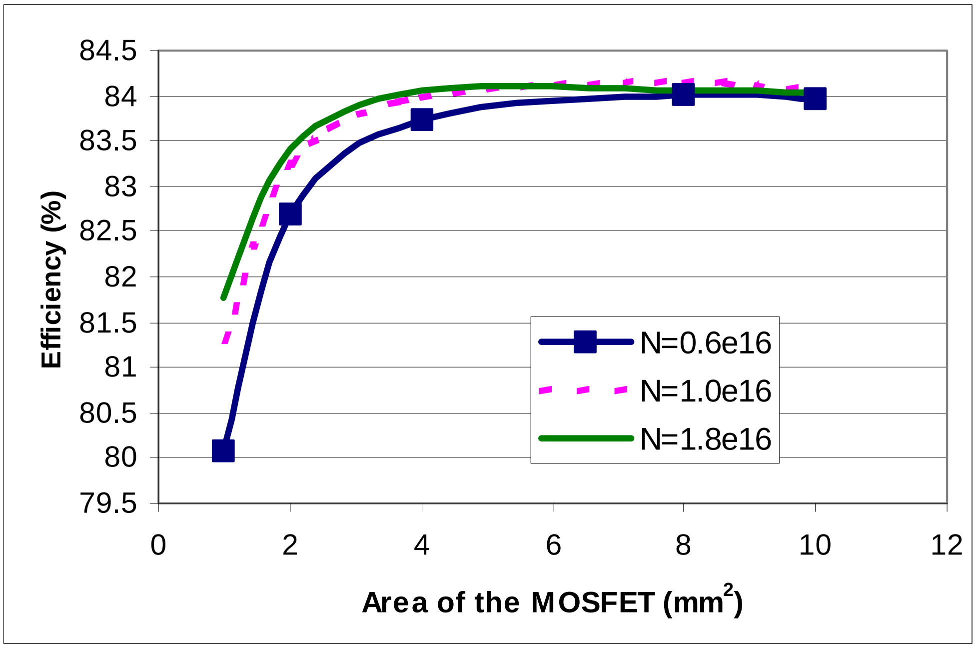


Fig. 4.20 Effect of the doping concentration of the drift region on the efficiency.

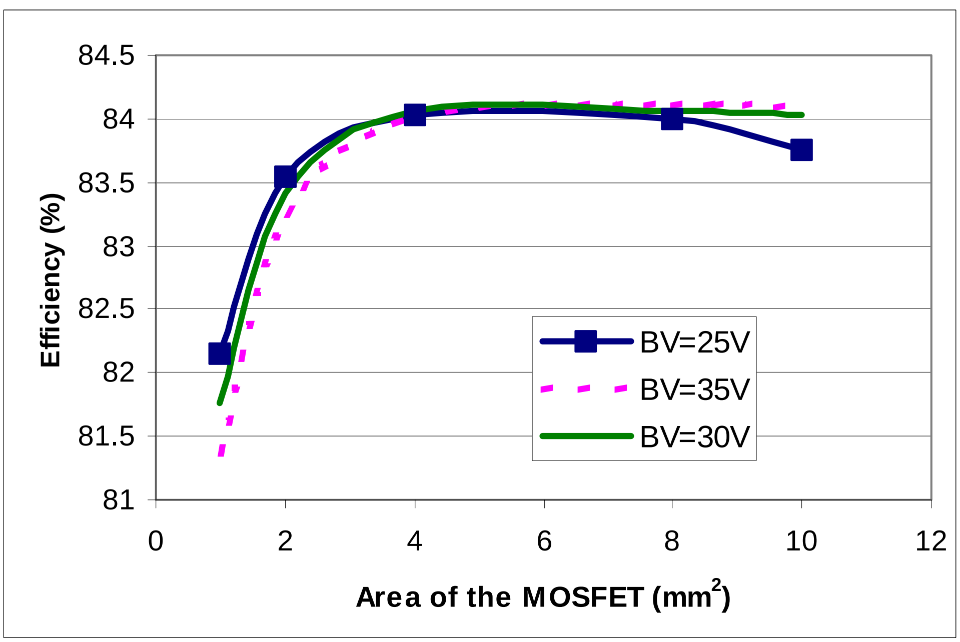


Fig. 4.21 Effect of the breakdown voltage (BV) on efficiency.

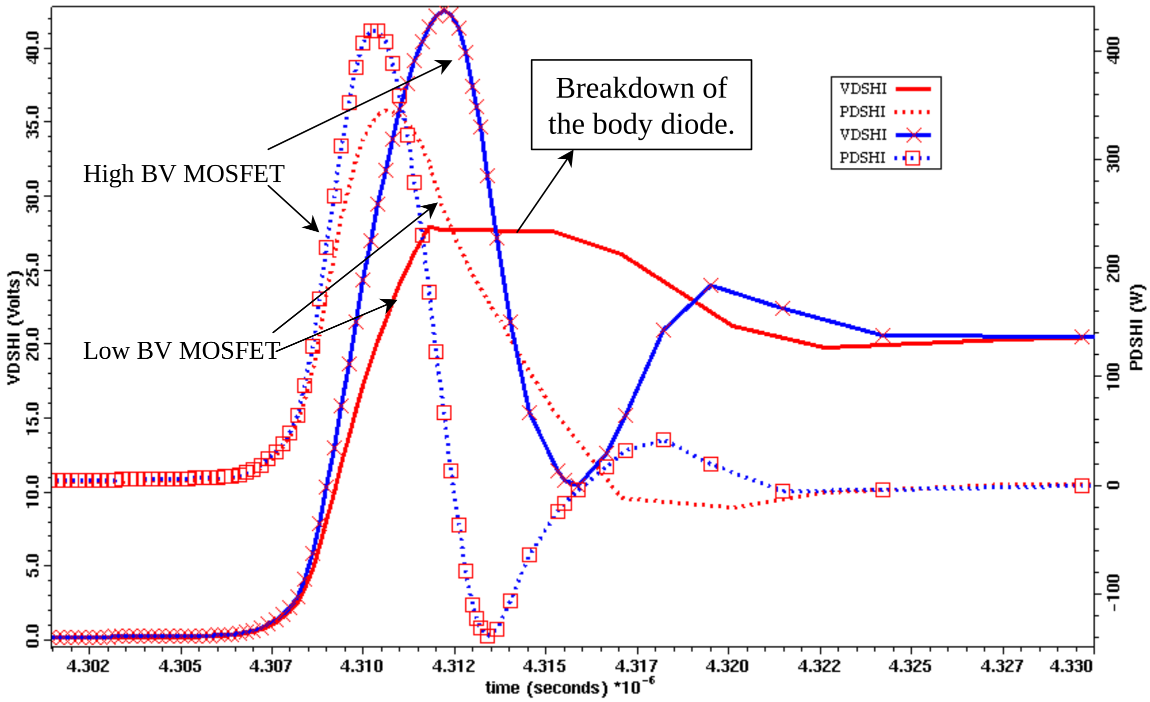


Fig. 4.22 Turn-off waveforms of the high-side MOSFET.

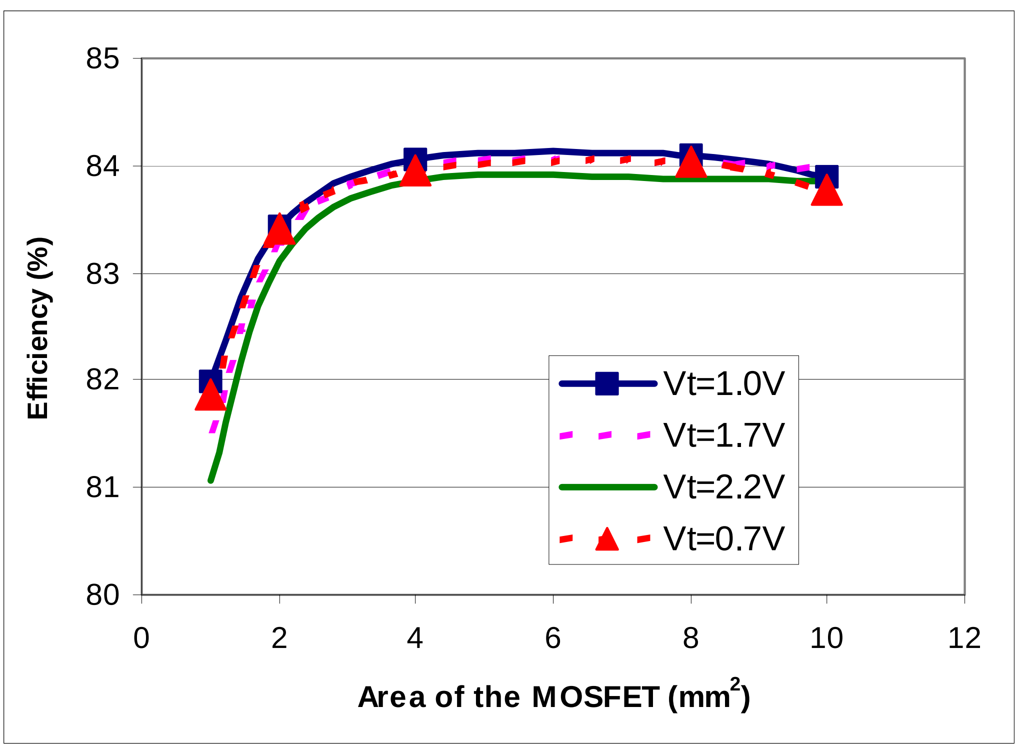


Fig. 4.23 Effect of V_t on efficiency.

4.4.2 Effect of the Design Parameters of the Low-side MOSFET on Efficiency

In this section, the effect of the design parameter of the low-side MOSFET on the efficiency of the buck converter is investigated in the same manner as used in the preceding section. Also, it is important to determine whether or not the FOM is a good index for the low-side MOSFET from the efficiency standpoint

.

(1) Trench width (W_t)

Fig. 4.24 shows the effect of the trench width on efficiency. Although the conduction loss is dominant in the power loss of the low-side MOSFET, if the device area of the low-side MOSFET is too large, the efficiency drops. The reason is that a larger MOSFET has more C_{gd}, and consequently is more prone to the spurious turn-on loss. This also explains the advantage of a narrower trench width, which has less C_{gd}.

Conclusion 4.8: Less W_t leads to higher efficiency, if the device area is chosen properly.

(2) Mesa width (W_m)

Fig. 4.25 shows the effect of the mesa width on efficiency. At 300KHz switching frequency, a wider trench width is preferred from the efficiency standpoint; at 1 MHz, a narrow trench width is better. The less FOM of the wider W_m explains the simulation results obtained at 300KHz. At higher frequencies, the loss of the output capacitance can be substantial. Therefore, a narrow W_m is preferable.

Conclusion 4.9: Although there is an optimum value of Wm, less Wm is preferred in terms of cost.

(3) Thickness of the gate oxide (T_{ox})

Because T_{ox} impacts on-resistance, C_{gd} and C_{oss}, it influences the tradeoff between the conduction loss, spurious turn-on loss and the output capacitance loss. Fig. 4.26 shows that at 300 KHz, thinner Tox is preferred.

Conclusion 4.10: Thinner gate oxide leads to less power loss if the device area is chosen properly.

(4) The separation between the bottom of the trench and the bottom of the P-body (Ovp).

Since a small Ovp can pinch off the current path under the gate trench, and a larger Ovp results in more C_{gd}, there is an optimum Ovp for the low-side MOSFET. Fig. 4.27 shows the effects of Ovp on efficiency.

Conclusion 4.10: At 300 KHz, the optimum Ovp is about 0.

(5) The doping concentration of the drift region (N).

Fig. 4.28 shows that the non-punch-through design is better at 300 KHz.

Conclusion 4.11: The optimum doping concentration of the drift region depends on the switching frequency.

(6) Effect of the BV on efficiency.

The low-side MOSFET experiences high voltage stress when the high-side MOSFET is turning on. Such voltage stress determines the optimum voltage rating of the low-side MOSFET. Fig. 4.29 shows the next conclusion.

Conclusion 4.12: For the low-side MOSFET, 30V voltage rating is a reasonable choice for 20V input buck converter.

(7) Effect of the threshold voltage on the efficiency.

In the preceding simulations, all the threshold voltages of the low-side MOSFETs are fixed at 1.7 V. However, the V_t influences the power loss in the following two ways:

- Lower V_t decreases the on-resistance of the MOSFET.
- Lower V_t results in more spurious turn-on loss.

Actually, there must be a optimum V_t for the low-side MSOFET in terms of the power loss, because of the following evidence.

- if Vt is close to 0, the spurious turn-on loss can be significant.
- if Vt is close Vdr, the conduction loss of the low side MOSFET will be dominant.

As shown in Fig. 4.30, the optimum V_t of the low-side MOSFET is about 2 V. It should be noted that the optimum value of V_t depends on many conditions, for example, the switching frequency, the input and output voltage, etc.

Conclusion 4.13: There is an optimum V_t of the low-side MOSFET.

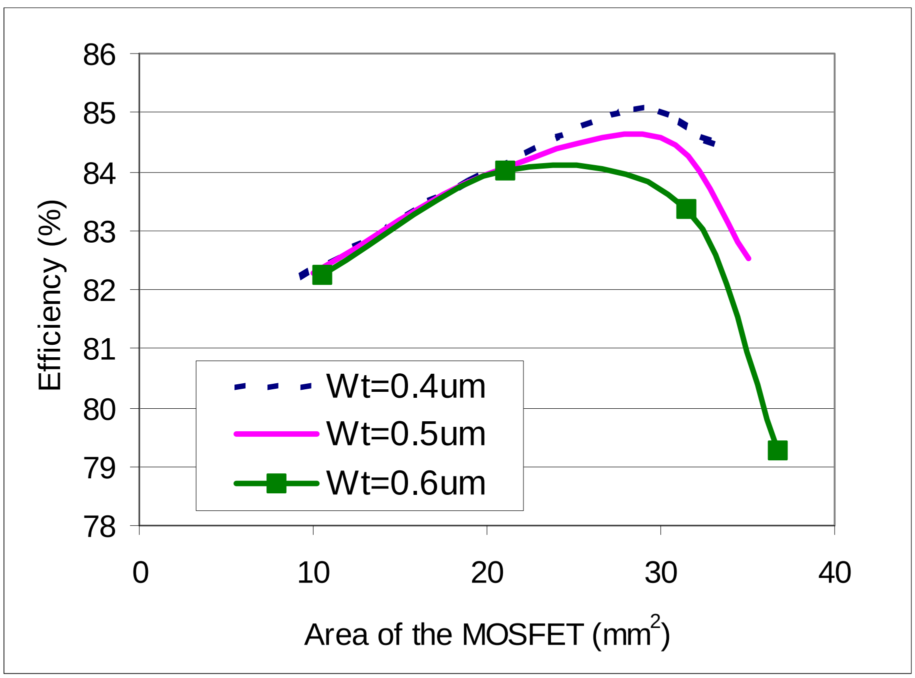


Fig. 4.24 Effect of trench width on efficiency.

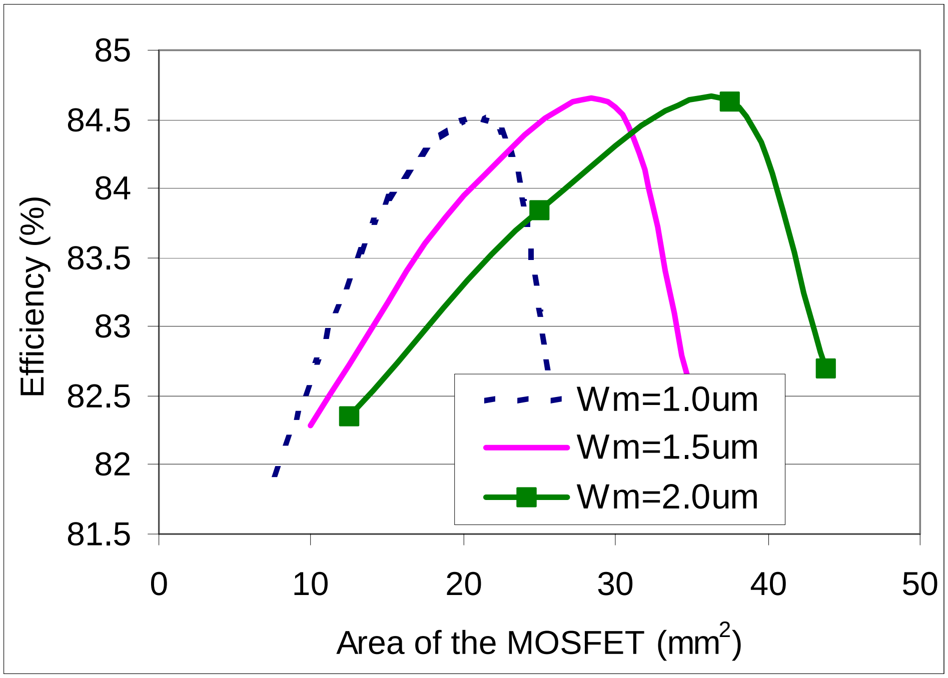


Fig. 4.25 Effect of mesa width on efficiency.

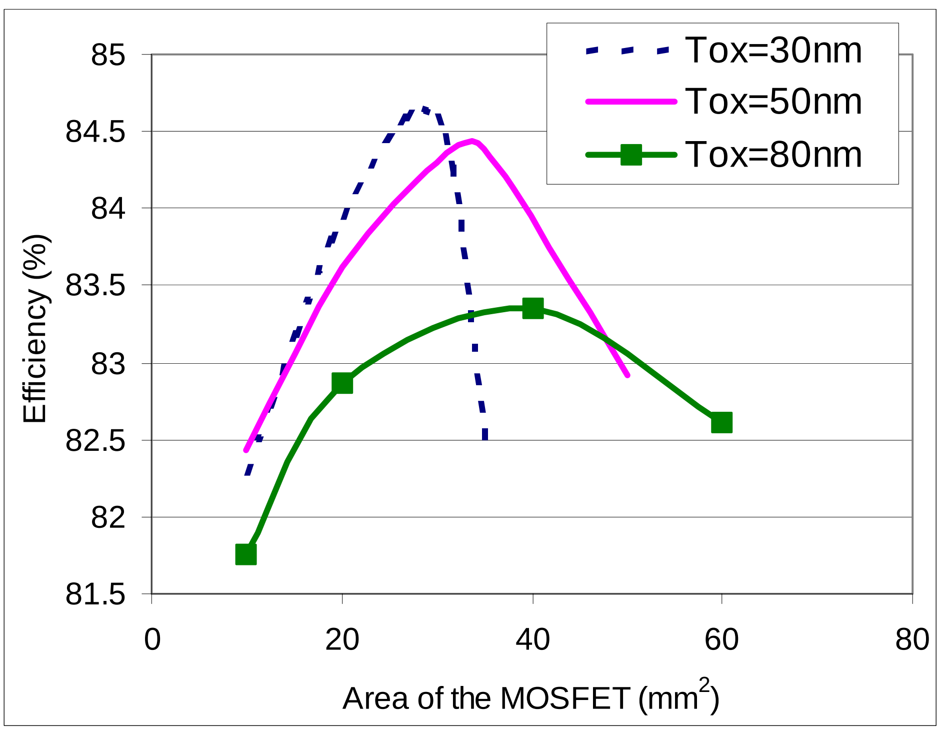


Fig. 4.26 Effect of the gate oxide thickness on efficiency.

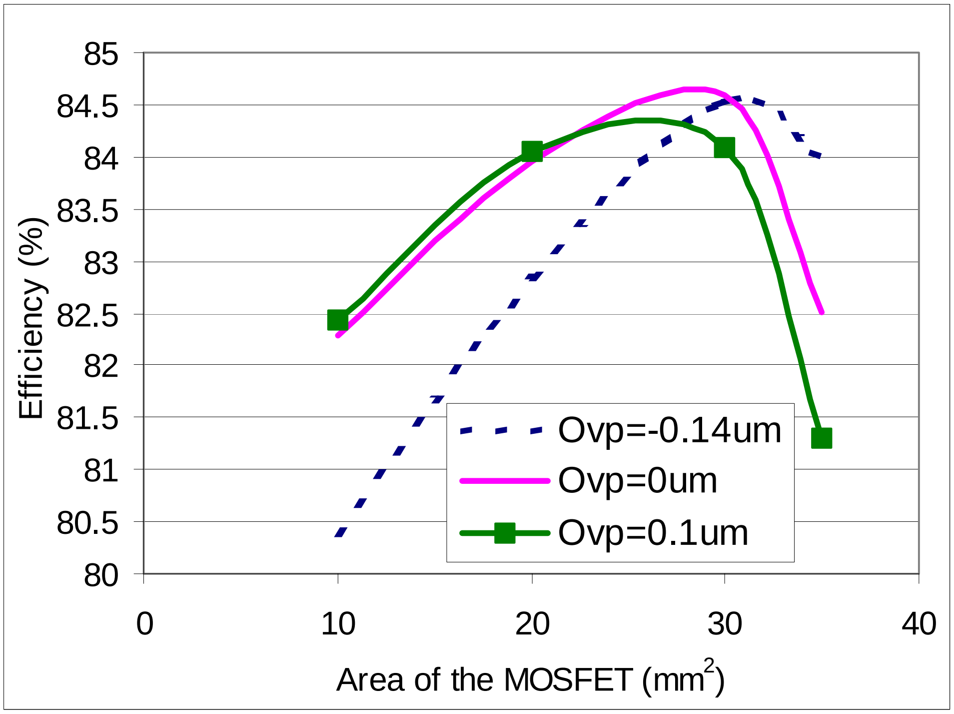


Fig. 4.27 Effect of Ovp on efficiency.

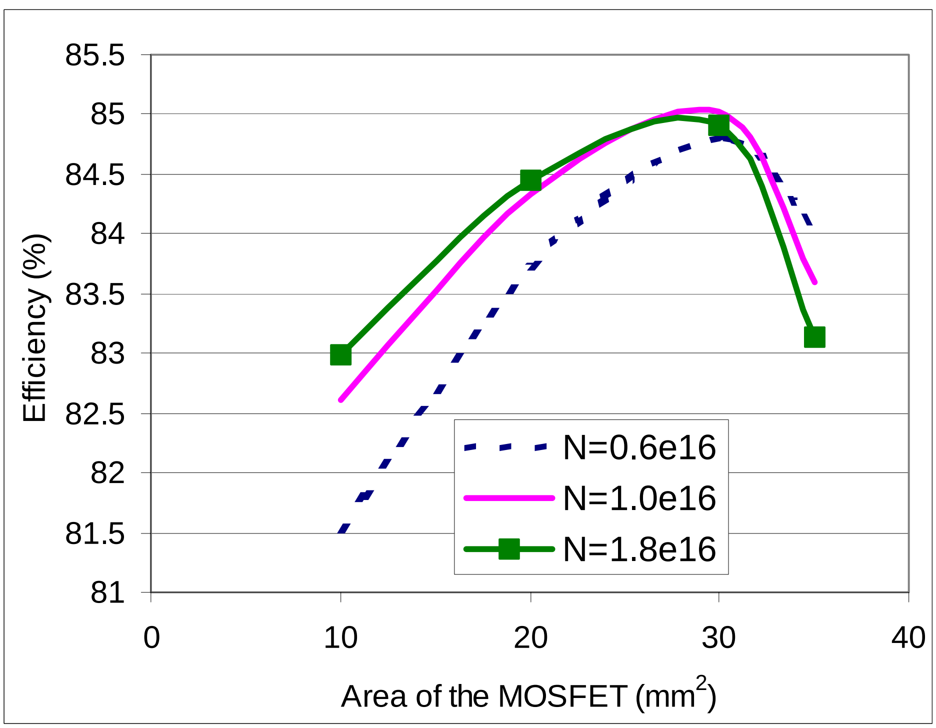


Fig. 4.28 Effect of the doping concentration of the drift region on efficiency.

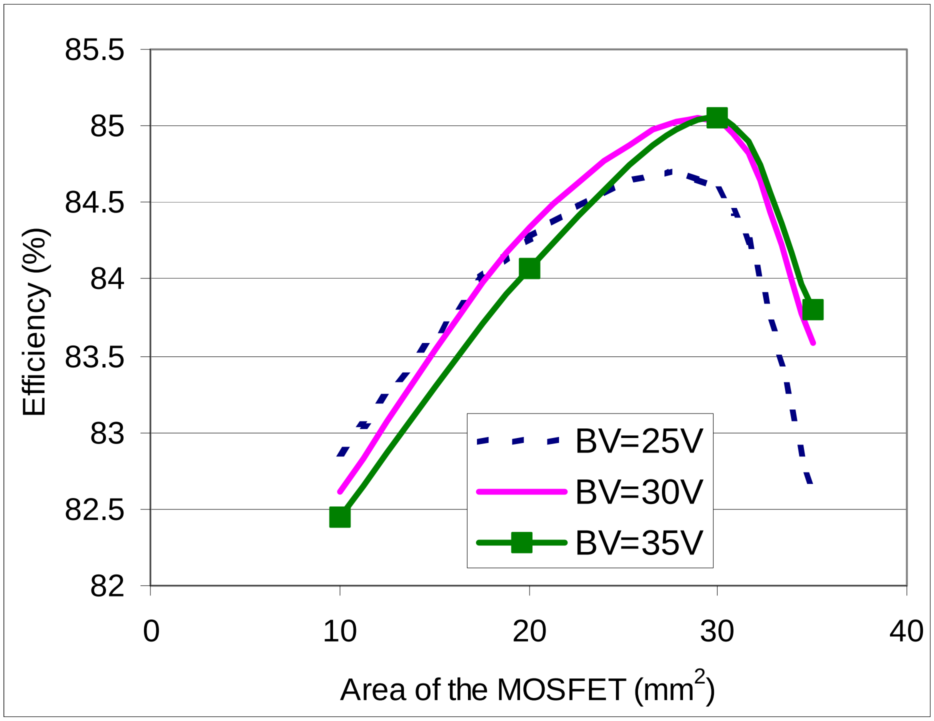


Fig. 4.29 Effect of the breakdown voltage (BV) on efficiency.

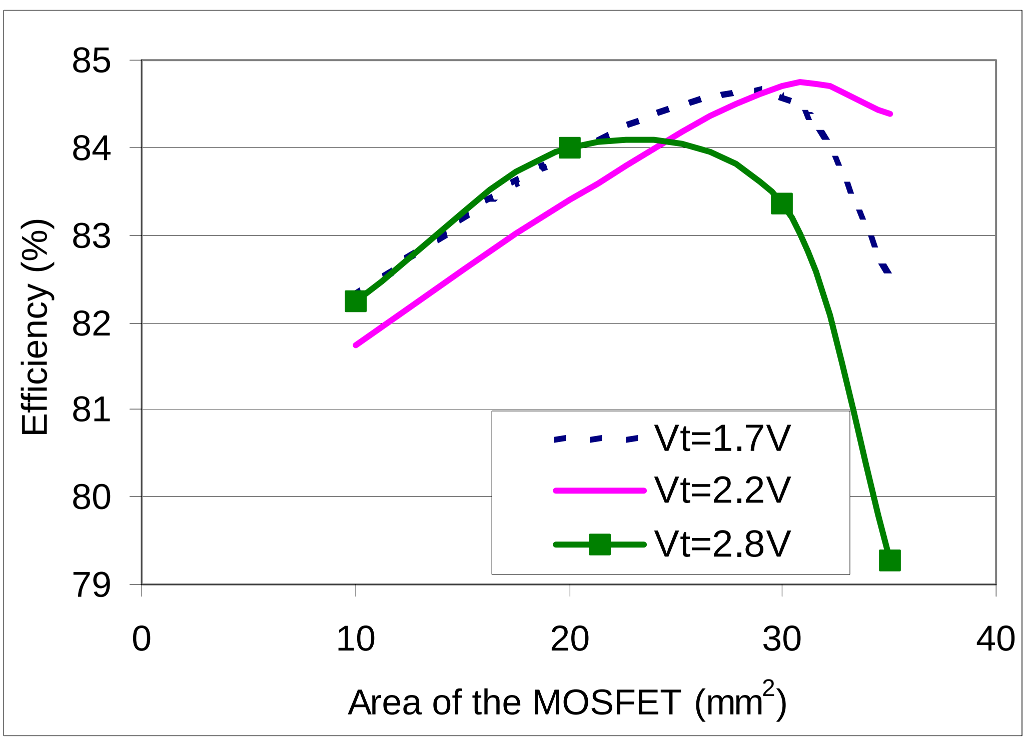


Fig. 4.30 Effect of V_t on efficiency.

4.4.3 Effect of the Parasitic Inductance on Efficiency

The effects of the parasitic inductances L_{dhi} and L_{shi} on the switching loss are addressed in Chapter 3. In this section, such effects are quantified by FEA simulations.

(1) Effect of the L_{dhi} on efficiency.

Fig. 4.31 shows the effect of L_{dhi} on efficiency. In the practical range of L_{dhi}, the variation of the efficiency is very small. Therefore, less L_{dhi} is preferred, because larger L_{dhi} leads to more voltage stress on the MOSFET, as shown in Fig. 4.32.

(2) Effect of the L_{shi} on efficiency.

The impact of L_{shi} on the switching process of the high-side MOSFET is addressed in Chapter 3. Fig. 4.33 quantitatively demonstrated the conclusion that a larger L_{shi} leads to more switching loss and has significant effect on the efficiency.

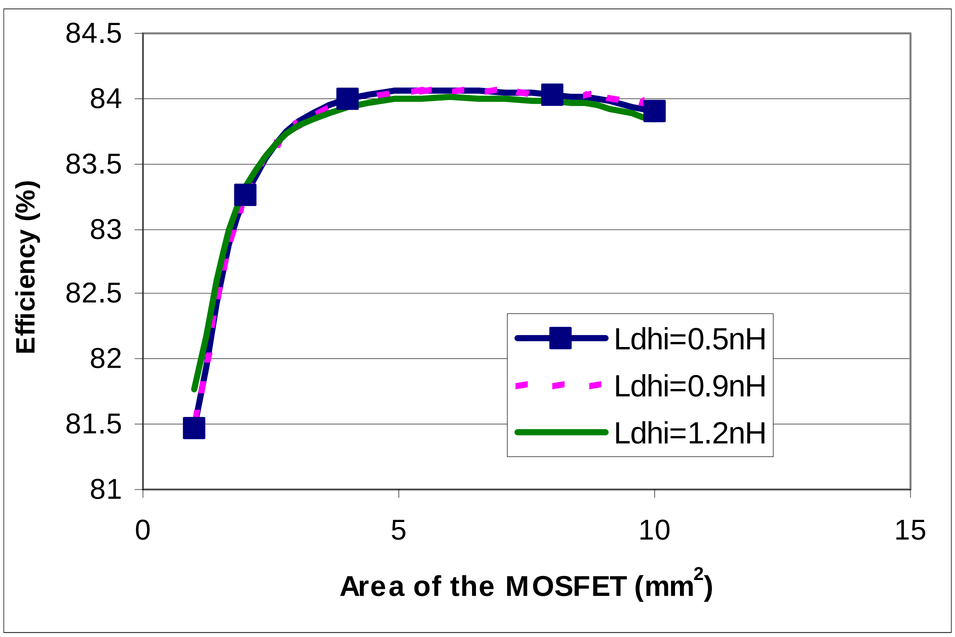


Fig. 4.31 Effect of L_{dhi} on efficiency.

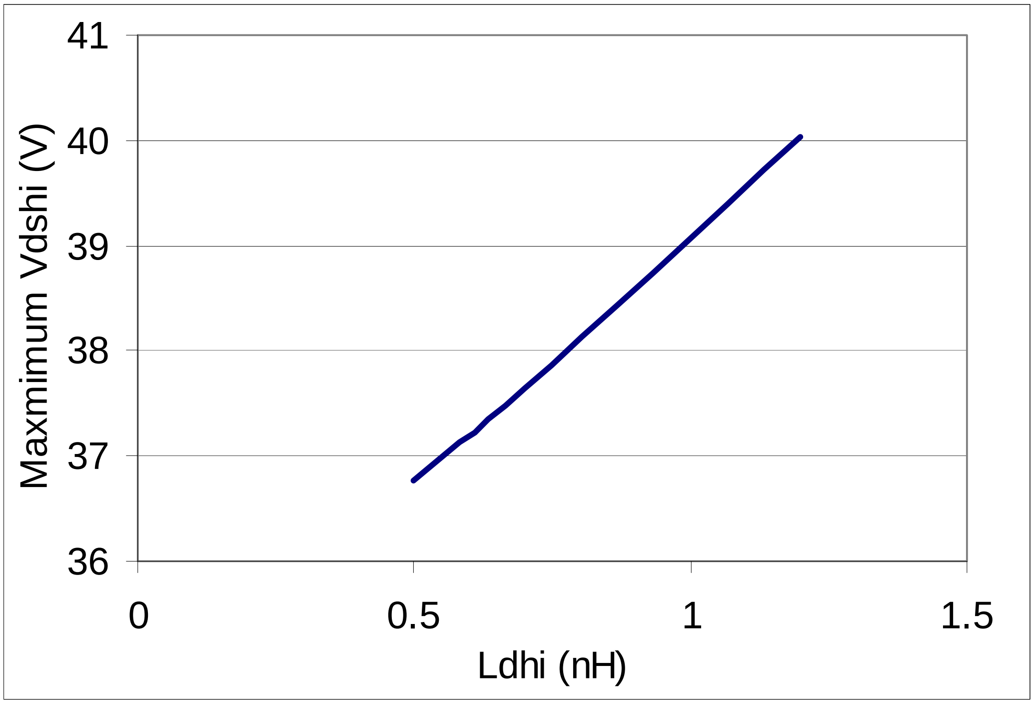


Fig. 4.32 Effect of L_{dhi} on $V_{dshimax}$.

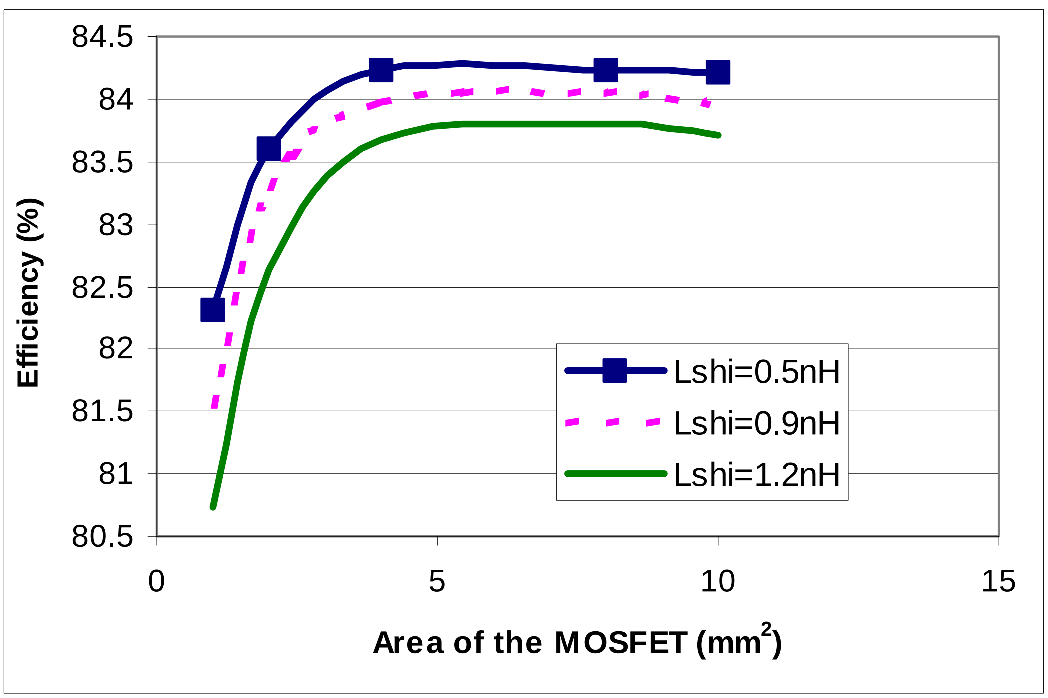


Fig. 4.33 Effect of L_{shi} on efficiency.

4.5 Summary

First of all, the simulation shows that the traditional definition of FOM does not precisely reflect the performance of the MOSFET. For example, thicker T_{ox} leads to less FOM, however, from the efficiency standpoint, thinner T_{ox} is required. Second of all, even if the lower FOM is caused by other design parameters, such as W_t or W_m, the device area must be selected correctly in order to achieve higher efficiency.

Another important simulation result is that the switching loss of the high-side MOSFET is not proportional to the device area. As shown in Fig. 4.34, there is an optimized area for the turn-on loss of the high-side MOSFET when L_{shi} = 0.9nH. This explains why the efficiency drops dramatically when the area of the high-side MOSFET is less than a certain value.

The difference between the analytical and simulation results shows that, for today's high-frequency applications, an optimized design cannot be achieved by the analytical models.

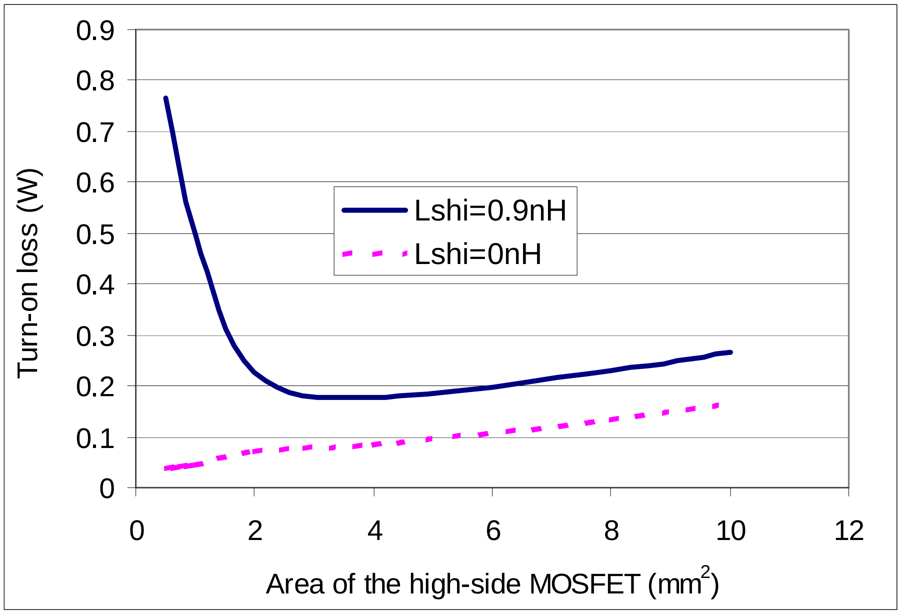


Fig. 4.34 Effect of the area of the high-side MOSFET on the switching loss of the high-side MOSFEF.

Chapter 5 Design of the Buck Converter Monolithically

5.1 Introduction

For the microprocessor, reducing the size of the power supply is very important, because small size can decrease the parasitic elements, which degrade the performance of the power supply. In order to minimize the effect of the parasitic elements, the power supply must be arranged around the microprocessor. However, the estate of the motherboard is very expensive. Therefore, smaller size is potentially more cost-effective from the system point of view.

The major barrier for the small size power supply is the thermal issue, because smaller size means poorer heat dissipation capability. If the temperature is very high, (the wildly accepted temperature of the package case of the MOSFET is about 120°C.) the reliability of the power system will be impaired. Currently, there are three types of power supply employed for the microprocessor in terms of integration level.

- Discrete application. The power MOSFETs are packaged separately. For the desktop, widely used package is DPAK or DDPAK; for the notebook, is SO8 or Power-PAK SO8. The driver and controller are integrated monolithically or packaged individually.
- Co-package solution. The power MOSFET and the driver (controller) are packaged in the same case.
- Monolithic integration. The power MOSFET and the diver (controller) are built on the same silicon die.

In order to handle large current, the multi-phase topology is used. However, the more the phase is, the more complex and expensive the power supply will be. Therefore, the number of the phase tends to be as small as possible. Hence, high current capability of each phase is preferred. The discrete application can handle more current, because the heat is dissipated by much more package cases. Indeed, the discrete solution is dominant in the market [C5]-[C10] now. However, as the switching frequency of the power supply keep increasing and the parasitic elements of the package play more important role in the power loss, the co-package and monolithic integration still have chance in the future [C11]-[C16]. With the advance of the device technology and the performance of the lateral MOSFET [A19]-[A24], the current capability of the monolithic solution increases steadily.

The basic function blocks in the monolithic integrated buck converter are illustrated in Fig. 5.1. The high voltage part includes the power MOSFET and the lever shift circuit; the low voltage part includes the deadtime generation and the switching control. In this chapter, an economical 5V/12V process is demonstrated. Then, a monolithic design is presented.

5.2 Process Design

Although the UMOSFET has larger current capability than the LDMOS, UMOSFETs can not be integrated monolithically in the buck converter, because of the following facts.

- In the buck converter, the source of the high-side MOSFET is connected with the drain of the low-side MOSFET. However, in the monolithic integration, the drains of UMOSFETs are tied together, because all the UMOSFETs share the same substrate.
- The substrate of the main stream CMOS process is of p-type. It is not suitable for the integration of the N-type UMOSFET.

In this section, an economical 5V/12V process is presented, which uses only two masks in addition to standard p-well technology. This process features a broad range of MOSFET and bipolar devices integrated on a common p-type substrate, including 5V CMOS, LDNMOS, LDPMOS, LIGBT and bipolar transistors. The self-isolation approach on p-type substrate allows the integration of the low voltage circuit, bootstrap circuit, low-side switch and high-side switch monolithically.

5.2.1 Process Flow

For the 12V VRM application, the voltage rating of the power MOSFET should be about 20V, which can be realized in several processes. However, most of these processes are very complicated or don't provide fully isolation between high-side and low-side MOSFETs. Hence, we developed a cost-effective CMOS-compatible technology, which has been demonstrated in Cornell Nanofabrication Facility (CNF).

The basic problem should be solved in the monolithic integration is how to isolate the low voltage MOSFET from the high voltage MOSFET. Fig. 5.2 shows device structure of different function blocks. The low voltage CMOS circuit feeds switching signals to the gate of the low-side MOSFET and to the input of the level shift circuit, which passes the signal to the driver of the high-side MOSFET. Except the block of the CMOS circuit, all MOSFET employs the lateral power MOSFET to realize the isolation.

The process starts on a 100~200 Ω·cm p-type substrate. The key process steps are as follows.

(1) Property of the silicon: P type <100>, 500-550 μm, 100-200 Ω.cm.

(2) Screen oxidation 50nm. Diffusion time = 30 min, Temperature = 1050 °C.

(3) Phosphor implantation. The implantation parameters are determined by the threshold voltage of the low voltage PMOS. Dose = 1.3×10^{12}, Energy = 50 kev.

(4) Boron implantation. The implantation parameters are determined by the threshold voltage of the low voltage NMOS (Fig. 5.3). Dose = 1.3×10^{13}, Energy = 50 kev.

(5) P-well alignment etching. Etching oxide 20 nm for the alignment of the active region in the next step. Remove photo resist.

(6) Diffusion (Fig. 5.4). Time = 685 min, Temperature = 1150 °C.

(7) Deposition of 12 nm nitride for the field oxidation.

(8) Etching off the nitride from the inactive area (Fig. 5.5).

(9) 0.94 μm field oxidation (Fig. 5.6). Time = 80 min, Temperature = 1150 °C.

(10) 35 nm gate oxidation.

(11) Poly gate definition (Fig. 5.7).

(12) Boron implantation for the P-body of the LDMOS (Fig. 5.8). Dose = 2.5×10^{13}, Energy = 30 kev.

(13) Phosphor implantation for the N-region of the LDMOS (Fig. 5.9). Dose = 1.0×10^{13}, Energy = 20 kev.

(14) Diffusion (Fig. 5.10). Time = 35 min, Temperature = 1150 °C.

(15) Boron implantation for the P^+ contact (Fig. 5.11). Dose = 2.0×10^{15}, Energy = 10 kev.

(16) Phosphor implantation for the N^+ contact (Fig. 5.12). Dose = 4.0×10^{15}, Energy = 20 kev.

(17) Fast anneal (Fig. 5.13). Time = 0.5 min, Temperature = 920 °C.

Compared with standard p-well CMOS process, only two masks (p-body and n-regrion) are added. There are totally ten masks used in the process:

(1) Pwell layer. In step 4 to define the region of P-well.

(2) Active layer. In step 8 to define the active region.

(3) Gatepoly layer. In step 11 to define the poly gate.

(4) Pbody layer. In step 12 to define the P-body of the LDMOS.

(5) Nregion layer. In step 13 to define the N-region of the LDMOS.

(6) Pplus layer. In step 15 to define the P^+ region.

(7) Nplus layer. In step 16 to define the N^+ region.

(8) Contact layer.

(9) Metal layer.

(10) Passivation layer.

This work was performed at the Cornell Nanofabrication Facility (a member of the National Nanofabrication Users Network). The top view of a fabricated LDMOS and the SEM picture of the poly gate are shown in Fig. 5.14.

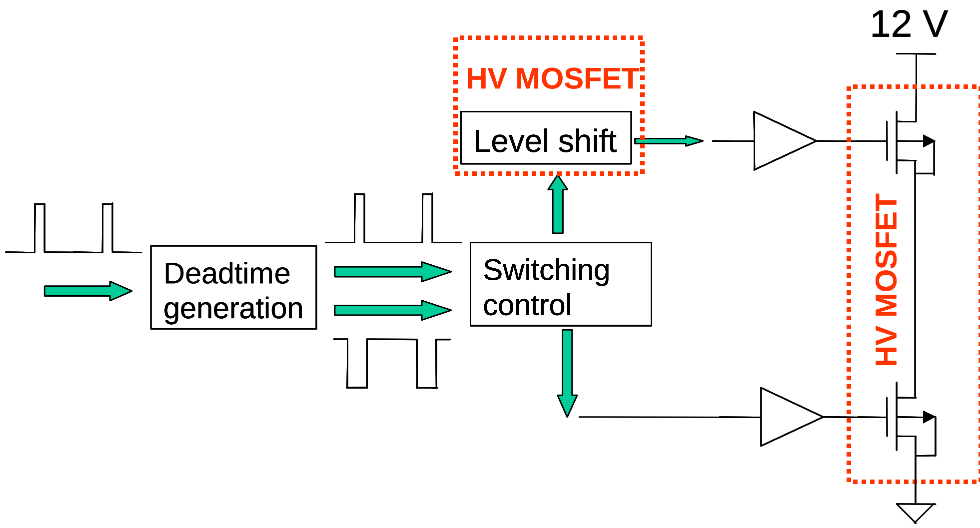


Fig. 5.1 Topology of monolithically integrated buck converter.

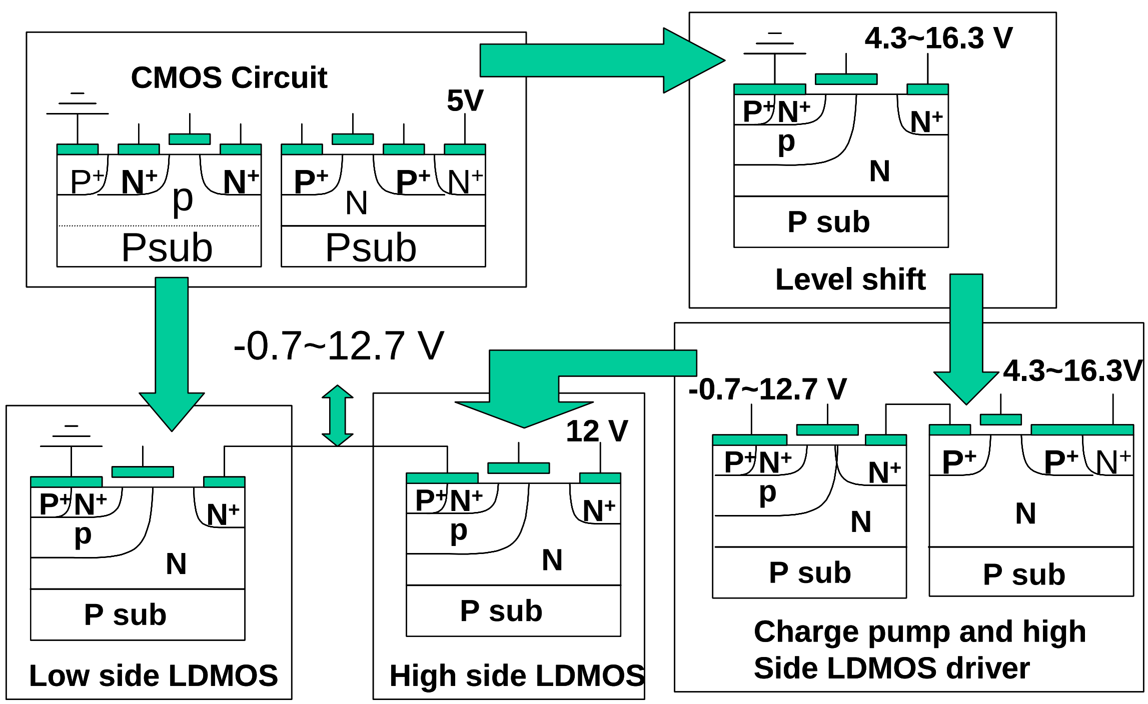


Fig. 5.2 Isolation and signal flow in the monolithically integrated buck converter.

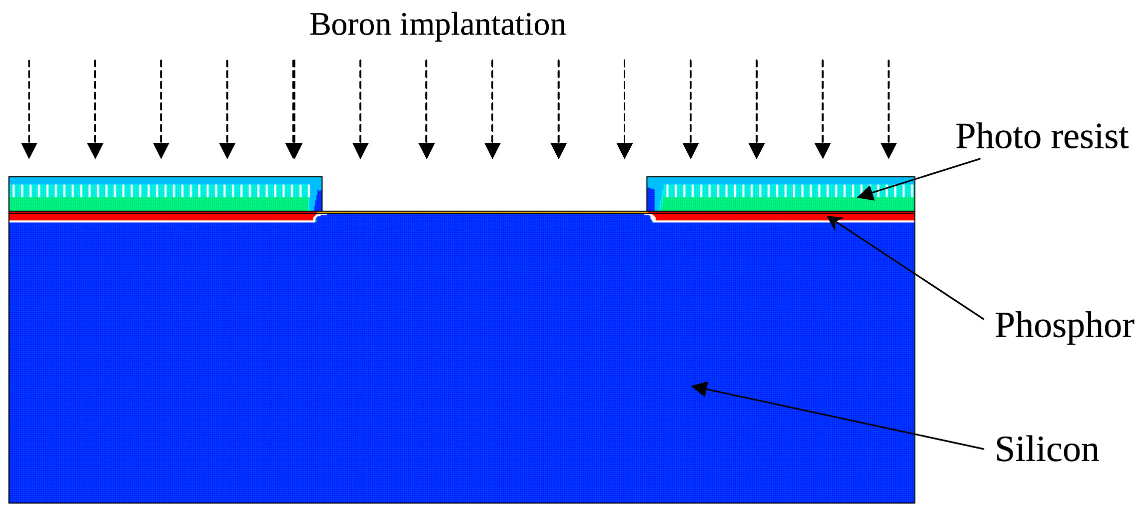


Fig. 5.3 Simulated cross section of the process flow (Step 4).

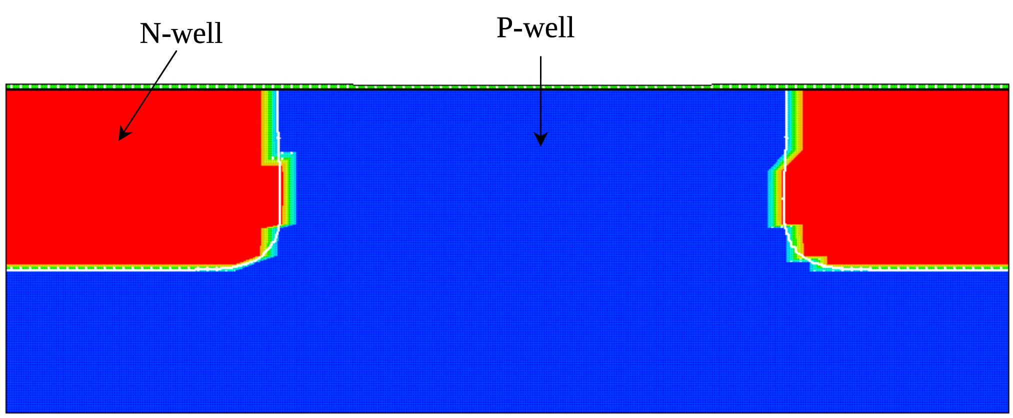


Fig. 5.4 Simulated cross section of the process flow (Step 6).

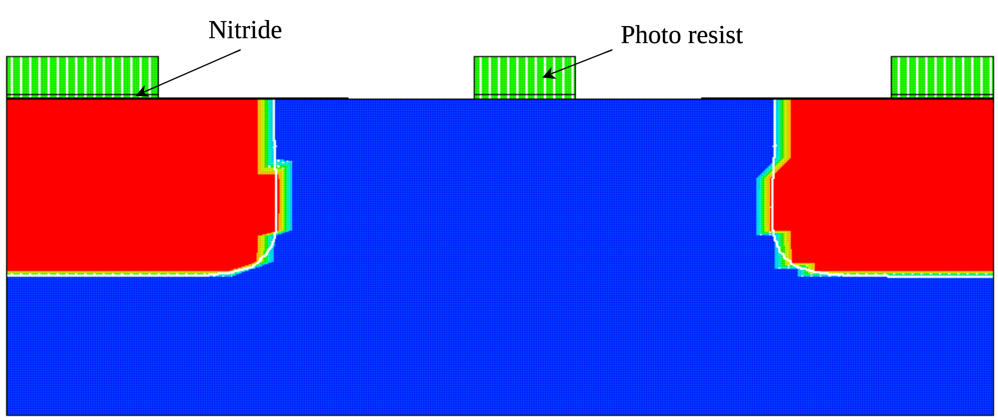


Fig. 5.5 Simulated cross section of the process flow (Step 8).

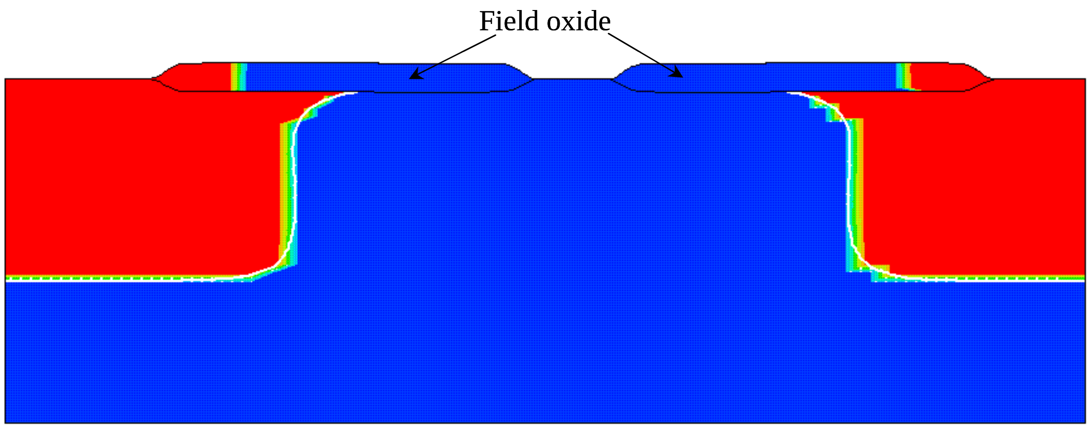


Fig. 5.6 Simulated cross section of the process flow (Step 9).

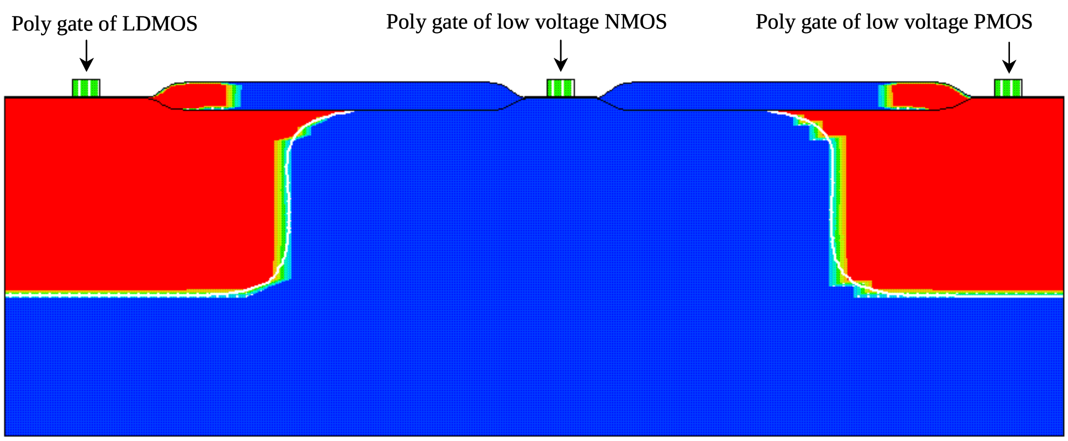


Fig. 5.7 Simulated cross section of the process flow (Step 11).

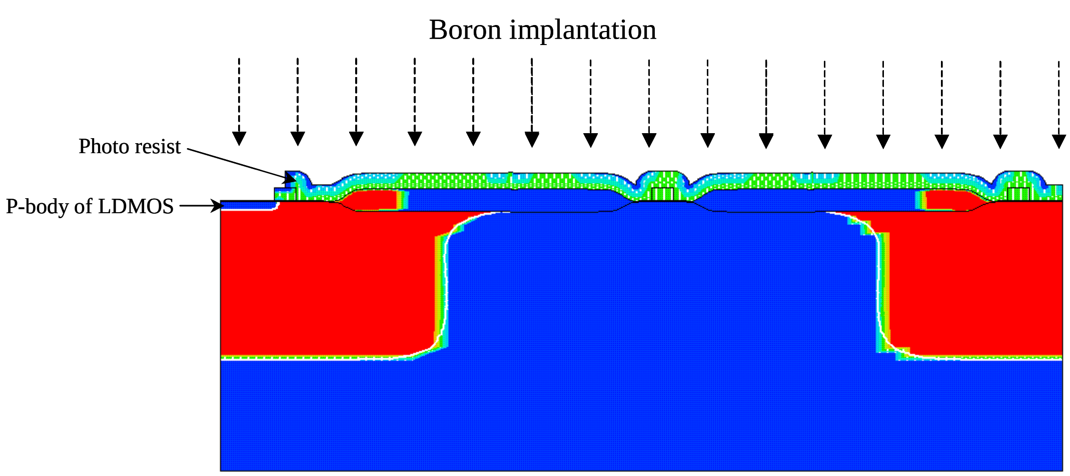


Fig. 5.8 Simulated cross section of the process flow (Step 12).

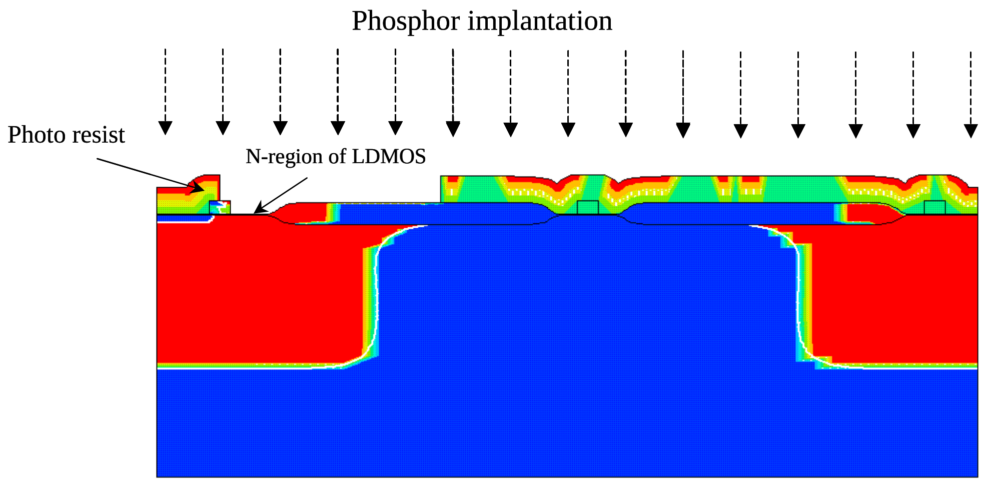


Fig. 5.9 Simulated cross section of the process flow (Step 13).

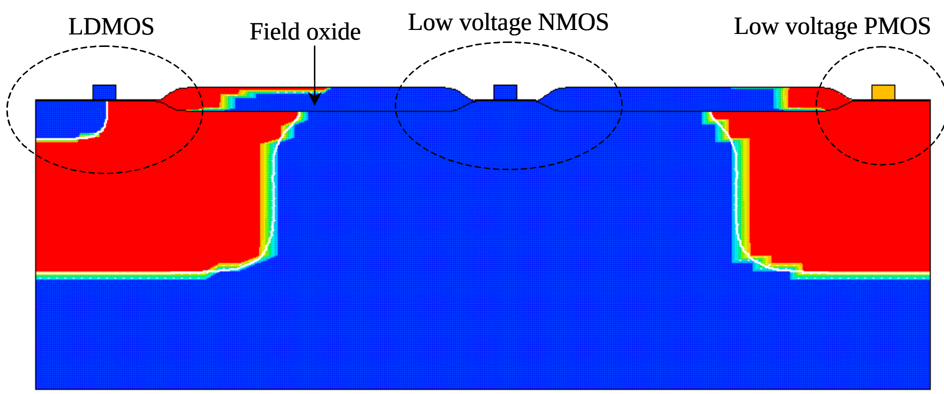


Fig. 5.10 Simulated cross section of the process flow (Step 14).

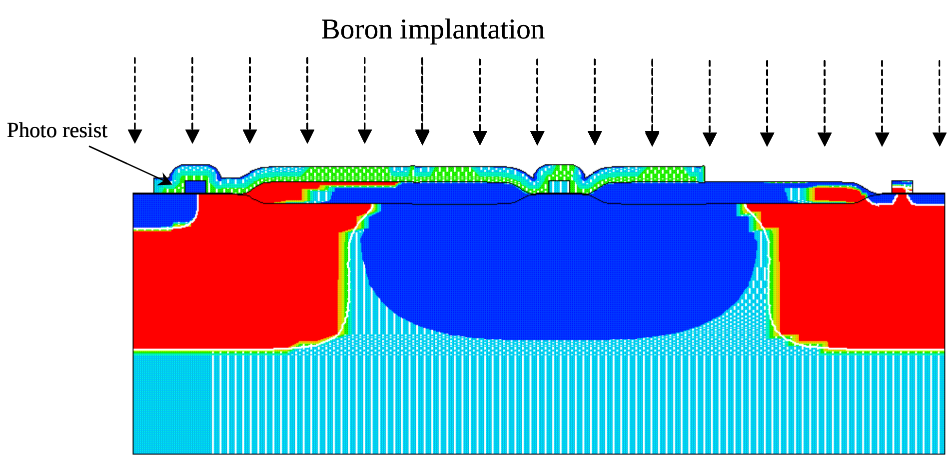


Fig. 5.11 Simulated cross section of the process flow (Step 15).

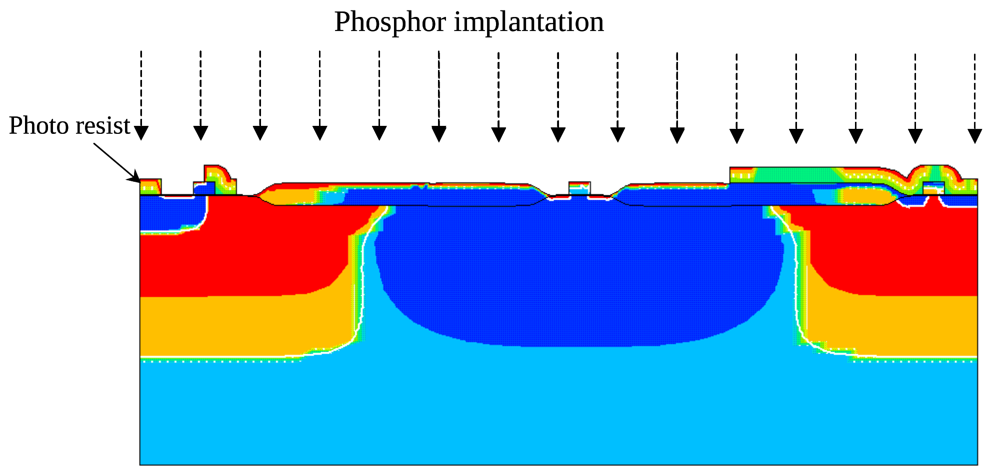


Fig. 5.12 Simulated cross section of the process flow (Step 16).

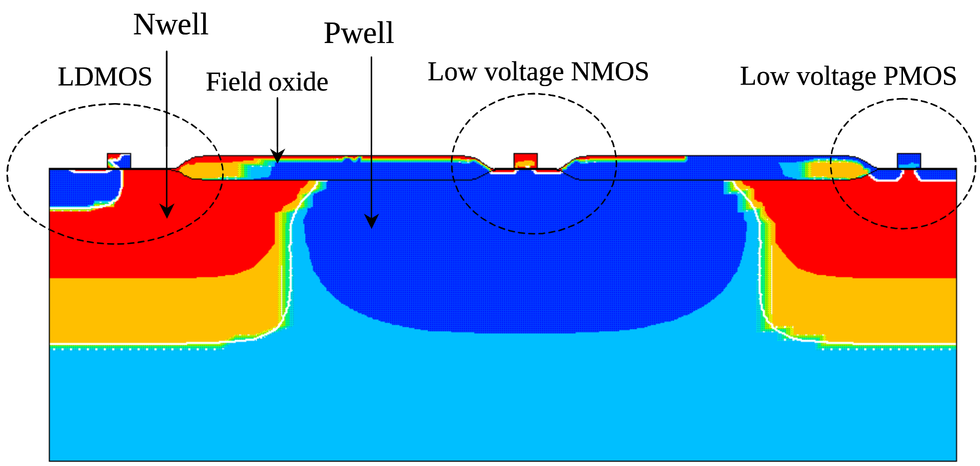


Fig. 5.13 Simulated cross section of the process flow (Step 17).

5.2.2 Experimental Results and Discussion

5.2.2.1 Voltage blocking capability

The isolation between the low-voltage CMOS and the high-voltage LDMOS is a basic function of the power IC process. Such capability is achieved by the PN junction descried in the preceding section.

Fig. 5.15 shows the breakdown characteristic between the N-well and the P-well. The breakdown voltage is above 140 V. Because the LDMOS is located in the N-well, this means the isolation voltage between the LDMOS and the CMOS can be as high as 140V. Such voltage is enough for the 20 V input buck converter.

Fig. 5.16 shows breakdown characteristic between the N-well and the P-body of the LDMOS. The breakdown voltage is above 43 V. This is the maximum voltage rating of the LDMOS. It also meets the design target.

5.2.2.2 Performance of the MOSFETs

The structure and the forward conduction characteristics of the PMOS and NMOS are shown in Fig. 5.17 and Fig. 5.18 respectively. Both NMOS and PMOS demonstrate good performance, which is suitable for 5V application.

Fig. 5.19 shows the structure and the characteristic of the LDMOS. The breakdown voltage of the LDMOS is about 18V. Table 5.1 compares the experimental and simulation results of the MOSFETs. The difference between the simulation and experiment is reasonable, because the contamination in the process is almost inevitable.

Table 5.1 Comparison of the experimental and simulation results

	V_t (V)	BV (V)	Ron (kΩ•μm)
NMOS L_g = 0.8 μm	0.6 0.7 (simulation)	12 13 (simulation)	7 5 (simulation)
PMOS L_g = 0.8 μm	0.8 0.9 (simulation)	16 13 (simulation)	20 18 (simulation)
LDMOS L_g = 0.8 μm L_d = 0.8 μm	1.4 1.3 (simulation)	18 20 (simulation)	8.7 6.8 (simulation)

Besides the voltage blocking capability and the performance of the MOSFETs, the characteristics of the inverter is also tested. Fig. 5.20 illustrates the DC transfer characteristic of a single stage inverter, the AC gain of which is pretty high.

The experimental results demonstrate the proposed process has enough isolation capability for the monolithic integration of 12V input buck converter, the characteristics of the MOSFETs are close to the simulation results and the performance of the inverter is good. The whole circuit of the buck converter is not built up based on this process, because the fabrication facility is not suitable for the large area device. However, the monolithic integration is performed using another process developed in the National Semiconductor Company as discussed in the next section.

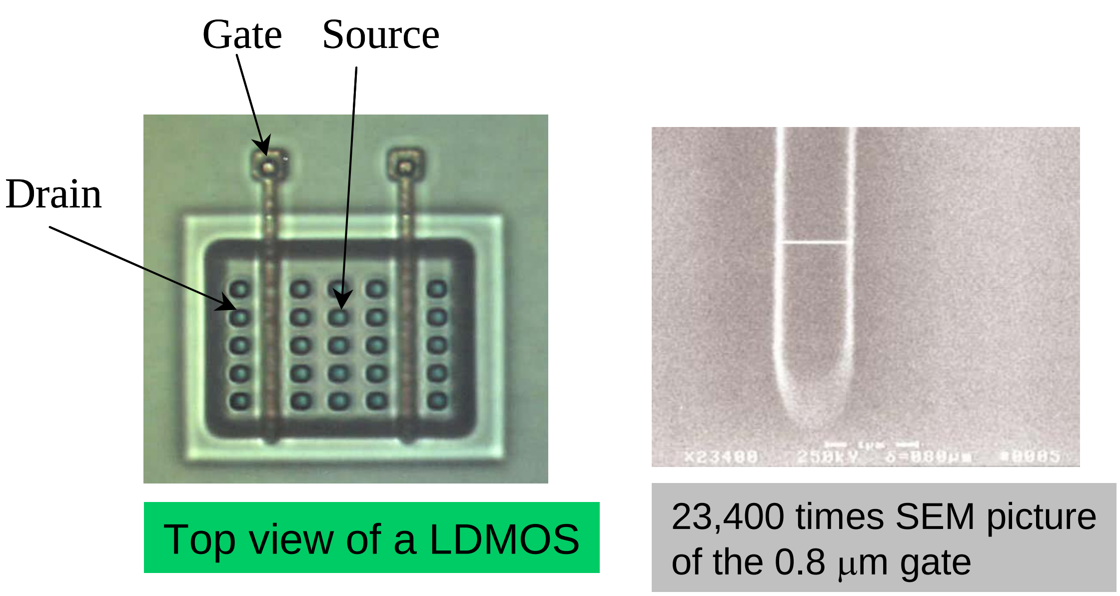


Fig. 5.14 Pictures of the fabricated device structure

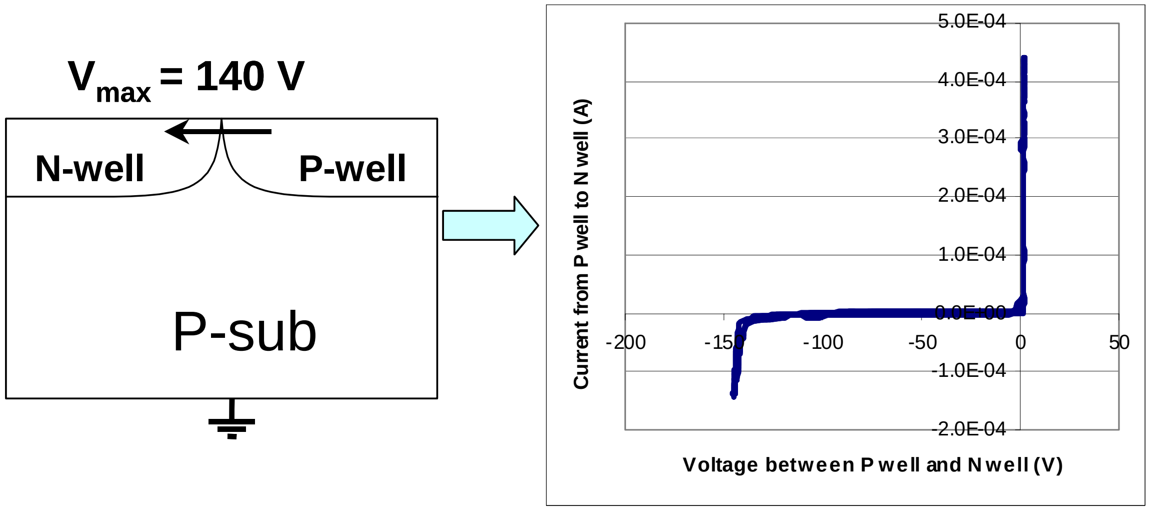


Fig. 5.15 Experiment results of the breakdown characteristic between the P-well and N-well.

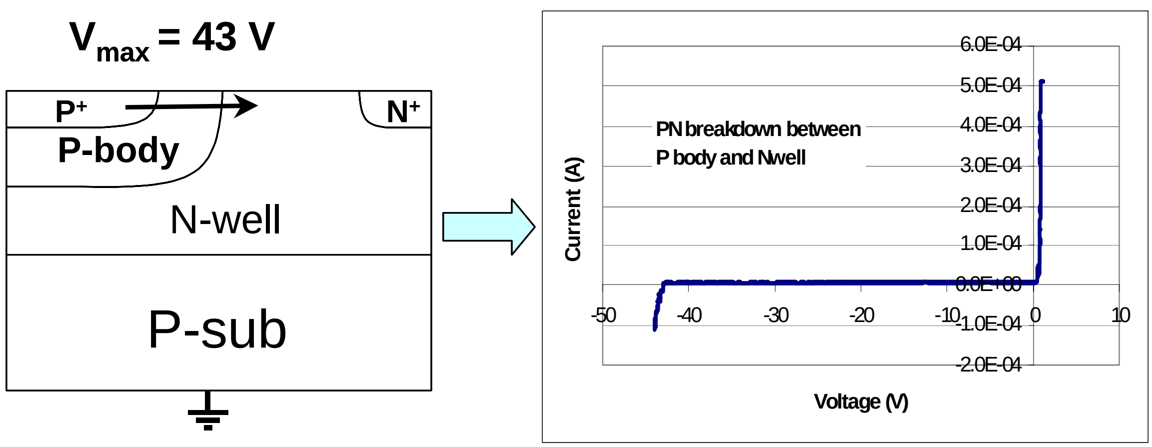


Fig. 5.16 Experiment results of the breakdown characteristic between the P-body and N-well.

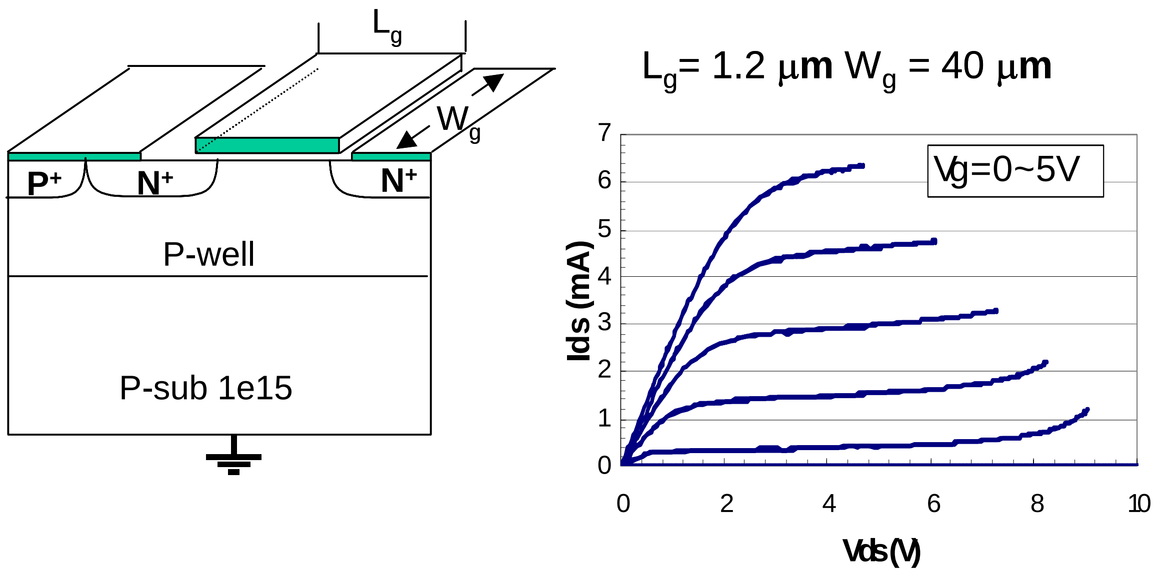


Fig. 5.17 Experiment results of the forward conduction characteristic of the low-voltage NMOS.

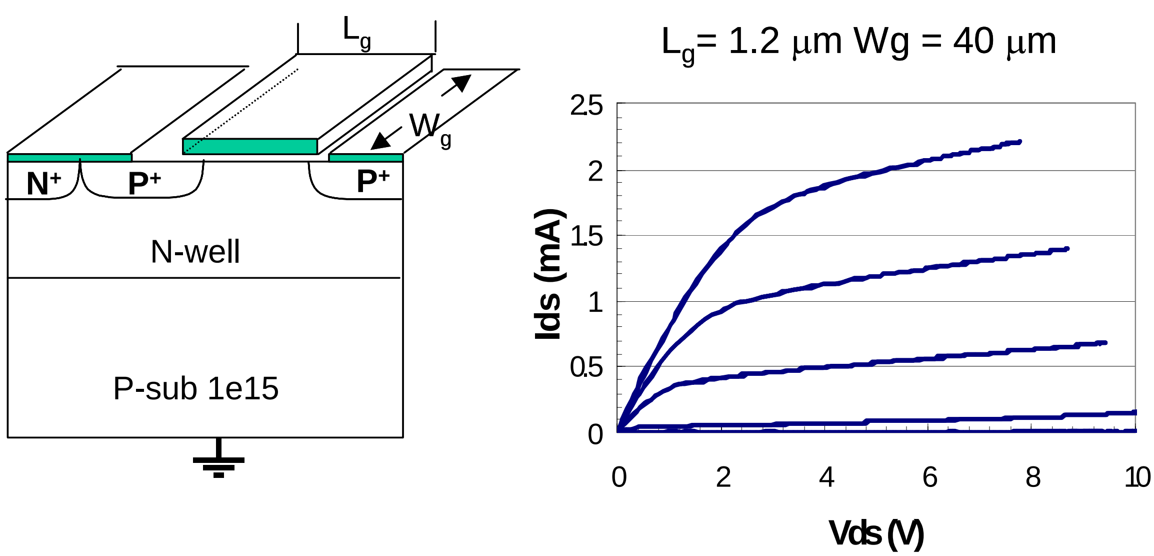


Fig. 5.18 Experiment results of the forward conduction characteristic of the low-voltage PMOS.

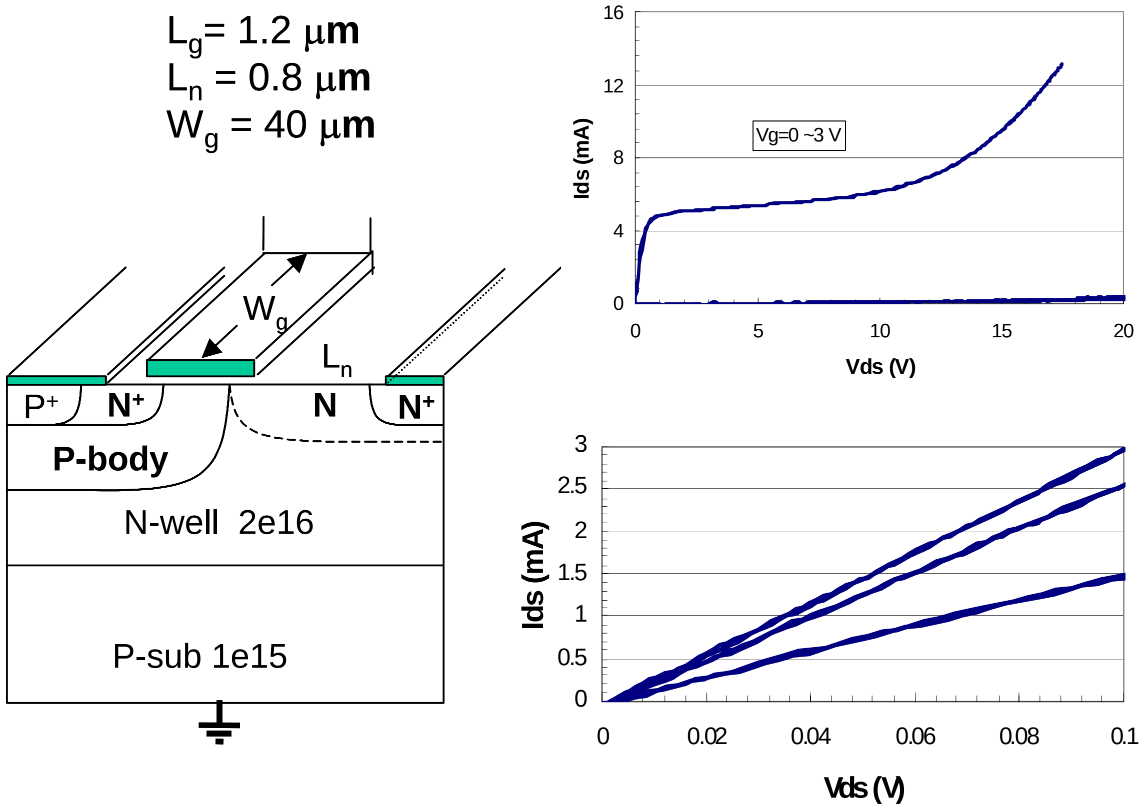


Fig. 5.19 Experiment results of the forward conduction characteristic of the LDMOS

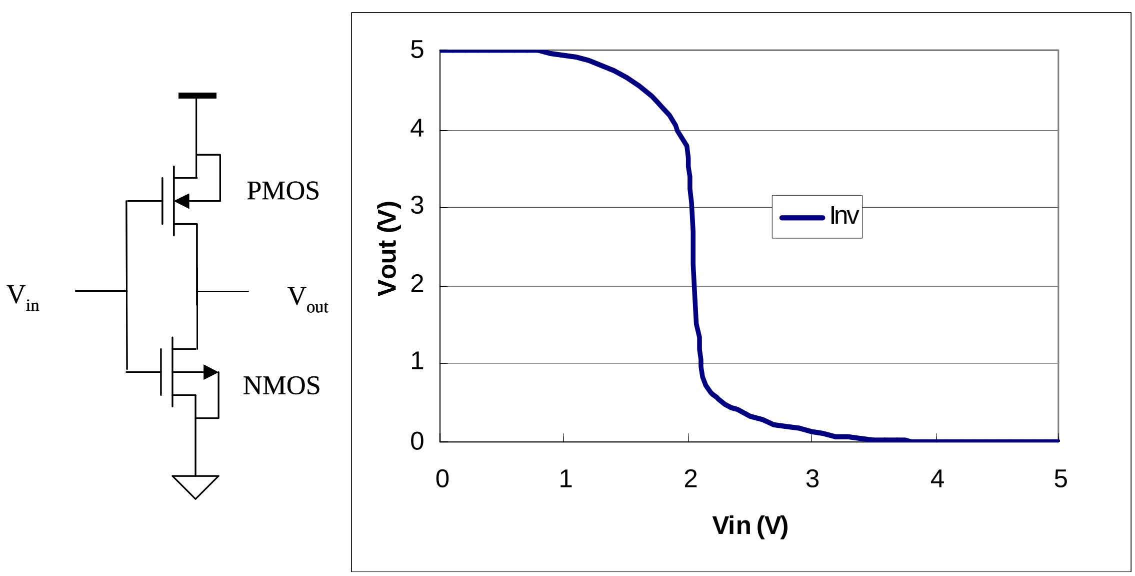


Fig. 5.20 DC transfer characteristic of the inverter.

5.3 Monolithic Design of the Buck Converter

This section presents a monolithic design of the buck converter, which employs National Semiconductor's power IC process. In this process, the isolation is realized by deep trench filled by polysilicon. The typical devices of this process includes

- Vertical NPN and PNP bipolar transistor,
- 30V N-type LDMOS,
- Low voltage PMOS and NMOS,
- High voltage PMOS and NMOS,
- Zener diode.

5.3.1 Design of the LDMOS

The main design challenge of the monolithic integration of the high voltage LDMOS is that the on resistance of LDMOS is much larger than that of the power UMOSFET, because of the following facts.

- As addressed in the section (2.1.2), the specific on resistance (resistance per unit area) of LDMOS is inherently larger than that of the UMOSFET. The typical specific on resistance of the 30 V LDMOS is about 40 $m\Omega \cdot cm^2$, while it is below 30 $m\Omega \cdot cm^2$ for the 30 V UMOSFET.
- It is impractical to reduce the resistance of the LDMOS by increasing the device area, because the metal debiasing effect can significantly increase the total resistance when the device area is large and the maximum the device area is limited by the package.

Since the main current path of the LDMOS is from the drain to the source and the source of high-side MOSFET is connected with drain of the low-side MOSFET, the shape of the layout of both the high-side and low-side MOSFET is flat as shown in Fig. 5.21. In order to handle large current, three pins are dedicated for the drain of the high-side MOSFET and source of the low-side MOSFET, for pins for the switching node. One problem associated with such flat design of the power MOSFET is that the connection between the last stage of the driver to the gate of the power MOSFET is very long. The parasitic resistance and inductance of the long connection path can slow down the switching speed of the MOSFET. This effect is more significant for the low-side MOSFET, since it has more gate charge than the high-side MOSFET. Therefore, the last stage of the gate driver is designed like a narrow bar and located by the side of the low-side MOSFET to accelerate the switching of the low-side MOSFET (Fig. 5.22).

The final selection of the area of the MOSFET depends on the optimization results. Since the process is fixed, the only parameter can be tuned is the area of the MOSFET. The simulated efficiency as the function of the MOSFET area is shown in Fig. 5.23. The simulation condition is

- input voltage is 12 V,
- output voltage is 1.7 V,
- output current is 4 A,
- switching frequency is 1MHz.

Based on Fig. 5.22, the area of the low-side MOSFET is 2.535mm^2, the area of the high-side MOSFET is 1.211mm^2. Fig. 5.23 shows the overall design. The adaptive deadtime control is addressed in the next section.

5.3.2 Adaptive Deadtime Control of the Buck Converter

As described in Chapter 4, the power loss due to the deadtime (deadtime loss) is not trivial in the buck converter. In the duration of the deadtime, the current goes through the body diode of the low-side MOSFEF, resulting in instantaneous high power loss, because the forward voltage drop of the body diode (typically is 0.7V) is much larger than the voltage drop of the MOSFET (typically is 0.05 V). Another loss associated with the conduction of the body diode is the reverse recovery loss. Therefore, reducing the deadtime can substantially decrease the power loss especially at high switching frequency. Usually the deadtime is fixed and determined by the driver/controller. The duration of the deadtime can’t be designed too short. Otherwise, it may cause the turn-on of both the high-side and low-side MOSFETs. The basic idea of the adaptive deadtime control is to sense the turn-on of the body diode. Upon sensing the turn-on, the voltage sensor triggers a gate controller to turn on a switch in the regulator, and thereby terminate a dead time. The voltage sensor and gate controller are high-speed circuits, and therefore can reduce the duration of the dead time. Reducing the dead time duration improves efficiency by reducing the duration of body diode conduction. The dead time can be reduced to less than a turn-on time of the body diode, thereby preventing charge buildup in the body diode, and consequently preventing reverse recovery loss in the body diode.

Sensing the high-side MOSFET turn off (deadtime2) will typically be an easier task than sensing the low-side MOSFET turn off (deadtime1). This is because V_{sw} (Fig. 5.23) has a relatively large change from V_{in} to about -0.7 volts when the high-side MOSFET is turn-off, and Vsw has a relatively small change from about zero volts to about -0.7 volts when the low-side MOSFET is turning off. Therefore, the voltage sensor must be able to sense small, rapid voltage changes, and produce a trigger for the gate controller in response. In addition, the voltage sensor must be capable of withstanding without damage relatively high voltage spikes in V_{sw}. Preferably, the voltage sensor can respond to a change in the swing node voltage from -0.1 to -0.3 volts in about 1 nanosecond.

Several circuits can be used as the voltage sensor, including high speed voltage amplifiers, high speed voltage comparators, and the like. The voltage sensor must have high sensitivity to voltage reversals, high speed, and a tolerance for high peak voltages.

Fig. 5.24 shows a specific embodiment of the present invention where the voltage sensor is an NPN bipolar transistor with an emitter E connected to the swing node. The transistor has a base B connected to ground potential, or to a potential in the range of about zero to +0.6 volts. The collector C is connected to the switching control. A resistor R is connected to the collector C and a voltage source (+5V) providing, for example, a digital signal level voltage (e.g. 5 volts). The resistance of resistor R is selected so that voltage at collector C drops to about zero and switching control receives triggers when the deadtime occur. An appropriate resistance value for resistor R can be, for example about 50 kΩ to 250 kΩ. The gain of the transistor can have a wide ranging value, for example in the range of about 10-100.

In operation, transistor is off while the high-side MOSFET or the low-side MOSFET is on. Transistor turns on at the deadtime, when the swing node voltage V_{sw} falls below approximately ground potential. At this time, the transistor triggers the switching control by low voltage level. The switching control in response turns on the high-side MOSFET or the low-side MOSFET, depending on which deadtime has just occurred.

It is noted that the speed and sensitivity of the bipolar transistor can be improved by connecting the base B to a slightly positive voltage in the range of about 0 to + 0.6 volts. Such a slightly positive voltage tends to cause the bipolar transistor to turn on sooner, thereby allowing for shorter dead times. However, it is noted that if the base voltage is too high (e.g. 1 volt), false triggering of the gate controller will result.

Also, it is important for transistor to be able to withstand without damage the high voltage spike that occurs at the swing node. This voltage spike is applied across the emitter-base junction, which is often an easily damaged junction in bipolar transistors. A particularly useful bipolar transistor for is a parasitic bipolar transistor integral to the power LDMOS. The parasitic bipolar transistor integral to an LDMOSFET shown in Fig. 5.24 has high emitter-base voltage capability (due to junction between P-body and N-well), and can be manufactured monolithically with the power LDMOSFET. In fact, the power LDMOSFET and the transistor can have exactly the same doping structure, with the transistor having different electrical connections, as shown in Fig. 5.24. Monolithic fabrication of the power LDMOS and the transistor is advantageous because it can provide a sensor at low cost.

Fig. 5.25 shows another specific embodiment where the voltage sensor comprises a first sensor LDMOSFET and a second sensor NMOSFET connected in series. The gate of the first sensor is connected to a reference voltage V_{ref} (e.g. 5 volts). The first sensor LDMOSFET can be identical to the power LDMOSFET, thereby simplifying monolithic fabrication. The gate of second NMOSFET is connected to ground potential, or a potential close to ground potential (i.e. within about 1 volt of ground potential). The second sense NMOSFET should have a low turn-on threshold voltage, for example a threshold in the range of about 0-0.5 volts. In a particularly useful embodiment, the second sense NMOSFET is a native MOSFET, which typically have a turn on threshold voltage of about zero volts.

In operation, the first sensor LDMOSFET is off while the high-side MOSFET is on, and voltage sensor output voltage is +5V. At the deadtime, the swing voltage V_{sw} becomes negative, turning on both the LDMOSFET, and native NMOSFET. This causes the output of the voltage sensor to become negative, triggering the switching control. When the low-side MOSFET is on, V_{sw} is approximately zero, the native NMOSFET 40c will be off, and output voltage will be approximately zero.

The present adaptive deadtime control provides unique and substantial advantages over conventional buck regulators. Specifically, it is capable of providing much shorter deadtimes. Because this method senses voltage at the swing node (instead of at the gates of the high-side or the low-side MOSFETs), the circuit directly senses the turn-off of switches. This allows for extremely short deadtimes because variations in the commutation times of the switches are automatically compensated for, and hence, such variations do not effect the durations of the deadtimes. By comparison, some conventional buck regulators sense gate voltage of the switches in order to provide feedback control. This can be problematic because actual turn-on time of the high-side and low-side MOSFETs varies substantially with operating conditions, resulting in variation in durations of the deadtimes, and possible damage the circuit if the dead time is reduced to zero.

The whole layout of the monolithic buck converter is shown in Fig. 5.26. The silicon area is about $6\times1.6 = 9.6$ mm^2.

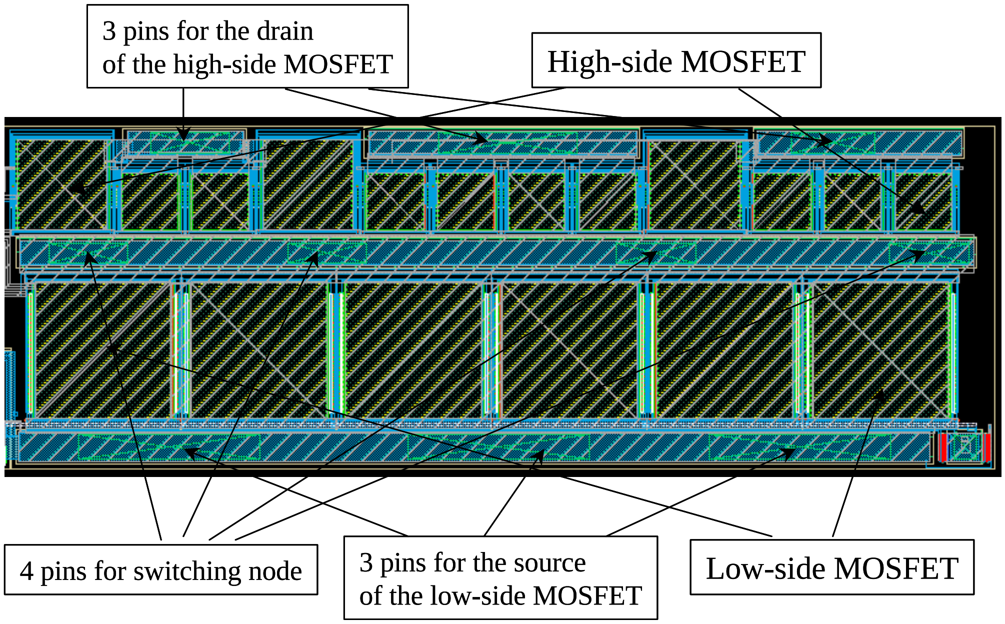


Fig. 5.21 Layout of the power LDMOS

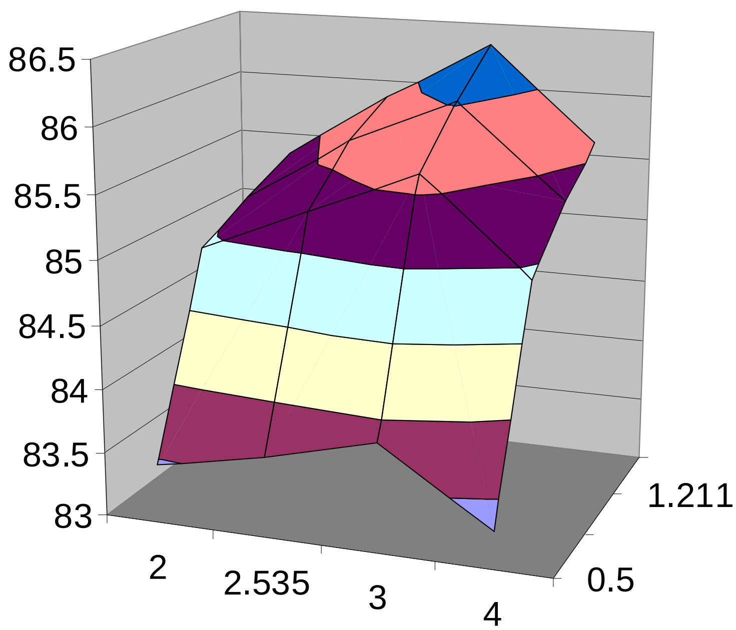


Fig. 5.22 Optimization of the device area

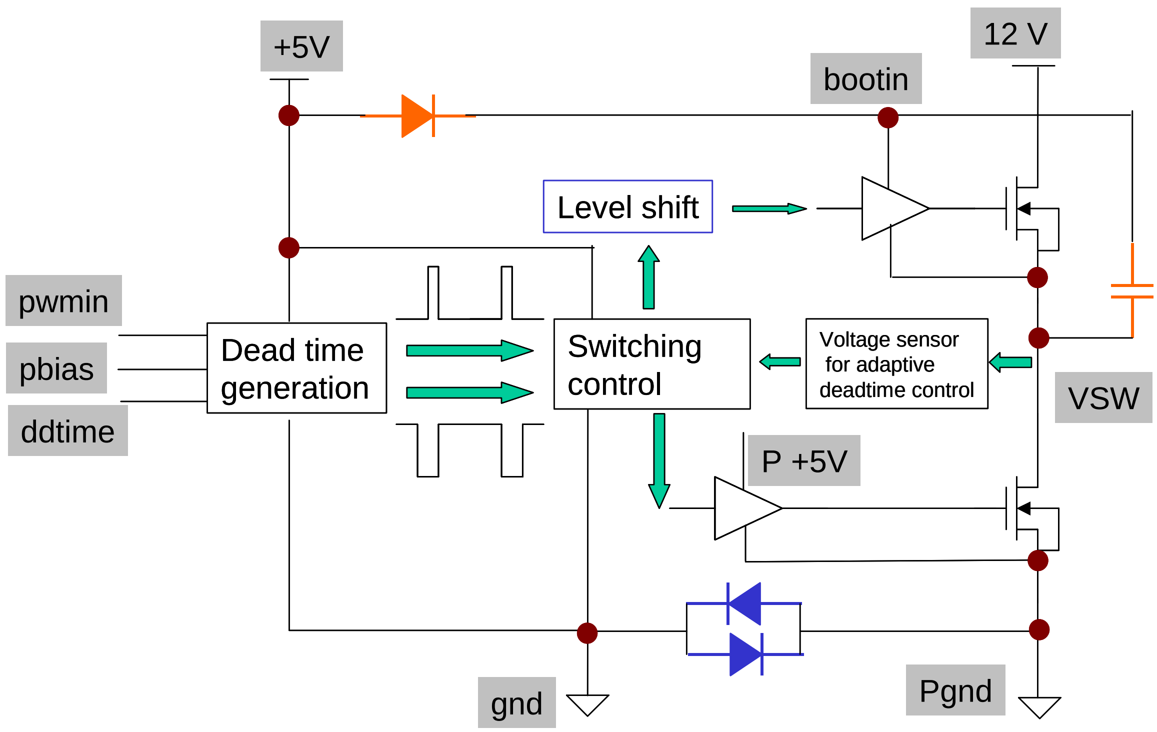


Fig. 5.23 Function diagram of the design

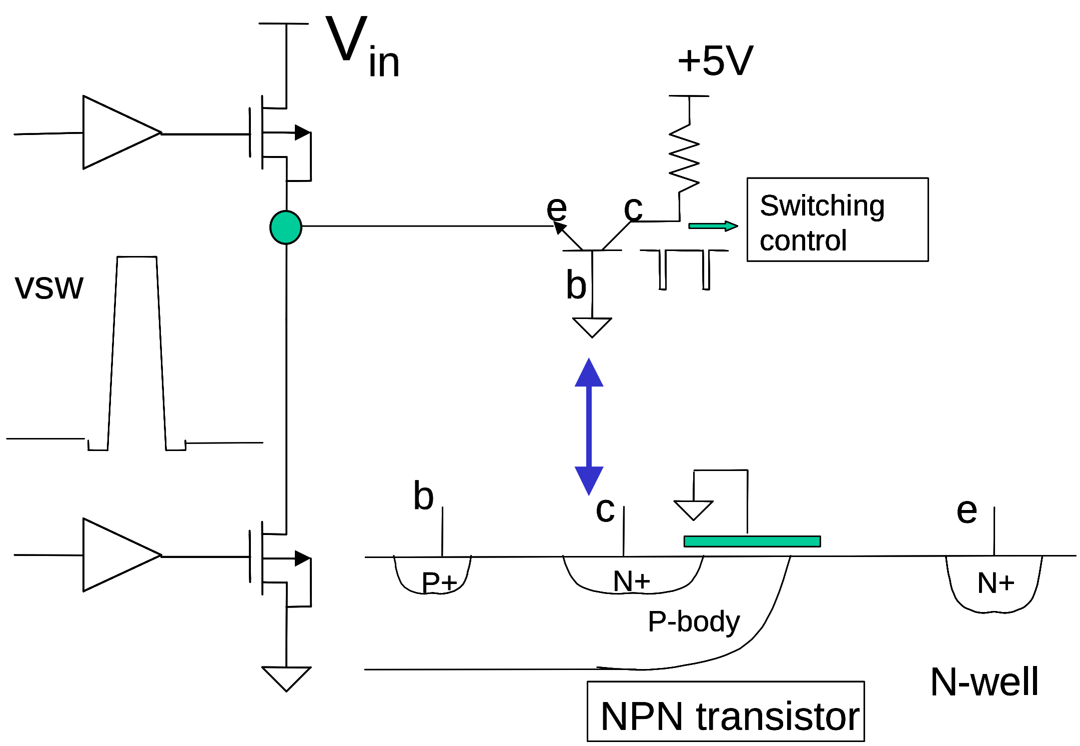


Fig. 5.24 Using the parasitic NPN transistor as the voltage sensor

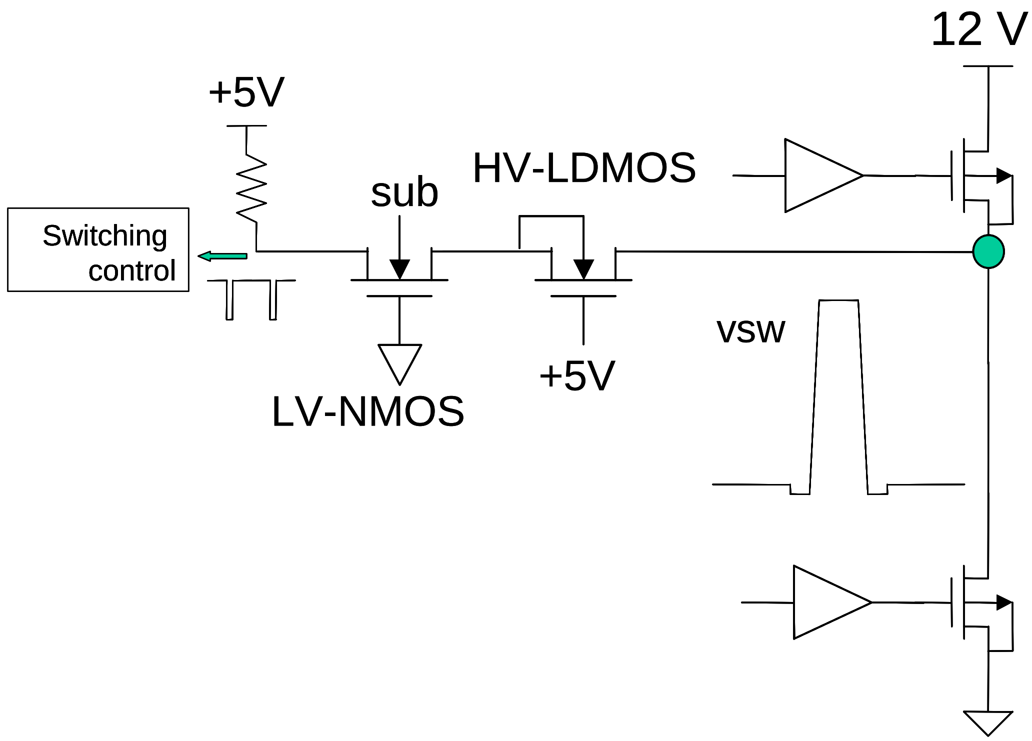


Fig. 5.25 Using the LDMOS and a low voltage MOSFET as the voltage sensor

5.3.3 Experimental Results and Discussion

The design is fabricated in the National Semiconductor and packaged in the SOIC20 ceramic frame as shown in Fig. 5.27. Fig. 5.28 shows the circuit used for the efficiency measurement. The efficiency at 1 MHz is shown is Fig. 5.29. The results are lower than the design values. The main reasons are as follows.

- The on resistances of both the low-side MOSFET and the high-side MOSFET are much larger than the design. Fig. 5.30 and Fig. 5.31 show the V_{ds} of the low-side MOSFET and high-side MOSFET respectively. The on resistances of the MOSFETs can be estimated from the waveforms. Such high resistance may due to the metal debiasing effect and the process control.
- There is substantial leakage current from the input voltage (V_{in}) to the ground. As shown in Fig. 5.32, the leakage power is significant when V_{in} = 12 V. Without such leakage power the light load efficiency would be much higher as shown in Fig. 5.33.

Besides the efficiency, the adaptive function of deadtime control also works well. Fig. 5.34 compares the voltage on the switching node with and without adaptive deadtime control. The durations of the deadtime are reduced significantly when voltage level on the pin ddtime is high.

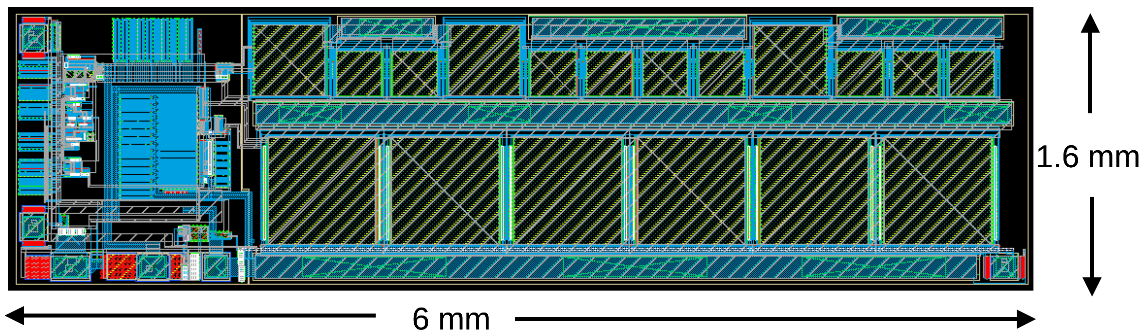


Fig. 5.26 Layout of the design

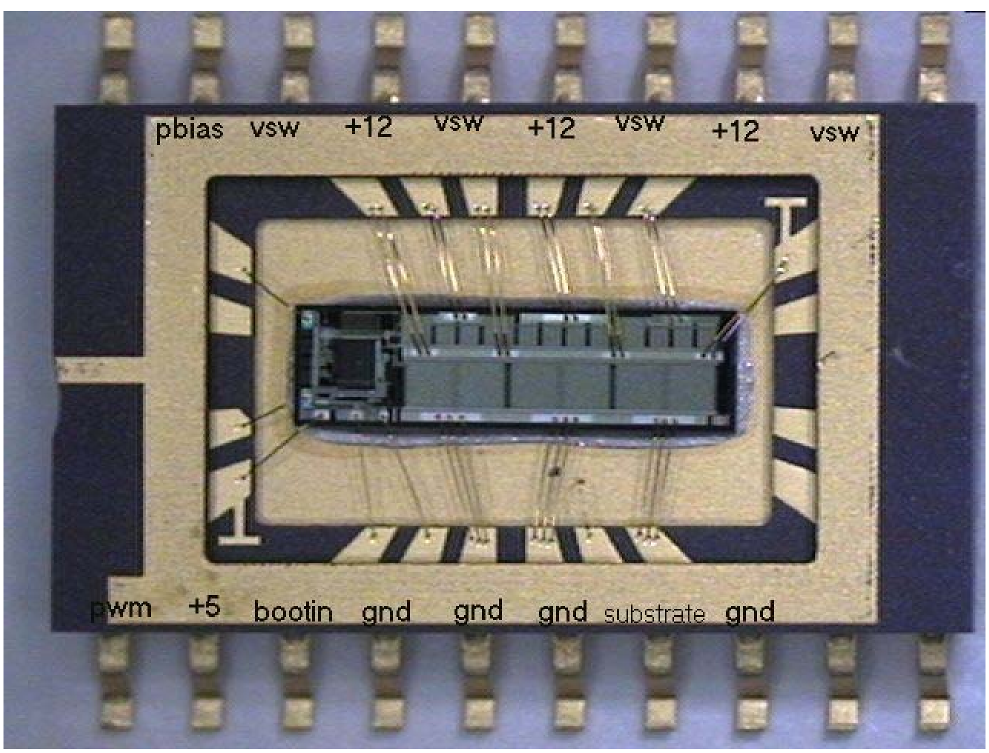


Fig. 5.27 Die in the SOIC20 ceramic frame

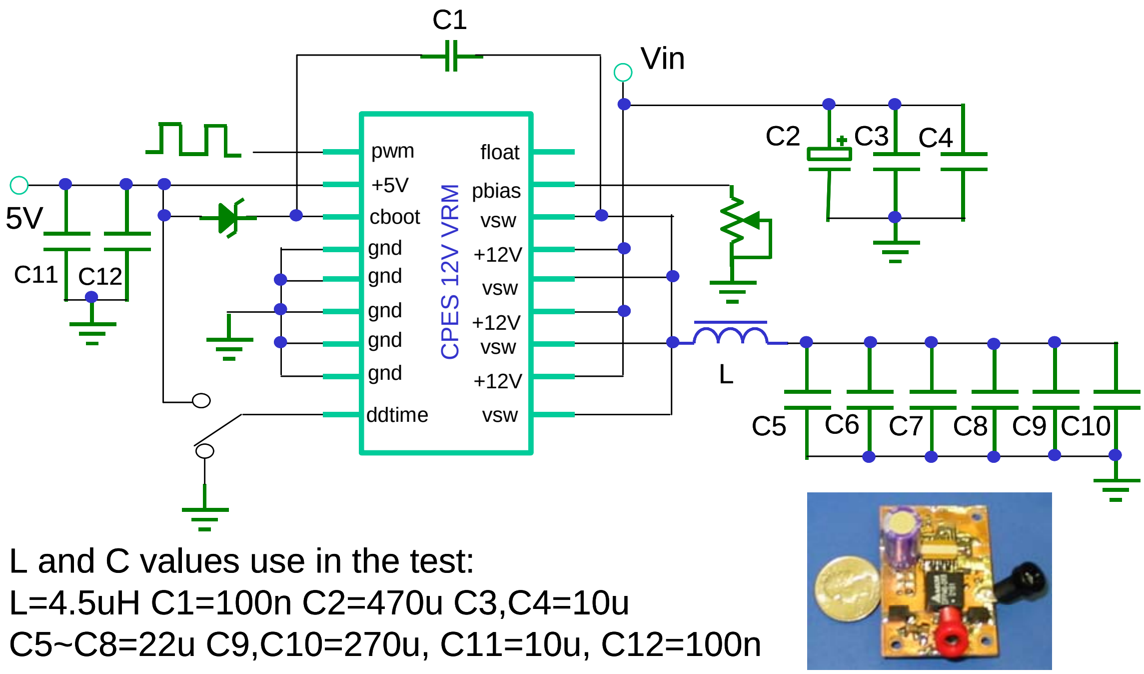


Fig. 5.28 Circuit for the efficiency measurement

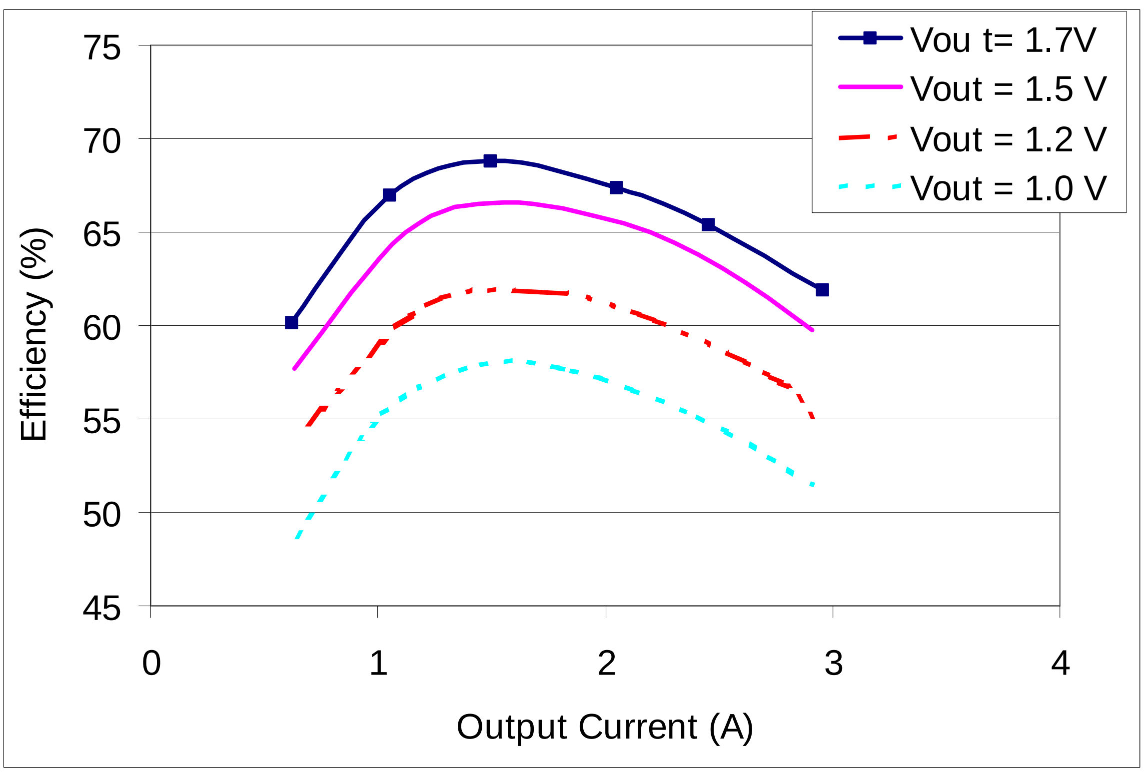
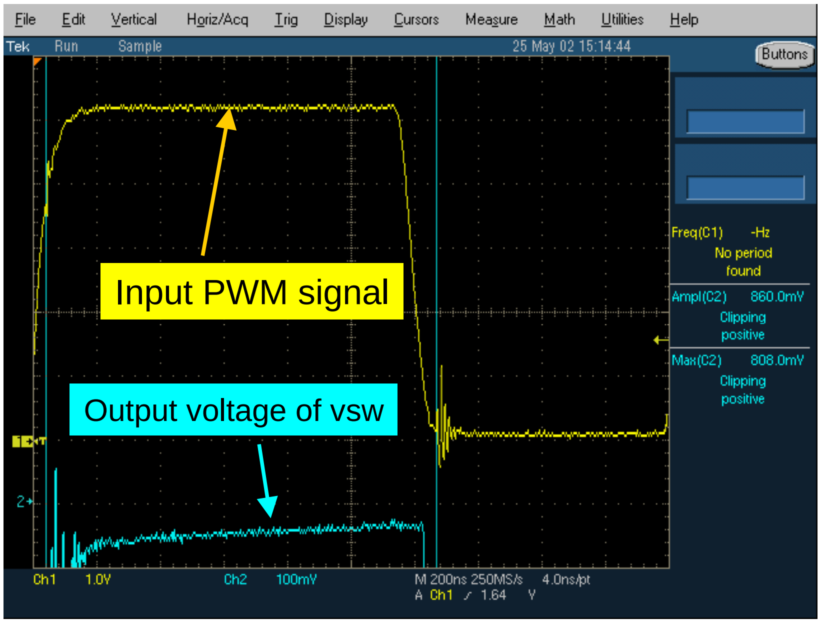


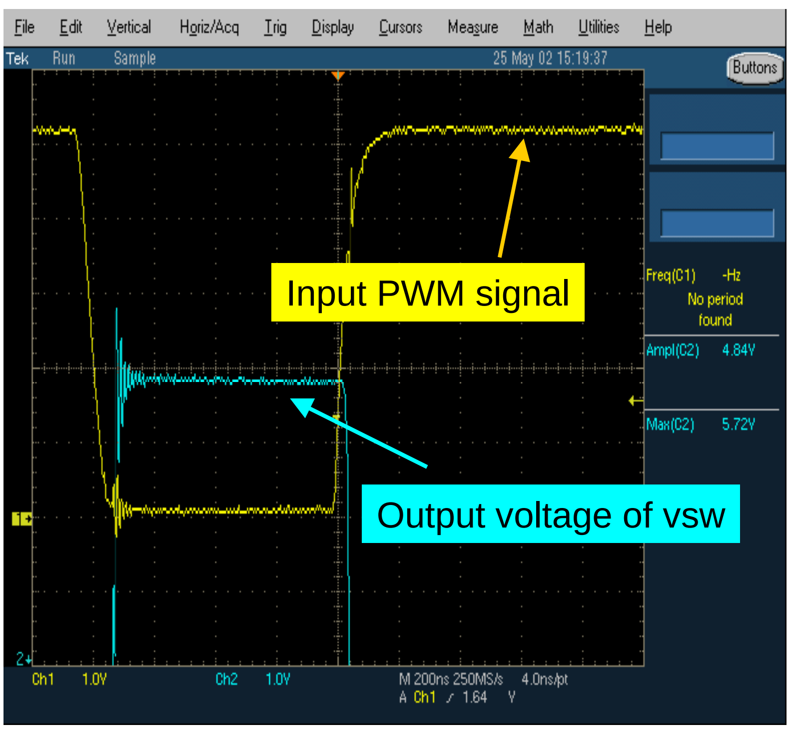
Fig. 5.29 Measured efficiency V_{in}=12V @1MHz



V_{in} = 5V
V_o = 1.75 V
I_o = 1A

V_{dslo} = 45 mV
R_{dslo} = 45 mΩ
Designed value
= 21.7 m Ω

Fig. 5.30 Switching waveforms of the low-side MOSFET



V_{in} = 5V
V_o = 1.75 V
I_o = 1A

V_{dshi} = 180 mV
R_{dshi} = 180 mΩ
Designed value
= 45.4 mΩ

Fig. 5.31 Switching waveforms of the high-side MOSFET

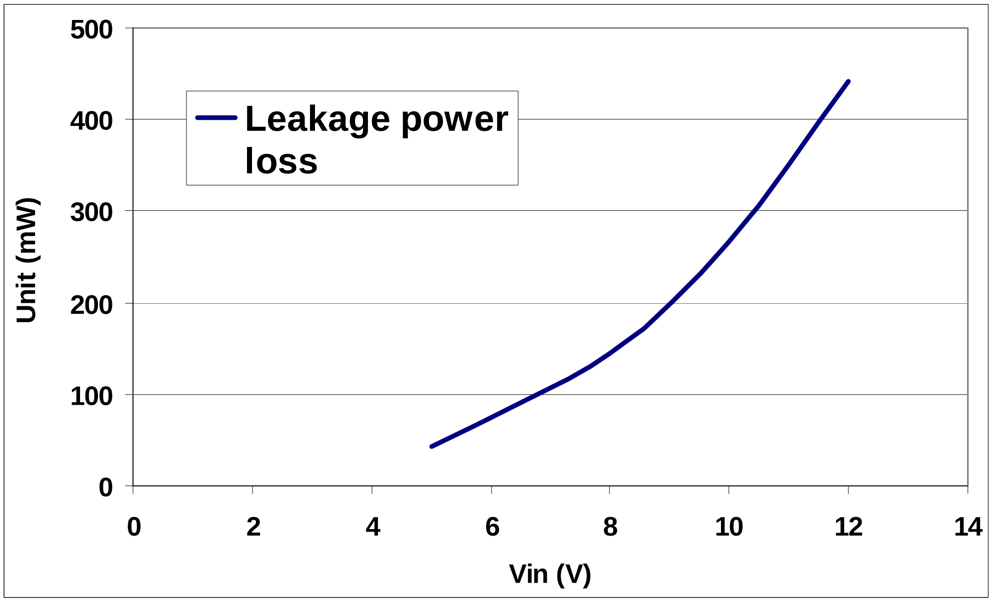


Fig. 5.32 Leakage power loss

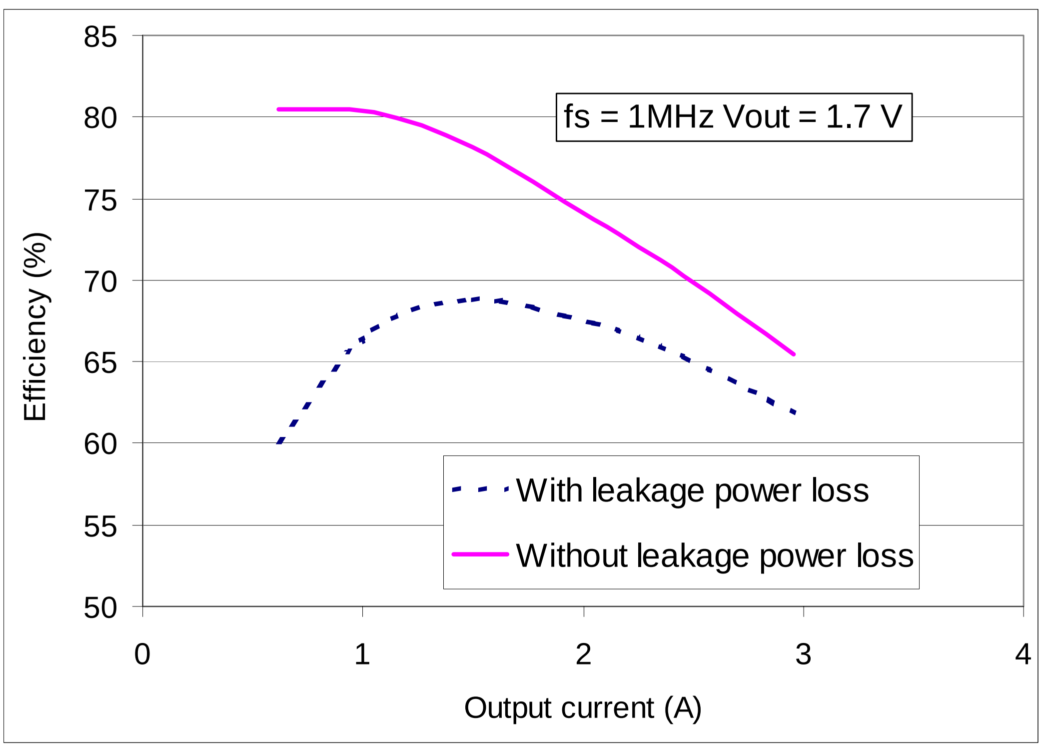
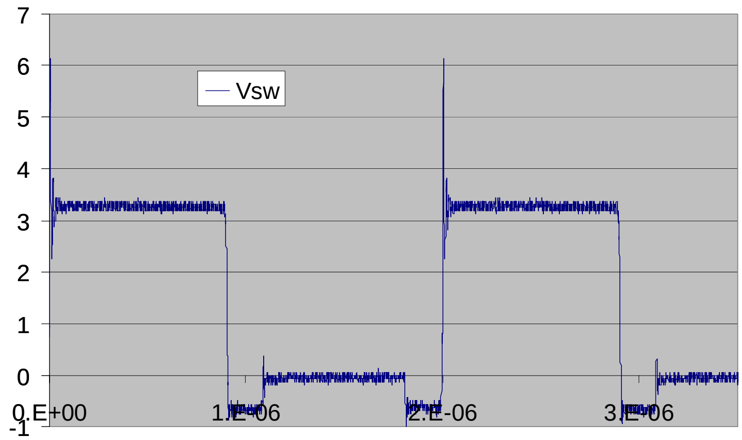
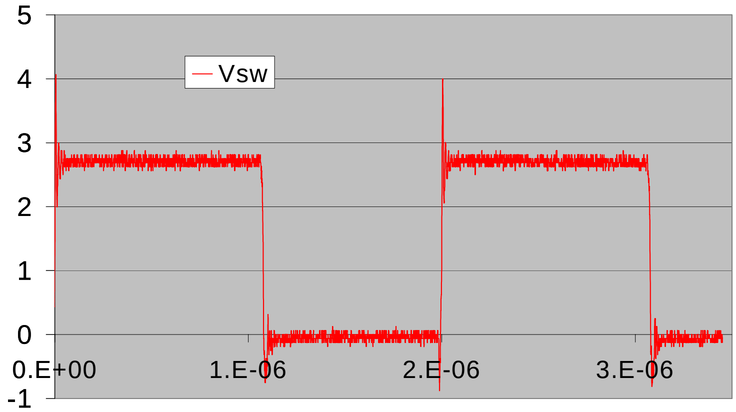


Fig. 5.33 Efficiency without the leakage power



Fixed deadtime



Enable deadtime control

Fig. 5.34 Experimental results of the adaptive deadtime control

Chapter 6 Optimization of the MOSFET for the Buck Converter

To increase the speed and decrease the power consumption of microprocessors, the on-board DC-DC converter that powers the microprocessor must operate with high efficiency. Although much effort has gone toward improving the performance of the converter through novel topologies and advanced power devices [A25]-[A31], a way to optimize the power MOSFET based on a specific device technology is not well known [A32]-[A35]. This kind of an optimization plays an important role in the world of production, because a small change in the performance and cost can mean the difference between success and failure for a business. Conventionally, the MOSFET is optimized by a trial-and-error method [B26]. This approach not only costs money and time, but also never clearly shows whether or not device really reaches its optimum point.

The effects of various MOSFET design parameters on the efficiency of the buck converter are studied by FEA in Chapter 4. In this chapter, the conclusions of chapter 4 are employed in the optimization of the MOSFET for discrete applications. The mixed-mode simulator and the optimization approach are verified by experimental results.

6.1 PWM-Optimized Power MOSFET

The mathematical definition of optimization is to obtain the best possible design properties by changing the setting of independent variables in a continuous manner. Usually, there are two criteria in the optimization: one is the design target to be optimized, and the other criterion is the constraint on the design. Algebra, calculus and the calculus of variations are widely used in classic optimization. However, in finite element analysis, optimization is more difficult, because it takes a significant amount of time to evaluate the effect of the variable on the design target. This can make the iterative optimization excessively time consuming. The design variables of the power MOSFET identified and discussed in the Chapter 4 by FEA simulation are as follows.

- Trench width (W_t)

- Mesa width (W_m)
- Gate oxide thickness (T_{ox})
- The separation between the bottom of the trench and the bottom of the P-body (Ovp).
- Doping concentration of the drift region (N)
- Voltage rating of the power MOSFET (BV)
- Threshold voltage (V_t)
- Area of the MOSFET (AA)

Because both the high-side MOSFET and the low-side MOSFET have these variables, there are a total of 16 variables in the optimization. Considering the process simulation, which may take an hour longer than the mixed-mode circuit simulation, the total simulation time for evaluating the effect of a single variable is about 1.5 hours. Although the traditional optimization approach is a possible solution, from the engineering standpoint, a more efficient way is preferred.

The relationship between the efficiency (E) of the buck converter and the MOSFET design variables can be expressed as

$$E = F(X_1, X_2, X_3, ..., X_n)\,. \tag{6.1}$$

In the practical variable range, all theses variables can be further classified into two types, which are described as follows:

[a]
$$\frac{\partial E}{\partial X_a} > 0 \;\text{ or }\; \frac{\partial E}{\partial X_a} < 0 \tag{6.2}$$

The efficiency is a monotonic function of the [a]-type variable. Such variables include the following.

- Trench width (W_t) of both the high-side and the low-side MOSFET.

Fig. 4.12 and Fig. 4.24 demonstrate that a narrow trench is preferred for both the low-side and high-side MOSFETs. The minimum value of W_t is limited by the photolithography and etching techniques. For the state-of-art technology, W_t can be as small as 0.2 um.

- Mesa width (W_m) of the high-side MOSFET.

Fig. 4.14 shows that a wider W_m is preferred for higher efficiency. However, wider W_m also results in much greater silicon area required to achieve less than 0.5% more efficiency. Therefore, the selection of the mesa width is a tradeoff between cost and performance.

- Mesa width (W_m) of the low-side MOSFET.

Fig. 4.25 shows that at 300KHz switching frequency, 2.0um W_m yields the highest efficiency. However, because the maximum device area is limited by the package and by the number of devices used as the low-side MOSFET, the maximum device area is less than 25 mm^2. Therefore, actually, the smaller W_m is preferred for both 300KHz and 1MHz switching frequencies. In addition, the minimum value of Wm is limited by the contact-masking misalignment tolerance. For the commercial modern MOSFET, W_m is more than 1 um.

- Gate oxide thickness (T_{ox}) of both the high-side and the low-side MOSFET.

As shown in Fig. 4.16 and Fig. 4.26, a thinner T_{ox} is required for higher efficiency, although this will lead to larger FOM (Fig. 4.15). The minimum value of T_{ox} is constrained by the voltage rating of V_{gs}, the typical value of which is about 12 V for the 5V gate-to-source voltage.

- Doping concentration of the drift region (N) of both the high-side and the low-side MSOFET

Fig. 4.20 and Fig. 4.28 show that the non-punch-through design is the best in terms of efficiency. Therefore, the doping concentration of the drift region should be as high as possible, as long as it can satisfy the breakdown voltage.

[b]
$$\left.\frac{\partial E}{\partial X_b}\right|_{X_b = X_{bi}} = 0 \qquad (6.3)$$

This type of parameter plays an important role in the efficiency and should therefore be optimized, because the maximum E occurs at

$$\frac{\partial E}{X_{b1}} = \frac{\partial E}{X_{b2}} = \frac{\partial E}{X_{b3}} = ... = \frac{\partial E}{X_{bN}} = 0\,. \qquad (6.4)$$

The following design parameters can be identified as [b]-type variables.

- Ovp of both low-side and high-side MOSFET

As shown in Fig. 4.18 and Fig. 4.27, the optimum value of Ovp is about zero. And this value is valid for both the high-side and the low-side MOSFETs at different switching frequencies.

- Voltage rating (BV) of both the low-side and high-side MOSFET

Fig. 4.21 and Fig. 4.29 show that the 30V BV is a good candidate for use in the 20V-input DC-DC converter.

- Threshold voltage of both the low-side and high-side MOSFETs

As shown in Fig. 4.23 and Fig. 4.30, the low-side and high-side MOSFETs have different optimized threshold voltages. The minimum value of the threshold voltage is limited by the noise immunity requirement of the circuit.

- Device area of both the low-side and high-side MOSFETs

Actually, device area is the most important design parameter of the MOSFET, because it is directly related to the cost of the device. As shown in the simulation results presented in Chapter 4, there is always an optimized area for both the low-side and the high-side MOSFETs. Assuming Aop is the optimized area, if the designed device area is larger than Aop, this design is a failure, because the extra device area (A - Aop) decreases efficiency; if the designed device area is less than Aop, there is generally a tradeoff between the efficiency and the device area.

Table 6.1 A summary of the PWM-optimized MSOFET.

Design parameter		Design trend	Comment
Trench width (W_t)	Hi-MOS	Narrower	Limited by litho and etching techniques
	Lo-MOS	Narrower	
Mesa width (W_m)	Hi-MOS	Wider	Tradeoff btw cost and E
	Lo-MOS	Narrower	Limited by misalignment
Gate oxide thickness (Tox)	Hi-MOS	Thinner	Limited by the voltage rating of Vgs
	Lo-MOS	Thinner	
Doping concentration of the drift region (N)	Hi-MOS	Non-punch-through	Limited by the breakdown voltage
	Lo-MOS	Non-punch-through	
Spr btw trench btm & P-body btm (Ovp)	Hi-MOS	Optimized	Optimized value is close to zero
	Lo-MOS	Optimized	
Breakdown voltage (BV)	Hi-MOS	Optimized	For 20V input, 30 V is close to optimized value.
	Lo-MOS	Optimized	
Threshold voltage (V_t)	Hi-MOS	Optimized	Lowest V_t is limited by the noise immunity capability.
	Lo-MOS	Optimized	
Device area (AA)	Hi-MOS	Optimized	Most important design parameters
	Lo-MOS	Optimized	

Traditionally, the PWM-optimized MOSFET means that the FOM is reduced by fine-tuning the design variable of W_t, W_m, Ovp and T_{ox}. However, there are two disagreements between the design trends for the minimized FOM and maximized efficiency.

- Gate oxide thickness.

Fig. 4.15 shows that thick gate oxide is needed to achieve less FOM. However, Fig. 4.16 and Fig. 4.26 show that the thinner gate oxide is preferred for higher efficiency.

- The mesa width of the low-side MOSFET

Fig. 4.15 shows that wider mesa is needed to achieve less FOM. However, because the maximum device area is limited by the package type and the number of MOSFETs used in the circuit, a narrower mesa is better. In fact, the efficiency is not sensitive when the mesa width ranges from 1.0 um to 1.5 um.

Table 6.1 lists the design trends for various parameters of both the high-side and low-side MOSFETs for 20V input voltage and 300KHz switching frequency. If we assume that the optimized parameters of the MOSFET structure are independent of the other design variables, then the PWM-optimized MOSFETs have the following features.

- Narrower trench.
- Thinner gate oxide.
- Non-punch-through design of the drift region.
- Zero separation between the bottom of the trench and the bottom of the P-body.
- Narrower mesa of the low-side MOSFET.
- Wider mesa of the high-side MOSFET.

6.2 Optimization Based on PWM Optimized Power MOSFET

Two optimization procedures are described in this section. The first one uses the traditional Hooke-Jeeves algorithm; the second uses a decoupling method to decrease the simulation time.

6.2.1 Optimization Using Hooke-Jeeves Algorithm

The Hooke-Jeeves algorithm is a traditional optimization method for multi-variable problems. Basically, this approach starts from the initial condition and searches for the correct direction of each variable's variation. If the direction is good, it will increase the variation step. Otherwise, it searches for the direction again until it meets the criteria.

Fig. 6.1 shows the optimization procedure of the MOSFET. There are four function blocks in Fig. 6.1 as follows.

- The Mixed Mode Circuit Simulator is the circuit simulator, which uses an FEA model for the two power MOSFETs and a Pspice model for the driver. The FEA models are generated by the block of the Device Simulator. The device areas are given by the block of Performance Evaluation and Procedure Control.
- The Device Simulator performs the device simulation, providing basic electrical characteristics of the MOSFET.
- The Process Simulator inputs parameters that are controlled by the Performance Evaluation and Procedure Control block.
- The Performance Evaluation and Procedure Control calculates the efficiency of the circuit and determines how to try the next variable value. It feeds the MOSFET design parameters to the Process Simulator block and the device area data to the Mixed-Mode Circuit Simulator block

As an example, the optimization can be performed using the device area (A_{hi}) and P-body doping (P_{bdhi}) of the high-side MOSFET, and the device are (A_{lo}) and P-body doping (P_{bdlo}) of the low-side MOSFET. The final result obtained by using the Hooke-Jeeves algorithm is shown in Fig. 6.2, where the starting conditions are V_{thi}=1.24 V, A_{hi}=2.4mm^2, V_{tlo}=1.86 V, A_{lo}=4.8mm^2, and E=83.51% and the optimized results are V_{thi}=1.51V, A_{hi}=1.2mm^2, V_{tlo}=2.12 V, A_{lo}=7.44mm^2, and E=85.89%. The optimization process results in an optimized device area with higher efficiency.

6.2.2 Optimization Using Decoupled Loops

The preceding optimization process can be realized, but it takes a long time to run the whole simulation cycle. Assume the time needed for the mixed-mode circuit simulation is T_0, and the process simulation takes KT_0 (usually process simulation takes much longer than the circuit simulation, and K>>1): if only the device area is changed, it will take T_0 to reach a new value of the target function. However, if the P-body dose is changed, it will take $(K+1)T_0$ to run the process simulation. For the example shown in Fig. 6.2, half of the simulation steps are the process simulation. The total simulation time is about $31(K+1)T_0$ (for P-body change)+$31T_0$ (for area change), and most of time ($31KT_0$) is spent on the process simulation.

Therefore, we need to find another algorithm that spends less time on the process simulation. Because the loss of the high-side MOSFET (P_{hi}) consists of turn-on loss, turn-off loss and conduction loss, the parameters A_{lo} and V_{tlo} do not greatly affect the P_{hi}. Therefore, A_{hi} and V_{tlo} can be optimized first, and then A_{lo} and V_{tlo} can be optimized. As proposed in Fig. 6.3, because the optimization of the threshold voltage is placed at the outer loop, the number of the process simulation is minimized in order to save computation time. One optimization example is shown in Fig. 6.4, and the optimized results are V_{thi}=1.40V, A_{hi}=0.95mm^2, V_{tlo}=1.97 V, A_{lo}=6.18mm^2, and E=85.87%. Compared to the results found by the Hooke-Jeeves method, the efficiency is almost the same. Although it takes more steps for the optimization, the total computation time is actually reduced by 30%, because most of the steps are spent on the circuit simulation.

6.3 A Design Example and Experimental Results

So far, all the discussion and conclusions are based on the simulation results. In this section, a design example is presented to answer two fundamental questions.

- How accurate is the FEA model?
- Is the design guideline of the PWM-optimized MOSFET described in sedction 6.1 correct?

The first question can be answered by a comparison between the simulation and experimental results. The second question is answered by comparing the efficiency with the most recently released product from one of the major suppliers (R company) of low-voltage MOSFET for the notebook application.

6.3.1 Design Background

Since the efficiency of the buck converter depends not only on the performance of the power MOSFET but also on other factors, the design environment should be defined and justified before the optimization of the power MOSFET.

- Selection of driver

The driver of the power MOSFET plays an important role in the optimization of the MOSFET, because the switching loss of the high-side MOSFET and the deadtime power loss of the low-side MOSFET are directly related to the characteristics of the driver. Currently, there are two major suppliers of the driver for the notebook application. They are MAXIM and INTERSIL. This design uses MAX1718 as the driver/controller, and the efficiency tests are performed on the commercial efficiency evaluation board MAX1718MS.

- Switching frequency

MAX1718 supports four switching frequencies: 200, 300, 550 and 1,000 KHZ. The 300 KHz is selected as the design parameter, because it is still widely used in the industry. The efficiency at higher switching frequencies is also tested, and will be presented in this chapter.

- Input voltage

The input voltage has a substantial impact on the switching loss of the high-side MOSFET. In the notebook application, the highest input voltage is 20 V. This is the worst case in terms of the switching loss; therefore, 20 V is selected as the design parameter.

- Output voltage

The output voltage of MAX1718 ranges from 0.6 V to 1.75 V. 1.3 V is selected as the design parameter.

- Load current

Load current affects not only the switching loss of the high-side MOSFET, but also the conduction loss of both MOSFETs. The 20 A for each phase is usually used to compare efficiency.

For a long time, R company's products have dominate the market of the high-side MOSFET for the notebook application, while the most popular low-side MOSFETs are provided by the S company. This design focuses on the optimization of the high-side MOSFET using S company's device (SL) as the low-side MOSFET.

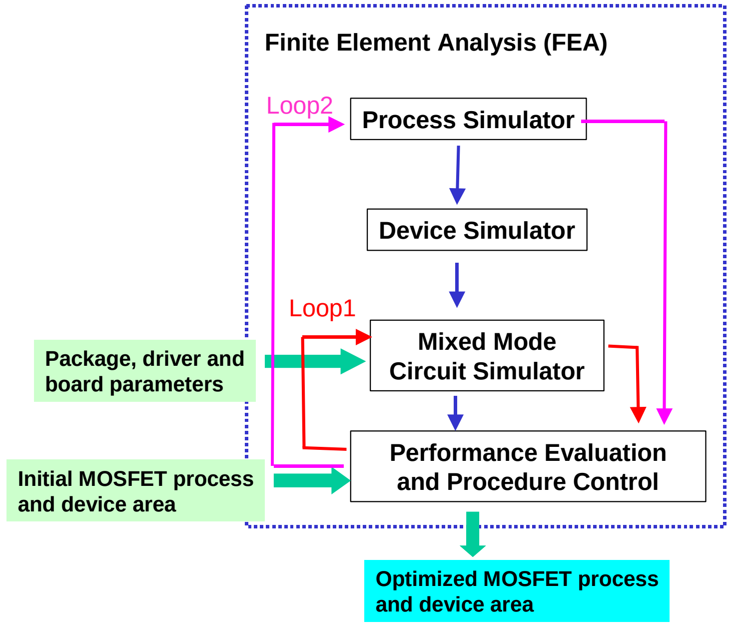


Fig. 6.1 General optimization procedure

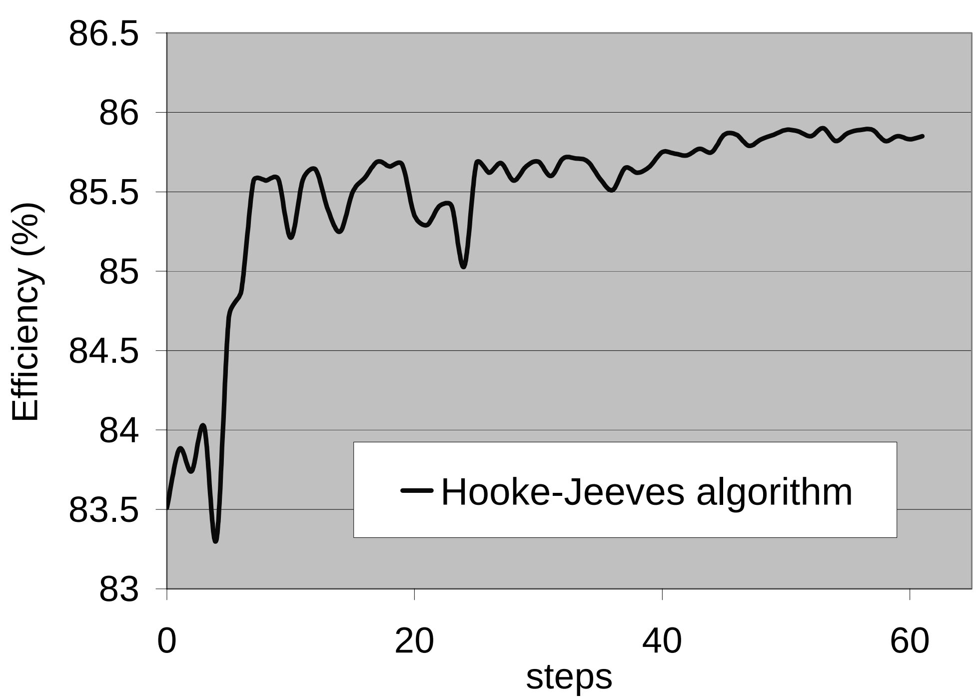


Fig. 6.2 An optimization example using Hooke-Jeeves algorithm

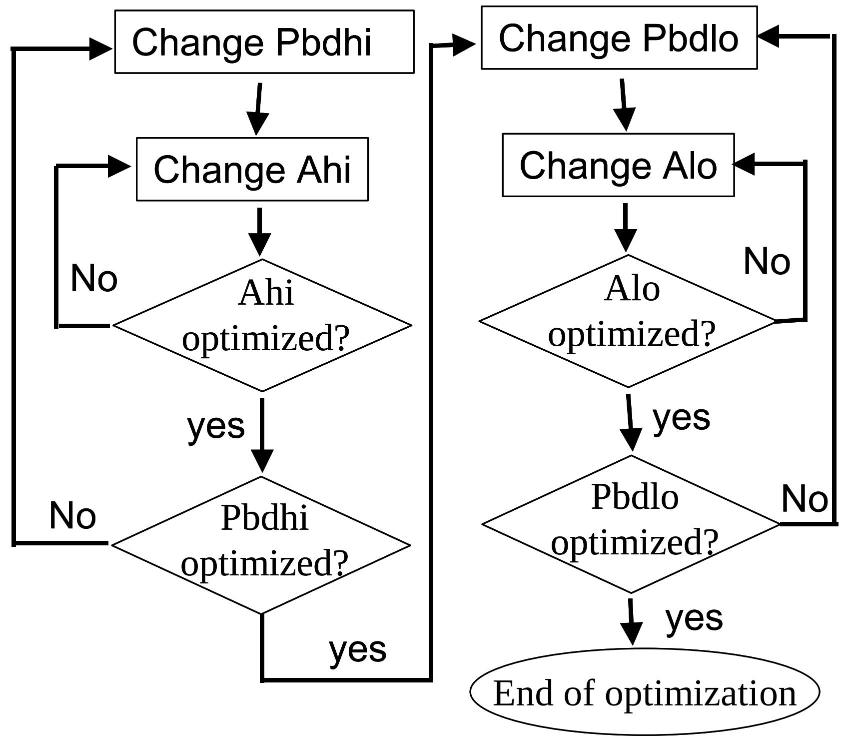


Fig. 6.3 Optimization using decoupled method

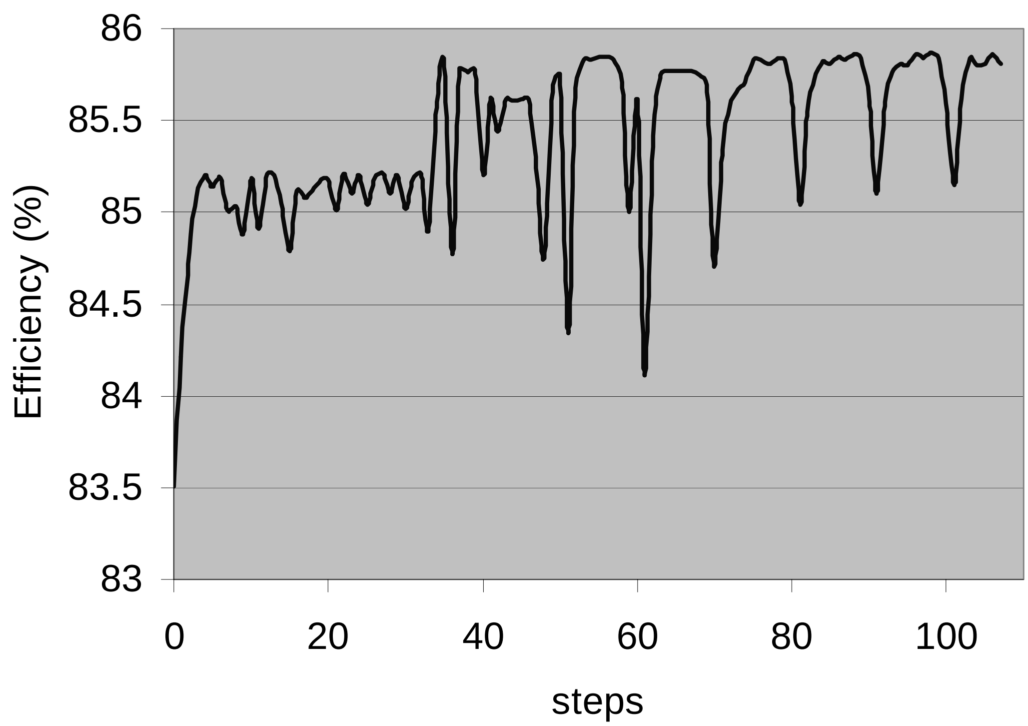


Fig. 6.4 An optimization example using decoupled method

6.3.2 Design Procedure

Some optimization approaches are presented in section 6.2. Actually, the design procedure can be rather flexible as based on PWM-optimized MOSFET, because a tradeoff between the device area and the performance exists in the design of the high-side MOSFET. As addressed in section 6.2, the wider mesa is preferred for higher efficiency. However, in order to achieve 1% higher efficiency, the area of the MOSFET may double. Therefore, instead of using the maximum device area for the highest efficiency, the device areas are optimized based on two different mesa widths, which are selected for the purposes of cost reduction with a narrower mesa (high-density), and higher efficiency with a wider mesa (low-density).

The simulated efficiency is shown in Fig. 6.5. In the efficiency calculation, a fixed magnetic loss is used for the filter inductor. Although this value can substantially affect the absolute efficiency value, it has trivial influence on the optimization of the MOSFET. On the other hand, the magnetic loss is also almost independent of the power MOSFET, because its loss is determined by both the current and the switching frequency.

In Fig. 6.5, the H design is selected for the purpose of low cost. If the device area is less than H, there is a dramatic drop in efficiency. However, the L design is selected for the purpose of high efficiency.

6.3.3 Experimental Results and Discussion

In order to minimize the error of the efficiency test, the measurement is controlled by the computer. For each test point, a duration of five minutes is used for the burn-in time to make sure the circuit and the operation temperature reach the steady state. Then, the input voltage, input current, output voltage and output current are sampled every 30 seconds. After eliminating the three minimum and three maximum values of the data, the efficiency is calculated using the average value by

$$\eta = \frac{\overline{V_{out}} \times \overline{I_{out}}}{\overline{V_{in}} \times \overline{I_{in}}}. \qquad (6.5)$$

The experiment shows that the error of the efficiency is within 1%. The gate loss is not included in the optimization and the test, because of the following.

- The gate loss is much less than the conduction and switching losses at 300 KHz.
- It is unlikely that the gate loss can be accurately measured, because it is not easy to separate the gate loss from the driver loss.
- Currently, for the notebook application, industry does not consider the gate loss in the efficiency measurement.

Fig. 6.6 compares the simulated and measured efficiencies of the H and L designs at switching frequencies of 300 KHz and 500 KHz. Good agreements are achieved at both frequencies.

Fig. 6.7 summarizes the efficiency and the device area at the two switching frequencies. The design target is achieved at 300 KHz by the L design in terms of the performance. Compared to R, H is still a better design, because its area is less than one-third of R, while the efficiency is only lower by 0.1%. At 500 KHz, designs H and L beat R in terms of both cost and performance.

The experimental results demonstrate that the design based on the PWM-optimized MOSFET, using the mixed-mode simulation is successful.

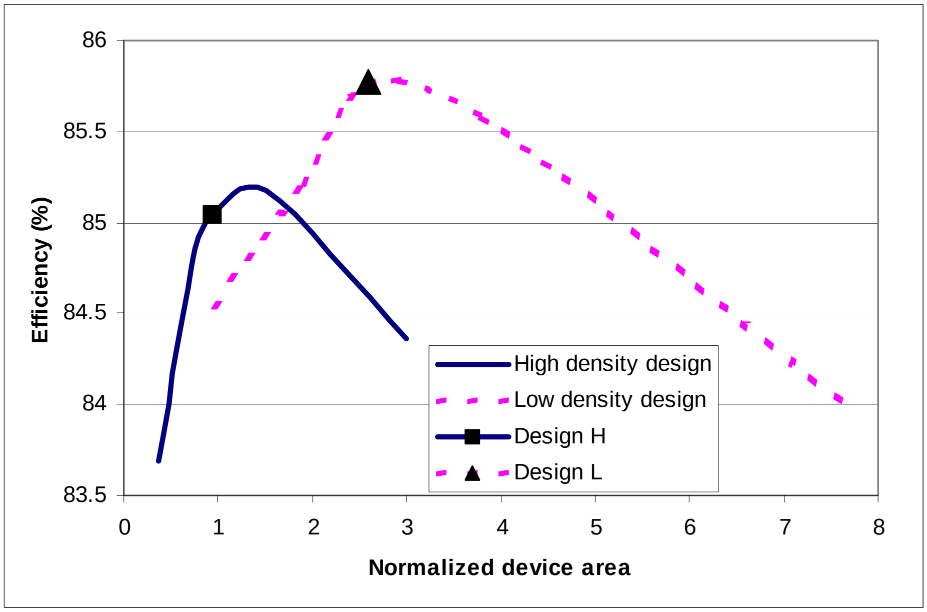


Fig. 6.5 Simulated efficiency of the design.

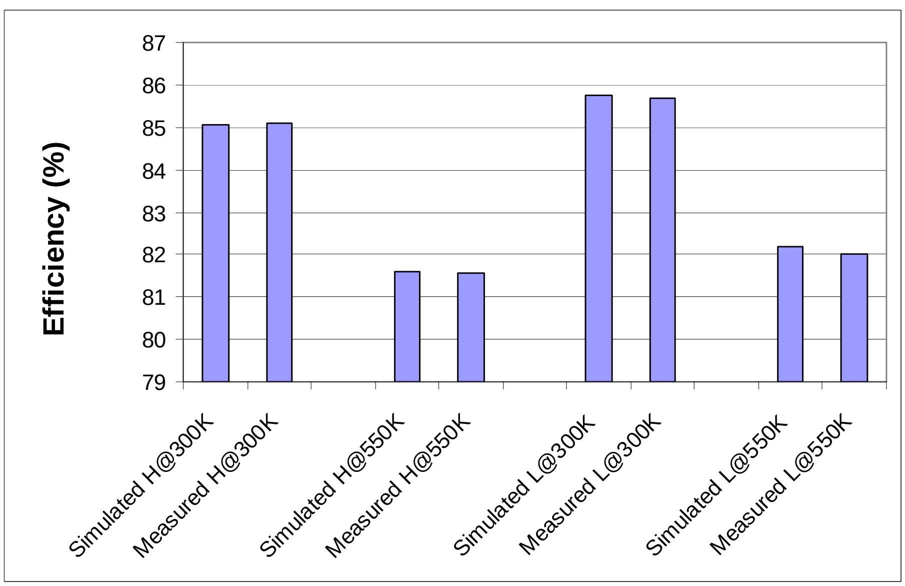


Fig. 6.6 Comparison of the measured and simulated efficiency at full load.

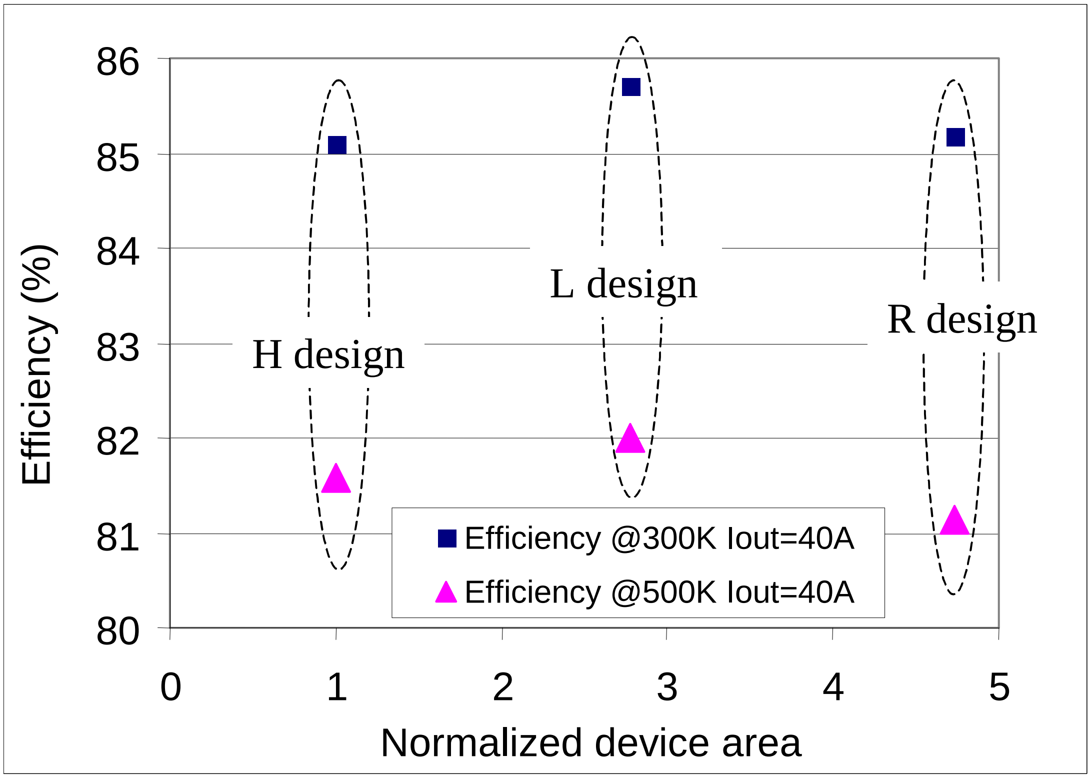


Fig. 6.7 Comparison of the efficiency and device area.

Chapter 7 Conclusions and Future Work

7.1 Conclusions

In the high-frequency DC-DC buck converter, which is the required voltage supply of microprocessors, the performance of the power MOSFETs (including the high-side MOSFET and the low-side MOSFET) can not be accurately predicted by traditional analytical models, because the parasitic elements of the package and the PCB and nonlinear characteristics of the power MOSFETs play a more important role in the switching process. The complexities of both the turn-on and the turn-off processes of the high-side MOSFET and the possible spurious turn-on loss of the low-side MOSFET are demonstrated in this dissertation. In order to achieve good MOSFET design, the FEA model must be employed in the evaluation of various losses associated with the power MOSFETs.

Although FEA has long been widely used in semiconductor modeling, it has not been employed in the buck converter due to the convergence problem and the long simulation time needed for the circuit to reach the steady state. In this dissertation, the convergence problem is solved by setting the initial voltage and current of the buck circuit to zero and then ramping the voltage and current up to the desired values; the simulation time is reduced by using the current source instead of LCR network as the load; hence, the circuit can avoid the transient process and can immediately enter the stead state. With the help of the power loss extraction program, both the detailed power loss information for the MOSFET and the parasitic elements can be determined quickly and conveniently. This FEA method not only takes into account the nonlinear effect of the MOSFET, the driving capability of the controller/driver, and the major parasitic components of the circuit, but also directly links the power loss of the MOSFETs to the device structure and the device technology.

The design trends of PWM-optimized MOSFETs are studied by extensive simulation. The major tradeoff between cost and performance is identified. Finally, a successful design is demonstrated. Compared with the mainstream commercial MOSFET, the design not only has small device area (low cost), but also has higher efficiency at its designed operation condition. Therefore, the proposed FEA method provides a novel methodology for the PWM-optimized MOSFETs.

7.2 Summary of Research Contributions

This dissertation is dedicated to the optimization of the low-voltage MOSFET used in the high-frequency buck converter. Besides the high precision FEA model, several other novel models are developed to achieve greater understanding if the dynamic process of both the high-side and the low-side MOSFETs. In addition, the feasibility of monolithic integration of the buck converter is investigated in terms of the process and device optimization.

The major research contributions associated with this dissertation are listed below.

- A novel model for MOSFET switching loss calculation. This model describes the effect of the parasitic inductance on the switching process.
- A novel model for the dt/dv induced spurious turn-on voltage. This model takes into account the parasitic inductance in the analytical solution.
- A novel model for Q_{gd} calculation. This model describes the influences of the gate oxide and the doping condition of the drift region on the Q_{gd}. Ignoring the parasitic inductance, the turn-on and turn-off loss processes of the power MOSFET can be predicted by this model.
- The FEA model is applied to the simulation of the buck converter. By solving the convergence problem and dramatically reducing the simulation time, the switching performance of the power MOSFET in the buck converter is extensively studied. The design trench of the PWM-optimized power MOSFETs are identified.
- Based on the FEA simulation, different optimization approaches of the MOSFETs are studied and verified experimentally by a successful MOSFET design for the notebook application.

- An economical 5V/20V CMOS-compatible power IC process is proposed. The isolation capability and the device performance are demonstrated experimentally.
- A novel adaptive deadtime control method for the monolithic integrated buck converter can detect the two deadtimes in one switching cycle, and is absolutely compatible with the power IC process.

7.3 Future Research Directions

In this dissertation, the application of the FEA model focuses on the optimization of the traditional power UMOSFET used in the synchronous buck converter for the personal computer. However, this technique can be extended to other research areas as the follows.

(1) System optimization.

The optimization of the MOSFET strongly depends on its operation conditions. Although for a MOSFET designer, the operation conditions are fixed, from the system standpoint, these variables are subject to change. Examples of these variables include the input voltage of the buck converter, the gate driving voltage of the MOSFET, etc. Now, these parameters can be determined more accurately.

(2) Evaluation of new circuit topologies.

Besides the traditional synchronous buck converter, there are other topologies [D17]-[D19] for the high-frequency DC-DC application. After proper modification of the circuit, the FEA model also can be used to calculate its power loss and to help select the MOSFET. In addition, the advantage of the new idea can be verified more academically.

(3) Evaluation of new device structures.

Although the UMOSFET is the most popular power device adopted by the high-frequency DC-DC converter, other device structures [A6],[A7], [A36]-[A40] are also potential candidates. Because the FEA model is directly based the physical structure of the device, this method can be conveniently used to investigate the switching performance of other devices.

Therefore, not only the device designer, but also the circuit and system engineers, can benefit from the new simulation method proposed in this dissertation. I hope my approach can contribute to these areas in the near future.

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Appendix A Equivalence of $\frac{dQ}{dV}$ and $\frac{\varepsilon_{si}}{W_d}$ in the Calculation of Depletion Region Capacitance

In this appendix, the equivalence of $\frac{dQ}{dV}$ and $\frac{\varepsilon_{si}}{W_d}$ are demonstrated for both non-punch-through and punch-through type of silicon. The general definition of the capacitance is

$$C = \frac{dQ}{dt} \tag{A1}$$

1. For the non-punch-through type silicon

The depletion width of the non-punch-through type silicon is

$$W_d = \sqrt{\frac{2\varepsilon_{si} V_{si}}{qN}} \tag{A2}$$

Then, the charge in the depletion region is

$$Q_d = qNW_d = \sqrt{2qN\varepsilon_{si} V_{si}} \tag{A3}$$

Using the general definition of the capacitance, we have

$$C = \frac{dQ_d}{dV_{si}} = \sqrt{\frac{qN\varepsilon_{si}}{2V_{si}}} = \frac{\varepsilon_{si}}{W_d} \tag{A4}$$

where W_d is expressed in the Equation (A2).

Equation (A4) shows $\frac{dQ_d}{dV_{si}}$ is equivalent to $\frac{\varepsilon_{si}}{W_d}$ in the capacitance calculation for non-punch-through type silicon.

2. For the punch-through type silicon

The slope of the electric filed in the depleted silicon is determined from Poisson's Equation, which, for a one-dimensional analysis, is

$$\frac{dE}{dx} = \frac{qN}{\varepsilon_{si}} \tag{A5}$$

Therefore, the voltage sustained by the silicon is

$$V_{si} = E_2 L_n - \frac{qNL_n^2}{2\varepsilon_{si}} \tag{A6}$$

where L_n is the width of the drift region.

Using Gauss's law, the total charge is

$$Q = \varepsilon_{si} E_2 = \frac{\varepsilon_{si} V_{si}}{L_n} + \frac{qNL_n}{2\varepsilon_{si}} \tag{A7}$$

Because Since L_n is constant, we have

$$\frac{dQ}{dV_{si}} = \frac{\varepsilon_{si}}{L_n} \tag{A8}$$

Since, in the punch-through type silicon, the depletion width is equal to the width of the drift region, we can conclude that $\frac{dQ}{dV}$ and $\frac{\varepsilon_{si}}{W_d}$ are equivalent for both non-punch-through and punch-through type of silicon.

Vita

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