Transceiver Design for Ultra-Wideband Communications

by

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Abstract

Despite the fact ultra-wideband (UWB) technology has been around for over 30 years, there is a newfound excitement about its potential for communications. With the advantageous qualities of multipath immunity and low power spectral density, researchers are examining fundamental questions about UWB communication systems. In this work, we examine UWB communication systems paying particular attention to transmitter and receiver design.

This thesis is specifically focused on a software radio transceiver design for impulse-based UWB with the ability to transmit a raw data rate of 100 Mbps yet encompasses the adaptability of a reconfigurable digital receiver. A 500 ps wide Gaussian pulse is generated at the transmitter utilizing the fast-switching characteristics of a step recovery diode. Pulse modulation is accomplished via several stages of RF switches, filters, and amplifiers on a fully designed printed circuit board specifically manufactured for this project. Critical hardware components at the receiver consist of a bank of ADCs performing parallel sampling and an FPGA employed for data processing. Using a software radio design, various modulation schemes and digital receiver topologies are accommodated along with a vast number of algorithms for acquisition, synchronization, and data demodulation methods. Verification for the design is accomplished through transmitter hardware testing and receiver design simulation. The latter includes bit error rate testing for a variety of modulation schemes and wireless channels using a pilot-based matched filter estimation technique. Ultimately, the transceiver design demonstrates the advantages and challenges of UWB technology while boasting high data rate communication capability and providing the flexibility of a research testbed.

Acknowledgements

Throughout my life I have found there are several constants, which I feel should be acknowledged first and foremost because without these things, I would not be writing this thesis. The most significant comes in the form of my Almighty Savior, Jesus Christ, who has not only given me the strength and ability to achieve my goals, but has surrounded me with the greatest family, friends, and professional colleagues. If there is one thing I have learned in my adult life, it is that "for with God all things are possible" (Mark 10:27).

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Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

1.1 Motivation For The Use of Ultra-Wideband

The concept of Ultra-Wideband (UWB) was formulated in the early 1960s through research in time-domain electromagnetics and receiver design, both performed primarily by Gerald F. Ross. Through his work, the first UWB communications patent was awarded for the short-pulse receiver which he developed while working for Sperry Rand Corporation [1]. Throughout that time, UWB was referred in broad terms as "carrierless" or impulse technology. The term UWB was coined in the late 1980s to describe the development, transmission, and reception of ultra-short pulses of radio frequency (RF) energy. Even though the knowledge has been in existence for over thirty years, UWB technology is an emerging research topic in the wireless communications field for a variety of reasons. For communication applications, high data rates are possible due to the large number of pulses that can be created in a short time duration. Due to its low power spectral density, UWB can be used in military applications that require low probability of detection. Other common uses of UWB are in radar and imaging technologies, where the ability to resolve multipath delay is in the nanosecond range, allowing for finer resolution, whether it be from a target or for an image.

After recognizing the potential advantages of UWB, the Federal Communications Commission (FCC) developed a report to allow UWB as a communications and imaging technology. A UWB definition was created as a signal with a fractional bandwidth greater than 0.2 or which occupies more than 500 MHz of spectrum. The fractional bandwidth is defined as $2(f_H-f_L)/(f_H+f_L)$, where f_H and f_L are the upper and lower frequencies, respectively, measured at -10 dB below the peak emission point. To allow government and industry to conduct UWB testing, frequency spectrum from 3.1GHz to

10.6GHz was allocated for communications use below specified power levels, while imaging was limited to below 960 MHz, as seen in Figure 1.1 below. A significant amount of testing will be performed to calculate the amount of interference that UWB causes to narrowband signals. Therefore, until more knowledge is acquired in this area, the FCC established EIRP levels for various ranges of frequencies influenced by pre-existing emitting sources. For indoor systems, the average output power spectral density is limited to -41.3 dBm per MHz, which complies with the long standing Part 15 general emission limits to successfully control radio interference [2].

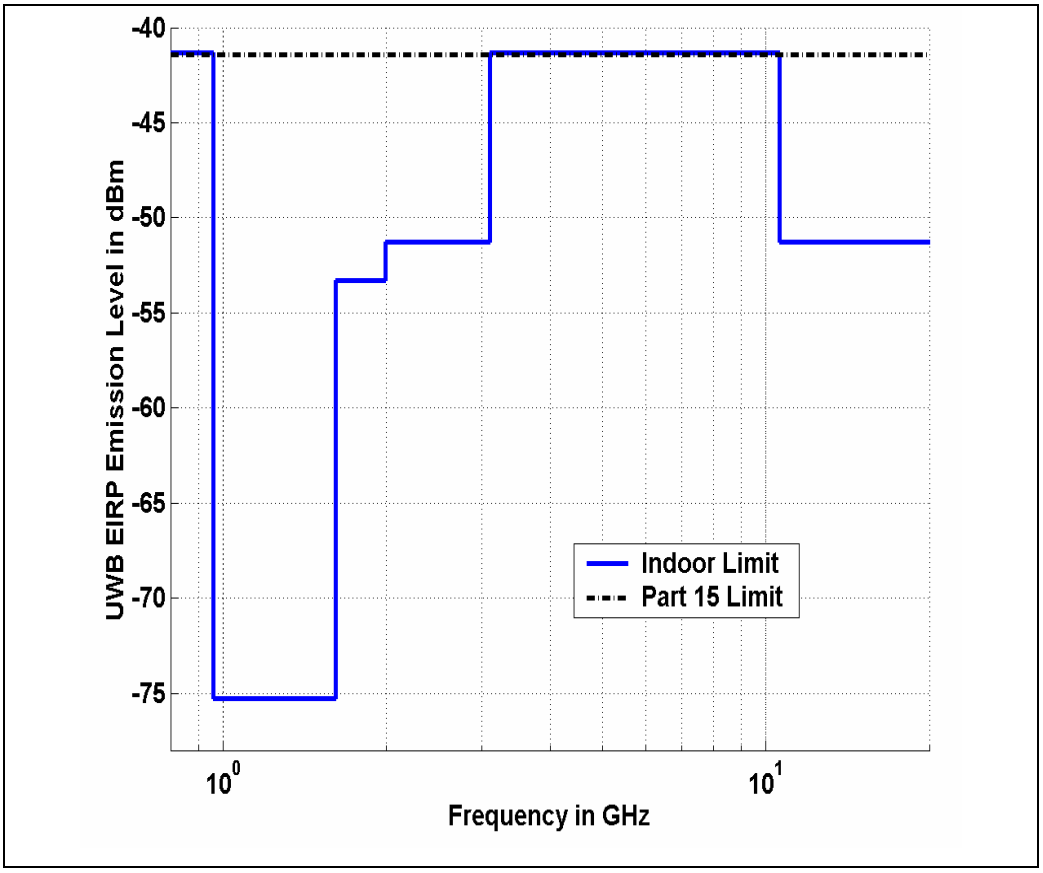


Figure 1.1. FCC Spectral Mask for UWB Indoor Communication Systems [3]

Although the FCC has regulated spectrum and power levels for UWB, there is currently no standard for industry to follow. Discussions have developed on the use of two standards, specifically, multiband orthogonal frequency division multiplexing (OFDM) and direct sequence spread spectrum (DS-SS), which is based on impulse radio technology. The Multiband OFDM alliance and Motorola (DS-SS) are presently

attempting to persuade the IEEE to adopt their respective approach. Each of these schemes has their advantages in a communications system although OFDM is currently a more mature technology. Prior to the recent industry boom with these standards, the most common UWB system implementation was impulse radio, where ultra-short baseband pulses are used with a variety of modulation schemes to transfer data. Impulse radio has various advantages over OFDM, with its ability to penetrate through materials and resolve multipath with path length differences on the order of a foot or less. Impulse radio also allows for lower power consumption with a low duty cycle, making it very beneficial in low probability of detection applications. Numerous multiple access techniques such as time-hopping and direct sequence are commonly applied to impulse radio, giving it the ability to service many users in a network. There are three primary drawbacks to current implementations of impulse radio, namely lack of high data rates, lack of long communication range, and analog components are necessary to construct the system. The primary focus of this thesis is to develop a receiver design that improves all three shortcomings and allows impulse radio to extend into high speed commercial applications, particularly in indoor environments. As will be shown in this design, high data rates with digital processing using impulse radio technology are possible.

1.2 Advantages of Software-Radio Implementation

A number of various receiver design architectures have been examined to investigate UWB communication performance, most of them hardware based. For data demodulation purposes, hardware implementations such as a sampling bridge circuit and a matched filter are frequently used. The primary disadvantage of the sampling bridge circuit is the loss of data rate, as it undersamples the incoming pulse with a sliding sampling position, taking a series of snapshots to produce a final waveform. Therefore, multiple pulses per bit are required to transmit data, limiting the maximum data rate [3]. To perform data demodulation using a matched filter in hardware, an estimated received pulse must be generated at the receiver and correlated with the incoming waveform. A system with this architecture must have a highly stable oscillator and precise timing

accuracy. Other receiver performance improvements, such as a Rake receiver, which is necessary to capture multipath to create adequate signal energy, are difficult to implement using hardware. Multiple correlators are necessary to capture each multipath with a channel estimator running in parallel to detect the time when each correlator should be triggered and to determine channel polarity. Timing accuracy is again an issue when the pulse rate is high, as data processing time and signal propagation delay become problems. Additional drawbacks include extra hardware and the limited number of Rake fingers due to the fixed number of correlators.

Many of the disadvantages using a hardware implementation can be solved by using software-defined, reconfigurable radio concepts. The software-defined radio implementation provides tremendous flexibility compared to a single hardware implementation—providing the capability to utilize one of several different popular UWB modulation schemes. Other benefits of a software radio UWB receiver are the variation of pulse rate, use of multiple receiver topologies, and pilot-based matched filter channel estimation. Pulse rates can adapt to the environment in a transceiver application, where two-way communication is available. Therefore, for a lower bit error rate (BER) in a noisy, dense multipath location, multiple pulses per bit can be sent after the pilot-based matched filter template is formed. In this scenario, a digital matched filter algorithm is necessary to demodulate the data using the pilot-based matched filter template generated in software. An increase in data rate for indoor line-of-sight (LOS) communication is also a possibility. In this case, the software must process data quickly, where a digital threshold detect is very useful. All of these different situations can be controlled more easily in software, which makes a software radio UWB system more adaptable to a variety of real world environments. This type of flexibility led to the UWB system design presented throughout this thesis.

1.3 Project Overview

The overall goal of this project is to create an impulse-based ultra-wideband communication system design based on software-defined/reconfigurable radio concepts. The design objectives for the software-radio UWB system are as follows:

- Raw Data rate of 100 Mbits/second
- Multiple Modulation Schemes: On-Off Keying (OOK), Binary Pulse Position Modulation (Binary PPM), or Biphase Modulation
- Multiple receiver topologies: Digital Leading Edge Detection and Digital Pilot-Based Matched Filter
- Receiver may be upgraded with a software change

It should be noted that these design objectives are solely based on the first generation system, which will be constructed primarily to validate the design and demonstrate an overall proof-of-concept. These design goals will change to increase data rate, transmission range, and modulation schemes when the second generation system is designed. Of course, one primary reason for designing a software-radio UWB system is that the creation of future generations is ideally a software change. With this flexibility, modifications can be made to the system overnight provided there is sufficient processing horsepower, compared to building another hardware configuration.

As for the initial hardware implementation, one specific design goal should be mentioned due to its effect on the design. In order to leverage MPRG's existing experience in board and system-level design, an emphasis was placed on the communication system being implemented using commercially available off-the-shelf (COTS) components. The use of COTS components places some significant constraints on the system, but results in a significant time and resource savings compared to designing a custom integrated circuit.

In addition to the design, the main hardware construction goal was to produce a UWB transmitter with the capability to produce 500 ps wide pulses with the modulation

and pulse repetition functionality discussed in the design objectives. Therefore, the transmitter schematic and printed circuit board (PCB) design were created using the PADS PCB Design Solutions [4] software provided by MPRG. Since MPRG does not have the facilities to assemble multiple layer circuit boards, the transmitter fabrication was performed using an out-of-house PCB manufacturer. Finally, to verify an acceptable pulse waveform and pulse repetition rate, tests on the transmitter output were completed to demonstrate that the transmitter design goals were attained.

Without the time or money to construct the receiver hardware in the immediate future, a system simulation was essential to uncover design flaws and calculate system performance statistics such as BER curves and synchronization performance based on the final system design. Agilent ADS [5] and Matlab [6] were the software tools utilized to perform the necessary simulations. Each software package is known for its RF circuitry and data processing simulation capabilities, respectively. Optimistic results from these simulations help support the overall goal of producing a UWB transceiver capable of high data rates with a software-radio receiver structure.

1.4 Thesis Overview

There are three primary topics of interest discussed in this thesis, including UWB transmitter design and construction, a UWB software-radio receiver design, and a simulation to evaluate the performance of the overall system.

Chapter 2 provides some basic background information on UWB, specifically detailing pulse generation, common UWB modulation schemes, and UWB receiver designs. UWB pulses can be generated with numerous devices, although only the more popular ones are discussed. The second section of the chapter describes the UWB modulation techniques presented in the design, along with some relevant theoretical performance curves. Notes on the three digital receiver topologies, leading edge detection, matched filter, and a pilot-based matched filter, are provided with some additional performance statistics.

A thorough discussion of the transmitter design is given in Chapter 3. The SRD pulse generator, along with schematics, is discussed, as is the remainder of the transmitter components. Additional information such as the design of the DC power supply and on-board data generation is also given. Details of the transmitter schematic, PCB layout, and PCB fabrication are discussed to allow the reader to fully understand the construction process. Finally, results from the pulse sampled in the lab are shown to verify the transmitter design.

The receiver design is described in Chapter 4. COTS limitations and sampling techniques are discussed to assist in validation of the receiver design structure. Several sections are included to explain the hardware design, including the RF, sampling, and data processing segments of the receiver. System aspects such as receiver topologies and the air interface follow the hardware sections to demonstrate the functionality of the overall system. Within the signal processing hardware, considered the backbone of any software-radio design, common communication system responsibilities such as acquisition, synchronization, and data demodulation are performed. The description of these processes is included in Chapter 4, along with the pilot-based matched filter estimation, an essential component of receiver algorithm.

Chapter 5 focuses on receiver design testing through simulation of the system in Agilent ADS and Matlab. The transmitter is replicated in Agilent ADS and the results are stored for Matlab. Matlab performs the system simulation by inserting data and performing the digital processing after sampling the waveform. Each of these procedures, along with the channel details, is described in Chapter 5. Receiver performance statistics from the simulations and the overall results are discussed to conclude the chapter.

The conclusion in Chapter 6 concentrates on the UWB software-radio transceiver design in general and re-emphasizes the encouraging initial results shown in this thesis. Future work is discussed in the conclusion since several design additions and changes are possible. Also included is the work necessary to implement the receiver design.

The references for this thesis directly follow the conclusion. Appendix A contains the schematic and PCB layout for the transmitter for the reader to follow along with the discussion in Chapter 3. Details for the system simulation can be found in

Appendix B where the Agilent ADS schematics and a listing of the Matlab code are located. The vita for the author of this thesis is included in the final section.

Chapter 2 UWB Communications

2.1 Introduction

In this chapter, we present the basic theory behind the use of UWB pulses for communications. Specifically, we discuss the generation and shaping of UWB pulses, the modulation of the resulting pulses, and receiver architectures. Additionally, we briefly discuss signal design for multiple access.

2.2 Ultra-Short Pulse Generation Theory

Before generating an ultra-short pulse, the desired wave shape must be determined for the system. The most popular pulse shape for UWB communication systems is the Gaussian pulse due to mathematical convenience and ease of generation, which is illustrated in Figure 2.1 and can be described by:

$$s(t) = Ae^{-\frac{(t-\mu)^2}{2\sigma^2}} \tag{2.1}$$

where:

A	is the pulse amplitude (volts)
t	is time (seconds)
σ	is the standard deviation of the Gaussian pulse (seconds)
μ	is the mean value of the Gaussian pulse (seconds)

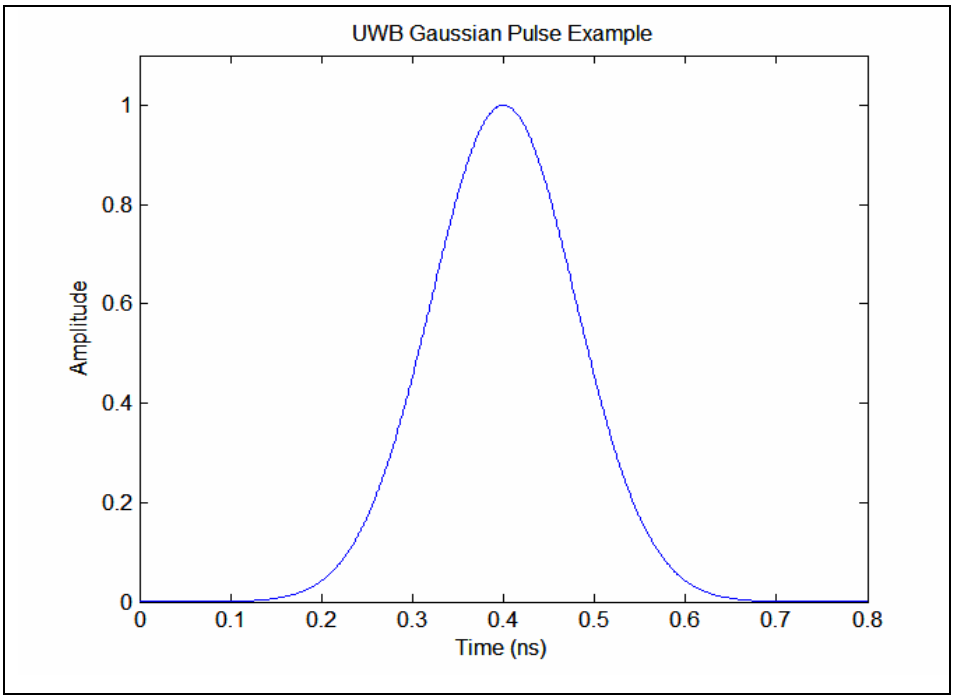


Figure 2.1. UWB Gaussian Pulse Example

The pulse width of the Gaussian pulse is typically defined as:

$$\tau = \sigma \cdot 2\pi \quad (\text{sec}) \tag{2.2}$$

With a typical Gaussian pulse width on the order of one nanosecond or less, the energy of the pulse is spread over a broad range of frequencies, as can be seen in Figure 2.2. For a limited amount of transmit power, the resulting power spectral density is very low. This characteristic results in a low probability of detection and limits the amount of in-band interference caused to narrowband systems. The interference due to UWB is more of a noise tolerance issue, as it mostly results in a slight raising of the noise floor of the victim receiver. Therefore, UWB signals can co-exist with current communication signals, even within the same frequency band.

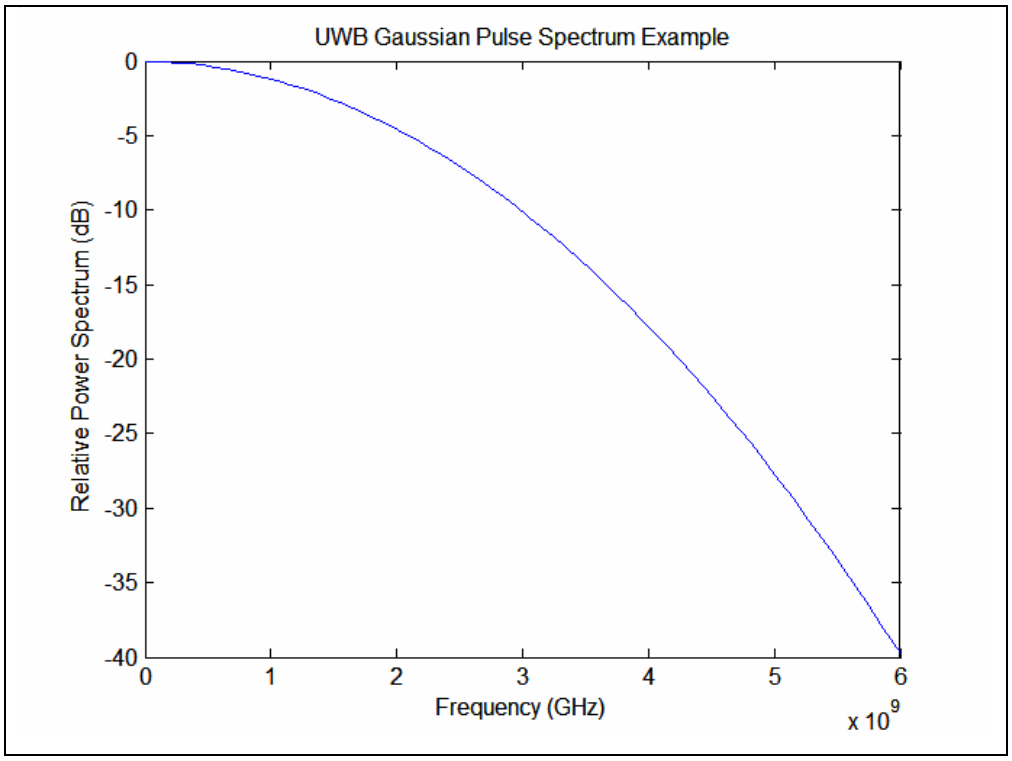


Figure 2.2. UWB Gaussian Pulse Spectrum Example

The Gaussian baseband pulse described in the previous paragraph does not comply with FCC UWB communication regulations, as it uses spectrum from DC to some finite frequency, often over 1 GHz. To adhere to FCC regulations, as seen previously in Figure 1.1, the pulse needs to be bandlimited using a bandpass filter. Performing this operation causes the pulse to be further distorted, as do the antenna and communication channel. The pulse shape also incurs time dispersion, causing maximum pulse repetition rates to be limited to avoid intersymbol interference. To compensate for the pulse distortion throughout the system, an adaptive pilot-based digital matched filter receiver technique can be employed. The pulse shape can be adapted at the receiver, allowing for the use of different pulse shapes and antennas in the system with minimal reconfiguration at the receiver. This will be discussed in more detail in section 2.4.

To generate an ultra-short pulse for a UWB communications system, historically two devices have been used. A tunnel diode was the original method in early UWB transmitters, including the system built by Gerald F. Ross [1]. The tunnel diode is very successful in fast switching applications due to its negative resistance region over part of its operating point, as seen in Figure 2.3 below. For a tunnel diode, a current can be

created using only a small amount of biasing voltage due to a process known as "tunneling," as electrons cross the P-N junction aided by special doping procedures, as they would otherwise not have a sufficient amount of energy to do so [7]. Once the potential voltage is greater than the peak point shown in the figure, it causes the current to decrease until it reaches the valley point. This is caused by less overlap between the valence and conduction bands [7], essentially creating a negative resistance region due to the decrease in current. Since the negative resistance region causes the tunnel diode to be in an unstable state, it almost instantaneously switches to the forward point, triggering a small voltage step pulse on the order of picoseconds. A Gaussian pulse is then created from the step pulse generated from the tunnel diode using a simple short-circuit stub, as will be seen later in Figure 2.4.

Although tunnel diodes once seemed more attractive than transistors due to these unique switching characteristics, they have not been in mainstream production since the 1960s. The primary drawbacks of tunnel diodes are their low impedance, low voltage output, and the fact that they have two terminals. Most engineers did not have experience designing amplifiers with these traits, as vacuum tubes and transistors were popular three terminal devices most commonly associated with amplifier design. Without the willingness to overcome this design challenge, most companies decided to move in a different direction. Consequently, the tunnel diode was seen as only a pulse generating

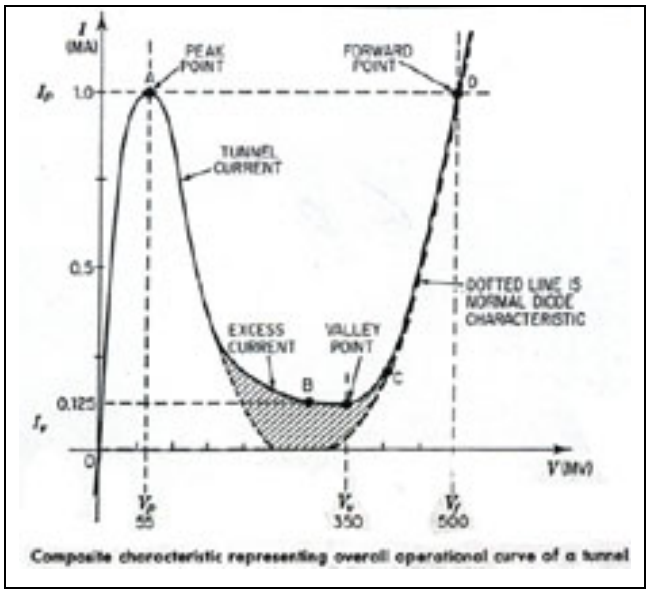


Figure 2.3. Tunnel Diode Characteristic Curve [8]

commodity, reducing its marketability. Since then, finding tunnel diodes to purchase has become a daunting task, given the limited amount of commercial suppliers [9].

With tunnel diodes being difficult to find, step recovery diodes (SRD) have become the most common source for generating UWB pulses. An SRD acts as a charge controlled switch using a P-I-N junction with faster switching characteristics than a typical p-n junction. A stored charge is created in the junction as a result of the minority carriers inserted during the forward bias state, where a recombination time (or carrier lifetime) must occur. The junction impedance is abruptly dependent on the stored charge, which has the capability to lead to fast rise time pulses. Explicitly, if a forward biased SRD is suddenly reversed biased, the diode appears to have a low impedance until the charge within the junction is depleted. Then, the diode snaps back into a high impedance state, essentially stopping the reverse current of the SRD. This impedance transition, along with the current within the SRD prior to cutoff, causes a voltage spike [10]. The amount of time for this transition to occur is often referred to as "snap" time, leading some engineers to identify SRDs as snap diodes. The typical snap time ranges from 30 to 250 ps, allowing SRDs to generate pulse widths on the order of picoseconds. Also, the carrier lifetime usually varies from 5 to 15 ns in SRDs, meaning pulse repetition frequencies for UWB transmitters are thus limited to 100 to 200 MPulses/s, which may or may not be sufficient for impulse radio to flourish as a high data rate technology.

If you consider pulse generation using an SRD and given the information in the previous paragraph, it appears as though an SRD produces a ramp-like pulse instead of the desired Gaussian shape. One common SRD Gaussian pulse generator configuration is shown in Figure 2.4. The ramp-like pulse produced by the SRD splits at Point A, traveling down the reverse transmission line and also propagating down the forward transmission line. The ramp-like pulse moving down the reverse transmission line reflects from the stub and is converted into an opposite polarity ramp-like time delayed pulse due to the negative reflection coefficient of the short circuit. At the forward transmission line, the two pulses recombine to form a Gaussian pulse shape. Using the same configuration shown in Figure 2.4, the SRD can be replaced by a tunnel diode and produce the same pulse shape.

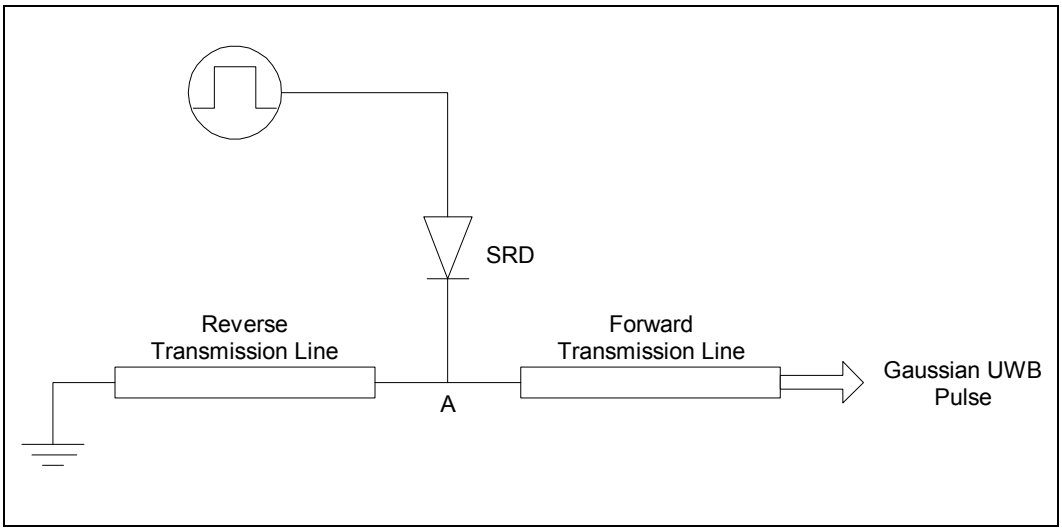


Figure 2.4. SRD Pulse Generator Example

The width of the pulse is determined by the length of the short circuited transmission line and is analytically computed using [11]:

$$\tau = \frac{2L_{TL}}{v_p} \tag{2.3}$$

where:

L_{TL} is length of the reverse transmission line (meters)
v_p is the phase velocity along the reverse transmission line (meters/second)

The phase velocity along a microstrip transmission line (used since implementation will be done on a printed circuit board) is found using [12]:

$$v_p = \frac{c}{\sqrt{\varepsilon_e}} \tag{2.4}$$

where:

c is the speed of light (meters/second)
ε_e is the effective permittivity constant of the microstrip

The effective permittivity constant is the equivalent homogeneous medium replacing the air and microstrip substrate. This variable is calculated using [12]:

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(\frac{1}{\sqrt{1 + 12d/w}}\right) \tag{2.5}$$

where:

ε_r	is the relative permittivity constant of the microstrip substrate
d	is the thickness of the microstrip substrate (meters)
w	is the width of the microstrip transmission line (meters)

To give an example using the formulas above, typical FR4 PCB material has a relative permittivity constant of 4.6, uses 7.2 mil substrate thickness, and utilizes 12 mil trace widths for RF transmission lines. The effective permittivity and phase velocity can then be calculated using Equations (2.5) and (2.4), respectively. For a transmission line length of 1 inch, after converting to metric, the resulting pulse width is 315 picoseconds.

For system design purposes, a particular pulse width is often desired. Equation (2.3) can be rearranged to determine the length of the transmission line, finalizing the design of the simple SRD pulse generator example shown in Figure 2.4. In RF applications, the Gaussian pulse shape is often distorted, as excessive ringing occurs due to the fast rise time of the pulse and parasitic effects of the packaging. This problem can be avoided with pulse shaping circuitry on the output, as will be shown later in Chapter 3.

2.3 UWB Modulation Techniques

Although numerous modulation techniques are used with impulse-radio UWB, three common schemes are often found in research papers and journals. On-Off Keying (OOK), Biphase Modulation, and Binary Pulse Position Modulation (Binary PPM) are popular UWB modulation techniques due to their simplicity and flexibility towards low duty cycle pulsed communication systems.

2.3.1 OOK

OOK, or otherwise known as unipolar signaling in the analog baseband world, is a simple pulse modulation technique where a pulse is transmitted to represent a binary "1", while no pulse is transmitted for a binary "0". The baseband representation, which is illustrated in Figure 2.5a, of the transmitted signal is [13]:

$$w(t) = \sum_{j=-\infty}^{\infty} b_j s(t - jT_f) \tag{2.6}$$

where:

w(t)	is the transmitted UWB signal
b_j	$\epsilon\{0,1\}$ data bits
s(t)	is the pulse shape
T_f	is the frame period (seconds)

One obvious advantage to using OOK is the simplicity of the physical implementation, as one pulse generator is necessary, as opposed to two, as is the case with biphase modulation. A single RF switch can control the transmitted pulses by switching on for a "1" data bit and off for a "0" data bit. This effortless transmitter configuration makes OOK popular for less complex UWB systems.

Although OOK has a very straightforward implementation, there are numerous system drawbacks. In either a hardware or software based receiver design, synchronization can be easily lost if the data contains a steady stream of "0's." Also, the BER performance of OOK is worse than biphase modulation due to the smaller symbol separation for equal symbol energy. As shown in Figure 2.6, the difference in pulse amplitude is A, whereas in biphase modulation the difference is twice the pulse amplitude, or 2A. Bit errors occur less often when the amplitude difference is greater because more distortion is necessary in the channel to affect a bit decision. This effect is demonstrated in the probability of bit error for baseband OOK using a matched filter receiver, which is compared in Figure 2.7 with biphase modulation and binary PPM [14]:

$$P_e = Q\left(\sqrt{\frac{E_b}{N_o}}\right) \tag{2.7}$$

where:

Q	is the Q-function
E_b	is the average energy per bit (Joules)
N_o	is the noise power spectral density at the detector (Joules)

The Q-function is defined by [14]:

$$Q(z) \triangleq \frac{1}{\sqrt{2\pi}} \int_z^\infty e^{-\lambda^2/2} d\lambda \tag{2.8}$$

2.3.2 Biphase Modulation

In generic pulse modulation terms, pulse amplitude modulation (PAM) transmits data by varying the amplitude of each pulse based on binary data. The most common form of PAM in UWB communications is 2-PAM, or biphase modulation, where the polarity of a pulse is modulated. In this situation, a positive pulse is transmitted for a "1" and a negative pulse is transmitted for a "0". The signaling waveform for the biphase modulation technique is shown in Figure 2.5b and mathematically described as [13]:

$$w(t) = \sum_{j=-\infty}^{\infty} b_j s(t - jT_f) \tag{2.9}$$

where:

b_j	ϵ {-1,1} data bits

One advantage of biphase modulation is its improvement over OOK in BER performance, as the E_b/N_o is 3 dB less than OOK for the same probability of bit error, as shown in Figure 2.7. The probability of bit error for biphase modulation assuming matched filter reception is [13]:

$$P_e = Q\left(\sqrt{\frac{2E_b}{N_o}}\right) \tag{2.10}$$

Another benefit of biphase modulation is its ability to eliminate spectral lines due to the change in pulse polarity. This aspect minimizes the amount of interference with conventional radio systems. A decrease in the overall transmitted power could also be attained, making biphase modulation a popular technique in UWB systems when energy efficiency is a priority.

A disadvantage of biphase modulation is the physical implementation is more complex, as two pulse generators, one of them with the opposite polarity, are necessary instead of one, as is the case with OOK. This presents a problem when attempting to transmit a stream of pulses, as the time between pulses can become non-periodic if the pulse generators are not triggered in a timely fashion. Despite these issues, biphase modulation is a very efficient way to transmit UWB pulses.

2.3.3 Binary PPM

The last popular UWB modulation scheme to be discussed is PPM, which is a technique where the timing of each pulse is altered to transmit data instead of varying the amplitude. The simplest form of PPM is binary PPM, where a pulse in a uniformly spaced pulse train represents a "0" and a pulse offset in time from the pulse train represents a "1." Conceptually, the binary PPM technique is shown in Figure 2.5c and stated in equation form as [13]:

$$w(t) = \sum_{j=1}^{\infty} s(t - jT_f - \delta b_j) \tag{2.11}$$

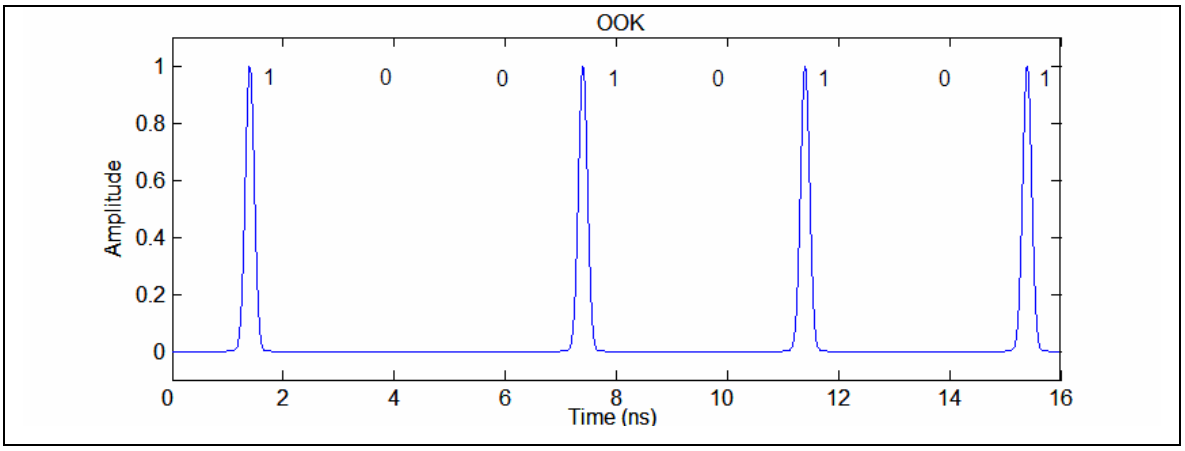
where:

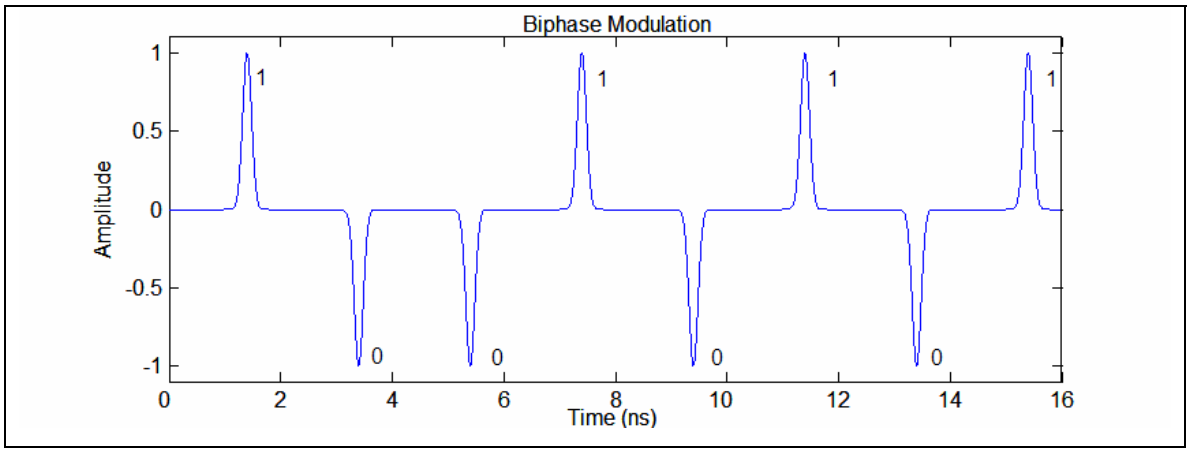
b_j ϵ {0,1} data bits
δ is the modulation index

The most advantageous feature of PPM is the orthogonal signaling present in its data. Each of the pulses in time is independent of one another, meaning the time during the symbol period can be broken up to look for each pulse within a specified time slot. In the case of M-ary modulation schemes, PPM provides better error performance than PAM and also has the advantage of permitting non-coherent reception.

One of the disadvantages of PPM is its BER performance. As shown in Figure 2.6, the distance between symbols is the same as in OOK. This lack of signal energy causes binary PPM to have the same probability of bit error as OOK, or 3 dB worse than biphase modulation. This similarity between binary PPM and OOK is displayed in Figure 2.7 and the probability of bit error equation for binary PPM can be described by Equation 2.7 [13].

Another apparent drawback to PPM is its susceptibility to intersymbol interference, as multiple positions are required to transmit at a higher data rate. PPM must lower the transmitted pulse rate to account for this effect. Therefore, there is a data rate limitation when using M-ary PPM in impulse-radio UWB applications. Even when the intersymbol interference is reduced at the transmitter by decreasing the pulse rate, multipath are more likely to overlap with the next data pulse, causing bit errors at the receiver if the reflections are strong. These types of problems lead to a more complex receiver design, which hampers the use of PPM.





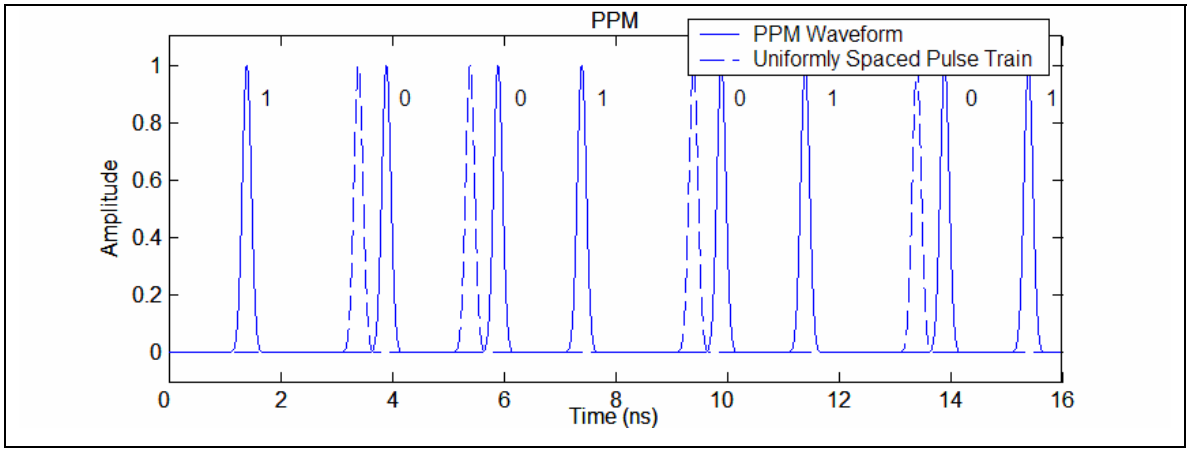


Figure 2.5. Common UWB Modulation Techniques (a) On-Off Keying, (b) Biphase Modulation, (c) Pulse Position Modulation with Binary "0" Offset from the Regularly Spaced Pulse Train (Binary PPM).

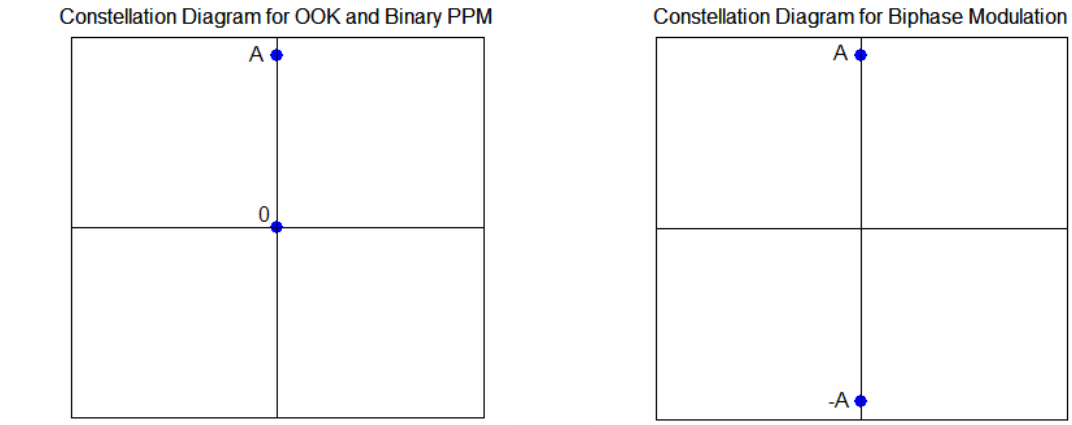


Figure 2.6. Constellation Diagram of OOK, Binary PPM, and Biphase Modulation

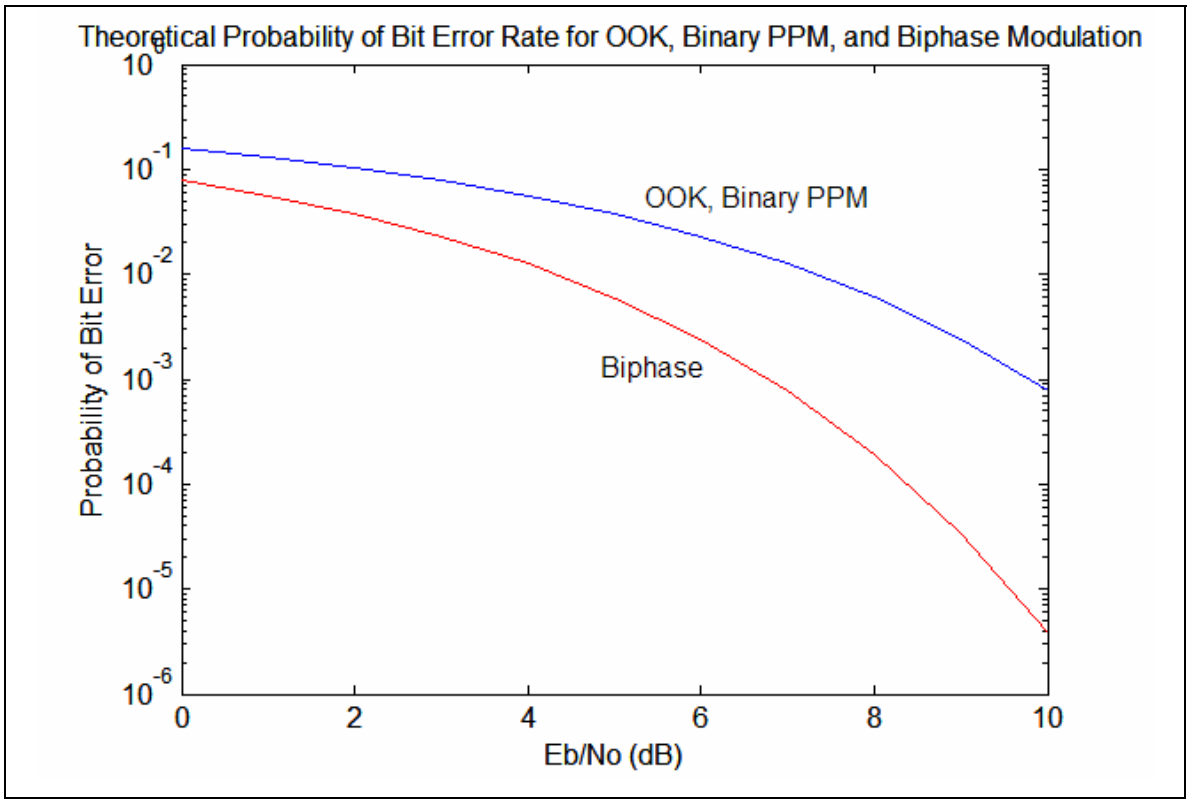


Figure 2.7. Theoretical Probability of Bit Error Rates for OOK, Binary PPM, and Biphase Modulation

2.3.4. Typical Multiple Access Techniques

Using impulse-radio UWB, two common multiple access (MA) techniques are typically applied to the modulation schemes previously discussed. Time-hopping (TH) can be applied to all of the modulation schemes, where each user is assigned a time-

hopping sequence. This sequence reduces collisions in the communication system by assigning each user a unique time shift pattern. Each receiver can detect a signal during its own unique hopping pattern, mitigating interference. The mathematical representation for the k^{th} user's transmit signal is given as [15]:

$$w^{(k)}(t^{(k)}) = \sum_{j=-\infty}^{\infty} s\left(t^{(k)} - jT_f - c_j^{(k)}T_c - \delta b_{[j/N_s]}^{(k)}\right) \tag{2.12}$$

where:

$t^{(k)}$	is the k^{th} transmitter clock time (seconds)
s	is the transmitted baseband pulse waveform
T_f	is the pulse repetition time (seconds)
$c_j^{(k)}$	is the time-hopping sequence
T_c	is the duration of the time delay bins (seconds)
$b_j^{(k)}$	is the data sequence
N_s	is the number of pulses in any given binary symbol
δ	is the modulation index

Direct sequence (DS) is the other form of MA commonly used with impulse-radio UWB, although it is typically limited to OOK and biphase modulation schemes. The idea is to modulate an antipodal PN sequence with a continuous string of pulses. At the receiver, the waveform is demodulated using the same PN sequence, which is unique at the time of communication. Therefore, a minimal amount of interference occurs with other users as they are assigned different PN codes with good auto-correlation and cross-correlation properties. The transmitted DS-UWB waveform is defined as [16]:

$$w^{(k)}(t) = \sum_{i=-\infty}^{\infty} \sum_{n=0}^{N_r-1} b_i^{(k)} a_n^{(k)} s(t - iT_r - nT_c) \tag{2.13}$$

where:

N_r	is the spread spectrum processing gain
$b_i^{(k)}$	is the modulated data symbols for the k^{th} user
$a_n^{(k)}$	is the k^{th} user spreading chips
w	is the transmitted baseband pulse waveform
T_r	is the bit period (seconds)
T_c	is the chip period (seconds)

2.4 Digital UWB Receiver Designs

As discussed in Chapter 1, there are many UWB receiver hardware implementations currently being used, including the sampling bridge circuit, matched filter, and threshold detector. Digital receiver topologies such as leading edge detection and matched filter techniques, including one based on pilot pulses, will be explained in this section. It is important to note that all of these receiver topologies can be implemented in an analog form, although a discussion of each is not warranted due to the digital nature of the receiver design presented in this thesis.

2.4.1 Digital Leading Edge Detection

Digital leading edge detection is the simplest receiver topology used in UWB data demodulation. After the incoming waveform is sampled, each sample is compared to a data threshold, which is a pre-determined value based on the expected pulse amplitude and the standard deviation of the noise, or the noise threshold. Commonly used in radar applications, a noise threshold is necessary in calculating the data threshold to reduce the number of false alarms. Frequent noise spikes will trigger the data demodulation function to incorrectly count pulses, increasing bit errors and causing synchronization problems. Once the data threshold is found, data is processed based on the modulation scheme. For OOK or biphase modulation, the sampled value must be either above or below the threshold (two thresholds for the case of biphase modulation) to determine a bit decision. In the case of binary PPM, when a sampled value is above the threshold, the sample index must be utilized to determine a bit decision. One noticeable benefit of leading edge detection is the short amount of time it takes to process data, making it valuable in high data rate situations. A sample or index comparison is time friendly compared to correlation calculations, as will be seen in the next section with matched filters.

Even though digital leading edge detection is straightforward to implement, it is not flexible in the types of modulation schemes or channels it can support. In any UWB

system, the input bandwidth of the receiver is large, meaning narrowband signals using the same spectrum will also be processed without any interference cancellation. False alarms will result if the signal is sufficiently strong compared to the data threshold value. The same effect occurs in communication channels with a significant amount of additive noise or multipath, which can cause too many bit errors for a reliable link. Finally, pulse shapes such as Gaussian monocycles cannot be used in biphase modulation, limiting the system to impulse transmission and antennas with minimal pulse distortion. Despite these disadvantages, leading edge detection is a primary candidate for processing data in high data rate environments due to its low complexity.

2.4.2 Digital Matched Filter

Digital matched filtering is a data processing routine which is optimal in term of signal-to-noise ratio (SNR). Specifically, it can be shown [14] for an additive white Gaussian noise (AWGN) channel with no interference that the matched filter maximizes the SNR for a pulse modulated system. To perform this operation, the received waveform is oversampled to allow for multiple samples per pulse period. Oversampling gives a more accurate representation of the pulse shape, which then produces better results using a digital matched filter. Correlation processing, another form of matched filtering, is often used in the digital domain when dealing with white noise channels. The method for calculating the correlation output is the following:

$$g[k] = \sum_{t=1}^{N-1} r[t]h[t] \tag{2.14}$$

where:

g[k]	is the resulting correlation value
k	is the k^{th} pulse period
N	is the number of samples in one pulse width
r[t]	is the received sampled waveform
h[t]	is the known pulse waveform

One of the primary drawbacks of the matched filter receiver topology is the lack of knowledge of the pulse shape at the receiver due to distortion in the channel.

Imperfect correlations can occur by processing the data with an incorrect pulse shape, causing a degradation in correlation energy. There are numerous ways to correct this problem, including an adaptive digital equalizer or matching a template by storing multiple pulse shapes at the receiver. A more accurate approach is to estimate the pulse shape from the pilot pulses, which will experience the same channel distortion as the data pulses. This estimation technique is a promising solution to UWB pulse distortion.

2.4.3 Digital Pilot-Based Matched Filter

One of the major advantages of incorporating a digital receiver is its ability to include multipath energy throughout the symbol period to enhance probability of bit error performance without the hardware headache of correlator banks. This concept, which is referred to as a pilot-based matched filter receiver, implicitly combines the energy of multipath to increase the amount of the received energy per symbol. When sampling in the time domain, the entire symbol period is sampled for each pilot pulse, not solely the pulse waveform. An example of a symbol waveform is illustrated in Figure 2.8 and demonstrated mathematically below:

$$r[t] = \sum_{i=1}^{x} A_i s[t - \tau_i] \tag{2.15}$$

where:

- s is the pulse waveform
- x is the number of multipath components
- A_i is the amplitude of the i^{th} multipath pulse (including polarity)
- τ_i is the multipath delay of the i^{th} path

In this scenario with multipath, the entire symbol period should be used to demodulate the data, not just a single pulse waveform. Using a digital receiver with a pilot-based matched filter results in a correlation value that accounts for all of the multipath energy:

$$g[k] = \sum_{t=1}^{n-1} r[t]p[t] \tag{2.16}$$

where:

n	is the number of samples in one sample period
p[t]	is the estimated pulse shape

Equations (2.7) and (2.9), which are probability of bit error results for a perfect matched filter without multipath, have the same performance as using a matched filter with multipath using a perfect matched filter estimate. In both cases, the maximum amount of energy is used to process data, which increases the likelihood of correct bit decisions. It should be noted this technique is valid for both LOS and non-LOS cases. The downside is that in order to obtain good estimation of the pulse shape, a large number of pilot symbols may be necessary.

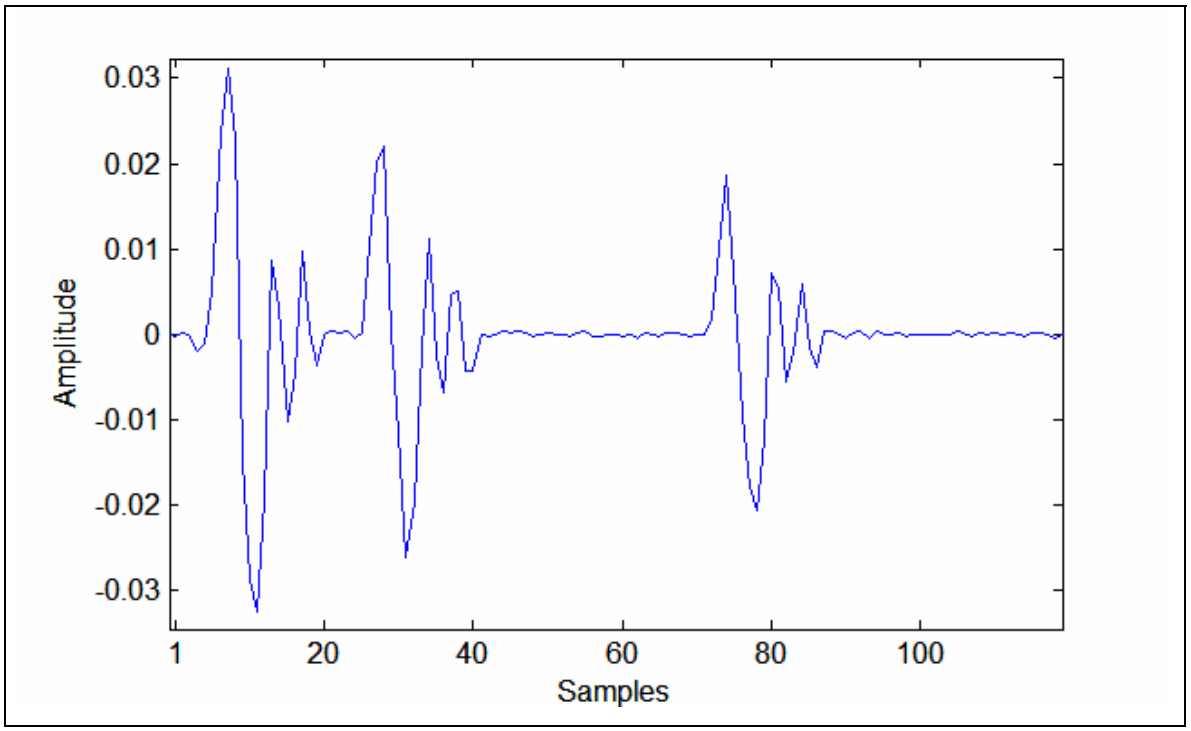


Figure 2.8. Symbol Period Waveform Example

2.5 Conclusion

This chapter discussed the fundamentals of communications using UWB pulses including techniques to generate ultra-short Gaussian pulses with either tunnel diodes or SRDs using simple circuitry. Both of these diodes are very effective due to their fast switching characteristics, allowing for fast transitions in voltage. In this chapter we also discussed various modulation schemes that are possible with pulse-based UWB. Additionally, we examined multiple access techniques and receiver architectures suitable for UWB systems.

Chapter 3 Transmitter Design and Construction

3.1 Introduction

In this chapter, the UWB transmitter design is thoroughly detailed by explaining the pulse generation circuitry and the on-board RF components. Other parts of the transmitter such as the low pass filters and the two likely choices for an antenna are included. Since the design has proposed three modulation schemes, data generation is also described. Construction of the transmitter consisted of producing a detailed schematic and PCB layout, which are explained in this chapter but illustrated in Appendix A. Finally, testing of the manufactured transmitter board is presented, along with the suggested changes for future revisions.

3.2 Transmitter Design

A block diagram of the UWB transmitter is shown below in Figure 3.1. The UWB pulses are generated by SRDs, whose characteristics were discussed in Chapter 2. The SRDs are triggered by one of three sources—a highly stable on-board 100 MHz Voltage Controlled Crystal Oscillator (Fox Jito-2-DP5DEC), a user supplied external clock, or directly from a pre-existing data waveform. If the oscillator or external oscillator input is used, data originates from an off-board source to control the Mini-Circuits M3SWA-2-50DR RF switch, which connects the output of the SRD pulse generator to the RF portion of the transmitter. To transmit at lower pulse rates (i.e. 50 MHz, 10 MHz, etc), the switch may be left open so that only every N^{th} pulse is

transmitted. Other pulse rates may be achieved by utilizing a highly stable external clock source. The outputs of the pulse generators are then filtered using the Mini-Circuits LFCN-2400 and LFCN-2000 low pass filters, pre-amplified by the Mini-Circuits GALI-6, combined using the Mini-Circuits RPS-2-30, and transmitted using an off-board power amplifier and an antenna. Note that if biphase modulation is utilized, two data input lines are required—one to trigger a positive pulse to transmit a "1" and another to trigger a negative pulse to transmit a "0". For OOK or binary PPM, either the positive or negative pulses may be used. The following sections will explain the transmitter design in further detail.

3.2.1 SRD Pulse Generator

The pulse generator for the transmitter is a circuit based on the transition characteristics of an SRD. These diodes are designed to have a very abrupt switching time from their forward bias state to their reverse bias state, making them very popular devices for pulse generators. The circuit in Figure 3.2 shows the schematic of the SRD positive pulse generator design, with a highly stable 100 MHz square wave oscillator, labeled in Figure 3.1 as a Fox Jito-2 part, as its input. The negative transition of the waveform causes the SRD (a Metelics SMMD-0840 part with 10 ns carrier lifetime and 70 ps transition time) to switch into a high impedance state from a constant current state, giving rise to a high negative voltage output. Once the pulse arrives at the transmission line, it splits into two negative ramp pulses, each propagating down opposite sides. One of the pulses travels down a short-circuited stub, which reflects a symmetrically opposite time delayed ramp pulse due to the negative reflection coefficient. The two ramp pulses then combine to form a Gaussian pulse at the input of the attenuator, which is necessary to minimize reflections on the transmission line and assist with impedance matching. The length of the short-circuited stub determines the width of the pulse due to the propagation delay of the reflecting ramp pulse down the microstrip transmission line. With the intent to use FR4 material for the transmitter PCB, a value of 1589 mils[1] was calculated based on a desire for a 500 ps pulse using Equations (2.3)—(2.5) in Chapter 2. Using Agilent ADS to adjust and verify the design, a simulation was performed to

[1] A mil is 1/1000th of an inch.

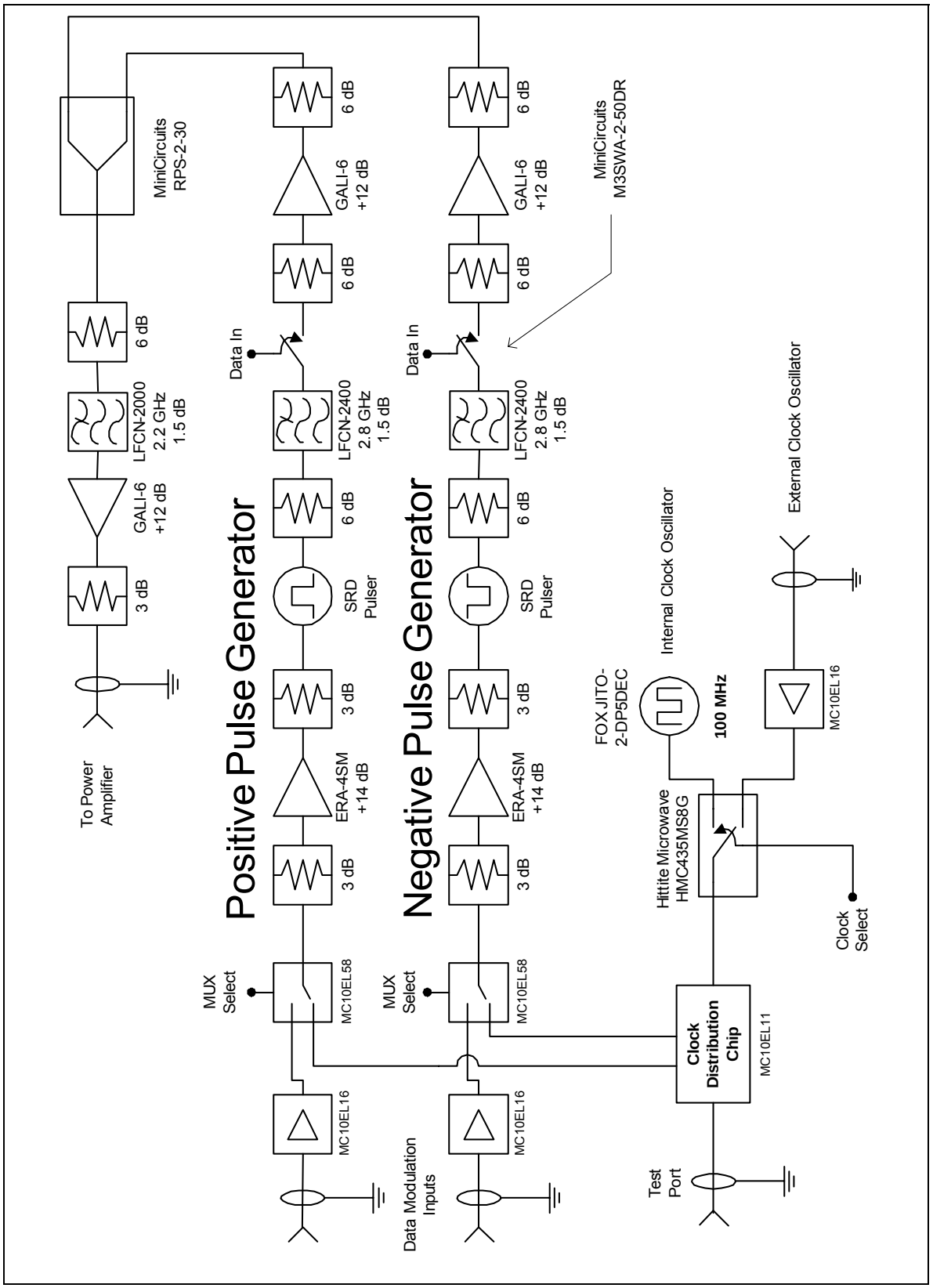


Figure 3.1. Basic Block Diagram of the UWB Transmitter [17]

determine the length of the transmission line with parasitic effects. The resulting value was slightly less than the theoretical one, and the final length was set at 1420 mils.

The remaining circuitry is designed to shape the pulse and reduce the amount of ringing [18]. The series Schottky diode (DIODE2 in Figure 3.2) accomplishes this task by removing any negative ringing, essentially acting as a half-wave rectifier. Any voltage below the forward voltage of approximately 0.6 volts in the input waveform causes the diode to be reversed biased, which effectively disables the output until the input reaches a positive voltage state. The series blocking capacitor (C1) eliminates the DC offset in the ringing, which causes a small amount of positive and negative ringing to be present. The shunt Schottky diode (DIODE3) reduces the ringing in the pulse train by acting as a switch with a DC bias circuit. As the pulse passes through the shunt diode section, the current is switched off due to the surge in voltage, allowing the pulse to pass through without distortion. Once the voltage surge subsides, the diode switches back on, which enables it to become a short circuit again. Effectively, the ringing acts as an AC waveform and since its voltage is not high enough to reverse bias the diode, it passes through the diode to ground due to the low impedance. Both of the Schottky diodes used in the pulse shaping section are also Metelics parts, specifically the SMSD-6004. Capacitor C3 in the diagram also serves as a blocking capacitor, while C2 is an RF bypass capacitor for the DC source. The circuit was simulated in Agilent ADS and the results can be found in the Chapter 5. One important note is the presence of two SRD pulsers in the transmitter design, one that produces a positive pulse, while the other produces a negative pulse. To generate a negative voltage pulse, the SRD produces a ramp pulse using the positive transition of the clock, while the Schottky diodes are both reversed to create the opposite effect as the ones in the positive pulse case. Therefore, both circuits have the same components with the Schottky diodes configured in an opposite manner.

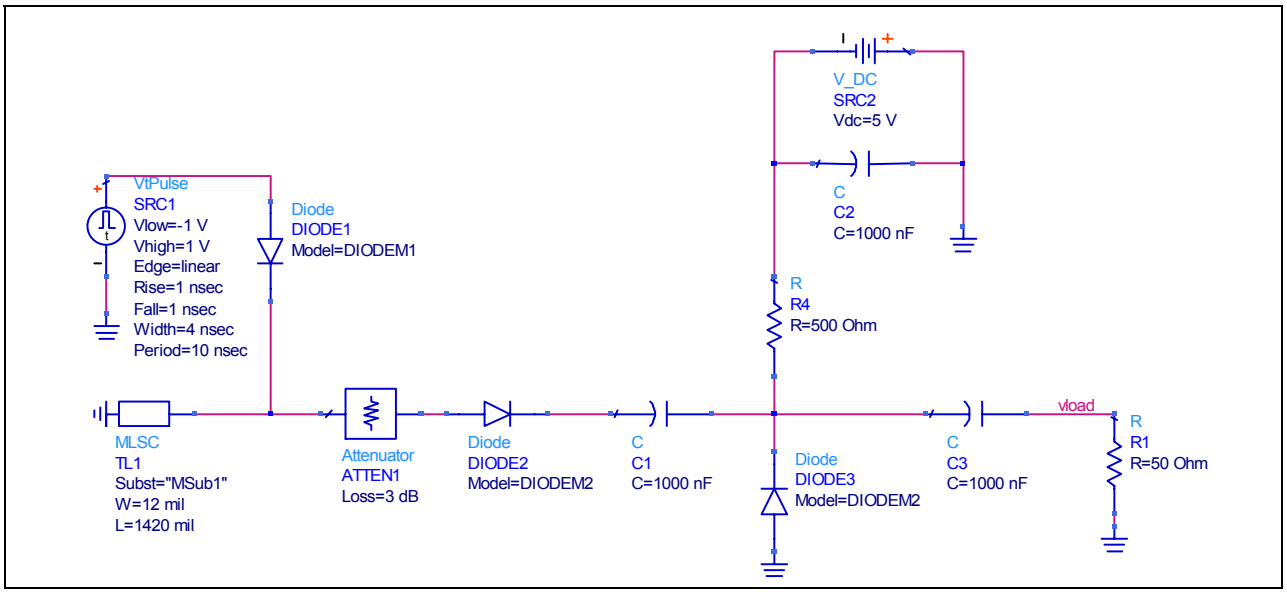


Figure 3.2. Schematic for the SRD Pulse Generator

3.2.2 RF Amplifiers and Switches

There are two uses for RF amplifiers in the transmitter design. One is necessary to trigger the SRD, while the other is for signal amplification. In the first situation, the MC100EL58 multiplexer outputs a positive emitter-coupled logic (PECL) signal with a peak-to-peak (PP) amplitude of 1 volt. To trigger the SRD, a PP voltage of 2 volts was necessary to produce a 4.5 peak voltage pulse calculated by Agilent ADS, causing a need for an increase in signal amplitude. To complete the design, an ERA-4SM Mini-Circuits amplifier was used due to its high gain (13.4 ±0.9 dB) over a 4 GHz wide bandwidth. The high gain was necessary because of the desire to use attenuators on the input and output of the amplifier to increase isolation and provide some impedance matching. The other part specifications for the ERA-4SM are a third order intercept point (IP_3) of +34 dBm and an output power of +17.3 dBm.

After the SRD pulser is triggered, each of the SRD pulse outputs is filtered, individually amplified, and then combined into a single signal. To minimize distortion of the pulse, both amplifier and switch must have the following characteristics:

- Nominal bandwidth significantly greater than the bandwidth of the pulse
- Highly linear (High IP_3)
- Flat gain across the bandwidth of the pulse

The Mini Circuits GALI-6 broadband amplifier meets all of the above criteria. The GALI-6 has a bandwidth of DC—4 GHz, a gain of 12 ±0.3 dB across the entire band, an IP_3 of +35 dBm, and an output power of +19 dBm. Attenuators are placed on each side of the amplifier to assist with impedance matching and reduce the reflections in the transmission line. Their values were chosen based on the gain of the GALI-6, making the overall effect of the amplifier gain negligible. In this scenario, the amplifier is used mostly as a transmission line driver, which is why the amplifier gain was not one of the more significant characteristics.

There are two RF switches used in the transmitter design, namely the Hittite Microwave HMC435MS8G and the Mini Circuits M3SWA-2-50DR RF switches. The Hittite will be used to choose between the on-board 100 MHz clock signal and the external clock. It was chosen to perform this task since its specifications are less stringent and samples were readily available in the lab. The Hittite switch has a bandwidth of DC—3.5 GHz, an insertion loss of 0.6 ±0.3 dB across the entire band, a 1 dB compression point of +24 dBm, 50 dB of input-output isolation, and 40 ns switching time. To perform switching of the UWB pulse train, the Mini Circuits part was chosen due to its low switching time of 10 ns, which allows for an increase in the transmitter pulse rate and satisfies the design goal of 100 MPulses/sec. The Mini Circuits switch has a bandwidth of DC—4.5 GHz, an insertion loss of 0.7 ±0.2 dB across the entire band, 1 dB compression point of +25 dBm, and 57 dB of input-output isolation. The output of the Mini-Circuits switches both include 6 dB attenuators to help preserve the pulse shape with additional isolation by reducing reflections in the transmission line.

3.2.3 Filters and Antenna

The Mini-Circuits LFCN-2400 (DC—2.8 GHz) and LFCN-2000 (DC—2.275 GHz) ceramic filters on the output of the SRD pulsers reduce high frequency components which may be present in the pulses. These filters help to smooth the shape of the SRD pulse and prevent the pre-amplification stage from wasting power by boosting unnecessary frequency components. The Mini-Circuits RPS-2-30 power combiner merges the two individual SRD signals into a single signal, which is then bandlimited, sent through a final pre-amplification stage, and then sent to the external power amplifier

and antenna. Also, several attenuators have been placed at the output to help ensure a 50 Ω termination impedance as well as to reduce reflections from the board-component interface.

External to the transmitter board is a power amplifier and an antenna. The specific part number for the power amplifier will be determined once an inventory is done in the lab to determine the availability of such a device. To ensure the transmission of impulses, the use of a non-dispersive antenna is imperative, such as a biconical antenna. Figure 3.3 is the output pulse shape using an input Gaussian impulse of 100 ps time duration, meaning a biconical antenna effectively introduces little distortion to the input pulse, as explained in [19]. This type of configuration is necessary to operate the UWB system using biphase modulation and digital leading edge detection mode at the receiver, as distinct positive and negative pulses are necessary at the receiver. A disadvantage to the biconical antenna is its omnidirectional nature, which increases the number of multipath and the maximum excess delay of the channel. As will be discussed in the next section, the data rate is affected by an increase in channel reflections. The use of a Vivaldi antenna, which has a beamwidth of approximately 45 degrees, reduces the number of multipath and allows for higher data rates. It essentially acts as a differentiator, as shown in Figure 3.4 with the output pulse shape shown as a Gaussian doublet after the same Gaussian input pulse described previously is applied to its input. Another advantage of the Vivaldi is its relatively flat, yet strong, frequency response over a broad range of spectrum. Obviously, there is a downside to the narrow beamwidth, as the transmit and receive antennas must always be pointed towards each other, limiting the flexibility in direction and location. Even though these are the primary choices for antennas in the design, other ones could be utilized—assuming an appropriate reference pulse shape was downloaded to the data processor at the receiver when using matched filter receiver topology.

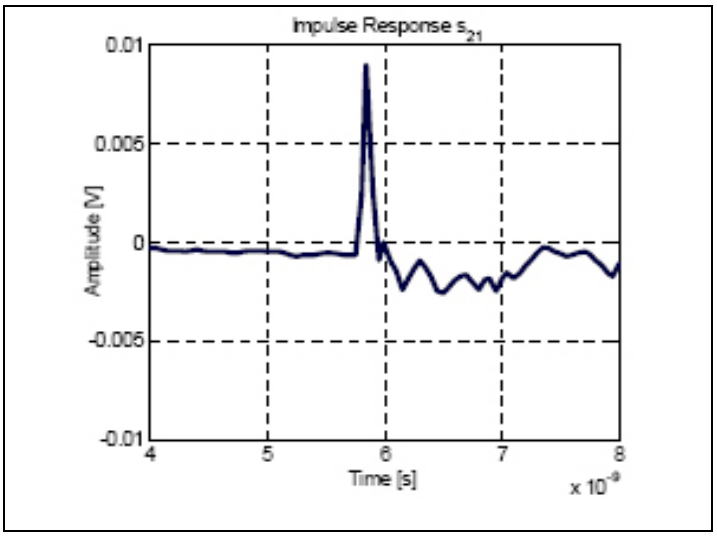


Figure 3.3. Impulse Response of a Biconical Antenna [19]

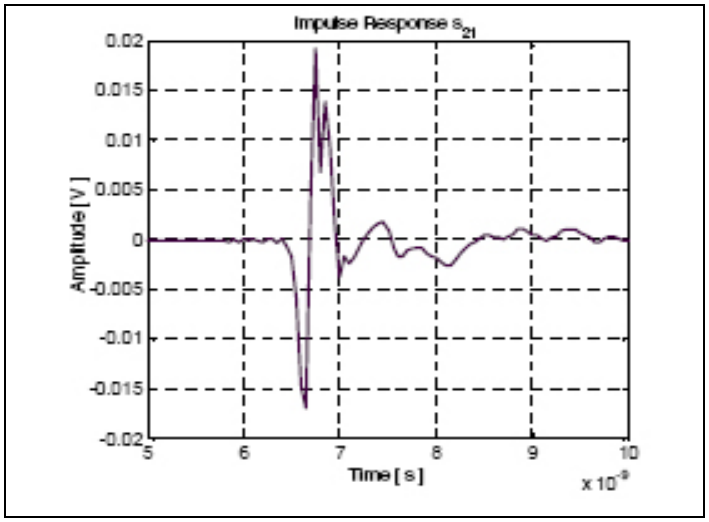


Figure 3.4. Impulse Response of a Vivaldi Antenna [19]

3.2.4 Data Generation

The RF sections of the transmitter have been discussed, but there is still a need to explain the data generation technique of the transmitter for the three modulation schemes, OOK, biphase modulation, and binary PPM, discussed in Chapter 2. This occurs in one of two ways—either through a clock or a pre-existing data waveform.

The on-board oscillator is a Fox Electronics part, JITO-2, that will be operated at 100 MHz. Using this oscillator, the SRDs can generate periodic pulse waveforms at 100 MPulses/sec. The series Mini-Circuits RF switches can be turned on and off depending

on the desired data rate or modulation technique. To create a signal at lower pulse rates, the select pin of the RF switch is controlled to transmit every other pulse (50 MPulses/sec), every 4th pulse (25 MPulses/sec), etc. In Figure 3.5 below, a 25 MPulses/sec pulse train is formed using the on-board oscillator. For this scenario, the SRD pulse generator produces pulses at 100 MPulses/sec (solid and dashed pulses) and the select pin of the RF switch determines which pulse is output (solid pulses). Therefore, the rate at which the select pin is triggered establishes the output pulse rate.

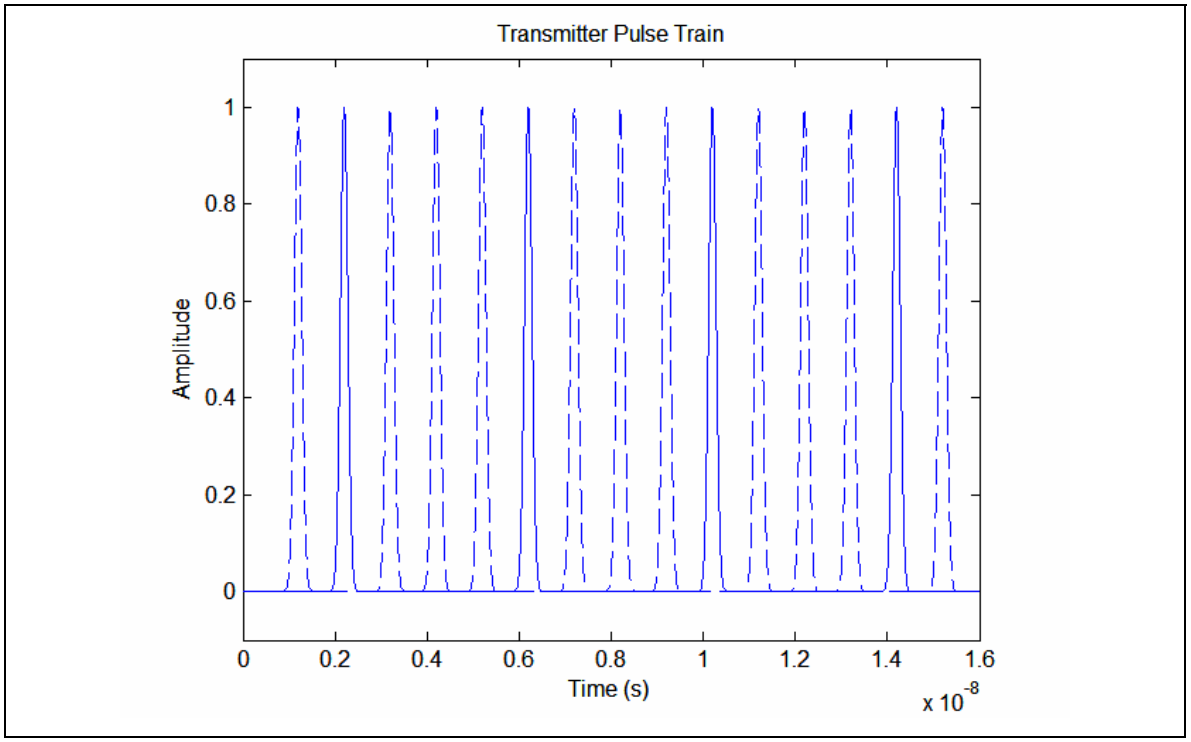


Figure 3.5. Transmitter Pulse Train at Lower Pulse Rates Using the On-Board Oscillator

For the suggested modulation schemes, specifically OOK, one of the RF switches would always be turned off because only one pulse polarity is necessary. The other will be toggled based on the data input select from an off-board source. When using biphase modulation for data transmission, each select pin on the RF switch toggles according to the data. To generate a positive pulse on the output, the select pin of the RF switch on the positive path should be on, while the select pin on the negative path should be off. The opposite is true for a negative pulse output. A signal for binary PPM can be generated using an oscillator running much faster than the transmitted pulse rate. The RF

switch would have to operate non-periodically to choose the correct pulse to output. Although binary PPM is an option using this method, it would not be the optimal choice. Another way to trigger the SRDs is to use an external clock source, if one is readily available with a highly stable output waveform. A PECL differential receiver, specifically the MC100EL16 from On-Semiconductor, is necessary to convert the external oscillator signal into PECL form, as is the case with the other triggering sources. The Hittite Microwave RF switch, previously discussed, will determine which clock reference to use. Using either method, the result using an oscillator input is a pulse train at a pulse repetition frequency determined by the user.

Synchronization between the oscillator signal and the RF switch is key to transmitting the correct pulse repetition frequency and the entire pulse itself. If the data select on the Mini-Circuits RF switch is not in synch with the clock, entire pulses will be excluded or the switch will toggle in the middle of a pulse, causing distorted output pulses. The primary reason for the test port is to eliminate this problem by synchronizing it with the data select input to the RF switch. Using a PLL (zero-delay clock buffer) yet to be determined on a daughter card, the correct timing signal can be sent to the data select pin on each of the RF switches for biphase modulation and OOK. The daughter card has not been designed, which is the reason this feature has yet to be fully implemented. Until then, the transmitter will simply output a stream of pulses, although it might be possible to synchronize another oscillator with the external clock to perform toggling of the RF switch.

With synchronization of the clock and RF switch being a difficult task, the easiest method of implementing a data modulated signal is the data waveform inputs. The idea is to generate an external waveform to trigger the SRDs at the precise time, which is optimal for creating a binary PPM signal, although biphase modulation and OOK can also be produced. Two inputs were placed in the transmitter design to allow for each SRD pulser to trigger independently of each other, which eliminates the need for the synchronization circuit used with the clock input. Each input uses a MC100EL16 PECL differential receiver to convert the input signal to PECL. It has yet to be determined how the square wave signal will be created externally, although it will most likely involve a

processor and high speed clock. An arbitrary waveform generator is also a possibility for testing purposes.

One final note on data generation is that ultimately the data rate in a UWB communication system is limited by the maximum excess delay of the wireless channel, as mentioned in the previous section. If multipath signals from a previous data pulse overlap with the current data pulse, it is possible that the receiver will demodulate the multipath signal—rather than the true data pulse unless complex equalization is employed. Multipath delay spreads are a product not only of the wireless propagation environment, but are also a function of the directionality of the antennas used in the communication system. This is the reason this point was emphasized in the antenna section, as the Vivaldi antenna will result in smaller maximum excess delay than the biconical antenna in the same channel. Higher data rates are thus possible with directional antennas.

3.2.5 DC Power Supply

The power supply for the transmitter is a modified design, with the original being designed by Chris Anderson for a PN generator. There were three voltages necessary to be converted from the +12 volt supply. Those values, +7, +5, and -5 volts were generated using converters and inverters, along with filtering components, as is shown in the transmitter schematic located in Appendix A. Even though PECL was used in the design, which calls for a +3 volt termination at every transmission line, it only appeared in few instances. Since it was determined insufficient to warrant a +3 volt power plane, voltage dividers using resistors terminated to +5 volts were used instead.

To generate the +7 volts necessary for the RF components, a LT1765 switching regulator was incorporated. The proper biasing components were included, as suggested by Linear Technology, the part manufacturer. The resistor values were set specifically for a +7 voltage output, while the capacitors on the output are filters for high frequency noise. As for the +5 volts, the output of the +7 volts was used in conjunction with the LT1086 voltage regulator. Finally, the -5 volts is created using the +5 volts as an input to the National Semiconductor LM2660 voltage inverter. Again, the added components are filtering suggestions from each manufacturer to provide the best performance. A light

emitting diode (LED) was also included on the transmitter circuit board to indicate the power status of the transmitter.

3.3 Transmitter Construction and Testing

There were three primary steps in constructing the transmitter including the schematic layout, PCB layout, and the PCB hardware fabrication. Details of each process will be discussed in further detail in this section.

3.3.1 Transmitter Schematic

The transmitter schematic was created in PADS PCB Design Solutions using the schematic capture program entitled PowerLogic [4]. Tutorials were very helpful in getting started with the software. The tutorials teach one how to create new schematic sheets, use modeless commands, and add connections between parts. Once some type of familiarity with PowerLogic was attained, the first step in the schematic was to generate an inventory of parts in the parts library. To create a part, the three necessary components are the schematic symbol, the component footprint, and the electrical characteristics, mostly consisting of pin numbers. Since Chris Anderson had already designed a PN generator PCB using many of the same parts, he created most of those used in the UWB transmitter schematic.

For reference, the transmitter schematic, consisting of seven pages, is located in Appendix A. It contains all of the necessary parts to form the transmitter block diagram in Figure 3.1, such as SMA connectors, header pins for off-board data, etc. There are several important items to mention in order to clarify our presentation of the schematic. On page 1 of the schematic in Figure A.1, resistors are located throughout the design to properly terminate every PECL chip used. Instead of creating a +3 volt layer plane, a voltage divider was employed with +5 volts, as was previously mentioned. Values of 80.6 Ω and 130 Ω were combined to form a 50 Ω parallel connection and the proper voltage. All of the attenuators used for isolation purposes in the transmitter design were designed using a pi-network, as shown starting in Figure A.2. Surface mount attenuators

were not used in the design due to the flexibility and cost-effectiveness of the pi-network configuration. While surface mount attenuators can be easily replaced, they are not as readily available in the lab as 0603 size resistors. If attenuator values need to be adjusted in the future, the process can be performed in minutes by replacing the resistors, instead of placing an order for new parts. Resistor values for the 3 and 6 dB attenuators are shown in Figure 3.6 [20]. The other components in Figures A.1-A.5 are mainly the block diagram parts and biasing techniques for each RF device, most of which were suggestions from each manufacturer. Figure A.6 contains the DC power supply, while Figure A.7 includes the power supply filtering capacitors for all of the on-board chips being powered by a DC voltage pin. This is necessary because power and ground pins were not included in the schematic symbol for parts to simplify cluttered connections.

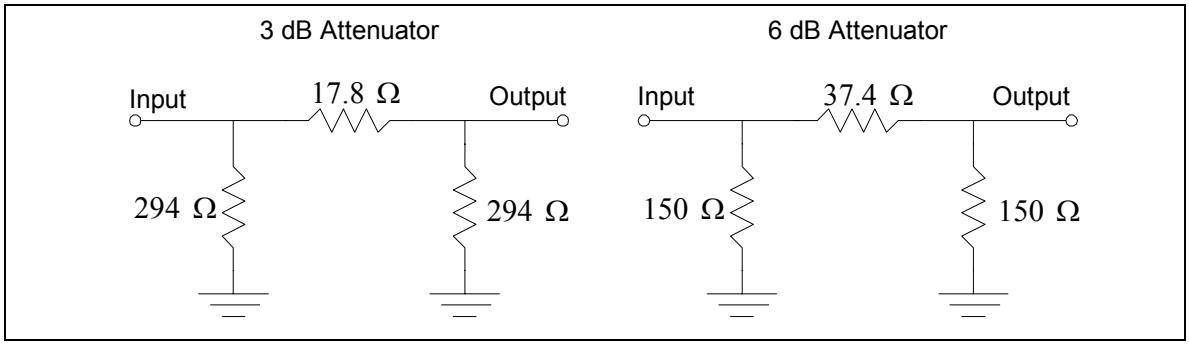


Figure 3.6. Pi-Network Attenuators [20]

3.3.2 PCB Layout

PADS PCB Design Solutions was also used to create the PCB layout using the program PowerPCB [4]. Once the schematic was completed, a netlist was formed from PowerLogic and imported into PowerPCB. The result was scattered components and connections located everywhere on the screen. One of the first tasks performed to complete the PCB design was establishing the number of layers and orientation of each. With four different voltages necessary for IC power pins and PECL termination, more power planes are necessary to make each connection without cluttering routing space on the board. Therefore, a six-layer board was chosen instead of a four-layer board due to the ability to add another power plane. As seen in Figure 3.7, +5 and -5 volts have their own layer. The voltage of +7 volts was connected via traces on the top and bottom layers

while the +3 PECL voltage was terminated using a voltage divider, as discussed in the previous section. The rest of the PCB layer stack is shown with numbers and descriptions given for each layer, as well as the substrate thicknesses in between each in Figure 3.7.

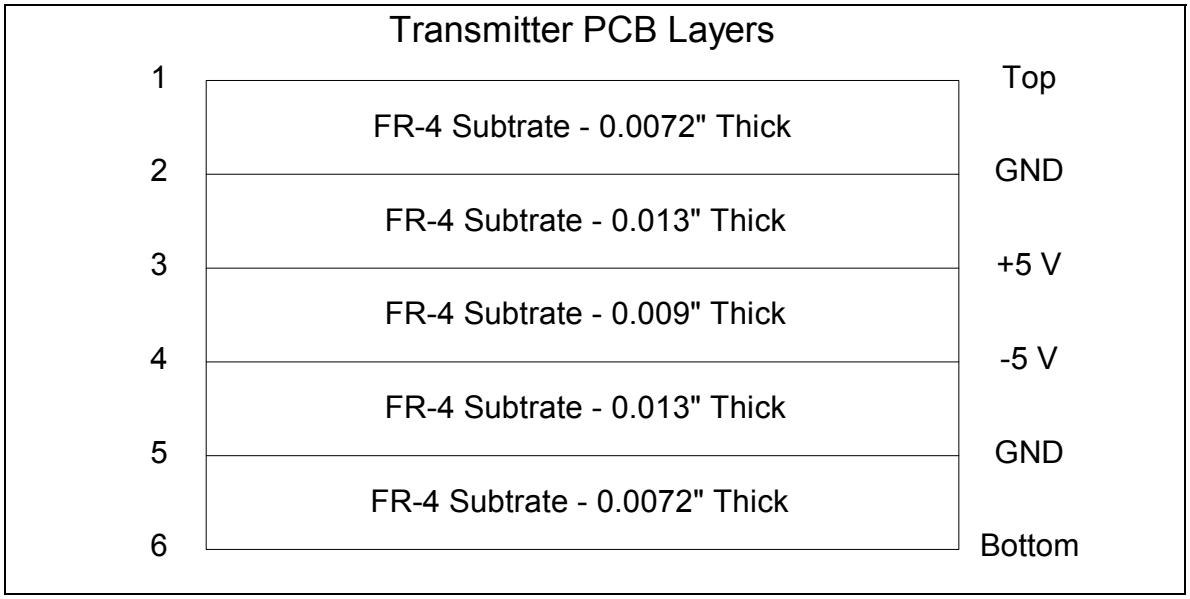


Figure 3.7. Transmitter PCB Layers

Once the layers were determined, the outline of the board was made to be four by six inches, sufficient to include all of the necessary components while minimizing the size for space and economic efficiency. To avoid any additional parasitic effects, the RF circuitry was placed on the top layer while the bottom layer was used for the DC power supply. This scenario also allows for uncluttered routing on the bottom layer for the +7 volt traces to the RF devices. Parts were then placed on the board accordingly, starting with the SMA connectors and header pin connectors on the outside of the board. One of the connectors on the circuit board was added due to a request that power be supplied to a daughter card if one were used in the future. This connector is only located in the PCB design only, not the schematic. Placement of the rest of the parts can be seen in Appendix A, where the PCB layout for each layer is shown. Before routing any traces or including any vias, trace and via sizes had to be determined. Using AppCAD, RF and microwave software from Agilent [21], the RF trace width was found to be 12 mils for a

50 Ω transmission line characteristic impedance using FR-4 circuit board material. PCB Express, the PCB company chosen to fabricate the board, only sells FR-4 circuit boards. The decision to purchase the boards from them was based on a positive prior experience by another graduate student at MPRG. Widths for the DC power traces were designed to be 20 or 30 mils depending on power consumption, allowing them to transfer more power than the RF traces. Finally, via sizes were established based on the PCB Express drill tool sizes. Vias containing RF signals, which were limited to maintain signal integrity, had a 13.5 mils hole. Meanwhile, vias for DC power and ground used a 20 mil hole size. For mounting purposes, four 125 mil vias were placed at the corners of the circuit board. Finally, using the existing connections imported from the schematic, traces were laid out making an attempt to minimize RF vias. Typical PCB layout techniques, such as eliminating 90 degree RF traces due to the increase in effective transmission line width causing extra parasitic capacitance, were employed. Lastly, two keepout regions were placed around the short circuit stubs because the software recognized it as being grounded.

Once the traces were routed in an optimal fashion, the length of each path was measured. In [22], the calculation of the propagation delay of RF signals for a microstrip transmission line is shown to be:

$$t_p = \frac{B_r\sqrt{\varepsilon_r}}{11.8} \quad (ns/in) \tag{3.1}$$

The variable B_r is an estimated factor, given by:

$$B_r = 0.8566 + (0.0294)\ln(w) - (0.00239)h - (0.0101)\varepsilon_r \tag{3.2}$$

and:

w	is the trace width (mils)
h	is the height above the ground plane (mils)
ε_r	is the relative permittivity constant

Using the FR-4 material values of PCB Express (w=12, h=7.2, ε_r=4.6), the propagation delay of the transmission line was determined to be 160 ps/inch. Since two paths, one positive and the other negative, were used to generate the transmitted signal via a power

combiner, the transmission line length of each must be the same or an unintentional non-periodic pulse train results. As an example, if the two paths differ in length by 2 inches, there is a 320 ps delay in one of the pulse polarities. This type of timing inaccuracy will cause numerous problems when sampling at the receiver, which will be further detailed in Chapter 4. To eliminate this problem, the trace lengths for both paths from the SMA connectors to the power combiner were measured and adjusted accordingly. Although no exact path length difference was calculated, a good approximation of the difference was 50 mils, or proportional to 0.8 ps in time.

Once all of the parts and traces were placed in the proper position, a copper pour was performed on all of the layers. The back-off for the top and bottom layers was 16 and 50 mils for traces and vias, respectively, to comply with the manufacturing rules of PCB Express. Finally, CAM files were generated in PowerLogic to print and create Gerber files for the manufacturer. All six of the layer files were produced, along with the top and bottom silkscreen, top and bottom solder mask, and the NC drill file.

3.3.3 Fabrication of PCB

Once the Gerber files were ready, they were sent via e-mail to PCB Express. After two weeks for fabrication, the boards were delivered to Blacksburg. Final construction of the board then took place using the previously delivered parts stored in the lab. The process began by coating the location on the circuit board where soldering was being performed with flux for easier component placement and fewer false connections with closely placed pads. Solder paste was used as the primary source of connecting components to the circuit board. The process involved spreading a thin amount of solder over the pads and heating the substance with a soldering iron or the hot-air soldering station. The solder mask on the circuit board allowed for a very small amount of solder paste, cleaning up the procedure. Afterwards, the flux was scrubbed from the board using alcohol. The initial parts placed on the board were the DC power supply components, mainly to perform tests on the power before soldering the other parts and creating more problems in the future. Finally, the remainder of the components were soldered on the board for testing, although one mistake was found in the board layout. Due to an error in the PCB footprint for the Mini-Circuits M3SWA-2-50DR RF switch, it

could not be soldered to the board. The pins were inadvertently reversed, forcing a direct connection from the input trace to the output trace using a small wire. Although the various modulation schemes could not be demonstrated, the transmitter hardware testing was continued to verify the other circuitry and show pulse generation results.

3.3.4 Transmitter Hardware Testing

After the DC power supply components were soldered to the board, DC voltages were tested using a multimeter to ensure +7, +5, and -5 volts were properly generated. Initially, none of the voltages were correct because of a soldering issue with one of the tantalum capacitors. Once this problem was fixed, the +7 and +5 voltages were accurately measured at the LT1086 voltage regulator. When the power supply was switched on, the voltage inverter chip output -5 volts. However, after a few seconds, the output voltage would abruptly disappear and read 0 volts. After searching through the data sheet, it was discovered that the part in use was the LM2661, which has a shut-down pin, as opposed to the desired LM2660. Therefore, since the incorrect part was ordered, a quick fix was performed to tie the shut-down pin of the LM2661 to ground by soldering in a wire to the closest ground via. Since all of the other pins on the two chips are identical, the LM2661 produced -5 volts and remained on. Even though this situation proved to be successful, the LM2660 was ordered and will be used for future transmitter boards.

Even though it appeared as though the DC power supply was working, a decrease in voltage occurred after approximately five minutes, except the -5 V was reduced to -2.5 V instead of zero. The power supply in use was current-limited and the board began to heat up quickly. Unexpectedly, the circuit board was using 10 watts of power and after no negative results found with the multimeter, it was determined that overheating caused the board to draw too much current. Once a cooling fan was placed near the board, it was powered for 30 minutes without a reduction in voltage before it was intentionally shut down.

After the DC power supply was stable, a 15 MHz square wave was input to the positive pulse data port on the transmitter board. Using an oscilloscope probe, the input PECL signal was verified on the output of the MC100EL16 PECL receiver and the

MC100EL58 multiplexer. Due to the select pin being internally tied to ground, none of the select pins were connected because the proper output was already selected. The output PP voltage of the square wave signal was 850 mV, an expected value for PECL. An obvious problem occurred when the output signal after the ERA-4SM amplifier was only 900 mV PP in amplitude, as the signal amplitude only increased 50 mV for an amplifier with 14 dB of gain. The source of the problem was found to be the RF choke, where initially a high Q-inductor was thought to be the proper component. The Q (Quality Factor) of an inductor is defined as:

$$Q = \frac{2\pi(Total \quad Energy \quad Stored)}{(Power \quad Dissipated \quad Per \quad Cycle)} \tag{3.3}$$

Therefore, an inductor with a higher Q offers a better quality in terms of stored energy. However, even though the ELJFJR12JF2 Panasonic 120 nH inductor had a high Q of 40 (minimum value), the inductor value was deemed the more important characteristic, as it only presented the pulse waveform with a 12 Ω resistance to ground. This led to a 6 dB decrease in voltage, essentially eliminating any chance for the SRD to trigger. After a thorough search on the Internet, a 10 μH inductor manufactured by TDK was found in the same 0603 package with a minimum Q of 30. Even though the inductor was lower in quality, the higher value of inductance would lead to a 950 Ω impedance to ground. A brief simulation was run in Agilent ADS and produced sufficient amplitude results, leading to a redesign of the RF choke for every amplifier on the transmitter circuit board. This change is reflected in the transmitter schematic located in Appendix A.

To temporarily make up for the 6 dB loss in gain through the RF choke, the 3 dB attenuators on the input and output of the ERA-4SM amplifiers were replaced with zero Ω resistors. The result was a square wave input signal of approximately 2 volts on the input of the SRD. Probing the output provided a 500 ps wide pulse shown in Figure 3.8, with a 500 mV peak amplitude along with ringing. This pulse shape was probed prior to the pulse shaping network, as the amplitude did not have enough voltage swing to turn on the series Schottky diode. According to the system simulation described earlier, the SRD should have produced a 4.5 volt amplitude. However, the input current to the SRD was not limited in that particular simulation. Since the SRD is a current driven device, a

current limiting resistor was added to the simulation, producing results shown in Figure 3.9. This scenario more accurately describes the situation in the physical transmitter with approximately 30 mA of current supplied to the SRD. If 6 dB of power loss occurred due to the inductor, the amount of current output from the ERA-4SM was reduced from its 65 mA maximum by more than half, as dissipated heat must also be included. Therefore, even though a sufficient voltage was supplied, the limiting factor was the SRD input current. One solution to the current limiting problem would be to bias the amplifier at a higher current rating, which is given as an absolute maximum of 120 mA for the ERA-4SM amplifier on the Mini-Circuits website. A different biasing resistor was necessary to successfully make this revision, although the effect would not be sufficient to forward bias the series Schottky diode until the inductor was included to eliminate the 6 dB of loss through the biasing network. With the power supply already incurring heating problems, this solution might not be the most adequate due to the increase in power delivered to the amplifier, although no other ideas have been discussed.

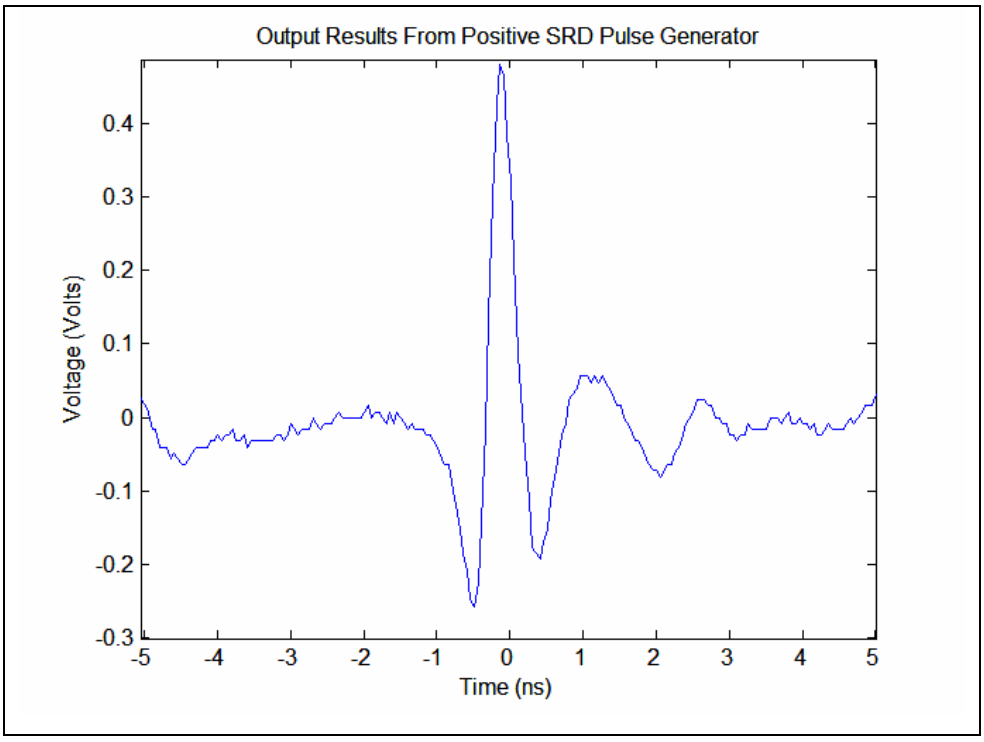


Figure 3.8. Output Pulse from Positive SRD Pulse Generator

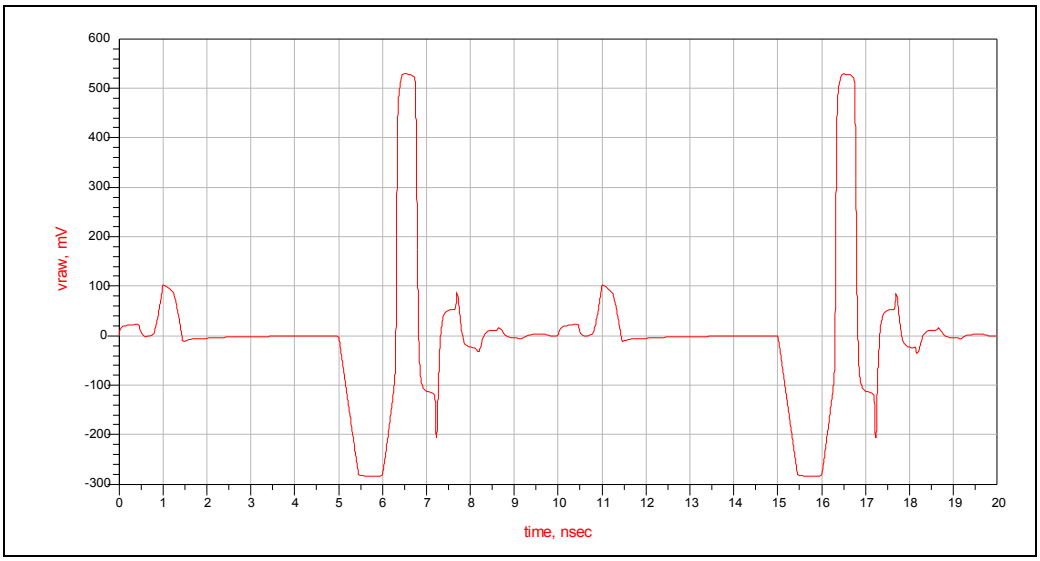


Figure 3.9. Simulated Result from Positive SRD Pulse Generator with a Current Limiting Resistor

To trigger the series Schottky diode and allow the pulse shaping network to properly operate, the input current to the SRD should be approximately 100 mA, which produced an output pulse (after the pulse-shaping network) shown in Figure 3.10 using the updated simulation. This current rating leads to a biasing resistor value of 25 Ω for the ERA-4SM amplifier, assuming there are no power supply limitations. Obviously, since the simulation results were incorrect for the original design, this resistor value will be thoroughly tested in the lab before an exact value is determined. Also, the effect on the power supply will also need to be determined. For this reason, the transmitter schematic in Appendix A does not reflect a change in the biasing resistor value of the ERA-4SM amplifier.

Despite the amplifier biasing setbacks, the testing on the transmitter circuit board and the updated ADS simulation indicate that if the amplifier were biased with the correct components, the SRD pulse generator would produce a clean, minimally distorted pulse. However, due to lack of time, these changes will be made in the future after the biasing circuits are re-designed.

It is important to note that the negative SRD pulse generator was also tested and produced similar results, as shown in Figure 3.11. A problem involving one of the probes led to the rough pulse shape, as its use created more noise, illustrated in the figure below.

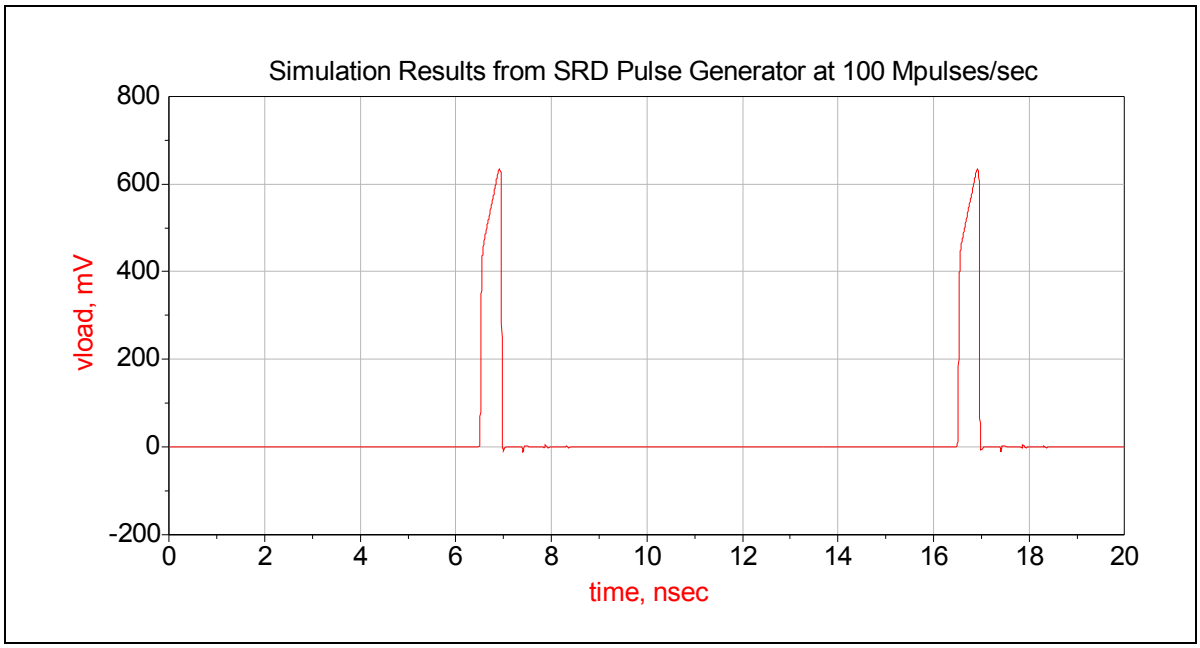


Figure 3.10. Simulated Result from Positive SRD Pulse Generator After Pulse-Shaping Network with ERA-4SM Amplifier Correctly Biased

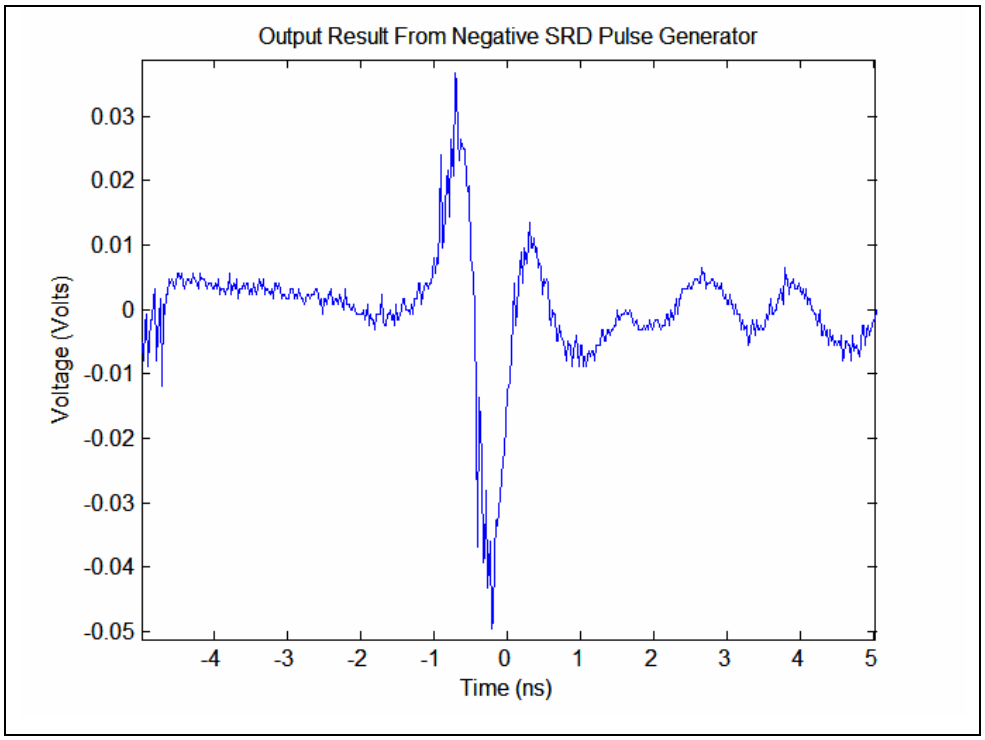


Figure 3.11. Output Pulse from Negative SRD Pulse Generator

3.4 Conclusion

In this chapter, the transmitter design was detailed beginning with the block diagram down to the components in the SRD pulse generator. Other aspects of the transmitter such as the RF circuitry, pulse modulation, and power supply were also thoroughly described. Explanations of the transmitter schematic and PCB layout were given, along with the actual construction of the transmitter circuit board. After a discussion of some of the hardware testing, the final result was a transmitter circuit board that produced a relatively clean signal for both the positive and negative polarity pulses. Suggestions for improvement such as a new RF choke and a new biasing resistor for the ERA-4SM amplifier were made after probing the signal in various locations on the board. Also, a cooling fan is necessary to operate the transmitter, as overheating causes the DC power supply to draw excessive amounts of current, reducing the necessary on-board voltages to unacceptable levels. Even though the transmitter was not fully completed, the modifications proposed after hardware testing, if implemented, will lead to a successful revision in the future.

Chapter 4 Receiver Concept and Design

4.1 Introduction

The receiver description is divided up into two sections within this chapter. Before the design is outlined, the concept behind the receiver, such as the sampling techniques and implementation limitations, are discussed in section 4.2. Then, the receiver design is detailed in section 4.3, beginning with the RF and digital hardware. System implementations, such as the digital receiver topologies and the proposed air interface, are also discussed. Finally, the digital algorithms for the receiver are described for acquisition, synchronization, and data demodulation.

One of the important issues to keep in mind while reading this chapter is the lack of performance criteria set out from the beginning in terms of synchronization and BER performance. There were no explicit characteristics to optimize, as the original design is considered more of a testbed with its tremendous amount of flexibility. Therefore, the receiver is left open-ended for communication system and software algorithm design, although there are arbitrary suggestions in this chapter to achieve the design criteria proposed in Chapter 1.

4.2 Receiver Design Concept

To help explain the basic idea behind the UWB receiver design, this section was included to assist with the conceptual background for some of the decisions made during the design process. Two different sampling techniques are discussed, including the advantages and disadvantages of each. The use of Commercial Off-The-Shelf (COTS)

parts was necessary due to the lack of resources in the lab for designing and manufacturing custom integrated circuits (IC). This placed some constraint on the receiver design as we will see.

4.2.1 Sampling Techniques

The UWB receiver design discussed in this thesis is based on a sampling architecture with digital demodulation. The basic concept is to oversample the analog received signal (sampling at a rate greater than the Nyquist frequency) and then perform demodulation in the digital domain. Sampling the received signal may be accomplished using a Direct Sampling or a Parallel Time-Domain Sampling approach.

4.2.1.1 Direct Sampling

This method involves sampling the received signal at a very high rate of 10-20 GHz with a 1-4 bit ADC. The overall waveform is essentially preserved and demodulation in the digital domain may be performed. The major challenge in the Direct Sampling approach is implementing a very high speed data bus on the order of 10-80 Gbps. For the best performance, the ADC and digital demodulation hardware should be implemented on a single IC, where the designer has very tight control over signal propagation delay and skew. If an implementation based on COTS components was used, the ADC and digital processing hardware will be on separate chips, and a high-speed data bus must be developed on the circuit board. While implementing such a high-speed data bus on a PCB is possible, taking care of clock synchronization, distribution, and signal propagation delay is a major design challenge. Therefore, the Direct Sampling approach is ideally suited for a custom designed IC approach, which cannot be implemented using the resources in the lab.

4.2.1.2 Parallel Time-Domain Sampling

The idea behind Parallel Time-Domain Sampling is to relax the requirements on the data bus while still sampling the received signal at a very high rate. Essentially, the received waveform is sampled by a number of ADCs operating in parallel, with each ADC clock slightly offset from the others. Thus, each ADC samples a slightly different

point of the time-domain waveform, and the effective sampling rate is the individual ADC sample rate multiplied by the total number of ADCs, as illustrated in Figure 4.1 and Figure 4.2 with a set of 4 ADCs. This technique can also be implemented by delaying each incoming signal in time with each ADC sampling a different part of the waveform, which will be discussed later in more detail.

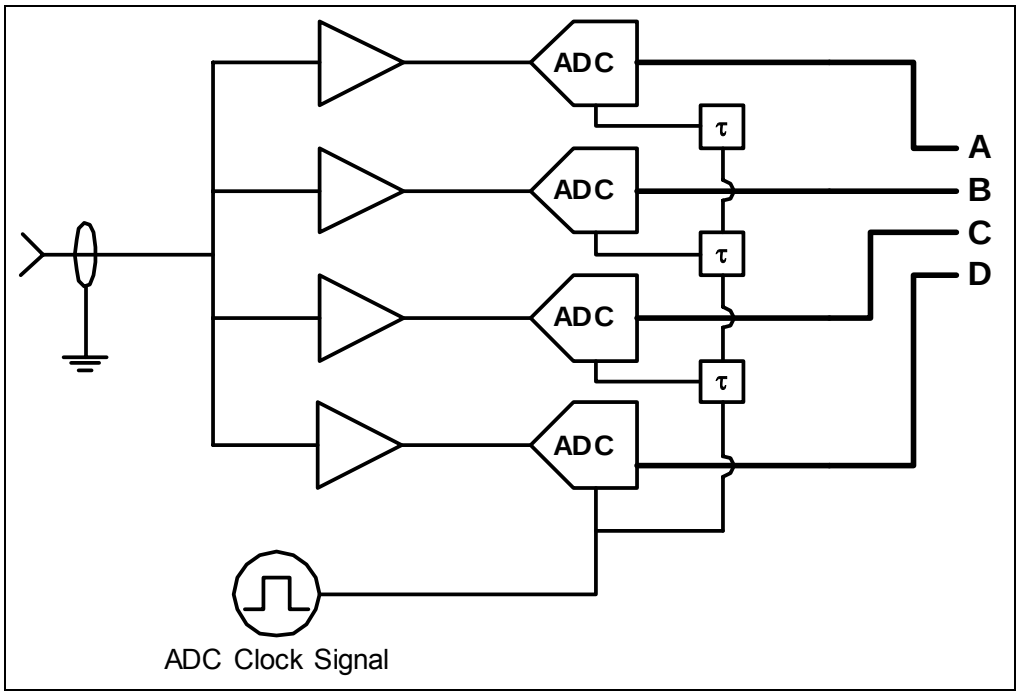


Figure 4.1. Block Diagram of the Parallel Time-Domain Sampling Technique Utilizing Four ADCs [17]

ADC #1 samples the received signal at point A as shown in Figure 4.2a. ADC #2 has a clock signal delayed by a small interval, τ, as compared to ADC #1, and will sample the received signal at point B (Figure 4.2b). ADC #3 has a clock signal delayed by the same small interval τ as compared to ADC #2 (2τ as compared to ADC #1), and will sample the received signal at point C (Figure 4.2c), and so forth. The data bus which connects each ADC to the digital hardware is able to run at a much lower rate. Additionally, the digital hardware can recreate the received signal as if it had been sampled by a single, high-speed ADC (Figure 4.2e). While the Parallel Time-Domain Sampling technique adds hardware complexity, it significantly relaxes the timing requirements of the data bus as data is being transferred at the parallel sampling rate. As an example, if a UWB signal was sampled at 8 GHz using COTS components, the Direct

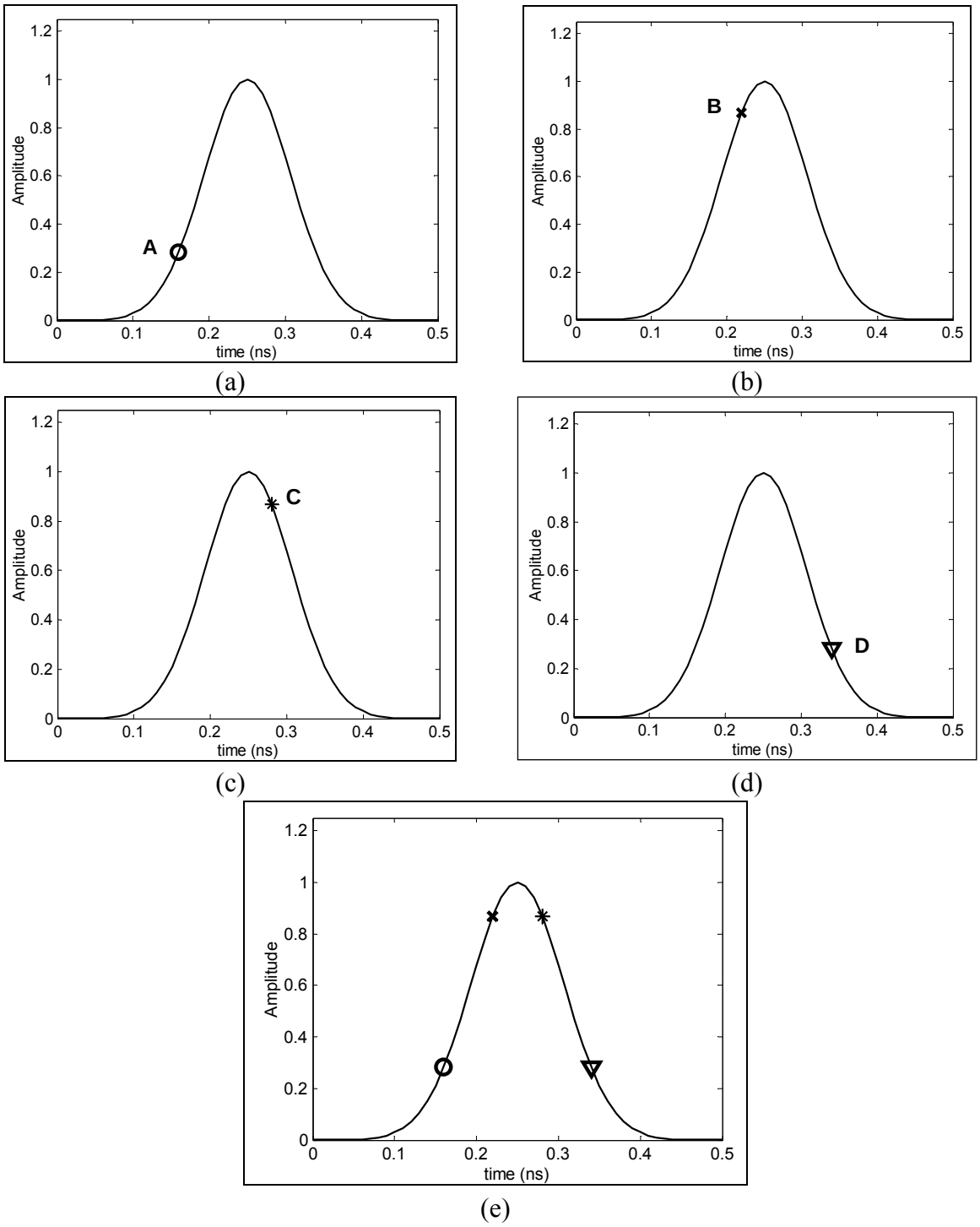


Figure 4.2. Graphical Representation of the Parallel Time-Domain Sampling Technique [17]
(a) ADC #1 samples the signal at Point A
(b) ADC #2 samples the signal at Point B—a time offset of τ relative to ADC #1
(c) ADC #3 samples the signal at Point C—a time difference of τ relative to ADC #2
(d) ADC #4 samples the signal at Point D—a time difference of τ relative to ADC #3
(e) The original waveform may be reconstructed by putting all 4 samples together

Sampling technique would need a single transmission line data bus capable of transferring 32 Gbps for 4-bit resolution. In the Parallel Time-Domain Sampling scenario using 8 ADCs, 32 transmission lines are used for the data bus but must only be capable of operating at 1 Gbps. Another advantage of parallel sampling is the reduction in data rate relaxes the data input timing requirements of the signal processing hardware. For these reasons, the Parallel Time-Domain Sampling technique is better suited to a COTS implementation.

4.2.2 COTS Limitations

Two of the vital receiver components, the ADCs and the digital processor, along with the clock distribution hardware have parts commercially available to meet the system requirements. However, the use of these components, even ones with optimal specifications, places some significant constraints on the overall system design.

4.2.2.1 Analog to Digital Converter

The primary limitation of a practical ADC is the analog input bandwidth, or the range of frequencies which the ADC can sample a signal with very little loss in fidelity. Most mass-produced commercial grade ADCs, such as those manufactured by Analog Devices or Texas Instruments, have input bandwidths on the order of DC—500 MHz. The highest performance commercially available ADCs, manufactured by Atmel or Maxim, can have input bandwidths which extend into the 2—3 GHz range. Higher performance specialized ADCs are available, however, the increase in cost is significant. Therefore, using a commercially available ADC restricts the UWB communication system to utilizing a baseband UWB pulse of below 2—3 GHz or greater than 333—500 picoseconds (ps) in time duration depending on the choice of ADC.

Another limitation of a practical ADC is the aperture delay variation. The aperture delay is the time delay between the rising edge of the ADC clock signal and the point where the ADC actually samples the input signal. For a system utilizing a single ADC, aperture delay is a minor concern. For the Parallel Time-Domain Sampling technique, the performance of the receiver is predicated on each ADC sampling the received signal at precisely spaced intervals. If the aperture delay on each ADC is

constant, the time between samples remains constant, causing the aperture delay variation to be zero. However, if the aperture delay varies significantly among ADCs, then the received signal will become distorted because the time spacing is uneven. Typical ADCs with sampling rates on the order of 100 MSamples/sec or greater possess an aperture delay variation ranging from 50 ps to 1 ns. The performance of a digital receiver will severely degrade if the aperture delay variation is greater than the sampling rate, causing samples to overlap in time.

4.2.2.2 Digital Processing

The heart and soul of the receiver is the digital processing hardware; as it must be capable of handling multiple data streams from the ADCs and then demodulating the data in real time. In order to meet the design objectives, the digital processing must also be reconfigurable, in order to provide the flexibility demanded by a software radio design. Given these limitations, a powerful FPGA is the optimal choice for the digital processing block on the receiver. Current top-of-the-line FPGAs are capable of handling multiple high data rate input streams, have several embedded processor cores for any DSP operations which may be required, and may be easily reconfigured for a variety of different modulation/demodulation schemes. Practical FPGAs are limited by the rate at which they can input data; and the maximum achievable data rate of the wireless link is limited by the time required to process and demodulate each received pulse. Xilinx, however, produces several FPGAs capable of inputting data at the rates used in the design presented in this thesis, as well as demodulating the proposed data rate of 100 Mbps.

4.2.2.3 Clock Distribution

As discussed above, the performance of the Parallel Time-Domain Sampling technique is highly dependant on sampling the received signal at precisely spaced intervals. Thus, an ultra-low skew clock distribution network is required. Manufacturers such as On Semiconductor produce clock distribution chips with pin-pin skew on the order of ± (10 – 20) ps. Additionally, constraint-driven routing of the clock signals on the PCB must be used to ensure that all trace lengths are synchronized. Eventually, this

will lead to routing difficulties on the board by needing to re-arrange components and traces accordingly.

4.3 Receiver Design Specifics

The receiver hardware is divided into three separate sections: the RF Front End, ADC/Clock Distribution, and Digital Processing. Figure 4.3 illustrates the overall block diagram of the receiver, with the basic function of each of these sections discussed below.

4.3.1 RF Front End

The RF Front End is composed of a series of broadband amplifiers, a bandlimiting filter, a broadband variable gain amplifier/variable attenuator, and a power divider. The ERA-4SM Mini-Circuits amplifier, which acts as a low-noise amplifier (LNA), is crucial to ensuring both the longest possible range of the communication link by minimizing the amount of noise and distortion added to the received signal. Originally, a broadband LNA was used in the design, although it was removed for the cheaper ERA-4SM Mini Circuits part. The gain is recovered in the latter stages of the receiver before the power splitter, as five gain stages are used in series. To limit the reflections on-board, a 3 dB attenuator was placed in-between each amplifier as an isolation device. A Mini Circuits ceramic filter bandlimits the incoming signal and limits the input noise. Additionally, the variable gain amplifier/variable attenuator allows the receiver to reduce the overall gain of the RF Front End to avoid overdriving the ADCs. The power divider then sends the signal through a series of delay lines to the ADC bank. These delay lines will likely be made out of hard-line coaxial cable, the same form of signal transmission used by many digital oscilloscopes. They will be cut to the specific length of the time delay needed based on their propagation delay properties. To perform the parallel sampling, the delay lines present each ADC with a slightly delayed version of the input waveform. Delaying each input signal with respect to the previous one in the chain is essentially identical to successively delaying each ADC's clock signal, but removes the hassle of precision clock distribution and routing.

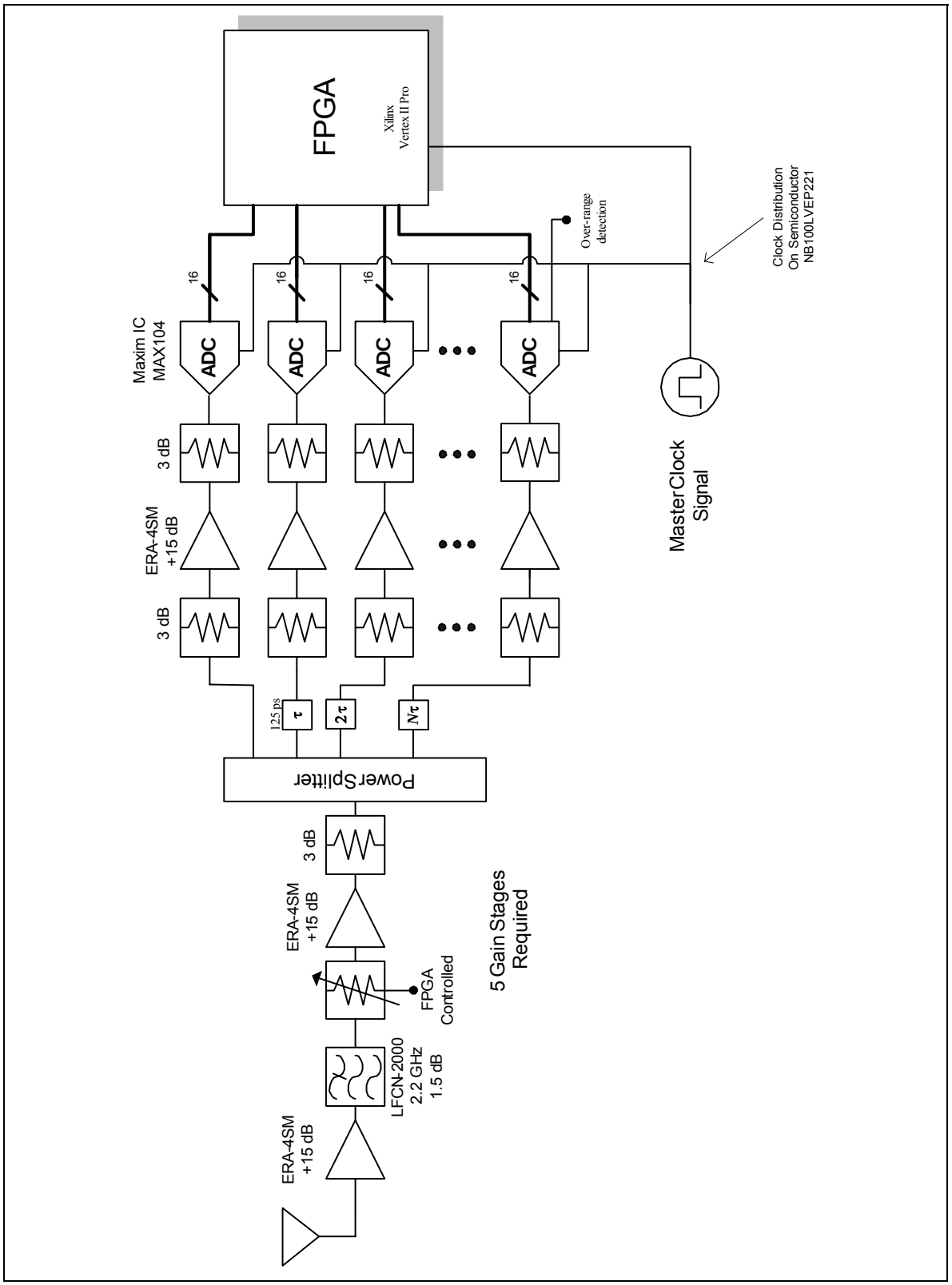


Figure 4.3. Basic Block Diagram of the UWB Receiver [17]

4.3.2 ADC/Clock Distribution

The most critical part of the receiver is the bank of ADCs and clock distribution network which will be responsible for parallel sampling the received UWB pulse. As discussed above, the proper selection of an ADC is significant to the optimal operation of the receiver. Furthermore, the cost of the ADC is extremely important, since a number of them will be used on a single receiver. After a thorough search, the Maxim 104 ADC was found to offer an input bandwidth of 2.2 GHz, a maximum sampling rate of 1 GHz with 8-bit quantization, an aperture delay of 100 ps with part-to-part variation of less than 30%. With 8 of the Maxim 104 ADCs operating in parallel at an individual sampling rate of 1 GHz, each successive ADC's samples the signal at 125 picosecond increments, yielding an effective sampling rate of 8 GHz. Another benefit of the Maxim 104 is a demultiplexer feature that allows for two output data paths at half of the sampling rate. This will allow digital data to be processed at a clock frequency of 500 MHz instead of 1 GHz, relaxing the input timing requirements of the FPGA. Obviously, the internal data processing will be more strenuous using this technique but should not present a problem if the FPGA software optimally recombines the samples.

As seen in the block diagram located in Figure 4.3, clock distribution will be accomplished using On Semiconductor's NB100LVEP221 low-skew clock distribution chip, which provides an output-output skew of less than 15 ps. Clock signal PCB trace lengths must be precise to ensure that each ADC is clocked at exactly the right instant in time.

4.3.3 Digital Processing Hardware

As discussed above, a software-defined radio implementation of the receiver architecture provides a tremendous amount of flexibility over hardware-based implementations. For the UWB receiver design presented in this thesis, data demodulation is performed by reconfigurable logic—in the form of an FPGA—in the digital domain. This approach allows the user to choose between one of three different modulation schemes (OOK, biphase modulation, and binary PPM) as well as one of two

receiver topologies (Digital Leading Edge Detection and Digital Pilot-Based Matched Filter). Additional receiver topologies and/or Rake combining algorithms can easily be generated and downloaded into the FPGA—without making a single hardware change. The user then has the ability to match schemes and topologies based on application requirements or research interests.

Due to the nature of the Sampling Receiver design, the processing requirements are extremely strenuous. The FPGA must be able to handle the 32 ADC outputs (16 differential pairs from each ADC using the demultiplexer feature), at an individual data rate of 500 MHz and 8 bits/sample—an aggregate data rate of 64 Gbps. Furthermore, assuming a target raw data rate of 100 Mbps (using a pulse rate of 100 MHz), for real-time data transfer, the FPGA must be capable of demodulating data in under 10 ns. After surveying the available FPGAs on the market, it was determined that the Xilinx Vertex II Pro XC2VP70 was the best suited for the task. The Vertex II Pro XC2VP70 contains up to 996 high-speed I/O pins, 328 hardware multipliers, up to two 400 MHz PowerPC processor cores, and was designed especially for processing large amounts of data at very high rates. This is evident by the Vertex II Pro implementation of double-data rate (DDR) registers. These registers store data on the rising and falling edge of the clock, which allows for the FPGA clock to be run at 250 MHz to input 500 MHz data. Even though the clock timing requirements are relaxed using DDRs, the data must be stored within the allotted 2 ns time duration between samples. Performing a preliminary input timing analysis, the setup and hold times of the I/O blocks for the Vertex II Pro are 0.84 ns and 0.61 ns, respectively. This translates into 0.55 ns of extra standby time, sufficient for external input data. Internally, various hardware devices must be capable of transferring data from register-to-register on the order of 100 MHz, or the raw data rate since a parallel sampling technique is being used. The performance of the hardware devices necessary for this design is shown in Table 4.1. Even though all of these devices meet the transfer rate specification, the critical aspect of internal data processing is the software performance. The code must be written to eliminate any extraneous clock cycles and allow the hardware to operate in an optimal fashion. This timing analysis cannot be accomplished without the Xilinx System Generator [23] software package or by testing the FPGA hardware with fully-functional code downloaded to memory. With

confidence that the software will be properly implemented, the FPGA has the internal hardware to accommodate the proposed data rate.

Hardware Description	Register-to-Register Performance (MHz)
128-bit Adder	131
32:1 MUX	400
Multiplier 18x18 (with Block RAM inputs)	135
Block RAM	355

Table 4.1. Register-to-Register Performance of Internal FPGA Hardware

To reduce the difficulty of the circuit board design including 8 ADCs and an FPGA, both of which are ball grid arrays (BGAs), the design includes an additional FPGA on a different board. Therefore, two digital boards consisting of 4 ADCs and 1 FPGA each will be employed. The delay lines from the power splitter will be interleaved to supply more time to process data within the FPGA. As far as the digital processing goes, one FPGA will act as a master while the other will be a slave. This communication will take place using the Rocket I/O transceivers on each FPGA that will operate at 2.5 Gbps. Although no board-to-board transmission line has been firmly decided upon, a shielded twisted pair has been mentioned as the preferred method for connection between the FPGAs.

4.3.4 Digital Receiver Topologies

For the purpose of this system, two receiver topologies will be developed: Digital Leading Edge Detection (D-LED) and Digital Pilot-Based Matched Filtering (DPBMF). As discussed previously, one of the primary benefits of a software-radio approach is that additional receiver topologies are possible and may be easily downloaded into the FPGA.

In both receiver topologies, data from the ADCs will be read directly into Block RAM. When the DMF receiver is being utilized, one of the available PowerPC processors will be dedicated to processing the data from the pilot pulses, while the other will be performing pilot-based matched filter estimation and updating the template waveform, which will be detailed later in the chapter.

4.3.4.1 Digital Leading Edge Detection

For UWB communications, the basic D-LED receiver is the simplest of all UWB receiver architectures. The D-LED receiver sets a threshold and any incoming pulse which crosses the threshold is detected and demodulated as a data bit. The problem with the threshold reception technique is that noise spikes which happen to cross the threshold will also be erroneously detected as a data pulse (known as a "False Alarm" or "False Detection"). To mitigate the problem of false detections, the receiver must continuously monitor the input noise signal and set a threshold such that only a small percentage of false detections will occur, similar to a Constant False Alarm Rate (CFAR) RADAR system [24].

While the D-LED receiver is a relatively unsophisticated technique—subject to noise, interference, and jamming, it is an extremely simple implementation, requiring only a simple comparison (which could be implemented in the FPGA's logic gates) on every group of input samples. In a relatively noise-free and benign multipath environment, the D-LED receiver provides the fastest continuous data rates, as it requires no extended processing other than adaptively determining the threshold.

4.3.4.2 Digital Pilot-Based Matched Filter

The DPBMF receiver is similar to the matched filtering receiver which has been used in narrowband communications for many years. A digitized version of the transmitted pulsed is stored in the FPGA's memory; this reference pulse is then correlated with the received line of sight (LOS) and any multipath signals for acquisition and synchronization purposes. The correlation procedure is explained in further detail in Chapter 2, specifically Equation 2.15. Then, a data demodulation template is formed based on the pilot pulse shape by using an averaging technique. Included in the template are any resolvable multipath, which form a pilot-based matched filter estimation to combine all of the received signal energy to improve performance. It is well known that the matched filter is optimal in an AWGN channel. The challenge in UWB systems is that due to pulse distortion, the pulse shape is unknown. Even in non-line of sight scenarios, the averaging template should compensate for any pulse distortion in the

received data pulses since the pilot pulses are being used to determine the pulse shape. The primary drawback to DPBMF is the noisy template formed after averaging the pilot pulse waveforms. This extraneous energy causes the BER performance of the receiver to degrade due to the lack of correlation between the pilot-based template and the perfectly matched waveform. It will be shown in Chapter 5 that increasing the number of pilot pulses per frame minimizes this effect. The three important aspects of the DPBMF receiver—Synchronization, Pilot-Based Matched Filter Estimation, and Data Demodulation—will be discussed in detail below.

4.3.5 Air Interface

To initiate communication, the transmitter begins by broadcasting a long string of UWB pulses at a relatively low pulse repetition frequency. These pulses, termed acquisition pulses for the remainder of this thesis, will be detected by the receiver using the template sliding matched filter synchronization technique, which is discussed in section 4.3.6, as a valid UWB transmission and data acquisition will begin. Initial estimates of the channel response and delay spread are performed, which will determine the pulse rate for the subsequent transmission and relayed to the user. Otherwise, the multipath signals from a previous data pulse could overlap with the current data pulse (i.e. Intersymbol Interference) which could severely degrade performance. If the transmitter data pulse rate is higher than the estimated pulse rate at the receiver, the system will need to be re-powered at a lower transmission rate since there are no current plans for complex equalization techniques.

Once the acquisition pulses are acquired, the transmitter will send one superframe (explained shortly) containing a test sequence. At the receiver, one of the PowerPC processors will demodulate the test sequence to ensure that it was received error-free. If the data was valid, then the communication link is established and data transfer will begin. Otherwise, the receiver will output an error message indicating a faulty link and the system will be re-started.

To facilitate synchronization and pilot-based matched filter estimation, the transmitted pulses for data will be grouped into frames, with a representation of the low-duty cycle pulse period shown in Figure 4.4, where T_s is the pulse repetition period and

T_p is the pulse width. Figure 4.5a illustrates the basic structure of the UWB frame. Each frame consists of 960 data pulses, 48 pilot pulses, and 16 guard time slots where no pulses are transmitted, arbitrarily chosen because of the unspecified performance criteria in the design. The polarity of the pilot pulses will be either positive or negative, with a maximal length sequence (m-sequence) as an option for biphase modulation if the frame structure is revised. The maximal length implementation allows synchronization to be performed with more accuracy due to an improved sequence auto-correlation, as will be discussed in section 4.3.6. This sequence will be repeated every frame to allow the receiver to know the exact sequence of the pilot pulses throughout transmission. For binary PPM, the pilot pulses will be shifted in time based on a particular sequence, although we will focus on modulating the polarity of the pulses throughout the remainder of the chapter. A guard time equal to the time duration of eight pulses is positioned at the end of the pilot pulses as well as at the end of the frame. Since the pilot pulses are separated from the data pulses via the guard time, the receiver can develop a pilot-based matched filter template. Also, if synchronization between the transmitter and receiver is completely lost, the receiver can search for the pilot pulses (again because the guard time allows for easy differentiation from data pulses) and re-acquire the signal.

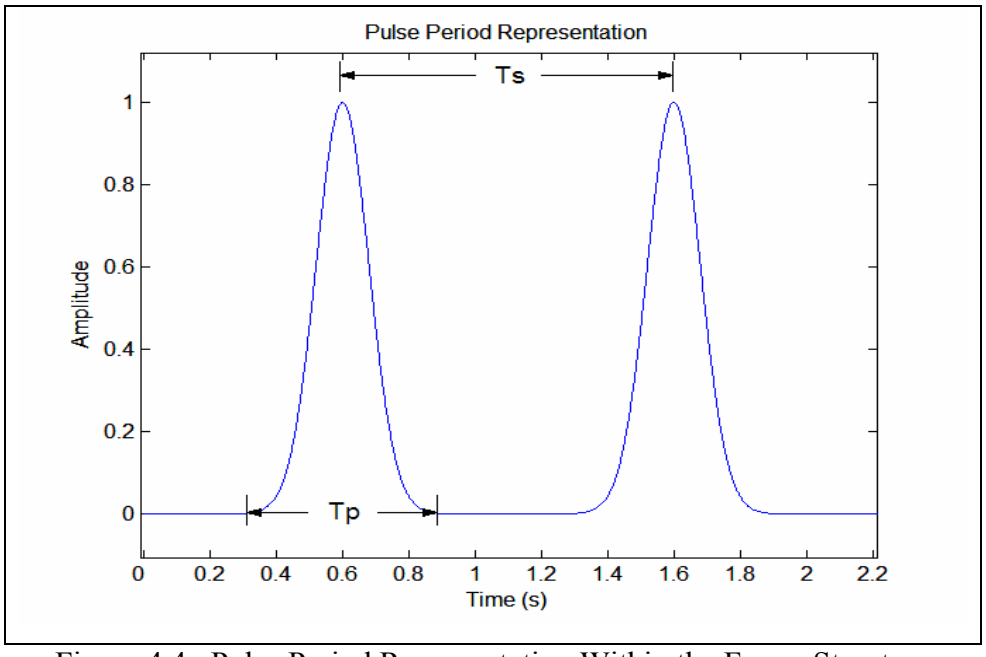


Figure 4.4. Pulse Period Representation Within the Frame Structure

Even though multiple access techniques are not the primary concern for the initial design, a superframe (Figure 4.5b) was created, which is made up of two regular frames. In the case of time division multiple access (TDMA), each user would transmit a superframe in the hyperframe, consisting of the same number of slots as users. Therefore, the overall data rate would reduce as the number of users increases. The superframe was included in the design to accommodate TDMA, even though other multiple access techniques can be used.

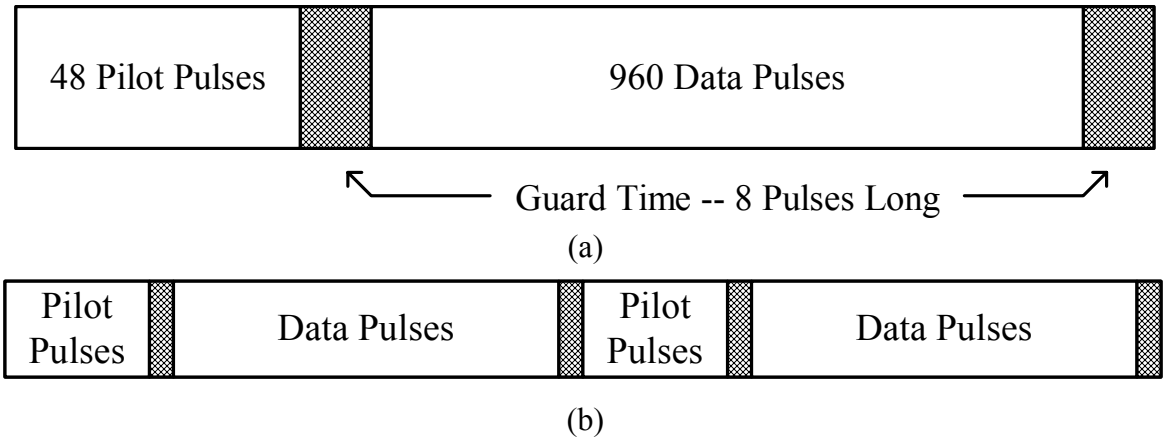


Figure 4.5. Air Interface for the UWB Communication System [17]
(a) UWB Data Frame, (b) UWB Superframe

One final note: The frame and superframe can be adjusted accordingly to change the data rate or allow for better BER performance, as will be seen in Chapter 5. The numbers for pilot, guard, and data pulses, as well as number of frames per superframe, were chosen somewhat arbitrarily and after further investigation, might be changed in the future to optimize system performance.

4.3.6 Synchronization

The synchronization routine begins by using a single pulse sliding matched filter technique demonstrated in Figure 4.6, as the expected received pulse shape stored within the FPGA internal memory is correlated with the incoming sampled data. The use of the "expected" pulse shape is necessary because there is no knowledge of the true pulse shape (i.e. after channel distortion) prior to synchronization. An algorithm is implemented to determine the location of the pulses based on a set threshold value. This

value is calculated from the first values stored in memory, as the matched pulse shape is correlated with randomly sampled noise to find a maximum noise correlation value. Then, the value is multiplied by a constant based on the standard deviation of the noise. Once a threshold is calculated, the first LOS pulse is found based on its correlation value and successive LOS pulses being periodically (or close due to aperture delay variation) separated in memory. While moving through the data, multipath are found as well and the corresponding indices are saved. The algorithm concludes when all of the pilot

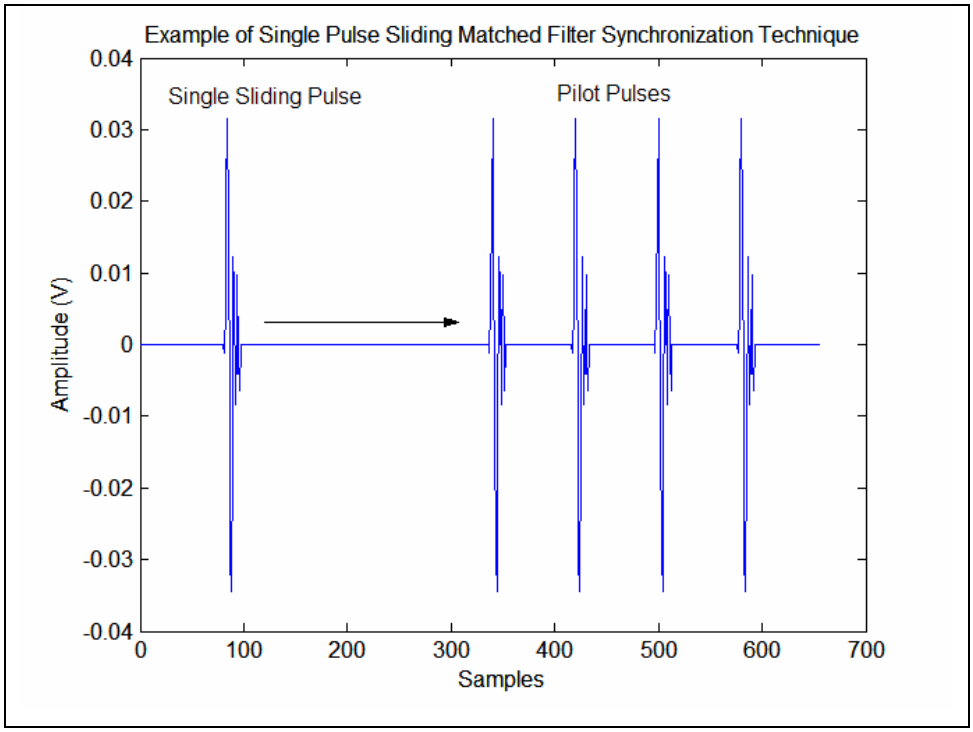


Figure 4.6. Illustration of the Single Pulse Sliding Matched Filter Synchronization Technique

pulses are calculated or the sliding matched filter pulse reaches the guard time where there are no more periodic correlations crossing the threshold. The start of the data index is found by taking the index of the last LOS pulse and adding the number of samples in the guard time. This synchronization technique is well-suited for lower noise applications because a more accurate pilot-based matched filter template can be formed by including only the necessary samples for data demodulation. If the single pulse sliding matched filter synchronization technique only detects an LOS pulse and a single multipath pulse within half of the amount of samples in a symbol period, a template can

be formed without the other half of the symbol period containing random noise. Without this unnecessary energy, a more accurate bit decision can be determined, increasing the BER performance of the system. Also, if this synchronization technique is successful, the receiver can inform the user of a lower noise channel. By doing this, fewer pilot pulses (need less averaging for the template since noise has less of an affect) are necessary within the frame, meaning an increase in data rate can occur with a change of frame structure. Also, using this algorithm can help determine the delay spread of multipath components and an adjustment in the pulse rate can be made accordingly.

Another synchronization algorithm is in place to calculate the start of the data index in the case of noisy channels called the template sliding matched filter technique, shown in Figure 4.7 below. This algorithm is implemented when all of the LOS pilot

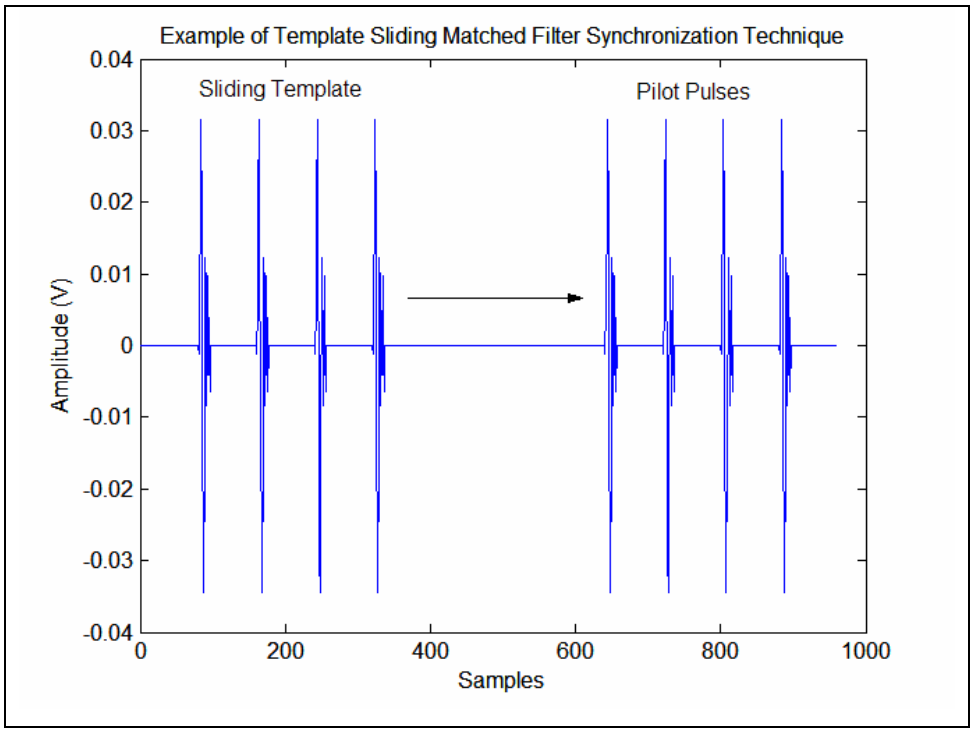


Figure 4.7. Illustration of the Template Sliding Matched Filter Synchronization Technique

pulses in the previous algorithm are not detected. When this occurs, a template with the number of pilot pulses is formed using the expected pulse, including the polarity of the pulses. When the template is correlated with the received data, the cross-correlation function is similar to an impulse, illustrated in Figure 4.8 below using the simulated pulse

shape shown in Figure 5.3. Note that the maximum point is the index where the template and the pilot pulses align. The algorithm moves through the data every sample and ends a specific number of pulses after a pre-determined threshold is crossed. This threshold was found by computing synchronization curves consisting of the probability of detection versus the probability of false alarm. Using the 48 pilot pulses suggested in this chapter, these curves were simulated and the results are given in Chapter 5. Once the threshold has been exceeded, the start of the data index is determined by taking the threshold crossing index and adding the sampled length of the pilot pulses and guard time.

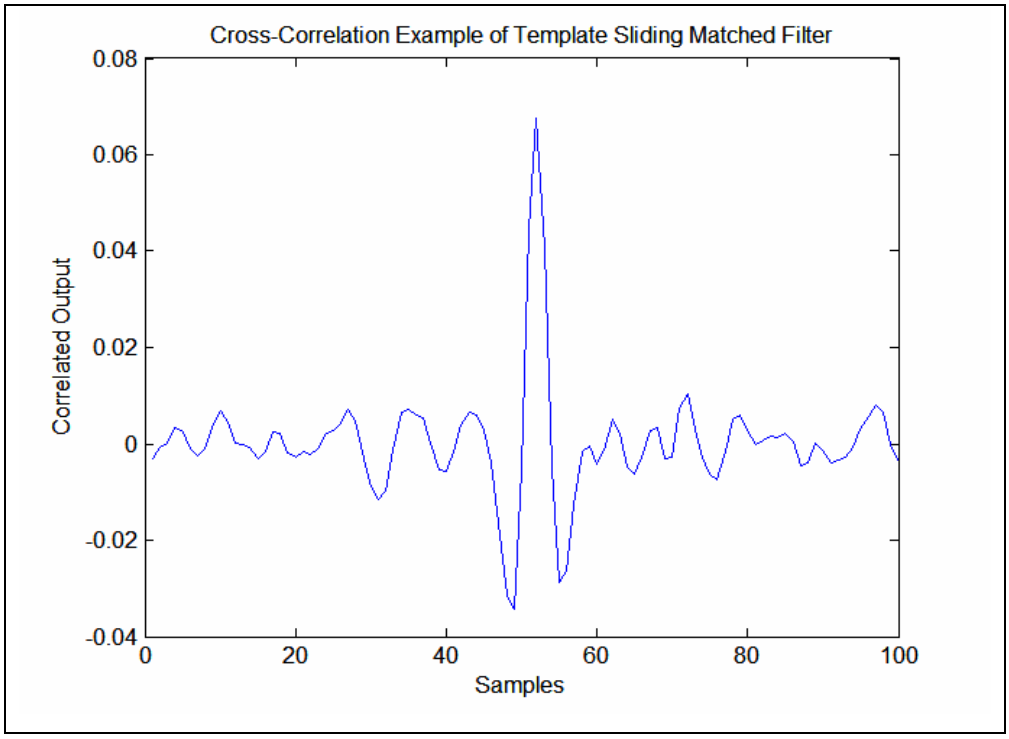


Figure 4.8. Cross-Correlation Output of the Template Sliding Matched Filter Synchronization Technique Using Gaussian Doublet Pulse Shape

Finally, the PowerPC processor within the FPGA will continuously monitor the number of samples between successive UWB pulses and fine tune the master clock signal or the start of the data index. This will be accomplished using an early-late algorithm in data demodulation (explained in further detail in section 4.3.8) where multiple templates are correlated with the data. For example, at a pulse rate of 100 MHz, there will be exactly 80 samples between the start of any two successive UWB pulses. If the processor observes a trend of more or less samples between pulses, then either the master clock

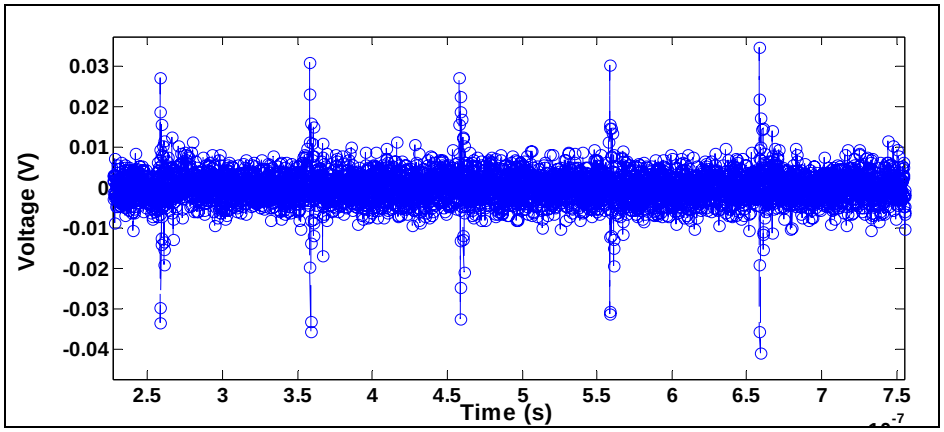
signal can be fine tuned or samples can be added or subtracted in memory to bring the stored waveform back into alignment.

4.3.7 Pilot-Based Matched Filter Estimation

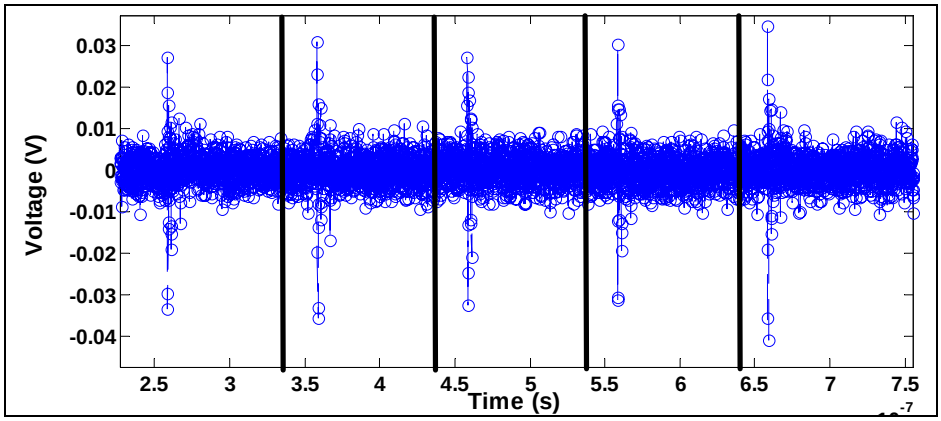
Pilot-based matched filter estimation will be performed every frame by a second dedicated PowerPC processor. By examining samples of the pilot bits, the PowerPC processor can establish an estimate of the pulse resulting from the channel multipath. Based on the pilot pulses, a template waveform is generated for the matched filtering operation to process data for the following frame. Due to lack of time between pilot and data pulses, the pilot-based matched filter template will be updated while a different PowerPC processor is determining bit decisions for the current frame. This template will then be used to process data for the following frame. Therefore, data is demodulated using the pilot-based matched filter template from the previous frame, not the current one. This should not be an issue in channels with low Doppler spreads (i.e. low mobility).

It is important to note the pilot-based matched filter template algorithm is slightly different depending on the method of synchronization the receiver uses. If the single pulse sliding matched filter technique is used, the length of the template is based on the indices provided from the synchronization algorithm given the number of multipath detected. The template waveform is then created by breaking the pilot pulses into segments which contain the correct array length. These pilot pulse segments are then averaged together to create the matched filter template waveform. Figure 4.9 is a simplified graphical illustration of the template generation process, with the end result being a low-noise template with a channel estimate including two multipath. Averaging reduces the effects of AWGN present in the channel and helps to minimize the aperture delay variation in the receiver.

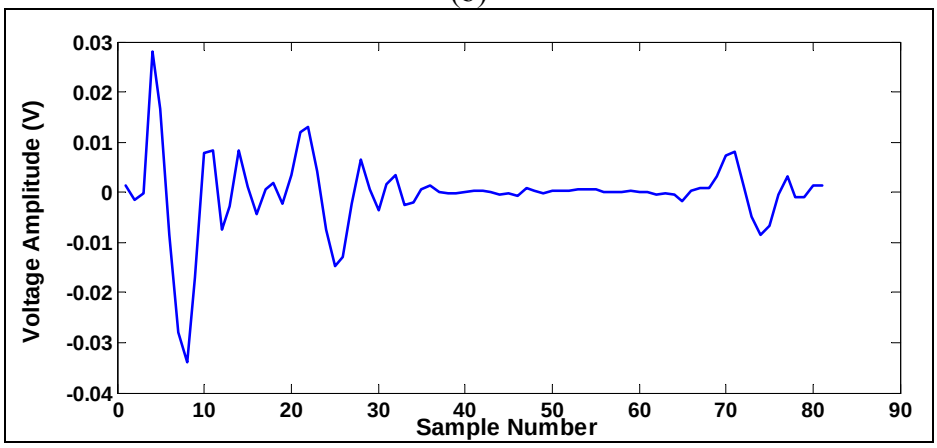
If the template sliding matched filter synchronization technique is necessary, a pilot-based matched filter template using one entire symbol period (80 samples at a pulse rate of 100 MHz) is used. Using the entire symbol period to generate the template waveform allows the receiver to capture all or nearly all multipath energy in the channel. However, if no multipath energy is present at the receiver, the additional samples cause



(a)



(b)



(c)

Figure 4.9. Graphical Representation of the Template Generation Process [17]
(a) Five pilot pulses recorded by the receiver
(b) Each of the five pilot pulses is broken down into one-symbol segments (denoted by the vertical bar)
(c) The one-symbol segments are averaged together to create the template

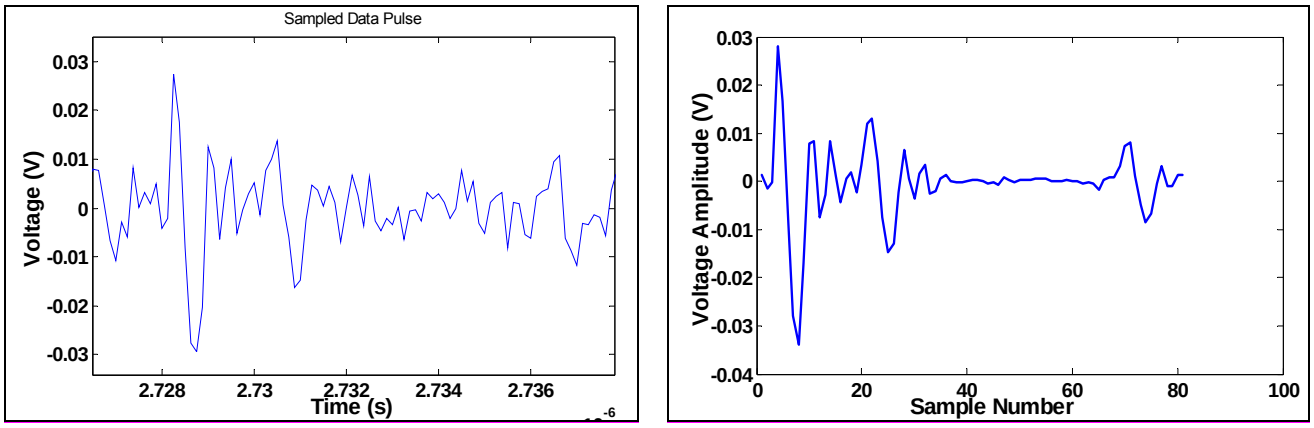
more bit errors due to the additional noise in the data demodulation calculation. This is the primary reason the single pulse sliding matched filter synchronization technique is included, as it only includes the samples containing energy.

4.3.8 Data Demodulation

Data demodulation is accomplished depending on the receiver topology of choice. Using the D-LED method, demodulation is performed by using the start of the data index and comparing it to threshold value. This value is based on the received pulse amplitude and the standard deviation of the noise. The data index will be incremented based on the number of samples per pulse period and the expected number of samples between a "1" and a "0" if using binary PPM. Bit decisions are made based on the selected modulation technique, as OOK and biphase modulation are compared to the threshold value, which is half of the pulse amplitude and zero for each, respectively. In the case of binary PPM, two sample values for each pulse are taken and they are compared to each other. The higher sampled value will be chosen as the correct bit.

The DPBMF technique is more complex, as data demodulation is achieved through a matched filtering operation. The receiver uses the pilot-based matched filter template to determine bit decisions by performing the correlation calculation described in Equation 2.15. An example of a LOS pulse plus two distinct multipath signals is shown in Figure 4.10. Figure 4.10a shows the received waveform (with added noise) and 4.10b shows template waveform generated by the pilot-based matched filter estimation algorithm.

Using the Vertex II Pro XC2VP70 in the design, there is an estimated ± 30 ps of aperture delay variation. Therefore, since the sampling time of the receiver is 125 ps, it is conceivable that the data index with the highest correlation value could be ± 1 sample from the true time delay. To help compensate for the effects of the aperture delay variation, the template waveform will be replicated, with each replica offset from the ideal timing by one or more samples. This process, referred to as an early-late algorithm, uses each of the templates to perform the matched filtering operation with the received pulse. Ideally, the FPGA will perform all matched filtering operations in parallel and then examine the results to determine the maximum correlation.



(a) (b)

Figure 4.10. Pilot-Based Matched Filtering of the Received Pulse [17]
(a) Received UWB signal along with 2 multipath signals and added noise
(b) Template generated by the FPGA based on the Pilot-Based Matched Filter Estimate

For example, at a pulse rate of 100 MPulses/sec, each UWB pulse period will occupy time duration of 80 samples. Since the FPGA has 328 multiplier blocks to perform a correlation operation, three matched filtering operations can be done in parallel using 240 multipliers. An odd number was chosen to create templates symmetrically around the original one. Thus, three templates will be generated (illustrated later in Figure 5.7):

- one template advanced in time by 1 sample
- one template with the ideal timing
- one template delayed in time by 1 sample

The receiver then performs a matched filtering operation by correlating the received UWB pulse with the template. As can be seen in Figure 4.6, these two waveforms will correlate much higher than a single pulse alone, as the energy from multipath is included in the calculation. Each of the matched filter outputs will then be examined and the one with the strongest correlation will be chosen for data demodulation. The index of the strongest correlation will be used for tracking, as previously mentioned. The matched filter outputs could also be averaged or combined together to help mitigate the effects of aperture delay variation in the ADCs. As a side note, this algorithm must be performed twice for binary PPM at different indices depending on the time between data pulses.

To speed up the correlation process, multiplications will be performed in parallel using the FPGA's block of dedicated multipliers. The resulting output will be summed using the internal hardware adders and a decision routine will determine if a "1" or a "0" was received.

After determining the correct correlation value using the time-shifted template algorithm, bit decisions are made based on the modulation technique employed. For OOK, half of the maximum correlation value is used as a threshold to decide on a bit outcome. Since opposite polarity pulses are used for biphase modulation, bit decisions are made using a threshold of zero. A bit decision for binary PPM is a comparison of correlation values from each of the positions in time. The higher correlation value results in the position where the pulse should be located.

4.4 Conclusion

The two sampling methods considered for this software radio based system were described at the beginning of the chapter with the Parallel Time-Domain Sampling technique being more practical using COTS parts. Using this approach, other limitations were placed on the design due to a COTS implementation, as certain parts created design difficulties. After a discussion on the receiver concept, the receiver hardware was detailed, including the critical components such as the ADCs and FPGA. Digital receiver topologies such as D-LED and DPBMF, along with the general frame structure, were proposed for receiver algorithm implementation in this chapter. Since the design utilizes a digital receiver, sections on algorithm design were incorporated for the acquisition, synchronization, and data demodulation techniques. In conclusion, the receiver design presented will supply the flexibility of software-defined/reconfigurable radio with the high data rates and low power spectral density advantages of impulse-based UWB communication.

Chapter 5 System Design Testing

5.1 Introduction

In this chapter, the system simulation created for receiver design testing is outlined, as two software packages were used to accurately simulate the transmitter and receiver. Also included is a description on how the data was generated and the type of channel used. Although the information for the simulation is presented in this chapter, Appendix B contains the ADS schematic and a listing of the necessary Matlab files. Results from synchronization curves to find acceptable threshold values are illustrated in the section 5.3. Finally, to verify the receiver design and perform a comparison with other systems, BER curves were generated using the simulation.

5.2 System Simulation

System simulation was performed to verify the design of the UWB system that has been outlined in this thesis. The software packages Agilent ADS and Matlab were the primary tools to determine design modifications, validate software algorithms, and confirm the overall proof-of-concept for the system. A block diagram describing the procedure of each software package is shown in Figure 5.1 below. This section will feature details of the functions labeled within each block. The general details of the system simulation are a data pulse rate of 100 MPulses/sec, a 118.55 μs time duration (12111 total pulses) with a 25 ps time step. Both biphase modulation and binary PPM can be used as the modulation technique and the number of multipath components is variable. The Digital Pilot-Based Matched Filtering receiver topology is employed due

to the use of a Vivaldi antenna, which receives Gaussian monocycles. These pulse shapes cannot be used by the digital leading edge detection technique because of they include both positive and negative voltages with relatively equal amplitudes unless OOK is employed, which is not a valid modulation scheme in the system simulation.

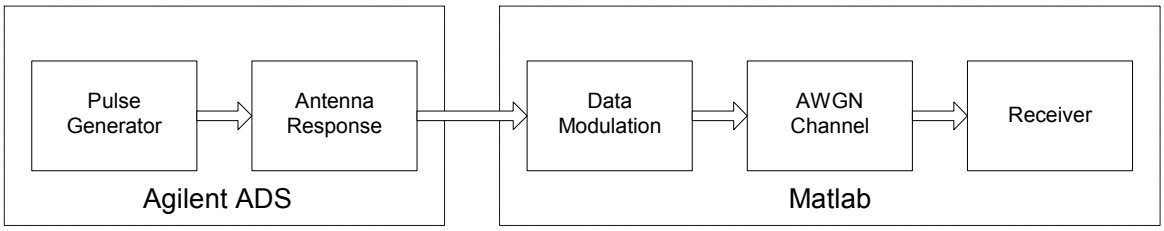


Figure 5.1. System Simulation Procedure

5.2.1 Transmitter

The transmitter was simulated in Agilent ADS due to its well-known capabilities of simulating RF circuitry. Two project files were formulated to determine the performance of the SRD pulse generator and the transmitter as a whole.

The components simulated for the SRD pulse generator were discussed in Chapter 3 and shown in Figure 3.2. Figure 5.2 below displays the simulated output voltage on the 50 Ω load resistor. The result from the SRD pulse generator was a 100 MPulses/sec pulse train with very little noise and amplitude of approximately 3.5 volts. It is important to note these simulations were performed prior to the transmitter circuit board testing, which is why the pulse amplitude is larger than the result shown in Figure 3.10. Many simulations were conducted to tweak component values in an attempt to determine the robustness of the circuit design, as the pulse shape was preserved throughout the evaluation. Numerous other simulations were performed to increase the frequency of the SRD pulse generator for a future generation system with high data rates. Although the amplitude of each pulse was reduced, the pulse shape remained in tact at 400 MPulses/sec with some slight modifications in the circuit design.

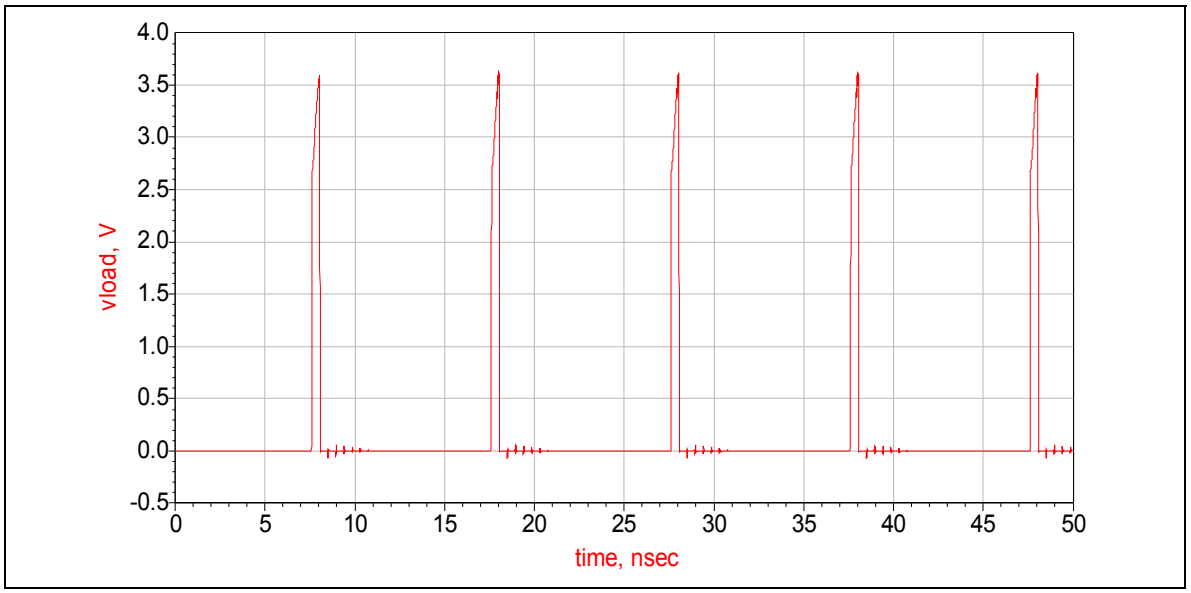


Figure 5.2. Simulation Results from SRD Pulse Generator at 100 MPulses/sec

In addition to the SRD pulse generator, two low pass filters, an amplifier, and a differentiator were added to simulate the transmitter. The differentiator represents the impulse response of a Vivaldi antenna, which is a likely choice for the UWB system when high data rate is a priority due to its narrow beamwidth. The gain value for the differentiator was found by calculating the power loss in the impulse response of two Vivaldi antennas [19], one as the transmit and the other as the receive antenna. This was achieved using the frequency response plot, where it has been shown an approximate 10 dB loss at 1.2 meters up to 2 GHz, where the pulse is bandlimited. In the simulation, the input to the differentiator has a 2 volt peak, which translates to a 450 mV peak-to-peak Gaussian doublet after the 10 dB loss using the average normalized power equation per pulse period for evaluation [14]:

$$P = \frac{1}{T} \int_{-T/2}^{T/2} s^2(t) \quad dt \tag{5.1}$$

where:

P	is the average normalized power per period (Watts)
T	is the pulse period (seconds)
s	is the pulse waveform (volts)

Equation 5.1 was used to calculate the average power in the 2 V Gaussian impulse which was translated into the power in a Gaussian doublet, where the pulse period used was 10 ns. The constant differentiator gain to satisfy this equation was $1/(33 \cdot 10^9)$. After including this value in the schematic, specifications from each of the components were input into each of the ADS component models to realistically simulate the transmitter.

In Appendix B, the transmitter schematic is shown in Figure B.1, with the component models and two additional components on the output. The component models located at the bottom of the schematic are printed circuit board and diode specifications to accurately simulate the transmission lines, SRD, and Schottky diodes. With the assumption that the amplifiers and channel frequency response are linear, the series of ERA-4SM Mini-Circuits amplifiers at the receiver and the attenuation due to path loss (calculated at 10 meters) were also added to this part of the simulation for overall simplicity. A path loss equation was found based on the free-space Friis transmission formula, given in Equation 5.2 below:

$$P_r = P_t G_r G_t \left(\frac{\lambda}{4\pi d} \right)^2 \tag{5.2}$$

where:

- P_r is the received power (Watts)
- P_t is the transmitted power (Watts)
- G_r is the gain of the receive antenna
- G_t is the gain of the transmit antenna
- λ is the wavelength (meters)
- d is the distance between the receiver and transmitter (meters)

under the assumption the antenna has a constant gain over the bandwidth of interest. The gain of each antenna is related to the frequency by:

$$G_A = \frac{4\pi A_e}{\lambda^2} \tag{5.3}$$

where:

- A_e is the effective aperture area of the antenna (meters^2)

Using Equation 5.3, the assumption made is that the effective aperture area reduces by a squared factor as the frequency increases. This claim is supported by [19], as the frequency response can be assumed to be constant around 2 GHz. Even though this assumption is not precise, it leads to a semi-accurate path loss value, which is not consequential to the simulation performance results due to the use of E_b/N_o as a calibration point, only the accuracy in terms of received signal amplitude, which is not considered significant for this simulation.

If the constant antenna gain assumption is made, the loss in the channel can be found by dividing the received power by the transmitted power, which in dB is:

$$L_p = 20 \quad \log \quad \left(\frac{4\pi d}{\lambda} \right) \tag{5.4}$$

where:

L_p is the path loss

Since the baseband pulse contains frequencies up to 2 GHz, the maximum frequency was used to compute the 58.5 dB final value since it provides the worst-case scenario. Both the path loss and receiver amplifier functionality could have been performed in Matlab with additional work but equal or less accuracy.

The transmitter file was executed based on the three different segments of the incoming waveform necessary to accurately simulate the system. In the first file, the transmitter simulation was run at 10 MPulses/sec with a 250 ns delay to demonstrate the acquisition pulses sent at the beginning of transmission for acquisition and pilot-based matched filter estimation. The pulse rate is variable but was made less than the data pulse rate as an accurate representation of the system. Secondly, the transmitter simulation was run at 100 MPulses/sec after a fixed time delay of 1.1 μs to represent the test frame, which is used to verify the proper operation of the system. Finally, the third run consisted of another time delay of 500 ns followed by data frames. The results from these files were saved to disk and transferred to Matlab, where the rest of the system simulation (i.e. the receiver simulation) was performed. It should be noted the following transmitted data in ADS does not include both positive and negative pulses. A pseudo-noise (PN) generator algorithm was used in Matlab modulate the pulses, as will be seen in the following section, again using the assumption of system linearity.

The transmitted pulse (before modulation) was not similar to the SRD pulse generator pulses due to the added ringing of the two low pass filters and the impulse response of the Vivaldi antennas. Figure 5.3 displays the waveform before the path loss and a series of ERA-4SM amplifiers as a clean, minimally distorted pulse train with exponentially decaying ringing. Although the peak-to-peak amplitude of the pulses was only 450 mV, a power amplifier could easily be inserted to boost the signal level further. With the pulse amplitude in the physical transmitter lower than expected, this addition is likely.

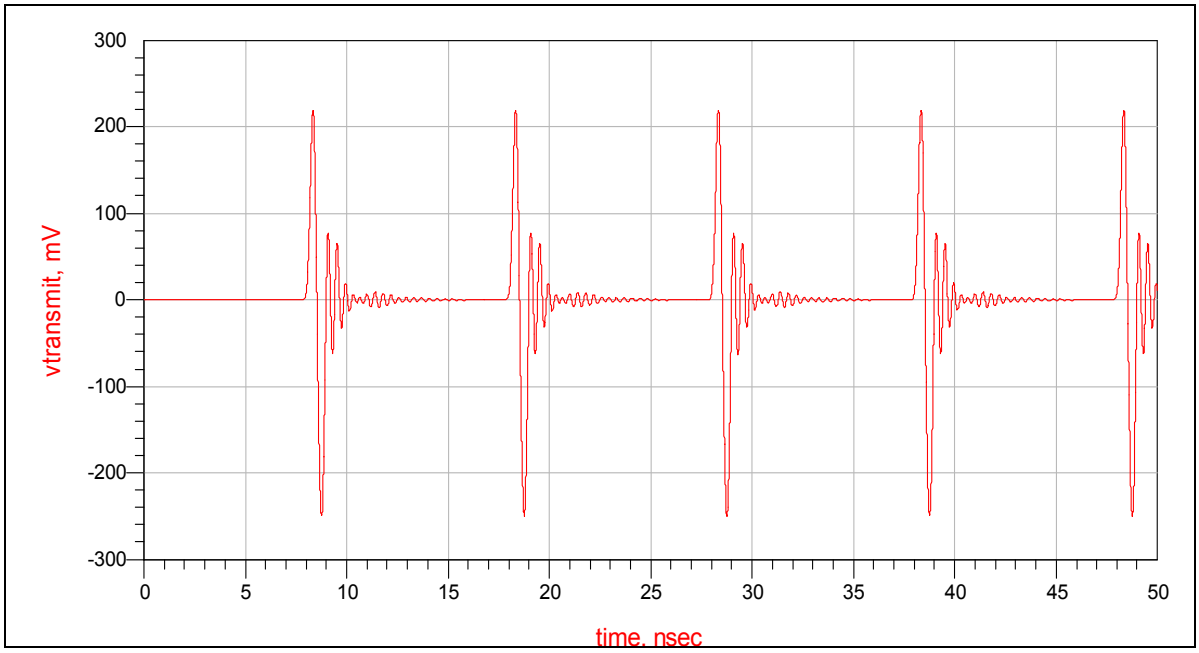


Figure 5.3. Simulated Results for the 100 MPulses/sec Pulse Train at the Output of the Receiver Antenna

5.2.2 Data Generation

The data generation was performed in Matlab for simplicity and flexibility when running simulations. As an example, it is much easier to place data on pilot pulses within Matlab and synchronize at the receiver if the data used on the pilot pulses is already available. Also, this implementation gives the capability to change modulation schemes and the number of multipath without having to re-run ADS and store more data files. Located in Appendix B, a list of the m-files necessary for the execution of the simulation is provided.

The system simulation in Matlab imported each of the three saved files from ADS and stored them in an array by appending each data file to the end of the previous one, creating one array including acquisition pulses, a test frame, and data frames. Then, the program set variables for the simulation such as the number of data frames, the number of multipath, and the modulation scheme. To modulate the pulses, indices and array lengths must be known or mistakes will be made such as changing the polarity of a pulse half way through its time duration. Values such as the period index, acquisition index, and delay indices were all calculated based on the simulation time step.

Since the overall goal of the simulation was to calculate BER curves based on the ratio of the energy per bit to the noise power spectral density (E_b/N_o), the noise generated in the ADS simulation had to be removed to accurately include the standard deviation of the noise in the data array, which will be discussed in further detail in the next section. Therefore, a function called place_zero was written to eliminate the noise from the imported data by placing zeroes around every pulse. The noise generated within the data pulse was left alone because it was considered to be part of the pulse itself. The remaining array then contained only data pulses with no extraneous noise in between.

To begin constructing the received waveform, data was generated to change the pulse polarity or position in time depending on the modulation scheme. A pseudo-noise (PN) generator algorithm was written in an m-file entitled pngen, to produce data bits. Since 960 data pulses were used per frame, a sequence length of 15 was selected since it was a divisible number, although any sequence length can be used in the simulation with slight modifications. The function outputs an array of the data bits and a PN waveform based on the period, which is shown below in Figure 5.4.

Depending on the modulation scheme of choice, two functions were used to create the frame structure and include data in the received waveform. For biphase modulation, a function entitled data_gen was used to place zeroes in the guard time, which was specified in the variables section. Then, data was placed on the received waveform, as the original pulses were simply multiplied by the PN sequence values for biphase modulation. In the case of binary PPM, the data array from the pngen function was used to shift the pulse within its pulse repetition period if the bit was a “0” using a function called ppm. In every situation, the pulse was shifted by one pulse width.

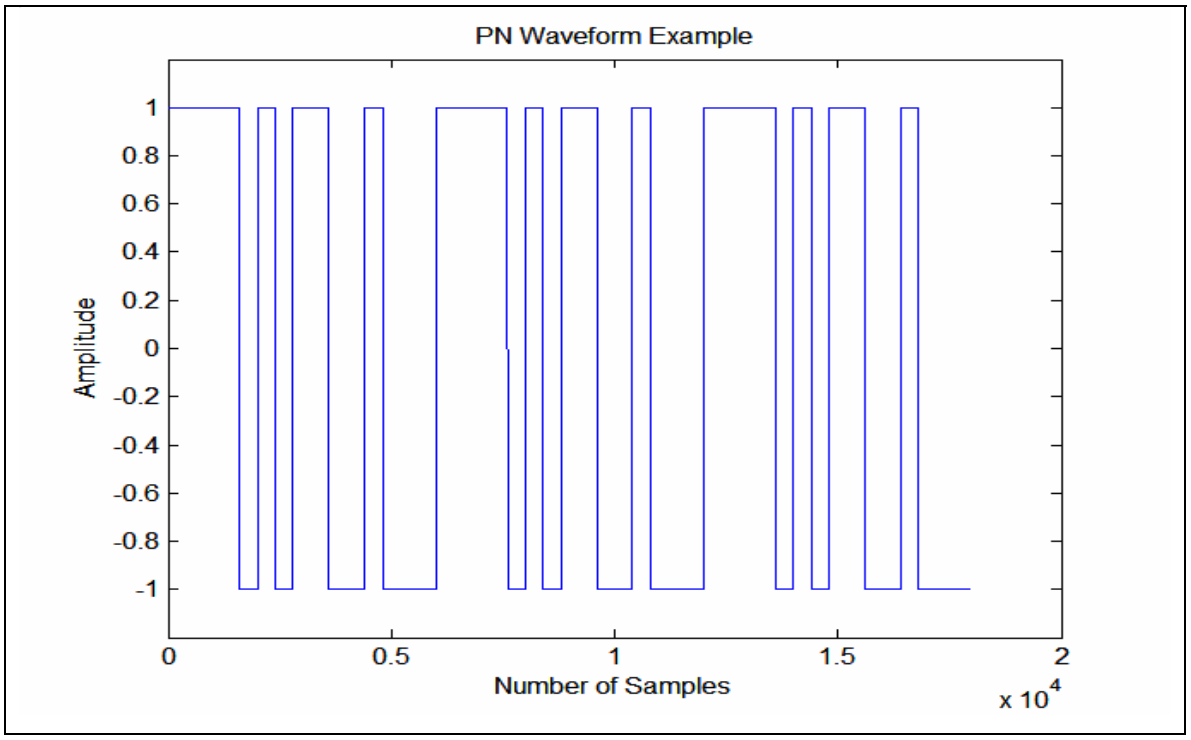


Figure 5.4. PN Sequence Example

Otherwise, the pulse remained in the same location in the array for a "1". The ppm function also eliminated the pulses originally placed in the guard time to create the proper frame structure.

Since the maximal length sequence for acquisition was not placed in the simulation until later, a function entitled pp_m_seq was established to change the polarity of the acquisition and pilot pulses. This function took the same PN waveform of length 15 and multiplied with the array containing both sets of pulses, similar to the data_gen function described. This function was employed for biphase modulation and binary PPM, although PPM would not use this in the physical system. It was necessary in this scenario to perform synchronization even at low E_b/N_o values used in generating the BER curves. Originally, the pilot pulses were all positive polarity, but the cross-correlation of the template waveform did not result in a peak, leading to the use of biphase pilot pulses. Even when using biphase pilot pulses, this is not the optimal way to polarize 48 pilot pulses, as some correlation will occur on either side of the peak, as will be shown later in Figure 5.9. However, due to the lack of time at the end of the semester and with a frame structure in place, using a previously generated PN sequence of 15 chips was the quickest

solution. To optimize this simulation, a maximal length sequence of 31 or 63 chips should be used with an equivalent number of pilot pulses (changing the frame structure) to produce one correlation peak. Also, the use of the same data and acquisition sequence would not be used in the physical system, as there is a possibility that the synchronization routine would lock onto the data pulses. This problem was eliminated in the system simulation due to the use of a guard time, which allowed the pilot pulses to be distinguished from the data pulses. Therefore, the auto-correlation of the pilot pulses contained a unique maximum, as a sudden decrease in correlation occurred when the template "slid" into the guard time.

5.2.3 Wireless Channel

Intertwined with the data generation code is the functionality to insert multipath into the signal. The multipath code began by ensuring the maximum number of multipath was not exceeded for each modulation technique. In the simulation, no more than four multipath are able to be used for biphase modulation using a 100 MPulses/sec pulse rate since the "received" pulse was slightly greater than 2 ns, as previously seen in Figure 5.2. Since binary PPM shifts the data pulse in time, only three multipath are able to be simulated using the same interference restriction. Although this number of multipath is small in comparison with a typical indoor channel, the pulse rate only allowed a few multipath without causing intersymbol interference.

Once the number of multipath were set, they were inserted using the create_mp function. In the create_mp function, a random array was created based on the number of vector elements (i.e. time samples) between each line-of-sight (LOS) pulse. An algorithm determined whether the indices generated were valid in terms of spacing without intersymbol interference. After determining the position of the multipath, their amplitude was randomly selected within a pre-determined range smaller than the LOS pulse amplitude. If a non-LOS channel was desired, these values could easily be adjusted to allow for multipath stronger than the first pulse. Assuming a primarily static channel, the multipath were then inserted into the signal periodically using a replica of the received pulse saved in a file from ADS. If no multipath were desired in the simulation, this function was skipped completely.

One of the primary objectives of this simulation was to determine the performance of the system and compare it with theoretical performance. To evaluate the system, a BER versus E_b/N_o plot must be generated. A function entitled energy_calc was written to calculate the energy per pulse, since each pulse represented one bit. The formula typically used in an energy calculation is [14]:

$$E_b = \sum_{i=1}^{N} w^2(t) \quad dt \tag{5.5}$$

where:

N	is the number of samples per pulse
w	is the pulse (volts)
dt	is the time step (seconds)

Since the time step, dt, was a constant in all cases and canceled later in the simulation, it was left out of the computation. The pulse, w(t), is a replicated pulse imported from a stored file initially generated in ADS. If multipath were present, N in Equation (5.5) became the number of samples per period. This was evaluated in a different function for simplicity, called the energy_calc_mp function. Once the correct energy was found, the standard deviation of the noise was calculated using the desired E_b/N_o. After solving for N_o, the power spectral density (PSD) of the noise using a matched filter at the receiver is [14]:

$$\sigma^2 = \frac{N_o}{2} \tag{5.6}$$

The standard deviation, σ, was then computed by taking the square root of the PSD, or variance of the noise. To generate an additive white Gaussian noise (AWGN) array, the standard deviation was multiplied by the randn function in Matlab, which has a mean of zero and a standard deviation of one. Once this process was completed, the noise array was added to the signal, allowing for a basic wireless channel model with multipath and AWGN.

5.2.4 Receiver

The system simulation for the UWB receiver will be discussed in the following sections to distinguish the various functions including the air interface, sampling, synchronization, and data demodulation.

5.2.4.1 Air Interface

First, the received waveform should be detailed to give the basic numbers regarding the air interface. The system simulation contains 15 acquisition pulses at 10 MPulses/sec with a 250 ns time delay. These acquisition pulses are created in the system to determine the delay spread of multipath and inform the receiver the next set of pulses is the test frame. They were included in the system simulation as an accurate representation of the air interface, although its functionality was not simulated. Once these were generated, a 1.1 μs time delay occurred and the test frame followed to ensure a reliable link was established. The same frame structure was used here as discussed in Chapter 4, with 48 pilot pulses, 960 data pulses, and 16 pulses worth of guard time. After the test frame had been formed, the simulation continued with 500 ns of delay time and 11 data frames, all with the same structure as the test frame. The number of data frames was chosen to be 11 to allow for 10560 simulated data pulses, permitting BERs on the order of 10^{-4}. A simplified version of the data received is plotted in Figure 5.5 to illustrate the air interface since the full version does not convey any information due to its complexity. A couple of the changes made for the figure below were 10 acquisition pulses, 15 pilot pulses, 4 pulses of guard time, and 45 data pulses. Also, the plot was generated using an E_b/N_o of 50 dB to display pulses and the general frame structure. Figure 5.5 shows a basic example of the waveform at the input of the bank of ADCs.

5.2.4.2 Sampling

Sampling of the incoming waveform is performed in the system by the bank of 8 ADCs, each sampling at 1 GHz, giving an effective sampling rate of 8 GHz using the Parallel Time-Domain Sampling technique. In an ideal system, sampled data would be stored in an array every 125 ps, which would be input to the FPGA in parallel form. In

the system simulation, the sampling was done in serial form, even though the data processing in the physical system will be done in parallel. The parallel technique could be implemented in Matlab with more complexity in the code, but the result would remain unchanged.

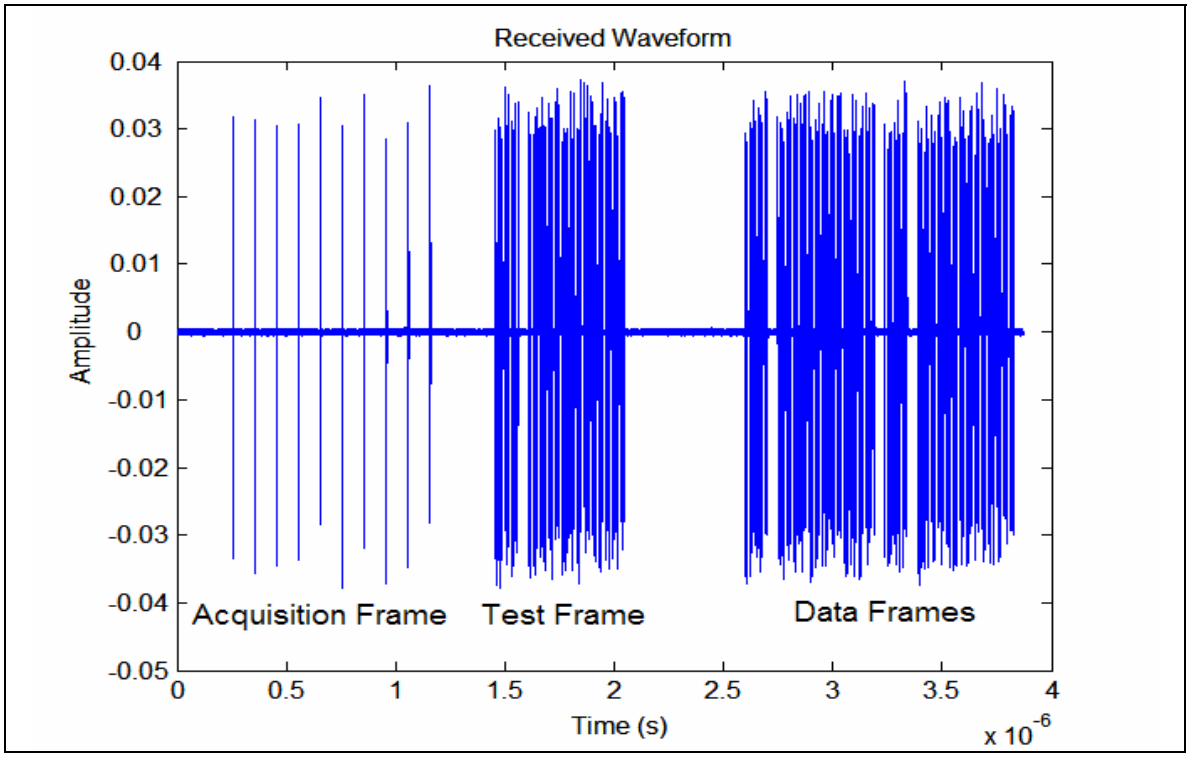


Figure 5.5. Graphical Representation of the Received Waveform at the Input of the ADCs

One of the timing problems associated with the rapid sampling time presented in this design is the aperture delay variation in each of the ADCs. The system simulation must account for a sampling time variation of 50 ps (actually 60 ps maximum but the number needs to be a multiple of the 25 ps time step), which is the worst case scenario for the MAX 104 ADCs used in the design. In the Matlab code, samples were stored in an array every 125 ± 25 ps based on a random number generated in the function entitled aperture_delay. The results showed minor changes in pulse distortion as shown in Figure 5.6 where both perfect sampling and sampling using aperture delay variation are displayed for a single pulse period. It should be noted that when the aperture delay variation was increased, the pulse shape became heavily distorted. Figure 5.6 also

illustrates the cross-correlation of the two signals, where the sampled waveform with aperture delay variation has the same correlation output shape with a 0.5 dB lower peak. This difference is not a significant one and should not cause any negative effects for the system. This simulation confirmed the MAX 104 ADC as an adequate choice, having a sufficiently small aperture delay variation while also having an acceptable sampling rate.

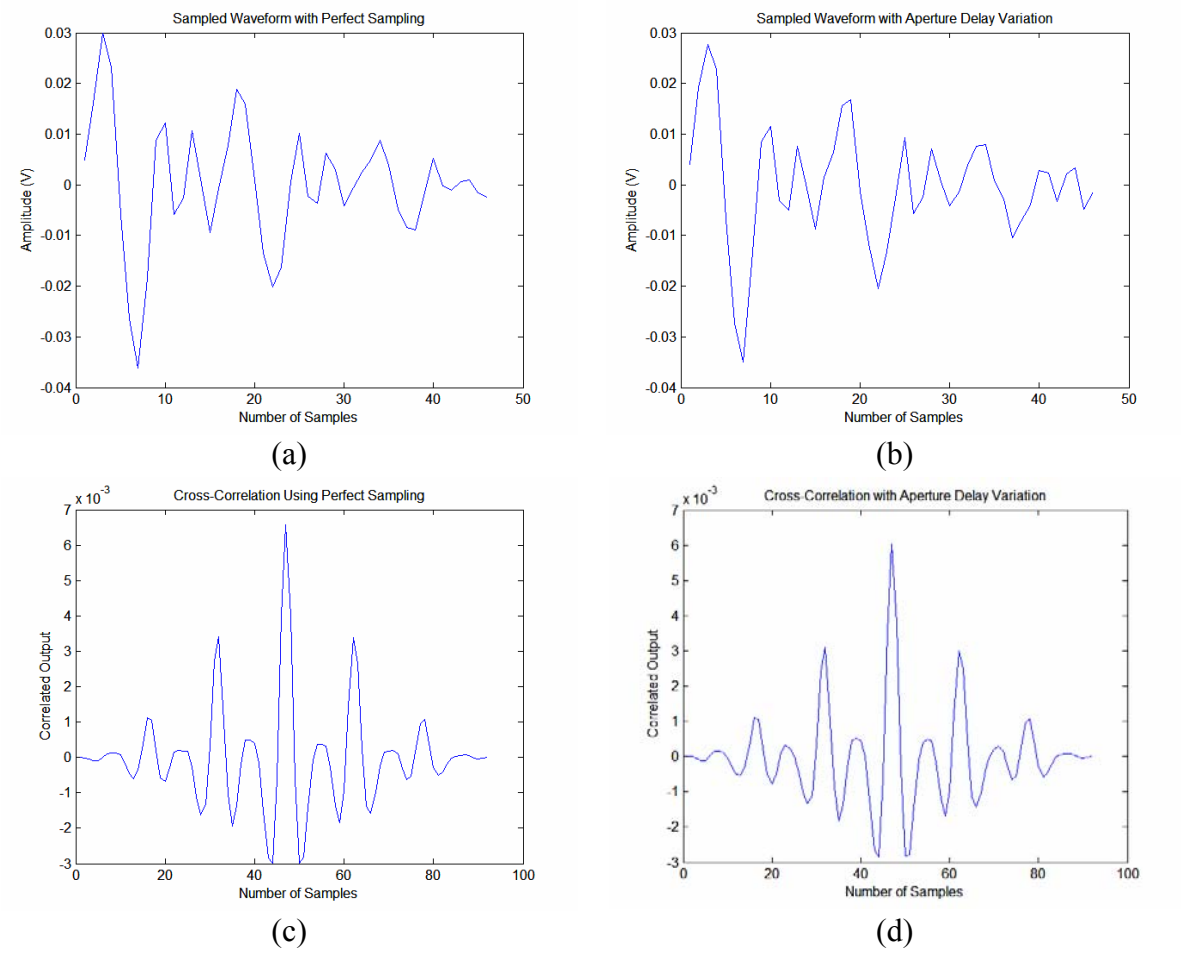


Figure 5.6. Sampled Waveform Comparison (a) Sampled Waveform with Perfect Sampling, (b) Sampled Waveform with Aperture Delay Variation, (c) Cross-Correlation with Perfect Sampling, (d) Cross-Correlation with Aperture Delay Variation

5.2.4.3 Synchronization for Acquisition Pulses

Once the waveform was sampled, it was important to know where the acquisition pulses start in memory. A function entitled acquisition was written in Matlab to implement the single pulse sliding matched filter synchronization technique previously discussed. In the physical system design, the receiver begins to record data after

detecting the initial burst of pulses sent from the transmitter. This implementation leaves noise as the first sampled data, followed by a known number of header pulses (in this case fifteen), one test frame of data, and finally the data frames that need to be demodulated. The acquisition function performed a matched filter operation using a matched pulse of 16 samples, or the number of samples in the width of a pulse. The algorithm began by correlating and integrating with 2000 samples of noise to find a threshold correlation number. To calculate the final value, the maximum value of the correlation was multiplied by a noise constant, which was arbitrarily chosen based on the standard deviation of the noise, varying from 0.0035 to 0, using the function nt_calc. Values for the noise constant ranged from 0.8 to 1.1. These numbers were obtained empirically in the simulation and are not more strictly investigated since the acquisition function does not operate above a noise standard deviation of 0.0035 (or an SNR on the order of 13 dB), where the template sliding matched filter synchronization technique was employed.

After the threshold correlation number was found, the matched filter pulse was then "slid" across the data until it reached the first acquisition pulse, where the absolute value of the correlation exceeded the threshold correlation number and the corresponding index was saved. Since the time step was so small, the first index crossing the threshold correlation number might be one sample in front (or behind) of the perfect alignment, meaning the maximum correlation value was used within the width of the pulse. This also allowed for distinction between sidelobes and multipath, as samples crossing the threshold were compared within the number of samples in a pulse width. The maximum value was taken for each scenario since it should indicate the index of perfect alignment. This operation occurred for each of the acquisition pulses and their corresponding multipath. Once the index of the last header pulse was found, the algorithm continued until it found the remaining multipath, which was based on the statistical mode of the number of multipath previously found for each pulse. The algorithm also quit when a counter, which started at the first LOS pulse index, exceeded the length of the acquisition frame.

The conclusion of the acquisition function also included code to determine the indices of the positive polarity LOS pulses and the number of multipath following each

one. This data was used by the pilot-based matched filter estimation routine to calculate a template waveform for data demodulation. As discussed in Chapter 4, this synchronization technique is not useful for high noise and non-LOS scenarios, but allows for an accurate pilot-based matched filter template in LOS applications. Using this technique, additional samples without multipath energy are not included in the template. This results in a more accurate representation of the incoming pulse symbol waveform, where less bit errors typically occur without processing the extraneous noise samples if the entire pulse period is used.

After the acquisition function has concluded, a variable called data_search was set to "0" if all of the acquisition pulses were found and "1" if any of them were missing. Using the data_index_calc function, the template sliding matched filter synchronization technique was implemented if the acquisition routine did not detect every acquisition pulse. The routine began by generating a template of pulses using the same polarity and pulse rate at which they are "transmitted", which would be known at the receiver (i.e. there is always knowledge of the pilot sequence). This template then "slid" from the beginning of the data until it crossed a threshold value, determined for acquisition pulses to be 0.04 and 0.045 for a noise standard deviation below and above 0.028, respectively. As will be seen in the following section, probability of detection and false alarm curves were created to determine these values. Due to the small time step, fifty samples were correlated after the threshold was crossed and the index of the maximum correlation was used as the maximal correlation point (start of the acquisition pulses) and output back to the main file. Also, the indices of each of the positive polarity acquisition pulses were calculated periodically from the maximal correlation point and transferred to the pilot-based matched filter estimation routine.

One significant reason to include acquisition pulses is the change in pulse polarity when traveling through a non-LOS channel. At the conclusion of the data_index_calc function, the correlation value at the maximal correlation point was determined to be either positive or negative. A negative result indicates a change in polarity, whereas a positive result indicates the opposite. This decision of pulse polarity was output for the data decisions later in the simulation. Obviously, this function was added for non-LOS only because no change of polarity should occur for the LOS pulse. For this reason, it

does not have an effect on the system simulation because the data does not reflect a change in pulse polarity, although it was incorporated to provide realistic simulation options in the future if the data were manipulated.

5.2.4.4 Pilot-Based Matched Filter Estimation

Once synchronization occurs, the indices of the positive polarity acquisition pulses and the corresponding multipath (if any) were imported to the ce_template function, which produces a pilot-based matched filter template for data demodulation. Only the positive polarity pulses were used to form the template for simplicity, although all of them can be utilized, as explained in Chapter 4. The number of multipath for each LOS pulse was determined, which was the deciding factor on the length of the estimation array. The length was determined by starting at the initial pulse and adding 20 samples to the last multipath index, meaning a few indices past the last valid pulse are included in the template to account for any error due to aperture delay variation. If the data_index_calc function was necessary for synchronization (meaning pilot pulses were missing from the acquisition function), then the pilot-based matched filter template was the length of a symbol period, or in this case 80 samples. This approach was taken to include any multipath energy in the symbol period, although bit decisions would be made with unnecessary random noise if no energy was present. Once the length of the array was computed, a two-dimensional array was formed with each initial index followed by the number of samples calculated for the template length. These arrays were then averaged to find the final template used to demodulate data using the Digital Pilot-Based Matched Filter technique. Averaging the waveforms reduces the amount of noise in the template. An example of a pilot-based matched filter template with two multipath is shown in Figure 5.7.

5.2.4.5 Synchronization for Pilot Pulses

Continuing with the simulation, a test frame was processed to ensure the proper operation of the system. The algorithm began by using the acquisition function discussed earlier to provide indices of the pilot pulses and multipath detected. The maximum noise correlation number was updated using the noise samples prior to the test frame to give a

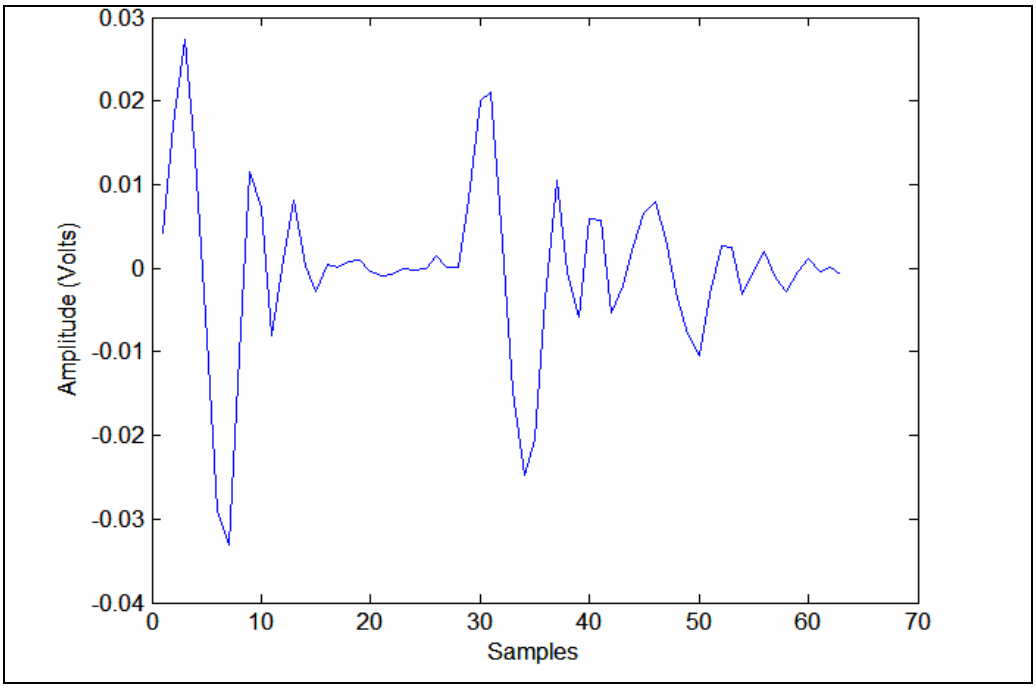


Figure 5.7. Pilot-Based Matched Filter Template Waveform

more accurate correlation threshold value. Using the acquisition function, the start of the data index was calculated using:

$$D_{(start\quad data)} = D_{(last\quad pilot\quad pulse)} + N_g + N_p \tag{5.7}$$

where:

$D_{(start\ data)}$	is the index where the data begins
$D_{(last\ pilot\ pulse)}$	is the index where the last pilot pulse begins
N_g	is the number of samples in the guard time
N_p	is the number of samples per pulse repetition period

If synchronization was accomplished using the data_index_calc function, the threshold value to find the start of the pilot pulses was 0.16 and 0.17 for a noise standard deviation below and above 0.028, respectively. These values were found based on synchronization curves seen later in this chapter. They differ from the acquisition threshold values due to the number of pulses being correlated in each case. In this scenario, the start of the data index was computed using:

$$D_{(start\quad data)} = D_{(start\quad pilot\quad pulse)} + N_g + N_{pp} \tag{5.8}$$

where:

$D_{(\text{start pilot pulse})}$ is the index where the first pilot pulse begins
N_{pp} is the number of samples in the pilot pulses

5.2.4.6 Data Demodulation

With frame synchronization achieved, the test_frame function was utilized with the start of data index. Within the test_frame function, either a matched_filter or a matched_filter_ppm function analyzed the data, although a threshold_detect function was included.

The threshold_detect function, which implements the digital leading edge detection topology, set a threshold voltage based on the incoming signal. Specifically, three-quarters of the maximum signal amplitude was used for the threshold voltage, although this value is flexible and will be adjusted accordingly when simulations are performed with Gaussian impulse data. A "1" or a "0" was output into an array as the received signal exceeds the threshold voltage in either a positive or negative fashion, respectively. If multiple pulses were detected within one time period, an error was given that states the noise level is too high to use this technique, which is the reason it should be utilized only in short range, low noise applications.

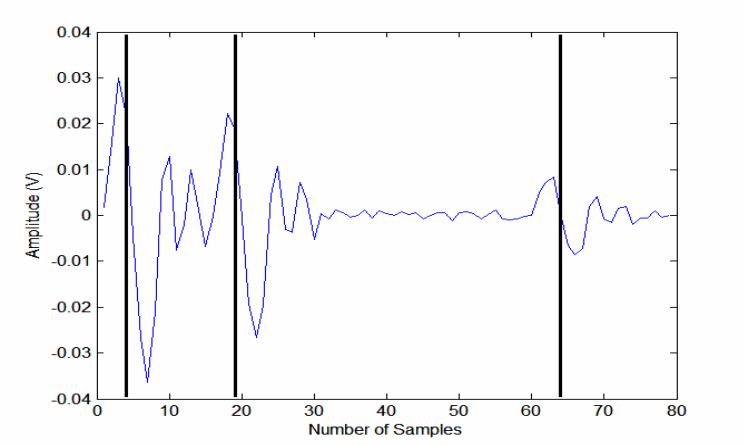
It should be noted threshold_detect is a completed function in the system simulation although it was not implemented for any of the simulation results. This technique can only be utilized with an antenna that does not differentiate the received pulse into a Gaussian doublet, such as a biconical antenna. In this system simulation, ADS uses a differentiator to represent a Vivaldi antenna, where there are no distinct positive and negative pulses, making a threshold detector useless.

Therefore, the digital matched filter approach was utilized when demodulating the data. Specifically, the matched_filter function was written to demodulate biphase modulation data. In this function, the pilot-based matched filter template performed an early-late digital matched filter operation over three sample points within an 80 sample region determined by the start of the data index. This was accomplished by generating two matched filter templates shifted in time around the center time of the original template, as shown in Figure 5.8 below. The lines indicate the timing of the positive peak amplitude of the LOS pulse and each multipath pulse of the original template in Figure 5.7b. These three templates were then correlated within a sample region where a

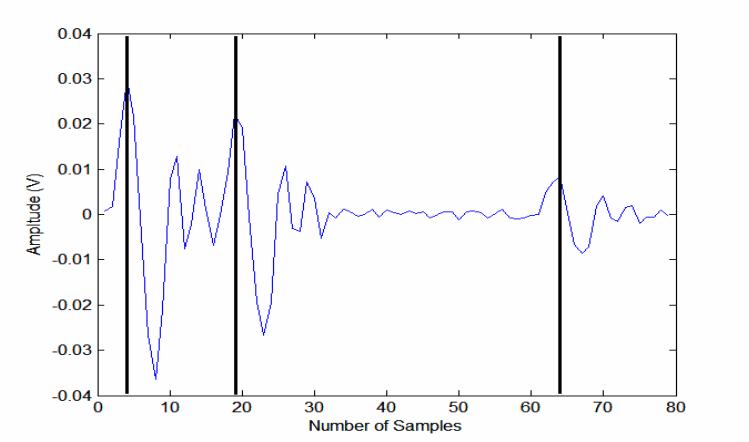
data pulse was expected. The objective of this algorithm was to find the position of maximum correlation as the index of the highest correlating template was saved, compensating for errors due to aperture delay variation. This technique is only sub-optimal, as the majority of the samples must move in the same direction, which is not always the case. The result from the maximum correlation point was then output to the test_frame function, where a data decision on the pulse was made using a threshold of zero to determine the data bit outcome.

Using primarily the same technique, the matched_filter_ppm function (for binary PPM demodulaton) used the early-late digital matched filter operation to generate three matched filter templates. However, each template was compared at two different indices since binary PPM was being used. The function determined a bit decision from the highest correlated value at each index. A "1" was output if the correlated value within the periodic pulse train was higher, while a "0" was output for a correlated value offset from the periodic pulse train was higher.

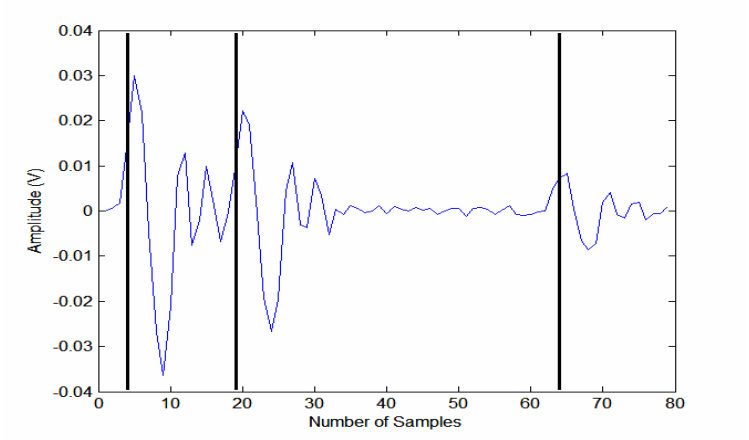
After an array of data bits were calculated and sent back to the test_frame function, the pulse polarity bit decided whether or not to invert the data. For this specific simulation, this option was never valid in any LOS channels. Then, the array of data was compared to the data expected (known at the receiver), where the valid_frame variable was set to "1" for correct data and "0" if the data was incorrect. When the test_frame function concluded, a message was displayed in the Matlab window if the data received was invalid, allowing for an easy debugging technique when perfect data demodulation was expected. When simulating high noise channels, the simulation was run despite an invalid test frame because bit errors were anticipated.



(a)



(b)



(c)

Figure 5.8. Pilot-Based Matched Filter Template Using Early-Late Algorithm. (a) Template Advanced by 1 Sample in Time, (b) Original Template, (c) Template Delayed by 1 Sample in Time

5.2.4.7 Tracking

The index of the maximum correlation point was used to adjust the timing offset of the template and the current data index. In the physical UWB system, if the correlation occurs with the original pilot-based matched filter template, the sampling time of the ADCs is correct and no timing adjustment is necessary. However, due to clock drift and aperture delay variation between ADCs, this will not always be the case. To perform a short term fix, the data index was adjusted in the system simulation for the next frame based on the maximum correlation point. If the pulse contained sampling error advanced in time due to aperture delay variation, the matched filter template advanced in time by one sample maximally correlated with the incoming signal. Therefore, the start of the data index for the following frame was advanced in time from its typical value by subtracting one sample point to compensate for the timing offset. The opposite was true for a pulse delayed in time. If the maximum correlation point is consistently advanced or delayed in time, a long term solution is necessary to control the ADC clocks, although this option was not simulated. Using the software timing adjustment technique, the receiver can maintain maximum correlation when utilizing digital matched filtering.

5.2.4.8 Processing of Data Frames

At the conclusion of the test_frame routine, the pilot-based matched filter template was updated by averaging the positive polarity pilot pulses in the test frame using the ce_template function. The timing of this operation occurred after data processing as a realistic model for the system. As the FPGA processes the data in the test frame, the pilot-based matched filter template will be created in parallel. Therefore, the updated version of the template will not be ready until the next data frame.

Once the acquisition, validation, and the matched filter template were formed, the data frames were processed in the same manner as the test frame without the verification of data. The acquisition function was used to find the pilot pulses and multipath indices if possible. Again, if synchronization was not achieved, the data_index_calc function was employed to find the start of the data index. Then, a process_data function implemented the digital matched filter topology previously discussed. The data was

stored in a two-dimensional array with the rows representing the frame number and the columns containing the data bits. Finally, the pilot-based matched filter template was updated based on the pilot pulses in the data frames. This process was repeated for the number of data frames specified in the simulation.

5.2.4.9 BER Calculation

With the intention to determine receiver performance, a BER calculation was the last function implemented. Since the data "transmitted" in the simulation was known, an array was created for comparison purposes in the function entitled ber_calc. For each data frame, an exclusive-or (XOR) Matlab function was used to determine when the calculated data bits differed from the known data sequence using the formula:

$$n_{be} = \sum_{i=1}^{N_s} (b_i \oplus k_i) \tag{5.9}$$

where:

n_{be}	is the number of bit errors
N_s	is the number of bits simulated
B_i	is the calculated bit decision
K_i	is the known bit decision

Using this result, the BER was calculated using:

$$BER = \frac{n_{be}}{N_s} \tag{5.10}$$

5.3 Receiver Performance Results

After the system simulation was completed, the results were used to improve the design and validate the proof-of-concept. Before simulating BER performance, synchronization curves were created to find an appropriate threshold value when

correlating with the pilot pulses. To compare the design with theoretical data, BER curves were generated for various system characteristics.

5.3.1 Synchronization Performance

In an ideal system, synchronization for a matched filter digital receiver is achieved when the data index aligns perfectly with the matched demodulation template. This alignment is demonstrated by the highest correlated peak in Figure 5.9 below, where the autocorrelation of the pilot sequence is illustrated. The peak correlations on either side of the highest peak are due to the replication of an m-sequence within the pilot pulses. As explained earlier, this is not the optimal way of modulating the pilot pulses because of the additional correlation spikes, causing unnecessary false alarms. However, with very little time at the end of the semester, this method was the quickest. A true m-sequence would only contain one peak, which is the most advantageous implementation.

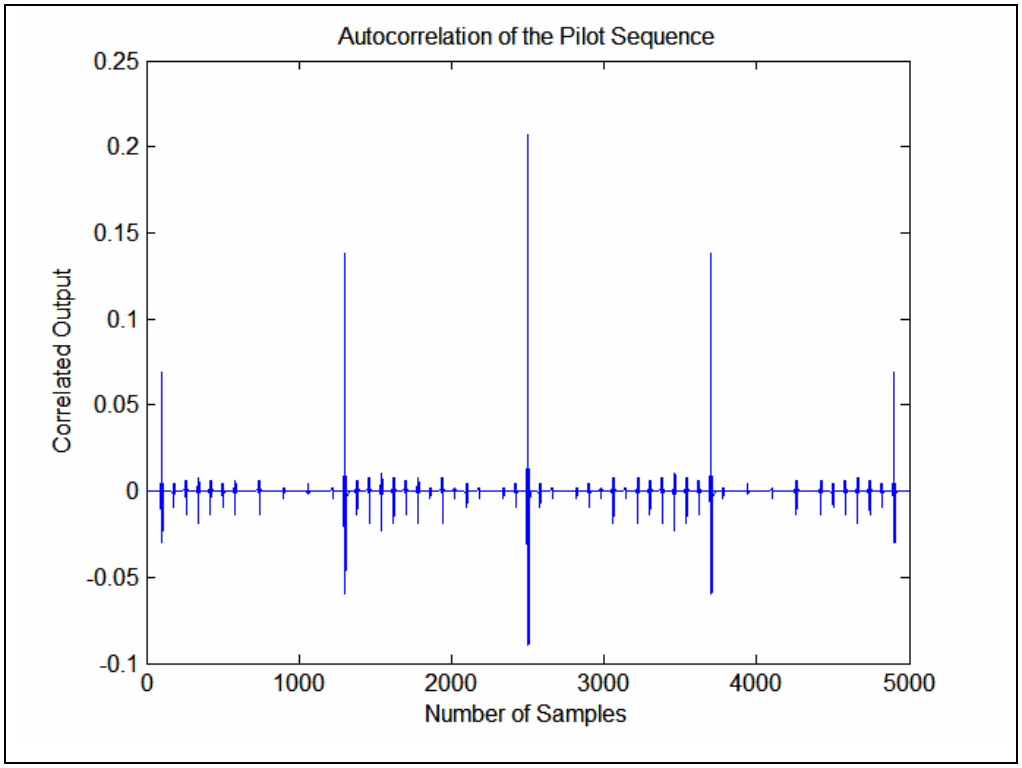


Figure 5.9. Autocorrelation of the Pilot Sequence

Due to the short sampling time (125 ps) of this UWB receiver design, several data indices can correlate relatively high because of the high sampling rate. The synchronization curves for this design were created based on the aperture delay variation within the simulation. Since ± 25 ps of aperture delay variation existed, it was conceivable the synchronized data index was located ± 1 sample from the estimated data index. With this in mind, a valid detection consisted of three samples, while a false alarm was defined as a threshold crossing anywhere outside of these samples. The probability of detection was then calculated as:

$$P_{\text{det}} = \frac{N_d}{n_{ed} k_f} \tag{5.11}$$

where:

N_d is the total number of detections
n_{ed} is the number of expected detections per frame
k_f is the number of frames

Similarly, the probability of false alarms was defined as:

$$P_{fa} = \frac{M_{fa}}{(m_{dp} - n_{ed})k_f} \tag{5.12}$$

where:

M_{fa} is the total number of false alarms
m_{dp} is the number of data points simulated per frame

Since the number of acquisition and pilot pulses differed, curves were generated for each to determine an acceptable correlation threshold value. The system simulation was modified to perform synchronization only while calculating the two probabilities above. For the acquisition pulse curves seen in Figure 5.10, the values used for Equations (5.11) and (5.12) were n_{ed}=3, k_f=5, and m_{dp}=2107, meaning the total number of data points simulated was 10535. Simulation numbers n_{ed}=3, k_f=15, and m_{dp}=5814 were used for the pilot pulse curves illustrated in Figure 5.11, resulting in 87210 simulated

sample points. Data was generated at E_b/N_o values of 1, 3, 5, and 7 dB to accurately determine correlation threshold values based on the noise in the channel.

Synchronization curves for the acquisition pulses illustrate a typical result, with a low E_b/N_o producing more false alarms while the opposite occurs for a higher E_b/N_o. Since there is a gap for the probability of detection at low probability of false alarms between the 3 and 5 E_b/N_o curves, two thresholds were established. For an E_b/N_o 5 dB or greater, 0.04 was chosen as the correlation threshold with a probability of detection of 0.8 and a probability of false alarm of 10^{-4}. A second threshold for an E_b/N_o less than 5 dB was created at a higher threshold of 0.045 to mitigate false alarms. Even for the worst case scenario for these threshold values, an E_b/N_o of 1 dB has a probability of detection of 0.67 while maintaining a $3 \cdot 10^{-4}$ probability of false alarm using this correlation threshold. While it appears the probability of detection is uncharacteristically low for each threshold value, one should remember the probability of detection is calculated based on three sample points, all of which are valid frame synchronization indices due to the use of an early-late algorithm in data demodulation. Therefore, since there are three possible detections per frame, only one of those sample points need to cross the threshold to achieve frame synchronization, meaning a probability of detection of 0.33 or higher indicates frame synchronization.

As shown in Figure 5.11, the synchronization curves for the pilot pulses do not follow the same shape as those for the acquisition pulses. Since aperture delay variation was used in the synchronization results, there often are times when two of the three samples points used in the probability of detection calculation are above the correlation threshold. However, this result is entirely random, meaning there will not be any specific time when this event occurs. Therefore, the probability of detection between 0.33 and 1 is an unpredictable value. If attention is focused on the areas around the 0.33 and 1 probability of detection values, one will notice the same shape taking place as in the acquisition pulse curve due to the stability of those two values. They are predictable from the fact that when the threshold is low enough, despite the aperture delay variation, all three samples will be above the threshold. When the threshold is high, typically the peak sample point will be above the threshold, as was the case during these simulations. In the acquisition pulse curves, aperture delay variation was also included, although the

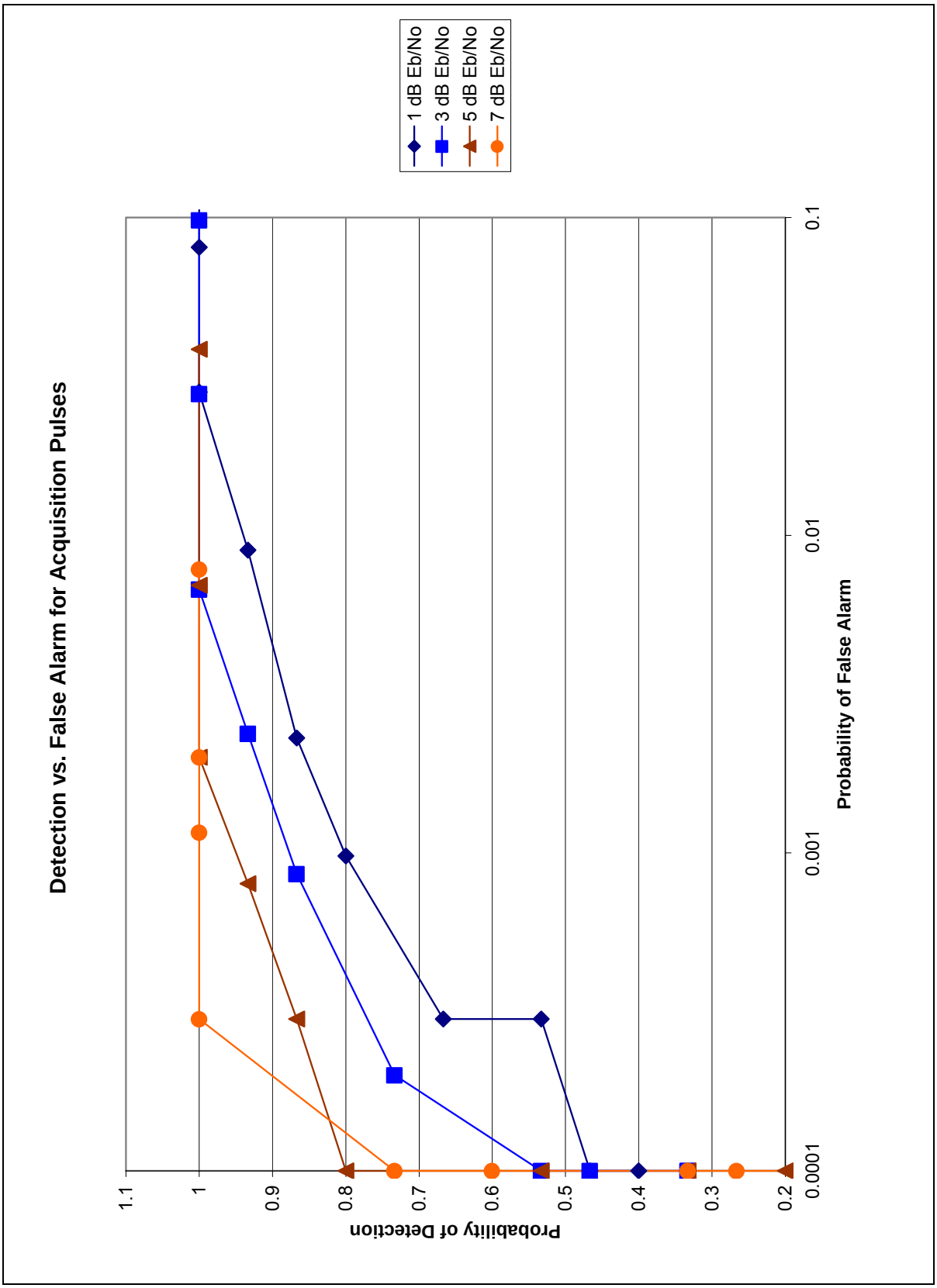


Figure 5.10. Probability of Detection vs. Probability of False Alarm for Acquisition Pulses

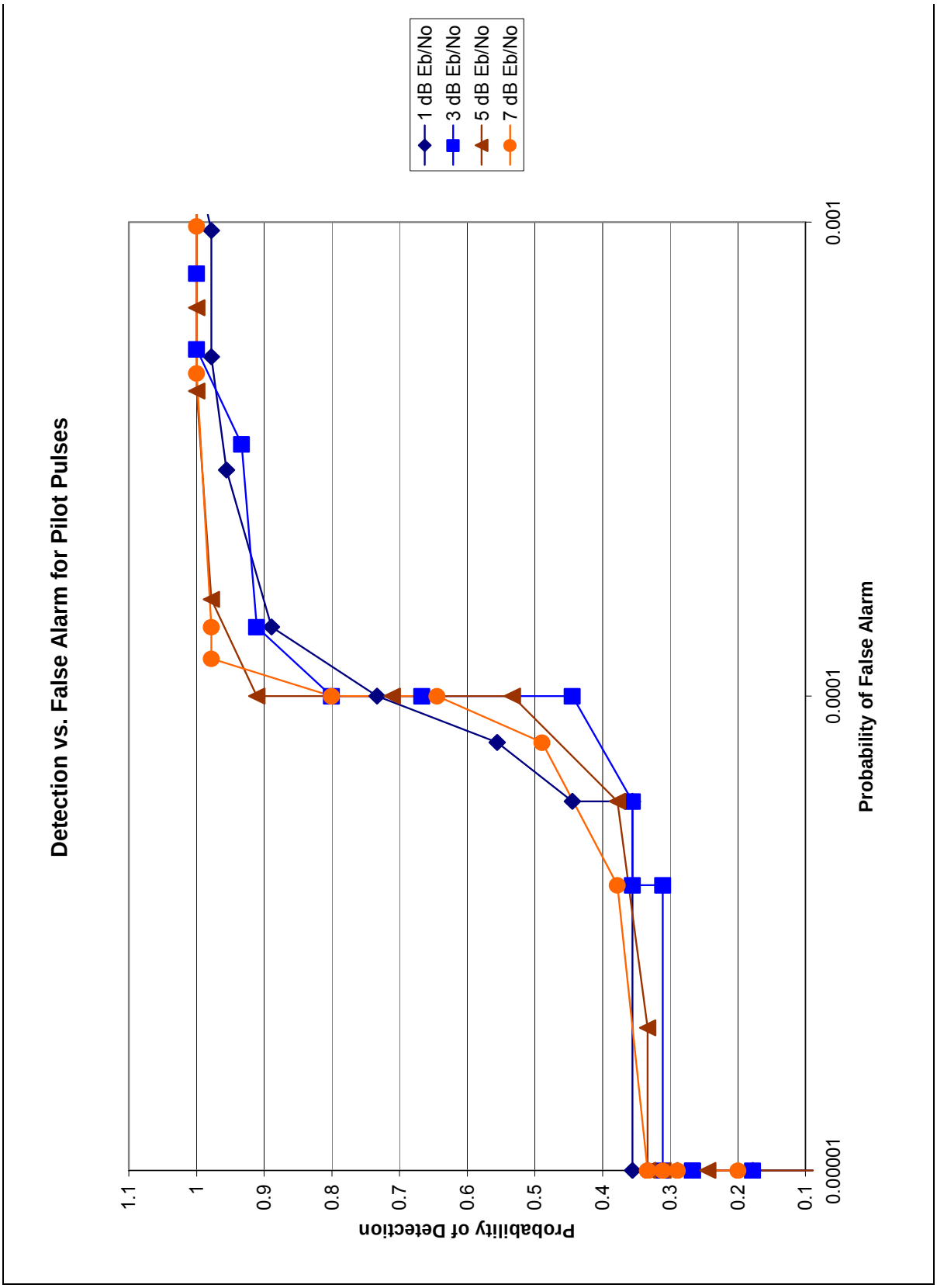


Figure 5.11. Probability of Detection vs. Probability of False Alarm for Pilot Pulses

effect was small because of the limited number of pulses (15) per frame. With less pulses, the correlation threshold values were focused in a compact range (0.015—0.06) where a successful correlation threshold would be found. The increment between each correlation threshold value was less, causing the aperture delay variation to have less affect. This effect is more exaggerated for the pilot pulses (48) because the range of correlation threshold values (0.03—0.22) were spread, giving the synchronization plot for pilot pulses less resolution. The curves for the pilot pulses could also be distorted due to the difference in pulse rate. The acquisition pulses were run at a pulse rate of 10 MPulses/sec, whereas the pilot pulses were simulated at 100 MPulses/sec. Therefore, for the number of sample points run, the pilot pulses were more often aligned. This effect could have skewed the probability of false alarm data and caused the curves for the pilot pulses to move closer together.

Despite this effect, the values obtained from the synchronization simulations using pilot pulses provided accurate values. Again, two correlation thresholds were established between the 3 and 5 E_b/N_o curves, as the probability of false alarm was different at these threshold values. For an E_b/N_o 5 dB or greater, 0.16 was chosen as the correlation threshold with a probability of detection of 0.37774 and a probability of false alarm $2 \cdot 10^{-4}$. A second threshold for an E_b/N_o less than 5 dB was created at a higher threshold of 0.17 to reduce the number of false alarms. Even for the worst case scenario for these simulations, an E_b/N_o of 1 dB has a probability of detection of 0.35552 while maintaining a $2 \cdot 10^{-4}$ probability of false alarm using this correlation threshold, both sufficient for the simulation.

The final correlation thresholds were input to the simulation and utilized in the BER curves presented below. They proved to be effective, as each simulation run achieved synchronization for every frame using the probability of detection values listed above. Even though these values must be updated for every frame structure involving a different number of acquisition or pilot pulses, this synchronization procedure provided excellent results.

5.3.2 BER Curves

Once the correlation threshold values were in place, BER curves were run to determine the performance of the UWB receiver. As discussed previously, a pilot-based receiver was used by averaging the pilot pulse symbols to find a template waveform. Then, the data was demodulated using the pilot-based matched filter template with an early-late algorithm.

The results for biphase modulation are shown in Figure 5.12 along with the perfectly matched BER, previously shown in mathematical form in Equation (2.10). The performance of the UWB receiver designed in this thesis is slightly worse than the theoretical curve, as expected. Due to the noise in the template after averaging, the performance will not be equivalent to perfectly matched biphase modulation, but is sufficiently close.

Figure 5.13 displays the BER results for binary PPM with its theoretical curve, described in Equation (2.7). These results are similar to the biphase modulation performance, as they are slightly worse than a perfectly matched receiver due to the noisy nature of the pilot-based matched filter template used in data demodulation.

One of the most important aspects of the UWB receiver design presented in this thesis is its ability to optimize a particular system characteristic. It is shown in [13] and in Figure 5.14 below that increasing the number of averaged pilot pulses decreases the amount of noise in the pilot-based matched filter template, causing the BER of the system to converge to the perfectly matched receiver performance. Therefore, the frame structure of the system can re-arranged to enhance this effect, although increasing the number of pilot pulses per frame leads to a decrease in data rate. If a higher data rate is desired, the number of pilot pulses can be reduced with a sacrifice in performance. This type of flexibility will be useful in various types of communication environments, specifically when varying transmitter-receiver distance or experiencing fluctuations in noise levels.

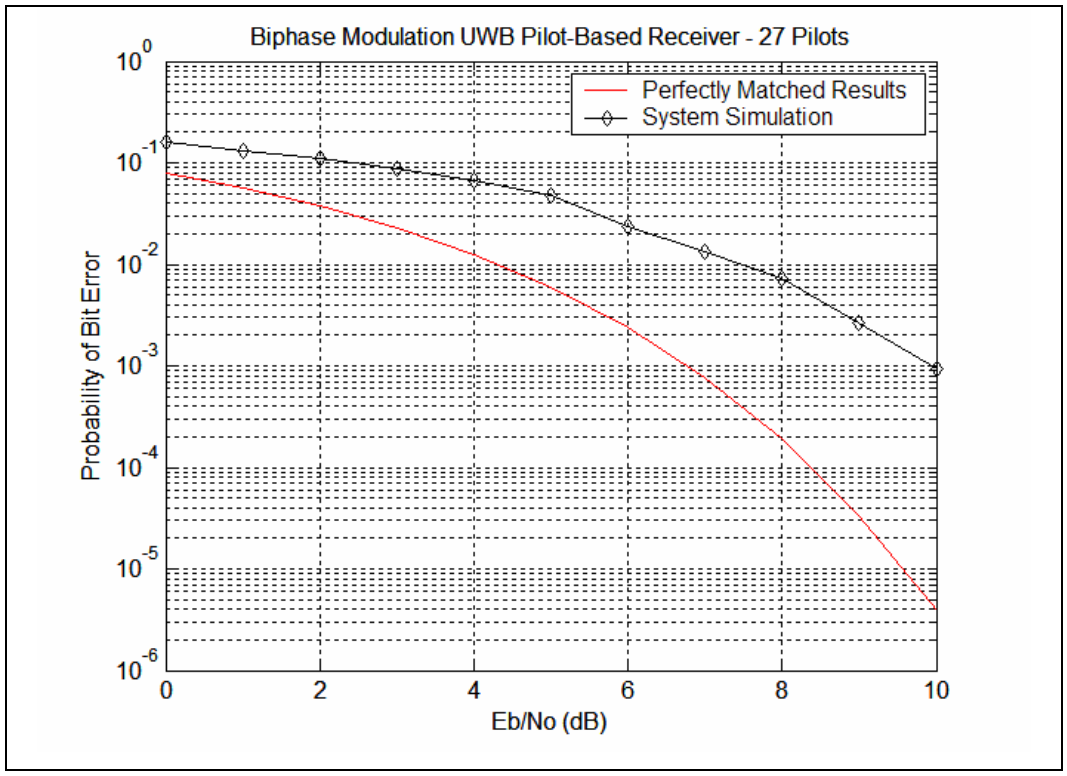


Figure 5.12. BER Curves for Biphase Modulation for a Single Path Channel

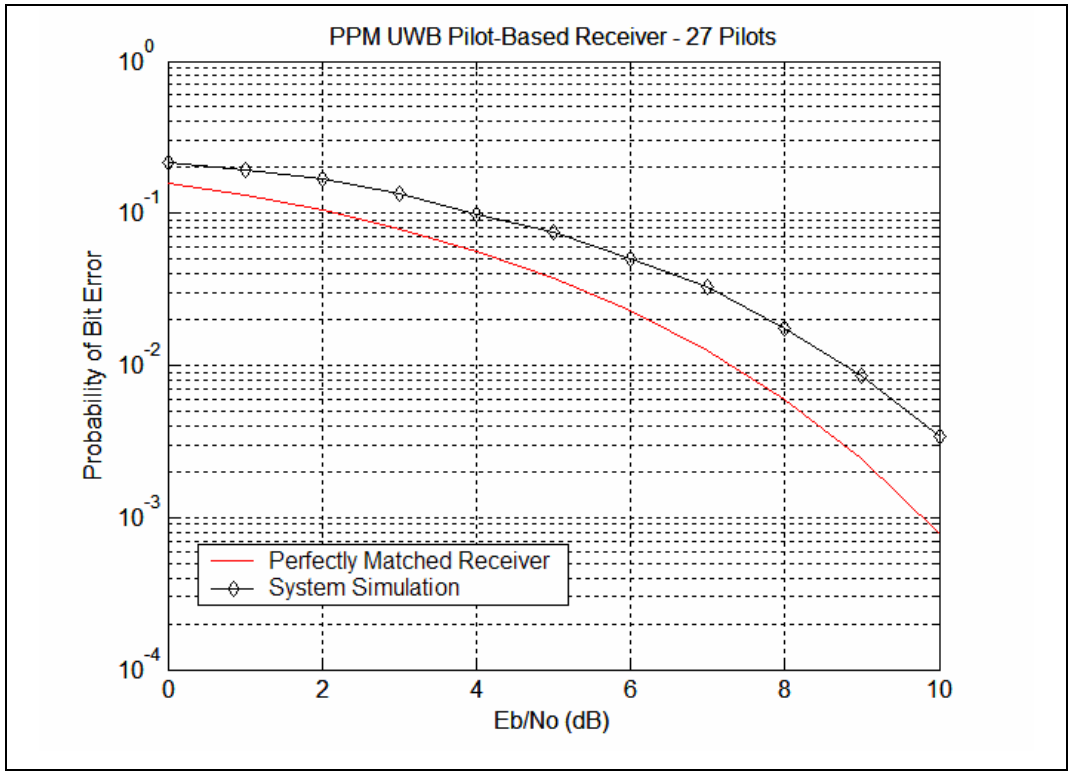


Figure 5.13. BER Curves for Binary PPM for a Single Path Channel

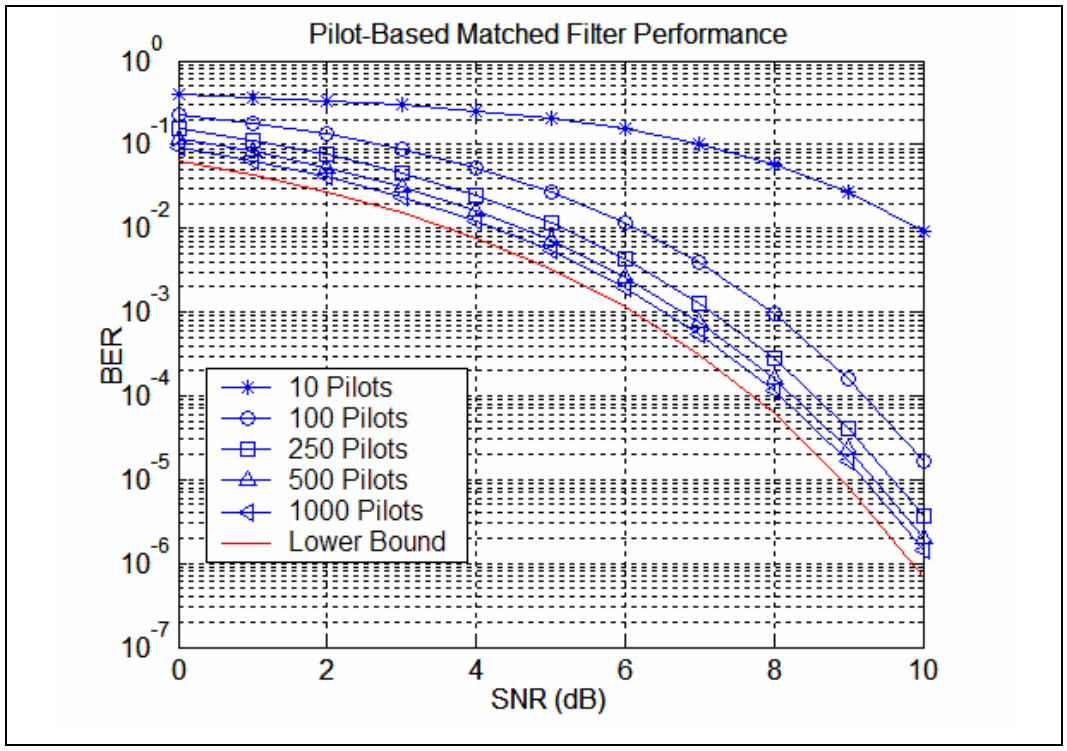


Figure 5.14. Performance Comparison for the Number of Pilot Pulses [13]

To cover more densely populated areas, the receiver must have the capability to include multipath energy in its demodulation routine, which is the reason for the pilot-based matched filter implementation. BER curves were also generated for a three path LOS channel to characterize the UWB receiver performance in such an environment. Since a different amount of energy and thus, noise level, was used in this simulation, the synchronization curve results shown earlier were not valid. With this in mind, these results were created with perfect synchronization without the time to re-generate correlation threshold values. It is also important to note that no intersymbol interference occurred in the multipath simulation, as previously discussed.

The results are shown in Figures 5.15 and 5.16 for biphase modulation and binary PPM, respectively. Compared with the single path perfect synchronization case, the curves for biphase modulation in a multipath channel illustrate slightly worse BER performance due to the decrease in SNR of the template as the number of multipath increases. This is caused by the addition of noise in the template due to more energy per bit, leading to a higher BER for multipath channels, although the degradation is minor. The results in Figure 5.15 also show the system does not drastically degrade for biphase

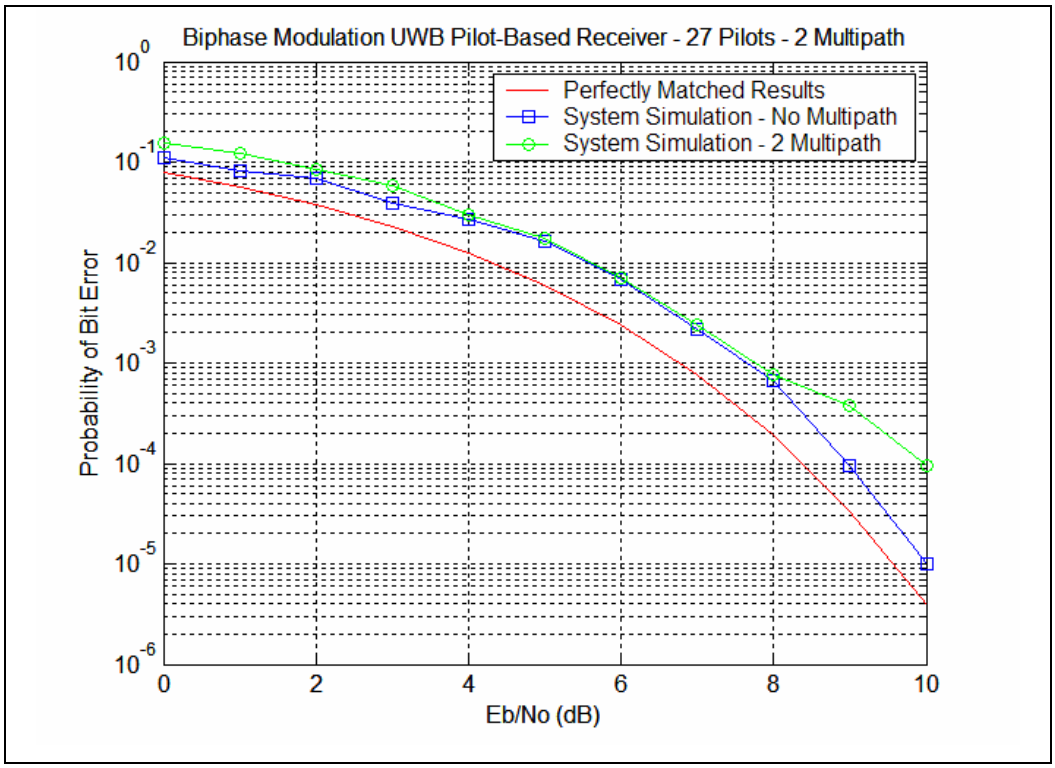


Figure 5.15. BER Curves for Biphase Modulation with Two Multipath

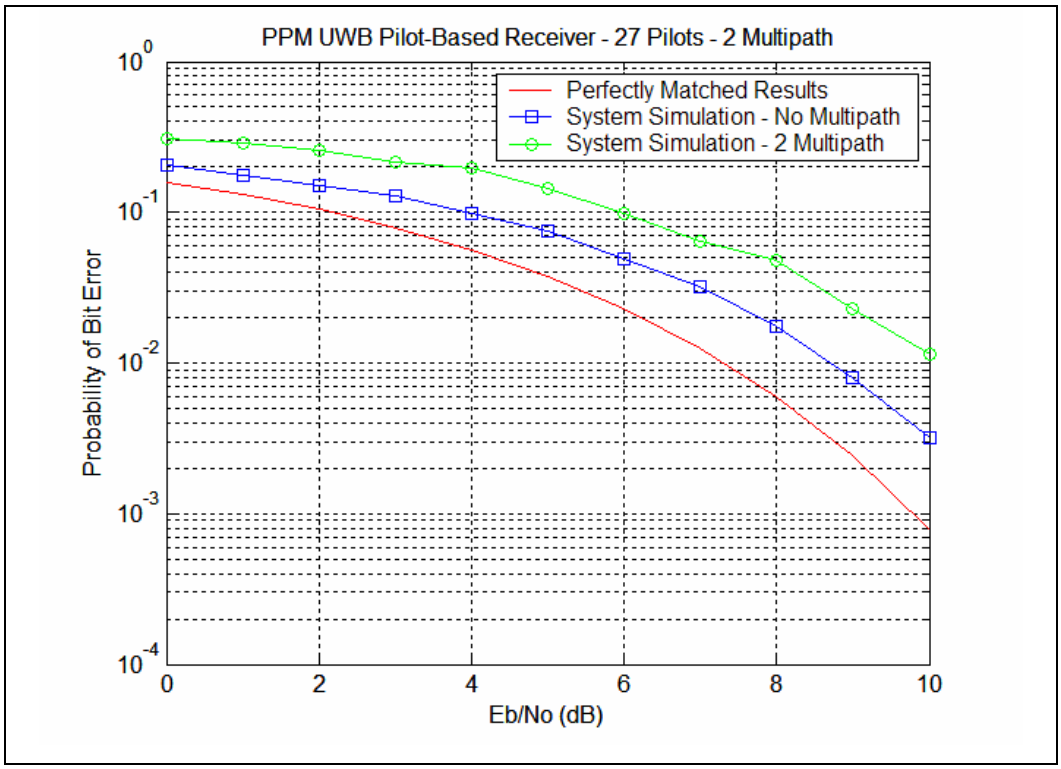


Figure 5.16. BER Curves for Binary PPM with Two Multipath

modulation in a multipath environment from perfectly matched theoretical values, as would be the outcome without including multipath energy in the pilot-based matched filter template. In Figure 5.16, binary PPM also performed less effectively in a multipath channel, although the degradation in performance is more severe. PPM is significantly more sensitive to channel dispersion since orthogonality is lost. The loss in orthogonality causes the probability of detecting a "1" more likely than a "0", leading to a higher BER.

A comparison for a template sliding matched filter synchronization technique using a single path LOS channel was generated for biphase modulation, as shown in Figure 5.17 below. The results demonstrate a decline in BER performance when using the synchronization routine due to an offset in samples from the ideal timing. Although tracking was performed using the early-late algorithm, it did not prevent additional bit errors in the simulation.

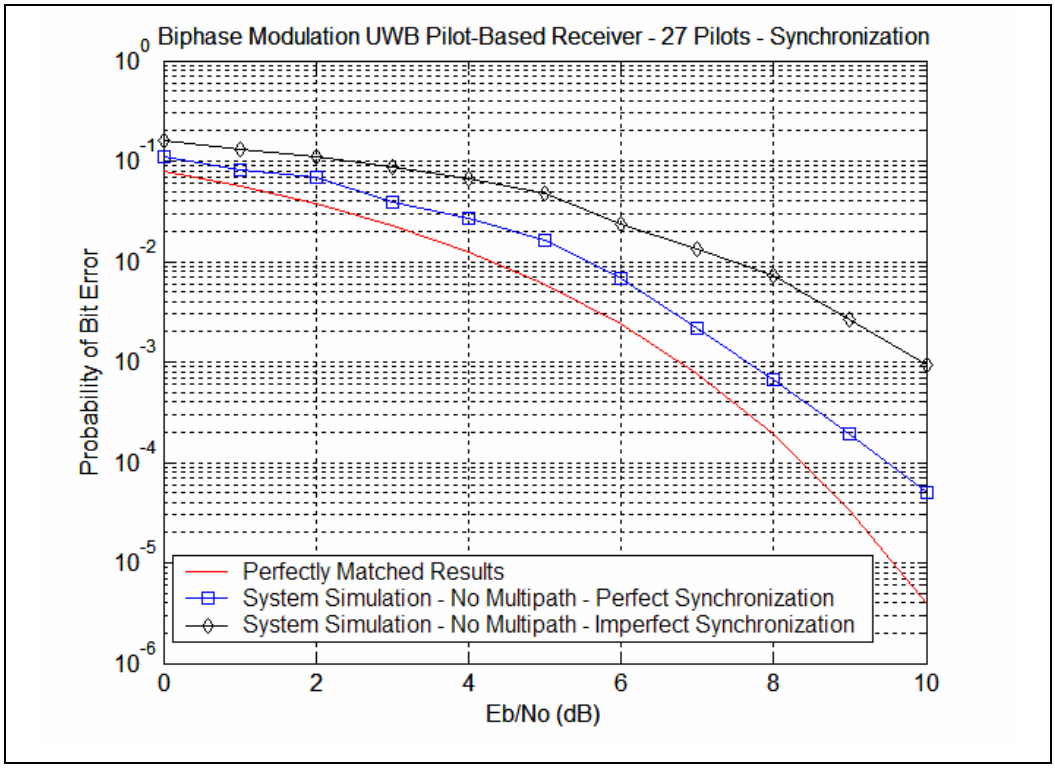


Figure 5.17. BER Curves for Biphase Modulation Using Perfect and Imperfect Synchronization

5.4 Conclusion

The results from the system simulation were very encouraging for the UWB receiver design presented in this thesis. The proof-of-concept was validated as the BER curves are slightly worse than theoretical values for a perfectly matched receiver due to the imperfections in the template caused by noise and aperture delay variation. It was also shown by increasing the number of averaged pilot pulses in the pilot-based matched filter template, better performance can be obtained, although the data rate will suffer. Performance for multipath was also examined (albeit for perfect synchronization) and was close to the theoretical values. Finally, use of the template sliding matched filter synchronization routine led to worse BER performance when compared with perfect synchronization results.

Although these simulations were specific in terms of data bits and number of multipath, other simulations were successfully run on a smaller-scale varying these two parameters. The results of the system simulation give a solid foundation for the design as a whole, but also will assist in the future with issues such as the implementation of receiver algorithms within the FPGA and determining timing limitations when the receiver is being constructed.

Chapter 6 Conclusion

6.1 Final Design Analysis

An impulse-based software radio UWB transceiver design was presented to accomplish goals such as a raw data rate of 100 Mbits/sec, flexibility in terms of modulation schemes and receiver topologies, and a method which can incorporate multipath energy in dense environments. Another benefit of this implementation is the capability to upgrade performance of system characteristics with a software change instead of building a new hardware configuration, making the system ideal for a UWB testbed. Each of these advantages was demonstrated in this thesis, along with system verification through either hardware testing or simulation.

In the case of the transmitter, the design introduced in Chapter 3 was built around an SRD pulse generator, where an input square wave triggered an SRD and formed Gaussian pulse using a short circuit stub. A pulse-shaping network then reduced the ringing using series and shunt Schottky diodes. Other components in the transmitter consisted of RF devices for bandlimiting and amplifying the pulse, along with multiplexers and switches to perform pulse modulation. After the transmitter design was completed, a schematic and board layout were created, as shown in Appendix A. After board fabrication and construction was finished, testing of the DC power supply validated the correct voltages present on the board, although a cooling fan was necessary to prevent overheating. Finally, after probing the circuit board, the result on the SRD output was a 500 ps wide Gaussian pulse with a 500 mV amplitude. Even though the amplitude was not sufficient, re-biasing the input amplifier should allow the pulse to pass through the pulse-shaping network with more current supplied to the SRD. If this adjustment is made, a successful revision can be achieved in the future.

The UWB receiver concept discussed in Chapter 4 concentrated on the Parallel Time-Domain Sampling technique, where a bank of ADCs was used to sample a delayed version of the input waveform. Another important implementation concept was the use of COTS components, where a custom designed IC was not necessary. The software radio UWB receiver design contained two critical hardware devices; the bank of ADCs and the FPGA. Each of these was detailed in terms of their sampling and data processing capabilities, respectively. Digital receiver topologies such as Digital Leading Edge Detection (D-LED) and Digital Pilot-Based Matched Filter (DPBMF), along with the general frame structure, were detailed. The data processing algorithm design was incorporated describing the acquisition, synchronization, and data demodulation techniques.

The system performance and proof-of-concept for the receiver was demonstrated through simulation in Chapter 5, where the DPBMF topology was used to calculate BER for biphase modulation and binary PPM. The system simulation for biphase modulation performed worse than a theoretical perfectly matched curve done using pilot-based matched filter estimation and a single path channel. Binary PPM also produced similar results due to the imperfections in the template waveform used for data demodulation. It was also shown that increasing the number of pilot pulses per frame reduces the amount of noise in the template, causing BER performance to improve. Finally, to verify the goal of including multipath energy for data demodulation, a three path channel was simulated with perfect synchronization. Two conclusions were made from the BER plots of the different modulation schemes. A degradation in BER performance was experienced for binary PPM, as orthogonality between pulses is lost in multipath channels. For this reason, it was determined binary PPM is not an optimal modulation scheme in a multipath environment. Also, the template sliding matched filter synchronization algorithm degrades the performance of the receiver versus a perfectly synchronized system, as biphase modulation BER results were worse due to an offset from ideal timing.

As demonstrated in this thesis, the design goals for an impulse-based software radio UWB system were met, as the system provides the flexibility of a testbed with common UWB characteristics such as high data rate and low power spectral density.

Despite an incomplete system implementation, the foundation for a high performance UWB communication device is in place.

6.2 Future Design Modifications and Work

Throughout the design presented in this thesis, suggestions have been made to make improvements to the design, as not all of the work has been completed on the design or implementation. Also, the findings in this thesis will lead to revisions made in the future as more system specifications are defined. As discussed previously, since the software radio UWB system was designed to be flexible, many of the communication system and receiver algorithm designs are not finalized. Future design modifications not proposed in this thesis will be made based on future simulation and implementation results.

One of the obvious problems with the transmitter is the lack of signal strength obtained when triggering the SRD. The design change suggested focuses on re-biasing the ERA-4SM amplifier prior to the SRD to increase its output current. The primary reason for this idea is based on the small amount of effort involved for testing. If a 10 μH inductor and new bias resistor are ordered, there are no changes to the circuit board design and thus, no new boards need to be fabricated. Obviously, this design change has disadvantages such as drawing more current from the power supply, which already has an overheating issue, but would the simplest in terms of implementation. Then, if a solution to the pulse amplitude problem is not resolved using this suggestion, further research will be necessary to determine the proper combination of hardware to supply more current to the SRD.

There is a large amount of future work left on the UWB system, as none of the construction for the receiver has begun. The initial work consists of creating a schematic and PCB layout, which will take more than six months due to the strenuous layout criteria necessary, such as determining trace lengths for the ADC clock and routing up to 500 pins to the FPGA's ball grid array footprint. A mechanical design for the heat sink must also be completed, as the dissipated heat on the digital boards at the receiver is on the

order of 100 Watts per board. One of the last hardware considerations is the implementation of the Rocket I/O transceivers to communicate between the two digital circuit boards. A high speed data bus must be designed with the capability to handle data at 2.5 Gbps. Finally, to perform the acquisition, synchronization, and data demodulation techniques presented, software must be developed to process data within the FPGA. The software must be optimized to reduce the amount of processing time for each algorithm, as it will ultimately control the system's data rate.

References

[1] G. F. Ross, "Transmission and reception system for generating and receiving base-band duration pulse signals without distortion for short base-band pulse communication system," US Patent 3,728,632, April 17, 1973.

[2] Authorization of Ultrawideband Technology, First Report and Order, Federal Communications Commission, February 14, 2002.

[3] C. R. Anderson, "Ultrawideband Communication System Design Issues and Tradeoffs," Ph.D. Qualifier Exam, Virginia Polytechnic Institute and State University, May 12, 2003.

[4] PADS PCB Design Solutions, Version 5.1, Mentor Graphics, Wilsonville, OR.

[5] Agilent ADS 2003A, Agilent Eesof EDA, Palo Alto, CA.

[6] Matlab, Version 6.5 Release 13, The Mathworks, Inc., Natick, MA.

[7] Integrated Publishing (2004, May 22), "The Tunnel Diode," Available: http://www.tpub.com/neets/book7/26a.htm.

[8] American Microsemiconductor (2004, April 24), "Tunnel Diode and Back Diode Tutorial," Available: http://www.americanmicrosemi.com/tutorials/tunneldiode.htm.

[9] G. Rotsky (2003, August 30), "Tunnel diodes: the transistor killers," *EETimes Online*. Available: http://www.eetimes.com/special/special_issues/millenium/milestones/holonyak.html.

[10] Hewlett Packard, "Pulse and Waveform Generation with Step Recovery Diodes," Application Note 918, October, 1984.

[11] J. S. Lee, C. Nguyen, and T. Scullion, "New uniplanar subnanosecond monocycle pulse generator and transformer for time-domain microwave applications," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 49, No. 6, pp. 1126-1129, June 2001.

[12] The Madscientist Company (2003, October 2), "Microwave Theory," Available: http://www.madscientist.com/html/Theory.html.

[13] J. Ibrahim, "Notes on Ultra Wideband Receiver Design," April 14, 2004.

[14] L. W. Couch II, *Digital and Analog Communication Systems*, 6th Edition, New Jersey: Prentice Hall, 2001.

[15] M. Z. Win and R. A. Scholtz, "Impulse radio: how it works," *IEEE Communications Letters*, Vol. 2, No. 1, pp. 10-12, January 1998.

[16] J. R. Foerster, "The performance of a direct-sequence spread ultra-wideband system in the presence of multipath, narrowband interference, and multiuser interference," *IEEE Conference on Ultra Wideband Systems and Technologies*, May 2002.

[17] C. R. Anderson, A. M. Orndorff, R. M. Buehrer, and J. H. Reed, "An Introduction and Overview of an Impulse-Radio Ultrawideband Communication System Design," tech. rep., MPRG, Virginia Polytechnic Institute and State University, June 2004.

[18] J. Han and C. Nguyen, "A new ultra-wideband, ultra-short monocycle pulse generator with reduced ringing," *IEEE Microwave and Wireless Components Letters*, Vol. 12, No. 6, pp. 206-208, June 2002.

[19] S. Licul, J. A. N. Noronha, W. A. Davis, D. G. Sweeney, C. R. Anderson, T. M. Bielawa, "A parametric study of time-domain characteristics of possible UWB antenna architectures," submitted to *IEEE Vehicular Technology Conference*, February 2003.

[20] International Telephone and Telegraph Corporation, *Reference Data for Radio Engineers*, 5th Edition, New York: International Telephone and Telegraph Corporation, 1968.

[21] AppCAD for Windows, Version 3.0.2, Agilent Technologies, Santa Clara, CA.

[22] E. Bogatin, *Signal Integrity - Simplified*, 1st Edition, New Jersey: Prentice Hall PRT, 2004.

[23] Xilinx System Generator for DSP, Version 6.1, Xilinx, San Jose, CA.

[24] M. I. Skolnik, Introduction to Radar Systems, 3rd Edition. New York: McGraw-Hill, 2001.

Appendix A UWB Transmitter Schematic and PCB Layout

In Appendix A, the schematic and PCB layout of the UWB transmitter are illustrated to detail all of the necessary components, including the biasing circuits, DC power supply, and bypass capacitors. Page 1 of the schematic shown in Figure A.1, includes the input clock and data waveforms using SMA connectors, data selects for on-board chips using header pin connectors, PECL terminating resistors, and other important ICs. To boost the signal into the SRD, the ERA-4SM amplifier is displayed in Figure A.2 along with input and output attenuators. The SRD pulse generator circuits are shown in Figure A.3, while the paths for the positive and negative pulses are located in Figure A.4, which includes RF switches, amplifiers, and attenuators. Figure A.5 of the schematic begins with the power combiner and contains a low pass filter, amplifier, and the output SMA connector. The DC power supply is illustrated in Figure A.6 and the bypass capacitors for each IC are found in Figure A.7. The PCB layout begins with the top layer of the circuit board containing the RF components, which can be seen in Figure A.8. Finally, the DC power supply is shown in Figure A.9 on the bottom layer.

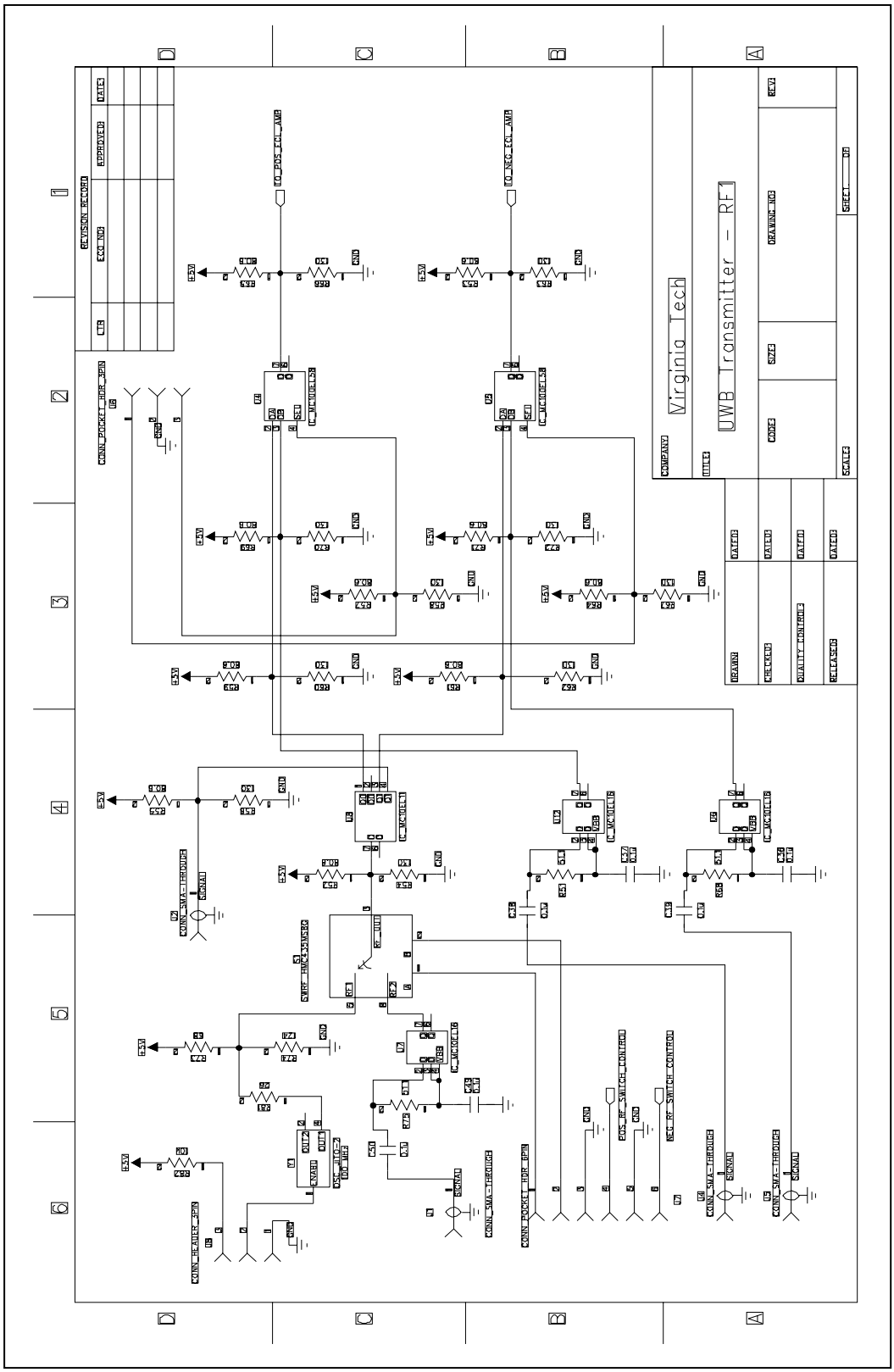


Figure A.1. UWB Transmitter Schematic of Input

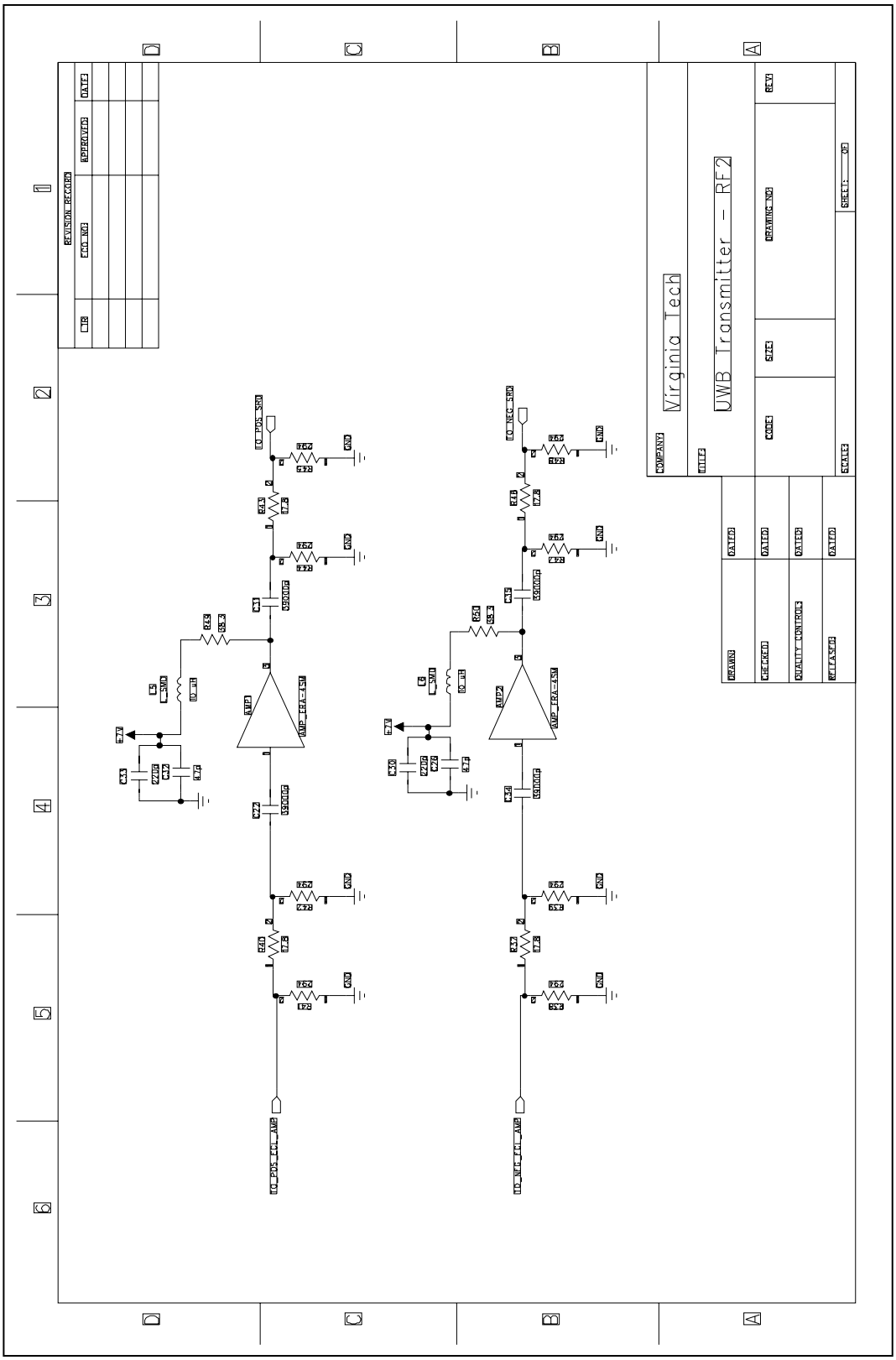


Figure A.2. UWB Transmitter Schematic of RF Components Prior to each SRD Pulse Generator

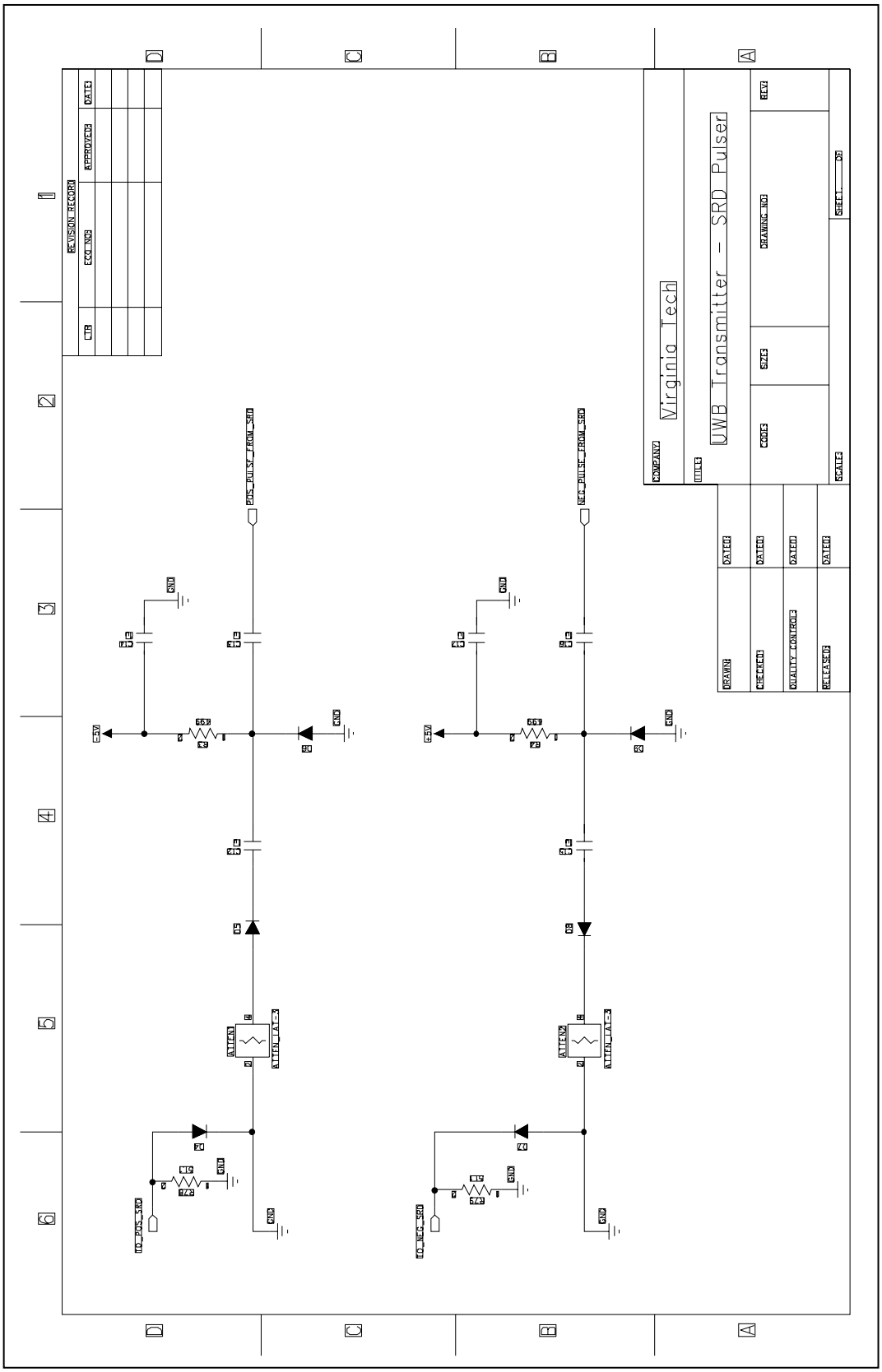


Figure A.3. UWB Transmitter Schematic of each SRD Pulse Generator

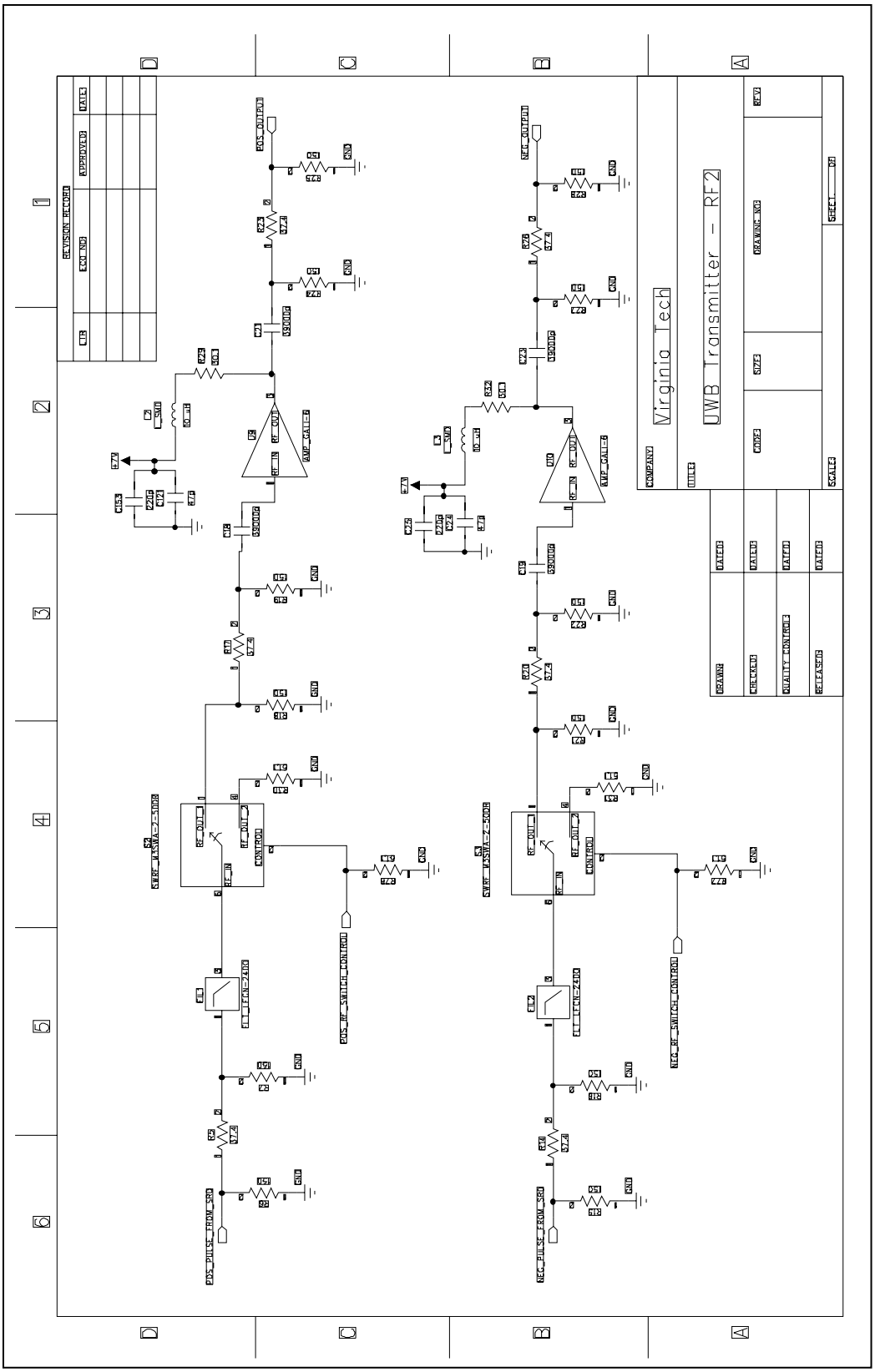


Figure A.4. UWB Transmitter Schematic of RF Components Following each SRD Pulse Generator

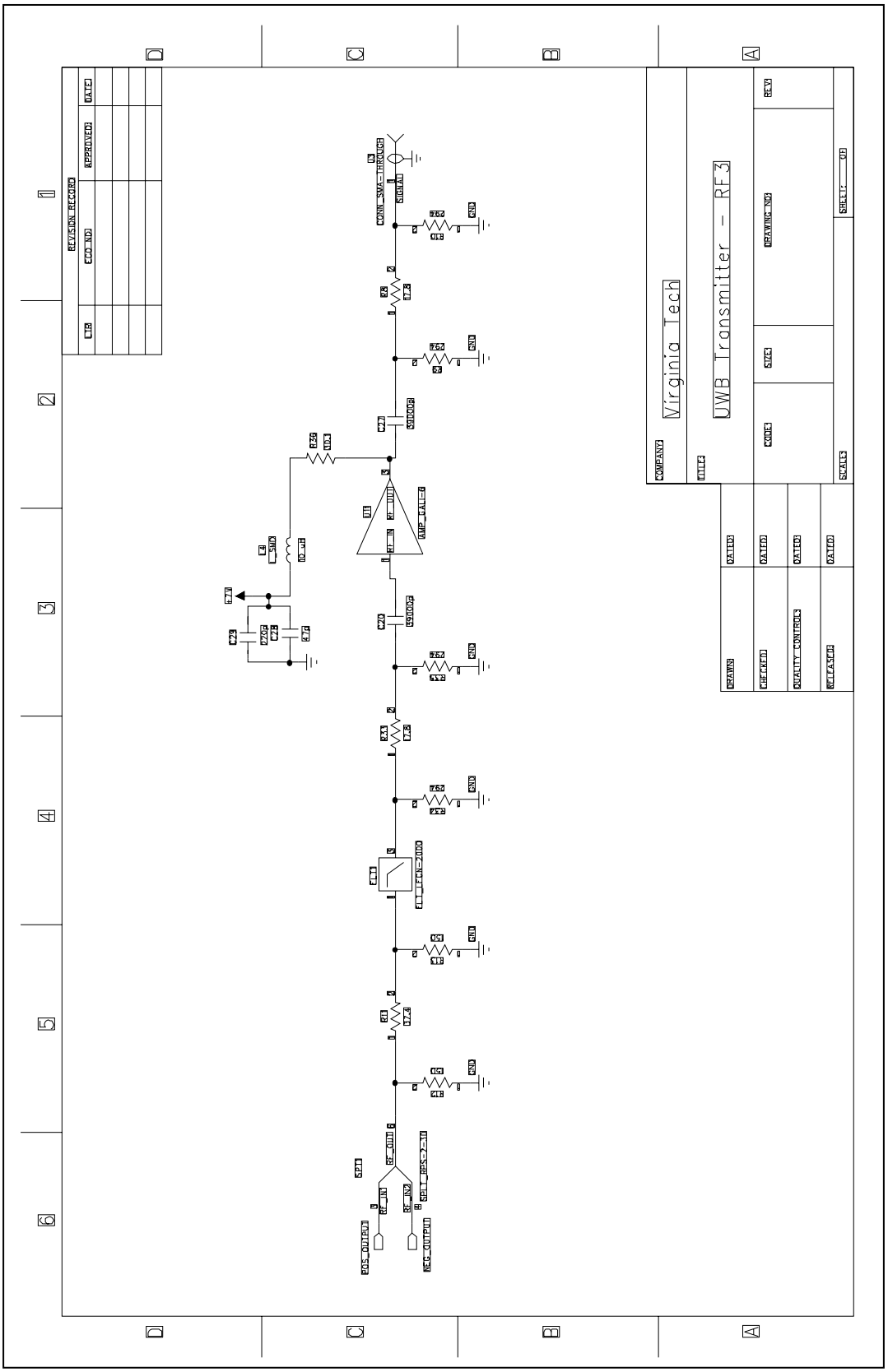


Figure A.5. UWB Transmitter Schematic of Output

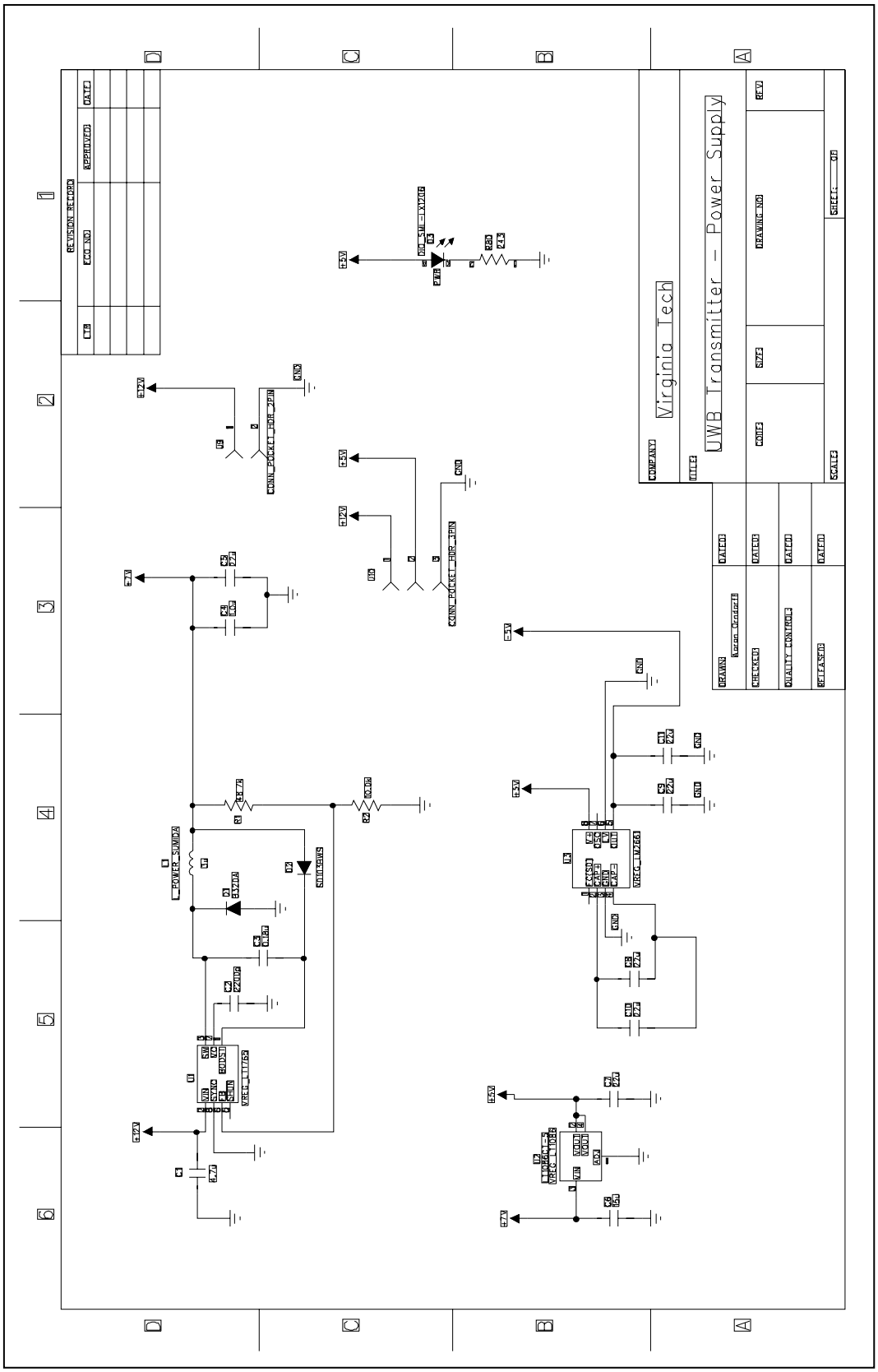


Figure A.6. UWB Transmitter Schematic of DC Power Supply

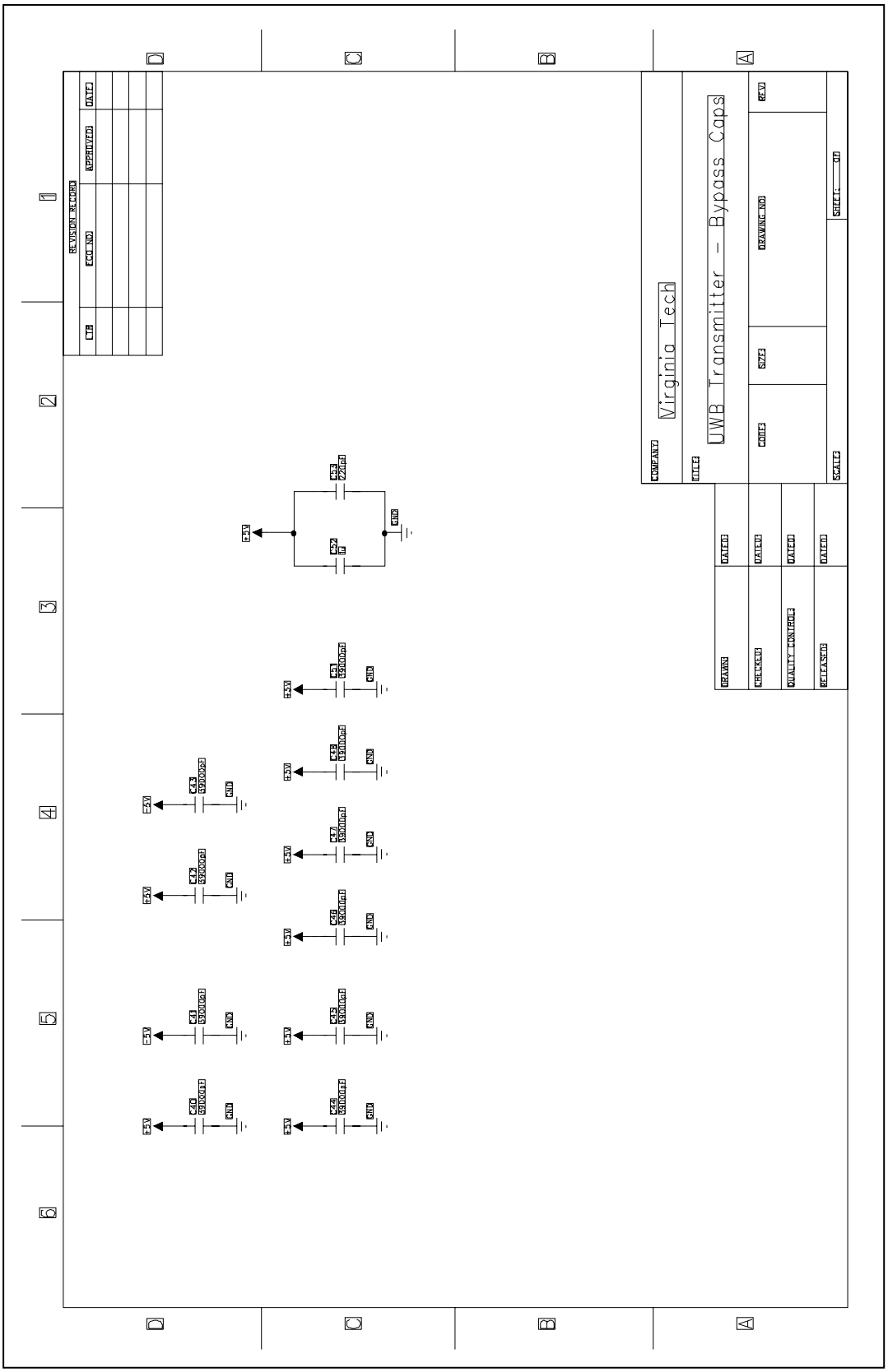


Figure A.7. UWB Transmitter Schematic of Bypass Capacitors

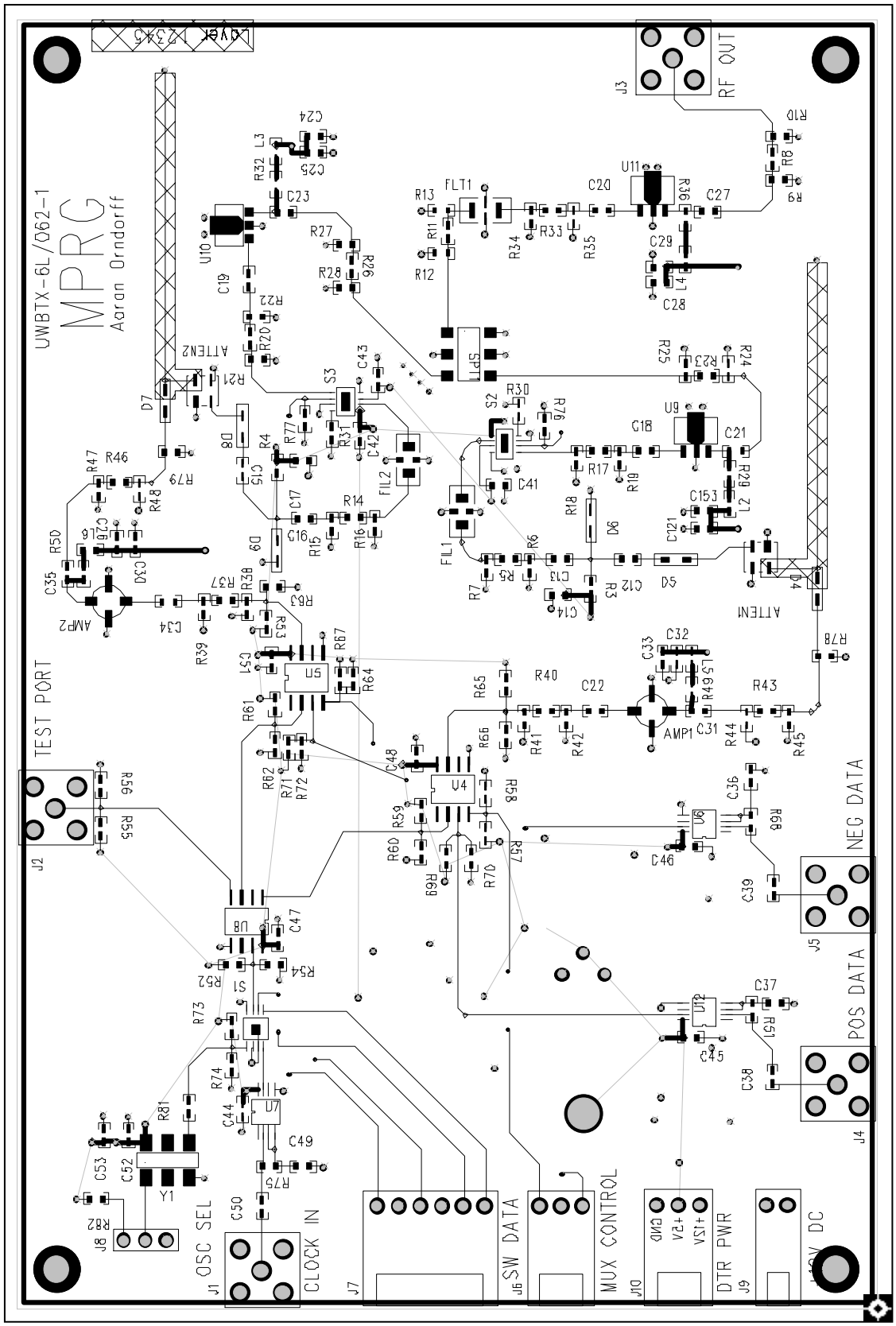


Figure A.8. UWB Transmitter PCB Layout for Top Layer

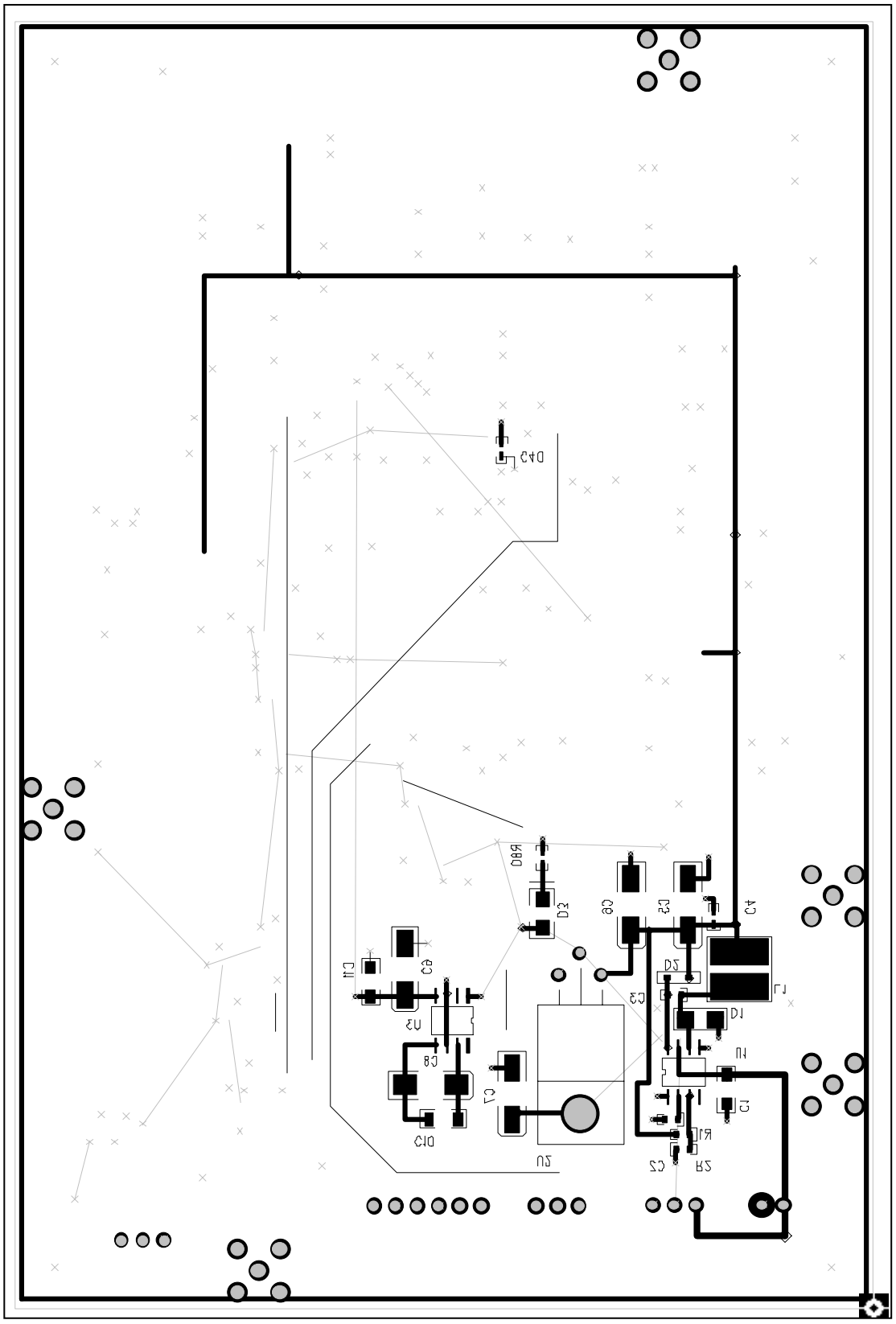


Figure A.9. UWB Transmitter PCB Layout for Bottom Layer

Appendix B Schematic and Listing of Code for the System Simulation

B.1 System Simulation Transmitter Schematic

The transmitter schematic for the system simulation, which was described in Chapter 5, is shown in Figure B.1 below. The components themselves are very tough to distinguish, but it was difficult to incorporate the entire schematic due to its size. The file for this simulation schematic can be found on the MPRG web at \U5\aorndorf\ADS Schematics.

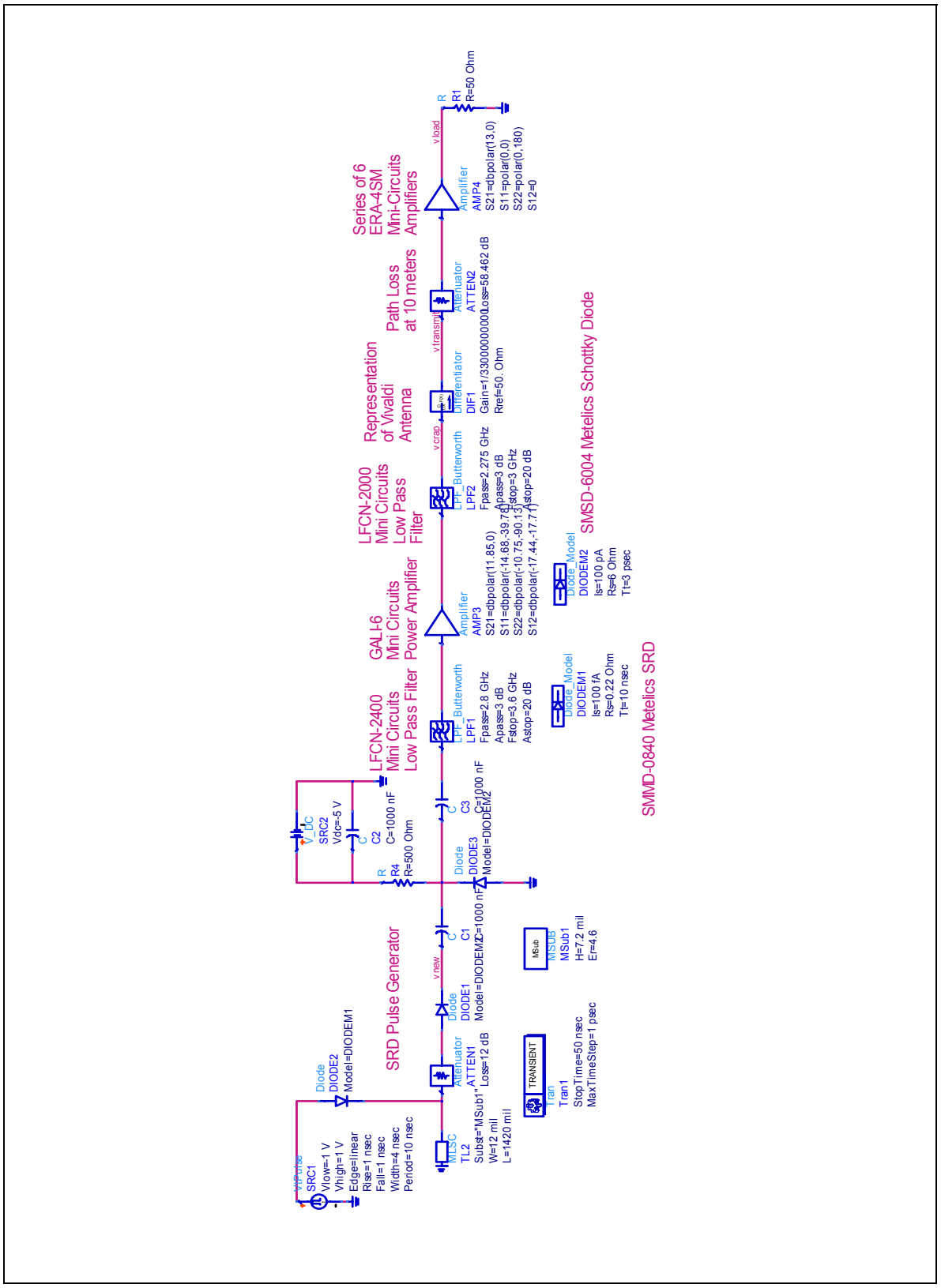


Figure B.1. ADS Transmitter Schematic for System Simulation

B.2 Listing of System Simulation M-files

The following is a listing of m-files necessary to run the system simulation in Matlab. This code can be located on the MPRG web at \U5\aorndorf\Matlab Code.

acquisition.m
aperture_delay.m
ber_calc.m
ce_template.m
create_mp_new.m
data_find.m
data_gen.m
data_index_calc.m
energy_calc.m
energy_calc_mp.m
los_mp.m
matched_filter.m
matched_filter_ppm.m
mf_pulse.m
mf_threshold_detect.m
mp_pulse.m
nt_calc.m
place_zero.m
pngen.m
pp_m_seq.m
ppm.m
process_data.m
system_simulation.m
test_frame.m
threshold_detect.m

Vita

Aaron Michael Orndorff, the son of James and Debra Orndorff Jr., was born on May 30, 1980 in Winchester, VA. He graduated from James Wood High School in 1998 and began pursuing his Electrical Engineering degree in the Fall of 1998 at Virginia Tech. While completing undergraduate classes and performing research under Dr. T. S. Rappaport, he wrote an Honors Thesis entitled "Miniaturization of a Sliding Correlator Spread Spectrum Channel Sounder", where a PN sequence clock generator and data processing routines for a digital oscilloscope were designed. After graduating Summa Cum Laude and In Honors in 2002, he enrolled in the Graduate School at Virginia Tech due to interests in furthering his education in the electromagnetic and antenna fields. Although this thesis does not focus on these topics, a developed interest in Ultra-Wideband communication led to this transceiver design project.